REDUCED SWITCH COUNT MULTILEVEL INVERTERS: TOPOLOGIES, PWM SCHEMES AND FAULT TOLERANT OPERATION

Submitted in partial fulfilment of the
requirements for the award of the
degree of

DOCTOR OF PHILOSOPHY

By

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CERTIFICATE

This is to certify that the thesis entitled **"Reduced switch count multilevel inverters: Topologies, PWM schemes and Fault tolerant operation**," which is being submitted by **Hari Priya Vemuganti (Roll No. 714118)**, is a bona fide work submitted to National Institute of Technology, Warangal in partial fulfilment of the requirement for the award of the degree of **Doctor of Philosophy** in Department of Electrical Engineering. To the best of my knowledge, the work incorporated in this thesis has not been submitted elsewhere for the award of any degree.

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DECLARATION

This is to certify that the work presented in the thesis entitled "Reduced switch count multilevel inverters: Topologies, PWM schemes and Fault tolerant operation" is a bona fide work done by me under the supervision of Dr. D. Sreenivasarao and Dr. G. Siva Kumar, Department of Electrical Engineering, National Institute of Technology Warangal, India and was not submitted elsewhere for the award of any degree.

I declare that this written submission represents my ideas in my own words and where others ideas or words have been included; I have adequately cited and referenced the original sources. I also declare that I have adhered to all principles of academic honesty and integrity and have not misrepresented or fabricated or falsified any idea/date/fact/source in my submission. I understand that any violation of the above will be a cause for disciplinary action by the institute and can also evoke penal action from the sources which have thus not been properly cited or from whom proper permission has not been taken when needed.

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(*Hari Priya Vemuganti*)

ABSTRACT

The fast growing energy needs and drastic globalization have increased the requirement of reliable, high efficient and uninterruptible power for various industrial, transport, telecommunication, aerospace, traction, energy storage, residential and domestic applications. Hence, an efficient and controllable power converter is a pre-requisite for meeting the desired specifications at the load end. Conventional controllers such as thyratrons, mercury-arc rectifiers, magnetic amplifiers and rheostat controllers possess various limitations in terms of size, cost, complexity, maintenance, reliability, efficiency, safety and robustness. The advent of self-commutating devices, the era of power converters have changed enormously. Among, ac-dc (rectifiers) and dc-ac (inverters) converters plays a significant role in most of the applications.

AC-DC power conversion can be broadly categorised into voltage source (VSI) and current source inverters (CSI). However, one may prefer CSI due to its robustness or the VSI due to its high efficiency, low initial cost, and smaller physical size. Among these, VSI based power converters has been considered in the present work as they have higher market penetration and noticeable development in last two decades. The poor harmonic performance, high device ratings and requirement of input and output filters makes the two-level VSI impractical for direct use in high-power, medium-voltage applications. Thus, to realize VSI for high-power applications, multipulse and multilevel inverters (MLI) are the two popular solutions reported in literature. The first one requires phase-shifting transformers which increases the converter size, cost and complexity. However, the later one does not involve any phase-shifting transformers and can be directly incorporated for high-power medium-voltage applications with matured medium power electronic devices. Owing to this, MLIs have gathered much attention in industry and academia as one of the preferred choice for high-power applications and successfully made their way into the industry.

MLIs are proven as a matured technology for various commercialized and customized products for a wide power range of applications such as traction, compressors, extruders, pumps, fans, grinding mills, rolling mills, conveyors, crushers, blast furnace blowers, gas turbine starters, mixers, mine hoists, electric vehicles, reactive power compensators, renewable energy generation, custom power devices, marine propulsion, high-voltage direct-current (HVDC) transmission. Among the topologies of MLIs, diode clamped (DCMLI), flying capacitor (FCMLI), and cascade H-bridge (CHB) are widely popular and termed as classical MLIs. These topologies gathered a great attention both from academia and industry. Their practical implementation is heavily influenced by the application, control complexity and cost.

The requirement of large number of power components and voltage unbalance problem at higher levels limits the DCMLI for low power rating applications. The requirement of large number of capacitors and their pre-charge requirement limits FCMLI to high bandwidth applications such as traction drives.

The modular structure and high fault tolerance ability makes CHB best suited for high-voltage medium-power applications (13.8 kV, 30 MVA). However, CHB requires isolated dc sources for active power transfer applications. As similar to DCMLI and FCMLI, switch count of CHB increases with number of levels in phase-voltage. In addition, topologies of classical MLIs present great deal of challenge in implementation to higher levels. This is due to its increased device count at higher levels, which complicates its circuit configuration and imparts size, cost and maintenance limitations. Hence, researchers continued to explore and evolve newer topologies by making more or less changes on the classical MLIs. CHB with unequal dc link voltages or hybrid combination with DCMLI can increase the number of levels with significant reduction in switch count. However, unequal blocking voltages of switching devices and limited switching redundancies of these topologies cause uneven utilization of dc sources.

The increased component count of power semiconductor devices and capacitor/dc sources of classical MLI topologies has provoked the researchers to contribute further to evolve newer topologies with reduction in size and cost. Thus, MLI with reduced device count originated and this domain of MLIs are called as reduced switch count (RSC) MLIs. From the past decade, various enthusiasts carried out extreme research on RSC-MLIs and developed numerous topologies with significant reduction in component count, total blocking voltage, cost and ease of control. Several RSC-MLI topologies such as multilevel dc link (MLDCL), packed U-cell (PUC), cascaded bi-polar switched cells (CBSC), reverse voltage (RV), switched dc sources (SDS), basic unit MLI, envelope-type (E-type), T-type, hybrid T-type, series-connected switched sources (SCSS), switched series parallel sources (SSPS), nested MLI, switched capacitor unit, reduced cascaded and various other three-phase and cascaded topologies are reported in literature.

In this connection, qualitative and quantitative features of RSC-MLI topologies have discussed in this thesis and, a comparison has made to facilitate a well-informed selection of topology for a given application. For this, a comprehensive comparison between various RSC-MLI topologies is presented in terms of performance parameters such as device count, device ratings, blocking voltages, requirement of bi-directional switches, nature of dc link, modularity, fault tolerant ability, switching and conduction losses, power distribution and utilization of dc link voltages. Considering the above factors, RSC-MLIs are categorized into symmetrical and asymmetrical configurations, topologies with separate level and polarity generator, generalized

and unit-based configurations, H-bridge and hexagonal switch cell (HSC) structures, topologies with uni-directional and bi-directional switches, topologies with isolated/floating dc sources and topologies with series/parallel operation of dc sources.

The reduction in switch count, even power sharing among dc voltage sources and adequate switching redundancies are the paramount criteria for the selection of inverter topology. Among these, MLDCL possess simplified and modular structure with appreciable reduction in switch count, multiple switching redundancies, symmetric and simplified switching operation, fault tolerant ability, even power distribution, equal device blocking voltages and dc link voltage balancing ability. Owing to these key and worthy benefits, this topology had gathered more attention and further served as a viable alternative for CHB in applications such as grid-connected photo-voltaic system, uninterrupted power supplies (UPS), custom power devices (CPD), adjustable speed drives (ASD), battery energy storage systems (BESS), active front-end (AFE) applications and electric vehicles (EV).

The significant reduction in switch count of RSC-MLI topologies has simplified their circuit configuration such that, each switch may involve in attaining more than one voltage level. Asymmetrical RSC-MLIs further reduced the switch count and made the topologies much simpler. However, significant reduction in switch count have reduced the redundancies and modified the switching combination such that, devices conducting for obtaining lower voltage level may not remain in conduction at higher levels as well. This acted as a limitation of conventional carrier based pulse width modulation (PWM) schemes such as level-shifted (LSPWM) and phase-shifted (PSPWM) to control these RSC-MLIs.

To control any RSC-MLI, selective harmonic elimination (SHE) and space vector (SV) PWM are often preferred. However, these schemes require elusive calculations and complexity increases at higher number of levels. Hybrid PWM is another popular scheme reported for implementing asymmetrical cascaded configurations such as CHB and SSPS (with an addition of H-Bridge). However, requires estimation of output voltage of the higher voltage bridge/units, to derive the reference signal for lower voltage bridge/units. Switching schemes using low frequency carrier reported for MLDCL, CBSC, basic unit RSC-MLI, T-type and Hybrid T-type topologies are easy to realize but, produces lower order harmonics. On the other hand, among the carrier based PWM schemes, multi reference, reduced carrier and hybrid switching function are widely popular. Multi reference modulation results high THD in line-voltage and requires multiple dc off shifted references which increases the complexity in closed loop-applications. Hybrid switching function PWM results in satisfactory THD but requires numerous comparators at higher levels, which increases computational burden. Reduced carrier PWM

scheme with logical expressions are the simplest. However, these logical expressions are not generalized and vary with topology and number of levels.

Therefore, to overcome the limitations of conventional PWM schemes of RSC-MLI, modified carrier and modulating signal arrangements are proposed in this thesis. The performance of the modified PWM schemes with the proposed carrier arrangement is evaluated on five-level inverter topologies and its superior THD performance over the conventional schemes is validated. Further, a simple carrier based PWM scheme with unified logical expressions is proposed. The proposed logical expression remains valid to control any RSC-MLI, irrespective to the voltage ratios and topological arrangement and produces good THD performance with less computation burden.

To validate the ability of the proposed switching logic, the PWM scheme is implemented in MATLAB/Simulink environment for thirteen-level asymmetrical RSC-MLI configurations such as MLDCL, SDS, Cascaded T-type, Improved T-type and E-type. The simulation results are validated experimentally by developing various topologies of RSC-MLIs by interconnecting two inverter modules with 24 isolated IGBTs on each. The PWM scheme is implemented on dSPACE MicroLabBox R&D controller. Further to validate the superiority of the proposed PWM scheme, its performance in-terms of computation burden and line-voltage THD is compared with the state-of-the-art PWM schemes reported in the literature.

Another aspect for selection of inverter is its reliability. The ability of an inverter to work under fault conditions plays a vital in ensuring the safety and uninterrupted operation of the overall system. There are several reasons for occurrence of fault in inverters, and every fault will ends up with either open-circuit (OC) or short-circuit (SC) of a particular switch or associated unit/bridge. SC fault results in dangerously high current and cause a possible damage to the inverter. To avoid these faults, a fast acting over-current protection circuits are required to by-pass the faulty phase-leg or inverter. On the other hand, OC faults are not severe and can be compensable. Hence, this thesis analyses the affects and compensation of OC faults.

The reduction in switch count of RSC-MLI has reduced the probability of fault occurrence as compared to MLI. However, the extreme reduction in switching redundancies restricted their fault tolerant ability. In literature, SVM and carrier based schemes are reported for compensating single switch fault in RSC-MLI such as T-type. Among these, SVM is an attractive scheme which can achieve fault tolerant operation (FTO) by creating switching redundancies. Nevertheless, its complex implementation acts as a limitation at higher level. In general, the fault tolerant schemes (FTS) generates a new set of modulating signals to reconfigure the inverter to achieve FTO. This FTO is feasible for modular and redundant topologies such as MLDCL.

By-passing method is one of the most feasible FTS to restore balanced operation. However, this method of fault compensation derates the inverter as the healthy units are by-passed. To obtain FTO without derating the inverter, the burden of faulty units of one phase is shared across the healthy units of same phase such that its overall phase-voltage is equal to pre-fault voltage. This method results in non-uniform burdening of healthy units, which effects their dc link voltages and power distribution among operating units. To obtain balanced operation with equal power distribution among the healthy units, neutral shifting (NS) FTS is reported. This scheme modifies the magnitude and angle between phase-voltages such that the inverter produce balanced line-voltages with uniform burden on all healthy units. NS involves manual calculation of modified phase-angles to ensure magnitude and angle balance among line-voltages. This method can compensate multiple switch faults, only if the number of faulty units in any two phases are same. Another approach to achieve NS is to inject a zero-sequence voltage to shift the neutral point of the inverter. The magnitude of injected zero-sequence voltage depends on the number of faulty units. In literature, this method is reported on CHB for compensating single switch fault (per phase), and is not reported for compensating multiple OC faults. Moreover, this scheme is not directly applicable for tolerating OC faults on RSC-MLIs.

Therefore in this thesis, a generalized NS zero-sequence injection FTS is proposed for compensating multiple OC switch faults on MLDCL inverter. Generalised equations are proposed to determine the magnitude of injected zero-sequence voltage and fault tolerant modulating signals, for any fault case. The proposed generalized fault tolerant modulating signals are operated with carrier rotation based reduced carrier PWM scheme to obtain balanced set of line-voltages with uniform power distribution among all the operating units. To investigate the ability of the proposed generalized FTS, simulation study on three-phase fifteen-level MLDCL inverter is performed. The inverter is controlled with the proposed modified reduced carrier PWM scheme and to achieve uniform burden among healthy operating units, the carriers are rotated at the end of each carrier time period. After the initiation of FTO, the balanced operation of the inverter is observed from their line-voltage and current waveforms and their respective RMS values. In addition, power delivered by each unit ensures the uniform performance (power distribution) among all the operating units. To corroborate the simulation results, a nine-level three-phase IGBT based MLDCL inverter is developed and controlled, using OPAL-RT 4500. However, performance of proposed FTS is validated assuming stiff sources in the dc link and the effect of charging and discharging currents on dc link voltages during fault compensation is excluded.

Therefore, to investigate the efficacy of proposed FTS in closed-loop application, an active rectifiers is considered. Multilevel converter (MLC) based active rectifiers gained more

prominence for high-power applications such as UPS, grid-connected applications, BESS, battery chargers and ASD. Owing to challenges such as voltage balance of dc link capacitors, even power sharing and fault tolerant operation, the implementation of RSC-MLI topologies as an active rectifiers is not yet reported.

In literature, various voltage and current control techniques are reported for three-phase regenerative active rectifiers. Among these, direct power control (DPC) and voltage oriented control (VOC) are commonly used control schemes. DPC produces fast and accurate response, and involves either hysteresis, predictive or adaptive controllers, followed by PWM or look-up tables. Practice of predictive or adaptive controllers increases the difficulty in realizing DPC for MLCs/RSC-MLCs based active rectifiers. On the other hand, VOC is simple and more robust, and can be easily implemented for MLCs and RSC-MLCs. The objective behind VOC is to regulate the dc link voltages, irrespective to the load variations. On the other hand, to regulate the power delivered by the converter, irrespective to the load conditions, grid active reactive power control (GARPC) is reported. This method senses and controls the dc link voltage such that a rated power with unity power factor is delivered to the converter for any load condition. GARPC is also known as instantaneous active and reactive power control.

The above control algorithms can be effective only if the converter is able to provide an appropriate path for charging and discharging of dc link capacitors. If the converter operation is faulty, then its operation is restricted and results dc link voltage unbalance. As the design and control of RSC-MLC based active rectifier for healthy and faulty operation of the converter is not yet reported, and therefore an attempt is made in this thesis.

In this thesis, a three-phase, 1 MVA, 3.3 kV, fifteen-level MLDCL based active rectifier is proposed with a comprehensive control scheme. In this scheme, the control objective are achieved by involving modified reduced carrier rotation PWM and proposed fault tolerant scheme with VOC or GARPC algorithms. The pre and post-fault performance of considered MLDCL based active rectifier for dynamic variation in load, change in set-point references and regeneration operation is demonstrated in MATLAB/Simulink environment for VOC and GARPC algorithms under various fault conditions. Further, the efficacy of the proposed scheme in balancing converter dc link voltages, even power distribution of dc sources, and fault tolerant ability is demonstrated on OPAL-RT 4500 real-time controller.

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LIST OF ACRONYMS

RSC-MLI	Reduced Switch Count Multilevel Inverter
CSI	Current Source Inverter
VSI	Voltage Source Inverter
VSR	Voltage Source Rectifier
ac, AC	Alternating Current
dc, DC	Direct Current
DCMLI	Diode Clamped Multilevel Inverter
CHB	Cascade H-bridge
FCMLI	Flying Capacitor Multilevel Inverter
AFC	Active Front-end Converter
ASD	Adjustable Speed Drive
HEV	Hybrid Electric Vehicle
THD	Total Harmonic Distortion
pf, PF	Power Factor
IGBT	Insulated Gate Bipolar Transistor
PWM	Pulsewidth Modulation
LSPWM	Level-shifted Pulsewidth Modulation
PSPWM	Phase-shifted Pulsewidth Modulation
PI	Proportional and Integral
rms, RMS	Root Mean Square
RSC	Reduced Switch Count
MLDCL	Multilevel dc-link (RSC-MLI topology)
SDS	Switched dc-sources (RSC-MLI topology)
CBSC	Cascaded Bi-polar Switched Cell (RSC-MLI topology)
MLM	Multilevel Module (RSC-MLI topology)
E-type	Envelope Type (RSC-MLI topology)
DPC	Direct Power Control
VOC	Voltage Oriented Control
GARPC	Grid Active Reactive Power Control
FTS	Fault Tolerant Scheme
FTO	Fault Tolerant Operation
NS	Neutral Shifting
OC, oc	Open-Circuit
SC, sc	Short-Circuit

LIST OF SYMBOLS

n	Number of dc voltage sources per phase
m	Number of levels in phase-voltage of inverter
f_{cr}	Carrier signal frequency
f_m	Modulating signal frequency
m_a	Amplitude modulation index
m_f	Frequency modulation index
x	Number of OC switch faults in phase-a
y	Number of OC switch faults in phase-b
z	Number of OC switch faults in phase-c
v_{sabc}	Three-phase supply voltages
i_{sabc}	Three-phase source currents
V_m	Peak value of modulating signal
V_c	Peak value of carrier signal
v_a'', v_b'' and v_c''	Post-fault phase-voltages
v_a', v_b' and v_c'	Burdened balanced Phase-voltages
$v_{Da,}$ v_{Db} and v_{Dc}	Output signals of decoupled current control block
$v_{Ca,}$ v_{Cb} and v_{Cc}	Output signals of cluster voltage balancing controller
$v_{Ia,}$ v_{Ib} and v_{Ic}	Output signals of Individual voltage balancing controller
$v_{ma,}$ v_{mb} and v_{mc}	Normalized modulating signals
v_{ma}*, v_{mb}* and v_{mc}*	fault tolerant modulating signals
v_{dc}	Mean dc link voltage of all capacitors
P*	Reference power (total active power demand) in GARPC
V*	Reference voltage (voltage of each dc-link) in VOC
v_{dca}1.3...7; v_{dcb}1.3..7 ; v_{dcc}1..3..7;	Instantaneous voltage of each dc link capacitor
v_{dca} , v_{dcb} and v_{dcc}	Mean voltage of each cluster

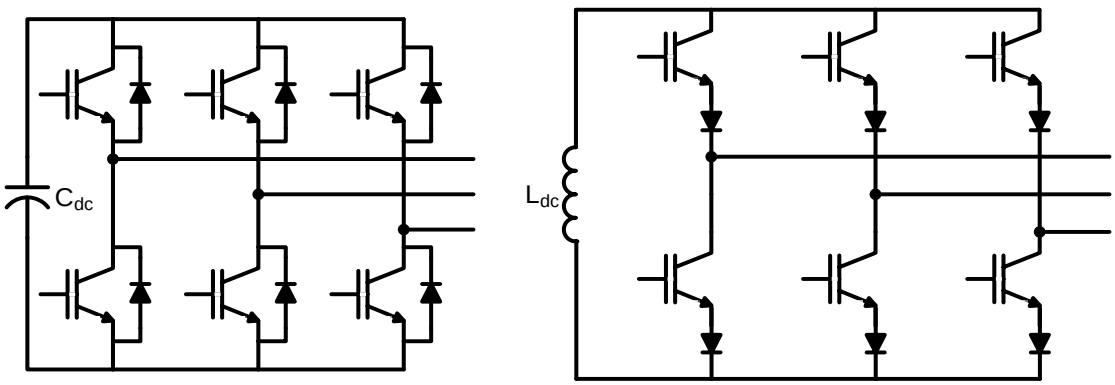
CHAPTER 1: HIGH POWER DC-AC CONVERTERS

This chapter presents literature survey on dc-ac power converters for high-power medium-voltage applications. It starts with brief background on dc-ac power converters and then discusses the prominence of multilevel inverters (*MLIs*). *Further, investigates the limitations of classical topologies of MLIs and then demonstrates the significance of reduced switch count (RSC) MLIs. Next, scope of the work, contributions and thesis outlines are explained.*

1.1 Introduction

DC to AC static power conversion (inverter) plays a vital role in generation, transmission, distribution and utilization of electric power. High-performance and cost-effective inverter is a prerequisite for realization of power electronic applications such as adjustable speed drives (ASD), uninterruptible power supplies (UPS), high-voltage dc (HVDC) transmission, flexible ac transmission system (FACTS), custom power devices (CPD), active frond end converters (AFC), battery energy storage systems (BESS), renewable energy generation (REG) and electric vehicles (EV). In early days, static power converters are realized with forced commutating switches such as thyristors. However, with the advent of semiconductor devices and remarkable progress of gate commutated semiconductor devices, attention has been focused on power electronic inverters with self-commutating devices.

Depending on the dc link energy storage component, the inverters fall under either voltage source inverters (VSIs) or current source inverters (CSIs) [1-3]. The voltage source approach shown in Fig. 1.1(a) uses a capacitor with a regulated dc voltage, while the CSI, shown in Fig. 1.1(b) uses a reactor supplied with a regulated dc current. A critical comparison of VSI and CSI is beyond the scope of this thesis. However, one may prefer CSI due to its robustness or the VSI due to its high efficiency, low initial cost, and smaller physical size [4, 5]. Since VSI technology is widely used in industrial applications, this has also been more common in applications such as FACTS, CPD, ASD and REG [1] and hence, VSI has been considered in this thesis.



(a) Voltage source inverter (b) Current source inverter

Fig. 1.1: Topologies of inverters.

The well-known two-level VSI is also applicable for medium and high-power applications [6]. To cater the required voltage and current level of the inverter, several semiconductor switches are connected in series and parallel respectively. Thus, an inverter leg is comprised of two groups of active switches, each consisting of two or more switches in series/parallel, depending on the ratings of dc link voltage, load current and available switching devices. In addition to this, multiple capacitors in series could be necessary to achieve the desired voltage in dc link [6]. The circuit of high-power two-level VSI is shown in Fig. 1.2. In this circuit, each switch is comprised of three semiconductor devices connected in series and controlled with same gate signal.

The output voltage of this inverter with sinusoidal pulsewidth modulation technique (SPWM) is shown in Fig. 1.3(a) for 1 kHz carrier signal frequency. The harmonic spectrum of the output voltage is shown in Fig. 1.3(b). The output voltage is of quasi-square nature with a total harmonic distortion (THD) of 75.26%. The high harmonic content of the output voltage and increased number of switching devices makes this simple inverter impractical for direct use in high-power applications [6, 7].

Instead of using filters to improve the output voltage waveform of the basic two-level VSI, various solutions are reported in the literature [6, 7]. Among them, multipulse and multilevel inverters (MLIs) are the most popular. These inverter configurations produce good THD performance and are directly applicable for high-power medium-voltage applications with matured medium-power semiconductor devices [6, 7]. Operating principle, merits and limitations of these high-power VSI configurations are explained below.

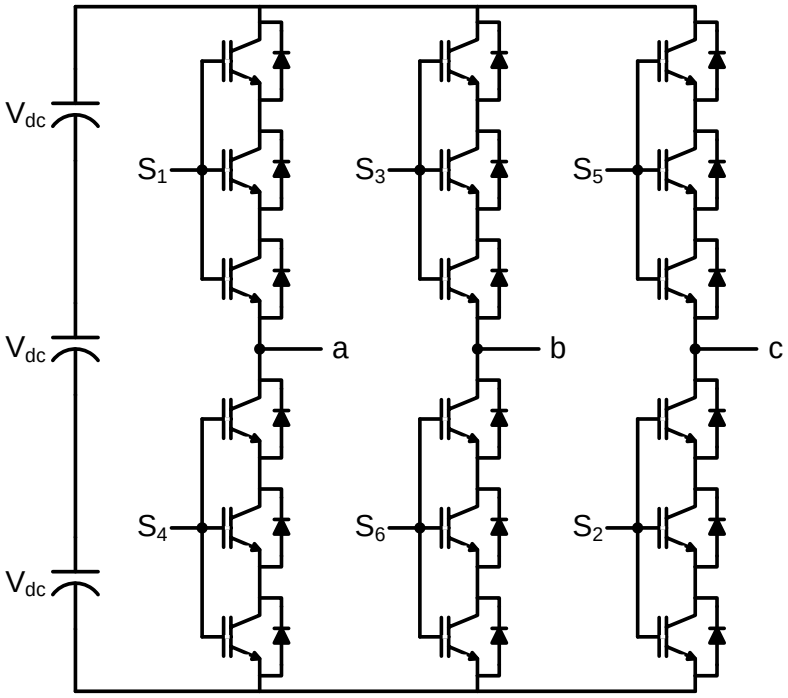
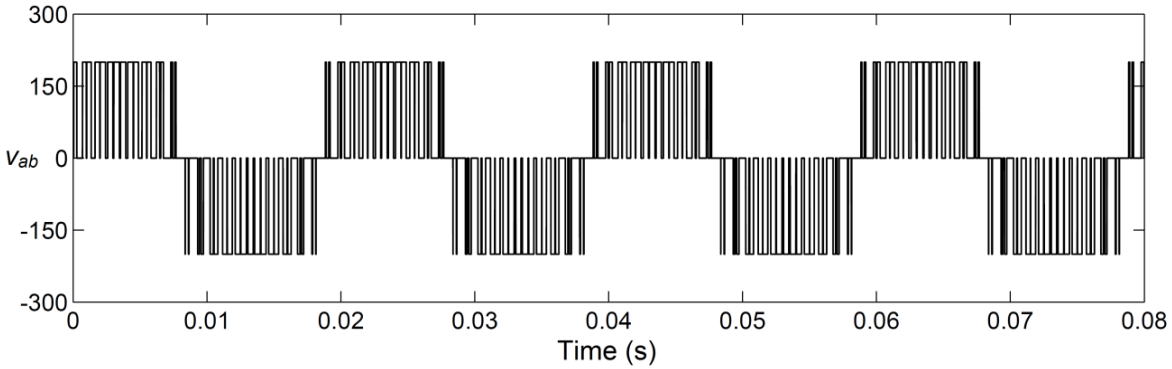
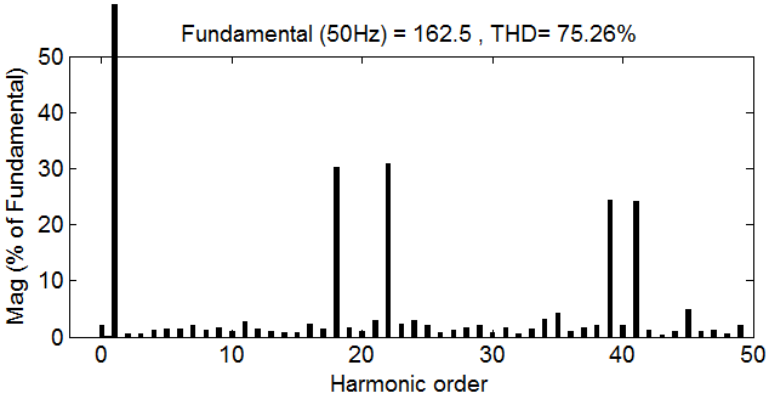


Fig. 1.2: Two-level high-power VSI.



(a) Line-voltage (V)



(b) Harmonic spectrum

Fig. 1.3: Performance of two-level VSI.

1.2 Inverters for high-power medium-voltage applications

The different topologies of VSI for high-power medium-voltage applications can be broadly categorized into two groups: multipulse and multilevel inverters (MLIs) [6-11]. These inverters present great advantages in comparison with conventional two-level VSI [11]. These advantages primarily deal with improvement in output signal quality and increase in power rating of the inverter.

1.2.1 Multipulse inverters

Multipulse inverters involve interconnection of multiple two-level inverters such that the harmonics generated from one inverter are cancelled by harmonics produced by other inverter. In multipulse inverters, several three-phase two-level (six-pulse) inverter units are interconnected as shown in Fig. 1.4, using transformers as magnetic interfaces for achieving high-power rating and harmonic neutralization [3, 9, 12, 13]. Higher the number of inverter units, lower is the distortion of resultant output voltage. For instance, eight six-pulse inverter units can be combined by means of magnetic interfaces (such as zigzag and polygon transformers) to form an equivalent 48-pulse inverter. In this case, the first harmonic order is 47^{th} in the ac voltage and 48^{th} in the dc current [12, 13]. The amplitude of the harmonics decreases as the harmonic order increases. In general, combination of N_P number of six-pulse inverter units gives rise to a $6N_P$ pulse inverter. In this inverter, all harmonic orders except those at $6kN_P \pm 1$ are cancelled in the ac voltage (k is any

integer). The corresponding phase difference between two successive inverter units is given by $360°/6N_P$. For transmission line applications, a pulse number of 24 or higher is required to achieve adequate waveform quality without passive filters [8].

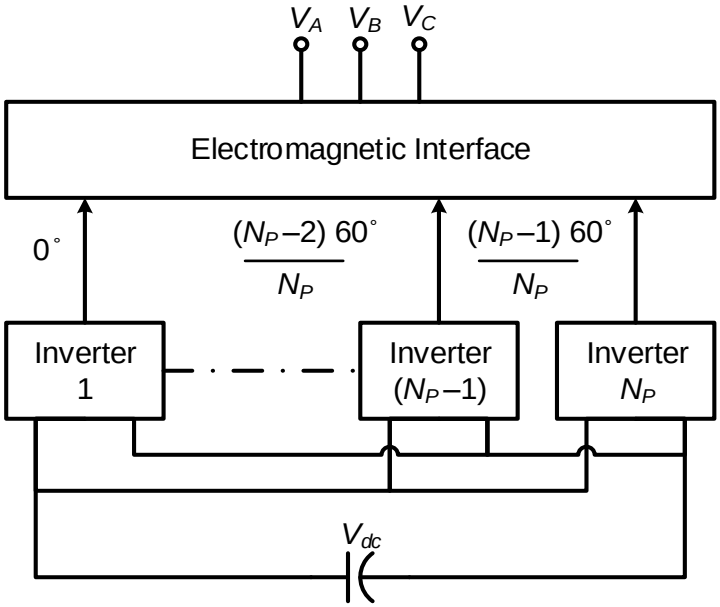


Fig. 1.4: General structure of multipulse inverter.

The main advantages of multipulse inverters are their lower switching losses and reduced input current harmonics. These features are particularly useful in applications with high-voltage and high-power ratings [3, 12]. However, involvement of complex phase-shifting transformers (also called harmonic neutralizing magnetics) acts as major drawback of multipulse inverters and produces the following effects [14]:

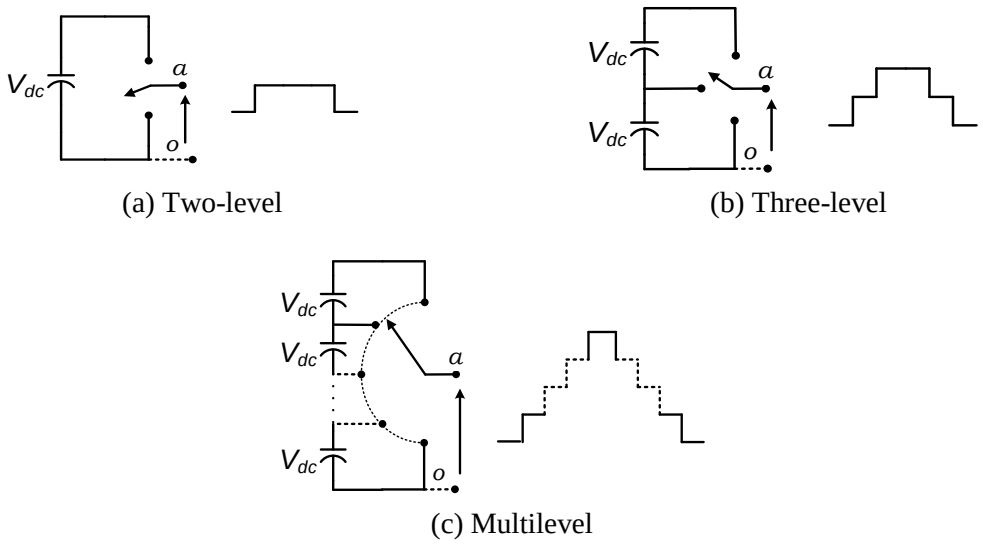
- Most expensive equipment and predominantly influence overall inverter cost.
- Produces about 50% of the total losses of the inverter.
- Occupies up to 40% of the total real estate requirement of the inverter, which is excessively large.
- Difficulty to control due to dc magnetizing and surge overvoltages resulting from saturation of transformers in transient conditions.

Even though, these transformers are less prone to failure (due to the rugged construction) but to overcome the above drawbacks, multilevel inverters (MLIs) are proposed in literature.

1.2.2 Multilevel inverters (MLIs)

Multilevel inverters (MLIs) have become increasingly popular in recent years [6, 10, 11, 15-17]. It uses the concept of aggregating multiple small voltage levels to perform power conversion at an appropriate high-voltage level. The principle behind multilevel voltage generation and advantages offered by MLIs are explained here under.

MLIs utilize several power semiconductor devices and capacitors (or dc voltage sources) to synthesise stepped output voltage waveform. The commutation of these switches permits the addition of capacitor or dc source voltages, and produce higher output voltage (with different number of voltage levels), without increasing the power semiconductor device ratings. The operating principle of MLI to produce multiple levels in output voltage is shown in Fig. 1.5.



(a) Two-level (b) Three-level

(c) Multilevel

Fig. 1.5: Multilevel voltage generation.

Fig. 1.5 shows schematic diagram of an MLI considering one leg. The switching action of power semiconductors is represented by an ideal switch with multiple ports. By operating an ideal switch, Fig. 1.5(a) generates two-level output voltage of either V_{dc} or zero with respect to the negative terminal of the capacitor. Similarly, Fig. 1.5(b) produces output voltage with three-levels and Fig. 1.5(c) generates output voltage with multiple levels. Assuming m is the number of levels in phase-voltage with respect to the negative terminal of the inverter, then the possible number of levels in line-voltage is $2m–1$. Advantages of MLIs include good power quality, good electromagnetic compatibility (EMC), low switching losses, and high-voltage capability [10]. MLIs are considered today as a very attractive solution for high-power medium-voltage applications, because of the following reasons [6, 10, 11, 15-17]:

- Produce output voltages with matured medium-power semiconductor technology with low distortion and low dv/dt.
- Draw input current with very low distortion.
- Can operate with a lower switching frequency.
- Fault tolerant, less prone to failure and their cost is relatively low.
- Generate smaller common-mode (CM) voltage, thus reducing the stress in the motor bearings. In addition, using sophisticated modulation methods, CM voltages can be eliminated.

In contrast, with increase in number of voltage levels, the inverter size, cost and control complexity increases and may introduce voltage unbalance in dc link. However, with the advent of power electronic devices, digital controllers, sensors and modern control techniques, the practice of MLIs has increased tremendously and provoked the researchers to carry out work in the area of MLIs. In this connection, the next section presents an overview of various topologies of MLIs.

1.3 Classical topologies of MLIs

Among the various topologies of MLIs, diode clamped (DCMLI), flying capacitor (FCMLI) and cascade H-bridge (CHB) are the benchmark topologies reported in the literature [6, 7, 10, 15-17]. These three topologies are considered as classical/traditional topologies of MLIs and are predominately incorporated into various industrial applications during last two decades [6, 7, 10, 16]. These topologies are widely accepted both from academia and industry, and enacted as a motivation to incarnate new MLI topologies [16]. Topological configuration, switching operation, features, modulation schemes, applications and other information related to classical topologies is well reported in [6, 7, 10, 15-17] and a brief description is presented below.

1.3.1 Diode clamped multilevel inverter (DCMLI)

The diode clamped multilevel inverter (DCMLI) is reported in [18] and is considered as the first practically succeeded MLI. This employs clamping diodes and multiple non-isolated dc sources to produce ac output voltage with multiple levels [18, 19]. This inverter is configured for both even and odd number of levels in phase-voltage. DCMLI for odd levels in phase-voltage is often reported as neutral-point clamped (NPC) inverter.

A three, four or five-level DCMLI are widely used in various industrial applications such as medium-voltage drives [6, 16, 18, 19]. Fig. 1.6 shows the circuit diagram of five-level DCMLI topology [20]. Although this structure can be extended to higher number of levels, but are less attractive because of higher losses and uneven distribution of power losses in the outer and inner devices [6]. The clamping diodes, which are connected in series to block the higher voltages, introduce higher conduction losses and produce reverse recovery currents during commutation. These currents can affect the switching losses of the other switching devices. Furthermore, at higher levels, charge balance of dc link capacitors turns more complex and complicates its implementation for applications where dc link voltage balance plays a key.

The main drawback of the DCMLI is unequal loss distribution which further leads to uneven distribution of junction temperature and imparts limitations on maximum power rating, output current, and switching frequency of the inverter [16, 21]. This unequal loss distribution can be substantially improved by replacing the clamping diodes with active switches. These active switches, forces the current to flow through upper or lower clamping path. This can be used to

control the distribution of power loss and overcome the limitations of DCMLI, by substantially enabling the inverter for high power rating. These additional devices are called active neutral clamping switches, as shown in Fig. 1.7 and thus, this inverter configuration is named as active neutral point clamped (ANPC) or active diode-clamped multilevel inverter (ADCMLI) [21]. However, the advantages with ANPC come at the expense of more complex circuit and the need to control the additional switching devices.

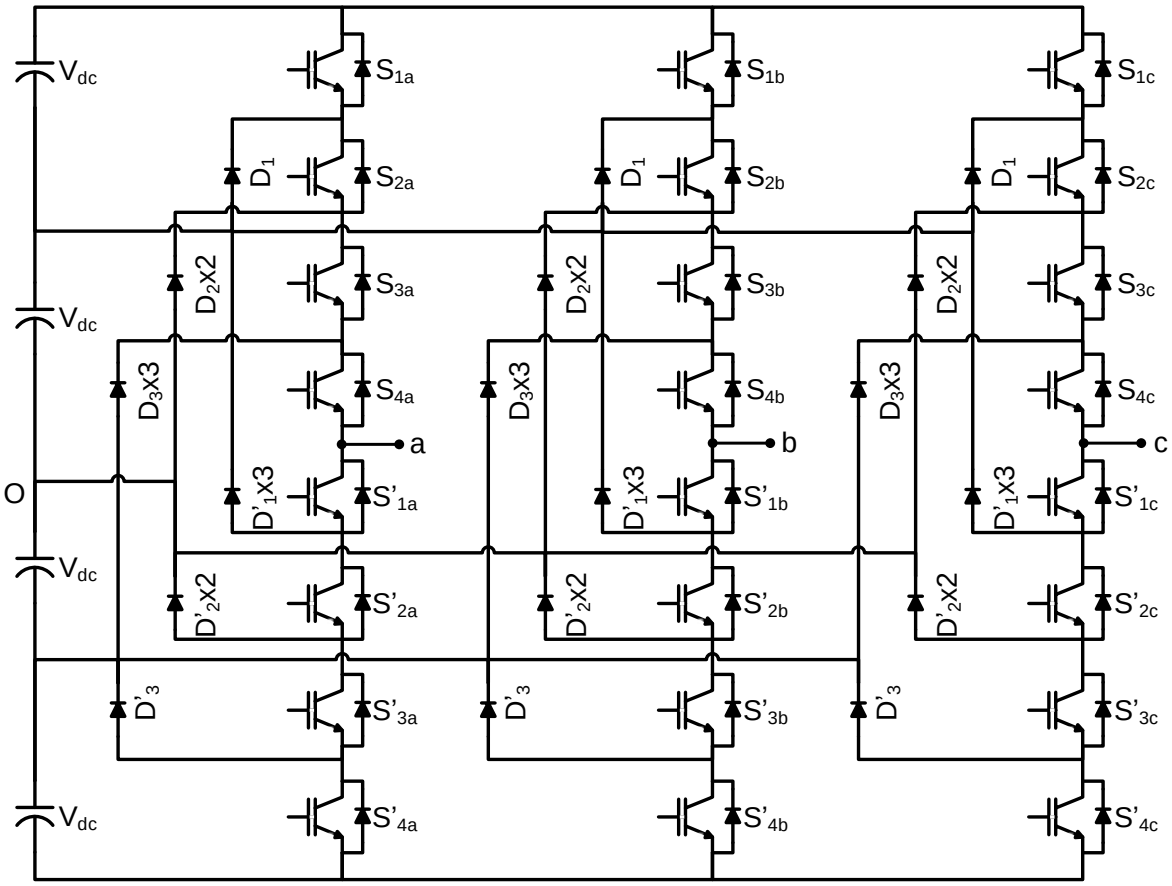


Fig. 1.6: A three-phase five-level DCMLI.

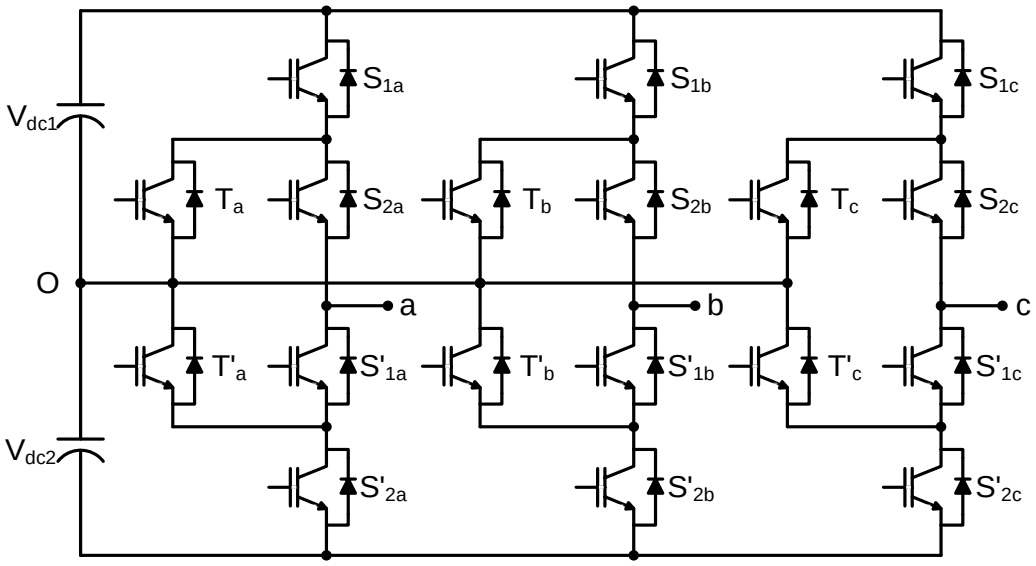


Fig. 1.7: A three-phase three-level active DCMLI.

1.3.2 Flying capacitor multilevel inverter (FCMLI)

Among the classical topologies, flying capacitor is a unique configuration, which involves a series connection of capacitor switching cells [15, 22, 23]. The circuit configuration of a five-level FCMLI is depicted in Fig. 1.8.

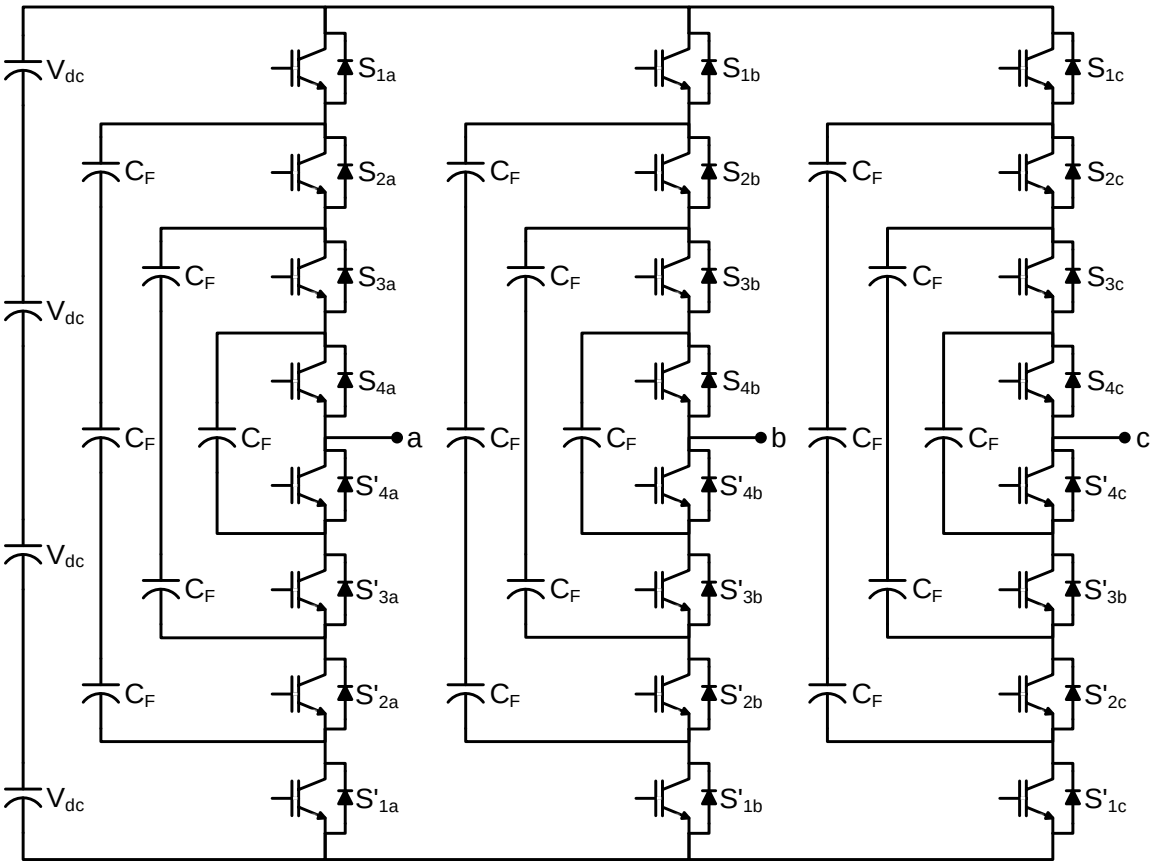


Fig. 1.8: A three-phase five-level FCMLI.

When compared to DCMLI, this topology has several attractive and beneficial features such as absence of clamping diodes, natural balancing of dc link voltages, switching redundancies and uniform power loss distribution. In detail, switching redundancy with in a phase of FCMLI, helps to balance the voltages of the flying capacitors (C_F) and equally distribute the switching and conduction losses of the semiconductor switches [15, 22-25]. Merits and demerits of FCMLI topology are summarized below:

Advantages:

- Modular and scalable topological structure.
- Large number of capacitors provide extra ride through capabilities during power outage [15].
- The switching state redundancy provides a great flexibility for the design of the switching pattern and natural balancing of capacitor voltages [24, 25].
- Reconfiguration of circuit is possible during fault or under-rated conditions [26].

Disadvantages:

- At start-up, the capacitors have to be pre-charged to their nominal value [6, 10].
- The number of clamping capacitors increases with number of levels in phase-voltage and becomes much excessive at higher levels making the topology more difficult, bulky and expensive [11].

The above disadvantages make this inverter limited to medium-voltage, high-power applications. However, FCMLI have found particularly viable for high bandwidth high switching frequency applications such as medium-voltage traction drives [15].

1.3.3 Cascaded H-bridge multilevel inverter (CHB MLI)

CHB appeared first in 1988 [23], matured during 1990s and gained more attention after 1997 [14, 27]. CHB is characterized by cascade connection of several H-bridges in each phase. This brings flexibility in circuit design, and produces high output voltages by aggregating the output of cascaded H-bridges. With n number of H-bridge cells (or n equal dc sources) per phase, the number of levels (m) in phase-voltage is $m = 2n+1$. As n is an integer, the number of levels in CHB is always odd. Fig. 1.9 shows the topological configuration of a five-level CHB in star configuration. CHB can be incorporated directly for high or medium-voltage power conversion without line-frequency transformer and acts as a profound motivation for next-generation MLIs [28]. Topological merits and demerits of CHB is presented below [16, 28-30].

Advantages:

- They can achieve high or medium-voltage power levels with mature medium-voltage semiconductor devices.
- Modular, scalable and flexible topological structure, switching redundancies, natural voltage balancing, even power distribution and uniform device rating [31].
- Doesn't require any extra clamping diodes or clamping capacitors.
- A direct connection to the system is possible by eliminating the line-frequency transformer. This is particularly advantageous as the existence of the transformer makes the inverter heavy and bulky [32], and also induces a dc magnetic flux deviation during line-to-ground faults [33].
- Switching redundancies of CHB helps in reconfiguration of circuit during under-rated or fault conditions [29].
- Predominantly suitable for applications such as AFC, ASD, BESS, HVDC, FACTS and CPD [14, 16, 28, 30, 34-37].

Disadvantages:

- Needs isolated/floating dc sources for power conversion.

In CHB, if the dc link voltage ratios are unequal then there is a significant increase in number of voltage levels is achieved [30, 38]. CHB with unequal dc voltages is known as asymmetrical CHB. The ratio of these dc sources can be either in arithmetic progression (AP) or geometric progression (GP). To have an effective reduction in switch count, geometric progression is normally practiced. Voltage ratios in geometric progression with common ratio two i.e., 1: 2: 4: 8… (2^0: 2^1: 2^2: 2^3…) is known as binary voltage ratios. Similarly, dc link voltages with common ratio three i.e., 1: 3: 9: 27 ... (3^0: 3^1: 3^2: 3^3…) is called as trinary voltage ratios.

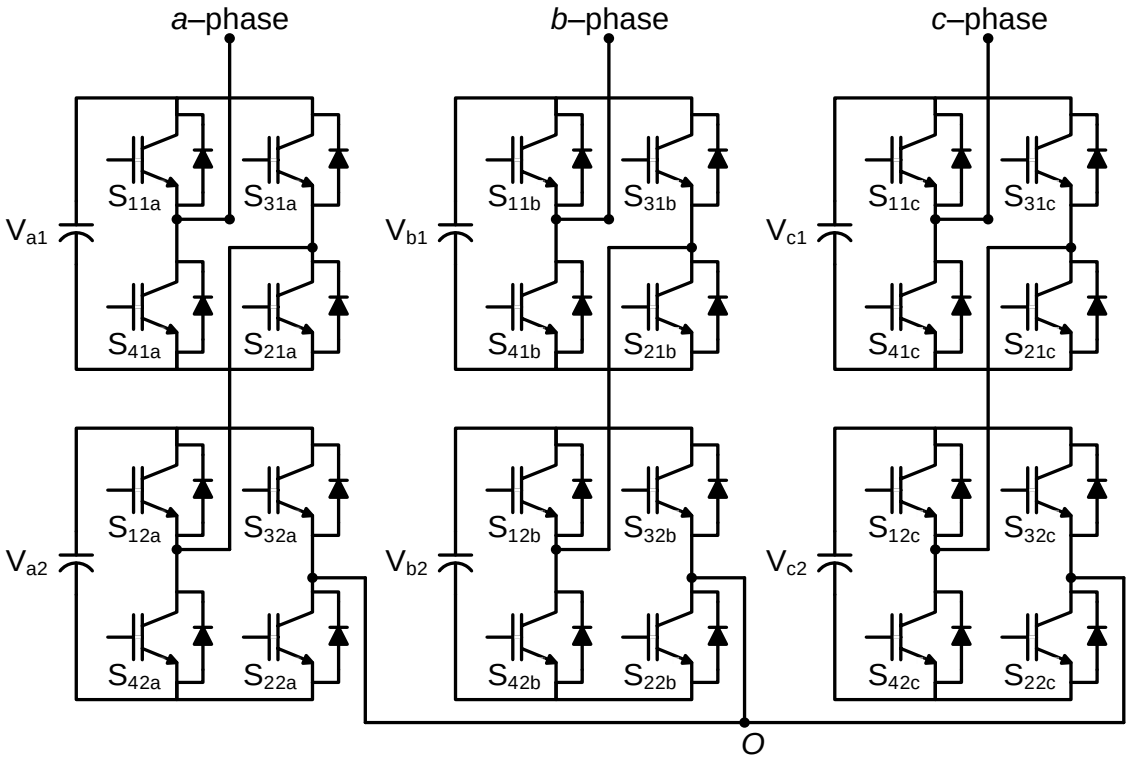


Fig. 1.9: A three-phase five-level CHB MLI.

The main advantage with asymmetrical CHB is to obtain more number of levels with less number of dc sources and switching devices. This reduces gating requirements, switch count and size of the inverter, when compared to its counter symmetrical configuration for the same level. With binary and trinary ratios of dc link voltages, the circuit configuration shown in Fig. 1.9 can produce seven and nine-levels respectively. This results in reduction of switch count of 33.33% and 50% for seven-level and nine-level respectively, in comparison to symmetrical CHB. On the flip side, different ratings of dc link voltages reduces switching redundancies and causes uneven utilization of dc sources. Further, in front-end applications, asymmetrical dc sources disables the multipulse rectifier function and avoids cancellation of input current harmonics [38].

Cascaded family of inverters are also characterized by cascade connection of modular chopper cells to form each cluster/phase-leg/arm. Cascaded MLI with H-bridge cells is known as cascade H-bridge (CHB) MLI. On the other hand, cascaded MLI composed with bi-directional chopper cells are known as modular multilevel inverters (MMI). However, the common concepts

hidden in the family members are “modular” structure and “cascade” connection. These concepts allow power electronics engineers to use the common term “modular multilevel cascade inverter (MMCI)” as a family name [28].

1.4 Other MLI topologies

Though “classical topologies” have gathered great attention both from academia and industry, their practical implementation is heavily influenced by the application, control complexity and cost. Also there exists no specific MLI topology, which is found to be absolutely advantages in any sort of application. This is due to the intrinsic characteristics of MLI, which are well suitable for few applications and totally in-appropriate for some other. Hence, researchers continued to explore and evolve newer topologies with an application oriented approach.

A single-phase MLI topology for PV application is reported in [39]. This configuration involves both uni-directional and bi-directional switches of different ratings. In [40], a CHB based hybrid inverter is reported for motor drive application and then investigated its performance in terms of design optimization, harmonic profile of the output waveform and capacitor voltage balance on a 500 HP, 4.5 kV induction motor drive. To solve the issue of series connected diodes in DCMLI, a modified diode clamped topology is reported in [41]. This topology involves mutual clamping amongst the clamping diodes in addition to the clamping of the main switches with clamping diodes. To achieve effective voltage balance of dc link capacitors in STATCOM based BESS, an additional circuit integrated with the diode clamped inverter is reported in [42]. In [43], a three-phase asymmetrical nine-level topology for medium-voltage drive application is reported by cascading three-level thyristor based inverter with two-level IGBT based H-bridge.

A fault tolerant topology to obtain uncompromised multilevel voltage waveform in the event of partial failure(s) of power circuit is reported in [44]. A CHB based active front-end converter for laminators and downhill conveyors loads is reported in [45]. In [46], an MLI involving two-level inverters to reduce current harmonics and mitigate output voltage derivatives is reported for medium/high power grid connected PV systems. Cascaded MLIs for battery charging of EV are reported in [47, 48]. To reduce dead-time effect and harmonic content in low-voltage high-speed motor drive applications, a three-level NPC topology with coupled reactors is reported [49].

1.5 Limitations of MLIs and significance of RSC-MLIs

To elevate the topological and performance limitations of classical MLI topologies to a generalized level, this section presents a comparison of their device count, modularity, fault tolerance, circuit complexity, ratings and cost [6, 7, 10, 11, 15, 16, 19, 30, 50, 51]. Table 1.1 shows the comparison of per-phase components requirement among CHB, DCMLI, and FCMLI for

obtaining *m* levels in phase-voltage. Table 1.2 presents the features and applications of these classical MLIs.

Table 1.1: Comparison of per phase-leg component requirement of classical MLI topologies.

Power component	**Inverter topology**		
	DCMLI	**FCMLI**	**CHB**
Main switching devices	$2(m-1)$	$2(m-1)$	$2(m-1)$
Anti-parallel diodes	$2(m-1)$	$2(m-1)$	$2(m-1)$
Clamping diodes	$(m-1)(m-2)$	0	0
DC bus capacitors	$(m-1)$	$(m-1)$	$\frac{(m-1)}{2}$
Flying capacitors	0	$\frac{(m-1)(m-2)}{2}$	0

Table 1.2: Comparison of classical MLI topologies based on implementation factors.

Implementation factor	**Inverter topology**		
	DCMLI	**FCMLI**	**CHB**
Specific requirements	Clamping diodes	Additional capacitors and their initialization	Isolated dc sources
Modularity	Low	High	Very high
Design and implementation complexity	Low	Medium	Least (with transformer-less applications)
Control concerns	Voltage balancing	Voltage setup	Power sharing
Fault tolerance	Difficult	Easy	Easy
Applications	CPDs, ASDs, conveyors, marine applications, and regenerative applications such as mining and renewable energy.	ASDs, medium-voltage traction drives.	FACTS, CPDs, High-power ASDs, electric and hybrid vehicles, photovoltaic power conversion, uninterruptible power supplies, and magnetic resonance imaging.
Cost [7, 50, 51]	Low (3-level), high (>= 4-level).	Medium (3-level), high (>= 4-level).	Very low (transformer-less applications), high (input transformer applications).
Available commercial ratings [6, 16]	2.3 to 6.6 kV, 3.7 to 44 MVA.	2.3 to 4.16 kV, 2.24 to 8 MVA.	2.3 to 13.8 kV, 6.2 to 120 MVA.

From the Table 1.1, Table 1.2 and literature survey on MLIs presented in the previous sections, the following observations can be drawn:

- DCMLI topologies seem to be the most suited for BESS, ASD and improved power quality converters (IPQC). But, the requirement of large number of power components and voltage unbalance problem at higher levels, limits DCMLI for low to medium-power applications [50, 51].
- FCMLI possess a modular structure with natural voltage balancing ability [25], but its application in realization of AFC and CPD is limited, due to the requirement of large number of capacitors and their pre-charge requirement [16].
- Least component count requirement, modular structure, high fault tolerance ability and absence of pre-charging requirements makes CHB best suited for high-voltage, medium-power applications (13.8 kV, 30 MVA) [30].
- As similar to DCMLI and FCMLI, switch count of CHB also increases with number of levels in phase-voltage and increases size, complexity, power losses.

Asymmetrical CHB-MLI possess appreciable reduction in switch count in comparison to symmetrical configurations. However, this reduction in switch count is achieved by compromising switching redundancies, unequal device ratings, and non-uniform utilization of dc sources. Therefore, the increased component count of power semiconductor devices and capacitor/dc sources of MLIs has led to the development of new area power converters named as reduced switch count multilevel inverters (RSC-MLI) [52]. As the name vindicates, a significant reduction in component count is achieved in these inverters when compared to traditional MLIs of same level. From the past decade, various enthusiasts carried out extreme research on RSC-MLIs and developed numerous topologies with significant reduction in component count, cost and ease of control.

1.6 Scope of the work and contributions

The advent of matured medium-voltage self-commutating power electronic devices has increased the prominence of MLIs for medium-power high-voltage applications. Despite this, the benchmark topologies of MLIs suffer with increased switch count and control complexity at higher levels. Hence the demand for reducing the size and switch count of MLI, has led to the development of RSC-MLIs. In last decade, a wide number of RSC-MLIs topologies are reported in the literature. Therefore, this thesis investigate the switching operation, features, modulation schemes and fault tolerant ability of RSC-MLI topologies and alleviated the performance limitations with the conventional schemes. The major contributions of this thesis are summarized below:

- This thesis, discuss the literature on various RSC-MLI topologies and classify them on their topological arrangement, switching operation, features and applications. Further, a

comprehensive comparison in terms of their device count, utilization of dc sources, device blocking voltages and power distribution is presented.

- ❖ Explored the limitations of conventional PWM schemes of RSC-MLIs in terms of generalization to higher level, controller complexity, computation time and THD performance and contributed the following:
  - Proposed a modified reduced carrier arrangement to improve inverter line-voltage THD performance and proposed a switching logic with unified logical expressions, such that the proposed PWM can be applicable to any RSC-MLI topology, irrespective to its topological arrangement and dc voltage ratio.
  - Simulation and experimental performance of the proposed PWM scheme is investigated on various asymmetrical thirteen-level RSC-MLI topologies.
  - Further, the superiority of the proposed PWM scheme in-terms of computation burden and line-voltage THD is compared with state-of-the-art PWM schemes reported for RSC-MLI topologies.
- ❖ Next, investigated the fault tolerant ability of modular redundant RSC-MLI topologies such as multilevel dc link (MLDCL), for multiple open-circuit (OC) switch faults.
  - Discussed the limitations of conventional fault tolerant schemes (FTS) reported for single/multiple OC switch faults in inverters.
  - Proposed a fault tolerant scheme (FTS) using neutral-shifting (NS) zero-sequence injection method, to tolerate simultaneous OC faults on multiple switches.
  - Generalised equations are derived to determine the magnitude of injected zero-sequence voltage and obtain fault tolerant modulating signals for the appeared fault condition. The fault tolerant ability of the inverter is investigated for multiple fault cases on fifteen and nine-level symmetrical MLDCL inverter in both simulation and experimental platforms.
- ❖ Further, investigated the closed-loop performance of proposed PWM and FTS on MLDCL based active rectifier.
  - A three-phase fifteen-level MLDCL based active rectifier with voltage oriented control (VOC) and grid active and reactive power control (GARPC) algorithms, involving proposed FTS and reduced carrier rotation PWM is implemented on OPAL-RT 4500 real-time simulator.
  - Investigated the performance of active rectifier and results are analyzed for set-point change in reference variables, regeneration capacity and dynamic variations in load.
  - Further, the efficacy of the proposed FTS in compensating multiple OC switch faults and balancing converter dc link voltages and powers is demonstrated by considering a

fault condition in MATLAB/Simulink environment. Finally, the obtained simulation results are validated on OPAL-RT 4500 real-time controller.

1.7 Organization of thesis

Apart from this chapter, this thesis contains six more chapters and the work included in each of these chapters is briefly outlined as follows:

CHAPTER 2 presents the literature survey on various topologies of RSC-MLI and analyses the effect of reduction in switch count on inverter operation. Further, presents a comparative study of their features in terms of device count, device blocking voltages, power distribution, dc link voltage balancing, structural modularity, extension to higher levels and feasibility of asymmetry is discussed. Later, the criterion for selecting multilevel dc link (MLDCL) inverter for further study is investigated.

CHAPTER 3 presents the PWM schemes of RSC-MLI topologies. Initially this chapter presents the literature survey on various modulation schemes reported for RSC-MLIs and explores their limitations in terms of switching logic and THD performance. Then, proposes a modified reduced carrier PWM with unified logical expressions and evaluates its simulation and experimental performance on various thirteen-level RSC-MLIs. Further, its superiority is compared with PWM schemes reported in literature.

CHAPTER 4 aims to investigate fault tolerant ability of modular RSC-MLI topologies. This chapter starts with literature survey on conventional FTS for compensating OC switch faults and discuss their limitations for compensating multiple OC switch faults and application to RSC-MLIs topologies. Further, proposes a generalized FTS to compensate simultaneous OC switch faults on one or more phases of MLI/RSC-MLI. The efficacy of the proposed FTS in obtaining balanced operation with uniform burdening of the operating units is verified for various fault cases on fifteen-level MLDCL inverter in Simulink environment. Obtained simulation results are validated experimentally by developing nine-level MLDCL inverter controlled by OPAL-RT 4500.

CHAPTER 5 intends to analyse the closed-loop performance of the proposed PWM and NS-FTS on a modular redundant RSC topology for front-end converter application. Thus, this chapter proposes a fifteen-level MLDCL based active rectifier and investigates its pre and post-fault performance. Furthermore, the efficacy of proposed FTS in obtaining required balanced line-voltages, currents, dc link voltages and load powers is validated in real-time using OPAL-RT 4500 simulator.

The main conclusions of the presented work and possible future scope of research are summarized in **CHAPTER 6**. The detailed description in developing experimental and real-time studies is described in **Appendix A.** This includes the detailed description in developing generalized

inverter module with 24 isolated IGBT switches and implementation of control algorithms in dSPACE MicroLabBox and OPAL-RT 4500 controller.

CHAPTER 2: TOPOLOGIES OF RSC-MLI

This chapter presents literature survey on various reduced switch count multilevel inverters (RSC-MLIs) topologies. Based on this, a comprehensive comparison of these RSC-MLIs topologies is presented in terms of device count, device blocking voltage, power distribution, modularity, fault tolerant capability and ability to balance capacitor voltages.

2.1 Introduction

MLIs served as a cutting-edge technology for high-power, medium-voltage systems by incorporating matured medium-power semiconductor devices. Classical topologies of MLIs such as DCMLI, FCMLI and CHB have their own merits and demerits and are well suited for a specific sort of application. However in common, their component requirement and switching device count significantly increases with number of output voltage levels. Increase in switch count involves additional driver, dead-band, isolation circuits and their associated heat sink and protection circuit requirement. Moreover, increased switch count further increases computational burden on the controller. Thus, size, cost and complexity of classical MLIs increases at higher levels, makes the overall inverter expensive and imposes limitations on its practical implementation and market penetration [6, 7, 50, 51]. To overcome the above limitations, a new domain of MLIs named as reduced switch count multilevel inverters (RSC-MLI) are emerged in recent times. The objective of these inverters is to reduce the size, cost and complexity as compared to classical topologies. From past decade, various topologies of RSC-MLIs are reported [52]. This chapter presents a brief literature survey on these topologies and analyse the effect of reduction in device count on their topological structure and operational features.

2.2 Factors considered in proposing new RSC-MLI topology

In past decade, due to an extensive research, various RSC-MLIs topologies are reported in literature. Researchers often consider various performance factors in proposing a new RSC-MLI topology and these factors are summarised below.

- **Reduction in device count**: This factor indicates the overall reduction in number of switching devices, diodes, capacitors and other auxiliary components.
- **Device blocking voltage**: Unlike in classical MLIs, the device blocking voltage in RSC-MLI topologies may be unequal. This necessities the requirement of devices with different voltage ratings.
- **Nature of dc link**: Based on the converter topology, the dc link may be equipped with isolated or non-isolated dc sources or a congregation of dc sources and capacitors.

- **Modular structure**: The structure of topology may be modular by connecting several basic units/H-bridges in series, parallel or in cascade. An RSC-MLI with modular structure can easily extended to higher levels.
- **Requirement of bi-directional switches**: In some topologies, switches with bi-directional voltage blocking and bi-directional current conducting capability are required.
- **Fault tolerant capability**: Ability of the inverter to work under abnormal operating conditions such as faults on switching devices or dc sources. Higher fault tolerant capability ensures greater reliability of the inverter.
- **Switching and conduction losses**: Developing a new RSC-MLI topology such that it produces desired output voltage by operating the switching devices with minimized switching and conduction losses.
- **Even power distribution**: Ability of the inverter to obtain required phase-voltage levels by distributing uniform power across all basic units/H-bridges. This feature contributes to charge balance among dc link voltages.
- **Application area**: In this, a critical analysis is made to the newly developed topology in finding out its best application in the areas such as FACTS, HVDC, CPD, BESS, ASD, IPQC, EV and consumer electronics.

2.3 Classification of RSC-MLI topologies

RSC-MLI topologies can be classified into several categories based on the factors discussed above. The possible classification of these RSC-MLI topologies is presented below.

2.3.1 Based on the physical structure or topological arrangement

Considering the physical arrangement of switches, dc link voltages (capacitors or dc sources) and other auxiliary devices such as diodes, the following classifications can be made for the structure of RSC-MLIs.

***(a) Modular topologies*:** The topological arrangement of most of the RSC-MLIs is framed by involving multiple identical units connected in series or parallel or cascade. These topologies can easily be extended to higher levels and are known as modular topologies. Each basic building unit (modular unit) of these topologies produce a finite number of output voltage levels with positive or negative polarity.

***(b) Topologies with generalized structure*:** Most of the RSC-MLI possess the topological arrangement that realize any number of phase-voltage levels. These topologies can be called as generalized RSC-MLI. Multilevel dc link inverter (MLDCL) [53, 54], reverse voltage (RV) [55], T-type [56-61] and switched series parallel sources (SSPS) [62, 63] are few of such topologies. On the other hand, few RSC-MLIs possess a topological arrangement to obtain only

a specific number of voltage levels. In detail, each unit of these topologies is designed for obtaining fixed number of output voltage levels (higher than three) and can be grouped as unit-based RSC-MLIs. One of the best example is E-Type RSC-MLI [64], where each unit of E-type is framed to obtain thirteen-levels in phase-voltage. Most often, these unit-based RSC-MLIs are extended to higher levels through series or cascade connection.

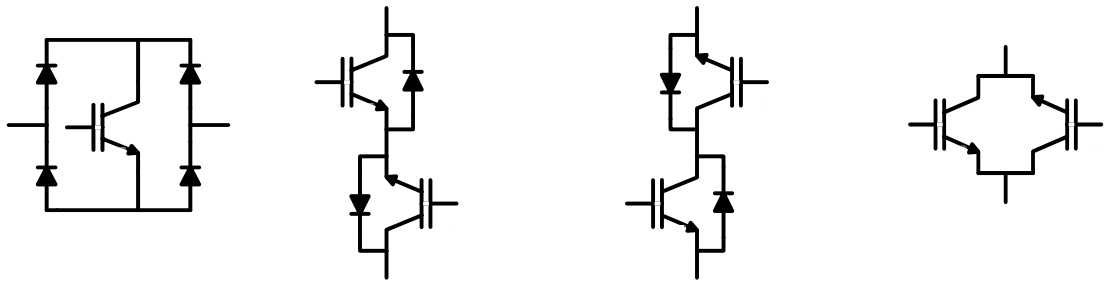
***(c) Physical arrangement*:** The interconnection of the switching devices and dc link voltages of RSC-MLIs involve multiple units (modular or non-modular) connected in a specific physical pattern. This physical arrangement may be of ladder, stair case, column or U-shaped. They may also have cascade structure or sometimes may not have any specific layout.

***(d) Topologies with H-bridge/HSC structure*:** Due to the modular structure of CHB over the other classical MLIs, various RSC-MLI topologies are reported by incorporating H-bridge integrated with multiple modular/non-modular units. It is to be noted that the purpose and operation of the H-bridge in RSC-MLIs is different and vary with topology. On the other hand, few topologies involve hexagon switched cell (HSC) rather than H-bridge structure. Presence of HSC permits the inverter to produce output for multiple switching combinations. Examples of such MLIs are hybrid T-type [65, 66] and cascaded MLI with HSC [67, 68].

***(e) Topologies with bi-directional switching devices*:** The topological pattern of few RSC-MLIs such as T-type [56-61], cascaded bipolar switched cells (CBSC) [69] require power semiconductor switches which have the ability to block voltage and conduct current in both directions. Unfortunately, there are no such switches currently available. Therefore, discrete semiconductor devices are incorporated to construct a switch with bi-directional voltage blocking and current conducting capability. Fig. 2.1 shows the possible arrangements with IGBTs and diodes to obtain bi-directional switch. Fig. 2.1(a) shows bi-directional switch formed with one controllable switch (such as IGBT) and four diodes. The diodes are arranged to form a single-phase diode bridge rectifier and the controllable switch is placed in between the legs of diode bridge rectifier. This bi-directional device arrangement shown in Fig. 2.1(a) requires only one IGBT and one gate driver. On the other hand, device losses are relatively high, since, there are three devices (two diodes and IGBT) in each conduction path and moreover the direction of current through the switch cell cannot be controlled. The common emitter and common collector bi-directional switch cell arrangements with two diodes and two IGBTs connected in antiparallel are shown in Fig. 2.1(b) and (c) respectively. In these arrangements diodes are included to provide the reverse blocking capability. There are several advantages in these arrangements when compared to the former one. In these arrangements, it is possible to independently control the direction of the current. Moreover, the conduction losses are also reduced since only two devices (IGBT and diode) carry the current in each conduction path.

The conduction losses are same in both these switch cell arrangements. One possible disadvantage of Fig. 2.1(c) is that each IGBT requires an isolated gate driver circuit, so the gate driver circuits will be expensive [69, 70].

However, in common emitter configuration, the central connection allows both devices to be controlled from one isolated gate driver. Alternatively, two reverse-blocking (RB) IGBTs in an antiparallel connection as shown in Fig. 2.1(d), can block voltage and current in both directions and offer a convenient way to implement a bi-directional switch. This configuration is similar to Fig. 2.1(b) and (c), but without the central common connection, nevertheless this connection provide the transient benefits during switching. The most important benefit of Fig. 2.1(d) is the reduction of conduction losses. However, the reverse voltage blocking capability is obtained by changing the structure of a normal IGBT.



(a) Diode-bridge (b) Common-emitter (c) Common-collector (d) Reverse-blocking IGBT

Fig. 2.1: Possible arrangement of bi-directional switch.

***(f) Requirement of isolated dc sources*:** Depending on the topological arrangement, the dc link capacitors (or stiff voltage sources) of RSC-MLIs may be isolated (floating) or non-isolated [53]. The dc link voltage requirement of RSC-MLI with floating or isolated dc sources can be obtained from batteries or photo-voltaic (PV) cells or multipulse converter with phase-shifting transformers. Similarly, few RSC-MLI topologies involve non-isolated dc link voltages with the dc sources or capacitors connected in series/parallel through multiple intermediate nodes [55-60]. In specific topologies, such as nested and three-phase symmetrical RSC-MLI involve non-isolated dc link voltages such that a dc link is connected in common to all the three-phases [71-73]. These topologies can be an alternative to DCMLI and FCMLI.

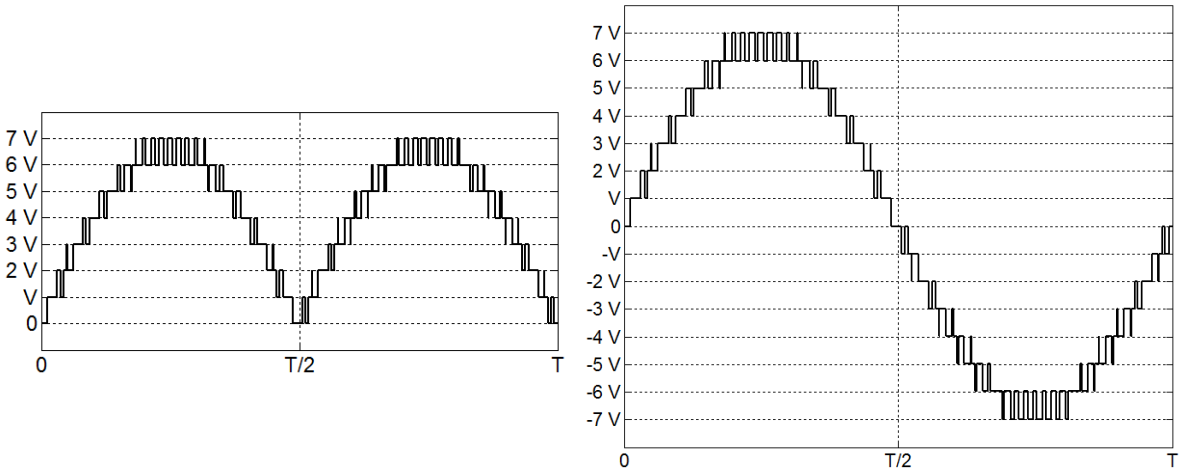
2.3.2 Based on operation and performance

Considering the inverter switching operation, ratio of dc link voltages, device blocking voltages, utilization of dc sources, load power distribution, and fault tolerant ability, the following classifications can be made.

***(a) Symmetrical and asymmetrical RSC-MLI topologies*:** To obtain more number of levels, without modifying the inverter physical structure, asymmetrical configuration are opted.

Asymmetrical MLI topologies involves unequal magnitude of dc link voltages and obtains the required output voltage levels for additive or subtractive combination of dc link voltages. Thus, an inverter with equal ratio of input dc sources is called as symmetrical configuration and the inverter with unequal ratio of input dc sources is called as asymmetrical configuration. Asymmetrical ratio of dc voltages produces appreciable reduction in switch count in comparison with symmetrical configuration. These voltage ratios can either be in geometric progression (GP) or arithmetic progression (AP). However, voltage ratios in GP produces more voltage levels with extensive reduction in switch count. Most often, GP with common ratio of two (binary) or three (trinary) is preferred. It is to be noted that an asymmetrical configuration with trinary voltage ratios will be realized, only if the inverter configuration can facilitate output for additive and subtractive combinations of dc link voltages. Asymmetrical RSC-MLI configurations reduces size and complexity, but reduces the switching redundancies drastically. This further restricts inverter fault tolerant ability, limits capacitor voltage balancing, increases device blocking voltages and produce non-uniform power distribution among basic units. E-type [64] and square T-type [74] are the examples of unit-based asymmetrical RSC-MLI configurations.

***(b) Topologies with separate level and polarity generators*:** To obtain the required number of phase-voltage levels, the structure of most of the RSC-MLIs comprises of a separate polarity and level generators. The level generator involves multiple switching devices interconnected with dc link voltages to produce a unipolar staircase voltage waveform. Further, polarity generator converts this unipolar voltage to bipolar using an H-bridge. For example, if a level generator of RSC-MLI produces unipolar voltage with n-level, then polarity generator converters this unipolar voltage to bipolar with $(2n–1)$ levels. Fig. 2.2 shows the voltage waveforms generated from level and polarity generators. Few of such RSC-MLIs are MLDCL [53], SSPS [62, 63] and RV [55]. Most often, blocking voltage of each device in polarity generator is equal to the total dc link voltage. Therefore, device rating in polarity generator is quite high and operated at fundamental or low switching frequency.



(a) Output of level generator (unipolar) (b) Output of polarity generator (bipolar)

Fig. 2.2: Output voltage of level and polarity generators.

***(c) Topologies with even power distribution or equal load sharing*:** When the multilevel dc to ac conversion is carried out in such a way that each input source contributes equal power to the load, the power distribution amongst the sources is said to be "even". Some authors also refer it as "charge balance control" or "equal load sharing" [75]. Even power distribution is a feature of control aspect only when the topology permits. When the inverter configuration is symmetric, the control algorithm is designed such that the average current drawn from each source is equal, thereby making average powers equal. For a given topology, even power distribution is possible if each input source contributes towards all the output levels in one or more output cycles. For example, if a topology has three symmetric input dc sources V_{dc1}, V_{dc2} and V_{dc3} ($V_{dc1} = V_{dc2} = V_{dc3} = V_{dc}$), then a natural even power distribution is possible if all the combinations shown in Table 2.1 are permitted by the topology.

Table 2.1: Required switching combinations for even power distribution with three dc sources.

Output voltage level	**Required combination of input dc levels**
$\pm V_{dc}$	$\pm V_{dc1}$
$\pm V_{dc}$	$\pm V_{dc2}$
$\pm V_{dc}$	$\pm V_{dc3}$
$\pm 2V_{dc}$	$\pm(V_{dc1}+V_{dc2})$
$\pm 2V_{dc}$	$\pm(V_{dc2}+V_{dc3})$
$\pm 2V_{dc}$	$\pm(V_{dc3}+V_{dc1})$
$\pm 3V_{dc}$	$\pm(V_{dc1}+V_{dc2}+V_{dc3})$

***(d) Topologies with equal blocking voltages*:** Reduction in switch count of RSC-MLIs has modified their topological arrangement by changing the interconnection between dc sources, uni-directional and bi-directional switching devices. This interconnection of the dc link voltages and switching devices impacts the rating and voltage stress of the operating devices, such that they encounter unequal blocking voltages. Thus, considering the device blocking voltages,

RSC-MLI can be classified into topologies with even and uneven blocking voltages. However, RSC-MLI topologies with uniform device blocking voltages are more preferred as they involve devices with equal ratings and have a provision to operate uniform conduction losses. In industrial applications, RSC-MLIs with modular structure, and uniform switch ratings have remarkable prominence. Further, the sum of the device blocking voltages of all the operating devices contributes to the maximum voltage blocking capability of the overall inverter. For example, if an inverter consists of four switches rated at V_{dc} and six switches rated at $2V_{dc}$, then the total voltage blocking capability of the inverter can be calculated as: $(4 \times V_{dc}) + (6 \times 2V_{dc}) = 16V_{dc}$.

***(e) Topologies with switched series/parallel dc sources*:** In multilevel voltage generation, the phase-voltage level is increased with series operation of each dc source and the phase-voltage maximum value or level may achieved with turn-on of all dc sources in that phase. However, in topologies such as SSPS, to obtain a particular voltage level, all or some of the dc sources need to be connected in series/parallel [62, 63]. This series/parallel operation allows greater utilization of dc sources and is particularly advantageous in PV applications. Also this nature of series/parallel switching of dc sources balance the rate of charge and discharge of the dc link capacitors with ease.

***(f) Fault tolerant ability*:** With the development of matured medium-power electronic devices, MLIs are found viable for high-voltage and medium-power applications. However, ability of the inverter to work in fault prone conditions plays a vital role in ensuring the safety, continuity and reliability of the overall system. Any internal or external fault(s) on the inverter will restrict the phase-voltage levels and further produces unbalance in its corresponding phase-voltages, line-voltages and currents. This dysfunction of inverter degrades the overall system performance, produces temperature effects with abnormal voltages/currents and results dangerous effects on the load side. In case of the switch faults, switching redundancies provide an alternate path for the fault switch and helps in restoring the balanced operation. Thus, switching redundancies play an important role in reconfiguration of the inverter during faulty condition. However, extreme reduction in switch count of RSC-MLI has drastically reduced its switching redundancies and restricted its fault tolerant ability. However, the growing interest on RSC-MLIs for industrial and domestic applications has increased the prominence of RSC-MLIs topologies with fault tolerate ability. One of such example is MLDCL, where effect of fault on any basic unit is similar to effect of fault on H-bridge in CHB MLI.

2.4 Topologies of RSC-MLIs

This Section presents the properties, specifications, operation and applications of various RSC-MLI topologies. Properties of the topology is defined in terms of modularity, redundancy,

fault tolerant capability, regeneration capability, dc voltage requirement and capability to support asymmetric dc voltage ratios. On the other hand, the specifications of the topology include device count, type of switching device, maximum blocking voltages and device ratings.

2.4.1 Multilevel dc-link (MLDCL) RSC-MLI

Among the recently reported RSC-MLI topologies, MLDCL is one of the popular topology with modular structure. This topology is reported by S. Gui-Jia in 2005 [53, 54]. The topological structure of MLDCL involves a separate level and polarity generator. The modular and redundant structure of MLDCL with floating dc link capacitors turns it to be an attractive alternative to CHB for regenerative front-end converters, power quality improvement and grid connected applications. The level generator of MLDCL consists of series connection of several basic units. Each basic unit consists of a half-bridge or chopper-cell with an isolated dc source. The switching operation of each basic unit produces an output voltage of either V_{dc} or zero. With n number of basic units, the level generator produces unipolar voltage with levels ranging from zero to nV_{dc}, with n+1 levels. Polarity generator involves an H-bridge with switches operating at fundamental frequency and converts this unipolar voltage to bipolar voltage with 2n+1 levels in phase-voltage. The switches in the level generator operates with uniform voltage stress and equal device blocking voltage (V_{dc}). However, the blocking voltages of switches in the polarity generator is equal to the total dc link voltage (nV_{dc}). Topological arrangement of MLDCL possess the capability to realize both symmetrical and asymmetrical configurations. A single-phase MLDCL RSC-MLI with three dc sources is shown in Fig. 2.3.

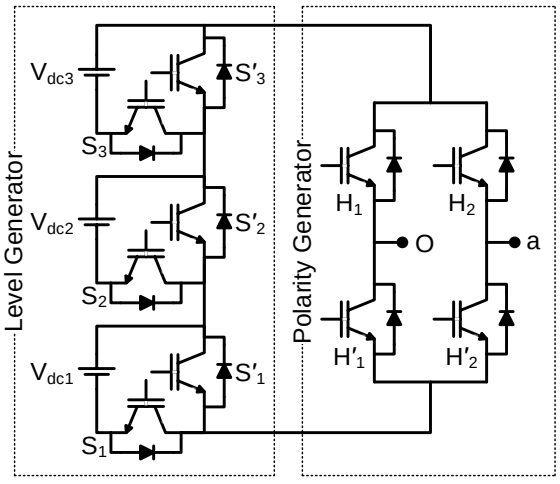


Fig. 2.3: Multilevel dc link (MLDCL) RSC-MLI with three dc sources.

With equal sources in the dc link, Fig. 2.3 produces seven-level in phase-voltage. On the other hand, selecting dc sources with 1: 2: 3 ratio, Fig. 2.3 produces thirteen-levels. Switching operation of symmetrical and asymmetrical configuration of this MLDCL inverter is shown in Table 2.2.

Table 2.2: Switching states of MLDCL inverter.

Num. of states	Voltage combinations	Switches in conduction		Output voltage	Output voltage
		Level generator	Polarity generator	$V_{dc1} = V_{dc2} = V_{dc3} = V_{dc}$	$V_{dc1}: V_{dc2}: V_{dc3} = 1: 2: 3\ V_{dc}$
1	$V_{dc1}+V_{dc2}+V_{dc3}$	S_1-S_2-S_3	H_1-H'_2	$+3V_{dc}$	$+6V_{dc}$
2			H_2-H'_1	$-3V_{dc}$	$-6V_{dc}$
3	$V_{dc2}+V_{dc3}$	S_1'-S_2-S_3	H_1-H'_2	$+2V_{dc}$	$+5V_{dc}$
4			H_2-H'_1	$-2V_{dc}$	$-5V_{dc}$
5	$V_{dc1}+V_{dc3}$	S_1-S_2'-S_3	H_1-H'_2	$+2V_{dc}$	$+4V_{dc}$
6			H_2-H'_1	$-2V_{dc}$	$-4V_{dc}$
7	$V_{dc1}+V_{dc2}$	S_1-S_2-S_3'	H_1-H'_2	$+2V_{dc}$	$+3V_{dc}$
8			H_2-H'_1	$-2V_{dc}$	$-3V_{dc}$
9	V_{dc3}	S_1'-S_2'-S_3	H_1-H'_2	$+V_{dc}$	$+3V_{dc}$
10			H_2-H'_1	$-V_{dc}$	$-3V_{dc}$
11	V_{dc2}	S_1'-S_2 -S_3'	H_1-H'_2	$+V_{dc}$	$+2V_{dc}$
12			H_2-H'_1	$-V_{dc}$	$-2V_{dc}$
13	V_{dc1}	S_1-S_2'-S_3'	H_1-H'_2	$+V_{dc}$	$+V_{dc}$
14			H_2-H'_1	$-V_{dc}$	$-V_{dc}$
15	0	S_1'-S_2'-S_3'	H_1-H'_2	0	0
16			H_2-H'_1		

2.4.2 Switched series parallel sources (SSPS) RSC-MLI

Switched series parallel sources (SSPS) RSC-MLI topology utilizes switching of dc voltage sources in series/parallel to increase the number of levels. This topology is reported by Hinago and Koizumi in 2009 [62, 63]. SSPS possess a modular structure with separate polarity and level generator. As level generator cannot produce zero-voltage level, this is obtained from polarity generator. The structure of SSPS with three voltage sources is shown in Fig. 2.4. With *n* identical dc voltages, SSPS produces $2n+1$ levels in phase-voltage, by involving $3(n-1)$ switches in level generator and four switches in polarity generator. With series/parallel operation, SSPS is operated in self-balancing mode, where one stiff dc link voltage of V_{dc} is sufficient to charge all the dc link capacitors such that the voltage across each dc link capacitor is V_{dc}. Thus, the output voltage of the inverter is boosted by *n* times the input voltage. This nature of SSPS is well suitable for battery charging and energy storage applications. Further, the series/parallel operation increases the utilization of dc sources, which is advantageous in grid-connected photovoltaic systems. The switching operation of SSPS with symmetrical and asymmetrical dc sources is given in Table 2.3. From this table it is observed that, for any voltage level, only two devices of level generator remains in conduction for both positive and negative polarity of a specific voltage level.

Considering equal dc voltages in Fig. 2.4, SSPS produces seven-level in phase-voltage. The switching redundancies shown in Table 2.3 of symmetrical SSPS helps in obtaining equal utilization of dc sources and improve its fault tolerant ability. For considered symmetrical case, the maximum

blocking voltage across each device in level and polarity generator is V_{dc} and $3V_{dc}$ respectively. Similar to MLDCL, SSPS cannot operate with trinary voltage ratios. Switching operation of asymmetrical SSPS with dc sources in 1: 2: 3 voltage ratio to obtain thirteen-levels in phase-voltage is shown in Table 2.3. A further reduction in switch count and switching losses are also possible with an addition of an H-bridge to SSPS as reported in [62]. To reduce the switching losses, the additional H-bridge can be operated at carrier frequency and level generator at fundamental frequency.

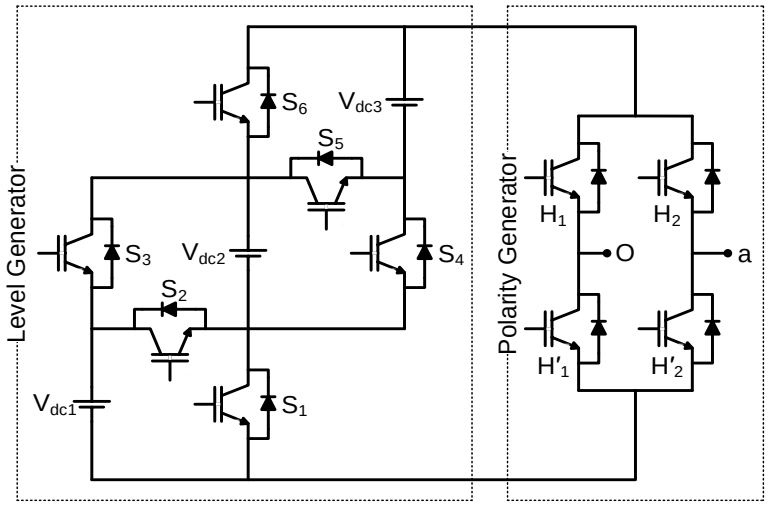


Fig. 2.4: Switched series parallel sources (SSPS) RSC-MLI with three dc sources.

Table 2.3: Switching states of SSPS inverter.

Num. of states	**Voltage combinations**	**Switches in conduction**		**Output voltage**	**Output voltage**
		Level generator	**Polarity generator**	**$V_{dc1} = V_{dc2} = V_{dc3} = V_{dc}$**	**$V_{dc1} : V_{dc2} : V_{dc3} = 1: 2: 3\ V_{dc}$**
1	$V_{dc1}+V_{dc2}+V_{dc3}$	S_2-S_5	H_1-H'_2	$+3V_{dc}$	$+6V_{dc}$
2			H_2-H'_1	$-3V_{dc}$	$-6V_{dc}$
3	$V_{dc2}+V_{dc3}$	S_1-S_5	H_1-H'_2	$+2V_{dc}$	$+5V_{dc}$
4			H_2-H'_1	$-2V_{dc}$	$-5V_{dc}$
5	$V_{dc1}+V_{dc3}$	S_3-S_5	H_1-H'_2	$+2V_{dc}$	$+4V_{dc}$
6			H_2-H'_1	$-2V_{dc}$	$-4V_{dc}$
7	$V_{dc1}+V_{dc2}$	S_2-S_6	H_1-H'_2	$+2V_{dc}$	$+3V_{dc}$
8			H_2-H'_1	$-2V_{dc}$	$-3V_{dc}$
9	V_{dc3}	S_1-S_4	H_1-H'_2	$+V_{dc}$	$+3V_{dc}$
10			H_2-H'_1	$-V_{dc}$	$-3V_{dc}$
11	V_{dc2}	S_1-S_6	H_1-H'_2	$+V_{dc}$	$+2V_{dc}$
12			H_2-H'_1	$-V_{dc}$	$-2V_{dc}$
13	V_{dc1}	S_3-S_6	H_1-H'_2	$+V_{dc}$	$+V_{dc}$
14			H_2-H'_1	$-V_{dc}$	$-V_{dc}$
15	0	----	H_1-H_2	0	0
16			H'_2-H'_1		

2.4.3 Reverse voltage (RV) RSC-MLI

In 2012, Ehsan Najafi introduced a new topology with a reversing-voltage phenomenon and thus named it as reverse voltage (RV) RSC-MLI [55, 76] . This topology requires less components particularly at higher levels, which leads to the reduction in overall cost and complexity of the inverter. The structure of RV topology with three voltage sources is shown in Fig. 2.5. This topology has modular structure with separate polarity and level generators and is extended to higher levels by duplicating the encircled middle stage of level generator shown in Fig. 2.5.

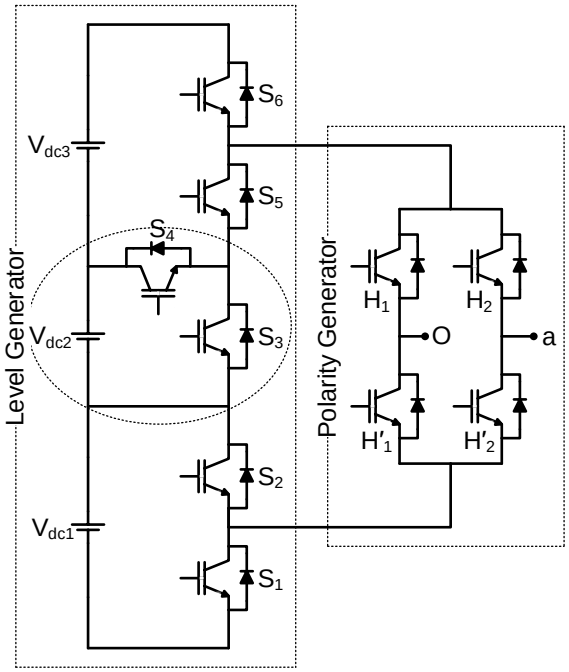


Fig. 2.5: Reverse voltage (RV) RSC-MLI with three dc voltage sources.

With *n* identical dc sources, RV involves 2*n* switches in level generator and four switches in the polarity generator and obtains 2*n*+1 levels in phase-voltage. Further, with identical dc sources, the switches in level generator operates with equal blocking voltages. This topology uses isolated dc supplies. However, by using isolation transformers at the load terminals, three-phase RV can be implemented with a common dc link for all the phases. This will reduce the requirement of dc sources to 1/3, as compared to CHB MLI [55]. An asymmetrical RV inverter configuration is also possible for appropriate combination of dc sources. The switching operation of symmetrical and asymmetrical RV (shown in Fig. 2.5) for obtaining seven and thirteen-levels in phase-voltage is given in Table 2.4. From Table 2.4, it is observed that RV produce voltage levels for additive combinations of dc sources and doesn't have adequate switching redundancies to obtain even utilization of dc sources.

Table 2.4: Switching states of RV inverter.

Num. of states	Voltage combinations	Switches in conduction		Output voltage	Output voltage
		Level generator	Polarity generator	$V_{dc1} = V_{dc2} = V_{dc3} = V_{dc}$	$V_{dc1}: V_{dc2}: V_{dc3} = 1: 3: 2\ V_{dc}$
1	$V_{dc1}+V_{dc2}+V_{dc3}$	S_1-S_6	H_1-H'_2	$+3V_{dc}$	$+6V_{dc}$
2			H_2-H'_1	$-3V_{dc}$	$-6V_{dc}$
3	$V_{dc2}+V_{dc3}$	S_2-S_6	H_1-H'_2	$+2V_{dc}$	$+5V_{dc}$
4			H_2-H'_1	$-2V_{dc}$	$-5V_{dc}$
5	$V_{dc1}+V_{dc2}$	S_1-S_4-S_5	H_1-H'_2	$+2V_{dc}$	$+4V_{dc}$
6			H_2-H'_1	$-2V_{dc}$	$-4V_{dc}$
7	$V_{dc1}+V_{dc3}$	---	----------		
9	V_{dc2}	S_2-S_4-S_5	H_1-H'_2	$+V_{dc}$	$+3V_{dc}$
10			H_2-H'_1	$-V_{dc}$	$-3V_{dc}$
11	V_{dc3}	S_2-S_3-S_4-S_6	H_1-H'_2	$+V_{dc}$	$+2V_{dc}$
12			H_2-H'_1	$-V_{dc}$	$-2V_{dc}$
13	V_{dc1}	S_1-S_3-S_5	H_1-H'_2	$+V_{dc}$	$+V_{dc}$
14			H_2-H'_1	$-V_{dc}$	$-V_{dc}$
15	0	S_2-S_3-S_5	H_1-H'_2	0	0
16			H_2-H'_1		

2.4.4 Series connected switched sources (SCSS) RSC-MLI

Series connected switched sources (SCSS) is a symmetrical RSC-MLI topology with separate polarity and level generators [77, 78]. With *n* dc sources, SCSS produces 2*n*+1 levels in phase-voltage, by involving 2*n* switches in level generator and four switches in polarity generator. Level generator possess multiple modular units connected in series and arranged in stair-case structure, as shown in Fig. 2.6.

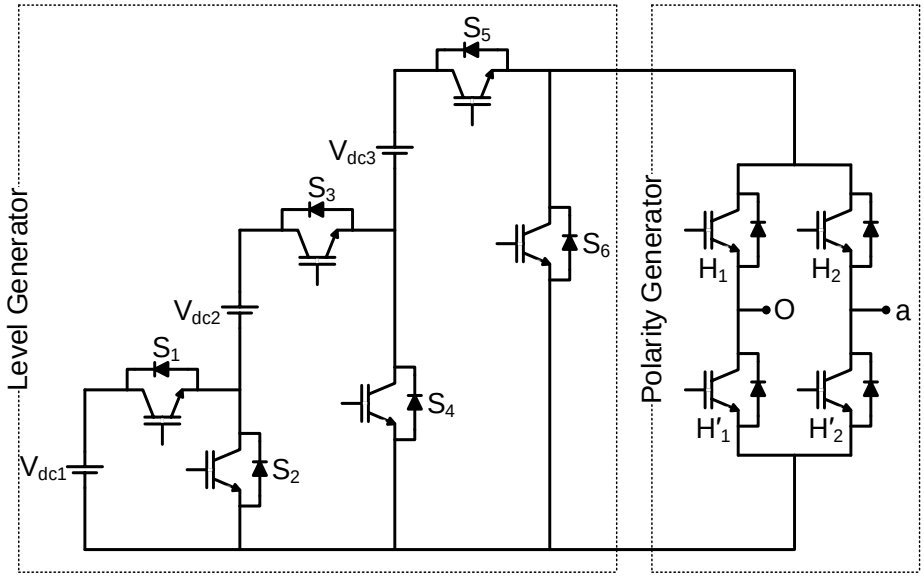


Fig. 2.6: Series connected switched sources (SCSS) RSC-MLI with three dc voltage sources.

Each unit of level generator has a dc source with complimentary switch pair. As the name of the inverter conveys, SCSS achieves the required phase-voltage levels by switching the series connected dc sources. The switching devices in level generator are operated at carrier frequency and the devices in the polarity generator are operated at fundamental frequency. This topology can easily be extended to higher levels, however, the devices blocking voltages are unequal and increases with the maximum dc link voltage. The dc sources are non-isolated and can be replaced with PV or solar cell in the grid connected applications. The topological arrangement of SCSS with three dc sources is shown in Fig. 2.6 and its switching operation to obtain seven-levels in phase-voltage is shown in Table 2.5. From this table, it is observed that the absence of switching redundancies in this topology increases difficulty in balancing dc link voltages.

Table 2.5: Switching states of seven-level SCSS topology.

Num. of states	**Voltage combinations**	**Switches in conduction**		**Output voltage**
		Level generator	**Polarity generator**	**$V_{dc1}= V_{dc2}= V_{dc3} = V_{dc}$**
1	$V_{dc1}+V_{dc2}+V_{dc3}$	S_1-S_3-S_5	H_1-H'_2	$+3V_{dc}$
2			H_2-H'_1	$-3V_{dc}$
3	$V_{dc2}+V_{dc3}$	S_2-S_3-S_5	H_1-H'_2	$+2V_{dc}$
4			H_2-H'_1	$-2V_{dc}$
5	V_{dc3}	S_4-S_5	H_1-H'_2	$+V_{dc}$
6			H_2-H'_1	$-V_{dc}$
7	0	S_6	H_1-H'_2	0
			H_2-H'_1	

2.4.5 T-type topologies

Among the various RSC-MLI topologies, T-type is one of the most popular topology with appreciable reduction in switch count. This MLI involves a combination of uni-directional and bi-directional switches. In literature, this topology is reported in three different arrangements. They are (a) T-type [56, 58, 61, 79, 80] (b) Half-leg T-type [81] and (c) Cascaded T-type [60]. All these topologies are modular in structure and can be generalized for any level, however each of them has their own merits and limitations. Next section demonstrates their topological arrangement, operation and features.

2.4.5.1 T-type RSC-MLI

This H-bridge based topology is reported by Ceglia *et al*. in 2006 and is well reported for grid connected PV based applications [56, 58, 61, 79, 80]. With *n* (identical) dc voltage sources, this topology involves *n*+1 bi-directional switches and four uni-directional switches and produce 2*n*+1 levels in phase-voltage. The uni-directional switches are arranged to form an H-bridge and the mid-point of one phase-leg of H-bridge is connected to the dc link voltages through bi-directional switches. The switching devices in a phase-leg of an H-bridge to which the bi-directional switches

are connected are operate at carrier frequency and the devices in the other phase-leg are operate at modulating signal frequency. At any instant, only two devices are in conduction, which helps in reducing the conduction losses. Compared to CHB, T-type topology offers 24% reduction in switch count for five-level and 37.5% for nine-level. The per phase structure of T-type with three dc voltage sources is shown in Fig. 2.7 and the possible switching combinations to achieve seven-levels in phase-voltage is shown in Table 2.6.

From Fig. 2.7 and Table 2.6, it is observed that the T-type does not have switching redundancies and cannot operate with asymmetrical dc sources. Further, this topology does not facilitate even power distribution and produces unequal device blocking voltages. In Fig. 2.7, the maximum blocking voltage for S_5 and S_6 is $2V_{dc}$ and for switches in H-bridge is $3V_{dc}$.

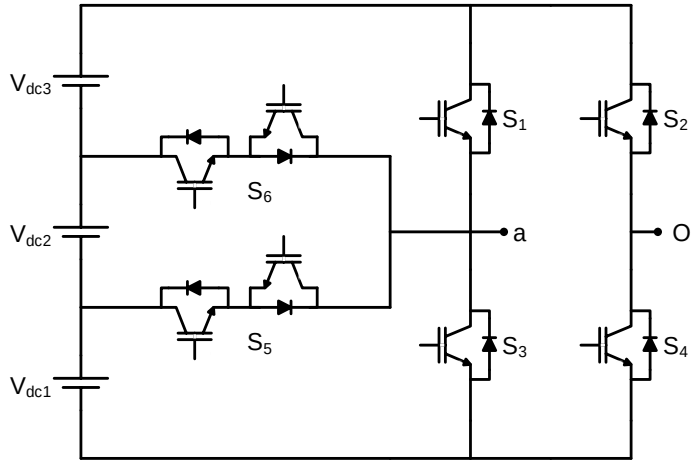


Fig. 2.7: Seven-level T-type RSC-MLI.

Table 2.6: Switching states of seven-level T-type RSC-MLI.

Num. of states	Voltage combinations	Switches in conduction	Output voltage
			$\mathbf{V_{dc1} = V_{dc2} = V_{dc3} = V_{dc}}$
1	$+(V_{dc1}+V_{dc2}+V_{dc3})$	S_1-S_4	$+3V_{dc}$
2	$+(V_{dc1}+V_{dc2})$	S_6-S_4	$+2V_{dc}$
3	$+V_{dc1}$	S_5-S_4	$+V_{dc}$
4	$-V_{dc3}$	S_6-S_2	$-V_{dc}$
5	$-(V_{dc2}+V_{dc3})$	S_5-S_2	$-2V_{dc}$
6	$-(V_{dc1}+V_{dc2}+V_{dc3})$	S_3-S_2	$-3V_{dc}$
7	0	(S_1-S_2) or (S_3-S_4)	0

2.4.5.2 Half-leg T-type RSC-MLI

A half-bridge based T-type topology [81, 82] acts as a viable alternative to active neutral pointed clamped (ANPC), neutral-point piloted (NPP) [83] and DCMLI topologies for medium-voltage, high-power applications. The dc link in this topology is common to all the phases and each phase-leg is connected to the dc link through bi-directional switches. With *n* identical sources, this topology involves (*n*–1) bi-directional and two uni-directional switches in each phase. This

topology can produce even and odd levels in phase-voltage and can be extended to higher levels by increasing the dc sources with bi-directional switches. In this topology, at any time, two devices are in conduction and leads to the reduction in conduction losses as compared to DCMLI. The structure of this topology for three-level is shown in Fig. 2.8 and its corresponding switching operation is given in Table 2.7.

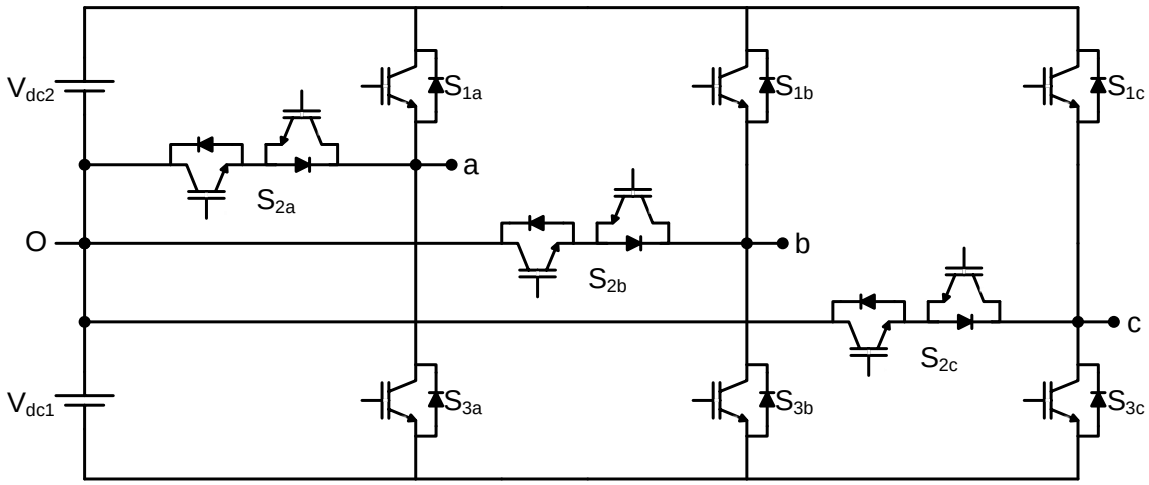


Fig. 2.8: Three-phase half-leg three-level T-type RSC-MLI.

Table 2.7: Switching states of three-level half-leg T-type RSC-MLI.

No. of states	**Voltage combinations**	**Switches in conduction**	**Output voltage: $V_{dc1} = V_{dc2} = V_{dc}$**
1	$+V_{dc1}$	S_1-S_2	$+V_{dc}$
2	0	S_2	0
3	$-V_{dc2}$	S_2-S_3	$-V_{dc}$

The voltage rating of bi-directional switches is lower than the devices in phase-leg. For example, with equal dc link voltages in Fig. 2.8, the maximum voltage rating of bi-directional switch is $V_{dc}/2$, whereas the devices in phase-leg are rated at V_{dc}. Thus, this topological configuration produce lower conduction losses and blocking voltages compared to DCMLI, NPP and ANPC. This topology is reported for various PV and grid connected applications [84]. Fault tolerant strategies and reconfiguration of this inverter for OC switch faults is also reported in [82]. Further, Table 2.7 shows that this topology does not possess switching redundancies, operates with unequal device blocking voltages, does not facilitate uniform power distribution and mandatorily requires dc voltage ratios to be symmetrical. However, the charge balance among the dc link voltages can be obtained by equalizing the rate of charge over a fundamental cycle [61] or by involving sophisticated modulation techniques such as space vector modulation (SVM).

2.4.5.3 Cascaded T-type RSC-MLI

T-type RSC-MLI can be extended to higher levels either by increasing the number of dc sources with bi-directional switches as shown in Fig. 2.7 or by cascading several T-type modules [60]. Connecting modules in cascade facilities the inverter to operate for both symmetrical and asymmetrical voltage ratios. However, dc link voltage ratio in an individual T-type module should be identical. The number of phase-voltage levels of this cascaded configuration depends on the number of levels in each T-type module.

Fig. 2.9 shows the cascaded T-type MLI with two five-level T-type modules and its corresponding switching operation is shown in Table 2.8. Cascading k number of symmetrical l-level T-type modules, produces $k(l–1)+1$ levels in phase-voltage. Assuming symmetrical voltage ratios, Fig. 2.9 (operates for k = 2 and l = 5) produces nine-levels in phase-voltage and its corresponding switching operation is shown in Table 2.8.

Switching redundancies shown in Table 2.8 verifies the ability of cascaded T-type RSC-MLI to facilitate equal load distribution among the cascaded modules. Further, operating Fig. 2.9 with binary (1: 2) voltage ratios, produces thirteen-levels in phase-voltage and its corresponding switching is shown in Table 2.8.

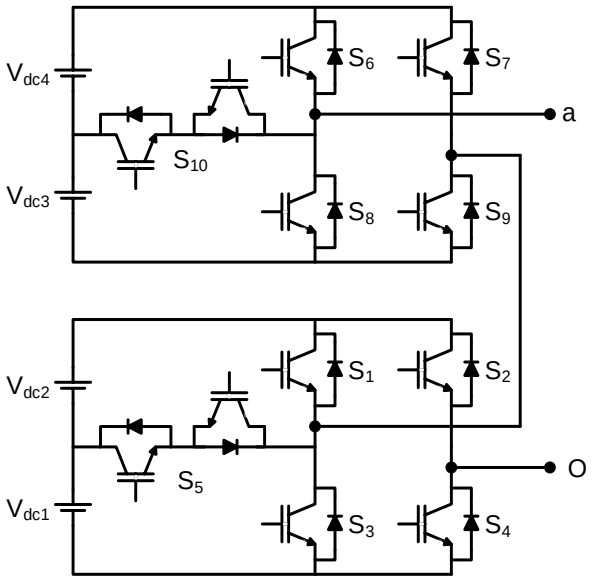


Fig. 2.9: Topological structure of cascaded T-type RSC-MLI.

Table 2.8: Switching states of cascaded T-type RSC-MLI.

Num. of states	Voltage combinations	Switches in conduction	Output voltage	
			Symmetrical	**Asymmetrical**
			9-level	**13-level**
			$\mathbf{V_{dc1} = V_{dc2} = V_{dc3} = V_{dc4} = V_{dc}}$	$\mathbf{V_{dc1} = V_{dc2} = V_{dc}}$ $\mathbf{V_{dc3} = V_{dc4} = 2V_{dc}}$
1	$+(V_{dc1}+V_{dc2}+V_{dc3}+V_{dc4})$	S_4-S_1-S_9-S_6	$+4V_{dc}$	$+6V_{dc}$
2	$+(V_{dc1}+V_{dc3}+V_{dc4})$	S_4-S_5-S_9-S_6	$+3V_{dc}$	$+5V_{dc}$
3	$+(V_{dc1}+V_{dc2}+V_{dc3})$	S_4-S_1-S_9-S_{10}	$+3V_{dc}$	$+4V_{dc}$
4	$+(V_{dc3}+V_{dc4})$	S_3-S_4-S_6- S_9	$+2V_{dc}$	$+4V_{dc}$
5	$+(V_{dc1}+V_{dc3})$	S_4-S_5-S_9-S_2	$+2V_{dc}$	$+3V_{dc}$
6	$+(V_{dc3}+V_{dc4}–V_{dc2})$	S_2-S_5-S_9-S_6	$+V_{dc}$	$+3V_{dc}$
7	$+V_{dc3}$	S_3-S_4-S_9-S_{10}	$+V_{dc}$	$+2V_{dc}$
8	$+(V_{dc1}+V_{dc2})$	S_4-S_1-S_9-S_8	$+2V_{dc}$	$+2V_{dc}$
9	$+V_{dc1}$	S_4-S_5-S_9-S_8	$+V_{dc}$	$+V_{dc}$
10	0	S_4-S_3-S_9-S_8 (or) S_2-S_1-S_7-S_6	0	0
11	$–V_{dc2}$	S_2-S_5-S_7-S_6	$–V_{dc}$	$–V_{dc}$
12	$–V_{dc4}$	S_2-S_1-S_7-S_{10}	$–V_{dc}$	$–2V_{dc}$
13	$–V_{dc3}–V_{dc4}+V_{dc1}$	S_4-S_5-S_7-S_8	$–V_{dc}$	$–3V_{dc}$
14	$–(V_{dc1}+V_{dc2})$	S_2-S_3-S_7-S_6	$–2V_{dc}$	$–2V_{dc}$
15	$–(V_{dc2}+V_{dc4})$	S_2-S_5-S_7-S_2	$–2V_{dc}$	$–3V_{dc}$
16	$–(V_{dc3}+V_{dc4})$	S_2-S_1-S_7-S_8	$–2V_{dc}$	$–4V_{dc}$
17	$–(V_{dc1}+V_{dc2}+V_{dc4})$	S_2-S_3-S_7-S_{10}	$–3V_{dc}$	$–4V_{dc}$
18	$–(V_{dc2}+V_{dc3}+V_{dc4})$	S_2-S_5-S_7-S_8	$–3V_{dc}$	$–5V_{dc}$
19	$–(V_{dc1}+V_{dc2}+V_{dc3}+V_{dc3})$	S_2-S_3-S_9-S_6	$–4V_{dc}$	$–6V_{dc}$

2.4.6 Multilevel module (MLM) based RSC-MLI

Multilevel module (MLM) based MLI is reported by E. Babaei in 2012 [85]. MLM RSC-MLI with three dc sources is shown in Fig. 2.10 This topology possess separate level and polarity generator and involves a congregation of bi-directional and uni-directional switches. The bi-directional switches are placed in level generator and uni-directional switches are in polarity generator. The level generator possess bi-directional voltage blocking and bi-directional current conducting capability, whereas the polarity generator have uni-directional voltage blocking and bi-directional current conducting capability. Level generator possess column based arrangement formed by interconnecting dc link voltages and bi-directional switches at multiple nodes. This topology is extended to higher levels by adding voltage sources with bi-directional switches. At any instant, one device in level generator and two devices in the polarity generator remains in conduction.

With *n* identical voltage sources, this topology involves (*n*+1) bi-directional switches in the level generator and four uni-directional switches in the polarity generator to produce a phase-voltage with (2*n*+1) levels. Operating MLM topology shown in Fig. 2.10 with equal voltages

produces seven-levels in phase-voltages and, its corresponding switching operation is given Table 2.9. From Table 2.9, it is evident that absence of switching redundancies, increases difficult to facilitate equal load sharing among the dc sources. Further, the structure of this topology does not allow asymmetrical voltages and operates the devices with non-uniform blocking voltages.

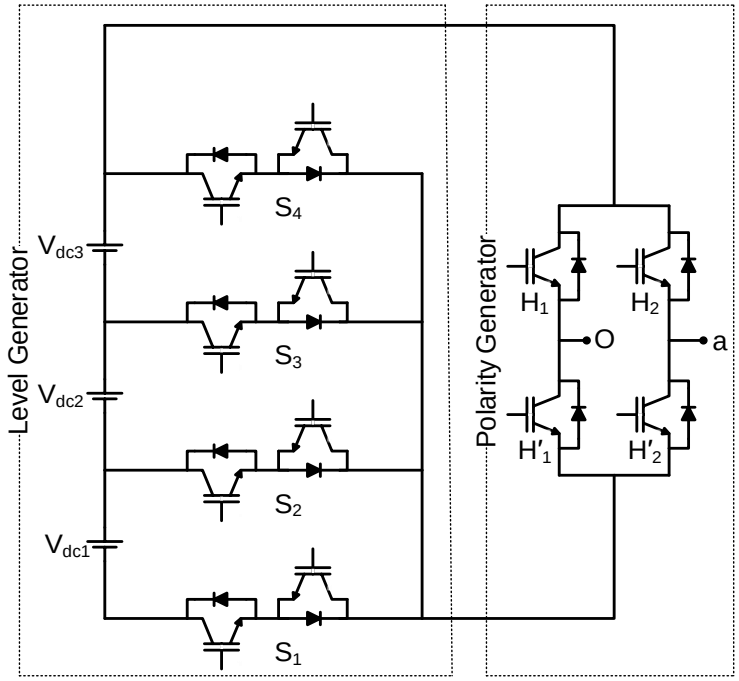


Fig. 2.10: Multilevel module (MLM) based RSC-MLI topology with three dc sources.

Table 2.9: Switching states of MLM based RSC-MLI.

Num. of states	Voltage combinations	Switches in conduction		Output voltage
		Level generator	Polarity generator	$V_{dc1} = V_{dc2} = V_{dc3} = V_{dc}$
1	$V_{dc1}+V_{dc2}+V_{dc3}$	S_1	H_1-H'_2	$+3V_{dc}$
2			H_2-H'_1	$-3V_{dc}$
3	$V_{dc2}+V_{dc3}$	S_2	H_1-H'_2	$+2V_{dc}$
4			H_2-H'_1	$-2V_{dc}$
5	V_{dc3}	S_3	H_1-H'_2	$+V_{dc}$
6			H_2-H'_1	$-V_{dc}$
7	0	S_4	H_1-H'_2	0
			H_2-H'_1	

2.4.7 Hybrid T-type RSC-MLI

This topology does not have a separate polarity or level generator and involves the combination of uni-directional and bi-directional switches. The uni-directional switches are connected to form a hexagon switch cell (HSC) structure and bi-directional switches are used to connect HSC to the dc link. In the other way, HSC structure is formed by back to back connection of two half-leg connected through a pair of uni-directional switching devices. This HSC structure permits the topology to operate for more switching combinations to obtain the required output

voltage. This topology is extended to higher levels by increasing the number of bi-directional switches. This topology resembles T-type, as its structure is similar to back to back connection of two half-leg T-type modules through a pair of uni-directional devices. Thus, this configuration can be called as hybrid T-type or improved T-type MLI and is reported by Shivam Prakash Gautam *et al*. in 2015. Based on the involvement and placing of bi-directional switches, two possible topological arrangements are reported [65, 66].

2.4.7.1 Topology – I

(*Hybrid T-type MLI with bi-directional switch on one side of HSC* [65, 66])

The topological structure of this MLI with two stiff dc sources V_{S1} and V_{R1} on either side of HSC is shown in the Fig. 2.11. Several dc link capacitors are connected across V_{S1} and these dc link capacitors are connected to HSC through bi-directional switches. These dc link capacitors shares voltage across V_{S1} equally. With n capacitors in dc link, this topology involves (n–1) bi-directional switches and six uni-directional switches. This topology with one bi-directional switch is shown in Fig. 2.11. Further, extension of this topology by increasing the bi-directional switches and by cascading several modules is shown in Fig. 2.12(a) and (b) respectively.

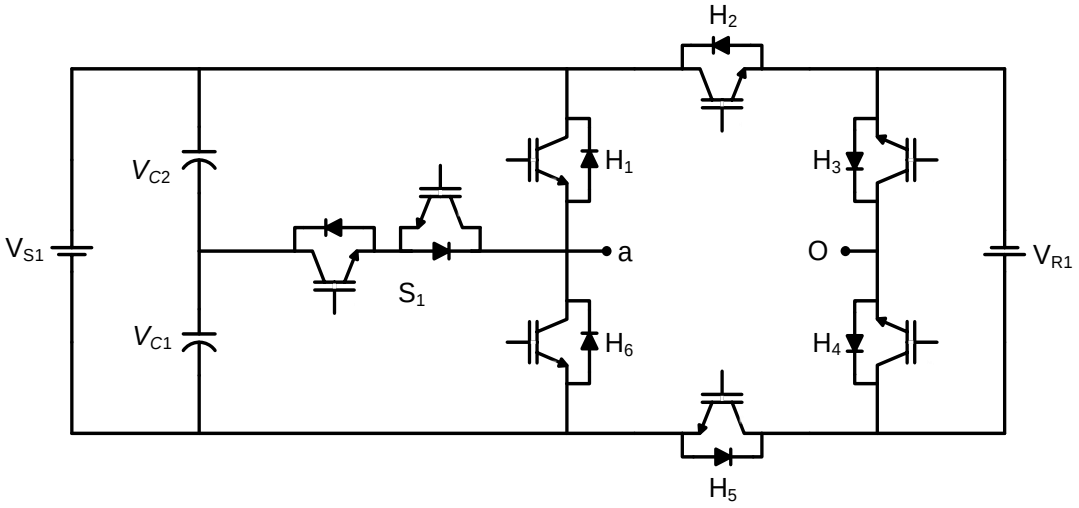


Fig. 2.11: Hybrid T-type MLI topology – I.

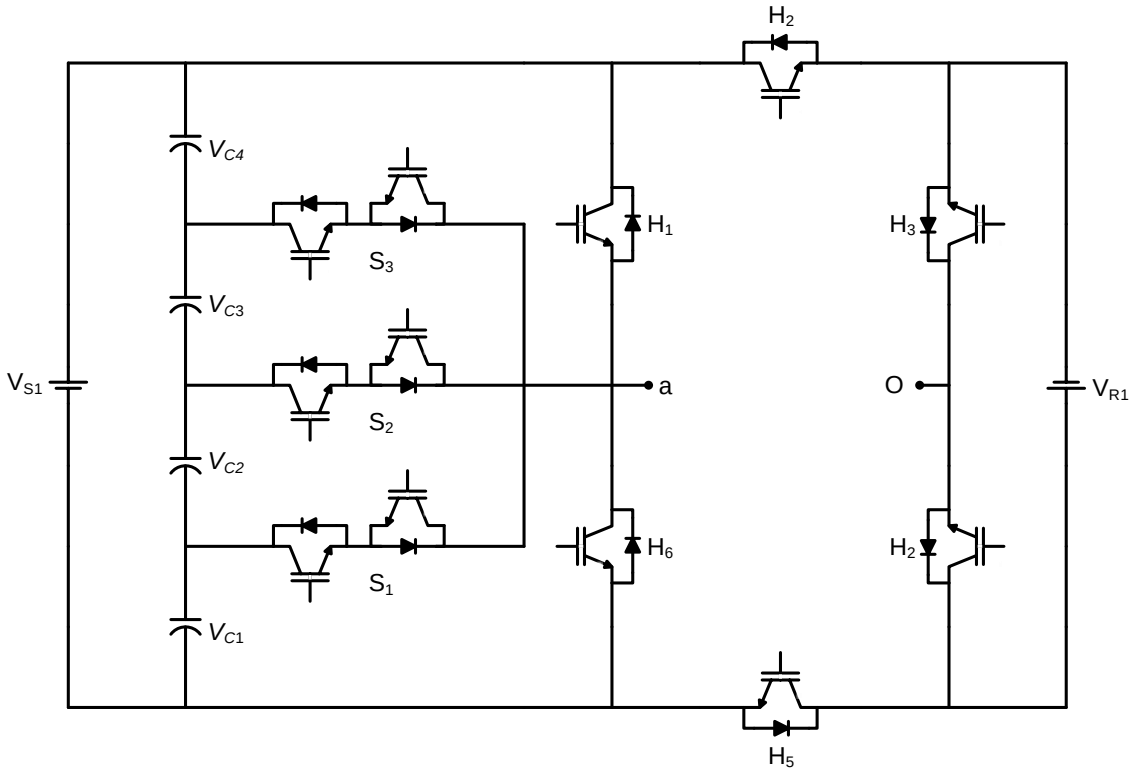
From Fig. 2.11, it is observed that short circuiting uni-directional switches H_5 and H_2 and, open circuiting voltage source V_{R1} in Fig. 2.11, makes this topology identical to five-level T-type MLI presented in Section 2.4.5.1. Thus, the addition of uni-directional switches modifies the H-bridge to HSC and, facilitates the topology to operate for asymmetrical configurations.

Further, for $V_{S1} = V_{R1}$, the configuration shown in Fig. 2.11 operates as symmetrical MLI and is asymmetrical if $V_{S1} \neq V_{R1}$. Symmetrical configuration of this topology with n dc link capacitors can produce $4n$+1 levels in phase-voltage, that means the inverter can be operated for 9, 13, 17, 21…. levels. Thus to operate the inverter for other voltage levels, asymmetrical configuration with appropriate voltage ratios should be selected.

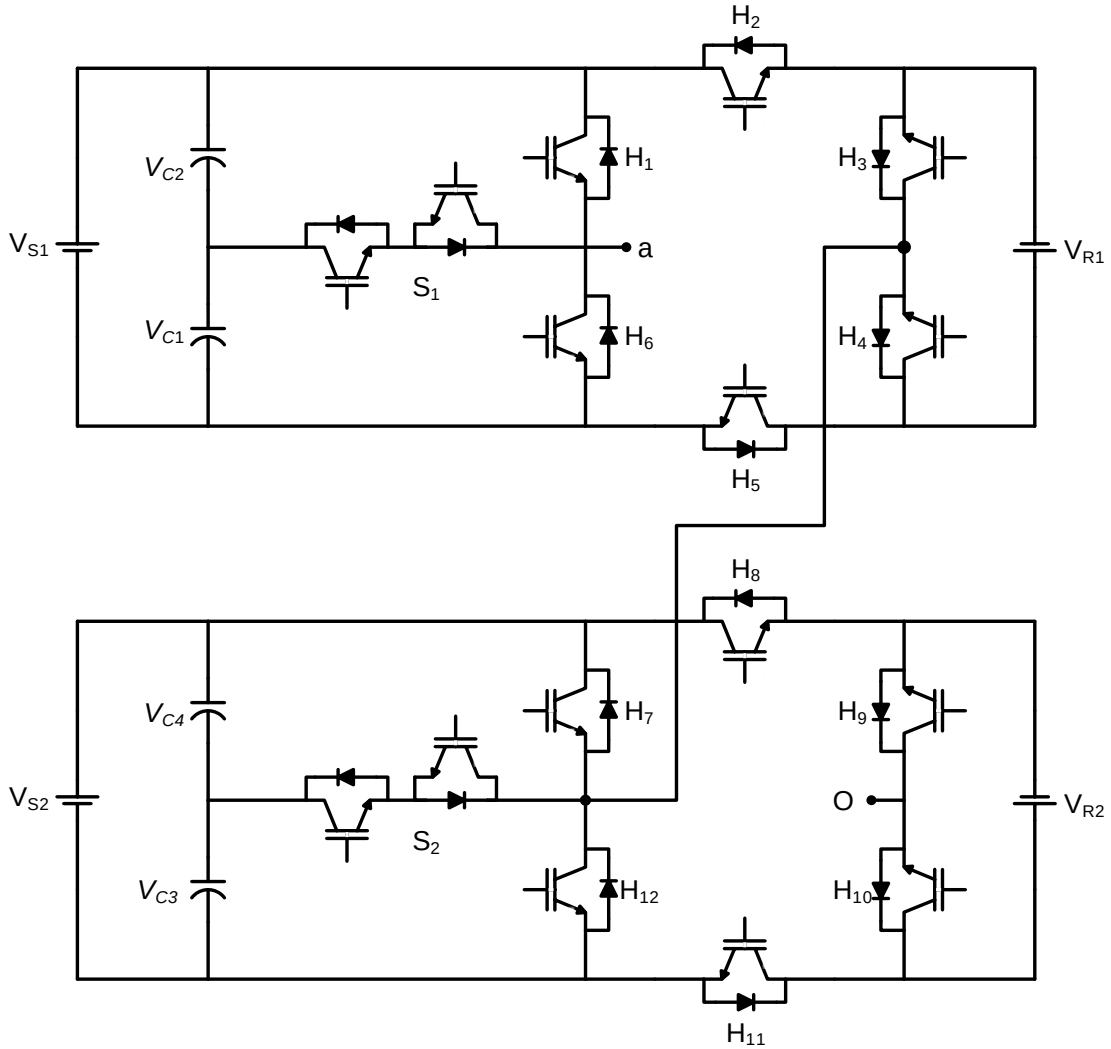
For instance, considering $V_{S1} = V_{R1} = 2V_{dc}$ in Fig. 2.11, then $V_{C1} = V_{C2} = V_{S1}/2 = V_{dc}$ and the inverter operates for nine-level as given in Table 2.10. If $V_{S1} = 2V_{R1} = 2V_{dc}$, Fig. 2.11 produces seven-level in phase-voltage with magnitude varying from $+3V_{dc}$ to $-3V_{dc}$ as shown in Table 2.10. Further, switching operation of this topology with $V_{S1} = \frac{2}{3} V_{R1} = 2V_{dc}$ in Fig. 2.11, produces eleven-levels in phase-voltage as given in Table 2.10. Cascaded structure of this topology with two hybrid T-type modules (one bi-directional switch in each) is shown in Fig. 2.12. Thus, cascading two-modules with n dc link capacitors in each, then topological configuration of this inverter requires $2(n-1)$ bi-directional switches and 12 uni-directional switches.

Table 2.10: Switching states of hybrid T-Type topology – I.

Num. of states	**Voltage combinations (V_{C1}, V_{C2}, V_{R1})**	**Switches in conduction**	**Output voltage**		
			Symmetrical	**Asymmetrical**	
			Nine-level $V_{S1} = 2V_{dc}$ $V_{R1} = 2V_{dc}$ ($V_{C1} = V_{C2} = V_{dc}$)	**Seven-level** $V_{S1} = 2V_{dc}$ $V_{R1} = V_{dc}$ ($V_{C1} = V_{C2} = V_{dc}$)	**Eleven-level** $V_{S1} = 2V_{dc}$ $V_{R1} = 3V_{dc}$ ($V_{C1} = V_{C2} = V_{dc}$)
1	$+(V_{C1}+V_{C2}+V_{R1})$	H_3-H_5-H_1	$+4V_{dc}$	$+3V_{dc}$	$+5V_{dc}$
2	$+(V_{R1}+V_{C1})$	H_3-H_5-S_1	$+3V_{dc}$	$+2V_{dc}$	$+4V_{dc}$
3	$+(V_{C1}+V_{C2})$	H_4-H_5-H_1	$+2V_{dc}$	$+2V_{dc}$	$+3V_{dc}$
4	$+V_{R1}$	H_3-H_5-H_6	$+2V_{dc}$	$+V_{dc}$	$+2V_{dc}$
5	$+V_{C1}$	H_4-H_5-S_1	$+V_{dc}$	$+V_{dc}$	$+V_{dc}$
6	0	H_4-H_5-H_6	0	0	0
7	$-V_{C2}$	H_3-H_2-S_1	$-V_{dc}$	$-V_{dc}$	$-V_{dc}$
8	$-V_{R1}$	H_4-H_2-H_1	$-2V_{dc}$	$-V_{dc}$	$-2V_{dc}$
9	$-(V_{C1}+V_{C2})$	H_3-H_2-H_6	$-2V_{dc}$	$-2V_{dc}$	$-3V_{dc}$
10	$-(V_{R1}+V_{C2})$	H_3-H_2-S_1	$-3V_{dc}$	$-2V_{dc}$	$-4V_{dc}$
11	$-(V_{C1}+V_{C2}+V_{R1})$	H_4-H_2-H_6	$-4V_{dc}$	$-3V_{dc}$	$-5V_{dc}$



(a) Increasing number of levels without cascading



(b) Increasing number of levels with cascading

Fig. 2.12: Extension of hybrid T-type topology – I to higher levels.

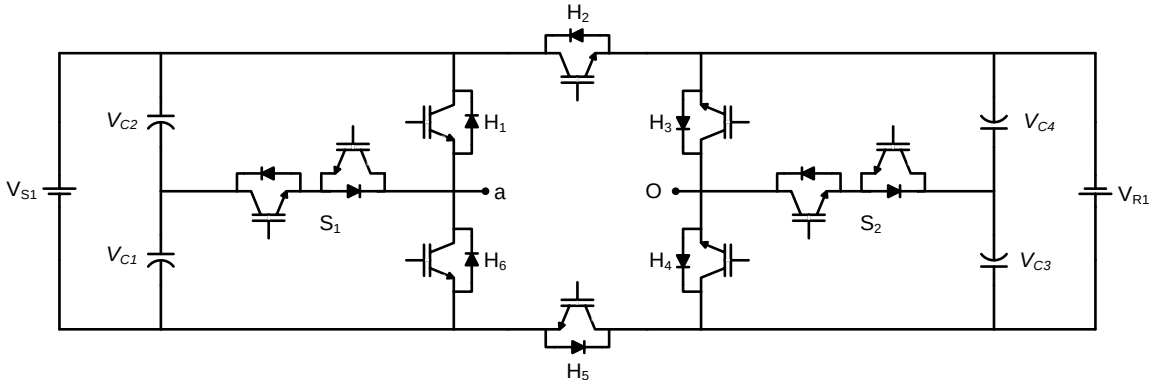
2.4.7.2 Topology – II

(*Hybrid T-type MLI with bi-directional switches on either side of HSC* [65, 66])

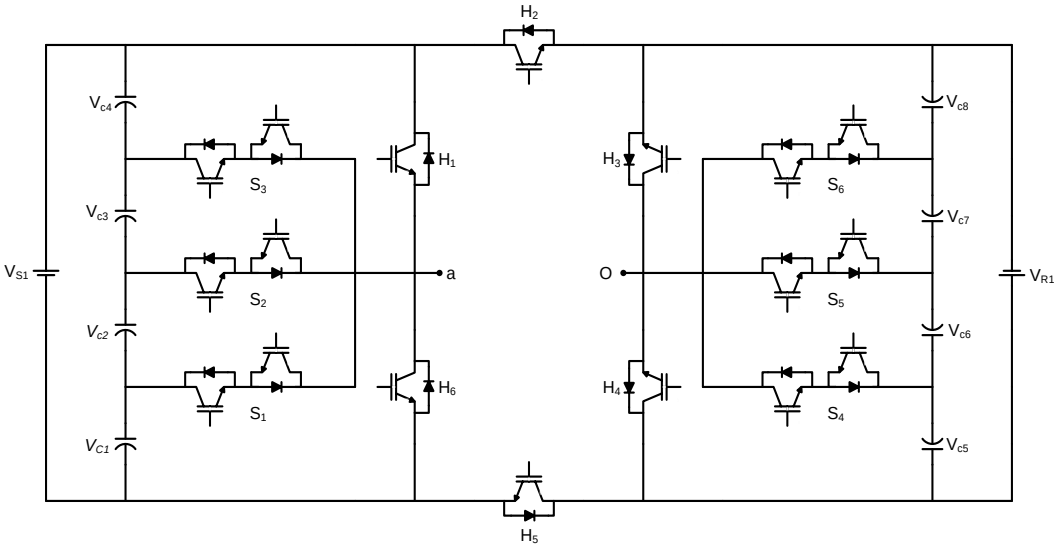
This configuration is similar to Topology-I presented above, but interconnects both sides of HSC to dc link through bi-directional switches as shown in Fig. 2.13. Involving bi-directional switches on both sides of HSC increases asymmetrical ability of the inverter and enables to obtain voltage levels with significant reduction in switch count. However, the remaining features and operation of this topology remains to be similar as Topology – I.

With n capacitors with equal voltage ratios in each set of dc link, this topology involves $2(n-1)$ bi-directional switches and six uni-directional switches and produces $4n+1$ levels in phase-voltage. From Fig. 2.13, it is observed that this topology is obtained by connecting two half-leg T-type RSC-MLIs in anti-parallel through a pair of uni-directional switches. Topological configuration of this topology with one bi-directional switch on either side of HSC is shown in Fig. 2.13(a). Extension of this topology by increasing bi-directional switches is shown in Fig. 2.13(b).

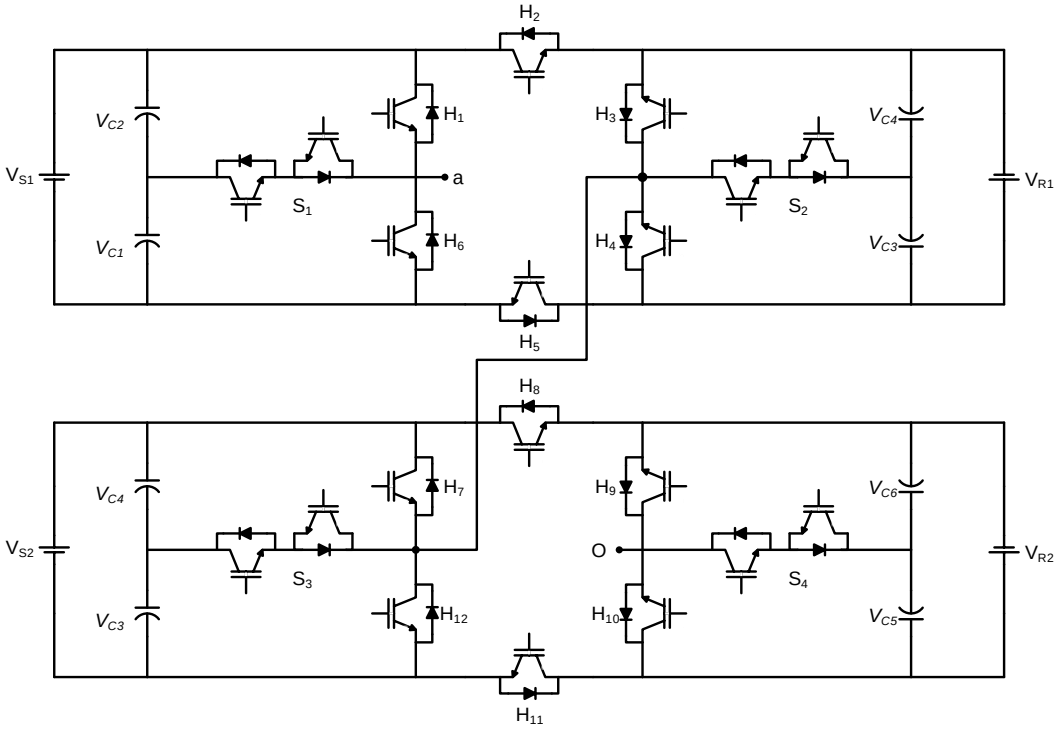
Further extension of Fig. 2.13(a), through cascading multiple modules is shown in Fig. 2.13(c). Switching combinations of Fig. 2.13(a) for symmetrical and asymmetrical voltage ratios is given in Table 2.11. From Table 2.11, it is evident that, with $V_{C1} = V_{C2} = V_{S1}/2$ and $V_{C3} = V_{C4} = V_{R1}/2$ Fig. 2.13(a) operates as a nine-level inverter. Further selecting, $V_{S1} = V_{dc}$ and $V_{R1} = 2V_{dc}$, produces thirteen-level asymmetrical inverter with magnitude varying from $+3V_{dc}$ to $-3V_{dc}$. Their corresponding switching operation is shown in Table 2.11. Therefore, both the topologies of hybrid T-type are highly flexible to operate with symmetrical and asymmetrical dc voltage ratios and possess appreciable reduction in switch count.



(a) Single module



(b) Increasing number of levels without cascading



(c) Increasing number of levels with cascading

Fig. 2.13: Hybrid T-type MLI topology – II.

Table 2.11: Switching states of hybrid T-type topology – II.

Num. of states	Voltage combinations $V_{C1}= V_{C2}= \frac{V_{S1}}{2}$ $V_{C3} = V_{C4} = \frac{V_{R1}}{2}$	Switches in conduction	Output voltage	
			Symmetrical	Asymmetrical
			Nine-level	Thirteen-level
			$V_{S1}= 2V_{dc}$ $V_{R1} = 2V_{dc}$ $V_{C1}= V_{C2} = V_{dc}$ $V_{C1}= V_{C2} = V_{dc}$	$V_{S1} = V_{dc}$ $V_{R1} = 2V_{dc}$ $V_{C1}= V_{C2} = \frac{V_{dc}}{2}$ $V_{C3} = V_{C4} = V_{dc}$
1	$+(V_{C1}+V_{C2}+V_{C3}+V_{C4})$	H_3-H_5-H_1	$+4V_{dc}$	$+3V_{dc}$
2	$+(V_{C1}+V_{C3}+V_{C4})$	H_3-H_5-S_1	$+3V_{dc}$	$+(5/2)V_{dc}$
3	$+(V_{C3}+V_{C1}+V_{C2})$	S_2-H_5-H_1	$+3V_{dc}$	$+2V_{dc}$
4	$+(V_{C3}+V_{C4})$	H_3-H_5-H_6	$+2V_{dc}$	$+2V_{dc}$
5	$+(V_{C3}+V_{C1})$	S_2-H_5-S_1	$+2V_{dc}$	$+(3/2)V_{dc}$
6	$+V_{C3}$	S_2-H_5-H_6	$+V_{dc}$	$+V_{dc}$
7	$+(V_{C1}+V_{C2})$	H_4-H_5-S_1	$+2V_{dc}$	$+V_{dc}$
8	$+V_{C1}$	H_4-H_5-S_1	$+V_{dc}$	$+(1/2)\ V_{dc}$
9	0	H_3-H_2-H_1 (or) H_4-H_5-H_6	0	0
10	$-V_{C2}$	H_3-H_2-S_1	$-V_{dc}$	$-(1/2)V_{dc}$
11	$-(V_{C1}+V_{C2})$	H_3-H_2-H_6	$-2V_{dc}$	$-V_{dc}$
14	$-V_{C4}$	S_2-H_2-H_1	$-V_{dc}$	$-V_{dc}$
15	$-(V_{C2}+V_{C4})$	S_2-H_2-S_1	$-2V_{dc}$	$-(3/2)V_{dc}$
13	$-(V_{C3}+V_{C4})$	H_4-H_2-H_1	$-2V_{dc}$	$-2V_{dc}$
12	$-(V_{C1}+V_{C2}+V_{C4})$	S_2-H_2-H_6	$-3V_{dc}$	$-2V_{dc}$
16	$-(V_{C2}+V_{C3}+V_{C4})$	H_4.H_2-S_1	$-3V_{dc}$	$-(5/2)V_{dc}$
17	$-(V_{C1}+V_{C2}+V_{C3}+V_{C4})$	H_4-H_2-H_6	$-4V_{dc}$	$-3V_{dc}$

2.4.8 Cascaded bipolar switched cells (CBSC) based RSC-MLI

Cascaded bipolar switched cells (CBSC) based RSC-MLI involves bi-directional switches and is reported by E. Babaei in 2008 [69]. This is a modular topology with column based physical structure and connects bi-directional switches on either side of dc link at multiple nodes. This topology does not involve a separate polarity or level generator and extended to higher levels by connecting a pair of bi-directional switches with an additional voltage source. The circuit configuration of CBSC with three dc sources is shown in Fig. 2.14 and its corresponding switching operation for symmetrical and asymmetrical voltage ratios for producing seven and thirteen-levels in phase-voltage is given in Table 2.12. With *n* identical sources in the dc link, this topology involving 2(*n*+1) bi-directional switches and produces 2*n*+1 levels. Even though each bi-directional

switch have two IGBTs, the total number of gate drivers are equal to the number of bi-directional switches. This results in reduction in cost and overall complexity of the control circuit.

From Table 2.12, it is evident that this topology produces the output voltage levels for additive combinations of dc sources and does not have sufficient redundancies to facilitate equal utilization of input dc sources.

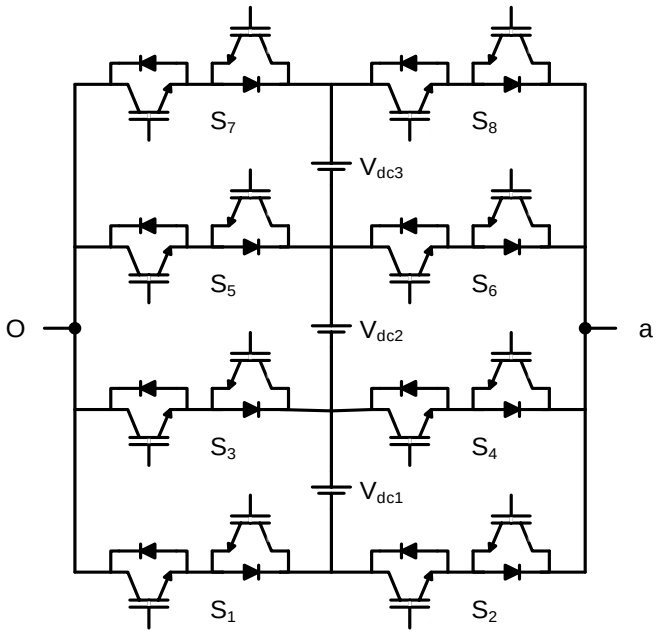


Fig. 2.14: Cascaded bipolar switched cells (CBSC) RSC-MLI with three dc sources.

Table 2.12: Switching states of CBSC RSC-MLI.

Num. of states	**Voltage combinations**	**Switches in conduction**	**Output voltage**	
			Symmetrical	**Asymmetrical**
			$V_{dc1} = V_{dc2} = V_{dc3} = V_{dc}$	**$V_{dc1} = V_{dc}$ $V_{dc2} = 3V_{dc}$ $V_{dc3} = 2V_{dc}$**
1	$+ (V_{dc1}+V_{dc2}+V_{dc3})$	S_1-S_8	$+ 3V_{dc}$	$+ 6V_{dc}$
2	$+ (V_{dc2}+V_{dc3})$	S_3-S_8	$+ 2V_{dc}$	$+ 5V_{dc}$
3	$+ (V_{dc1}+V_{dc2})$	S_1-S_6	$+ 2V_{dc}$	$+ 4V_{dc}$
4	$+V_{dc2}$	S_3-S_6	$+ V_{dc}$	$+ 3V_{dc}$
5	$+V_{dc3}$	S_5-S_8	$+ V_{dc}$	$+ 2V_{dc}$
6	$+V_{dc1}$	S_1-S_4	$+ V_{dc}$	$+ V_{dc}$
7	0	S_1-S_2	0	0
8	$- V_{dc1}$	S_2-S_3	$- V_{dc}$	$- V_{dc}$
9	$- V_{dc2}$	S_4-S_5	$- V_{dc}$	$- 2V_{dc}$
10	$- V_{dc3}$	S_6-S_7	$- V_{dc}$	$- 3V_{dc}$
11	$- (V_{dc1}+V_{dc2})$	S_2-S_5	$- 2V_{dc}$	$- 4V_{dc}$
12	$- (V_{dc2}+V_{dc3})$	S_4-S_7	$- 2V_{dc}$	$- 5V_{dc}$
13	$- (V_{dc1}+V_{dc2}+V_{dc3})$	S_2-S_7	$- 3V_{dc}$	$- 6V_{dc}$

In Fig. 2.14, for the considered symmetric combinations, outermost switches S_1, S_2, S_7 and S_8 need to block $3V_{dc}$. On the other hand, the inner switches S_3, S_4, S_5, and S_6 need block $2V_{dc.}$ Thus, the topological arrangement of this RSC-MLI produces unequal device blocking voltages and requires devices with different ratings. However, this configuration produces lower conduction losses as at instant two devices are in conduction. Inability of this topology to realize output for subtractive combinations of dc sources limits its asymmetrical capability.

CBSC can be extended to higher levels either by directly increasing the number of bi-directional switches or by connecting an additional CBSC module in cascade. These topologies are reported as cascaded CBSC topologies [69]. Cascaded CBSC configuration can produce voltage levels for both additive and subtractive combination of dc sources and can be implemented for both symmetrical and asymmetrical configurations.

2.4.9 Unit based RSC-MLIs

Few researchers reported some novel MLIs with fixed topological arrangement. Each unit of these topologies produces a fixed number of voltage levels such as five, nine, eleven and thirteen-levels and acts as an MLI itself. Further to extend the configuration to higher levels, these novel units are connected in an organized pattern such as cascade, series or parallel. Thus, these RSC-MLIs can produce only specific range of voltage levels. For a specific range of voltage levels, these unit based topologies possess appreciable reduction in switch count when compared to other RSC-MLI configurations. Few of such topologies are: Basic unit, envelope type (E-type), square T-type, and cascaded MLI (CMLI). In this thesis, this category of RSC-MLIs are grouped as unit based RSC-MLI. This section presents the topological configuration, switching operation, features, limitations, and applications of these unit based RSC-MLIs.

2.4.9.1 Basic unit RSC-MLI

This H-bridge based RSC-MLI is reported by Ebrahim Babaei in 2015 [86]. This RSC-MLI involves separate polarity and level generators. The topological arrangement of the basic unit RSC-MLI is shown in Fig. 2.15. The structure of level generator of this RSC-MLI has two parts i.e., three-cell structure and single-cell structure as shown in Fig. 2.15. Three cell structure involves three voltage sources connected through five uni-directional switches and single cell structure consists of one voltage and two uni-directional switches. The purpose of single-cell structure is to facilitate the voltage levels (missing levels in phase-voltage) that are not produced by three-cell structure. With symmetrical voltage ratios, level generator (operating both single and three-cell structures) produces five-level unipolar voltage as shown in Table 2.13. Processing the output of level generator through a polarity generator, produces nine-level phase-voltage. Table 2.13 shows that, this topology possess limited switching redundancies and produces unequal device blocking

voltages. To extend this RSC-MLI to higher levels, several basic units (with separate polarity and level generator in each module) are connected in cascade. However, to increase the voltage levels with appreciable reduction in switch count, several units of level generator (duplicating only three-cell structure) are connected in series followed by a common polarity generator as shown in Fig. 2.16.

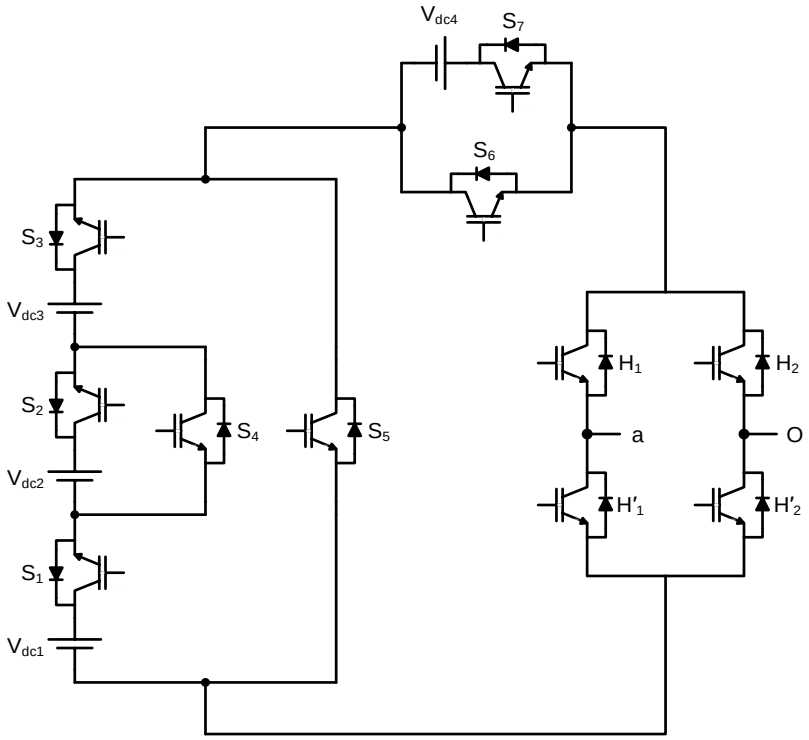


Fig. 2.15: Topological structure of basic unit RSC-MLI.

Table 2.13: Switching states of basic unit RSC-MLI.

Num. of states	**Voltage combinations**	**Devices in conduction**	**Output voltage $V_{dc1} = V_{dc2} = V_{dc3} = V_{dc}$**
1	$V_{dc1}+V_{dc2}+V_{dc3}+V_{dc4}$	S_1-S_2-S_3-S_7-H_1-H_2'	$+4V_{dc}$
2	$V_{dc1}+V_{dc3}+V_{dc4}$	S_1-S_4-S_3-S_7-H_1-H_2'	$+3V_{dc}$
4	$V_{dc1}+V_{dc2}+V_{dc3}$	S_1-S_2-S_3-S_6-H_1-H_2'	$+3V_{dc}$
5	$V_{dc1}+V_{dc3}$	S_1-S_4-S_3-S_6-H_1-H_2'	$+2V_{dc}$
6	V_{dc4}	S_5-S_7-H_1-H_2'	$+V_{dc}$
7	0	S_5-S_6-H_1-H_2' (or) S_5-S_6-H_2-H_1'	0

Operating Fig. 2.16 with equal voltage ratios produces multiple switching redundancies and facilitates uniform power distribution among the cascaded units. Referring to Fig. 2.16, three-cell structure of level generator can be called as modular unit and single cell structure as non-modular unit. Thus, with *n* identical modular units, Fig. 2.16 involves 5*n*+6 uni-directional switches, 3*n*+1 voltage sources, and produces 6*n*+3 levels in phase-voltage with voltage magnitude varying from

$(3n+1)V_{dc}$ to $-(3n+1)V_{dc}$. However, this configuration of RSC-MLI operates with limited redundancies and does not support asymmetric configuration with trinary voltage ratios. Further, operating Fig. 2.16 with binary voltage ratios, involves $5n+6$ uni-directional switches, $3n+1$ voltage sources and produces $6\left(2^n-1\right)+3$ levels in phase with output voltage magnitude of $\pm\left(3\left(2^n-1\right)+1\right)V_{dc}$.

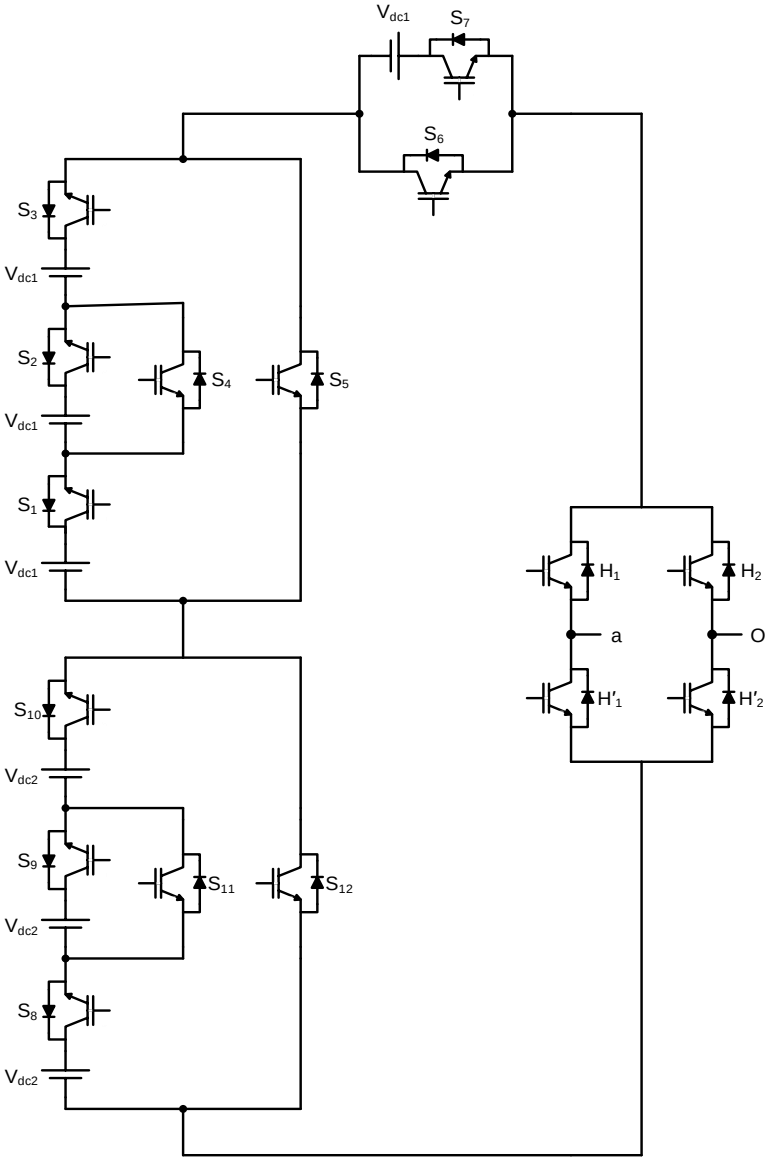
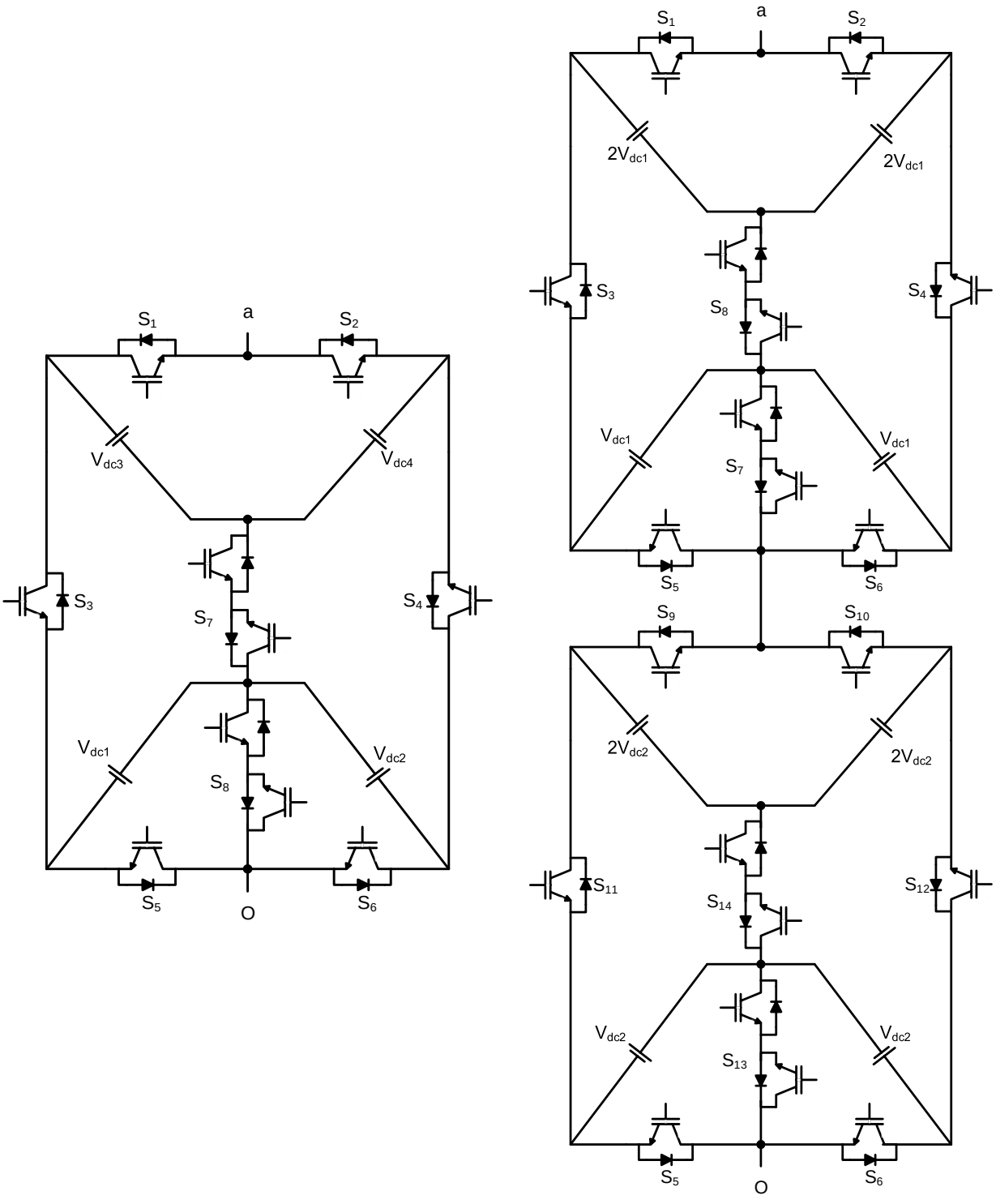


Fig. 2.16: Extension of basic unit RSC-MLI to higher levels.

2.4.9.2 Envelope type (E-type) RSC-MLI

Envelope-type (E-type) MLI is a unique modular and asymmetrical configuration proposed by Emad Samadaei in 2017 [64]. This RSC-MLI does not involve any separate polarity or level generator, and is extended to higher levels by connecting several E-type modules in series.

Topological configuration of this RSC-MLI is shown in Fig. 2.17, where Fig. 2.17(a) shows topological arrangement of each E-type unit and Fig. 2.17(b) shows its extension to higher levels.



(a) Each E-type module (b) Connecting two E-type modules

Fig. 2.17: Topological configuration of E-type RSC-MLI.

Each E-type unit possess a fixed topological structure by involving four dc sources with 1: 2 voltage ratio, two bi-directional and six uni-directional switches to produce thirteen-levels in phase-voltage. Thus, each unit of E-type MLI operates as a thirteen-level inverter itself and its

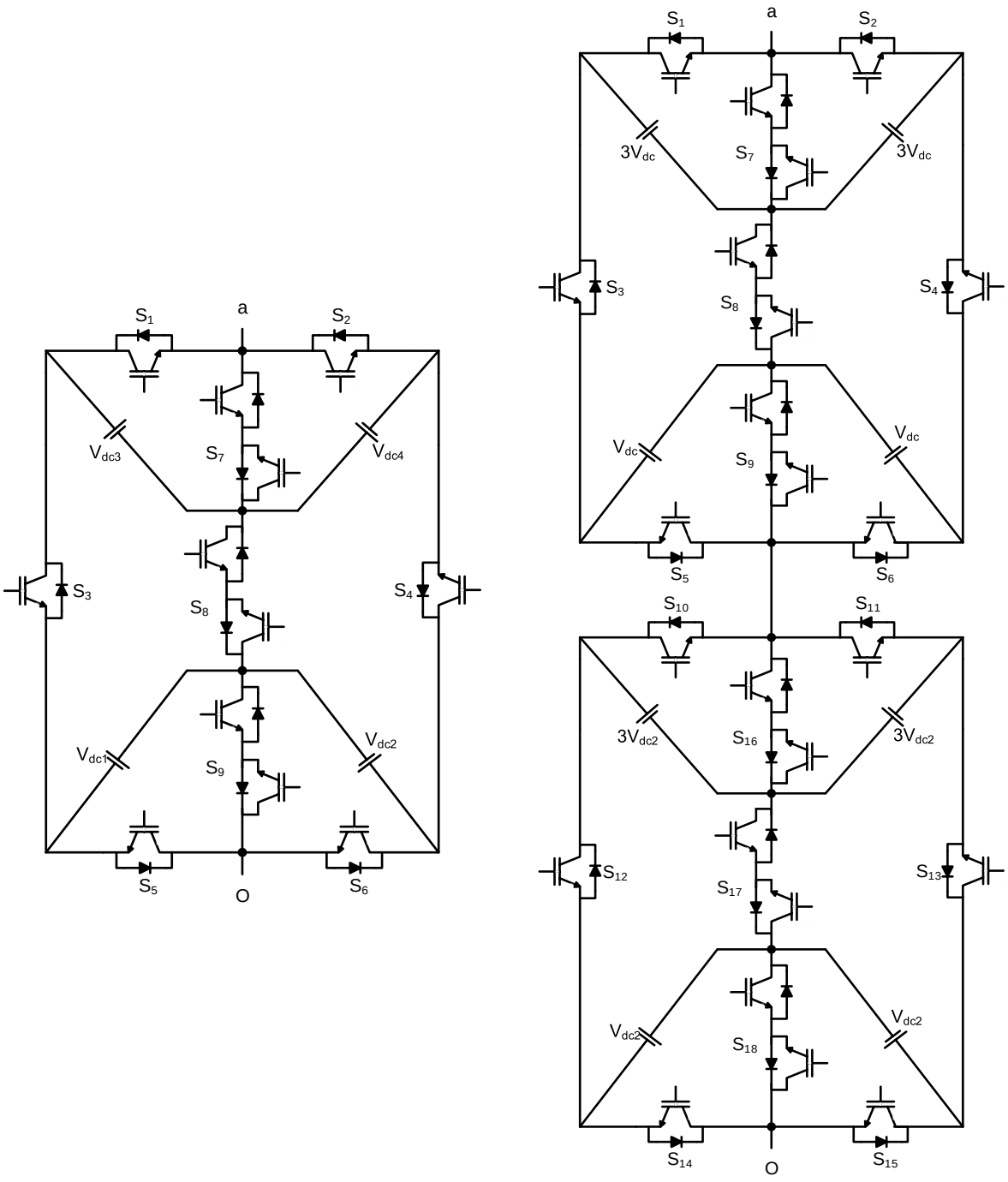
corresponding switching states are shown in Table 2.14. This RSC-MLI possess limited switching redundancies and produces unequal device blocking voltages. Considering *n* identical E-type units in series, Fig. 2.17(b) involves 6*n* uni-directional switches, 2*n* bi-directional switches, 4*n* dc sources and produces 12*n*+1 levels in phase-voltage.

Table 2.14: Switching states in a single unit of E-type RSC-MLI.

Num. of states	**Voltage combinations**	**Devices in conduction**	**Output voltage $V_{dc1}=V_{dc2}=V_{dc}$ $V_{dc3}=V_{dc4}=2V_{dc}$**
1	$V_{dc1}+V_{dc2}+V_{dc3}+V_{dc4}$	S_5-S_4-S_1	$+6V_{dc}$
2	$V_{dc2}+V_{dc3}+V_{dc4}$	S_8-S_4-S_1	$+5V_{dc}$
3	$V_{dc3}+V_{dc4}$	S_6-S_4-S_1	$+4V_{dc}$
4	$V_{dc1}+V_{dc3}$	S_5-S_7-S_1	$+3V_{dc}$
5	$V_{dc1}+V_{dc2}$	S_5-S_4-S_2	$+2V_{dc}$
6	V_{dc3}	S_8-S_7-S_1	$+2V_{dc}$
7	V_{dc2}	S_8-S_4-S_2	$+V_{dc}$
8	$V_{dc3}-V_{dc2}$	S_6-S_7-S_1	$+V_{dc}$
9	0	S_6-S_4-S_2 (or) S_5-S_3-S_1	0
10	$V_{dc4}-V_{dc1}$	S_5-S_7-S_2	$-V_{dc}$
11	V_{dc1}	S_8-S_3-S_1	$-V_{dc}$
12	$V_{dc1}+V_{dc2}$	S_6-S_3-S_1	$-2V_{dc}$
13	V_{dc4}	S_8-S_7-S_2	$-2V_{dc}$
14	$V_{dc2}+V_{dc4}$	S_6-S_7-S_2	$-3V_{dc}$
15	$V_{dc3}+V_{dc4}$	S_5-S_3-S_2	$-4V_{dc}$
16	$V_{dc1}+V_{dc3}+V_{dc4}$	S_8-S_3-S_2	$-5V_{dc}$
17	$V_{dc1}+V_{dc2}+V_{dc3}+V_{dc4}$	S_6-S_3-S_2	$-6V_{dc}$

2.4.9.3 Square T-type (ST-Type) RSC-MLI

Square T-type (ST-Type) RSC-MLI is inspired from E-type, where each basic unit acts as a seventeen-level inverter by itself [74]. As similar to E-type, this topology also possess a modular structure and increases phase-voltage levels by connecting multiple identical units in series. The basic unit of ST-Type RSC-MLI shown in Fig. 2.18(a) involves four dc voltages with 1: 3 voltage ratio and produces seventeen-levels in phase-voltage with six uni-directional and three bi-directional switches. The corresponding switching operation of ST-Type shown Fig. 2.18(a) is given in Table 2.15. To increase the number of levels, multiple ST-Type units are connected in series as shown in Fig. 2.18(b). Connecting *n* ST-Type units in series, this configuration involves 4*n* dc sources, 3*n* bi-directional switches, 6*n* uni-directional switches and produces 16*n*+1 levels in phase-voltage. However, this topology have the same limitations of E-type RSC-MLI such as unequal device blocking voltages and non-uniform power distribution among the dc sources.



(a) Each square T-type module

(b) Connecting two square T-type modules

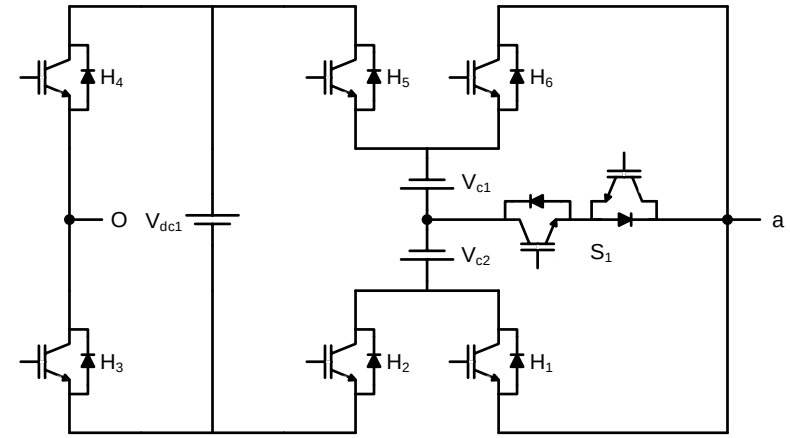
Fig. 2.18: Square T-type (ST-Type) RSC-MLI.

Table 2.15: Switching states in a unit of Square T-type (ST-Type) RSC-MLI.

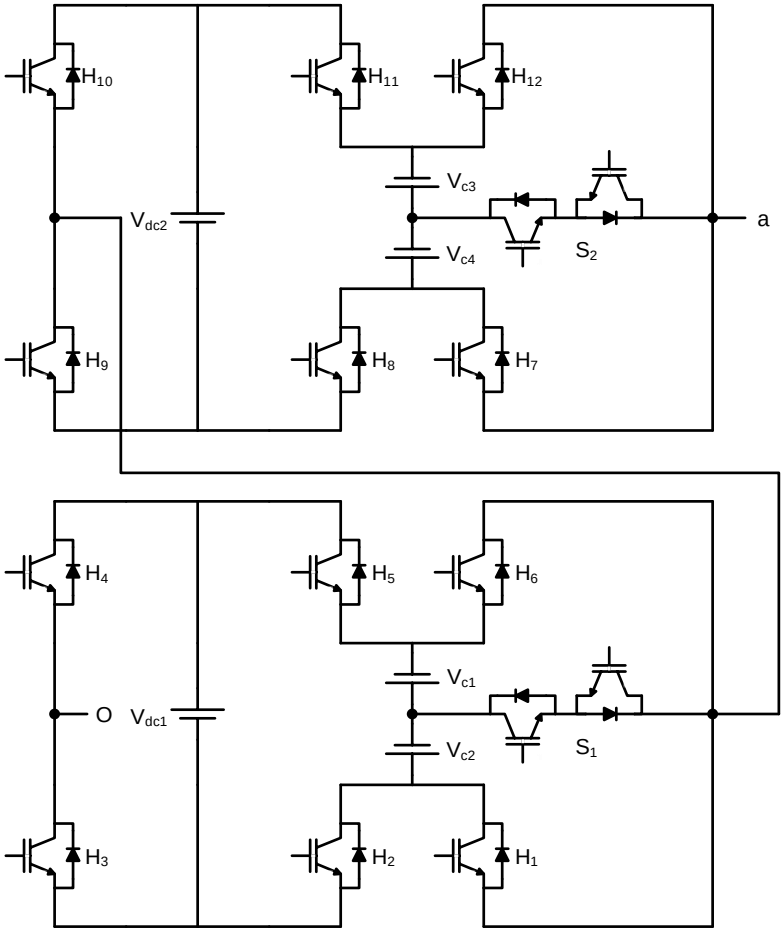
Num. of states	**Voltage combinations**	**Devices in conduction**	**Output voltage $V_{dc1} = V_{dc2} = V_{dc}$ $V_{dc3} = V_{dc4} = 3V_{dc}$**
1	$V_{dc1}+V_{dc2}+V_{dc3}+V_{dc4}$	S_5-S_4-S_1	$+8V_{dc}$
2	$V_{dc1}+V_{dc3}+V_{dc4}$	S_5-S_4-S_7	$+7V_{dc}$
3	$V_{dc1}+V_{dc2}$	S_5-S_4-S_2	$+6V_{dc}$
4	$V_{dc2}+V_{dc3}+V_{dc4}$	S_9-S_4-S_1	$+5V_{dc}$
5	$V_{dc2}+V_{dc4}$	S_9-S_4-S_7	$+4V_{dc}$
6	V_{dc2}	S_9-S_4-S_2	$+3V_{dc}$
7	$V_{dc3}+V_{dc4}$	S_6-S_4-S_1	$+2V_{dc}$
8	V_{dc3}	S_9-S_8-S_1	$+V_{dc}$
9	0	S_5-S_3-S_1 (or) S_6-S_4-S_2	0
10	V_{dc4}	S_9-S_8-S_2	$-V_{dc}$
11	$V_{dc3}+V_{dc4}$	S_5-S_3-S_2	$-2V_{dc}$
12	V_{dc1}	S_9-S_3-S_1	$-V_{dc}$
13	$V_{dc1}+V_{dc3}$	S_9-S_3-S_7	$-4V_{dc}$
14	$V_{dc1}+V_{dc3}+V_{dc4}$	S_9-S_3-S_2	$-5V_{dc}$
15	$V_{dc1}+V_{dc2}$	S_6-S_3-S_1	$-6V_{dc}$
16	$V_{dc1}+V_{dc2}+V_{dc3}$	S_6-S_3-S_7	$-7V_{dc}$
17	$V_{dc1}+V_{dc2}+V_{dc3}+V_{dc4}$	S_6-S_3-S_2	$-8V_{dc}$

2.4.9.4 Cascaded RSC-MLI: Topology – I

This topology is reported by Charles Ikechukwu O deh in 2015 [87]. Each unit of this RSC-MLI shown in Fig. 2.19(a) acts as a nine-level inverter. Further extension of this topology to higher levels is shown in Fig. 2.19(b). The topological arrangement of each unit of this RSC-MLI shown in Fig. 2.19(a) is similar to the Topology – I of hybrid T-type RSC-MLI. However, the topological structure of this RSC-MLI involves only stiff sources in dc link. This topology operates only with asymmetrical configuration, where in each basic unit, three dc sources (V_{dc1}, V_{c1} and V_{c2}) and 6 uni-directional and one bi-directional switches are involved. In any unit, V_{c1} and V_{c2} are arranged to form split voltage dc source structure. The voltage of these split dc sources (V_{c1} and V_{c2}) are equal and twice of V_{dc1}. This configuration produces unequal device blocking voltages and operates with limited switching redundancies.



(a) Basic unit



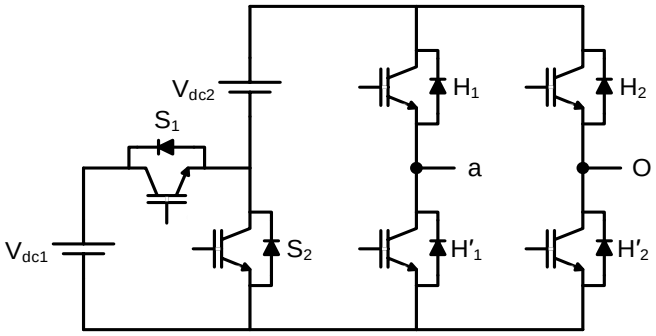
(b) Cascading two units

Fig. 2.19: Cascaded RSC-MLI Topology – I.

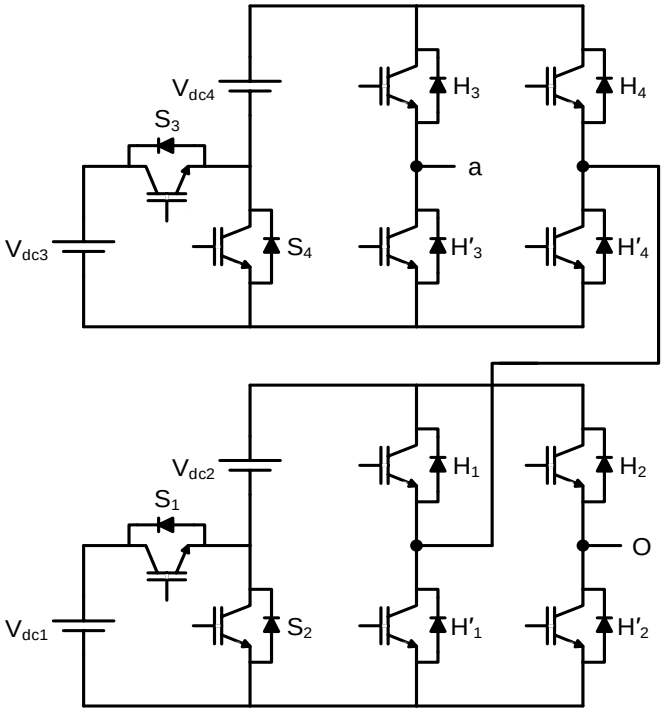
2.4.9.5 Cascaded RSC-MLI: Topology – II

This configuration of cascaded MLI is also reported by Charles Ikechukwu Odeh [88]. Each unit of this RSC-MLI produce five-levels in phase-voltage by involving six uni-directional switches and two identical dc sources. The topological structure is shown in Fig. 2.20. Topological structure of each unit of this RSC-MLI is shown in Fig. 2.20(a) and its corresponding switching operation is shown in Table 2.16. This RSC-MLI also operates with unequal device blocking voltages. Further

connecting multiple units in cascade as shown in Fig. 2.20(b), facilitates the inverter to operate with asymmetrical dc voltage ratios. Topological configuration of this RSC-MLI with two units (shown in Fig. 2.20(b)) produces nine-levels in phase-voltage. With *n* identical units in cascade, Fig. 2.20(b) requires 6*n* uni-directional switches, 2*n* dc sources and produces 4*n* + 1 levels in phase-voltage.



(a) Basic unit



(b) Cascading two units

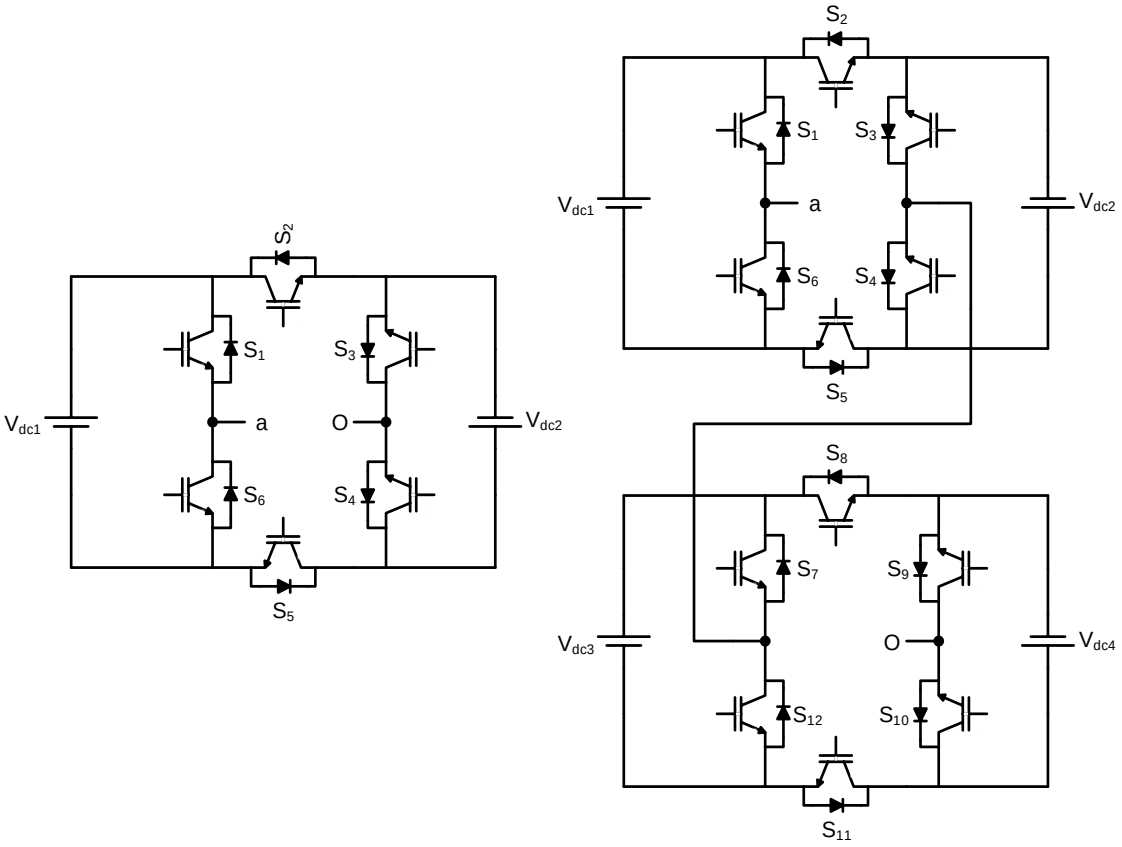
Fig. 2.20: Cascaded MLI Topology – II.

Table 2.16: Switching states of five-level cascaded MLI toplogy – II.

Num. of states	**Voltage combinations**	**Devices in conduction**	**Output voltage $V_{dc1} = V_{dc2} = V_{dc}$**
1	$V_{dc1}+V_{dc2}$	S_1-H_1-H_2'	$+2V_{dc}$
2	V_{dc2}	S_2-H_1-H_2'	$+V_{dc}$
3	0	H_1-H_2 (or) H_1'-H_2	0
4	$-V_{dc2}$	S_2-H_2-H_1'	$-V_{dc}$
5	$-(V_{dc1}+V_{dc2})$	S_1-H_2-H_1'	$-2V_{dc}$

2.4.9.6 Cascaded RSC-MLI with HSC

This HSC based RSC-MLI is reported by E. Babaei in 2014 [67, 68]. The topological configuration of the proposed RSC-MLI is shown in Fig. 2.21. Circuit configuration of each unit of this RSC-MLI is shown in Fig. 2.21(a) and its cascaded configuration is shown in Fig. 2.21(b).



(a) Basic unit (b) Cascading two units

Fig. 2.21: Cascaded RSC-MLI with HSC based structure.

Each unit of this RSC-MLI involves two dc sources interconnected with six uni-directional switches and forms an HSC structure (as explained in section 2.4.7.1). Each HSC unit can operate with symmetrical and asymmetrical voltage ratios and, obtains the voltage levels for additive combinations of the dc sources. With equal voltage ratios, each unit of this cascaded RSC-MLI shown in Fig. 2.21(a) operates as five-level inverter and its corresponding switching operating is shown in Table 2.17. This RSC-MLI produces unequal device blocking voltages, where in Fig. 2.21(a) the blocking voltage of switches S_1 and S_2 is V_{dc1}; S_3 and S_4 is V_{dc2}; S_5 and S_6 is V_{dc1}+V_{dc2}. Extension of this MLI to higher levels by cascading two basic units is shown in Fig. 2.21(b). This cascade configuration can be operated with asymmetrical dc voltages as well. With n HSC units in cascade (symmetrical), this RSC-MLI involves $6n$ uni-directional switches, $2n$ dc sources and produces $4n$+1 levels in phase-voltage, with magnitude varying from $+2nV_{dc}$ to $-2nV_{dc}$. The total blocking voltage of this symmetrical cascaded RSC-MLI is $8nV_{dc}$.

Table 2.17: Switching states of H-bridge based basic unit.

Num. of states	Voltage combinations	Devices in conduction	Output voltage $V_{dc1} = V_{dc2} = V_{dc}$
1	$V_{dc1}+V_{dc2}$	H_3-H_5-H_1	$+2V_{dc}$
2	V_{dc2}	H_5-H_6-H_3	$+V_{dc}$
3	V_{dc1}	H_1-H_4-H_5	$+V_{dc}$
4	0	H_1-H_2-H_3 (or) H_4-H_5-H_6	0
5	V_{dc1}	H_6-H_2-H_3	$-V_{dc}$
6	V_{dc2}	H_1-H_2-H_4	$-V_{dc}$
7	$V_{dc1}+V_{dc2}$	H_4-H_2-H_6	$-2V_{dc}$

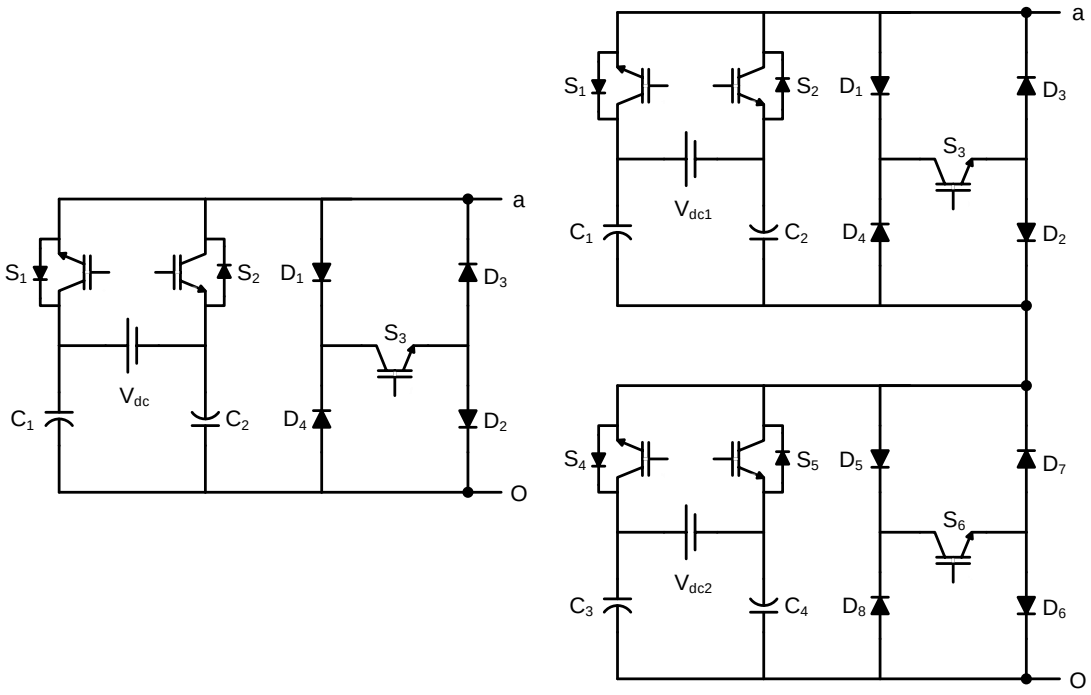
2.4.10 Switched capacitor topologies

To address the issue of voltage unbalance among the dc link capacitors and reduce the requirement of input dc sources, few RSC-MLIs are reported with switched capacitor topologies. These topologies possess modular structure with novel capacitor based units connected in organized pattern such as series, parallel or cascade. These topologies produce the desired voltage levels ensuring charge balance of dc link capacitors by switching in series/parallel combinations. In this thesis, these RSC-MLIs are categorised as switched capacitor topologies and popular configurations under this category are explained below.

2.4.10.1 Spilt capacitor unit RSC-MLI

To facilitate uniform device blocking voltages and to equalize the rate of charge/discharge of dc link capacitors, Reza Barzegarkhoo reported this modular topology with split capacitor unit [89]. Each unit, shown in Fig. 2.22(a) involves three uni-directional switches, four diodes, two capacitors and one stiff dc voltage source. The dc link capacitors are arranged to form a spilt capacitor structure across the dc voltage source, which charges each capacitor to half of the dc source voltage. Further, operating S_1, S_2 and S_3, each of the split capacitor unit produces three voltage levels (positive, negative and zero) as shown in Table 2.18. However, it is to be noted that, the considered dc voltage source will not directly involves in the load current paths, and is only responsible for charging the capacitors. Cascading of two units to extend the inverter to higher levels is shown in Fig. 2.22(b).

Further cascading n identical units, this RSC-MLI require $3n$ uni-directional switches, n dc sources, $4n$ diodes and $2n$ capacitors to produce $2n+1$ levels in phase-voltage. However, in Fig. 2.22(a) replacing the arrangement of diode bridge and uni-directional switch S_3, with a bi-directional switch, reduces the device count to $2n$ uni-directional switches, n bi-directional switches and $2n$ capacitors to produce $2n+1$ levels in phase-voltage with phase-magnitude varying from $+(n/2)V_{dc}$ to $-(n/2)V_{dc}$. Further, this configuration is valid for asymmetrical configuration (for binary and trinary dc voltage ratios) as well.



(a) Basic unit (b) Cascading two units

Fig. 2.22: Split capacitor unit RSC-MLI.

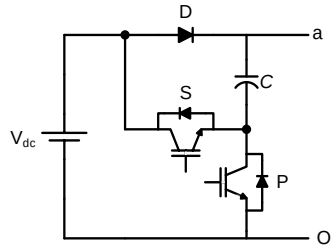
Table 2.18: Switching states of spilt capacitor unit RSC-MLI.

Num. of states	**Voltage combinations**	**Devices in conduction**	**Output voltage** $\mathbf{V_{C1} = V_{dc}/2}$ $\mathbf{V_{C2} = -V_{dc}/2}$
1	V_{C1}	S_1	$+V_{dc}/2$
2	0	S_1-S_3	0
3	0	S_2-S_3	0
4	V_{C2}	S_2	$-V_{dc}/2$

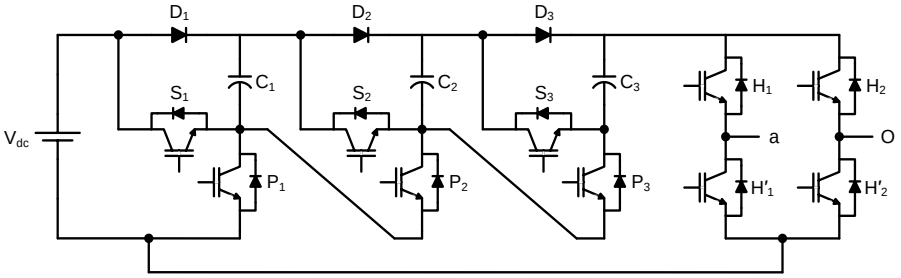
2.4.10.2 Switched capacitor RSC-MLI

Ebrahim Babaei reported a RSC-MLI with novel switched capacitor based unit in 2014 [90]. The objective of this topology is to obtain multilevel output voltage by operating the inverter in boost mode with efficient balance of dc link voltages. The circuit diagram of switched capacitor unit is shown in Fig. 2.23(a), where each unit involves one power diode, a complimentary pair of uni-directional switches (*P* and *S*), one capacitor and one stiff dc source. In any unit, if *P* is ON (*S* is OFF), capacitor (*C*) charges to V_{dc} through the power diode *D* and produces an output voltage of V_{dc}. When *S* is ON, *D* becomes reverse biased and *C* starts discharging to load, producing an output voltage of $2V_{dc}$. Further, connecting *n* units in series and energizing through one stiff dc source is shown in Fig. 2.23(b). For this configuration, switching of *S* and *P* connects the capacitor in series and parallel with the dc voltage source (V_{dc}) and controls the rate of charge and discharge of the capacitors. This will produce an output voltage varying from $+V_{dc}$ to $+nV_{dc}$. Negative and zero-voltage levels are obtained from H-bridge.

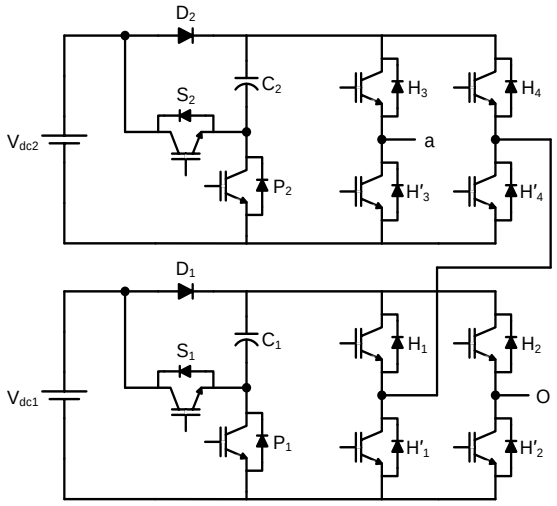
The circuit diagram of this RSC-MLI with separate level generator and polarity generator is shown in Fig. 2.23(b). To *n* units in level generator, the circuit configuration shown in Fig. 2.23(b) involves one stiff dc source (V_{dc}), $2n+4$ uni-directional switches, *n* diodes, *n* capacitors to produce $2n+3$ levels in phase-voltage, with magnitude varying from $(n+1)V_{dc}$ to $(n-1)V_{dc}$. In addition, this configuration shown in Fig. 2.23(b) produces equal device blocking voltages, operates in boost mode (magnitude of output voltage greater than input) with self-balancing of dc link capacitor voltages. However at higher levels, increase in number of capacitors, increases voltage drop among capacitors and adversely affect its performance.



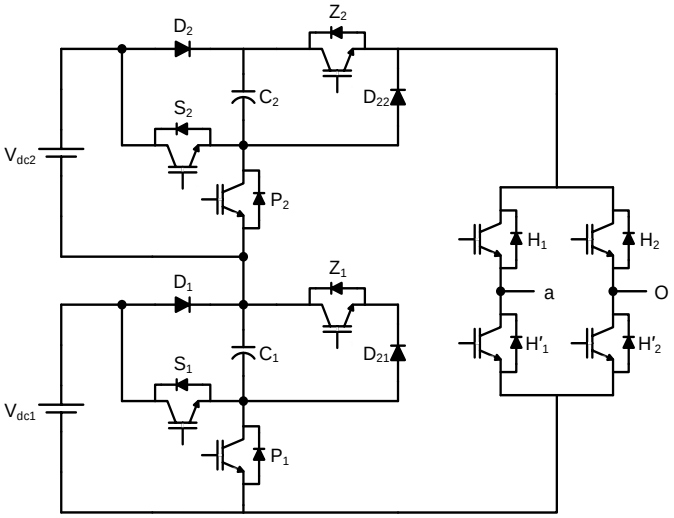
(a) Each basic (capacitor) unit



(b) Topology-I: Series connection of capacitor units with common polarity generator



(c) Topology-II: Cascade connection of capacitor units with individual polarity generator



(d) Topology-III: Cascade connection of capacitor units with common polarity generator

Fig. 2.23: Switched capacitor unit RSC-MLI.

Another possible way to extend this RSC-MLI is by connecting the units in cascade as shown in Fig. 2.23(c) and (d), where Fig. 2.23(c) involves a separate polarity generator for each unit and Fig. 2.23(d) shows the configuration with common polarity generator for all units. Switching operation of Fig. 2.23(c) is similar to Fig. 2.23(b), however involves a stiff dc source for each unit. Thus connecting *n* units in parallel, the configuration shown in Fig. 2.23(c), require $6n$ switches, *n* diodes, *n* capacitors, and *n* dc sources to produce $4n+1$ levels in phase-voltage with magnitude varying from $+2nV_{dc}$ to $-2nV_{dc}$. Further this configuration produces equal device blocking voltages and can be operated with asymmetrical dc voltages (binary and trinary voltage ratios). However,

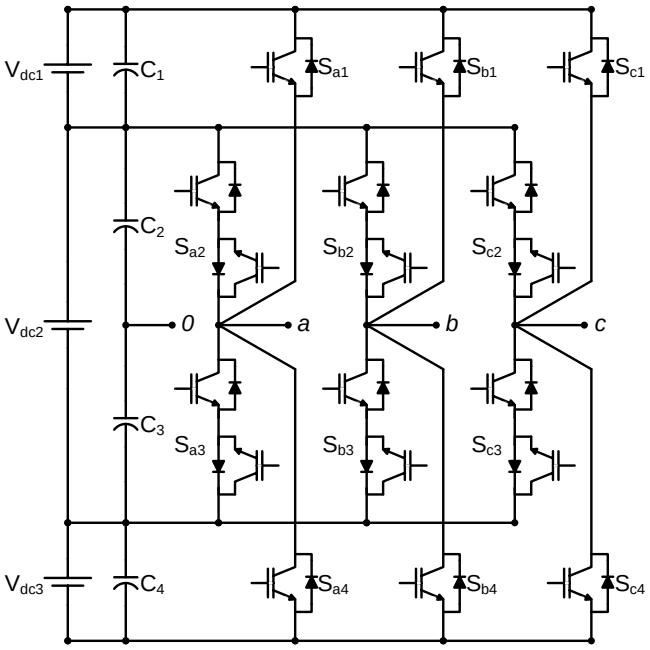
involvement of separate polarity generator for each unit increases the device count of the inverter at higher levels. Therefore, to extend this topology to higher levels, Fig. 2.23(d) is preferred.

Another configuration of this RSC-MLI with series connection of multiple switch capacitor units, minimizing the capacitor voltage drop and involving a common polarity generator is shown in Fig. 2.23(d). This configuration involves, an additional uni-directional switch Z_j and diode D_{2j} in each unit. These auxiliary devices minimize the capacitor voltage unbalance and helps to connect multiple units in series or parallel. In Fig. 2.23(d), a unit is bypassed, when its corresponding switch P_j is ON (with Z_j OFF) and D_{2j} is forward biased, where j is unit number i.e., $j = 1, 2, 3 \ldots n$. When Z_j is ON, D_{2j} becomes reverse biased and the corresponding unit capacitor charges to V_{dc}, and by operating P_j and S_j, a unit can either be connected in series or parallel with the remaining units. It is to be noted that the purpose of D_{2j} is to prevent current flowing backward when the unit is bypassed. Thus, with the involvement of Z_j and D_{2j} each unit can produce either V_{dc} or $2V_{dc}$ or zero. Further replacing D_{2j} with a controlled uni-directional switch, Fig. 2.23(d) can be operated for inductive loads as well. With n basic units, the configuration shown in Fig. 2.23(d) requires $3n+4$ switches, $2n$ diodes, n capacitors, n dc sources and produces $4n+1$ levels in phase-voltage with magnitudes varying from $+2nV_{dc}$ to $-2nV_{dc}$. This topology can also be implemented with asymmetrical voltage ratios as well.

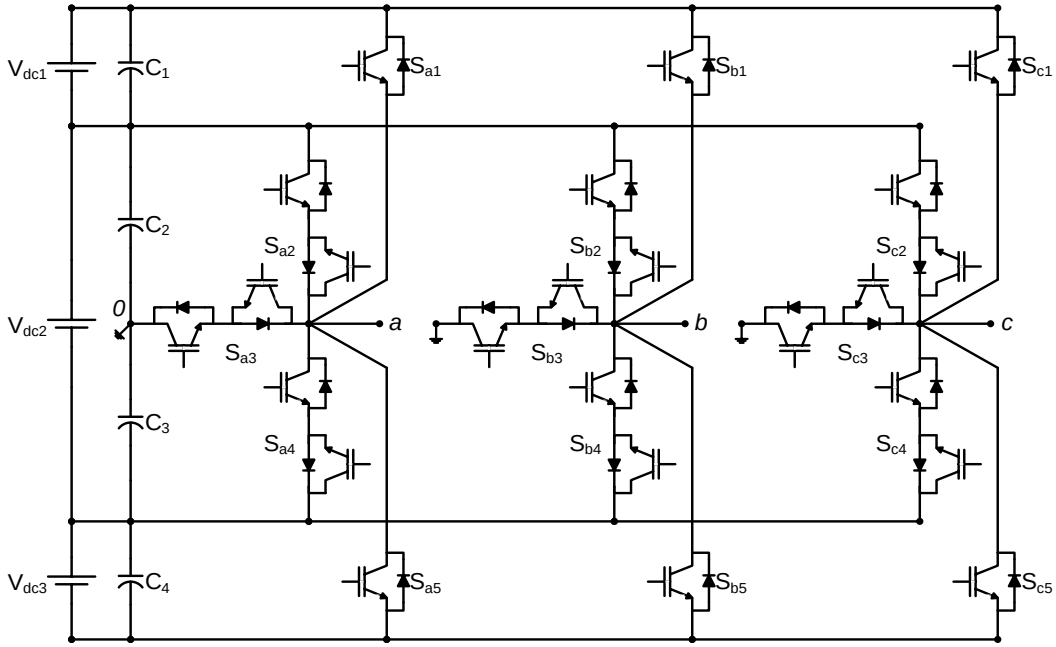
2.4.11 Nested topologies

Nested topologies involve the concept of nested arrangement where each phase will have multiple legs emerged from a common central point such that the outer legs includes the inner legs [71]. Topological structure of this RSC-MLI involve both bi-directional and uni-directional switches, and connects all phase legs to a common dc link. This topology produce any number of phase-voltage levels (both even and odd) and present advantages as compared to DCMLI topology in terms of higher efficiency, absence of clamping diodes and effective balance of dc link voltages. Topological arrangement of nested RSC-MLI is shown in Fig. 2.24, where Fig. 2.24(a) and (b) shows the configuration for four-level and five-level respectively. The switching operation of Fig. 2.24(a) and (b) for equal ratio of dc source voltages is shown in Table 2.19 and Table 2.20, respectively.

From Table 2.19 and Table 2.20, it is observed that these nested topologies operate with limited redundancies, does not facilitate even utilization of dc sources and produce unequal device blocking voltages. Further, these topologies cannot operate with asymmetrical voltage ratios. Replacing the dc link capacitors with stiff dc sources, generalization of this topology to higher levels can be achieved. With n (even or odd) identical sources in dc link, involves 6 uni-directional and $3(n-1)$ bi-directional switches to produce $(n+1)$ levels in phase-voltage.



(a) Four-level



(b) Five-level

Fig. 2.24: Nested RSC-MLI configurations.

Table 2.19: Switching states in phase-*a* of four-level nested RSC-MLI.

S_{a1}	S_{a2}	S_{a3}	S_{a4}	V_{ao}	$V_{C1} = V_{C4} = V_{dc}$; $V_{C2} = V_{C3} = \frac{V_{dc}}{2}$
1	0	0	0	$V_{C1}+V_{C2}$	$+3V_{dc}/2$
0	1	0	0	V_{C2}	$+V_{dc}/2$
0	0	1	0	$-V_{C3}$	$-V_{dc}/2$
0	0	0	1	$-(V_{C3}+V_{C4})$	$-3V_{dc}/2$

Table 2.20: Switching states in phase-*a* of five-level nested RSC-MLI.

S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{a5}	V_{ao}	$V_{C1} = V_{C4} = V_{dc}$; $V_{C2} = V_{C3} = V_{dc}$
1	0	0	0	0	$V_{C1}+V_{C2}$	$+2V_{dc}$
0	1	0	0	0	V_{C2}	$+V_{dc}$
0	0	1	0	0	0	0
0	0	0	1	0	$-V_{C3}$	$-V_{dc}$
0	0	0	0	1	$-(V_{C3}+V_{C4})$	$-2V_{dc}$

2.4.12 Packed U structures

These RSC-MLIs are modular with uni-directional switches arranged on either of dc link in U-shaped structure. The switching devices are arranged such that the inverter can block and conduct in both the directions. These topologies does not involve any separate polarity or level generator and produces output for additive and subtractive combinations of dc sources. Depending on the arrangement of the dc link and switching devices, there are two popular topological configurations, which are explained below.

2.4.12.1 Switched dc-sources (SDS) RSC-MLI

In literature, this topology is reported as cross connected sources (CCS) based RSC-MLI and switched dc sources (SDS) RSC-MLI [91-93]. With *n* sources in dc link, this topology involves 2(*n*+1) uni-directional switches and produce 2*n*+1 levels in phase-voltage with identical dc link voltages. Topology of SDS with three sources in dc link is shown in Fig. 2.25 and its switching operation with symmetrical and asymmetrical voltages produces seven and thirteen-levels in phase-voltage respectively as shown in Table 2.21.

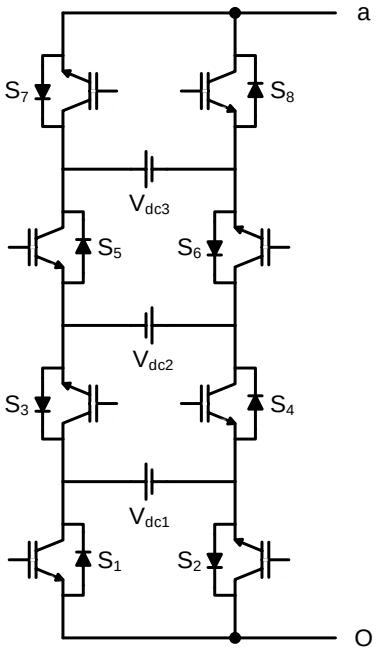


Fig. 2.25: Switched dc sources (SDS) RSC-MLI with three dc sources.

Table 2.21: Switching operation of SDS RSC-MLI.

Num. of states	Voltage combinations (V_{dc1}, V_{dc2}, V_{dc3})	Switches in conduction	Output voltage	
			Symmetrical	Asymmetrical
			Seven-level $V_{dc1} = V_{dc2} = V_{dc3} = V_{dc}$	Thirteen-level $V_{dc1} = V_{dc}$; $V_{dc2} = 3V_{dc}$; $V_{dc3} = 2V_{dc}$
1	$V_{dc1}+V_{dc2}+V_{dc3}$	S_2-S_3-S_6-S_7	$+3V_{dc}$	$+6V_{dc}$
2	$V_{dc2}+V_{dc3}$	S_1-S_3-S_6-S_7	$+2V_{dc}$	$+5V_{dc}$
3	$V_{dc1}+V_{dc2}$	S_2-S_3-S_6-S_8	$+2V_{dc}$	$+4V_{dc}$
4	V_{dc2}	S_1-S_3-S_6-S_8	$+V_{dc}$	$+3V_{dc}$
5	V_{dc3}	S_2-S_4-S_6-S_7	$+V_{dc}$	$+2V_{dc}$
6	V_{dc1}	S_2-S_3-S_5-S_7	$+V_{dc}$	$+V_{dc}$
7	$V_{dc3}-V_{dc1}$	S_1-S_4-S_6-S_7	0	$+V_{dc}$
8	0	S_1-S_3-S_5-S_7	0	0
		S_2-S_4-S_6-S_8		
10	$V_{dc1}-V_{dc3}$	S_2-S_3-S_5-S_8	0	$-V_{dc}$
11	V_{dc1}	S_1-S_4-S_6-S_8	$-V_{dc}$	$-V_{dc}$
12	V_{dc3}	S_2-S_4-S_5-S_7	$-V_{dc}$	$-2V_{dc}$
13	V_{dc2}	S_1-S_3-S_5-S_8	$-V_{dc}$	$-3V_{dc}$
14	$V_{dc1}+V_{dc2}$	S_1-S_4-S_5-S_7	$-2V_{dc}$	$-4V_{dc}$
15	$V_{dc2}+V_{dc3}$	S_2-S_4-S_5-S_8	$-2V_{dc}$	$-5V_{dc}$
16	$V_{dc1}+V_{dc2}+V_{dc3}$	S_2-S_3-S_6-S_7	$-3V_{dc}$	$-6V_{dc}$

From Table 2.21, it is verified that this topology possess switching redundancies, nevertheless does not facilitate equal utilization of dc sources and produces unequal device blocking voltages. For example, symmetrical configuration of Fig. 2.25, operates S_1, S_2, S_7 and S_8 with a blocking voltage of V_{dc} and, S_3, S_4, S_5 and S_6 with a blocking voltage of $2V_{dc}$.

2.4.12.2 Packed U-cell (PUC) RSC-MLI

Topological configuration of packed U-cell (PUC) RSC-MLI is similar to SDS as discussed above, however includes few modifications in arrangement of switches and dc voltage ratios. Circuit configuration of PUC with three dc sources is shown in Fig. 2.26 and its corresponding switching operation is shown in Table 2.22 [52, 94]. PUC produces uniform device blocking voltages, however does not facilitate even utilization of dc sources.

Table 2.22 shows that PUC operates for both additive and subtractive combinations of dc sources. However with symmetrical dc sources, these switching combinations cannot produce more than three-levels in phase-voltage. This is due to the consecutive additive and subtractive combination of dc voltages in any switching path as shown in Table 2.22. Thus with any number of dc sources, symmetrical configuration of PUC produces only three-levels with magnitude varying from V_{dc} to $-V_{dc}$. Therefore, this topology is advantageous with asymmetrical dc sources. Further operating PUC with asymmetrical dc voltages, levels can be increased, however the

magnitude of the output voltage will be always less than the total dc input voltage. Considering $V_{dc1} = V_{dc}$, $V_{dc2} = 3V_{dc}$ and $V_{dc3} = 6V_{dc}$ in Fig. 2.26, produces thirteen-levels in phase-voltage, with magnitudes varying from $+6V_{dc}$ to $-6V_{dc}$ as given in Table 2.22. However, the maximum output voltage (in phase) is $6V_{dc}$, even though the total dc link voltage is $10V_{dc}$.

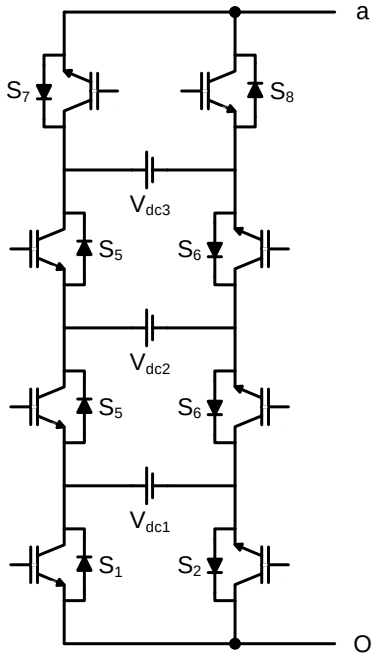


Fig. 2.26: Topological structure of PUC RSC-MLI.

Table 2.22: Switching states of PUC topology.

Num. of states	**Voltage combinations (V_{dc1}, V_{dc2}, V_{dc3})**	**Switches in conduction**	**Output voltage**	
			Symmetrical	**Asymmetrical**
			$V_{dc1} = V_{dc2} = V_{dc3} = V_{dc}$	**$V_{dc1} = V_{dc}$; $V_{dc2} = 3V_{dc}$; $V_{dc3} = 6V_{dc}$**
1	V_{dc3}	S_2-S_4-S_6-S_7	$+V_{dc}$	$+6V_{dc}$
2	$-V_{dc1}+V_{dc3}$	S_1-S_4-S_6-S_7	0	$+5V_{dc}$
3	$V_{dc1}-V_{dc2}+V_{dc3}$	S_2-S_3-S_6-S_7	$+V_{dc}$	$+4V_{dc}$
4	V_{dc2}	S_2-S_4-S_5-S_7	$+V_{dc}$	$+3V_{dc}$
5	$-V_{dc2} + V_{dc3}$	S_1-S_3-S_6-S_7	0	$+3V_{dc}$
6	$-V_{dc1}+V_{dc2}$	S_1-S_4-S_5-S_7	0	$+2V_{dc}$
7	V_{dc1}	S_2-S_3-S_5-S_7	$+V_{dc}$	$+V_{dc}$
8	0	S_1-S_3-S_5-S_7 (or) S_2-S_4-S_6-S_8	0	0
9	$-V_{dc1}$	S_1-S_4-S_6-S_8	$-V_{dc}$	$-V_{dc}$
10	$V_{dc1}-V_{dc2}$	S_2-S_3-S_6-S_8	0	$-2V_{dc}$
11	$-V_{dc2}$	S_1-S_3-S_6-S_8	$-V_{dc}$	$-3V_{dc}$
12	$V_{dc2}-V_{dc3}$	S_2-S_4-S_5-S_8	0	$-3V_{dc}$
13	$-V_{dc1}+V_{dc2}-V_{dc3}$	S_1-S_4-S_5-S_8	$-V_{dc}$	$-4V_{dc}$
14	$V_{dc1}-V_{dc3}$	S_2-S_3-S_5-S_8	0	$-5V_{dc}$
15	$-V_{dc3}$	S_1-S_3-S_5-S_8	$-V_{dc}$	$-6V_{dc}$

2.4.13 Three-phase topologies

In most of the RSC-MLI topologies, each phase is independently operated such that the output voltage of one phase does not impact the output of other phase. However to have an effective reduction in device count, three-phase topologies can be prefered, where the operation of inverter is dependent on all phases as similar to two-level inverter. Switching operation of these three-phase topologies should be appropriately controlled such that the pole-voltage produces the desired number of levels in line-voltage. Topologically, these MLIs possess a three-leg six switch inverter with few auxiliary components between dc link and six switch inverter module. The arrangement of dc link and auxiliary switches majorly decides the topological configuration of these RSC-MLIs. Popular topologies reported under this category of RSC-MLIs are explained here under.

2.4.13.1 Topology – I

A new three-phase symmetrical RSC-MLI configuration is reported by Ahmed Salem in 2015 [95]. This configuration possess a modular structure and can be easily extended to higher voltage levels. This configuration involves a two-level inverter with upper switches of each leg connected to dc ink through multiple modular units connected in series. Each of this modular unit produces an output, either V_{dc} or 0. Topological configuration of this MLI for five-level (in line-voltage) is shown in Fig. 2.27, and its corresponding switching operation for three-level pole-voltage is shown in Table 2.23. Extension of this three-phase RSC-MLI configuration to higher levels is shown in Fig. 2.28, where the configuration is shown for seven-level. Similarly with n units, this topology involves $3(2n+2)$ switches to produce $n+2$ levels in pole-voltage and $2n+3$ levels in line-voltage. This configuration facilitates uniform utilization of dc sources but produces unequal device blocking voltages.

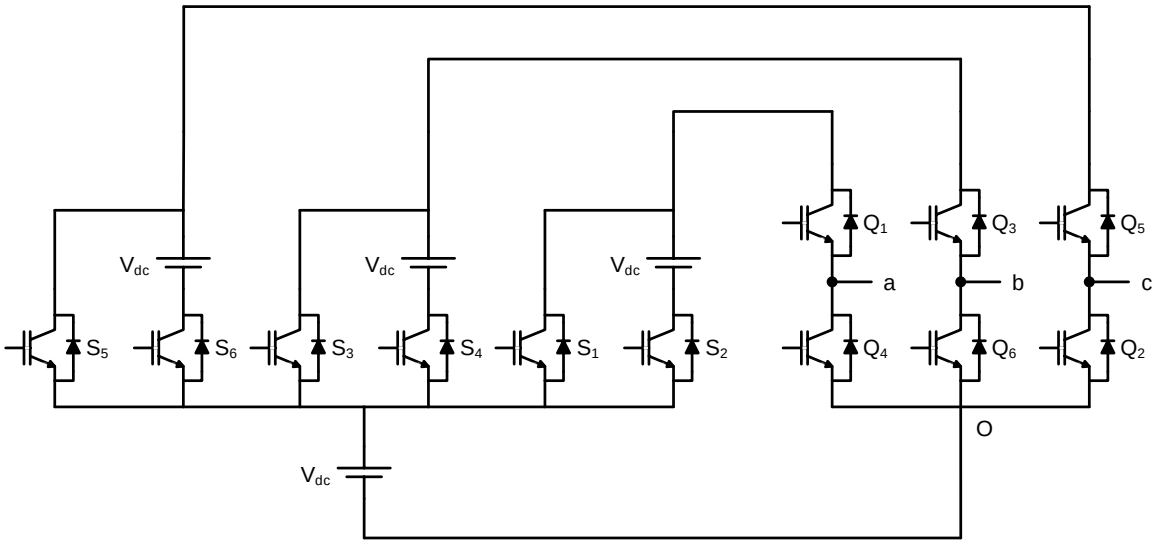


Fig. 2.27: Five-level three-phase RSC-MLI Topology – I.

Table 2.23: Switching states of Topology – I for three-level pole-voltage.

Num. of states	Switches in conduction				Pole-voltage (V_{ao})
	S_1	S_2	Q_1	Q_2	
1	0	0	0	1	0
2	1	0	1	0	E
3	0	1	1	0	2E

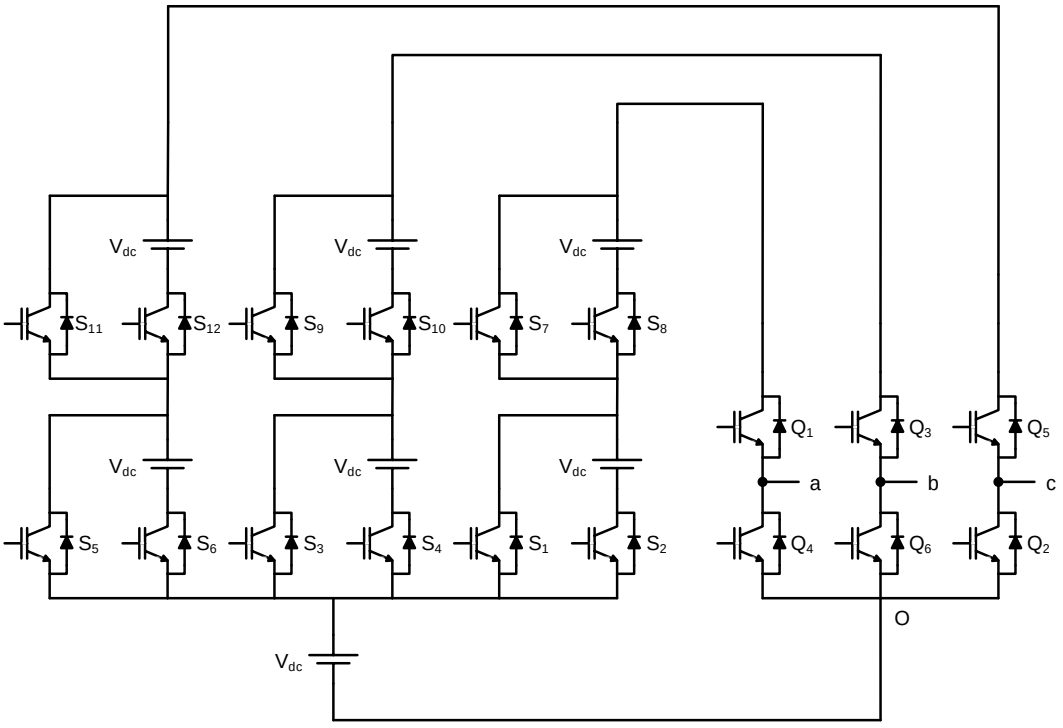


Fig. 2.28: Seven-level three-phase RSC-MLI Topology – I.

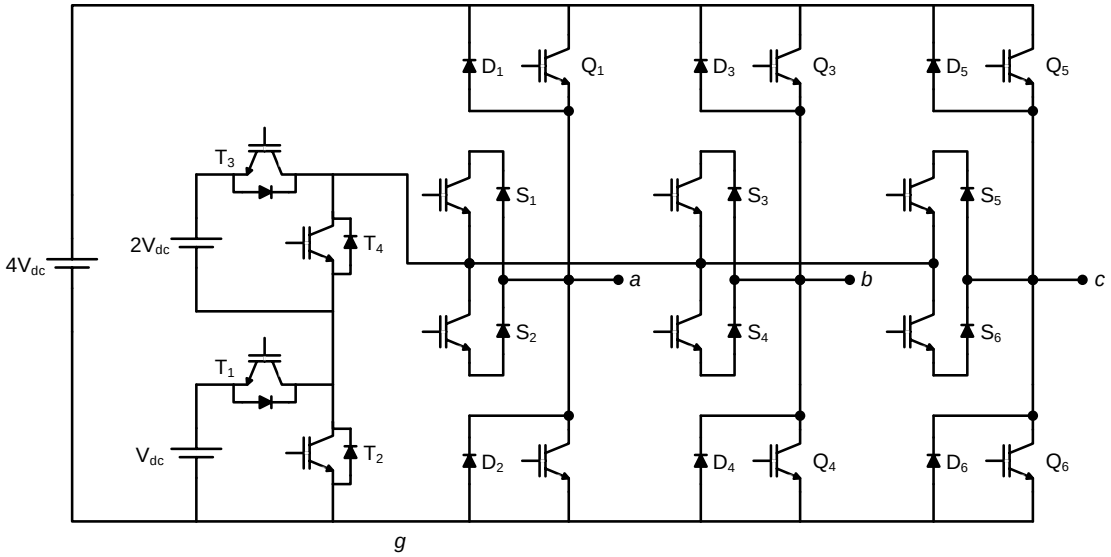
2.4.13.2 Topology – II

These topologies are reported by Ammar Masaoud in 2014 [72, 73]. These RSC-MLIs possess a generalized topological arrangement and can be operated with symmetrical and asymmetrical dc voltages. These configurations are reported for five-levels in pole-voltage and are shown in Fig. 2.29 and Fig. 2.30. From these figures, it can be observed that, these MLIs have few key similarities in their topological arrangement, which are:

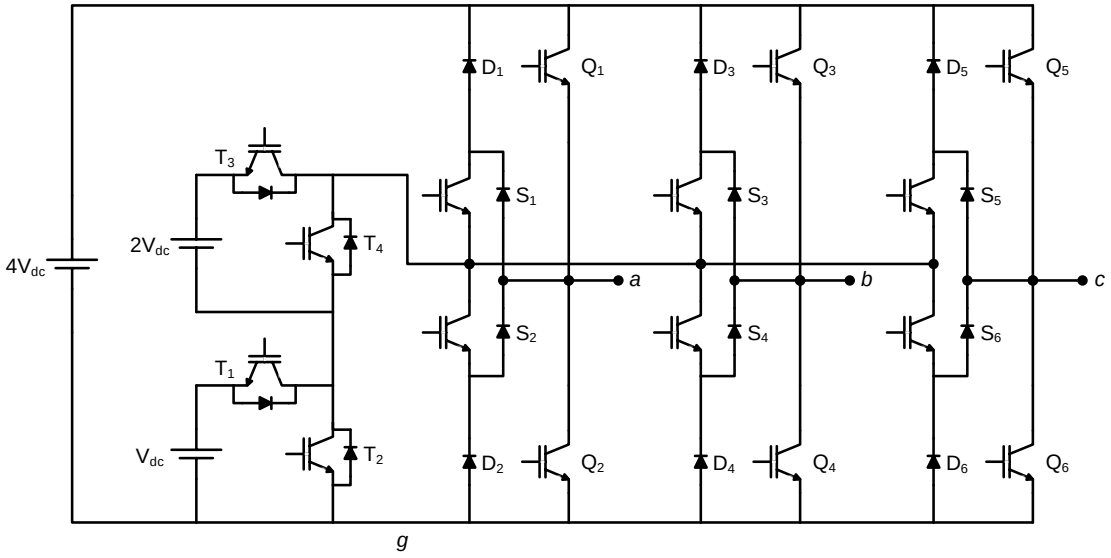
- Similarities in dc link: Maximum input dc voltage in all cases is fixed to $4V_{dc}$.
- Each phase-leg arrangement: Each leg of the inverter involves one bi-directional switch (S_1-S_2) and one complimentary uni-directional switch pair Q_1 and Q_2.

Further, Fig. 2.29(b) and Fig. 2.30(b) have identical leg structure, where, S_1 is connected to the higher potential of dc link through D_1 and S_2 is connected to the lower potential of dc link through D_2. Further, the mid-point of bi-directional switch on three legs is connected to dc link through auxiliary switches. These auxiliary switches are responsible for obtaining multiple input dc voltages and thus form supporting unit for level generation. Usually the merit of any three-phase

RSC-MLI lays in fabrication of this supporting unit. For the considered topologies shown in Fig. 2.29(b) and Fig. 2.30(b), the supporting unit is formed with four uni-directional switches and two dc sources, however their position and arrangement is different in both topologies. Similarly Fig. 2.29(a) and Fig. 2.30(a), possess identical leg structure, where the bi-directional switch is neither connected to the higher potential nor to lower potential of the dc link, but its mid-point is connected to dc link through auxiliary switches. This auxiliary structure in both these topologies is different. However, the auxiliary structure of Fig. 2.29(a) and (b) is identical and similarly the auxiliary structure of Fig. 2.30(a) and (b) is identical. Switching operation of these topologies shown in Fig. 2.29 and Fig. 2.30 is given in Table 2.24. It is to be noted that this switching table is valid for the generation of five-levels in pole-voltage and nine-levels in line-voltage. However, these RSC-MLI does not have switching redundancies, produces unequal blocking voltages and may result in non-uniform utilization of dc sources.

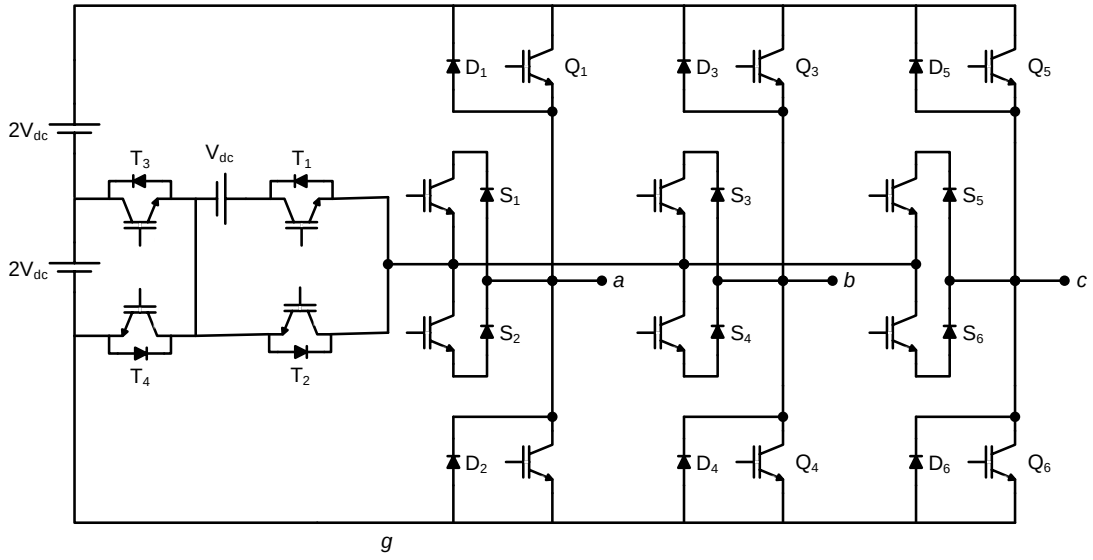


(a) Configuration – 1

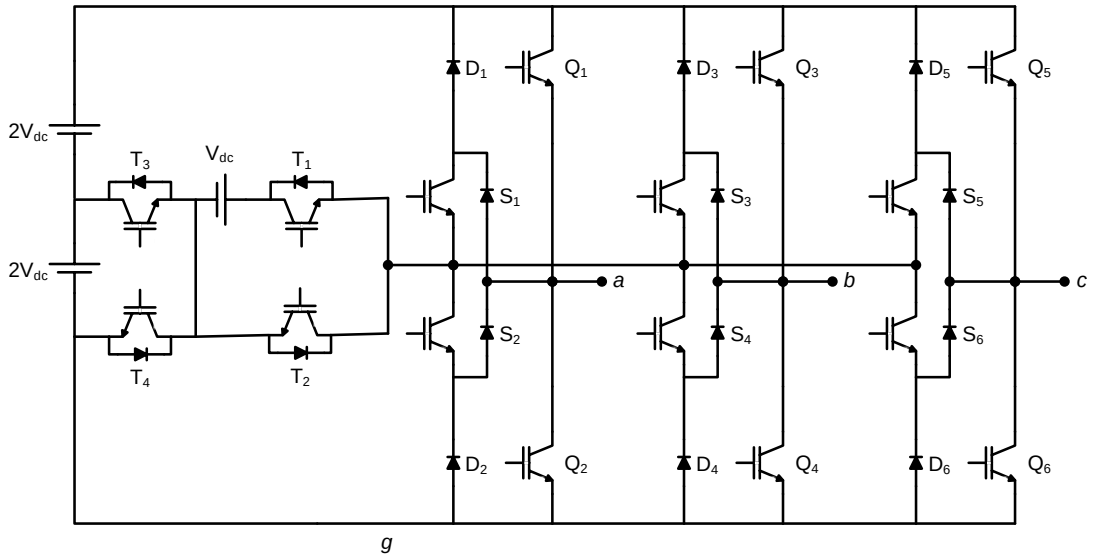


(b) Configuration – 2

Fig. 2.29: Three-phase asymmetrical five-level RSC-MLI configurations of Topology – II.



(a) Configuration – 3



(b) Configuration – 4

Fig. 2.30: Three-phase asymmetrical five-level RSC-MLI configurations of Topology – II. (Contd.)

Table 2.24: Switching states of five-level three-phase RSC-MLIs.

Q_1	S_1	S_2	Q_2	T_1	T_2	T_3	T_4	V_{ag}
1	0	0	0	1	0	1	0	$+4V_{dc}$
0	1	1	0	1	0	1	0	$+3V_{dc}$
0	1	1	0	0	1	1	0	$+2V_{dc}$
0	1	1	0	1	0	0	1	$+V_{dc}$
0	0	0	1	1	0	1	0	0

Further, the topologies shown in Fig. 2.29(a) and (b) can be extended to higher levels [72, 73]. Generalizing the inverter configuration depicted in Fig. 2.29(a) and (b), for *n* sources (each V_{dc}) in the auxiliary unit, then maximum dc link voltage is $(1+n)V_{dc}$ and produces (*n*+2) levels in

pole-voltage. In case, if the supporting structure involves *n* units with binary voltage ratios, then the maximum dc link voltage will be $\left(1+\frac{n(n+1)}{2}\right)V_{dc}$ and produces $\left(2+\frac{n(n+1)}{2}\right)$ levels in pole-voltage.

2.5 Comparison of RSC-MLI topologies

This section presents a comprehensive comparison on the features, merits and limitations of various RSC-MLIs. The parameters considered for comparative study are: topological arrangement, physical structure, switching nature of level and polarity generators, requirement of dc supply, involvement of uni-directional or bi-directional switches, device count, devices blocking voltages, utilization of dc sources, load power distribution, dc link voltage balancing, possibility to operate with asymmetrical dc sources, voltage boosting, switching redundancies, generalization of the topology to higher levels and fault tolerance ability. This comparison is summarized in Table 2.25.

Table 2.25: Comparison of device count and salient features of RSC-MLIs topologies reported in literature.

GENERALIZED RSC-MLIs : Topologies generalized for any number of phase-voltage levels											
Topology name	**H-bridge /HSC based/ other**	**With *n* dc sources (Identical)**					**Symmetrical/ Asymmetrical /Both**	**Blocking voltages (Equal/Unequal)**		**DC sources utilization (Even/ Uneven)**	• **Features** ✓ **Merits** × **Limitations**
		Levels in phase-voltage (*m*)	**Device count/phase: Uni-directional (*U*), bi-directional (*B*) switches, diodes (*D*) and capacitors (*C*)**					**Level generator**	**Polarity generator**		
			U	***B***	***D***	***C***					
MLDCL [53, 54] S. Gui-Jia	H-bridge	2*n*+1	2*n*+4	---	---	---	Both	Equal	Equal	Even	✓ Easily scalable, highly modular, redundant level generator and fault tolerant ✓ Symmetric switching operation for positive and negative voltages levels ✓ dc link voltage balancing ✓ Voltage stress on the operating devices (level generator) remains same for any number of levels × Cannot support trinary dc voltages
SSPS [62, 63] Hinago & Koizumi	H-bridge	2*n*+1	2*n*+4	---	---	---	Both	Equal	Equal	Even	✓ Series/parallel operation ✓ Self-balancing topology ✓ Voltage boosting ability ✓ Symmetric switching operation for positive and negative cycles × Cannot support trinary dc voltages
RV [55, 76] Ehsan Najafi	H-bridge	2*n*+1	2*n*+4	---	---	---	Both	Unequal	Equal	Uneven	✓ Symmetric switching operation for positive and negative cycles × Limited redundancies. × Device ratings increases with number of levels × Asymmetry with binary and trinary voltage ratios is not possible.
SCSS [77, 78]	H-bridge	2*n*+1	2*n*+4	---	---	---	Symmetrical	Unequal	Equal	Uneven	✓ level generator: Modular and stair case structure ✓ Symmetric switching operation for positive and negative voltage levels × No switching redundancies × Asymmetry is not possible

MLM [85] E. Babaei	H-bridge	2*n*+1	4	*n*+1	---	---	Symmetrical	Unequal	Equal	Uneven	× No switching redundancies × Voltage balancing is very difficult × Asymmetry not possible × Device voltage ratings increases number of levels ✓ Symmetric switching operation for positive and negative voltage levels ✓ Modular structure
CBSC [69] E. Babaei	U-shaped, Flying capacitor structure	2*n*+1	---	2*n*+2	---	---	Both	Unequal		Uneven	✓ Does not involve a separate polarity or level generator. ✓ Modular structure ✓ Involves only bi-directional switches ✓ Always two switching devices in conduction × Asymmetry with binary and trinary voltages ratios is not possible. × Inadequate redundancies to achieve dc link voltage balance
T-type MLI [56, 58, 61, 79, 80] Ceglia *et al*	H-bridge	2*n*+1	4	*n*–1	---	---	Symmetrical	Unequal		Uneven	× Absence of redundancies increase the difficulty in obtaining dc link voltage balancing × Voltage rating of operating devices increases with dc link voltage • No separate polarity and level generator ✓ Appreciable reduction in switch count ✓ Modular structure ✓ Can be extended to higher levels with /without cascading. ✓ Voltage rating of operating devices increases with dc link voltage ✓ Only two devices remains in conduction at any instant

Cascaded T-type [60]	H-bridge	With *n* identical *l*-level T-type units in cascade					Both	Unequal	Uneven	• All the merits and features of T-type MLI are valid to each T-type unit in cascade ✓ Possess multiple switching redundancies ✓ Facilitates even power distribution among all the modules (units). × Each module of T-type requires its corresponding dc link voltages (in same module) to be equal.
		$m = n(l-1)+1$	$4n$	$n\frac{l-3}{2}$		$n\frac{l-1}{2}$				
Three leg T-type MLI [61, 82, 84]	Half bridge	$\frac{(n-1)}{2}+1$ (n should be even)	2	$(n-1)$	---	---	Symmetrical	Unequal	Uneven	✓ Common dc link to all phases ✓ lower conduction losses and high efficiency × Absence of switching redundancies × dc voltage balancing is difficult × cannot operate with asymmetrical dc sources ✓ Alternate to NPC, ANPC and NPP MLIs.
PUC [52, 94]	Packed U-cell structure	For $n > 2$ $m=3$ For $n \leq 2$ $m=2n+1$	$2n+2$	---	---	---	Both	Equal	Uneven	× Cannot produce more than three-level in phase-voltage with symmetrical dc voltage sources. × Switching path of any voltage levels involves consecutive addition and subtraction of dc sources. ✓ Extended to higher levels with asymmetrical voltage ratios. × Maximum output voltage is less than total dc voltage: operates in buck mode.
SDS [91-93]	Packed U-cell structure	$2n+1$	$2n+2$	---	---	---	Both	Unequal	Uneven	✓ Overcomes the demits of PUC RSC-MLI × Binary and trinary voltage ratios are not valid. ✓ Modular structure and appreciable reduction in switch count

Hybrid T-type [65, 66] Shivam Prakash Gautam *et al.*	HSC Topology-I [65, 66]	m	6	$\frac{m-5}{4}$	---	$\frac{m-1}{4}$	Both	Unequal	Uneven	• Only two stiff dc sources are sufficient i.e., always $n = 2$. • Symmetrical configuration of this RSC-MLI is valid for generating m voltage level only for integer values of $(m–1)/4$, such as $m = 9, 13, 17…$ • For other levels, asymmetrical configuration should be opted. × Cannot support trinary voltage-ratios • Does not involve separate polarity or level generator ✓ Modular structure and appreciable reduction in switch count. ✓ Extended to higher levels with or without cascading × Limited switching redundancies
	HSC Topology-II [65, 66]	m	6	$\frac{m-5}{2}$	---	$\frac{m-1}{2}$	Both	Unequal	Uneven	✓ Includes all features of Topology-I, ✓ operates with more switching redundancies than Topology- I ✓ DC link capacitors can be replaced by stiff dc sources
Nested MLI [71]	Three-leg nested structure	n+1	2	n–1			Symmetrical	Unequal	Uneven	✓ Common dc link to all phases. • Involves both bi-directional and uni-directional switches. ✓ Obtains both even and odd levels with uniform *dv/dt* × No redundancies. × Asymmetry is not possible. • If n even, produces odd levels in phase-voltage and vice versa. × Output voltage magnitude for even levels is relatively less than odd-levels.

SWITCHED CAPACITOR RSC-MLIs: Unit based but generalized for any level										
Topology name	**H-bridge /HSC based/ other**	**With *n* dc sources (Identical)**					**Symmetrical/ Asymmetrical /Both**	**Blocking voltages (Equal/Unequal)**	**DC sources utilization (Even/ Uneven)**	• **Features** ✓ **Merits** × **Limitations**
		Levels in phase-voltage (*m*)	**Device count/phase: Uni-directional (*U*), bi-directional (*B*) switches, diodes (*D*), capacitors (*C*)**							
			U	***B***	***D***	***C***				
Split capacitor unit RSC-MLI [89] Reza Barzegark-hoo	Each unit is a three-level inverter	$2n+1$	$2n$	n	$4n$	---	Both	Equal	Even	✓ Natural voltage balancing through split capacitor ✓ Extended to higher levels by cascading ✓ asymmetry is possible ✓ Equal blocking voltages ✓ Equal load power distribution among dc link capacitors × output phase voltage magnitude varies from $(n/2)\ V_{dc}$ to $-(n/2)\ V_{dc}$ i.e., less than input voltage
Switched capacitor RSC-MLI [90] E. Babaei	**Topology -I** H-bridge	One Stiff dc voltage $2n+3$	$2n+4$	---	$2n$	n	Symmetrical	Equal	Even	• Level generator possess multiple modular units in series with single dc source ✓ Self-balancing of dc link voltages ✓ Boost operation: n capacitors charged through one source such that the output voltage is $(n+1)V_{dc}$. × Multiple switching redundancies × Complicated topological arrangement. × Least fault tolerant capability: Not possible to by-pass any faulty unit

Switched capacitor RSC-MLI [90] E. Babaei	**Topology -II** H-bridge	[each unit is five-level inverter] 4*n*+1	6*n*	---	*n*	*n*	Both	Equal	Even	• Each unit possess one voltage source and a separate and level generator • Level generator cannot produce zero voltage level. ✓ Operates in boost mode: *n* units in series produces an output voltage magnitude of $2nV_{dc}$ ✓ Asymmetry is possible ✓ Reduces the problem of capacitor voltage drop of Topology - I ✓ Self-balancing of dc link voltages. ✓ Multiple redundancies. × Complicated topological arrangement × Relatively increased switch count at higher levels (in comparison to other topologies).
Switched capacitor RSC-MLI [90] E. Babaei	**Topology -III** H-bridge	each unit produces only positive levels 4*n*+1	3*n*+4	---	2*n*	*n*	Both	Unequal	Even	✓ Each unit possess a stiff dc source and capacitor ✓ Multiple units are connected in series with one polarity generator ✓ Symmetric switching logic for positive and negative levels ✓ Operates in boost mode: *n* units in series produces an output voltage magnitude of $2nV_{dc}$ ✓ Multiple redundancies ✓ Asymmetry is possible. ✓ Self-balancing of dc link voltages × Complicated topological arrangement × Fault tolerant capability: Not possible to by-pass any faulty unit

UNIT BASED MLIs: Topologies for obtaining specific number of phase-voltage levels.

Topology name	H-bridge /HSC based/ other	levels from each unit	With *n* identical units: uni (*U*) & bi (*B*) directional switches, diodes (*D*), capacitors (*C*), phase-voltage levels (*m*) and dc sources (*N*)						Symmetrical/ Asymmetrical /Both	Blocking voltages Equal/ Unequal	dc sources utilization Even/ Uneven	Features • **Features** ✓ **Merits** × **Limitations**
			m	***N***	***U***	***B***	***D***	***C***				
Basic unit MLI [86] Ebrahim Babaei	H-bridge	9-level	$6n+3$	$3n+1$	$5n+6$	n	---	---	Both	Unequal	Uneven	• Separate polarity and level generator • Polarity generator operates at modulating frequency × Cannot support trinary voltage × Symmetric switching operation for positive and negative voltage levels
E-type MLI [64]	Envelope type Emad Samadaei *et.al*	13-level	$12n+3$	$4n$	$6n$	$2n$	---	---	Asymmetrical	Unequal	Uneven	• Purely asymmetrical RSC-MLI ✓ Appreciable reduction in switch count × DC link voltage balancing is not possible ✓ Cascaded configuration has multiple redundancies
Square T-type [74]		17-level	$16n+1$	$4n$	$6n$	$3n$	---	---	Asymmetrical	Unequal	Uneven	• All merits, limitations and features of E-type are applicable ✓ Superior reduction in switch count compared to E-type
Cascaded MLI [87, 88]. Charles Ikechukwu Odeh	Topology–I HSC-based [87]	9-level	$8n+1$	$3n$	$6n$	n	---	---	Asymmetrical	Unequal	Uneven	✓ Does not involve separate polarity or level generator • Similar to Hybrid T-type topology-I × Topological orientation is difficult to synthesize
	Topology - II H-bridge based. [88]	5-level	$4n+1$	$2n$	$6n$	---	---	---	Symmetrical	unequal	Even	• Each unit comprises a separate polarity and level generator ✓ Modular and redundant structure ✓ Equal utilization of dc sources
HSC cascade MLI [67, 68] E. Babaei	HSC based	5-level	$4n+1$	$2n$	$6n$	---	---	---	Both	Unequal	Even	✓ Does not involve separate polarity or level generator ✓ Attractive and simplified topological structure.

Three-phase RSC-MLIs												
Topology name	**Type**	**levels in pole-voltage**	**With *n* units (identical)**						**Symmetrical/ Asymmetrical /Both**	**Blocking voltages Equal/ Unequal**	**Dc sources utilization Even/ Uneven**	**Features**
			Switches uni (*U*) & bi (B) directional; diodes (*D*), capacitors (*C*); and dc sources (*N*), levels in line-voltage (*M*)									• **Features** ✓ **Merits** × **Limitations**
			M	***N***	***U***	***B***	***D***	***C***				
***Topology*-I** [95] Ahmed Salem	3-leg based	$n+2$	$2n+2$	$3n+1$	$6n+9$	--	--	--	Symmetrical	unequal	even	✓ Modular and redundant structure (level generator) × Cannot support trinary voltage ratios × Complex switching logic × Asymmetry is not possible
***Topology*-II** [72, 73] Ammar Masaoud	3-leg based	$n+2$	$2n+5$	$n+1$	$2n+6$	3	---	---	Both	unequal	uneven	✓ Modular and redundant structure (level generator) × Asymmetry with trinary voltage ratios is not possible × Complex switching logic

From the Table 2.25, following observations can be drawn:

1. Modularity of RSC-MLIs: The extension of topology to higher levels with the addition of new devices, does not affect the blocking voltage and rating of the existing devices.
2. In H-bridge and HSC based RSC-MLI topologies, the voltage rating of the devices in H-bridge and HSC are higher than the total dc link voltage. Few such topologies are MLDCL, SSPS, T-TYPE, RV, SCSS, improved T-type, MLM, basic unit RSC-MLI, cascaded MLI with H-bridge and hybrid MLI using switched Capacitor units.
3. The topologies with separate polarity generator and level generator, possess symmetric switching operation for both positive and negative voltage levels. Most often, level generator of RSC-MLIs always produce the output voltage for additive combination of dc sources and does not facilitate switching states for subtractive combinations. This limits the asymmetry of the topology with trinary voltage ratios. Few of such RSC-MLIs are MLDCL, SSPS, RV and SSPS.
4. Reduction in switch count, reduces the switching redundancies and creates unequal voltage stress and blocking voltages on the switches and limits the capability to balance the dc link voltages thus, leads to the unequal utilization of dc sources.
5. Switching redundancies play a key role in reconfiguration of the inverter in faulty condition. Thus, limited or absence of switching redundancies in RSC-MLI topologies such as T-type, and E-type topologies restricts their fault tolerant ability.
6. Level generator of few RSC-MLIs does not produce zero voltage across and is produced from polarity generator. In case of open circuit (OC) faults, these configurations may not permit to by-pass faulty operating unit and limits the fault tolerant ability of the topology.
7. Requirement of dc supply: Few RSC-MLI possess the topological structure where a common dc link will be connected to all the phases such as nested MLIs, three-phase RSC-MLI topology–II. Also few other topologies require non-isolated dc voltages.
8. In some topologies such as, switched capacitor RSC-MLI, the dc sources can be replaced by capacitors and a single dc supply can be connected in parallel to them. This reduces the requirement of dc sources, however this cannot be preferred for high-voltage applications, as it causes voltage unbalance.
9. Few other topologies such as SSPC, possess boost circuit configuration, where the topology charges multiple capacitors through one stiff dc source such that voltage across each capacitor is equal to the dc source voltage.

2.6 Summary

The dominating factors for selecting a topology is concluded as:

- Uniform and unaffected blocking voltages (with increase in number of levels).
  Example: MLDCL, switched capacitor MLIs and SSPS.
- Modular and generalized topological structure.
  Example: MLDCL, RV, SSPS and SCSS.
- Appreciable reduction in switch count at any level:
  Example: T-type, E-type, Square E-type, Improved T-type and MLDCL.
- Uniform utilization of dc sources, dc link voltage balancing
  Example: MLDCL, SSPS and switched capacitor MLIs.
- Fault tolerant operation of the inverter, where a fault unit can be effectively bypassed:
  Example: MLDCL
- Voltage boosting nature:
  Example: SSPS and switched capacitor MLIs
- Simplified topological structure
  Example: SCSS, T-type and MLDCL

Among these most attractive topologies are MLDCL, Switched capacitor MLIs (Topology–II) and T-type RSC-MLI. However, switched capacitor MLIs does not possess an appreciable reduction in switch count at higher levels and involves complicated topological structure with limited fault tolerant ability. T-type RSC-MLI possess appreciable reduction in switch count but lack of switching redundancies, inability to cope with asymmetrical dc sources, inability to achieve even power distribution of dc sources, non-uniform blocking voltages and restricted fault tolerance acts as major limitations. On the other hand, MLDCL possess simplified, modular and generalized topological structure with appreciable reduction in switch count, multiple switching redundancies, symmetric and simplified switching operation, fault tolerant ability, even power distribution, equal blocking voltages and dc link voltage balancing capability. Owing to these key and worthy benefits, this topology had gathered more attention among other RSC-MLIs topologies. Further, MLDCL serves as viable alternate to CHB MLI for applications such as grid connected PV system, active front-end converters, custom power devices, BESS, and HEV. Therefore in this thesis, to analyze fault tolerant ability and closed-loop implementation of RSC-MLI topologies, MLDCL RSC-MLI is considered.

CHAPTER 3: PWM SCHEMES OF RSC-MLI

This chapter discusses the challenges of conventional PWM schemes of RSC-MLI topologies and elevates the necessity of novel and unified carrier based modulation schemes for controlling RSC-MLI topologies.

3.1 Introduction

In many industrial applications, it is often necessary to control the output voltage of inverter for (1) coping with the variations of the dc input voltage, (2) regulating the voltage of the inverter, and (3) satisfying the constant voltage/frequency control requirement in the drives systems [20, 96, 97]. Many modulation techniques have been developed for controlling the output voltage of a multilevel inverter [97]. They are aimed at generating a stepped switched waveform that best approximates an arbitrary reference signal with adjustable amplitude, frequency, and phase of a fundamental component that is usually a sinusoid in steady-state. The modulation algorithms are divided into two main groups, depending on the domain in which they operate: the state-space vector domain, in which the operating principle is based on the voltage vector generation, and the time-domain, in which the method is based on the voltage level generation over a time frame [6, 7, 10, 16, 20, 30, 97, 98].

The state-space vector domain algorithms such as space vector modulation (SVM) based PWM algorithms for various topologies of MLI are reported in [20, 71-73, 99]. However, they are not the dominant modulation schemes found in industrial applications [16], as SVM is a computationally intensive method and its complexity increases with increase in number of levels in the inverter [20]. However, these methods have advantages such as greater utilization of dc sources but usually at the expense of more complex implementation. The time-domain approaches are derived from the control of basic two-level VSI and they can be broadly categorized into carrier based PWM techniques and multilevel selective harmonic elimination (SHE) [100]. However, selective harmonic mitigation (SHM), third-harmonic injection [101] and synchronized optimum PWM are also derived by making few remarkable modifications on the SHE and carrier based PWM schemes. SHE scheme operates at fundamental frequency and has an advantage of achieving a better efficiency with low switching losses. However, involvement of multiple offline computations and look-up tables increases the computational burden on digital interface control boards. Moreover, SHE scheme produces slow dynamic response and complex to implement for closed-loop system in real-time applications.

On the other hand, carrier based PWM schemes are the most popular [16, 98] and widely accepted schemes due to their easiness in implementation and realization of switching logic on digital controllers. phase-shifted PWM (PSPWM) and level-shifted PWM (LSPWM) are the

popular carrier based PWM schemes reported for classical MLIs [20]. These techniques are the natural extensions of carrier-based sinusoidal PWM technique used for two-level inverters. Both PSPWM and LSPWM involve sine wave as modulating signal and (m–1) carriers to obtain m levels in phase-voltage. Carriers in PSPWM are shifted on time scale whereas, the carriers in LSPWM are shifted in dc level [20]. However, both the methods have their own merits and limitations. Carriers in PSPWM are of equal magnitude and frequency but shifted in phase. Phase-shift among the carriers ensures to rotate the switching pulses such that all the switches are operated with equal switching frequency. This results in uniform conduction losses and naturally balance the dc link capacitor voltages. However, this scheme results in poor line-voltage THD and can be applicable only to the topologies with multiple switching redundancies such as CHB and FCMLI [102].

Carriers in LSPWM are vertically disposed such that the bands they occupy are contiguous. Depending upon arrangement of these level shifted carriers, LSWPM is classified into three types named as LSPWM-IPD (in-phase disposition), LSPWM-OPD (opposite phase disposition) and LSPWM-APD (alternate phase disposition) [20, 102]. The switching logic to implement all the three LSPWM approaches is same. However, compared to OPD and APD, IPD produces best harmonic profile. This is due to the nature of IPD, where harmonics in consecutive phase-voltages are in co-phasal, which dissolves the dominant harmonic in line-voltages [102]. Thus, LSPWM-IPD is more often reported for controlling three-phase MLIs. However, the switching pattern of LSPWM is not uniform and produces unequal device conduction periods. This resulted in smaller market penetration of LSPWM even in input transformer-less application such as grid-connected PV system, APF, FACTS, EV, UPS, and magnetic resonance imaging (MRI). To distribute the switching and conduction losses evenly, the switching patterns should be rotated and these carrier rotation schemes are presented in [103-108]. These carriers can be rotated either at the end of each modulating cycle or at the end of carrier cycle. Both the schemes are well reported in [109].

To obtain m levels in phase-voltage, LSPWM or PSPWM schemes require (m–1) carriers and each carrier is used to control a pair of complementary switching devices. On the other hand, to obtain m levels in phase-voltage, RSC-MLI topologies require less number of switches when compared to conventional MLIs. Therefore, these modulation schemes are not directly applicable to control RSC-MLIs and led path for development of novel modulation schemes.

3.2 Conventional modulation schemes of RSC-MLI

The significant reduction in switch count of RSC-MLI topologies has simplified their circuit configuration such that each switch may involve in attaining more than one voltage level. Asymmetrical RSC-MLIs further reduced the switch count and made the topologies much

simpler. However, significant reduction in switch count have certainty reduced the redundancies and modified the switching combination such that devices conducting at lower level may not remain in conduction at higher level. This acted as a limitation of the conventional carrier based schemes such as LSPWM and PSPWM to control RSC-MLIs topologies.

Thus, to serve the purpose of controlling any RSC-MLIs, SHE is most often preferred as an alternative. SHE is a low frequency switching scheme and is reported for various asymmetrical RSC-MLI such as E-type [64]. In this scheme, switching angles changes with the modulation index (m_a) and involves pre-determined look-up tables to select the switching angles. Space vector (SVPWM) reported for PUC, nested cell and various three-phase RSC-MLI topologies require elusive calculations to obtain switching instants [71-73, 99]. Thus, implementation of these schemes for closed-loop applications is very complex and requires expensive real-time digital controllers. On the other hand, hybrid PWM is another popular scheme reported for implementing asymmetrical cascaded topologies such as CHB [38, 89, 110]. This scheme can also be implemented for non-cascaded topologies such as SSPS, by adding an additional H-bridge in each phase [62]. This scheme requires measurement or estimation of output voltage of the higher voltage bridge/units, to derive the reference signal for lower voltage bridge/units. Hence, any lag or errors in the estimation or measurement will impact the output voltage.

Switching schemes using low frequency carrier (50 or 100 Hz) with and without logical operators are reported for various RSC-MLIs such as MLDCL, CBSC, basic unit, T-type and hybrid T-type [53, 59, 65, 66, 69, 73, 86, 89]. These low frequency PWM schemes are easy to realize but produces lower order harmonics and results in poor THD. Therefore, to control RSC-MLI with simplified switching logic and produce good harmonic profile, novel carrier based PWM schemes are reported [55-58, 60, 77, 87, 88, 91, 95]. Among them multi-reference [58, 60, 87, 88], reduced carrier [55-57, 95] and hybrid switching function [77, 91] are the most popular PWM schemes reported for controlling various symmetrical and asymmetrical RSC-MLI topologies. However, all these novel schemes possess their own limitations in terms of carrier and modulating signal arrangement, switching logic implementation and computational burden. Next section of this chapter discusses the merits and limitations of each modulation scheme in controlling RSC-MLIs and elevates their adverse effects on harmonic performance of the inverter.

3.2.1 Multi reference modulation scheme

Multi reference modulation is a single carrier based PWM scheme and is reported for T-type, cascaded T-type and few other cascaded RSC-MLI topologies [58, 60, 87, 88]. This is a generalized scheme, which can be easily scalable to any number of levels. This scheme produce

switching pulses by comparing multiple unipolar sinusoidal dc shifted references with a unipolar carrier signal. To obtain *m* levels in phase-voltage, this scheme involves (*m*–1)/2 dc shifted references. The dc shifted references are obtained by shifting the unipolar sinusoidal reference with the carrier signal peak.

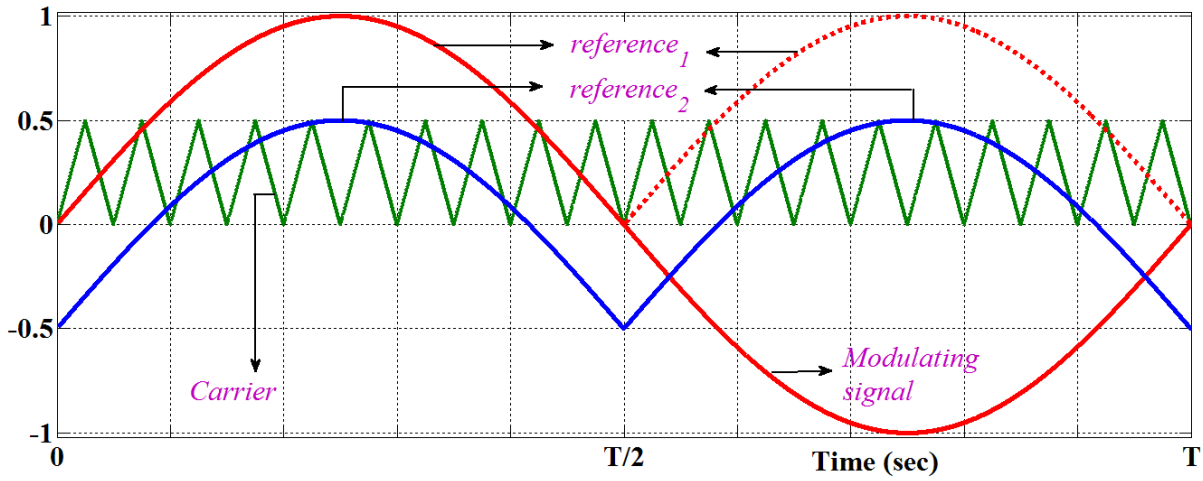


Fig. 3.1: Carrier and modulating signal arrangement of multi reference modulation scheme to obtain five-levels in phase-voltage.

To obtain five-levels in phase-voltage, multi reference scheme requires two dc shifted references i.e., *reference*$_1$ and *reference*$_2$, and one unipolar carrier signal as shown in Fig. 3.1. *Reference*$_1$ is the unipolar modulating signal and *reference*$_2$ is obtained by dc off-shifting *reference*$_1$ by carrier peak value. Comparison of *reference*$_1$ with the carrier obtains voltage band between 0 and *V* in phase-voltage. Similarly, comparison of *reference*$_2$ with the carrier obtains voltage band between *V* and 2*V* in phase-voltage. *Reference*$_1$ is compared with the carrier, if the instantaneous value of the *refrerence*$_1$ is less than the carrier peak. If the *reference*$_1$ is greater than carrier, then *reference*$_2$ is compared with the carrier and this goes on for the higher levels.

Comparison of *reference*$_1$ and carrier signal, obtains voltage band between 0 and *V* such that zero-level is obtained, if the *reference*$_1$ is less than the carrier and, *V* level is obtained if the *reference*$_1$ is greater than the carrier. Similarly comparison of *reference*$_2$ and carrier signal, obtains voltage band between *V* and 2*V*, where *V* level is obtained if the *reference*$_2$ is less than the carrier and 2*V* level is obtained if the *reference*$_2$ is greater than carrier. However, polarity of these voltage levels is decided by the polarity of the modulating signals such that positive and negative levels are obtained for the positive and negative half of the modulating signal respectively. Switching logic of this multi reference modulation scheme can control any RSC-MLI irrespective of the voltage ratios and topological arrangement [58, 60, 87, 88]. In literature, this multi reference modulation scheme is reported for T-type RSC-MLI. Fig. 3.2 shows circuit configuration of three-phase five-level T-type RSC-MLI.

Operation of the T-type MLI for five-levels in phase-voltage: To obtain five-levels in phase-voltage, i.e., 2*V*, *V*, 0, –*V*, and –2*V*, two dc sources in each phase are required. Switching states to obtain desired voltage level in phase-*a* are shown in Table 3.1.

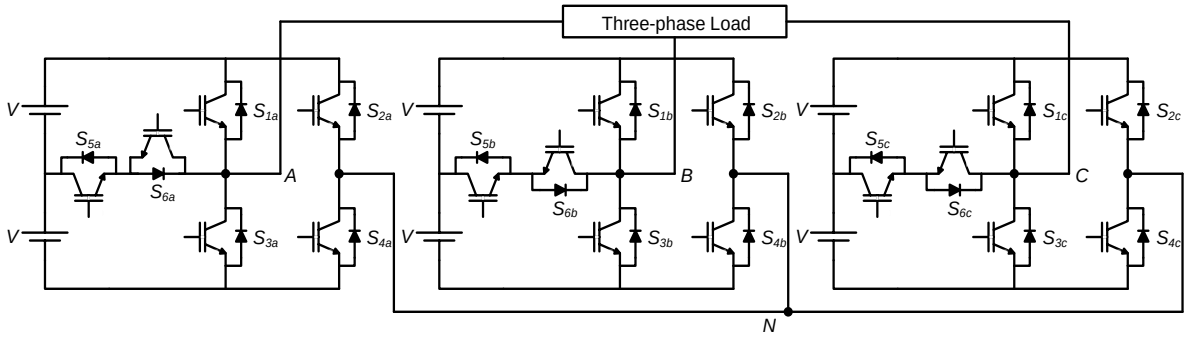


Fig. 3.2: Three-phase five-level T-type RSC-MLI.

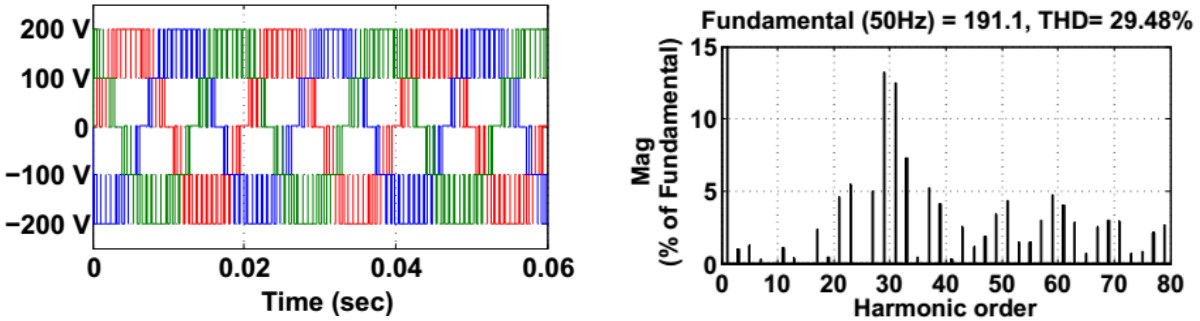
Table 3.1: Switching states of five-level T-type RSC-MLI.

Switches in conduction	**Voltage level (v_{an})**
S_{5a} and S_{4a}	$+V$
S_{1a} and S_{4a}	$+2V$
(S_{1a} and S_{2a}) or (S_{3a} and S_{4a})	0
S_{6a} and S_{2a}	$-V$
S_{3a} and S_{2a}	$-2V$

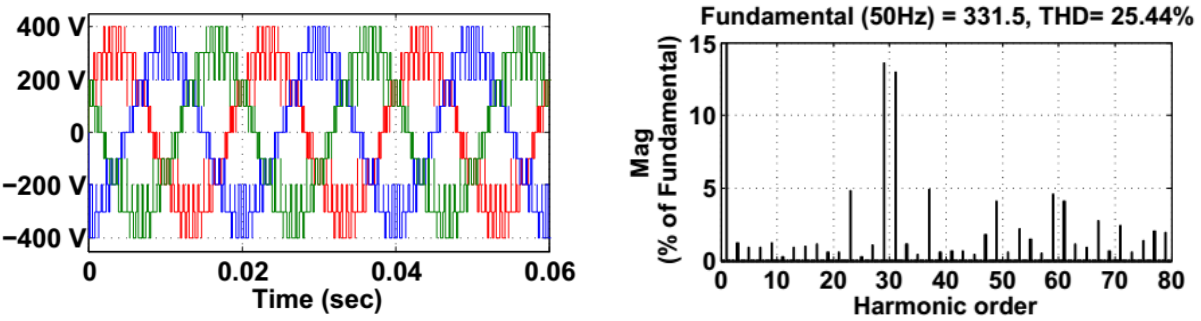
3.2.1.1 Performance evaluation

The performance of five-level T-type MLI with multi reference PWM scheme is evaluated in MATLAB/Simulink environment. Each dc source voltage of 100 V and an *RL* load of 2 kW, 0.9 power factor (PF) are considered. Carrier and modulating signal frequency are selected as 1.5 kHz and 50 Hz respectively. Simulation is carried out at amplitude modulation index (m_a) of 0.95. The obtained output voltage and current are shown in Fig. 3.3, where Fig. 3.3(a), (b) and (c) depict the waveform and harmonic spectra of phase-voltage, line-voltage and line-currents respectively. From Fig. 3.3, the following observations are made:

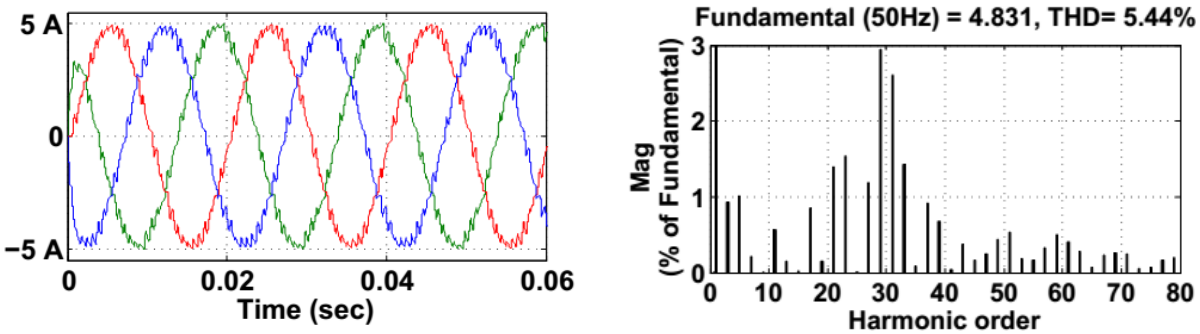
- The phase-voltage THD is obtained as 29.48% with side band harmonics are centred at m_f = 30, with dominant harmonics at $m_f \pm 1$.
- Line-voltage THD is 25.44% and line-current THD is 5.44%.
- Side band harmonics in line-voltage are similar to phase-voltage, except the absence of triplen harmonics.
- Amplitude of harmonic component at integer multiples of carrier frequency is zero. Odd order harmonics appear in the side band centred at integer multiples of carrier frequency.



(a) Phase-voltage



(b) Line-voltage



(c) Line-current

Fig. 3.3: Performance of five-level T-type RSC-MLI with multi reference modulation scheme.

3.2.1.2 Comparative analysis

To investigate the harmonic performance of conventional multi reference modulation scheme, the obtained phase and line-voltage THD performance shown in Fig. 3.3 is compared with the performance of LSPWM-IPD. Among the carrier based PWM schemes reported in literature, LSPWM-IPD is the most popular scheme due to its clean THD performance and is often considered as the benchmark [102].

Fig. 3.4 depicts the comparative harmonic performance of conventional multi reference modulation scheme on a five-level T-type RSC-MLI and LSPWM-IPD scheme on five-level CHB-MLI for m_f = 30 at different modulation indices (m_a). From Fig. 3.4, it is observed that the conventional multi reference modulation results in high THD in line-voltages compared to LSPWM-IPD modulation.

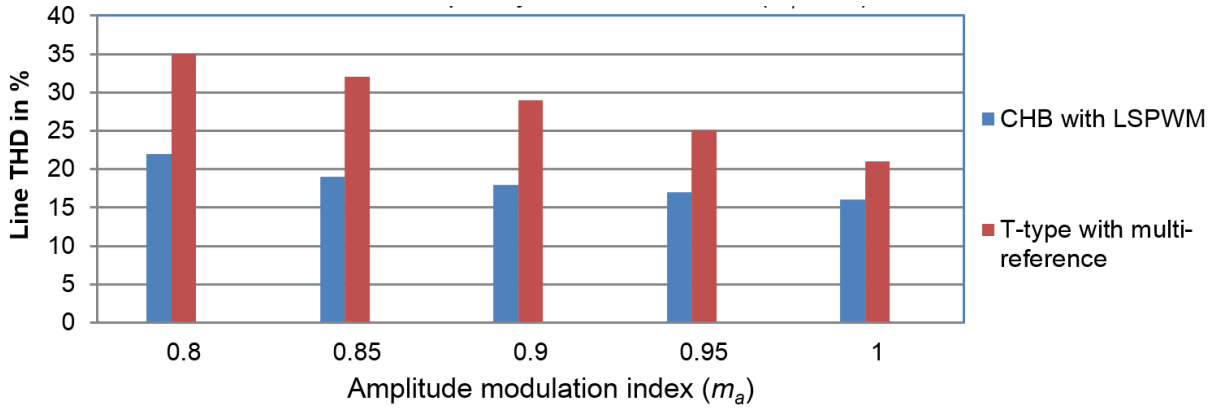
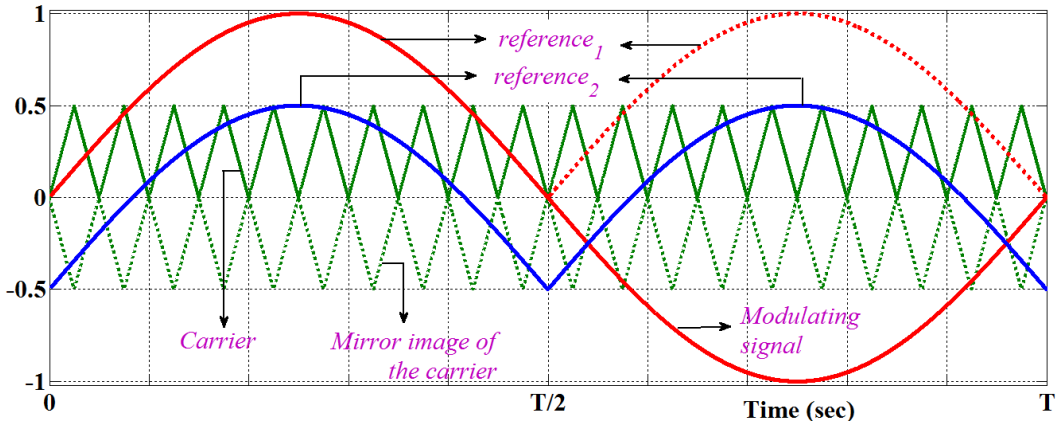


Fig. 3.4: Line-voltage harmonic performance of multi reference and LSPWM schemes for $m_f = 30$.

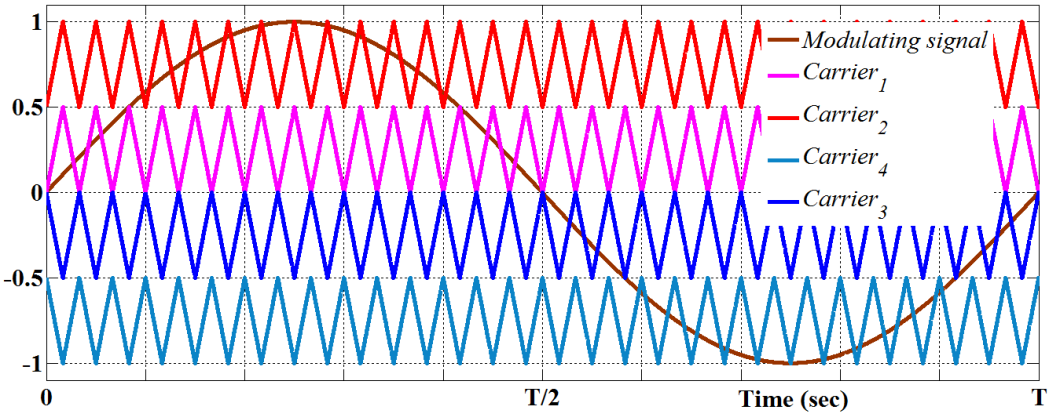
3.2.1.3 Reasons for degraded THD performance

The reason for poor THD performance of conventional multi reference scheme can be analysed by referring its carrier arrangement with LSPWM-OPD scheme as shown in Fig. 3.5. From Fig. 3.5(a) it is observed that, referring $carrier_1$ to $reference_1$ (unipolar reference) is equivalent to referring $carrier_1$ and its mirror image to positive and negative half of the modulating signal respectively. Further, the arrangement of carrier and its mirror image with respect to the modulating signal shown in Fig. 3.5(a) resembles the position of carriers in LSPWM-OPD scheme shown in Fig. 3.5(b). Thus, examination of Fig. 3.5(a) and (b) reveals that carrier arrangement in multi reference PWM is identical to LSPWM-OPD. This can be further confirmed by observing harmonic performance of these conventional schemes. For $m_a = 0.95$ and $m_f = 30$, Fig. 3.6 shows the harmonic performance of LSPWM-OPD on a five-level CHB, where Fig. 3.6(a) and (b) shows the waveform and harmonic spectra of phase and line-voltages respectively. In LSPWM-OPD, the side band harmonics are centred at integer multiples of m_f and their respective THD values are similar to Fig. 3.3. Further, Fig. 3.5 and Fig. 3.6, verifies that the performance of multi reference PWM is similar to LSWPM-OPD.

In literature, LSPWM-OPD is not preferred for three-phase MLIs, due to its degraded line-voltage THD performance [102]. Therefore, referring this conventional multi reference modulation scheme to any RSC-MLI configuration results in poor line-voltage THD.

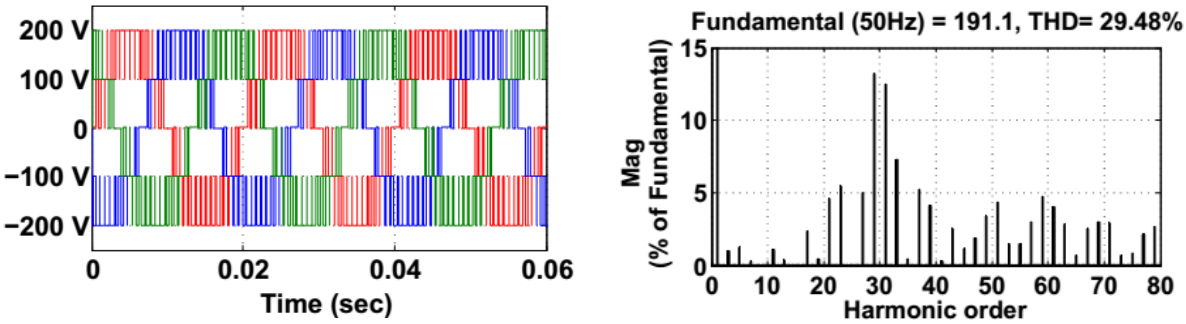


(a) Carrier arrangement in multi reference modulation scheme

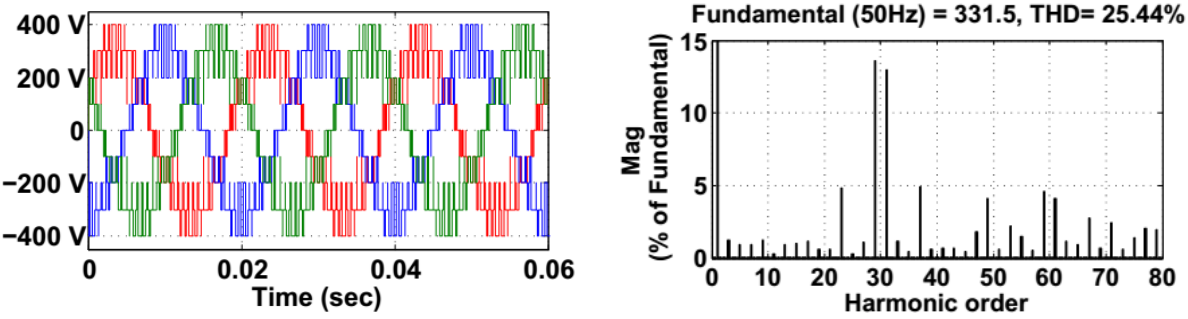


(b) Carrier arrangement in LSPWM-OPD

Fig. 3.5: Carrier arrangement in multi reference and LSPWM-OPD schemes.



(a) Phase-voltage



(b) Line-voltage

Fig. 3.6: Performance of LSPWM-OPD on five-level CHB MLI.

3.2.1.4 Experimental validation

To examine the performance of the conventional multi reference modulation scheme experimentally, a prototype of a five-level T-type RSC-MLI is developed with generalized 24 switch IGBT inverter module (explained in Appendix - A). Firing pulses for switching devices are obtained from dSPACE-1104 R&D controller with dead-time delay of 1 μs. The input dc voltage to the prototype is provided by isolated dc regulated power supplies (RPS). The experimental results are recorded for m_f = 30, m_a = 0.95 and controller sampling period of 50 μs. The considered experimental parameters to develop a prototype of five-level T-type RSC-MLI are given in Table 3.2.

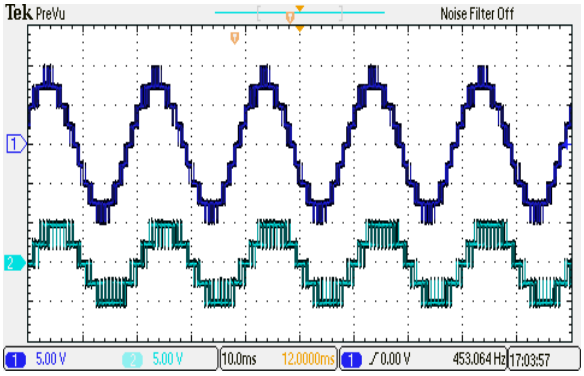
Table 3.2: Experimental parameters.

Circuit	**Component**	**Specification - Type**
Input dc voltage	Isolated regulated dc power supplies	25 V/3 A and 25 V/5 A
Power circuit	Switching device (IGBT) with anti-parallel diode	1200 V/40 A
Controller	dSPACE Sampling time	DS1104 R&D Controller Board 50 μs
THD measurement	Power quality analyser	Fluke 435 Series II

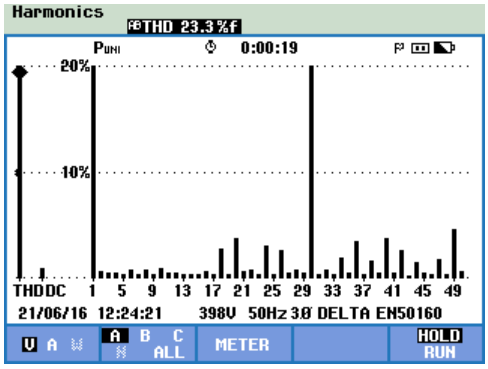
To evaluate the performance of multi reference PWM, its THD performance on five-level T-type RSC-MLI is compared with conventional LSPWM on five-level CHB. Thus, a prototype of five-level CHB is also developed using the generalized inverter module for the same experimental parameters given in Table 3.2.

Conventional LSPWM-IPD and OPD:

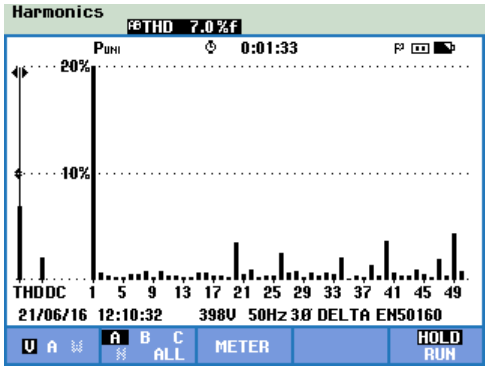
The line and phase-voltage performance of developed five-level CHB with conventional LSPWM-IPD and OPD schemes is shown in Fig. 3.7 and Fig. 3.8, respectively. The obtained phase and line-voltage waveforms with LSPWM-IPD are depicted in Fig. 3.7(a) and their corresponding harmonic spectra in Fig. 3.7(b) and (c), respectively. In Fig. 3.7(a), the top trace depicts the nine-level line-voltage and the bottom trace is five-level phase-voltage. As the experiment is demonstrated for 1500 Hz carrier frequency, the obtained phase and line-voltage harmonic spectra shown in Fig. 3.7(b) and (c) are centred at m_f = 30. The experimental phase-voltage THD is recorded as 23.3% and line-voltage THD as 7.0%. Fig. 3.7(b) shows the presence of dominant harmonic at carrier frequency, with all lower order harmonics being suppressed. It is to be noted that presence of dominant harmonic component (more than 20%) at m_f is resulting in high THD in phase-voltage, even though the magnitude of its side band harmonics are relatively low (less than 4%). However, the co-phasal nature of the side band harmonics in consecutive phases, results in cancellation of this dominant harmonic in line-voltage. This results an appreciable difference in phase and line-voltage THDs.



(a) Line and phase-voltage waveforms (X-axis: 10 ms/div. and Y-axis: 50 V/div.)

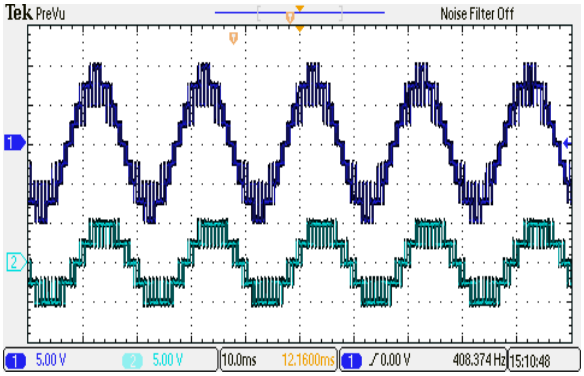


(b) Phase-voltage harmonic spectrum

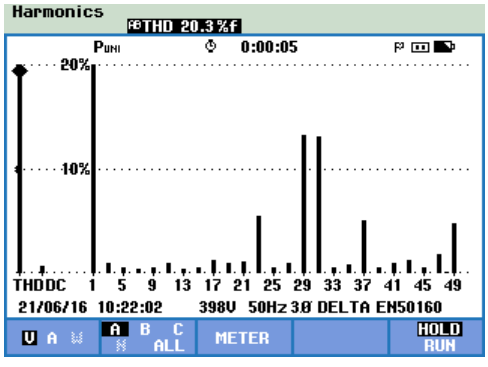


(c) Line-voltage harmonic spectrum

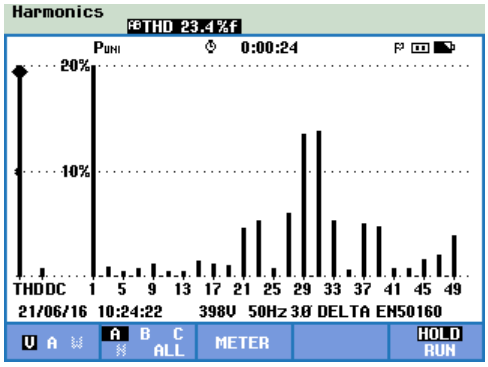
Fig. 3.7: Experimental performance of LSPWM-IPD scheme on five-level CHB MLI.



(a) Line and phase-voltage waveforms (X-axis: 10 ms/div. and Y-axis: 50 V/div.)



(b) Phase-voltage harmonic spectrum



(c) Line-voltage harmonic spectrum

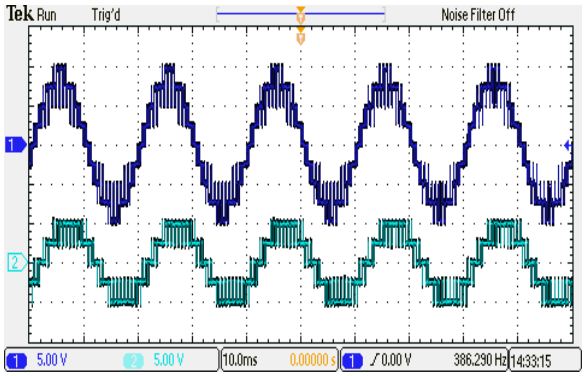
Fig. 3.8: Experimental performance of LSPWM-OPD scheme on five-level CHB MLI.

The inverter phase and line-voltage waveforms with LSWPM-OPD are depicted in Fig. 3.8(a) and their corresponding harmonic spectra are depicted in Fig. 3.8(b) and (c) respectively.

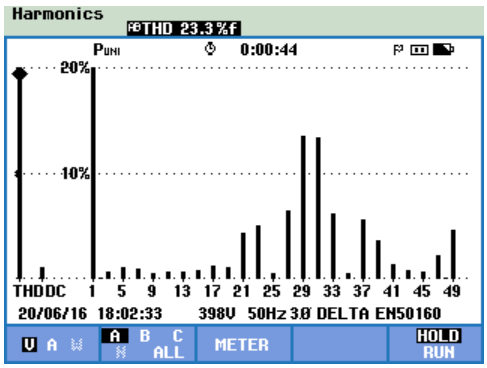
Inverter phase-voltage levels shown in Fig. 3.8(a) (Trace-2) appears to be clean and uniform as similar to LSPWM-IPD shown in Fig. 3.7(a) (Trace-2). However, this is not true for line-voltages. The levels in line-voltage of LSPWM-OPD shown in Fig. 3.8(a) (Trace-1) appears to be over-lapped at higher voltage levels. These distortions in line-voltage results in high THD. In Fig. 3.8, phase-voltage THD is recorded as 20.3% and line-voltage THD as 23.4%. In both phase and line-voltages side band harmonics are centered at m_f and triplen harmonics are absent in line-voltages. Therefore, the recorded experimental results justifies the inferior line-voltage THD performance of LSPWM-OPD over LSPWM-IPD.

Conventional multi reference PWM:

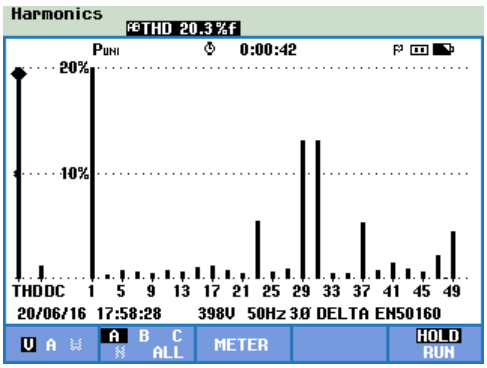
Experimental performance of the developed five-level T-type RSC-MLI with the conventional multi reference PWM is recorded and shown in Fig. 3.9. The obtained phase and line-voltage waveforms are depicted in Fig. 3.9(a), with their corresponding harmonic spectra shown in Fig. 3.9(b) and (c), respectively. The experimentally recorded phase and line-voltage THD are 23.4% and 20.3%, respectively. The side-band harmonics are absent at m_f, but appeared in the side bands of m_f. The results shown in Fig. 3.8 and Fig. 3.9 are identical in terms of waveform shape and harmonic performance. Comparing the performance of multi reference modulation scheme shown in Fig. 3.9, with LSWPM-IPD shown in Fig. 3.7, verifies its poor line-voltage THD.



(a) Line and phase-voltage waveforms (X-axis: 10 ms/div. and Y-axis: 50 V/div.)



(b) Phase-voltage harmonic spectrum



(c) Line-voltage harmonic spectrum

Fig. 3.9: Experimental performance of multi reference PWM scheme for five-level T-type RSC-MLI.

3.2.2 Reduced carrier PWM

Reduced carrier PWM [55-57, 95] involves a unipolar modulating and (m–1)/2 unipolar level shifted carrier signals to obtain m-levels in phase-voltage. Among the various carrier based PWM schemes, this scheme is simplest and can be easily realizable on digital platforms. However, this scheme possess few limitations due to its nature of switching logic and carrier signal arrangement. The switching pulses are obtained by comparing unipolar reference and carrier signals. These pulses are responsible for producing positive voltage levels for positive half of the modulating signal and negative voltage levels for negative half. Carrier and modulating signal arrangement of reduced carrier PWM to control five-level inverter is shown in Fig. 3.10. The switching pulse (P_2) is obtained by comparing *reference* and *carrier*$_2$, as shown in Fig. 3.10. The pulse P_2, actively varying from 0 to 1, when the *reference* is in *carrier*$_2$ limits, and due this active switching, a voltage band of V to 2V is obtained in phase-voltage.

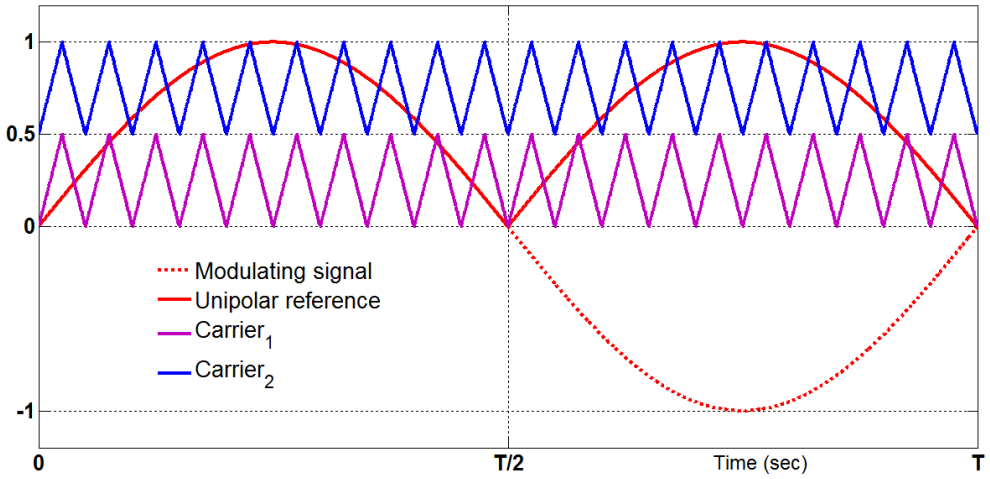
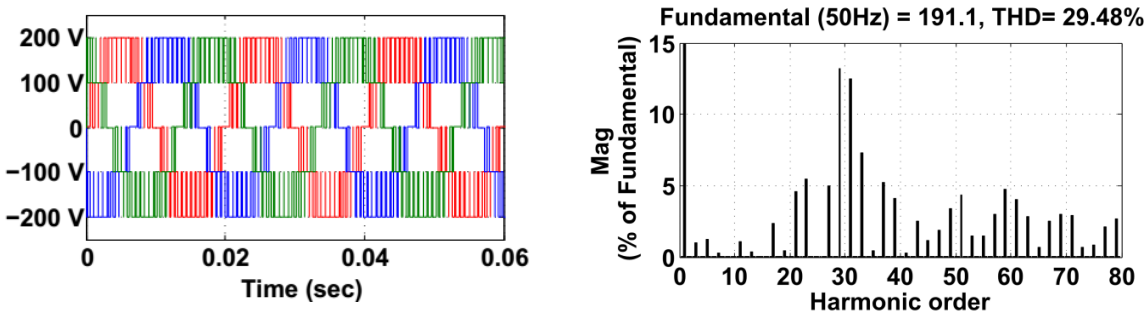


Fig. 3.10: Carrier and modulating signal arrangement of conventional reduced carrier PWM for five-levels in phase-voltage.

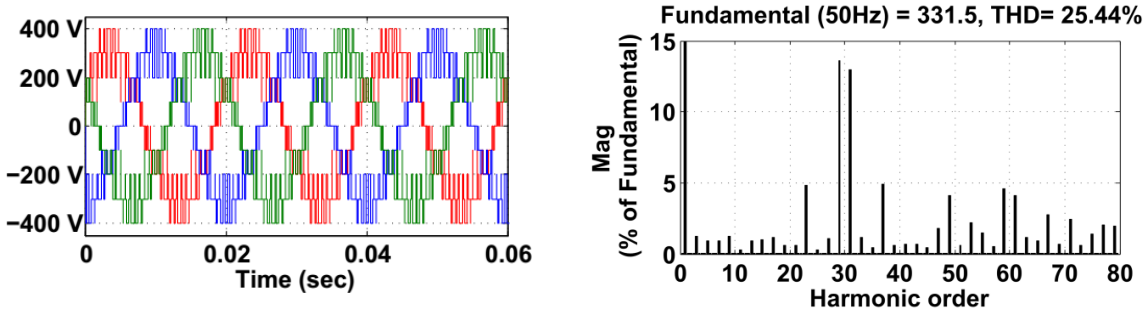
Similarly, when the *reference* is in the limits of *carrier*$_1$, switching pulse (P_1) is obtained and is responsible for obtaining 0 to V band in phase-voltage. However, this pulse remains to be active high even though the *reference* is above *carrier*$_1$ limits. Thus, applying this pulse directly to control an inverter ensures the switching devices responsible for obtaining lower level (V level) to remain in conduction at higher levels (2V level) as well. Therefore, this nature of switching is not suitable for direct application to control RSC-MLIs.

Hence, reduced carrier PWM with logical expressions are reported, where the pulses are obtained by comparing unipolar reference and carrier signals. Further, these pulses are operated with user defined logical expressions such that they meet the switching action of the inverter to be controlled. Among the carrier based PWM schemes reported for RSC-MLI, reduced carrier PWM scheme with logical operations are the simplest. However, the nature of the reported logical expressions are not generalized and vary with inverter topological arrangement.

Performance of reduced carrier PWM on five-level MLDCL inverter is shown in Fig. 3.11, where the corresponding waveform and harmonic spectra of the obtained phase and line-voltage are given in Fig. 3.11(a) and (b) respectively. From these results, it is observed that reduced carrier PWM scheme results THD of 29.48% in phase-voltage and 25.44% in line-voltage.



(a) Phase-voltage



(b) Line-voltage

Fig. 3.11: Harmonic performance of conventional reduced carrier PWM on five-level inverter.

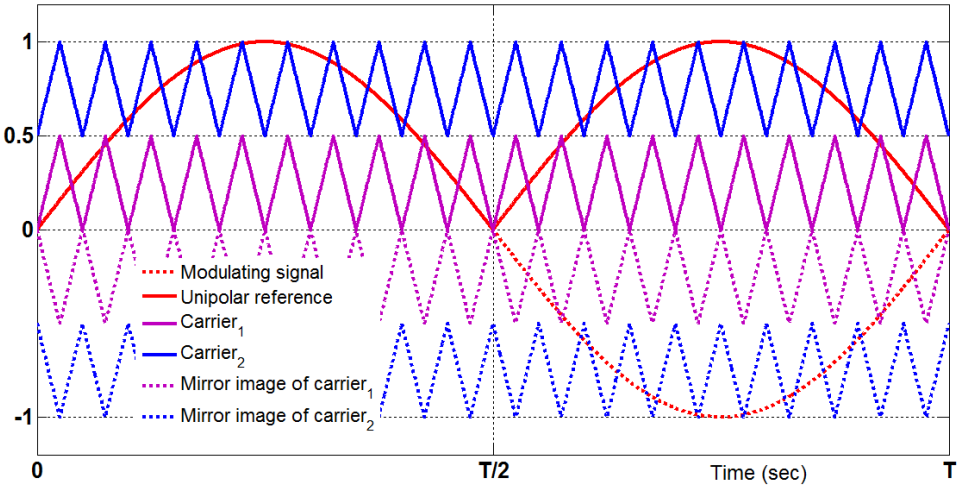


Fig. 3.12: Carrier arrangement of reduced carrier PWM in terms of LSWPWM-OPD.

The obtained wave shape and harmonic performance of both phase and line-voltages shown in Fig. 3.11 are similar to the results obtained from LSPWM-OPD and conventional multi reference PWM schemes shown in Fig. 3.6 and Fig. 3.3 respectively. Therefore, similar to LSPWM-OPD and multi reference PWM, this conventional reduced carrier PWM also results in poor harmonic performance with high THD in line-voltages. This is due to the carrier

arrangement of reduced carrier PWM scheme being equivalent to LSPWM-OPD, which can be verified from Fig. 3.12.

Thus from the above analysis, it can be concluded that conventional reduced carrier PWM scheme suffers with high THD in line-voltage and cannot applicable to most of the RSC-MLIs.

3.2.3 Hybrid switching function PWM

Hybrid switching function PWM is one of the novel modulation scheme reported for many symmetrical and asymmetrical RSC-MLIs such as PUC, switched dc sources and hybrid T-type topologies [77, 91]. Carrier and modulating signal arrangement of this PWM scheme is similar to LSPWM-IPD and involves (*m*–1) carriers to obtain *m* levels in phase-voltage. The switching logic of this scheme is well suited for implementing any RSC-MLI. This scheme develops a hybrid function using minimum and maximum limits of each carrier.

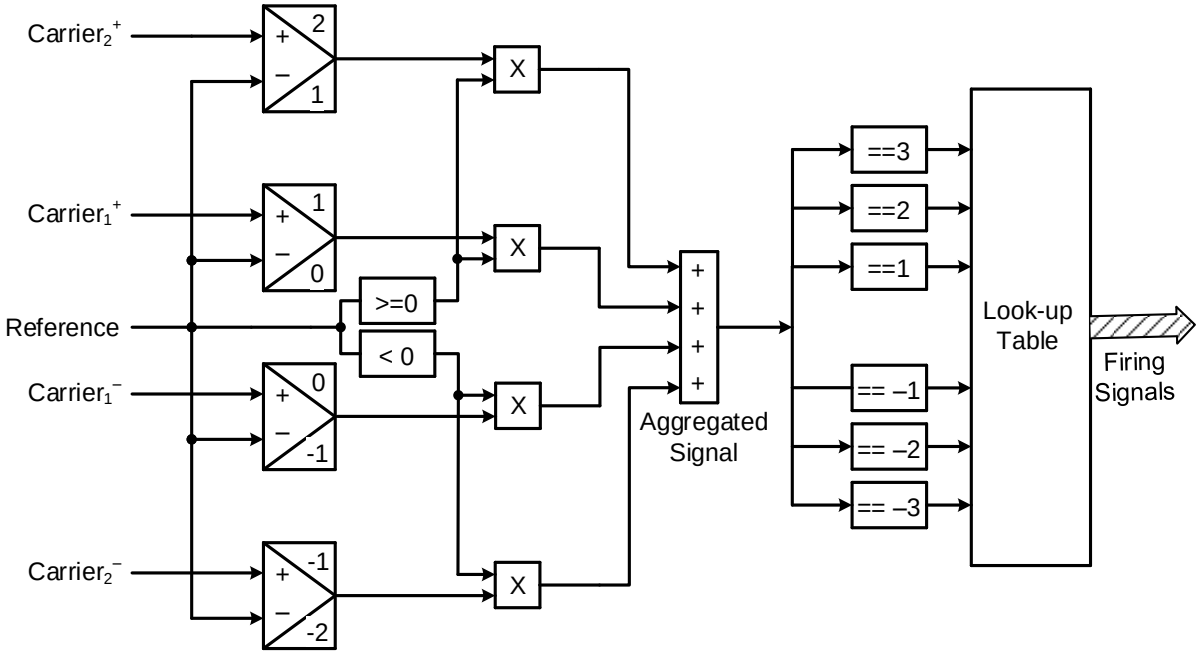


Fig. 3.13: Hybrid switching function PWM for five-levels in phase-voltage.

Fig. 3.13 shows the implementation of hybrid switching function PWM to obtain five-levels in phase-voltage. The obtained pulses can be applied to a five-level inverter with the help of look-up table. In detail, if the reference is greater than each carrier, a value equal to carrier peak is obtained otherwise, a value equal to the respective carrier minimum is obtained. Based on the polarity of modulating signal, the obtained values are aggregated to decide the voltage level to be obtained. Thus, the aggregated signal is given to a look-up table to obtain switching pulses.

Therefore, this method requires a look-up table for selection of appropriate switching devices to achieve the required voltage level. This method can be applicable for any RSC-MLI and is readily scalable. However, the involvement of (*m*–1) carriers, realization of switching

function and requirement of 2(m–1) comparators increases the computational burden of this control scheme at higher levels.

3.3 Summary of conventional PWM schemes for RSC-MLIs

By reviewing the modulation schemes reported for RSC-MLIs, a summary of various PWM schemes is given in Table 3.3. From this, the following conclusions can be drawn.

- Low frequency switching schemes such as SHE results in lower order harmonics. PWM schemes such as SHE and SVM involve complex mathematical calculations which increases the complexity of the controller in closed-loop applications. Further, generalizing these schemes to higher levels is an elusive task.
- Multi reference modulation is a generalized scheme reported for various symmetrical and asymmetrical RSC-MLIs. However, the performance of this scheme results high THD in line-voltage. Also, requirement of multiple dc off shifted references increases the complexity in realizing the controller.
- Switching function PWM is other carrier based PWM scheme which can be applicable for any RSC-MLIs and results in satisfactory THD performance. However to realize the switching logic, controller requires numerous comparators, which increases the complexity and computational burden at higher levels.
- Among the modulation schemes reported for RSC-MLIs, reduced carrier PWM scheme with logical expressions are the simplest. However, these logical expressions are not generalized and vary with inverter topology and number of levels.

Therefore, to overcome the limitations of conventional PWM schemes in controlling RSC-MLIs, simple carrier based PWM schemes are proposed in next section.

Table 3.3: Summary of various RSC-MLI and their reported modulation schemes.

Topology	Topology description	Symmetrical / Asymmetrical	Modulation schemes reported in literature		Demerits of the modulation scheme
			Symmetrical	Asymmetrical	
MLDCL [53]	Separate level and polarity generators	Both	Low frequency switching scheme		Complicated at higher levels and poor THD
PUC [99]	Can be extended with and without cascading	Both	SVPWM		Complicated at higher levels
CBSC [69]	can be extended with and without cascading	Both	Low frequency switching scheme		Complicated at higher levels and poor THD
RV [55]	Separate level and polarity generators	Both	Reduced carrier PWM		Poor THD in line-voltage
Switched dc sources [91]	Involves separate dc link for all phases	Both	Switching function PWM		Increased computation burden at higher levels
SSPS [62, 63]	Separate level and polarity generators	Both	LSPWM with maximum and minimum conditions [63]	Hybrid PWM [62]	Increased comparisons at higher levels [63]
SCSS [77]	Separate level and polarity generators	Symmetrical	Switching function PWM at low frequency		Complicated at higher levels
T-type [56-60]	T-type: Extended without cascading [56-58]	Symmetrical	Multi reference PWM [58] Reduced carrier with logic gates [56, 57]		Poor THD in line voltages [56-58]
	Cascaded T-type: Extended with and without cascading [59, 60]	Both	Fundamental frequency switching [59] Phase shifted multi reference [60]		Complicated at higher levels [59] and Poor THD [59, 60]
Basic unit MLI [86]	Separate level and polarity generators	Both	An algorithm based PWM		Complicated at higher levels and poor THD
Nested cell [71]	Common dc link to all phases	Both	SVPWM		Complicated at higher levels
Hybrid T-type [65, 66]	Can be extended with and without cascading	Both	Low frequency carrier switching [65, 66]	Low frequency switching [66]	Complicated at higher levels and poor THD [65, 66]
E-type [64]	Extended by cascading	Asymmetrical		SHE	Complicated at higher levels and slow dynamic response
Reduced cascaded [67, 87, 88, 110]	Extended to higher level by cascading	Both [67, 110]		Hybrid PWM [110]	Mixed frequency modulation scheme
		Symmetrical [88]	Multi reference with logic gates [88]		Complicated at higher levels and poor THD
		Asymmetrical [87]		Multi reference-low frequency carrier [87]	Complicated at higher levels and poor THD
Switched capacitor RSC-MLI [90]	Extended by cascading or series connection of capacitor units	Symmetrical	Fundamental switching scheme		Complicated at higher levels and poor THD
Split-capacitor MLI [89]	Extended by series connection of capacitor units	Both		Hybrid PWM	Mixed frequency modulation scheme
RSC-MLI with 3-phase [72, 73, 95]	With common dc link to three phases [72, 73]	Asymmetrical [72, 73]	Low frequency reduced carrier using logical operators [95]	SVPWM [72, 73]	Complicated at higher levels [72, 73, 95] and poor THD [95]
	Separate dc link to three-phases [95]	Symmetrical [95]			

3.4 Modified PWM schemes for RSC-MLIs

Among the PWM schemes reported for RSC-MLIs, schemes with unipolar carrier and modulating signal arrangement such as multi reference and reduced carrier are easy to realize on digital platforms due to symmetric switching logic implementation for positive and negative half of the modulating signal. However, the carrier arrangement of these schemes is produces high THD in line-voltages and requires necessary modifications to improve their THD performance. This section proposes two PWM schemes with modified carrier arrangement. They are:

- ❖ Modified multi reference dual carrier PWM
- ❖ Modified reduced carrier PWM

Methodology and superiority of these modified PWM schemes are explained below.

3.4.1 Modified multi reference dual carrier PWM

One possible approach to improve THD performance of the conventional multi reference modulation scheme is to change its carrier's position, such that its arrangement is equivalent to LSPWM-IPD as referred in section 3.2.1.3. Hence, a modified multi reference dual carrier modulation scheme is presented in this section. This modified scheme involves two carriers and $(m-1)/2$ dc shifted references to obtain m levels in phase-voltage. Both these carriers are of same polarity and magnitude, but opposite in phase, as shown in Fig. 3.14. Switching logic of this modified multi reference dual carrier modulation is similar to the conventional multi reference modulation, however $carrier_1$ is responsible for obtaining positive levels in output voltage whereas $carrier_2$ is involved in attaining negative voltage levels.

For a normalized modulating signal, formulae to determine the magnitude of carrier signal (V_c) and modulation index (m_a) are given in (3.1) and (3.2) respectively, where V_m is the peak of the modulating signal and m is the number of levels in phase-voltage.

$$V_c = \frac{2}{m-1} \tag{3.1}$$

$$m_a = \frac{V_m}{(m-1)V_c} \tag{3.2}$$

Arrangement of carrier and reference signals of this modified scheme to control a five-level inverter is shown in Fig. 3.14. To obtain five-levels in phase-voltage, two references, i.e., $reference_1$ and $reference_2$ are required where, $reference_1$ is in unipolar form of the modulating signal and $reference_2$ is obtained by dc off shifting $reference_1$ with carrier peak value. Comparison of $carrier_1$ with $reference_1$ and $reference_2$, produces positive levels in phase-voltage for the positive half of the modulating signal. Similarly, $carrier_2$ is involved to obtain negative voltage levels for negative half of the modulating signal. The main reason behind using

an additional carrier i.e., *carrier*$_2$ is to improve the THD performance by making its carrier alignment similar to LSPMW-IPD. This can be observed by referring Fig. 3.15, where the position of *carrier*$_1$ and mirror image of *carrier*$_2$, together resemble the position of the carriers in LSPWM-IPD modulation scheme [102].

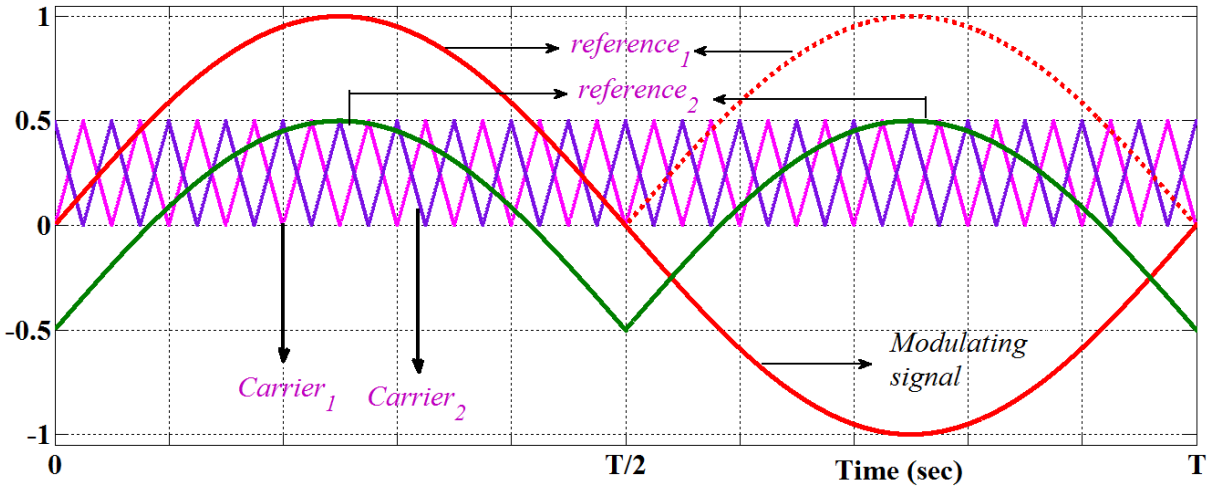


Fig. 3.14: Carrier and modulating signal arrangement of modified multi reference dual carrier PWM scheme for five-level phase-voltage.

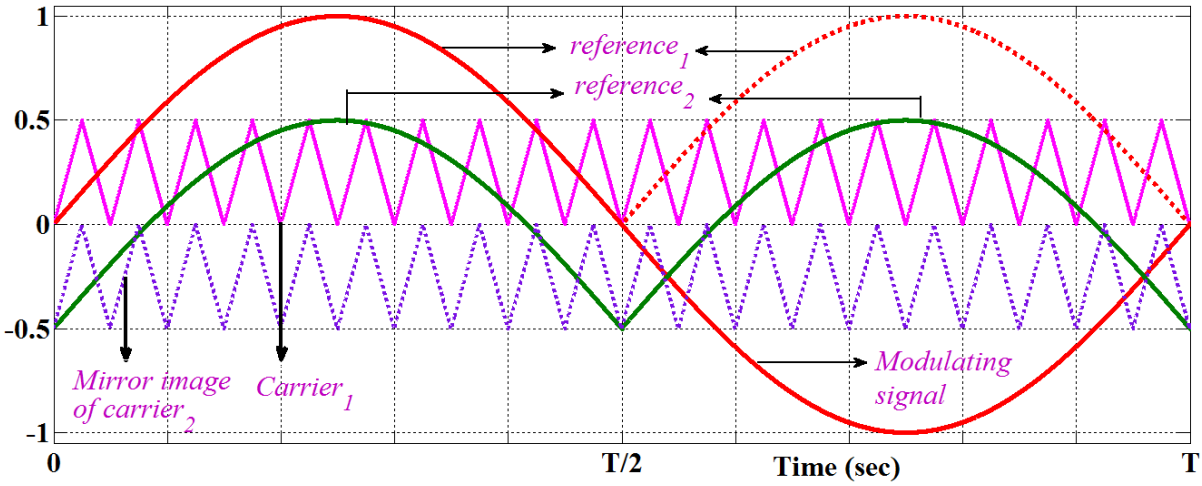
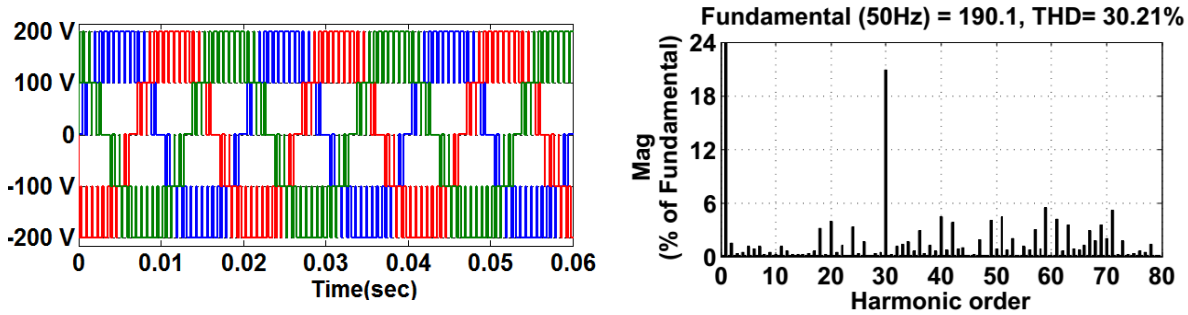


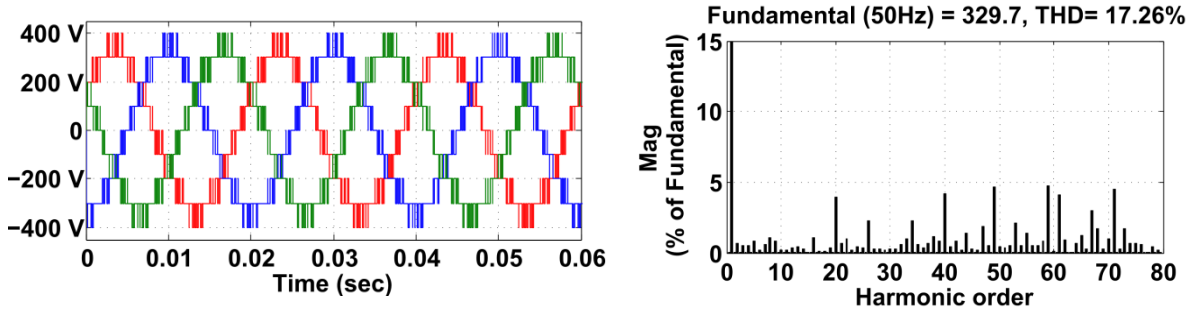
Fig. 3.15: Carrier and modulating signal arrangement of modified multi reference dual carrier PWM in terms of LSPWM-IPD.

3.4.1.1 Performance evaluation

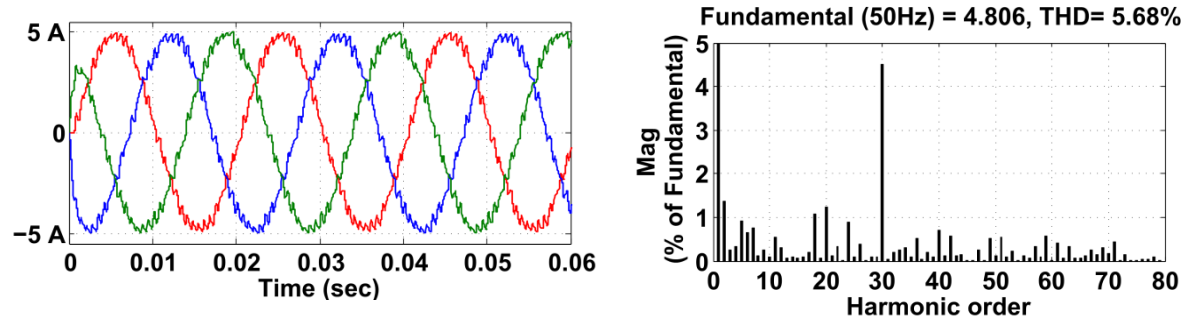
Performance analysis of modified multi reference dual carrier PWM scheme on a five-level T-type for 2 kW, 0.9 PF *RL* load, at 1500 Hz carrier frequency is shown in Fig. 3.16. Evaluation is carried out for simulation parameters given in section 3.2.1.1. The obtained phase-voltage, line-voltage, and line-currents with their harmonic spectra are depicted in Fig. 3.16(a), (b) and (c) respectively.



(a) Phase-voltage



(b) Line-voltage



(c) Line-current

Fig. 3.16: Performance of modified multi reference dual carrier PWM on five-level T-type RSC-MLI for $m_a = 0.95$.

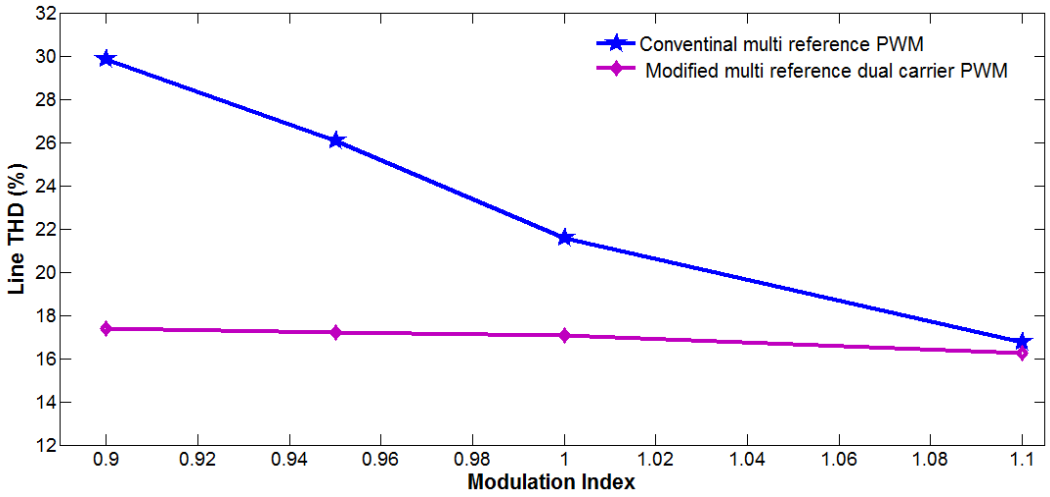
From the harmonic performance shown in Fig. 3.16, the following observations can be made.

- ❖ Amplitude of harmonic content at even multiples of carrier frequency is zero, but the dominant harmonics appear at odd multiples of carrier frequency.
- ❖ Even order harmonic components appear in the side bands centred at odd multiples of carrier frequency. Similarly, odd order harmonic components appear in the side bands centred at even multiples of carrier frequency.

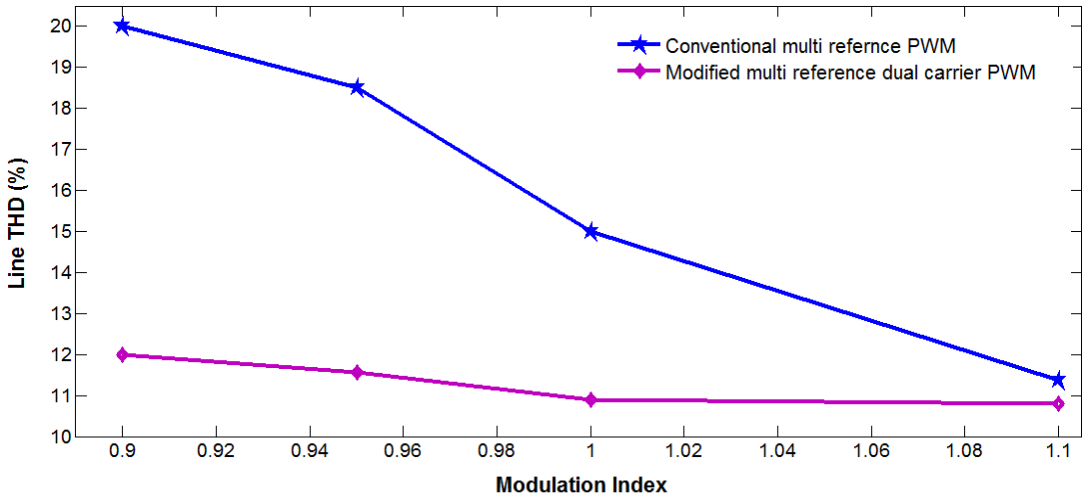
From the above observations, it can be concluded that harmonic performance of this proposed scheme is identical to LSPWM-IPD reported in [102]. It is to be noted that, even though the % of phase-voltage THD of both the modified multi reference dual carrier PWM shown in Fig. 3.16(a) and conventional multi reference PWM shown in Fig. 3.3(a) are almost same, there is an appreciable difference in their line-voltage THD. This is due to the difference in the nature of side band harmonics in their phase-voltage harmonic spectra. In modified multi reference dual carrier modulation (and LSPWM-IPD) scheme harmonics present at odd

multiples of m_f in consecutive phases are co-phasal in nature. Thus, they cancel out in line-voltages, resulting in huge reduction in line-voltage THD [102].

Further, to verify the improved THD performance of this modified PWM over the conventional multi reference PWM, a comparative THD performance of both schemes on five-level and seven-level T-type RSC-MLI for different values of m_a is shown in Fig. 3.17. Fig. 3.17(a) and (b), shows the line-voltage THD performance on five-level and seven-level respectively. From Fig. 3.17, superior line-voltage THD performance of the modified multi reference dual carrier PWM over the conventional multi reference PWM scheme can be verified.



(a) For five-level



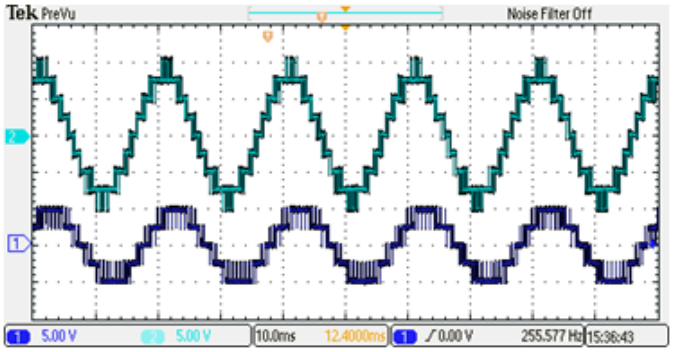
(b) For seven-level

Fig. 3.17: Comparison of line-voltage THD with modified and conventional multi reference PWM schemes for various values of m_a on T-type RSC-MLI.

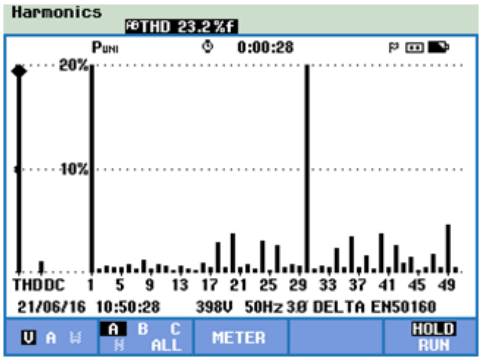
3.4.1.2 Experimental validation

An experimental set-up of five-level T-type RSC-MLI is developed to evaluate the performance of modified multi reference dual carrier modulation scheme. Experimentation is carried for the parameters considered in Table 3.2. Experimental performance of the proposed

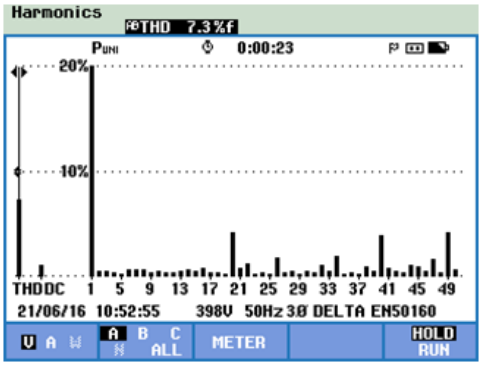
modified multi reference dual carrier modulation on five-level T-type MLI is shown in Fig. 3.18. The obtained phase and line-voltage waveforms are depicted in Fig. 3.18(a), where Trace 1 shows five-levels in phase-voltage and Trace 2 shows nine-levels in line-voltage (Scale: X-axis: 50 V/div and Y-axis: 10 ms/div.).



(a) Line and phase-voltage waveforms (X-axis: 10 ms/div. and Y-axis: 50 V/div.)



(b) Phase-voltage harmonic spectrum



(c) Line-voltage harmonic spectrum

Fig. 3.18: Experimental performance of modified multi reference dual carrier PWM on five-level T-type RSC-MLI.

Waveforms of phase and line-voltage remain clean and uniform as similar to LSPWM-IPD shown in Fig. 3.7. Corresponding phase and line-voltage harmonic spectra of Fig. 3.18 are depicted in Fig. 3.18(b) and (c) respectively. As the experimental results are recorded at m_f =30, the side band harmonics in the obtained phase and line-voltages are centred at m_f. Fig. 3.18(b) shows the presence of dominant harmonic in phase-voltage at m_f and the magnitude of this dominant harmonic is supressed in line-voltage shown in Fig. 3.18(c). Therefore from Fig. 3.18(b) and (c), an appreciable difference in THD of phase-voltage (23.2%) and line-voltage (7.3%) can be noticed. Further, comparing the experimental performance of modified multi reference modulation scheme shown in Fig. 3.18, with the performance of conventional multi reference PWM shown in Fig. 3.9, verifies the superior line-voltage THD performance. Also comparison of Fig. 3.18 and Fig. 3.7, shows that the THD performance of phase-voltage (23.2%) and line-voltage (7.3%) of this PWM scheme is similar to the THD performance of phase-voltage (23.3%) and line-voltage (7%) of LSPWM-IPD.

Though the proposed modified multi reference dual carrier PWM produces improved line-voltage THD performance, involvement of multiple dc shifted references increases its complexity in real-time applications. This can be alleviated by modified reduced carrier modulation scheme, proposed in next section.

3.4.2 Modified reduced carrier PWM

The proposed modified reduced carrier PWM involves same number of carriers as of the conventional reduced carrier scheme, nevertheless modifies the carrier arrangement such that its carrier arrangement is similar to LSPMW-IPD. The carrier and modulation signal arrangement of the proposed modified reduced carrier PWM to obtain five-levels in phase-voltage is shown in Fig. 3.19, where the difference in carrier position for positive and negative half of the modulating signal can be noticed. In the other way, each carrier in Fig. 3.19 is the effective way of representing $carrier_1$ and $carrier_2$ of the modified multi reference dual carrier PWM shown in Fig. 3.14.

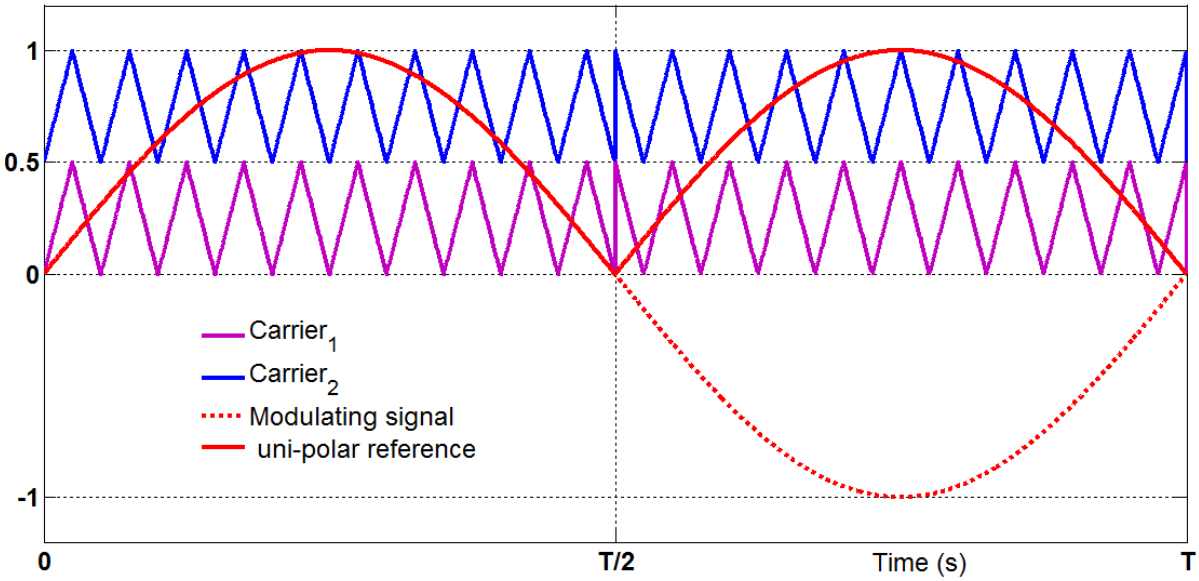


Fig. 3.19: Carrier and modulating signal arrangement for proposed modified reduced carrier PWM scheme for five-level phase-voltage.

In Fig. 3.19, if the unipolar reference is in the limits of $carrier_1$, switching pulse is obtained by comparing reference and $carrier_1$. This pulse is responsible for producing 0–V voltage band in phase-voltage. Similarly, if the unipolar reference is greater than $carrier_{1\text{-max}}$, pulse is obtained by comparing reference and $carrier_2$, which produces voltage band between V and $2V$ in phase-voltage. This repeats for higher levels as well.

The maximum and minimum value of each carrier can be calculated from (3.3) and (3.4) respectively, where i is the carrier number varying from 1 to $(m-1)/2$. Further, m_a and m_f are defined in (3.5) and (3.6).

$$Carrier\, i_{\max} = \frac{2}{m-1} i \tag{3.3}$$

$$Carrier\, i_{\min} = \frac{2}{m-1}(i-1) \tag{3.4}$$

$$m_a = \frac{2V_m}{(m-1)V_c} \tag{3.5}$$

$$m_f = \frac{f_{cr}}{f_m} \tag{3.6}$$

Here, V_m: peak of the modulating signal, V_c : peak of the carrier signal, f_{cr} : frequency of carrier signal, f_m: frequency of the modulating signal, and *m:* levels in phase-voltage. Thus, the proposed modified reduced carrier PWM scheme generates switching pulses by comparing unipolar reference with carrier signal, if the reference is in the limits of respective carrier as defined in (3.3) and (3.4). Each obtained pulse is responsible for producing a specific magnitude of voltage band. Polarity of these voltage bands is decided by polarity of the modulating signal, such that, positive levels are obtained for the positive half of the modulating signal and negative levels are obtained for the negative half of the modulating signal. However, verifying maximum condition for $carrier_{(m-1)/2}$ should be avoided. Since, it is the carrier with peak magnitude, involving maximum condition to this carrier will limit the switching logic to undermodulation.

Modified reduced carrier arrangement for three-phase MLI:

To implementing the modified reduced carrier modulation, for a three-phase MLI, the arrangement of phase-*b* and phase-*c* carriers are obtained by shifting phase-*a* carriers. The criteria of shifting carriers is framed such that phase-*b* and phase-*c* are equivalent to phase-*a* carriers and, phase opposition condition between the carriers for positive and negative half of its respective modulating signal is maintained for each phase. For example, with the carrier frequency of 2 kHz and modulating frequency of 50 Hz, 40 carrier cycles are present per one cycle of the modulating signal and, 13.33 cycles are covered for 120˚ of the modulating signal. Therefore, shifting the carriers of phase-*a*, with a delay equivalent to 13 cycles, results in the phase-*b* carriers, which are equivalent to phase-*a* carriers. Also this delay of 13 cycles ensures the phase-*b* carriers to stay synchronism with its respective modulating signal. Generalized formula for calculating time delay among the carriers of each phase is given in (3.7).

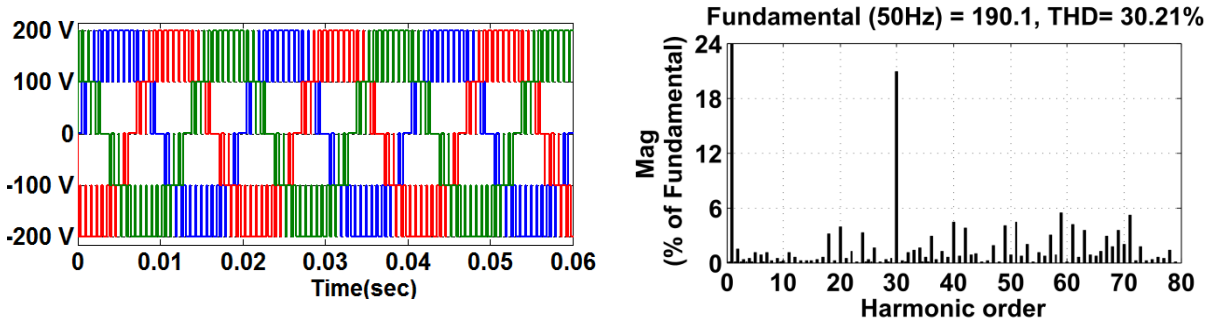
$$Time\, delay = \left[Integer\left(\frac{\varphi m_f}{360^\circ} \right) \right] \left[\frac{1}{f_{cr}} \right] \tag{3.7}$$

Here, φ : modulating signal phase angle with respect to reference phase i.e., 120˚ for phase-*b* and 240˚ for phase-*c*. In other way, this time delay can be avoided by choosing f_{cr} as three times the integral multiple of f_m as given in (3.8), where, *N is* any finite positive integer.

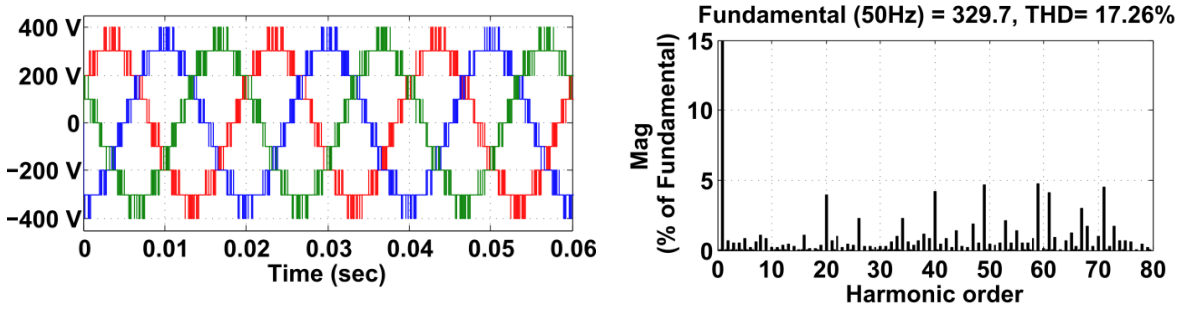
$$f_{cr} = 3Nf_m \tag{3.8}$$

3.4.2.1 Performance evaluation

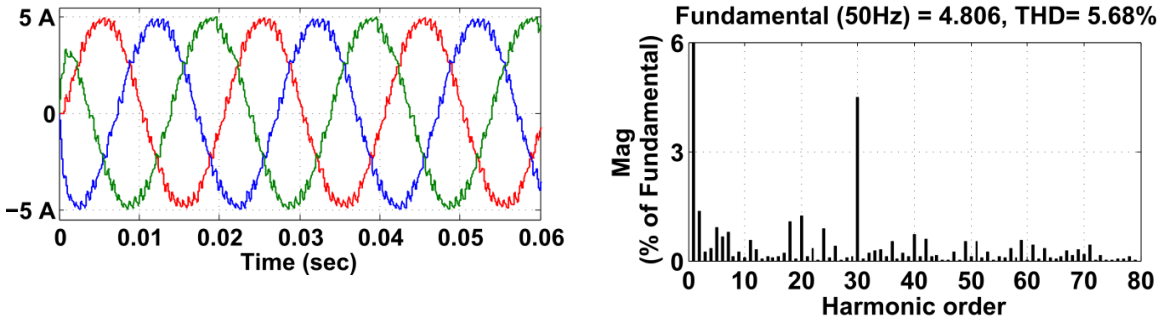
Performance of modified reduced carrier modulation scheme on a five-level T-type RSC-MLI is shown in Fig. 3.20. Evaluation is carried out for the same simulation parameters considered in section 3.2.1.1. Obtained phase-voltage, line-voltage and line-current with its respective harmonic spectra are shown in the Fig. 3.20(a), (b) and (c) respectively.



(a) Phase-voltage



(b) Line-voltage



(c) Line-current

Fig. 3.20: Simulation performance of modified reduced carrier PWM on five-level T-type RSC-MLI.

Comparing line THD performance of the modified reduced carrier modulation shown in Fig. 3.20(b), with conventional multi reference modulation shown in Fig. 3.3(b), verifies the superior performance of the proposed modulation over conventional scheme. Comparative line-voltage THD performance of the proposed modified reduced carrier and conventional reduced carrier PWM arrangement on a five-level inverter is shown in Fig. 3.21. This verifies the superior THD performance of the proposed carrier arrangement over conventional reduced carrier arrangement.

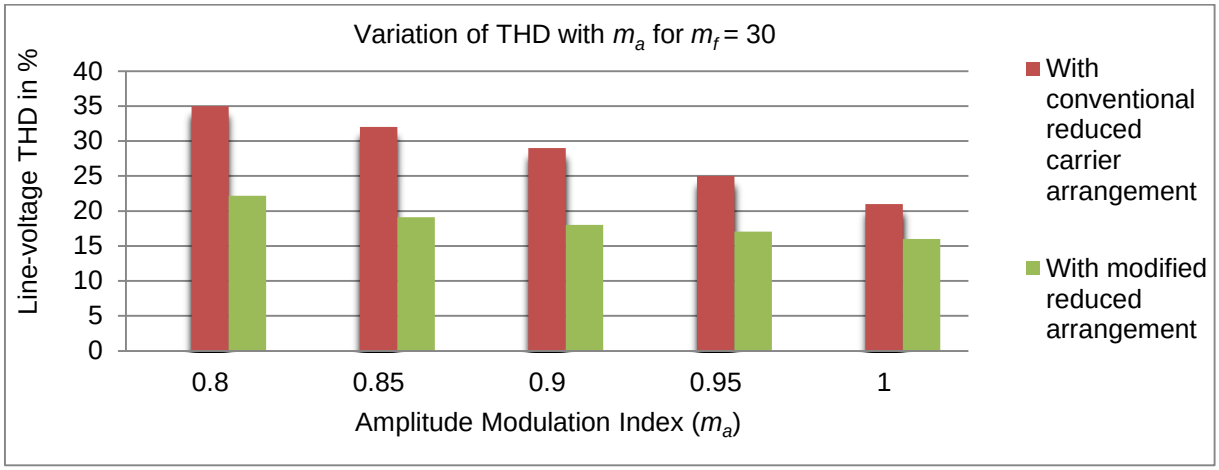
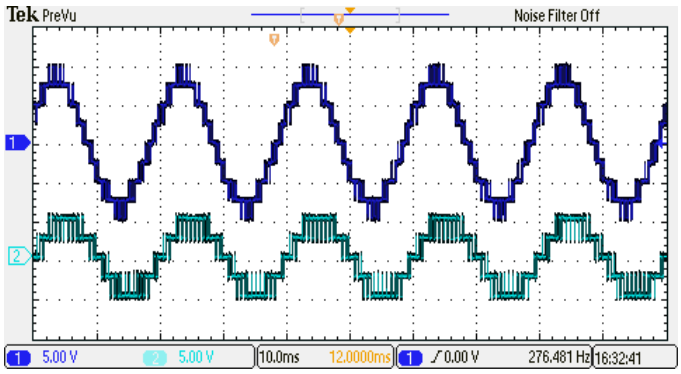


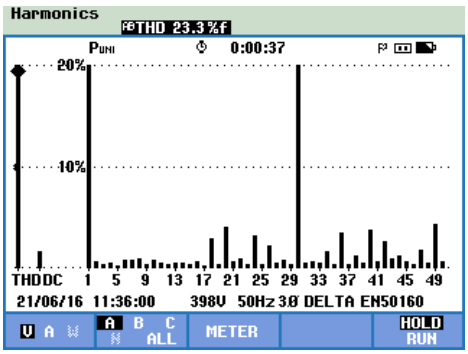
Fig. 3.21: Line-voltage THD performance of conventional and modified reduced carrier PWM.

3.4.2.2 Experimental validation

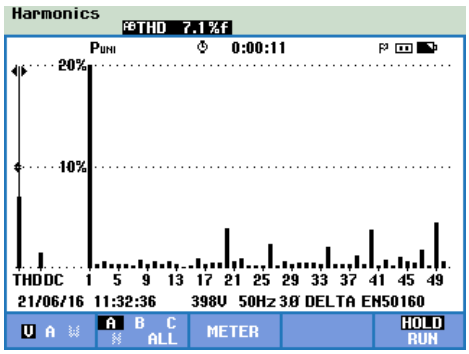
An experimental set-up of five-level T-type RSC-MLI is developed to evaluate the performance of the proposed modified reduced carrier PWM scheme. Experimentation is carried for the parameters given in Table 3.2. Experimental performance of the proposed modified reduced carrier modulation scheme on five-level T-type RSC-MLI is shown in Fig. 3.22.



(a) Line and phase-voltages waveforms (X-axis: 10 ms/div. and Y-axis: 50 V/div.)



(b) Phase-voltage harmonic spectrum



(c) Line-voltage harmonic spectrum.

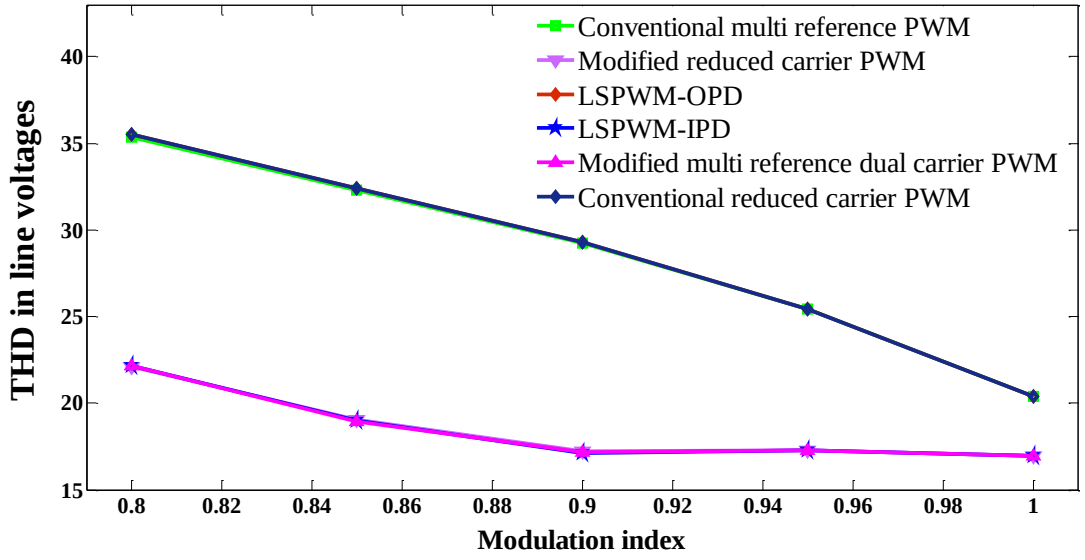
Fig. 3.22: Experimental performance of the proposed modified reduced carrier PWM.

The obtained phase and line-voltage waveforms are depicted in Fig. 3.22(a), where Trace-2 shows five-level phase-voltage and Trace-1 shows nine-level line-voltage. Voltage

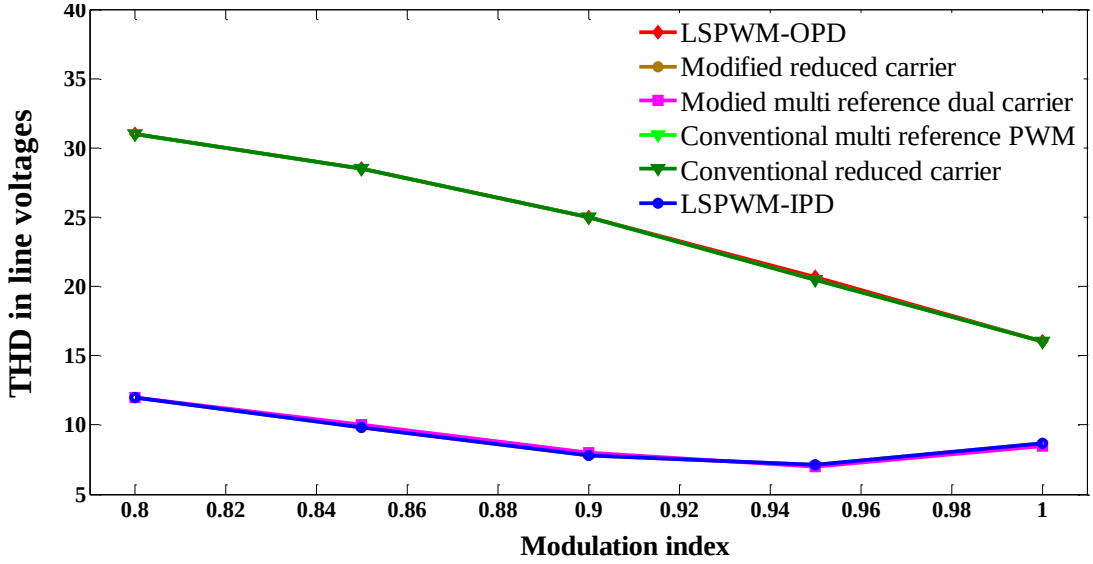
waveforms of phase and line are similar to LSPWM-IPD shown in Fig. 3.7. The harmonic spectra of phase and line-voltages are depicted in Fig. 3.22(b) and(c) respectively. As the experimental results are recorded at m_f = 30, the side band harmonics in the obtained phase and line-voltages are centred at m_f. Fig. 3.22(b) shows the presence of dominant harmonic in phase-voltage at m_f and the magnitude of this dominant harmonic is supressed in line-voltage, shown in Fig. 3.22(c). Therefore from Fig. 3.22(b) and (c), an appreciable difference in THD of phase-voltage (23.3%) and line-voltage (7.1%) can be noticed.

3.4.3 Comparative performance of the proposed PWM schemes

The simulation and experimental line-voltage THD comparison of the proposed two PWM schemes with conventional PWM schemes on a five-level MLI is shown in Fig. 3.23.



(a) Simulation performance



(b) Experimental performance

Fig. 3.23: Comparative THD performance of the proposed and conventional PWM schemes on five-level inverter.

Fig. 3.23 infers that line-voltage THD of the proposed PWM schemes is similar to LSPWM-IPD, where the line-voltage THD of conventional reduced carrier and conventional multi reference PWM schemes is similar to LSPWM-OPD. Fig. 3.23, validates the superior THD performance of the proposed PWM schemes over conventional schemes on both experimental and simulation studies. The variation in THD recorded for simulation and experimental is due to the MATLAB simulator, which measures the THD upto Nyquist frequency (i.e., 499th order harmonic), where power quality analyser (Fluke) measures the experimental THD up to 49th order harmonic.

3.4.4 Merits and limitations of the modified PWM schemes

The modified multi reference dual carrier PWM and modified reduced carrier PWM schemes are readily scalable for any number of levels and produces superior THD performance over the conventional modulation schemes. However, both the proposed schemes suffers with their own limitations, which are mentioned here under.

Modified multi reference dual carrier PWM: Involvement of multiple dc off shifted references increases the difficulty in implementing the modulation scheme for closed-loop applications.

Modified reduced carrier PWM: Involvement of maximum and minimum constraints for each carrier (to realize the switch logic) increases the computational burden on the controller. Thus, this proposed scheme suffers with difficulty in implementing the switching logic at higher levels on real-time controllers such as dSPACE.

Hence, a modified reduced carrier PWM with unified logical expressions is proposed in the next section, where the switching logic remains to be simplified irrespective to the number of levels and topological arrangement.

3.5 Proposed reduced carrier PWM with unified logical expression

The proposed PWM scheme intends to perform logical operations on the pulses obtained from conventional switching logic, such that the obtained (modified) pulses will realize switching states of any RSC-MLI. Fig. 3.24 shows the carrier and modulating signal arrangement of the proposed modified reduced carrier arrangement for obtaining seven-levels in phase-voltage. Fig. 3.25 shows the switching pulses and the conduction interval of each pulse obtained by using modified reduced carrier PWM scheme shown in Fig. 3.24. Each pulse (*P*) shown in Fig. 3.25 is obtained for carrier greater than reference, and the conduction interval (*Q*) show the duration over which each of these switching pulse is active and is defined in (3.9).

$$\begin{aligned} Q_i &= reference > carrier_{\,i-\min} \\ Q_i &= 0;\ else \end{aligned} \tag{3.9}$$

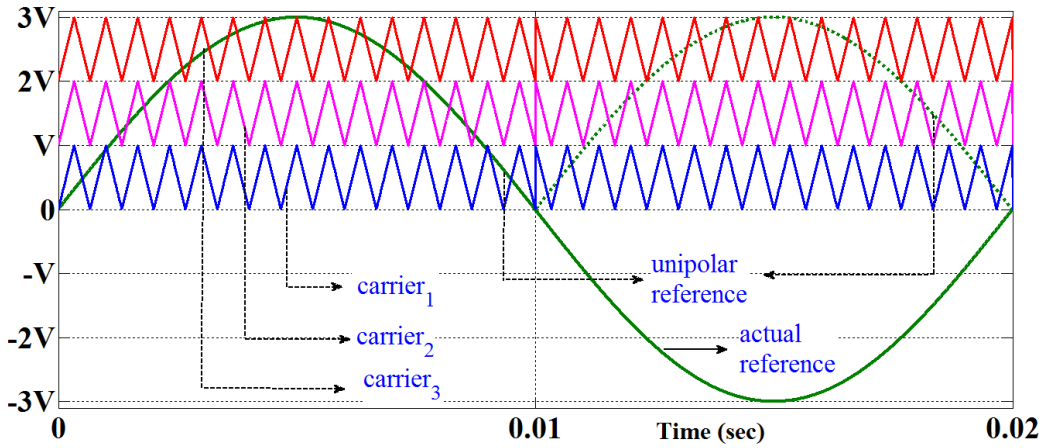
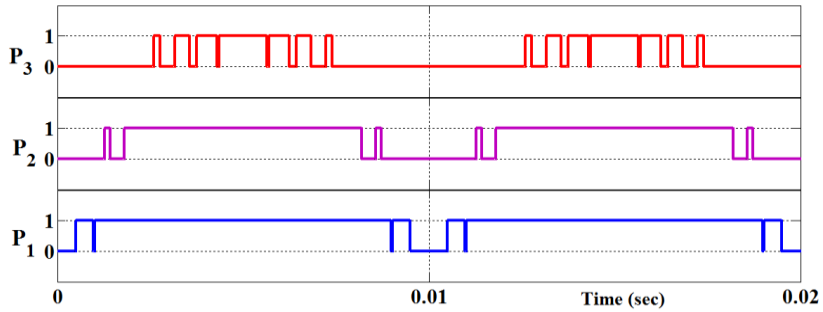
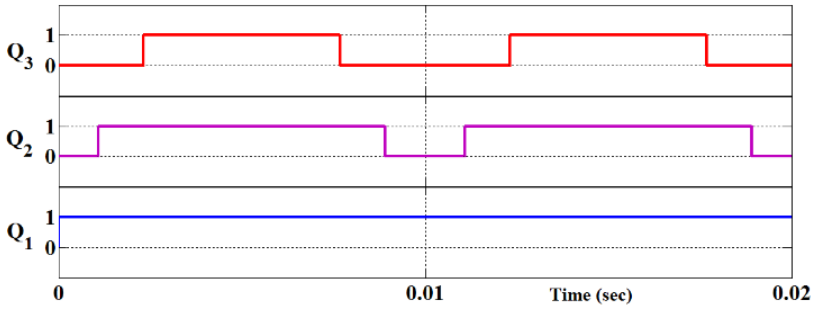


Fig. 3.24: Carrier and modulating signal arrangement for proposed modified reduced carrier arrangement for obtaining seven-levels in phase-voltage.



(a) Switching pulses (*P*)

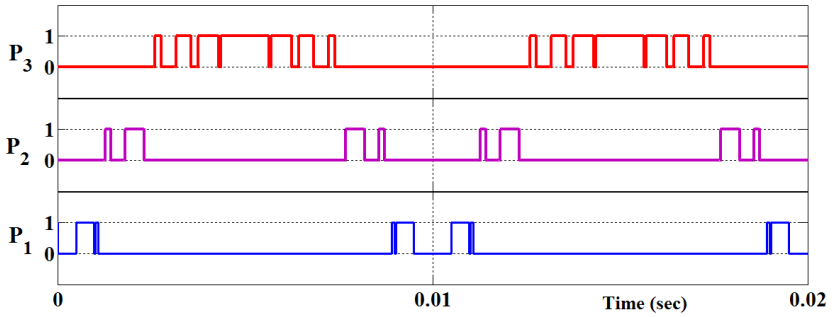


(b) Conduction intervals (*Q*)

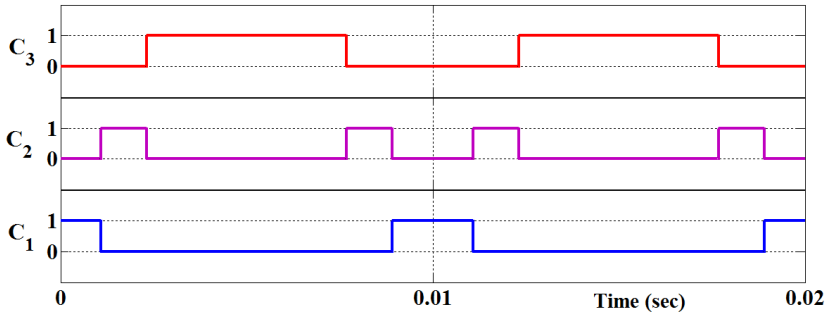
Fig. 3.25: Conventional switching pattern of reduced carrier PWM scheme for seven-level inverter.

Fig. 3.25(a) and (b), conveys the overlapping nature of switching pulses and justifies that the conventional switching logic cannot realize most of RSC-MLI topologies. Including carrier constraints modifies the pattern of *P* to *P**, such that the switching pulse *P** can be applicable for any RSC-MLI. These modified switching pulses (*P**) and the conduction interval (*C*) of each pulse for seven-level phase-voltage is shown in Fig. 3.26.

By observing Fig. 3.25 and Fig. 3.26, it can be inferred that, application of over-lapped pulses shown in Fig. 3.25(a), across the non-overlapped conduction interval (*C*), shown in the Fig. 3.26(b), results in desired non-overlapped pulses shown in Fig. 3.26(a). Thus instead of controlling the nature of switching pulse directly, conduction interval of the pulse can be controlled.



(a) Switching pulses (*P**)



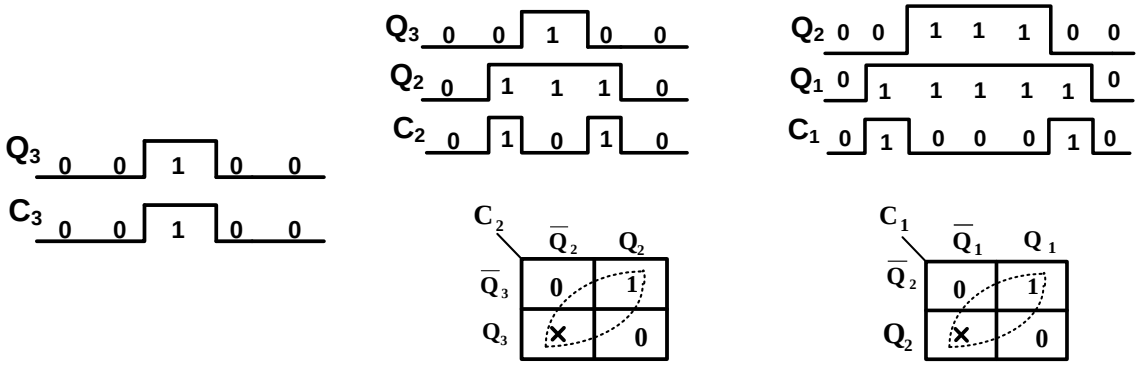
(b) Conduction intervals (*C*)

Fig. 3.26: Desired switching pattern with reduced carrier PWM for obtaining seven-level phase-voltage.

In detail, modifying the nature of overlapped conduction interval (*Q*) to non-overlapped conduction interval (*C*), can obtain desired non-overlapped switching pulses even with conventional switching logic. This acts as vital observation behind the proposed PWM scheme.

3.5.1 Methodology: Proposed unified logical expression

To derive a unified logic relation for obtaining non-overlapped interval (*C*) from the overlapped interval (*Q*), the nature of both these conduction intervals should be analyzed. Fig. 3.27 which is obtained from Fig. 3.25(b) and Fig. 3.26(b), shows the conduction intervals *Q* and *C* together. Fig. 3.27 infers that the desired conduction interval *C*, can be obtained by performing a logical operation on *Q* with its adjacent bands.



(a) (b) (c)

Fig. 3.27: Mapping of overlapped conduction intervals (*Q*) with non-overlapped conduction intervals (*C*) and their associated K-maps.

From Fig. 3.27(a), by observing Q_3 and C_3, reveals their identical nature of switching and hence,

$$C_3 = Q_3 \tag{3.10}$$

But Q_2 and C_2 are different from each other and from Fig. 3.27(b) following relationships are obtained.

If $Q_3 = 0$ and $Q_2 = 0$, then $C_2 = 0$

If $Q_3 = 1$ and $Q_2 = 1$, then $C_2 = 0$

If $Q_3 = 0$ and $Q_2 = 1$, then $C_2 = 1$

It should be noted that $Q_3 = 1$ and $Q_2 = 0$ case does not appear as lower conduction interval Q_2 always remains high when upper conduction interval Q_3 is high. To obtain a logical relation for C_2 in terms of Q_3 and Q_2, a two variable Karnaugh-map (*K*-map) is implemented in Fig. 3.27(b). From Fig. 3.27 (b), logical relation for C_2 is obtained as $C_2 = \bar{Q}_3 Q_2$. To realize this logic in hardware two logic gates NOT and AND are required. To reduce these logic gates, a *don't care* variable is included in K-map and the logical relation (3.11) is obtained, which requires an Ex-OR gate only.

Applying the pulse P_i (|ref| > $carrier_i$) across the interval C_i, results in desired non-overlapped switching pulses. This switching action of the proposed modulation scheme to control seven-level inverter is shown in Fig. 3.28.

$$C_2 = \bar{Q}_3 Q_2 + Q_3 \bar{Q}_2 = Q_2 \oplus Q_3 \tag{3.11}$$

To obtain conduction interval C_1, Fig. 3.27(c) is considered and following relationships are obtained.

If $Q_2 = 0$ and $Q_1 = 0$, then $C_1 = 0$

If $Q_2 = 1$ and $Q_1 = 1$, then $C_1 = 0$

If $Q_2 = 0$ and $Q_1 = 1$, then $C_1 = 1$

With the help of *K*-map shown in Fig. 3.27(c), logical relation (3.12) is obtained for conduction interval C_3.

$$C_1 = Q_1 \oplus Q_2 \tag{3.12}$$

Further, generalizing (3.10)-(3.12), (3.13) can be obtained, where *i* is the carrier number.

$$\begin{aligned} &for \quad i = (n-1)/2 \\ &\qquad\qquad C_i = Q_i \\ &for \quad 1 \le i < (n-1)/2 \\ &\qquad\qquad C_i = Q_i \oplus Q_{i+1} \end{aligned} \tag{3.13}$$

Thus referring (3.13) to Fig. 3.28, C_3 should be active to obtain voltage band of 3*V* to 2*V*. Similarly, C_2 and C_1 should be active for obtaining voltage band of 2*V* to *V* and *V* to 0

respectively. C_3 high with P_3 high i.e., pulse C_3P_3 is responsible for obtaining $3V$ voltage state. C_3 high with P_3 low or C_2 high with P_2 high i.e., pulse $C_3\bar{P}_3 + C_2P_2$ obtains $2V$ voltage state.

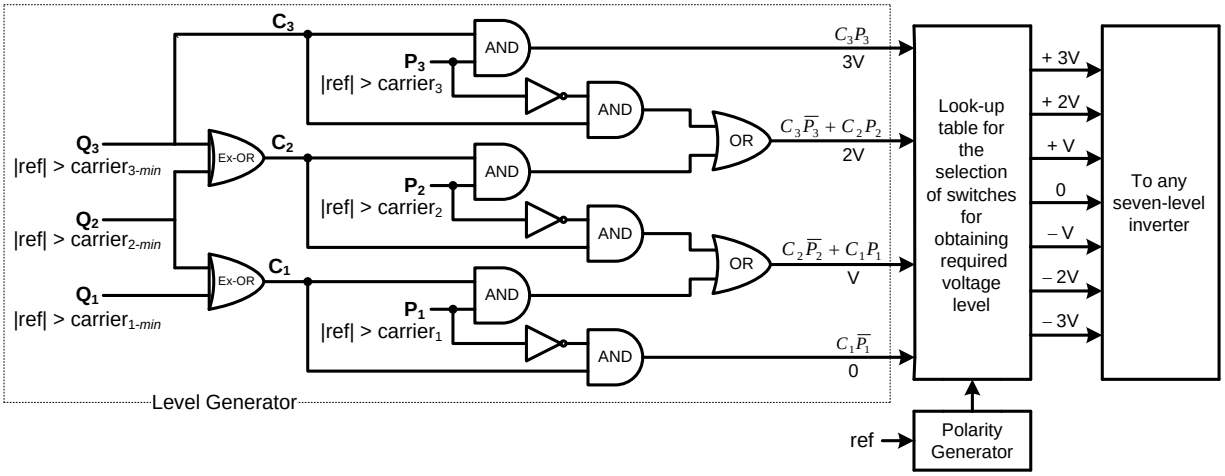


Fig. 3.28: Implementation of the proposed switching logic for obtaining seven-level phase-voltage.

Similarly C_2 high with P_2 low or C_1 high with P_1 high i.e., $C_2\bar{P}_2 + C_1P_1$ results in V voltage state. C_1 high with P_1 low i.e., pulse $C_1\bar{P}_1$ results in zero-voltage. The polarity of these voltage states is decided by the polarity of the modulating signal, where positive voltage levels are obtained for the positive half of the reference and negative voltage levels are obtained for negative half of the modulating signal. Table 3.4 shows the implementation of the proposed switching logic to realize a seven-level asymmetrical MLDCL inverter topology shown in Fig. 3.29. From Table 3.4, for example, to obtain +3V voltage-level, switches H_4, S_1, S_3 and H_1 should be in conduction. Therefore, these switches are applied with pulse C_3P_3 for the positive half of the reference. Similarly to obtain $-3V$ voltage-level, pulse C_3P_3 applied to switches H_2, S_1, S_3 and H_3 for the negative half of the reference. A similar explanation holds good for remaining voltage level as presented in Table 3.4.

Therefore in the proposed switching logic, the number of switching pulses generate from the proposed PWM are equal to the number of phase-voltage levels. Each pulse is responsible for specific level in phase-voltage and further, each of these pulses will be given to the devices in the considered inverter to achieve the respective voltage state. Further, generalizing the switching pulses for higher voltage levels, (3.14) is obtained.

$$
\begin{aligned}
&for\ \frac{n-1}{2}V \Rightarrow switching\ pulse = C_{\frac{n-1}{2}}\,P_{\frac{n-1}{2}} \\
&for\ V \le iV \le \left(\frac{n-1}{2}-1\right)V \Rightarrow switching\ pulse = C_{i+1}\,\bar{P}_{i+1} + C_i\,P_i \\
&for\ 0\,V \Rightarrow switching\ pulse = C_1\bar{P}_1
\end{aligned}
\tag{3.14}
$$

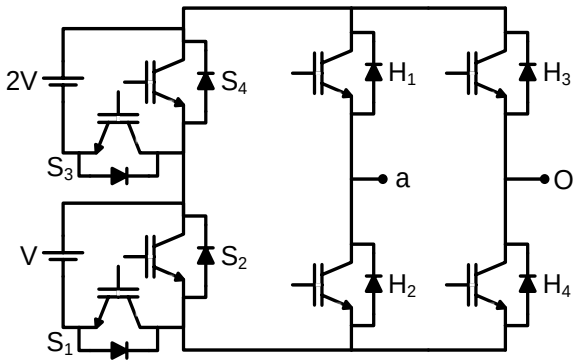


Fig. 3.29: Seven-level single-phase configuration of asymmetrical RSC-MLI based MLDCL.

Table 3.4: Implementation of the proposed switching logic to control seven-level asymmetrical MLDCL RSC-MLI.

Polarity generation	Voltage level	Switching pulse	Switching path
ref ≥ *0*	+3V	C_3P_3	H_4-S_1-S_3-H_1
	+2V	$C_3\bar{P}_3 + C_2P_2$	H_4-S_2-S_3-H_1
	+V	$C_2\bar{P}_2 + C_1P_1$	H_4-S_1-S_4-H_1
zero-level	0	$C_1\bar{P}_1$	H_4-S_2-S_4-H_1 *(or)* H_2-S_2-S_4-H_3
ref< *0*	−V	$C_2\bar{P}_2 + C_1P_1$	H_2-S_1-S_4-H_3
	−2V	$C_3\bar{P}_3 + C_2P_2$	H_2-S_2-S_3-H_3
	−3V	C_3P_3	H_2-S_1-S_3-H_3

3.5.2 Implementation to RSC-MLIs

The ability of the proposed PWM switching scheme to control any RSC-MLI, irrespective of the topological arrangement can be better evaluated by observing the implementation of the proposed PWM in controlling various asymmetrical RSC-MLI.

In literature, among the various asymmetrical RSC-MLIs, E-type has an appreciable reduction in switch count where each unit in E-type can obtain thirteen-levels in phase-voltage. However, its implementation with simple carrier based PWM is not yet reported. MLDCL, SSPS, cascaded T-type, RV, PUC, switched dc-sources (SDS) and hybrid T-type are few popular RSC-MLI topologies, mostly reported for their symmetrical configurations. Implementation of their asymmetrical configurations is not yet reported in literature. Switching behavior and operation of these RSC-MLIs for symmetrical and asymmetrical configurations is reported in Chapter 2. Fig. 3.30 shows the typological arrangement of these RSC-MLI for thirteen-level. Therefore, to evaluate ability of the proposed PWM switching scheme in controlling any RSC-MLI, implementation of the proposed PWM scheme on MLDCL, SSPS, SDS, Hybrid T-type and E-type RSC-MLIs, shown in Fig. 3.30 is investigated.

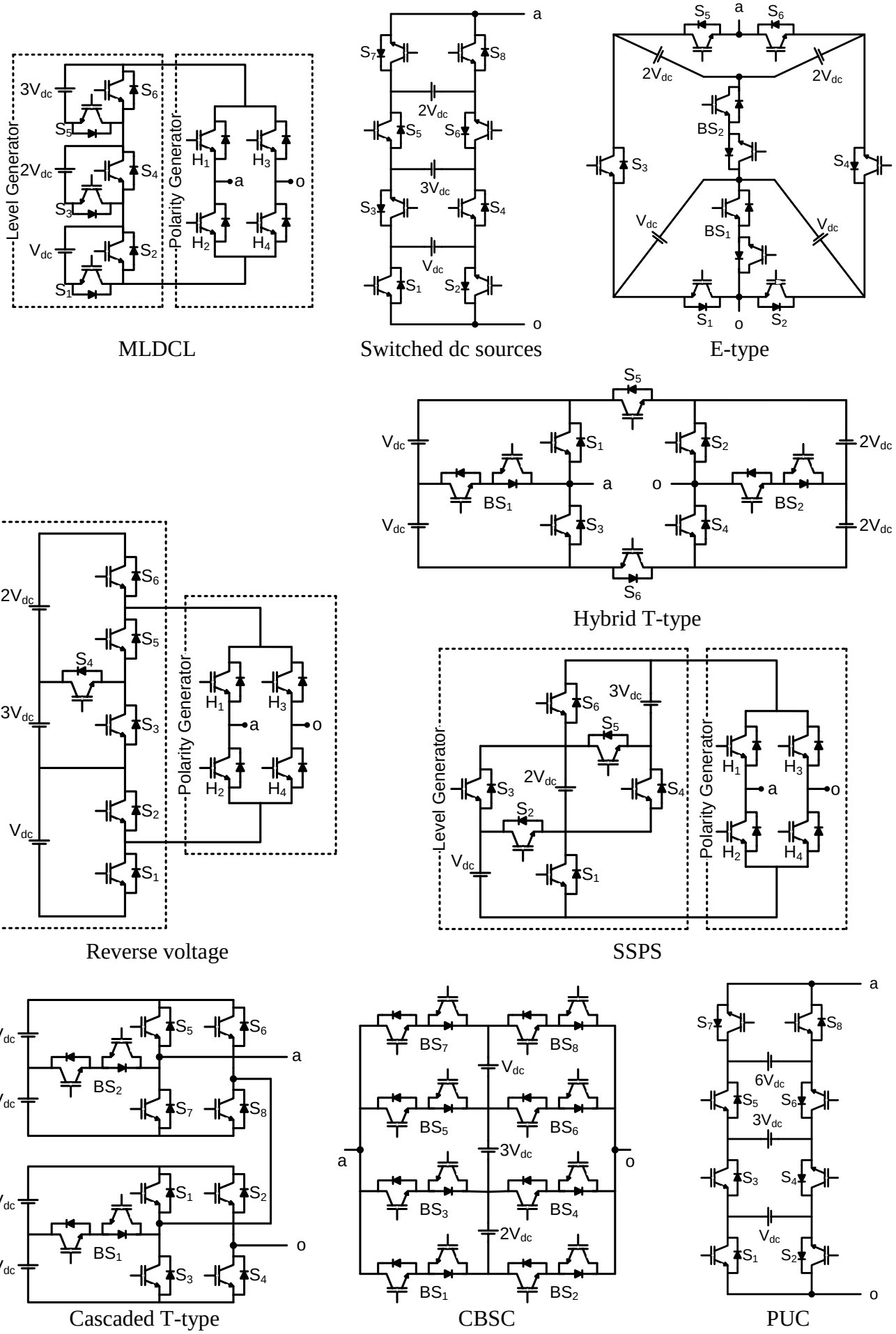


Fig. 3.30: Single-phase configurations of thirteen-level asymmetrical RSC-MLI topologies.

Table 3.5 shows the implementation of the proposed switching logic to realize asymmetrical configuration of thirteen-level MLDCL, SSPS, SDS, Hybrid T-type and E-type RSC-MLIs shown in Fig. 3.30. On the other way, Table 3.5 is obtained by extending Fig. 3.28 and Table 3.4 for thirteen-level. To obtain thirteen-levels in phase-voltage, proposed PWM generates thirteen switching pulses, where each switching pulse is responsible for obtaining a specific voltage level.

The generalized logical expression to obtain these desired switch pulses is given in (3.14). Following (3.14), for example in thirteen-level asymmetrical MLDCL RSC-MLI shown in Fig. 3.30, conduction of S_1, S_3, S_5, H_1 and H_4 produces an voltage of $+6V$ in phase-voltage of MLDCL inverter. Therefore, to obtain the $+6V$ voltage state in the required thirteen-level phase-voltage, pulse C_6P_6 (for the positive half of the modulating signal) is applied to S_1, S_3, S_5, H_1 and H_4. Similarly to obtain $+6V$ in the thirteen-level phase-voltage of SSPS MLI inverter shown in Fig. 3.30, pulse C_6P_6 (for the positive half of the modulating signal) is applied to S_2-S_3-S_6-S_7. In the same way to obtain $-6V$ in the thirteen-level phase-voltage of SSPS RSC-MLI inverter shown in Fig. 3.30, pulse C_6P_6 (for the negative half of the modulating signal) is applied to H_2-S_2-S_5-H_3. Thus to obtain any voltage level, switching pulse responsible for obtaining the respective voltage level is given to the devices to be in condition in the considered RSC-MLI. A similar explanation is valid for remaining voltage levels of all the RSC-MLI, shown in Fig. 3.30 and is given in Table 3.5.

Table 3.5: Implementation of the proposed scheme to control thirteen-level asymmetrical RSC-MLIs.

Polarity generation	**Level**	**Switching pulse**	**Devices to be in conduction to obtain the respective voltage level**				
			MLDCL	**SSPS**	**Switched dc sources**	**Hybrid T-type**	**E-type**
ref > 0	+6V	C_6P_6	H_4-S_1-S_3-S_5-H_1	H_4-S_2-S_5-H_1	S_2-S_3-S_6-S_7	S_2-S_6-S_1	S_1-S_4-S_5
	+5V	$C_6\bar{P}_6 + C_5P_5$	H_4-S_2-S_3-S_5-H_1	H_4-S_1-S_5-H_1	S_1-S_3-S_6-S_7	S_2-S_6-BS_1	BS_1-S_4-S_5
	+4V	$C_5\bar{P}_5 + C_4P_4$	H_4-S_1-S_4-S_5-H_1	H_4-S_2-S_4-H_1	S_2-S_3-S_6-S_8	BS_2-S_6-S_1	S_2-S_4-S_5
	+3V	$C_4\bar{P}_4 + C_3P_3$	H_4-S_1-S_3-S_6-H_1	H_4-S_1-S_4-H_1	S_1-S_3-S_6-S_8	BS_2-S_6-BS_1	S_1-BS_2-S_5
	+2V	$C_3\bar{P}_3 + C_2P_2$	H_4-S_2-S_3-S_6-H_1	H_4-S_1-S_6-H_1	S_2-S_4-S_6-S_7	S_4-S_6-S_1	S_1-S_4-S_6
	+V	$C_2\bar{P}_2 + C_1P_1$	H_4-S_1-S_4-S_6-H_1	H_4-S_3-S_6-H_1	S_2-S_3-S_5-S_7	S_4-S_6-BS_1	BS_1-S_4-S_6
zero-level	0	$C_1\bar{P}_1$	H_4-S_2-S_4-S_6-H_1 or H_2-S_2-S_4-S_6-H_3	H_1-H_3 or H_2-H_4	S_1-S_3-S_5-S_7	S_4-S_6-S_3	S_1-S_3-S_5
ref < 0	−V	$C_2\bar{P}_2 + C_1P_1$	H_2-S_1-S_4-S_6-H_3	H_2-S_3-S_6-H_3	S_1-S_4-S_6-S_8	S_2-S_5-BS_1	BS_1-S_3-S_5
	−2V	$C_3\bar{P}_3 + C_2P_2$	H_2-S_2-S_3-S_6-H_3	H_2-S_1-S_6-H_3	S_1-S_3-S_5-S_8	S_2-S_5-S_3	BS_1-BS_2-S_6
	−3V	$C_4\bar{P}_4 + C_3P_3$	H_2-S_1-S_3-S_6-H_3	H_2-S_1-S_4-H_3	S_2-S_4-S_5-S_7	BS_2-S_5-BS_1	S_2-BS_2-S_6
	−4V	$C_5\bar{P}_5 + C_4P_4$	H_2-S_1-S_4-S_5-H_3	H_2-S_2-S_4-H_3	S_1-S_4-S_5-S_7	BS_2-S_5-S_3	S_1-S_3-S_6
	−5V	$C_6\bar{P}_6 + C_5P_5$	H_2-S_2-S_3-S_5-H_3	H_2-S_1-S_5-H_3	S_2-S_4-S_5-S_8	S_4-S_5-BS_1	BS_1-S_3-S_6
	−6V	C_6P_6	H_2-S_1-S_3-S_5-H_3	H_2-S_2-S_5-H_3	S_1-S_4-S_5-S_8	S_4-S_5-S_3	S_2-S_3-S_6

3.5.3 Performance evaluation

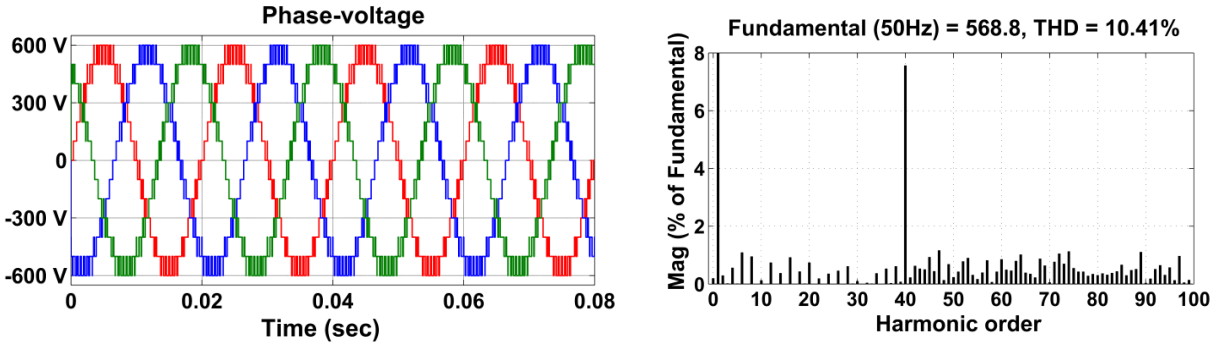
The performance of the proposed scheme is investigated with computer simulation studies performed in MATLAB/Simulink environment. Simulation studies have been carried out for thirteen-level asymmetrical MLDCL, SPPS, SDS, Hybrid T-type and E-type RSC-MLIs shown in Fig. 3.30. Considered simulation parameters are shown in Table 3.6 and, the performance of obtained phase and line-voltages are depicted in Fig. 3.31 and Fig. 3.32 respectively.

Table 3.6: Simulation parameters.

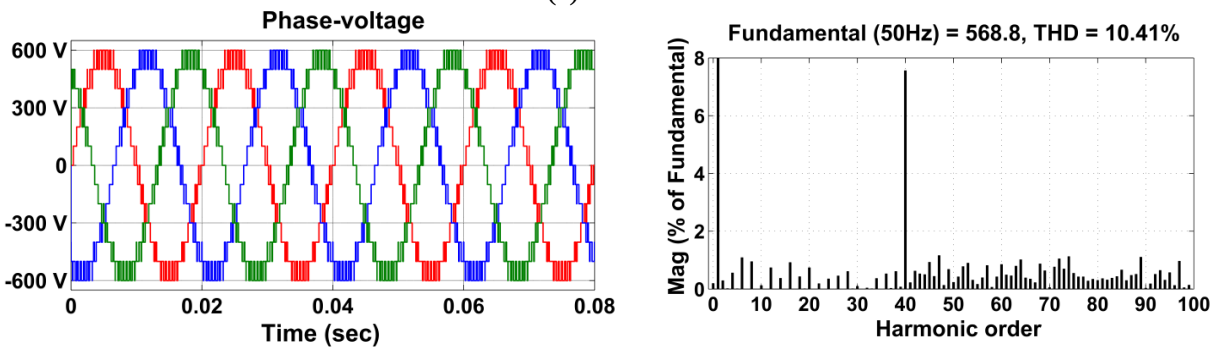
Parameter	Value
Carrier signal frequency (f_{cr})	2 kHz
Amplitude modulation index (m_a)	0.95
Modulating signal frequency (f_s)	50 Hz
DC source voltages	100 V, 200 V and 300 V
Sampling time (T_s)	5 μs

Fig. 3.31 shows the Simulink performance of phase-voltages and their corresponding harmonic spectra obtained from various RSC-MLI shown in Fig. 3.30 using the proposed modified reduced carrier PWM. Fig. 3.31(a)-(e) shows the phase-voltage performance of thirteen-level MLDCL, SSPS, SDS, hybrid T-type and E-type asymmetrical topologies with the proposed PWM scheme. From Fig. 3.31, it is observed that all the waveforms and their harmonic spectra are identical with side-band harmonics centered at frequency modulation index (m_f = 40). The phase-voltage THD performance of the proposed modified reduced carrier PWM is recorded as 10.39%, 10.41%, 10.39%, 10.39% and 10.39% on thirteen-level asymmetric MLDCL, SSPS, SDS, hybrid T-type and E-type respectively.

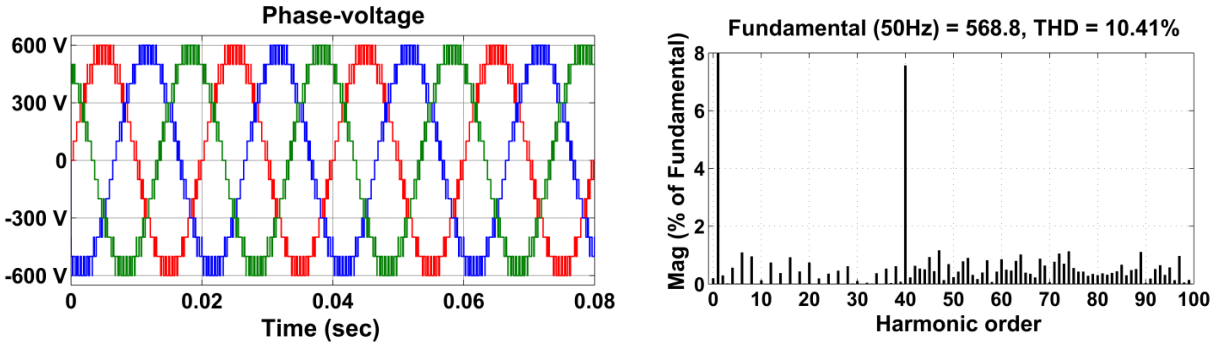
Fig. 3.32(a)-(e) shows the line-voltage performance of thirteen-level MLDCL, SSPS, SDS, hybrid T-type and E-type asymmetrical topologies with proposed PWM scheme. From Fig. 3.32(a)-(e), it is observed that all the waveforms are identical with similar harmonic spectrum. The obtained line-voltage THD of the proposed scheme is recorded as 5.86%, 5.87%, 5.86%, 5.86% and 5.86% on thirteen-level asymmetric MLDCL, SSPS, SDS, Hybrid T-type and E-type respectively. The side-band harmonics of these spectra are centered at m_f = 40. Therefore from Fig. 3.31 and Fig. 3.32, it can be stated that the proposed switching scheme can be applicable to any RSC-MLI and produce identical performance for a given level.



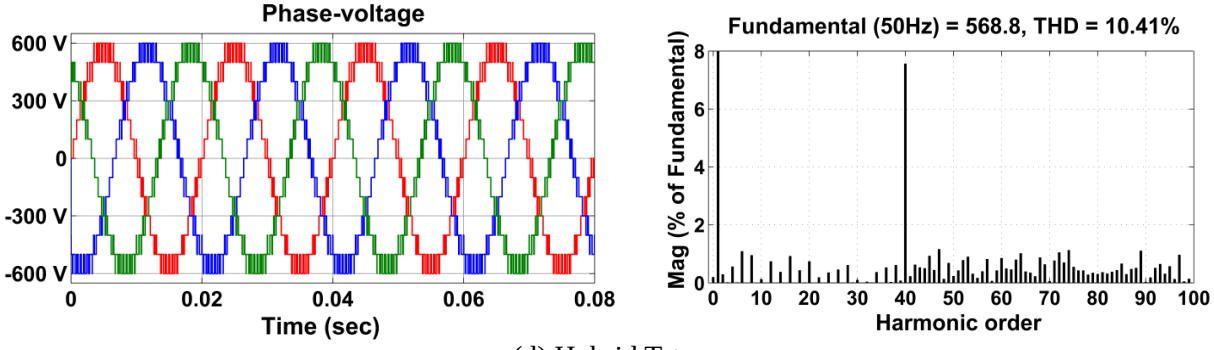
(a) MLDCL



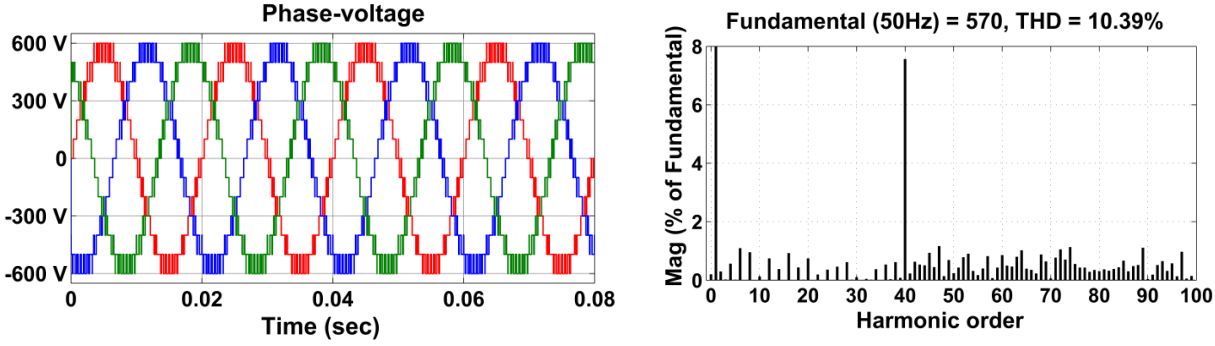
(b) SSPS



(c) SDS

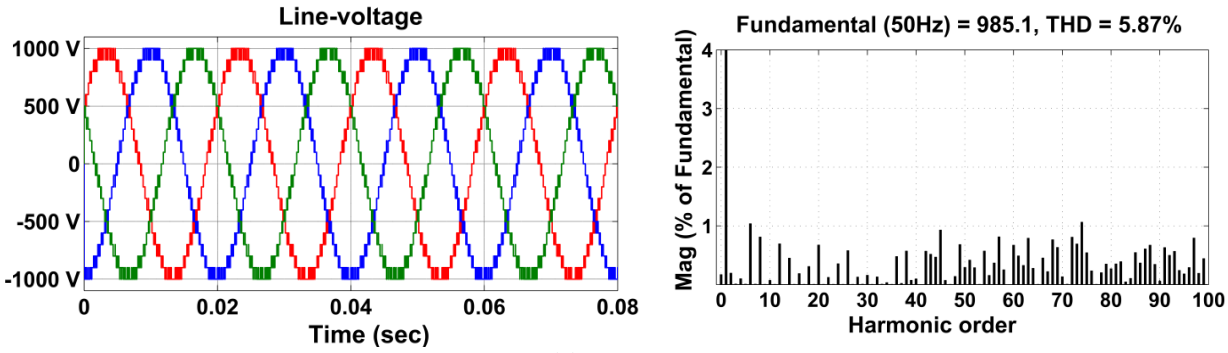


(d) Hybrid T-type

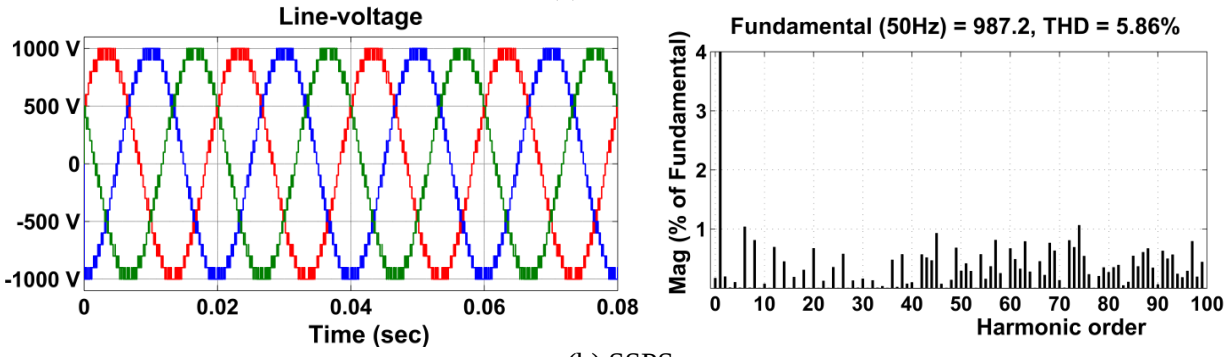


(e) E-type

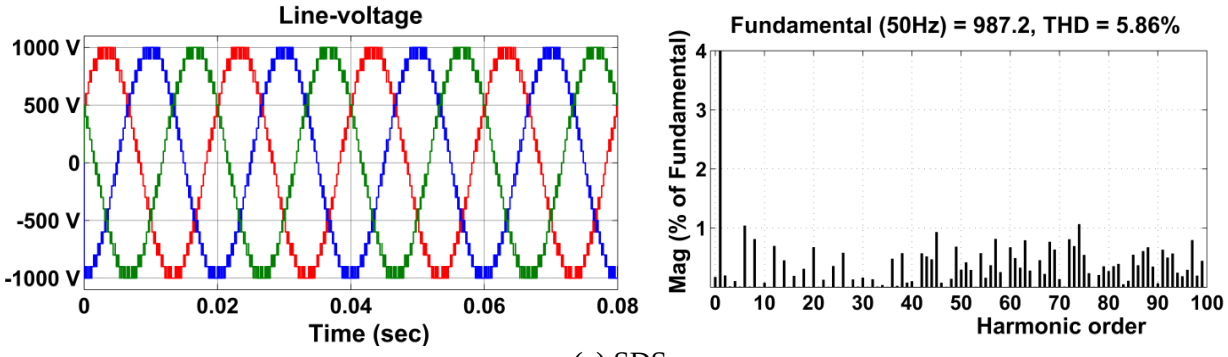
Fig. 3.31: Phase-voltage performance of various RSC-MLI with the proposed PWM.



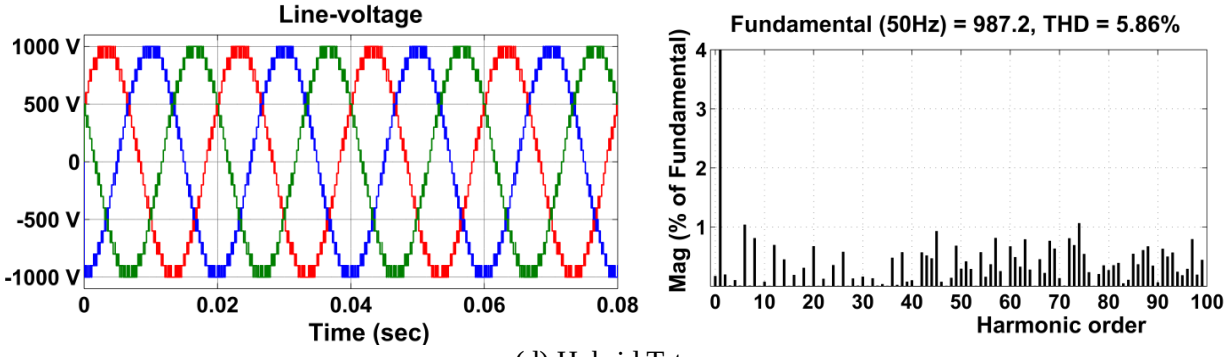
(a) MLDCL



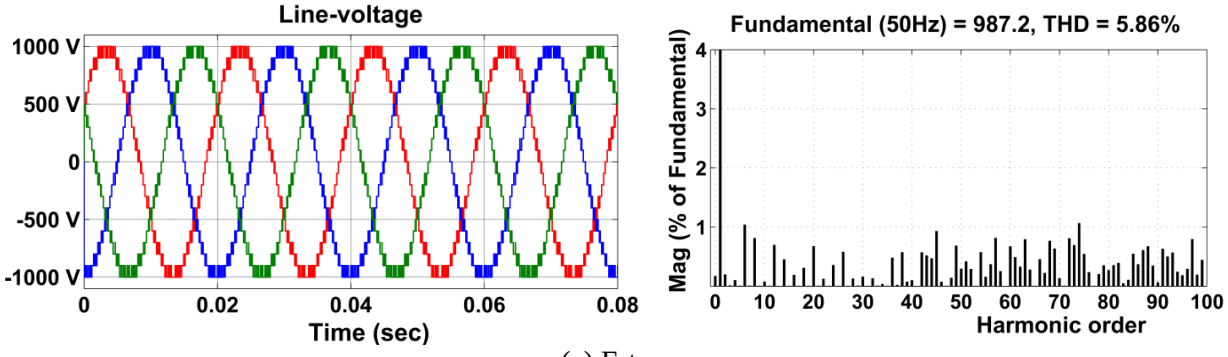
(b) SSPS



(c) SDS



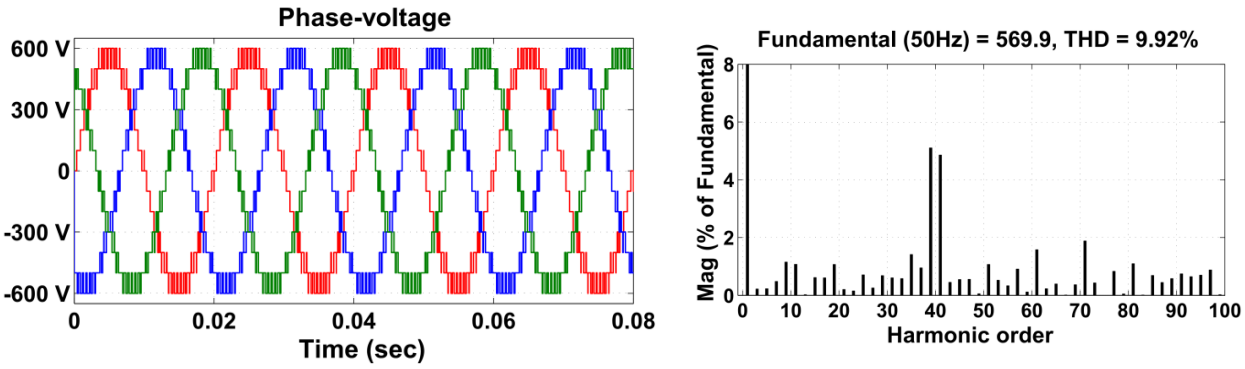
(d) Hybrid T-type



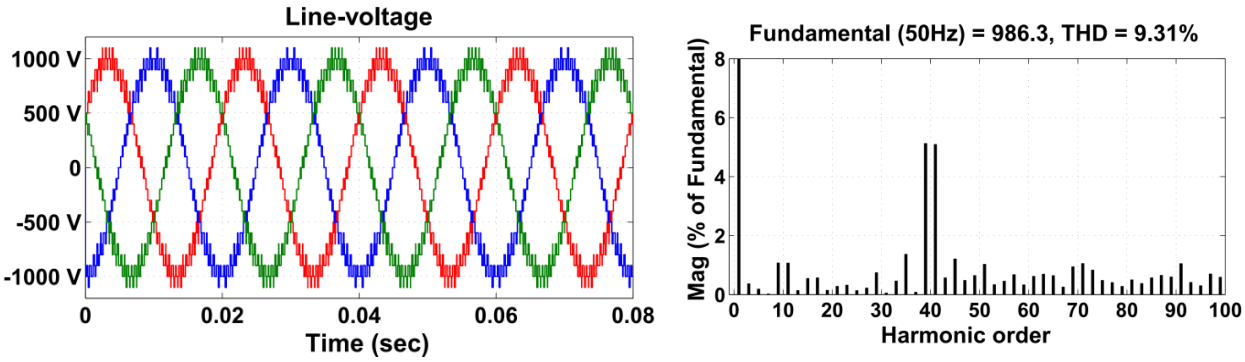
(e) E-type

Fig. 3.32: Line-voltage performance of various RSC-MLI with the proposed PWM.

To validate the superiority of the proposed modulation scheme, its performance is compared with conventional reduced carrier PWM scheme on thirteen-level asymmetrical MLDCL. The performance of thirteen-level asymmetrical MLDCL RSC-MLI shown in Fig. 3.33 with conventional reduced carrier arrangement. Fig. 3.33(a) depicts the phase-voltage waveform and harmonic performance of MLDCL inverter with conventional reduced carrier arrangement.



(a) Phase-voltage



(b) Line-voltage

Fig. 3.33: Performance of MLDCL with conventional reduced carrier arrangement.

Similarly, Fig. 3.33(b) depicts the line-voltage performance of MLDCL inverter with conventional reduced carrier arrangement. From Fig. 3.33(a) and (b), it is observed that this conventional method produces a THD of 9.92% in phase-voltage and 9.31% in line-voltage. Comparing Fig. 3.31(a)-(e) with Fig. 3.33(a), it can be observed that phase-voltage THD of proposed scheme (~10.39%) and conventional reduced carrier scheme (9.92%) are same and harmonics are centered around m_f. Even though their phase-voltage THD values are almost same and side-band harmonics are centered at m_f, but the order and magnitudes of the harmonics are different in both methods, which leads to significant difference in line-voltage THD as discussed in Section 3.2.1.1, 3.4.1.1, and 3.4.2.1. Comparing Fig. 3.32(a)-(e) with Fig. 3.33(b), proves the above statement where the line-voltage THD of proposed scheme (5.36%) is superior to conventional reduced carrier (9.31%) scheme. Finally, it can be concluded that the proposed modulation scheme produces identical performance on any RSC-MLI topologies with superior performance both in terms of waveform shape and line-voltage THD. Further, to ensure the

superior performance of the proposed scheme and evaluate the effect of computational burden on controller, next section presents the experimental validation.

3.5.4 Experimental validation

The performance of the proposed PWM scheme is validated by developing experimental set-ups of different three-phase IGBT based thirteen-level asymmetrical RSC-MLI topologies using two generalized inverter modules with 24-IGBTs in each.

The developed topologies are MLDCL, SSPS, switched dc sources, hybrid T-type and E-type (as shown in Fig. 3.30). To validate the superiority of the proposed PWM scheme, the above developed topologies are controlled using conventional reduced carrier PWM scheme. The modulation schemes are implemented in dSPACE Micro-lab box RTI1202 R&D controller. The carrier signal frequency (f_{cr}) and amplitude modulation index (m_a) are selected as 2 kHz and 0.98 respectively. The dc input source voltage (V_{dc}) is selected as 30 V and with this, the maximum amplitude of phase-voltage is 180 V. The complete list of parameters used in experimental study are given in Table 3.7.

Table 3.7: Experimental parameters.

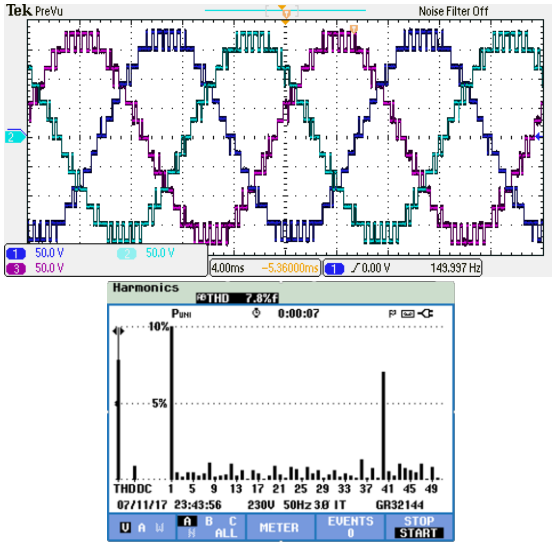
Circuit/Parameter	**Component/Value**
30V isolated dc power supplies (12 No.)	30 V, 3 A dual channel regulated power supply
Thirteen-level asymmetrical RSC-MLI	Developed using 2 modules of generalized converter with 24 IGBTs each
IGBT switch model and rating	IKW40T120, 40 A and 1200 V
Carrier frequency (f_{cr})	2 kHz
Amplitude modulation index (m_a)	0.95
Load	Three-phase star-connected 1 kW 0.85 power factor lagging.
Controller (To obtain firing signals for IGBTs)	dSPACE MicroLabBox RTI1202 R&D controller Sampling time (20 μs)

Fig. 3.34(a)-(e) shows the phase-voltage performance of thirteen-level MLDCL, SSPS, switched dc sources, hybrid T-type and E-type asymmetrical topologies with proposed switching logic involving modified reduced carrier arrangement (Scale: X-axis: 4 ms/div. and Y-axis: 50 V/div.). Fig. 3.34(f) depicts the phase-voltage performance of thirteen-level MLDCL with conventional reduced carrier arrangement. From Fig. 3.34(a)-(e), it is observed that all the phase-voltage waveforms and their harmonic spectra are identical with dominant harmonic appeared at frequency modulation index (m_f = 40). Comparing Fig. 3.34(f) with Fig. 3.34(a)-(e), it can be observed that THD values of conventional reduced carrier scheme (6.1%) is less when compared to proposed scheme (7.8%). Nevertheless, the conventional reduced carrier

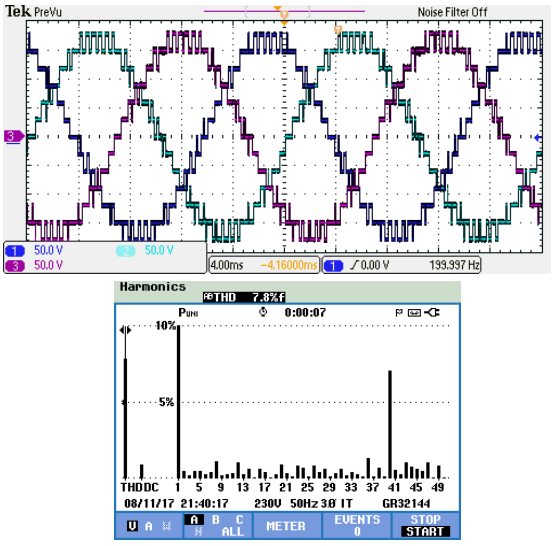
PWM scheme has less THD value but its side-band harmonics are different and centered at m_f. Magnitude of the harmonics are also different in both methods, which leads to significant difference in line-voltage THD.

Similarly, Fig. 3.35 depicts the experimental line-voltage performance of these RSC topologies with proposed and conventional reduced carrier PWM (Scale: X-axis: 10 ms/div. and Y-axis: 5 V/div.). Line-voltages and their corresponding harmonic spectra of the considered thirteen-level asymmetrical topologies with the proposed scheme are shown in Fig. 3.35(a)-(e). Fig. 3.35(f) depicts the line-voltage performance of thirteen-level MLDCL with conventional reduced carrier PWM scheme are identical in terms of waveform shape and harmonic performance. The obtained THD are identical with side-band harmonics centered at $m_f = 40$. Comparing Fig. 3.35(a)-(e) with Fig. 3.35(f), it is observed that the proposed scheme produces improved harmonic performance (2.8%) when compared to conventional reduced carrier PWM scheme (6.0%). The reason for this is the proposed PWM scheme will helps for better cancelation of harmonics presented in phase-voltages.

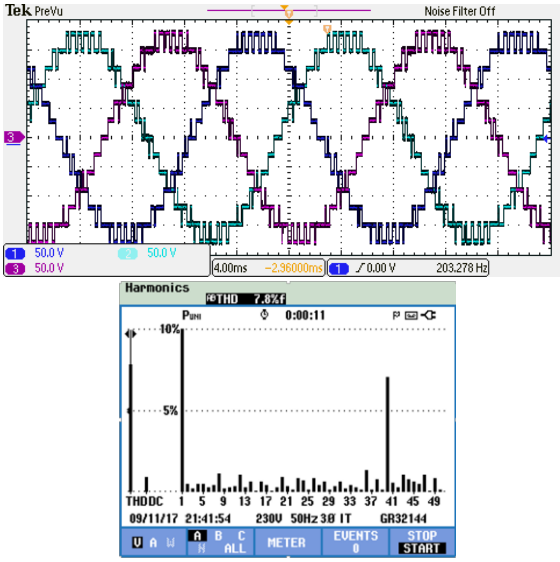
In order to evaluate the whole inverter system, it is necessary to show the performance of the inverter currents. Fig. 3.36 depicts the experimental line-current performance of RSC topologies with the proposed and conventional reduced carrier PWM schemes for three-phase star-connected load (Scale: X-axis: 10 ms/div. and Y-axis: 2 A/div.). Line-current and their corresponding harmonic spectra of the proposed scheme for considered thirteen-level asymmetrical topologies are shown in Fig. 3.36(a)-(e). Fig. 3.36(f) depicts the line-current performance of thirteen-level MLDCL with conventional reduced carrier PWM. From line-current performance shown in Fig. 3.36, it is observed that line-current waveforms and their corresponding harmonic spectra with the proposed PWM scheme are identical in terms of waveform shape and harmonic performance. It can also be observed that the proposed scheme produces improved harmonic performance (2.3%) when compared to conventional reduced carrier PWM scheme line-currents (5.4%) shown in Fig. 3.36(f). Further, the comparison between the obtained simulation and experimental performance of various RSC-MLIs controlled with proposed switching logic involving modified and conventional reduced carrier arrangement is depicted in Table 3.8.



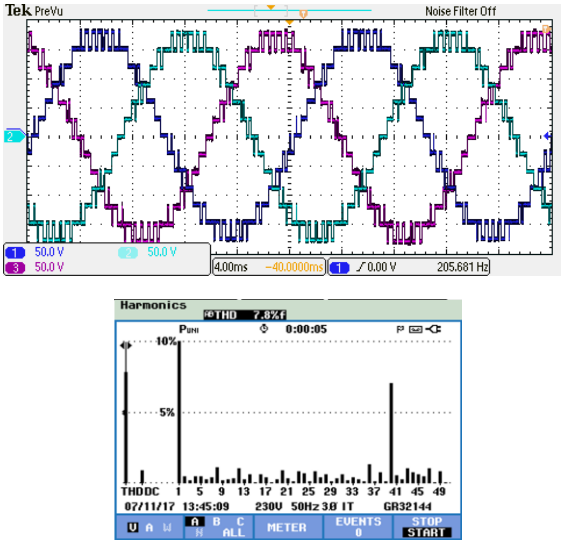
(a) MLDCL



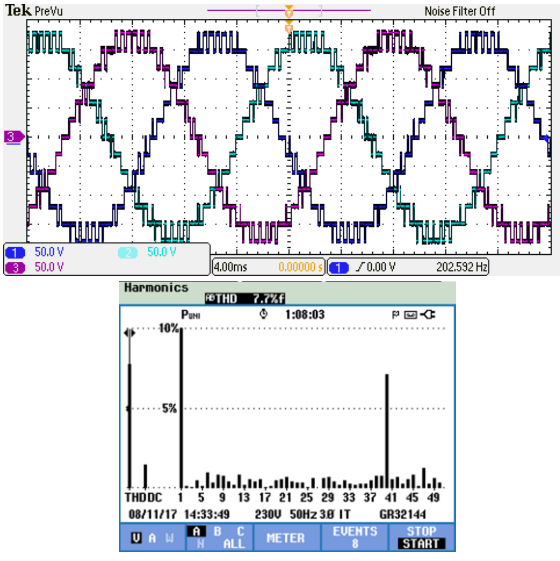
(b) SSPS



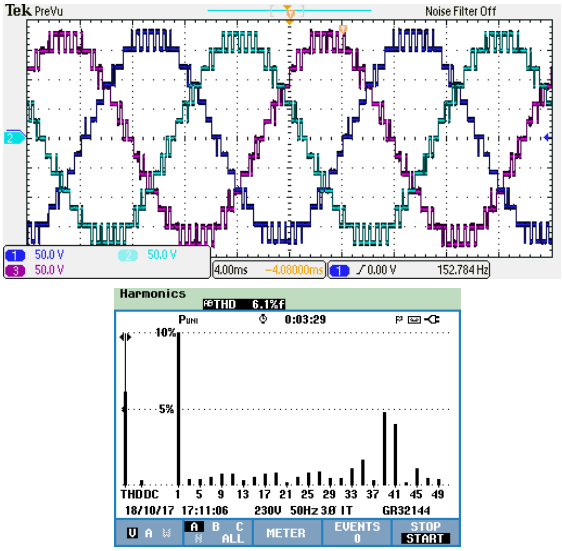
(c) Switched dc sources



(d) Hybrid T-type

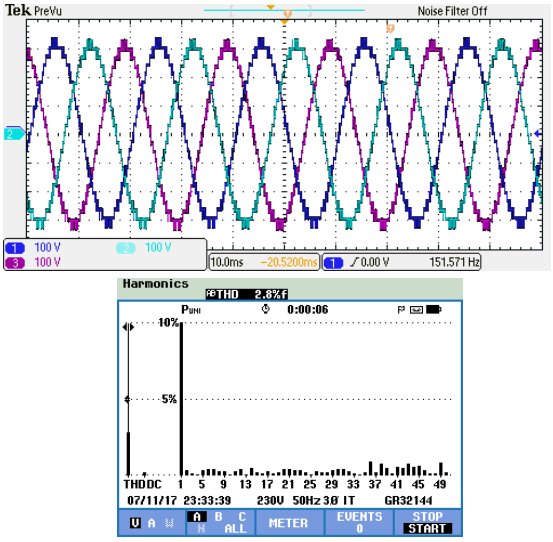


(e) E-type

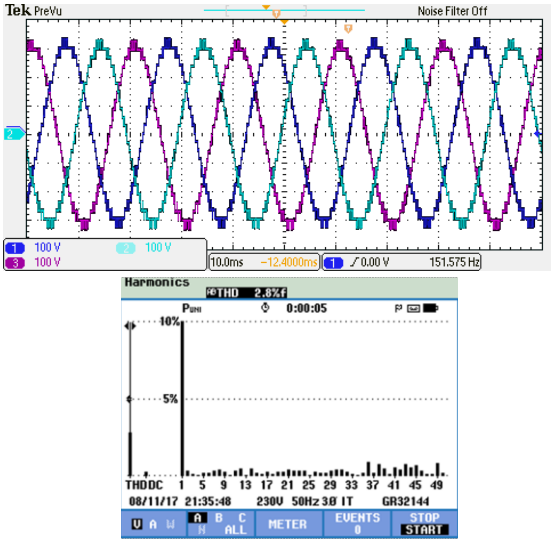


(f) MLDCL with conventional reduced carrier PWM

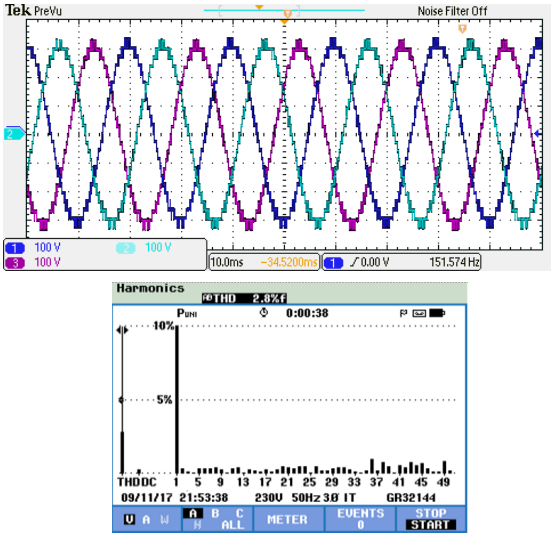
Fig. 3.34: Experimental phase-voltage performance of various RSC-MLI topologies.



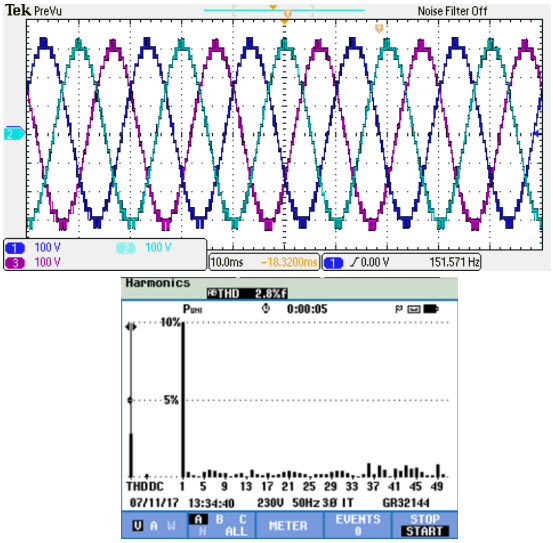
(a) MLDCL



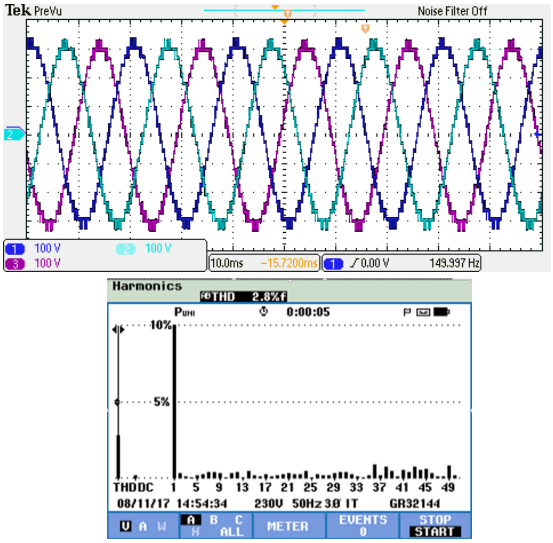
(b) SSPS



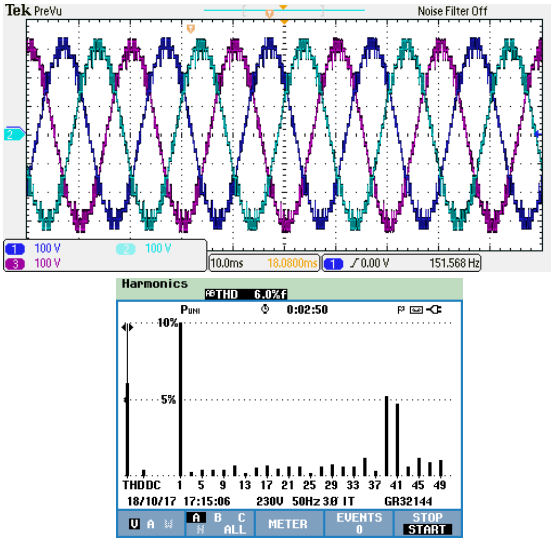
(c) Switched dc sources



(d) Hybrid T-type

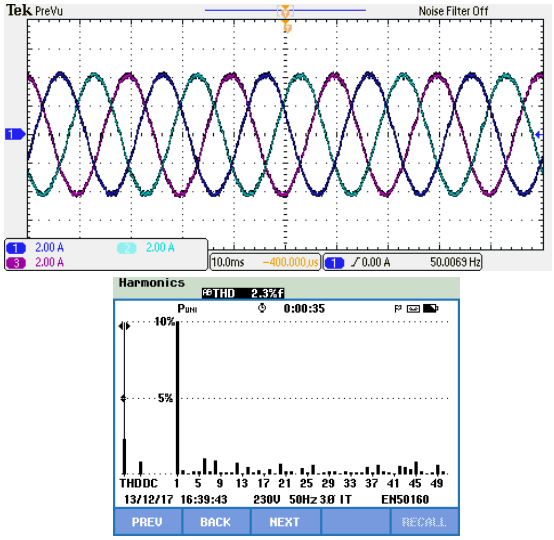


(e) E-type

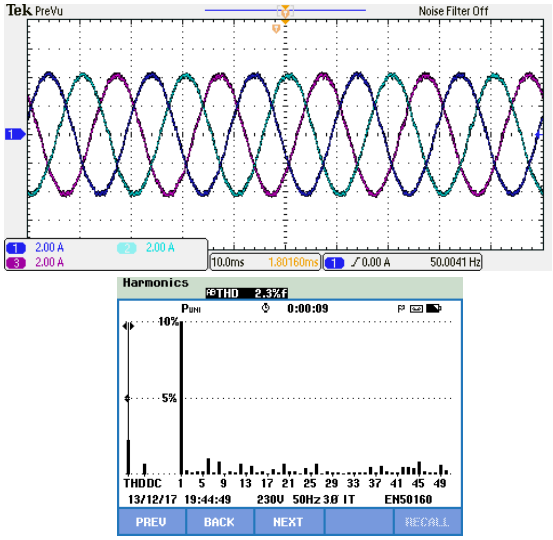


(f) MLDCL with conventional reduced carrier PWM

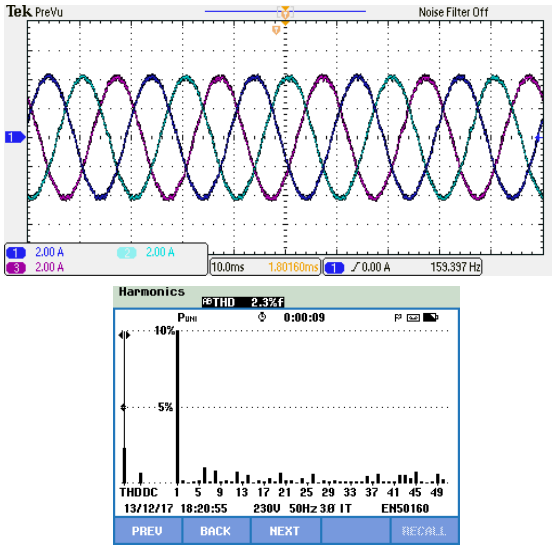
Fig. 3.35: Experimental line-voltage performance of various RSC-MLI topologies.



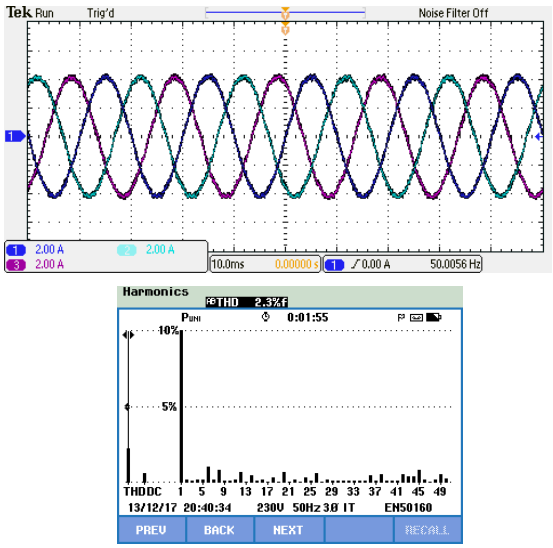
(a) MLDCL



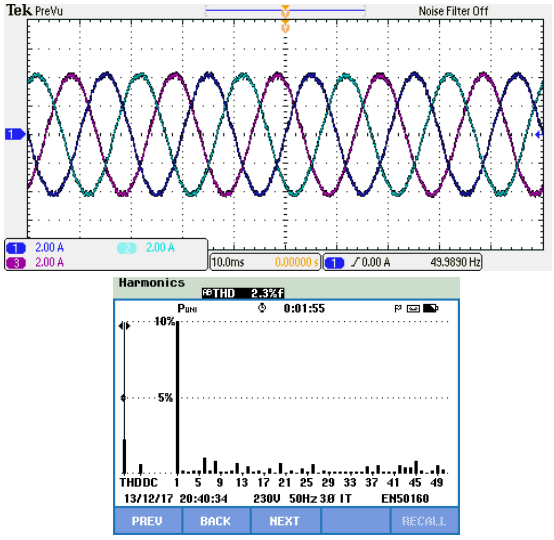
(b) SSPS



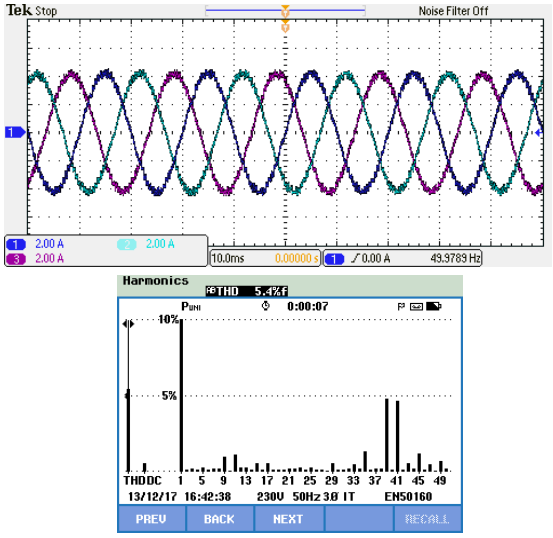
(c) Switched dc sources



(d) Hybrid T-type



(e) E-type



(f) MLDCL with conventional reduced carrier PWM

Fig. 3.36: Experimental line-current performance of various RSC-MLI topologies.

From Table 3.8, superior line-voltage THD performance of the proposed PWM over the conventional reduced carrier arrangement can be clearly verified. Also, Table 3.8 verifies the capability of proposed switching logic to control any RSC-MLI, irrespective to the voltage ratios and topological arrangement. From the Table 3.8, it is inferred that considered the thirteen-level phase-voltage level, computation time of proposed switching logic remains to be same (9 μs) irrespective to the topological configuration.

Table 3.8: Simulink and experimental performance of the proposed modified reduced carrier PWM on thirteen-level asymmetrical RSC-MLIs.

Proposed switching logic	**Topology**	**Simulation performance**		**Experimental performance**		
		Phase-voltage THD	**Line-voltage THD**	**Phase-voltage THD**	**Line-voltage THD**	**computation time**
Modified reduced carrier arrangement	MLDCL	10.39%	5.86%	7.8 %	2.8 %	9.2 μs
	SSPS	10.41%	5.97%	7.8 %	2.8 %	9.3 μs
	Switched dc sources	10.39%	5.86%	7.8 %	2.8 %	8.9 μs
	Hybrid T-type	10.39%	5.86%	7.8 %	2.8 %	9.1 μs
	E-type	10.39%	5.86%	7.7 %	2.8 %	9.2 μs
Conventional reduced carrier arrangement	MLDCL	9.92%	9.31%	6.0%	5.4%	9.1 μs

From Table 3.8, a variation in THD recorded in simulation and experimental studies are observed. This is due to the MATLAB simulator, which measures the THD upto Nyquist frequency (i.e., 499th order harmonic), where Fluke power quality analyser used for recording experimental THD measures up to 49th order harmonics. However, minimizing measurable THD frequency limit to 49th order in MATLAB simulator makes the simulation THD equal to experimental THD recorded. But this is not opted in simulation, because it is necessary to observe the complete harmonic spectrum of inverter output voltages.

Hence Fig. 3.36 and Table 3.8, verifies that the proposed PWM scheme obtains superior line-voltage performance compared to the conventional reduced carrier PWM and the proposed switching logic can realize any RSC-MLI irrespective to the voltage ratios. Also implementation of the proposed switching logic produces nearly uniform controller computation time on any RSC-MLI, for a given level. Further, to investigate the potentiality of the proposed reduced carrier PWM, its performance is compared with state-of-the-art schemes reported in the literature and is presented in the next section.

3.5.5 Comparison with state-of-the-art of PWM schemes

In a view to estimate the effectiveness of the proposed PWM scheme, a comprehensive comparison is carried out with conventional carrier based PWM schemes reported for RSC-MLI topologies. For this, the PWM scheme along with the inverter reported in literature is implemented experimentally and compared with proposed PWM scheme in terms of harmonic performance, complexity in implementation and computation burden. The summery of merits and demerits are presented in Table 3.9.

Finally, from the performance evaluation presented in Table 3.8 and Table 3.9, the following conclusions are derived.

- The proposed switching logic with unified logic expressions is directly applicable to any MLI topology and easily scalable to higher number of levels irrespective of topological arrangement and dc voltage ratios.
- The proposed reduced carrier arrangement produces improved line-voltage THD compared to conventional reduced carrier and multicarrier PWM schemes and similar THD performance when compared to switching function PWM scheme.
- The turnaround time for implementation of the proposed switching logic is significantly reduced and remains almost same for a given number of levels in any inverter. The less computation burden of the proposed scheme will allow the controller to accurately implement higher switching frequencies.

Table 3.9: Performance comparison of proposed unified logic PWM with conventional PWM schemes of RSC-MLI.

Carrier based PWM scheme and topology reported in literature					**With proposed PWM scheme**			**Merits and demerits of PWM scheme reported in literature**
PWM Scheme	**Topology**	**Phase-voltage THD**	**Line-voltage THD**	**Turnaround time**	**Phase-voltage THD**	**Line-voltage THD**	**Turnaround time**	
Multi-reference [58, 60, 87, 88]	T-type Seven-level [11]	**15.7%**	**14.8%**	**6.5 μs**	**15.7%**	**4.9%**	**6.2 μs**	✓ Require less computational time ✓ Scalable to higher levels ✓ Directly applicable to all topologies ✓ High line-voltage THD × Difficulty in implement for closed-loop applications due to the presence of multiple references
Reduced carrier with logic gates [9, 10, 27]	Modified T-type Seven-level [10]	**15.8%**	**15.0%**	**19 5 μs**	**15.6%**	**4.8%**	**5.9 μs**	× High line-voltage THD × Switching logic is complex and requires more computational time × Neither scalable nor directly applicable to all topologies
Switching function PWM [77, 91]	Symmetrical Seven-level Switched dc sources	**15.6%**	**4.8%**	**7.5 μs**	**15.5%**	**4.7%**	**6.0 μs**	✓ Good line-voltage THD performance ✓ Scalable and applicable to all topologies × Involves large number of comparators which occupies more memory and requires more computation time to realize the switching pulses
Reduced carrier [55]	RV Seven-level [55]	**15.7%**	**14.9%**	**5.3 μs**	**15.6%**	**4.8%**	**6.1 μs**	✓ Scalable with simplified switched logic ✓ Less computational time. × Not applicable to all topologies × High line-voltage THD
Hybrid PWM [17, 20, 22, 32]	Asymmetrical SSPS with H-bridge Eleven-level [17]	**9.9%**	**3.1%**	**6.6 μs**	**9.6%**	**3.0%**	**7.2 μs**	✓ Good line-voltage THD performance ✓ Scalable and possess simplified switched logic ✓ Less computational time × Applicable only to asymmetrical cascaded topologies × May involves mixed switching frequencies, hence may produce unwanted voltage spikes in phase and line-voltages

3.6 Summary

To overcome the limitations of the conventional PWM schemes, this chapter presented a modified reduced carrier PWM scheme with unified logical expressions. The efficacy of the proposed switching logic is validated with experimental studies on various thirteen-level asymmetrical RSC-MLI topologies. Further, superior performance of proposed scheme is verified by comparing its performance with conventional carrier PWM schemes. Topology independent operation, simplified switching logic generalization to higher levels, less computation burden and improved line-voltage THD performance of the proposed reduced carrier PWM scheme serves as a viable solution to overcome the demerits of conventional multicarrier, reduced carrier and multi reference PWM schemes.

CHAPTER 4: FTO OF MLDCL BASED RSC-MLI

This chapter presents the fault tolerant nature of RSC-MLIs to ensure its reliability. First, various fault tolerant strategies reported for compensating open-circuit faults on MLIs are discussed. Further, a generalized fault tolerant scheme is proposed to compensate simultaneous failure of multiple switches in MLDCL based RSC-MLI.

4.1 Introduction

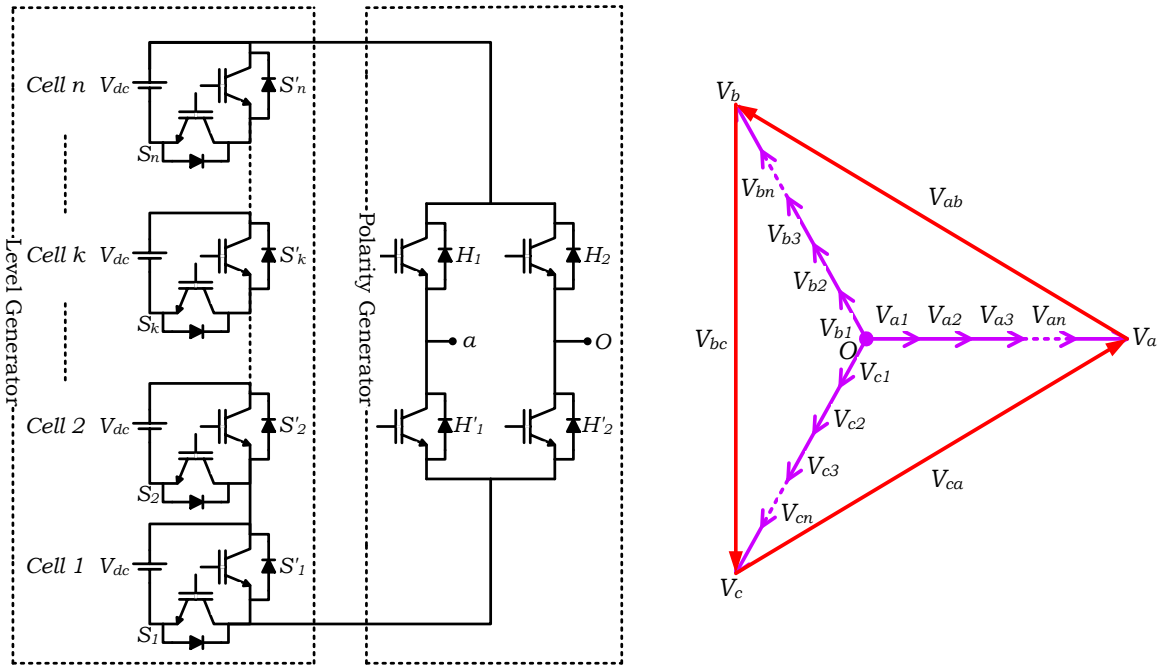
The ability of an inverter to work in fault prone conditions plays a vital role in ensuring the safety and reliability of the overall system. Any fault(s) on the inverter will restrict the phase-voltage levels and produce unbalance in line-voltage and currents. Malfunction of the inverter may degrade the overall system performance, produce temperature effects with abnormal voltages/currents and result dangerous effects on the load end. There are multiple internal and external reasons for occurrence of fault in power converters, however every fault ends up with either open-circuit (OC) or short-circuit (SC) of a particular switch or associated unit/bridge [111-113]. However, SC fault results in dangerously high current not only through the faulted switch but also through faulted phase and cause a possible damage to the inverter. Therefore to avoid these faults, a fast acting over current protection circuits are required [111-114]. On the other hand, OC faults are not severe and can be compensable [111, 115, 116]. Hence, this chapter analyses the effect of OC faults only.

In case of OC switch faults, switching redundancies play an important role in reconfiguration of the inverter. However, extreme reduction in switch count of RSC-MLI has drastically reduced its switching redundancies and restricted its fault tolerant ability [52, 116, 117]. This increases the difficulty in achieving fault tolerant operation (FTO) of the inverter [111, 118]. Among the various RSC-MLIs reported in the literature, topologies with modular and redundant structure such as MLDCL possess an ability to restore the balanced condition by compensating an OC fault fully/partially [52, 53]. However, their FTO is limited and bounded in comparison to classical CHB MLI. Further, the growing interest of RSC-MLI for various industrial and domestic applications, has increased the necessity and prominence of RSC-MLI topologies with the ability to tolerate and operate in fault conditions. Therefore, this chapter investigates the OC fault tolerant ability of modular redundant RSC-MLIs such as MLDCL.

4.2 Fault analysis of MLDCL based RSC-MLI

Among the recently reported RSC-MLI topologies, MLDCL is one of the popular topology with modular structure and adequate switching redundancies [52, 53]. The redundant structure of MLDCL with floating dc link capacitors turns it to be an attractive alternative to CHB for

regenerative front-end converters, power quality improvement and grid connected applications. This section presents the operation of MLDCL inverter for normal and faulty operating conditions. Generalized circuit of MLDCL with *n* basic units per phase is shown in Fig. 4.1(a). The structure of MLDCL is divided into level generator and polarity generator. Level generator is responsible for producing *n*-level unipolar voltage. Polarity generator has an H-bridge in each phase with switches operating at fundamental frequency and converts this unipolar voltage to bipolar with $(2n-1)$ levels in phase-voltage. The switching operation of MLDCL can be refereed from Chapter 2. From the switching operation it can be observed that, each basic unit of level generator has one isolated dc source with complimentary switch pair (S_k and S_k') and produces either V_{dc} or zero, where k is an intermediate unit between 1 to n. In any unit, conduction of S_k produces V_{dc} across the respective unit and conduction of S_k' forces the voltage across the respective unit to zero.



(a) Single-phase MLDCL circuit (b) Phasor diagram of inverter voltages

Fig. 4.1: Generalized structure of MLDCL and its phasor diagram.

If v_{a1}, v_{a2},…., and v_{an} are the output voltages of each basic unit of phase-*a*, obtained after processing through the polarity generator, then the total voltage of phase-*a*, v_a is expressed as (4.1) [119]. The modulating signals for phase-voltages are expressed in (4.2) and the corresponding phasor diagram for balanced operation of the inverter is shown in Fig. 4.1(b).

$$v_a = \sum_{k=1}^{n} v_{ak} = v_{a1} + v_{a2} + ... + v_{an} \tag{4.1}$$

Where, $v_{a1} = v_{a2} = v_{an} = m_a V_{dc} \sin \omega t$ and m_a is amplitude modulation index. Similarly, for phase-*b* and *c*, $v_b = \sum_{k=1}^{n} v_{bk}$ and $v_c = \sum_{k=1}^{n} v_{ck}$.

Therefore,

$$\left.\begin{aligned} v_a &= n\,m_a V_{dc}\sin\omega t \\ v_b &= n\,m_a V_{dc}\sin\left(\omega t - 120^\circ\right) \\ v_c &= n\,m_a V_{dc}\sin\left(\omega t - 240^\circ\right) \end{aligned}\right\} \tag{4.2}$$

OC faults in MLDCL can occur either in polarity generator or in level generator or in both. However, as the switches in polarity generator operate at fundamental frequency, any fault(s) on polarity generator result in missing of either positive/negative half cycle or complete waveform. Under such conditions FTO is not feasible. On the other hand, OC faults on level generator can be partially/fully compensated due to its modular structure with identical basic units. OC faults on level generator are analyzed by considering the deviations in phase-voltage levels. Referring to Fig. 4.1(a), OC faults in MLDCL (on level generator) are classified into Type-1 (OC of S_k) and Type-2 (OC of S_k') faults. It is to be noted that, S_k and S_k' are complimentary switch pair and, at any instant one among them should remain in conduction to ensure the connectivity of k^{th} unit with the adjacent units (which ensures the inverter connectivity with the load).

Type-1 *fault* (*OC fault on switch* S_k): OC fault on S_k in k^{th} basic unit, should ensure S_k' to remain in conduction. Conduction of S_k' forces the voltage of the corresponding unit to zero i.e., the voltage across the k^{th} basic unit to zero. This further limits the maximum voltage across level-generator to $(n-1)V_{dc}$ (phase-voltage levels to $\pm(n-1)V_{dc}$), but produces phase-voltage levels with uniform $\mathrm{d}v/\mathrm{d}t$. The effect of Type-1 fault(s) on inverter phase-voltage is given in Table 4.1. If the number of faulty units on one phase is different from other, then this produces unbalance in phase-voltages without effecting the $\mathrm{d}v/\mathrm{d}t$. This nature of unbalance is compensable with various fault tolerant schemes (FTS) reported in literature.

Table 4.1: Effect of Type-1 fault on phase-voltage levels.

OC fault of S_k	**Missing levels**
No fault	None
Fault in one basic unit	$\pm nV_{dc}$
Fault in two basic units	$\pm nV_{dc}$ & $\pm(n-1)V_{dc}$
Fault in 'k' basic units	$\pm nV_{dc}$, $\pm(n-1)V_{dc}$... & $\pm(n-k+1)V_{dc}$

Type-2 *fault* (*OC fault on* S_k'): OC of S_k', ensures S_k to remain in conduction. This maintains the voltage across the k^{th} basic unit (faulty unit) as V_{dc}. Therefore, the minimum voltage of the level generator raise to V_{dc} and the output of the level generator varies from V_{dc} to nV_{dc}. This results in missing of zero-level in phase-voltage. However, this zero level can be achieved in polarity generator. Hence, Type-2 fault on any single unit is compensable and does not require fault tolerant scheme (FTS). The effect of Type-2 faults on phase-voltage levels is given in Table 4.2.

However, if such a fault appears on two units of same phase, then the minimum voltage of level generator raises to $2V_{dc}$, which results in missing of $\pm V_{dc}$ and 0 levels in phase-voltage. Missing of $\pm V_{dc}$ level cannot be restored by any other switching path and results in unequal dv/dt. Hence, this type of fault is intolerable and further cannot be compensated by any FTS. Table 4.1 and Table 4.2 concludes that FTO can be achieved only for Type-1 faults. Effect of Type-1 fault on MLDCL is similar to the effect of an OC fault of an H-bridge in CHB MLI. To tolerate such type of faults, several FTS are reported on CHB. If an OC fault occurs on any unit of a modular redundant MLI such as CHB or MLDCL, then the voltage obtained from the corresponding faulty unit is forced to zero. This by-passes the faulty unit and produces unbalance in phase and line-voltages.

Table 4.2: Effect on Type-2 fault on phase-voltage levels.

OC fault of S'_k	**Missing levels**
No fault	None
Fault in one basic unit	None
Fault in two basic units	$\pm V_{dc}$
Fault in three basic units	$\pm V_{dc}$ & $\pm 2V_{dc}$
Fault in 'k' basic units	$\pm V_{dc}, \pm 2V_{dc} \ldots$ & $\pm(k-1)V_{dc}$

Assuming OC fault on multiple units of an inverter shown in Fig. 4.1(a), such that x units in phase-a, y units in phase-b and z units in phase-c are faulty. This creates an unbalance in phase and line-voltages as shown in Fig. 4.2 where $k = 1, 2, \ldots (n-x)$ for phase-a; $k = 1, 2, \ldots (n-y)$ for phase-b and $k = 1, 2, \ldots (n-z)$ for phase-c. This unbalance in terms of phase-voltages is given in (4.3).

$$\left.\begin{aligned} v_a &= (n-x)\left[n\, m_a V_{dc} \sin \omega t\right] \\ v_b &= (n-y)\left[n\, m_a V_{dc} \sin\left(\omega t - 120^\circ\right)\right] \\ v_c &= (n-z)\left[n\, m_a V_{dc} \sin\left(\omega t - 240^\circ\right)\right] \end{aligned}\right\} \qquad (4.3)$$

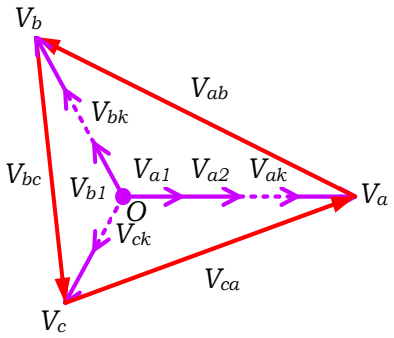


Fig. 4.2: Illustrating unbalanced operation under faulted condition.

4.3 Fault tolerant methods for compensating OC faults

In literature, various methods have been reported to diagnosis, isolate and compensate OC faults [111-118, 120-123]. To identify the location of OC faults, methods using measurement of

voltage and current of either switching device or inverter are reported in [114, 116]. Further to isolate the fault, either passive protection devices such as fuses or active protection devices such as relays or TRIACs are incorporated. However, involvement of these auxiliary equipment for fault compensation complicates the topology and raises the overall cost [111, 115, 116]. Hence, various pulse width modulation (PWM) schemes which does not require any auxiliary equipment to obtain FTO are reported [82, 111, 116, 121-124]. PWM schemes such as space vector modulation (SVM) and carrier based schemes are reported for compensating single switch/bridge/basic unit fault in two-level or MLI/RSC-MLI such as T-type are reported [82, 116, 118]. Among these PWM based schemes, SVM is an attractive scheme which can achieve FTO by creating switching redundancies, and however its complex implementation acts as a limitation at higher levels. On the other side, irrespective to the hardware solutions or PWM schemes, fault tolerant schemes (FTS), which generates a new set of modulating signals to reconfigure the inverter to obtain FTO are reported [29, 116, 118, 119, 125-129]. These schemes can be applicable to the inverter with modular redundant topological structures such as CHB [29, 111, 116, 119, 125-129]. Among these schemes, (a) by-passing method [29, 111, 116, 119, 125], (b) increasing the burden on healthy units/cells [119] and (c) Neutral shifting (NS) FTS [29, 111, 119, 125-129] are the popular schemes reported to tolerate OC switch faults in CHB MLI.

Therefore, this chapter investigates the fault tolerant ability of these schemes and discusses their limitations in compensating multiple switch faults on modular redundant RSC-MLIs such as MLDCL. Further, proposes a generalized NS-FTS to compensate multiple switch faults and evaluates its ability in obtaining FTO of MLDCL inverter for various fault conditions.

4.3.1 By-passing method

One of the simplest approach to restore the balanced operation is to ensure the number of operating units on all the phases are equal [29, 111, 116, 119, 125]. To restore the balanced operation, this method by-passes few healthy units on one or more phases, such that the number of operating units on all the phases are same. Thus, this method of compensation forces the voltage contributed by few healthy units on one or more phases to zero, such that voltage contributed by all the phases is same. The number of healthy units to be by-passed depends on number of operating units on each phase. It is to be noted that the by-passing should not be carried out on the phase with maximum number of faulty units, as this phase contributing lowest voltage. For example, three units are operating in each phase in healthy condition, this fault tolerant method for one unit fault in phase-*a* is illustrated in Fig. 4.3. If a fault appears on one unit of phase-*a*, then the total voltage contributed by phase-*a*, *b* and *c* are $\pm 2V_{dc}$, $\pm 3V_{dc}$ and $\pm 3V_{dc}$. Thus to restore the balanced operation, this method by-passes one unit on phase-*b* and phase-*c*. By-passing of one unit in phase-*b* and phase-*c*, ensures the operating units on all phases are same with each phase producing a maximum

voltage of $\pm 2V_{dc}$ as shown in Fig. 4.3. This method is easy to implement and can compensate simultaneous failure of multiple switches. However by-passing of the operating units, derates the inverter and reduces its efficiency. Thus, for achieving FTO without by-passing any healthy unit, "increasing burden" FTS is reported and is presented below.

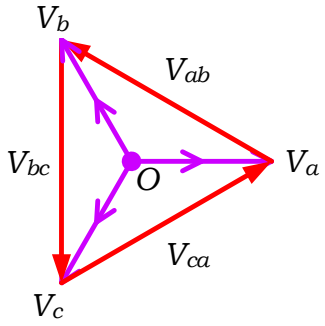


Fig. 4.3: Illustrating balanced condition with by-passing method.

4.3.2 Increasing burden

This method obtains FTO by sharing the burden of faulty units of a phase across the healthy units of same phase, such that magnitude of the overall phase-voltage after compensation is equal to its pre-fault voltage [119]. Sharing this fault burden, enforces additional burden on healthy units thus this method of fault compensation is called as increasing burden method. For example, consider a CHB with fault condition shown in Fig. 4.2, where the unbalanced phase-voltages are given in (4.3). In such condition, to compensate the fault, this method shares the burden of x faulty units of phase-a across $(n-x)$ healthy units of the same phase, such that total voltage contributed by these $(n-x)$ healthy units is same as that of the total voltage contributed by n units in pre-fault condition. This increases a burden of $\frac{n}{(n-x)}$ in each operating unit of phase-a. Similarly, a burden of $\frac{n}{(n-y)}$ for phase-b and $\frac{n}{(n-z)}$ for phase-c is increased for each operating unit. Thus, this method of compensation produces balanced phase-voltages (v_a', v_b' and v_c') as given in (4.4) and shown in Fig. 4.4.

$$\left.\begin{aligned} v_a' &= (n-x)\left[\frac{n}{(n-x)} m_a V_{dc} \sin \omega t\right] \\ v_b' &= (n-y)\left[\frac{n}{(n-y)} m_a V_{dc} \sin(\omega t - 120°)\right] \\ v_c' &= (n-z)\left[\frac{n}{(n-z)} m_a V_{dc} \sin(\omega t - 240°)\right] \end{aligned}\right\} \quad (4.4)$$

This scheme can compensate simultaneous failure of multiple switches and obtains balanced operation without by-passing any of the operating (healthy) unit. However, this method possess the following limitations.

- **Non-uniform power distribution among operating units**: From Fig. 4.4, the magnitude of voltage contributed by each unit in phase-*a,* is different from phase-*b* and *c*, respectively. This non-uniform burden among the operating units result non-uniform power distribution. This further reflects unbalance in dc link voltages, which is not desired in closed-loop applications.
- **Drives to overmodulation***:* If the number of faulty units increases, then the amplitude modulation index increases and drives the phase-voltage to overmodulation.

Thus, to overcome the limitations of this method, neutral shifting (NS) FTS is reported and is discussed in next section.

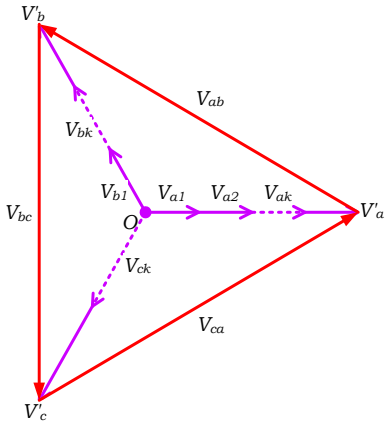


Fig. 4.4: Illustrating fault compensation with increasing burden method.

4.3.3 Neutral shifting

Investigating the effect of OC fault shown in Fig. 4.2, it can be observed that these faults produce unbalance in phase-voltage magnitudes but not among phase-angles. As the magnitude of line-voltages depends on the magnitude and angle of phase-voltages, the appeared unbalance in phase-voltages reflects in line-voltages as well. Therefore, this method of FTS intends to obtain balanced line-voltages by controlling both the magnitude and angle of phase-voltages. Thus, this method modifies the angle between consecutive phase-voltages, such that they produce balanced set of line-voltages. Hence, the magnitude unbalance due to faulty units and changing the angles between phase-voltages shifts the neutral point of the inverter and thus the name neutral shifting (NS) is derived.

Usually, this method of NS involves manual calculations to modify the angle between consecutive phase-voltages to ensure balanced line-voltages [29, 111, 125-128]. If V_a, V_b and V_c are the pre-fault phase-voltages, and θ_{ab}, θ_{bc}, θ_{ca} are phase-angles between the consecutive phases, then the line-voltage magnitudes can be expressed as given in (4.5).

$$\left.\begin{aligned} |V_{ab}| &= V_a^{\,2} + V_b^{\,2} - 2V_aV_b\cos(\theta_{ab}) \\ |V_{bc}| &= V_b^{\,2} + V_c^{\,2} - 2V_bV_c\cos(\theta_{bc}) \\ |V_{ca}| &= V_c^{\,2} + V_a^{\,2} - 2V_cV_a\cos(\theta_{ca}) \end{aligned}\right\} \tag{4.5}$$

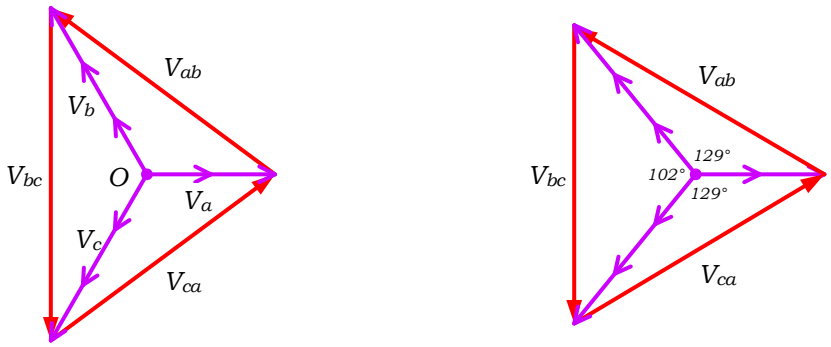
Under faulted condition, NS FTS modifies the angles of the unbalanced phase-voltages (V_a, V_b and V_c) such that they result in balanced set of line-voltages. The modified phase-angles θ'_{ab}, θ'_{bc}, θ'_{ca} are calculated by equalizing the magnitude of line-voltages as shown in (4.6).

Further, implementing these modified phase-angles (θ'_{ab}, θ'_{bc}, θ'_{ca}) among unbalanced phase-voltages, produces additional unbalance and shifts the neutral point of the inverter away from the origin. Shifting of the neutral creates new set of unbalanced phase-voltages (both angle unbalance and magnitude unbalance), which produce a balanced set of line-voltages.

$$\left.\begin{aligned} V_a^{\,2} + V_b^{\,2} - 2V_aV_b\cos(\theta'_{ab}) &= V_b^{\,2} + V_c^{\,2} - 2V_bV_c\cos(\theta'_{bc}) \\ V_b^{\,2} + V_c^{\,2} - 2V_bV_c\cos(\theta'_{bc}) &= V_c^{\,2} + V_a^{\,2} - 2V_cV_a\cos(\theta'_{ca}) \\ \theta'_{ab} + \theta'_{bc} + \theta'_{ca} &= 360° \end{aligned}\right\} \tag{4.6}$$

In literature, this method is reported for seven-level symmetrical CHB. Assuming an OC fault on one unit in phase-*a* of a seven-level inverter, the unbalance in phase-voltages is shown in Fig. 4.5(a) and given in (4.7).

$$\left.\begin{aligned} v_a &= 2m_aV_{dc}\sin\omega t \\ v_b &= 3m_aV_{dc}\sin(\omega t - 120°) \\ v_c &= 3m_aV_{dc}\sin(\omega t + 120°) \end{aligned}\right\} \tag{4.7}$$



(a) Before compensation (b) After compensation

Fig. 4.5: Implementation of NS-FTS for single unit fault on seven-level CHB MLI.

Substituting the magnitude of (4.7) in (4.6), the modified set of phase angles θ'_{ab}, θ'_{bc}, θ'_{ca} (129°, 129° and 102°) are determined, such that the line-voltages are balanced. Further, using these modified phase-angles, the modulating signals of phase-voltages (v_a'', v_b'' and v_c''), given in (4.8) are obtained and the corresponding FTO with (4.8) is shown in Fig. 4.5(b). Further, the phasor-representation of Fig. 4.5(b) verifies that ability of unbalanced post-fault phase-voltages (4.7) to obtain balanced set of line-voltages.

$$\left.\begin{aligned} v_a'' &= 2\,m_a V_{dc} \sin \omega t \\ v_b'' &= 3\,m_a V_{dc} \sin\left(\omega t - 129°\right) \\ v_c'' &= 3\,m_a V_{dc} \sin\left(\omega t + 129°\right) \end{aligned}\right\} \tag{4.8}$$

Usually, this method of NS involves manual calculations to modify the angles between phase-voltages to ensure balanced line-voltages. This method of NS with SHE PWM is reported for single/multiple faults in CHB MLI [126, 128]. In [128], this method is generalized for multiple switch faults on all phases, but can be implemented only if the number of faulty units in any two phases are same. If the number of faulty units on all the phases are different then, few healthy units on any phase are bypassed such that the number of operating units on any two phases are same. This method of bypassing healthy units reduces the performance and derates the inverter. In [126] multi-fault NS-FTS with modified SHE is reported. However, this method of NS-FTS involves complex mathematical calculations and is difficult to implement in closed-loop applications.

4.3.4 NS with zero-sequence injection

To overcome non-uniform power distribution of increasing burden FTS, NS with zero-sequence injection FTS is reported [119, 125, 129]. NS with zero-sequence injection FTS, injects a voltage component into the burdened balanced phase-voltages, such that they produce balanced line-voltages with uniform power distribution among all the operating units [119, 125, 129]. Addition of zero-sequence voltage shifts the neutral point of inverter [119] and thus this method is called as NS-FTS. The magnitude of injected zero-sequence voltage depends on the number of faulty units and plays a crucial role in retrieving FTO of the inverter. In literature, this scheme is reported for failure of single unit on CHB [119, 129]. In order to investigate the limitations of this scheme, its implementation for single unit fault on CHB is presented below.

Considering a three-phase CHB MLI with *n* units/phase, the unbalanced phase-voltages obtained for single unit fault on phase-*a* are given in (4.9).

$$\left.\begin{aligned} v_a &= \left(n-1\right)\left[m_a V_{dc} \sin \omega t\right] \\ v_b &= n\left[m_a V_{dc} \sin\left(\omega t - 120°\right)\right] \\ v_c &= n\left[m_a V_{dc} \sin\left(\omega t - 240°\right)\right] \end{aligned}\right\} \tag{4.9}$$

Compensation of this appeared fault (one unit fault on phase-*a)* with conventional "increasing burden" method is carried out and the obtained compensated phase-voltages v_a', v_b' and v_c' are given in (4.10), (4.11) and (4.12) respectively.

$$v_a' = \left(n-1\right)\left[\frac{n}{\left(n-1\right)} m_a V_{dc} \sin \omega t\right] \tag{4.10}$$

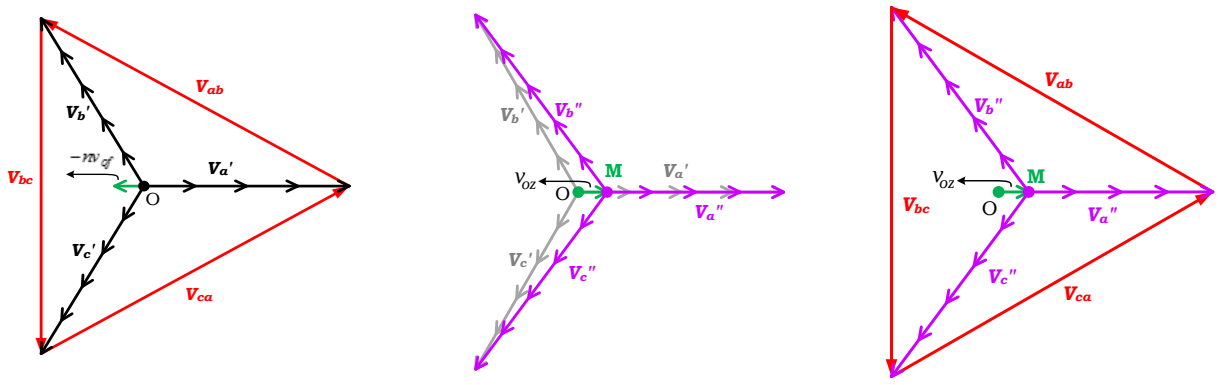
$$v_b' = n\left[m_a V_{dc}\sin\left(\omega t - 120°\right)\right] \tag{4.11}$$

$$v_c' = n\left[m_a V_{dc}\sin\left(\omega t - 240°\right)\right] \tag{4.12}$$

To overcome the demerit of unequal voltage distribution across the operating units, a zero-sequence voltage component (v_{of}) is injected in phase-opposition to the faulty phase as shown in Fig. 4.6(a). Thus, a voltage component of $-v_{of}\sin\omega t$ is injected in each operating unit of all phases, which results in injection of zero-sequence voltage $v_{oz}= -nv_{of}\sin\omega t$ in each phase-voltage v_a', v_b' and v_c'. The injection v_{oz} shifts the neutral point of inverter from O to M as shown in Fig. 4.6(b) and results new set of phase-voltages (v_a'', v_b'' and v_c'') as shown in Fig. 4.6(c) and given in (4.13).

$$\left.\begin{aligned} v_a'' &= (n-1)\left[\frac{n}{n-1}\left(m_a V_{dc}\sin\omega t - v_{of}\sin\omega t\right)\right] \\ v_b'' &= n\left[\left(m_a V_{dc}\sin\left(\omega t - 120°\right) - v_{of}\sin\omega t\right)\right] \\ v_c'' &= n\left[\left(m_a V_{dc}\sin\left(\omega t - 240°\right) - v_{of}\sin\omega t\right)\right] \end{aligned}\right\} \tag{4.13}$$

To achieve FTO, the obtained fault tolerant modulating signals (v_a'', v_b'' and v_c'') should be operated with appropriate PWM scheme. It is to be noted that the magnitude of injected voltage component plays a key role in attaining FTO.



(a) Burdened phase-voltages

(b) Injection of zero-sequence voltage

(c) After compensation.

Fig. 4.6: NS zero-sequence injection FTS for single unit fault on CHB MLI.

Thus, v_{of} should be determined such that the power delivered by each operating unit on all the phases is equal. Determination of v_{of} for tolerating single unit fault on phase-*a* is given in (4.14) [119]. The magnitude of v_{oz} depends on the number of faulty units in each phase. However, determination of v_{oz} reported in [119] is valid only for single unit fault and cannot be applicable for simultaneous failure of multiple switches on two or more phases [119, 129].

$$v_{of} = \frac{2}{3n-1} m_a V_{dc} \tag{4.14}$$

Therefore by reviewing various FTS for OC faults, the following conclusions are drawn.

- ❖ Among the various FTS reported on MLIs, NS is the most attractive scheme to tolerate OC faults.
- ❖ NS-FTS, reported for CHB MLI is also valid to control modular redundant inverter topologies such MLDCL [52, 53]. However, direct implementation is not possible.
- ❖ NS-FTS with SHE PWM involves elusive mathematical calculations to determine the switching instants.
- ❖ Generalized NS method reported for multiple faults in [128] requires by-passing of healthy units and thus derates the inverter.
- ❖ NS with zero-sequence injection FTS [119, 129] is reported for single unit fault and is not valid to compensate multiple faults.

Therefore, this thesis contributes to:

- ❖ Propose NS with zero-sequence injection FTS to RSC-MLIs with modular and redundant topological structures such as MLDCL
- ❖ Generalised equations are presented to determine the magnitude of injected zero-sequence voltage and fault tolerant modulating signals for any fault case.
- ❖ Involves modified reduced carrier PWM with carrier rotation.
- ❖ The proposed FTS obtains balanced line-voltages with uniform power distribution among the operating units of all phases.

4.4 Proposed generalized NS zero-sequence injection FTS

NS zero-sequence injection FTS is an efficient method to tolerate OC switch faults on MLIs and its fault compensation depends on the magnitude of injected zero-sequence voltage v_{oz}, which intern depends on the number of faulty units in the inverter. Determination of v_{oz} reported in [119] is not valid to compensate multiple switch faults. Therefore, this section proposes a generalized NS zero-sequence injection FTS.

4.4.1 Zero-sequence voltage injection for multiple faults

This section generalizes NS-FTS for simultaneous failure of multiple switches on all phases of MLDCL inverter and proposes formulae to determine the zero-sequence voltage for the given fault condition. The phasor diagram to implement NS zero-sequence injection FTS for simultaneous OC fault on multiple switches for various case studies are shown in Fig. 4.7, Fig. 4.8 and Fig. 4.9. In all these figures, v_a', v_b' and v_c' represent the balanced phase-voltages obtained from increasing burden method for various fault conditions. From these figures, it can be observed that the magnitude of phase-voltages v_a', v_b' and v_c', remain to be same for different fault conditions. This leads to the non-uniform voltage distribution and power sharing among the operating units. Therefore, to ensure uniform burden among the operating units of all phases, the proposed method

injects a zero-sequence voltage (v_{oz}) into the phase-voltages v_a', v_b' and v_c'. Fig. 4.7 shows the injection of v_{oz} for x number of faulty units in phase-*a*. Fig. 4.8 presents the injection of v_{oz} for multiple faults in two phases, i.e., x and y faulty units in phase-*a*, and *b* respectively. Similarly, Fig. 4.9 depicts injection of v_{oz} for multiple faults on all phases i.e., x, y and z faulty units in phase-*a*, *b* and *c* respectively.

In Fig. 4.7, as faulty units (x) are only in phase-*a*, a voltage component of xv_{of} in phase-opposition to phase-*a*, is injected into the operating units of all phases. Where v_{of} corresponds to the fraction of burden due to each faulty unit. Therefore for the considered fault case, a zero-sequence voltage $v_{oz} = -nxv_{of}\ sin\ \omega t$ is injected into v_a', v_b' and v_c' which results new set of phase-voltages (v_a'', v_b'' and v_c'') as given in (4.15)-(4.17). Injection of this zero-sequence voltage v_{oz} shifts the neutral point of the inverter from *O* to *M*, as shown in Fig. 4.7(b) and produces new set of phase-voltages (v_a'', v_b'' and v_c''). These new set of modified phase-voltages (reference voltages) given in (4.19)-(4.21) contribute to balance the line-voltages with uniform voltage distribution across the operating units on all phases as shown in Fig. 4.7(c).

For x-faulty units in phase-*a*:

$$v_a'' = (n-x)\left[\frac{n}{n-x}\left(m_a V_{dc}\sin\omega t\right)\right] + v_{oz} \tag{4.15}$$

$$v_b'' = n\ m_a V_{dc}\sin\left(\omega t - 120°\right) + v_{oz} \tag{4.16}$$

$$v_c'' = n\, m_a V_{dc}\sin\left(\omega t - 240°\right) + v_{oz} \tag{4.17}$$

Where, $v_{oz} = -\left(n\,x\,v_{of}\sin\omega t\right)$ (4.18)

Substituting (4.18) in (4.15), (4.16) and (4.17), produces (4.19)-(4.21).

$$v_a'' = (n-x)\left[\frac{n}{n-x}\left(m_a V_{dc}\sin\omega t - x\,v_{of}\sin\omega t\right)\right] \tag{4.19}$$

$$v_b'' = n\left[m_a V_{dc}\sin\left(\omega t - 120°\right) - xv_{of}\sin\omega t\right] \tag{4.20}$$

$$v_c'' = n\left[m_a V_{dc}\sin\left(\omega t - 240°\right) - xv_{of}\sin\omega t\right] \tag{4.21}$$

Considering simultaneous failure of x units in phase-*a*, and y units in phase-*b*, a voltage component xv_{of} in phase-opposition to phase-*a*, and yv_{of} in phase-opposition to phase-*b* should be injected into each operating unit of all phases as shown in Fig. 4.8. This results injection of zero-sequence voltage $-\left(n\,x\,v_{of}\sin\omega t + n\,y\,v_{of}\sin\left(\omega t - 240°\right)\right)$ into v_a', v_b' and v_c' as shown Fig. 4.8(b), given in (4.22), (4.23) and (4.24). Injection of this zero-sequence voltage v_{oz} shifts the neutral point of the inverter from *O* to *M*, and produces new set of phase-voltages (v_a'', v_b'' and v_c'') as shown in Fig. 4.8(c) and given (4.26)-(4.28).

For x faulty units in phase-a, and y faulty units in phase-b:

$$v_a'' = (n-x)\left[\frac{n}{n-x}\left(m_a V_{dc}\sin\omega t\right)\right] + v_{oz} \tag{4.22}$$

$$v_b'' = (n-y)\left[\frac{n}{n-y}\left(m_a V_{dc}\sin\left(\omega t - 120°\right)\right)\right] + v_{oz} \tag{4.23}$$

$$v_c'' = (n-z)\left[\left(m_a V_{dc}\sin\left(\omega t - 240°\right)\right)\right] + v_{oz} \tag{4.24}$$

Where, $v_{oz} = -\left(n\,x\,v_{of}\sin\omega t + n\,y\,v_{of}\sin\left(\omega t - 240°\right)\right)$ (4.25)

Further, substituting (4.25) in (4.22), (4.23) and (4.24), produces (4.26)-(4.28).

$$v_a'' = (n-x)\left[\frac{n}{n-x}\left(m_a V_{dc}\sin\omega t - \left(x\,v_{of}\sin\omega t + y\,v_{of}\sin\left(\omega t - 120°\right)\right)\right)\right] \tag{4.26}$$

$$v_b'' = (n-y)\left[\frac{n}{n-y}\left(m_a V_{dc}\sin\left(\omega t - 120°\right) - \left(x\,v_{of}\sin\omega t + y\,v_{of}\sin\left(\omega t - 120°\right)\right)\right)\right] \tag{4.27}$$

$$v_c'' = n\left[m_a V_{dc}\sin\left(\omega t - 240°\right) - \left(x\,v_{of}\sin\omega t + y\,v_{of}\sin\left(\omega t - 120°\right)\right)\right] \tag{4.28}$$

Fig. 4.8(c), shows the balanced line-voltages from modified phase-voltages, with uniform voltage distribution among the operating units in all phases. Finally, injection of v_{oz} and extraction of fault tolerant modulating signals (v_a'', v_b'' and v_c'') for a generalized fault condition shown in Fig. 4.9, where x, y, and z units are number of faulty units in phase-a, b and c respectively. For x–y–z fault, the injected v_{oz} possess three components of v_{of} i.e., xv_{of}, yv_{of} and zv_{of} acting in phase-opposition to phase-a, b and c respectively. This results in injection of v_{oz} in to v_a', v_b' and v_c' as shown Fig. 4.9(b) and given in (4.29), where the resultant v_{oz} is given in (4.30).

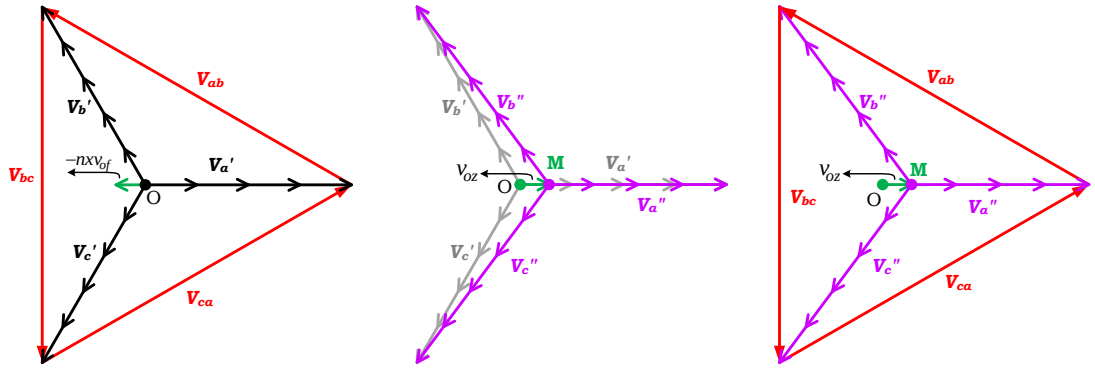
$$\left.\begin{aligned} v_a'' &= (n-x)\left[\frac{n}{n-x}m_a V_{dc}\sin\omega t\right] + v_{oz} \\ v_b'' &= (n-y)\left[\frac{n}{n-y}m_a V_{dc}\sin\left(\omega t - 120°\right)\right] + v_{oz} \\ v_c'' &= (n-z)\left[\frac{n}{n-z}m_a V_{dc}\sin\left(\omega t - 240°\right)\right] + v_{oz} \end{aligned}\right\} \tag{4.29}$$

$$v_{oz} = n\left[m_a V_{dc}\sin\left(\omega t - 240°\right) - \left(x\,v_{of}\sin\omega t + y\,v_{of}\sin\left(\omega t - 120°\right) + z\,v_{of}\sin\left(\omega t - 240°\right)\right)\right] \tag{4.30}$$

Addition of v_{oz} to (4.29), redistributes the fault burden among the operating units of all phases and shifts the neutral point of the inverter from O to M as shown in Fig. 4.9(b). Shifting of neutral modifies the magnitude and angle between phase-voltages and obtains new set of phase-voltages v_a'', v_b'' and v_c'' as given in (4.31) and shown in Fig. 4.9(c). Even though v_a'', v_b'' and v_c'' are unbalanced, nevertheless they produce balanced line-voltages with equal power sharing among the operating units of all phases.

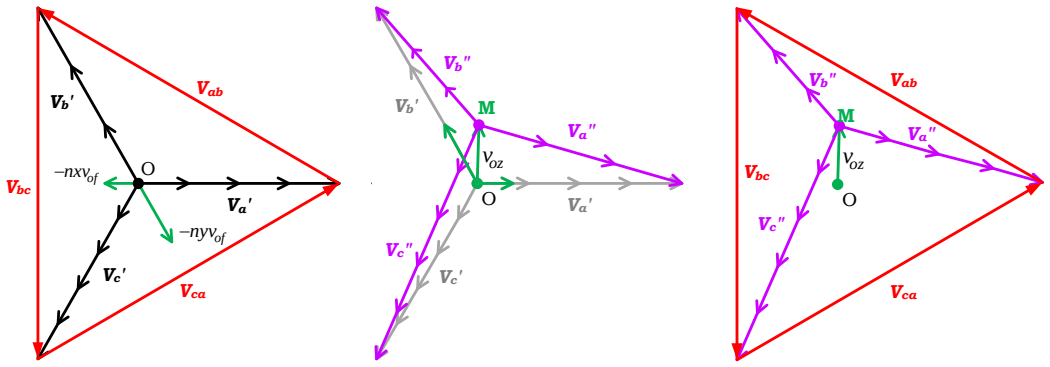
$$
\left.
\begin{aligned}
v_a'' &= (n-x)\left[\frac{n}{n-x}\left(m_a V_{dc}\sin\omega t - x v_{of}\sin\omega t - \right.\right.\right. \\
&\qquad \left.\left.\left. y\,v_{of}\sin(\omega t-120^\circ) - z\,v_{of}\sin(\omega t-240^\circ)\right)\right] \\
v_b'' &= (n-y)\left[\frac{n}{n-y}\left(m_a V_{dc}\sin(\omega t-120^\circ) - x v_{of}\sin\omega t - \right.\right.\right. \\
&\qquad \left.\left.\left. y\,v_{of}\sin(\omega t-120^\circ) - z\,v_{of}\sin(\omega t-240^\circ)\right)\right] \\
v_c'' &= (n-z)\left[\frac{n}{n-z}\left(m_a V_{dc}\sin(\omega t-240^\circ) - x v_{of}\sin\omega t - \right.\right.\right. \\
&\qquad \left.\left.\left. y\,v_{of}\sin(\omega t-120^\circ) - z\,v_{of}\sin(\omega t-240^\circ)\right)\right]
\end{aligned}
\right\} \qquad (4.31)
$$

Finally, extraction of generalized equation for fault tolerant modulating signals (v_a'', v_b'' and v_c'') to compensate simultaneous failure of multiple switches on all phases is given in (4.31).



(a) Injection of zero- sequence voltage (b) Shifting of neutral point (c) After fault compensation

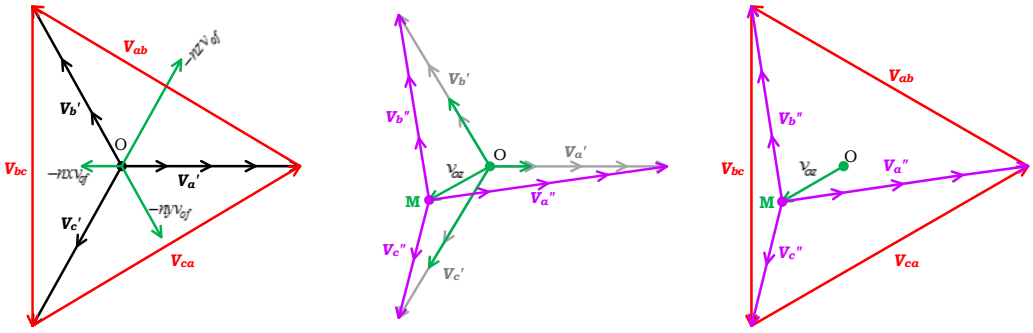
Fig. 4.7: Generalized NS zero-sequence injection FTS for *x* faulty units in phase-*a*.



(a) Injection of zero-sequence voltage (b) Shifting of neutral point (c) After fault compensation

Fig. 4.8: Generalized NS zero-sequence injection FTS for *x* faulty units in phase-*a*, and *y* faulty units in phase-*b*.

By observing (4.31), it can be concluded that the magnitude of v_{of} plays a key role in achieving FTO of the inverter. Therefore, the magnitude v_{of} should calculated such that it result balanced line-voltages and operate healthy units on all phases uniformly.



(a) Injection of zero-sequence voltage

(b) Shifting of neutral point

(c) After fault compensation

Fig. 4.9: Generalized NS zero-sequence injection FTS for *x* faulty units in phase-*a*, *y* faulty units in phase-*b* and, *z* faulty units in phase-*c*.

4.4.2 Determination of zero-sequence voltage

To ensure equal power distribution across all the operating units, the individual powers of each healthy basic unit in phase-*a*, *b* and *c* should be same. To determine the power delivered by each healthy unit, the voltage across and current through each healthy unit are required. After fault compensation, it is expected that the line-currents become balanced (4.32), and the voltage across each healthy unit is given in (4.33). Therefore, the power delivered by each healthy basic unit in phase-*a*, *b* and *c* are calculated over one fundamental time period given in (4.34), (4.39) and (4.41), results (4.38), (4.40) and (4.42). By equating these powers shown in (4.38), (4.40) and (4.42), magnitude of v_{of} for any fault condition is obtained and is given in (4.47).

Considering the line-currents are balanced after fault compensation,

$$\left.\begin{aligned} i_a(t) &= I\sqrt{2}\sin\omega t \\ i_b(t) &= I\sqrt{2}\sin(\omega t - 120^\circ) \\ i_c(t) &= I\sqrt{2}\sin(\omega t - 240^\circ) \end{aligned}\right\} \tag{4.32}$$

From (4.31) after the injection of v_{oz}, the voltage produced by any healthy unit can be expressed as

$$\left.\begin{aligned} v_{ak}'' &= \left[\frac{n}{n-x}\left(m_a V_{dc}\sin\omega t - x v_{of}\sin\omega t - y\,v_{of}\sin(\omega t - 120^\circ) - z\,v_{of}\sin(\omega t - 240^\circ)\right)\right] \\ v_{bk}'' &= \left[\frac{n}{n-y}\left(m_a V_{dc}\sin(\omega t - 120^\circ) - x v_{of}\sin\omega t - y\,v_{of}\sin(\omega t - 120^\circ) - z\,v_{of}\sin(\omega t - 240^\circ)\right)\right] \\ v_{ck}'' &= \left[\frac{n}{n-z}\left(m_a V_{dc}\sin(\omega t - 240^\circ) - x v_{of}\sin\omega t - y\,v_{of}\sin(\omega t - 120^\circ) - z\,v_{of}\sin(\omega t - 240^\circ)\right)\right] \end{aligned}\right\} \tag{4.33}$$

Where, $k = 1, 2, \ldots (n-x)$ for phase-*a*; $k = 1, 2, \ldots (n-y)$ for phase-*b*; $k = 1, 2, \ldots (n-z)$ for phase-*c*.

The output electric power of each healthy basic unit in phase-*a* is given by

$$p_{ak} = \frac{1}{T}\int_{0}^{2\pi/\omega} v''_{ak}(t)\, i_a(t)\, dt \tag{4.34}$$

$$p_{ak} = \frac{1}{T}\left(\frac{n}{n-x}\right)\left(\int_{0}^{2\pi/\omega}\begin{pmatrix} m_a V_{dc}\sin\omega t - x\, v_{of}\sin\omega t \\ - y\, v_{of}\sin(\omega t - 120^\circ) \\ - z\, v_{of}\sin(\omega t - 240^\circ)\end{pmatrix}\sqrt{2}\, I\sin\omega t\, dt\right) \tag{4.35}$$

$$p_{ak} = \frac{1}{T}\left(\frac{n\, I\sqrt{2}}{n-x}\right)\left(\int_{0}^{2\pi/\omega}\begin{pmatrix}(m_a V_{dc} - x\, v_{of})\sin^2\omega t \\ - y\, v_{of}\sin(\omega t - 120^\circ)\sin\omega t \\ - z\, v_{of}\sin(\omega t - 240^\circ)\sin\omega t\end{pmatrix} dt\right) \tag{4.36}$$

$$p_{ak} = \frac{1}{T}\left(\frac{n\, I\sqrt{2}}{n-x}\right)\left(\frac{\pi}{\omega}\right)\left(V_{dc}\, m_a - x\, v_{of} + \frac{y\, v_{of}}{2} + \frac{z\, v_{of}}{2}\right) \tag{4.37}$$

$$p_{ak} = \left(\frac{n}{n-x}\right) I\,\frac{1}{\omega\sqrt{2}}\left[V_{dc}\, m_a - x\, v_{of} + \frac{y\, v_{of}}{2} + \frac{z\, v_{of}}{2}\right] \text{ for } k = 1, 2, 3, \ldots\ldots\ldots (n-x) \tag{4.38}$$

Similarly, the output electric power of each healthy basic unit in phase-*b* and *c* are given by

$$p_{bk} = \frac{1}{T}\int_{0}^{2\pi/\omega} v''_{bk}(t)\, i_b(t)\, dt \tag{4.39}$$

$$p_{bk} = \frac{n}{n-y}\, I\,\frac{1}{\omega\sqrt{2}}\left[V_{dc}\, m_a - y\, v_{of} + \frac{x\, v_{of}}{2} + \frac{z\, v_{of}}{2}\right] \text{for } k = 1, 2, 3, \ldots\ldots\ldots (n-y) \tag{4.40}$$

$$p_{ck} = \frac{1}{T}\int_{0}^{2\pi/\omega} v''_{ck}(t)\, i_c(t)\, dt \tag{4.41}$$

$$p_{ck} = \frac{n}{n-z}\, I\,\frac{1}{\omega\sqrt{2}}\left[V_{dc}\, m_a - z\, v_{of} + \frac{y\, v_{of}}{2} + \frac{x\, v_{of}}{2}\right] \text{ for } k = 1, 2, 3, \ldots\ldots\ldots (n-z) \tag{4.42}$$

To ensure uniform burden among all healthy basic units, v_{of} is selected such a way that these powers ($p_{ak,}\, p_{bk}$ and p_{ck}) are equal. To ensure that (4.43) is considered.

$$p_{ak} + p_{bk} = 2\, p_{ck} \text{ and } p_{ak} - p_{bk} = 0 \tag{4.43}$$

To determine v_{of}, (4.43) is considered. Substituting (4.38), (4.40) and (4.42), in (4.43), v_{of} is obtained as (4.47).

$$\left[\begin{array}{l}\dfrac{1}{n-x}\left[m_a V_{dc}-x\,v_{of}+\dfrac{y\,v_{of}}{2}+\dfrac{z\;v_{of}}{2}\right]\\ +\;\dfrac{1}{n-y}\left[m_a V_{dc}-y\,v_{of}+\dfrac{x\,v_{of}}{2}+\dfrac{z v_{of}}{2}\right]\end{array}\right]=\frac{2}{n-z}\left[m_a V_{dc}-z\,v_{of}+\frac{y\,v_{of}}{2}+\frac{x v_{of}}{2}\right] \tag{4.44}$$

$$v_{of}=\frac{m_a\;V_{dc}\left[\dfrac{1}{n-x}+\dfrac{1}{n-y}-\dfrac{2}{n-z}\right]}{\left[(x+y-2z)\dfrac{1}{n-z}\right]+\left[\left(x-\dfrac{y}{2}-\dfrac{z}{2}\right)\dfrac{1}{n-x}\right]+\left[\left(y-\dfrac{x}{2}-\dfrac{z}{2}\right)\dfrac{1}{n-y}\right]} \tag{4.45}$$

$$v_{of}=\frac{\left[(x+y-2z)n-(2xy-yz-zx)\right]2m_a\;V_{dc}}{\left[(x+y-2z)n-(2xy-yz-zx)\right](3n-x-y-z)} \tag{4.46}$$

$$v_{of}=\frac{2m_a\;V_{dc}}{3n-(x+y+z)} \tag{4.47}$$

Therefore, the generalized formulae for determining the magnitude of v_{of}, for x faults in phase-a, y faults in phase-b and z faults in phase-c is given in (4.47).

4.4.3 Extraction of fault tolerant modulating signals

To extract the generalized equations of fault tolerant modulating signals given in (4.48), the magnitude of v_{of} given in (4.47), to be substituted in (4.31).

$$\begin{aligned}
v_a'' &= (n-x)\left[\frac{\sqrt{3}nm_aV_{dc}\sqrt{3(n-x)^2+(y-z)^2}}{(n-x)(3n-x-y-z)}\right.\\
&\qquad\left.\sin\left(\omega t+\sin^{-1}\left(\frac{(y-z)}{\sqrt{3(n-x)^2+(y-z)^2}}\right)\right)\right]\\
v_b'' &= (n-y)\left[\frac{nm_aV_{dc}\sqrt{9(-n-x+y+z)^2+3(-3n+x+3y-z)^2}}{2(n-y)(3n-x-y-z)}\right.\\
&\qquad\left.\sin\left(\omega t-\pi-\sin^{-1}\left(\frac{\sqrt{3}(-3n+x+3y-z)}{\sqrt{9(-n-x+y+z)^2+3(-3n+x+3y-z)^2}}\right)\right)\right]\\
v_c'' &= (n-z)\left[\frac{nm_aV_{dc}\sqrt{9(-n-x+y+z)^2+3(3n-x+y-3z)^2}}{2(n-z)(3n-x-y-z)}\right.\\
&\qquad\left.\sin\left(\omega t+\pi-\sin^{-1}\left(\frac{\sqrt{3}(3n-x+y-3z)}{\sqrt{9(-n-x+y+z)^2+3(3n-x+y-3z)^2}}\right)\right)\right]
\end{aligned} \tag{4.48}$$

The modulating signals given in (4.48) represents the fault tolerant modulating signals in terms of x, y, z, n, m_a and V_{dc}. From (4.48), it can be observed that, during FTO the pre-fault m_a is multiplied by a scaling factor (different in each phase) as given in (4.49). This increases m_a of the modified modulating signals to m_a* and, may drive the inverter into overmodulation in one or more phases. This results in reduced RMS values of line-voltages (as compared to pre-fault) and produce lower order harmonics. Therefore, to avoid overmodulation, if the inverter application permits, the modulation index (m_a*) can be suitability adjusted as given in (4.50).

$$\left.\begin{aligned} m_a^{*}{}_{(a-ph)} &= \frac{\sqrt{3}n\sqrt{3\left(n-x\right)^2+\left(y-z\right)^2}}{\left(n-x\right)\left(3n-x-y-z\right)}m_a \\ m_a^{*}{}_{(b-ph)} &= \frac{n\sqrt{9\left(-n-x+y+z\right)^2+3\left(-3n+x+3y-z\right)^2}}{2\left(n-y\right)\left(3n-x-y-z\right)}m_a \\ m_a^{*}{}_{(c-ph)} &= \frac{n\sqrt{9\left(-n-x+y+z\right)^2+3\left(3n-x+y-3z\right)^2}}{2\left(n-z\right)\left(3n-x-y-z\right)}m_a \end{aligned}\right\} \quad (4.49)$$

$$m_a^{*} = \min\left(m_a^{*}{}_{(a-ph)} \le 1,\ m_a^{*}{}_{(b-ph)} \le 1,\ m_a^{*}{}_{(c-ph)} \le 1\right) \quad (4.50)$$

4.4.4 Limitations of the proposed FTS scheme

- Applicable only to modular redundant topologies such as CHB and MLDCL, where the effect of OC faults on phase-voltages does not create non-uniform $\mathrm{d}v/\mathrm{d}t$.
- With increase in number of faulty units, the modulation index of the corresponding phase modulating signal is high. If the pre-fault m_a is high, and the faulty units on a phase is more than 33%, then it drives the corresponding phase-voltage to near square wave operation and the fault compensation will not be effective. Under such conditions, for an effective FTO, the pre-fault m_a should be reduced to bring the post-fault m_a* to linear modulation range.

4.5 Performance evaluation on 15-level MLDCL inverter

In order to demonstrate the proposed FTS, A 3.3 kV, 200 kVA, 50 Hz 15-level MLDCL is considered with seven basic units in each phase and each unit is fed from an isolated 385 V dc supply. To obtain uniform power sharing among all basic units, a carrier rotation based reduced carrier PWM technique with 2.5 kHz carrier frequency (f_{cr}) is used to control this MLDCL configuration [109].

Implementation of PWM: The obtained modulating signals are operated with carrier ration PWM involving proposed reduced carrier arrangement. During the healthy operating condition, to operate the 15-level inverter, seven unipolar carriers are required and these carriers are rotated at the end of each carrier cycle [109]. Arrangement and rotation of carriers for healthy operating

conditions is shown in Fig. 4.10, considering phase-*a* as an example (m_a = 0.9). The objective behind carrier rotation is to operate each switch in level generator of MLDCL with equal conduction period, which contributes to uniform power distribution among the operating units.

The switching pulse obtained by comparing a carrier and reference signal is responsible for obtaining positive levels in output voltage during positive half-cycle of the modulating signal and negative levels in output voltage for negative half-cycle of the modulating signal. This pulse is given to S_k device of each operating unit and its respective complimentary pulse is given to S'_k, where $k = 1, 2, 3\ldots. (n–1)/2$. It should be noted that, during fault compensation, the switching pulses to the faulty unit are seized and the carriers are rotated across the remaining units of the phase. Modulating signals to compensate the appeared fault are extracted from (4.48). Assuming a single unit fault on phase-*a* of the considered 15-level MLDCL inverter, rotation of carriers in faulty and, healthy phases during fault compensation is shown in Fig. 4.11 and Fig. 4.12.

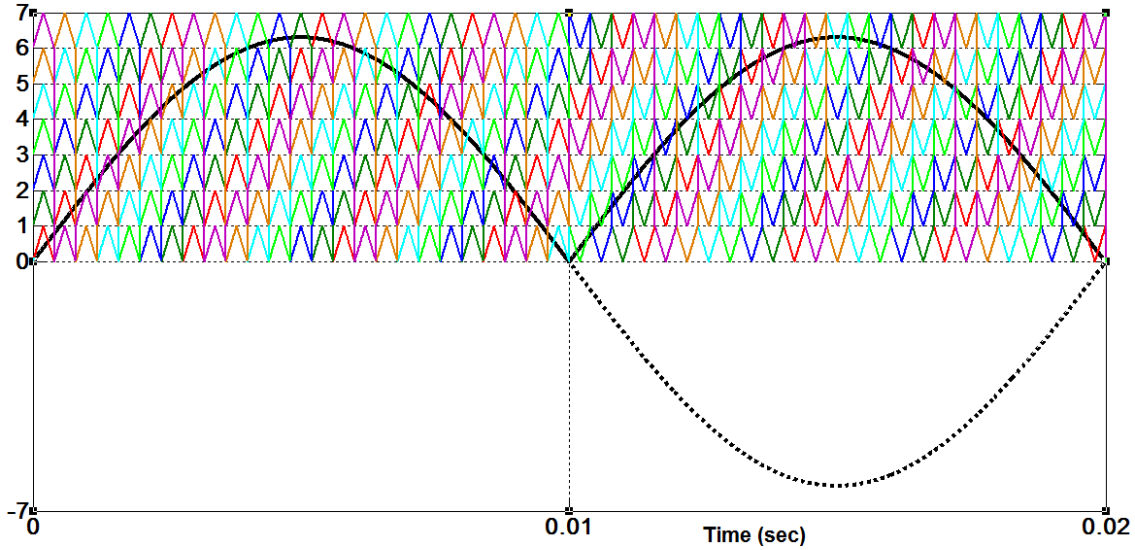


Fig. 4.10: Rotation of carriers in phase-*a* of 15-level MLDCL under healthy operating condition.

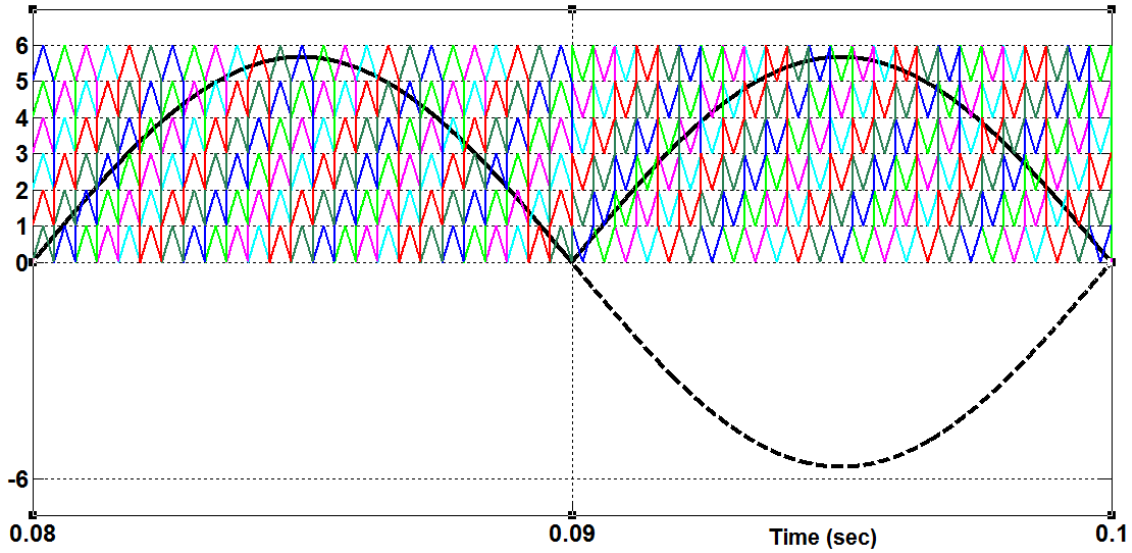


Fig. 4.11: Rotation of carriers in phase-*a* of 15-level MLDCL under compensation of 1–0–0 fault.

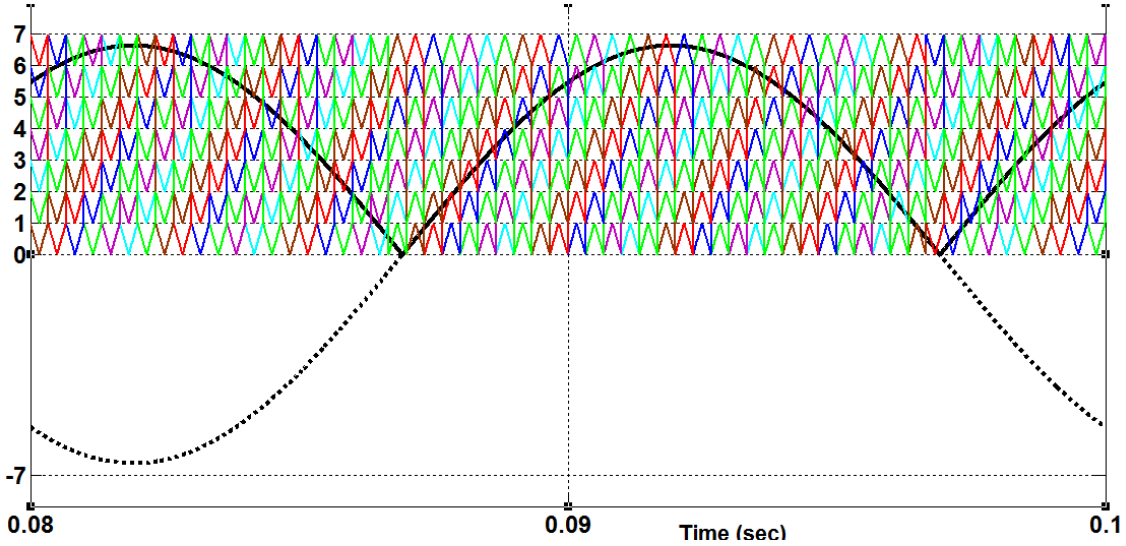


Fig. 4.12: Rotation of carriers in phase-*b* of 15-level MLDCL under compensation of 1–0–0 fault.

As one unit is faulty in phase-*a*, carriers are to be rotated among the remaining (six) healthy operating units of phase-*a*, thus six carriers are considered as shown in Fig. 4.11. As there are no faulty units in phase-*b* and *c*, all seven carriers are considered and rotated among the healthy units of respective phase as shown in Fig. 4.12 (shown for phase-*b* as an example).

To observe the efficacy of the proposed method the following simulation studies are performed in MATLAB/Simulink environment.

***Case*-1:** *One unit failure*: $x = 1$, $y = 0$ and $z = 0$

***Case*-2:** *Two unit failure*: $x = 1$, $y = 0$ and $z = 1$

***Case*-3:** *Three unit failure*: $x = 3$, $y = 0$ and $z = 0$

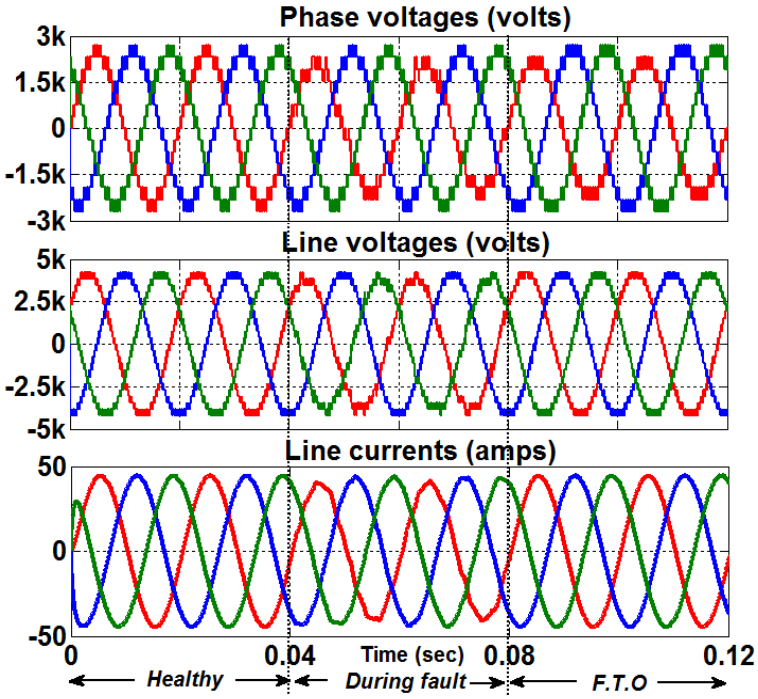
***Case*-4:** *Four unit failure*: $x = 3$, $y = 0$ and $z = 1$

***Case*-5:** *Six unit failure*: $x = 2$, $y = 3$ and $z = 1$

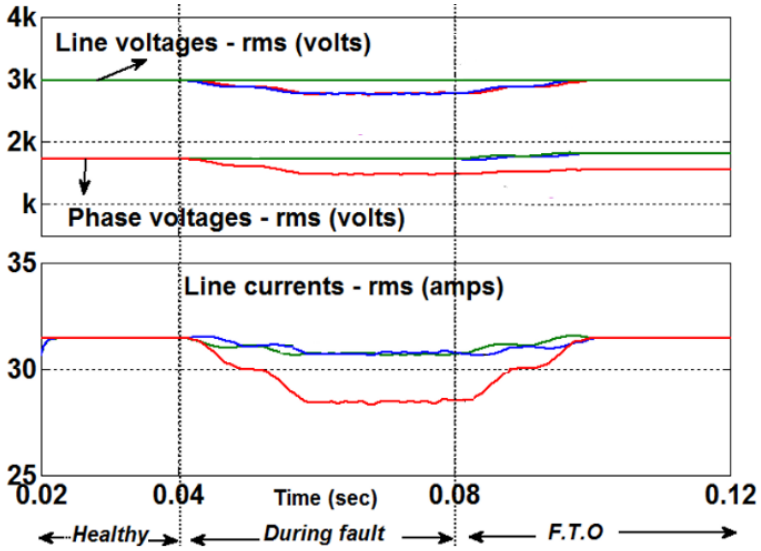
In simulation study, it is assumed that for first two cycles, the inverter is healthy. At 0.04 s, fault is assumed to be occurred and the effect of fault is studied for subsequent two cycles. At 0.08 s FTS is enabled. Results are recorded for $f_{cr} = 2.5$ kHz and $m_f = 50$ Hz.

4.5.1 *Case*-1: OC fault on one unit ($x = 1$, $y = 0$ and $z = 0$)

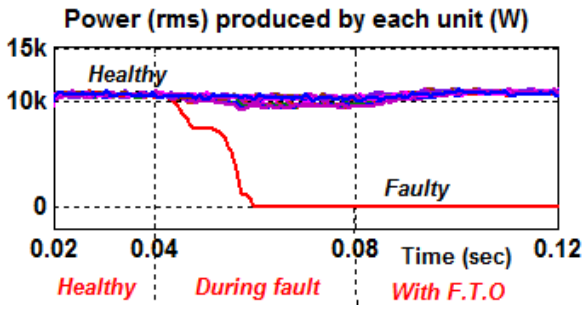
The pre and post-fault performance of 15-level MLDCL RSC-MLI for one faulty unit in phase-*a* is shown in Fig. 4.13 for $m_a = 0.9$, where the waveforms of phase-voltage, line-voltage and line-currents are shown in Fig. 4.13(a) and their corresponding RMS values are shown in Fig. 4.13(b). Fig. 4.13(c) shows the power delivered by each unit in healthy, faulty, and fault tolerant operating modes. The harmonic performance of considered 15-level MLDCL RSC-MLI in healthy operating condition is shown in Fig. 4.14, where the THD of phase-voltage, line-voltage and line-current are shown in Fig. 4.14(a), (b) and (c) respectively.



(a) Wave forms of inverter voltages and currents

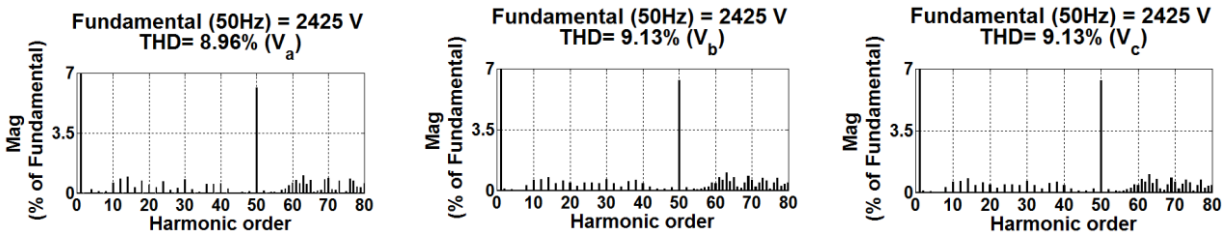


(b) RMS values of inverter voltages and currents

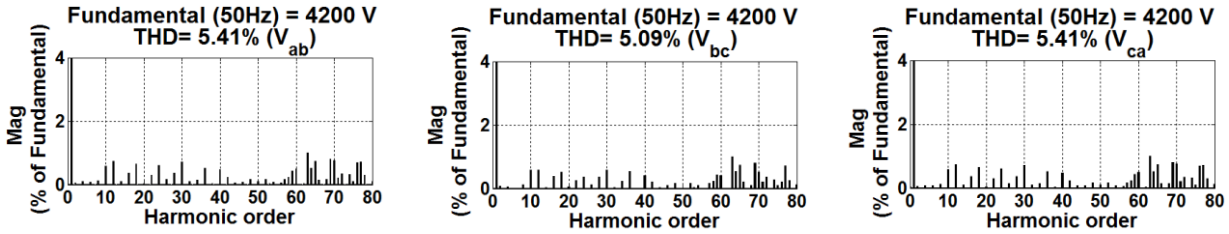


(c) Power delivered by each operating unit

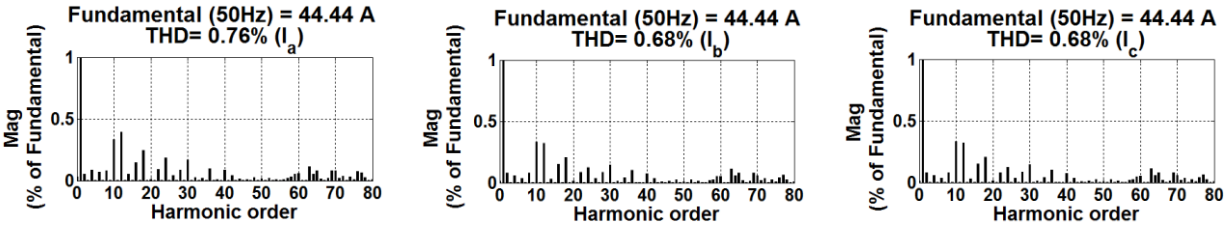
Fig. 4.13: Pre and post-fault performance of 15-level MLDCL for 1–0–0 fault with m_a= 0.9.



(a) Phase-voltages



(b) Line-voltages



(c) Line-currents

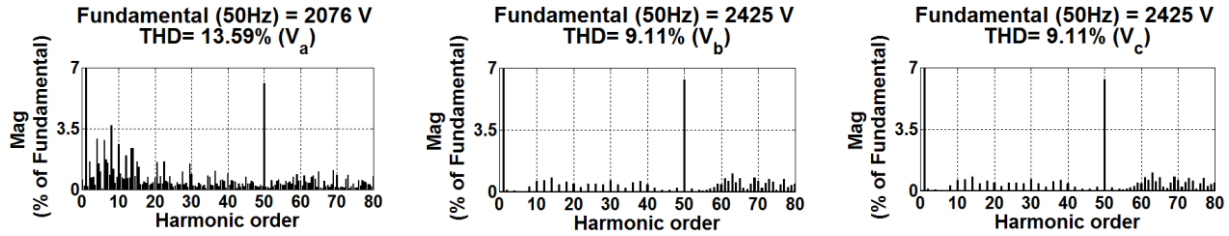
Fig. 4.14: Harmonic performance of 15-level MLDCL inverter in healthy condition for m_a= 0.9.

Fig. 4.13 and Fig. 4.14 verifies the balanced operation of the considered inverter in healthy condition, where the RMS and corresponding THD values of phase-voltage, line-voltage and line-currents are 1722 V (~9.0%), 2974 V (~5.4%) and 31.42 A (~0.7%) respectively. Fig. 4.13(c) shows the uniform power distribution across all the operating units, where each unit is contributing a power of 11.5 kW.

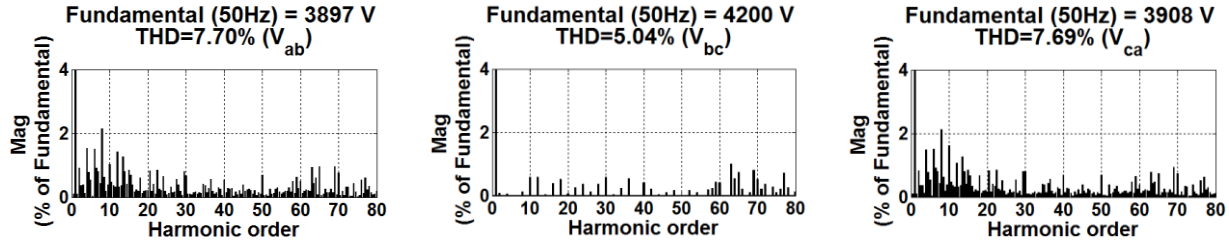
At 0.04 s, an OC fault in one basic unit of phase-*a*, is occurred and this results in unbalanced phase-voltage, line-voltage and line-current as shown in Fig. 4.13(a). The unbalance in their RMS values can also be observed in Fig. 4.13(b). The RMS values of unbalanced phase-voltages are 1477, 1722 and 1722 V, line-voltages are 2760, 2974 and 2768 V and line-currents are 28.4, 30.6 and 30.7 A. After 0.04 s in Fig. 4.13(c), it can be observed that power contributed by the faulty unit tends to zero and leads to unbalance among the remaining units. The effect of fault on harmonic performance of inverter is shown in Fig. 4.15, where the non-uniform harmonic distortion in phase-voltage (5.41%, 9.13% and 9.13%), line-voltage (5.41%, 9.13% and 9.13%) and line-currents (5.41%, 9.13% and 9.13%) are shown in Fig. 4.15(a), (b) and c respectively. Therefore, to tolerate the fault and achieve balanced operation of the inverter, at 0.08 s the proposed generalized NS zero-sequence injection FTS is enabled.

Therefore, a new set of modulating signals given in (4.51) are derived by substituting the values of $x = 1$, $y = 0$, $z = 0$, and $n = 7$ in (4.48).

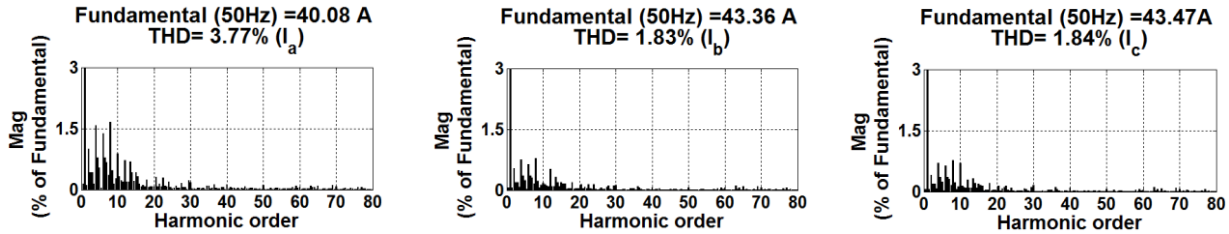
$$\left.\begin{aligned} v_a'' &= 6*1.05*m_a \sin(\omega t) \\ v_b'' &= 7*1.04*m_a \sin(\omega t - 124.1°) \\ v_c'' &= 7*1.04*m_a \sin(\omega t + 124.1°) \end{aligned}\right\} \quad (4.51)$$



(a) Phase-voltages



(b) Line-voltages



(c) Line-currents

Fig. 4.15: Harmonic performance of 15-level MLDCL inverter during 1–0–0 fault for m_a= 0.9.

From (4.51), it can be observed that post-fault amplitude modulation index (m_a*) of phase-*a*, *b* and *c* is 1.05, 1.04 and 1.04 times pre-fault m_a. Further substituting m_a = 0.9 in (4.51) produce required modulating signals given in (4.52). During fault compensation, with m_a = 0.9, the inverter operating in linear modulating range (0.945, 0.936 and 0.936).

$$\begin{aligned} v_a'' &= 6*0.945 \sin \omega t \\ v_b'' &= 7*0.936 \sin(\omega t - 124.1°) \\ v_c'' &= 7*0.936 \sin(\omega t + 124.1°) \end{aligned} \quad (4.52)$$

The fault compensation and balanced operation of inverter can be observed after 0.08s in Fig. 4.13(a), (b) and (c). After fault compensation, the unbalanced phase-voltages (with RMS values of 1552, 1814 and 1814 V) produced a balanced set of line-voltage and currents with RMS values of 2974 V and 31.4 A respectively as shown in Fig. 4.13(a) and (b). The power produced by each operating unit after fault compensation shown in Fig. 4.13(c) is at 12 kW, against 10.5 kW in pre-fault case. Further, the effectiveness of fault compensation can be observed from the harmonic

performance of inverter shown in Fig. 4.16. The unbalanced phase-voltages (10.51%, 8.97% and 8.97%) shown in Fig. 4.16(a) produces balanced line-voltages and line-currents with THD of ~5.35% and ~0.7% respectively as shown in Fig. 4.16(b) and (c).

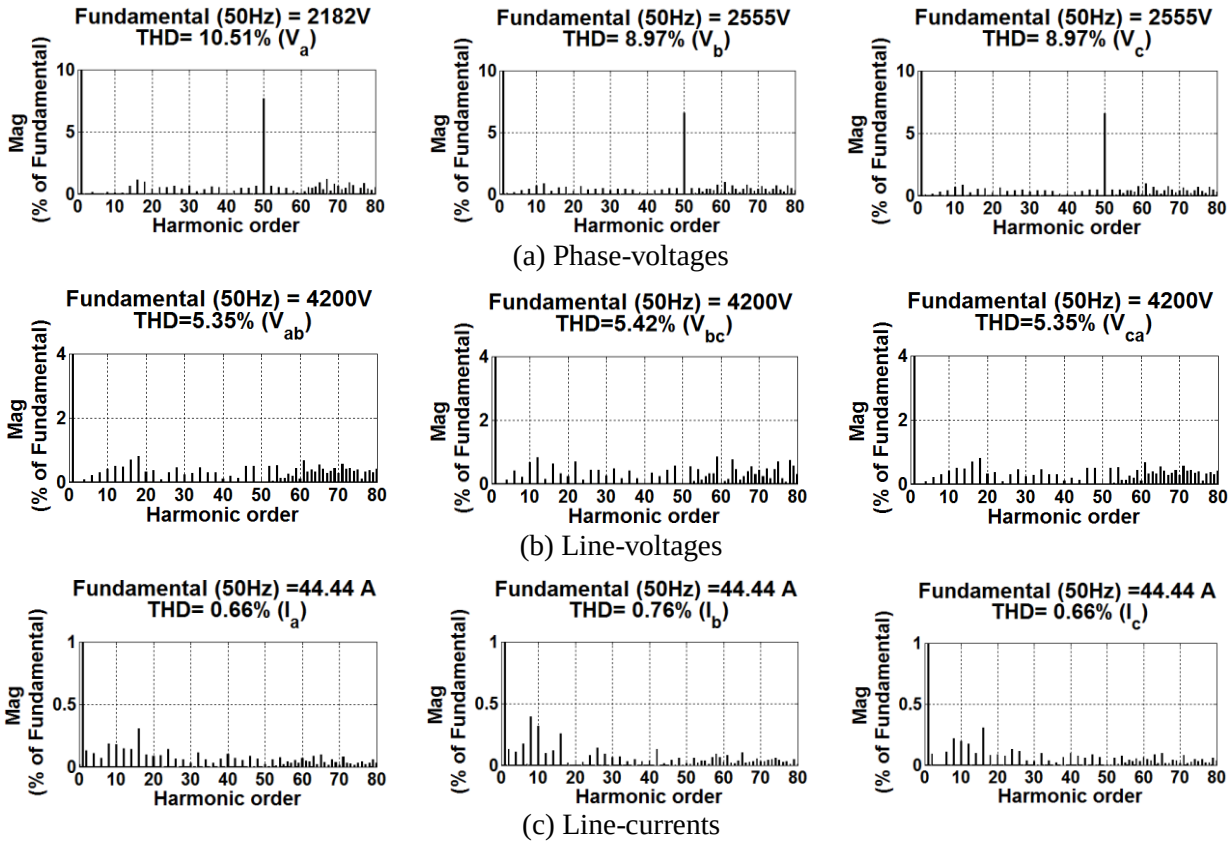
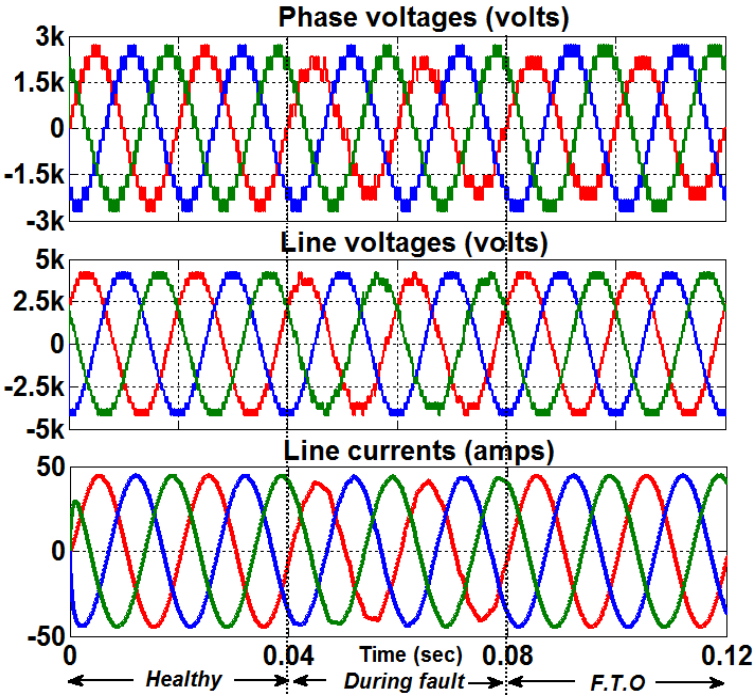


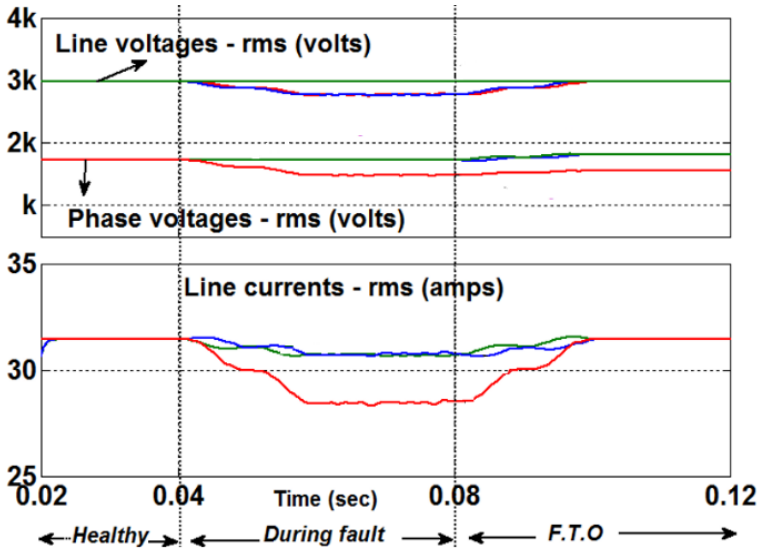
Fig. 4.16: Harmonic performance of 15-level MLDCL inverter after compensation of 1–0–0 fault with proposed FTS for m_a= 0.9.

4.5.2 *Case*-2: OC fault on two units (x = 1, y = 0 and z = 1)

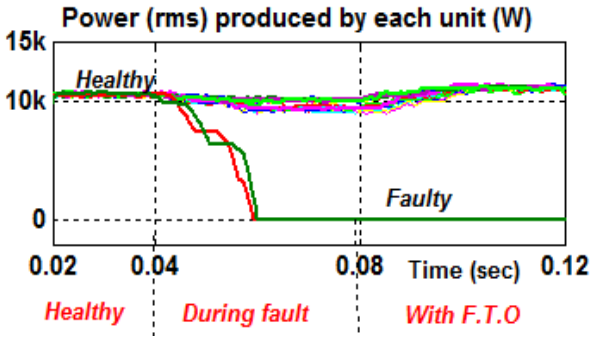
The pre and post-fault performance of 15-level MLDCL RSC-MLI with two faulty units (one unit in phase-*a*, and other in phase-*c*) at m_a = 0.9 is shown in Fig. 4.17. The obtained simulation waveforms and their corresponding RMS values of phase-voltage, line-voltage and line-currents are shown in Fig. 4.17(a) and (b) respectively. Further, Fig. 4.17(c) shows the power delivered by each unit during all operating modes. Fig. 4.17(a), (b) and (c) shows the balanced operation of inverter in healthy condition, where each unit is contributing a power of 11.5 kW. With the initiation of fault at t = 0.04 s, the power contributed by the faulty units tends to zero, which distorts the inverter voltages, currents and power delivered by each operating unit. The unbalance in phase-voltages (1470, 1722 and 1470 V), line-voltages (2765, 2765 and 2780 V) and line-currents (28.4, 30.6 and 30.4 A) can be further verified by referring to their respective RMS values shown in Fig. 4.17(b). Therefore, to tolerate the fault and restore the inverter balanced operation, at t = 0.08 s, the proposed FTS is enabled. The fault tolerant modulating signals given in (4.53) are obtained by substituting the values of x, y, z, and n in (4.48).



(a) Phase-voltage, line-voltage and line-current waveforms



(b) Phase-voltage, line-voltage and line-current RMS values



(c) Power delivered by each operating unit

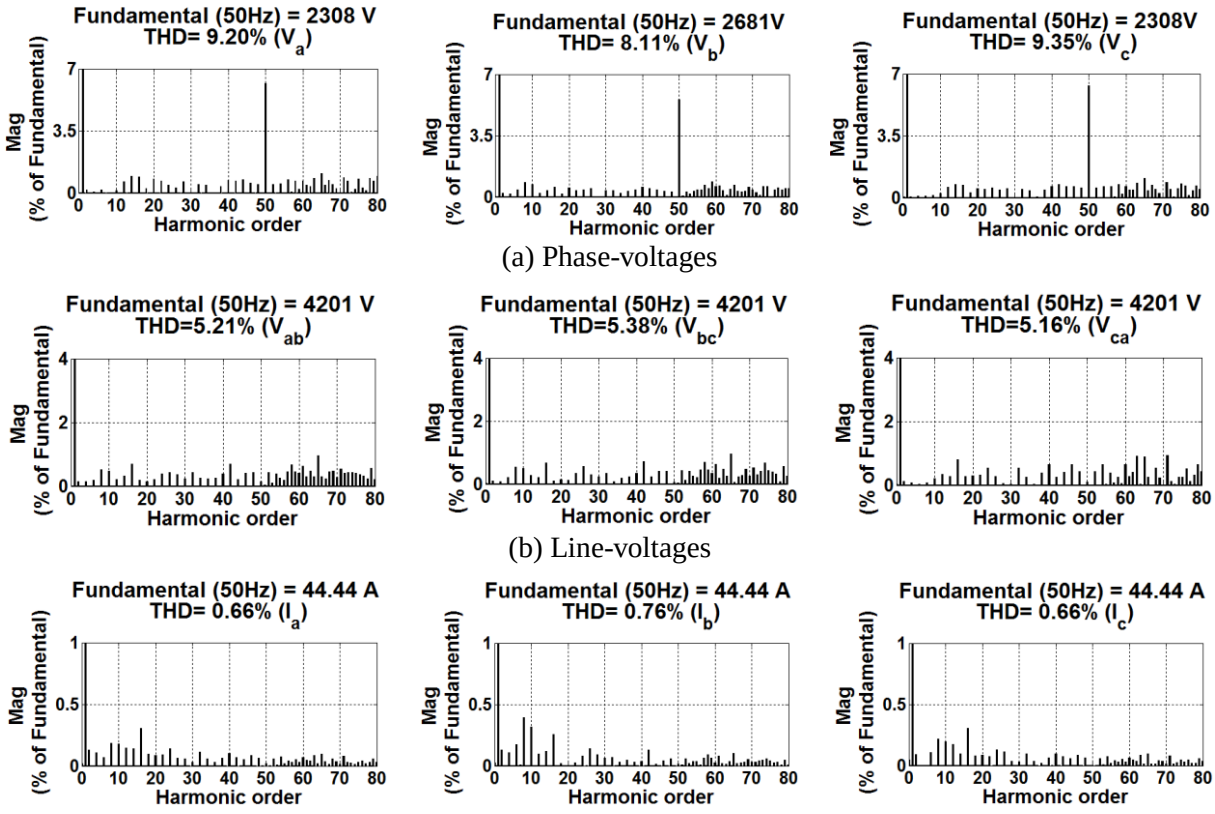
Fig. 4.17: Pre and post-fault performance of 15-level MLDCL for 1–0–1 fault with $m_a = 0.9$.

$$
\begin{aligned}
v_a'' &= 6*1.11*m_a \sin\left(\omega t - 5.49°\right) \\
v_b'' &= 7*1.10*m_a \sin\left(\omega t - 120°\right) \\
v_c'' &= 6*1.11*m_a \sin\left(\omega t + 125.49°\right)
\end{aligned} \tag{4.53}
$$

From (4.53), it can be observed that post-fault amplitude modulation index of phase-*a*, *b* and *c* are 1.11, 1.10 and 1.11 times pre-fault m_a, respectively. Further, substituting m_a = 0.9 in (4.53), results the final modulating signals given in (4.54).

$$
\left.
\begin{aligned}
v_a'' &= 6*0.99 \sin\left(\omega t - 5.49°\right) \\
v_b'' &= 7*0.99 \sin\left(\omega t - 120°\right) \\
v_c'' &= 6*0.99 \sin\left(\omega t + 125.49°\right)
\end{aligned}
\right\} \tag{4.54}
$$

FTO of the inverter with (4.54) is shown in Fig. 4.17, where the balanced operation of inverter after fault compensation can be observed. After fault compensation, the unbalanced phase-voltages (with RMS values of 1639, 1902 and 1639 V) produced a balanced set of line-voltage and currents with RMS values of 2974 V and 31.4 A respectively as shown in Fig. 4.17(a) and (b). Further, the power contributed by each operating unit is 12.7 kW as shown in Fig. 4.17(c). The harmonic performance of the obtained compensated phase-voltages (9.2%, 8.11% and 9.35%), line-voltages (~5.2%) and line-currents (~0.7%) are shown in Fig. 4.18(a), (b) and (c) respectively.



(a) Phase-voltages

(b) Line-voltages

(c) Line-currents

Fig. 4.18: Harmonic performance of 15-level MLDCL inverter after compensation of 1–0–1 fault with proposed FTS for m_a = 0.9

Fig. 4.17 and Fig. 4.18 verify that the proposed scheme produces balanced line-voltages from unbalanced phase-voltages such that the performance of post-fault line-voltage is equal to pre-fault.

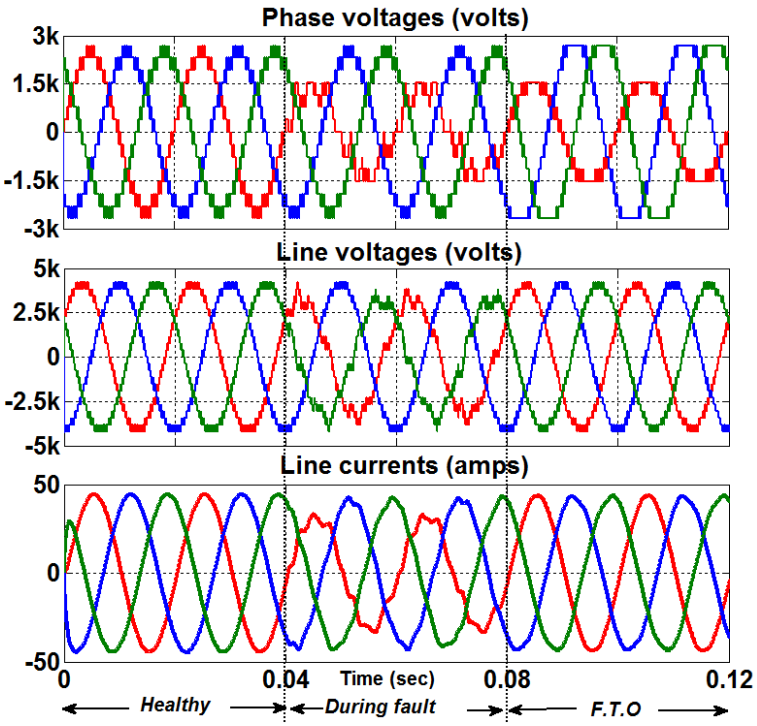
4.5.3 *Case*-3: OC fault on three units ($x = 3$, $y = 0$ and $z = 0$)

Pre-fault and post-fault performance of 15-level MLDCL inverter with three faulty units on phase-*a* for m_a= 0.9 is shown in Fig. 4.19, where the waveforms of output voltages and currents are shown in Fig. 4.19(a) and its corresponding RMS values are depicted in Fig. 4.19(b). The power delivered by each unit is given in Fig. 4.19(c). Further, Fig. 4.19 shows the balanced operation of the inverter with uniform power distribution, for the healthy operating conditions. Fig. 4.19(a) and (b) shows that, appearance of fault at t = 0.04 s, creates unbalance in phase-voltages (1025, 1722 and 1722 V), line-voltages (2374, 2974 and 2395 V) and line-currents (22.56, 29.35 and 29.57 A). Also, Fig. 4.19(c) shows the non-uniform power distribution among the operating units due to the three faulty units. Thus to reconfigure the inverter, at t = 0.08 s, the proposed generalized NS-FTS is enabled. The desired modulating signals given in (4.55) are obtained by substituting the values of x = 3, y = 0, z = 0 and n = 7 in the generalized modulating signals given in (4.48). Further, substituting m_a = 0.9 in (4.55), produces final fault tolerant modulating signals given in (4.56).

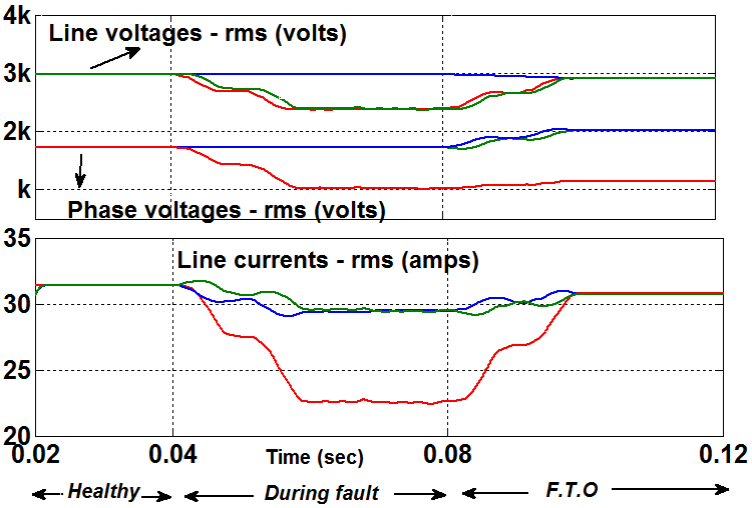
$$\left.\begin{aligned} v_a'' &= 4*1.23*m_a \sin(\omega t) \\ v_b'' &= 6*1.20*m_a \sin(\omega t - 133°) \\ v_c'' &= 6*1.20*m_a \sin(\omega t + 133°) \end{aligned}\right\} \quad (4.55)$$

$$\left.\begin{aligned} v_a'' &= 4*1.10 \sin(\omega t) \\ v_b'' &= 6*1.08 \sin(\omega t - 133°) \\ v_c'' &= 6*1.08 \sin(\omega t + 133°) \end{aligned}\right\} \quad (4.56)$$

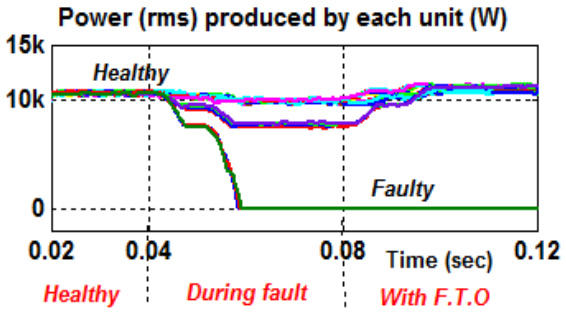
After fault compensation, the unbalanced phase-voltages (with RMS values of 1138, 2016 and 2016 V) produced a balanced set of line-voltage and currents with RMS values of 2910 V and 30.7 A respectively. However, it can be noted that the waveform shape of line-voltages and line-currents appears to be deviated from pre-fault condition. This can be further verified from their respective harmonic spectra shown in Fig. 4.20. Fig. 4.20 shows the presence of lower order harmonics and dissimilar harmonic spectra of line-voltage (5.8%, 6.1% and 5.8%) and current (1.37%, 2.49% and 2.49%). This is due to the non-linear modulation range of the inverter in fault tolerant mode. Even though the inverter is desired to operate in undermodulation (m_a = 0.9), the modulating signals in the FTO are driven to overmodulation (m_a* = 1.10, 1.08 and 1.08) to compensate the fault burden as given in (4.56). This overmodulation in phase-voltages during FTO can be observed from Fig. 4.19. Thus, high-value of pre-fault m_a with increased number of faulted units, the burden on healthy units further increases and drives inverter to high overmodulation.



(a) Phase-voltage, line-voltage and line-current waveforms

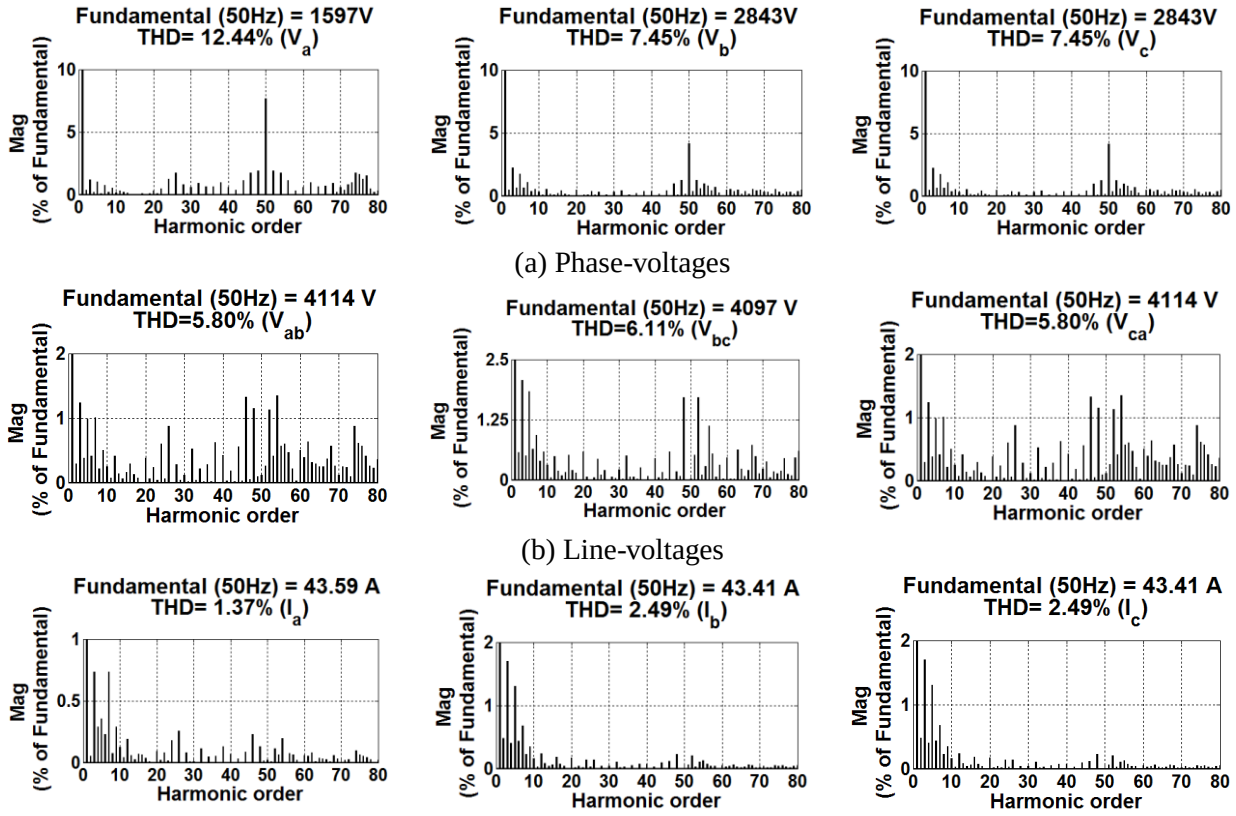


(b) Phase-voltage, line-voltage and line-current RMS values



(c) Power delivered by each operating unit

Fig. 4.19: Pre and post-fault performance of 15-level MLDCL for 3–0–0 fault with m_a = 0.9.



(a) Phase-voltages

(b) Line-voltages

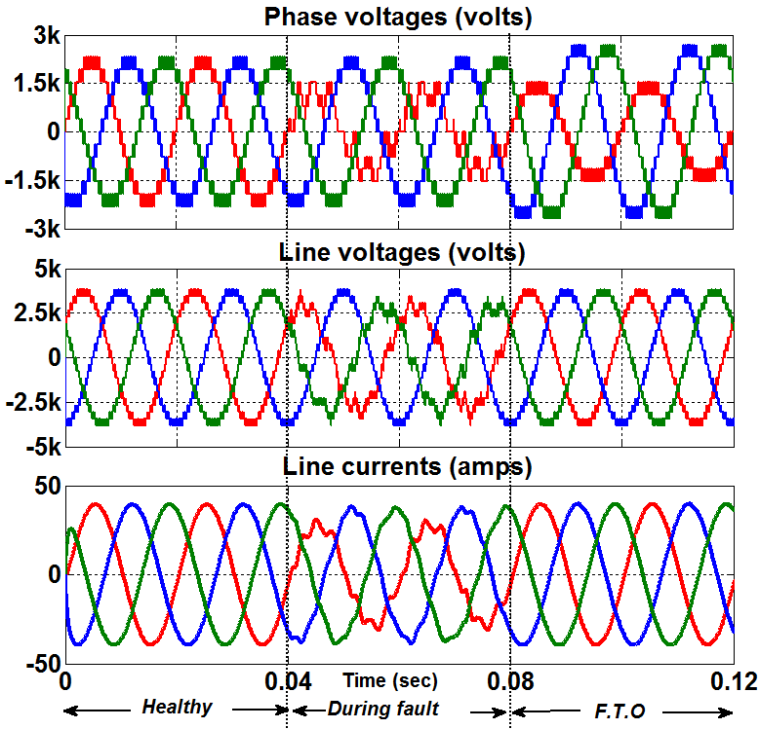
(c) Line-currents

Fig. 4.20: Harmonic performance of 15-level MLDCL inverter after compensation of 3–0–0 fault with proposed FTS for m_a= 0.9

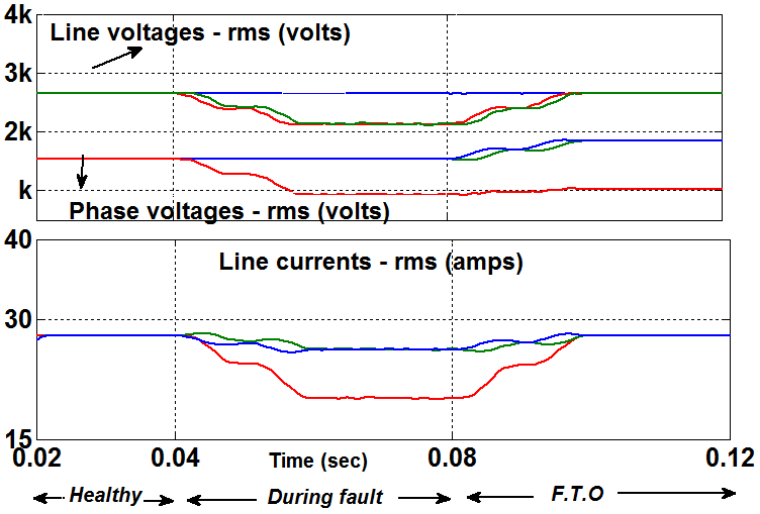
In such a case, the RMS value of the line-voltages and currents appears to be balanced but their waveforms are distorted with the appearance of lower order harmonics. Therefore to avoid this scenario, the pre-fault m_a should be reduced following the condition given in (4.50). For the considered fault case, reducing the pre-fault m_a to 0.8, the fault tolerant modulating signals are modified as given in (4.57). Reduction in pre-fault m_a limits the modulation index of (4.57) to the linear modulation range (i.e., 0.98, 0.96 and 0.96), which increases the ability to achieve FTO effectively. For the considered fault case, the pre and post-fault performance of this inverter for m_a= 0.8 as given in Fig. 4.21.

$$\left.\begin{aligned} v_a'' &= 4*0.98\sin(\omega t) \\ v_b'' &= 6*0.96\sin(\omega t - 133°) \\ v_c'' &= 6*0.96\sin(\omega t + 133°) \end{aligned}\right\} \quad (4.57)$$

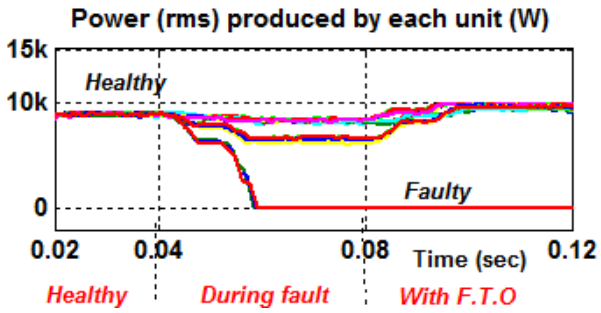
From Fig. 4.21, it is observed that the wave shape of line-voltages and currents and their respective RMS values (2645 V and 27.9 A) appears to be same in pre and post-fault compensation modes. Further, Fig. 4.21(c) depicts the effective and uniform power distribution (10.0 kW from each unit) among operating units. The effectiveness of FTO can be further verified by evaluating inverter harmonic performance as shown in Fig. 4.22. Comparing Fig. 4.22 with Fig. 4.20, the elimination of lower order harmonies in line-voltages and currents can be observed.



(a) Phase-voltage, line-voltage and line-current waveforms

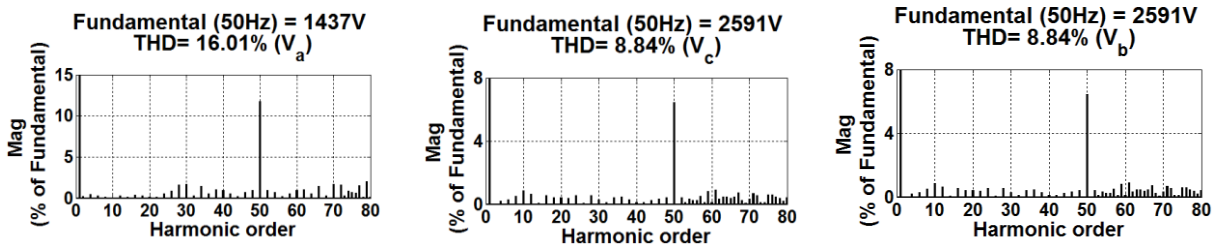


(b) Phase-voltage, line-voltage and line-current RMS values

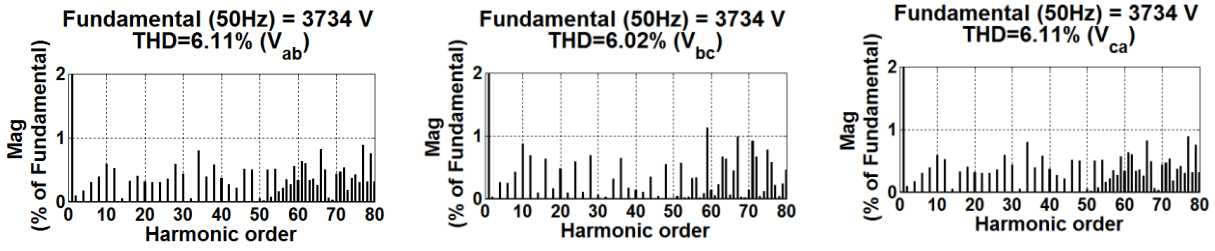


(c) Power delivered by each operating unit

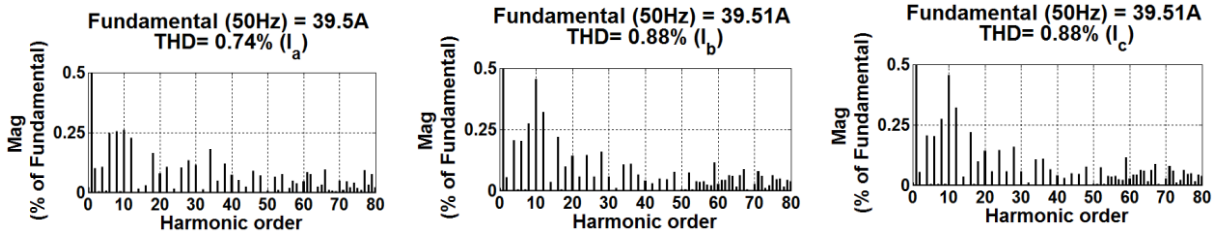
Fig. 4.21: Pre and post-fault performance of 15-level MLDCL for 3–0–0 fault with m_a = 0.8.



(a) Phase-voltages



(b) Line-voltages



(c) Line-currents

Fig. 4.22: Harmonic performance of 15-level MLDCL inverter after compensation of 3–0–0 fault with proposed FTS for m_a= 0.8.

4.5.4 *Case*-4: OC fault on four units (x = 3, y = 0 and z = 1)

Performance of the considered 15-level MLDCL inverter with three faulty units in phase-*a*, and one unit in phase-*c* is investigated here. Thus, its pre and post-fault performance for m_a = 0.9 is shown in Fig. 4.23. Fig. 4.23 shows that, with the initiation of fault at 0.04 s, the operation of the inverter is restricted and produces unbalance in phase-voltages (1025, 1722 and 1477 V), line-voltages (2374, 2760 and 2100 V) and line-currents (26, 25 and 27 A) with non-uniform power distribution among the operating units. For the appeared fault condition, the modulating signals to restore the balanced operation, obtained by substituting x= 3, y= 0, z= 1 and n= 7 in (4.48) results (4.58). Further operating (4.58) for m_a = 0.9 produces (4.59).

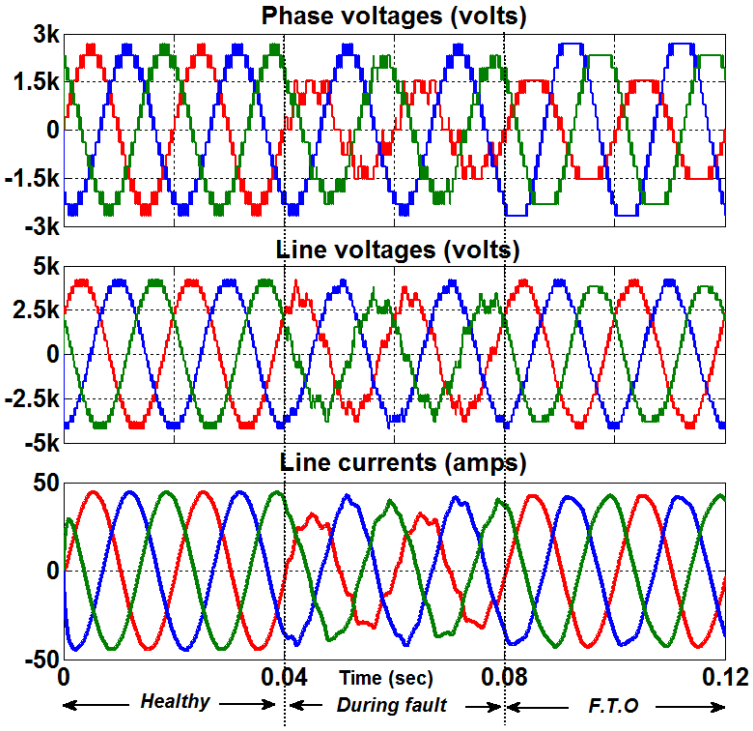
$$\left.\begin{aligned} v_a'' &= 4*1.248*m_a \sin\left(\omega t - 8.21°\right) \\ v_b'' &= 7*1.25*m_a \sin\left(\omega t - 129.35°\right) \\ v_c'' &= 6*1.26*m_a \sin\left(\omega t + 135°\right) \end{aligned}\right\} \tag{4.58}$$

$$\left.\begin{aligned} v_a'' &= 4*1.12\sin\left(\omega t - 8.21°\right) \\ v_b'' &= 7*1.125\sin\left(\omega t - 129.35°\right) \\ v_c'' &= 6*1.134\sin\left(\omega t + 135°\right) \end{aligned}\right\} \tag{4.59}$$

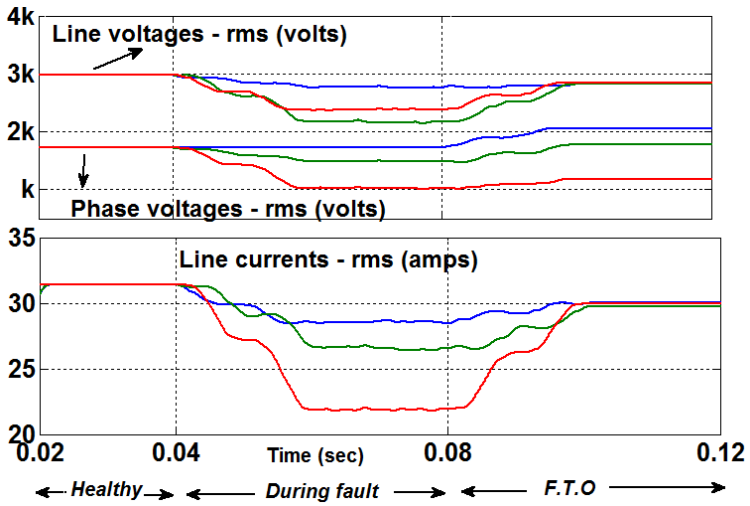
To compensate the fault burden, the obtained fault tolerant modulating signals, drives the inverter to overmodulation (i.e., 1.12, 1.125 and 1.134). Its corresponding effect on inverter performance is shown in Fig. 4.23, where overmodulation in phase-voltages is well noticed. The non-linear operation of phase-voltages, distorts the wave shape and harmonic spectra of line-voltages and line-currents. Also the power delivered by operating units are appeared to be less uniform. As NS-FTS loses its effectiveness, therefore to achieve the required FTO, the pre-fault m_a should be reduced such that the obtained fault tolerant modulating signals are in linear modulation range. Following (4.50), and operating (4.58) for pre-fault m_a of 0.8, produces the modulating signals given in (4.60).

$$\left.\begin{aligned} v_a'' &= 4*0.998\sin\left(\omega t - 8.21°\right) \\ v_b'' &= 7*1.001\sin\left(\omega t - 129.35°\right) \\ v_c'' &= 6*1.008\sin\left(\omega t + 135°\right) \end{aligned}\right\} \tag{4.60}$$

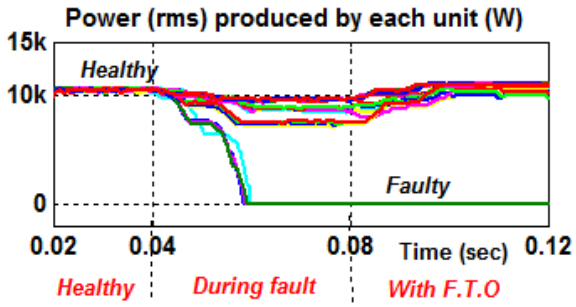
The pre and post-fault performance of 15-level MLDCL for the considered fault condition with m_a = 0.8 is shown in Fig. 4.24. From this figure, it is observed that the wave shape of line-voltages and currents and their respective RMS values (2640 V and 27.9 A) appears to be same as pre-fault mode. Further, Fig. 4.24(c) depicts the effective and uniform power distribution (10 kW from each unit) among operating units. The effectiveness of FTO can be further verified by evaluating inverter harmonic performance as shown in Fig. 4.25. From Fig. 4.25(b) and (c), it can be observed that, lower order harmonies in line-voltages and line-currents are suppressed with THD of ~6.15 % and ~0.9 % respectively.



(a) Phase-voltage, line-voltage and line-current waveforms

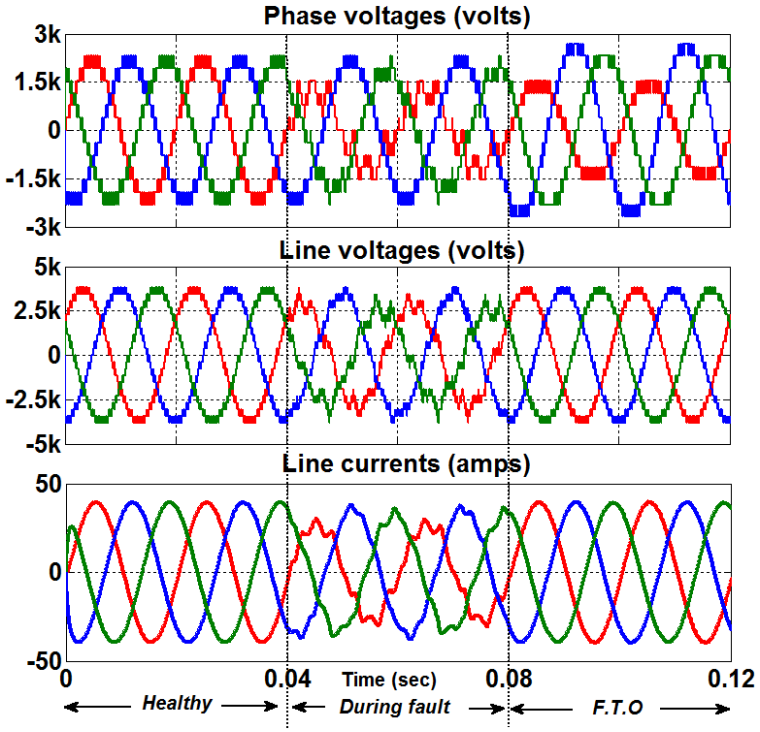


(b) Phase-voltage, line-voltage and line-current RMS values

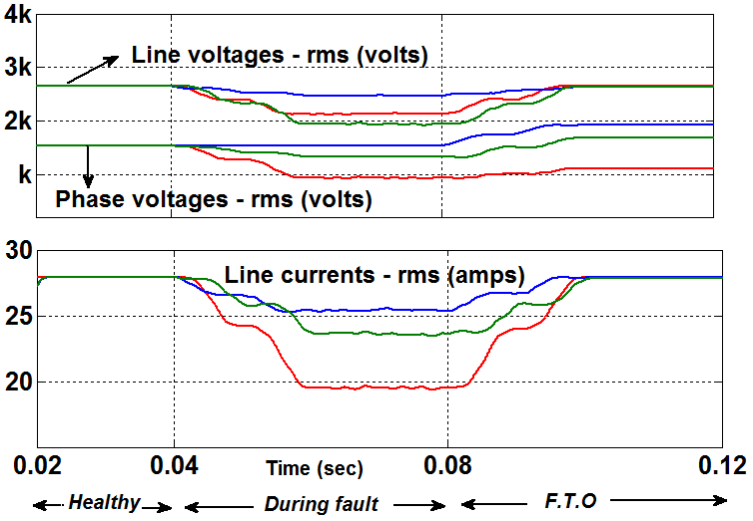


(c) Power delivered from each unit

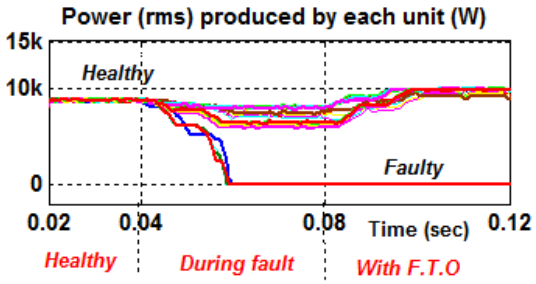
Fig. 4.23: Pre and post-fault performance of 15-level MLDCL for 3–0–1 fault with m_a= 0.9.



(a) Phase-voltage, line-voltage and line-current waveforms

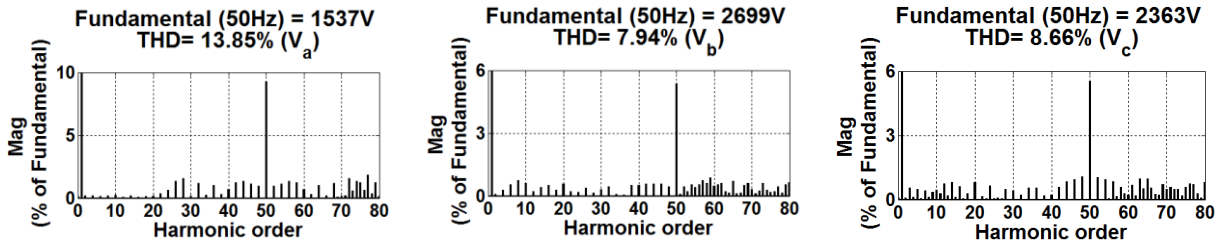


(b) Phase-voltage, line-voltage and line-current RMS values

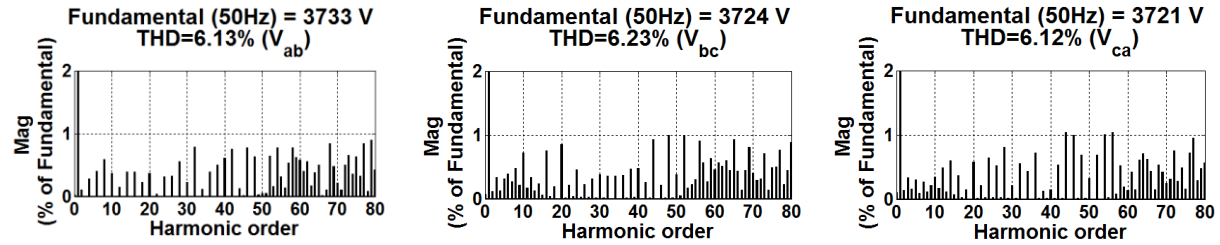


(c) Power delivered by each operating unit

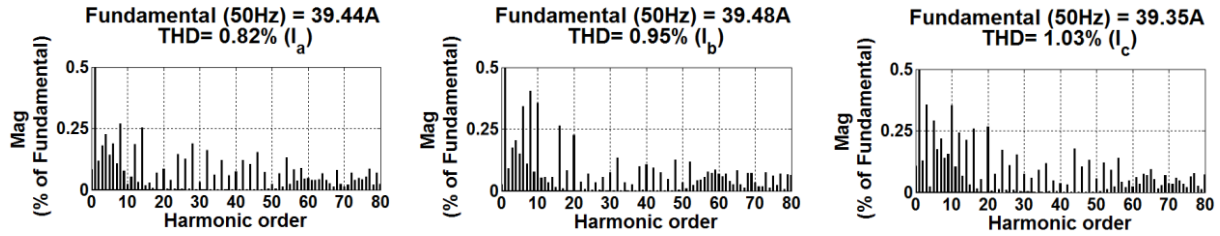
Fig. 4.24: Pre and post-fault performance of 15-level MLDCL for 3–0–1 fault with m_a= 0.8.



(a) Phase-voltages



(b) Line-voltages



(c) Line-currents

Fig. 4.25: Harmonic performance of 15-level MLDCL inverter after compensation of 3–0–1 fault with proposed FTS for m_a= 0.8.

4.5.5 *Case*-5: OC fault on six units (x = 2, y = 3 and, z = 1)

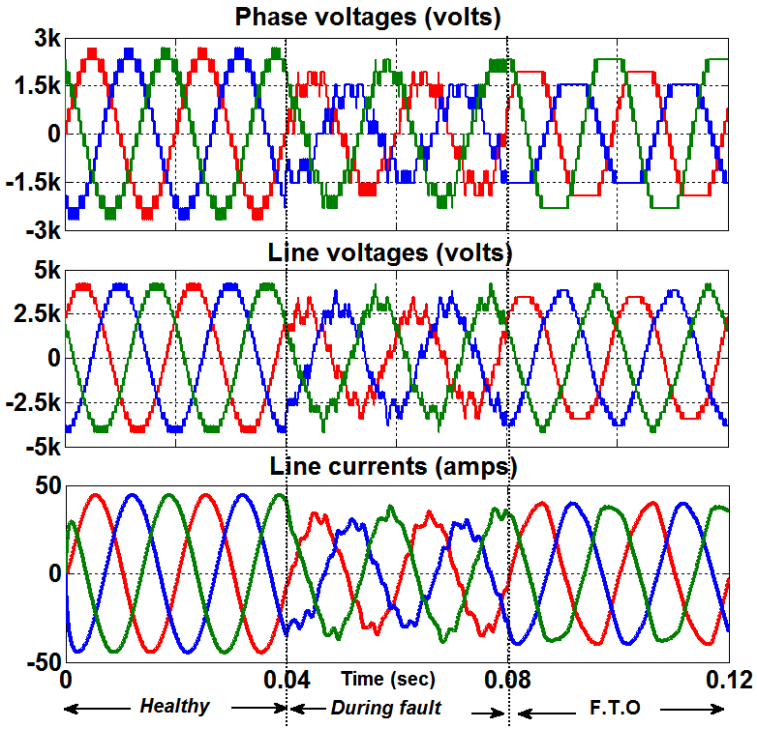
During FTO, high value of pre-fault m_a with more number of faulted units, the burden on healthy units further increases and drives the modulating signals to high overmodulation. In such a case, the RMS value of the line-voltages and currents are almost same but their waveforms are distorted. This can be observed by considering six faulty units. The desired modulating signals given in (4.61) are derived by substituting the values of x = 2, y = 3, z = 1 and n = 7 in the generalized modulating signals given in (4.48). For m_a = 0.9 and 0.7, the fault tolerant modulating signals for the appeared fault condition are given in (4.62) and (4.63) respectively.

$$\left.\begin{aligned} v_a'' &= 5*1.434*m_a \sin\left(\omega t + 13^\circ\right) \\ v_b'' &= 4*1.411*m_a \sin\left(\omega t - 153^\circ\right) \\ v_c'' &= 6*1.401*m_a \sin\left(\omega t + 114.6^\circ\right) \end{aligned}\right\} \quad (4.61)$$

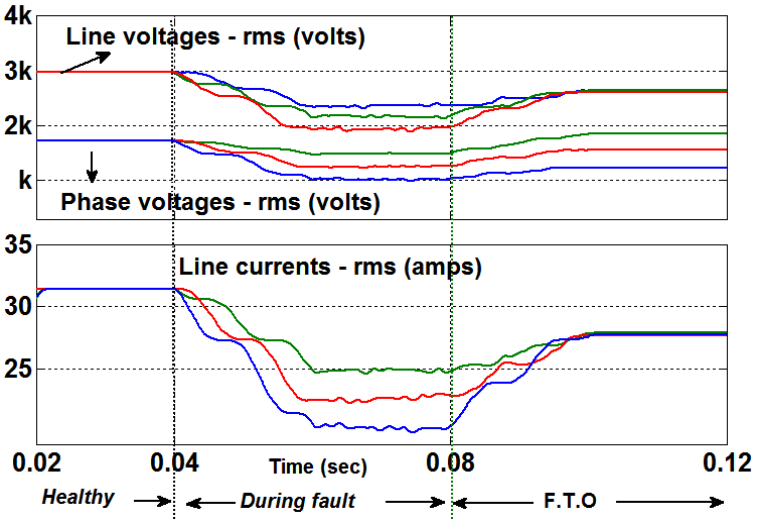
$$\left.\begin{aligned} v_a'' &= 5*1.29\sin\left(\omega t+13°\right) \\ v_b'' &= 4*1.27\sin\left(\omega t-153°\right) \\ v_c'' &= 6*1.26\sin\left(\omega t+114.6°\right) \end{aligned}\right\} \quad (4.62)$$

$$\left.\begin{aligned} v_a'' &= 5*1.00\sin\left(\omega t+13°\right) \\ v_b'' &= 4*0.98\sin\left(\omega t-153°\right) \\ v_c'' &= 6*0.98\sin\left(\omega t+114.6°\right) \end{aligned}\right\} \quad (4.63)$$

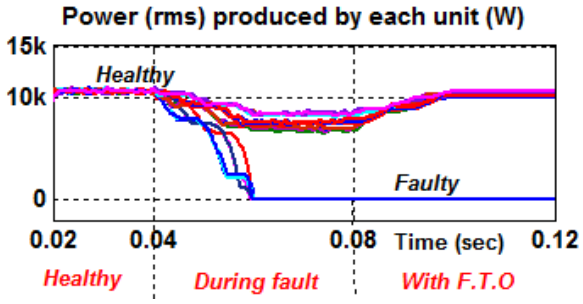
Simulated waveforms and their RMS values for this fault condition are shown in Fig. 4.26 and Fig. 4.27 for m_a = 0.9 and 0.7 respectively. During FTO, with m_a = 0.9, the inverter is operated in overmodulation (m_a* = 1.29, 1.27 and 1.26). This results in distorted shape for line-voltage waveforms but achieves almost equal RMS line-voltages (~ 2630 V) and currents (~ 27.8 A), as shown in Fig. 4.26(a) and (b). However in Fig. 4.27, with m_a = 0.7, the modulating signals are within the linear range (1.0, 0.98 and 0.98). This results balanced line-voltages and currents, both in terms of wave shape, RMS values (2315 V and 24.4 A), with uniform power distribution among operating units. The harmonic performance of the inverter voltages and currents after fault compensation with m_a = 0.7 are shown in Fig. 4.28, where the THD performance of phase-voltages, line voltages and line-currents are given in Fig. 4.28(a), (b) and (c) respectively. Thus, Fig. 4.28 verifies the elimination of lower order harmonics and uniform harmonic performance in line-voltages (~7.0%) and currents (~0.8%).



(a) Phase-voltage, line-voltage and line-current waveforms

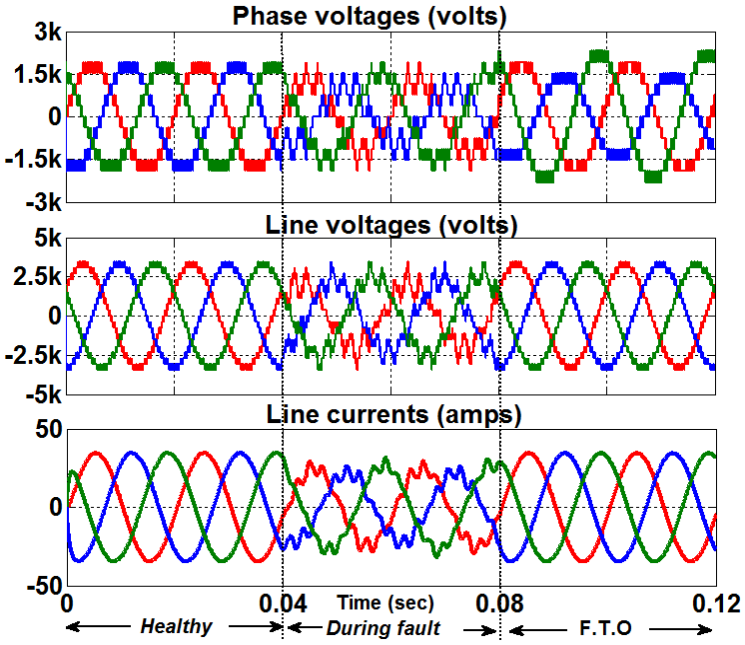


(b) Phase-voltage, line-voltage and line-current RMS values

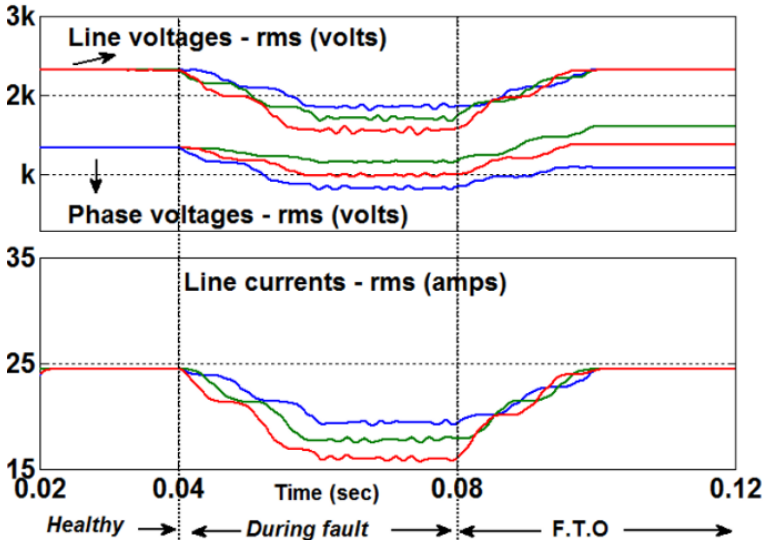


(c) Power delivered by each operating unit

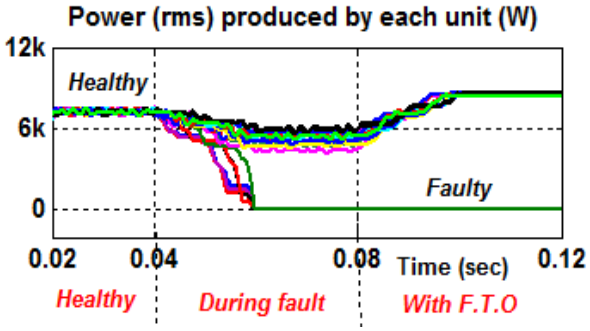
Fig. 4.26: Pre and post-fault performance of 15-level MLDCL for 2–3–1 fault with m_a= 0.9.



(a) Phase-voltage, line-voltage and line-current waveforms

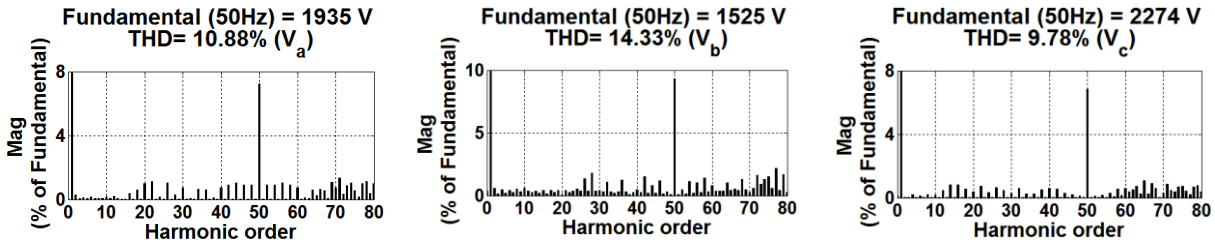


(b) Phase-voltage, line-voltage and line-current RMS values

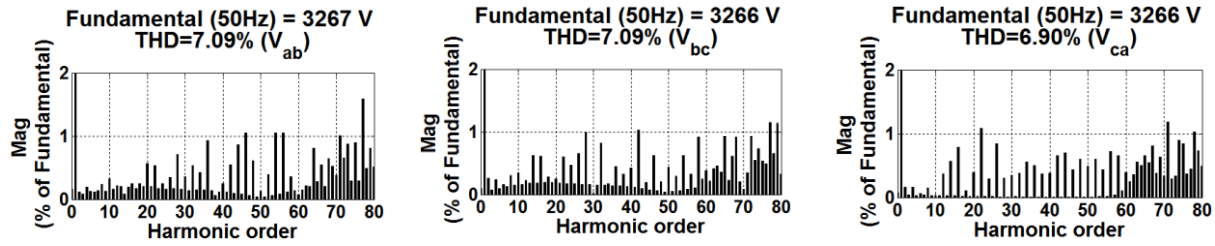


(c) Power delivered by each operating unit

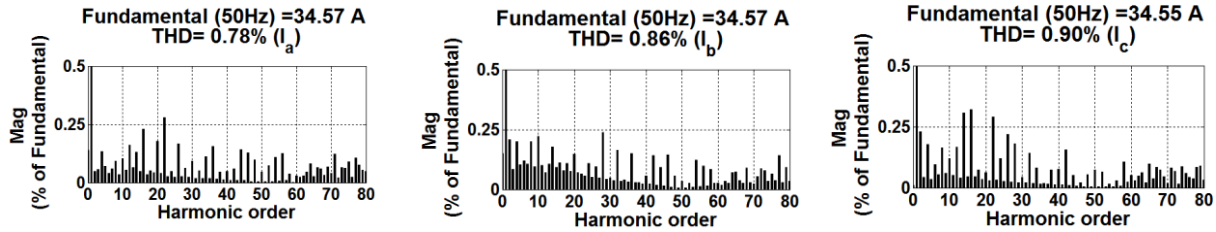
Fig. 4.27: Pre and post-fault performance of 15-level MLDCL for 2–3–1 fault with m_a= 0.7.



(a) Phase-voltages



(b) Line-voltages



(c) Line-currents

Fig. 4.28: Harmonic performance of 15-level MLDCL inverter after compensation of 2–3–1 fault with proposed FTS for $m_a = 0.7$.

Ability of the proposed generalized scheme to obtain FTO for various fault conditions with different values of m_a is presented in Table 4.3. From this table it can be observed that, high value of pre-fault m_a with increased number of faulty units, the inverter may produce balanced line-voltages. However, it may drive inverter to overmodulation and may not reach its pre-fault voltage. Therefore, to reduce the risk of going to high overmodulation, the inverter m_a should be appropriately adjusted. Finally, for any fault condition the proposed FTS produces balanced line-voltages and currents with equal power sharing among all the operating units.

Table 4.3: RMS values of phase and line-voltages for various fault conditions after fault compensation.

$x-y-z$	Phase-voltages (rms, V)				Line-voltages (rms, V)		
	m_a	V_a	V_b	V_c	V_{ab}	V_{bc}	V_{ca}
0–0–0 (Healthy)	0.9	1722	1722	1722	2974	2974	2974
	0.8	1533	1533	1533	2645	2645	2645
	0.7	1533	1533	1533	2315	2315	2316
1–0–1	0.9	1639	1902	1639	2974	2974	2974
	0.8	1459	1691	1459	2645	2645	2645
	0.7	1280	1483	1280	2316	2316	2316
2–0–0	0.9	1362	1925	1925	2973	2973	2973
	0.8	1214	1714	1715	2645	2645	2645
	0.7	1065	1503	1503	2316	2316	2316
3–0–0	0.9	1138	2016	2016	2914	2903	2914
	0.8	1029	1839	1839	2645	2645	2645
	0.7	902	1611	1611	2316	2316	2316
3–0–1	0.9	1179	2058	1786	2845	2827	2819
	0.8	1097	1914	1677	2645	2639	2636
	0.7	965	1677	1478	2315	2315	2316
2–3–0	0.9	1535	1224	2103	2685	2740	2737
	0.8	1463	1985	1985	2557	2594	2587
	0.7	1333	1054	1764	2317	2314	2316
2–2–2	0.9	1539	1539	1539	2652	2652	2652
	0.8	1469	1469	1469	2537	2537	2537
	0.7	1343	1343	1343	2316	2316	2316

4.6 Experimental validation on nine-level MLDCL inverter

To validate the efficacy of the proposed generalized FTS experimentally, a nine-level, three-phase, 170 V and 2 kVA IGBT based MLDCL RSC-MLI is developed in the laboratory. The requirement of isolated dc voltage to each bridge is obtained from dual and single channel regulated dc power supplies (RPS). Each of the isolated dc source is maintained at 30 V and a three-phase star-connected 1 kW with 0.8 power factor lagging load is used for experimentation. The experimental parameters are given in Table 4.4.

Table 4.4: Experimental parameters.

Circuit	Component
30 V isolated dc power supplies (12 No.)	Regulated power supplies: 30 V/3 A and 30 V/5 A
Three-phase nine-level MLDCL RSC-MLI	2 modules of generalized converter with 24 IGBTs each (Only 36 switches are used) IGBT model and rating (IKW40T120, 40 A and 1200 V)
Carrier frequency (f_{cr})	2.5 kHz
Load	Three-phase 1 kW *RL* load with 0.8 pf lagging
Controller (To obtain firing signals for IGBTs)	OPAL-RT (OP4500 RT Lab RCP/HIL system) Sampling time (40 μs)

The proposed FTS is implemented on OPAL-RT controller and obtained firing pulses are given to the developed inverter. To observe the efficacy of the proposed FTS the following experimental studies are performed.

Case*-1*: Two unit failure: x = 1, y = 0 and z = 0: One faulty unit in phase-*a* (16.66% fault on the inverter: Phase-*a* 25% faulty)

Case*-2*: Three unit failure: x = 2, y = 1 and z = 0: Two faulty units in phase-*a*, and one faulty unit in phase-*b*. (25% fault on the inverter: 50% fault on phase-*a*, and 25% fault on phase-*b*)

Case*-3*: Four unit failure: x = 2, y =1 and z = 1: Two faulty units in phase-*a*, and one unit on each phase-*b* and *c* (33.33% fault on the inverter: 50% fault on phase-*a*, and 25% fault on phase-*b* and *c* each)

The experimental pre and post-fault performance of the nine-level MLDCL inverter is evaluated for the various cases. The corresponding inverter voltages and currents are demonstrated such that the balanced operation of inverter during healthy condition is shown in first cycle. In subsequent two cycles, the unbalance in voltages and currents due to fault initiation is shown and in next two cycles FTO of the inverter is demonstrated with the proposed FTS.

4.6.1 *Case*-1: Failure of one unit (x = 1, y = 0 and z = 0)

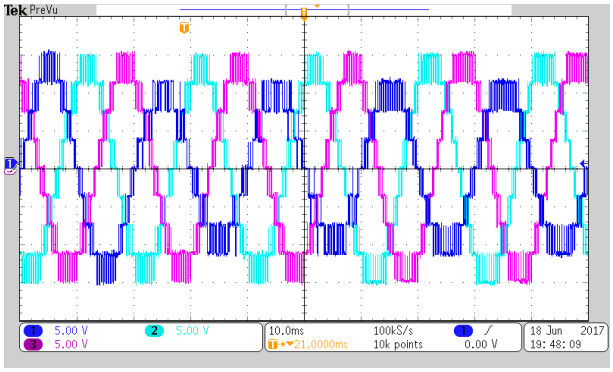
Modulating signals obtained from the proposed NS zero-sequence injection FTS to compensate OC fault in one unit of phase-*a* in the considered nine-level MLDCL RSC-MLI are given in (4.64). These fault tolerant modulating signals are obtained by substituting x = 1, y = 0, z = 0 and n = 4 in (4.48).

$$\left.\begin{aligned} v_a'' &= 3*1.091*m_a \sin(\omega t) \\ v_b'' &= 4*1.102*m_a \sin(\omega t - 127.9°) \\ v_c'' &= 4*1.102*m_a \sin(\omega t + 127.9°) \end{aligned}\right\} \quad (4.64)$$

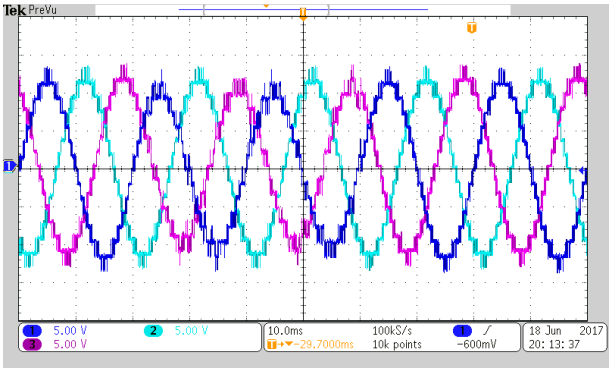
From (4.64), it is observed that modulation index of phase-*a*, *b* and *c* is 1.109, 1.102 and 1.102 times pre-fault m_a. Further, substituting m_a = 0.9 in (4.64), results (4.65) and controlling the inverter with these modulating signals produces balanced set of line-voltages and line-currents. The obtained pre and post-fault experimental performance of nine-level MLDCL inverter operating for m_a = 0.9 is shown in Fig. 4.29.

$$\left.\begin{aligned} v_a'' &= 3*0.98 \sin(\omega t) \\ v_b'' &= 4*0.99 \sin(\omega t - 127.9°) \\ v_c'' &= 4*0.99 \sin(\omega t + 127.9°) \end{aligned}\right\} \quad (4.65)$$

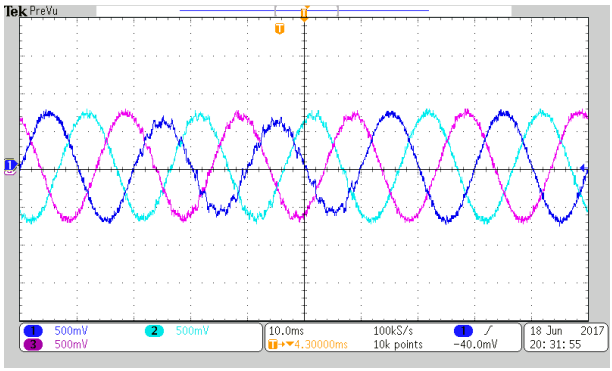
Fig. 4.29 shows the pre and post-fault performance of 9-level MLDCL with 1–0–0 fault condition, where the waveforms of the phase-voltages, line-voltages and line-currents are shown in Fig. 4.29(a), (b) and (c) respectively.



(a) Phase-voltages

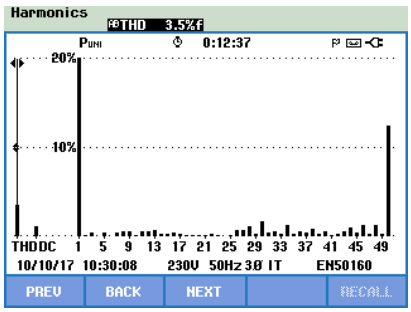


(b) Line-voltages

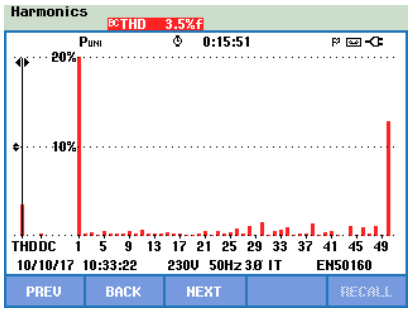


(c) Line-currents

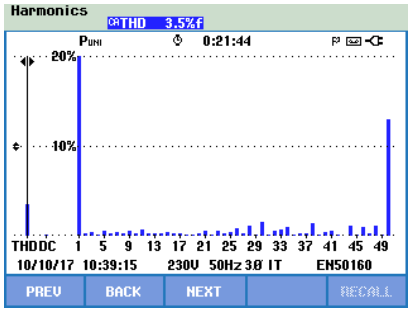
Fig. 4.29: Pre and post-fault performance of nine-level MLDCL inverter for 1–0–0 fault with m_a= 0.9.



V_a

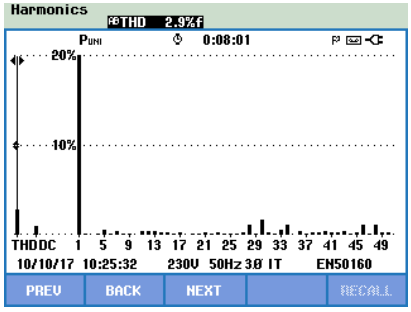


V_b

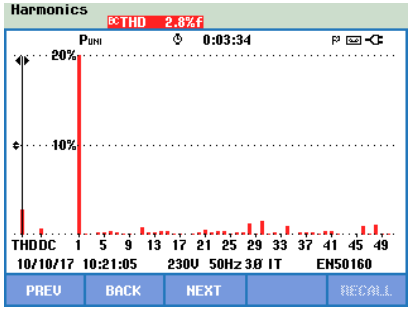


V_c

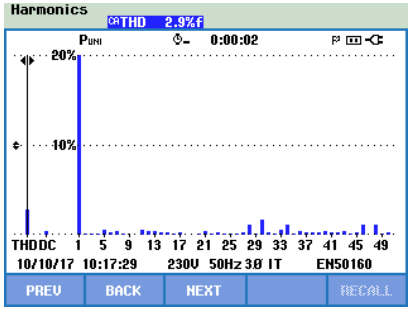
(a) Phase-voltages



V_{ab}



V_{bc}

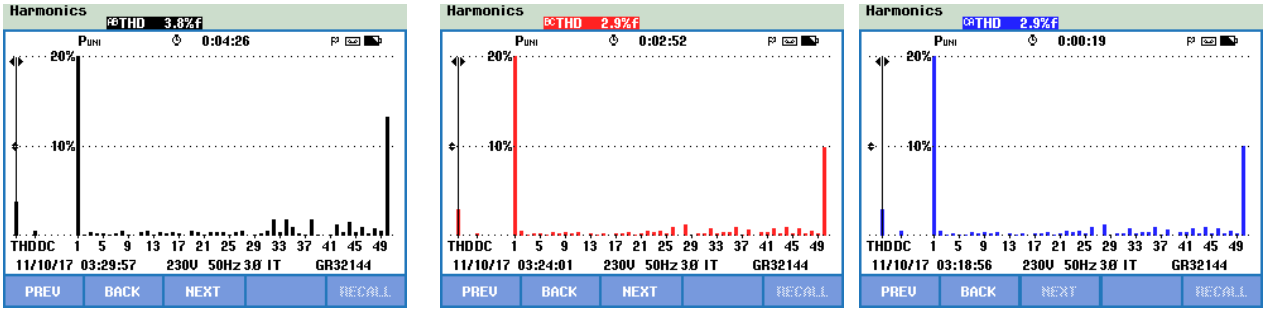


V_{ca}

(b) Line-voltages

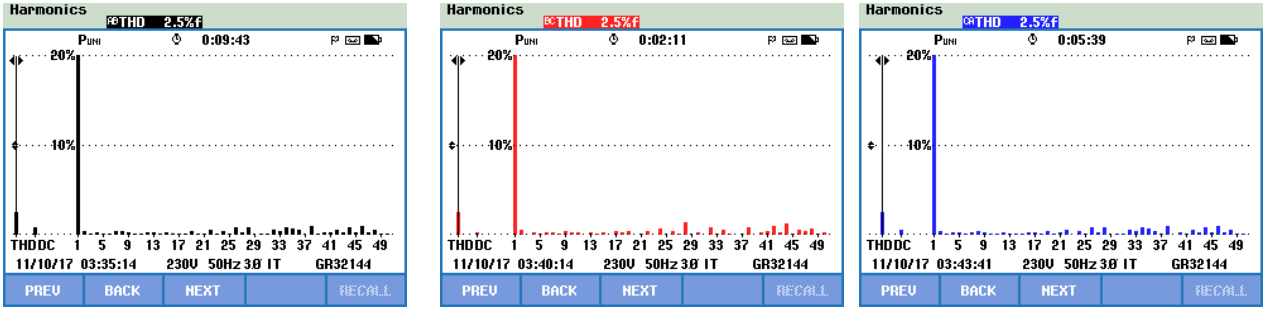
Fig. 4.30: Harmonic performance of nine-level MLDCL inverter in healthy condition for m_a= 0.9.

Fig. 4.29 shows the balanced operation of the inverter in healthy condition, which can further verified by their harmonic performance. Fig. 4.30 shows the harmonic performance of the inverter phase-voltage (3.5%) and line-voltage (2.9%) for m_a = 0.9. From Fig. 4.29, with the initiation of fault, the unbalanced phase-voltages distorts the line-voltages and line-currents. In order to restore the balanced operation, the proposed FTS produces balanced set of line-voltages and line-currents using new set of modulating signals derived in (4.65). The fault compensation and balanced operation of inverter can be observed in Fig. 4.29. The phase and line-voltage harmonic performance after fault compensation is shown in Fig. 4.31. Thus, Fig. 4.29 and Fig. 4.31 verifies the effectiveness of FTO of proposed FTS, where the unbalanced phase-voltages produces balanced line-voltages with THD of 2.5%, 2.5% and 2.5% respectively in three- phases.



V_a V_b V_c

(a) Phase-voltages



V_{ab} V_{bc} V_{ca}

(b) Line-voltages

Fig. 4.31: Harmonic performance of nine-level MLDCL after compensation of 1–0–0 fault for m_a= 0.9.

4.6.2 *Case*-2: Failure of three units (x = 2, y = 1 and z = 0)

Fault tolerant modulating signals to compensate simultaneous failure on two-units in phase-*a*, and one unit in phase-*b* of nine-level MLDCL inverter are given in (4.66). From (4.66), it can be observed that to overcome the fault burden, the proposed FTS operates phase-*a*, *b* and *c* at 1.38, 1.42 and 1.34 times pre-fault m_a respectively. Substituting m_a = 0.9 in (4.66), results (4.67), where modulation index of phase-*a*, *b* and *c* are 1.24, 1.27 and 1.20 respectively.

$$\left.\begin{aligned} v_a'' &= 2*1.38*m_a \sin(\omega t+16.1^\circ) \\ v_b'' &= 3*1.42*m_a \sin(\omega t-141.0^\circ) \\ v_c'' &= 4*1.34*m_a \sin(\omega t+128.21^\circ) \end{aligned}\right\} \quad (4.66)$$

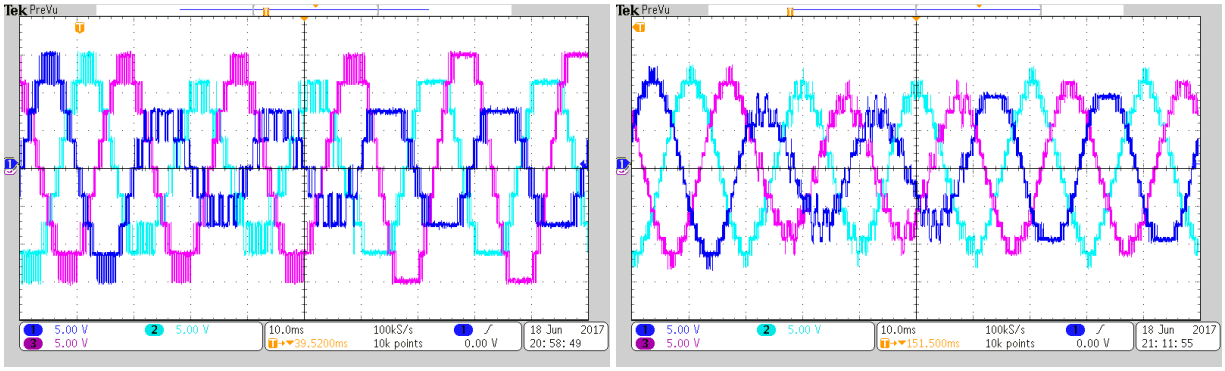
$$\left.\begin{aligned} v_a'' &= 2*1.24\sin(\omega t+16.1^\circ) \\ v_b'' &= 3*1.27\sin(\omega t-141.0^\circ) \\ v_c'' &= 4*1.20\sin(\omega t+128.21^\circ) \end{aligned}\right\} \quad (4.67)$$

Thus, controlling inverter with (4.67) drives it to non-linear range of operation and cannot synthesize the desired FTO. This can be verified from Fig. 4.32, where the FTO of the considered inverter with (4.67) is shown, for m_a = 0.9. Its corresponding harmonic performance of phase and line-voltages after compensation is shown in Fig. 4.33.

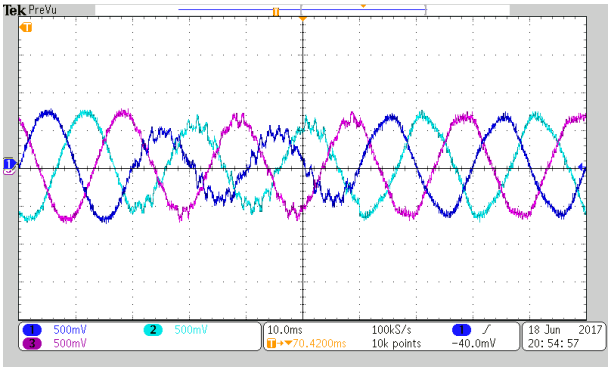
Thus, Fig. 4.32 shows that the waveforms of line-voltages and currents obtained after fault compensation are dissimilar. Further Fig. 4.33, shows their unbalance in harmonic spectra of phase-voltages (12.4%, 9.8% and6.4 %) and line-voltages (7.7%, 7% and 4.4%). Thus, Fig. 4.32 and Fig. 4.33, confirms the inability of the proposed FTS to achieve desired FTO. Hence to compensate the fault effectively, the pre-fault m_a should be reduced such that modulation index of (4.66) operates in linear range. Thus, substituting m_a = 0.7 in (4.66) produces fault tolerant modulating signals in linear range as given in (4.68).

$$\left.\begin{aligned} v_a'' &= 2*0.966\sin(\omega t+16.1^\circ) \\ v_b'' &= 3*0.868\sin(\omega t-141.0^\circ) \\ v_c'' &= 4*0.938\sin(\omega t+128.21^\circ) \end{aligned}\right\} \quad (4.68)$$

The pre and post-fault performance of the inverter at m_a = 0.7 is shown in Fig. 4.34, where its corresponding phase-voltages, line-voltages and line-currents are given in Fig. 4.34(a), (b) and (c) respectively. The harmonic spectra of the inverter phase and line-voltages obtained after fault compensation are shown in Fig. 4.35. From Fig. 4.34, it can be observed that initiation of proposed FTS, produces balanced set of line-voltages and line-currents from unbalanced phase-voltages. The waveforms of balanced line-voltages and line-currents obtained after fault compensation is similar to pre-fault condition. Further, the respective THD performance of phase and line-voltages shown in Fig. 4.35, verifies the ability of proposed FTS in tolerating the fault.

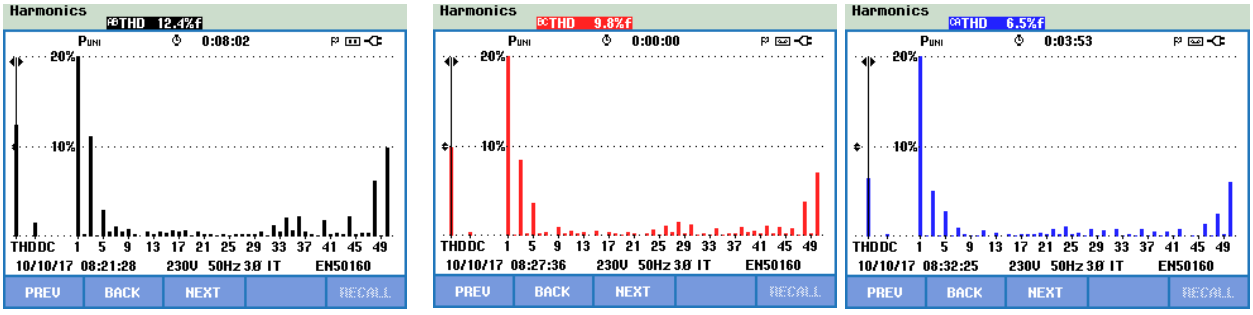


(a) Phase-voltages (b) Line-voltages



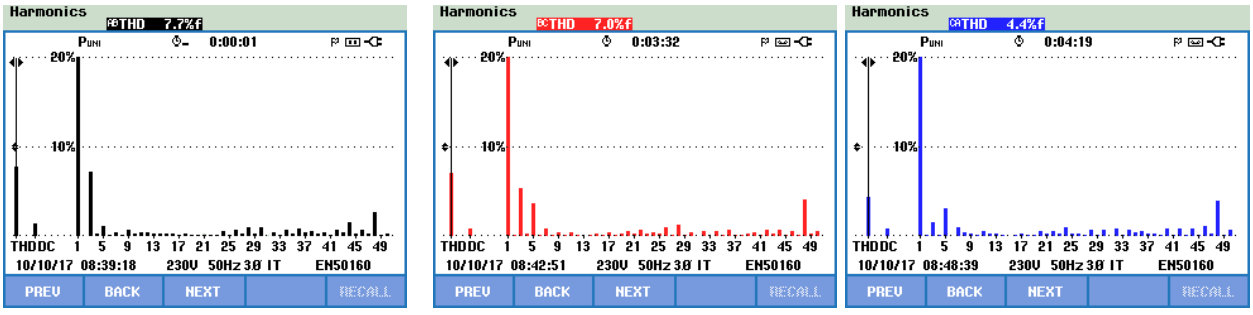
(c) Line-currents.

Fig. 4.32: Pre and post-fault performance of nine-level MLDCL inverter for 2–1–0 fault with m_a = 0.9.



V_a V_b V_c

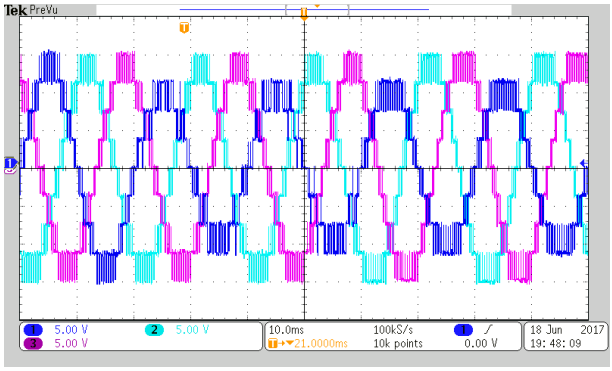
(a) Phase-voltages



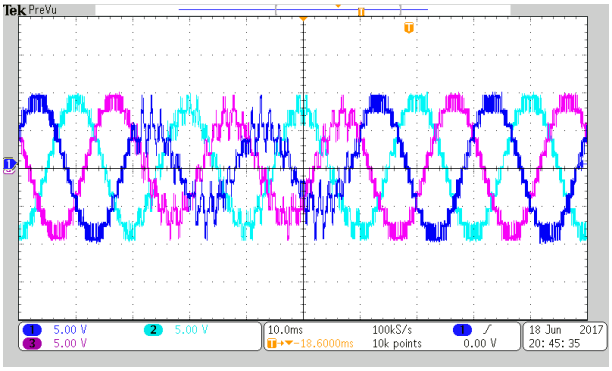
V_{ab} V_{bc} V_{ca}

(b) Line-voltages

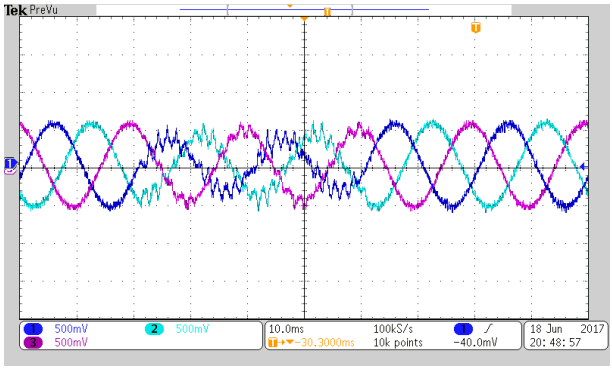
Fig. 4.33: Harmonic performance of nine-level MLDCL, after compensation of 2–1–0 fault for m_a = 0.9.



(a) Phase-voltages

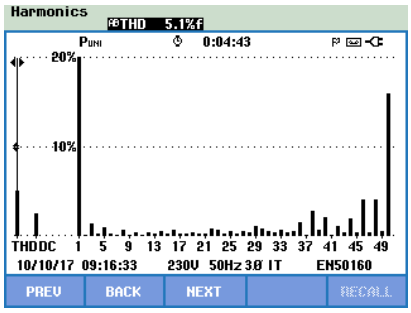


(b) Line-voltages

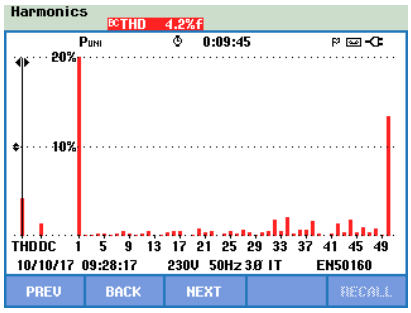


(c) Line-currents.

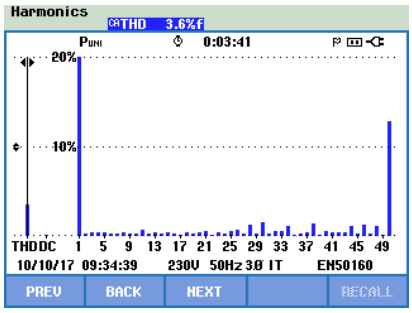
Fig. 4.34: Pre and post-fault performance of nine-level MLDCL inverter with 2–1–0 fault for m_a = 0.7.



V_a

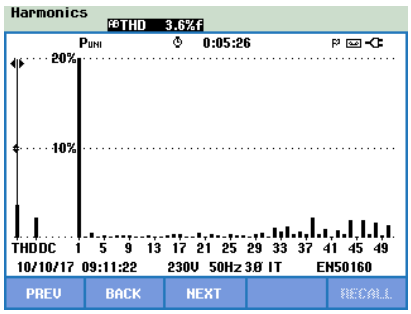


V_b

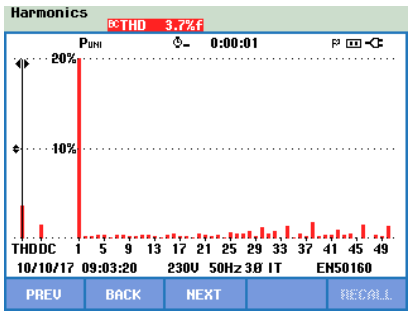


V_c

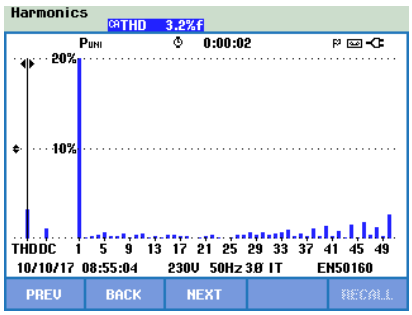
(a) Phase-voltages



V_{ab}



V_{bc}



V_{ca}

(b) Line-voltages

Fig. 4.35: Harmonic performance of nine-level MLDCL, after compensation of 2–1–0 fault for m_a = 0.7.

4.6.3 *Case*-3: Failure of four units (x = 2, y = 1 and z = 1)

Fault tolerant modulating signals to compensate simultaneous failure on two-units in phase-*a*, and one unit in phase-*b* and phase-*c* of nine-level MLDCL inverter are given in (4.69). From (4.69) it is observed that, to tolerate the appeared fault, the proposed FTS operates phase-*a*, *b* and *c* at 1.5, 1.53 and 1.53 times pre-fault m_a respectively. Substituting m_a = 0.9 in (4.69), results (4.70), where the operating modulation index of phase-*a*, *b* and *c* are 1.35, 1.37 and 1.37 respectively. Controlling faulty inverter with (4.70) drives to non-linear range of operation and may not synthesize a satisfactory waveforms for line-voltages. This can be verified from Fig. 4.36, where the FTO of the considered inverter with (4.70) is shown with respect to its performance in pre-fault mode, for m_a = 0.9.

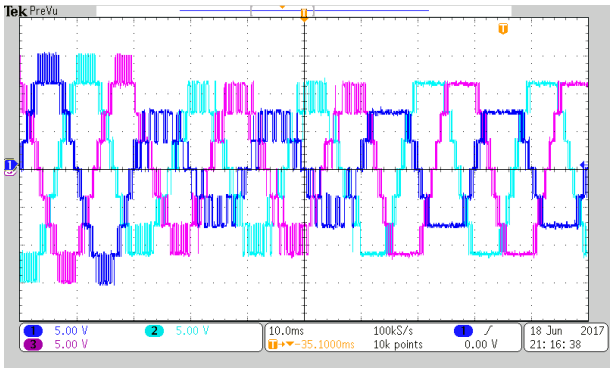
$$\left.\begin{aligned} v_a'' &= 2*1.5*m_a \sin\ \omega t \\ v_b'' &= 3*1.527*m_a \sin\left(\omega t - 130.89°\right) \\ v_c'' &= 3*1.527*m_a \sin\left(\omega t + 130.89°\right) \end{aligned}\right\} \tag{4.69}$$

$$\left.\begin{aligned} v_a'' &= 2*1.35 \sin\ \omega t \\ v_b'' &= 3*1.374 \sin\left(\omega t - 130.89°\right) \\ v_c'' &= 3*1.374 \sin\left(\omega t + 130.89°\right) \end{aligned}\right\} \tag{4.70}$$

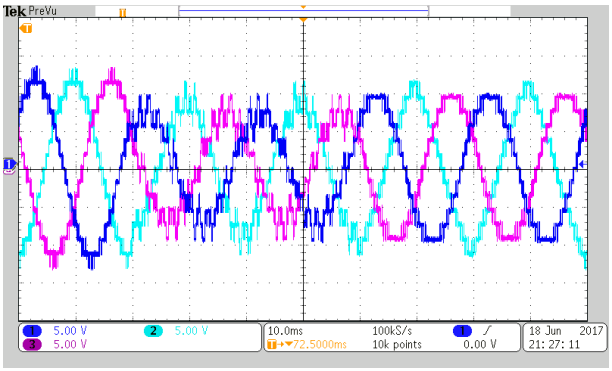
Thus, Fig. 4.36 shows that the wave shape of the obtained compensated line-voltages and currents appears to be dissimilar and unbalanced. Hence to compensate fault effectively, (4.69) should be operated in linear-range of modulation. Substituting m_a = 0.7 in (4.69), produces fault tolerant modulating signals in linear range (4.71).

$$\left.\begin{aligned} v_a'' &= 2*1.05 \sin\ \omega t \\ v_b'' &= 3*1.06 \sin\left(\omega t - 130.89°\right) \\ v_c'' &= 3*1.06 \sin\left(\omega t + 130.89°\right) \end{aligned}\right\} \tag{4.71}$$

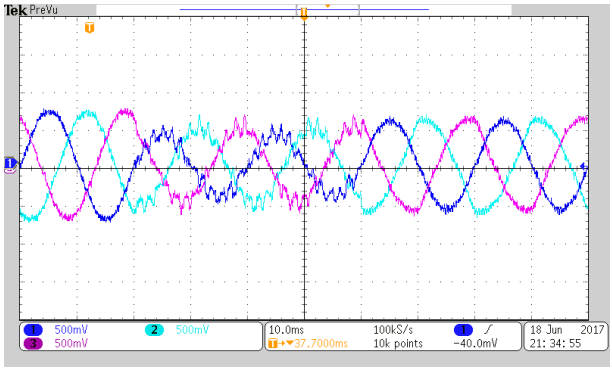
The pre and post-fault performance of the inverter at m_a = 0.7 is shown in Fig. 4.37, where its corresponding phase-voltages, line-voltages and line-currents are given in Fig. 4.37(a), (b) and (c) respectively. The Harmonic spectra of the inverter phase and line-voltages obtained after fault compensation are shown in Fig. 4.38. From Fig. 4.37, it is observed that initiation of proposed FTS, produces balanced set of line-voltages and line-currents from the unbalanced phase-voltages. Also the nature of magnitude and waveform of the balanced line-voltages and line-currents obtained after the faulted compensation is similar to their respective nature in pre-fault condition. Further, the respective THD performance of compensated phase-voltage and line-voltages are shown in Fig. 4.38 verifies the ability of proposed FTS in tolerating the fault.



(a) Phase-voltages

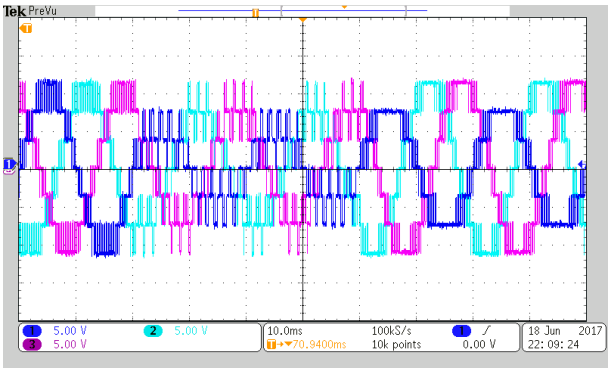


(b) Line-voltages

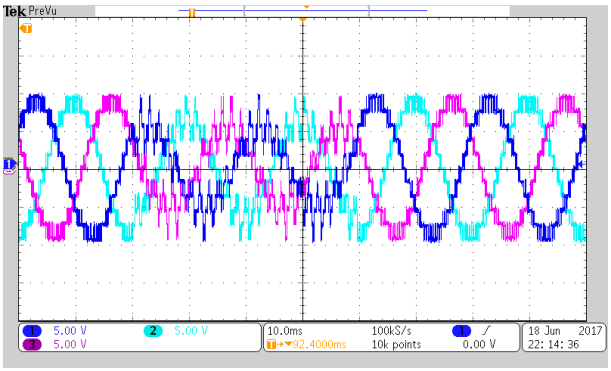


(c) Line-currents.

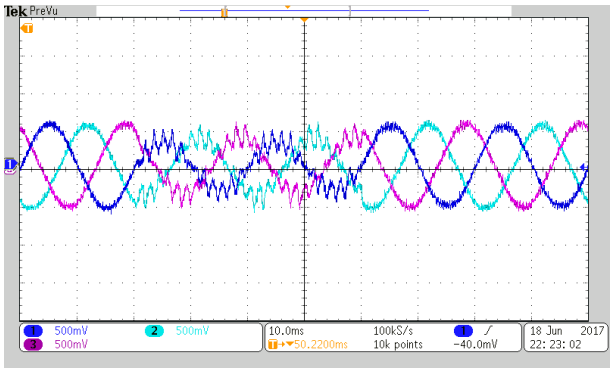
Fig. 4.36: Pre and post-fault performance of nine-level MLDCL inverter for 2–1–1 fault with m_a= 0.9.



(a) Phase-voltages

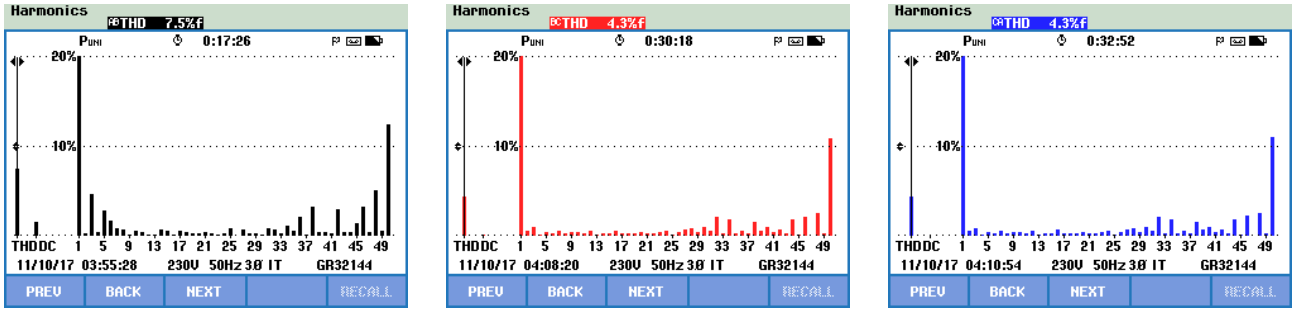


(b) Line-voltages



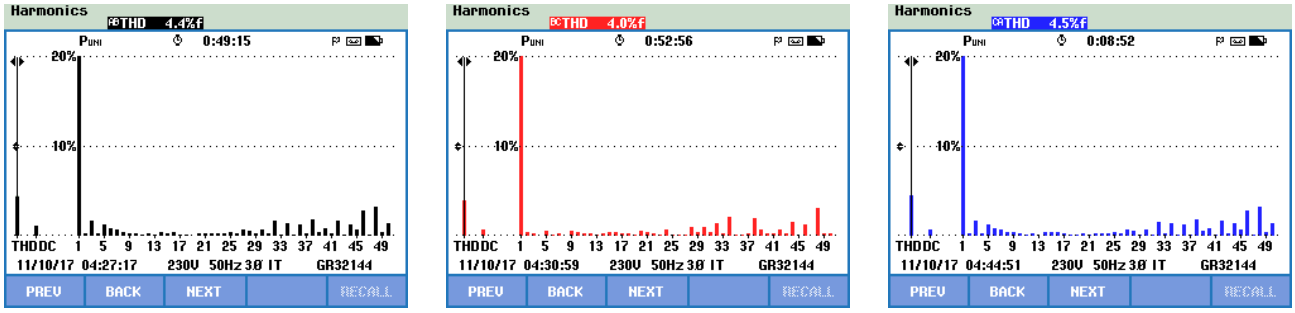
(c) Line-currents.

Fig. 4.37: Pre and post-fault performance of nine-level MLDCL inverter for 2–1–1 fault with m_a = 0.7.



V_a V_b V_c

(a) Phase-voltages



V_{ab} V_{bc} V_{ca}

(b) Line-voltages

Fig. 4.38: Harmonic performance of nine-level MLDCL inverter, after compensation of 2–1–1 fault for m_a = 0.7.

Therefore, evaluating the performance of MLDCL RSC-MLI and its corresponding harmonic performance in healthy, faulty and fault tolerant operating modes for various fault cases shown in Fig. 4.29 to Fig. 4.38, the following observations can be drawn.

- During pre-fault condition, the 9-level MLDCL inverter operates with balanced voltages and currents with similar THD performance on all the phases
- With the initiation of the fault, the inverter operation is restricted and produced unbalanced phase-voltages, line-voltages and line-currents (as shown in Fig. 4.32 and Fig. 4.36)
- With initiation of the proposed FTS and controlling the faulty inverter with the modified fault tolerant modulation signals as per the appeared fault condition with the appropriate m_a, compensated the fault effectively and restored the inverter balanced operation (as shown in Fig. 4.29, Fig. 4.34 and Fig. 4.37).

However, it is to be noted that these fault tolerant modulating signals can compensate the fault effectively only if their new amplitude modulation index (m_a*) on all phases operates in linear range. Increase in the number of faulty units, increases the burden on these modulating signals and produce dissimilar line-voltages with lower order harmonics due to overmodulation. Thus, consequently to limit m_a* to linear-range, pre-fault m_a should be reduced. Therefore, the proposed FTS can compensate simultaneous failure of multiple switches, where the unbalanced phase-voltages produces balanced set of line-voltages and currents, with a performance similar to the pre-fault condition.

To further verify the efficacy of the proposed FTS scheme, simulation studies are performed on nine-level MLDCL inverter with same experimental parameters. A comprehensive comparison between nine-level simulation and experimental studies are presented in Table 4.5. From this table it can be observed that the simulation results are in good agreement with experimental results and further supports the effectiveness of the proposed FTS. It should be noted that in experimental harmonic spectra, up to 49^{th} order harmonics are considered.

Table 4.5: Comparison of simulation and experimental studies of the proposed FTS on nine-level MLDCL inverter for various fault conditions.

Experimental performance								**Simulation performance**					
Fault case		**Phase-voltage RMS (%THD)**			**Line-voltage RMS (%THD)**			**Phase-voltage RMS (%THD)**			**Line-voltage RMS (%THD)**		
$x-y-z$	m_a	V_a''	V_b''	V_c''	V_{ab}	V_{bc}	V_{ca}	V_a''	V_b''	V_c''	V_{ab}	V_{bc}	V_{ca}
0−0−0	0.9	76.3 (3.5%)	76.8 (3.5%)	76.1 (3.5%)	131.2 (2.9%)	131.9 (2.8%)	132.0 (2.9%)	77.8 (17.0%)	77.2 (16.9%)	77.3 (16.9%)	132.8 (8.7%)	132.7 (8.8%)	132.8 (8.6%)
1−0−0	0.9	62.3 (3.9%)	83.4 (2.9%)	83.7 (2.9%)	130.7 (2.5%)	130.9 (2.5%)	131.0 (2.5%)	63.5 (19.5%)	84.6 (14.8%)	84.6 (14.8%)	132.3 (9.2%)	131.9 (8.7%)	132.3 (9.2%)
2−1−0	0.9	41.4 (12.4%)	71.6 (9.8%)	93.0 (6.5%)	116.6 (7.7%)	118.6 (7.0%)	119.1 (4.4%)	42.2 (22.2%)	72.9 (16.7%)	94.8 (13.0%)	117.7 (11.7%)	120.1 (13.5%)	120.8 (11.7%)
2−1−1	0.9	48.7 (15.5%)	72.6 (11.3%)	72.5 (11.3%)	110.4 (4.7%)	110.0 (7.2%)	110.5 (4.5%)	49.7 (22.2%)	74.09 (17.3%)	74.0 (17.3%)	111.8 (11.2%)	111.4 (14.4%)	111.8 (11.2%)
0−0−0	0.7	59.9 (4.3%)	58.9 (4.2%)	59.3 (4.2%)	101.3 (3.6%)	102.0 (3.5%)	102.6 (3.6%)	60.8 (21.2%)	61.0 (21.4%)	61.0 (21.4%)	103.9 (12.0%)	104.1 (11.9%)	103.9 (12.0%)
2−1−0	0.7	41.7 (5.1%)	63.2 (4.2%)	79.3 (3.6%)	102.2 (3.6%)	101.6 (3.7%)	101.9 (3.2%)	42.5 (30.5%)	64.4 (19.3%)	80.9 (16.5%)	102.8 (12.1%)	103.2 11.7%)	103.0 (11.9%)
2−1−1	0.7	44.2 (7.5%)	66.1 (4.3%)	66.2 (4.3%)	101.0 (4.4%)	100.6 (4.2%)	101.9 (4.4%)	45.1 (25.6%)	67.4 (16.7%)	67.4 (16.7%)	101.6 (12.4%)	101.2 (12.6%)	101.6 (12.4%)

4.7 Summary

In this Chapter, NS-FTS is the proposed for compensating multiple OC faults in RSC based MLDCL topology. Mathematical equations for obtaining the modified modulating signals in achieving FTO for a generalised fault condition are derived. Simulation and experimental studies are carried out under various fault conditions on fifteen-level and nine-level MLDCL respectively. From these results, the following conclusions are derived.

- The unbalanced phase-voltages produced a balanced set of line-voltages and currents with equal RMS values.
- During FTO, if the inverter is operating in overmodulation, then it results in lower-order harmonics in the compensated line-voltages. However, their RMS values remain almost equal.
- This scheme achieved fault compensation for multiple faulty units along with uniform power distribution among all the healthy units.
- Uniform power distribution among the healthy units will ensure balance of dc capacitor voltages and equal heat distribution even under fault conditions.

CHAPTER 5: MLDCL BASED ACTIVE RECTIFER

This chapter presents the significance of RSC-MLC based active rectifiers and then investigates the performance of three-phase MLDCL based active rectifier. For this, a comprehensive control strategy is proposed for effective balance of dc link voltages under healthy and faulty operating conditions. Further, the performance of the proposed control strategy is validated on OPAL-RT controller for change in set-point references and multiple fault conditions.

5.1 Introduction

Solid-state ac–dc conversion of electric power is widely employed in switched-mode power supplies (SMPS), adjustable-speed drives (ASD), grid integration of non-conventional energy sources, uninterrupted power supplies (UPS), battery energy storage system (BESS), electroplating, welding, battery chargers, and power supplies for telecommunication systems [130-135]. In the early days, diode bridge rectifiers (uncontrolled rectifiers) and thyristor bridge rectifiers (phase-controlled rectifiers) are primarily developed for ac-dc conversion. Even though these rectifiers are simpler and widely popular, its application is limited in high performance applications due to the following demerits [16, 134]:

- Poor input power factor
- Input current distortion and poor THD
- Output voltage ripple
- Large filter size: Input ac filter (*LC*) and output dc filter (*C*)
- Inability to regulate dynamic voltage variations
- Non-regenerative (uncontrolled rectifiers) and limited regeneration (phase-controlled rectifiers)
- Slow dynamic response

To improve the input power factor of these phase-controlled rectifiers, various power factor improvement methods are suggested by replacing the line-commutated devices with self-commutated devices. These power factor improvement methods include extinction angle control, symmetric angle control and PWM control. However, these methods partially improve the source power factor with limited regeneration capacity and further not suitable for high power applications.

With the advent of self-commutated switching devices, conceptually different way of ac-dc converters are developed. These converters are known as unity power factor converters or improved power quality converters (IPQC). These converters involves self-commutated devices to actively change the shape of input current waveform, improves power factor and

maintains desired voltage on dc side [136]. Since in some applications, a constant regulated output dc voltage is required with uni-directional power flow such as in SMPSs, low-rating ASDs, air conditioners, while in few applications such as battery chargers, UPS, BESS and high-performance motor drives require a bi-directional power flow converter. These bi-directional power flow converters are also known as active front-end (AFE) converters. These converters can be of isolated or non-isolated with bi-directional or uni-directional nature.

In literature, various topologies of IPQC converters are reported. They are mainly classified into four major categories, namely boost, buck, buck-boost and multilevel converters [134, 135]. However, among all topologies of IPQCs, bi-directional boost PWM rectifier is the simplest configuration and is widely incorporated for various ac-dc applications. The topological configuration of this PWM regenerative rectifier is developed by replacing the line-commutated devices with self-commutated devices.

IPQCs can be classified into voltage source rectifiers (VSRs) and current source rectifiers (CSRs) [1-3]. VSR regulates dc output voltage and involves solid-state devices with uni-directional voltage blocking and bi-directional current conducting capability such as IGBTs. Similarly, CSR produces dc output current and involves solid state devices with bi-directional voltage and current blocking capability [96, 136]. CSR produces high di/dt due to the unavoidable high inductance at the ac mains and to alleviate this problem, it is mandatory to incorporate *C*-filter at the ac input side. Moreover, CSR involves an *L*-filter in the output to reduce the dc current ripple. This requirement of bulky filters at input and output side increases the complexity of CSR over VSR. Thus, VSR based PWM rectifiers are most common for front-end converters [4, 5].

5.2 VSR based front-end converter

These converters involve voltage controlled self-commutating solid-state switching devices arranged in bridge configuration and possess the capability of regeneration. These converters are widely used in applications such as ASD, UPS, BESS, PV, HVDC systems and electric vehicles [96, 136].

VSR is equivalent to VSI with power flow from ac to dc (rectification). VSR produces a regulated dc output voltage from ac-mains and incorporates a dc link at the output side. This dc link involves single/multiple capacitors and accomplishes a feedback control loop to regulate the dc link voltage (output voltage). Thus, the basic operating principle of VSR contains a feedback control loop to ensure the load dc link voltage at a desired reference value V^* (i.e., $V_{dc,\,ref}$) [137]. This V^* has to be high enough to block the feedback diode conduction. Now, the actual dc link voltage (V_{dc}) is sensed and compared with the V^*. The error is processed in a PI

controller, and the output of PI controller corresponds to the magnitude of the active component of the current to be controlled. The circuit configuration of conventional three-phase active rectifier is obtained by replacing thyristors with self-commutating devices and this brings the following advantages [96, 136].

- Dynamic control of dc link voltage
- Source unity power factor
- Active and reactive power control
- Regeneration capability
- Improved source current THD
- Reduced filter size and voltage ripple.

Further, the gating pulses for switching devices are given such that the developed active rectifier delivers the desired dc output voltage (regulation of dc link voltage). To control the dc link voltage, the corresponding current should be controlled, and thus the the input ac current is to be controlled. This method of dc link voltage regulation is applicable for both single-phase and three-phase converters.

5.2.1 Control strategies

The main objective of the active rectifier is to regulate the dc link voltage, ensuring unity power factor at the ac mains. Depending on the design and application of active rectifier, there are multiple control algorithms reported. These algorithms can be broadly classified into voltage oriented control (VOC) and direct power control (DPC) [138-141].

Both VOC and DPC are motivated from field oriented control (FOC) and direct torque control (DTC) of drive (power-torque) control methods, respectively. In addition, by combining the benefits of all these control algorithms, there are various virtual flux (VF) based control algorithms such as VF-VOC and VF-DPC are reported in the literature. However, all these methods emerge from the basic platform of VOC and DPC. Both these methods have their own merits, limitations and intends to regulate dc link voltages, reduce the number of voltage and current sensors involved on the ac and dc side. Thus, various methods for implementing these control algorithms are reported and the popular methods are discussed here under.

5.2.1.1 Voltage oriented control (VOC)

VOC is the simplest classic two-loop control method reported most often [16, 32, 35, 37, 96, 136, 138-151]. The main objective of the VOC is to control the active component of the converter current (in-phase with source voltage) such that the dc link voltage tracks the reference voltage [138-141]. In this method, error between the desired and actual dc link voltage corresponds to the magnitude of active component of current that is needed to be controlled.

Further, the dc link voltages are regulated and the converter is controlled in current or voltage control mode [96, 136].

Driving a VSI as a current controlled converter, intends to control the instantaneous magnitude of source (phase) currents to ensure the dc link voltage as of the reference value. A three-phase two-level VSR with VOC using current controlled method, considering the instantaneous phase currents in stationary reference frame is reported in [136, 142, 152]. Similarly, a three-phase two-level VSR with VOC using current controlled method in rotating (*dq*0) reference frame is reported in [142-144]. Current controlled method is simpler, insensitive to parameter variations, stable and produces fast dynamic response.

To drive VSR in voltage controlled mode, the voltage (voltage drop between ac mains and converter) at the ac terminals of the converter is to be controlled, such that the converter draws currents in phase with source voltage and regulates the dc link voltage. Fig. 5.1 shows equivalent circuit diagram of VSI in voltage controlled mode [136]. This diagram represents an equivalent circuit for ideal waveforms, i.e., pure sinusoidal at the mains and pure dc voltage at the dc link. Referring to Fig. 5.1, the control is achieved by modifying amplitude and angle of voltage template $v_{k,mod}$, such that $i_k(t)$ is in phase with $v_k(t)$, where k is phase-a, b or c.

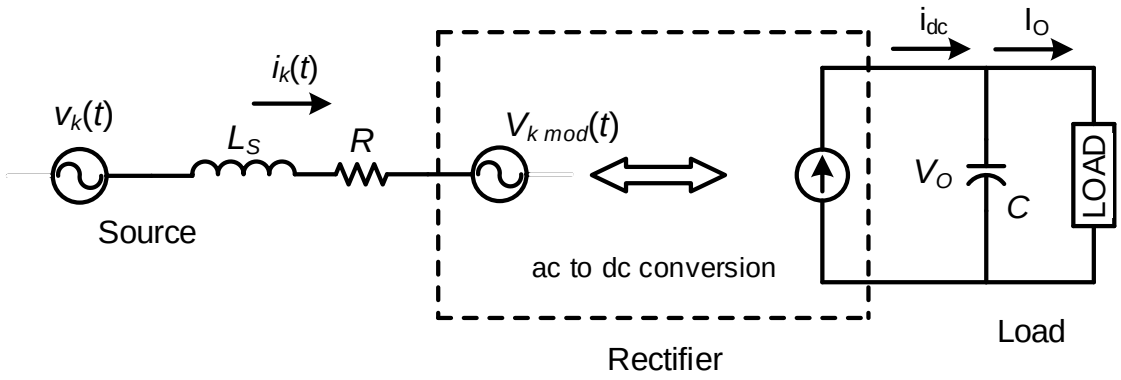


Fig. 5.1: Single-phase equivalent model of VSR in voltage controlled mode.

A three-phase two-level voltage controlled VSR with VOC, in stationary reference frame is reported in [136, 142, 145, 151]. A three-phase two-level voltage controlled converter with VOC in rotating frame of reference involving decoupled is reported in [35, 145-148]. To operate VSR in voltage control mode, the system parameters have to emulate and reproduce exact real values of source resistance and inductance (R and L_s) in power circuit. However, these parameters do not remain constant and varies with converter switching frequency and operating voltage. Thus, voltage controlled method is less stable than current controlled method.

For high power applications, front-end converters implemented with two-level converters require expensive input transformer, high device ratings, and large input and output filters. In addition, two-level converter based VSR possess limited fault tolerant ability and does not

ensure reliability with limb to home potential. With the advent of MLIs [32, 37], multilevel converter based active rectifiers gained more prominence for high power applications [16, 149]. A three-phase CHB–MLC as voltage controlled VSR with VOC using cross coupled control is reported in [35, 37, 119]. This classic two-loop control strategy (VOC) is mostly reported with coordinate transformation involving decoupled or cross coupled control [142, 146, 147, 150]. However, if the converter is required to deliver rated power, irrespective to the dc link voltage and load changes then, VOC cannot serve the purpose. Therefore, to regulate the power delivered to the converter to a desired a value, irrespective of the load condition, grid active reactive power control (GARPC) is reported [35]. GARPC is also based on instantaneous active and reactive power control [35, 153-155]. Similar to VOC, GARPC is also a two-loop control nevertheless excludes the requirement of outer voltage loop, and involves inner current controller. Further, GARPC regulates the dc link voltages such that the developed converter draws rated power at unity power factor. A CHB-MLC based three-phase active rectifier with GARPC and VOC, involving decoupled current control for BESS application is reported in [35, 119].

5.2.1.2 Direct power control (DPC)

DPC directly controls three-phase instantaneous active and reactive powers to regulate the dc link voltage (or) converter power to the reference value [156]. This single loop control method produces fast response and is well reported for two-level converter based VSR [138, 139, 143, 151, 156-159]. The basic concept of DPC is to select the best switching state (for the operating switches) among the eight possible states (two-level converter) to regulate the dc link voltage and ensure unity source power factor. Selection of switching state is carried out through a lookup table with bang-bang controllers such as hysteresis [156]. But, involvement of hysteresis controller, directs the converter to operate with variable switching frequency. A two-level VSR with DPC using SPWM and SVPWM with/without involving predictive and adaptive controllers are reported in [138, 139, 151, 157-159]. Thus, DPC involves hysteresis [143] or predictive or adaptive based controllers [138, 139, 151, 157-159] followed by PWM or look-up tables to control the converter on stationary and rotating reference frames. In general, the schematic diagram for implementing DPC control algorithm is shown in Fig. 5.2. Depending on the requirement of number of voltage and current sensors, extraction of active and reactive powers and estimation of switching states, there are various methods for implementing DPC [141, 151, 156, 158]. Though DPC is well reported for two-level VSR, practice of predictive or adaptive controllers increases the difficulty in realizing MLC based active rectifiers [138, 139, 143, 151, 157-159]. DPC for MLC based VSR is not reported in literature.

However, any control algorithm can be effective, only if the converter is able to provide adequate path for charging and discharging of dc link capacitors. An unbalance in the source voltages or any fault(s) on the converter, restricts output performance of the converter and produces unbalance in dc link voltages [116, 118, 160]. If the converter operation is in-appropriate or faulty, then its operation is restricted and results in dc link voltage unbalance. In literature, various methods are reported for diagnosis and isolation of OC switch faults. Also to obtain effective fault tolerant operation (FTO), without involving any additional hardware, various fault tolerant schemes (FTS) are reported in [115, 116, 125, 161]. Among all these FTS, NS (neutral shifting) is the most popular scheme. FTO of CHB based active rectifier with NS FTS involving PSPWM for single switch OC fault is reported in [119].

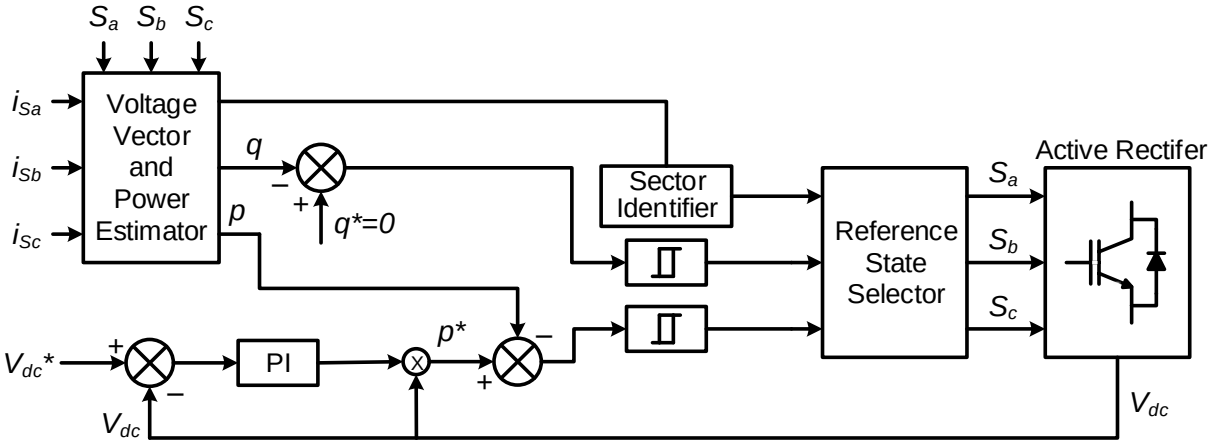


Fig. 5.2: Schematic diagram of DPC control algorithm.

5.2.2 Significance of RSC-MLC based VSR

For medium or high-voltage system, conventional voltage source PWM rectifier based front-end converter must be equipped with a transformer for galvanic isolation and voltage matching between the converter and grid. However, weight and size of the transformer is more than 50% of the overall weight and size of the power converter [32]. To address this issue, a new type of transformer based on power electronics circuits has been presented in [162] for voltage transformation, galvanic isolation, and power quality enhancements. However, this method requires additional power electronic circuits and adds to the cost of the converter.

To alleviate this problem, design of MLC based active rectifier without line frequency transformer are emerged. MLC based VSR involve multiple medium/low rated dc link capacitors in the place of bulky heavy rated dc link capacitor in two-level converter. This reduces the size and cost of the filter at both input and output side of the converter, reduces output voltage ripple, improves the input current THD, and improves regeneration capability. But, as MLCs involve multiple capacitors in the dc link, their charge/voltage balancing has

become prominent issue. Unbalance in dc link voltages, produces unbalance on converter and distorts the source currents. To obtain natural voltage balance of dc link capacitors, phase-shifted and carrier rotation PWM schemes are reported [102]. These PWM techniques operate the converter with even power distribution and thus corresponds to natural voltage balance of dc link voltages. In addition, to ensure stiff voltage balancing, cluster voltage balancing and individual voltage balancing are also incorporated in the control algorithm. Thus, the developed MLC should have redundant switching states to achieve even power distribution (equal utilization of dc link).

In addition, converter switching redundancies also play a key role in providing an alternate path to the faulty unit/switch to circulate the load current without effecting the voltage level. However, high device count of classical MLCs have led to the origination of RSC converters. The reduction in switching redundancies of RSC-MLCs increased the difficulty in obtaining equal utilization of dc link voltages. In addition, limited switching redundancies of RSC-MLCs, have restricted their fault tolerant capability such that, the conventional NS-FTS cannot directly applicable to RSC-MLCs [52, 161, 163].

Among various RSC converters, MLDCL is a profound topology with modular redundant structure. The redundant structure of MLDCL with floating dc link capacitors turns it to be an attractive alternative to CHB for regenerative front-end converters, power quality improvement and grid connected applications. When compared to CHB, a significant reduction in switch count (~36% for 15-level) can be achieved in MLDCL converter [52, 53]. However its implementation as three-phase front-end converter is not reported in the literature.

Hence by reviewing the literature, following conclusions can be drawn:

- GARPC and VOC are the popular approaches to design and control MLC based active rectifier. However, these schemes are not yet reported to RSC-MLC.
- FTO of active rectifier using NS zero-sequence injection FTS reported for CHB in [119]. However, it is not valid for compensating simultaneous failure of multiple switches.
- Effect of multiple OC switch faults on dc link voltages of RSC-MLC based active rectifier is not investigated.

Therefore, this chapter presents:

- Implementation of 3.3 kV three-phase MLDCL converter based active rectifier with VOC and GARPC algorithms, using reduced carrier rotation PWM scheme.
- Proposes a comprehensive control scheme for effective balancing of dc link voltages, in healthy and faulty (multiple OC switch faults) operating modes of the converter.

- ❖ Demonstrates the pre and post fault performance of the considered active rectifier for dynamic variation in load, change in set point references and regeneration using OPAL-RT 4500 hardware-in-loop controller.

5.3 MLDCL converter based active rectifier

Fig. 5.3 shows the circuit configuration of three-phase 15-level MLDCL based active rectifier, where, C is the dc link capacitor of each unit, R is the load resistor and L_{ac} is the coupling inductance to support the voltage difference between ac-side of the converter and grid. Operation of MLDCL to perform dc-ac conversion is presented in Chapter 2 [52, 53].

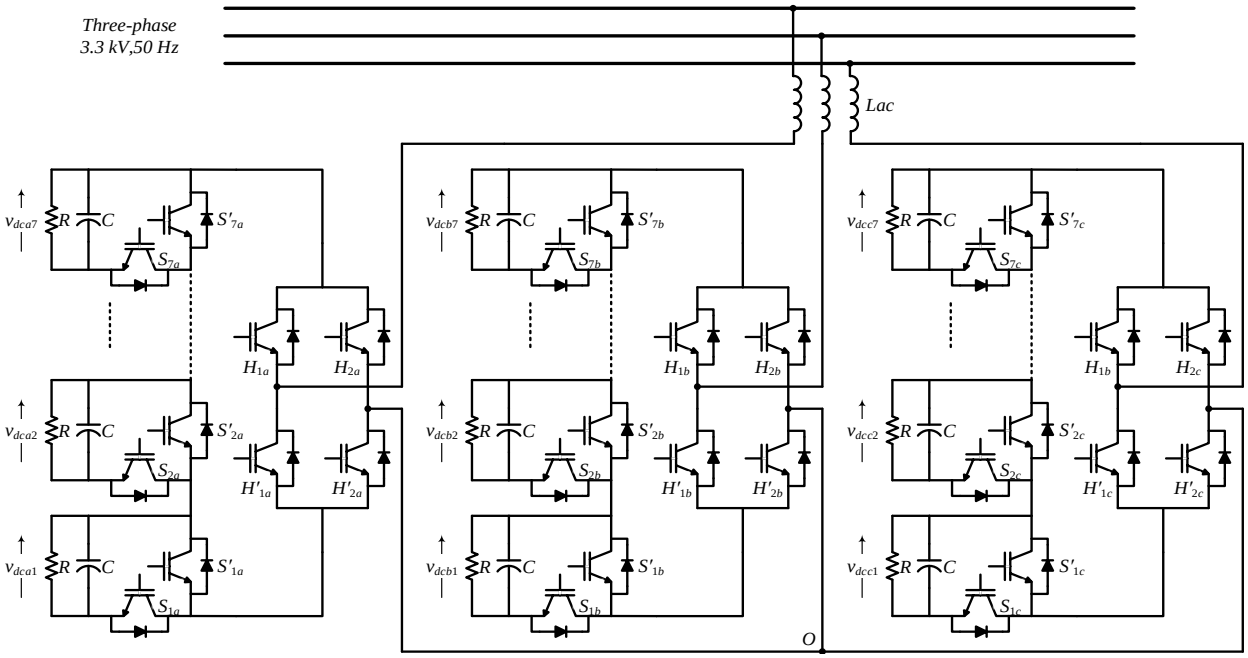


Fig. 5.3: Circuit configuration of three-phase MLDCL based active rectifier.

Polarity generator of MLDCL (shown in Fig. 5.3) consists of an H-bridge with switches operating at fundamental frequency. Level generator is formed by cascading several basic units, where each unit comprises of a dc link capacitor and a complimentary switch pair. Switching operation of the level generator is controlled such that dc link capacitor voltages are balanced. Thus, to charge these capacitors uniformly, the switching pattern should be rotated. Hence, carrier rotation PWM with proposed reduced carrier arrangement is opted. The design of system parameters such as L_{ac}, n and C are explained in next section [35].

5.3.1 Selection of dc link voltage

To design RSC-MLC based active rectifier without any line frequency transformer, let n be the cascade number, i.e., the number of dc link capacitors involved in each phase. If V_s is the grid voltage (line-voltage) and V_{dc} is the expected voltage across each capacitor, then for the proper operation of active rectifier, (5.1) should be satisfied [37].

$$V_{dc} \geq \frac{\sqrt{2}V_s}{\sqrt{3}}\frac{1}{n} \tag{5.1}$$

The relation shown in (5.1) ensures the total dc link voltage/phase of the converter must be greater than the peak of supply phase-voltage. Thus, an active rectifier never operates in over modulation and the operating modulation index (m_a) is given in (5.2). Thus for a given n and V_s, m_a reduces as V_{dc} increases.

$$m_a = \frac{1}{V_{dc}}\frac{\sqrt{2}}{\sqrt{3}}\frac{V_s}{n} \tag{5.2}$$

For example, consider an active rectifier for 3.3 kV (line-voltage) designed with fifteen-level MLDCL converter involving seven dc link capacitors per phase. Using (5.1), the minimum possible dc link voltage of each capacitor is 385 V. Thus, the minimum value of total dc link voltage is equal to 2695 V, and the system operates with $m_a = 1$. Further, for the same system, if each dc link capacitor is required to be charged for 600 V, then the total dc link voltage/phase is 4200 V and thus the converter operates with $m_a = 0.64$. However, increase in V_{dc}, increases voltage stress and blocking voltage of the operating devices.

5.3.2 Selection of coupling inductor

PWM converters generate undesirable current harmonics around the switching frequency and its multiples. If the switching frequency of the PWM converter is sufficiently high, these undesirable current harmonics can easily filtered out by coupling inductor. The coupling inductor (L_{ac}) is one of the key component that influence the performance of the active rectifier [35, 164]. The connection of the coupling inductor to the ac system is shown in Fig. 5.3. Presence of coupling inductor smoothens the converter currents and it should be selected such that is supports the voltage difference between the grid and converter. For high power ratings, coupling inductance should be 10% and source impedance should be chosen as 4% of base impedance [35]. Neglecting source impedance, coupling inductance can selected as 14% of base impedance. For the considered 3.3 kV and 1 MVA system, the determination of L_{ac} is given in (5.3) and (5.4).

The base impedance,

$$Z = \frac{\left(kV_{L-L}\right)^2}{\left(MVA_{3-\varphi}\right)} = \frac{3.3*3.3}{1} = 10.89\ \Omega \tag{5.3}$$

$$L_{ac} = \frac{0.14*Z}{2*\pi*f_s} = \frac{0.14*10.89}{2*\pi*50} = \frac{1.524}{100*\pi} = 0.0048\ \text{H} \tag{5.4}$$

Thus, coupling inductor L_{ac} in Fig. 5.3 can selected as ~5mH.

Coupling inductor L_{ac} can also be determined from the converter switching frequency (f_c) and maximum allowable current ripple ($i_{cr,(p\text{-}p)}$) as given in (5.5) [165].

$$L_{ac} = \frac{\sqrt{3}V_m}{12 * a * f_c * i_{cr(p-p)}} \text{H} \tag{5.5}$$

Where, a is overloading factor. Here, switching frequency of the converter (f_c) depends on the PWM method used for controlling the converter. Considering carrier rotation PWM involving reduced carrier arrangement at carrier frequency f_{cr} as 3 kHz, then the converter switching frequency f_c is given in (5.6).

$$f_c = n\, f_{cr} = 7 * 3000 = 21 \text{ kHz} \tag{5.6}$$

Considering 2% current ripple of base current (2% of ~175 A) i.e., 3.5 A, the switching frequency of the converter (nf_{cr}) is 21 kHz, phase-to-neutral grid voltage (V_m) = 2.6 kV and overload factor (a) = 1, the value is calculated ~5 mH as given in (5.7) and (5.8)
Thus for the considered system rating,

$$I_{base} = \frac{MVA_{3-\varphi} * 1000}{\sqrt{3} * kV_{L-L}} = \frac{1 * 1000}{\sqrt{3} * 3,3} = 174.9 \text{ A} \tag{5.7}$$

$$L_c = \frac{\sqrt{3}V_m}{12 * f_c * i_{cr(p-p)}} = \frac{\sqrt{3} * 2694}{12 * 21 * 1000 * 3.5} = 5.29 \text{ mH} \tag{5.8}$$

For a better harmonic cancellation and smoothening of current ripple, higher value of inductance is preferable. On the other hand, very high value of inductance will result in slow dynamic response of current [164]. Therefore, a compromise solution has to be found.

5.3.3 Selection of dc link capacitor

The rating of the capacitor C (in farads) gives its available energy W (in joules) as follows [35, 164-167], where, $V_{dc\text{-}max}$ and $V_{dc\text{-}min}$ are (in V) are the maximum and minimum capacitor voltages due to the ripple, respectively.

$$W = \frac{1}{2} C \left(V_{dc\max}^2 - V_{dc\min}^2 \right) \tag{5.9}$$

From the principles of energy transformation, equation (5.9) can be written as (5.11) [165]

$$\frac{1}{2} C_{dc} \left(V_{dc,ref}^2 - V_{dc,\min}^2 \right) = \frac{P_{3-\phi}}{3n} * a * t \tag{5.10}$$

Where, C_{dc} is capacitance of each basic unit (in farads), $P_{3\text{-}ph}$ is total power rating of the active rectifier, a is over loading factor (considered as 1) and t is response time of the active rectifier [165, 167].

$$C_{dc} = 2\frac{P_{3-\phi} * a * t}{3n\left(V_{dc,ref}^2 - V_{dc,\min}^2\right)} \tag{5.11}$$

Considering, t = 1500 μs, V_{dc} = 650 V and 4% ripple in dc capacitor voltages in (5.11), C_{dc} is obtained as 4312 μF as given in (5.12).

$$C_{dc} = \frac{2*1000*1000*1500*10^{-6}}{3*7*\left(650^2 - \left(0.04*650^2\right)\right)} = \frac{3000}{21*\left(33124\right)} = 4312\ \mu\text{F} \tag{5.12}$$

5.3.4 Comprehensive control algorithm

Active front-end converter (active rectifier) aims to regulate the dc link voltages by ensuring the source unity power factor and thus incorporates an efficient controller along with appropriate PWM (to regulate dc link voltages). This controller produces modulating signals as per the set point reference, which are further fed to the PWM block to generate the gating pulses to drive the converter. Most often carrier based PWM schemes such as LSPWM with carrier rotation, or PSPWM are opted as their switching pattern facilitates the converter to operate with equal utilization of dc link (flexible dc link balancing). However, these schemes cannot be applicable to the topologies with limited redundancies such as RSC-MLCs. Thus, this work considers modified reduced carrier PWM with carrier rotation.

Hence, in this section a comprehensive control algorithm is proposed to control the developed MLDCL based active rectifier, tracking the set-point reference in healthy and faulty operating conditions. The proposed control algorithm has the proficiency to compensate simultaneous OC faults on multiple switches and contribute stiff and uniform balance of dc link capacitors as per the set-point reference. The proposed controller uses voltage averaging method and supports implementation of VOC and GARPC control algorithms. The major control blocks of the proposed comprehensive control algorithm are:

1. Decoupled current control
2. Voltage balancing control (cluster and individual voltage balancing)
3. Fault tolerant control followed by modified reduced carrier PWM with carrier rotation.

Fig. 5.4 shows the schematic block diagram of the proposed comprehensive control algorithm. In Fig. 5.4, $v_{s,abc}$ are the instantaneous three-phase voltages, $i_{s,abc}$ are the instantaneous three-phase currents, V^* (or V_{dc}^*) is the set point reference (dc link voltage) in VOC, P^* is the set point reference (demand active power) in GARPC and Q^* reactive power reference (assumed to be zero as to maintain unity power factor at source terminals). As the considered converter is of 15-level, each phase possess seven dc link capacitors. Thus, sensing voltage across all the dc link capacitors and averaging them with respective each phase (cluster),

obtains mean cluster voltage $v_{dc,a}$ $v_{dc,b}$ $v_{dc,c}$. Further, averaging these mean cluster voltages i.e., $v_{dc,a}$ $v_{dc,b}$ $v_{dc,c}$, gives their overall mean $v_{dc,}$ as shown in Fig. 5.4. Schematic implementation of the developed comprehensive control algorithm shown in Fig. 5.4 is, as follows:

Instantaneous voltage of each dc link capacitor is controlled to track their respective cluster mean (individual voltage balancing), each cluster mean is controlled to track their overall mean (cluster voltage balancing) and, then overall mean (mean of average voltage of all clusters) is controlled to track the voltage to be regulated across each dc link (decoupled current control).

The output voltage signals obtained from decoupled current controller (v_{Da}, v_{Db} and v_{Dc}), cluster voltage balancing (v_{Ca}, v_{Cb} and v_{Cc}) and individual voltage balancing (v_{Ia}, v_{Ib} and v_{Ic}) are added and normalized to obtain modulating signals (v_{ma}, v_{mb}, and v_{mc}). These normalized modulating signals are further processed through fault tolerant control block to obtain fault tolerant modulating signals v_{ma}*,v_{mb}*, and v_{mc}*.

In the developed comprehensive controller, *n* is the number of dc link capacitors in each phase and, *x*, *y* and *z* are the number of OC faults in phase *a*, *b* and *c* respectively. The obtained fault tolerant modulating signals operated with reduced carrier PWM scheme with carrier rotation to produce gating pulses to control the switching action of the converter. Detailed explanation for implementation of each these control blocks is explained here under

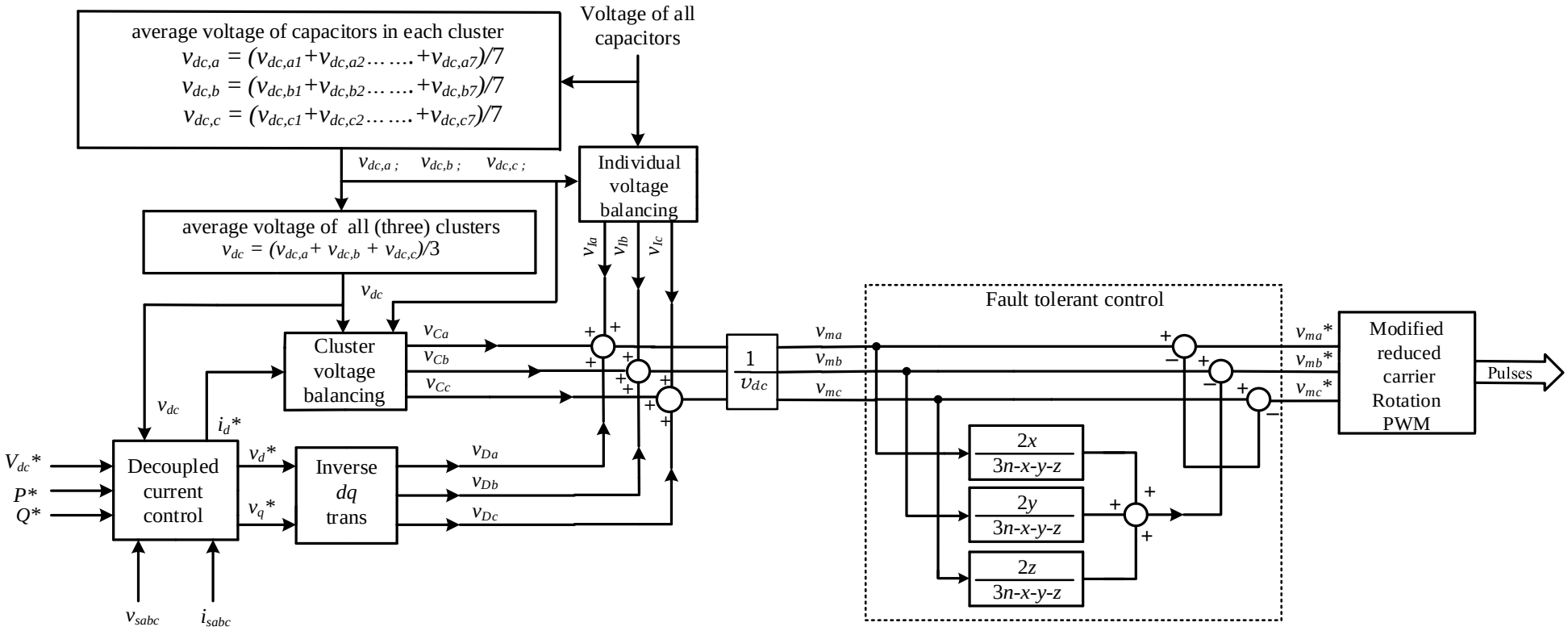


Fig. 5.4: Block diagram of proposed comprehensive control.

5.3.4.1 Decoupled current controller

The objective of decoupled current controller shown in Fig. 5.5 is to generate voltage controlled modulating signals for the desired specifications by controlling the supply active and reactive current components. The sensed v_{sabc} and i_{sabc} are transformed to synchronously rotating reference frame (dq) using Park's transformation. Thus, the d-axis and q-axis, voltage and current components v_{sd} and v_{sq} and, i_{sd} and i_{sq} are extracted. The decoupled current controller generates the voltage controlled modulating signals by controlling the i_{sd} and i_{sq}, such that they track their reference current i_d* and i_q*. Thus to regulate dc link voltage as of the desired value, decoupled current controller controls the active component of current drawn by the converter i_d to track i_d*. The methodology for implementing this control block is nearly same for both GARPC and VOC, however the difference lies in extraction of i_d* as shown in Fig. 5.5.

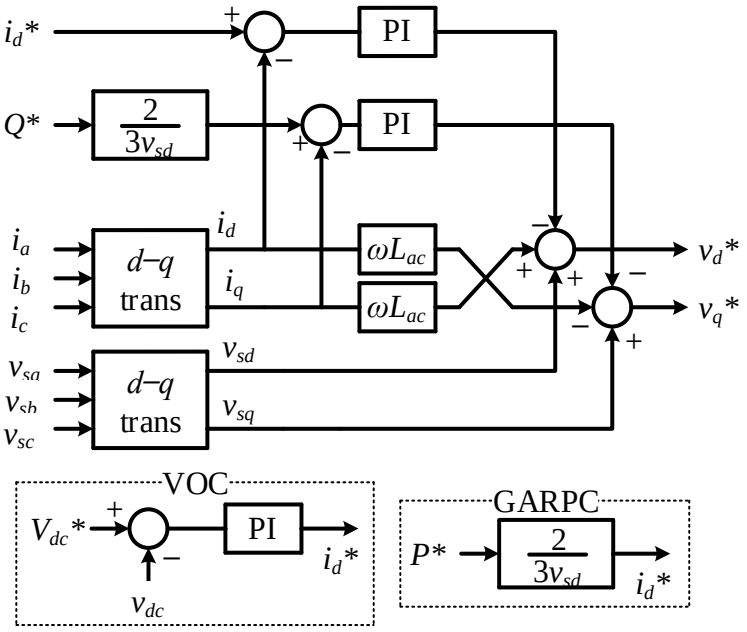


Fig. 5.5: Schematic diagram of decoupled current controller.

In detail, VOC intends to regulate dc link voltage as of the desired (rated) value and thus extracts i_d* from outer dc voltage regulator. In detail, the error between V* ($V_{dc,ref}$) and v_{dc} corresponds (after process though a PI controller) to the active/d-axis component of the reference current i_d*. On the other hand, GARPC anticipates to control the voltage across the dc link capacitors such that they deliver a set point rated power (P*) to load. Thus i_d* in GARPC can be directly extracted from P* and v_{sd} as shown in Fig. 5.5. For the considered work, to ensure unity power factor, q* is assumed to be zero. In both VOC and GARPC, the error between reference and actual currents of direct and quadrature axis are operated with cross coupled controller, and produce control signals v_d*, v_q* as shown in Fig. 5.5 [35]. Further, the obtained v_d*, v_q* are operated with inverse parks transformation to obtain the control signals v_{Da}, v_{Db} and v_{Dc} as shown in Fig. 5.4.

These output control signals v_{Da}, v_{Db} and v_{Dc} correspond to the modulating signals for driving the converter to track set point reference i.e., voltage or power.

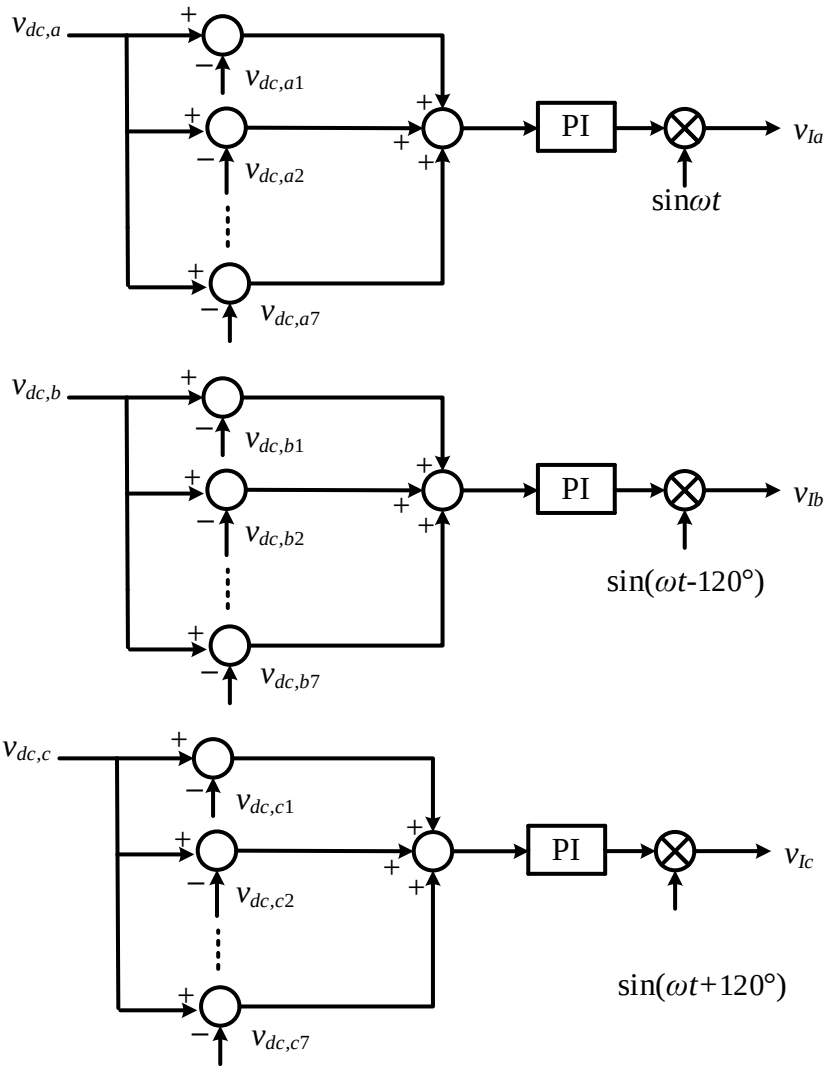
5.3.4.2 Voltage balancing controller

To achieve stiff balancing of dc link voltages, cluster and individual voltage balancing circuits are incorporated adapting averaging method. Schematic diagram of individual and cluster voltage balancing circuit of the considered 15-level MLDCL based active rectifier is shown in Fig. 5.6(a) and (b) respectively.

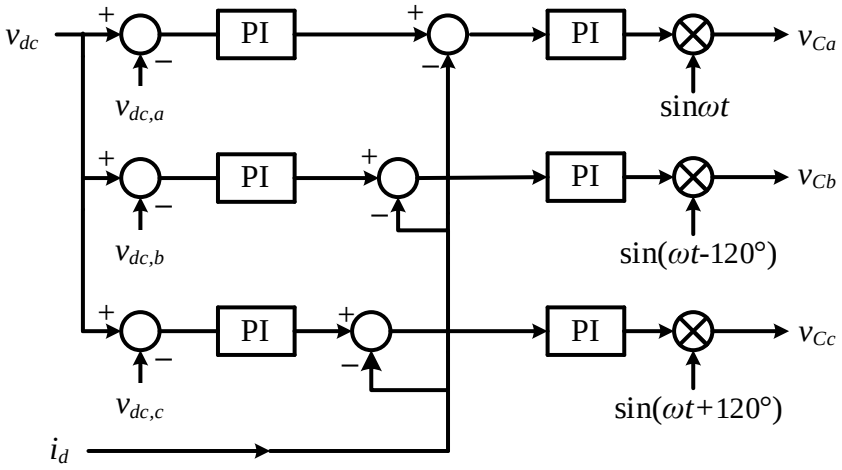
Individual voltage balancing circuit, controls the voltage across each capacitor to follow mean voltage of the respective cluster. Consecutively, this ensures the voltage balance among the dc link voltages of the respective cluster. For example, in Fig. 5.3, if $v_{dc,k1}$, $v_{dc,k2}$… $v_{dc,k7}$ are the instantaneous voltage across each capacitor of cluster- k and, $v_{dc,k}$ is the average voltage of cluster-k, where $k = a$, b and c phase respectively. Individual voltage balancing controller controls the error between $v_{dc,k\,1\ldots4\ldots7}$ and $v_{dc,k}$, such that i.e., $v_{dc,k1\ldots4\ldots7}$, follows v_{dck} respectively as shown in Fig. 5.6(a). The error between the voltage of each dc link capacitor and its respective cluster mean are processed through a PI controller. The output of PI controller corresponds to the voltage template to control the error between each dc link voltage and mean voltage. Further, this voltage template is multiplied with unit vector of respective cluster. This produces control signals to drive the converter, such that voltage of each dc link capacitor follow their respective cluster mean. This ensures the voltage balance among the dc link voltages of an individual cluster.

Further, to establish the balance among the dc link voltages of one cluster with respect to the other cluster, cluster voltage balancing is incorporated. Fig. 5.6(b) shows the block diagram for implementing cluster voltage balancing controller. Here, v_{dc} is the mean of $v_{dc,a,}$ $v_{dc,b}$ and $v_{dcc,}$ where $v_{dc,a,}$ $v_{dc,b}$ and $v_{dc,c,}$ are the mean voltage of cluster a, b and c respectively. Error between v_{dc} and $v_{dc,k}$ (where $k = a$, b and c respectively) is processed through a PI controller, and the output of PI corresponds to the active component of the current required to control the voltage error stiffly. Thus, operating it with i_d, and further processing the error through another PI controller, produces voltage template. This voltage template is multiplied by the unit vectors of the respective phase to produce the control signals i.e., v_{Ca}, v_{Cb} and $v_{Cc,}$ which can obtain stiff balance among dc link voltages of all clusters. Further to drive the converter, to track the set-up reference variable with stiff balance of dc link voltages, the control signals obtained from individual voltage balancing i.e., v_{Ia}, v_{Ib} and v_{Ic} and, cluster voltage balancing v_{Ca}, v_{Cb} and v_{Cc} are added to the output of decoupled current controller i.e., v_{Da}, v_{Db} and v_{Dc} as shown in Fig. 5.4. Further, to normalize the obtained modulating signals over the range of n, a gain factor of $1/v_{dc}$ is included, where n is the number of dc link capacitors in each phase. This obtains the normalized modulating signals v_{ma}, v_{mb}, and v_{mc} which are further passed

through fault tolerant control block to obtain fault tolerant modulating signals v_{ma}*, v_{mb}*, and v_{mc}* as shown in Fig. 5.4.



(a) Individual voltage balancing



(b) Cluster voltage balancing

Fig. 5.6: Block diagrams of individual and cluster voltage balancing controllers.

5.3.4.3 Fault tolerant control

Referring Chapter 4, with *x*, *y* and *z* faulty units on phase *a*, *b* and *c* respectively, on a converter with *n* units/phase, a voltage component $\frac{2}{3n-x-y-z}$ multiplied by number of faulty units of respective phase is added to the voltage controlled signals v_{ma}, v_{mb}, and v_{mc}, as shown in Fig. 5.4. Addition of this voltage component modifies the magnitude and angle of v_{ma}, v_{mb} and v_{mc}, and produce new set of normalized modulating signals v_{ma}*, v_{mb}*, and v_{mc}*, which tolerate the appeared fault and contribute to balanced sources currents and dc link voltages. If the converter is healthy, i.e., $x = y = z = 0$, injected voltage component is zero and thus $v_{mk} = v_{mk}$*, where $k = a, b$ and *c* respectively. The obtained fault tolerant modulating signals v_{ma}*, v_{mb}* and v_{mc}* are operated with proposed modified reduced carrier PWM with carrier rotation.

Controlling the switching action of the converter with the obtained normalized fault tolerant modulating signals v_{ma}*, v_{mb}*, and v_{mc}* regulates the dc link voltages to meet the set point reference even in faulty conditions. Further, to generate the gating pulses to control the switching action of the converter, proposed reduced carrier PWM with carrier rotation is opted. For the considered converter with seven dc link capacitors, seven unipolar level shifted carriers are required as shown in Fig. 4.10.

5.3.5 Relation between dc link voltage and load power

In GARPC, to deliver the rated power (*P**), the power delivered by each basic unit (P_{dc}) is given in (5.13).

$$P_{dc} = \frac{P^*}{3n} \tag{5.13}$$

Following (5.13), the expected voltage across the each capacitor (V_{dc}) is given in (5.14), where *R* is the load on each unit.

$$V_{dc} = \sqrt{\frac{R\,P^*}{3n}} \tag{5.14}$$

If each capacitor charges to V_{dc}, then the expected phase-voltage across *n*-level converter is $nV_{dc}m_a \sin\omega t$. However, the coupling inductance (L_{ac}) is tuned such that it supports the voltage difference between the converter and three-phase supply. Neglecting the drop across the inductor, the total power of each phase should be equal before and after the coupling inductance as is given in (5.15). Therefore, modulation index (m_a) can be defined as given in (5.16). For linear operation, m_a of the considered active rectifier should not be greater than unity (5.16) i.e., nV_{dc} should be greater than V_m.

$$nV_{dc}\, m_a \sin(\omega t)\, i_a = V_m \sin(\omega t)\, i_a \tag{5.15}$$

$$m_a = \frac{V_m}{nV_{dc}} \tag{5.16}$$

In GARPC as the reference variable P^* increases, then to meet to the power demand, i_d also increases, which further increases V_{dc} as shown in (5.12). Thus following V_{dc}, v_{dc} increases and m_a reduces. Similarly, if P^* decreases, then i_d and v_{dc} decreases, and m_a increases. In a similar way, as V^* is the reference variable in VOC, increase in V^* increases $v_{dc,}$ which further increases i_d^* and P_{dc}. Similarly, if V^* decreases, then i_d, v_{dc}, and P_{dc} decreases, and m_a increases. During regenerative braking, both these control algorithms ensures reversal power flow with phase opposition between source current and source voltage.

5.4 MLDCL based active rectifier for healthy condition

To validate the above control algorithms, a 15-level MLDCL based three-phase active rectifier is developed in real-time with OPAL-RT 4500 controller and results are discussed for variations in load and reference parameters in this section. Real-time implementation of 3.3 kV, 50 Hz 15-level MLDCL based active rectifier with VOC for dynamic variation in load and reference variable are shown in Fig. 5.7 and Fig. 5.8 respectively. Similarly, performance of the considered converter with GARPC algorithm is shown in Fig. 5.9 and Fig. 5.10. Each result is recorded for a period time of 0.6 s for the considered simulation parameters shown in Table 5.1.

Table 5.1: Simulation parameters.

Parameter			**Value**	
Line-voltage (RMS)			3.3 kV	
Supply frequency			50 Hz	
Coupling inductance (L_{ac})			5 mH	
DC link capacitance (C)			4300 μF	
Sample time (T_s)			20 μs	
Switching frequency (f_{cr})			3 kHz.	
PI Parameters			Kp	K_i
Decoupled current controller	GARPC	Inner loop	50	1
			50	2
	VOC	Inner loop	20	2
		outer loop	0.5	25
Cluster voltage balancing			0.1	1
Individual voltage balancing			0.1	1
Regenerative voltage			1.125 V_{dc}	
Regenerative resistance			3 Ω	

To validate the converter response for dynamic variation in load, the reference variable in VOC i.e., V^*, and GARPC i.e., P^* are set at 600 V and 200 kW respectively. In order to study the performance, the following events are assumed to occur in the system.

- At t = 0 s, a load of R =20 Ω is connected across each capacitor unit.
- At t = 0.2 s, a series RL load of 25 Ω and 15 mH is added.
- At t = 0.4 s, last added RL load is removed.

To validate the converter response for dynamic variation in reference variable, a load of R = 25 Ω is considered. The considered events in simulation study are:

- At t = 0 s, V^* is set at 600 V in VOC and P^* at 300 kW in GARPC.
- At t = 0.2 s, V^* = 450 V and P^* = 170 kW.
- At t = 0.4 s, regenerative operation is initiated.

5.4.1 Response with VOC

Performance of converter with VOC, for dynamic variation in load is shown in Fig. 5.7. Referring to $0 < t < 0.2$ s in Fig. 5.7, it is observed that, V^* = 600 V with R = 20 Ω, delivers a power (P_{dc}) of 18 kW to each load to charge each dc link capacitor to V^* as given in (5.14). This operates the converter with m_a = 0.64 from (5.16), and delivers a total load power of P_c = 378 kW. Further, increase in load impedance at t = 0.2 s, reduces load current and load powers P_{dc} and P_c, to regulate voltage of each dc link tracking V^*. As dc link voltage unchanged, m_a remains to be at 0.64. At t = 0.4 s, load current increases, which increases P_{dc} and ensures dc link voltage to be regulated. Further, Fig. 5.7 verifies unity power factor (UPF) operation under all loading conditions.

The ability of VOC to track dynamic variation in reference variable is shown in Fig. 5.8. From $0 < t < 0.2$ s of Fig. 5.8, it can be inferred that to charge each dc link capacitor to 600 V for the given load of 25 Ω, P_{dc} =14.4 kW, P_c = 302 kW and m_a = 0.64 is maintained. Reducing V^* to 450V at t = 0.2 s, reduce the magnitude of load and source currents such that, voltage across each dc link capacitor (V_{dc}) track the new reference voltage V^*, i.e., 450 V. Thus, reduces P_{dc} and P_c to 8.1 kW and 170 kW respectively, and operates the inverter at m_a = 0.87.

The regeneration capability of converter with VOC algorithm, can be analysed referring to Fig. 5.8 from t = 0.4 s. Regenerative mode of operation is initiated at t = 0.4 s, maintaining V^* at 450 V. Its corresponding change in converter operation can be verified by observing current reversal $i_{s\text{-}abc}$, power flow reversal in P (–170 kW) and phase opposition of v_{sa} and i_{sa}, ensuring UPF.

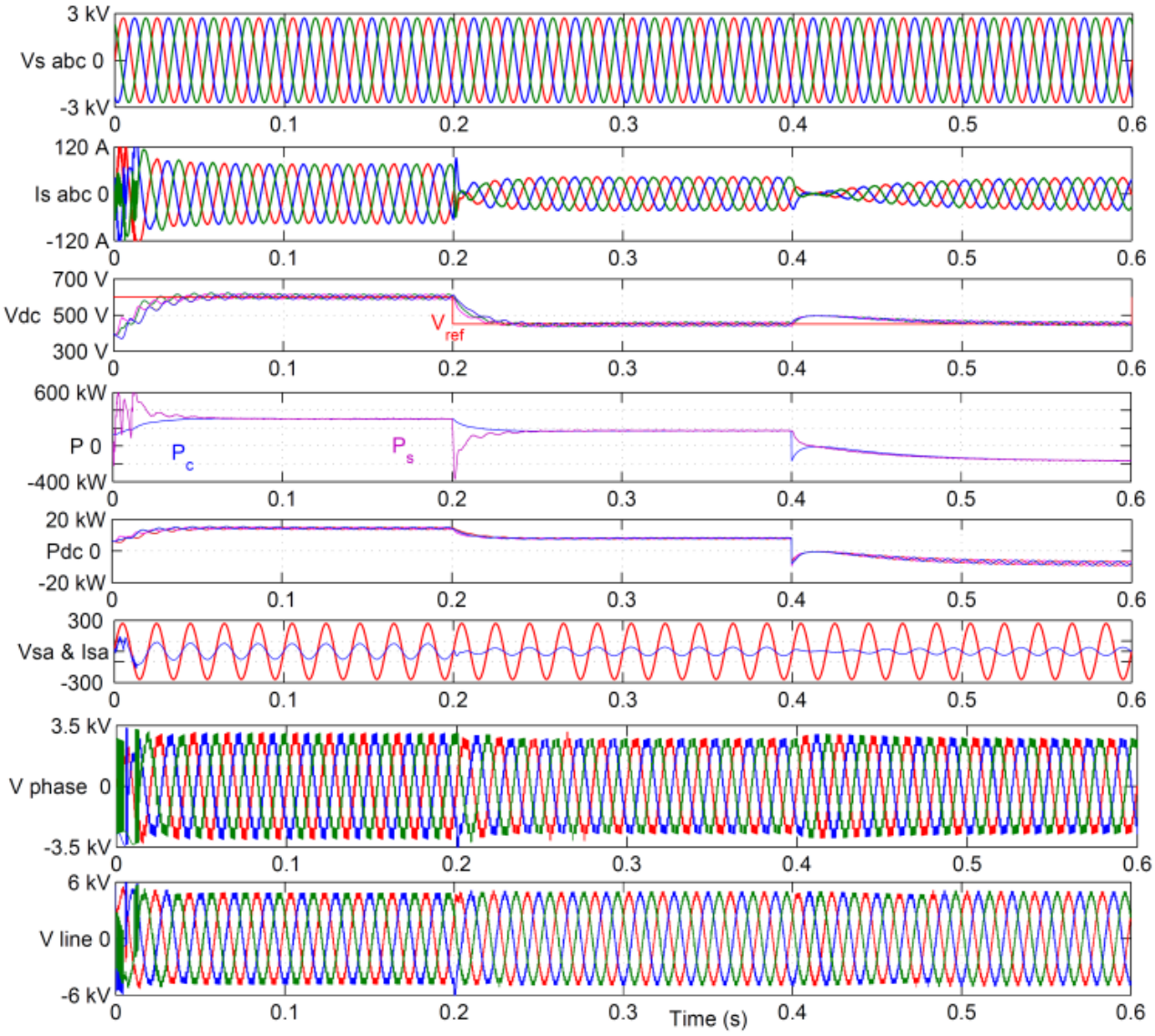


Fig. 5.7: Performance of MLDCL based active rectifier with VOC for dynamic variation of load.

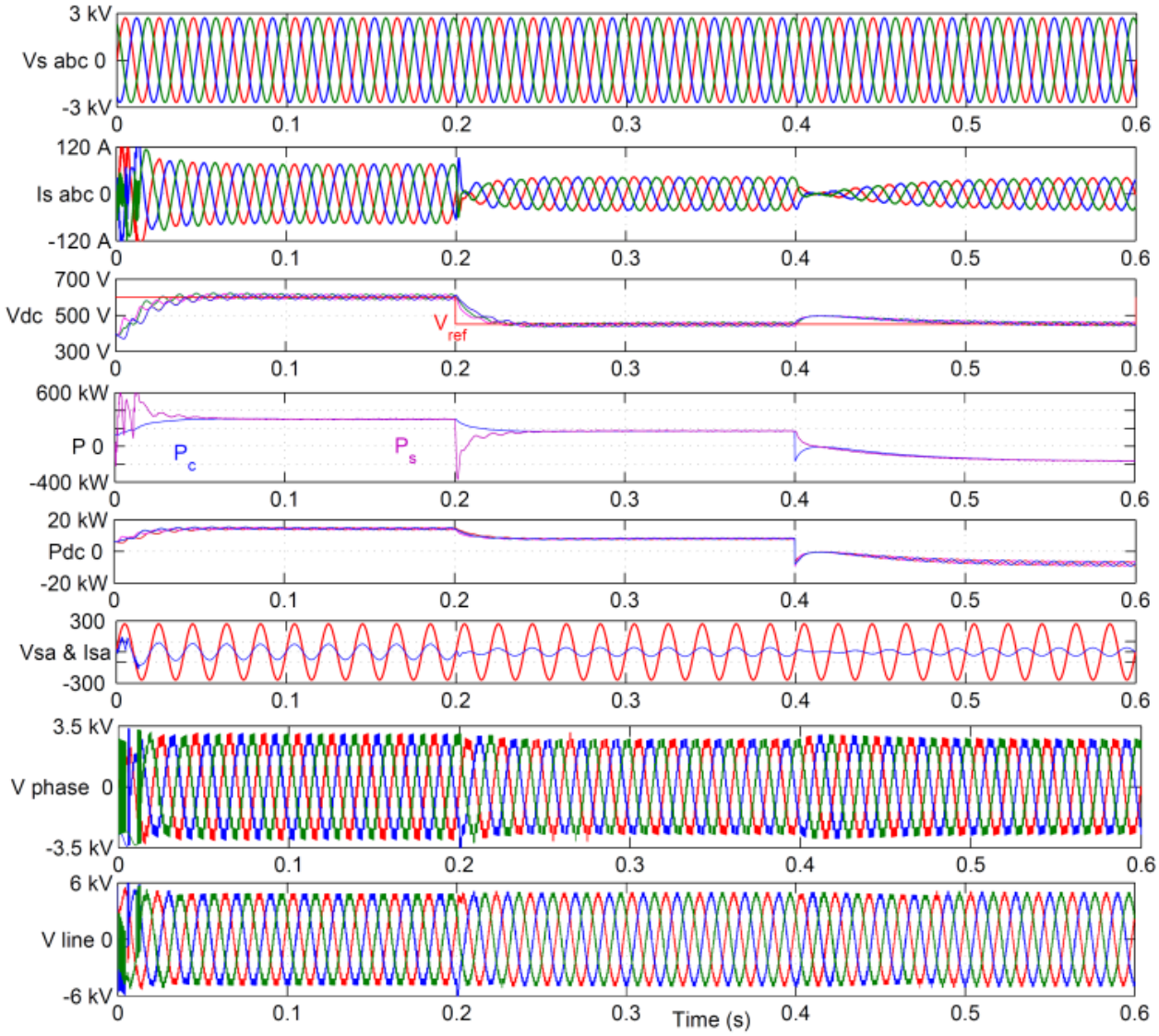


Fig. 5.8: Performance of MLDCL based active rectifier with VOC for dynamic variation of reference variable.

5.4.2 Response with GARPC

The efficacy of GARPC algorithm in regulating P^*, irrespective to the load condition is analysed in Fig. 5.9. Observing $0 < t < 0.2$ s of Fig. 5.9 shows that, for a load of $R = 20\ \Omega$, each dc link capacitor charges to 436 V (operates the converter at $m_a = 0.88$) and produces $P_{dc} = 9.5$ kW to ensure $P^* = 200$ kW. With the increase in load impedance at $t = 0.2$ s, dc link voltage increases to 656 V and reduces m_a to 0.58, to ensure load current and load power invariant. Once the additional load is removed at $t = 0.4$ s, dc link voltages reduce to 436V and m_a increases to 0.88.

The ability of GARPC algorithm in tracking the dynamic variation in reference power is shown in Fig. 5.10. From Fig. 5.10, up to 0.2 s, it can be inferred that to ensure $P^* = 300$ kW, each dc link capacitor charges to 597 V, and delivers a power output of 14.2 kW, operating at $m_a = 0.58$. At $t = 0.2$ sec, with decrease in P^* to 170 kW, dc link voltage reduces to 449 V, m_a increases to 0.85 and power delivered to each load (P_{dc}) is reduced to 8 kW. Reduction in v_{dc} from 597 to 449

V, increases m_a from 0.64 to 0.85, which can be observed from last two traces of Fig. 5.10. However, in both cases the converter operates with unity power factor, which can be observed from v_{sa} and i_{sa}.

The regeneration capability of converter with GARPC algorithm can be analysed by referring Fig. 5.10 from t = 0.4 s, by changing P^* to –170 kW. Its corresponding change in operation can confirmed by power reversal, current ($i_{s\text{-}abc}$) reversal, phase opposition of v_{sa} and i_{sa} and, regulation of dc link voltages (at 450 V). Thus, the current and power reversal with UPF and regulating the dc link voltages verifies the regenerative breaking operation of the converter.

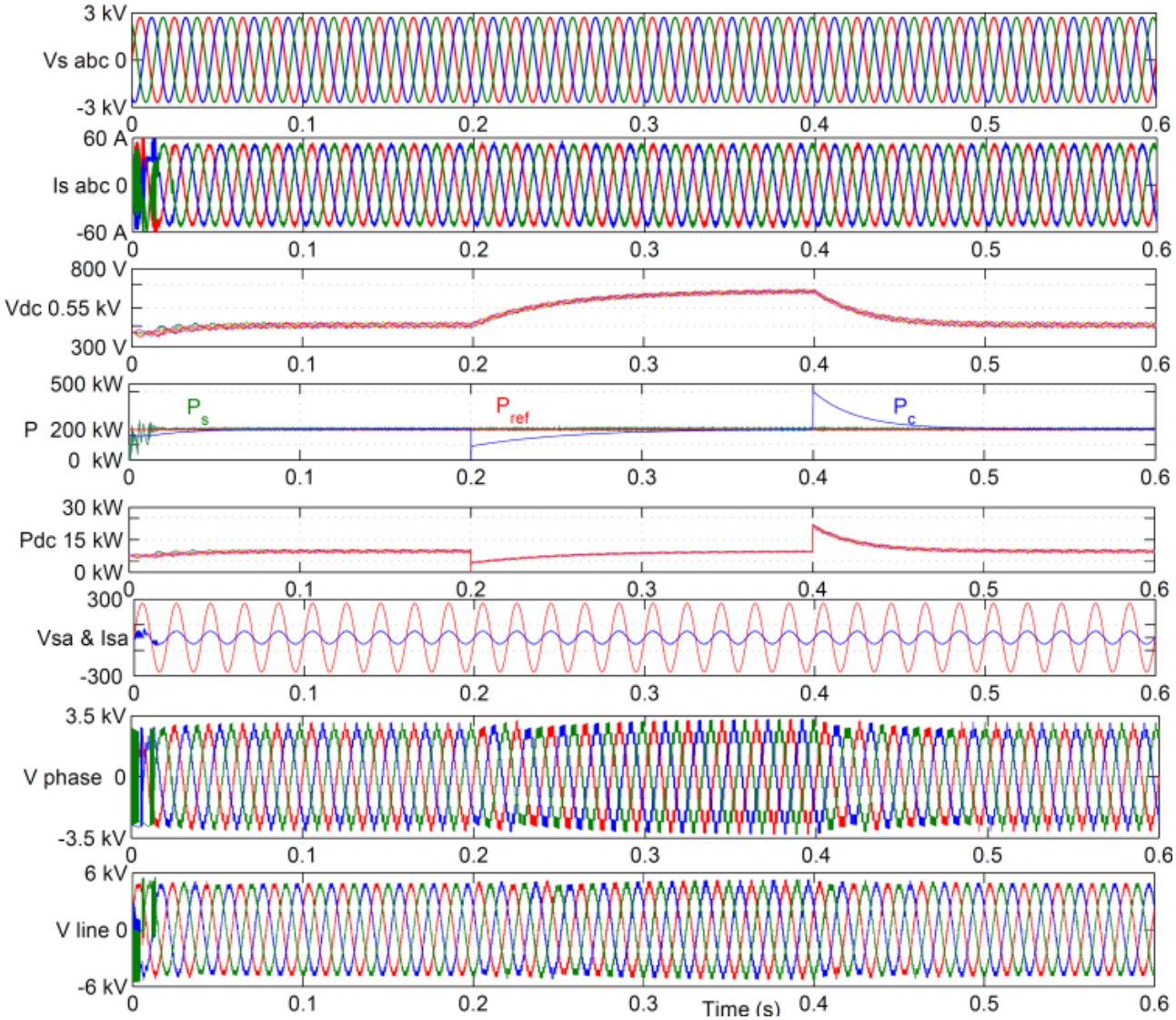


Fig. 5.9: Performance of 15-level MLDCL based active rectifier with GARPC for dynamic variation in load.

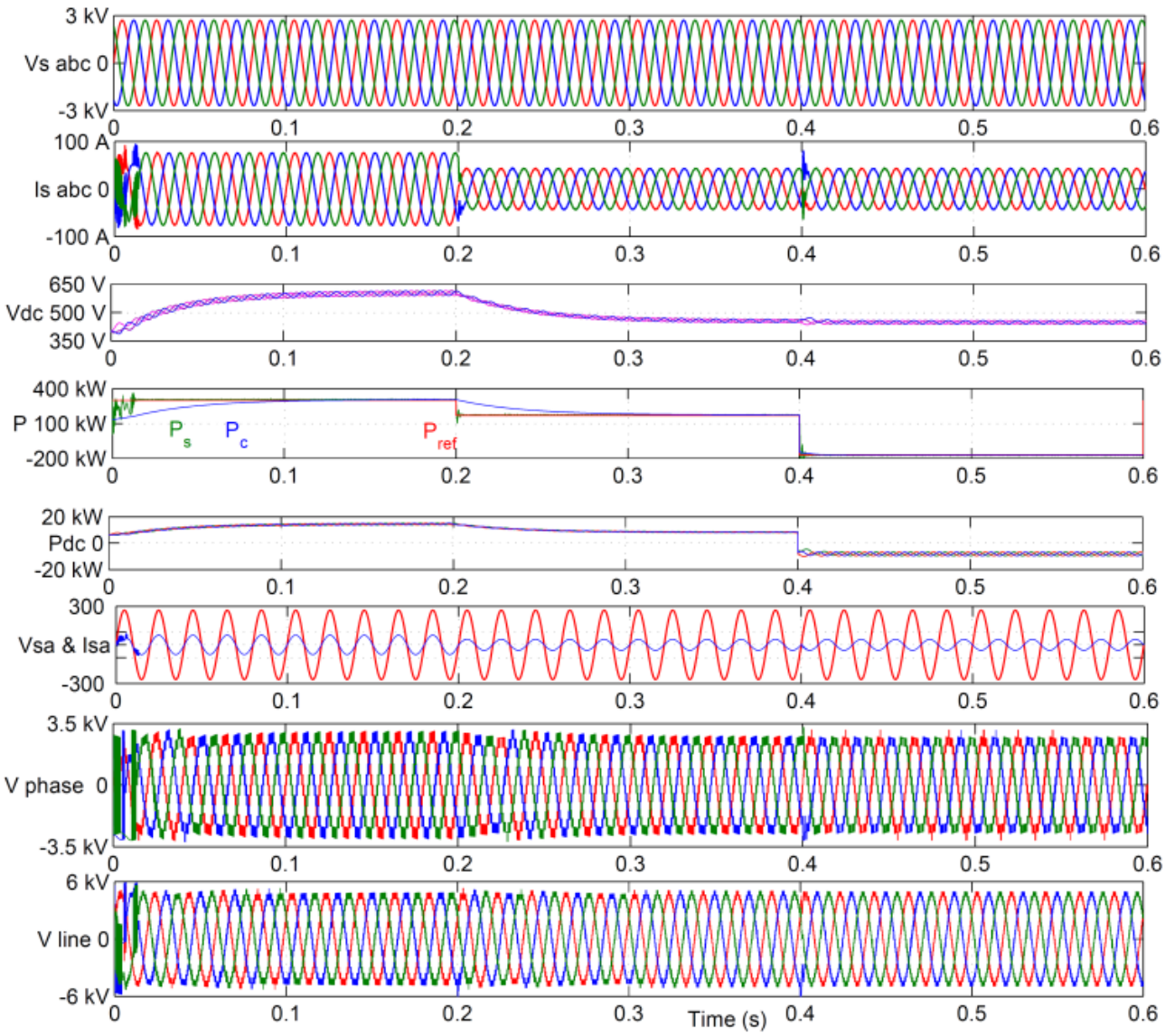


Fig. 5.10: Performance of MLDCL based active rectifier with GARPC for dynamic variation in reference variable.

5.4.3 Performance observations of VOC and GARPC

Observing the overall performance of the considered active rectifier with VOC and GARPC, the following points can concluded.

- Both VOC and GARPC are vice-versa. In detail, for identical system parameters, if opting V^* as 600 V in VOC, delivers ~300 kW of load power, then opting P^* as 300 kW in GARPC, charges each dc link capacitor to ~600 V.
- In GARPC as current reference i_d^* is obtained from P^* (which is constant), currents i_{sabc} reaches steady state earlier than capacitor voltages. Similarly, in VOC as V^* is the command signal and i_d^* is obtained by the error between the actual dc voltage and desired dc voltage, steady state in capacitor voltages reaches earlier than the currents i_{sabc} and power 'P'.

Reduction in power command P^* or voltage command V^*, will result increase in the m_a of the obtained modulating signals, however, it should be noted that considered command signal P^*

or V^* should ensure that the total dc link voltage/phase is greater than the peak of the supply phase voltage.

5.5 MLDCL based active rectifier for multiple OC switch faults.

This section investigates the fault tolerant capability of 15-level MLDCL based active rectifier for multiple OC switch faults on converter using generalized NS zero-sequence injection FTS. Implementation of generalized NS-FTS to extract fault tolerant modulating signals from GRAPC/VOC algorithms is shown with dashed lines in Fig. 5.4. In this fault tolerant method, a zero-sequence component in multiple of respective phase faulty units, is injected into pre-fault modulating signals of each phase i.e., v_{ma}, v_{mb} and v_{mc} to obtain fault tolerant modulating signals v_{ma}^*, v_{mb}^* and v_{mc}^*. Addition of this zero-sequence component, modifies the magnitude and angle of post fault modulating signals such that they can obtain balanced and regulated dc link voltages with uniform burdening, even though the number of dc link capacitors are different on each phase. Further the obtained fault tolerant modulating signals v_{ma}^*, v_{mb}^* and v_{mc}^* are operated with modified reduced carrier rotation PWM scheme.

To evaluate the fault tolerant ability of the considered active rectifier with seven operating units in each phase, a case study of five faulty units with three faulty units in phase-*a*, two faulty units in phase-*b* and no faulty units on phase-*c* is considered i.e., $n = 7$, $x = 3$, $y = 2$ and $z = 0$. Further, in phase-*a*, unit-5, 6 and 7 and in phase-*b*, unit 6 and 7, are assumed as faulty. Fig. 5.11 and Fig. 5.12 shows the pre-fault and post-fault performance of the considered active rectifier with VOC and GARPC algorithms respectively. At $t = 0.4$ s, the above multiple faults are occurred, and at $t = 0.6$ s, the fault tolerant operation is initiated. The results are demonstrated with OPAL-RT real-time controller with $V^* = 600$V in VOC and $P^* = 300$ kW in GARPC.

5.5.1 Performance with VOC

Pre and post-fault preference of the considered active rectifier with VOC control algorithm is shown in Fig. 5.11. For the considered load, in pre-fault operating mode, charging each dc link capacitor to 600 V, delivers a total load power i.e., P_c of ~302.2 kW. This is depicted in Fig. 5.11, for 0.3 s to 0.4 s. Occurrence of fault on the converter at $t = 0.4$ s, disturbs the converter creating unbalance in dc link. This leads to unbalance on the converter phase and line-voltages, distorts the currents and produces non-uniform power distribution among the operating units. To achieve FTO of the converter, at $t = 0.6$ s, generalized NS zero-sequence injection FTS is initiated. With initiation of FTS, dc link voltage of healthy unit tends to charge towards reference voltage V^*, with converter drawing balanced sinusoidal currents at UPF. However, it is observed that magnitude of source currents and active power P_c reduces (from ~302 kW to ~230 kW). This is due to the faulty units

which does not contribute any power. However, the dc link voltage of healthy units follows V^* i.e., 600 V.

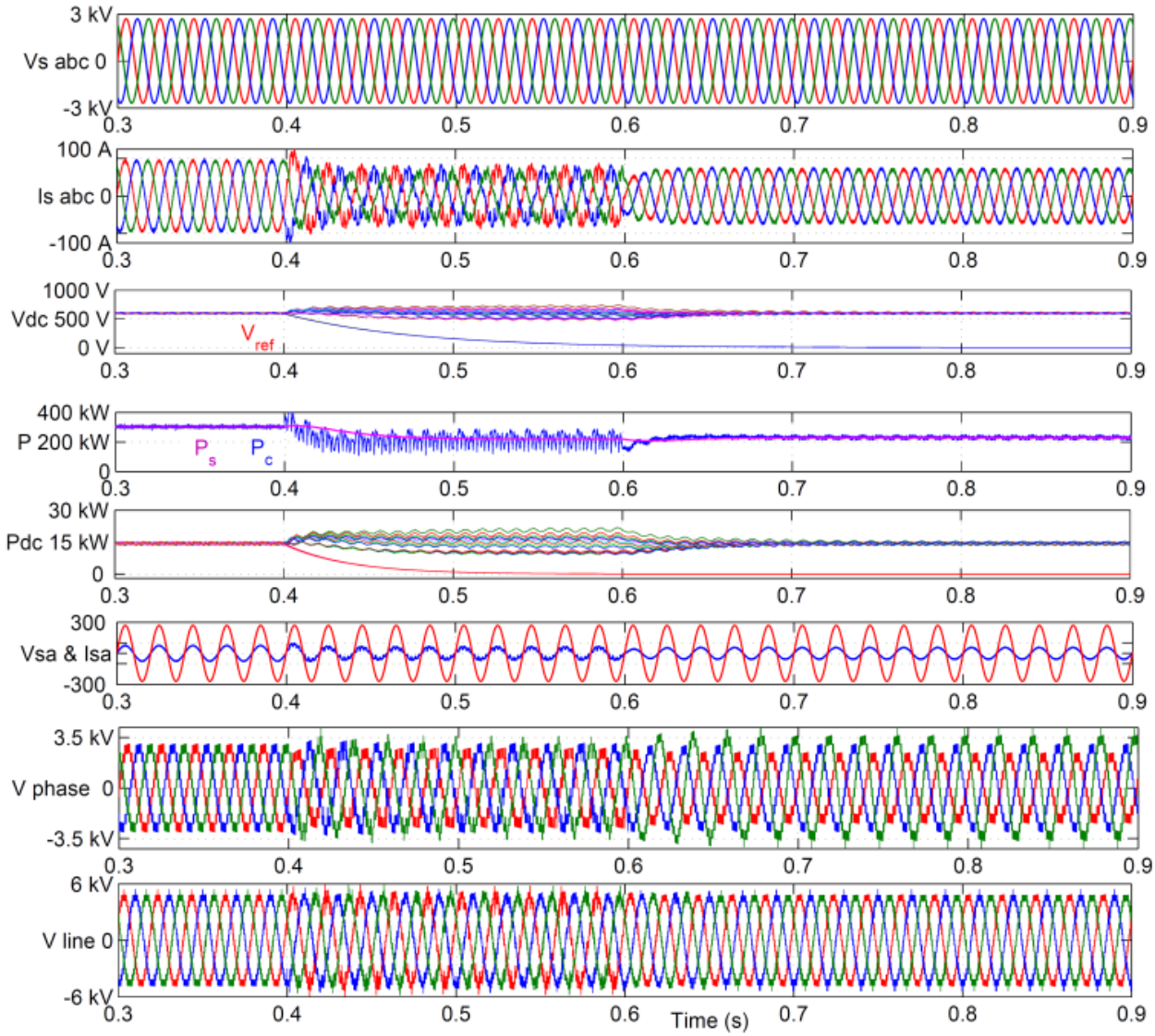


Fig. 5.11: Pre and post-fault performance of MLDCL based active rectifier with VOC algorithm.

If the number of operating units on all phases are different, each phase operates with different m_a. Thus for the appeared fault, in FTO, as four units are operating in phase-*a*, with 600 V across each capacitor, m_a of phase-*a*, should be greater than one, i.e., 1.36 (5.16). This drives the converter to over modulation, and the FTO cannot synthesized. However, this is not happening due to the addition of v_{oz} . Injection of v_{oz} to $v_{m,abc}$ produces $v_{m,abc}^*$, with modulation index m_a^*. In phase-*a*, injection of v_{oz} modifies pre-fault modulation index m_a, i.e., 0.64 to m_a^*, i.e., 0.87, and appropriate analysis for the above statement is given in (5.17).

$$
\left.
\begin{aligned}
m^{*}_{a,(a-ph)} &= \frac{\sqrt{3}n\sqrt{3(n-x)^2+(y-z)^2}}{(3n-x-y-z)(n-x)}m_a = \frac{7\sqrt{3}\sqrt{3(4)^2+(2)^2}}{64} * 0.64 = 0.87 \le 1 \\
m^{*}_{a,(b-ph)} &= \frac{n\sqrt{9(-n-x+y+z)^2+3(-3n+x+3y-z)^2}}{2(3n-x-y-z)(n-y)}m_a \\
&= \frac{7\sqrt{9(-8)^2+3(-12)^2}}{160} * 0.64 = 0.88 \ \le \ 1 \\
m^{*}_{a,(c-ph)} &= \frac{n\sqrt{9(-n-x+y+z)^2+3(3n-x+y-3z)^2}}{2(3n-x-y-z)(n-z)}m_a \\
&= \frac{7\sqrt{9(-8)^2+3(20)^2}}{224} * 0.64 = 0.84 \ \le \ 1
\end{aligned}
\right\} \quad (5.17)
$$

5.5.2 Performance with GARPC

Fig. 5.12 shows the pre and post-fault performance of 15-level MLDCL based three-phase active rectifier with GARPC algorithm. Under healthy condition, to a deliver a reference total load power of 300 kW. Under this condition, the converter operates at m_a = 0.64 and each capacitor in dc link charges to 597 V and delivers a power output of 14.4 kW. At t = 0.4 s, with multiple OC faults, the operation of active rectifier disturbs and become unbalanced.

With the initiation of NS FTS at 0.6 s, a zero-sequence voltage component corresponding to the fault condition is added to the pre-fault modulating signals. This generates new set of modulating signals corresponding to m_a*, as given in (5.17). Operating these fault tolerant modulating signals with the carrier rotation PWM (rotating carriers only among the healthy units and seizing the carrier rotation among faulty units) and seizing the gating pulses to the faulty switches, converter restores the balanced operation with UPF, which can be verified from Fig. 5.12. It is to be noted that in pre-fault condition, all the operating units i.e., 3*7 = 21, together contribute to P*, where as in post-fault condition only healthy units i.e., 16, contribute to P*. Therefore to meet the required power demand of P* in post fault condition, the power contributed by each healthy unit (P_{dc}) is increased to 18.75 kW. However, the magnitude of i_{dref} remains same as P* is same. Thus, to maintain P_c as P* in FTO, voltage across each dc link capacitor is boosted to 684 V.

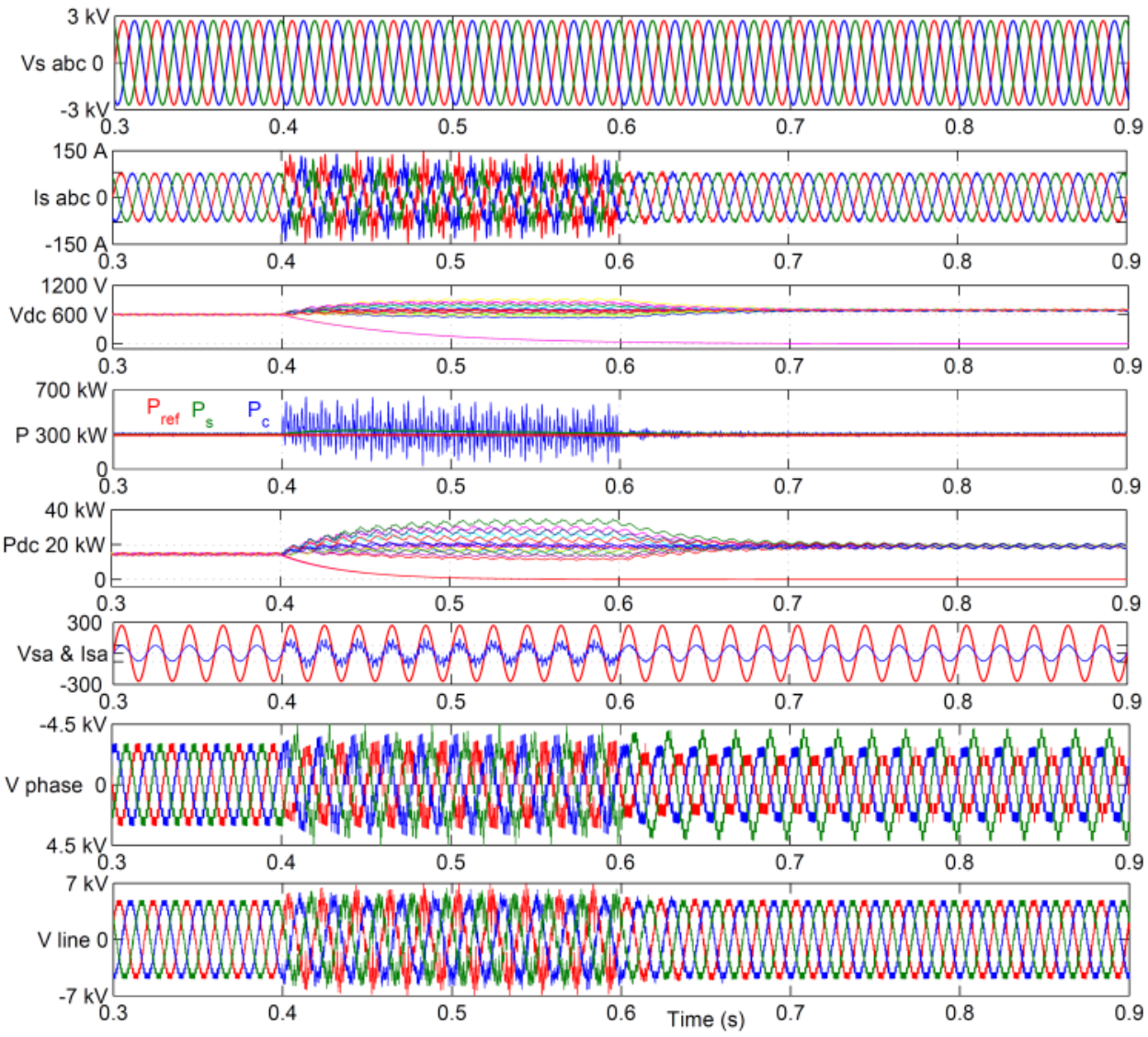


Fig. 5.12: Pre and post-fault performance of MLDCL based active rectifier involving GARPC algorithm.

However, operating the converter with VOC or GARPC, to compensate the appeared fault satisfactorily, the modulation index m_a* of the fault tolerant modulating signals should in linear range. Therefore, to obtain effective FTO, a few constraints on the pre-fault m_a and the expected dc link voltage should be considered, as given in (5.18). The constraints given in (5.18) presents the limits of dc link voltage to operate converter in linear modulation range during FTO.

$$\begin{aligned} V_{dc,a-ph} &\geq \frac{\sqrt{3}n\sqrt{3(n-x)^2+(y-z)^2}}{(n-x)(3n-x-y-z)}\frac{V_m}{n} \geq 525.75 \text{ V} \\ V_{dc,b-ph} &\geq \frac{n\sqrt{9(-n-x+y+z)^2+3(-3n+x+3y-z)^2}}{2(n-y)(3n-x-y-z)}\frac{V_m}{n} \geq 534.5 \text{ V} \\ V_{dc,c-ph} &\geq \frac{n\sqrt{9(-n-x+y+z)^2+3(3n-x+y-3z)^2}}{2(n-z)(3n-x-y-z)}\frac{V_m}{n} \geq 337.89 \text{ V} \end{aligned} \tag{5.18}$$

In detail (5.18) refers that, for the considered fault condition, dc link capacitors in phase-*a* should be operated such that the voltage across each capacitor is greater than 525 V. Similarly, minimum acceptable voltage limit of each capacitor in phase-*b* and *c* are 534.5 and 337.8 V respectively. Hence, the reference variable *P** or *V** can be tracked, only if the voltage of each capacitor is greater than the minimum limit in all phases as given in (5.18). Following this, the operating modulating index will be less than one and an effective FTO is feasible.

5.6 Summary

FTO of converter plays a vital role in defining the reliability of three-phase active rectifier. This chapter analysed the pre and post fault performance of MLDCL based three-phase active rectifier by adopting VOC and GARPC algorithms. Initially, the performance of the considered active rectifier for healthy operating conditions is demonstrated for the regenerative operation, dynamic variation in command signal and load. Further, the performance of the considered active rectifier for simultaneous failure of multiple units in converter is investigated. The prominence of the proposed generalized NS-FTS in restoring balanced operation is demonstrated on OPAL-RT 4500 real-time simulator The obtained results ensures its fault tolerant capability.

CHAPTER 6: CONCLUSION AND FUTURE SCOPE

The main conclusions of the presented work and possible future research have been summarised in this chapter.

6.1 Conclusion

This thesis investigated the features, limitations, modulation schemes and fault tolerant ability of various RSC-MLI topologies. The key conclusions of this thesis are given here under.

- This thesis initially investigated the effect of reduction in switch count of RSC-MLIs on its topological structure, operation and switching logic realization. A qualitative and quantitative features of RSC-MLI topologies have been discussed and a comparison has been made so as to facilitate a well-informed selection of topology for a given application. Based on this study, it is observed that multilevel dc-link (MLDCL) inverter possess modular structure with appreciable reduction in switch count, adequate switching redundancies and fault tolerant ability. Further, it is observed that MLDCL serves as viable alternate to CHB MLI for applications such as grid connected PV system, active front-end applications, custom power devices, BESS, and HEV. Owing to this features, MLDCL RSC-MLIs is considered to analyse the fault tolerant ability and closed-loop implementation.
- To control RSC-MLIs, the carrier based modulation schemes such as LSPWM and PSPWM are directly applicable. This is due to the reduction in switch count and variations in the topological structures as compared to MLIs. Therefore to control RSC-MLIs, novel carrier based modulation schemes such as multi reference, reduced carrier and switching function PWM are reported. This thesis explored the limitations of these schemes in terms of generalization to higher levels, scalability, line-voltage THD performance and computation burden. Therefore, to control any RSC-MLI topology, irrespective to the voltage ratios and topological arrangement, a modified reduced carrier PWM with unified logical expressions is proposed. The generalized nature of the proposed switching logic and THD performance is verified with Simulink and experimental studies on various RSC-MLI topologies. Further, comparison with state-of-the-art schemes reported in the literature in terms of computational burden on controller, extension to higher-level and THD performance verified the superiority of proposed method.
- Another aspect to select the inverter topology is the ability to work in fault prone conditions. The faults on inverter will restrict the phase-voltage levels and produce unbalance in line-voltage and currents. The reduction in switch count of RSC-MLI has reduced the probability of fault occurrence as compared to MLI. However, the extreme reduction in switching redundancies restricted fault tolerant ability of RSC-MLIs. Nevertheless, the fault tolerant

operation (FTO) is feasible for modular and redundant topologies such as MLDCL. In general, the fault tolerant schemes (FTS) generates a new set of modulating signals to reconfigure the inverter to achieve FTO. The demerits of conventional fault tolerant methods such as by-passing, increasing burden, neutral shifting (NS) and neutral shifting with zero-sequence injection FTS are discussed in terms of power sharing among basic units and failure of multiple switches. Therefore, to compensate multiple OC faults with uniform power sharing among the basic units, a generalized neutral shifting zero-sequence injection FTS is proposed in this thesis. The inverter is controlled with the proposed modified reduced carrier PWM scheme and to achieve uniform burden among healthy operating units, the carriers are rotated at the end of each carrier time period. The proposed mathematical equations for obtaining the modified modulating signals to achieve FTO for a given fault condition are validated on fifteen-level MLDCL RSC-MLI in MATLAB/Simulink environment. The experimental studies presented on nine-level MLDCL inverter corroborated the simulation results in terms of balanced line-voltages and equal power sharing among basic units.

- The effectiveness of the proposed PWM and fault tolerant schemes are further analysed on closed-loop applications. For this, a 1 MVA, 3.3 kV three-phase fifteen-level MLDCL based active rectifier is considered. The active rectifier is controlled by (a) voltage oriented control (VOC) and (b) grid active reactive power control (GARPC). Therefore, a comprehensive control scheme is proposed by incorporating VOC/GARPC with the proposed fault tolerant scheme. The rectifier is controlled by proposed modified reduced carrier PWM scheme with carrier rotation. The demonstrated pre and post-fault performance of the considered active rectifier for dynamic variation in load, change in set-point references, regeneration using OPAL-RT 4500 simulator verified the effectiveness of the proposed comprehensive controller. The control scheme can extended to other applications such as UPS, BESS and ASD.

6.2 Future scope

The research work presented in this thesis discloses a number of issues that could be further investigated.

- Development of new modulation schemes for asymmetrical RSC-MLI topologies to achieve capacitor voltage balance and uniform power distribution among dc sources.
- Though the proposed FTS is implemented on MLDCL inverter, its feasibility can verified on other RSC-MLI topologies.
- Implementation of FTS to RSC-MLI with advanced modulation schemes such as space vector modulation (SVM).

- Development of a comprehensive control algorithm to diagnosis and compensate OC faults on RSC-MLI topologies can be developed.
- Implementation of RSC-MLI based active rectifier for energy storage or battery charging application.
- Development of a comprehensive control scheme by using non-linear controllers such as predictive and adaptive to compensate converter faults in closed-loop applications.

APPENDIX A: EXPERIMENTAL SETUP

The system hardware and interfacing with dSPACE MicroLabBox and OPAL-RT 4500 simulator for the laboratory prototype models have been described in detail to validate the simulation results.

Introduction

To verify the viability and effectiveness of the proposed PWM and fault tolerant schemes, the following experimental studies are performed in the laboratory.

1. Development of two generalized inverter modules and implementing proposed PWM scheme on various thirteen-level asymmetrical RSC-MLI topologies using dSPACE MicroLabBox.
2. Development of nine-level MLDCL RSC-MLI topology with two generalized inverter modules and implementing proposed fault tolerant scheme on inverter by using OPAL-RT 4500 controller.
3. Development of fifteen-level MLDCL based active front-end converter using voltage oriented control (VOC) and grid active reactive power control (GARPC) on OPAL-RT 4500 simulator.

Development of generalized inverter modules

In order to verify the proposed PWM schemes on various RSC-MLI topologies with different voltage levels, two generalized inverter modules are developed. Each of this module consists of 24 isolated IGBTs (IKW40T120, 40 A and 1200 V). Each IGBT is equipped with a snubber circuit, pulse amplification circuit, driver circuit, an isolation circuit and a separate heat sink. A gate signal of 5 V is required to trigger each IGBT. The three terminals of IGBT are available at outside of the module for purpose of connecting with other IGBTs to develop the required inverter topology. The photograph of front panel of the inverter modules are shown in Fig. A.1.

To avoid shoot-through problem and obtain safe turn-on and turn-off of the IGBTs, a dead band circuit shown in Fig. A.2 is designed, with a delay time of 1 μs. The delay time between complementary switches is introduced by a *RC* integrator circuit as shown in Fig. A.2. The different switching signals obtained experimentally for complementary switch pair are shown in Fig. A.3 with 1 μs delay.

The required isolated dc sources for inverter are obtained from regulated power supplies. The ratings of regulated power supplies are (i) 30 V and 3 A dual channel and (ii) 30 V and 5 A single channel. A three-phase star-connected 1 kW 0.85 power factor lagging load is developed. To record and store the inverter output waveforms such as line-voltages, phase-voltages and line-currents, a

four-channel digital storage oscilloscope and four-channel digital phosphor oscilloscope are used. A current probe is used measure current.

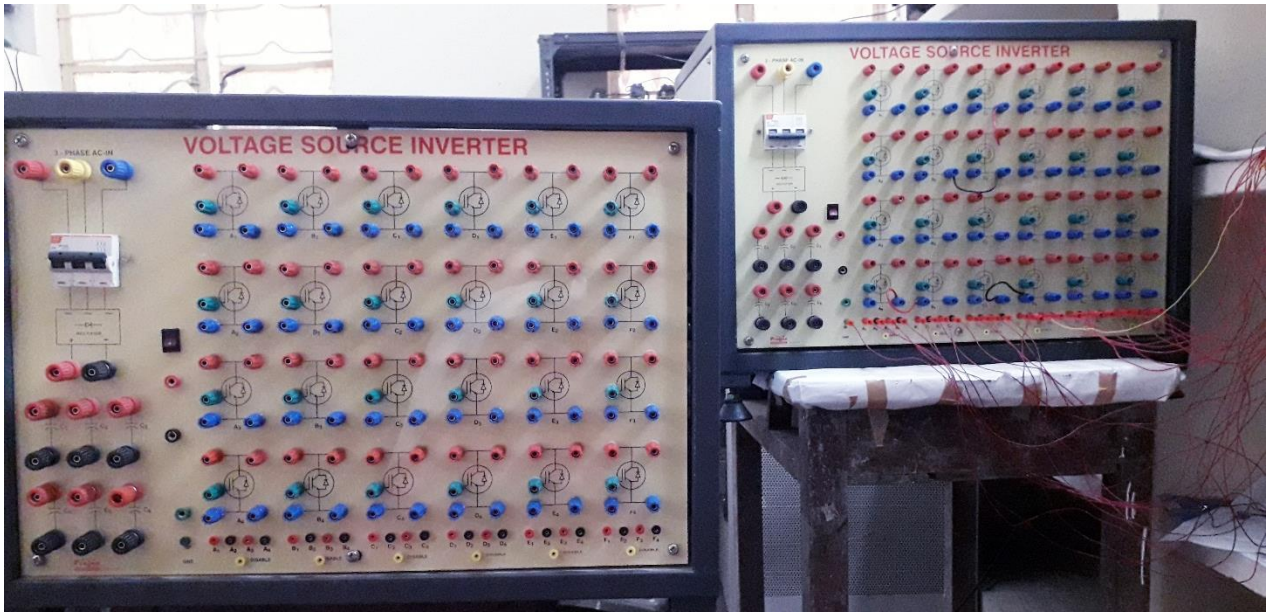


Fig. A.1: 24 switch IGBT inverter modules.

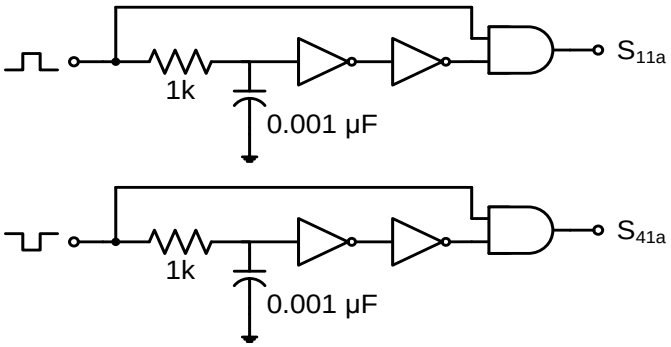


Fig. A.2: Dead-band circuit for a complementary switch pair.

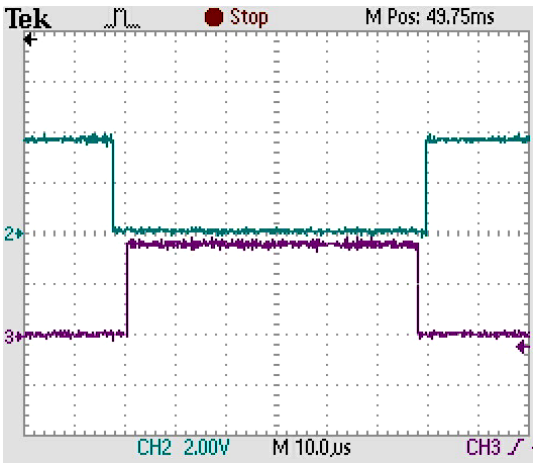


Fig. A.3: Firing signals for complementary switch pair with dead-band circuit.

Interfacing inverter with dSPACE MicroLabBox RTI1202 R&D controller

The inverter control circuit i.e., the PWM technique is developed in dSPACE MicroLabBox and is described here under.

Historically, control software was developed using assembly language. In recent years, industry began to adopt MATLAB/Simulink and Real-Time Workshop (RTW) platform based method such as dSPACE, provides a more systematic way to develop control software. Fig. A.4 shows the total development environment (TDE) of dSPACE.

dSPACE MicroLabBox is an all-in-one prototyping unit for the laboratory that combines compact size and low system costs with high performance and versatility. dSPACE MicroLabBox RTI1202 consists of 2 GHz dual-core real-time processor and user-programmable FPGA (Xilinx® Kintex®-7 XC7K325T) with more than 100 channels of high-performance I/O with easy access via integrated connector panel. MicroLabBox is supported by a comprehensive dSPACE software package, i.e., Real-Time Interface (RTI) for Simulink® for model-based I/O integration and the experiment software ControlDesk, which provides access to the real-time application during run time by means of graphical instruments.

By using Real-Time Workshop (RTW) of MATLAB and Real-Time Interface (RTI) feature of dSPACE-RTI1202, the Simulink models of the various PWM schemes of the inverter prototypes are implemented. The control algorithm is first designed in the MATLAB/Simulink software. The RTW of MATLAB generates the optimized code for real-time implementation. The interface between MATLAB/Simulink and FPGA of RTI1202 in dSPACE allows the control algorithm to be run on the hardware. The generated gate pulses are available at digital I/O of dSPACE-RTI1202 shown in Fig. A.5. These gate pulses are given to inverter via dead-time circuit shown in Fig. A.6. The photograph of complete experiment is shown in Fig. A.7.

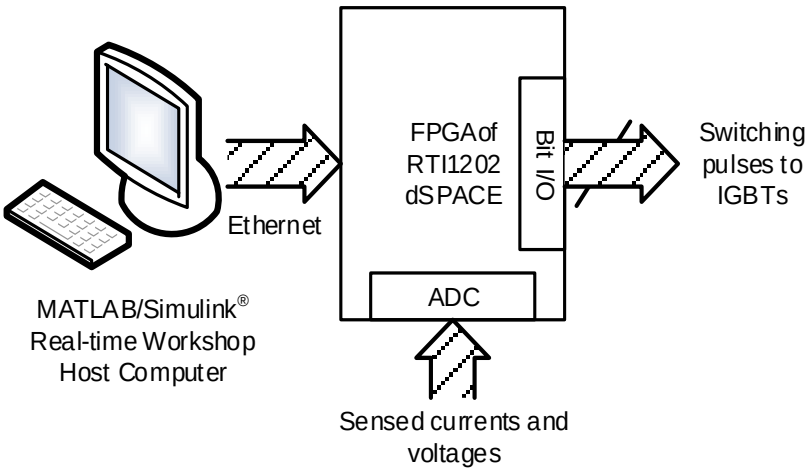


Fig. A.4: DSP (dSPACE-RTI1202) circuit board interfacing.

Fig. A.5: Digital I/Os of dSPACE-RTI1202 controller.

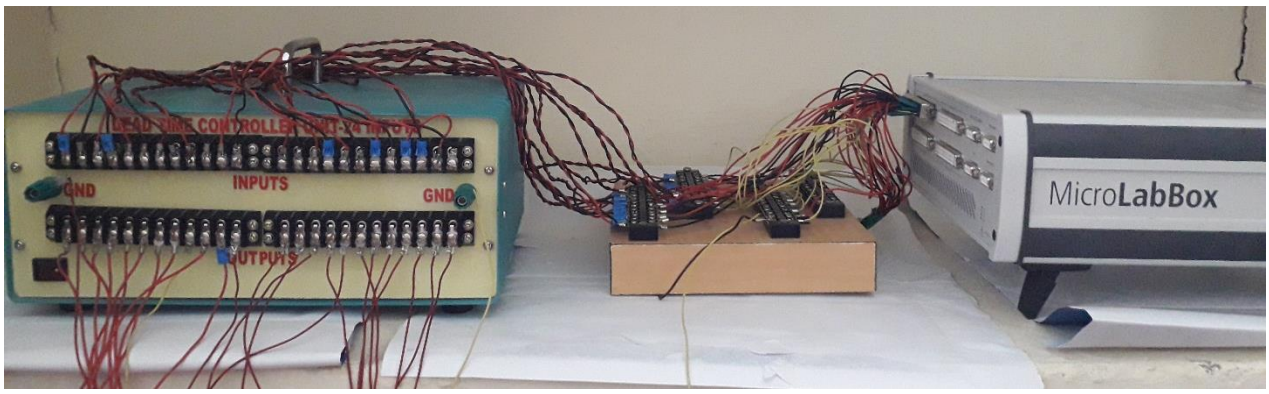


Fig. A.6: Digital I/Os of dSPACE-RTI1202 controller.

Fig. A.7: The experimental set-up with dSPACE RTI1202 controller.

Control of nine-level MLDCL RSC-MLI using OPAL-RT 4500 controller

To validate complex topologies and control strategies, a digital hardware-in-the-loop (HIL) simulator exhibits great advantage over a traditional analog test stand in terms of cost and flexibility. Validating, testing, designing and modelling of a closed-loop system with digital HIL real-time simulation tool involves two simulators, where one working as a plant and other working as a controller. This real-time tool possess multiple analog and digital I/O ports for commutating the data from external plant to simulator or external controller to simulator or from one simulator (plant) to other simulator (controller). The plant system along with its interface, generates analog signals according to the operating conditions which will be acquired by controller through communication channel. The controller system generates necessary control actions according to the selected control scheme. -

Among the various real-time simulation tools, OPAL–RT 4500 real-time simulator is an appreciable solution to validate controls of medium-voltage power converters. OPAL-RT possess a powerful multi-processor real-time computer with fast and reconfigurable I/O system based on field programmable gate array (FPGA) firmware with graphically designed Xilinx signal generator toolbox under Simulink environment and RT-XSG library. Opal-RT simulators are configured with different CPU cores to enable parallel computation of electric systems to facilitate model building, loading and compilation. This real-time simulator enables parallel computation of electric systems on different CPU cores. Therefore, sample time less than 50 μs is sufficient to compile any model with any rate of complexity. In addition, OPAL-RT possess direct integration with MATLAB/Simulink and SimPower Systems tool box, which makes it flexible and user friendly. The rear view of OPAL-RT simulator is shown in Fig. A.8. This figure shows the typical access points for the digital input/output port (Block A), analog input/output port (Block C), differential input/output port (Block B), and standard computer connection port (Block D). The sub-D connectors of I/O ports of OP4500 simulator are shown in Fig. A.9. Fig. A.9 shows the DB37 connector, incorporated for communicating with digital I/O and analog I/O of both A and C modules shown in Fig. A.8. DB37 connector is possess the portability to connect 16 channels of the associated I/O (either analog or digital). With these I/O interfacings and involved interactions between two OP4500 modules, an HIL system can be realized. Thus, HIL OPAL-RT 4500 system has proven record as an efficient platform for validating the real-time performance of larger system with complicated modelling of controller/plant/both.

In this thesis, the proposed fault tolerant scheme on nine-level MLDCL RSC-MLI topology is implementing OPAL-RT 4500 controller, the obtained firing signals for the IGBTs are available at DB37 connector. Implementing the proposed FTS on OPAL-RT 4500 controller reduces the

sampling time to 40 μs which enables accurate generation of firing signals with carrier signal frequency of 2.5 kHz.

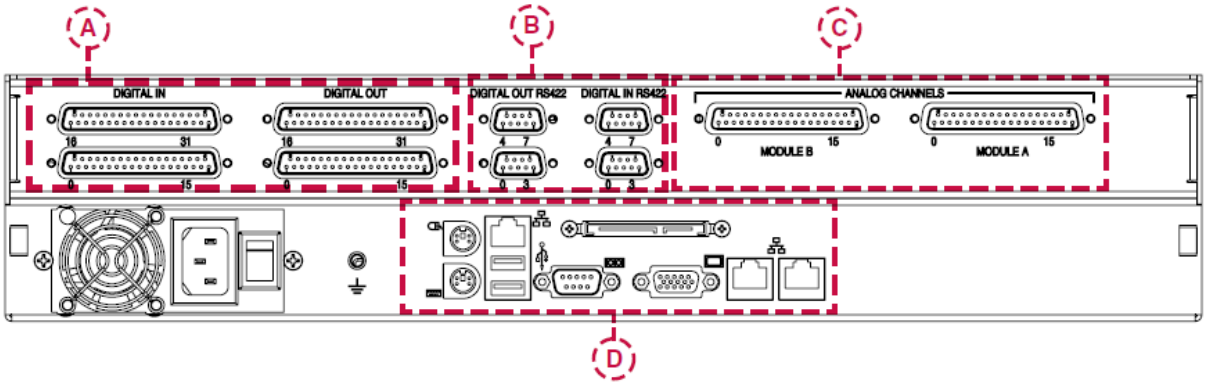


Fig. A.8: View of rear interface OP4500.

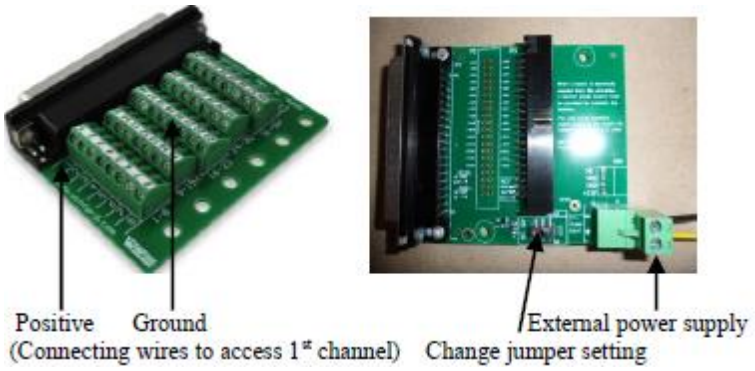


Fig. A.9: DB 37 Screw terminals.

Development of fifteen-level MLDCL based active front-end converter on OPARL-RT 4500 simulator

Further, this thesis considers OPARL-RT simulation tool to validate the pre and post-fault dynamic performance RSC-MLC based active rectifier with VOC and GARPC controllers for multiple open-circuit switch faults on the converter. The performance of the proposed three-phase MLC based active rectifier in real-time environment, two OP4500 simulators of OPAL-RT with one simulator working as a plant i.e., MLC based active rectifier configuration, and other simulator operating as controller, i.e., GARPC/VOC controller with proposed fault tolerant and modified reduced carrier rotation PWM schemes. Gating pulses generated from controller simulator are applied to power converter load in plant controller via digital interface. The instantaneous currents on the ac-side of the converter and voltages on the dc side of the converter are sensed and further communicates to the controller on the simulator for appropriate generation of modulating signals to produce. The dynamic response of the of the modelled 15-level RSC-MLC based active rectifier in real-time using Opal-RT systems, is validated for the sampling time of 20 μs with carrier frequency of 3 kHz.

APPENDIX B: PUBLICATIONS FROM THE WORK

Journals

1. V. Hari Priya, D. Sreenivasarao, and G. Siva Kumar, "Zero-sequence voltage injected fault tolerant scheme for multiple open circuit faults in reduced switch count based MLDCL inverter," IET Power Electronics, vol. 11, no. 8, pp. 1351–1364, July 2018.
2. V. Hari Priya, D. Sreenivasarao, and G. Siva Kumar, and A. Sai Spandana "Reduced carrier PWM scheme with unified logical expressions for reduced switch count multilevel inverters," IET Power Electronics, vol. 11, no. 5, pp. 912–921, May 2018.
3. V. Hari Priya, D. Sreenivasarao, and G. Siva Kumar, "Improved pulse-width modulation scheme for T-type multilevel inverter," IET Power Electronics, vol. 10, no. 8, pp. 968–976, June 2017.

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