Investigation on Transformerless Multi-Level Inverter Schemes for PV Systems

Submitted in partial fulfilment of the requirements

for the award of the degree of

Doctor of Philosophy

by
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CERTIFICATE

This is to certify that the dissertation work entitled **"Investigation on Transformerless Multi-Level Inverter Schemes for PV Systems"**, which is being submitted by **Mr. S. Venu** (Roll No. : 701319, is a bonafide work submitted to National Institute of Technology, Warangal in partial fulfilment of the requirement for the award of the degree of **Doctor of Philosophy** in Department of Electrical Engineering. To the best of our knowledge, the work incorporated in this thesis has not been submitted elsewhere for the award of any degree.

Dr. Sachin Jain
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DEDICATION

To my parents Mr. S. S. Lakshmi Narayana and Mrs. M. Ratna Manikyam, and my brother Mr. Sonti Vinay. Thanks for all your support and encouragement.

DECLARATION

This is to certify that the work presented in the thesis entitled "**Investigation on Transformerless Multi-Level Inverter Schemes for PV Systems"** is a bonafide work done by me under the supervision of **Dr. Sachin Jain,** Department of Electrical Engineering, National Institute of Technology, Warangal, India and was not submitted elsewhere for the award of any degree.

I declare that this written submission represents my ideas in my own words and where others ideas or words have been included I have adequately cited and referenced the original sources. I also declare that I have adhered to all principles of academic honesty and integrity and have not misrepresented or fabricated or falsified any idea/data/fact/source in my submission. I understand that any violation of the above will be a cause for disciplinary action by the institute and can also evoke penal action from the sources which have thus not been properly cited or from whom proper permission has not been taken when needed.

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APPROVAL SHEET

This Thesis entitled "**Investigation on Transformerless Multi-Level Inverter Schemes for PV Systems**" by **S. Venu** is approved for the degree of Doctor of Philosophy

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Venu Sonti

ABSTRACT

The solar PV power generating systems are gaining importance and popularity nowadays because of its salient and inherit features like abundant zero cost fuel (sunlight), zero pollution, and less maintenance etc. However, these systems require high initial investment which is basically due to the cost associated with the PV modules. Further, the low conversion efficiency of the PV cells (sunlight to electricity) also increases the initial investment cost. This also puts a constraint of high-efficiency operation for the power conditioning units used in the PV system. Therefore, the selection of PV inverter topology plays a critical role in minimizing the cost and efficiency of the overall PV system. Due to this reason, the transformerless PV inverter topologies are becoming more popular. These configurations can meet the above requirement satisfactorily both with respect to the cost and efficiency. However, the removal of the transformer eliminates the galvanic isolation between the PV source and output load (grid/stand-alone load). This increases the possibility for the flow of leakage current in the system. The flow of leakage current in the PV system degrades the characteristics or performance of the PV panels and also creates issues related to the safety of a person in contact with the panel. To prevent these safety-related issues, a German standard VDE 0126.1.1 has been imposed which restricts the magnitude of leakage current flowing in the PV system. Apart from meeting the VDE0126.1.1 standard, there is another requirement of feeding high quality of AC power into the grid. This objective can be fulfilled by incorporating the multilevel inverters (MLIs) in the PV power generating systems. However, in literature, many transformerless PV inverter topologies for the minimization of leakage current are proposed. But most of the topologies discussed in the literature are restricted to a maximum of three levels in the inverter output voltage. Also, some of the topologies have other drawbacks like high device count, high switching and conduction losses etc. Thus, there is a requirement of an efficient and economical transformerless MLI topology in the PV system. This thesis proposes such MLI configurations and PWM scheme for the minimization of leakage current in the PV systems. The solutions are given for both single-phase and three-phase systems.

To meet the objective of low cost and efficient operation, a new cascaded multilevel inverter (CMLI) for single-phase PV system is presented. The complete details of the operation of the proposed CMLI in symmetrical and asymmetrical modes along with its extension to the higher number of levels with simulation and experimental results are discussed in the thesis. The comparison of proposed CMLI with the other existing MLI topologies in the literature is also presented. However, the proposed CMLI using the existing PWM techniques requires additional circuitry to minimize the magnitude of leakage current flowing in the system.

A new pulse width modulation (PWM) scheme is proposed for single-phase five-level CMLI for the minimization of leakage current without the addition of any extra circuitry elements is presented. The proposed CMLI is also integrated with the MPPT algorithm and is applied to a five-level CMLI. The proposed PWM technique minimizes leakage current of PV panel and the size of the electromagnetic interference filter required in the system without the addition of any switches. Furthermore, the analysis of the terminal voltage across the PV array and the common mode voltage of the inverter based on the switching function is presented. Also, the proposed PWM technique requires a reduced number of carrier waves compared to the conventional sinusoidal pulse width modulation technique for the given CMLI. However, using the proposed PWM technique for the single-phase five-level CMLI, the objective of high efficiency is not achieved.

To overcome this drawback, a new efficient and reliable transformerless PV MLI configuration is proposed for the minimization of the leakage current in the single-phase systems. Apart from a reduced switch count, the proposed CMLI topology has additional features of low switching and conduction losses. The proposed topology with the given pulse width modulation PWM technique reduces the high-frequency voltage transitions in the terminal and common-mode voltages. Furthermore, the extension of the proposed CMLI along with the PWM technique for higher levels in the output voltage is also presented. A comparison of the proposed CMLI with the existing PV multilevel inverter topologies is also presented.

Apart from single-phase PV inverter topologies, a solution for the three-phase transformerless PV inverter topologies based on DC and NPC DC decoupling methodologies are also presented in the thesis. The new three-phase transformerless MLI topologies are presented for the minimization of leakage current. The leakage current in the three-phase MLI topology is minimized by reducing the transitions in the terminal voltage of the PV panel. The complete details of the proposed three-phase transformerless MLIs, analysis of the terminal voltage using switching functions, simulation and experimental were presented in the thesis.

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CHAPTER 1

Introduction

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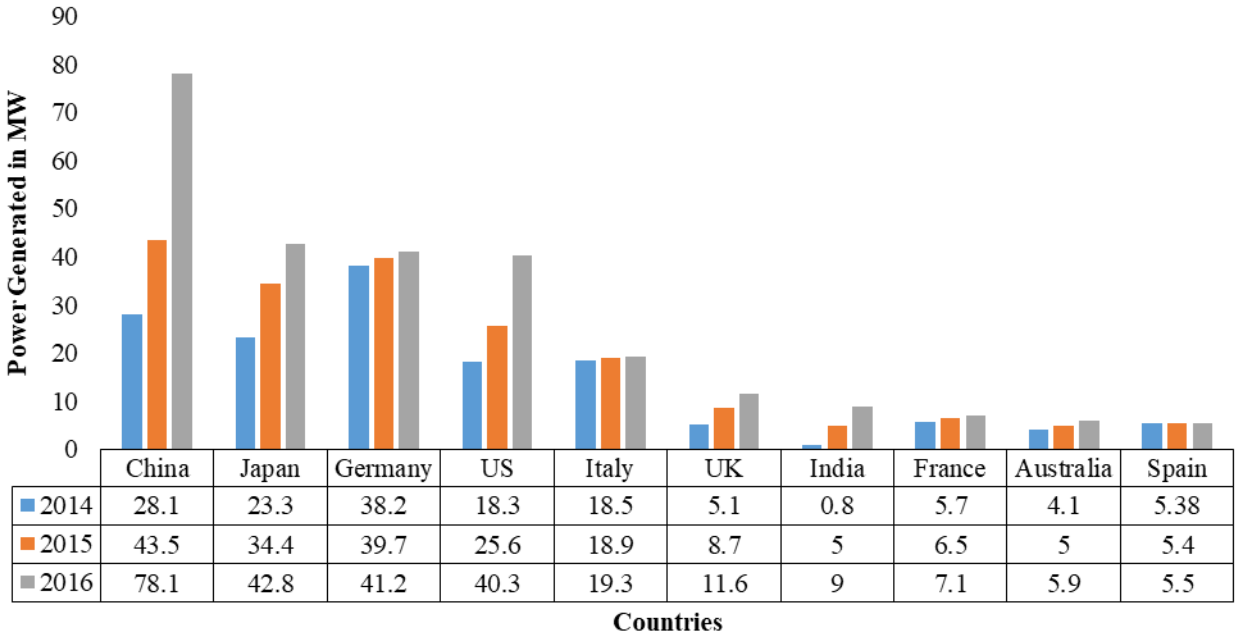
Introduction

1.1. General

In recent years, the solar photovoltaic (PV) power generation has become a feasible solution to cope with the increased electrical energy demand throughout the world. The eminent feature in choosing the solar PV power generation is the energy that drives them. The energy that drives the PV panels is the sunlight, which is abundantly and freely available. The second important feature in opting the PV power generation is zero pollution and green solution. The solar PV power generation does not create any pollution in terms of air, water and noise. Another, attractive feature related to the PV power generation, is it requires less or nearly zero maintenance. Since there are no moving parts associated with the PV power generation. Further, the PV panels used in power generation typically have a long lifetime of nearly 20-25 years. With all these added advantages, there is a lot of investment done in the PV power generation in many countries. The Fig. 1.1 shows the statistics of PV power generated in MW in various countries for the years 2014, 2015 and 2016 [1]. Nearly for all the countries, the capacity of PV power generated has gradually increased from the year 2014 to 2016.

Though a lot of investment is made in the PV power generation, one hurdle which pulls back the growth in the PV power generation is its high initial investment. However, this high initial investment is basically due to the cost associated with the PV modules. Besides modules cost, the low conversion efficiency of the PV cells (sunlight to electricity) further increases the initial investment cost. This also puts a constraint of high-efficiency operation for the power conditioning units used in the PV system. Therefore, the selection of the PV power conditioning unit plays a critical role in minimizing the cost and efficiency of the overall PV system. In this way, the PV power conditioning units [2] are gaining the attention of the researchers. The researchers have proposed various PV inverter topologies and classified them into different categories in the literature.



	China	Japan	Germany	US	Italy	UK	India	France	Australia	Spain
2014	28.1	23.3	38.2	18.3	18.5	5.1	0.8	5.7	4.1	5.38
2015	43.5	34.4	39.7	25.6	18.9	8.7	5	6.5	5	5.4
2016	78.1	42.8	41.2	40.3	19.3	11.6	9	7.1	5.9	5.5

Fig. 1.1. The statistics of PV power generated in MW in various countries from 2014 to 2016.

1.2. Classification of the PV inverter topologies

One such classification is based on the inclusion of the transformer in the system [2]. The PV inverter topologies are classified into:

1.2.1. Transformer based PV inverter topology

The PV solution which typically uses a transformer between the PV source and load comes under the category of transformer based solution. These configurations have the benefits of both boosting of PV voltage and the galvanic isolation due to the inclusion of transformer. The benefit of galvanic isolation further adds to the elimination of leakage current problem. However, these systems suffer from the disadvantage of high weight, size and losses. Based on the type of transformer used in the PV system, these systems can further be classified into

1.2.1.1 Low-frequency transformer based PV inverter topology

In the category of low-frequency transformer based PV inverter topology [3-4], a low-frequency (supply frequency) transformer is inserted in between the PV inverter output and the grid/stand-alone load as shown in Fig. 1.2. As the power rating of the system increases, the cost, size and weight of the low-frequency transformer are also increased. As a

result the cost, weight, losses and the size of the complete PV system are increased which makes the given solution unattractive and uneconomical.

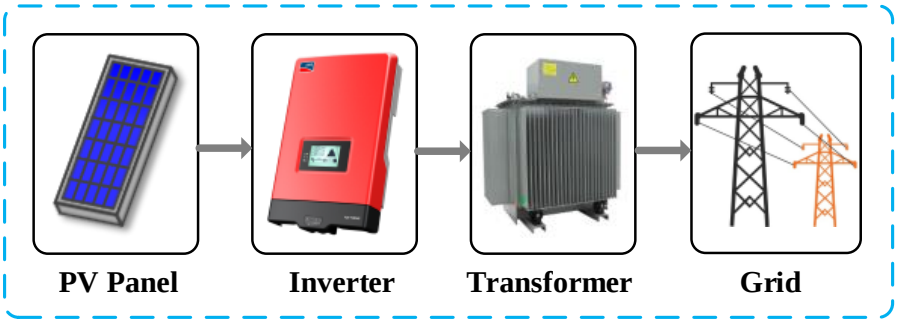


Fig. 1.2. The block diagram of a low-frequency transformer based PV inverter topology.

1.2.1.2. High-frequency transformer based PV inverter topology

The other category of high-frequency transformer based PV inverter topology [5-7] is an elegant solution with respect to the size and weight of PV system. A high-frequency transformer is inserted in between the PV array output and the input of inverter in the form of a DC-DC converter as shown in Fig. 1.3. Usage of a high-frequency transformer reduces the weight, cost and the size of the transformer. However, with the incorporation of the high-frequency DC-DC isolation stage, increases the number of power processing stages in the PV system. This results in the reduced efficiency and increased losses.

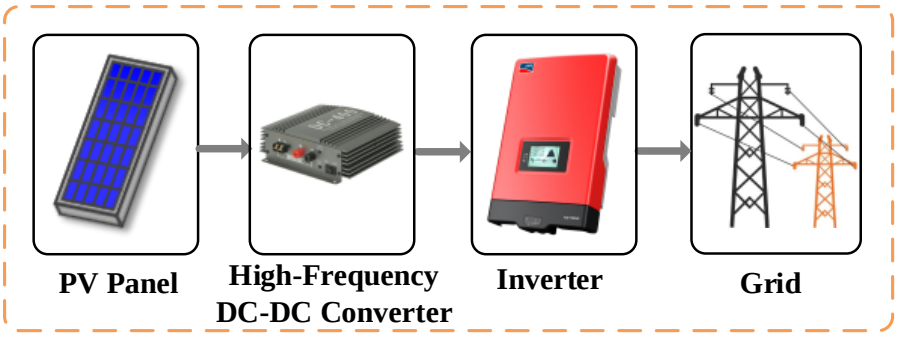


Fig. 1.3. The block diagram of a high-frequency transformer based PV inverter topology.

1.2.2. Transformerless PV inverter topology

In order to reduce the cost, size, losses and weight and to improve the efficiency of the system, the transformer used in the PV system is eliminated as given in Fig. 1.4. This idea had led to the development of many transformerless PV inverter topologies [8-12]. The

removal of the transformer in the PV inverter makes them economical and improves the efficiency. However, the removal of the transformer in the system results in elimination of galvanic isolation between the PV source and output load. This may result in the flow of the leakage current in the PV system.

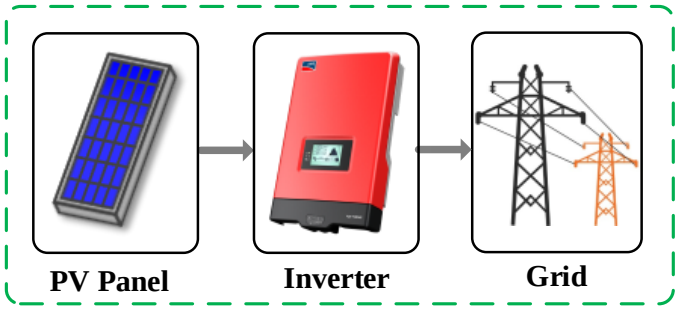


Fig. 1.4. The block diagram of transformerless PV inverter topology.

1.3. Leakage current

The removal of the transformer in the PV system results in the direct connection between the PV array and the grid/stand-alone load. This may lead to the flow of leakage current between the PV array and grid/stand-alone load via the parasitic capacitance of the PV panel as shown in Fig. 1.5. The flow of leakage current between the ground and parasitic capacitance of PV panel results in the mal-operation of PV cells. Further, the person in contact with PV panel can get electric shock as depicted in Fig. 1.5. Thus, various standards and regulations have been imposed on the PV system with respect to the flow of leakage current. In addition to the above, there is another regulation with respect to residual ground current which further restricts or put a constraint on the flow of leakage current in the PV

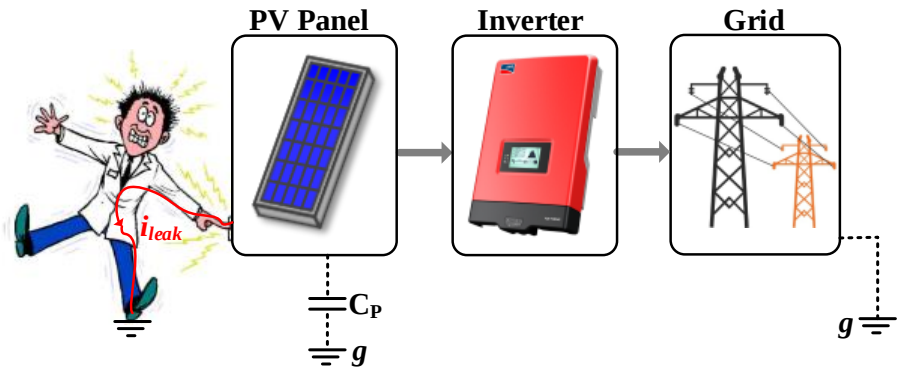


Fig. 1.5. The block diagram of showing the flow of leakage current in the transformerless PV inverter.

system to avoid unwanted tripping of PV system due to the high value of ground current. Considering all these effects, various standards are imposed on the PV systems, which comment on the magnitude of the leakage current flowing through the PV panel. One standard among them is VDE 0126-1-1 [13]. This standard specifies that the magnitude of the leakage current flowing through the PV panel must be less than 300mA (peak). So, all the commercially available PV inverter topologies are required to meet this VDE 0126-1-1 standard [14-18].

The leakage current path exists due to the presence of a parasitic capacitor between the PV source and ground. The parasitic capacitance exists mainly due to the PV panel structure which mainly consists of a solar cell, glass and frame as shown in Fig. 1.6. The parasitic capacitance [2] of the PV panel is formed between the PV cell and metallic frame of the PV panel. The value of parasitic capacitance formed mainly depends on the factors like the surface area of PV cell and frame, the distance between the PV cell and frame, atmospheric conditions, dust, humidity etc. So the value of parasitic capacitance is not constant and it varies depending on the environmental conditions. The typical value of the parasitic capacitance varies between 100pF to 3.6μF [2]. The current flowing through this parasitic capacitance is called leakage current, and the voltage across the parasitic capacitance is called terminal voltage.

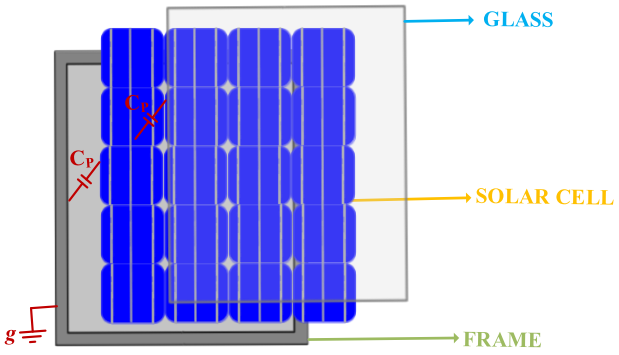


Fig. 1.6. The parasitic capacitances of the PV panels.

The magnitude of the leakage current flowing in the parasitic capacitance mainly depends on the two factors. One factor is the value of the parasitic capacitance which is determined by the environmental conditions. The other factor is the nature of the terminal voltage. If the terminal voltage has high-frequency switching transitions, then the parasitic capacitance offers minimum impedance for these high-frequency transitions. So, the magnitude of the leakage current may become high. Considering this fact, in this

thesis, various solutions were given to minimize the magnitude of leakage current flowing in the transformerless multi-level inverter based PV systems.

1.4. Organization of the document

This thesis has been structured into eight chapters (including the present chapter) which are arranged as explained below.

Chapter 2 addressed the comprehensive review of various single-phase PV inverter topologies for the minimization of the leakage current. Based on this comprehensive review, the PV inverter topologies are classified into DC decoupling, AC decoupling and neutral point clamped (NPC) decoupling. The analysis of the terminal voltage is done by using the switching function concept for each inverter topology. The PV inverter topologies discussed are then compared in terms of number of devices used, number of capacitors used, number of switches conducting in positive and negative half cycles etc. Finally, it sets motivation for the research work carried out in this thesis.

In **Chapter 3**, a new low cost and efficient cascaded multi-level inverter (CMLI) is proposed. The proposed CMLI is operated in both symmetrical and asymmetrical modes. First, the operation of the CMLI for both symmetrical and asymmetrical modes of operation is discussed. Then, the generalization of proposed CMLI for higher levels is presented. The simulation and experimental results of the proposed CMLI for both the symmetrical and asymmetrical operation are presented. Further, the proposed CMLI is compared with other multi-level inverter topologies to show the advantages in terms of switching and conduction losses.

Chapter 4 gives the details of a new pulse width modulation (PWM) technique for the minimization of the leakage current in the grid-connected/stand-alone transformerless photovoltaic (PV)-CMLI. First, the operation of the CMLI is discussed along with its switching states. The proposed PWM technique for symmetrical and asymmetrical operation along with its generalization is discussed. The procedure for integrating the maximum power point tracking maximum power point tracking (MPPT) to the CMLI for both symmetrical and asymmetrical operations is discussed. The analysis of the terminal voltage and common mode voltage for the five-level CMLI is given. Next, the simulation and experimental results were also presented to justify the correctness of given analysis.

In **Chapter 5**, a CMLI based on a highly efficient and reliable configuration for the minimization of the leakage current is proposed. First, the working principle and the operation of the proposed five-level grid-connected CMLI along with the generalized structure is described. The details of the PWM technique employed with its generalization for '*2m + 1*' levels are then explained. Next, the details of the MPPT algorithm which can be applied to the proposed five-level CMLI were explained. This is followed by the analysis of the terminal and CMVs for the proposed CMLI. The simulation and experimental results of the proposed five-level CMLI were presented. Finally, the comparison of the proposed CMLI with the other existing PV MLI topologies in the literature is presented.

Chapter 6 addresses the comprehensive review on analysis of terminal voltage for single-phase extended three-phase transformerless PV inverter topologies. The analysis of the terminal voltage is done by using the switching function concept for each inverter topology.

In **Chapter 7**, a new DC decoupling based three-phase PV CMLI is proposed for the minimization of the leakage current. First, the operation of the proposed three-phase CMLI is presented along with the PWM scheme used for the minimization of the leakage current. Next, the analysis of the terminal voltage for the proposed three-phase CMLI is given. The simulation and experimental results of the three-phase CMLI are also presented.

Chapter 8 proposes a new NPC DC decoupling based three-phase PV CMLI for the minimization of leakage current. In this chapter, the operation of proposed three-phase CMLI is discussed. Apart from the operation, the analysis of the terminal voltage using switching function concept for the proposed three-phase CMLI is presented. Then, the simulation and experimental results of the proposed three-phase CMLI are given to support the operation and switching function analysis.

Finally, **Chapter 9** highlights the main findings of the research work reported in this thesis and also suggests the scope for future work.

CHAPTER 2

Literature Survey of Single-Phase Transformerless PV Inverter Topologies

Chapter 2

Literature Survey of Single-Phase Transformerless PV Inverter Topologies

This chapter presents a comprehensive review of various single-phase transformerless PV inverter topologies. The reviewed PV inverter topologies are analyzed for the leakage current flowing through the parasitic capacitance of PV array using the terminal voltage expressions. Further, in the given chapter, the expression of the terminal voltages are derived for various PV inverter configurations using switching function analysis [19]. The given switching function analysis is very simple and is expressed in terms of switching states of the switches. Thus, the given analysis directly links the terminal voltage with PWM strategy or switching states. In other words, a PWM strategy can be modified or altered such that, the magnitude of leakage current can be minimized. Further, using the switching function analysis, the nature of terminal voltage of the PV inverter can be directly obtained without the help any simulation software.

In a given grid-tied PV system, mainly the topology or the configuration of the PV inverter varies. While, the other basic elements like a filter, grid and parasitic elements are nearly same in all the systems. Hence, the variables used in the schematic of the grid-tied PV inverter along with PV panel parasitic elements are commonly defined for all the reviewed configurations. The PV inverter output voltage 'v_{ab}' is connected to grid 'e_g' via an LCL filter. The terms 'L_f' and 'L' refer to the PV inverter side and grid side filter inductors respectively as shown in Fig. 2.1 (i). The terms 'R_d' and 'C_d' refer to the damping resistor and the filter capacitor respectively. The currents 'i_l', 'i_p' and 'i_g' refer to the inverter output current, the current flowing through the damping branch and the current flowing into the grid respectively. The capacitor 'C_{PV}' is the buffer capacitor between the PV array and inverter. The voltage across the capacitor 'C_{PV}' is represented as 'V_{PV}'. The connection of parasitic elements in the PV array is shown with dotted lines. The parasitic elements are connected to the positive terminal (node 'p') of the PV array. The negative terminal of the PV array is represented as node 'n'. The terms 'R_p' and 'C_p' refer to the parasitic resistor and capacitor of the PV array respectively. The term 'i_{leak}' represents the leakage current flowing in the

parasitic branch of the PV array. The parasitic capacitor in the PV array forms a resonant circuit with the low pass filter at the inverter output [20]. At the resonant frequency, the circuit offers minimum impedance which results in the flow of high magnitude leakage current [20].

The terminal voltage expressions for different PV inverter topologies are expressed in terms of switching functions of the individual switches used in the inverter, grid voltage 'e_g' and the PV array voltage 'V_{PV}'. The switches in the inverter topologies are represented by Sw_x where x=1, 2, 3, 4, 5, 6, 7 and 8. The switching states of the individual switch Sw_x are denoted by S_x, where x=1, 2, 3, 4, 5, 6, 7 and 8. The pulses for the individual switches are generated using the conventional sinusoidal pulse width modulation (SPWM) technique where the modulating sinusoidal reference wave is compared with the triangular carrier wave.

Using the switching function variables, grid voltage 'e_g' and the PV array voltage 'V_{PV}', the expressions for the terminal voltage have been derived. Once the terminal voltage expressions are obtained, then the analytical waveforms of the terminal voltages 'v_{pg}' and 'v_{ng}' are plotted in MATLAB SIMULINK. In the present case, the terminal voltage waveforms are obtained by considering the parameters 'e_g'=230V (RMS), the frequency of grid voltage 'f_g'=50Hz, PV array voltage 'V_{PV}' = 400V and switching frequency of the inverter 'f_{sw}'=500Hz. This is done to depict the switching transitions in the terminal voltage clearly.

2.1. Full-bridge inverter with bipolar PWM technique

Fig. 2.1 (i) shows the complete schematic of the PV full-bridge inverter connected to the grid via an LCL filter as described in previous sections. The output voltage of the inverter consists of two levels (i.e., 'V_{PV}' and '-V_{PV}') in the case of bipolar PWM technique [21]. The full-bridge inverter uses four switches Sw_1, Sw_2, Sw_3 and Sw_4 for the generation of two levels at the output terminals. The pairs of switches (Sw_1, Sw_2) and (Sw_3, Sw_4) are operated in a complementary manner. The various modes of operation of the full-bridge inverter with the bipolar PWM technique are shown in Fig. 2.1 (ii). Whenever the switches Sw_1 and Sw_4 are turned ON, the inverter output voltage becomes 'V_{PV}'. Similarly, the inverter output voltage attains '-V_{PV}', if the switches Sw_2 and Sw_4 are turned ON.

The waveforms of the gate pulses for the switches, output voltage and the terminal voltage of the full-bridge inverter with bipolar PWM technique are shown in Fig. 2.1 (iii). The bipolar PWM technique uses only one reference wave and a carrier wave. The switch pair (Sw_1 and Sw_4) is turned ON whenever the magnitude of the reference wave is greater than the carrier wave. Otherwise, the other switch pair (Sw_2 and Sw_3) is turned ON. The inverter output voltage oscillates within the levels 'V_{PV}' and '$-V_{PV}$' during the complete cycle of the grid voltage. The same can be observed from the waveform of the output voltage in Fig. 2.1 (iii). Due to the switching action of the individual switches, the inverter generates terminal voltages 'v_{pg}' and 'v_{ng}' at the nodes 'p' and 'n' with respect to the ground. From Fig. 2.1 (i), the terminal voltages 'v_{pg}' and 'v_{ng}' are related as:

$$v_{ng} = v_{pg} - V_{PV} \tag{2.1}$$

The pole voltages 'v_{ag}' and 'v_{bg}' are expressed in terms of the terminal voltages 'v_{pg}' and 'v_{ng}' as:

$$v_{ag} = S_1 v_{pg} + (1-S_1) v_{ng} \tag{2.2}$$

$$v_{bg} = S_3 v_{pg} + (1-S_3) v_{qg} \tag{2.3}$$

The voltages 'v_{ag}' and 'v_{bg}' are also expressed in terms of the grid voltage 'e_g' and voltage drops in filter inductors ('L' and 'L_f') as [19],

$$v_{ag} = \frac{L}{2}\frac{di_l}{dt} + \frac{L_f}{2}\frac{di_g}{dt} + e_g \tag{2.4}$$

$$v_{bg} = \frac{L}{2}\frac{di_l'}{dt} + \frac{L_f}{2}\frac{di_g'}{dt} \tag{2.5}$$

Adding (2.4) and (2.5) by assuming the currents 'i_l'='$-i_l$'and 'i_g'='$-i_g$' (Fig. 2.1) gives,

$$v_{ag} + v_{bg} = e_g \tag{2.6}$$

Adding (2.2) and (2.3) and substituting in (2.6) gives,

$$e_g = (S_1+S_3) v_{pg} + \big((1-S_1)+(1-S_3)\big) v_{ng} \tag{2.7}$$

Substituting (2.1) in (2.7) and simplifying gives,

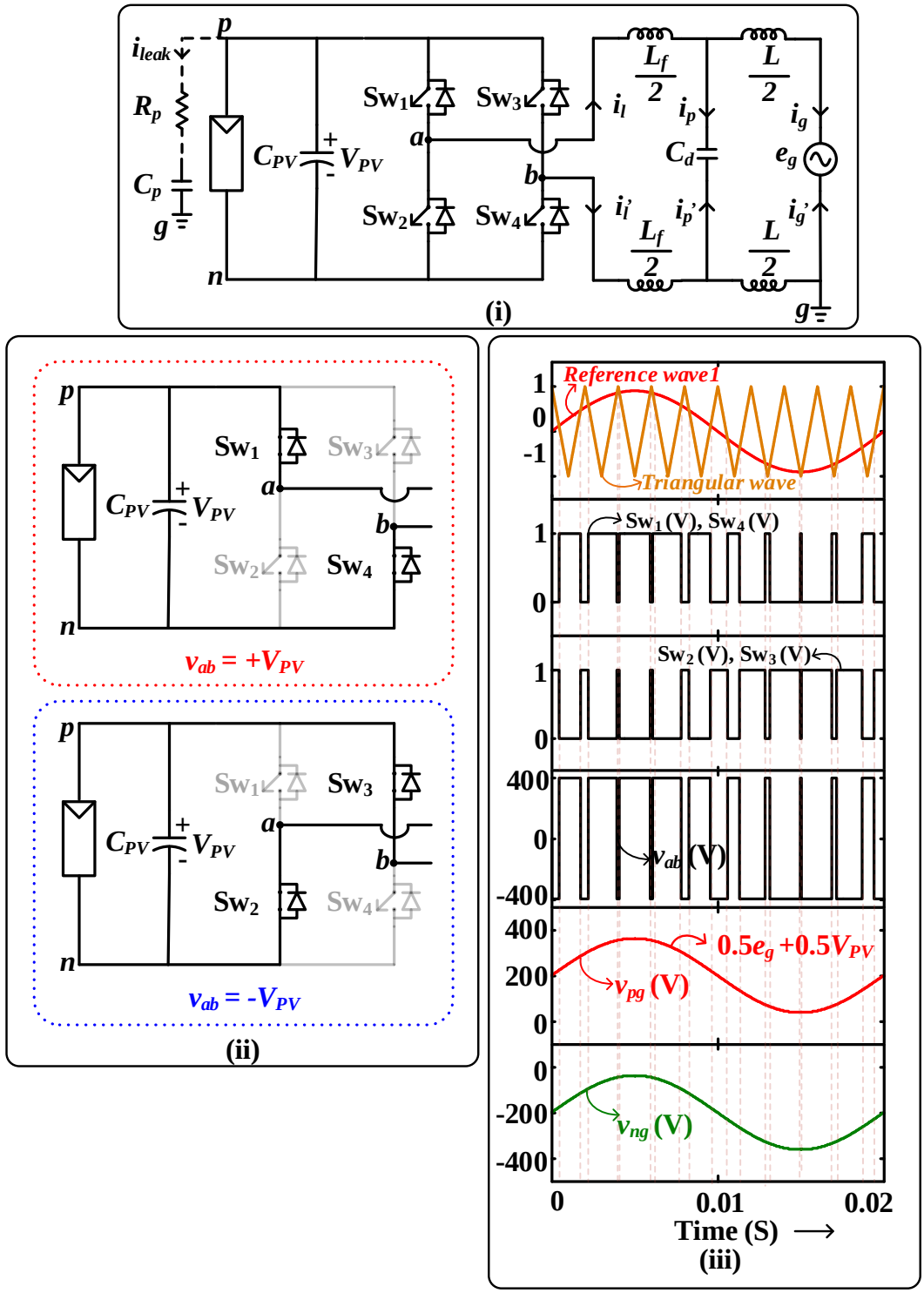


Fig.2.1 (i) Schematic of the PV full-bridge inverter connected to a grid via an LCL filter; (ii) Modes of operation of a full - bridge inverter with a bipolar PWM technique for the levels *'V_{PV}'* and '$-V_{PV}$'; (iii) Generation of pulses for the switches Sw_1, Sw_2, Sw_3 and Sw_4 from the reference wave and carrier wave, the output voltage of the inverter 'v_{ab}', analytical waveforms of the terminal voltages 'v_{pg}' and 'v_{ng}' from the expressions.

$$v_{pg} = 0.5e_g + 0.5\left((1-S_1)+(1-S_3)\right)V_{PV} \quad (2.8)$$

In the bipolar PWM technique, the pairs of switches (Sw_1 and Sw_3) or (Sw_2 and Sw_4) are not turned ON simultaneously due to the absence of '*0*' state. So, for the complete cycle of the output voltage, either switch Sw_1 or Sw_3 is turned ON. Substituting the values of switching states of the switches in (2.8), the terminal voltage 'v_{pg}' for the bipolar PWM technique is given by

$$v_{pg} = 0.5e_g + 0.5\,V_{PV} \quad (2.9)$$

The magnitude of the terminal voltage 'v_{pg}' is equal to the average of the instantaneous magnitude of grid voltage 'e_g' and the PV array output voltage 'V_{PV}'. From (2.9), it can be observed that the terminal voltage in the case of bipolar PWM technique is free from the effect of switching states. Thus, the terminal voltage is a low-frequency (grid frequency) sine wave with a DC offset equal to 0.5 times the PV array voltage 'V_{PV}'. This avoids the high-frequency switching transitions in the terminal voltages. The waveforms of the terminal voltages 'v_{pg}' and 'v_{ng}', shown in Fig. 2.1 (iii), are obtained using (2.1) and (2.9). From the waveforms, it can be depicted that the terminal voltages in case of bipolar PWM technique are free from high-frequency switching transitions.

2.2. Full-bridge inverter with unipolar PWM technique

The circuit schematic for full-bridge inverter remains same as shown in Fig. 2.1 (i). Unlike the bipolar PWM technique, the output voltage of the inverter has three levels (i.e., 'V_{PV}', '*0*' and -'-V_{PV}') in the case of the unipolar PWM technique [21]. The modes of operation of the full-bridge inverter using the unipolar PWM technique is shown in Fig. 2.2 (i). Whenever the switches Sw_1 and Sw_4 are turned ON, the inverter output voltage becomes 'V_{PV}'. Similarly, the inverter output voltage attains '-V_{PV}', if the switches Sw_2 and Sw_4 are turned ON. For the '*0*' voltage level, either of the top switches pair (Sw_1 and Sw_3) or bottom switches pair (Sw_2 and Sw_4) are turned ON. Hence, the inverter output current freewheels through the top or the bottom pair of switches.

Fig. 2.2 (ii) shows the waveforms of the generated gate pulses for the switches, output and the terminal voltages for the full-bridge inverter using the unipolar PWM technique. The unipolar PWM technique uses two modulating/reference waves (i.e., reference wave-1 and

reference wave-2) which are in phase opposition as shown in Fig. 2.2 (ii). The two generated reference waves are now compared with a single carrier wave at low-frequency operation (10 times the modulating frequency is chosen to show clearly the switching transitions within the cycle). This generates the PWM pulses for top switches of each leg of the inverter. Thus, in the case of unipolar PWM technique, each leg of the inverter is controlled independently. Reference wave-1 controls the first leg of the inverter and reference wave-2 controls the second leg. If the magnitude of reference wave-1 is greater than the carrier wave, then the switch Sw_1 is turned-ON else turned OFF. Similarly, if the magnitude of reference wave-2 is greater than the carrier wave, the switch Sw_3 is turned ON else turned OFF. With the unipolar PWM technique, the inverter output voltage switches between the levels 'V_{PV}' and '*0*' during the positive half-cycle of the grid voltage. During the negative half-cycle of the grid voltage, the inverter output switches between the levels '*0*' and '$-V_{PV}$', which can be easily observed from the waveform of the output voltage in Fig. 2.2 (ii). The expression for the terminal voltage 'v_{pg}' is same as given (2.8).

During the active states of the inverter output voltage (i.e., 'V_{PV}' or '$-V_{PV}$'), either the switch pair (Sw_1, Sw_4) or (Sw_2, Sw_3) is turned ON. Substituting the switching states (or switching function value) of the switches in (2.8) results in

$$v_{pg} = 0.5e_g + 0.5\,V_{PV} \tag{2.10}$$

Similarly, during the zero state, for the switch pair combination (Sw_1, Sw_3), the magnitude of the terminal voltage 'v_{pg}' is equal to,

$$v_{pg} = 0.5e_g \tag{2.11}$$

Now the value of terminal voltage during zero state using the bottom switch pair (Sw_2, Sw_4), is given by,

$$v_{pg} = 0.5e_g + V_{PV} \tag{2.12}$$

Similarly, the waveform of the other terminal voltage 'v_{pg}' can be obtained from (2.1) by substituting the value of 'v_{pg}'. Thus, in unipolar PWM technique, the terminal voltage switches between three values as derived in (2.10)-(2.12). This can be easily verified in the waveforms of the terminal voltages given in Fig. 2.2 (ii). The given terminal voltage waveform in Fig. 2.2 (ii) is drawn using the expression of 'v_{pg}' and 'v_{ng}' as derived above.

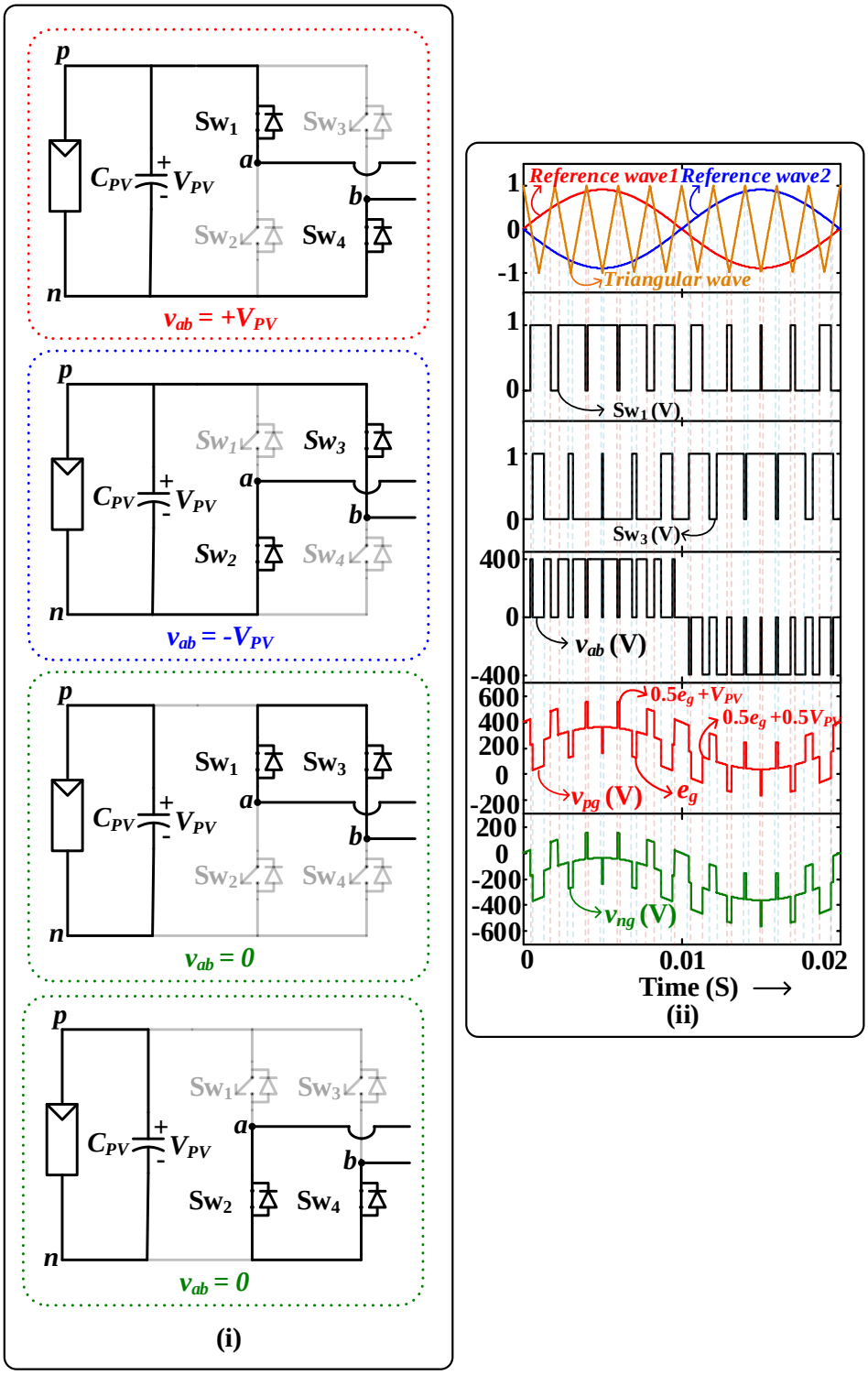


Fig.2.2 (i) Modes of operation of full-bridge inverter for the levels 'V_{PV}', '*0*' and '$-V_{PV}$'; (ii) Generation of pulses for the switches Sw_1, Sw_2, Sw_3 and Sw_4 from the reference wave and carrier wave, the output voltage of the inverter 'v_{ab}', analytical waveforms of the terminal voltages 'v_{pg}' and 'v_{ng}' from the expressions.

It can be noted that a switching transition in the terminal voltage occurs only during zero state.This results in the flow of leakage current through the parasitic capacitance of the PV array. Therefore, if the switching transition in the terminal voltage during zero state is avoided, then the magnitude of leakage current can be minimized. Based on this concept, various PV inverter topologies are proposed in the literature. Below it describes the various PV inverter configurations given for the minimization of leakage current.

2.3. H5 inverter topology

Fig. 2.3 (i) gives the circuit schematic diagram for H5 inverter [22] topology for grid-tied PV inverter. The H5 inverter topology consists of an H-bridge inverter with the additional decoupling switch Sw_5. The switch Sw_5 is used to isolate the grid and PV array during the '*0*' state or freewheeling state. The pairs of switches (Sw_1, Sw_2) and (Sw_3, Sw_4) operate in complementary mode. The H5 inverter generates three levels in the output voltage like full-bridge inverter with unipolar PWM technique. Fig. 2.3 (ii) shows the modes of operation of the H5 inverter for the three voltage levels 'V_{PV}', '*0*' and '$-V_{PV}$'. The voltage level 'V_{PV}' is obtained whenever the switches Sw_1, Sw_4 and Sw_5 are turned ON. Similarly, the voltage level '$-V_{PV}$' is obtained if the switches Sw_2, Sw_3 and Sw_5 are turned ON. During the '*0*' voltage level, the switch Sw_5 is turned OFF and the switches Sw_1 and Sw_3 are kept in turned ON state so that the inverter output current freewheels through these two switches. This provides isolation between the two sources, i.e., grid and PV array. Therefore, H5 inverter uses DC decoupling methodology for the minimization of leakage current in the PV systems.

Fig. 2.3 (iii) shows the generation of pulses for the switches, output voltage and the terminal voltage of the H5 inverter. The H5 inverter requires two carrier waves which are level shifted by 1V as shown in Fig. 2.3 (iii). Whenever, the magnitude of the reference wave is greater than the upper carrier wave, the switches Sw_1, Sw_4 and Sw_5 are turned ON. Similarly, whenever the magnitude of the reference wave is less than bottom carrier wave the switches Sw_2, Sw_3 and Sw_5 are turned ON. The '*0*' voltage level occurs whenever the magnitude of the reference wave is less than upper carrier wave and greater than the bottom carrier wave. The H5 inverter output voltage oscillates within the levels 'V_{PV}' and '*0*' during a positive half-cycle of the grid voltage. During the negative half-cycle of the grid voltage, the inverter output varies within the levels '*0*' and '$-V_{PV}$' which can be observed from the

waveform of the output voltage in Fig. 2.3 (iii). The derivation for the terminal voltage 'v_{pg}' is given below

The pole voltages 'v_{ag}' and 'v_{bg}' are expressed in terms of the terminal voltages 'v_{pg}' and 'v_{ng}' as:

$$v_{ag} = S_5 S_1 v_{pg} + (1\text{-}S_1) v_{ng} \tag{2.13}$$

$$v_{bg} = S_5 S_3 v_{pg} + (1\text{-}S_3) v_{ng} \tag{2.14}$$

Adding (2.13) and (2.14) and substituting in (2.6) gives,

$$e_g = S_5 (S_1 + S_3) v_{pg} + \left((1 - S_1) + (1 - S_3)\right) v_{ng} \tag{2.15}$$

Substituting (2.1) in (2.15) and simplifying gives,

$$v_{pg} = \frac{e_g + \left((1\text{-}S_1) + (1\text{-}S_3)\right) V_{PV}}{S_5 (S_1 + S_3) + \left((1\text{-}S_1) + (1\text{-}S_3)\right)} \tag{2.16}$$

The switch pair (Sw_1, Sw_4) or (Sw_2, Sw_3) are turned ON along with the switch Sw_5 during the active states (i.e., 'V_{PV}' or '$-V_{PV}$'). Substituting the switching states of these switches in (2.16) results in,

$$v_{pg} = 0.5 e_g + 0.5\, V_{PV} \tag{2.17}$$

Equation (2.17) is the same as what was obtained for unipolar and bipolar PWM during the active states. Now, during the '*0*' voltage level, the switch Sw_5 is turned OFF and the other switches Sw_1 and Sw_3 are turned ON. Hence the magnitude of the terminal voltage 'v_{pg}' becomes:

$$v_{pg} = \infty \tag{2.18}$$

Fig. 2.3 (iii) shows the waveforms of the terminal voltages 'v_{pg}' and 'v_{ng}' obtained from the (2.16) and (2.1). It can be observed that the terminal voltages are free from the high-frequency switching transitions like in the case of bipolar PWM technique.

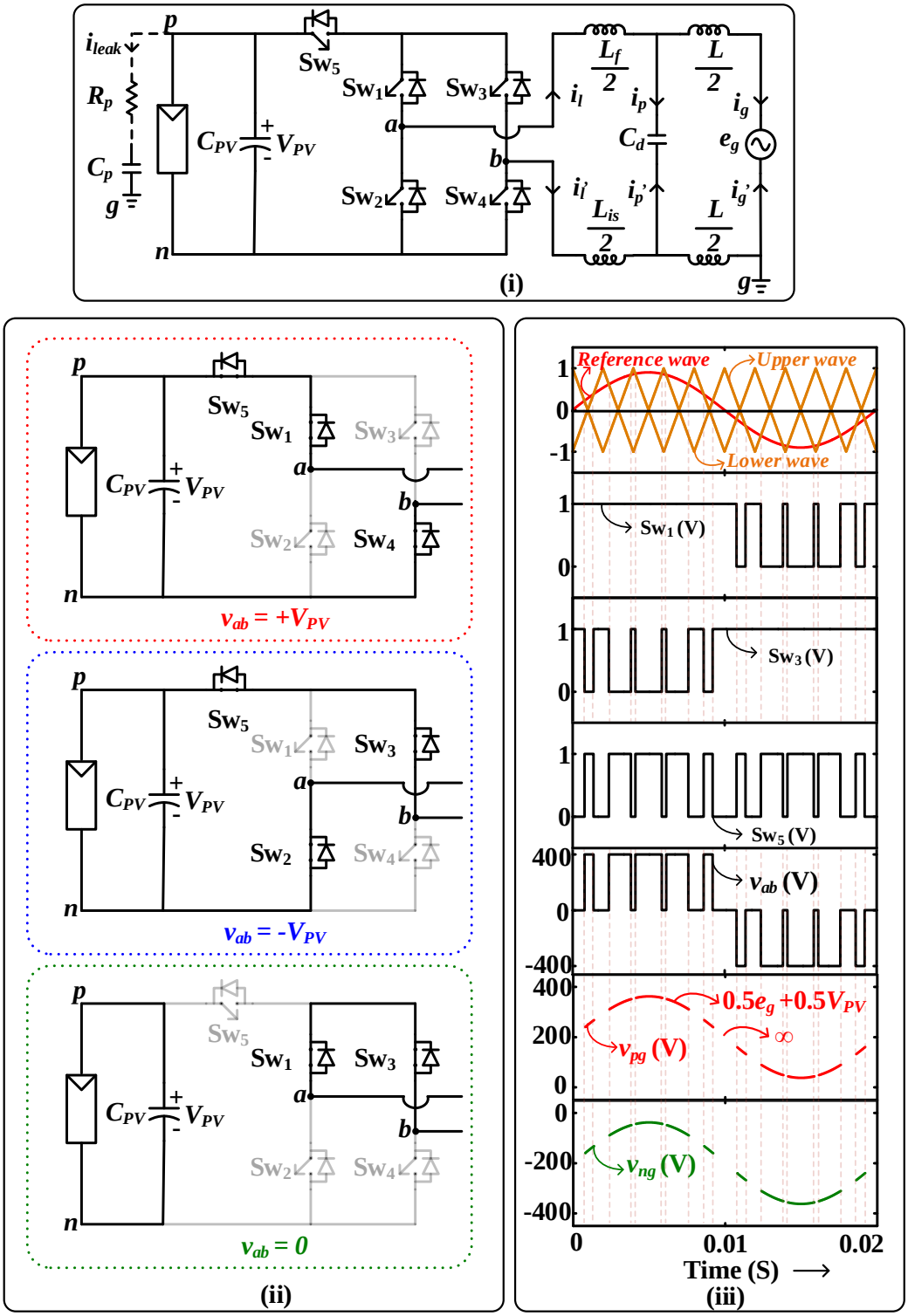


Fig.2.3 (i) Schematic of the H5 inverter connected to a grid via an LCL filter; (ii) Modes of operation of H5 for the levels 'V_{PV}', '$-V_{PV}$' and '0'; (iii) Generation of pulses for the switches Sw_1, Sw_2, Sw_3, Sw_4 and Sw_5 from the reference wave and carrier wave, the output voltage of the inverter 'v_{ab}', analytical waveforms of the terminal voltages 'v_{pg}' and 'v_{ng}' from the expressions.

2.4. HERIC inverter topology

The schematic of HERIC topology [23], connected to the grid via an LCL filter, is shown in Fig. 2.4 (i). The term HERIC refers to Highly Efficient and Reliable Inverter Configuration. The HERIC topology consists of an H-bridge inverter and the bi-directional switches Sw_5 and Sw_6. The switches Sw_5 and Sw_6 provide a free-wheeling path for the inductor current at the '*0*' voltage level. The HERIC topology also generates three levels in the output voltage.

The modes of operation of HERIC inverter for the voltage levels 'V_{PV}', '*0*' and '$-V_{PV}$' are shown in Fig. 2.4 (ii). The voltage level 'V_{PV}' is obtained whenever the switches Sw_1 and Sw_4 are turned ON. Similarly, the voltage level '$-V_{PV}$' is obtained if the switches Sw_2 and Sw_3 are turned ON. For '*0*' voltage level, grid current is freewheeled through AC-by-pass switches Sw_5 and Sw_6. The switches Sw_5 and Sw_6 are kept turned ON during the negative and positive half cycles of the grid voltage respectively. During '*0*' voltage level, the grid inductor current 'i_l' (in Fig. 2.4 (i)) free-wheels through the AC-by-pass switches Sw_5 and Sw_6. All the switches in H-bridge are turned OFF at the '*0*' voltage level. The turn-OFF switches in H-bridge during '*0*' voltage level result in isolation of grid and PV array [23]. Therefore, the HERIC inverter uses AC decoupling methodology for the minimization of leakage current in the PV systems.

The generation of pulses of the switches, output voltage and terminal voltage waveforms for HERIC inverter is shown in Fig. 2.4 (iii). The HERIC inverter requires one reference wave and two carrier waves, which are level shifted by 1V. Whenever the magnitude of the reference wave is greater than the upper carrier wave, the switches Sw_1 and Sw_4 are turned ON. Similarly, whenever the magnitude of the reference wave is less than the bottom carrier wave, the switches Sw_2 and Sw_3 are turned ON. From the waveform of output voltage shown in Fig. 2.4 (iii), it can be observed that during the positive half-cycle of the grid voltage, the HERIC output voltage varies between 'V_{PV}' and '*0*'. Similarly, in the negative half-cycle of the grid voltage, the inverter output varies within the levels '*0*' and '$-V_{PV}$'. The derivation for the terminal voltage 'v_{pg}' for the HERIC is given below.

The pole voltages 'v_{ag}' and 'v_{bg}' are expressed in terms of the terminal voltages 'v_{pg}' and 'v_{ng}' as

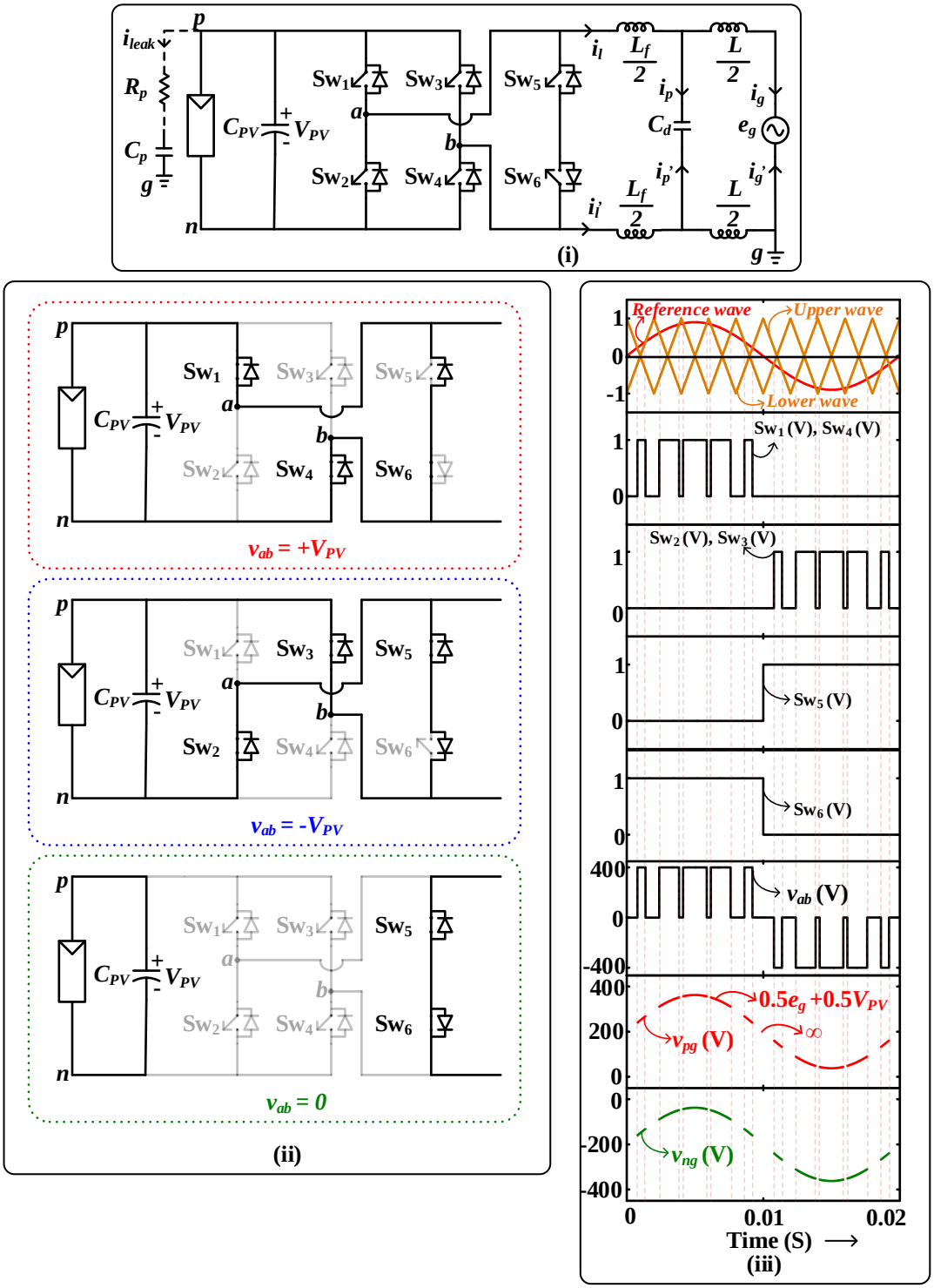


Fig.2.4 (i) Schematic of the HERIC inverter connected to a grid via an LCL filter; (ii) Modes of operation of HERIC for the levels 'V_{PV}', '-V_{PV}' and '0'; (iii) Generation of pulses for the switches Sw_1, Sw_2, Sw_3, Sw_4, Sw_5 and Sw_6 from the reference wave and carrier wave, the output voltage of the inverter 'v_{ab}', analytical waveforms of the terminal voltages 'v_{pg}' and 'v_{ng}' from the expressions.

$$v_{ag} = S_1 v_{pg} + S_2 v_{ng} \tag{2.19}$$

$$v_{bg} = S_3 v_{pg} + S_4 v_{ng} \tag{2.20}$$

Adding (2.19) and (2.20) and substituting in (2.6) gives

$$e_g = (S_1 + S_3) v_{pg} + (S_2 + S_4) v_{ng} \tag{2.21}$$

Substituting (2.1) in (2.21) and then simplifying gives,

$$v_{pg} = \frac{e_g + V_{PV}(S_2 + S_4)}{S_1 + S_2 + S_3 + S_4} \tag{2.22}$$

The switch pair (Sw_1, Sw_4) or (Sw_2, Sw_3) are turned ON along with the switch Sw_6 or Sw_5 in the active states (i.e., 'V_{PV}' or '$-V_{PV}$'). Substituting the switching states of these switches in (2.22) results in,

$$v_{pg} = 0.5 e_g + 0.5\, V_{PV} \tag{2.23}$$

During the '*0*' voltage level, the switches Sw_1, Sw_2, Sw_3 and Sw_4 are turned OFF and the other switches Sw_5 and Sw_6 are turned ON. From (2.22), the value of the terminal voltage 'v_{pg}' is equal to

$$v_{pg} = \infty \tag{2.24}$$

Fig. 2.4 (iii) shows the waveforms of the terminal voltages 'v_{pg}' and 'v_{ng}' obtained from the (2.22) and (2.1). It can be observed that the terminal voltages are free from the high-frequency switching transitions.

2.5. H6 inverter topology

The schematic of H6 inverter topology [24] connected to the grid via an LCL filter is shown in Fig. 2.5 (i). The H6 inverter topology consists of an H-bridge inverter with additional two switches Sw_5 and Sw_6. There is only one complementary switch pair (i.e., Sw_1 and Sw_3). The H6 inverter gives three levels in the output voltage. The modes of operation of the H6 inverter for the voltage levels 'V_{PV}', '*0*' and '$-V_{PV}$' is shown in Fig. 2.5 (ii). The voltage level 'V_{PV}' is obtained whenever the switches Sw_1, Sw_4 and Sw_5 are turned ON.

Similarly, the voltage level '-V_{PV}' is obtained, if the switches Sw_2 and Sw_6 are turned ON. During the '*0*' voltage level, the inverter output current freewheels among the switches Sw_1 and Sw_3. This results in the isolation of grid and PV array. Therefore, the H6 inverter uses the DC decoupling methodology for the minimization of leakage current in the PV systems.

The generation of pulses of the switches, output, and terminal voltage waveforms in the case of the H6 inverter is shown in Fig. 2.5 (iii). The H6 inverter requires two carrier waves which are level shifted by 1V. Whenever the magnitude of the reference wave is greater than the upper carrier wave, the switches Sw_4 and Sw_5 are turned ON. Similarly, whenever the magnitude of the reference wave is less than bottom carrier wave, the switches Sw_2 and Sw_6 are turned ON. The '*0*' voltage level occurs whenever the magnitude of reference wave lies in between both the carrier waves. The switch Sw_1 is kept in turned ON state during the positive half-cycle of the grid voltage. Similarly, the switch Sw_3 is kept in turned ON state during the negative half-cycle of the grid voltage. The H6 inverter output voltage oscillates within the levels 'V_{PV}' and '*0*' during the positive half-cycle of grid voltage. During the negative half-cycle of the grid voltage, the inverter output varies within levels '*0*' and '-V_{PV}'. The derivation of the terminal voltage is given below:

The pole voltages 'v_{ag}' and 'v_{bg}' are expressed in terms of the terminal voltages 'v_{pg}' and 'v_{ng}' as:

$$v_{ag} = S_1 S_5 v_{pg} + S_2 v_{ng} \tag{2.25}$$

$$v_{bg} = S_6 v_{pg} + S_4 v_{ng} \tag{2.26}$$

Adding (2.25) and (2.26) and substituting (2.6) gives

$$e_g = \left(S_6 + S_1 S_5\right) v_{pg} + \left(S_2 + S_4\right) v_{ng} \tag{2.27}$$

Substituting (2.1) in (2.27) and then simplifying gives,

$$v_{pg} = \frac{e_g + V_{PV}\left(S_2 + S_4\right)}{S_1 S_5 + S_2 + S_4 + S_6} \tag{2.28}$$

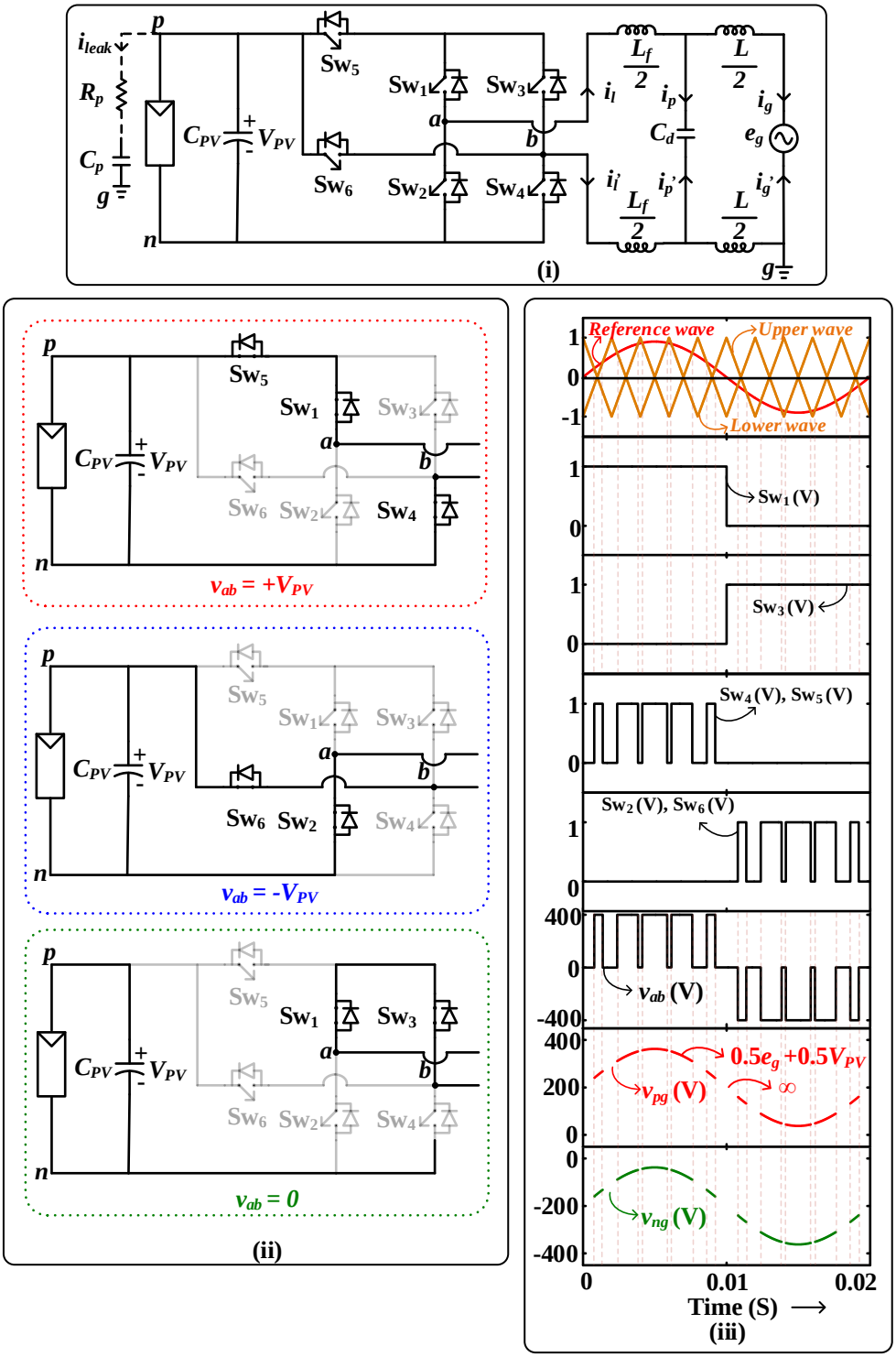


Fig.2.5 (i) Schematic of the H6 inverter connected to a grid via an LCL filter; (ii) Modes of operation of H6 for the levels 'V_{PV}', '$-V_{PV}$' and '0'; (iii) Generation of pulses for the switches Sw_1, Sw_2, Sw_3, Sw_4, Sw_5 and Sw_6 from the reference wave and carrier wave, the output voltage of the inverter v_{ab}, analytical waveforms of the terminal voltages 'v_{pg}' and 'v_{ng}' from the expressions.

The switch pair (Sw_1, Sw_4, Sw_5) or (Sw_2, Sw_6) are turned ON in the active states (i.e., 'V_{PV}' or '$-V_{PV}$'). Substituting the switching states of these switches in (2.28) results in,

$$v_{pg} = 0.5e_g + 0.5\, V_{PV} \tag{2.29}$$

During the '*0*' voltage level, all the switches are turned OFF except the switches Sw_1 and Sw_3. From (2.28), the magnitude of the terminal voltage 'v_{ag}' becomes:

$$v_{pg} = \infty \tag{2.30}$$

Fig. 2.5 (iii) shows the waveforms of the terminal voltages 'v_{pg}' and 'v_{ng}' obtained from the (2.28) and (2.1). It can be observed that the terminal voltages are free from the high-frequency switching transitions.

2.6. Neutral point clamped full-bridge topologies for transformerless PV grid-tied inverter proposed by Zhang *et.al.* [25]

The schematic of inverter topology [25] connected to the grid via an LCL filter is shown in Fig. 2.6 (i). The inverter topology consists of eight switches Sw_1 to Sw_8. The input PV voltage to the inverter is split into two halves with the help of two equal value capacitors as shown in Fig. 2.6 (i). The inverter topology [25] also generates three levels in the output voltage. The modes of operation of the inverter for the voltage levels 'V_{PV}', '*0*' and '$-V_{PV}$' is shown in Fig. 2.6 (ii). The voltage level 'V_{PV}' is obtained whenever the switches Sw_1, Sw_2, Sw_5 and Sw_6 are turned ON. Similarly, the voltage level '$-V_{PV}$' is obtained, if the switches Sw_3 and Sw_4 are turned ON. During the '*0*' voltage level, the inverter output current freewheels among the switches Sw_2, Sw_5, Sw_7 and Sw_8. This helps in the clamping the terminal voltage during zero state. Therefore, the given inverter topology uses neutral point clamped (NPC) methodology for the minimization of leakage current in the PV systems.

The generation of pulses for the switches, output, and terminal voltage waveforms of the given inverter is shown in Fig. 2.6 (iii). The inverter requires two carrier waves which are level shifted by 1V. Whenever the magnitude of the reference wave is greater than the upper carrier wave, the switches Sw_1, Sw_2, Sw_5 and Sw_6 are turned ON. Similarly, whenever the

magnitude of the reference wave is less than bottom carrier wave, the switches Sw_3 and Sw_4 are turned ON. The '*0*' voltage level occurs whenever the magnitude of reference wave lies in between both the carrier waves. The switches Sw_2 and Sw_5 are kept in turned ON state during the positive half-cycle of the grid voltage. Similarly, the switches Sw_7 and Sw_8 are kept in turned ON state during the negative half-cycle of the grid voltage. The given inverter output voltage oscillates within the levels 'V_{PV}' and '*0*' during a positive half-cycle of the grid voltage. During the negative half-cycle of the grid voltage, the inverter output varies within the levels of '*0*' and '-V_{PV}'. The derivation of the terminal voltage is given below:

The pole voltages 'v_{ag}' and 'v_{bg}' are expressed in terms of the terminal voltages 'v_{pg}' and 'v_{ng}' as:

$$v_{ag} = S_1 S_2 v_{pg} + S_3 v_{ng} + S_7 \left(v_{pg} - \frac{V_{PV}}{2} \right) \tag{2.31}$$

$$v_{bg} = S_4 v_{pg} + S_5 S_6 v_{ng} + S_8 \left(v_{pg} - \frac{V_{PV}}{2} \right) \tag{2.32}$$

Adding (2.31) and (2.32) and substituting (2.6) gives

$$e_g = \left(S_1 S_2 + S_4 \right) v_{pg} + \left(S_3 + S_5 S_6 \right) v_{ng} + \left(S_7 + S_8 \right) \left(v_{pg} - \frac{V_{PV}}{2} \right) \tag{2.33}$$

Substituting (2.1) in (2.33) and then simplifying gives,

$$v_{pg} = \frac{e_g + V_{PV} \left(S_3 + S_5 S_6 \right) + \frac{V_{PV}}{2} \left(S_2 S_7 + S_5 S_8 \right)}{S_1 S_2 + S_3 + S_4 + S_5 S_6 + S_7 + S_8} \tag{2.34}$$

The switch pair (Sw_1, Sw_2, Sw_5, Sw_6) or (Sw_3, Sw_4) are turned ON in the active states (i.e., 'V_{PV}' or '-V_{PV}'). Substituting the switching states of these switches in (2.34) results in,

$$v_{pg} = 0.5 e_g + 0.5\, V_{PV} \tag{2.35}$$

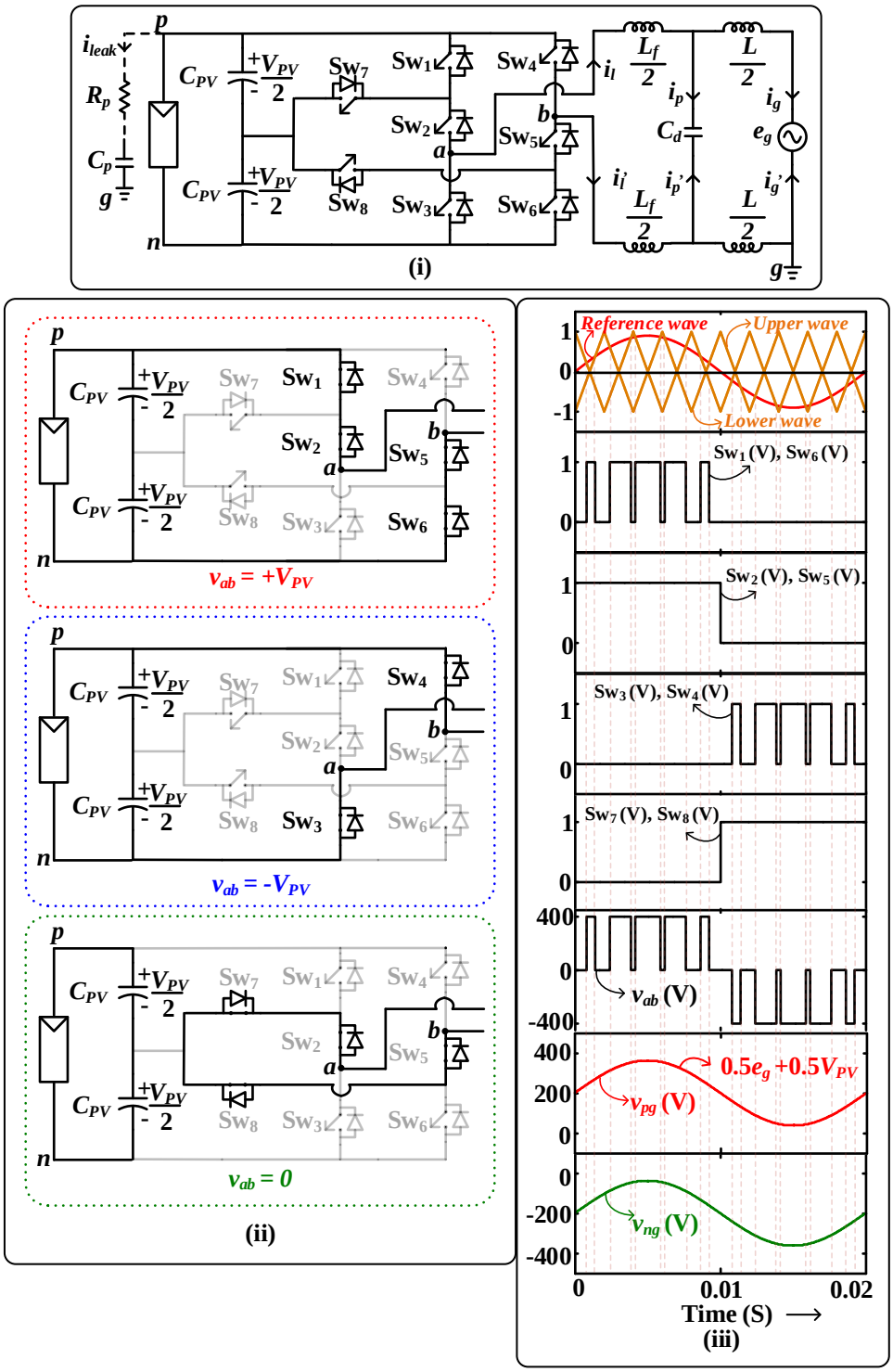


Fig.2.6. (i) Schematic of the PV inverter topology proposed by Zhang *et.al.* connected to a grid via an LCL filter; (ii) Modes of operation of H6 for the levels 'V_{PV}', '$-V_{PV}$' and '*0*'; (iii) Generation of pulses for the switches Sw_1, Sw_2, Sw_3, Sw_4, Sw_5, Sw_6, Sw_7 and Sw_8 from the reference wave and carrier wave, the output voltage of the inverter 'v_{ab}', analytical waveforms of the terminal voltages 'v_{pg}' and 'v_{ng}' from the expressions.

During the '*0*' voltage level, all the switches other than Sw_2, Sw_5, Sw_7 and Sw_8 are turned OFF. From (2.34), the magnitude of the terminal voltage 'v_{pg}' becomes:

$$v_{pg} = 0.5e_g + 0.5\,V_{PV} \tag{2.36}$$

Fig. 2.6 (iii) shows the waveforms of the terminal voltages 'v_{pg}' and 'v_{ng}' obtained from the (2.34) and (2.1). It can be observed that there is no undefined state in the terminal voltages.

2.7. H6-type transformerless single-phase inverter for grid-tied PV system by Islam *et.al.*[26]

The schematic of inverter topology [26], connected to the grid via an LCL filter, is shown in Fig. 2.7 (i). The given inverter topology consists of six switches Sw_1 to Sw_6. The given inverter topology also generates three levels in the output voltage. The modes of operation of the given inverter for the voltage levels 'V_{PV}', '*0*' and '$-V_{PV}$' are shown in Fig. 2.7 (ii). The voltage level 'V_{PV}' is obtained whenever the switches Sw_1, Sw_4 and Sw_6 are turned ON. Similarly, the voltage level '$-V_{PV}$' is obtained if the switches Sw_2, Sw_3 and Sw_5 are turned ON. For '*0*' voltage level, grid current is freewheeled through the switches Sw_5 and Sw_6. The switches Sw_5 and Sw_6 are kept turned ON during one-half cycle of the grid voltage and operate at a high switching frequency in the other half cycle respectively. During '*0*' voltage level, the grid inductor current 'i_l' free-wheels through the switches Sw_5 and Sw_6. The remaining switches Sw_1 to Sw_4 are turned OFF at the '*0*' voltage level. The turn-OFF of switches Sw_1 to Sw_4 during '*0*' voltage level results in the isolation of grid and PV array. Therefore, the given inverter topology uses AC decoupling methodology for the minimization of leakage current in the PV systems.

The generation of pulses for the switches, output voltage and terminal voltage waveforms for given inverter are shown in Fig. 2.7 (iii). The given inverter requires one reference wave and two carrier waves, which are level shifted by 1V. Whenever the magnitude of the reference wave is greater than the upper carrier wave, the switches Sw_1, Sw_4 and Sw_6 are turned ON. Similarly, whenever the magnitude of the reference wave is less than the bottom carrier wave, the switches Sw_2, Sw_3 and Sw_5 are turned ON. From the waveform of output voltage shown in Fig. 2.7 (iii), it can be observed that during the positive half-cycle of the grid voltage, the inverter output voltage varies between 'V_{PV}' and '*0*'. Similarly, in the

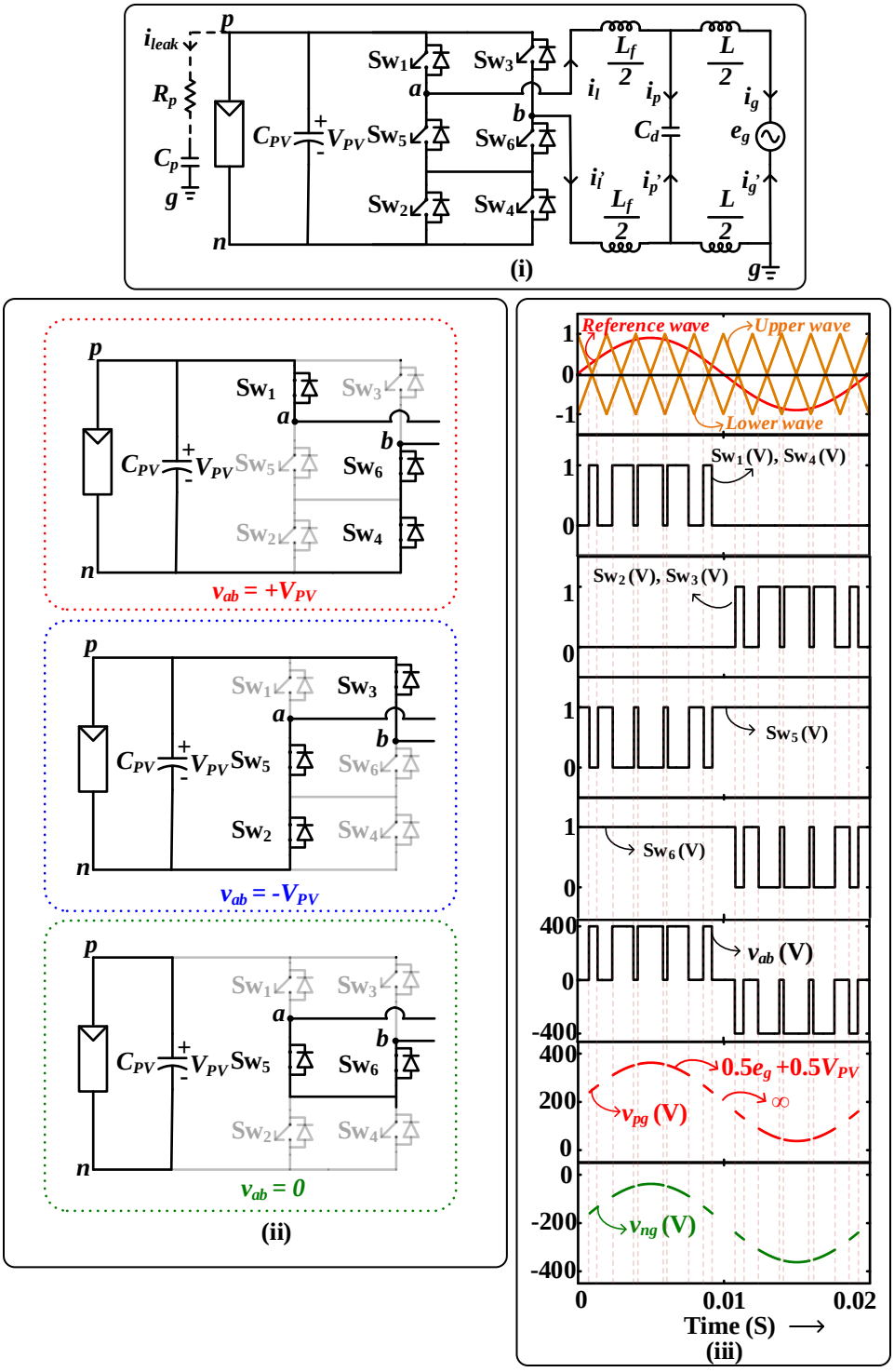


Fig.2.7. (i) Schematic of the PV inverter topology proposed by Islam *et.al*. connected to a grid via an LCL filter; (ii) Modes of operation of H6 for the levels 'V_{PV}', '-V_{PV}' and '*0*'; (iii) Generation of pulses for the switches Sw_1, Sw_2, Sw_3, Sw_4, Sw_5 and Sw_6 from the reference wave and carrier wave, the output voltage of the inverter 'v_{ab}', analytical waveforms of the terminal voltages 'v_{pg}' and 'v_{ng}' from the expressions.

negative half-cycle of the grid voltage, the inverter output varies within the levels of '*0*' and '-V_{PV}'. The derivation for the terminal voltage 'v_{pg}' for the inverter topology [26] is given below.

The pole voltages 'v_{ag}' and 'v_{bg}' are expressed in terms of the terminal voltages 'v_{pg}' and 'v_{ng}' as

$$v_{ag} = S_1 v_{pg} + S_2 S_5 v_{ng} \tag{2.37}$$

$$v_{bg} = S_3 v_{pg} + S_6 S_4 v_{ng} \tag{2.38}$$

Adding (2.37) and (2.38) and substituting in (2.6) gives

$$e_g = (S_1 + S_3) v_{pg} + (S_2 S_5 + S_4 S_6) v_{ng} \tag{2.39}$$

Substituting (2.1) in (2.39) and then simplifying gives,

$$v_{pg} = \frac{e_g + V_{PV}(S_5 S_2 + S_4 S_6)}{S_1 + S_3 + S_5 S_2 + S_4 S_6} \tag{2.40}$$

The switch pair (Sw_1, Sw_4, Sw_6) or (Sw_2, Sw_3, Sw_5) are turned ON in the active states (i.e., 'V_{PV}' or '-V_{PV}'). Substituting the switching states of these switches in (2.40) results in

$$v_{pg} = 0.5 e_g + 0.5\, V_{PV} \tag{2.41}$$

During the '*0*' voltage level, the switches Sw_1, Sw_2, Sw_3 and Sw_4 are turned OFF and the other switches Sw_5 and Sw_6 are turned ON. From (2.40), the value of the terminal voltage v_{pg} is equal to

$$v_{pg} = \infty \tag{2.42}$$

Fig. 2.7 (iii) shows the waveforms of the terminal voltages 'v_{pg}' and 'v_{ng}' obtained from the (2.40) and (2.1). It can be observed that the terminal voltages are free from the high-frequency switching transitions.

2.8. A quasi-unipolar SPWM full-bridge transformerless PV grid-connected inverter with constant common-mode voltage by Xiao *et. al.* [27]

The schematic of inverter topology [27] connected to the grid via an LCL filter is shown in Fig. 2.8 (i). The given inverter topology consists of an H-bridge inverter formed by switches Sw_1 to Sw_4, the AC-by-pass switches Sw_5 and Sw_6 and four diodes D_1 and D_4. The input PV voltage to the inverter is split into two halves with the help of two equal value capacitors as shown in Fig. 2.8 (i). The inverter topology [27] also generates three levels in the output voltage. The modes of operation of the inverter for the voltage levels 'V_{PV}', '*0*' and '$-V_{PV}$' is shown in Fig. 2.8 (ii). The voltage level 'V_{PV}' is obtained whenever the switches Sw_1 and Sw_4 are turned ON. Similarly, the voltage level '$-V_{PV}$' is obtained, if the switches Sw_2 and Sw_3 are turned ON. During '*0*' voltage level, the grid inductor current i_l free-wheels through the AC-by-pass switches Sw_5 and Sw_6. All the switches in H-bridge are turned OFF at the '*0*' voltage level. The turn-OFF switches in H-bridge during '*0*' voltage level result in the isolation of grid and PV array. Therefore, the given inverter topology uses NPC methodology for the minimization of leakage current in the PV systems.

The generation of pulses for the switches, output, and terminal voltage waveforms of given inverter is shown in Fig. 2.8 (iii). The inverter requires two carrier waves which are level shifted by 1V. Whenever the magnitude of the reference wave is greater than the upper carrier wave, the switches Sw_1 and Sw_4 are turned ON. Similarly, whenever the magnitude of the reference wave is less than bottom carrier wave, the switches Sw_2 and Sw_3 are turned ON. The '*0*' voltage level occurs whenever the magnitude of reference wave lies in between both the carrier waves. The switches Sw_1 and Sw_4 operate at higher switching frequency during the positive half-cycle of the grid voltage. Similarly, the switches Sw_2 and Sw_3 operate at higher switching frequency during the negative half-cycle of the grid voltage. The given inverter output voltage oscillates within the levels 'V_{PV}' and '*0*' during a positive half-cycle of the grid voltage. During the negative half-cycle of the grid voltage, the inverter output varies within the levels '*0*' and '$-V_{PV}$'. The derivation of the terminal voltage is given below:

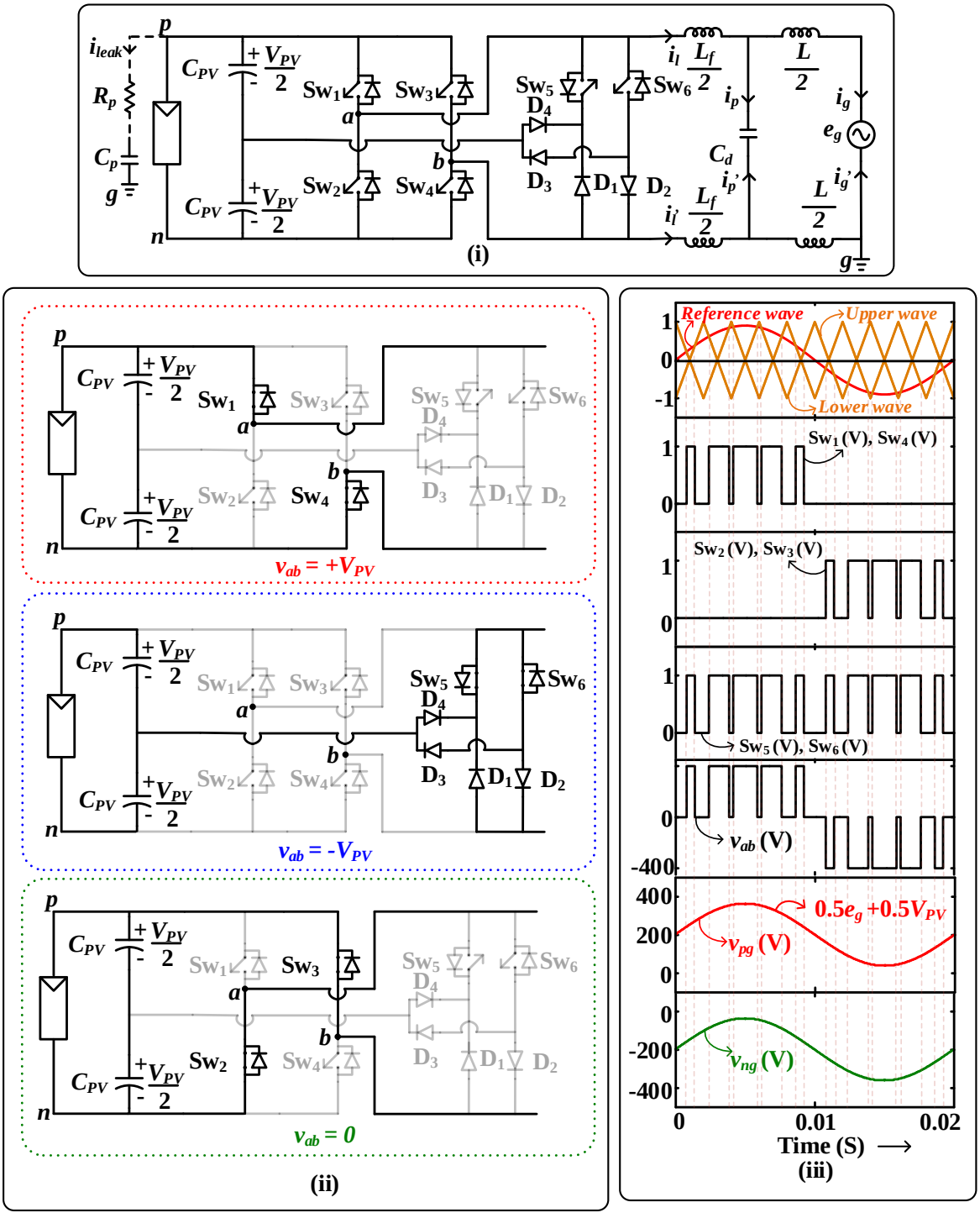


Fig.2.8. (i) Schematic of the PV inverter topology proposed by Xiao *et.al.* connected to a grid via an LCL filter; (ii) Modes of operation of H6 for the levels 'V_{PV}', '$-V_{PV}$' and '*0*'; (iii) Generation of pulses for the switches Sw_1, Sw_2, Sw_3, Sw_4, Sw_5 and Sw_6 from the reference wave and carrier wave, the output voltage of the inverter 'v_{ab}', analytical waveforms of the terminal voltages 'v_{pg}' and 'v_{ng}' from the expressions.

The pole voltages 'v_{ag}' and 'v_{bg}' are expressed in terms of the terminal voltages 'v_{pg}' and 'v_{ng}' as

$$v_{ag} = S_1 v_{pg} + S_2 v_{ng} + S_5 (1 - S_1) \left(v_{pg} - \frac{V_{PV}}{2} \right) \tag{2.43}$$

$$v_{bg} = S_3 v_{pg} + S_4 v_{ng} + S_6 (1 - S_3) \left(v_{pg} - \frac{V_{PV}}{2} \right) \tag{2.44}$$

Adding (2.43) and (2.44) and substituting (2.6) gives

$$e_g = (S_1 + S_3) v_{pg} + (S_2 + S_4) v_{ng} + (S_5 + S_6)(1 - S_1) \left(v_{pg} - \frac{V_{PV}}{2} \right) \tag{2.45}$$

Substituting (2.1) in (2.45) and then simplifying gives,

$$v_{pg} = \frac{e_g + V_{PV} (S_2 + S_4) + \frac{V_{PV}}{2} \left(S_5 (1\text{-}S_1) + S_6 (1\text{-}S_3) \right)}{S_1 + S_2 + S_3 + S_4 + S_5 (1\text{-}S_1) + S_6 (1\text{-}S_3)} \tag{2.46}$$

The switch pair (Sw_1, Sw_4) or (Sw_2, Sw_3) are turned ON in the active states (i.e., 'V_{PV}' or '-V_{PV}'). Substituting the switching states of these switches in (2.46) results in

$$v_{pg} = 0.5 e_g + 0.5\, V_{PV} \tag{2.47}$$

During the '*0*' voltage level, all the switches other than Sw_5 and Sw_6 are turned OFF. From (2.46), the magnitude of the terminal voltage 'v_{ag}' becomes:

. $$v_{pg} = 0.5 e_g + 0.5\, V_{PV} \tag{2.48}$$

Fig. 2.8 (iii) shows the waveforms of the terminal voltages 'v_{pg}' and 'v_{ng}' obtained from the (2.46) and (2.1). It can be observed that the there is no undefined state in the terminal voltages like the case of inverter topology proposed by Zhang *et.al*.

2.9. High efficiency single-phase transformerless PV H6 inverter with hybrid modulation method by Ji *et.al.* [28]

The schematic of inverter topology [28], connected to the grid via an LCL filter, is shown in Fig. 2.9 (i). The given inverter topology consists of six switches Sw_1 to Sw_6 and two diodes D_1 and D_2. The given inverter topology also generates three levels in the output voltage. The modes of operation of the given inverter for the voltage levels 'V_{PV}', '*0*' and '-V_{PV}' are shown in Fig. 2.9 (ii). The voltage level 'V_{PV}' is obtained whenever the switches Sw_1, Sw_4 and Sw_5 are turned ON. Similarly, the voltage level '-V_{PV}' is obtained if the switches Sw_2, Sw_3 and Sw_6 are turned ON. For '*0*' voltage level, grid current is freewheeled through the switches Sw_5 and Sw_6. The switches Sw_5 and Sw_6 are kept turned ON during the positive and negative half cycle of the grid voltage respectively. During '*0*' voltage level, the grid inductor current 'i_l' free-wheels through the switches Sw_5 and Sw_6. The remaining switches Sw_1 to Sw_4 are turned OFF at the '*0*' voltage level. The turn-OFF of switches Sw_1 to Sw_4 during '*0*' voltage level result in isolation of grid and PV array. Therefore, the given inverter topology uses AC decoupling methodology for the minimization of leakage current in the PV systems.

The generation of pulses for the switches, output voltage and terminal voltage waveforms for given inverter are shown in Fig. 2.9 (iii). The given inverter requires one reference wave and two carrier waves, which are level shifted by 1V. Whenever the magnitude of the reference wave is greater than the upper carrier wave, the switches Sw_1, Sw_4 and Sw_5 are turned ON. Similarly, whenever the magnitude of the reference wave is less than the bottom carrier wave, the switches Sw_2, Sw_3 and Sw_6 are turned ON. From the waveform of output voltage shown in Fig. 2.9 (iii), it can be observed that during the positive half-cycle of the grid voltage, the inverter output voltage varies between 'V_{PV}' and '*0*'. Similarly, in the negative half-cycle of the grid voltage, the inverter output varies within the levels '*0*' and '-V_{PV}'. The derivation for the terminal voltage 'v_{pg}' for the given inverter topology is given below.

The pole voltages 'v_{ag}' and 'v_{bg}' are expressed in terms of the terminal voltages 'v_{pg}' and 'v_{ng}' as

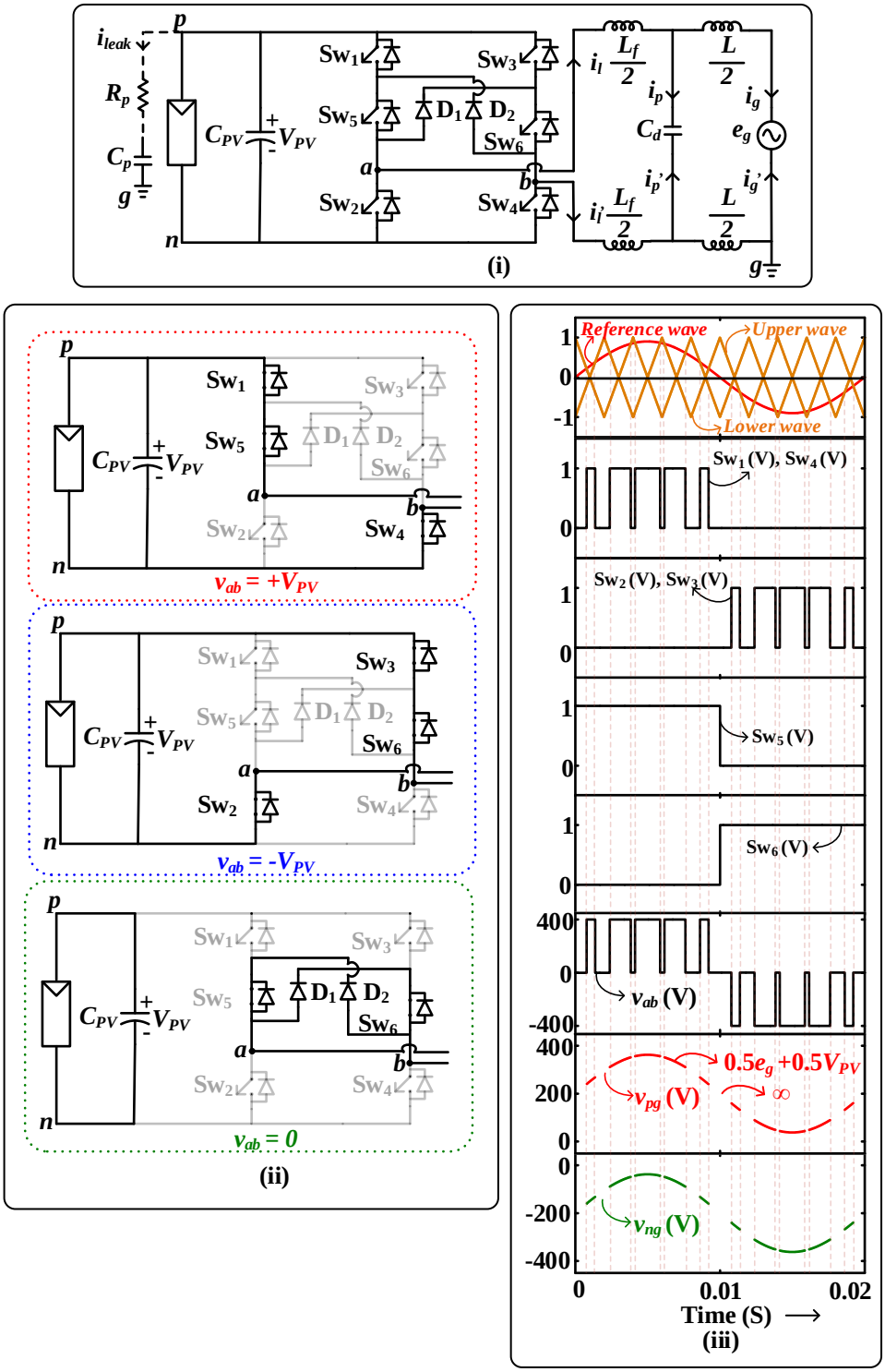


Fig.2.9. (i) Schematic of the PV inverter topology proposed by Ji.*et.al*. connected to a grid via an LCL filter; (ii) Modes of operation of H6 for the levels 'V_{PV}', '-V_{PV}' and '*0*'; (iii) Generation of pulses for the switches Sw_1, Sw_2, Sw_3, Sw_4, Sw_5 and Sw_6 from the reference wave and carrier wave, the output voltage of the inverter 'v_{ab}', analytical waveforms of the terminal voltages 'v_{pg}' and 'v_{ng}' from the expressions.

$$v_{ag} = S_1 v_{pg} + S_2 S_5 v_{ng} \tag{2.49}$$

$$v_{bg} = S_3 v_{pg} + S_6 S_4 v_{ng} \tag{2.50}$$

Adding (2.49) and (2.50) and substituting in (2.6) gives

$$e_g = (S_1 + S_3) v_{pg} + (S_2 S_5 + S_4 S_6) v_{ng} \tag{2.51}$$

Substituting (2.1) in (2.51) and then simplifying gives,

$$v_{pg} = \frac{e_g + V_{PV}(S_3 + S_4)}{S_1 S_5 + S_2 S_6 + S_3 + S_4} \tag{2.52}$$

The switch pair (Sw_1, Sw_4, Sw_5) or (Sw_2, Sw_3, Sw_6) are turned ON in the active states (i.e., 'V_{PV}' or '$-V_{PV}$'). Substituting the switching states of these switches in (2.52) results in

$$v_{pg} = 0.5 e_g + 0.5\, V_{PV} \tag{2.53}$$

During the '*0*' voltage level, the switches Sw_1, Sw_2, Sw_3 and Sw_4 are turned OFF and the other switches Sw_5 and Sw_6 are turned ON. From (2.52), the value of the terminal voltage 'v_{pg}' is equal to

$$v_{pg} = \infty \tag{2.54}$$

Fig. 2.9 (iii) shows the waveforms of the terminal voltages 'v_{pg}' and 'v_{ng}' obtained from the (2.52) and (2.1). It can be observed that the terminal voltages are free from the high-frequency switching transitions.

Apart from the minimization of leakage current, the losses in the PV inverter configuration plays a dominant role in choosing the inverter topology. Therefore, it becomes important to study the losses of the various PV inverter topologies. The next section describes the switching and conduction losses of the discussed PV inverter topologies.

2.10. Switching and conduction losses of various PV inverter topologies

The switching and conduction losses for the various PV inverter topologies discussed in the chapter are also calculated [28-29]. The parameters used for the calculation of switching and conduction losses are given in Table 2.1. Fig. 2.10 shows the bar graph of the (i) conduction and (ii) switching losses of the switches used in various PV inverter topologies discussed in this chapter.

TABLE 2.1. PARAMETERS CONSIDERED FOR THE CALCULATION OF SWITCHING AND CONDUCTION LOSSES

Parameter	P	V_{DC}	f_{sw}	e_g	f_g
Value	2.5kW	400V	10kHz	230V	50Hz

The switching and conduction losses of the switches in the unipolar and bipolar PWM technique are almost the same. However, the overall efficiency of the bipolar scheme is quite low. This can be attributed to the power fed back during the turn-OFF period of the switching cycle, which decreases the effective power transfer from the PV to the grid. Apart from this, it has a disadvantage of increased core losses in the filter inductor [30] due to two-level operation.

In the case of H5 inverter topology, due to the high-frequency operation of the switch Sw_5 in both the half cycles of the grid voltage, the switching loss of switch Sw_5 is quite high. The top switches of both the legs of the inverter are kept in a turn-ON state during the free-wheeling period for both the cycles of the output voltage. This results in higher conduction losses as can be observed in Fig. 2.10. In the case of HERIC configuration, inverter isolates the PV array and the grid/load during the freewheeling period. This is achieved by turning OFF the inverter switches during turn-OFF or free-wheeling period of the switching cycle. The output current free-wheels through the AC-bypass switches Sw_5 and Sw_6. These switches operate during the free-wheeling period in both the half cycles of the grid voltage. However, the output current flows through the switches Sw_5 and Sw_6 only during zero state. As a result, the conduction loss of these switches is almost same as the Sw_1 and Sw_4 in the H-bridge. The switches Sw_1 and Sw_4 in the H-bridge operate at high switching frequency in one of the

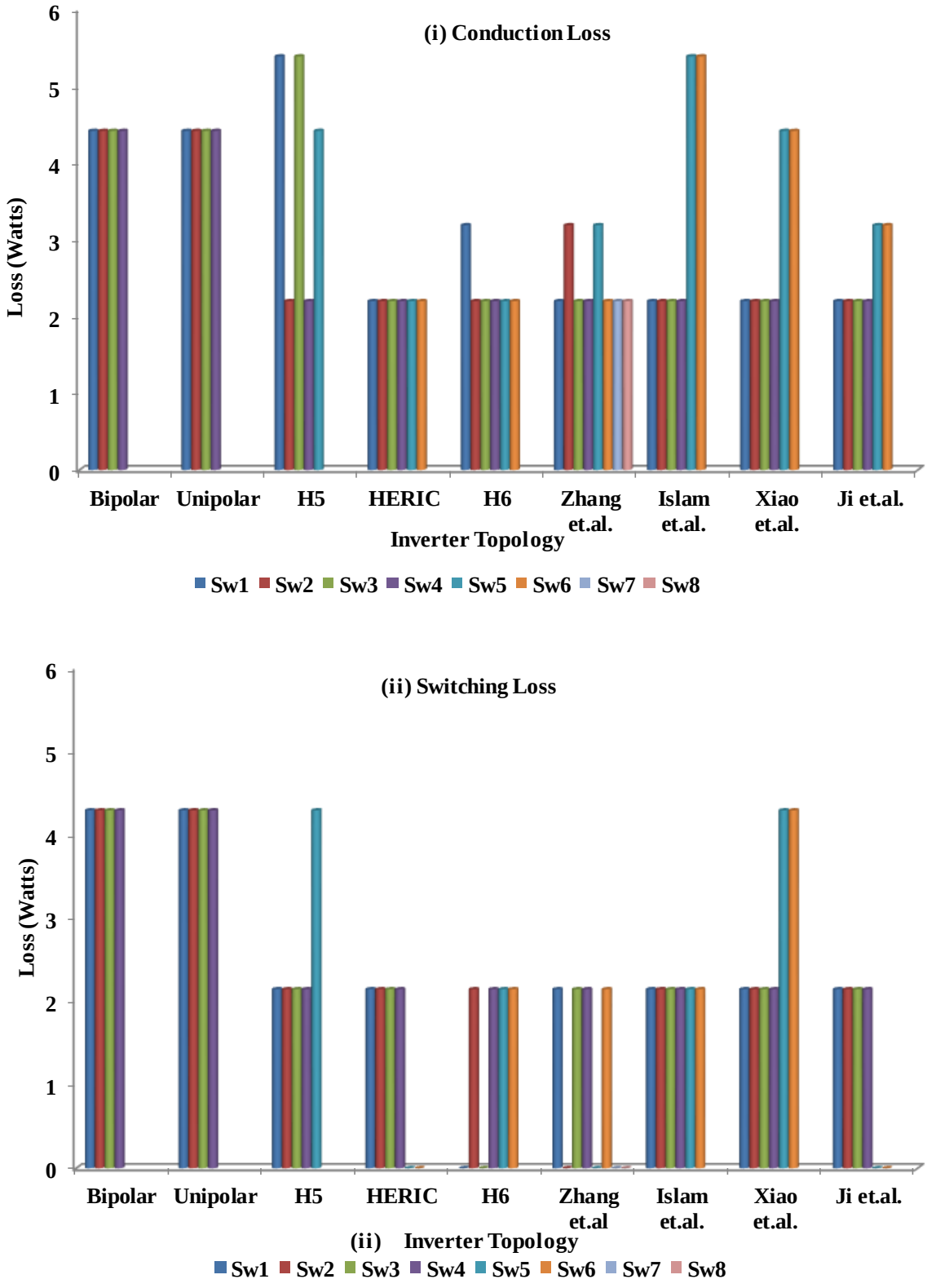


Fig.2.10. Bar graphs showing the (i) conduction loss; (ii) switching loss for the switches in various inverter topologies discussed.

positive half-cycle and turned OFF during the negative half-cycle. The other pair of switches Sw_2 and Sw_3 operate at high switching frequency in the negative half-cycle and turned OFF during the positive half-cycle. Due to this, the switching and conduction losses of the switches Sw_1 - Sw_4 are almost the same in the case of HERIC inverter topology. In the case of H6 inverter topology, the switch Sw_1 operates at low-frequency (grid-frequency). As a result, the conduction loss of the switch Sw_1 is high as seen in Fig 2.10. The other switch Sw_3 also operates at low-frequency. The output current flows through Sw_3 only at the zero voltage level and the voltage '$-V_{PV}$', the switch remains in turn ON state and no current flows through the switch. Hence the conduction loss of the switch Sw_3 is less than the switch Sw_1. The switches Sw_4 and Sw_5 operate at high-frequency during the positive half-cycle and remain turned OFF during the negative half-cycle. The other switches Sw_2 and Sw_6 operate at high-frequency during the negative half-cycle and remain turned OFF in the positive half-cycle. So the switches Sw_2, Sw_4, Sw_5 and Sw_6 have almost similar switching and conduction losses.

In the case of PV inverter topology proposed by Zhang *et.al.*, the switches Sw_1 and Sw_6 operate at higher switching frequency in the positive half-cycle and remains turned OFF during the negative half-cycle. The other pair of switches Sw_3 and Sw_4 operate at higher switching frequency in the negative half-cycle and remains turned OFF during the positive half-cycle. Because of which, the switching and conduction losses of switches Sw_1, Sw_3, Sw_4 and Sw_6 are same. The switches Sw_2 and Sw_5 remain turned ON in the positive half-cycle. As a result, the conduction loss of these two switches are high. The remaining switches Sw_7 and Sw_8 are turned ON only in negative half-cycle. But the output current flows through these two switches only during zero state. As a result, the conduction loss of these two switches Sw_7 and Sw_8 is same as the switches Sw_1, Sw_3, Sw_4 and Sw_6. In the PV inverter topology proposed by Islam *et.al.*, The switch pair Sw_1 and Sw_6 operate at a high switching frequency in the positive half - cycle and remains turned OFF in negative half-cycle. Similarly, the other switch pair Sw_1 and Sw_6 operate at a high - switching frequency in negative half-cycle and remains turned OFF in the positive half - cycle. This results in equal switching and conduction losses in these four switches. The switch Sw_5 is kept turned ON completely during the positive half-cycle and operate at a high switching frequency in the negative half-cycle. Similarly, the switch Sw_6 is kept turned ON completely during the negative half-cycle and operate at a high switching frequency in the positive half-cycle. As a result, the conduction

losses of the switches Sw_5 and Sw_6 are high. In addition to conduction loss, the switches Sw_5 and Sw_6 have same switching losses as the switches Sw_1, Sw_2, Sw_3 and Sw_4.

By using the PV inverter topology proposed by Xiao *et.al.*, the switch pair (Sw_1, Sw_4) or (Sw_2, Sw_3) operate in higher switching frequency in one half-cycle and remains turned OFF in the other half - cycle. Thus, the switching and conduction losses of the switches Sw_1, Sw_2, Sw_3 and Sw_4 are same. The remaining two switches Sw_5 and Sw_6 operate at a high switching frequency in both half cycles. Therefore, the switching and conduction losses of the switches Sw_5 and Sw_6 are high compared to the remaining switches in the PV inverter topology. In the PV inverter topology proposed by Ji *et.al.*, the switch pair Sw_1 and Sw_4 operate at a high switching frequency in the positive half-cycle and remains turned OFF in negative half-cycle. Similarly, the other switch pair Sw_2 and Sw_3 operate at a high-switching frequency in negative half-cycle and remains turned OFF in the positive half-cycle. As a result, the switching and conduction losses of the switches Sw_1, Sw_2, Sw_3 and Sw_4 are same. The other switches Sw_5 and Sw_6 operate at the fundamental frequency. Hence the conduction loss of the switches Sw_5 and Sw_6 are high. Apart from the switching and conduction losses of the PV inverter topologies, a detailed comparison of various PV inverter topologies discussed is given in the next section.

2.11. Comparison of various PV inverter topologies

Based on the information obtained from the operation and loss calculation, a comparison of the various PV inverter topologies discussed is given in Table 2.2. The comparison is made based on a number of switches and diodes used in topology, number of levels in output voltage, asymmetry in the inverter operation, etc. Further, PV inverter topologies discussed are classified depending on the technique used for the minimization of leakage current. The basic topologies like full-bridge inverter with bipolar and unipolar PWM techniques are not using any decoupling methodologies for the minimization of leakage current. The topologies like H5, H6 use DC decoupling methodology for the minimization of leakage current. While the remaining inverter configurations use AC and NPC decoupling methodologies for the minimization of leakage current as given in Table 2.2. And from the economic point of view in terms of the number of switches, bipolar and unipolar schemes are economical compared to the other topologies shown in Table 2.2. In terms of the switching

TABLE 2.2 COMPARISON OF VARIOUS PV INVERTER TOPOLOGIES

Inverter Topology	**A**	**B**	**C**	**D**	**E**	**F**	**G**	**H (Watts)**	**I**	**J**	**K**	**L**	**M (Watts)**	**N**	**O**
Bipolar	-	4	-	No	2	2	-	17.672	4	4	0	0	17.16	No	2
Unipolar	-	4	-	No	2	2	2	17.672	4	4	0	0	17.16	No	3
H5	DC	5	-	No	3	3	2	19.614	3	3	1	1	12.87	Yes	3
HERIC	AC	6	-	No	2	2	2	13.2	2	2	1	1	8.58	Yes	3
H6	DC	6	-	Yes	3	2	2	14.189	2	2	1	1	8.58	Yes	3
Zhang *et.al*	NPC	8	-	Yes	4	2	4	19.578	2	2	2	2	9.66	No	3
Islam *et.al.*	AC	6	-	No	3	3	2	19.578	3	3	1	1	12.87	Yes	3
Xiao *et.al.*	NPC	6	4	No	2	2	2	17.636	4	4	-	-	17.16	No	3
Ji *et.al.*	AC	6	2	No	3	3	2	15.178	2	2	1	1	8.58	Yes	3

A- Decoupling methodology used.

B- Number of switches used in topology.

C- Number of diodes used (other than the switch body diode)

D- Asymmetry in the inverter operation during positive and negative half cycles of the grid voltage.

E- Number of switches and diodes conducting during the positive voltage level.

F- Number of switches and diodes conducting during the negative voltage level.

G- Number of switches and diodes conducting in the '*0*' voltage level.

H- Total conduction loss for the inverter topology.

I- Number of switches operating at a higher frequency during the positive half-cycle of the grid voltage.

J- Number of switches operating at a higher frequency during the negative half-cycle of the grid voltage.

K- Number of switches operating at the fundamental frequency of the grid voltage during the positive half-cycle.

L- Number of switches operating at the fundamental frequency during the negative half-cycle of the grid voltage

M- Total switching loss for the inverter topology.

N- Undefined states in the terminal voltage.

O- Number of levels in the output voltage.

and conduction losses, HERIC inverter topology has low losses compared to the other inverter topologies. Further, there is an asymmetry in the operation during the positive and negative half cycles of the output voltage, for the inverter topology proposed by Zhang *et.al.* and H6 inverter topology. This may result in DC offset in the inverter output voltage. From Table 2.2., it can be observed that the inverter topologies proposed by Zhang *et.al.* and Xiao *et.al.* don't have any undefined state in the terminal voltage because of neutral point clamping.

Finally, from Table 2.2, the following conclusions can be observed

i. Among all the PV inverter topologies discussed, the full-bridge inverter with bipolar and unipolar PWM technique is economical.
ii. However, using the full-bridge inverter with unipolar PWM technique, the magnitude of leakage current is quite high which restricts its application in PV systems.
iii. In the case of the full-bridge inverter with bipolar PWM technique, the magnitude of leakage current is very less. But the number of levels in the output voltage are two, which results in higher THD in the output current.
iv. Among the topologies discussed, the HERIC topology is efficient. However, the given topology uses six switches for the generation of three-levels in the output voltage.

2.12. Motivation

Based on the above literature review, the following observations were made for the various transformerless PV inverter topologies:

i. Most of the PV inverter topologies discussed in the literature are given for three-level operation only. Further, the given topologies cannot be extended for higher-level operation in the output voltage.
ii. The topologies discussed in the literature require additional semiconductor devices for obtaining low-frequency in the terminal voltage. So these topologies are not economical.
iii. Apart from the additional semiconductor devices, some of the inverter topologies discussed require complex clamping circuitry for maintaining the terminal voltage low-frequency. This further increases the cost of the system.
iv. At last, not least most of the PV inverter topologies discussed above have high switching and conduction losses. This make the complete PV system inefficient.

2.13. Objectives

The objectives of the research work presented in this thesis are as follows:

i. To meet the objective of low cost and efficient operation, a new CMLI for single-phase PV system is presented. The complete details of the operation of the proposed CMLI in symmetrical and asymmetrical modes along with its extension to the higher number of levels with simulation and experimental results are discussed in the thesis. The comparison of proposed CMLI with the other existing MLI topologies in the literature is also presented. However, the proposed CMLI using the existing PWM techniques requires additional circuitry to minimize the magnitude of leakage current flowing in the system.

ii. A new PWM scheme is proposed for single-phase five-level CMLI for the minimization of leakage current. The proposed PWM is also integrated with the MPPT algorithm and is applied to a five-level CMLI. The proposed PWM technique minimizes leakage current of PV panels and reduces the size of the electromagnetic interference filter required in the system without the addition of any switches. Furthermore, the analysis of the terminal voltage across the PV array and the common mode voltage of the inverter based on the switching function is presented. Besides, the proposed PWM technique require reduced number of carrier waves compared to the conventional sinusoidal pulse width modulation technique for the given CMLI. However, using the proposed PWM technique for the single-phase five-level CMLI, the objective of high efficiency is not achieved.

iii. To overcome this drawback, a new efficient and reliable transformerless PV MLI configuration is proposed for the minimization of the leakage current in the single-phase systems. Apart from a reduced switch count, the proposed CMLI topology has additional features of low switching and conduction losses. The proposed topology with the given pulse width modulation PWM technique reduces the high-frequency voltage transitions in the terminal and common-mode voltages. Furthermore, the extension of the proposed CMLI along with the PWM technique for higher levels in the output voltage is also presented. A comparison of the proposed CMLI with the existing PV multilevel inverter topologies is also presented.

iv. Apart from single-phase PV inverter topologies, a solution for the three-phase transformerless PV inverter topologies is also presented in the thesis. The new three-phase transformerless MLI topologies based on DC and NPC DC decoupling methodologies are presented for the minimization of leakage current. The leakage current in the three-phase MLI topology is minimized by reducing the transitions in the terminal voltage of the PV panel. The complete details of the proposed three-phase transformerless MLI, analysis of the terminal voltage using switching functions, simulation and experimental were presented in the thesis.

CHAPTER 3

A New Low Cost and Efficient Cascaded Half-Bridge Multi-Level Inverter with Reduced Number of Switches

Chapter 3

A New Low Cost and Efficient Cascaded Half-Bridge Multi-Level Inverter with Reduced Number of Switches

In order to meet the objective of economical and efficient inverter topology, a new low cost and efficient CMLI configuration is proposed in this chapter. The proposed CMLI configuration requires less number of switching devices and isolated power supplies compared to the other basic MLIs given in the literature. Besides this, the proposed CMLI eliminates the problem related to neutral point fluctuations, DC offset current, diode reverse recovery as observed in the conventional neutral point clamped and flying capacitor configurations. Further, the given CMLI has the advantage of low conduction and switching losses. Thus, the proposed CMLI has the advantages of low cost and better efficiency. This chapter also gives the generalized version of the proposed configuration for '*2m+1*' levels. All the details regarding circuit schematic, modes of operation (symmetric and asymmetric operation) with simulation and experimental results are presented in this chapter.

3.1. Operation of the proposed CMLI

The circuit schematic for the proposed nine-level CMLI configuration is given in Fig. 3.1. The given topology consists of ten switches and four isolated power supplies. The pair of switches in each leg (Sw_1, Sw_2), (Sw_3, Sw_4), (Sw_5, Sw_6) and (Sw_7, Sw_8) operate in

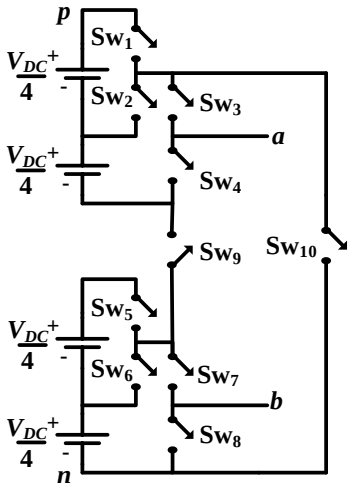


Fig. 3.1. Proposed cascaded multi-level inverter configuration with reduced switches.

a complementary mode with high-frequency and the switches Sw_9 and Sw_{10} are operated at the fundamental frequency of the reference voltage. Thus, these switches have a negligible switching loss. Further, as only five switches are conducting in a given state, the proposed configuration has the advantage of lower conduction losses compared to configuration given by E. Babaei *et.al.* [31].

In all, the proposed CMLI is the low-cost solution with better efficiency. Further, the proposed configuration can be used for both the symmetrical and asymmetrical operation. Details of the symmetrical and asymmetrical operation of the proposed CMLI are discussed in the next sub-section.

3.1.1 Operation of proposed CMLI in symmetrical case

During symmetrical CMLI configuration, the value of all the DC voltage sources considered is equal. For example 'V_1', 'V_2', 'V_3' and 'V_4' are four DC voltage sources, then for symmetrical configuration

$$V_1 = V_2 = V_3 = V_4 = \frac{V_{DC}}{4} \tag{3.1}$$

where 'V_{DC}' is the total DC bus voltage .The equal value of DC voltages limits the number of levels in the output voltage 'v_{ab}' of the proposed CMLI. There are nine levels in the output voltage during symmetrical operation. The output voltage 'v_{ab}' attains the level '$+V_{DC}$', if the

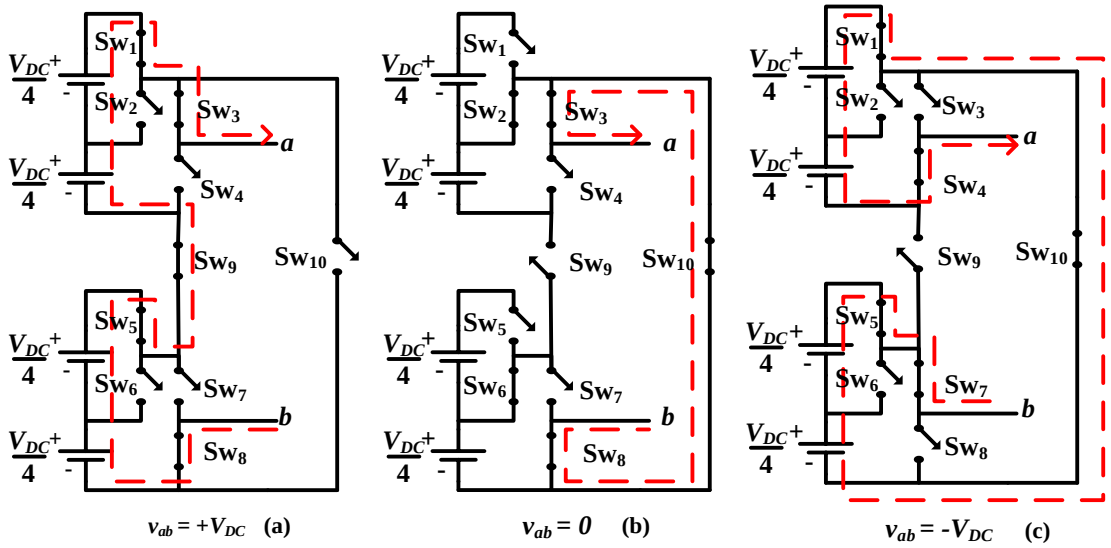


Fig. 3.2 Operation of proposed CMLI in the symmetrical operation for phase voltage levels (a) '+ V_{DC}'; (b) '*0*'; (c) '-V_{DC}'.

switches Sw_1, Sw_3, Sw_5, Sw_8, Sw_9 are turned ON. Fig. 3.2 shows the operation of the proposed CMLI in the symmetrical case for the output voltage levels of '$+V_{DC}$', '*0*' and '$-V_{DC}$'. Table 3.1 gives the details of the switching states and their respective output voltage levels for the proposed CMLI in the symmetrical operation.

TABLE 3.1. SWITCHING STATES AND THEIR RESPECTIVE VOLTAGE LEVELS IN THE CMLI DURING SYMMETRICAL OPERATION

Sw_1	**Sw_3**	**Sw_5**	**Sw_7**	**Sw_9**	**Output voltage level v_{ab}**
1	1	1	0	1	$+V_{DC}$
0	1	1	0	1	$+3V_{DC}/4$
0	1	0	0	1	$+1V_{DC}/2$
0	1	0	1	1	$+1V_{DC}/4$
0	0	0	1	1	*0*
0	1	0	0	0	*0*
0	1	0	1	0	$-1V_{DC}/4$
0	1	1	1	0	$-1V_{DC}/2$
0	0	1	1	0	$-3V_{DC}/4$
1	0	1	1	0	$-V_{DC}$

3.1.2 Operation of proposed CMLI in asymmetrical case

In asymmetrical CMLI configuration, the value of all the DC voltage sources are not necessary to be equal. Now to show the operation of proposed CMLI in asymmetrical case, the voltage values of DC sources can be taken as

$$V_1 = V_2 = \frac{V_{DC}}{3} \text{ and } V_3 = V_4 = \frac{V_{DC}}{6} \tag{3.2}$$

Fig. 3.3 shows the proposed asymmetrical multilevel inverter topology for thirteen-level operation. The output voltage attains the level '$+5V_{DC}$ /6', if switches Sw_1, Sw_3, Sw_6, Sw_8, Sw_9 are turned ON. Fig. 3.4 shows the operation of the proposed CMLI in the asymmetrical case for the output phase voltage levels of '$+5V_{DC}$/6', '*0*' and '$–5V_{DC}$/6'. To summarize all the possible voltage levels with their details of the switching states are given in Table 3.2 for the proposed CMLI in asymmetrical operation.

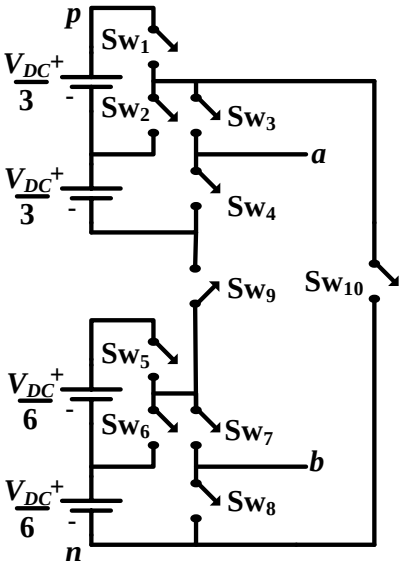


Fig. 3.3 Proposed cascaded multi-level inverter configuration in asymmetrical case.

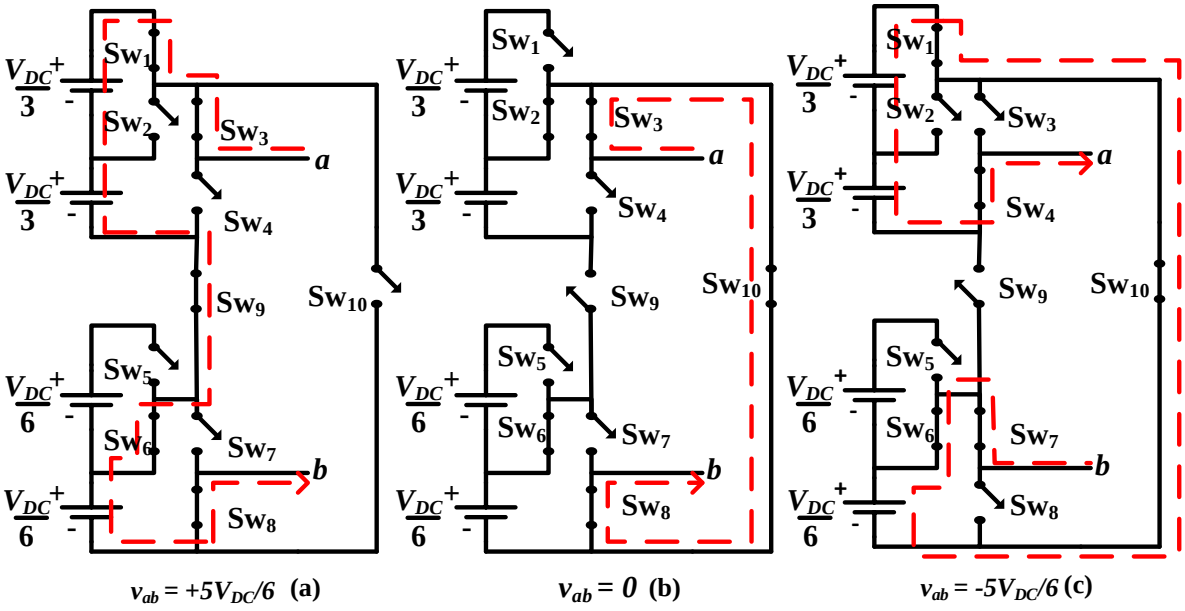


Fig. 3.4 Operation of proposed CMLI in the asymmetrical case for output voltage levels (a) '+5V_{DC} /6'; (b) '*0*'; (c) '-5V_{DC} /6'.

TABLE 3.2. SWITCHING STATES AND THEIR RESPECTIVE VOLTAGE LEVELS IN THE CMLI DURING ASYMMETRICAL OPERATION

Sw_1	Sw_3	Sw_5	Sw_7	Sw_9	Output voltage level v_{ab}
1	1	1	0	1	$+V_{DC}$
1	1	0	0	1	$+5V_{DC}/6$
1	1	0	1	1	$+4V_{DC}/6$
0	1	0	0	1	$+3V_{DC}/6$
0	0	1	0	1	$+2V_{DC}/6$
0	0	0	0	1	$+1V_{DC}/6$
0	0	0	0	1	*0*
0	1	0	0	0	*0*
0	1	0	1	0	$-1V_{DC}/6$
0	1	1	1	0	$-2V_{DC}/6$
0	0	0	1	0	$-3V_{DC}/6$
0	0	1	1	0	$-4V_{DC}/6$
1	0	0	1	0	$-5V_{DC}/6$
1	0	1	1	0	$-V_{DC}$

3.2. Generalized configuration of proposed CMLI for symmetrical operation

The proposed configuration can be extended to '*2m+1*' levels by cascading the individual two-level inverters where '*m*' is the number of DC sources used in the topology. The value of '*m*' is an even number and it starts from '*m*' =2. Fig. 3.5 shows the generalized configuration of proposed CMLI for symmetrical operation. The expression for output voltage 'v_{ab}' for generalized configuration is given by

$$v_{ab}=(V_1S_1+V_2S_3+.....V_{m/2}S_{m-1}+.....V_m\overline{S_{2m-1}})S_{2m+1}- (V_1S_1+V_2S_3+.....V_{m/2}\overline{S_{m-1}}+.....V_mS_{2m-1})\overline{S_{2m+1}} \quad (3.3)$$

where 'V_1', 'V_2',….. 'V_m' are the magnitudes of DC voltage sources used and S_1, S_3,…….. S_{2m+1} are the switching states of the switches Sw_1, Sw_3,…….. Sw_{2m+1} whose value is equal to '*1*' if the corresponding switch is turned ON else equal to '*0*'. The expression for the number of switches used in proposed CMLI for '*2m+1*' levels is given by,

$$N_{switch} = 2(m+1) \tag{3.4}$$

As there are '$m+1$' pairs of complementary switches, so the number of switches conducting is always half of the total number of switches used in the configuration. Thus, the expression for number of switches conducting $N_{conducting}$ in the CMLI is given by

$$N_{conducting} = m+1 \tag{3.5}$$

The forward blocking voltage V_{Block} for the switches used in the topology can be calculated using (3.6) to (3.8)

For the low-frequency switches Sw_{2m+1} and Sw_{2m+2}

$$V_{Block} = \sum_{k=1}^{m} V_k \tag{3.6}$$

Blocking voltage of the upper cell switches Sw_e and Sw_{e-1} where 'e' = 2,4... m is given by

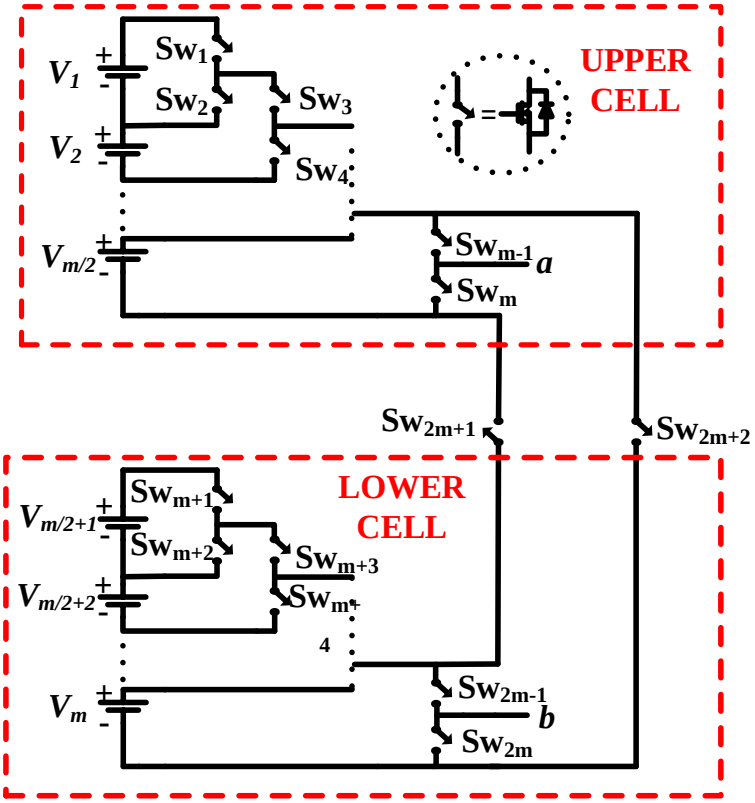


Fig. 3.5 Generalized structure of proposed CMLI for '$2m+1$' levels.

$$V_{Block} = \sum_{k=1}^{e/2} V_k \tag{3.7}$$

Similarly, blocking voltage for the lower cell Sw_{2e} and Sw_{2e-1} is given by

$$V_{Block} = \sum_{k=e/2+1}^{e} V_k \tag{3.8}$$

where '*e*' = *m*/2+2, *m*/2+4, …….2*m*.

3.3. Comparison of proposed CMLI with the existing topologies

The proposed CMLI is compared with the various existing MLIs in terms of power semiconductor device count, number of switches conducting etc. Fig. 3.6 shows the number of voltage levels versus the total number of switches used in different MLIs operated in symmetrical mode. For a thirteen-level output, the number of switches used in the proposed MLI is fourteen, which is less when compared to the other MLIs. The number of switches used is twenty four in case conventional MLIs and eighteen in case of the configuration proposed by E.Babaei *et.al.* [31]. The proposed configuration eliminates the requirement of clamping diodes [32], balancing capacitors [33] which are used in basic MLI.

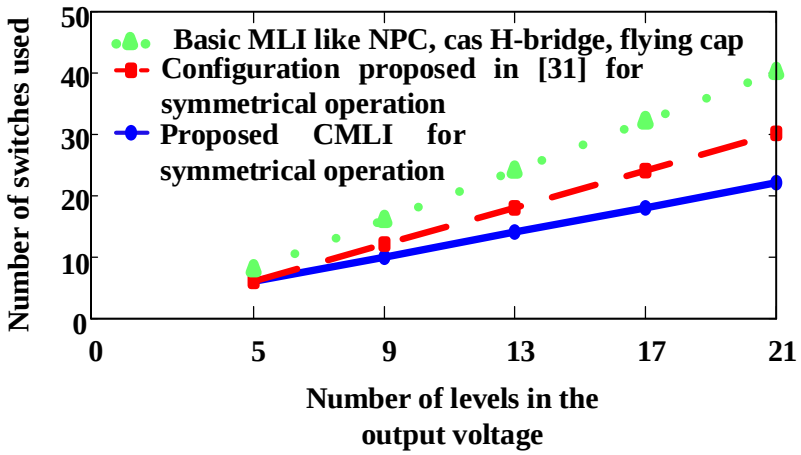


Fig. 3.6 Comparison of number of switches used in the proposed topology with other MLIs.

The proposed CMLI is also compared with respect to conduction losses. Fig. 3.7 shows the number of voltage levels versus the number of switches conducting for different inverter topologies in symmetrical operation. For a nine-level CMLI, the number of switches conducting is five. The number of switches conducting in the configuration proposed by

E.Babaei *et.al.* [31] is six, whereas in the other basic nine-level MLIs the number of switches conducting is sixteen. Hence, the proposed configuration has the advantages of low conduction loss and reduced number of switches.

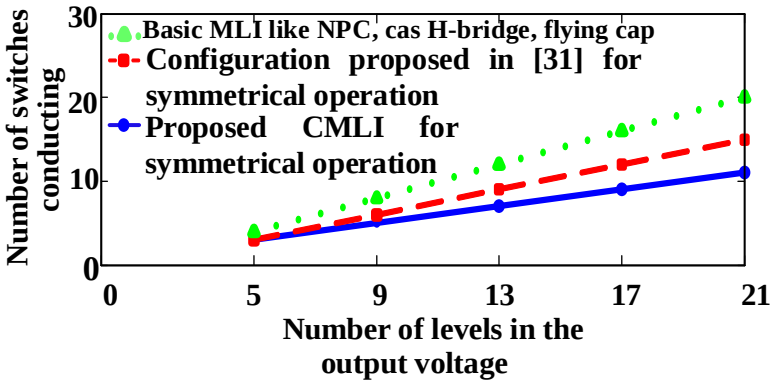


Fig. 3.7 Comparison of number of switches conducting in the proposed topology with other MLIs.

The switches Sw_{2m+1}, Sw_{2m+2} are operated at the low switching frequency, i.e. at the frequency of the reference wave. So the configuration has less switching losses when compared to configuration proposed by E.Babaei *et.al.* [31]. Fig. 3.8 shows the number of levels in the output versus the number of switches used for the proposed inverter and cascaded H-bridge in asymmetrical operation. Hence the proposed CMLI is economical as the number of components used are less and it is efficient because of reduced switching and conduction losses as observed from Figs. 3.6, 3.7 and 3.8 respectively.

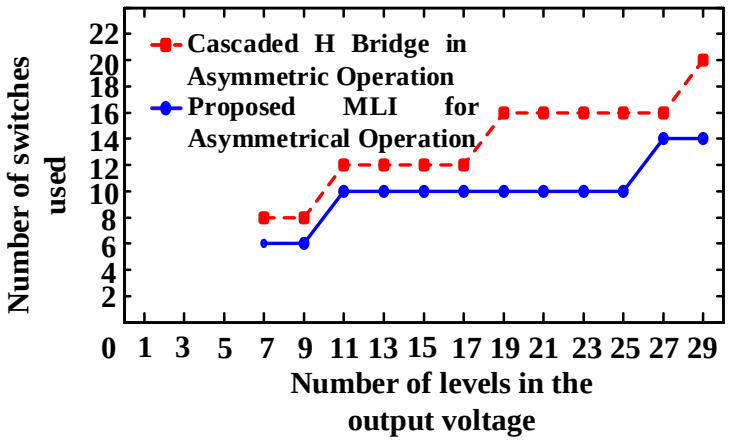


Fig. 3.8 Comparison of the number of switches used in proposed topology with cascaded H-bridge in asymmetrical operation.

3.4. Simulation and experimental results

To verify the operation of proposed CMLI, the simulation and experimental results were taken at different values of modulation indices 'm_a'. The simulation was performed using the MATLAB/SIMULINK software. The parameters considered in the simulation and experiment setups are given in Table 3.3. The MOSFETS IRF 640 were used in the hardware prototype developed. The driver IC HCPL 3120 were used for driving these MOSFETS. The pulses for these switches are generated using the SPARTAN 6 FPGA board. The DPO 3034 is used to capture the experimental waveforms from the hardware prototype developed. The programmable DC sources were used to produce DC input voltage in the power circuit of the proposed CMLI. The photograph of the experimental setup built is given in Fig. 3.9.

TABLE 3.3. SIMULATION AND EXPERIMENTAL PARAMETERS

Parameter	V_{DC}	f_{sw}	f_g	R_{load}
Value	100V	10kHz	50Hz	185Ω

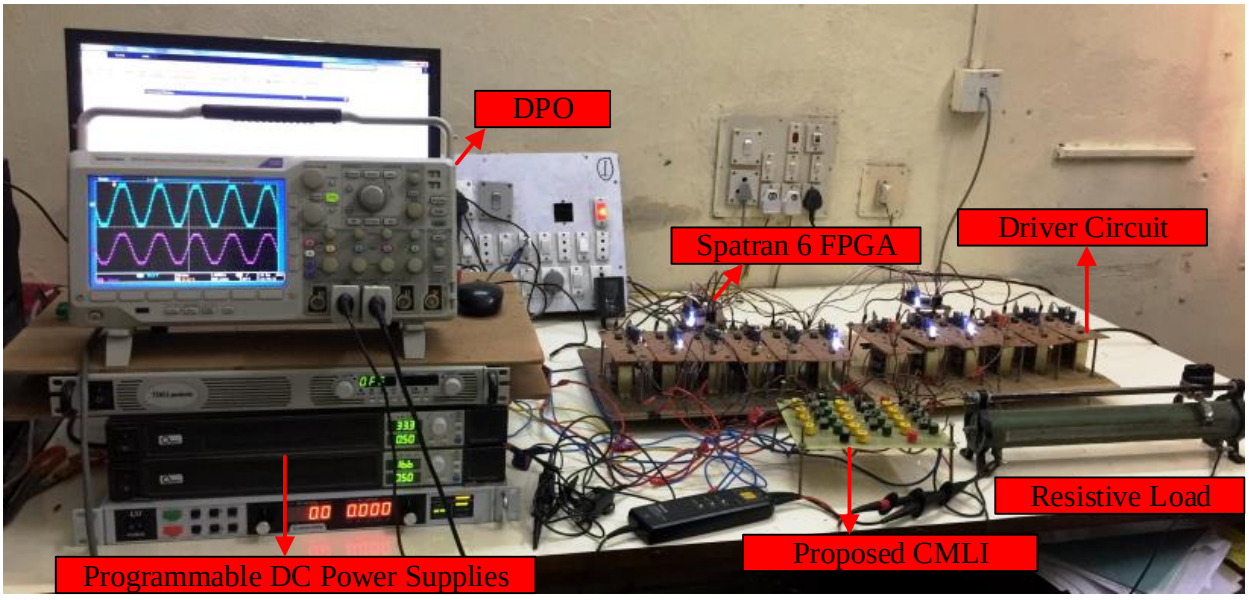


Fig. 3.9. Experimental prototype of proposed CMLI.

The waveforms shown in Fig. 3.10 are the output voltages of the proposed inverter for different modulation indices in symmetrical operation. For this configuration in symmetrical operation as the value of 'm_a' increases from zero to one the number of levels in the output voltage increases from three to nine. Further, the proposed configuration is simulated and

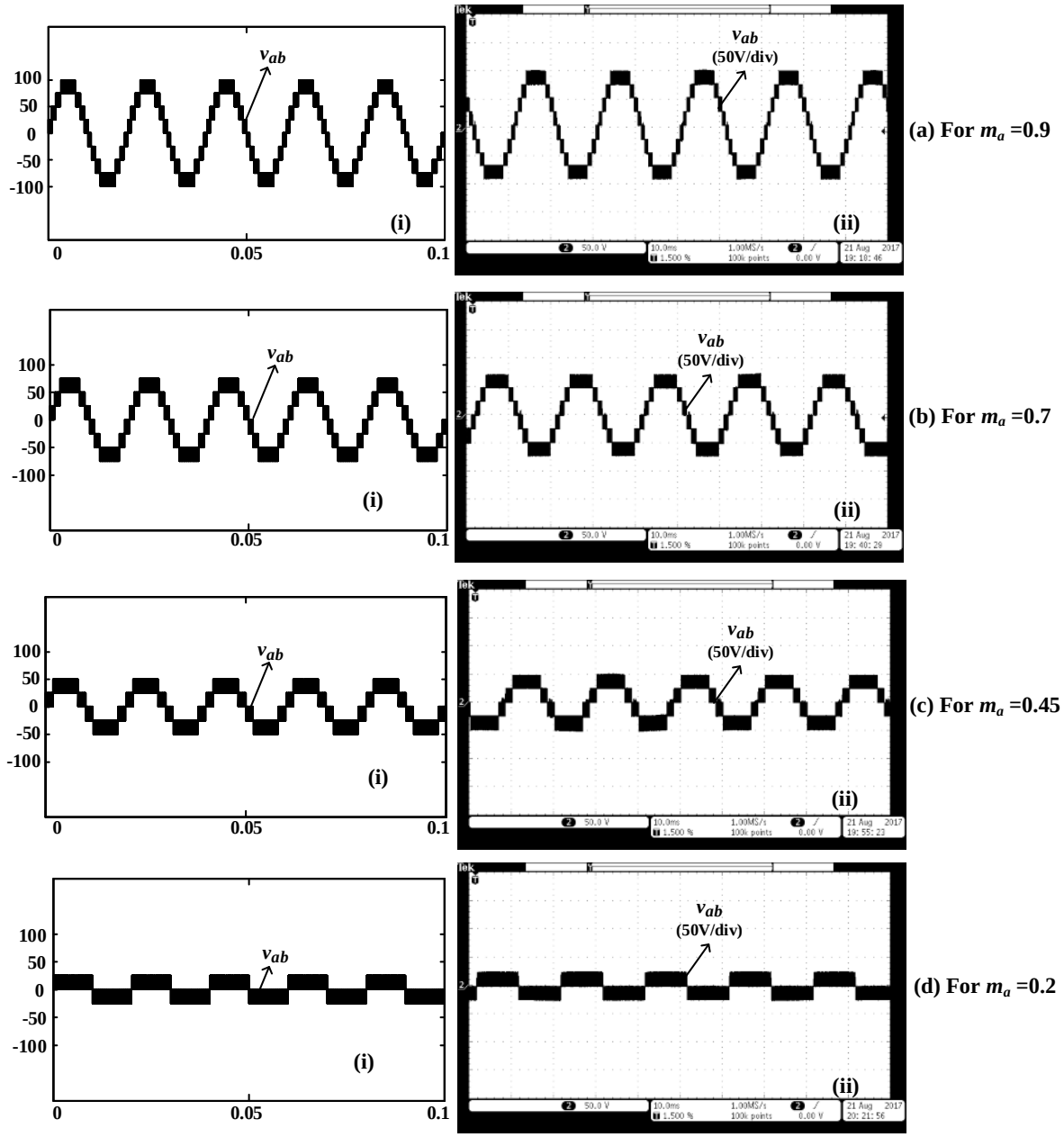


Fig. 3.10 (i) Simulation and (ii) experimental waveforms of output voltage 'v_{ab}' for different modulation indices 'm_a' (a) 'm_a' = 0.9; (b) 'm_a' = 0.7; (c) 'm_a' = 0.45; (d) 'm_a' = 0.2 in symmetrical configuration.

verified using the experimental setup for its operation in asymmetrical operation. Fig. 3.11 shows the inverter output voltage waveforms for different modulation indices. It can be observed that, with the increase of 'm_a', the number of levels in the output voltage increases from three to thirteen in the asymmetrical operation of the proposed inverter. Further, the proposed CMLI is tested for leakage current to extend its application in the PV system.

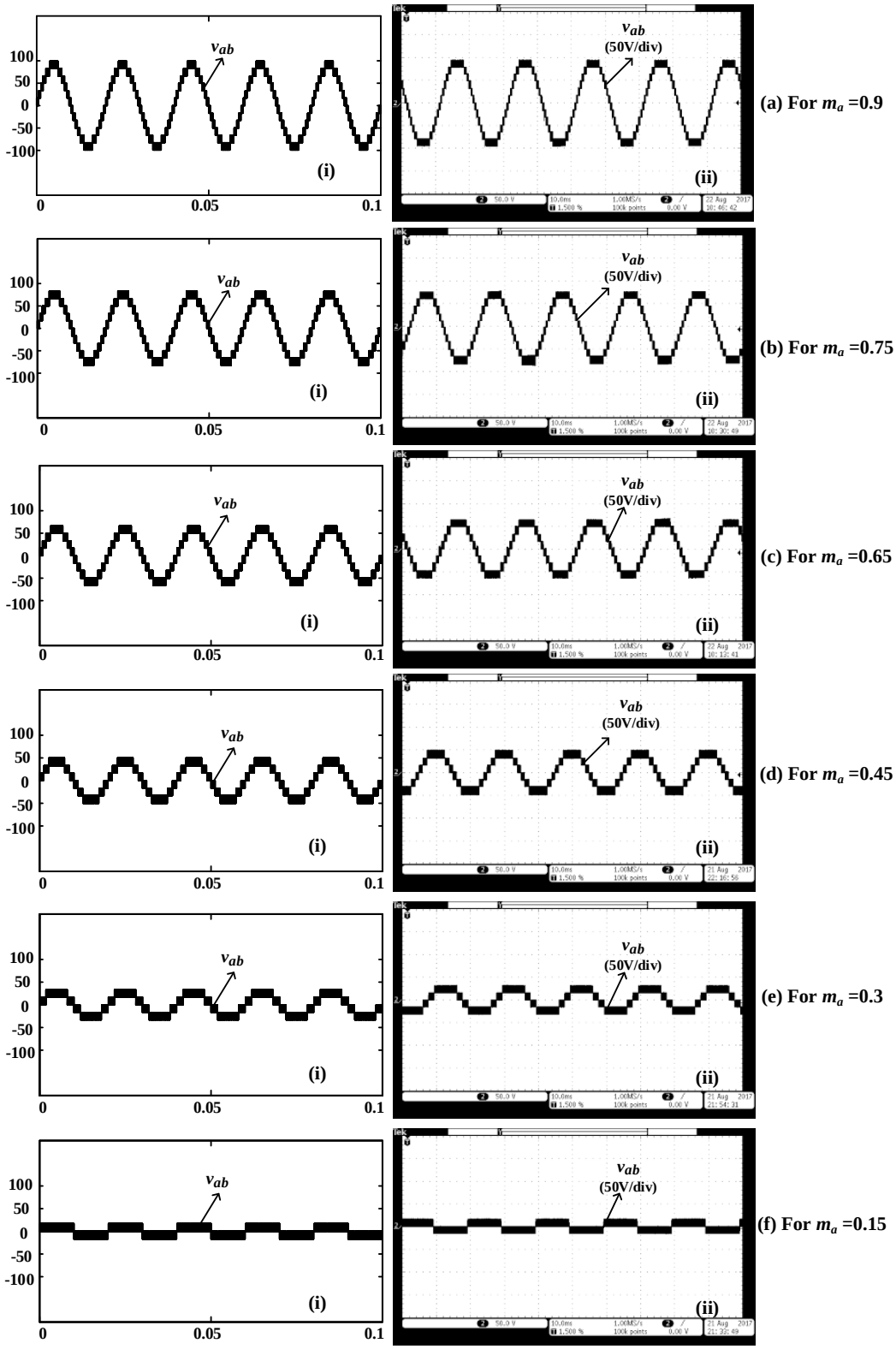


Fig. 3.11 (i) Simulation and (ii) experimental waveforms of output voltage *'v_{ab}'* for different modulation indices 'm_a' (a) 'm_a' = 0.9; (b) 'm_a' = 075; (c) 'm_a' = 0.65; (d) 'm_a' = 0.45; (e) 'm_a' = 0.3; (f) 'm_a' = 0.15 in asymmetrical configuration.

Therefore, the proposed CMLI is tested for the magnitude of leakage current flowing through its parasitic capacitance. To emulate the presence of parasitic capacitance in the simulation and experimental setup, a series branch of resistance 'R_p' = 10Ω and capacitance 'C_p'= 10nF connected between the nodal point 'p' and ground of the proposed CMLI. Fig. 3.12 shows the (i) simulation and (ii) experimental waveforms of (a) terminal voltage 'v_{pg}' and (b) leakage current 'i_{leak}' for the proposed CMLI. It can be observed from Fig. 3.12 that the terminal voltage 'v_{pg}' has high switching voltage transitions. This may result in leakage current flow through the parasitic capacitance 'C_p' as can be seen in simulation and experimental results. Thus, the given configuration needs to be modified or require high value of EMI filters at the PV input to supress the leakage current magnitude.

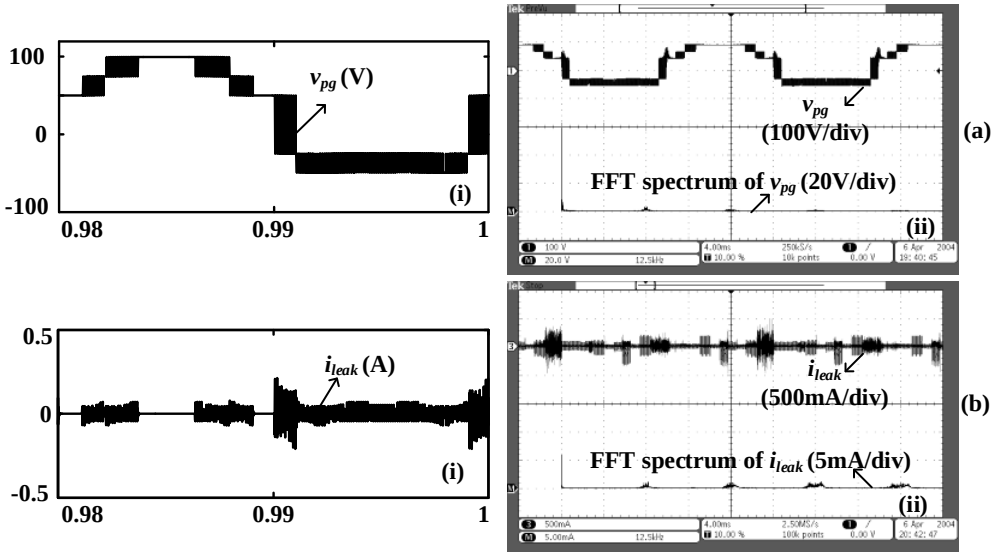


Fig. 3.12 (i) Simulation and (ii) experimental waveforms of (a) terminal voltage *'v_{pg}'*; (b) leakage current *'i_{leak}'*.

3.5. Conclusion

This chapter proposed a new low cost and efficient CMLI topology with a reduced number of switches, reduced switching, and conduction loss. This proposed CMLI requires less number of switching devices and isolated power supplies compared to the basic MLIs. The proposed CMLI operates in both symmetrical and asymmetrical modes. The operation of proposed CMLI is further justified from the simulation and experimental results. The simulation and experimental results presented are exactly matching. Further, the extension of proposed configuration for '*2m+1*' levels is also given.

CHAPTER 4

Analysis of Modulation Strategy for the Minimization of Leakage Current in the PV Grid Connected Cascaded Multi-Level Inverter

Chapter 4

Analysis of Modulation Strategy for the Minimization of Leakage Current in the PV Grid Connected Cascaded Multi-Level Inverter

In the previous chapter, the proposed low cost and efficient CMLI suffer with the problem of high leakage current which may restrict its application to the PV system. However, the magnitude of leakage current can be minimized by using a proper the PWM technique. Hence, a new PWM technique needs to be developed to minimize the magnitude of leakage current flowing in the CMLI based PV systems. This chapter presents a pulse width modulation (PWM) technique for the minimization of the leakage current in the grid-connected/stand-alone transformerless PV CMLI. The proposed PWM technique is integrated with the MPPT algorithm and is applied to the five-level CMLI. Furthermore, using the proposed PWM technique the high-frequency voltage transitions in the terminal and common mode voltages are minimized. Thus, the proposed PWM technique minimizes the leakage current of the PV array and electromagnetic interference filter requirement in the system without the addition of any extra switches. Furthermore, this chapter also presents the analysis for the terminal voltage across the PV array and the common mode voltage of the inverter based on the switching function. Using the given analysis, the effect of the PWM technique can be analyzed, as it directly links the switching function with the common mode voltage and leakage current. Also, the proposed PWM technique requires reduced number of carrier waves compared to the conventional sinusoidal pulse width modulation technique for the given CMLI. Complete details of the working principle and analysis with the support of simulation and experimental results of the proposed PWM technique are presented in the below sections.

4.1. Operation of cascaded multi-level inverter

The detail regarding the operation of CMLI is formulated by considering a five-level inverter topology [31]. The given configuration broadly consists of two converters (‘Conv 1’ and ‘Conv 2’) as shown in Fig. 4.1. The ‘Conv 1’ is a basic unit for the CMLI. It consists of a

switch Sw_1 and a bi-directional switch (Sw_2 and Sw_3). The purpose of switch Sw_3 is to eliminate the forward biasing condition due to the inherent diode in the switch Sw_2 during its operation [31]. The switches Sw_2 and Sw_3 of the first converter are operated simultaneously. The 'Conv 1' output voltage 'v_{zn}' attains voltage level 'V_{PV}' when switch Sw_1 is turned ON. Similarly, it attains the voltage level '$V_{PV}/2$' when switches Sw_2 and Sw_3 are turned ON respectively. The voltage levels of 'V_{PV}' and '$V_{PV}/2$' are generated using two PV sources 'PV_1' and 'PV_2' as shown in Fig. 4.1. The generated voltage 'v_{zn}' of 'Conv 1' instantaneously becomes the input to the 'Conv 2'. The 'Conv 2' comprises of H- bridge inverter formed by four switches Sw_4, Sw_5, Sw_6 and Sw_7. The 'Conv 2' generates positive, negative and zero voltage levels of 'v_{zn}' respectively. The pair of switches ((Sw_4, Sw_5) and (Sw_6, Sw_7)) in each leg are operated in complement manner. Thus, there are three pairs of complementary switches (Sw_1, Sw_2 (Sw_3)), (Sw_4, Sw_5) and (Sw_6, Sw_7) in the given five-level CMLI. Using the proposed PWM technique, the complementary action in one pair of switches (Sw_1, Sw_2 (Sw_3)) is not considered. Forefend of complementary action during zero state helps in minimizing the flow of leakage current through parasitic capacitance of the PV array. Also, the zero state is incorporated in all the voltage transitions in the output voltage 'v_{ab}'. The corresponding action is done to avoid the flow of the leakage current during the transitions

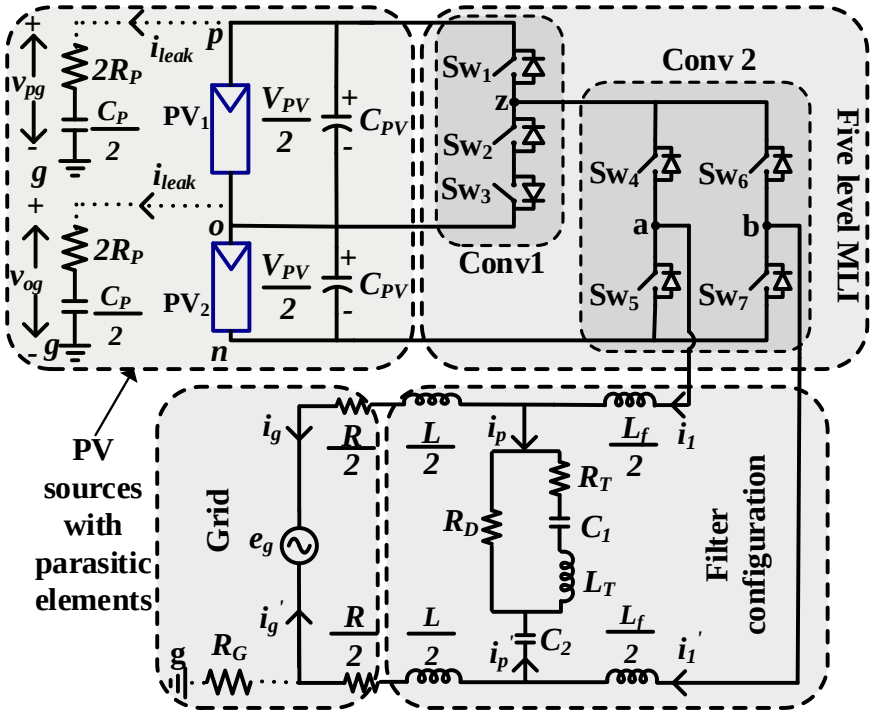


Fig. 4.1. Circuit schematic for single phase grid connected five-level CMLI with parasitic elements.

between voltage levels of 'V_{PV}' and '$V_{PV}/2$'. The complete details regarding the PWM technique is broadly discussed in the next section.

The switching states with their respective voltage levels for the five-level CMLI using proposed PWM are shown in Table 4.1. The given switching states can be used for determination of pole voltage at various voltage levels. The pole voltages 'v_{an}'& 'v_{bn}' can be expressed as,

$$v_{an}=\left(S_1+0.5S_2-\frac{1}{S_4}+\frac{1}{S_4\left(S_1+S_2\right)}\right)S_4V_{PV} \tag{4.1}$$

$$v_{bn}=\left(S_1+0.5S_2-\frac{1}{S_6}+\frac{1}{S_6\left(S_1+S_2\right)}\right)S_6V_{PV} \tag{4.2}$$

where S_x, represents switching function for switch 'x' with $x \in (1, 2, 3...7)$. The value of S_x is, '1' or '0' when the corresponding switch 'x' is turned ON or OFF respectively. Further, it can be noticed that, the nodal point 'z' (Fig. 4.1) in 'Conv 1' is floating or undefined with respect to ground nodal point 'n' during zero voltage state or turn-off period of switching cycle. Hence, the pole voltages 'v_{an}' and 'v_{bn}' are undefined (i.e., 0/0) during zero state. Fig. 4.2 shows the operation of five-level CMLI during zero state. During zero state the active switches or functioning unit are represented by dark lines. The output phase voltage 'v_{ab}' can be obtained

TABLE 4.1. SWITCHING STATES OF SWITCHES FOR THEIR CORRESPONDING OUTPUT VOLTAGE LEVEL

Output voltage level (v_{ab})	**+ V_{PV}**	**+ $V_{PV}/2$**	**0**	**-$V_{PV}/2$**	**- V_{PV}**
Sw_1	ON	OFF	OFF	OFF	ON
Sw_2	OFF	ON	OFF	ON	OFF
Sw_4	ON	ON	ON	OFF	OFF
Sw_6	OFF	OFF	ON	ON	ON

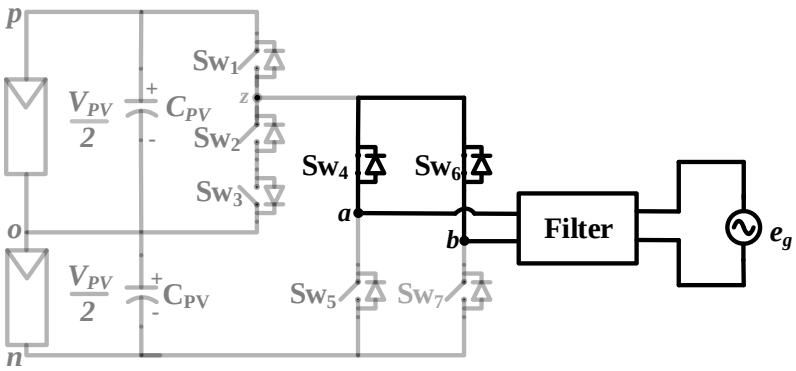


Fig. 4.2. Operation of five-level CMLI during zero state. Active or functioning circuit are shown with dark lines.

by subtracting the pole voltages 'v_{an}' and 'v_{bn}'. Therefore, the expression for output phase voltage 'v_{ab}' can be written as,

$$v_{ab} = v_{an} - v_{bn} \tag{4.3}$$

The inverter output voltage 'v_{ab}' is connected to the grid via filter inductors ('L_f' and 'L') and resistors ('R_G' and 'R') as indicated in Fig. 4.1 [20-21, 34]. The resistance 'R' and 'R_G' [21] refer to grid and ground resistance used in the system respectively. The filter configuration [35] used in the system have two separate paths. The first path formed by the components inductor 'L_T', capacitor 'C_1' and resistor 'R_T' are used for filtering the high-frequency current ripple at the inverter output. The second parallel path formed by capacitor 'C_2' and damping resistor 'R_d' is used to damp out the load and supply induced resonance. The term 'e_g' refers to instantaneous grid voltage and the terms 'R_p' and 'C_p' refers to parasitic resistance and capacitance of the PV array respectively. The parasitic elements in the PV system [20, 34] are represented using the dotted lines as shown in Fig. 4.1. Also, the parasitic capacitance in the PV array forms a resonant circuit with the filter inductors at the inverter output. The resonant frequency 'f_r' formed by resonant circuit is given by the expression [21],

$$f_r = \frac{1}{2\Pi\sqrt{\frac{1}{4}\left(L_f + L\right)C_p}} \tag{4.4}$$

At resonant frequency the parasitic capacitance offers minimum impedance. Hence, the magnitude of leakage current 'i_{leak}' flowing through parasitic capacitance is high for the harmonics in the terminal voltage with same frequency as resonance frequency 'f_r'. The

proposed PWM technique minimizes the resonant frequency component in the terminal voltage. Thus, it reduces the leakage current flowing at frequency 'f_r'. It also minimizes the voltage transitions in common mode voltage.

4.2. Proposed PWM strategy and its generalization for minimization of the leakage current

As discussed above, the given system requires two independent PV sources for five-level output. The two PV sources required, can have symmetrical or asymmetrical configuration. Thus, the proposed PWM strategy needs to operate in both symmetrical and asymmetrical configurations for the two PV sources as discussed below.

4.2.1. PWM strategy for symmetrical configuration of PV sources

The proposed PWM technique minimizes the leakage current by eliminating the high-frequency voltage transitions (ripple content) in the PV terminal voltage. The following action can be achieved by isolating the PV array and grid during zero state. This is similar to H5 inverter topology [22]. Further, the flow of leakage current in switching between the intermediate states '$V_{PV}/2$' to 'V_{PV}' or vice versa can be achieved by switching between '*0*' to 'V_{PV}' state or vice versa. In other words, the zero voltage level is maintained for all the voltage transitions in the complete cycle of output voltage 'v_{ab}'. During the zero state, terminal voltage and common mode voltage achieve undefined state. The incorporation of zero state results in avoiding the high-frequency transitions in the terminal and common mode voltages. In order to accommodate 'V_{PV}' bus voltage for switching between 'V_{PV}' to '*0*', the magnitude of reference wave 'v_{mod}' is reduced to half of its original value. The change in magnitude of reference wave is done only when switching is in between 'V_{PV}' to '*0*' or vice versa. The expression for modified reference wave is given below,

$$v_{ref\_modified} = \begin{Bmatrix} v_{mod} & for & 0 \le |v_{mod}| < \dfrac{m_a}{2} & at & \dfrac{V_{PV}}{2} \\ \dfrac{v_{mod}}{2} & for & \dfrac{m_a}{2} \le |v_{mod}| < m_a & at & V_{PV} \end{Bmatrix} \tag{4.5}$$

$v_{mod} = m_a \sin\omega t$, where '$m_a$' is amplitude of reference wave

The switching strategy of the proposed PWM technique for five-level CMLI is shown in Fig. 4.3. The absolute magnitude of modified reference wave '$v_{ref\_modified}$' is compared with

the triangle carrier wave. The amplitude of triangular carrier wave 'x_2' is ratio of bottom PV source 'PV_2' voltage '$V_{PV}/2$' to the overall PV voltage 'V_{PV}'. So, the instantaneous magnitude of triangular carrier wave varies from '0.5' to '0' in case of symmetrical PV array configuration. Therefore, the required triangular wave can be generated by multiplying ratio 'x_2' with the unit triangular carrier waveform (triangular waveform with unit amplitude). Now, within positive half cycle of 'v_{ab}', for the ranges of phase 'ωt' varying from 0^0 to 30^0 or 150^0 to 180^0, if the instantaneous magnitude of '$v_{ref\_modified}$' exceeds the magnitude of carrier wave then the output voltage attains the level '$V_{PV}/2$'. For the remaining range of 'ωt' (i.e. from 30^0 to 150^0), the output voltage attains level 'V_{PV}' whenever the instantaneous magnitude of '$v_{ref\_modified}$' exceeds the magnitude of carrier wave. Similar sequence is applicable for negative half cycle which helps in maintaining symmetry between positive and negative cycle of the fundamental output voltage. This can be further observed in Fig. 4.3 which shows the output voltage of the CMLI.

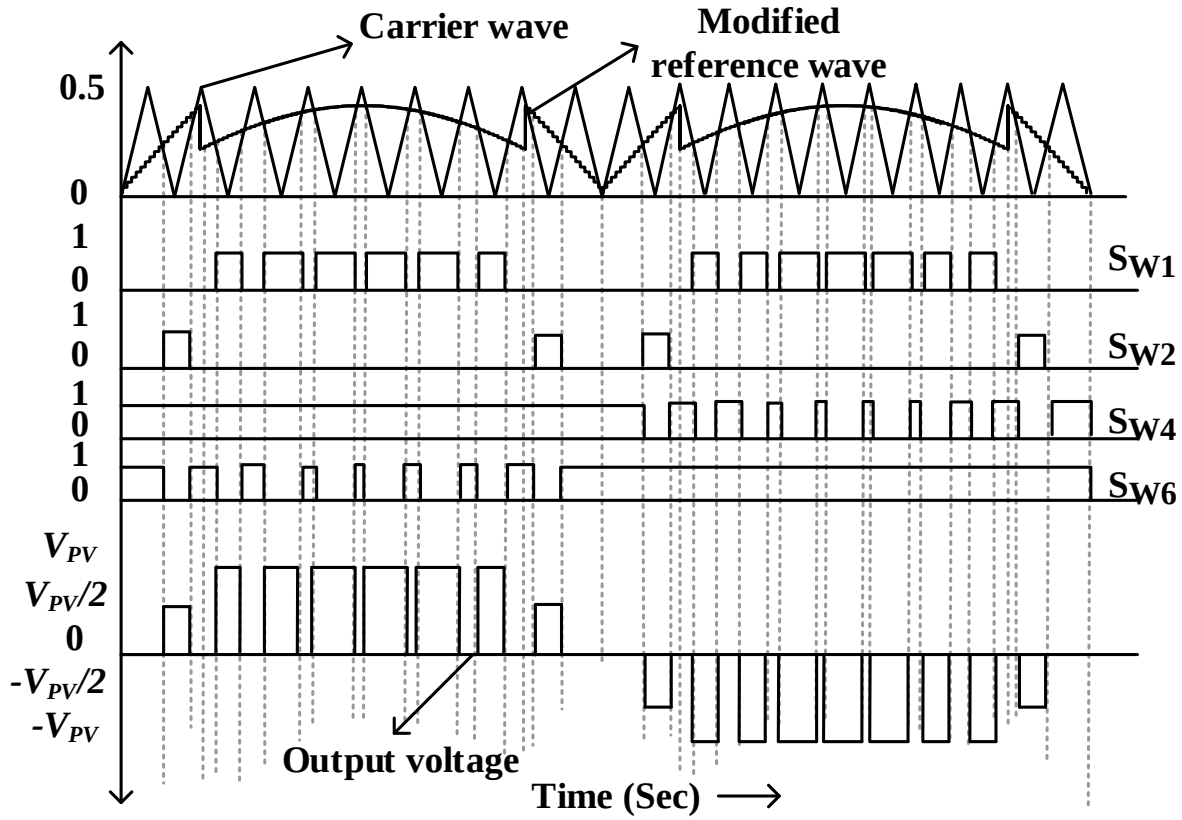


Fig. 4.3. Modified reference wave and the switching strategy of the proposed PWM technique.

The block diagram for the generation of modified reference wave is shown in Fig. 4.4. The instantaneous absolute value of reference wave 'v_{mod}' is compared with the amplitude

'$m_a/2$'. If the instantaneous value of reference wave is lower than '$m_a/2$', then there is no change in the amplitude of modified reference wave '$v_{ref\_modified}$'. However, when the instantaneous value of reference wave 'v_{mod}' exceeds '$m_a/2$', then the amplitude of modified reference wave '$v_{ref\_modified}$' is equal to half of the magnitude of reference wave 'v_{mod}' as given in (4.5). The value '0.5' is obtained from the ratio of bottom PV source 'PV_2' voltage '$V_{PV}/2$' to the overall PV voltage 'V_{PV}' as shown in Fig. 4.4.

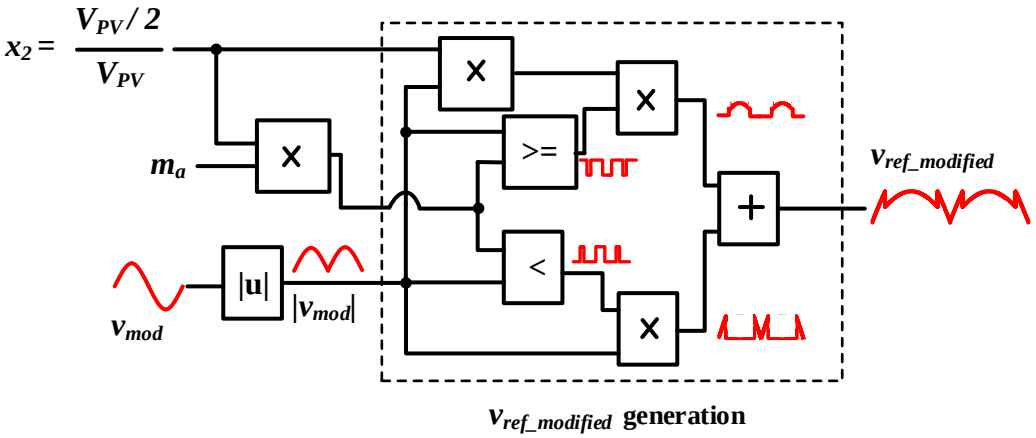


Fig. 4.4 Block diagram for generation of modified reference wave '$v_{ref\_modified}$' from reference wave 'v_{mod}', 'x_2' and 'm_a' for five-level CMLI.

The five-level CMLI can be generalized for '$2m+1$' levels. The term 'm' refers to number of PV sources and its value is always an even number (i.e. 'm'=2, 4…). Fig. 4.5 shows the generalized topology of CMLI for '$2m+1$' levels in the output voltage. In order to generate more than five levels in the output voltage, the basic unit consisting of 'Conv 1' and 'Conv 2' needs to be cascaded as shown in Fig. 4.5. During zero state, all the switches in the basic unit of 'Conv 1' are turned OFF so that the grid is isolated from the PV array. Further, the intermediate states used in CMLI are replaced by zero state with the required modifications in PWM technique. This helps in minimizing the flow of leakage current during other intermediate states. Further, the magnitude of 'v_{mod}' should be modified to accommodate or nullify the change in voltage level. This modification of 'v_{mod}' depends on the magnitude of levels in the output voltage of CMLI. Fig. 4.6 gives the waveform of modified reference wave for '$2m+1$' level inverter which is also expressed in (4.6). The amplitude of modified reference wave remains unchanged until the instantaneous value of reference wave 'v_{mod}' is less than 'm_a/m'.

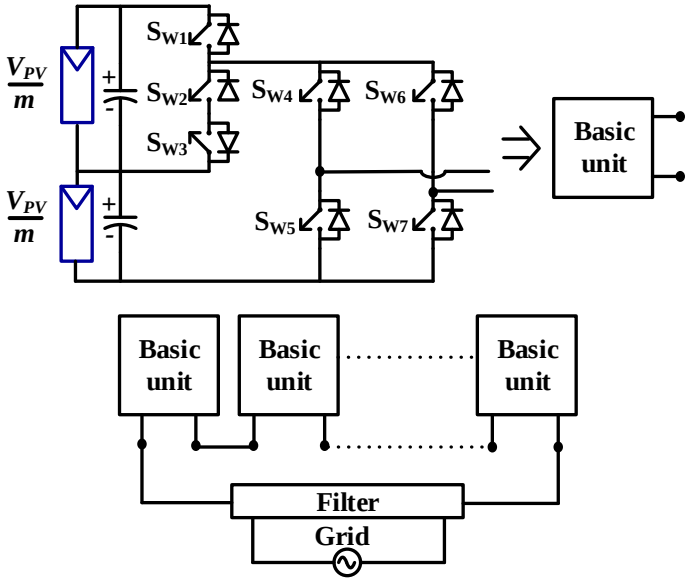


Fig. 4.5. Generalized topology of CMLI for '*2m+1*' levels in the output voltage.

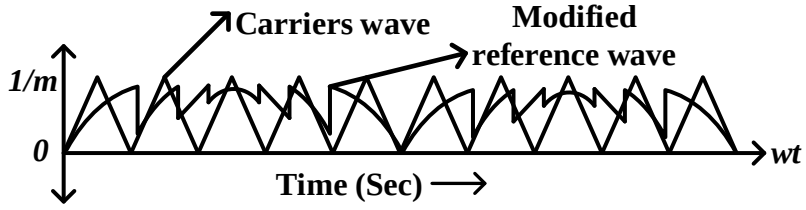


Fig. 4.6. Modified reference and carrier waves for '*2m+1*' level CMLI.

$$v_{ref\_modified} = \begin{Bmatrix} v_{mod} & for\ 0 \le |v_{mod}| < \frac{m_a}{m} & at\ \frac{V_{PV}}{m} \\ \frac{v_{mod}}{2} & for\ \frac{m_a}{m} \le |v_{mod}| < \frac{2m_a}{m} & at\ \frac{2V_{PV}}{m} \\ & . & \\ & . & \\ \frac{v_{mod}}{m} & for\ \frac{(m-1)m_a}{m} \le |v_{mod}| < m_a & at\ V_{PV} \end{Bmatrix} \quad (4.6)$$

4.2.2. PWM strategy for asymmetrical configuration of PV sources

When there is an asymmetry in the PV configuration, the output voltages of PV sources 'PV_1' and 'PV_2' are different. Let 'V_{PV1}' and 'V_{PV2}' are the output voltages of the PV sources 'PV_1' and 'PV_2' respectively as indicated in Fig. 4.7. The total PV voltage 'V_{PV}' is given by,

$$V_{PV} = V_{PV1} + V_{PV2} \tag{4.7}$$

Whenever the voltages 'V_{PV1}' and 'V_{PV2}' of source 'PV_1' and 'PV_2' are different, then the same proposed PWM technique can be used except for the value of 'x_2'. The value of modified reference wave '$v_{ref\_modified}$' depends on the ratio 'V_{PV2}/ V_{PV}'. The terms 'x_1'and 'x_2' can be represented in terms of 'V_{PV1}', 'V_{PV2}' and 'V_{PV}' as

$$x_1 = \frac{V_{PV1}}{V_{PV}} \tag{4.8}$$

$$x_2 = \frac{V_{PV2}}{V_{PV}} \tag{4.9}$$

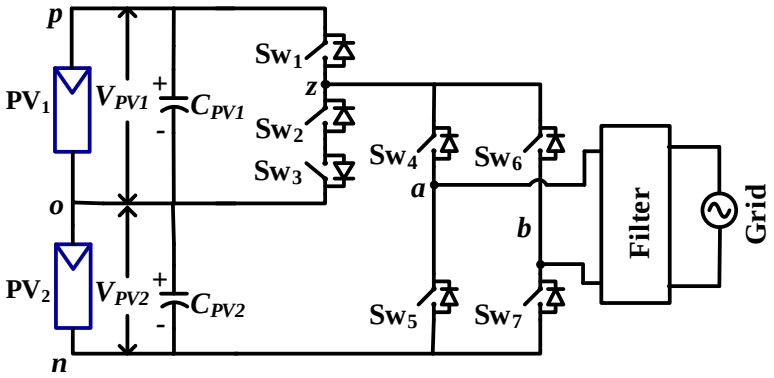


Fig. 4.7. Circuit schematic for single phase grid connected five-level CMLI for asymmetrical configuration.

The modulation index 'm_a' is multiplied with a sine wave having unity magnitude to obtain 'v_{mod}'. The instantaneous magnitude of 'v_{mod}' is compared with '$x_2 m_a$'. Whenever the instantaneous value of reference wave 'v_{mod}' exceeds '$x_2 m_a$', then the magnitude of modified reference wave '$v_{ref\_modified}$' becomes '$v_{mod} x_2$'. Once PWM strategy is defined for the given system, MPPT algorithm needs to be integrated with the proposed PWM strategy. Below section explains the MPPT operation for the system.

4.3. Integration of MPPT with the proposed PWM technique and the design of PV source capacitors

In order to operate the two PV sources at maximum power [36], perturb and observe (PO) algorithm [37] was employed in the given system. The PO algorithm requires average values of sensed PV voltages and PV currents. The sensed averaged values of voltage 'V_{PV1}' and current 'I_{PV1}' of source 'PV_1' are given to MPPT algorithm 'MPPT1' as shown in Fig.

4.8. Similarly, voltage 'V_{PV2}' and current 'I_{PV2}' of 'PV_2' are given to another MPPT algorithm 'MPPT2'. Thus, the sensed average values of PV voltage and current are given to respective MPPT algorithms. The individual MPPT algorithms 'MPPT1' and 'MPPT2' gives modulation index 'm_{a1}' and 'm_{a2}' respectively as shown in Fig. 4.8. In other words, the two PV sources are operated with their individual MPPT algorithms. The resultant modulation index 'm_a' is obtained by,

$$m_a = m_{a1}x_1 + m_{a2}x_2 \tag{4.10}$$

The resultant modulation index 'm_a' is now multiplied by an unit amplitude sine wave to obtain 'v_{mod}'. The reference wave 'v_{mod}' is then used for generating modified reference wave '$v_{ref\_modified}$' as indicated in Fig. 4.8. The obtained '$v_{ref\_modified}$' is compared with a

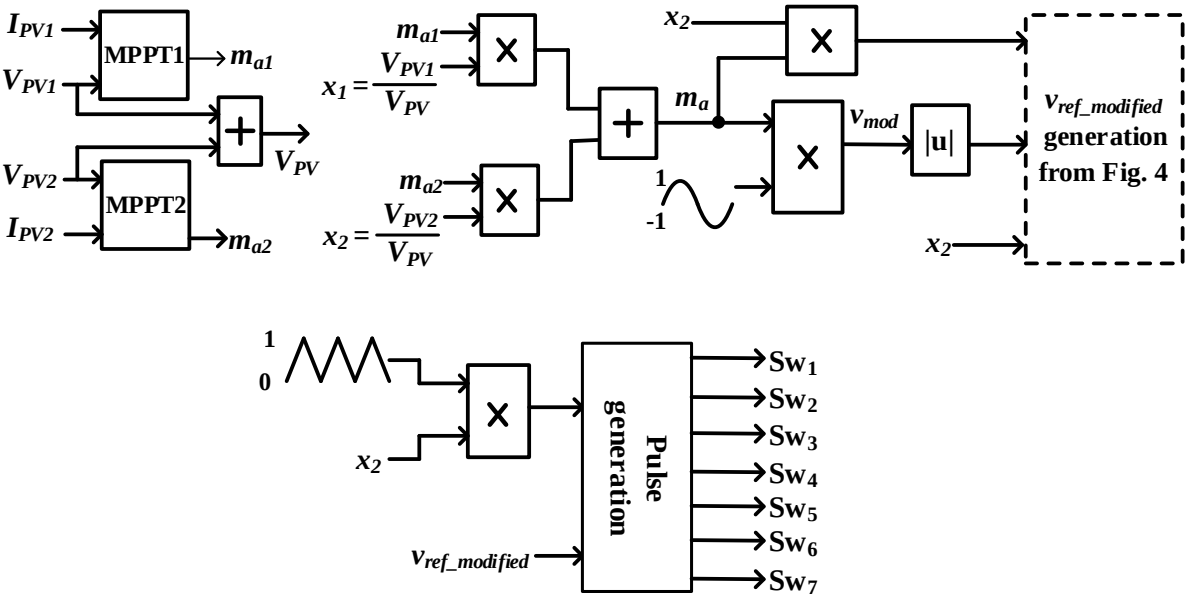


Fig. 4.8. MPPT and pulse generation for the single phase five-level CMLI.

triangular carrier wave having magnitude ranging from '0' to 'x_2' and the corresponding pulses for the switches are generated accordingly. In single phase system, it can be noted that the buffer capacitor used across PV sources plays an important role in the efficient operation of MPPT. Thus, proper design value of buffer capacitors ('C_{pv1}' and 'C_{pv2}') should be used in the given MLI.

4.3.1. Design calculation for PV source buffer capacitors 'C_{pv1}' and 'C_{pv2}'

The design of capacitor 'C_{PV1}' can be done by considering the non-active period of the source 'PV_1'. In other words, value of 'C_{PV1}' should be such that it maintains the PV source 'PV_1' near the maximum power point (MPP) voltage during the non-active period of PV source 'PV_1'. Thus, source 'PV_1' operating near MPP injects the current 'I_{PV1}' (near to MPP current) into the capacitor 'C_{PV1}'. The value of capacitor 'C_{PV1}' is given by [38],

$$C_{PV1} = \frac{I_{PV1} t_1}{\Delta V_{PV1}} \tag{4.11}$$

where 't_1' represents the non-active time period or duration in which the source 'PV_1' is not delivering any power to the output load, 'ΔV_{PV1}' is the allowed ripple content in the source 'PV_1' voltage 'V_{PV1}'. Let us consider five PV modules (where each module has 'V_{oc}' = 21.05V and 'I_{sc}' = 3.84A at STC) are connected in series to obtain desired 'V_{PV1}' and 'I_{PV1}'. For the fundamental value of grid frequency 50Hz, the PV source will not deliver any power for a period of '60^0' or '3.33ms' during symmetrical configuration. Also, considering the ripple in 'V_{PV1}' as 2% (i.e. V_{oc}*0.02= 2.105V) and 'I_{PV1}'=3.74A, the calculated value of 'C_{PV1}' is given by

$$C_{PV1} = 5.86\, mF \tag{4.12}$$

Similar, procedure can be used for the calculation of 'C_{PV1}' during asymmetrical PV source configurations. Now, as the source 'PV_2' is active in complete cycle of output voltage, therefore the value of capacitor 'C_{PV2}' can be calculated as [3],

$$C_{PV2} = \frac{P_{PV}}{2\omega_g \langle V_{PV2} \rangle \Delta V_{PV2}} \tag{4.13}$$

where 'P_{PV}' is total power from both the PV sources, 'ω_g' is the fundamental value of grid frequency in rad/sec, '$<V_{PV2}>$' is average 'PV_2' source voltage and 'ΔV_{PV2}' is the ripple in the voltage 'V_{PV2}'. By substituting the values of 'P_{PV}'=788W, 'ω_g'=314 rad/sec, 'ΔV_{PV2}'= 2.105V and '$<V_{PV2}>$' = 105.25V, the calculated value of 'C_{PV2}' is given by,

$$C_{PV2} = 5.66\, mF \tag{4.14}$$

4.4. Analysis of PV terminal voltage and common mode voltage for five-level inverter

For analysis of leakage current, it is necessary to derive the expression for PV terminal voltage with respect to ground point 'g' (Fig. 4.1). The expression for terminal voltage across the parasitic capacitances are derived using switching functions. From Fig. 4.1 the terminal voltage 'v_{pg}' across the PV array can be expressed as,

$$v_{pg} = S_1 v_{p1g} + S_2 v_{p2g} \tag{4.15}$$

where 'v_{p1g}'and 'v_{p2g}' are the terminal voltages at terminal 'p' when switches Sw_1 and Sw_2 are turned ON respectively. Similarly, the terminal voltage 'v_{og}' across the PV array can be expressed as,

$$v_{og} = S_1 v_{o1g} + S_2 v_{o2g} \tag{4.16}$$

where 'v_{o1g}' and 'v_{o2g}' are the terminal voltages at terminal 'o' when switch Sw_1 and Sw_2 are turned ON respectively. When switch Sw_1 is turned ON, then the terminal voltage 'v_{p1g}' and 'v_{ng}' at terminal 'n' are related as,

$$v_{ng} = v_{p1g} - v_{pn} \tag{4.17}$$

where 'v_{pn}' is the voltage across the terminals 'p' and 'n' (Fig. 4.1). Substituting v_{pn}= 'V_{PV}' in (4.17) gives,

$$v_{ng} = v_{p1g} - V_{PV} \tag{4.18}$$

Further, the voltage 'v_{ag}' (Fig. 4.1) can be expressed in terms of 'v_{p1g}' and 'v_{ng}' as

$$v_{ag} = S_4 S_1 v_{p1g} + (1 - S_4) v_{ng} \tag{4.19}$$

Similarly, the voltage 'v_{bg}' can also be expressed in terms of 'v_{p1g}' and 'v_{ng}' as,

$$v_{bg} = S_6 S_1 v_{p1g} + (1 - S_6) v_{ng} \tag{4.20}$$

Now, the voltage 'v_{ag}' can also be expressed in terms of grid voltage 'e_g', drop in filter inductors ('L_f' and 'L') and resistances ('R' and 'R_G') [19] as,

$$v_{ag} = \frac{L_f}{2}\frac{di_1}{dt} + \frac{L}{2}\frac{di_g}{dt} + \frac{R}{2}i_g + \frac{R_G}{2}i_g + e_g \tag{4.21}$$

Similarly, the voltage 'v_{bg}' is expressed as,

$$v_{bg} = \frac{L_f}{2}\frac{di_1}{dt} + \frac{L}{2}\frac{di_g}{dt} + \frac{R}{2}i_g + \frac{R_G}{2}i_g \tag{4.22}$$

Now neglecting the drop in resistances 'R_G' and '$R/2$' and adding (4.21) and (4.22) with assumptions of i_g=-$i_g{}'$, i_p=-$i_p{}'$ and i_1=-$i_1{}'$ [19] gives,

$$v_{ag} + v_{bg} = e_g \tag{4.23}$$

Now, replacing 'v_{ag}' and 'v_{bg}' in (4.23) and then simplifying the expression for the terminal voltage 'v_{p1g}' gives,

$$v_{p1g} = \left[\frac{e_g + V_{PV}\left(2 - S_4 - S_6\right)}{S_4(S_1 - 1) + S_6(S_1 - 1) + 2}\right] \tag{4.24}$$

Once '$v_{p1g}{}'$ is known, then the other terminal voltage 'v_{o1g}' (when switch Sw_1 is ON) can be calculated as,

$$v_{o1g} = v_{p1g} - \frac{V_{PV}}{2} \tag{4.25}$$

Now to calculate terminal voltage 'v_{pg}', it still requires calculation of terminal voltage when switch Sw_2 is turned ON. When switch Sw_2 is turned ON, then the terminal voltages 'v_{p2g}' and 'v_{o2g}' are related as,

$$v_{p2g} = v_{o2g} + \frac{V_{PV}}{2} \tag{4.26}$$

Also, the terminal voltage 'v_{o2g}' and 'v_{ng}' are related as,

$$v_{ng} = v_{o2g} - v_{on} \tag{4.27}$$

Substituting 'v_{on}' by '$V_{PV}/2$'gives,

$$v_{ng} = v_{o2g} - \frac{V_{PV}}{2} \tag{4.28}$$

Again the voltage 'v_{ag}' can be expressed in terms of 'v_{o2g}' and 'v_{ng}' as,

$$v_{ag} = S_4 S_2 v_{o2g} + (1 - S_4) v_{ng} \tag{4.29}$$

Similarly, the voltage 'v_{bg}' can also be expressed in terms of 'v_{o2g}' and 'v_{ng}' as,

$$v_{bg} = S_6 S_2 v_{o2g} + (1 - S_6) v_{ng} \tag{4.30}$$

Substituting (4.29) and (4.30) in (4.23) and simplifying for terminal voltage 'v_{o2g}' results in,

$$v_{o2g} = \left[\frac{e_g + \frac{V_{PV}}{2}(2 - S_4 - S_6)}{S_4(S_2 - 1) + S_6(S_2 - 1) + 2} \right] \tag{4.31}$$

Once 'v_{o2g}' is known, 'v_{p2g}' can be calculated using (4.26). Using (4.15), the final expression for terminal voltage 'v_{pg}' for PV source 'PV_1' is given by,

$$v_{pg} = e_g S_{z1} + V_{PV} S_{z2} + e_g S_{z3} + \frac{V_{PV}}{2} S_{z4} + \frac{V_{PV}}{2} S_2 \tag{4.32}$$

Similarly, using (4.16) the final expression for terminal voltage 'v_{og}' for PV source 'PV_2' is given by,

$$v_{og} = e_g S_{z1} + V_{PV} S_{z2} - \frac{V_{PV}}{2} S_1 + e_g S_{z3} + \frac{V_{PV}}{2} S_{z4} \tag{4.33}$$

where the terms S_{z1}, S_{z2}, S_{z3} and S_{z4} in (4.32) and (4.33) are given by

$$S_{z1} = \frac{S_1}{S_4(S_1 - 1) + S_6(S_1 - 1) + 2}; \; S_{z2} = \frac{(2 - S_4 - S_6) S_1}{S_4(S_1 - 1) + S_6(S_1 - 1) + 2};$$

$$S_{z3} = \frac{S_2}{S_4(S_2 - 1) + S_6(S_2 - 1) + 2}; \; S_{z4} = \frac{(2 - S_4 - S_6) S_2}{S_4(S_2 - 1) + S_6(S_2 - 1) + 2}$$

To analyse the expressions (4.32) and (4.33) of terminal voltages containing switching functions, simulation was performed for both conventional and proposed PWM techniques. The simulation was done for given five-level CMLI using SIMULINK block set of MATLAB/SIMULINK software. Specifications used in the simulation are, 'V_{PV}'=250V, 'e_g'= 162.63V and 'f_g'= 50Hz. In order to show the undefined states clearly the switching frequency 'f_{sw}' is limited to 1kHz. Fig. 4.9 (I) and (II) shows the systematic approach for the generation of terminal voltage waveform from the expressions given in (4.32) and (4.33) for

conventional SPWM and proposed PWM techniques respectively. The subplots (a) to (d) in Fig. 4.9 (I) and (II) shows the switching states S_1, S_2, S_4 and S_6 of switches Sw_1, Sw_2, Sw_4 and Sw_6 respectively for conventional SPWM and proposed PWM techniques. The subplots (e) to (h) of Fig. 4.9 (I) and (II) gives the waveform of complicated switching expressions S_{z1}, S_{z2}, S_{z3} and S_{z4} in the terminal voltage. The effect of presence of high-frequency switching terms in the complex expression can be easily observed. The subplots (i) to (k) of Fig. 4.9 (II) clearly indicate that the presence of high-frequency transitions in terminal voltage waveforms is eliminated in proposed PWM technique. Further, the instance of floating or undefined voltage during zero state is present in both the PWM techniques. This results in discontinuity in the terminal voltage waveforms as observed in subplots (e) to (n) of Fig. 4.9. This verifies that the proposed PWM technique eliminates the high-frequency switching pulses in the terminal voltage for PV sources as shown in bottom subplots (i), (j), (k) of Fig. 4.9 (II). This further helps in reducing the leakage current [39] magnitude in PV systems. This can also be justified with the fact that the impedance offered by parasitic capacitor is inversely proportional to the frequency [20]. Further, the subplots (l) and (m) of Fig. 4.9 (I) and (II) shows the voltage 'v_{an}' and 'v_{bn}' of the inverter for conventional and proposed PWM techniques. Subplot (n) of Fig. 4.9 (I) and (II) shows the common mode voltage 'v_{cm}' of inverter for conventional and proposed PWM techniques. It can be easily observed from the plot that a number of high-frequency switching transitions are absent in the proposed PWM technique. Due to absence of high-frequency switching's, the size of EMI filter required at the output of inverter may be reduced [40]. This may further reduce the cost, size and weight of the system.

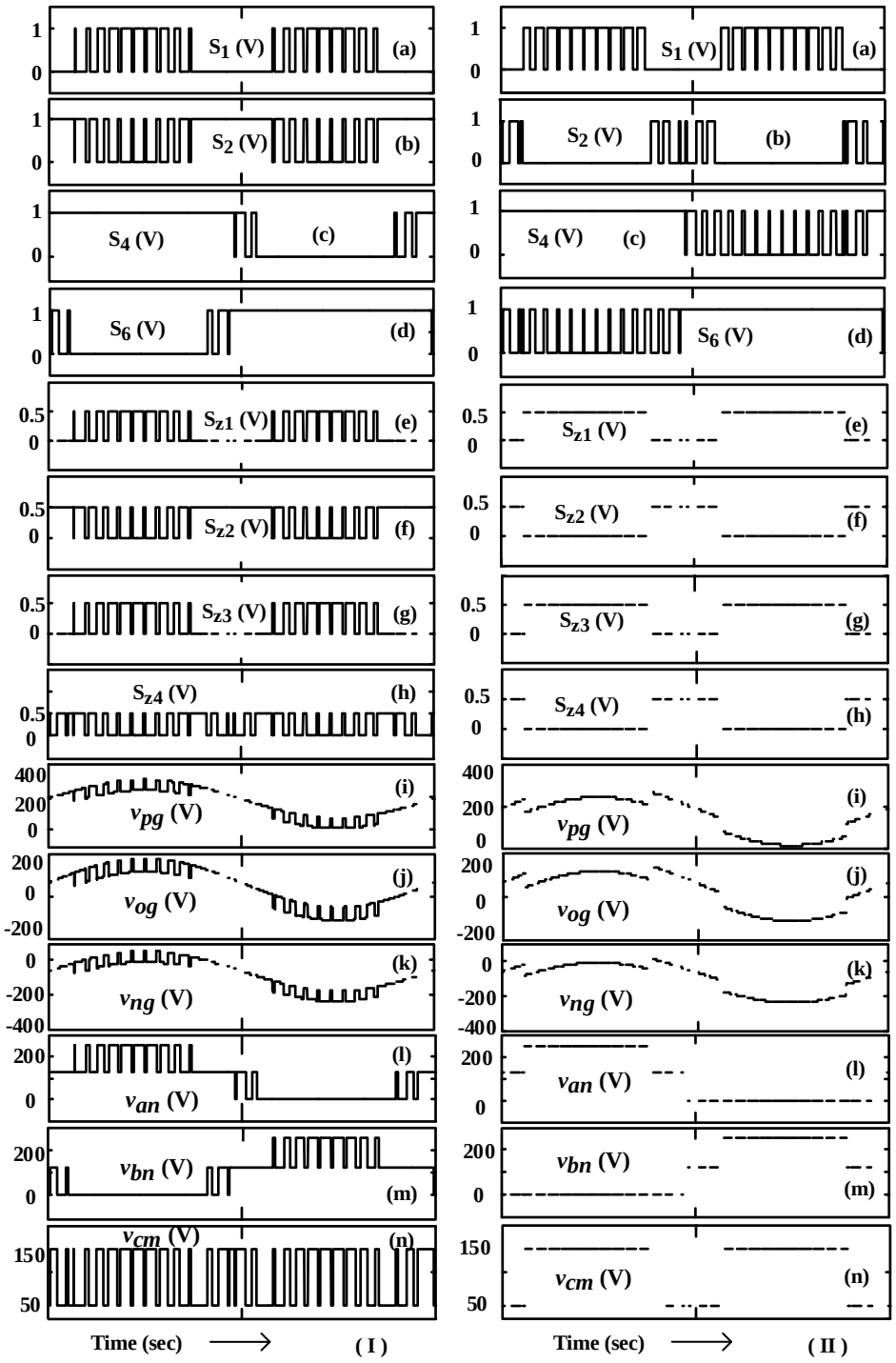


Fig. 4.9. Sequential steps for analysing the waveforms of terminal voltage 'v_{pg}', 'v_{og}' and common mode voltage 'v_{cm}' formed by using switching functions for the five-level CMLI with (I) conventional SPWM (II) proposed PWM techniques. The subplots give waveforms of : (a) switching state of switch Sw_1; (b) switching state of switch Sw_2; (c) switching state of switch Sw_4 ; (d) switching state of switch Sw_6; (e) expression S_{z1}; (f) expression S_{z2}; (g) expression S_{z3}; (h) expression S_{z4}; (i) terminal voltage 'v_{pg}'; (j) terminal voltage 'v_{og}'; (k) terminal voltage 'v_{ng}'; (l) voltage 'v_{an}'; (m) voltage 'v_{bn}'; (n) common mode voltage 'v_{cm}' (Discontinuity in the waveforms is due to existence of indefinite states in the expression).

4.5. Simulation results

Simulation of the proposed system was performed using the MATLAB/SIMULINK software. To justify the performance of the system for leakage current and MPPT operation, two separate simulations were performed as discussed in the following two subsections:

4.5.1. Simulation for leakage current

The simulation of the five-level CMLI shown in Fig. 4.1 was conducted in the MATLAB/SIMULINK software using its POWERSIM block-set to justify the analysis done with switching function. The conventional and proposed PWM techniques were applied to the five-level CMLI configuration with identical parameters. The parameters used in the simulation for proposed system are given in the Table 4.2. To deliver average active power 'P' into the grid, the inverter needs to generate a voltage 'V_r' with an angle 'δ_r'. The magnitude of angle 'δ_r' and voltage 'V_r' can be calculated as [21],

$$\delta_r = \arctan\left(\frac{2\Pi f_g \left(L_f + L\right)P}{e_g^2 + RP}\right) \tag{4.34}$$

$$V_r = \left(e_g + \frac{RP}{e_g}\right)\frac{1}{\cos\delta_r} \tag{4.35}$$

TABLE 4.2. PARAMETERS USED IN THE SIMULATION OF FIVE-LEVEL CMLI

Parameter	P	V_{DC}	f_{sw}	e_g	f_g	L	R_G	R_P
Value	2.5kW	250V	25kHz	162.63V	50Hz	1.4mH	0.1Ω	0.01Ω
Parameter	R	L_f	C_1	R_T	L_T	C_2	R_d	C_P
Value	0.1Ω	4mH	2μF	50mΩ	900μF	0.329μF	2Ω	10nF

A system with 'P'=2.5kW, then 'V_r' = 233V and 'δ_r'=0.158 rad was considered for both the simulations. Fig. 4.10 (i) and (ii) shows the simulation results of cascaded five-level CMLI with conventional SPWM and proposed PWM techniques respectively. The subplots (a) and (b) of Fig. 4.10 (i) and (ii) show the output voltage of five-level inverter 'v_{ab}' and the

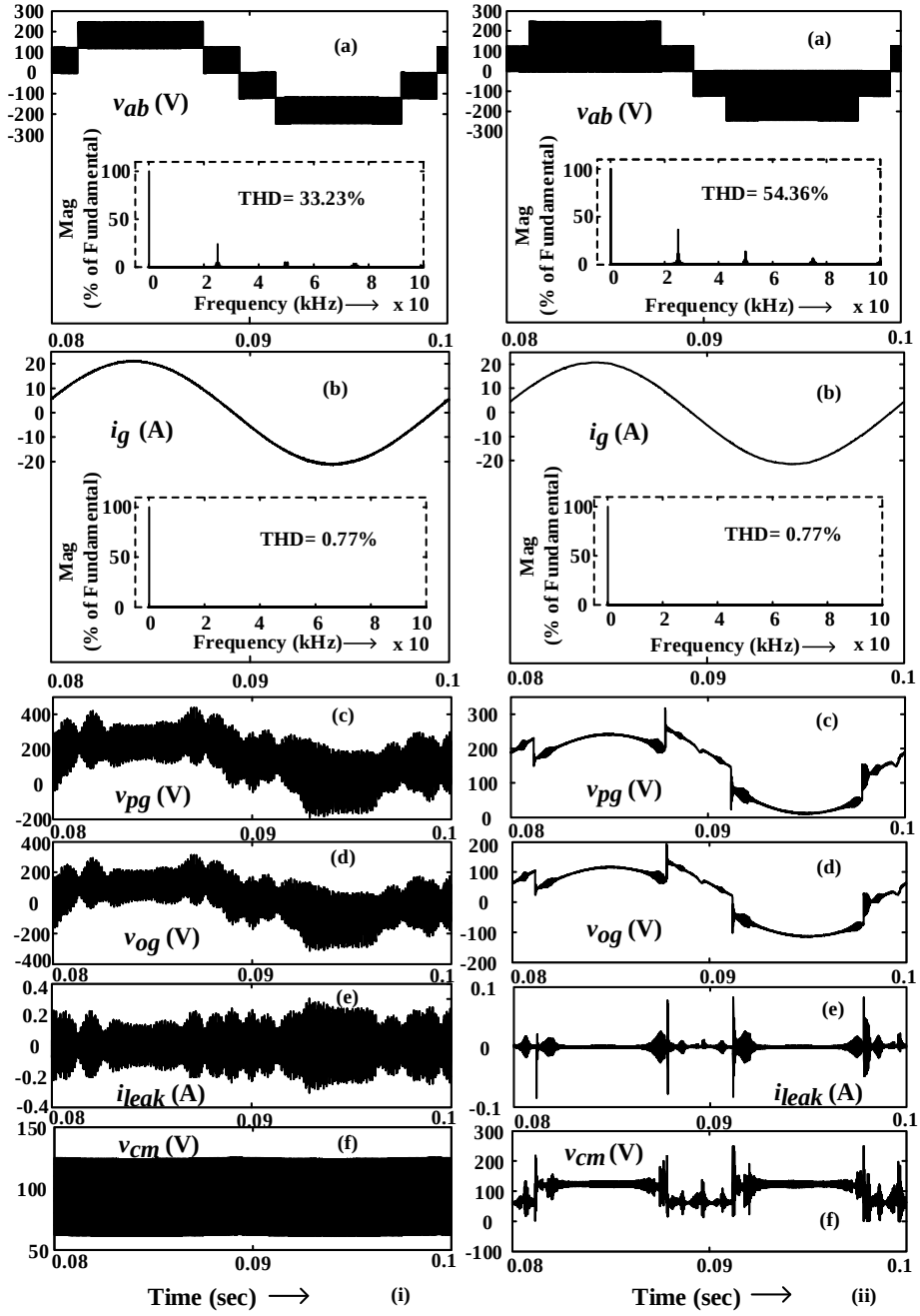


Fig. 4.10. Simulation waveforms of five-level CMLI with (i) conventional SPWM technique (ii) proposed PWM technique. The subplots give the waveforms of: (a) output voltage 'v_{ab}'; (b) grid current 'i_g'; (c) terminal voltage 'v_{pg}'; (d) Terminal voltage 'v_{og}'; (e) leakage current flowing through the parasitic capacitance 'i_{leak}'; (f) common mode voltage 'v_{cm}'.

corresponding grid current 'i_g' respectively. The Fast Fourier Analysis (FFT) of the five-level inverter output voltage 'v_{ab}' and the corresponding grid current 'i_g' was also shown inside the corresponding subplots. It can be observed that the magnitude of higher order harmonics is slightly high in the inverter output voltage 'v_{ab}' for the proposed PWM technique when

compared to the conventional SPWM technique. However, these higher order harmonics can be taken care by the proper design of filter. The subplots (a) of Fig. 4.10 (i) and (ii) also show that the harmonic components at the frequencies in multiple of 25kHz are dominant in both conventional SPWM and proposed PWM techniques. Therefore, design values of the filter remain same for both the cases with the cut-off frequency of 25kHz. It can be easily verified that Total Harmonic Distortion (THD) of the current waveform remains same for conventional SPWM and proposed PWM technique. The THD of the grid current in both the cases meets the requirement of standard IEEE 1547 [41] and it has nearly same value. Another important observation is that, the common mode and terminal voltage waveforms have high-frequency voltage transitions in the conventional SPWM as shown in subplots (c), (d) and (f) of Fig. 4.10 (i). These high-frequency voltage transitions are absent or removed in the case of proposed PWM technique as shown subplots (c), (d) and (f) of Fig. 4.10 (ii). The terminal and common mode voltage waveforms are matching with the results obtained using switching function analysis (Fig. 4.9). This also justifies the analysis done. The presence of high-frequency voltage transitions in the common mode voltage for conventional SPWM technique results in the flow of zero sequence current in the system. This may increase the THD of grid current. Further, the subplots (e) of Fig. 4.10 (i) and (ii) shows the waveform for leakage current 'i_{leak} 'of conventional SPWM and proposed PWM techniques respectively. It can be observed that value of leakage current is around 0.2A in conventional SPWM whereas with proposed PWM its value is less than 0.1A. This can be attributed to low-frequency voltage waveform on the terminal voltages 'v_{og}' and 'v_{pg}'.

Further, proposed PWM also eliminates high-frequency transitions in common mode voltage. This further helps in minimizing the EMI filter requirement for the system [40] using proposed PWM technique compared to conventional SPWM technique. Because of reduction in high-frequency transitions in common mode voltage, the size of EMI filter at the output of inverter is reduced [40]. This may further reduce the cost, weight and size of grid connected system. Again, the FFT was done to further analyze the presence of various high-frequency components in the terminal voltage due to both PWM techniques. Fig. 4.11 shows the FFT plots for terminal voltage of the five-level CMLI. It can be easily verified that the conventional SPWM has significant percentage of high-frequency components more than 50 percent at resonant frequency around 43.316kHz as obtained from (4.4). However, with proposed PWM technique, no significant high-frequency components are present at any value

of high-frequency. Fig. 4.12 shows the FFT analysis of leakage current flowing through the parasitic capacitance of the PV array for five-level CMLI with SPWM technique and proposed PWM technique. The peak magnitude of the leakage current is around 65mA at resonant frequency 43.316kHz calculated from (4.4). With the proposed PWM technique, the

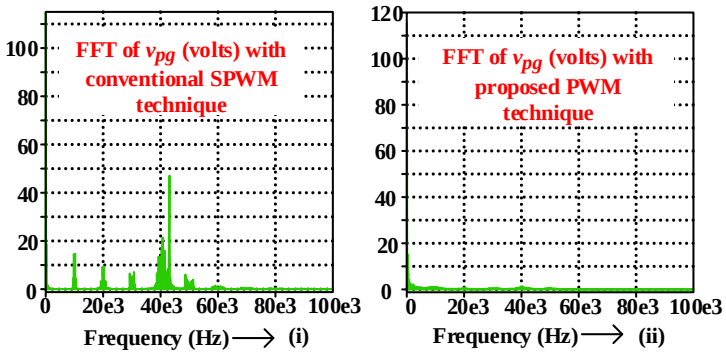


Fig. 4.11. FFT analysis of terminal voltage 'v_{pg}' of the cascaded five-level CMLI with (i) conventional SPWM technique (ii) proposed PWM technique.

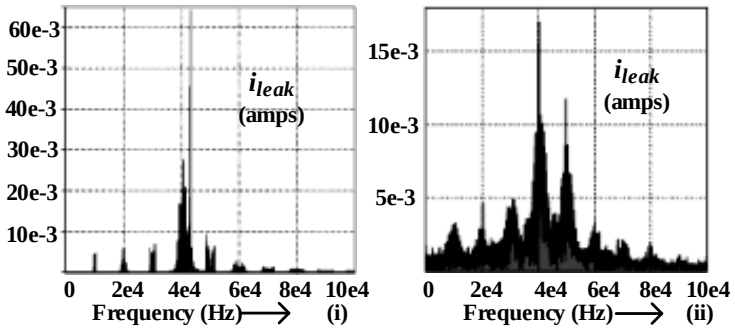


Fig. 4.12. FFT analysis of leakage current 'i_{leak}' flowing through the parasitic capacitance of the PV array for five-level CMLI with (i) conventional SPWM technique (ii) proposed PWM technique.

peak magnitude of leakage current is reduced to 2mA at resonant frequency. Thus, the proposed PWM technique minimizes the leakage current flowing through the parasitic capacitor along with the reduction in size, weight and cost of the grid connected inverter system. However, the switching losses are more in the proposed PWM technique compared to that of conventional SPWM technique. Hence, the five-level CMLI may have slightly reduced efficiency with the proposed PWM technique compared to that of conventional SPWM technique. However, the THD of grid current remains almost same for both the conventional SPWM and proposed PWM techniques.

4.5.2. Simulation for MPPT performance

Simulation was again performed in SIMULINK environment using PV source model. The model of PV module with short circuit current 'I_{sc}' of 3.74A and open circuit voltage 'V_{oc}' of 21.05V at STC is used in the simulation. Two sets having series connection of PV modules were used to form two PV sources 'PV_1' and 'PV_2' for the inverter. The two PV sources 'PV_1' and 'PV_2' are connected to inverter through buffer capacitors 'C_{PV1}' and 'C_{PV2}' respectively of value 6000μF each. The output of five level CMLI is connected to resistive load of 26Ω through the 'LC' filter. Resistive load was used for simplicity in the simulation. Further, the operation of five-level CMLI with the proposed PWM technique to eliminate leakage current will remain nearly same for the grid-connected and stand-alone systems. This can be justified with the fact that the modified reference wave '$v_{ref\_modified}$' will remain same for both, except for the additional calculations of the load angle given in (4.34) and (4.35) for the reference wave 'v_{mod}'.

Fig. 4.13 shows the waveforms obtained from the simulation of the five-level CMLI using two PV sources having same short circuit current of magnitude 3.74A under identical environmental conditions. Fig. 4.13 (I) shows the waveforms for the case when both the PV sources are symmetrical. The two PV sources have equal open circuit voltage given by 105.25 V. Fig. 4.13 (II) and (III) show the waveforms of the five-level CMLI, for the case when both the PV sources are asymmetrical. For Fig. 4.13 (II), the voltage magnitude 'V_{PV1}' for 'PV_1' source is less than the voltage magnitude 'V_{PV2}' for 'PV_2' source as can be seen in subplots (e) and (f) of Fig. 4.13 (II). The open circuit voltage of the PV sources 'PV_1' and 'PV_2' are given by 63.15V and 147.35V respectively. For Fig. 4.13 (III), the voltage magnitude 'V_{PV1}' is greater than the voltage magnitude 'V_{PV2}' as can be observed from subplots (e) and (f) of Fig. 4.13 (III). The open circuit voltages of the PV sources 'PV_1' and 'PV_2' are 147.35V and 63.15V respectively.

The subplots (a) of Fig. 4.13 show the waveform of resultant modulation index 'm_a' for the five-level CMLI. The sub-sub plot in subplots (a) of Fig. 4.13 show the value of resultant modulation index 'm_a' near MPP. Further, the power waveforms of both PV sources 'P_{PV1}' and 'P_{PV2}' are shown in subplots (b) and (c) of Fig. 4.13 respectively. The subplots (d) of Fig. 4.13 show the output power 'P_{OUT}' of the resistive load. It can be observed that the magnitude of power 'P_{OUT}' is nearly equal to sum of the two PV source powers 'P_{PV1}' and

'P_{PV2}'. Further, it also justifies the power balance phenomenon for the two PV sources ('PV_1' and 'PV_2') in the system. Oscillations in the value of 'm_a' and low ripple contents in PV power for both the PV sources indicate operation near to MPP for the proposed system. Further, the ripple content in the power 'P_{PV1}' is high in the case shown in Fig. 4.13 (II) when

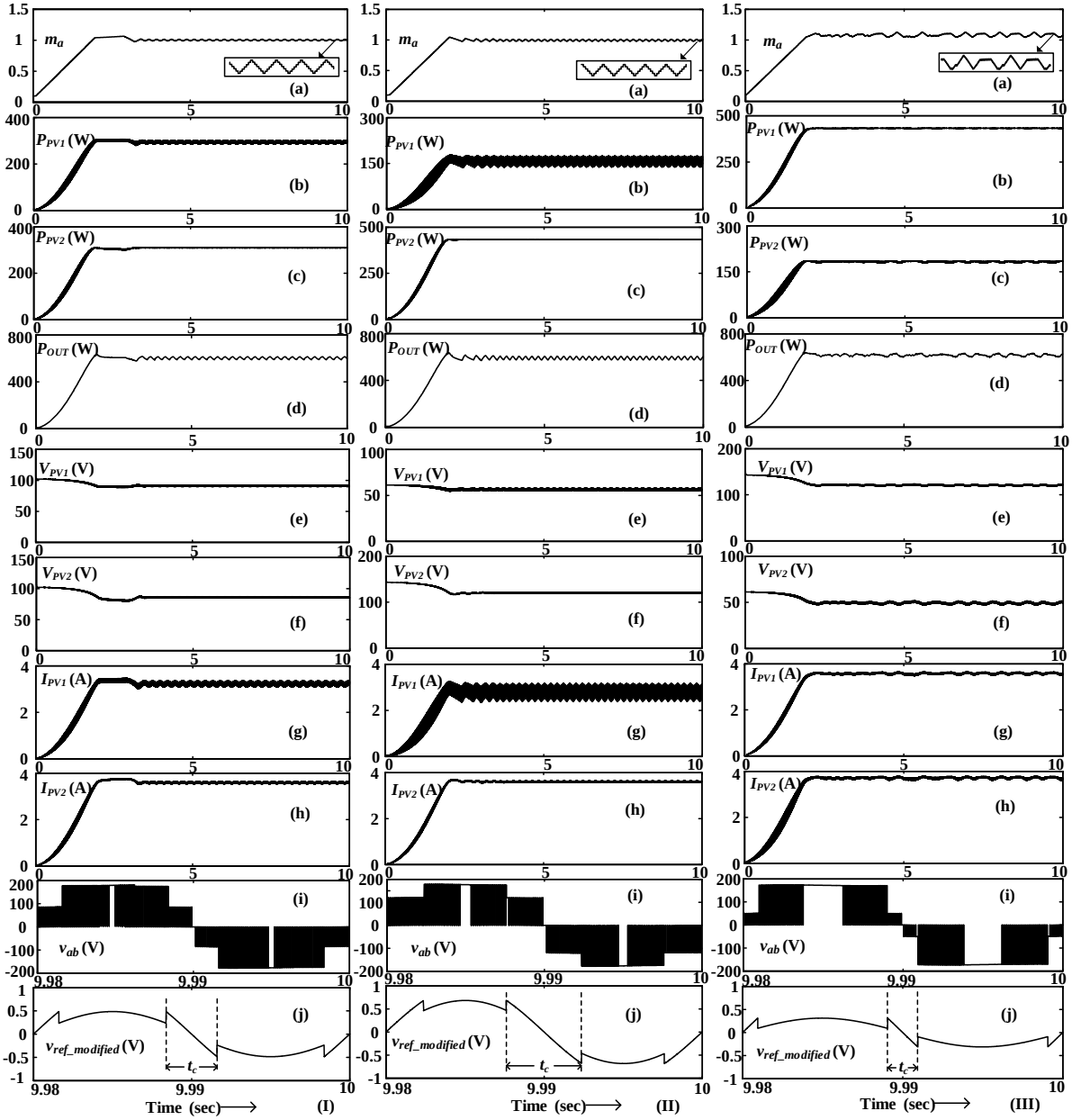


Fig. 4.13. Five-level CMLI with proposed PWM technique and MPPT for case when: (I) 'V_{PV1}' = 'V_{PV2}'; (II) 'V_{PV1}' < 'V_{PV2}'; (III) 'V_{PV1}' > 'V_{PV2}'. The subplots give waveforms of :(a) resultant modulation index 'm_a'; (b) power 'P_{PV1}' from the source 'PV_1' in Watts ; (c) power 'P_{PV2}' from the source 'PV_2' in Watts ; (d) output power 'P_{OUT}' at the resistive load ; (e) voltage 'V_{PV1}' from the source 'PV_1'; (f) voltage 'V_{PV2}' from the source 'PV_2'; (g) current 'I_{PV1}' from the source 'PV_1'; (h) current 'I_{PV2}' from the source 'PV_2'; (i) output voltage 'v_{ab}' of inverter; (j) modified reference wave '$v_{ref\_modified}$'.

compared to the cases shown in Fig. 4.13 (I) and (III). This is due to the fact that non-active power transfer period in the case of Fig. 4.13 (II) asymmetrical configuration is more when compared to that of symmetrical configuration. Therefore, the design value of capacitor 'C_{PV1}' will be still higher when compared to symmetrical configuration. Thus, ripple content in the power 'P_{PV1}' can be minimized by choosing proper value of capacitor 'C_{PV1}' for the asymmetrical configuration. The subplots (c) of Fig. 4.13 show the waveforms of PV power for source 'P_{PV2}'. High ripple content in the power 'P_{PV2}' can be observed in Fig. 4.13 (III) when compared to Figs. 4.13 (I) and (II). This can be attributed to lower value of source voltage when compared to symmetrical configuration. Thus, again the ripple content in 'P_{PV2}' for Fig. 4.13 (III) can be minimized by designing the capacitance 'C_{PV2}' with appropriate voltage of 'V_{PV2}'. The subplots (e) of Fig. 4.13 show the ripple content in the voltage 'V_{PV1}' of Fig. 4.13 (II) is high compared to Fig. 4.13 (I) and (III). Similarly, the ripple content in PV voltage 'V_{PV2}' in subplot (f) of Fig. 4.13 (III) is higher compared to Fig. 4.13 (I) and (II). Similar observations can be seen for the PV currents 'I_{PV1}' and 'I_{PV2}' given in subplots (g) and (h) of Fig. 4.13. Another observation with respect to magnitude of voltage levels can be observed in subplot (i) of Fig. 4.13. Asymmetry in the PV array configuration can be observed from the magnitude of voltage levels. The last subplot (j) of Fig. 4.13 shows the modified reference waveform '$v_{ref\_modified}$' for all cases. Increase and decrease in the non-active period of 'PV_1' source for asymmetrical configurations compared to that of symmetrical configuration can be easily observed as indicated by 't_c' in the subplot.

4.6. Experimental results

To validate the analysis and simulation of the PWM technique, a lab proto-type was fabricated. Specifications and values of the parameters used in the fabricated experimental set-up are described in Table 4.3. Fig. 4.14 gives the photograph of the experimental set-up. The built set-up consists of MOSFETs with part number A0T10T60PLF in the power circuit as a switching devices. Driver IC HCPL 316J is used for driving the switching devices. The

TABLE 4.3. PARAMETERS USED FOR EXPERIMENTAL SET-UP

Parameter	P	V_{DC}	f_{sw}	L	C	R_{load}
Value	400W	200V	10kHz	2mH	50µF	100Ω

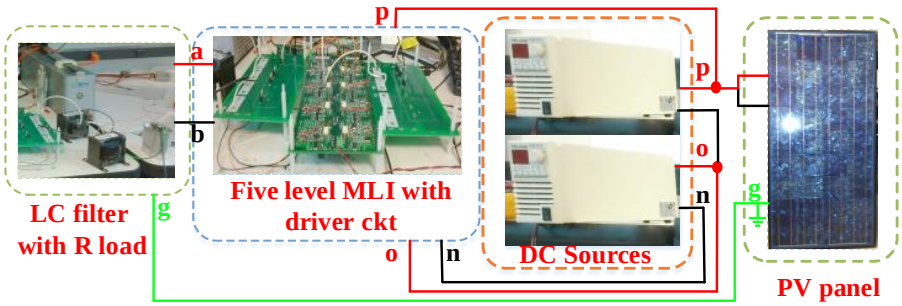


Fig. 4.14. Experimental set-up for five-level CMLI along with PV test source to measure the leakage current.

input of inverter is connected to two programmable DC power supplies made by TDK LAMBDA with model number ZUP120-1.8 as shown in Fig. 4.14. The output of inverter is connected to LC filter and resistive load [42]. The switching pulses for conventional SPWM and proposed PWM techniques for five-level inverter are generated using DSP TMS320F28335. The required PWM pulses are generated in DSP using VISSIM software. All the experimental waveforms were taken in Tektronix DPO 3034.

Fig. 4.15 (i) and (ii) shows the experimental results of the five-level CMLI without inclusion of PV test panel (Fig. 4.14) for conventional SPWM and proposed PWM techniques respectively. The subplot (a) of Fig. 4.15 (i) and (ii) show PWM pulses for switches Sw_1, Sw_2, Sw_4 and Sw_6. The waveform of voltage across resistive load 'v_{load}' is shown in subplot (b) of Fig. 4.15 (i) and (ii). The subplot (c) of Fig. 4.15 (i) clearly indicates the presence of high-frequency voltage transitions in the terminal voltages 'v_{pg}' and 'v_{og}' with the conventional SPWM technique. Experimental waveform for terminal voltage 'v_{pg}' and 'v_{og}' resembles with the waveforms given in the analysis and simulation. Similar observation is applicable for waveforms shown in subplot (c) of Fig. 4.15 (ii). The terminal voltage waveforms obtained from experimental results have low-frequency component and they are similar to what is obtained by simulation and analysis. The presence of low-frequency transitions in the PV terminal voltage justifies low leakage current. The subplot (d) of Fig. 4.15 (i) and (ii) shows the waveform of current 'i_{load}' flowing through resistive load. The peak amplitude of both the current waveforms is nearly same.

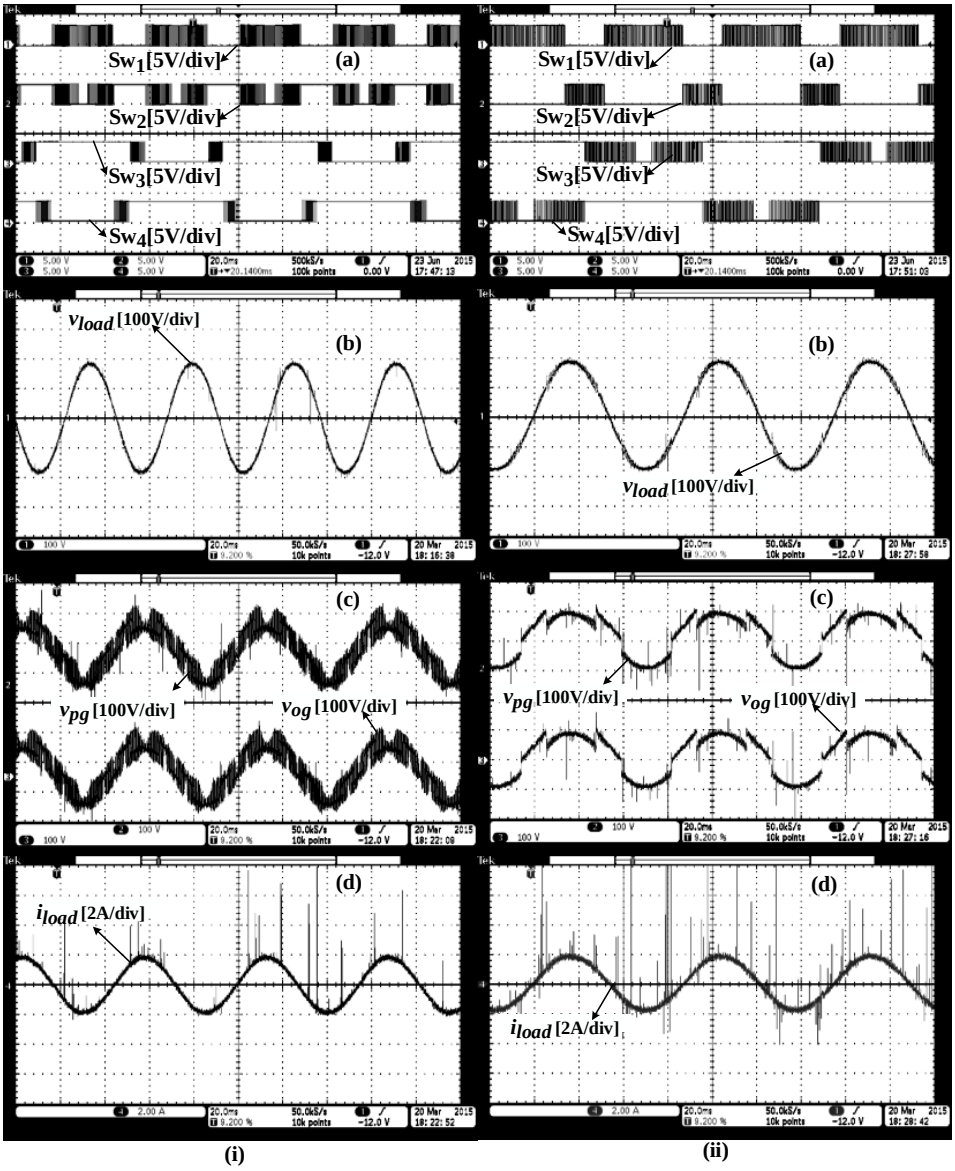


Fig. 4.15. Experimental waveforms of the five-level CMLI with the (i) conventional SPWM technique and (ii) proposed PWM technique. The subplots show: (a) PWM gating pulses for switches S_{W1}, S_{W2}, S_{W4}, S_{W6}; (b) voltage across load 'v_{load}'; (c) terminal voltage 'v_{pg}', 'v_{og}'; (d) load current flowing through resistive load 'i_{load}' set-up for five-level CMLI along with PV test panel to measure the leakage current.

To measure actual leakage current 'i_{leak}' again same set-up was utilized with the inclusion of PV module (Fig. 4.14). However, in the given set-up the power supply DC voltage is reduced to 50V. This is done to protect PV panel from damage. The positive and negative terminals of PV panel are shorted and are connected to node 'p' as indicated in Fig. 4.14. The metallic frame or ground point from PV module is connected to node 'g' (Fig. 4.14). Current flowing through between metallic frame and node 'g' is measured using current probe. Fig. 4.16 shows the experimental results obtained using (i) conventional SPWM and

(ii) proposed PWM techniques. It can be easily observed from the experimental result that the magnitude of leakage current in proposed PWM technique is lower in comparison with conventional SPWM.

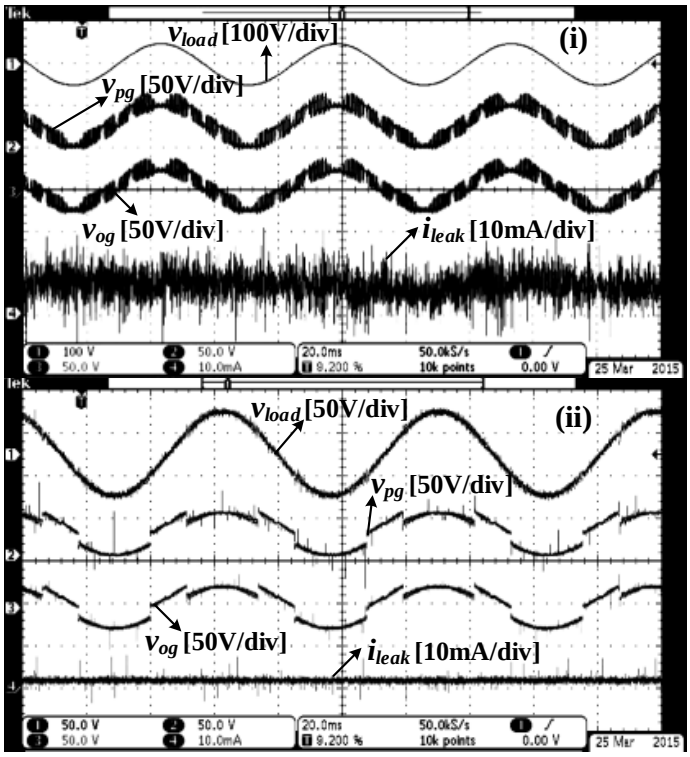


Fig. 4.16 Experimental waveforms of voltage across load 'v_{load}', terminal voltage 'v_{pg}', terminal voltage 'v_{og}' and current flowing through parasitic capacitance of PV test panel 'i_{leak}' for five-level CMLI with (i) conventional SPWM technique (ii) proposed PWM technique.

Again, now the experiment was performed to capture the waveform of leakage current with a series branch of resistance 'R_p' and capacitance 'C_p' connected at the nodal point 'p' (as shown in Fig. 4.1) of the fabricated inverter without inclusion of PV panel. The current flowing through this branch is measured using the Tektronix current probe TCS0030. Output of the inverter is connected to resistive load through a LC filter. The operation of five-level CMLI for the proposed PWM technique to eliminate leakage current will remain nearly same for the grid-connected and stand-alone systems except for the additional calculations of the load angle as given in (4.34) and (4.35) for 'v_{mod}'. During the zero state, grid or stand-alone load is isolated from the PV array. So, the concept for minimization of leakage current remains same for both the grid-connected and stand-alone load systems. Table 4.4 shows the value of different parameters considered for the experimental setup. Fig. 4.17 shows the waveforms of voltage across the resistive load 'v_{load}', terminal voltage 'v_{pg}', 'v_{og}' and the load

TABLE 4.4. VALUES USED FOR EXPERIMENTAL SET-UP

Parameter	P	V_{DC}	f_{sw}	L	C	R_{load}	R_p	C_p
Value	54W	100V	10kHz	2mH	1.25µF	185Ω	5 Ω	330nF

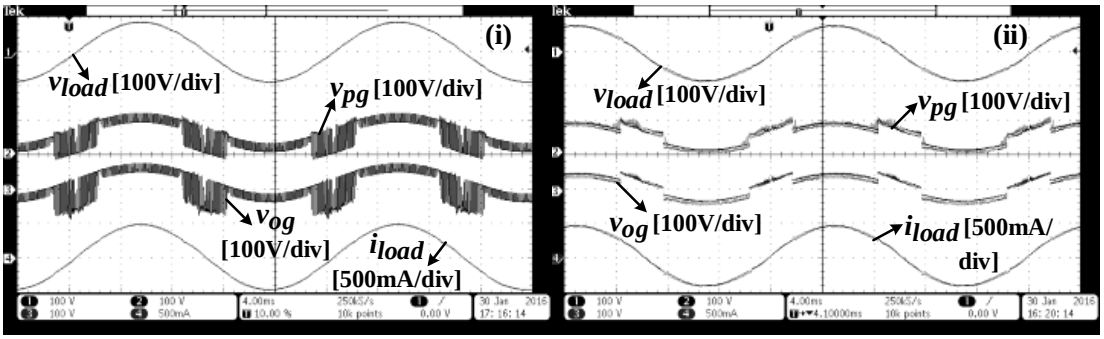


Fig. 4.17. Experimental waveforms of voltage across load 'v_{load}', terminal voltage 'v_{pg}', terminal voltage 'v_{og}' and 'i_{load}' current flowing through load for five-level CMLI with (i) conventional SPWM technique (ii) proposed PWM technique.

current flowing through the resistive load 'i_{load}' for the conventional SPWM technique and proposed PWM technique respectively. Fig. 4.18 shows the waveforms of terminal voltage 'v_{og}' and leakage current 'i_{leak}' flowing through the 'R_p' – 'C_p' branch for both conventional SPWM and proposed PWM techniques. With the conventional SPWM technique the spikes in the leakage current is observed for the complete cycle of terminal voltage 'v_{og}' as shown in Fig. 4.18 (i). Using the proposed PWM technique, spikes of comparatively low magnitude is observed in leakage current during the transition in the terminal voltage 'v_{og}' as observed from Fig. 4.18 (ii).

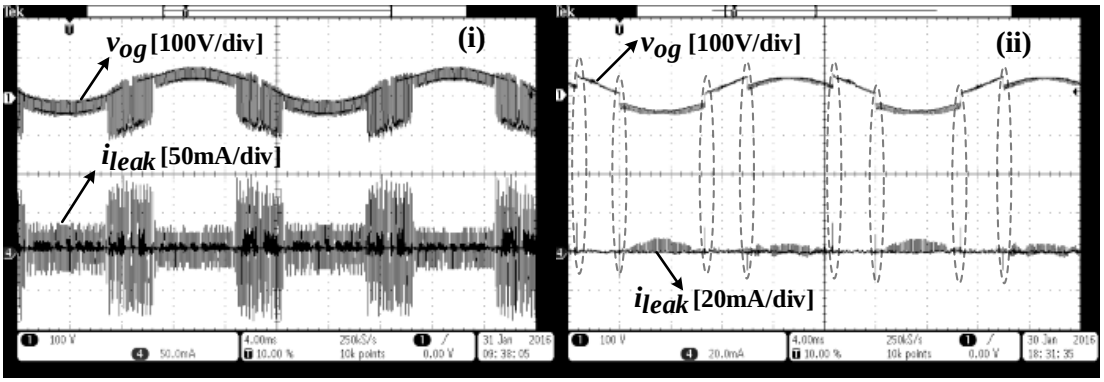


Fig. 4.18. Experimental waveforms of terminal voltage 'v_{og}' and 'i_{leak}' current flowing through 'R_p'-'C_p' branch for five-level CMLI with (i) conventional SPWM technique (ii) proposed PWM technique.

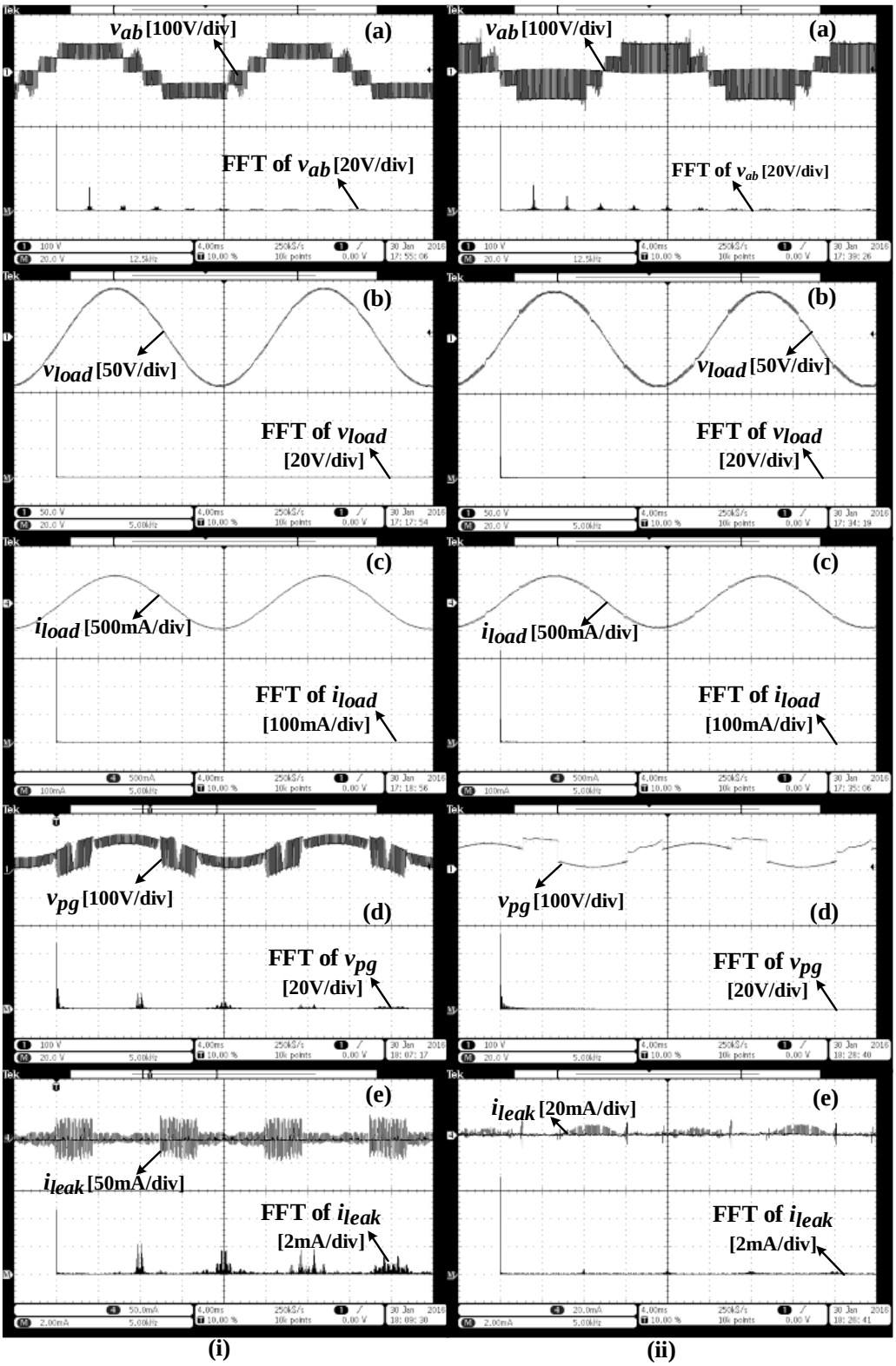


Fig. 4.19. Experimental waveforms for five-level CMLI with (i) conventional SPWM technique (ii) proposed PWM technique. The subplots shows: (a) output voltage 'v_{ab}' and FFT analysis of 'v_{ab}';(b) voltage across load 'v_{load}' and FFT analysis of 'v_{load}'; (c) current 'i_{load}' and FFT analysis of 'i_{load}'; (d) terminal voltage 'v_{pg}' and FFT analysis of 'v_{pg}'; (e) leakage current 'i_{leak}' and FFT analysis of 'i_{leak}'.

Fig. 4.19 shows the FFT analysis or harmonic spectrum of various waveforms of five-level CMLI with (i) conventional SPWM and (ii) proposed PWM techniques respectively. The subplots (a), (b) and (c) of Fig. 4.19 shows the FFT analysis spectrum for output voltage 'v_{ab}' of the inverter, load voltage 'v_{load}' across the load and current 'i_{load}' flowing through the resistive load respectively. It can be observed that the harmonic content in output voltage 'v_{ab}' of the inverter, load voltage 'v_{load}' across the load and current 'i_{load}' for both conventional SPWM and proposed PWM technique is nearly same. The subplots (d) and (e) of Fig. 4.19 show the FFT analysis spectrum for terminal voltage 'v_{pg}' and leakage current 'i_{leak}' flowing through series connected 'R_p'-'C_p' branch. It can be observed that the harmonic component at resonant frequency around 9kHz obtained using (4.4) is high in case of conventional SPWM technique. Using the proposed PWM technique, the high-frequency components are absent in the terminal voltage. Since the high-frequency components are absent with the proposed PWM, the size of EMI filter required is reduced. This may further reduce the cost, size and weight of the system. Hence, using the proposed PWM technique the leakage current flowing through the parasitic capacitance is less compared to that of conventional SPWM technique.

4.7. Conclusion

This chapter presents a PWM technique for minimization of the leakage current in transformerless grid tie PV inverter. The proposed PWM technique requires less number of carrier waves when compared to the conventional SPWM technique. The proposed PWM technique is also integrated with MPPT technique for the operation of two PV sources near MPP. Using the proposed PWM technique, leakage current is minimized without addition of any extra switches. The proposed PWM technique eliminates high-frequency voltage transitions in PV terminal and common voltage of the inverter. The elimination of high-frequency voltage transition results in reduction of leakage current magnitude flowing through the parasitic capacitance. It may also reduce the requirement or size of EMI or common mode filters required in the system. Further, the analysis for the PV terminal and common mode voltages is also explained in the chapter. Using the proposed analysis, PWM technique can be studied and modified, so that high-frequency voltage transitions can be avoided in the PV terminal and common mode voltage. So given analysis is useful in defining the appropriate PWM strategy for the minimization of the leakage current. The analysis given in the chapter is verified with simulation and experimental results in the chapter.

CHAPTER 5

A Highly Efficient and Reliable Inverter Configuration Based Cascaded Multi-Level Inverter for PV Systems

Chapter 5

A Highly Efficient and Reliable Inverter Configuration Based Cascaded Multi-Level Inverter for PV Systems

Using the proposed PWM technique for the single-phase five-level CMLI in chapter 4, the magnitude of leakage current is minimized. However, the objective of high efficiency is not achieved. In order to meet the objective of highly efficiency, an improved Cascaded Multi-Level Inverter (CMLI) based on a highly efficient and reliable configuration for the minimization of the leakage current is proposed in chapter 5. Apart from a reduced switch count, the proposed scheme has additional features of low switching and conduction losses. The proposed topology with the given PWM technique reduces the high-frequency voltage transitions in the terminal and common-mode voltages. Avoiding high-frequency voltage transitions achieves the minimization of the leakage current and reduction in the size of EMI filters. Furthermore, the extension of the proposed CMLI along with the PWM technique for '*2m+1*' levels is also presented, where '*m*' represents the number of Photo Voltaic (PV) sources. The proposed PWM technique requires only a single carrier wave for all '*2m+1*' levels of operation. The Total Harmonic Distortion (THD) of the grid current for the proposed CMLI meets the requirements of IEEE 1547 standard. A comparison of the proposed CMLI with the existing PV Multi-Level Inverter (MLI) topologies is also presented in the chapter. Complete details of the analysis of PV terminal and common-mode voltages of the proposed CMLI using switching function concept, simulations, and experimental results are presented in below sections.

5.1. Operation of proposed cascaded five-level MLI

The schematic circuit diagram of the proposed five-level CMLI for PV system is shown in Fig. 5.1. The given configuration consists of two converters ('Conv-1' and 'Conv-2'). 'Conv-1' is a half-bridge inverter comprising two switches Sw_1 and Sw_2. The 'Conv-2' comprises of a highly efficient and reliable inverter configuration [43] with six switches (Sw_3 to Sw_8). Among the six switches, four switches (Sw_3 to Sw_6) in 'Conv-2' constitute an H-bridge circuit. The remaining two switches Sw_7 and Sw_8 in 'Conv-2' are bi-directional switches. The switches in the 'Conv-1' are used to generate the voltage levels of 'V_{PV}' and

'$V_{PV}/2$'. When switch Sw_1 is turned ON, the voltage V_{PV} is applied at the terminal '*z*' with respect to the terminal '*n*'. Similarly, the terminal '*z*' attains the voltage '$V_{PV}/2$' when switch Sw_2 is turned ON. The switches Sw_1 and Sw_2 are complementary in nature. The generated voltage levels at the terminal '*z*' of 'Conv-1' are given as an input to the 'Conv-2'. The 'Conv-2' generates the positive, negative and zero levels of corresponding input voltage (voltage between the terminals '*z*' and '*n*') across the load. The bi-directional switches Sw_7 and Sw_8 provide the free-wheeling path during zero voltage state. The output of the five-level CMLI is connected to the grid through an LCL filter as shown in Fig. 5.1 [20-21, 34]. It consists of inverter side inductance 'L_f', capacitance 'C_f' and grid side inductance '*L*'. The resistance 'R_d' in the shunt branch of the filter is used as a damping resistor. The resistance '*R*' refers to the grid side resistance, and the resistance 'R_G' indicates resistance in the ground path. The variable 'e_g' refers to instantaneous grid voltage. The variables 'R_p' and 'C_p' refer to the parasitic resistance and capacitance in the PV system, respectively shown with dotted lines in Fig. 5.1. The parasitic capacitance in PV system forms a resonant circuit with the filter inductances [21]. The variables 'i_l', 'i_p' and 'i_g' denote the output current of five-level CMLI, current flowing through shunt branch of the filter and the current flowing into the grid respectively. The current 'i_{leak}' indicates the leakage current flowing from the PV array into the ground through parasitic capacitance (see Fig. 5.1).

The proposed MLI topology contains four pairs of complementary switches (Sw_1, Sw_2), (Sw_3, Sw_4), (Sw_5, Sw_6) and (Sw_7, Sw_8) in the proposed configuration. However,

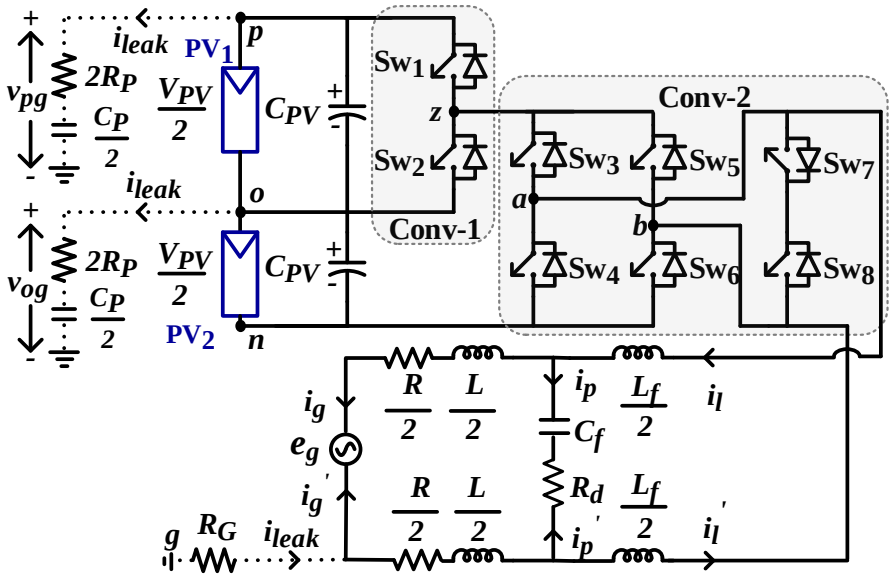


Fig. 5.1. Proposed five-level grid-connected CMLI with PV and parasitic elements.

to minimize the leakage current, the complementary switching is employed only for the two pairs of switches (Sw_1, Sw_2) and (Sw_7, Sw_8). Avoiding complementary action for the other pairs of switches helps in isolating the PV and the grid source during zero voltage state.

Fig. 5.2 shows the operation of the inverter in all its switching states. The inverter output voltage 'v_{ab}' at different voltage levels with the corresponding switching states of all the switches are shown in Table 5.1. The inverter output voltage 'v_{ab}' attains the voltage levels '$+V_{PV}$' or '$-V_{PV}$' when switch Sw_1 is turned ON along with other inverter switches (Sw_3, Sw_6) or (Sw_4, Sw_5) respectively as shown in Figs. 5.2 (a) and 5.2 (e). Similarly, the voltage levels '$+V_{PV}/2$' or '$-V_{PV}/2$' are obtained at 'v_{ab}' when switch Sw_2 is turned ON with the same switching combinations as shown in Figs. 5.2 (b) and 5.2 (d). The most important feature to be noticed during zero voltage state or free-wheeling stage is the isolation or disconnection between PV source and the grid. The isolation between the PV source and the grid can be achieved by turning OFF all the switches of H-bridge inverter as shown in Fig. 5.2 (c).

The turn-OFF state of four switches in H-bridge during zero voltage state results in the isolation of PV source from the grid. The bi-directional switches Sw_7 and Sw_8 provide a free-wheeling path for the inductor current during the turn-OFF period of a switching cycle. This action helps in minimizing the leakage current flowing through the parasitic capacitance. As there is no direct connection between the two sources, the PV terminal points (nodes '*p*', '*o*' and '*n*') float and have undefined voltages. The float or undefined value restricts the terminal voltages from becoming zero. Thus, high-frequency voltage transitions at the PV terminals are avoided. In other words, the possibility of the flow of leakage current can be minimized. Also, in the other intermediate states like switching between '$V_{PV}/2$' to 'V_{PV}' or vice-versa, again the same principle can be used. The above action further helps in the minimization of the leakage current in the PV system. The PWM technique for the proposed five-level CMLI is broadly discussed in next section. The expression for the pole voltages 'v_{an}' and 'v_{bn}' are given in (5.1) and (5.2) respectively.

$$v_{an} = \left(S_1 S_3 + 0.5 S_2 S_3 - \frac{1}{(S_3 + S_4)} + \frac{1}{(S_3 + S_4)(S_1 + S_2)} \right) V_{PV} \tag{5.1}$$

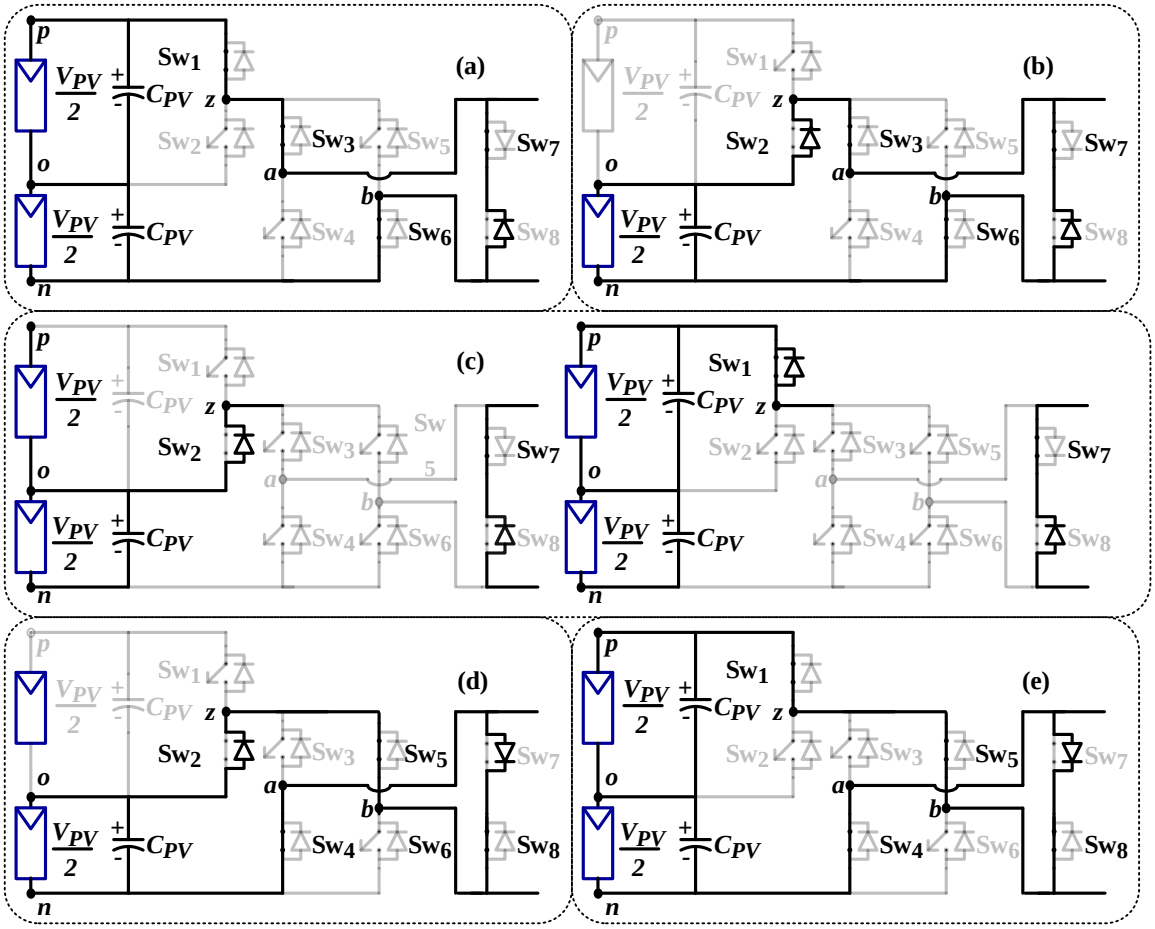


Fig. 5.2. Single Phase five-level cascaded MLI for output voltage levels (a) '$+V_{PV}$'; (b) '$+V_{PV}/2$'; (c) '*0*'; (d) '$-V_{PV}/2$'; (e) '$-V_{PV}$'.

TABLE 5.1. SWITCHING STATES WITH THEIR RESPECTIVE OUTPUT VOLTAGE

Sw1	**Sw2**	**Sw3**	**Sw4**	**Sw5**	**Sw6**	**Sw7**	**Sw8**	v_{ab}
1	0	1	0	0	1	1	0	$+ V_{PV}$
0	1	1	0	0	1	1	0	$+ V_{PV}/2$
0	1	0	0	0	0	1	0	0
1	0	0	0	0	0	1	0	0
0	1	0	1	1	0	0	1	$-V_{PV}/2$
1	0	0	1	1	0	0	1	$-V_{PV}$

$$v_{bn} = \left(S_1 S_5 + 0.5 S_2 S_5 - \frac{1}{(S_5 + S_6)} + \frac{1}{(S_5 + S_6)(S_1 + S_2)} \right) V_{PV} \qquad (5.2)$$

where S_x, (x=1, 2, 3...) is the switching state of switch Sw_x whose value can be either '*1*' (stands for turn-ON) or '*0*' (stands for turn-OFF) respectively.

Fig. 5.3 shows the switching pattern of all the switches for the corresponding inverter output voltage 'v_{ab}'. The switches Sw_1 and Sw_2 in the half-bridge are operated at low switching frequency. In order to eliminate the high switching frequency operation, the switch Sw_2 is kept turned ON in zero state during voltage transition between the levels '*0*' to '$V_{PV}/2$'. Similarly, the switch Sw_1 is kept turned ON, during voltage transition between levels '*0*' to 'V_{PV}'. The inverter switch pair (Sw_3, Sw_6) is operated with a high switching frequency during positive half-cycle, and it remains at the turn-OFF state during the negative half-cycle of the inverter output voltage 'v_{ab}'. A similar operation is applicable to the other inverter switch pair (Sw_4, Sw_5), which is operated with higher switching frequency during the negative half-cycle.

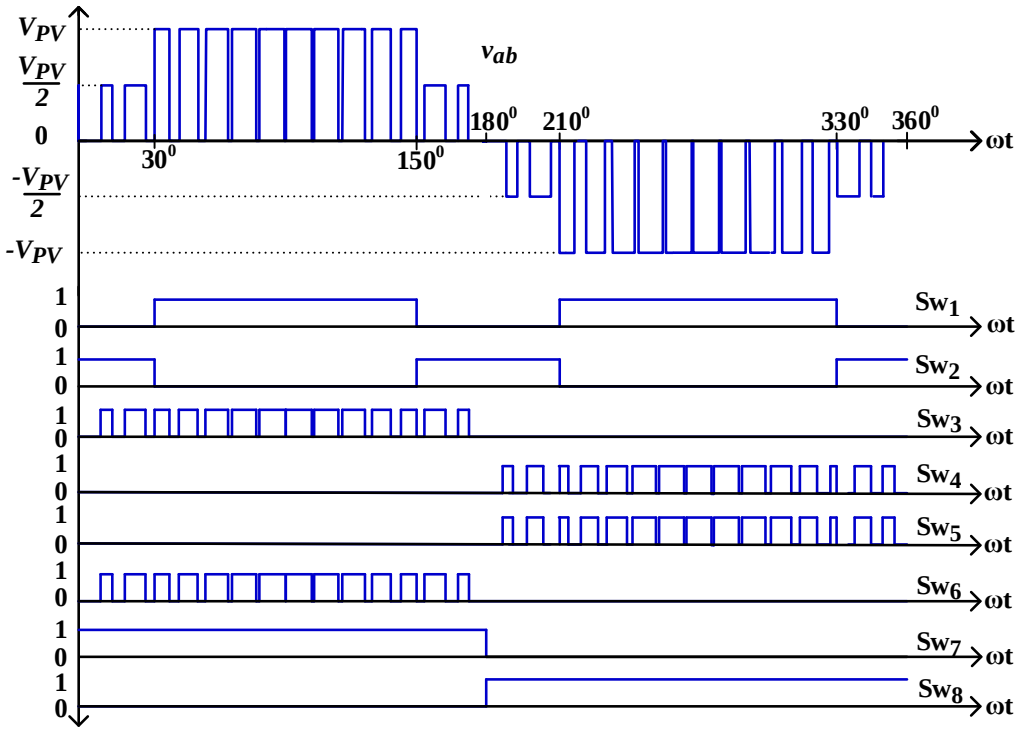


Fig. 5.3. Gate pulses for the switches corresponding to inverter output voltage.

The switches Sw_7 and Sw_8 are turned ON during positive and negative half cycles of the output voltage 'v_{ab}' respectively. The removal of complementary action from the pair of switches (Sw_3, Sw_4) and (Sw_5, Sw_6) facilitates complete turn-OFF of the switches during each

half-cycle of the output voltage 'v_{ab}'. Thus, the proposed system has the advantage of reduced switching losses, realizing to a highly efficient and reliable inverter configuration which may result in higher efficiency.

The generalized topology for '*2m+1*' levels can also be obtained for the proposed five-level CMLI. The number of PV sources in CMLI is denoted by the term '*m*'. The value of '*m*' is always an integral multiple of 2 (i.e., '*m*' =2, 4…). The extended version of the proposed CMLI for '*2m+1*' levels is presented in Fig. 5.4. The generalized topology is obtained by cascading the basic units consisting of half-bridge and H-bridge. The bi-directional switches are connected in between the output terminals for the free-wheeling period. The proposed generalized '*2m+1*' level MLI is also compared with the half-bridge and full-bridge modular multi-level converter. The half-bridge modular multi-level converter requires less number of switches when compared to the proposed generalized '*2m+1*' level MLI. However, it is difficult to reduce or minimize the flow of leakage current in the half-bridge modular multi-level converter. Also, the number of electrolytic capacitors used at the input side of the half-bridge modular multi-level converter is high compared to the proposed generalized '*2m+1*' level MLI. The proposed MLI has a lesser device count when compared to the full-bridge modular multi-level converter [44]. However, both can minimize the leakage current flowing through the PV system.

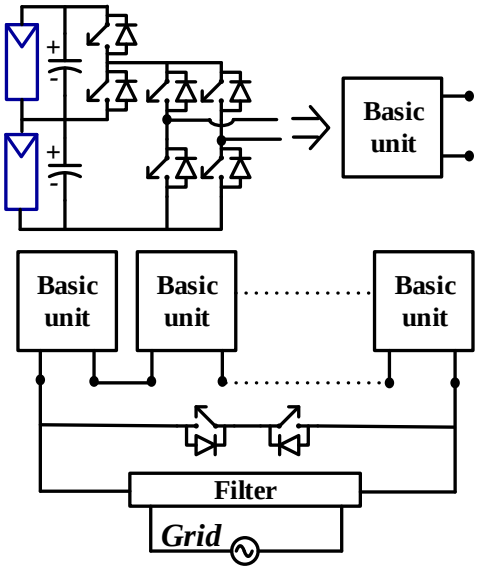


Fig. 5.4. Generalized '*2m+1*' level MLI topology derived from proposed five-level CMLI.

5.2. Proposed PWM strategy along with generalized strategy for minimization of the leakage current

The operation of the proposed PWM technique is explained by considering the given five-level CMLI. The high-frequency transitions in the terminal voltages 'v_{pg}' and 'v_{og}' of five-level CMLI are minimized using the proposed PWM technique. The suggested action can be achieved by switching from 'V_{PV}' to '*0*' state or vice-versa instead of the switching from 'V_{PV}' to '$V_{PV}/2$' state or vice-versa. Additionally, during the zero voltage state or free-wheeling period of the switching cycle, the PV array is isolated from the grid. The isolation of the PV array and the grid during zero voltage state is similar to the inverter configuration reported in [43]. The magnitude of reference wave 'v_{mod}' is lowered to 50% of its original value whenever the switching is toggled amongst the levels 'V_{PV}' and '*0*'. The above action is mainly done to accommodate the value of PV voltage 'V_{PV}'. The modification in the value of 'v_{mod}' is done whenever the instantaneous magnitude of modulating wave 'v_{mod}' exceeds the value of '$m_a/2$', where 'm_a' refers to the modulation index. By incorporating the desired modification, the output voltage includes the zero voltage state (i.e., free-wheeling state) in all its switching periods. The expression for modified reference waveform '$v_{ref\_modified}$' is given in (5.3).

$$v_{ref\_modified} = \begin{cases} v_{mod} & for \quad 0 \le |v_{mod}| < \dfrac{m_a}{2} \quad from \ \dfrac{V_{PV}}{2} \ to \ 0 \\ \dfrac{v_{mod}}{2} & for \quad \dfrac{m_a}{2} \le |v_{mod}| < m_a \quad from \ V_{PV} \ to \ 0 \end{cases} \tag{5.3}$$

where, $v_{mod} = m_a \sin\omega t$ gives the magnitude of v_{mod}.

The output voltage of the proposed PWM technique for the five-level CMLI is shown in Fig. 5.5. In Fig. 5.5 the modified reference wave is compared with the triangular carrier wave. During the positive half-cycle of voltage 'e_g', whenever the phase angle 'ωt' lies in range 0^0 to 30^0 and the instantaneous magnitude of '$v_{ref\_modified}$' exceeds the carrier wave, then 'v_{ab}' attains the voltage level of '$V_{PV}/2$' otherwise, it is switched zero voltage state. Similarly, when 'ωt' lies in the range 30^0 to 150^0, the inverter output voltage 'v_{ab}' attains the voltage level of 'V_{PV}' whenever the instantaneous magnitude '$v_{ref\_modified}$' exceeds the carrier wave or attains zero value otherwise. In the same positive half-cycle, for the remaining range of 'ωt' (i.e., between 50^0 to 180^0), 'v_{ab}' attains the voltage levels '$V_{PV}/2$' if the instantaneous

magnitude of '$v_{ref\_modified}$' is greater than the carrier wave. A similar sequence is adopted during the negative half-cycle of voltage 'e_g'. Thus, in the complete cycle if the magnitude of '$v_{ref\_modified}$' is less than the carrier wave, then 'v_{ab}' attains zero voltage level.

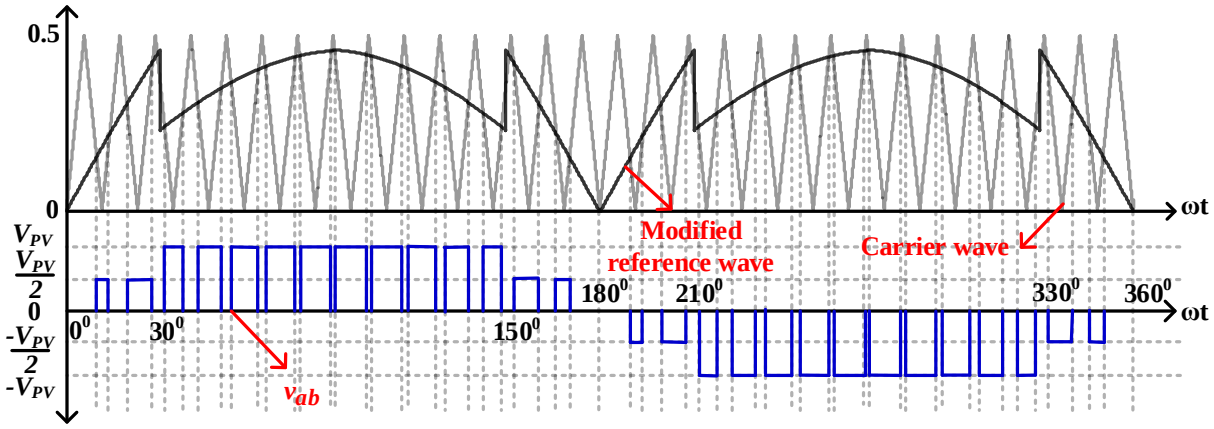


Fig. 5.5. The waveform of output voltage v_{ab} for the proposed PWM technique.

For the implementation of the proposed PWM to a '$2m+1$' level inverter, the waveform of generalized modified reference wave '$v_{ref\_modified\_gen}$' is shown in Fig. 5.6. The term 'm' refers to the number of PV sources used. Whenever the instantaneous absolute magnitude of 'v_{mod}' exceeds the value $j(m_a/m)$, the magnitude of '$v_{ref\_modified\_gen}$' becomes $k(|v_{mod}|/m)$ where j= 1, 2,… m-1, m and k = 1, 2, … m-1. The expression for the '$v_{ref\_modified\_gen}$' is given in (5.4).

$$v_{ref\_modified\_gen} = \begin{cases} v_{mod} \ for \quad 0 \le |v_{mod}| < \frac{m_a}{m} \quad from \ \frac{V_{PV}}{m} \ to \ 0 \\ \frac{v_{mod}}{2} \ for \quad \frac{m_a}{m} \le |v_{mod}| < \frac{2m_a}{m} \quad from \ \frac{2V_{PV}}{m} \ to \ 0 \\ \vdots \\ \frac{v_{mod}}{m} \ for \quad \frac{(m-1)m_a}{m} \le |v_{mod}| < m_a \quad from \ V_{PV} \ to \ 0 \end{cases} \tag{5.4}$$

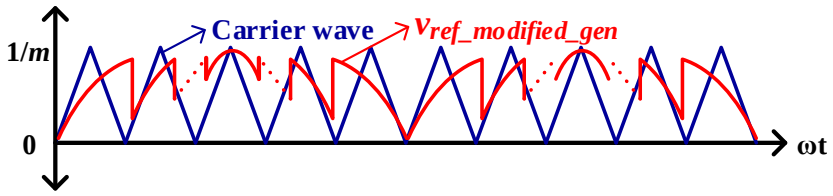


Fig. 5.6. The waveform of generalized modified reference wave $v_{ref\_modified\_gen}$.

5.3. Integration of MPPT for proposed five-level CMLI

The well-known perturb and observe algorithm [45] is employed for the two PV sources (considering five-level operation) individually to track Maximum Power Point (MPP). Thus, each MPPT algorithm tracks the MPP for respective PV sources. To track the MPP, the required information of (i) the average values of the two PV source voltages ('V_{PV1}' and 'V_{PV2}' for the PV sources PV_1 and PV_2 respectively) and (ii) the currents ('I_{PV1}' and 'I_{PV2}' for the PV sources 'PV_1' and 'PV_2' respectively) are sensed and then given to their respective MPPT algorithms. The MPPT algorithms then use the sensed values of the PV voltages and currents for the calculation of the individual values of the modulation indices 'm_{a1}' and 'm_{a2}' for the two PV sources 'PV_1' and 'PV_2' respectively. The outputs of two MPPT algorithms are then utilized for the calculation of overall modulation index m_a. The expression for 'm_a' is given in (5.5).

$$m_a = m_{a1}\frac{V_{PV1}}{V_{PV1}+V_{PV2}} + m_{a2}\frac{V_{PV2}}{V_{PV1}+V_{PV2}} \tag{5.5}$$

The calculated modulation index 'm_a' is then used by the PWM strategy as described in the above section to generate the PWM pulses for the proposed five-level CMLI.

5.4. Analytical expressions of PV terminal voltage and common-mode voltage for proposed cascaded five-level MLI

The analysis of the leakage current can be carried out from the expression of terminal voltages 'v_{pg}', 'v_{og}' and 'v_{ng}'. The expression for the PV terminal voltages can be derived from switching function analysis [19]. From Fig. 5.1, using the superposition theorem, the PV terminal voltages 'v_{pg}' and 'v_{og}' are expressed as follows:

$$v_{pg} = S_1 v_{p1g} + S_2 v_{p2g} \tag{5.6}$$

$$v_{og} = S_1 v_{o1g} + S_2 v_{o2g} \tag{5.7}$$

The terms 'v_{p1g}' and 'v_{o1g}' are the voltages at terminals 'p' and 'o' respectively when switch Sw_1 is turned ON. Similarly, 'v_{p2g}' and 'v_{o2g}' are the voltages at terminals 'p' and 'o' respectively when switch Sw_2 is turned ON.

The expression for the voltage 'v_{ng}' when switch Sw_1 is turned ON is given in (5.8).

$$v_{ng} = v_{p1g} - V_{PV} \tag{5.8}$$

Similarly, the expression for terminal voltage 'v_{ng}' when switch Sw_2 is turned ON is given in (5.9).

$$v_{ng} = v_{o2g} - \frac{V_{PV}}{2} \tag{5.9}$$

With the use of switching function analysis, the voltages 'v_{ag}' and 'v_{bg}' (from Fig. 5.1 and Fig. 5.2) expressed in terms of 'v_{p1g}' and 'v_{ng}' are shown in (5.10) and (5.11) respectively.

$$v_{ag} = S_1 S_3 v_{p1g} + S_4 v_{ng} \tag{5.10}$$

$$v_{bg} = S_1 S_5 v_{p1g} + S_6 v_{ng} \tag{5.11}$$

Similarly, the voltages 'v_{ag}' and 'v_{bg}' (from Fig. 5.1 and Fig. 5.2) expressed in terms of 'v_{o2g}' and 'v_{ng}' using switching functions are shown in (5.12) and (5.13) respectively.

$$v_{ag} = S_2 S_3 v_{o2g} + S_4 v_{ng} \tag{5.12}$$

$$v_{bg} = S_2 S_5 v_{o2g} + S_6 v_{ng} \tag{5.13}$$

Now expressing the voltages 'v_{ag}' and 'v_{bg}' in terms of the grid voltage 'e_g', the voltage drop in filter inductors ('L_f' and 'L') and resistances ('R' and 'R_g') [19] can be given by:

$$v_{ag} = \frac{L_f}{2}\frac{di_l}{dt} + \frac{L}{2}\frac{di_g}{dt} + e_g + \frac{R}{2} i_g - R_G i_{leak} \tag{5.14}$$

$$v_{bg} = \frac{L_f}{2}\frac{di_l'}{dt} + \frac{L}{2}\frac{di_g'}{dt} + \frac{R}{2} i_g' - R_G i_{leak} \tag{5.15}$$

Now with the addition of (5.14) and (5.15), and by ignoring the voltage drop in resistances 'R_G' and '$R/2$' with assumptions of 'i_g'= '$-i_g$'' and 'i_l'= '$-i_l$'' , [19] gives:

$$v_{ag} + v_{bg} = e_g \tag{5.16}$$

Substituting the values of 'v_{ag}' and 'v_{bg}' from (5.10) and (5.11) in (5.16) and simplifying those using (5.8) gives the expression for the terminal voltage 'v_{p1g}' in (5.17).

$$v_{p1g} = \frac{e_g + V_{PV}\left(S_4 + S_6\right)}{\left(S_1S_3 + S_1S_5 + S_4 + S_6\right)} \tag{5.17}$$

Now, the other terminal voltage 'v_{o1g}' (when switch S_{x1} is ON) can be calculated by subtracting 'v_{p1g}' and '$V_{PV}/2$'.

Similarly, substituting (5.12) and (5.13) in (5.16) and simplifying for terminal voltage 'v_{o2g}' using (5.9) results in (5.18).

$$v_{o2g} = \frac{e_g + \frac{V_{PV}}{2}\left(S_4 + S_6\right)}{\left(S_2S_3 + S_2S_5 + S_4 + S_6\right)} \tag{5.18}$$

The other terminal voltage 'v_{p2g}' can be calculated by adding 'v_{o2g}' and '$V_{PV}/2$'. Now by using (5.6) and (5.7), the complete expression for terminal voltages 'v_{pg}' and 'v_{og}' is given in (5.19) and (5.20) respectively.

$$v_{pg} = e_g S_{Z1} + V_{PV} S_{Z2} + e_g S_{Z3} + \frac{V_{PV}}{2} S_{Z4} + \frac{V_{PV}}{2} S_2 \tag{5.19}$$

$$v_{og} = e_g S_{Z1} + V_{PV} S_{Z2} + e_g S_{Z3} + \frac{V_{PV}}{2} S_{Z4} - \frac{V_{PV}}{2} S_1 \tag{5.20}$$

The terms S_{Z1}, S_{Z2}, S_{Z3} and S_{Z4} in (5.19) and (5.20) are given by,

$$S_{Z1} = \frac{S_1}{\left(S_1S_3 + S_1S_5 + S_4 + S_6\right)} \quad S_{Z2} = \frac{S_1(S_4 + S_6)}{\left(S_1S_3 + S_1S_5 + S_4 + S_6\right)} \quad S_{Z3} = \frac{S_2}{\left(S_2S_3 + S_2S_5 + S_4 + S_6\right)}$$

$$S_{Z4} = \frac{S_2(S_4 + S_6)}{\left(S_2S_3 + S_2S_5 + S_4 + S_6\right)}$$

Substituting the values S_3=0, S_4=0, S_5=0 and S_6=0 in the voltage state result in undefined value (0/0) in the terminal voltages 'v_{pg}', 'v_{og}' and 'v_{ng}'. The undefined value (0/0) during a zero voltage state is mainly because of isolating the PV source and grid. The isolation of PV source and grid can also be observed in Fig. 5.2 (c). The common-mode voltage 'v_{cm}' is obtained by taking the average of pole voltage 'v_{an}' and 'v_{bn}' given in (5.1) and (5.2) respectively. The expression for the 'v_{cm}' is expressed in (5.21).

$$v_{cm} = \left(\left(S_1 + 0.5S_2\right) \left(S_3 + S_5\right) + \left(\frac{1}{\left(S_3 + S_4\right)} + \frac{1}{\left(S_5 + S_6\right)} \right) \left(\frac{1}{\left(S_1 + S_2\right)} - 1 \right) \right) \frac{V_{PV}}{2} \tag{5.21}$$

Table 5.2 gives the values of pole voltages ('v_{an}', 'v_{bn}') and common-mode voltage 'v_{cm}' at different levels in the output voltage 'v_{ab}'. During the turn-OFF period in a switching cycle, all the switches in the H-bridge are in a cut-off state so that the switching states S_3, S_4, S_5 and S_6 are equal to zero value. Substituting the corresponding values of S_3, S_4, S_5, S_6 in (5.21) results in an undefined value (i.e., 'v_{cm}'= 0/0) during the zero voltage state. The common-mode voltage attains the value '$V_{PV}/2$' for both positive and negative levels of output voltage 'V_{PV}' and attains the value '$V_{PV}/4$' for both positive and negative levels of output voltage '$V_{PV}/2$'.

TABLE 5.2.VALUES OF COMMON-MODE VOLTAGE AND POLE VOLTAGES FOR CORRESPONDING OUTPUT VOLTAGE

v_{ab}	v_{an}	v_{bn}	v_{cm}
$+V_{PV}$	V_{PV}	0	$V_{PV}/2$
$+V_{PV}/2$	$V_{PV}/2$	0	$V_{PV}/4$
0	undefined	undefined	undefined
$-V_{PV}/2$	0	$V_{PV}/2$	$V_{PV}/4$
$-V_{PV}$	0	V_{PV}	$V_{PV}/2$

The expressions for terminal and common-mode voltages can be verified with MATLAB software using Simulink block-set. The parameters 'V_{PV}' =400V, switching frequency of the carrier wave 'f_{sw}' =1kHz, 'v_{ac}'= 220V (RMS) and the grid frequency 'f_g' =50Hz are considered for the simulation. The carrier wave frequency is restricted to 1kHz. This is done to demonstrate the undefined states clearly. Fig. 5.7 shows the waveforms of terminal voltages 'v_{pg}', 'v_{og}', 'v_{ng}' and common-mode voltage 'v_{cm}'. The discontinuity in the waveforms occurs when the PV source and grid are isolated. The isolation of grid and PV array results in an undefined value in the terminal and common-mode voltages (discontinuity in the waveform). Since the value of the terminal and common-mode voltages is undefined during the zero voltage state, they can be assumed to be restricted to the previous value. Thus, transitions in the voltage waveform can be minimized. In other words, it results in minimizing the high-frequency voltage transitions in the terminal and common-mode voltages. Minimization or reduction of high-frequency voltage transitions in the terminal voltage

further helps in reducing the leakage current in the PV system. The PV array parasitic capacitance [20] offers a high impedance for the low-frequency transitions in the terminal voltage. Thus, the magnitude of leakage current flowing through the parasitic capacitance is less. In other words, the proposed PWM technique minimizes the leakage current by reducing the high-frequency transitions in the terminal and common-mode voltages.

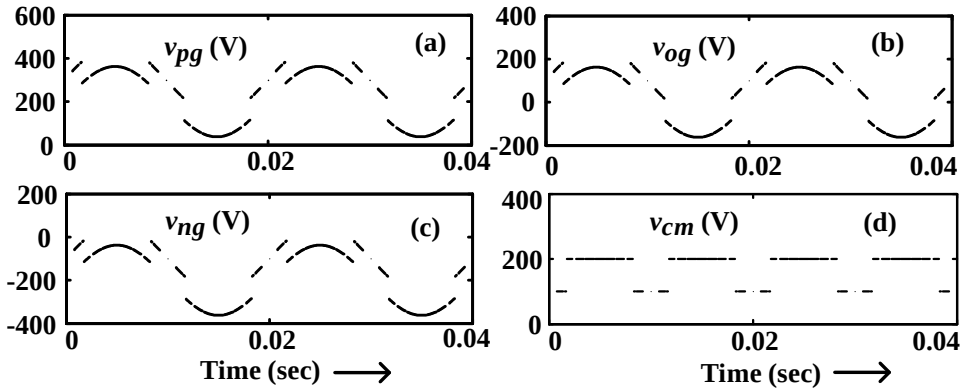


Fig. 5.7. The analytical results of proposed five-level CMLI showing the waveforms of: (a) terminal voltage 'v_{pg}'; (b) terminal voltage 'v_{og}'; (c) terminal voltage 'v_{ng}'; (d) common-mode voltage 'v_{cm}'.

5.5. Simulation results

To support the switching function analysis given in the previous section, the proposed five-level CMLI is simulated using POWERSIM blocks in the MATLAB/SIMULINK software. The PWM technique explained in section 5.2 is used for the proposed five-level CMLI configuration. Table 5.3 gives the value of various parameters used for simulating the proposed five-level CMLI. The proposed five-level CMLI needs to generate a voltage 'V_{inv}' having a phase 'δ_{inv}' [21] to feed the required amount of active power 'P' into the grid.

TABLE 5.3. PARAMETERS CONSIDERED FOR THE SIMULATION OF PROPOSED FIVE-LEVEL CMLI

Parameter	P	V_{DC}	f_{sw}	e_g	f_g
Value	2.5kW	400V	25kHz	230V	50Hz
Parameter	L	R	R_G	L_f	C_f
Value	4mH	0.01Ω	0.1Ω	4mH	0.1 µF
Parameter	R_d	C_p	R_p		
Value	50mΩ	200nF	1Ω		

$$\delta_{inv} = arctan\left(\frac{2\Pi f_g\left(L + L_f\right)P}{e_g^2 + RP}\right) \tag{5.22}$$

$$V_{inv} = \left(e_g + \frac{RP}{e_g}\right)\frac{1}{cos\ \delta_{inv}} \tag{5.23}$$

For a power of 'P' =2.5kW, the value of 'δ_{inv}' = 0.117 rad and 'V_{inv}' = 323 V are calculated by substituting the parameters from Table 5.3 in (5.22) and (5.23) respectively. The simulation waveforms of proposed five-level CMLI using the proposed PWM technique are shown in Fig. 5.8. Fig. 5.8 (a) shows the output voltage of five-level CMLI. The presence of zero voltage state in all the voltage transitions of 'v_{ab}' can be clearly noticed from the plot. The grid current 'i_g' is shown in Fig. 5.8 (b). The grid current is nearly sinusoidal. The Total Harmonic Distortion (THD) of grid current 'i_g' is around 1.76% and meets the requirement of standard IEEE 1547.

The waveform of terminal voltages 'v_{pg}', 'v_{og}' and 'v_{ng}' are shown in subplots (c), (d) and (e) of Fig. 5.8 respectively. The crucial observation made from these subplots is

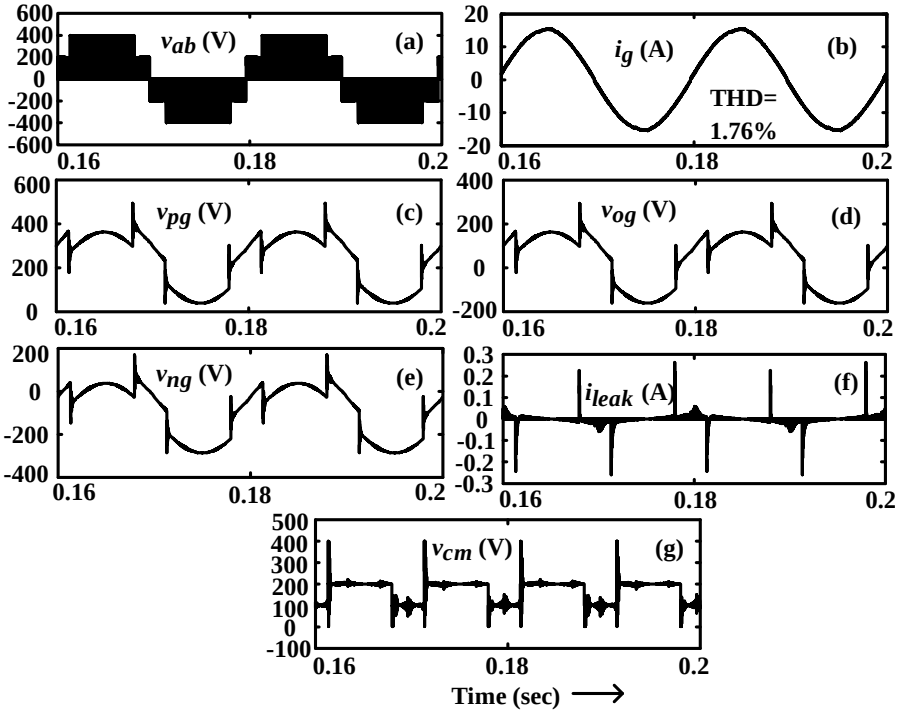


Fig. 5.8. Simulation results of proposed five-level CMLI showing the waveforms of : (a) output voltage 'v_{ab}'; (b) grid current 'i_g'; (c) terminal voltage 'v_{pg}'; (d) terminal voltage 'v_{og}'; (e) terminal voltage 'v_{ng}'; (f) leakage current 'i_{leak}'; (g) common-mode voltage 'v_{cm}'.

the absence of high-frequency voltage transitions. Also, these waveforms match with the result obtained using switching function analysis (Fig. 5.7). This justifies the analysis given in the previous section. Fig. 5.8 (f) shows the waveform for leakage current 'i_{leak}' flowing through the parasitic capacitor. The proposed PWM technique reduces the value of leakage current as can be observed in Fig. 5.8 (f). This is because of the low-frequency voltage transitions in the terminal voltages 'v_{pg}', 'v_{og}' and 'v_{ng}'. The spikes in the leakage current are observed when there is a sudden voltage transition in the terminal voltage. The RMS value of 'i_{leak}' is less than 20mA which is as per the standard VDE0126-1-1[46]. Fig. 5.8 (g) shows the waveform of common-mode voltage 'v_{cm}'. The high-frequency voltage transitions in the common-mode voltage are also avoided. This further brings down the size, weight and cost of the EMI filter to be used in the grid-connected system [47].

Another simulation is carried out with the proposed configuration to demonstrate the MPPT operation. The proposed five-level CMLI is operated using two MPPT algorithms to extract the maximum power from the individual PV arrays. As explained in section IV, the two individual MPPT algorithms are used for the two PV sources 'PV_1' and 'PV_2' which are identical (having same array configuration). Simulation is done considering a resistive load connected to the output of the inverter *via* an 'LC' filter. The PV modules with an open circuit voltage of 21.05V and short circuit current of 3.74A at STC are chosen for the array simulation. The electrolytic capacitors of 5000μF are used as a buffer between the PV sources and inverter as shown in Fig. 5.1. The inverter is connected to a load of 20Ω through an 'LC' filter with the inductor and capacitor values of 4mH and 2μF respectively. The two PV arrays 'PV_1' and 'PV_2' have an open circuit voltage of 126.90V and a short circuit current of 3.8A at an insolation of 1.0 Sun and the temperature of 50^0C.

Fig. 5.9 shows the simulation results of MPPT performance for the proposed five-level CMLI. The subplots (Figs. 5.9 (a) and Fig. 5.9 (b)) show the waveforms of PV voltages 'V_{PV1}' and 'V_{PV2}' for 'PV_1' and 'PV_2' sources respectively. The values of the operating voltages 'V_{PV1}' and 'V_{PV2}' of the two PV arrays are nearly equal. The PV currents 'I_{PV1}' and 'I_{PV2}' are shown in subplots Fig. 5.9 (c) and Fig. 5.9 (d) respectively. The voltage-current (v-i) characteristics of the PV array can be observed with the increasing value of current by decreasing voltage or vice-versa. The power 'P_{PV1}' and 'P_{PV2}' from the PV sources 'PV_1' and 'PV_2' are shown in subplots Fig. 5.9 (e) and Fig. 5.9 (f) respectively. The operation of two PV sources near MPP can be confirmed with the low value of ripple in the PV power and small

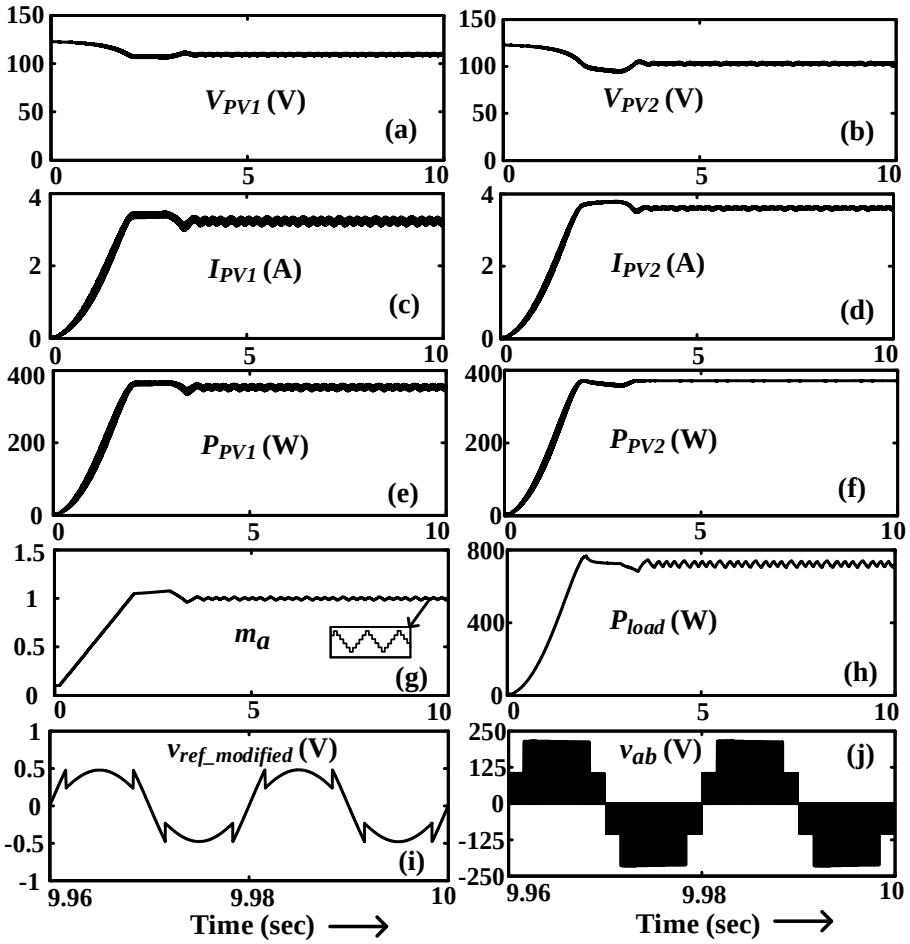


Fig. 5.9. Proposed five-level CMLI integrated with MPPT. The subplots give waveforms of : (a) voltage 'V_{PV1}'; (b) voltage 'V_{PV2}'; (c) current 'I_{PV1}'; (d) current 'I_{PV2}'; (e) power 'P_{PV1}'; (f) power 'P_{PV2}'; (g) resultant modulation index 'm_a'; (h) output power 'P_{OUT}'; (i) modified reference wave '$v_{ref\_modified}$'; (j) inverter output voltage 'v_{ab}'.

oscillations in the modulation index 'm_a', which can be observed in zoomed part of Fig. 5.9 (g). The waveform of output power across resistive load 'P_{load}' is shown in subplot Fig. 5.9 (h). It can be observed that the power across output load is nearly equal to the sum of the individual PV powers 'P_{PV1}' and 'P_{PV2}'. The waveforms of '$v_{ref\_modified}$' and 'v_{ab}' are also shown in subplots Fig. 5.9 (i) and Fig. 5.9 (j). Integration of MPPT for the proposed five-level CMLI makes the inverter suitable for the PV systems.

5.6. Experimental results

To validate the analysis and simulation of PWM technique for the given five-level CMLI, an experimental setup is established. Fig. 5.10 shows the photograph of the fabricated

experimental setup. The details of the parameters used for the experiment are given in Table 5.4. The MOSFET's with part number IRF840 are employed as switches in the power circuit. The driving pulses for the switches are generated using HCPL 3120. The programmable DC power supplies give the input DC voltage 'V_{DC}' to the inverter [48-50] as shown in Fig. 5.10. The output of the inverter is connected to a resistive load 'R_{load}' through an LC filter. The required PWM pulses are generated using DIGILENT ATLYS Spartran-6 FPGA board. The frequency of carrier wave 'f_{sw}' and the modified reference wave 'f_g' are selected as 10kHz and 50Hz respectively. The measurement of leakage current is done by connecting a capacitor 'C_p' in series with resistance 'R_p' at point 'p' of the given five-level inverter as shown in Fig. 5.1.

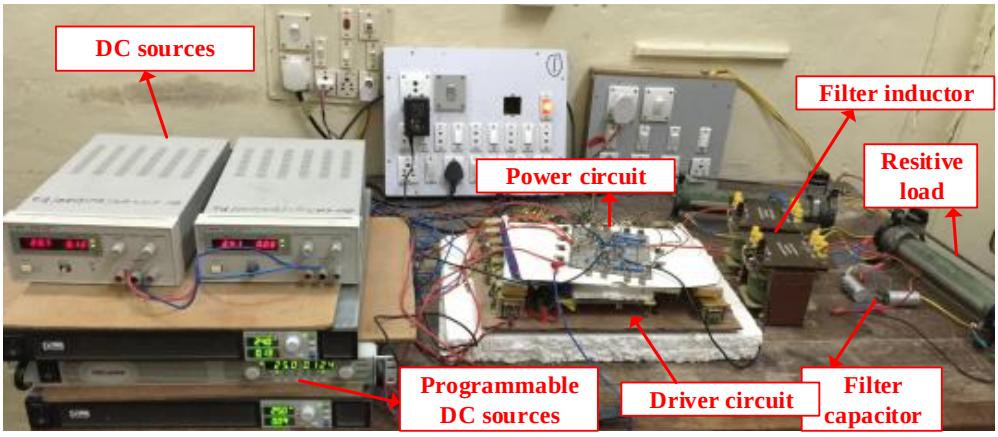


Fig. 5.10. Photograph of the experimental setup containing five-level and nine-level CMLI.

TABLE 5.4. PARAMETERS USED FOR EXPERIMENTAL SETUP

Parameter	P	V_{DC}	f_{sw}	f_g	L
Value	54W	220V	10kHz	50Hz	4mH
Parameter	C	R_{load}	C_p	R_p	
Value	1.25µF	370 Ω	200nF	5Ω	

Fig. 5.11 shows the experimental waveforms of the proposed five-level CMLI. Fig. 5.11 (a) shows the waveform of switching states of switches Sw_1, Sw_3, Sw_4, Sw_5, Sw_6 and Sw_7. The switches (Sw_1, Sw_2) and (Sw_7, Sw_8) are operated at low switching frequency. The remaining switches (Sw_3, Sw_6) and (Sw_4, Sw_5) operate only in positive and negative half cycles of the inverter output voltage 'v_{ab}' respectively. The inverter output voltage 'v_{ab}' is shown in Fig. 5.11 (b). The zero voltage state is present in all the switching's of the inverter output voltage. This may increase the filter inductor value at the output of MLI. However, the minimization of high-frequency transitions in the terminal voltage reduces EMI filter requirement for the proposed system. The waveforms of the voltage across resistive load 'v_{load}' and the current flowing through the resistive load 'i_{load}' are shown in Fig. 5.11 (c). The waveforms of the terminal voltages 'v_{pg}', 'v_{og}' and 'v_{ng}' are shown in Fig. 5.11 (d). It may be noted that the terminal voltage is free from high-frequency transitions, which demonstrates the effectiveness of the proposed PWM technique. Fig. 5.11 (e) shows the leakage current 'i_{leak}' flowing through the C_p-R_p branch. The magnitude of leakage current is less than 100mA and is as per standard VDE0126-1-1.

To demonstrate the upgradability of the proposed topology to any generalized '*2m+1*' level inverter, a hardware prototype for the nine-level CMLI is fabricated. The nine-level configuration of proposed CMLI is obtained by cascading two basic units in generalized configuration with the bi-directional switches as shown in Fig. 5.4. Fig. 5.12 shows the experimental waveforms obtained from the developed hardware prototype of the nine-level inverter connected to a resistive load. The parameters shown in Table 5.4 are again used, except the input DC voltage which is reduced to 100V. Fig. 5.12 (a) shows the waveform of inverter output voltage 'v_{ab}'. The nine levels of the inverter output voltage can be clearly observed in the voltage waveform. The presence of zero voltage state for a complete cycle of the output voltage is also observed from the plot. The waveforms of the voltage across the resistive load 'v_{load}' and the current flowing through resistive load 'i_{load}' are shown in Fig. 5. 12 (b).

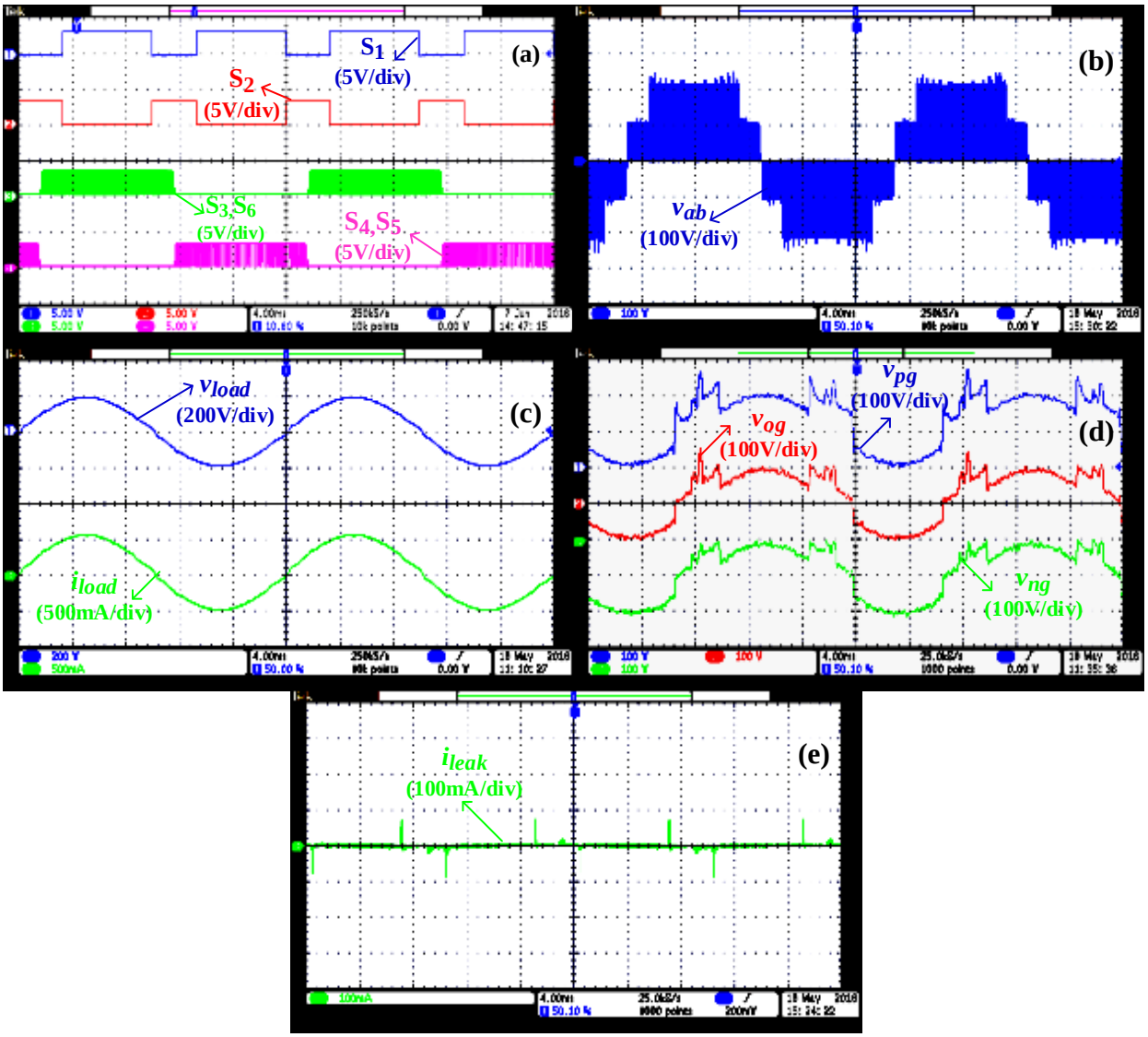


Fig. 5.11. The experimental waveforms of : (a) switching functions of switches Sw_1, Sw_3, Sw_4, Sw_5, Sw_6, Sw_7; (b) output voltage 'v_{ab}'; (c) voltage 'v_{load}' across and current 'i_{load}' flowing through resistive load; (d) terminal voltage waveforms of 'v_{pg}' , 'v_{og}' and 'v_{ng}'; (e) leakage current 'i_{leak}' in the parasitic capacitance for the proposed five-level CMLI.

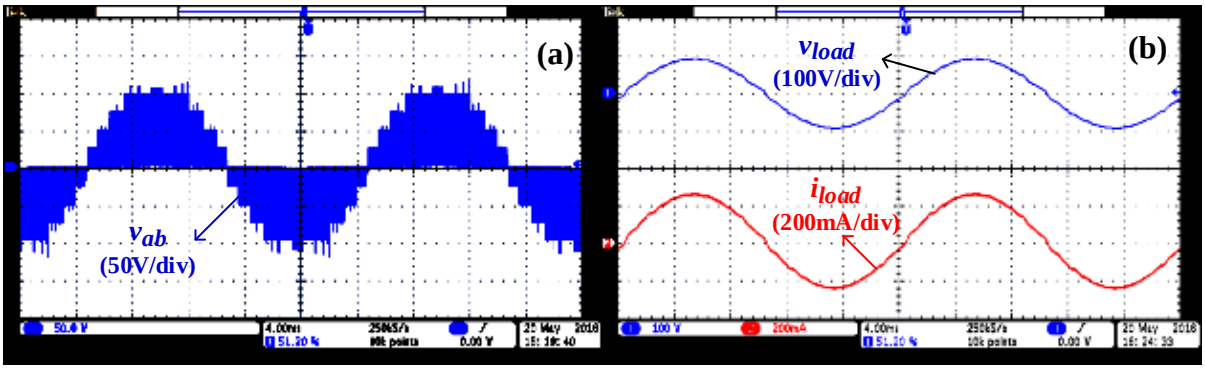


Fig. 5.12. The experimental waveforms of nine-level CMLI: (a) output voltage 'v_{ab}'; (b) voltage 'v_{load}' across and current 'i_{load}' flowing through the resistive load.

5.7. Comparison of proposed CMLI with the existing MLI topologies

The proposed five-level CMLI is compared with the existing PV MLI topologies from the literature available. Table 5.5 gives the comparison details of the proposed five-level CMLI with the existing PV MLI topologies. It can be observed that the other topologies (Table 5.5) require almost the same number of devices for the generation of three levels in the output voltage. The proposed CMLI also requires nearly the same number of semiconductor devices for the generation of five levels in the inverter output voltage. Hence, the proposed five-level CMLI is economical. Furthermore, the proposed five-level CMLI have reduced switching and conduction losses. The other existing topologies shown in Table 5.5 have either high switching loss or conduction loss. The problem of asymmetry in the output voltage of the inverter is also avoided in the proposed CMLI topology. Also, the number of devices conducting during zero voltage state always remains two. Thus, the proposed CMLI is expected to show high efficiency. To support the efficient operation of proposed CMLI, loss calculation (switching and conduction losses) for the controlled switching devices is done under identical conditions. The losses in other MLI topologies are also calculated under the same conditions of output power P=2.5kW, switching frequency 'f_{sw}'=25kHz, 'V_{DC}'=400V and 'm_a'=0.8125. The expressions for switching and conduction losses used for the calculation are obtained from [28-29]. Fig. 5.13 and Fig. 5.14 show the calculated value of conduction and switching losses in the form of bar charts for various MLI topologies reported in the literature. Furthermore, in Figs. 5.13 and 5.14, the terms 'P_c' and 'P_{sw}' refer to the conduction and switching losses respectively, for each of the MLI topologies reported in the literature. Conduction and switching losses of the individual switches in each MLI topology are shown in different color blocks in the bar chart of 'P_c' and 'P_{sw}' respectively. It can be observed that the proposed five-level CMLI shows higher efficiency compared to the other existing topologies. Hence, the proposed five-level CMLI is efficient and economical.

TABLE 5.5. COMPARISON OF PROPOSED CMLI WITH THE EXISTING TOPOLOGIES

S.No	Author name [Ref no], number of levels in output voltage	A	B	C		D		E		F	
				s	d	p	n	p	n	p	n
1	Zhang *et al.* [25], 3-L	Yes	4	8	-	4	2	2	2	2	2
2	Islam *et al* [26], 3-L	No	2	6	-	3	3	3	3	1	1
3	Xiao *et al.* [27], 3-L	No	2	6	4	2	2	4	4	0	0
4	Ji *et al.* [28], 3-L	No	2	6	2	3	3	2	2	1	1
5	Kerekes *et al* [42], 3-L	No	3	5	5	2	2	3	3	0	0
6	Islam *et al* [41], 3-L	Yes	2	7	3	2	3	3	3	1	1
7	Wu *et al* [51], 3-L (HBI MODE)	Yes	4	9	6	6	6	4	4	0	0
8	Wu *et al* [51], 5-L (CHI MODE)	No	4	8	2	6	6	8	8	0	0
9	Proposed 5-LCMLI	No	2	8	-	3	3	2	2	3	3

A- Asymmetry operation during positive and negative cycle of the MLI;

B- Number of devices conducting in zero voltage state including switches and diodes;

C- Number of devices used in the MLI:

s- Number of switches used in the MLI;

d- Number of diodes used in the MLI;

D- Number of devices including switches and diodes conducting:

p- During the positive half-cycle of the grid voltage;

n- During the negative half-cycle of the grid voltage;

E- Number of switches operating at high switching frequency;

F- Number of switches operating at low switching frequency;

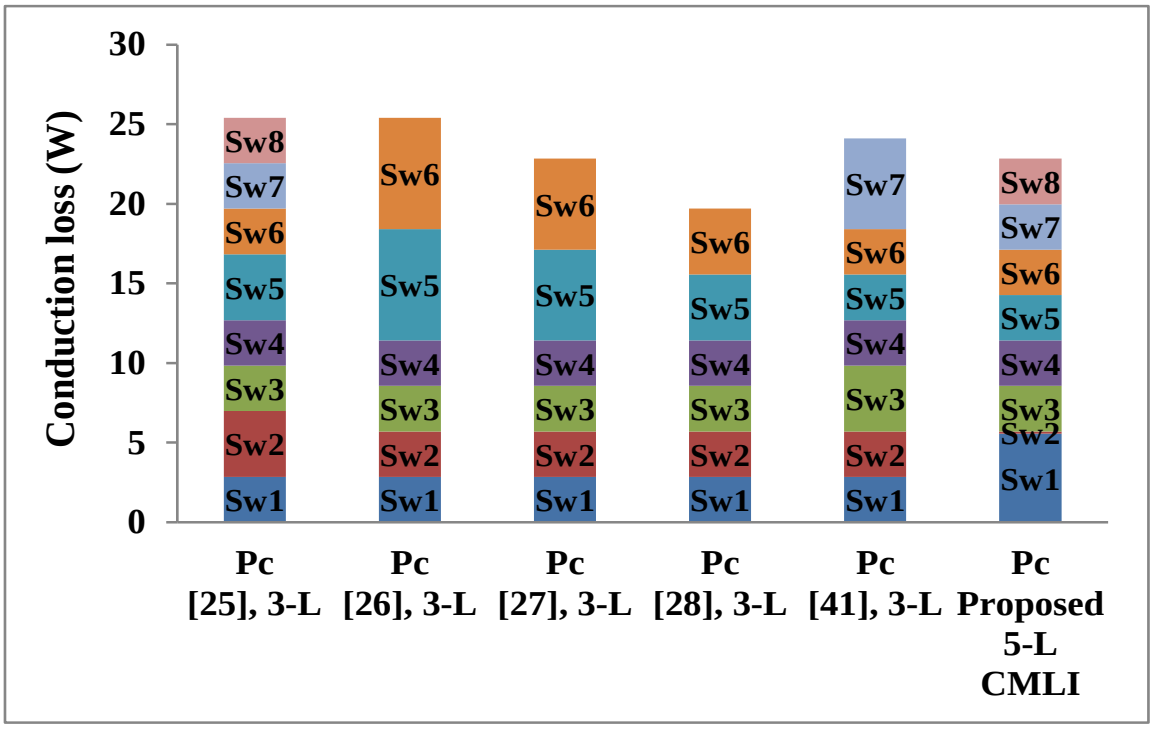


Fig. 5.13. The value of conduction losses 'P_c' of switches used in various MLI topologies given in the literature.

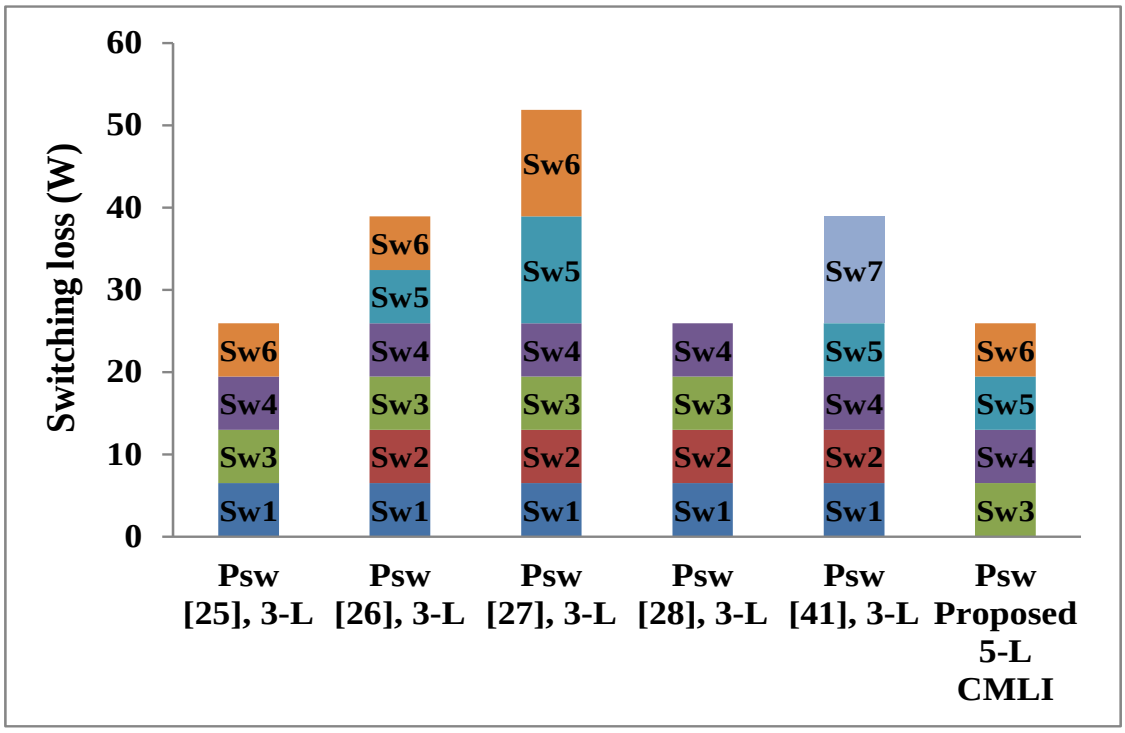


Fig. 5.14. The value of switching loss 'P_{sw}' of switches used in various MLI topologies presented in the literature.

5.8. Conclusion

In this chapter, an improved five-level CMLI with low switch count for the minimization of leakage current in a transformerless PV system is proposed. The proposed CMLI minimizes the leakage current by eliminating the high-frequency transitions in the terminal and common-mode voltages. The proposed topology also has reduced conduction and switching losses which makes it possible to operate the CMLI at high switching frequency. Furthermore, the solution for generalized '*2m+1*' levels CMLI is also presented in the chapter. The given PWM technique requires only one carrier wave for the generation of '*2m+1*' levels. The operation, analysis of terminal and common-mode voltages for the CMLI is also presented in the chapter. The simulation and experimental results validate the analysis carried out in this chapter. The MPPT algorithm is also integrated with the proposed five-level CMLI to extract the maximum power from the PV panels. The proposed CMLI is also compared with the other existing MLI topologies in Table 5.5 to show its advantages.

CHAPTER 6

Comprehensive Review on Analysis of Terminal Voltage in Single Phase Extended Three Phase Transformerless PV Inverter Topologies

Chapter 6

Comprehensive Review on Analysis of Terminal Voltage in Single Phase Extended Three Phase Transformerless PV Inverter Topologies

This chapter presents an insight view for the extension of single-phase to three-phase transformerless PV inverter topologies. Based on the method of isolation between the load and PV array, the transformerless PV inverters are classified into four categories, i.e., DC decoupling, AC decoupling, NPC DC decoupling and NPC AC decoupling. The single-phase PV inverter topology along with its extension to three-phase for each category is reviewed in the chapter. Apart from the three-phase extended topology, the analysis for the terminal voltage using the switching function concept for each PV inverter topology is also presented in the chapter.

6.1. Classification of transformerless PV Inverter topologies

Based on the method of isolation between the PV array and the inverter output load during zero state, the transformerless inverter topologies can be classified as,

6.1.1. DC decoupling

This category typically consists of PV inverter topologies which uses extra circuitry at the inverter DC bus. The extra circuitry is used to isolate the PV array and inverter output load during zero state. The isolation during zero state creates an undefined voltage condition at the PV terminals. The undefined voltage at PV terminals further helps in minimizing voltage transitions or switchings during zero state. This again helps in minimizing leakage current. The most popular H5 inverter topology [52] is one of the single-phase PV inverters, which employ the DC decoupling methodology. The schematic of the H5 inverter connected to a resistive load 'R' via a filter 'L_f' is shown in Fig. 6.1. The load current 'i_{ab}' flows through the resistive load. The PV array 'PV_1' output voltage is given by 'V_{PV}'. The parasitic resistance and capacitance are represented as 'R_P' and 'C_P' respectively. The nodes 'p' and 'n' represent the positive and the negative terminals of the PV array. The node 'g' represents

the ground point of the PV array. The term 'v_{pg}' represents the terminal voltage across the 'R_P'-'C_P' branch. The H5 inverter topology contains an H-bridge formed by switches Sw_{a1}, Sw_{a2}, Sw_{b1} and Sw_{b2} and a decoupling switch Sw_5. The H5 inverter topology generates three levels at the inverter output voltage 'v_{ab}'. During the voltage level 'V_{PV}', the switches Sw_{a1}, Sw_{b2} and Sw_5 are turned ON. Similarly, during the voltage level '$-V_{PV}$', the switches Sw_{a2}, Sw_{b1} and Sw_5 are turned ON. During the zero state, only the switches Sw_{a1} and Sw_{b1} are turned ON. The turn-OFF of switch Sw_5 results in the isolation of the PV array and the load during zero state. The load current 'i_{ab}' freewheels among the switches Sw_{a1} and Sw_{b1} during the zero state. The isolation of the PV array and the load during zero state, results in an undefined value of terminal voltage 'v_{pg}'.

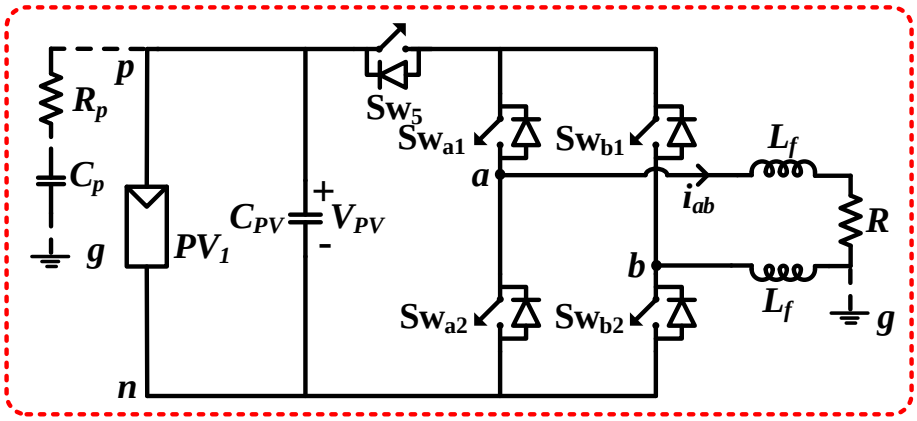


Fig. 6.1. The circuit schematic of H5 inverter topology.

Using the same concept, H7 inverter topology [50] is proposed for the three-phase systems. The schematic of the H7 inverter topology is shown in Fig. 6.2. The H7 inverter topology uses a conventional two-level inverter formed by switches Sw_{a1}, Sw_{a2}, Sw_{b1}, Sw_{b2}, Sw_{c1} and Sw_{c2} and a decoupling switch Sw_7. The operation of H7 inverter topology along with the pulse generation for the individual switches is given in [50]. During the zero state, the switch Sw_7 is turned OFF, and the switches Sw_{a1}, Sw_{b1} and Sw_{c1} are turned ON. This action results in a freewheeling of load current among the top switches of the two-level inverter topology.

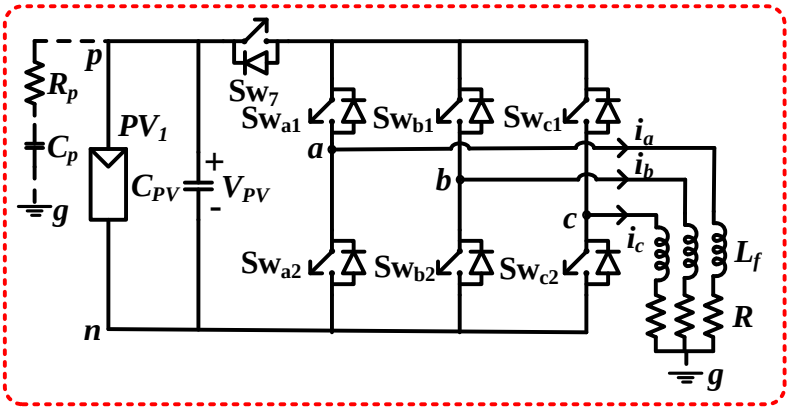


Fig. 6.2. The circuit schematic of H7 inverter topology.

6.1.2. AC decoupling

The AC decoupling based transformerless PV inverter topologies uses extra circuitry like switches and diodes to isolate the PV array and load during the zero state at the output side of the inverter. The transformerless inverter topology discussed in [52] is one example of the PV inverter using AC decoupling. The schematic of the given inverter topology is shown in Fig. 6.3. The circuit consists of an H-bridge inverter formed by switches Sw_{a1}, Sw_{a2}, Sw_{b1} and Sw_{b2} along with a single-phase diode rectifier formed by diodes D_1, D_2, D_3 and D_4 and a decoupling switch Sw_5. The given inverter topology generates three levels in the inverter output voltage. And for the inverter output voltage of 'V_{PV}', the switches Sw_{a1} and Sw_{b2} are turned ON. For the voltage level '$-V_{PV}$', the switches Sw_{a2} and Sw_{b1} are turned ON. During the zero state, all the switches in the inverter topology are turned OFF and the decoupling switch Sw_5 is turned ON. This results in the isolation of the PV array and the load during

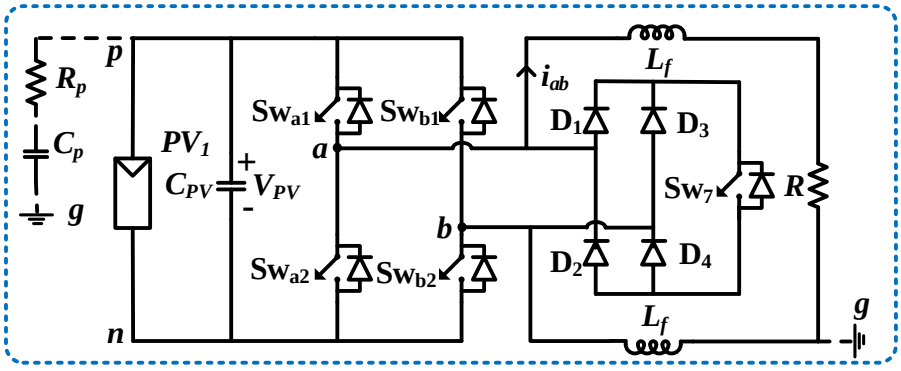


Fig. 6.3. The circuit schematic of single-phase inverter topology using AC decoupling.

zero state which further lead to an undefined value of PV terminal voltage 'v_{pg}'. Thus, during zero state the load current free-wheels through the diode rectifier and the switch Sw_5.

The given single-phase inverter topology can be extended to three-phase inverter topology. The extended three-phase inverter topology consists of seven switches with a three-phase diode rectifier circuit [53] as shown in Fig. 6.4. The seven switch inverter topology consists of a conventional two-level inverter topology formed by the switches Sw_{a1}, Sw_{a2}, Sw_{b1}, Sw_{b2}, Sw_{c1} and Sw_{c2} along with the three-phase diode rectifier formed using six diodes and a decoupling switch Sw_7. During the zero state, all the switches in the two-level inverter are turned OFF. The decoupling switch Sw_7 is turned ON. The load current free-wheels through the diode rectifier and the switch Sw_7.

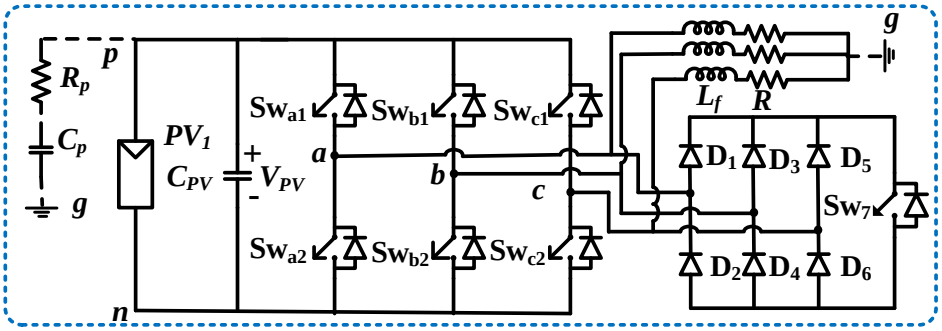


Fig. 6.4. The circuit schematic of three-phase inverter topology using AC decoupling.

6.1.3. NPC DC decoupling

In the case of NPC DC decoupling based transformerless inverter topology, the PV array output voltage is equally shared between the capacitors connected in series at the PV array output. The extra circuitry elements are used clamp the terminal voltage during the zero state to previous active state value. Apart from the isolation during the zero state, the terminal voltage 'v_{pg}' is clamped to its previous value with the help of the diodes and switches.

The single-phase transformerless PV inverter topology [54] shown in Fig. 6.5 employs NPC DC decoupling concept. The inverter topology consists of an H-bridge formed by the switches Sw_{a1}, Sw_{a2}, Sw_{b1} and Sw_{b2}, along with clamping circuitry formed by the switches Sw_5 and Sw_6, diodes D_1 and D_2 as shown in Fig. 6.5. The clamping circuit is further connected to the two capacitors connected in series as shown in Fig. 6.5. The magnitude of

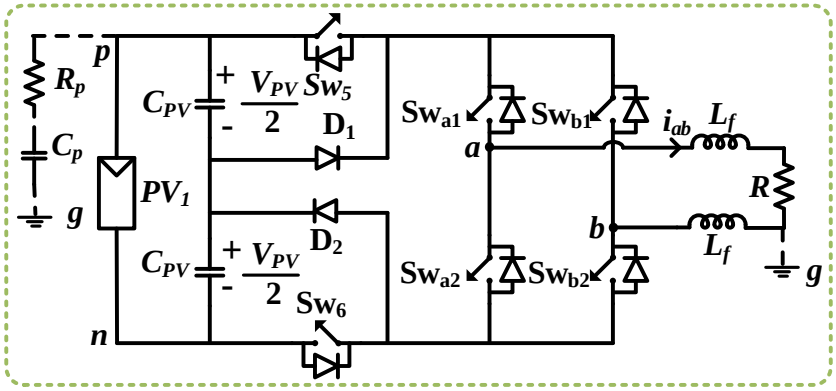


Fig. 6.5. The circuit schematic of single-phase inverter topology using NPC DC decoupling.

the voltage across each capacitor is maintained to the half of PV array voltage. This helps in clamping the terminal voltage to previous value during the zero state. During zero state, the switches Sw_{a1} and Sw_{b1} or Sw_{a2} and Sw_{b2} are turned-ON, so that the load current freewheels among these switches. The decoupling switches Sw_5 and Sw_6 are turned OFF. The diodes D_1 and D_2 clamp the terminal voltage to the previous value so that the transition in terminal voltage is avoided.

The same inverter topology can be extended to three-phase using eight switches [55]. The H8 inverter topology consists of the conventional two-level inverter formed by the switches Sw_{a1}, Sw_{a2}, Sw_{b1}, Sw_{b2}, Sw_{c1} and Sw_{c2}, along with the clamping circuitry formed by the switches Sw_7 and Sw_8, diodes D_1 and D_2 as shown in Fig. 6.6. The clamping circuit is connected to the three series connected capacitors at the output terminals of the PV array as shown in Fig. 6.6. The magnitude of the voltage across each capacitor is equal to the 1/3rd of the PV array voltage. This helps in clamping the terminal voltage to previous value during the

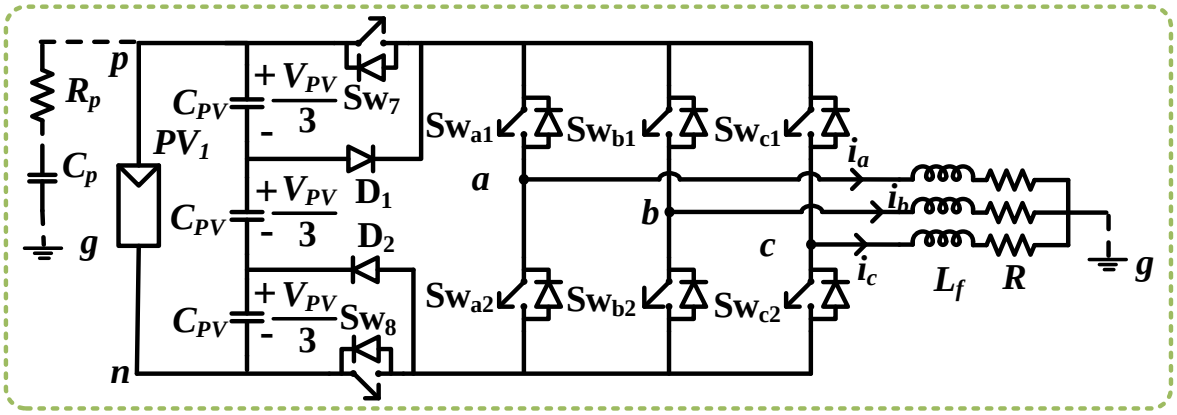


Fig. 6.6. The circuit schematic of three-phase inverter topology using NPC DC decoupling.

zero state. During the zero state, the switches Sw_7 and Sw_8 are turned OFF. For the zero state formed by turning ON the top switches Sw_{a1}, Sw_{b1} and Sw_{c1} (+++), the terminal voltage is clamped to a voltage of 2/3 V_{PV}. Similarly, the other zero state formed by turning ON the bottom switches Sw_{a2}, Sw_{b2} and Sw_{c2} (- - -), the terminal voltage is clamped to a voltage of '1/3 V_{PV}'.

6.1.4. NPC AC decoupling

In the case of NPC AC decoupling based transformerless inverter topologies, the PV array is equally shared among the capacitors like in the case of NPC DC. However, the clamping of terminal voltage to previous active state is done at the load side.

Fig. 6.7 shows the inverter topology employing the NPC AC decoupling [42]. The topology consists of an H-bridge formed by the switches Sw_{a1}, Sw_{a2}, Sw_{b1} and Sw_{b2}, along with the clamping circuitry formed by single-phase diode rectifier (formed by diodes D_1, D_2, D_3 and D_4), switch Sw_5 and diode D_5. The clamping circuit is then connected to capacitors like in the case of NPC DC as shown in Fig. 6.7 so that the terminal voltage is clamped to the previous value during zero state. During zero state, the switches in the H-bridge inverter are turned OFF. The switch Sw_5 is turned-ON, so that the load current free-wheels through the diode rectifier and switch Sw_5. The diode D_5 is used to clamp the terminal voltage to previous value so that the transitions in terminal voltage are avoided.

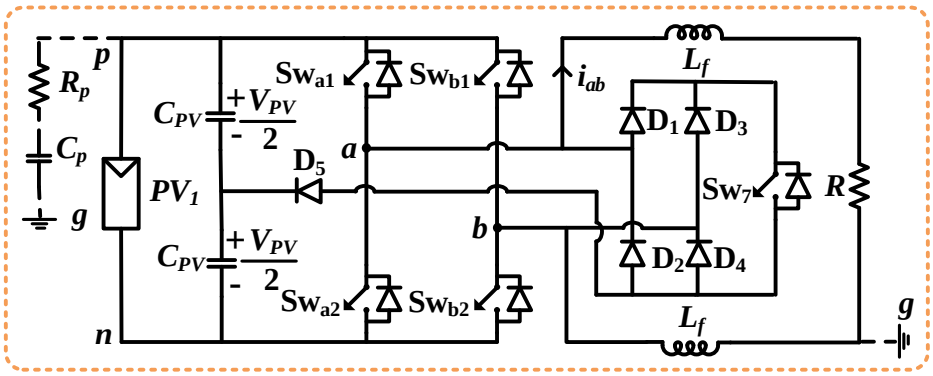


Fig. 6.7. The circuit schematic of single-phase inverter topology using NPC AC decoupling.

The same topology is extended to the three-phase as shown in Fig. 6.8. The extended three-phase topology consists of a conventional two-level inverter topology formed by the switches Sw_{a1}, Sw_{a2}, Sw_{b1}, Sw_{b2}, Sw_{c1} and Sw_{c2} along with the clamping branch formed by

the three-phase diode rectifier (formed by diodes D_1, D_2, D_3, D_4, D_5 and D_6), switches Sw_7, Sw_8 and Sw_9. During the zero state, the switch Sw_7 is turned ON so that the load current free-wheels through the diode rectifier and switch Sw_7. In order to clamp the terminal voltage to level '2/3 V_{PV}', the switch Sw_8 is turned ON. Similarly, in order to clamp the terminal voltage to level '1/3 V_{PV}', the switch Sw_9 is turned ON.

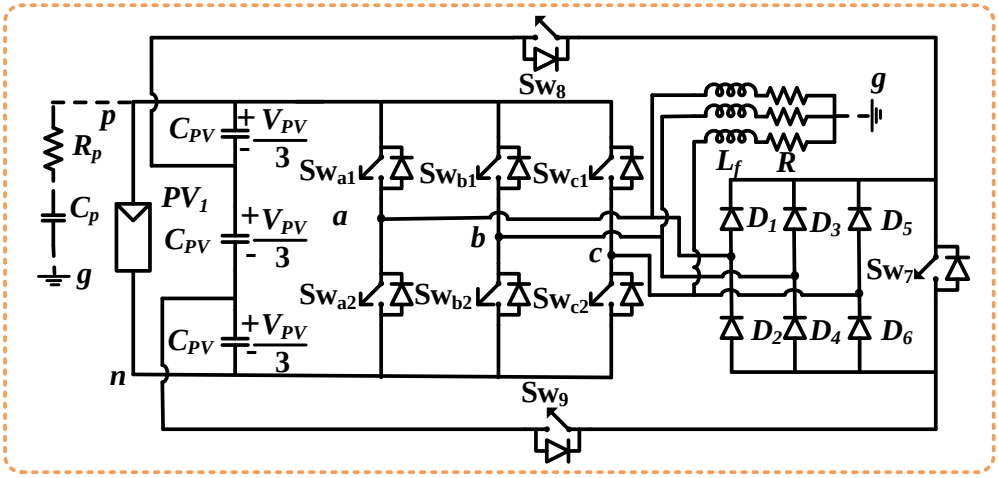


Fig. 6.8. The circuit schematic of three-phase inverter topology using NPC AC decoupling.

6.2. Analysis of terminal voltage in extended three-phase transformerless PV inverter topologies

The expression for the terminal voltage for the extended three-phase transformerless PV inverter topologies for each category is given by

6.2.1. DC decoupling

From Fig. 6.2, the expression for the voltages 'v_{ag}', 'v_{bg}' and 'v_{cg}' are expressed in terms of 'v_{pg}' and 'v_{ng}' as [19]

$$v_{ag} = S_7 S_{a1} v_{pg} + S_{a2} v_{ng} \tag{6.1}$$

$$v_{bg} = S_7 S_{b1} v_{pg} + S_{b2} v_{ng} \tag{6.2}$$

$$v_{cg} = S_7 S_{c1} v_{pg} + S_{c2} v_{ng} \tag{6.3}$$

Also, the voltages 'v_{ag}', 'v_{bg}' and 'v_{cg}' can be expressed as

$$v_{ag} = L_f \frac{di_a}{dt} + Ri_a \tag{6.4}$$

$$v_{bg} = L_f \frac{di_b}{dt} + Ri_b \tag{6.5}$$

$$v_{cg} = L_f \frac{di_c}{dt} + Ri_c \tag{6.6}$$

Adding (6.4), (6.5) and (6.6) results in

$$v_{ag} + v_{bg} + v_{cg} = L_f \frac{d\left(i_a + i_b + i_c\right)}{dt} + R\left(i_a + i_b + i_c\right) \tag{6.7}$$

In case of a balanced three-phase system, the sum of currents 'i_a', 'i_b' and 'i_c' is zero. Therefore (6.7) can be modified as

$$v_{ag} + v_{bg} + v_{cg} = 0 \tag{6.8}$$

Now adding (6.1), (6.2), (6.3) and substituting in (6.8) results in

$$S_7\left(S_{a1} + S_{b1} + S_{c1}\right) v_{pg} + \left(S_{a2} + S_{b2} + S_{c2}\right) v_{ng} = 0 \tag{6.9}$$

The voltage 'v_{ng}' can be represented in terms of 'v_{pg}' and 'V_{PV}' as

$$v_{ng} = v_{pg} - V_{PV} \tag{6.10}$$

Substituting (6.10) in (6.9) and simplifying it results in

$$v_{pg} = \frac{V_{PV}\ \left(S_{a2} + S_{b2} + S_{c2}\right)}{\left(S_7 S_{a1} + S_{a2} + S_7 S_{b1} + S_{b2} + S_7 S_{c1} + S_{c2}\right)} \tag{6.11}$$

The analytical waveforms for the terminal voltage are obtained from (6.11) using MATLAB software. The parameters taken are 'V_{PV}'=200V, switching frequency 'f_{sw}'= 500Hz. The switching is chosen very less to show the transitions clearly. The subplots (a) to (f) of Fig. 6.9 (I) clearly shows the waveforms of the switching states of the switches in the inverter topology. The subplot (h) of Fig. 6.9 (I) shows the waveform of the terminal voltage 'v_{pg}'. There are two levels ('V_{PV} /3' and '$2V_{PV}$ /3') in the waveform of terminal voltage 'v_{pg}'.

The discontinuity in the terminal voltage is observed at zero state. During zero state the value of terminal voltage from (6.11) becomes '∞' or undefined.

6.2.2. AC decoupling

From Fig. 6.4, the expression for the voltages 'v_{ag}', 'v_{bg}' and 'v_{cg}' are expressed in terms of 'v_{pg}' and 'v_{ng}' as

$$v_{ag} = S_{a1} v_{pg} + S_{a2} v_{ng} \tag{6.12}$$

$$v_{bg} = S_{b1} v_{pg} + S_{b2} v_{ng} \tag{6.13}$$

$$v_{cg} = S_{c1} v_{pg} + S_{c2} v_{ng} \tag{6.14}$$

Adding (6.12), (6.13), (6.14) and substituting in (6.8) results in

$$\left(S_{a1}+S_{b1}+S_{c1}\right) v_{pg} + \left(S_{a2}+S_{b2}+S_{c2}\right) v_{ng} = 0 \tag{6.15}$$

Substituting (6.10) in (6.15) and simplifying gives

$$v_{pg} = \frac{V_{PV}\ \left(S_{a2}+S_{b2}+S_{c2}\right)}{\left(S_{a1}+S_{a2}+S_{b1}+S_{b2}+S_{c1}+S_{c2}\right)} \tag{6.16}$$

Fig. 6.9 (II) shows the waveforms of switching states of individual switches and the terminal voltage for the inverter topology obtained from (6.16). The subplots (a) to (g) show the waveforms of the switching states of individual switches. The subplot (h) shows the waveform of terminal voltage 'v_{pg}'. The terminal voltage 'v_{pg}' have same two levels ('V_{PV} /3' and '$2V_{PV}$ /3'). During zero state, the value of the terminal voltage becomes '∞' or undefined.

6.2.3. NPC DC decoupling

From Fig. 6.6, the expression for the voltages 'v_{ag}', 'v_{bg}' and 'v_{cg}' are expressed in terms of 'v_{pg}' and 'v_{ng}' as

$$v_{ag} = S_7 S_{a1} v_{pg} + S_8 S_{a2} v_{ng} + S_{a1}\left(1-S_7\right)\left(v_{pg} - \frac{2V_{PV}}{3}\right) + S_{a2}\left(1-S_8\right)\left(v_{pg} - \frac{V_{PV}}{3}\right) \tag{6.17}$$

$$v_{bg} = S_7 S_{b1} v_{pg} + S_8 S_{b2} v_{ng} + S_{b1}(1-S_7)\left(v_{pg} - \frac{2V_{PV}}{3}\right) + S_{b2}(1-S_8)\left(v_{pg} - \frac{V_{PV}}{3}\right) \quad (6.18)$$

$$v_{cg} = S_7 S_{c1} v_{pg} + S_8 S_{c2} v_{ng} + S_{c1}(1-S_7)\left(v_{pg} - \frac{2V_{PV}}{3}\right) + S_{c2}(1-S_8)\left(v_{pg} - \frac{V_{PV}}{3}\right) \quad (6.19)$$

Adding (6.17), (6.18), (6.19) and substituting in (6.8) results in

$$\begin{aligned} &S_7(S_{a1}+S_{b1}+S_{c1})\, v_{pg} + S_8(S_{a2}+S_{b2}+S_{c2})\, v_{ng} + \\ &\left(v_{pg} - \frac{2V_{PV}}{3}\right)(1-S_7)(S_{a1}+S_{b1}+S_{c1}) + \left(v_{pg} - \frac{V_{PV}}{3}\right)(1-S_8)(S_{a2}+S_{b2}+S_{c2}) = 0 \end{aligned} \quad (6.20)$$

Substituting (6.10) in (6.20) and simplifying it results in

$$v_{pg} = \frac{V_{PV}\left(\frac{2(1-S_7)}{3}(S_{a1}+S_{b1}+S_{c1}) + \frac{(1+2S_8)}{3}(S_{a2}+S_{b2}+S_{c2})\right)}{(S_{a1}+S_{a2}+S_{b1}+S_{b2}+S_{c1}+S_{c2})} \quad (6.21)$$

The waveforms of the switching states of the individual switches and the terminal voltage 'v_{pg}' obtained from (6.21) are shown in Fig. 6.9 (III). The terminal voltage 'v_{pg}' have only two values ('V_{PV} /3' and '$2V_{PV}$ /3'). During zero state, the value of terminal voltage is either clamped to 'V_{PV} /3' and '$2V_{PV}$ /3'.

6.2.4. NPC AC decoupling

From Fig. 6.8, the expression for the voltages 'v_{ag}', 'v_{bg}' and 'v_{cg}' are expressed in terms of 'v_{pg}' and 'v_{ng}' as

$$v_{ag} = S_{a1} v_{pg} + S_{a2} v_{ng} + S_8\left(v_{pg} - \frac{2V_{PV}}{3}\right) + S_9\left(v_{pg} - \frac{V_{PV}}{3}\right) \quad (6.22)$$

$$v_{bg} = S_{b1} v_{pg} + S_{b2} v_{ng} + S_8\left(v_{pg} - \frac{2V_{PV}}{3}\right) + S_9\left(v_{pg} - \frac{V_{PV}}{3}\right) \quad (6.23)$$

$$v_{cg}=S_{c1}v_{pg}+S_{c2}v_{ng}+S_8\left(v_{pg}-\frac{2V_{PV}}{3}\right)+S_9\left(v_{pg}-\frac{V_{PV}}{3}\right) \quad (6.24)$$

Adding (6.22), (6.23), (6.24) and substituting in (6.8) results in

$$\left(S_{a1}+S_{b1}+S_{c1}\right)v_{pg}+\left(S_{a2}+S_{b2}+S_{c2}\right)v_{ng}+3\left(v_{pg}-\frac{2V_{PV}}{3}\right)S_8+3\left(v_{pg}-\frac{V_{PV}}{3}\right)S_9=0 \quad (6.25)$$

Substituting (6.10) in (6.25) and simplifying gives

$$v_{pg}=\frac{V_{PV}\left(S_{a2}+S_{b2}+S_{c2}+2S_8+S_9\right)}{\left(S_{a1}+S_{a2}+S_{b1}+S_{b2}+S_{c1}+S_{c2}+S_8+S_9\right)} \quad (6.26)$$

Fig. 6.9 (IV) shows the waveforms of the switching state of the individual switches and the terminal voltage waveform obtained from (6.26). The waveform of terminal voltage is same as that of the NPC DC decoupling.

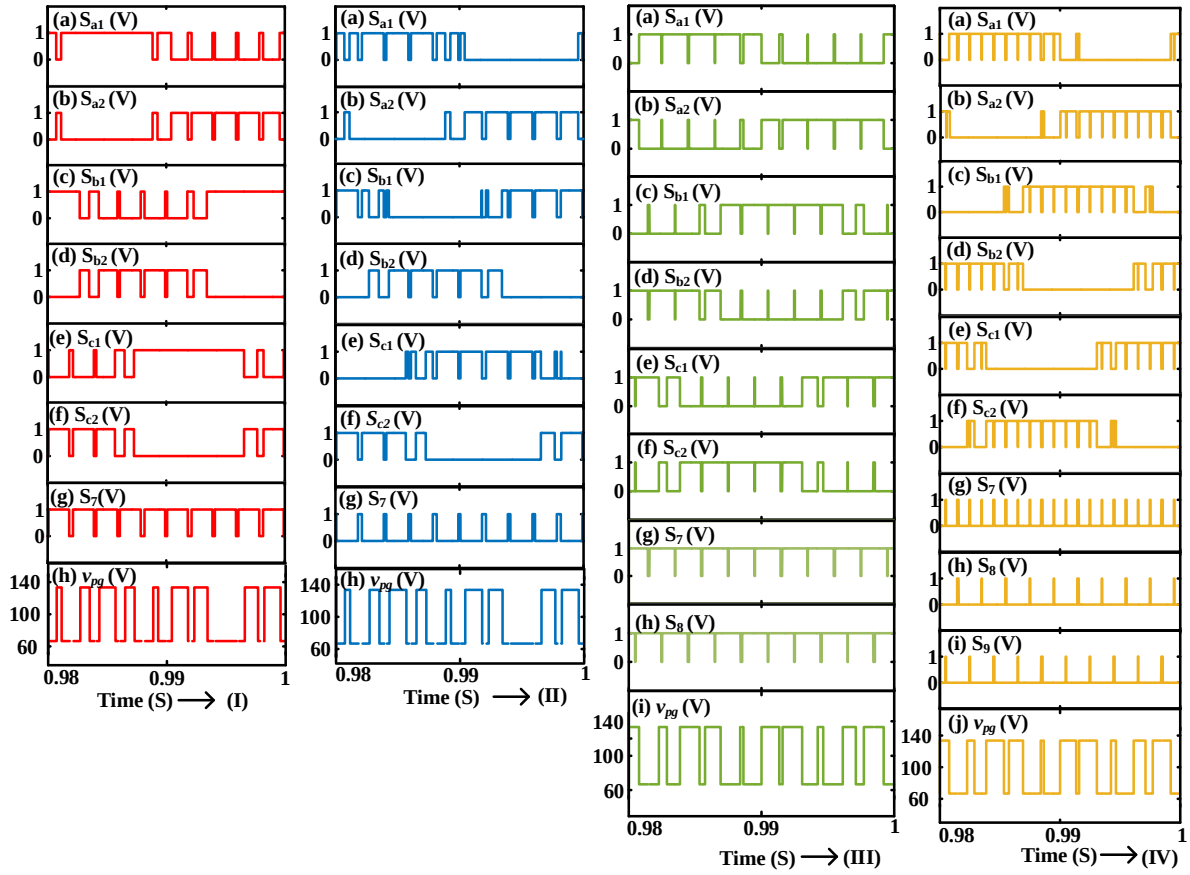


Fig. 6.9. The analytical waveforms of switching states of individual switches and terminal voltage 'v_{pg}' for (I) DC decoupling; (II) AC decoupling; (III) NPC DC decoupling; (IV) NPC AC decoupling.

6.3. Conclusion

The single-phase extended three-phase transformerless topologies for different decoupling methods were presented in the chapter. Thereafter the analysis of the terminal voltage for each inverter topology is presented in the chapter. The analysis given uses the switching function concept. Further, the analytical waveforms of the terminal voltage are obtained using its expressions. All the extended topologies are given only for two-level operation in the output. In the next chapters, the single-phase extended three-phase topologies are further extended for three-level operation.

CHAPTER 7

DC Decoupling Based Three-Phase Three-Level Transformerless PV Inverter Topology for Minimization of Leakage Current

Chapter 7

DC Decoupling Based Three-Phase Three-Level Transformerless PV Inverter Topology for Minimization of Leakage Current

Based on the knowledge obtained from chapter 6, the three-phase two-level topologies are further extended to three-levels in their output voltage. This chapter presents a three-phase three-level cascaded PV inverter configuration using DC decoupling strategy. The given configuration minimizes the leakage current by using two DC decoupling switches. The leakage current is minimized by avoiding or restricting the change in terminal voltage, during common zero state. And to identify or realize the common zero state in all the three phases, the phase opposition disposition PWM technique is utilized. Once, the common zero state is realized, then the DC decoupling switches are used to isolate the PV source and output load. Apart from the terminal voltage, the proposed configuration reduces the change in common mode voltage also. Further, the chapter also presents an analysis of the terminal voltage using the switching function concept. From, the given switching function analysis, the analytical waveforms of the terminal voltage is obtained. The analytical waveforms obtained using the derived expressions match with the simulation results. These results are further supported with the experimental waveforms which match both simulation and analytical waveforms.

7.1. Schematic of proposed DC decoupling based three-phase three-level transformerless CMLI

The circuit schematic of the proposed DC decoupled based three-phase three-level transformerless CMLI is shown in Fig. 7.1. The proposed topology consists of two converters 'Conv-1' and 'Conv-2'. The 'Conv-1' consists of conventional three-phase three-level CMLI [56] configuration formed by switches with three output and input terminals ('*a*', '*b*' and '*c*') and ('*u*', '*v*' and '*w*') respectively. The 'Conv-1' is formed by the switches Sw_{xy} where '*x*' = '*a*', '*b*' and '*c*' and '*y*'*=1, 2... 4*. The output terminals of 'Conv-1' are connected to a star connected three phase load '*R*' through a filter inductor 'L_f'. The terms 'i_a', 'i_b' and 'i_c' refer

to a load current of the corresponding three phases '*a*', '*b*' and '*c*' respectively. The term '*g*' refers to the ground point of the load. Further, the 'Conv-1' is connected to 'Conv-2' via a three terminals '*u*', '*v*' and '*w*' as indicated in Fig. 7.1. The 'Conv-2' consists of two DC decoupling switches Sw_{DC1} and Sw_{DC2}. The two switches Sw_{DC1} and Sw_{DC2} are used to isolate the PV array and the load during the common zero state. The 'Conv-2' is connected to the input PV arrays 'PV_1' and 'PV_2' via the terminals '*p*', '*o*' and '*n*' respectively. The terms 'C_{PV1}' and 'C_{PV2}' refer to the buffer capacitors connected across PV panels 'PV_1' and 'PV_2'. The parasitic resistance 'R_p' and capacitance 'C_p' are connected at node '*p*' (shown in dotted lines). The leakage current flowing through the parasitic resistance and capacitance is denoted by 'i_{leak}'.

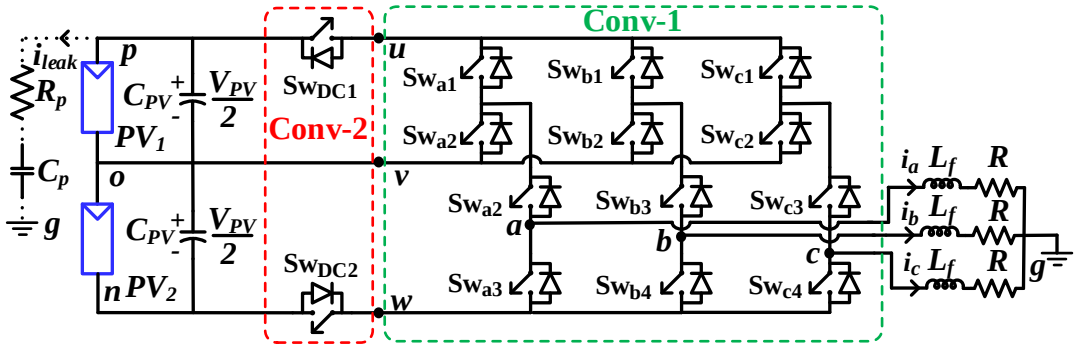


Fig.7.1. Circuit schematic of proposed DC decoupled three-phase three-level CMLI.

7.2. Working principle for the minimization of leakage current

The proposed three-phase configuration uses DC decoupling strategy [50] for the minimization of leakage current. Thus, there is a requirement of common zero state in all the three phases. Once common zero state in all three phases is achieved, then DC decoupling switches are used to isolate PV source and output load. To achieve the objective of common zero state in all the three phases, a level shifted phase opposition disposition (LS-POD) pulse width modulation (PWM) technique [57] is used as shown in Fig. 7.2 (a). Fig. 7.2 (b), (c), (d) and (e) shows the waveforms of the inverter output line voltages 'v_{ab}', 'v_{bc}', 'v_{ca}' along with the terminal voltage 'v_{pg}' for the proposed topology. The common zero state in the inverter line voltages can easily be seen in Fig. 7.2. Thus, using the DC decoupling technique during the common zero state with the help of switches Sw_{DC1} and Sw_{DC2} results in the undefined or infinite state in the terminal voltage 'v_{pg}'. This can be easily identified in Fig. 7.2.

Fig. 7.2 (e) shows the waveforms of the terminal voltage for one complete fundamental cycle of the output voltage (0^0 to 360^0). The terminal voltage is divided into two regions (Region 1 and Region 2) as shown in Fig. 7.2 (e). The Region 1 consists of the period between 0^0 to 60^0, 120^0 to 180^0 and 240^0 to 300^0 for one cycle of the output voltage. Similarly, the Region 2 consists of periods between 60^0 to 120^0, 180^0 to 240^0 and 300^0 to 360^0 of the output voltage. Now, during the common zero state in the Region 1, the load current free-wheels through the switches (Sw_{a1}, Sw_{a3}, Sw_{b1}, Sw_{b3}, Sw_{c1} and Sw_{c3}) of the CMLI, while keeping the switches Sw_{DC1} and Sw_{DC2} turned OFF as shown in Fig. 7.3 (a). Similarly, during the common zero state in the Region 2, the load current free-wheels

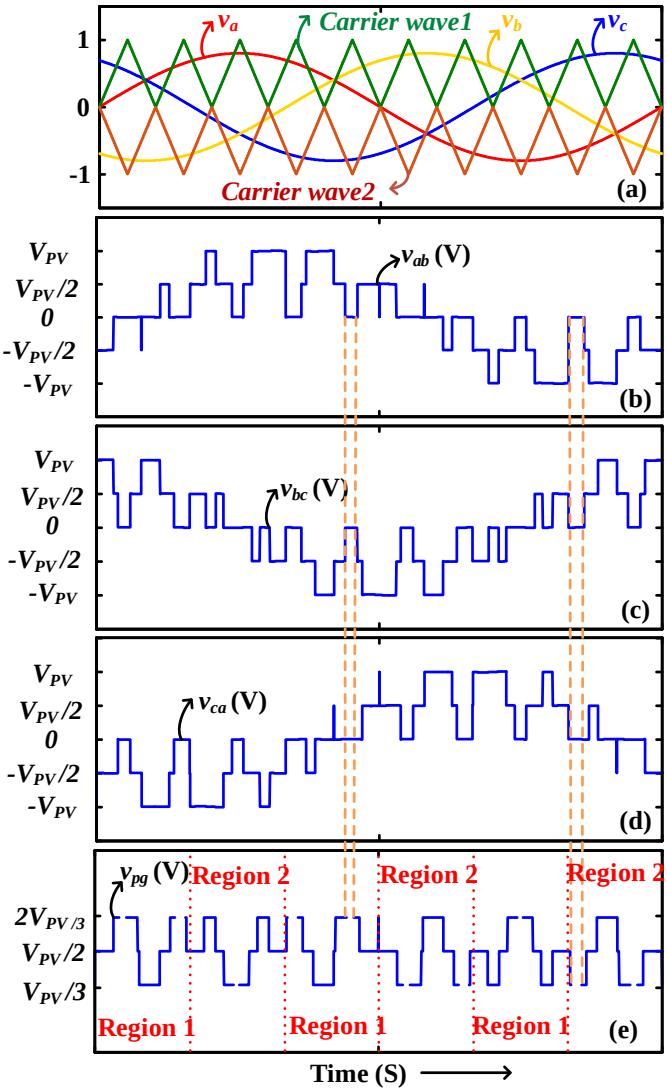


Fig. 7.2. The waveforms of the (a) carrier and reference waves; (b) output voltages 'v_{ab}'; (c) 'v_{bc}'; (d) 'v_{ca}'; (e) terminal voltage 'v_{pg}' for the proposed CMLI.

through the bottom switches (Sw_{a4}, Sw_{b4} and Sw_{c4}) of the CMLI while keeping the switches Sw_{DC1} and Sw_{DC2} turned OFF as shown in Fig. 7.3 (b). The isolation during common zero state results in an undefined value in the terminal voltage. This action results in minimizing the number of transitions in the terminal voltage for one switching cycle. As a result, the magnitude of the leakage current flowing through the parasitic capacitance is minimized. In the voltage levels other than common zero state, both the decoupling switches Sw_{DC1} and Sw_{DC2} remain turned ON.

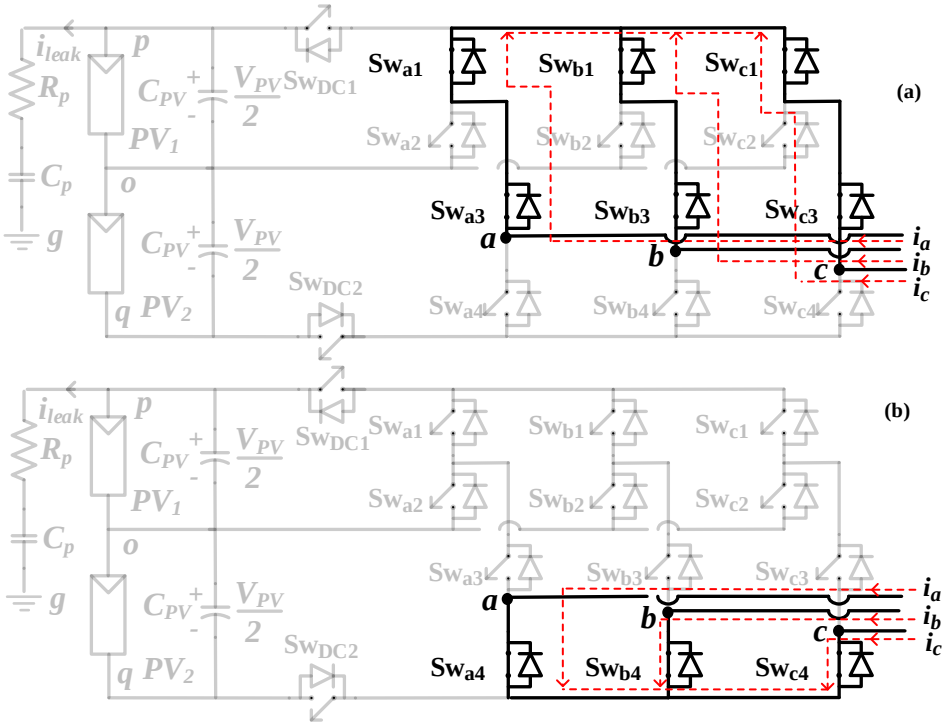


Fig. 7.3. Operation of the proposed CMLI during zero state in (a) Region 1; (b) Region 2.

7.3. Analysis of terminal voltage across the PV parasitic capacitance using the switching function concept

The magnitude of the leakage current flowing through the parasitic capacitance mainly depends on the nature of the terminal voltage. So, it is necessary to obtain the expression for the terminal voltage. The expression is derived using the switching function concept [19, 58].

From Fig.7.1, the voltages 'v_{ag}', 'v_{bg}' and 'v_{cg}' are expressed in terms of 'v_{pg}', 'v_{og}' and 'v_{ng}' as

$$v_{ag} = S_{DC1}S_{a1}S_{a3}v_{pg} + S_{a2}S_{a3}v_{og} + S_{DC2}S_{a4}v_{ng} \tag{7.1}$$

$$v_{bg} = S_{DC1}S_{b1}S_{b3}v_{pg} + S_{b2}S_{b3}v_{og} + S_{DC2}S_{b4}v_{ng} \quad (7.2)$$

$$v_{cg} = S_{DC1}S_{c1}S_{c3}v_{pg} + S_{c2}S_{c3}v_{og} + S_{DC2}S_{c4}v_{ng} \quad (7.3)$$

where Sw_{DC1} and Sw_{DC2} represent the switching states of the decoupling switches Sw_{DC1} and Sw_{DC2}. The term S_{xy} represents the switching states of switch Sw_{xy}, where '*x*'= '*a*', '*b*' and '*c*', '*y*'= *1, 2, 3* and *4*. The value of S_{sxy} = '*1*' is when switch Sw_{xy} is turned ON, else will be '*0*'. The same is applicable for the switching states Sw_{DC1} and Sw_{DC2} also. The terminal voltages 'v_{og}' and 'v_{ng}' are expressed in terms as 'v_{pg}' and 'V_{PV}' as

$$v_{og} = v_{pg} - \frac{V_{PV}}{2} \quad (7.4)$$

The same is applicable for

$$v_{ng} = v_{pg} - V_{PV} \quad (7.5)$$

In the case of balanced three-phase systems,

$$v_{ag} + v_{bg} + v_{cg} = 0 \quad (7.6)$$

Now, adding (7.1), (7.2) and (7.3) and simplifying the expression by using (7.4), (7.5) and (7.6) results in (7.7)

$$v_{pg} = \frac{V_{PV}\left(2S_{DC2}\left(S_{a4}+S_{b4}+S_{c4}\right)+S_{a2}S_{a3}+S_{b2}S_{b3}+S_{c2}S_{c3}\right)}{2S_{den}} \quad (7.7)$$

Where $S_{den} = S_{a3}\left(S_{DC1}S_{a1}+S_{a2}\right)+S_{b3}\left(S_{DC1}S_{b1}+S_{b2}\right)+S_{c3}\left(S_{DC1}S_{c1}+S_{c2}\right)+S_{DC2}\left(S_{a4}+S_{b4}+S_{c4}\right)$

In order to obtain the analytical waveforms of the terminal voltage 'v_{pg}', the expression (7.7) is simulated in the MATLAB software. The parameters considered for the simulation are 'V_{PV}'=200V, switching frequency 'f_{sw}'=500Hz and the reference wave frequency 'f_g' = 50Hz. The switching frequency is kept low (500Hz) in order to clearly indicate the transition in the terminal voltage 'v_{pg}'. Fig. 7.4 shows the analytical waveform of 'v_{pg}' for the proposed CMLI. A discontinuity in the terminal voltage waveform can be observed in Fig. 7.4, which result in avoiding the transitions in the terminal voltage. The discontinuity in terminal voltage is mainly because of the isolation of the PV array and load

during common zero state. The reduced transitions in the terminal voltage, further help in minimizing the magnitude of leakage current in the proposed CMLI.

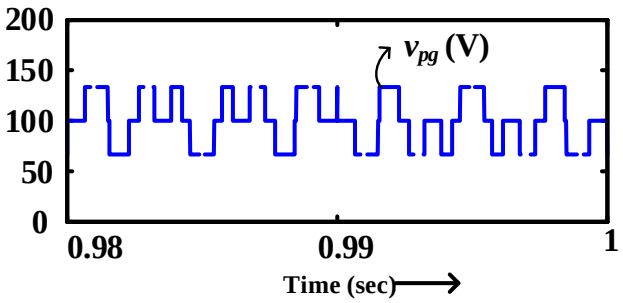


Fig. 7.4. Analytical waveform of the terminal voltage 'v_{pg}' obtained using the switching functions.

7.4. Simulation and experimental results

To justify the operation of the proposed DC decoupled three-phase three-level CMLI and its given analysis, the simulation and experimental results are presented. The simulation is performed in the MATLAB SIMULINK software using the POWERSIM block sets. The parameters considered for the simulation and experiment setups are shown in TABLE 7.1. The MOSFETS IRF 640 are used in the developed hardware prototype. The driver IC HCPL 3120 is used for driving these MOSFETS. The pulses for the switches are generated using the SPARTAN 6 FPGA board. The DPO 3034 is used to capture the waveforms of hardware prototype. And the programmable DC sources were used to produce DC input in the power circuit.

TABLE 7.1. SIMULATION AND EXPERIMENTAL PARAMETERS

Simulation Parameters						
Parameter	V_{DC}	f_{sw}	L	R_p	C_p	R_{load}
Value	200V	10kHz	2mH	1 Ω	10nF	100Ω
Experimental Parameters						
Parameter	V_{DC}	f_{sw}	L	R_p	C_p	R_{load}
Value	100V	10kHz	2mH	1 Ω	10nF	100Ω

Fig. 7.5 shows the (a) simulation waveforms and (b) experimental waveforms of the (i) three-phase three-level CMLI or conventional CMLI [56] and (ii) proposed CMLI. The

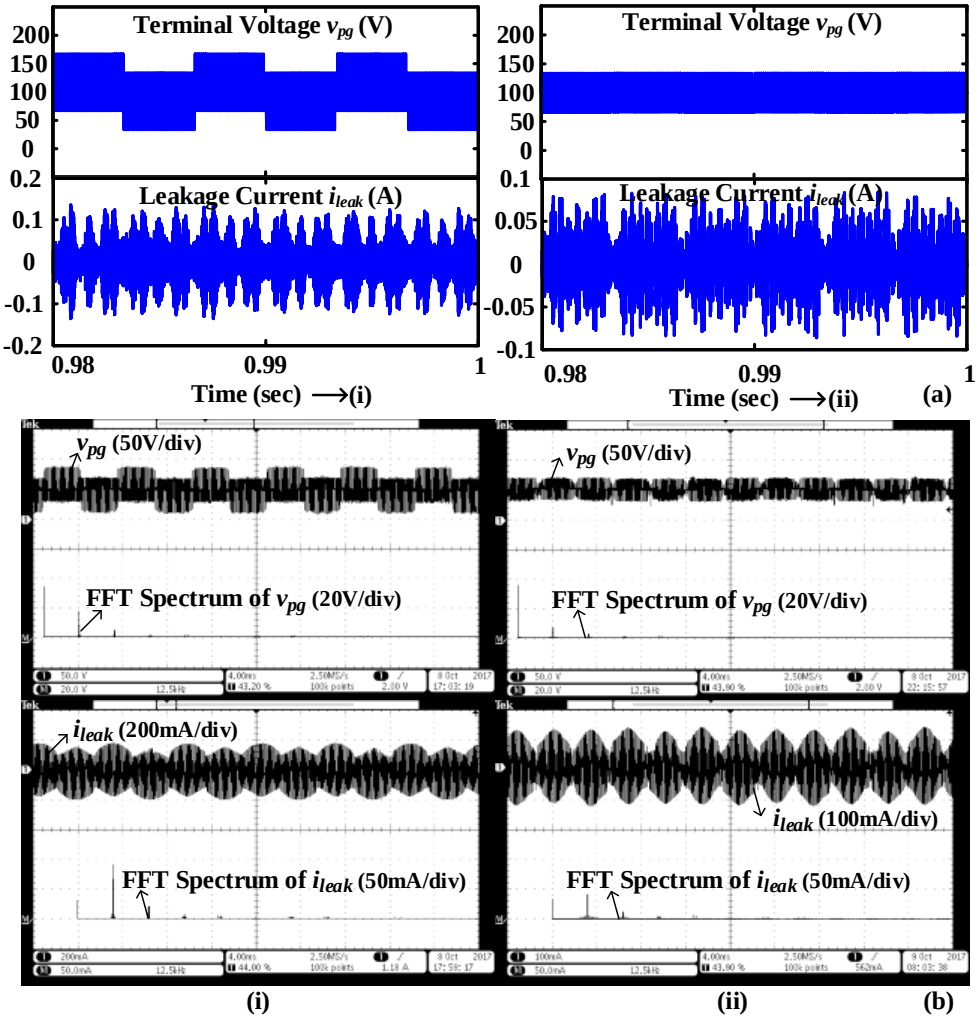


Fig. 7.5. The (a) simulation; (b) experimental waveforms of the terminal voltage and the leakage current for the (i) conventional and (ii) proposed CMLIs.

subplot (a) of Fig. 7.5 show the waveform of terminal voltage 'v_{pg}' for both the cases. It can be observed that the number of transitions in the terminal voltage 'v_{pg}' are less with the proposed CMLI when compared with the conventional CMLI. Because of these reduced transitions in the terminal voltage 'v_{pg}', the magnitude of the leakage current flowing through the parasitic capacitance is less in the proposed CMLI compared to the conventional CMLI. This can be observed from Fig. 7.5.

Fig. 7.6 shows the expanded view of Fig. 7.5 to justify the operation of the convention CMLI and proposed CMLI in Region 1 and Region 2. In the case of conventional CMLI, there are four levels in the terminal voltage in Region 1 and Region 2 as seen in subplots (a) and (b) of Fig. 7.6 (i). So, the number of transitions in the terminal voltage is six for one switching cycle. By using the proposed CMLI, the transition in the common zero state is

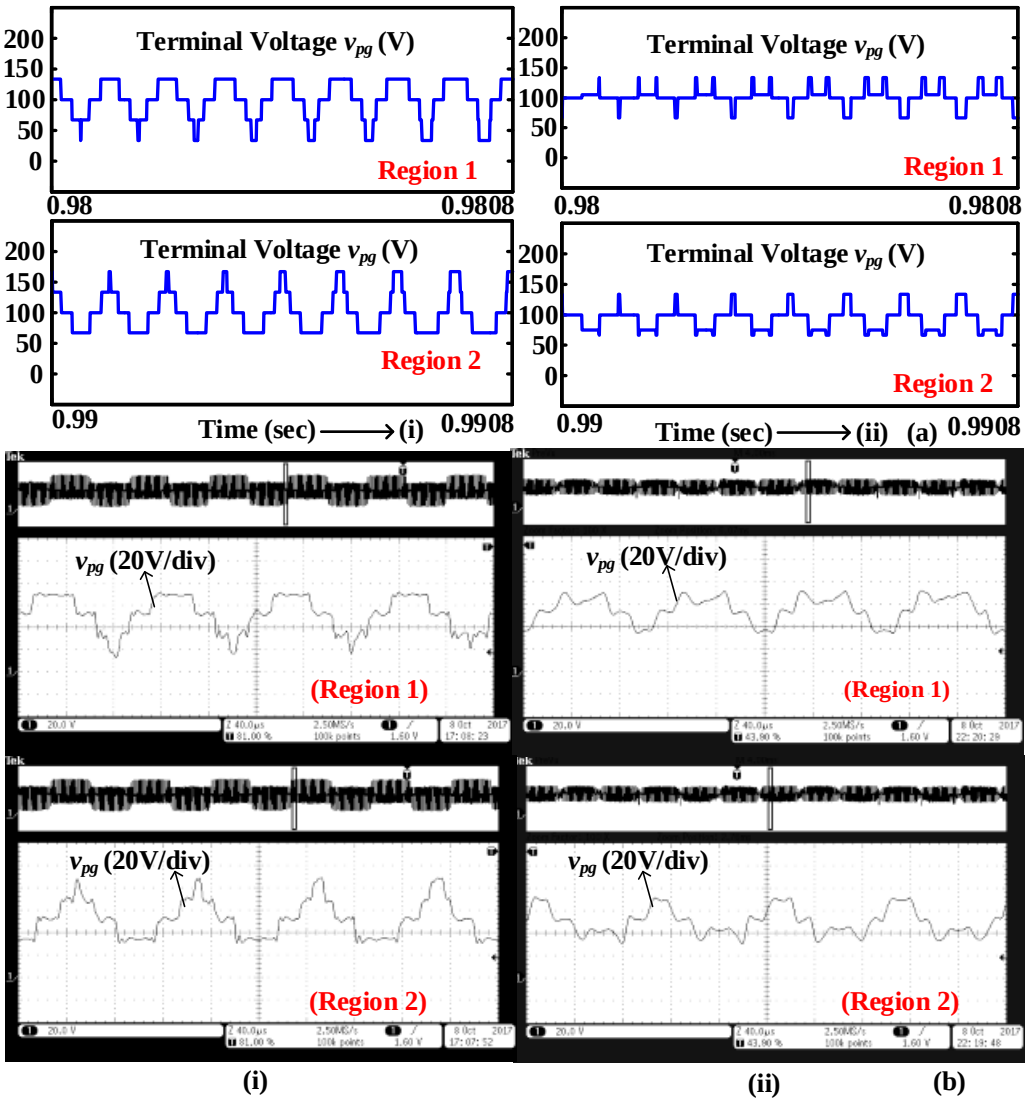


Fig. 7.6. The (a) simulation; (b) experimental waveforms of the terminal voltage v_{pg} in the Region 1 and Region 2 for (i) conventional and (ii) proposed CMLIs.

avoided in Region 1 and Region 2 as observed in the subplots (a) and (b) of Fig. 7.6(ii). However, a small transition is observed in the terminal voltage during the common zero state which is almost negligible. Further, the number of transitions in the terminal voltage in one switching cycle is reduced to four using proposed CMLI when compared to six in the case of conventional CMLI as can be seen in Fig. 7.6. Therefore, using the proposed CMLI with the given PWM technique, the size of common mode filter used at the input and output of the CMLI may be reduced.

The experimental waveforms of output voltages 'v_{ab}', 'v_{bc}' and 'v_{ca}' and the currents 'i_a', 'i_b' and 'i_c' flowing through the resistive load for the (i) conventional and (ii) proposed

CMLIs are shown in the Fig.7. It can be observed that the transitions in output voltages are observed from '*0*' to 'V_{PV}/2', 'V_{PV}/2' to 'V_{PV}' and vice versa using the conventional CMLI. But using the proposed CMLI, the transitions in the output voltages are done from '*0*' to 'V_{PV}/2', '*0*' to 'V_{PV}' and vice versa. Further, it can be clearly observed that the THD of the output current is nearly same for both conventional and proposed CMLIs [58].

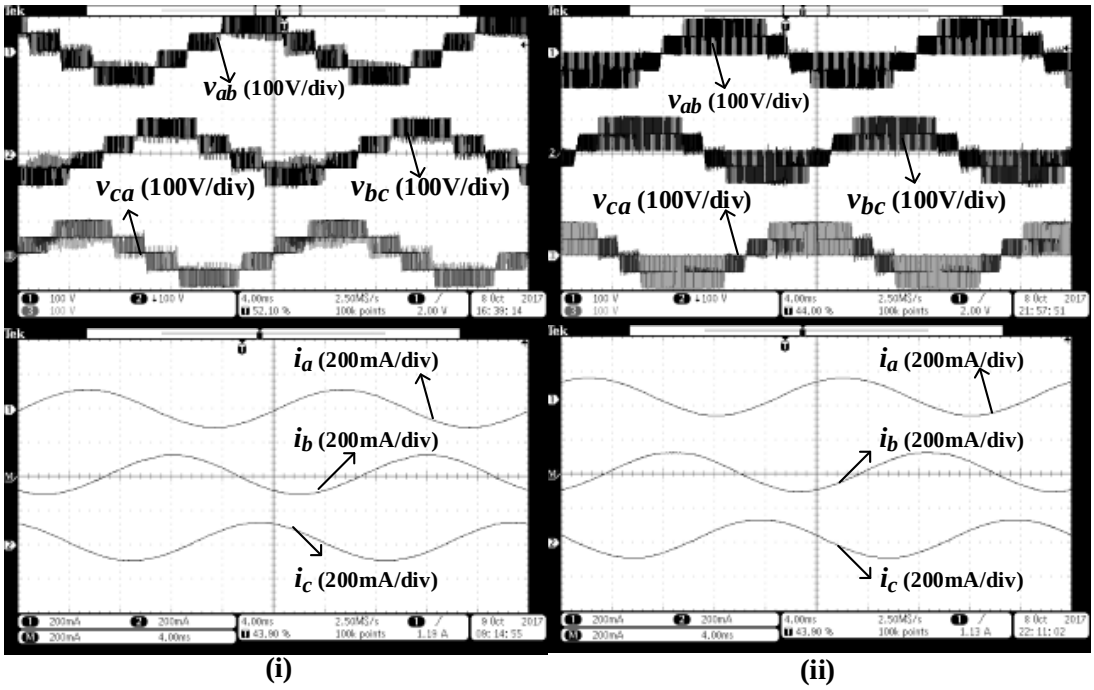


Fig. 7.7 The waveforms of output voltages 'v_{ab}', 'v_{bc}' and 'v_{ca}' and the currents 'i_a', 'i_b' and 'i_c' flowing through the resistive load for the (i) conventional; (ii) proposed CMLIs.

7.5. Conclusion

This chapter presents a three-phase three-level transformerless PV inverter topology for the minimization of the leakage current. The topology is built by cascading the three-phase three-level conventional CMLI with the DC decoupling switches. The proposed topology with the given PWM technique minimizes the leakage current by reducing the transitions in the terminal voltage. This further helps in reducing the transitions common mode voltage which may further reduce the size of EMI filter required both at the inverter input and the output. Apart from this, the proposed CMLI uses the common DC bus for all three phases.

CHAPTER 8

NPC DC Decoupling Based Three-Phase Three-Level Transformerless PV Inverter Topology for Minimization of Leakage Current

Chapter 8

NPC DC Decoupling Based Three-Phase Three-Level Transformerless PV Inverter Topology for Minimization of Leakage Current

This chapter presents a three-phase three-level cascaded PV inverter configuration based on NPC DC decoupling methodology [55]. The given configuration minimizes the leakage current by using decoupling switches, clamping switches and capacitors. The leakage current is minimized by avoiding or restricting the change in terminal voltage, during common zero state. Further, the common zero state in all the three phases is obtained using phase opposition disposition PWM technique. Once, the common zero state is realized, then the magnitude of terminal voltage is restricted to the previous active state value using the proper clamping switches and the capacitors. Further, the chapter also presents an analysis of the terminal voltage using the switching function concept. From, the given switching function analysis, the analytical waveform of the terminal voltages are obtained. The obtained analytical waveforms using the derived expressions match with the simulation results. The obtained results are further supported with the experimental waveforms which match both simulation and analytical waveforms.

8.1. Schematic of proposed NPC DC decoupling based three-phase three-level transformerless CMLI

The schematic of the proposed NPC DC decoupled three-phase three-level CMLI is shown in Fig. 8.1. The proposed CMLI consists of two converters 'Conv-1' and 'Conv-2' as shown in Fig. 8.1. The 'Conv-1' is a three-phase three-level CMLI [56] formed by the twelve switches Sw_{xy} where '*x*' = '*a*', '*b*' and '*c*' and '*y*'*=1, 2... 4*.. The three-phase output terminals ('*a*', '*b*' and '*c*') of 'Conv-1' are connected to the star connected three-phase resistive load '*R*' via a filter inductor 'L_f'. The terms 'i_a', 'i_b' and 'i_c' refer to the output currents flowing through star connected the resistive load. The neutral point of star connected resistive load is connected to ground '*g*'. Further, the input terminals of the 'Conv-1' is connected to the

'Conv-2' via the terminals '*u*', '*v*' and '*w*'. The 'Conv-2'is a neutral point clamped decoupling circuitry formed by the two decoupling switches Sw_{DC1}, Sw_{DC2} and two clamping switches Sw_{D1} and Sw_{D2} along with six capacitors of equal value 'C_{PV}' and sharing equal voltage of '$V_{PV}/6$'. The input to the 'Conv-2' is connected to two PV panels 'PV_1' and 'PV_2' via the terminals '*p*', '*o*' and '*n*'. The terms 'R_p' and 'C_p' connected at node '*p*' refer to the parasitic resistance and the capacitance of the PV panel. The voltage 'v_{pg}' is the terminal voltage across the parasitic resistance and capacitance of the PV panel. The term 'i_{leak}' refers to the leakage current flowing through the parasitic capacitance of the PV panel.

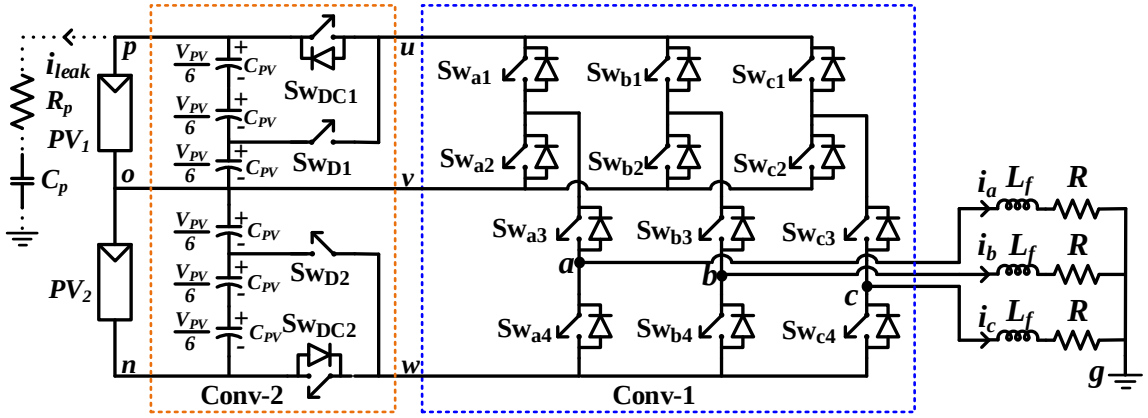


Fig.8.1. Circuit schematic of proposed NPC DC decoupled three-phase three-level CMLI.

8.2. Working principle for the minimization of leakage current

The proposed topology with the given PWM strategy minimizes the leakage current. This is achieved by clamping the terminal voltage during common zero state to its previous active state value and thus, eliminates the transition in the terminal voltage using the clamping circuit in 'Conv-2'. To achieve the objective of the common zero state in all the three phases, a level shifted phase opposition disposition (LS-POD) PWM technique [57] is employed as shown in Fig. 8.2 (a). Fig. 8.2 (b), (c), (d) and (e) shows the waveforms of the inverter output line voltages 'v_{ab}', 'v_{bc}', 'v_{ca}' along with the terminal voltage 'v_{pg}' for the proposed topology. The common zero state in the inverter line voltages can easily be seen in Fig. 8.2. Thus, using the NPC DC decoupling technique during the common zero state with the help of switches Sw_{DC1}, Sw_{DC2}, Sw_{D1} and Sw_{D2} the terminal voltage 'v_{pg}' is clamped to its previous active state values '$2V_{PV}/3$' in Region 1and '$V_{PV}/3$' in Region 2 as observed in Fig. 8.2. Fig. 8.2 (e) shows the waveform of the terminal voltage for one complete fundamental cycle of the output voltage (0^0 to 360^0). The terminal voltage is divided into two regions (Region 1 and Region 2) as shown in Fig. 8.2 (e). The Region 1 consists of the period between 0^0 to 60^0, 120^0 to 180^0

and 240^0 to 300^0 for one cycle of the output voltage. Similarly, the Region 2 consists of periods between 60^0 to 120^0, 180^0 to 240^0 and 300^0 to 360^0 of the output voltage. Now, during the common zero state in the Region 1, the load current free-wheels through the switches (Sw_{a1}, Sw_{a3}, Sw_{b1}, Sw_{b3}, Sw_{c1} and Sw_{c3}) of the CMLI, while keeping the switches

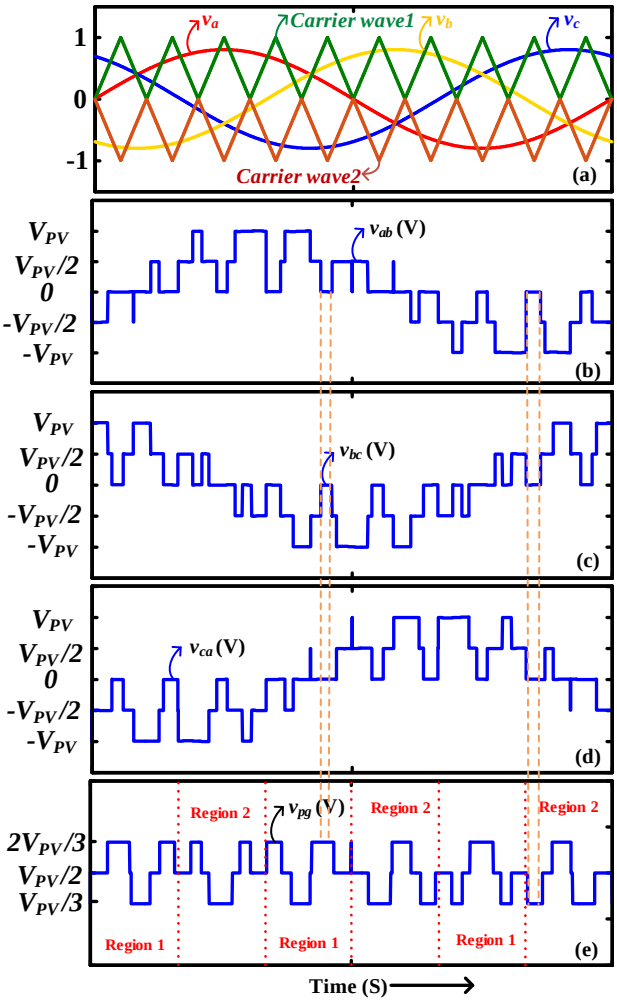


Fig. 8.2. The waveforms of the (a) carrier and reference waves; (b) output voltages v_{ab}; (c) v_{bc}; (d) v_{ca}; (e) terminal voltage v_{pg} for the proposed NPC DC decoupled CMLI.

Sw_{DC1} and Sw_{DC2} are turned OFF and the switches Sw_{D1} and Sw_{D2} are turned ON as shown in Fig. 8.3 (a). Thus, the magnitude of terminal voltage is clamped to '$2V_{PV}/3$', which is same as the previous active state value. Similarly, during the common zero state in the Region 2, the load current free-wheels through the bottom switches (Sw_{a4}, Sw_{b4} and Sw_{c4}) of the CMLI while keeping the switches Sw_{DC1} and Sw_{DC2} turned OFF and the switches Sw_{D1} and Sw_{D2} turned ON as shown in Fig. 8.3 (b). As a result, the magnitude of terminal voltage is clamped to '$V_{PV}/3$', which is same as the previous active state value. In this way, the magnitude of

terminal voltage during common zero state is clamped to its previous active state value in both Region 1 and Region 2. This action results in minimizing the number of transitions in the terminal voltage for one switching cycle. As a result, the magnitude of the leakage current flowing through the parasitic capacitance is minimized. In the voltage levels other than common zero state, both the decoupling switches Sw_{DC1} and Sw_{DC2} remain turned ON and the clamping switches Sw_{D1} and Sw_{D2} remain turned OFF.

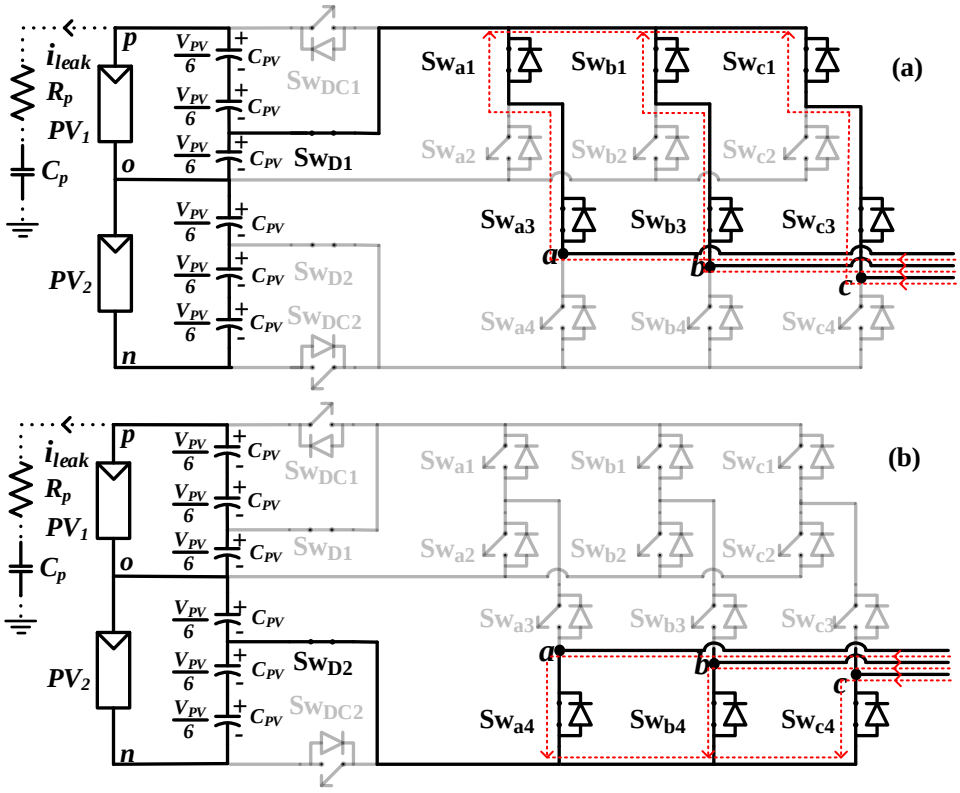


Fig. 8.3 Operation of the proposed NPC DC decoupled CMLI during zero state in (a) Region 1; (b) Region 2.

8.3. Analysis of terminal voltage across PV parasitic capacitance using switching function concept

The magnitude of the leakage current flowing through the parasitic capacitance mainly depends on the nature of the terminal voltage. So it is necessary to obtain the expression for the terminal voltage. The expression is derived using switching function concept [19, 58-59]. From Fig. 8.1, the voltages 'v_{ag}', 'v_{bg}' and 'v_{cg}' are expressed in terms of 'v_{pg}', 'v_{og}' and 'v_{ng}' as

$$v_{ag} = S_{DC1}S_{a1}S_{a3}v_{pg} + S_{a2}S_{a3}v_{og} + S_{DC2}S_{a4}v_{ng} + S_{a1}S_{a3}S_{D1}\left(v_{pg} - \frac{V_{PV}}{3}\right) + S_{a4}S_{D2}\left(v_{pg} - \frac{2V_{PV}}{3}\right)$$

(8.1)

$$v_{bg} = S_{DC1}S_{b1}S_{b3}v_{pg} + S_{b2}S_{b3}v_{og} + S_{DC2}S_{b4}v_{ng} + S_{b1}S_{b3}S_{D1}\left(v_{pg} - \frac{V_{PV}}{3}\right) + S_{b4}S_{D2}\left(v_{pg} - \frac{2V_{PV}}{3}\right)$$

(8.2)

$$v_{cg} = S_{DC1}S_{c1}S_{c3}v_{pg} + S_{c2}S_{c3}v_{og} + S_{DC2}S_{c4}v_{ng} + S_{c1}S_{c3}S_{D1}\left(v_{pg} - \frac{V_{PV}}{3}\right) + S_{c4}S_{D2}\left(v_{pg} - \frac{2V_{PV}}{3}\right)$$

(8.3)

Where S_{D1}, S_{D2}, S_{DC1} and S_{DC2} represent the switching states of the switches $Sw_{D1,}$ Sw_{D2}, Sw_{DC1} and Sw_{DC2}. Similarly, the term S_{xy} represents the switching state of the switch Sw_{xy}. The value of Sw_{xy} is '*1*' whenever the corresponding switch is turned ON else it is '*0*'. The same is applicable for the switching states $Sw_{D1,}$ Sw_{D2}, Sw_{DC1} and Sw_{DC2}.

The terminal voltages 'v_{og}' and 'v_{ng}' are expressed in terms as 'v_{pg}' and V_{PV} as

$$v_{og} = v_{pg} - \frac{V_{PV}}{2} \tag{8.4}$$

$$v_{ng} = v_{pg} - V_{PV} \tag{8.5}$$

In the case of balanced three-phase systems,

$$v_{ag} + v_{bg} + v_{cg} = 0 \tag{8.6}$$

Now, adding (8.1), (8.2) and (8.3) and simplifying the expression by using (8.4), (8.5) and (8.6) results in

$$v_{pg} = V_{PV}S_{DC2}S_{z1} + \frac{V_{PV}}{2}S_{z2} + \frac{V_{PV}}{3}S_{D1}S_{z3} + \frac{2V_{PV}}{3}S_{D2}S_{z1} \tag{8.7}$$

Where S_{z1}, S_{z2} and S_{z3} are given by

$$S_{z1} = \frac{S_{a4} + S_{b4} + S_{c4}}{S_{den}};\ S_{z2} = \frac{S_{a2}S_{a3} + S_{b2}S_{b3} + S_{c2}S_{c3}}{S_{den}};\ S_{z3} = \frac{S_{a1} + S_{b1} + S_{c1}}{S_{den}}$$

$$S_{den}=S_{a3}\left(S_{DC1}S_{a1}+S_{a2}\right)+S_{b3}\left(S_{DC1}S_{b1}+S_{b2}\right)+S_{c3}\left(S_{DC1}S_{c1}+S_{c2}\right)+$$
$$S_{DC2}\left(S_{a4}+S_{b4}+S_{c4}\right)+S_{D1}\left(S_{a1}+S_{b1}+S_{c1}\right)+S_{D2}\left(S_{a4}+S_{b4}+S_{c4}\right)$$

In order to obtain the analytical waveforms of the terminal voltage 'v_{pg}', the expression (8.7), are simulated in the MATLAB Software. The parameters considered for the simulation are 'V_{PV}' =200V, switching frequency 'f_{sw}' =1kHz and the reference wave frequency 'f_g' = 50Hz. Fig. 8.4 shows the analytical waveform of 'v_{pg}' for the proposed CMLI. It can be observed that using the proposed CMLI, the number of transitions in the terminal voltage for one switching cycle is four as seen in Fig. 8.4. The transition in the terminal voltage is avoided by clamping the terminal voltage to the previous value in the common zero state [55].

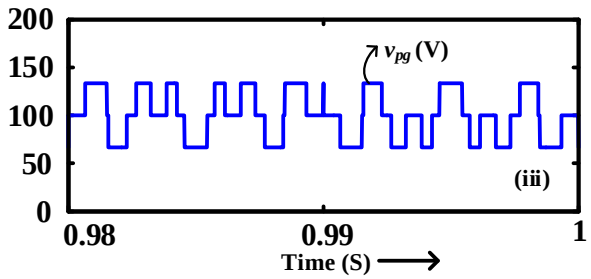


Fig. 8.4. Analytical waveform of the terminal voltage 'v_{pg}' obtained using the switching functions for proposed NPC DC decoupled CMLI.

8.4. Simulation and experimental results

In order to justify the operation of the proposed CMLI and the presented analysis, both the simulation and experimental results are presented. The parameters used in the simulation and experiment are listed in Table 8.1. The simulation is done in MATLAB software using the POWERSIM block sets. The photograph of the experimental prototype developed is shown in Fig. 8.5. The programmable DC sources were used instead of the PV panels to provide input DC voltage for the proposed CMLI. The MOSFETs IRF640 and IGBT IXXH30N60B3 were as power semiconductor switches. The driver IC HCPL 3120 is used to drive the power semiconductor switches. The input PWM pulses for these driver ICs are generated using the Digilent ATLYS SPARTAN 6 FPGA board.

TABLE 8.1. SIMULATION AND EXPERIMENTAL PARAMETERS

Simulation Parameters						
Parameter	V_{DC}	f_{sw}	L	R_p	C_p	R_{load}
Value	200V	10kHz	2mH	1 Ω	10nF	100Ω
Experimental Parameters						
Parameter	V_{DC}	f_{sw}	L	R_p	C_p	R_{load}
Value	100V	10kHz	2mH	1 Ω	10nF	100Ω

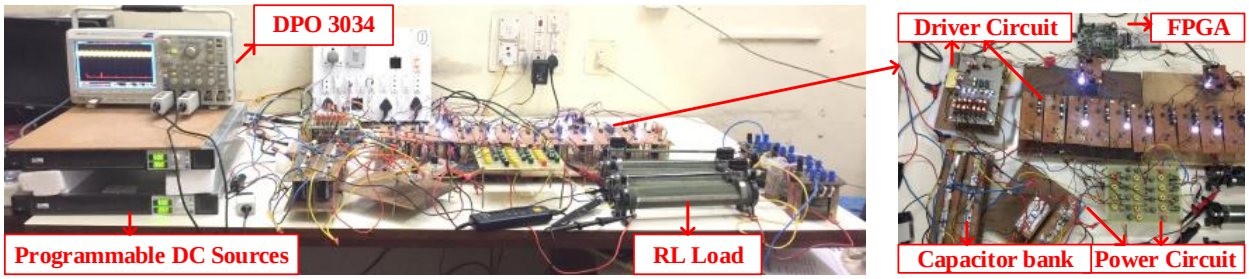


Fig.8.5. Photograph showing experimental setup for proposed NPC DC decoupled three-phase three-level CMLI.

The (a) simulation and (b) experimental waveforms of the (i) conventional three-phase three-level CMLI [56] and (ii) proposed CMLI are shown in Fig. 8.6. It can be observed that using the proposed CMLI, the transitions in the terminal voltage 'v_{pg}' can be minimized compared to the conventional CMLI. This minimizes the high-frequency switching transitions in the terminal voltage. Since the parasitic capacitance offers a high impedance to this low-frequency switching transitions [60], the magnitude of leakage current flowing through the parasitic capacitance is less in the proposed CMLI compared to the conventional three-phase three-level CMLI which can be clearly observed from Fig. 8.6.

In order to clearly show the reduced transitions in the terminal voltage 'v_{pg}' for the proposed CMLI compared to the three-phase three-level CMLI, the zoomed view of the terminal voltage v_{pg} in both the regions Region 1 and Region 2 are shown in Fig. 8.7. It can be seen that for one switching cycle 'f_{sw}' in both regions Region 1 and Region 2, the number of switching transitions in the terminal voltage is 6 in the case of conventional CMLI. Whereas using the proposed CMLI, the switching transitions in the terminal voltage is reduced to 4. This clearly justifies the reduction in the magnitude of leakage current.

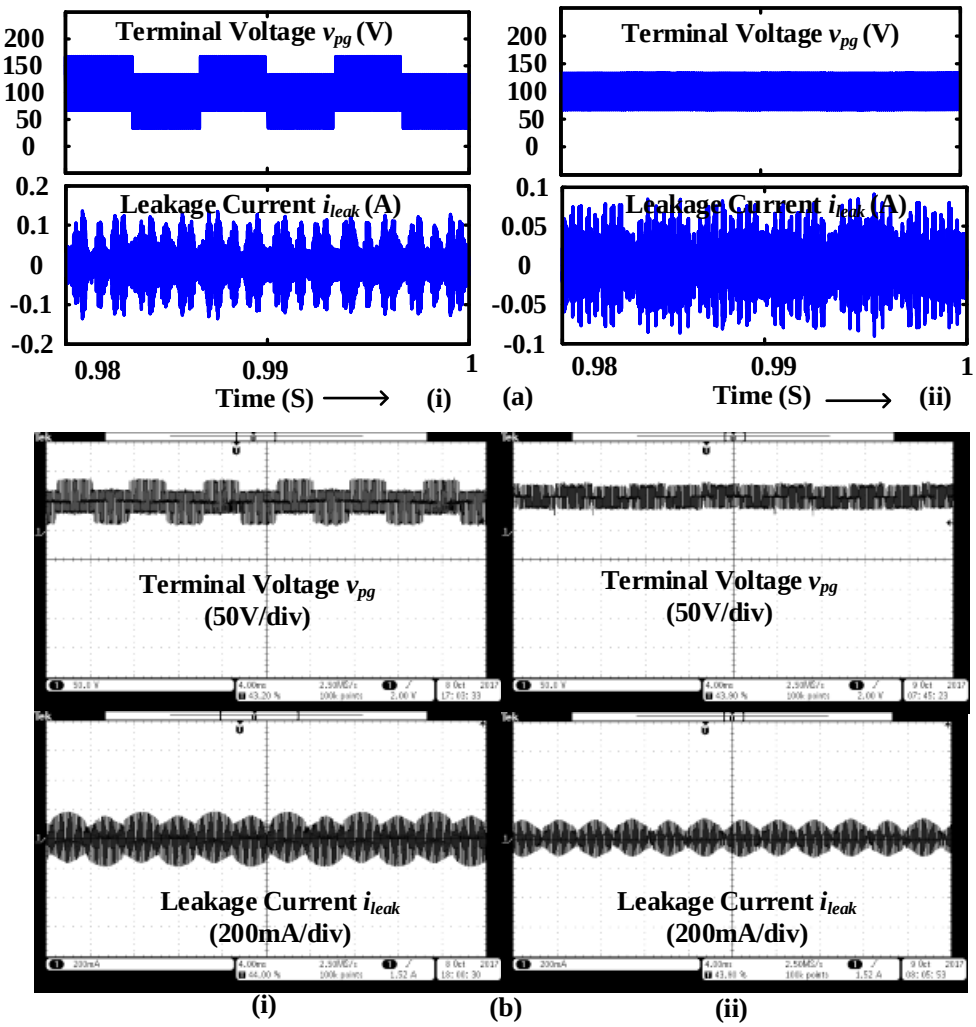


Fig. 8.6. The (a) simulation; (b) experimental waveforms of the terminal voltage and the leakage current for the (i) conventional CMLI and (ii) proposed NPC DC decoupled CMLI.

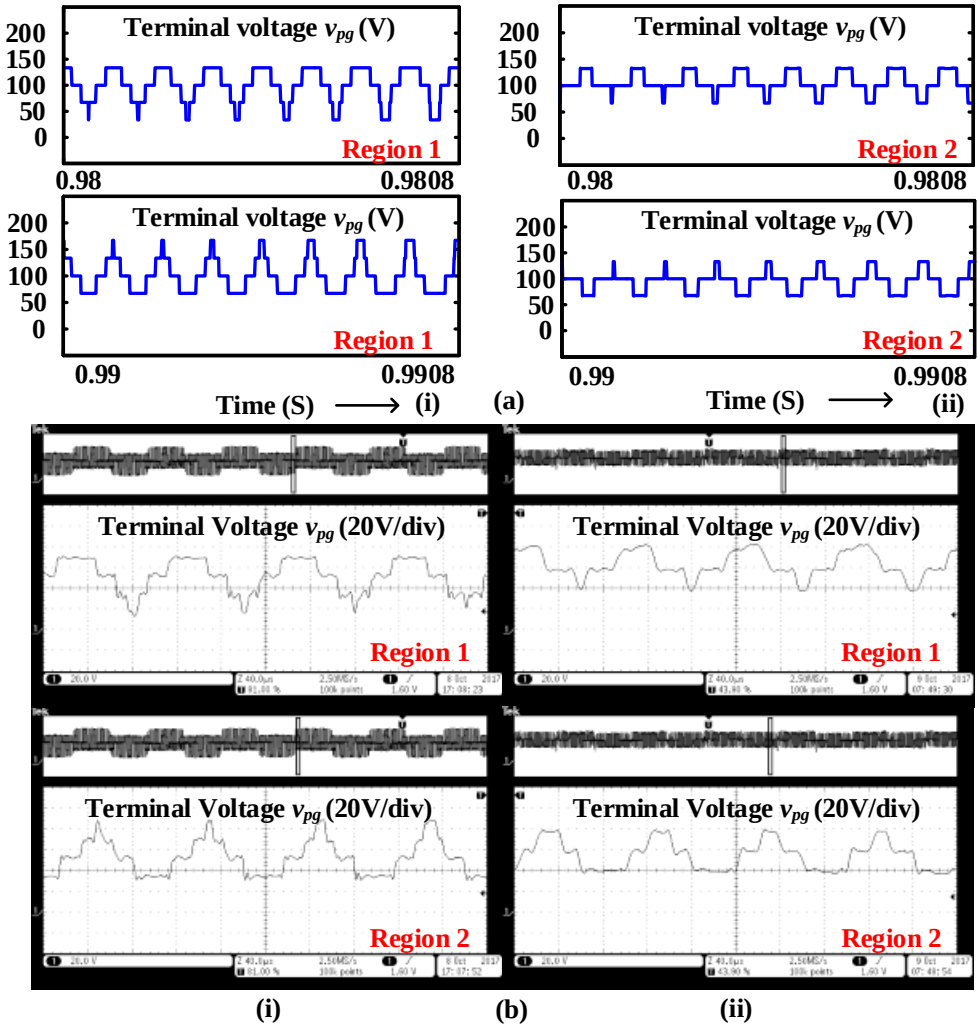


Fig. 8.7 The (a) simulation; (b) experimental waveforms of the terminal voltage 'v_{pg}' in the Region 1 and Region 2 for (i) conventional CMLI and (ii) proposed NPC DC decoupled CMLI.

8.5. Conclusion

This chapter presents a new NPC DC decoupling method based three-phase three-level CMLI for the minimization of leakage current in PV systems. The proposed inverter is obtained by clamping the three-phase three-level CMLI with the clamping circuitry formed by using switches and the capacitors. The proposed clamps the magnitude of terminal voltage during the common zero state to the previous active state value using the clamping circuit. This results in the reducing the number of transitions in the terminal and common mode voltage. The proposed CMLI reduces the number of transitions in the terminal to four from six compared to the conventional CMLI. Due to a reduction in the number transitions in the terminal voltage, the magnitude of leakage current flowing through the parasitic capacitance

of PV array in case of proposed CMLI is less compared to the conventional CMLI. This may further help in reducing the size of common mode choke and EML filter required in the proposed CMLI. The simulation and experimental results presented in the chapter also justify the given switching function analysis.

CHAPTER 9

Conclusion

Chapter 9

Conclusion

9.1. Summary

The work presented in this thesis mainly confers on the various transformerless multi-level inverter schemes for PV systems. Multi-level inverter solutions presented in the thesis minimizes the leakage current flow in the PV systems. The proposed solutions are either based on the PWM methods or configurations for the transformerless multi-level inverter based PV systems for the single-phase and three applications. The entire thesis is divided into nine chapters, including the present chapter.

Chapter 1 gives an introduction to the PV systems, classification of PV systems based on the inclusion of transformer, highlighting the problem of leakage current in the transformerless PV inverter topologies.

Chapter 2 addresses the comprehensive review of various single-phase PV inverter topologies for the minimization of the leakage current. The PV inverter topologies discussed are then compared in terms of number of devices used, number of capacitors used, number of switches conducting in positive and negative half cycles etc. Further, the analysis of the terminal voltage is given using the switching function concept, for reviewed inverter topologies are also presented. Finally, it sets motivation for the research work carried out in this thesis.

Chapter 3 presents a new low cost and efficient CMLI. The proposed CMLI is operated in both symmetrical and asymmetrical modes. Further, the generalized structure of proposed CMLI for higher levels in the output voltage is presented. The proposed CMLI operation in both symmetrical and asymmetrical modes is further supported by the simulation and experimental results.

Chapter 4 gives the details of the new PWM technique for the minimization of the leakage current in the grid-connected/stand-alone transformerless PV-CMLI. First, the operation of the CMLI is discussed along with its switching states. Next the analysis of the terminal voltage and common mode voltage for the five-level CMLI with proposed PWM

technique is given. The proposed PWM technique is further generalized for higher level operation. Further, the procedure for integrating the MPPT to the CMLI for both symmetrical and asymmetrical operations is discussed. Next, the simulation and experimental results were also presented to justify the correctness of given analysis.

In **Chapter 5**, a CMLI based on a highly efficient and reliable configuration for the minimization of the leakage current is proposed. First, the working principle and the operation of the proposed five-level grid-connected CMLI along with the generalized structure is described. The details of the PWM technique employed with its generalization for '*2m + 1*' levels are then explained. Next, the details of the MPPT algorithm which can be applied to the proposed five-level CMLI were explained. This is followed by the analysis of the terminal and CMVs for the proposed CMLI. The simulation and experimental results of the proposed five-level CMLI were presented. Finally, the comparison of the proposed CMLI with the other existing PV MLI topologies in the literature is presented.

Chapter 6 addresses the comprehensive review of various existing three-phase transformerless PV inverter topologies for the minimization of the leakage current. The analysis of the terminal voltage is done by using the switching function concept for each inverter topology.

In **Chapter 7**, a new three-phase PV inverter configuration based on CMLI is proposed for the minimization of the leakage current based on the DC decoupling methodology. First, the operation of the proposed three-phase CMLI is presented along with the PWM scheme used for the minimization of the leakage current. Next, the analysis of the terminal voltage for the extended three-phase CMLI is given. The simulation and experimental results of the three-phase CMLI are also presented.

Chapter 8 proposes a new three-phase PV inverter configuration based on CMLI is proposed for the minimization of the leakage current based on the NPC DC decoupling methodology. First, the operation of the proposed three-phase CMLI is presented along with the PWM scheme used for the minimization of the leakage current. Next, the analysis of the terminal voltage for the extended three-phase CMLI is given. The simulation and

experimental results of the proposed three-phase CMLI are presented to justify the switching function analysis.

9.2. Contributions

This section highlights the research work in the order they appear in the thesis.

i. **Analysis of terminal voltages of various single-phase transformerless PV inverter topologies using the switching function concept**

A comprehensive review of various single-phase PV inverter topologies for the minimization of the leakage current is presented. The analysis of the terminal voltage of various single-phase transformerless PV inverter topologies is done by using the switching function concept. The PV inverter topologies discussed are then compared in terms of number of devices used, number of capacitors used, number of switches conducting in positive and negative half cycles etc.

ii. **A new low cost and efficient CMLI topology**

A new low cost and efficient CMLI for single-phase PV system is presented. The complete details of the operation of the proposed CMLI in symmetrical and asymmetrical modes along with its extension to the higher number of levels with simulation and experimental results are discussed. The comparison of proposed CMLI with the other existing MLI topologies in the literature is also presented.

iii. **A new PWM technique for the minimization of leakage current in CMLI based single-phase PV system**s

A new PWM scheme is proposed for single-phase five-level CMLI for the minimization of leakage current without the addition of any extra circuitry elements is presented. The proposed CMLI is also integrated with the MPPT algorithm and is applied to a five-level CMLI. Furthermore, the analysis of the terminal voltage across the PV array and the common mode voltage of the inverter based on the switching function is presented.

iv. **A new efficient and reliable transformerless PV CMLI configuration for the minimization of the leakage current in the single-phase systems**

A new efficient and reliable transformerless PV CMLI configuration is proposed. Apart from a reduced switch count, the proposed CMLI topology has additional features of low switching and conduction losses. Furthermore, the extension of the proposed CMLI along with the PWM technique for higher levels in the output voltage is presented. A comparison of the proposed CMLI with the existing PV multilevel inverter topologies is also presented.

v. Review single-phase extended three-phase transformerless PV inverter topologies

A comprehensive review of various single-phase extended three-phase transformerless PV inverter topologies for the minimization of the leakage current. The analysis of the terminal voltage is done by using the switching function concept for each inverter topology.

vi. The new MLI topologies for the minimization of leakage current in three-phase systems

The new three-phase transformerless MLI topologies based on DC and NPC DC decoupling methodologies are presented for the minimization of leakage current. The complete details of the proposed three-phase transformerless MLI, analysis of the terminal voltage using switching functions, simulation and experimental were also presented.

9.3. Future scope of the research work

The research work presented in this thesis can be further investigated as pointed below:

i. Further, optimized PV multi-level inverter topologies for both single-phase and three-phase systems can be proposed which may require the reduced number of power semiconductor devices, components etc.

ii. The NPC decoupled MLI topologies can be extended using a switched capacitor for single-phase and three-phase systems.

iii. PWM techniques given for single-phase can be extended for three-phase systems.

iv. The proposed CMLI configurations and PWM techniques can be extended to the multi-phase system.

APPENDIX-I

Voltage/current ratings of switches used in CMLI topology discussed in chapter 4

The voltage ratings of switches used in CMLI topology used in chapter 4 is illustrated here. The switches in the Conv 1 (half –bridge) are connected across the PV panel PV_1 have a voltage of '$V_{PV}/2$'. So the blocking voltage of the switches Sw_1, Sw_2 and Sw_3 is equal to '$V_{OC}/2$', where 'V_{OC}' is the open circuit voltage of the PV panel and its voltage is equal to 1.2 times 'V_{PV}'. The switches in the Conv 2 (full-bridge) are connected across the complete DC bus so the blocking of the switches Sw_4, Sw_5, Sw_6 and Sw_7 is 'V_{OC}'. So the total KV rating of the switches used in the five-level inverter is 5.5 V_{OC}.

Voltage/current ratings of switches used in CMLI topology proposed in chapter 5

The voltage ratings of switches used in CMLI topology used in chapter 5 is illustrated here. The switches in the Conv 1 (half –bridge) are connected across the PV panel PV_1 having a voltage of '$V_{OC}/2$', where 'V_{OC}' is the open circuit voltage of the PV panel and its voltage is equal to 1.2 times 'V_{PV}'. So the blocking voltage of the switches Sw_1 and Sw_2 is equal to '$V_{PV}/2$'. The switches in the Conv 2 (full-bridge) are connected across the complete DC bus so the blocking of the switches Sw_3, Sw_4, Sw_5, and Sw_6 is 'V_{OC}'. The switches Sw_7 and Sw_8 are equal to 'V_{OC}'. So the total KV rating of the switches used in the five-level inverter is $7V_{OC}$.

REFERENCES

[1]. https://en.wikipedia.org/wiki/Solar_power_by_country

[2]. T. Kerekes, "Analysis and modeling of transformerless photovoltaic inverter systems", Institute of Energy Technology, Aalborg University, 2009.

[3]. S.B. Kjaer, "Design and control of an inverter for photovoltaic applications", Institute of Energy Technology, Aalborg University, 2005.

[4]. B. D. Reddy, M. P. Selvan, S. Moorthi, "Design operation and control of S3 inverter for single phase micro-grid applications", *IEEE Trans. Ind. Elect.*, vol. 62, no. 9, pp. 5569-5577, Mar. 2015.

[5]. Y. Hu, W. Xiao, W. Cao, B. Ji, D. J. Morrow, "Three-port DC-DC converter for stand-alone photovoltaic systems", *IEEE Trans. Power Elect.*, vol. 30, no. 6, pp. 3068-3076, Jun. 2015.

[6]. S. K. Mazumder, "Hybrid modulation scheme for a high-frequency AC-link inverter", *IEEE Trans. Power Elect.*, vol. 31, no. 1, pp. 861-870, Jan. 2016.

[7]. K. Basu, N. Mohan, "A high-frequency link single-stage PWM inverter with common-mode voltage suppression and source-based commutation of leakage energy", *IEEE Trans. Power Elect.*, vol. 29, no. 8, pp. 3907-3918, Aug. 2014.

[8]. J. S. Kim, J. M. Kwon and B. H. Kwon, "High-Efficiency Two-Stage Three-Level Grid-Connected Photovoltaic Inverter," *IEEE Trans. Ind. Elect.*, vol. 65, no. 3, pp. 2368-2377, March 2018.

[9]. R. T. H. Li, C. N. M. Ho and E. X. Chen, "Active Virtual Ground— Single-Phase Transformerless Grid-Connected Voltage Source Inverter Topology *IEEE Trans. Power Elect.*, vol. 33, no. 2, pp. 1335-1346, Feb. 2018.

[10]. H. F. Xiao, L. Zhang and Y. Li, "A Zero-Voltage-Transition HERIC-Type Transformerless Photovoltaic Grid-Connected Inverter," *IEEE Trans. Ind. Elect.*, vol. 64, no. 2, pp. 1222-1232, Feb. 2017.

[11]. G. E. Valderrama, G. V. Guzman, E. I. Pool-Mazún, P. R. Martinez-Rodriguez, M. J. Lopez-Sanchez and J. M. S. Zuñiga, "A Single-Phase Asymmetrical T-Type Five-Level Transformerless PV Inverter," *IEEE Jour. of Emer. and Selec. Topics Power Elect.*, vol. 6, no. 1, pp. 140-150, March 2018.

[12]. H. F. Xiao, L. Zhang and Y. Li, "An Improved Zero-Current-Switching Single-Phase Transformerless PV H6 Inverter With Switching Loss-Free," *IEEE Trans. Ind. Elect.*, vol. 64, no. 10, pp. 7896-7905, Oct. 2017.

[13]. G. Petrone, G. Spagnuolo, R. Teodorescu, M. Veerachary, M. Vitelli, "Reliability issues in photovoltaic power processing systems", *IEEE Trans. Ind. Elect.*, vol.55, no. 7, pp. 2569-2580, Jul. 2008.

[14]. L. Wang, Y. Shi, Y. Shi, R. Xie and H. Li, "Ground Leakage Current Analysis and Suppression in a 60-kW 5-Level T-Type Transformerless SiC PV Inverter," *IEEE Trans. Power Elect.*, vol. 33, no. 2, pp. 1271-1283, Feb. 2018.

[15]. Y. P. Siwakoti and F. Blaabjerg, "Common-Ground-Type Transformerless Inverters for Single-Phase Solar Photovoltaic Systems," *IEEE Trans. Ind. Elect.*, vol. 65, no. 3, pp. 2100-2111, March 2018.

[16]. F. Wang, Z. Li, H. T. Do and D. Zhang, "A Modified Phase Disposition Pulse Width Modulation to Suppress the Leakage Current for the Transformerless Cascaded H-Bridge Inverters," *IEEE Trans. Ind. Elect.*, vol. 65, no. 2, pp. 1281-1289, Feb. 2018.

[17]. M. Tofigh Azary, M. Sabahi, E. Babaei and F. Abbasi Aghdam Meinagh, "Modified Single-Phase Single-Stage Grid-Tied Flying Inductor Inverter With MPPT and Suppressed Leakage Current," *IEEE Trans. Ind. Elect.*, vol. 65, no. 1, pp. 221-231, Jan. 2018.

[18]. X. Guo, J. Zhou, R. He, X. Jia and C. A. Rojas, "Leakage Current Attenuation of a Three-Phase Cascaded Inverter for Transformerless Grid-Connected PV Systems," in *IEEE Trans. Ind. Elect.*, vol. 65, no. 1, pp. 676-686, Jan. 2018.

[19]. M. H. Hedayati, and V. John, "Filter Configuration and PWM Method For Single-Phase Inverters With Reduced Conducted EMI Noise," *IEEE Trans. Ind. Appli.*, vol. 51, no. 4, pp. 3236-3243, July 2015.

[20]. O. Lopez, F.D. Freijedo, A.G. Yepes, P. F. Comesaa, J. Malvar, R. Teodorescu and J. D. Gandoy, "Eliminating Ground Current in a Transformerless Photovoltaic Application," *IEEE Trans. Energy Conv.*, vol.25, no.1, pp.140-147, March 2010.

[21]. O. Lopez, R. Teodorescu, and J. Doval-Gandoy, "Multilevel transformerless topologies for single-phase grid-connected converters," Proc. IEEE IECON, pp. 5191–5196, 2006.

[22]. I. Patrao, E. Figueres, F. Gonzalez-Espin, and G. Garcera, "Transformerless topologies for grid-connected single-phase photovoltaic inverters, " *Elsevier Renewable and Sustainable Energy Review*, vol. 15, no. 7, pp. 3423–3431, September 2011.

[23]. Y. Yang, H. Wang, F. Blaabjerg, and K. Ma, "Mission profile based multidisciplinary analysis of power modules in single-phase transformerless photovoltaic inverters," Proc. EPE ECCE Eur., pp. 1–10, September 2013.

[24]. L. Zhang, K. Sun, Y. Xing, and M. Xing, "H6 Transformerless Full-Bridge PV Grid-Tied Inverters," *IEEE Trans. Power Elect.*, vol. 29, no. 3, pp. 1229-1238, March 2014.

[25]. L. Zhang, K. Sun, L. Feng, H. Wu and Y. Xing, "A Family of Neutral Point Clamped Full-Bridge Topologies for Transformerless Photovoltaic Grid-Tied Inverters," *IEEE Trans. Power Elect.*, vol.28, no.2, pp.730-739, Feb. 2013.

[26]. M. Islam and S. Mekhilef, "H6-type transformerless single-phase inverter for grid-tied photovoltaic system," *IET Elect. Power Elect.*., vol.8, no.4, pp.636-644, 2015.

[27]. H.F. Xiao, K. Lan and L. Zhang, "A Quasi-Unipolar SPWM Full-Bridge Transformerless PV Grid-Connected Inverter with Constant Common-Mode Voltage," *IEEE Trans. Power Elect*., vol.30, no.6, pp.3122-3132, June 2015.

[28]. B.Ji, J. Wang and J. Zhao, "High-Efficiency Single-Phase Transformerless PV H6 Inverter With Hybrid Modulation Method," *IEEE Trans. Ind. Elect*., vol.60, no.5, pp.2104-2115, May 2013.

[29]. Clemente, "A simple tool for the selection of IGBTs for motor drives and UPSs," Proc. IEEE APEC, pp. 755–764, March 1995.

[30]. T. Shimizu, and S. Iyasu, "A Practical Iron Loss Calculation for AC Filter Inductors Used in PWM Inverters," *IEEE Trans. Ind. Elect.,* vol. 56, no. 7, pp. 2600-2609, July 2009.

[31]. E. Babaei, M. F. Kangarla, M. Sabahi, M. R. A. Pahlavani, "Cascaded multilevel inverter using sub-multilevel cells", *Electr. Power Syst. Res.*, vol. 96, pp. 101-110, Mar. 2013.

[32]. A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Trans. on Ind. Appli*., vol. 17, no. 5, pp. 518-523, Sept 1981.

[33]. J. Rodriguez, Jih-Sheng Lai, and Fang Zheng Peng, "Multilevel inverters: a survey of topologies, controls, and applications," *IEEE Trans. Ind. Elect*., vol. 49, no. 4, pp. 724-738, Aug 2002.

[34]. O. Lopez, R. Teodorescu, F. Freijedo, J. D. Gandoy, "Leakage current evaluation of a single-phase transformerless PV inverter connected to the grid", Proc. IEEE APEC, pp. 907-912, Mar. 2007.

[35]. S. Bhattacharya, T. M. Frank, D. M. Divan, B. Banerjee, "Active filter system implementation", *IEEE Ind. Appli. Mag.*, vol. 4, no. 5, pp. 47-63, Oct. 1998.

[36]. S. Maity, P. K. Sahu, "Modeling and analysis of a fast and robust module-integrated analog photovoltaic MPP tracker", *IEEE Trans. Power Elect.*, vol. 31, no. 1, pp. 280-291, Jan. 2016.

[37]. S. Jain, A. K. Thopukara, R. Karampuri, V. T. Somasekhar, "A single-stage photovoltaic system for a dual-inverter-fed open-end winding induction motor drive for pumping applications", *IEEE Trans. Power Elect.*, vol. 30, no. 9, pp. 4809-4818, Sep. 2015.

[38]. S. Jain, R. Karampuri, V. T. Somasekhar, "An integrated control algorithm for a single-stage PV pumping system using an open-end winding induction motor", *IEEE Trans. Ind. Elect.*, vol. 63, no. 2, pp. 956-965, Feb. 2016.

[39]. W. Chen, X. Yang, W. Zhang, X. Song, "Leakage current calculation for PV inverter system based on a parasitic capacitor model", *IEEE Trans. Power Elect*., vol. 31, no. 12, pp. 8205-8217, Dec. 2016.

[40]. Z. Yang, H. Li, F. Lin, B. Zhang, J. Lu, "Common-mode electromagnetic interference calculation method for a PV inverter with chaotic SPWM", *IEEE Trans. Magn.*, vol. 51, no. 11, pp. 1-4, Nov. 2015.

[41]. M. Islam, S. Mekhilef, "Efficient transformerless MOSFET inverter for grid-tied photovoltaic system", *IEEE Trans. Power Elect.*, vol. 31, no. 9, pp. 6305-6316, Sep. 2016.

[42]. T. Kerekes, R. Teodorescu, P. Rodriguez, G. Vazque, E. Aldabas, "A new high-efficiency single-phase transformerless PV inverter topology", *IEEE Trans. Ind. Elect.*, vol. 58, no. 1, pp. 184-191, Jan. 2011.

[43]. S. V. Araujo, P. Zacharias, R. Mallwitz, "Highly efficient single-phase transformerless inverters for grid-connected photovoltaic systems", *IEEE Trans. Ind. Elect.*, vol. 57, no. 9, pp. 3118-3128, Sep. 2010.

[44]. G. Vazquez, P. R. M. Rodriguez, G. Escobar, J. M. Sosa, R. M. Mendez, "A PWM method for single-phase cascade multilevel inverters to reduce leakage ground current in transformerless PV systems", *Int. Trans. Elect. Energy Syst.*, vol. 26, no. 11, pp. 2353-2369, 2016.

[45]. M. Killi, S. Samanta, "Modified perturb and observe MPPT algorithm for drift avoidance in photovoltaic systems", *IEEE Trans. Ind. Elect.*, vol. 62, no. 9, pp. 5549-5559, Sep. 2015.

[46]. G. Buticchi, D. Barater, E. Lorenzani, C. Concari, G. Franceschini, "A nine-level grid-connected converter topology for single-phase transformerless PV systems", *IEEE Trans. Ind. Elect.*, vol. 61, no. 8, pp. 3951-3960, Aug. 2014.

[47]. D. Barater, G. Buticchi, E. Lorenzani, C. Concari, "Active common-mode filter for ground leakage current reduction in grid-connected PV converters operating with arbitrary power factor", *IEEE Trans. Ind. Elect.*, vol. 61, no. 8, pp. 3940-3950, Aug. 2014.

[48]. M. Cavalcanti, K. De Oliveira, A. M. de Farias, F. Neves, G. Azevedo, F. Camboim, "Modulation techniques to eliminate leakage currents in transformerless three-phase photovoltaic systems", *IEEE Trans. Ind. Elect.*, vol. 57, no. 4, pp. 1360-1368, Apr. 2010.

[49]. T. Kerekes, R. Teodorescu, M. Liserre, C. Klumpner, M. Sumner, "Evaluation of three-phase transformerless photovoltaic inverter topologies", *IEEE Trans. Power Elect.*, vol. 24, no. 9, pp. 2202-2211, Sep. 2009.

[50]. T. K. S. Freddy, N. A. Rahim, W. P. Hew, H. S. Che, "Modulation techniques to reduce leakage current in three-phase transformerless H7 photovoltaic inverter", *IEEE Trans. Ind. Elect.*, vol. 62, no. 1, pp. 322-331, Jan. 2015.

[51]. F. Wu, X. Li, F. Feng, H.B. Gooi, "Modified cascaded multilevel grid-connected inverter to enhance european efficiency and several extended topologies", *IEEE Trans. Ind. Elect.*, vol. 11, no. 6, pp. 1358-1365, Oct. 2013.

[52]. T. K. S. Freddy, N. A. Rahim, W. P. Hew and H. S. Che, "Comparison and Analysis of Single-Phase Transformerless Grid-Connected PV Inverters," *IEEE Trans. Power Elect.*, vol. 29, no. 10, pp. 5358-5369, Oct. 2014.

[53]. X. Guo, D. Xu and B. Wu, "Three-phase seven-switch inverter with common mode voltage reduction for transformerless photovoltaic system," Proc. IEEE IECON, pp. 2279-2284, 2014.

[54]. R. Gonzalez, J. Lopez, P. Sanchis and L. Marroyo, "Transformerless Inverter for Single-Phase Photovoltaic Systems," *IEEE Trans. Power Elect.*, vol. 22, no. 2, pp. 693-697, March 2007.

[55]. L. Concari, D. Barater, G. Buticchi, C. Concari and M. Liserre, "H8 Inverter for Common-Mode Voltage Reduction in Electric Drives," ," *IEEE Trans. on Ind. Appli*., vol. 52, no. 5, pp. 4010-4019, Sept.-Oct. 2016.

[56]. V. T. Somasekhar and K. Gopakumar, "Three-level inverter configuration cascading two two-level inverters," *IEE Proc. Elect. Power Appli.*, vol. 150, no. 3, pp. 245-254, May 2003

[57]. M. J. Tsai, H. C. Chen, M. R. Tsai, Y. B. Wang and P. T. Cheng, "Evaluation of Carrier-Based Modulation Techniques With Common-Mode Voltage Reduction for Neutral Point Clamped Converter," *IEEE Trans. Power Elect.*, vol. 33, no. 4, pp. 3268-3275, April 2018.

[58]. V. Sonti, S. Jain and S. Bhattacharya, "Analysis of the Modulation Strategy for the Minimization of the Leakage Current in the PV Grid-Connected Cascaded Multilevel Inverter," *IEEE Trans. Power Elect.*, vol. 32, no. 2, pp. 1156-1169, Feb. 2017.

[59]. S. Jain, and S. Venu, "A Highly Efficient and Reliable Inverter Configuration Based Cascaded Multilevel Inverter for PV Systems," *IEEE Trans. Ind. Elect.*, vol. 64, pp. 2865-2875, April 2017.

[60]. X. Guo, J. Zhou, R. He, X. Jia and C. A. Rojas, "Leakage Current Attenuation of a Three-Phase Cascaded Inverter for Transformerless Grid-Connected PV Systems," *IEEE Trans. Ind. Elect.*, vol. 65, no. 1, pp. 676-686, Jan. 2018.

LIST OF PUBLICATIONS

Refereed International Journal Publications:

1. S. Venu, S. Jain, and S. Bhattacharya, "**Analysis of the Modulation Strategy for the Minimization of the Leakage Current in the PV Grid-Connected Cascaded Multilevel Inverter**," *IEEE Transactions on Power Electronics*, vol. 32, pp. 1156-1169, Feb 2017.
2. S. Jain, and S. Venu, "**A Highly Efficient and Reliable Inverter Configuration Based Cascaded Multilevel Inverter for PV Systems**," *IEEE Transactions on Industrial Electronics*, vol. 64, pp. 2865-2875, April 2017.
3. S. Venu and S. Jain, "DC Decoupling Based Three-Phase Three-Level Transformerless PV Inverter Topology for Minimization of Leakage Current," (accepted for publication in *IEEE Transactions on Industrial Electronics*).

Conference Publications:

1. S. Venu, S. Jain and V. Agarwal, "**A new low cost and high efficiency cascaded half- bridge multilevel inverter with reduced number of switches**," Power Electronics, Drives and Energy Systems (PEDES), 2014 IEEE International Conference, vol., no., pp.1-6, Dec. 2014.
2. S. Venu, S. Jain and S. Bhattacharya, "**A new modulation strategy for the grid connected cascaded multi-level PV inverter to minimize the leakage current, "**National Power Electronics Conference (NPEC), vol., no., pp.1-5, Dec. 2015.