POWER MANAGEMENT CIRCUIT STRATEGIES FOR MOBILE APPLICATIONS

Submitted in partial fulfilment of the requirements

for the award of the degree of

Doctor of Philosophy

by

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2018

DECLARATION

This is to certify that the work presented in the thesis entitled **"Power Management Circuit Strategies for Mobile Applications"** is a bonafide work done by me under the supervision of **Dr. P. Sreehari Rao**, Associate Professor, Department of Electronics and Communication Engineering, National Institute of Technology Warangal, India and was not submitted elsewhere for the award of any degree.

I declare that this written submission represents my ideas in my own words and where others' ideas or words have been included, I have adequately cited and referenced the original sources. I also declare that I have adhered to all principles of academic honesty and integrity and have not misrepresented or fabricated or falsified any idea/ data/ fact/ source in my submission. I understand that any violation of the above will be cause for disciplinary action by the institute and can also evoke penal action from the sources which have thus not been properly cited or from whom proper permission has not been taken when needed.

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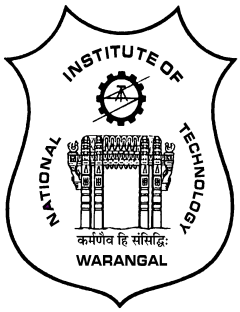

CERTIFICATE

This is to certify that the thesis entitled "**Power Management Circuit Strategies for Mobile Applications**" which is being submitted by **Mr. Suresh Alapati (Roll No. 701213)** in partial fulfilment for the award of the degree of **Doctor of Philosophy** to the Department of Electronics and Communication Engineering of National Institute of Technology Warangal, is a record of bonafide research work carried out by him under my supervision and has not been submitted elsewhere for any degree.

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Abstract

Majority of the portable systems driven by battery have become indispensable in every walk of life. It demands miniaturized System on Chip (SoC) solutions which are being supported by the scaled down technologies. The limited power available should be used judiciously to optimize the performance of these SoCs. This mandates deployment of efficient on-chip power management unit meeting the variety of applications. In particular, there exists a necessity to provide ripple free supply to the sensitive subsystems of the SoC. Low dropout voltage regulators being one of the best candidates meeting these demands, an attempt is made in this thesis to explore different topologies of on-chip capacitor-less low dropout voltage regulators to improve the transient performance, regulation, overall quiescent power requirement and stability for mobile applications including DDR3 IO circuits.

The conventional on-chip Low Dropout (LDO) voltage regulator suffers from poor stability particularly at lower load currents and bulky pass transistor makes the transient response sluggish against fast load transients. Towards this end an attempt is made to bias the regulator adaptive to load transients conserving the power. This topology achieves good transient response with fast settling time with a low compensation capacitance which also ensures stability at lower load currents.

Secondly, an LDO voltage regulator topology is presented with segmented pass transistors tailored made for lighter and heavier loads respectively. These pass transistors are driven by respective error amplifiers suitably designed to meet their individual requirements and the stability is improved by hybrid cascode compensation.

Thirdly, an adaptively biased LDO voltage regulator is presented that exploits bulk modulation of the segmented pass transistors. This reduces quiescent current consumption, overshoot/undershoot and corresponding settling times.

Further, a transient augmented path is employed transmitting the load transients swiftly to the gate of the segmented pass transistor through the control element. This improves the transient response along with adaptive bias which optimizes the power consumption.

These LDO circuits are designed using UMC 180nm CMOS process to deliver nominal output voltages ranging from 1.4 to 1.6V for the load variation of 0 to 100mA with a dropout voltage of 200 mV and a least quiescent current consumption of 1.5µA.

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Chapter 1

Introduction

System integration and portability are radically integrated into every walk of life. For example, mobile phones, laptops, wireless sensors and programmable digital appliances (PDA) have become indispensable. The growth of the battery-operated devices has been fuelling the silicon industry and hence global economy. This successful proliferation of usage of portable devices is attributed to concurrent evolution of increased functionality offering good sound, picture quality, increased display, size and massive computational capabilities in association with scaled down semiconductor technologies. However, these enhanced features consume a large power from the battery sooner.

The scaled down technologies augment portability paving the way for the entire system to be on-chip (SoC). This evolution of SoC further leads to fusion of several applications into a single portable device like mobile or hand-held PDAs. In addition, explosion of Internet of Things(IoT) into societal needs along with essential communication and entertainment features made these appliances power mongers taxing heavily the limited power resource. This prompts one to use battery thriftily.

The increasing demands for complex operations make the appliances to embed several high-performance analog and digital subsystems. These portable devices are powered generally by a single battery whose voltage varies in the course of operation as shown in Figure 1.1.

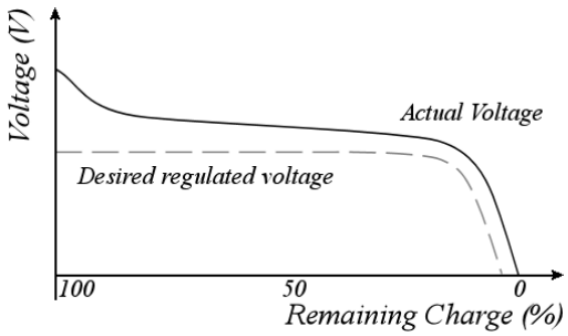

Figure 1.1 Battery characteristics [1]

The power requirements for analog and digital subsystems are different. Analog subsystems require relatively higher voltages with respect to their digital counterparts. Moreover, the density and cost benefits matter much for digital circuits but analog subsystems suffer from scaling [2]. These analog subsystems deal with feeble signals at the front end of systems. Thus, they cannot afford to use scaled down supply voltages as compared to their digital counterparts. On contrary, the digital subsystems enjoy relatively better noise margins. Also, high performance activities of subsystems deal with fast changing loads. Thus, there is necessity to employ a dedicated power management unit under mixed signal environment.

The task of managing power can be done using switching regulator (DC-DC converter) or linear regulator. DC-DC converters suffer from switching noise. The portable appliances with scaled down supply voltages cannot tolerate signal degradation due to noise. This prompts one to prefer linear regulators though DC-DC regulators are more efficient. Also, large filter components demand off-chip components pose challenges on transient response while discouraging their candidature for SoC. Since galaxies of different subsystems demand different power requirements while the appliance is powered by a single battery, it is required to optimally serve power free of switching noise where ever it is necessary which is addressed by linear regulators. However, the linear regulators suffer from dropout voltage which make them less attractive from the view point of efficiency. Thus, there is a necessity of linear

regulators that operate with low dropout voltage. Also, the large voltage dips during sudden load changes cause fault decisions in SoC which needs to be accounted.

An essential constituent of System on Chip is a high-performance power management unit. The complex system operations performed by the SoC subunits require right amount of power that ensures the correct operation of devices and also extends the life of the battery which is one of the prime requirements of portable devices. Dynamic voltage scaling a popular power distribution scheme used for System on Chip [3] applications. The power management integrated circuit (PMIC) of a mobile device is shown in Figure 1.2.

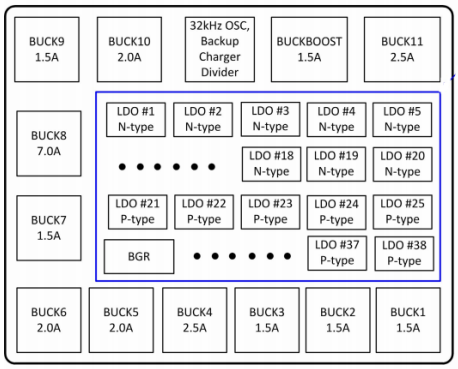

Figure 1.2 Floor plan of power management unit

A PMIC comprises of low dropout regulators generating different voltage levels such that they support applications such as application processor, memory, camera, radio frequency integrated circuits etc. The switching regulators switch the battery voltage to different voltage levels which in association with LDOs provide clean voltage levels to the analog and radio frequency circuits.

Typical mobile applications may require as large as 80 LDOs [4] that consume a large quiescent current and reduces the shelf life of battery. On contrary the digital circuits can operate at lowest possible supply voltages supported by available scaled down technology in order to exploit the fruits of advanced process nodes. However, the display and I/O interfaces operate at higher voltages. The power amplifiers are operated with a higher supply voltage relative to that of the other parts of analog /RF sub blocks to deliver required power to the output.

The different functions of subunits of a System on Chip and their corresponding energy consumptions [5] is shown in Figure 1.3.

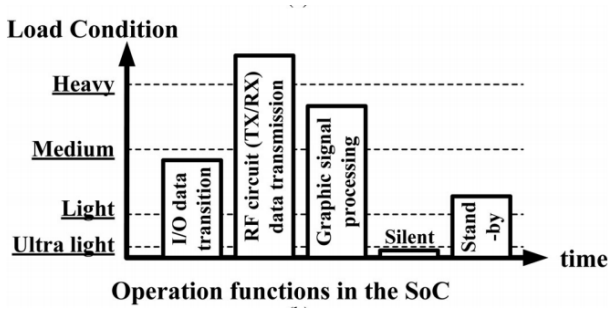

Figure 1.3 Power profiles of SoC sub systems

Thus varied power requirements can be met by suitable power managing circuits viz., switching regulators [6] , [7] and linear regulators [8], [9]. The load current conditions vary widely based on their functional requirements. With the explosion of Internet of Things(IoT), the portable gadgets have become indispensable addressing wide spread of applications ranging from essential communication, highly accurate low frequency bio medical processing, high speed video streaming etc. Figure 1.4 illustrates the usage of voltage regulators at different load conditions. When SoC is operated for high speed transmission or sudden camera flashing it requires larger energy i.e. a heavier load current. A switching regulator provides the required driving current guaranteeing good power efficiency.

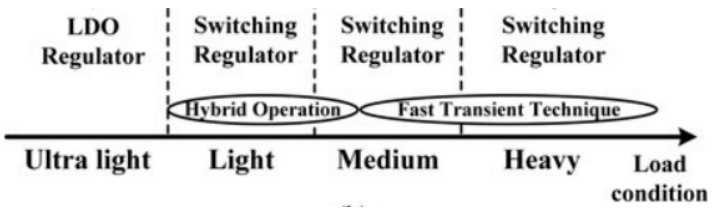

Figure 1.4 Regulators at different loads [4]

On the other hand, the power supply demands at medium and light loads is met by switching regulator with hybrid operation where as LDO regulator is used for powering relatively lighter loads that does not hamper efficiency and provides reasonably good transient response as it can offer relatively better loop gain bandwidth. Hence, issues such as power

efficiency and load transient response are considered simultaneously. Tandem operation of these two types yield better performance.

Conventional linear regulators make use of large off-chip components to pacify the effect of sudden load transients. But portable SoC systems discourage the use of external components as it demands for increase in IC pin count and occupies valuable board space. Thus, there is a necessity of a capacitor-less LDO voltage regulator that supplies power to the individual subsystems of these mobile appliances and making it completely on-chip.

Existing literature in this direction is extensively studied to identify parameters that influence the performance of on-chip LDO voltage regulators, and the corresponding circuit strategies are presented in the following sections.

1.1 Motivation

It is identified from the previous sections that portable mobile appliances demand dedicated power management unit to cater to the power needs of individual subsystems. It is realized that there is a necessity of on-chip LDO voltage regulator meeting the SoC requirements of these portable appliances. The literature survey reveals that the absence of large off-chip capacitor poses critical design challenges for the on-chip LDO voltage regulator. Stability, transient response and power consumption are identified as major design issues. Several attempts being made to improve transient response and reduce power consumption while maintaining stability for on-chip LDO voltage regulator is explored in the literature.

1.2 Problem statement

The mobile applications demand SoC solutions to augment portability. The conventional low dropout voltage regulator exhibits a dominant pole due to large off-chip capacitor and non-dominant pole due to error amplifier output node which is reasonably located farther away from the dominant pole making the system stable. Whereas in case of on-chip LDO, the absence of large off-chip capacitor makes the error amplifier pole dominant and pole due to output node to be non-dominant. Thus, variation of load current moves the

non-dominant pole back and forth. Under low load current, the non-dominant pole moves closer to the dominant one and makes the LDO unstable. Hence, it is aimed at developing circuit strategies for on-chip LDO voltage regulators while maintaining stability. In addition, the sudden load transients lead to large voltage shoots which are detrimental to the performance of the system. As the portable mobile appliances being driven by the battery, they cannot afford to consume much power towards regulation. This motivates one to investigate different circuit topologies for on-chip LDO voltage regulator to limit the voltage shoots while maintaining the trade off with quiescent current and settling time.

1.3 Objectives

- To explore different circuit strategies to improve transient response of on-chip LDO voltage regulator suitable for mobile applications.
- To identify the influence of varying loads on quiescent power consumption.
- To suggest circuit solutions to minimize quiescent power.
- Explore strategies to ensure stability across the load range.
- Modify the circuit topologies to offer improved regulation.

1.4 Contributions

The research work presented in the ensuing chapters of the thesis contributes in the field of on-chip LDO voltage regulators for portable applications which are mentioned briefly as following.

1. A Low dropout voltage regulator using improved folded cascode error amplifier with transient enhanced load tracking bias is presented in Chapter 4, section 4.5.

2. Segmentation of pass transistor was employed to mitigate the effects of single bulky pass transistor for improving transient response. In particular, the segmented pass transistors are driven by two exclusive error amplifiers optimized to meet their respective demands which is presented in Chapter 5, section 5.1.

3. A topology that makes use of pass transistor bulk modulation along with the segmentation and adaptive biasing that reduces the over/undershoots is presented in Chapter 5, section 5.2

4. Another topology is presented that employs transient augmentation path in addition to the bulk modulation which resulted in good performance is presented in Chapter 5, section 5.3.

1.5 Thesis Organization

The research work presents suitable circuit topologies that improve the transient response of on-chip low dropout voltage regulators. The organization of work is as follows:

Chapter 1 introduces the role of conventional voltage regulators in the power management unit. It also discusses the significance of capacitor-less LDOs to meet the requirements of portable PDAs and mobile applications.

Chapter 2 reviews the literature of state of the art capacitor-less low dropout regulators, their findings, and shortcomings. It concludes by stating the main objective of the thesis.

Chapter 3 presents characterization of on-chip LDO voltage regulator. Chapter 4 presents modelling and design of a transient enhanced load tracking bias low dropout regulator.

Chapter 5 presents different circuit strategies for LDO voltage regulator based on segmented pass transistor in order to improve the overall performance. Conclusions and future scope are given in chapter 6.

Chapter 2

Literature Survey

The fast-changing life styles of the mankind have become highly dependent on the multi-faceted battery driven portable gadgets. The diversified functionality slurps power from the battery at quicker rate that limits the shelf life of the battery. This necessitates a core power management that regulates the supply against the variation of the load current and battery voltages.

The situation gets exacerbated by the fact that wide variety of the features are integrated into the System on Chip (SoC) in portable appliances which demand contrast power supplies, e.g. a typical smartphone may need as high as 12 supply voltages to cater different subsystems including Power Amplifier, Wireless LAN, Display, Memory, video and audio processing applications etc. This makes design of power management unit to honour the

stringent demands of miniaturization, limited on board power and increased functionality [10].

The task of power management is achieved by the use of Linear Voltage regulators/Switching regulators. The most commonly used source of power happened to be the Li-Ion batteries in portable applications due to their better volumetric energy density [11]. The voltage of Li-Ion battery varies from 4.2V to 2.8V depending on its charge/discharge condition. Switching regulators offer requisite voltages against the wide battery variation efficiently [12]. However, they suffer from switching noise which cannot be tolerated with sensitive analog subsystems. Also, they require large off-chip filter components. On the other hand, linear regulators provide ripple free supply to the sensitive subsystems.

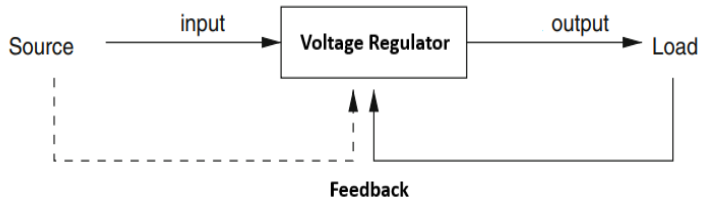

Figure 2.1 Block diagram of voltage regulator

The function of a voltage regulator is to provide a constant output voltage regardless of the changes to the supply or load as shown in Figure 2.1 [13]. A linear voltage regulator provides a constant output voltage by adjusting the regulator resistance according the load changes. Based on the placement of the regulating element, they can be classified as series or shunt regulator. Series regulators are more efficient than their shunt counterparts. In the series voltage regulator, the value of series resistance is varied in accordance with the load variations as shown in Figure 2.2.

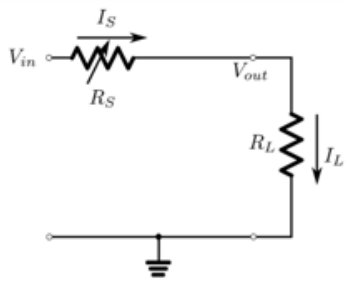

Figure 2.2 Series voltage regulator

The series element is implemented by an active element such as a BJT or MOSFET. The topology should be selected in such a way that the dropout voltage which is the difference between input and output should be minimum to improve the efficiency. A topology that uses NMOS pass transistor as pass element is shown in Figure 2.3. which offers low output impedance thereby maintaining good stability against load variations. However, higher input gate voltages required make them unsuitable for low voltage applications.

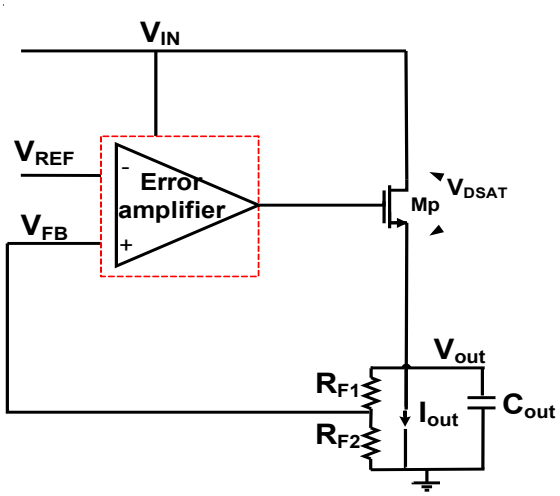

Figure 2.3 Linear voltage regulator with NMOS pass transistor

This problem can be addressed by replacing the NMOS transistor with PMOS pass transistor in the common source configuration a shown in Figure 2.4. This permits the gate voltage to approach as low as zero pulling the regulator output voltage as high as V_{IN}-V_{DSAT} that facilitates to minimize the dropout voltage by increasing the size of the pass transistor.

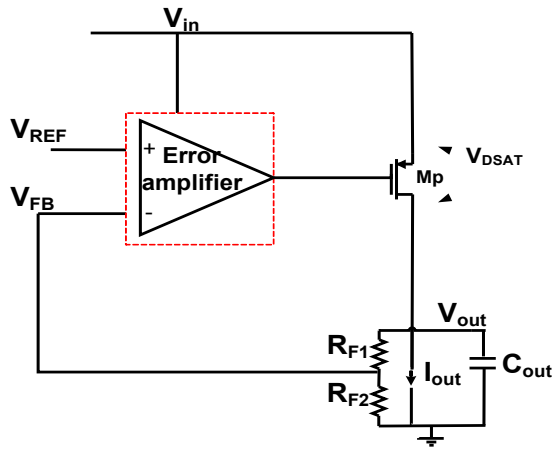

Figure 2.4 Low dropout regulator with PMOS pass transistor

The compensation of low dropout regulator is difficult due to the large inverting gain and the high output impedance of common source pass transistor [14], [15]. A shunt-series feedback operation is used for the low dropout regulator. The output voltage (V_{out}) sampled by feedback resistors R_{F1}, R_{F2} is series mixed with a constant reference voltage (V_{REF}) through a high gain error amplifier. Consequently, a virtual short between error amplifier inputs ensures the output voltage follows the reference voltage (V_{REF}). Any difference between them due to the output load variation generates a control signal that enables the PMOS pass transistor to source required current to replenish the regulated output voltage.

The transient response of the regulator is determined by its loop bandwidth and slew rate at the gate of pass transistor. The initial response of the regulator to load variations is usually slow due to the large gate capacitance of the pass transistor leading to large overshoot and undershoot voltages. This operation can be circumvented by a large value of load capacitor (C_{out}) that delivers the required charge that the load current demands to maintain a regulated output voltage. However, it occupies a large space on silicon and is not realizable for System on Chip applications. Portable SoC applications demand the regulator to be operated at lower supply voltages. However, its operation at lower supply voltages limits slew rate at the gate of pass transistor and reduces loop gain degrading load and line regulation.

Multiple approaches were adopted to improve the performance of LDOs [16], [17]. A current efficient buffer and forward biased pass transistor proposed in [16] enables LDO to be operated at lower voltages to overcome slew rate limitation and improving load regulation and

transient response. However, the trade-offs between output voltage accuracy, transient response and stability at lower currents is not accounted for. The LDO for low voltage applications require structural modifications and use of better compensation schemes. Hence a capacitor-less LDO that operates at lower voltages along with good stability and fast transient response is in demand. The load regulation performance of LDO is limited by DC loop gain and closed loop bandwidth and effect of frequency compensation on regulation performance was discussed in [17] A classical two-stage amplifier topology with pole splitting was considered to be not optimum as pass transistor could not function as a high gain stage in the dropout condition. Hence a topology in which LDO was viewed as a three-stage amplifier with pass transistor at last stage was proposed in [18] that makes use of damping factor control frequency compensation (DFC) as shown in Figure 2.5. It offers a fast load transient response and good power supply rejection ratio due to the large loop gain and uses a damping factor control frequency compensation scheme for attaining stability. However, the stability of the regulator at lower load currents was not ensured.

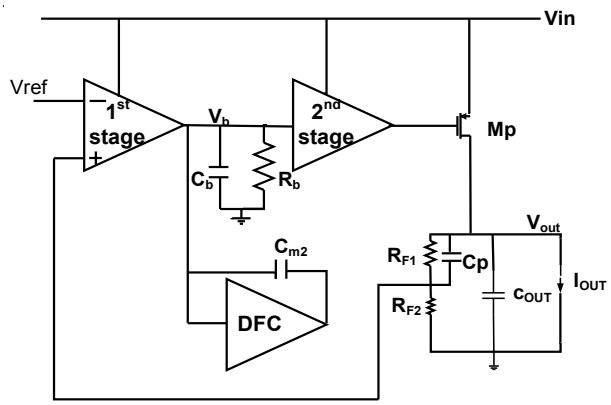

Figure 2.5 A three stage-based capacitor-less LDO regulator

A low dropout regulator that exploits voltage positioning and replica biasing techniques for voltage regulation was proposed in [19]. It consumes much larger quiescent current in full load conditions thereby lowering current efficiency and draining the battery power. A fast path based two stage capacitor-less LDO regulator topology was proposed by [8] is shown in Figure 2.6. which offered compensation by splitting the poles. However, the performance at ultra-light loads was not ensured.

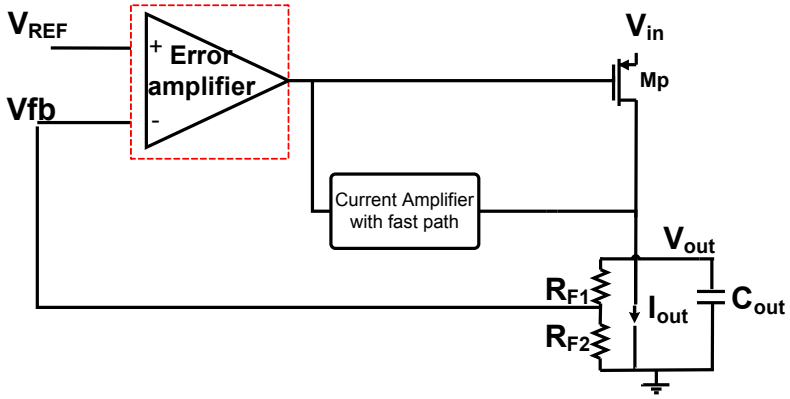

Figure 2.6 A two stage fully on-chip LDO regulator

The topology proposed in [8] was modified by introducing a bi-directional adaptive biasing structure in the feedforward signal path in [20] as shown in Figure 2.7. This structure improved stability for a wide range of load currents but a large compensation capacitance was used occupying more silicon space.

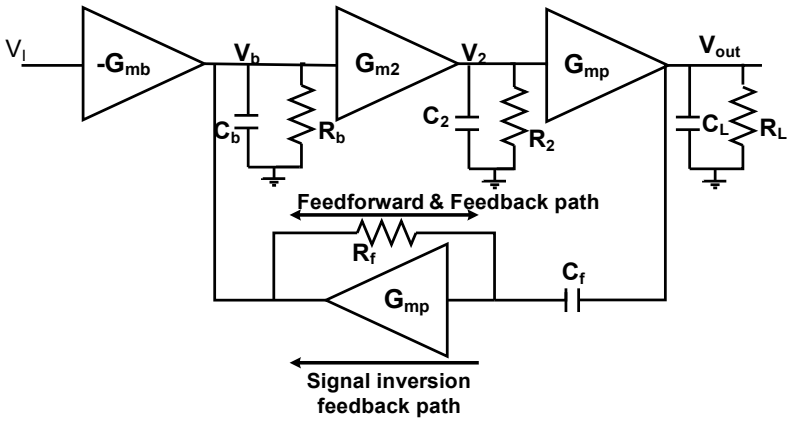

Figure 2.7 Capacitor-less LDO for SoC with bi-directional asymmetric buffer

An active feedback compensation strategy that uses a smaller on-chip capacitance in addition to pole splitting compensation proposed in [21] is shown in Figure 2.8. The slew rate enhancement stage employs two transconductance cells (G_{mx} and G_{ma}) for transient response improvement. However, the complex circuit consumes large quiescent current consuming more power.

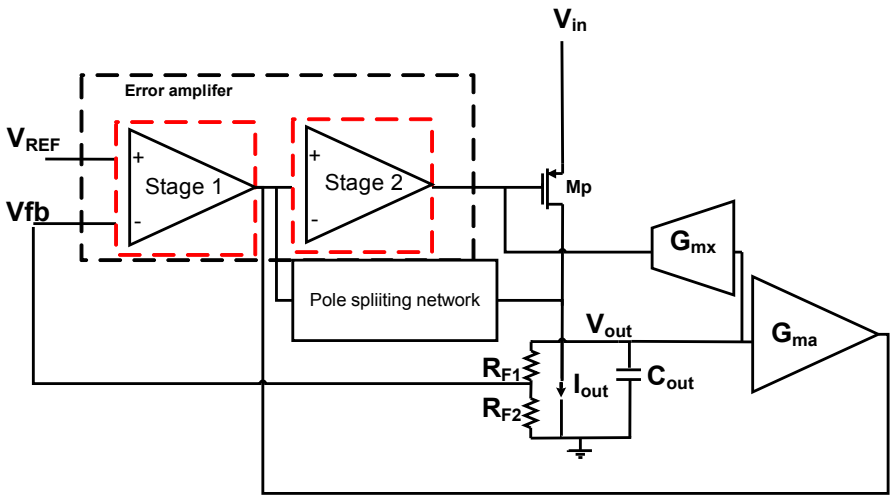

Figure 2.8 High speed active compensated slew rate enhanced circuit

The system on-chip (SoC) applications operate in sleep mode for a long period of time during which they demand lower quiescent current. Also, the stability at lower load currents needs to be addressed. The architectures cited so far focused on improving the performance by different compensation schemes. However, optimizing the error amplifier performance can further improve regulation and transient response with minimum quiescent current which was explored in the following architectures.

A push-pull configuration-based error amplifier as shown in Figure 2.9 was employed to improve transient response and reduce quiescent current by [22]. Though this topology minimized quiescent current, it suffered from large overshoots over a load range of 50µA to 50mA.

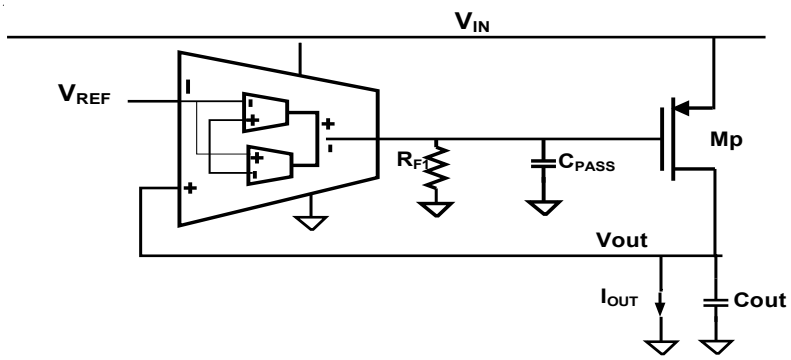

Figure 2.9 High slew rate push-pull configuration based LDO

A class AB trans-conductance error amplifier that increases current capability during large signal operation with a quiescent current of 41.5μA was reported by [23]. Although the dc gain is increased for better load regulation, the overshoot (200mV) and undershoot (385mV) are large while load current changes between 0.5mA to 200mA.

The LDOs with a large pass transistor to support low dropout and large load current are bulkier which results in sluggish transient response. A segmentation of pass transistor [24], [25] and use of control section for selection of pass transistor in accordance to load current demands provides a good solution and is shown in Figure 2.10. It offers stability at lower load currents along with less quiescent power consumption but voltage shoots are relatively high with moderate settling time.

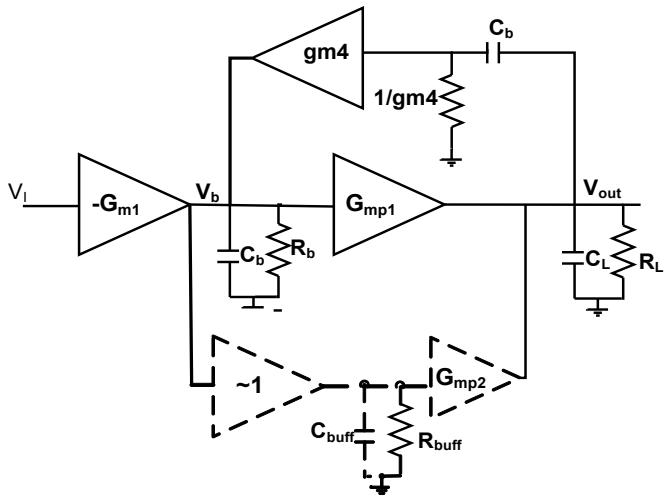

Figure 2.10 Basic block diagram of segmented pass transistor based LDO

The concept of flipped voltage follower was exploited to develop a low dropout voltage regulator using a single transistor without segmentation by [26]. However, the topology offers low loop gain affecting regulation and stability at low load currents. In addition, it uses large compensation capacitor of the order of nF. This topology was further modified to improve gain using additional gain stage by [27]. The topology uses a cascode stage at the gate of pass transistor that improves regulation and slew rate relatively. However, the transient response was poor even for a load current change from 3mA to 100mA.

An output capacitor-less LDO based on flipped voltage follower using damping factor control frequency compensation was presented in [28]. It demonstrated line and load regulation of 3.3mV/V and 62µV/mA respectively with a relatively larger settling time of 2.5µs. A flipped voltage follower based LDO is reported by [29] employing dual feedback loops to improve the transient performance. However, minimum load current of 1mA was considered, improvement in settling time was meagre. A flipped voltage follower based LDO employing two error amplifiers to cater low loads and high loads was proposed by [30] . The proposed topology with two individual error amplifiers with their individual segmented pass transistors improved transient response but consumes relatively large quiescent current.

Circuit strategies for LDO voltage regulators using adaptive biasing scheme were presented in [31] and shown in Figure 2.11a. The topology employed a gain enhanced structure that improves load regulation but requires 8µA quiescent current for a minimum load current of 3mA to maintain stability. However, this topology with its minimum load current limits its usage for applications that require lower load currents. An LDO topology with Q reduction technique was proposed by [32] is shown in Figure 2.11b. It requires a quiescent current of 30µA for a minimum load current of 50µA to maintain stability which is high for low power SoC applications. Another topology in which an auxiliary circuit with transistors biased in the subthreshold region was used to reduce undershoot in [33].

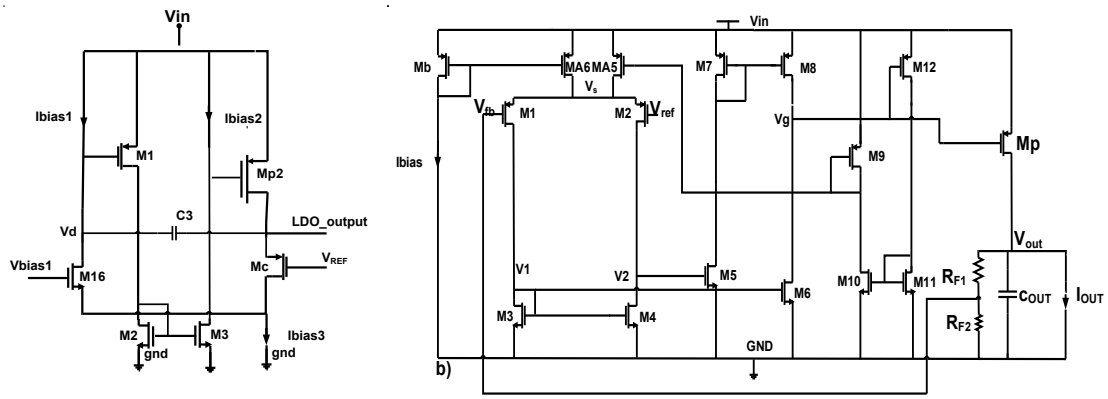

Figure 2.11 a) A 6-µW chip area efficient capacitor-less LDO b) Output-capacitor-free adaptively biased LDO

Although both the topologies use adaptive biasing architectures to improve the transient response but the bandwidth is limited due to the high gate capacitance of pass

transistor. So a large quiescent current is required for a faster transient response. The different trade-offs that exists among the performance parameters of LDO is analysed by [34] and a suitable design procedure for nested Miller compensated LDO was reported. Further, this topology optimized quiescent current with appropriate adaptive biasing as shown in Figure 2.12.

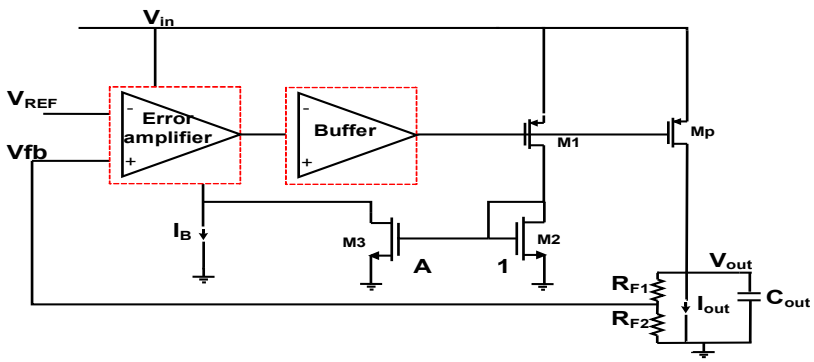

Figure 2.12 Adaptively biased low dropout regulator

Another LDO topology was reported by [35] that used to switch between two and three stages as the load current changes from low to high. At no load conditions, it dissipates only 0.9µA thus enhancing current efficiency, but the settling time is relatively high. An LDO topology with a cross coupled transistor along with adaptive biasing that improves transient response and load regulation, with a quiescent current of 242µA at full load was presented in [36]. However, the large gate capacitance of pass transistor limits output voltage settling time in response to wide range of load transients. A topology with bulk modulation of pass transistor [37] was explored to improve transient response of LDO as shown in Figure 2.13. However, the requirement for a separate error amplifier at the bulk of pass transistor consumes extra quiescent current which can be further optimized.

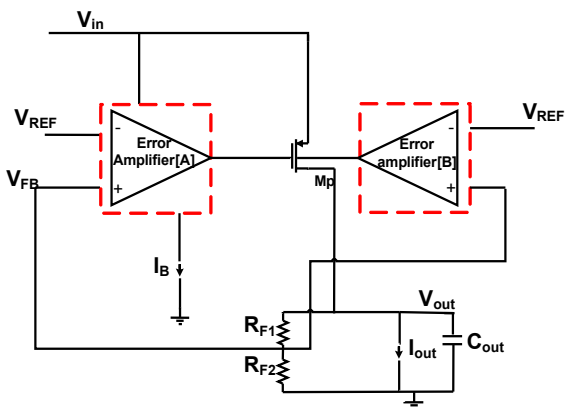

Figure 2.13 Bulk modulated LDO regulator

An analog assisted digital controlled LDO regulator [38] that employs passive elements to enhance the performance of the inverter is shown in Figure 2.14. However, as the regulation is controlled in steps by the discrete switching of pass transistors, the accuracy of the output is less.

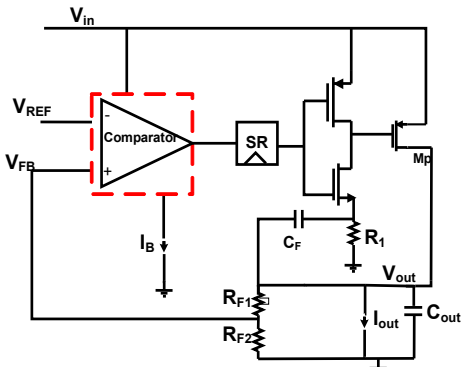

Figure 2.14 Analog assisted digital LDO regulator

A topology was attempted by [39] in which a conventional two stage operational amplifier was used as an error amplifier with a comparator in the fast path. But it reported the load variations from 0.5 mA to 100mA. LDO voltage regulator based on recycling folded cascode error amplifier as shown in Figure 2.15 was attempted by [40]. The error amplifier topology recycles the existent transistors for improvement of DC gain and bandwidth without consuming extra quiescent current thereby improving transient performance. But still there is a room for improvement of transient response.

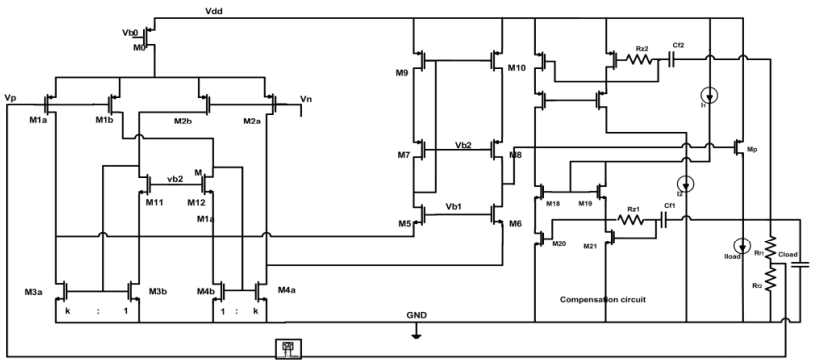

Figure 2.15 Capacitor-less LDO regulator with recycled folded cascode error amplifier

Similarly, a double recycled folded cascode [41] based error amplifier in Figure 2.16 with enhanced slew rate was employed by [42], [43] to improve the transient performance without consuming extra quiescent current. But the transient response reported for former took load variations from 0.5mA to 250mA, while the compensation capacitor size could be reduced for later.

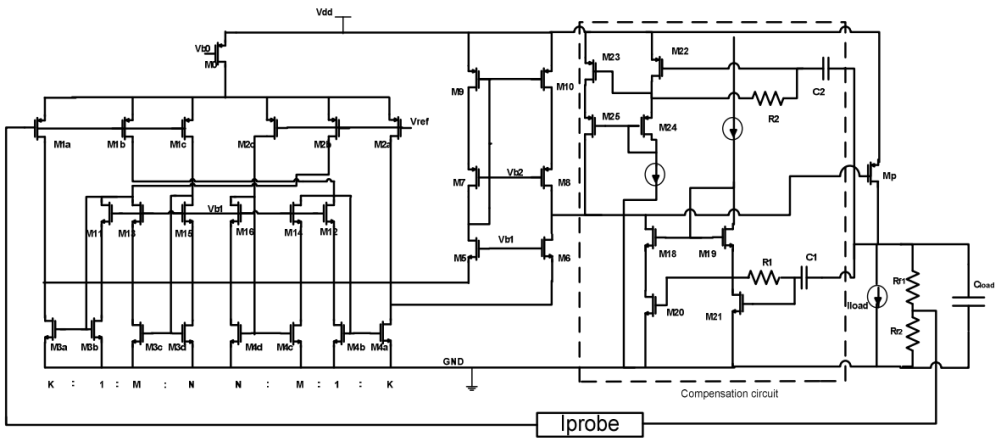

Figure 2.16 Capacitor-less LDO with double recycling folded cascode error amp. [42]

It is observed from literature that there exists trade off among stability, regulation, transient response, power consumption and speed of the on-chip LDO voltage regulator. This thesis explores to improve the performance of LDO voltage regulator aimed to power mobile applications including the I/O section of DDR3 memories.

Chapter 3

Characterization

3.1 Introduction

The performance of a regulator refers to the ability of an IC to offer a regulated output voltage against variable operating environment. The performance metrics include parameters such as load regulation, line regulation, power supply rejection, temperature drift, dropout voltage, transient response and efficiency. These parameters describe the circuit behaviour while subjected to variations of load current, input voltage and temperature. Some parameters such as quiescent current, ground current, power efficiency, current efficiency and dropout voltage portray the regulator power characteristics. The input voltage range, output voltage range, output capacitance (It's ESR) and load current determines the functionality requirements of the regulator adhering to the limits of circuit parameters. The battery dependent devices operate in different modes i.e. idle and wake up modes thus demanding the current consumption based on behavioural application. The current efficiency measures this performance and is primarily important during low load conditions. This thesis aims at providing the requisite supply to mobile applications including the DDR3 memory and other PDAs.

3.2 Nominal Output Voltage

The applications considered generally require a nominal voltage of the order of 1.5V. So, a nominal output voltage of 1.6V is chosen for the LDO regulator presented in the thesis.

3.3 Load Regulation

Load regulation is the steady state output voltage variation resulting from finite change of load current. A good regulator provides at its output a constant and reliable voltage within a tolerance that facilitates the smooth operation of the application without interruption. A lower load regulation value indicates best regulation. Conventionally the load regulation is defined as the ratio of difference between no load and full load voltage to the no load voltage. The

load regulation R_{LR} numerically represents a ohmic drop at the output of regulator as given in Equation 3.1.

$$R_{LR} = = \quad (3.1)$$

Where is the open loop output resistance,is the open loop gain, and is the feedback factor, and is the loop gain.

The asymmetric voltages and currents of the error amplifier, for example, current mirrors develop a systematic input offset voltage which further degrades the load regulation. Also the load dependent feedback voltage generates wide swing voltages at the internal nodes of error amplifier leading to an offset voltage impacting load regulation. So once these ill effects are included in the load regulation [44] the effective load regulation is modified as given in Equation 3.2.

$$\text{Effective } R_{LR} = + \quad (3.2)$$

Where is the offset voltage of error amplifier and is called the closed loop gain .

3.4 Line Regulation

Line regulation is defined as regulator ability to maintain the output voltage within a tolerance for the changes in the input line voltage by considering other influential factors remaining constant. It is expressed as percentage deviation from the nominal output voltage.

A power supply with tight line regulation delivers optimum voltages throughout the operating range of input line voltages. Typical line regulation characteristics of LDO regulator is shown in Figure 3.1.

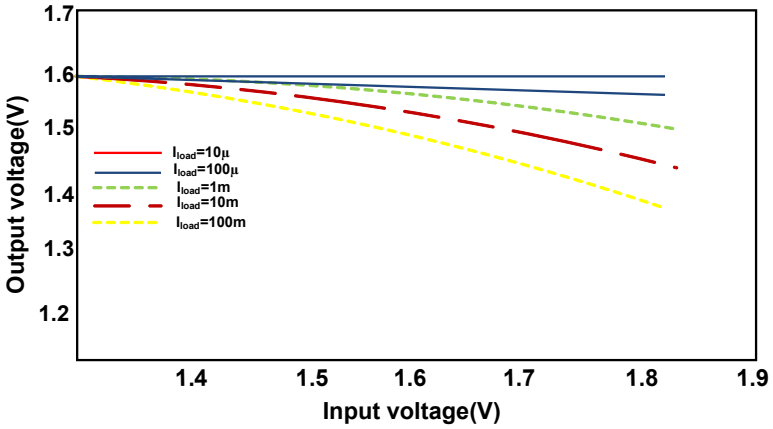

Figure 3.1 Line regulation characteristics

The changes in the input power supply voltage affects the regulator output voltage through the changes in the reference voltage V_{REF} and its closed loop gain A_{CL}. So, the overall supply gain A_G is given by Equation 3.3 [44].

$$A_G=+ \tag{3.3}$$

The typical battery-operated devices including DDR3 and other mobile applications require a load and line regulation of 1%.

3.5 Quiescent current and Ground current

The input current supplied to the internal circuitry of the regulator topology while the load current is zero is called quiescent current. The quiescent current comprises the operating current of bandgap reference, error amplifier, output voltage divider and other housekeeping functions like overcurrent and over voltage protection circuits. The total quiescent current used by the regulator depends on the configuration of topology, its input voltage and the extreme environments it is subjected. It can be noted that quiescent current is almost independent of input voltage variation as shown in the Figure 3.2

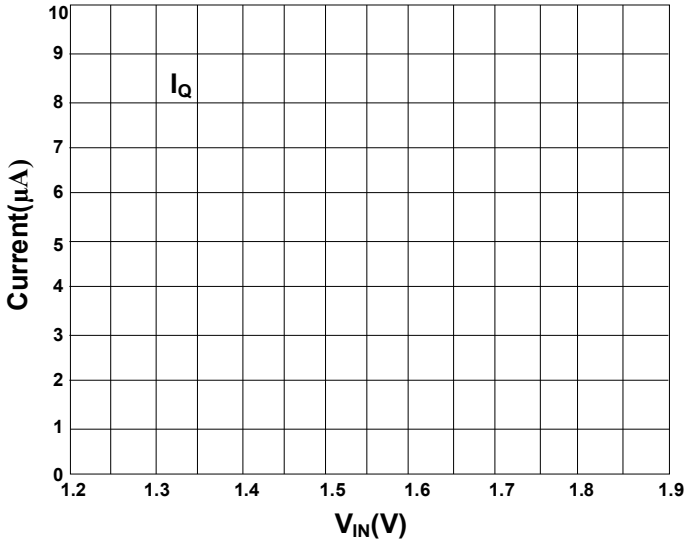

Figure 3.2 Quiscent current (I_Q) vs Input voltage (V_{IN}) [45]

The current difference between input and output of the topology is called ground current(I_{GND}). It includes quiescent current consumed by circuit topology. The lower the quiescent current the better the LDO efficiency.

$$I_{GND}=I_{IN}-I_{OUT} \tag{3.4}$$

The voltage drop that occurs across the pass transistor(Dropout) is compensated by increasing the gate drive of pass transistor by negative feedback operation which also increases the ground current. The ground current increases in the dropout region due to the saturation of driver stage.

3.6 Input and Output Voltage Range

The input voltage range corresponds to the permissible range of input voltages applied at the input of the regulator. The input voltage range should be adequate enough for meeting the specifications of a regulator. The relationship between input and output voltage is shown in Figure 3.3. The minimum operating input voltage is V_{OUT} +V_{DROP} or higher. If the input voltage to the regulator is less than effective input voltage range, then there is less likely that the output voltage is regulated. On further reduction, the output voltage may even drop down

to zero voltage. Some battery-operated appliances find its circuit operation at the lower limit of battery power supply.

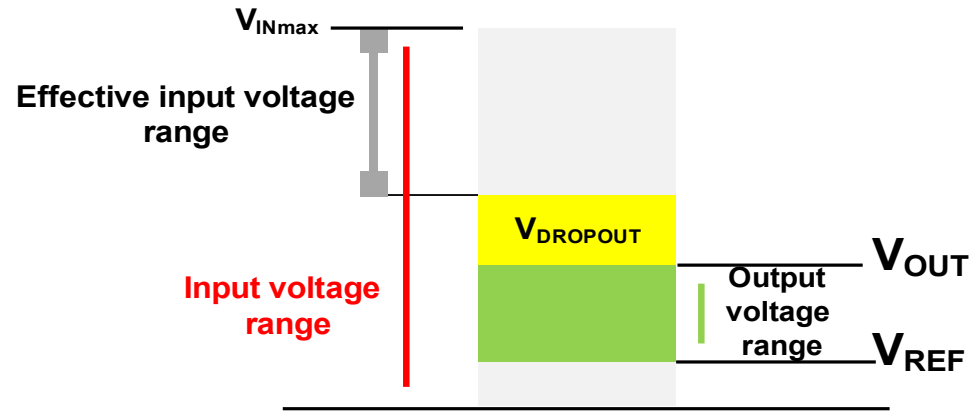

Figure 3.3 Input and Output Voltage Range [45]

The output voltage range is usually specified for an adjustable voltage regulator. The minimum voltage used for a better regulation is reference voltage(V_{REF}). If the circuits are operated below the V_{REF}, the regulation cannot be guaranteed. The maximum output voltage possible range is from V_{REF} to V_{INmax}-V_{DROP}. The extreme limits of operation are calculated based upon the maximum thermal conditions applicable without effecting the performance.

3.7 Efficiency

The two most important functions of a regulator are power conditioning and energy transfer from power source to the load [44]. The regulator's power conditioning ability is determined by the quality of power delivered (accuracy) to the application to operate it properly. Concurrently, efficiency determines the ability to transfer energy from power source to the load. Ideally, a regulator transfers the energy that a load demands but the conditioning operations of the regulator by the pass transistor lose energy across it. Efficiency is a performance metric that embraces the ratio of energy delivered to the load to the source supplied. The energy efficiency η is defined in Equation 3.5.

$$\eta = \qquad (3.5)$$

The power dissipated by the pass transistor is the product of the voltage drop (V_{IN}-V_{OUT}) and the current (I_{LOAD}). So, efficiency can be expanded as below in Equation 3.6. The parameter V_{IN}-V_{OUT} in the below equation is called as dropout voltage.

$$\eta= \tag{3.6}$$

The dropout voltage is the minimum voltage drop across the pass transistor below which the regulator stops regulating the output voltage. During this condition, the pass transistor supplies the maximum current through it to the load. An optimum efficiency is achieved while the dropout voltage is low.

3.8 Load and Line Transient

The behaviour of the regulator under sudden load transients is characterized by over shoot, under shoot and the settling time [46]. The open loop transfer function is shown in Figure 3.4. It comprises of output impedance $Z_{OUT}(s)$ and small signal gain from input to output as $G_{VIN}(s)$. The load and line step transient response are defined as $I_{LOAD}(s)$ and $V_{IN}(s)$ respectively. From the block diagram the output transient response is expressed as

$$V_{OUT}(s)=V_{IN}(s)*G_{VIN}(s)-I_{LOAD}(s)*Z_{OUT}(s) \tag{3.7}$$

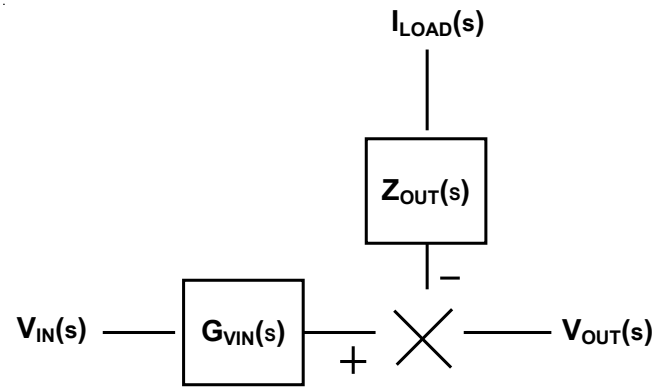

Figure 3.4 Open loop transfer function block diagram of LDO regulator

Any perturbation in the supply or at the output affects the output voltage. The closed loop control diagram is shown in Figure 3.5. In this diagram the feedback output is compared to a reference value, V_{REF} in order to make the necessary correction.

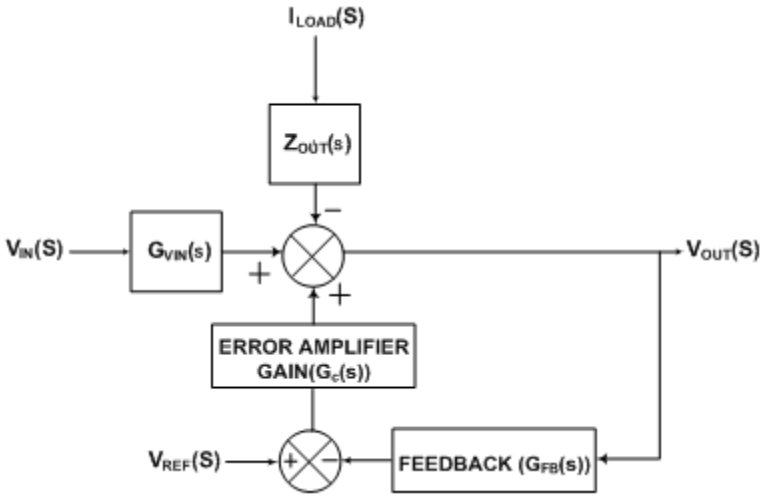

Figure 3.5 Closed loop control block diagram of LDO regulator

The output voltage is given as

$$= \qquad (3.8)$$

Where G_{FB} is the resistive feedback gain and $G_{C(s)}$ is the error amplifier gain and hence $G_{FB}*G_C(s)$ forms the loop gain.

It can be seen from the Equation 3.8 that disturbances of the input and output are attenuated by a factor [47].

The impact of the load/supply transients can be subsided if the corresponding influence is pushed beyond the unity gain frequency. This closed loop settles as '$V_{DC} = A_V$ x $(1-e^{t/\tau})$' with an initial drop of '$A_V = I_{LOAD}(s)$ x $Z_{OUT}(s)$' for the load variations. Similar argument can be applied to line variations. The LDO loop response time should be smaller relative to the rise and fall time of the load transients.

The maximum load that a DDR3 memory takes may rise up to 100mA as it gets loaded by eight data lines [48] per each data lane which is properly terminated for maximum data transfer rate along with differential clock. The overshoots and under shoots are to be kept within 10% to 15% of the supply which amounts to be around 200mV.

The settling time requirement is critical in the event of undershoot i.e. when load changes from low to high. This is justified from the fact that signal swing will be minimum under this condition and the receiver cannot detect the data change. The LDO should get settled within the duration of preamble sequence of the DDR3 memory. The duration of a 500bit preamble sequence can be 500ns with 1Gbps data rate. This requires the under shoot settling time to be of the order 300ns. It may be noted that the regulator supplies average current only while the switching current is taken care by the decap capacitor.

3.9 Temperature Drift

The input offset voltage of the regulator is influenced by the temperature effects of the components. The residue effects of temperature variations on the reference voltage are established at the output voltage through the closed loop gain A_{CL}. The performance parameter that measures the impact of temperature on the output is temperature coefficient T_C is given in Equation 3.9.

$$T_C = \qquad (3.9)$$

Where is the temperature affected voltage reference and is the change in the input offset voltage. This shows that a temperature independent reference voltage and a reduced input offset voltage are the factors that determine the temperature drift performance of regulator.

3.10 Power Supply Ripple Rejection

The power supply ripple rejection is the ability of a regulator to provide a constant output against low and high frequency small signals. The power supply rejection ratio(PSRR) measurement has gained importance due to the system integration of analog and digital blocks

on System on Chip(SoC). As shown in Figure 3.6, the pass transistor transmits the input voltage to the output which are undesirable for regulation. The error amplifier also plays a role in transmitting its own ripple to the output through the pass transistor. A higher error amplifier gain reduces the amount of ripple coupled to the output and thereby better power supply rejection.

The high precision applications require a bandgap reference circuit reference voltage with good power supply rejection ratio. The error amplifier dominates the LDO frequency response at low frequencies forcing the response to fall beyond the dominant pole till unity gain frequency. The ripple rejection at higher frequencies is attributed to the output capacitor.

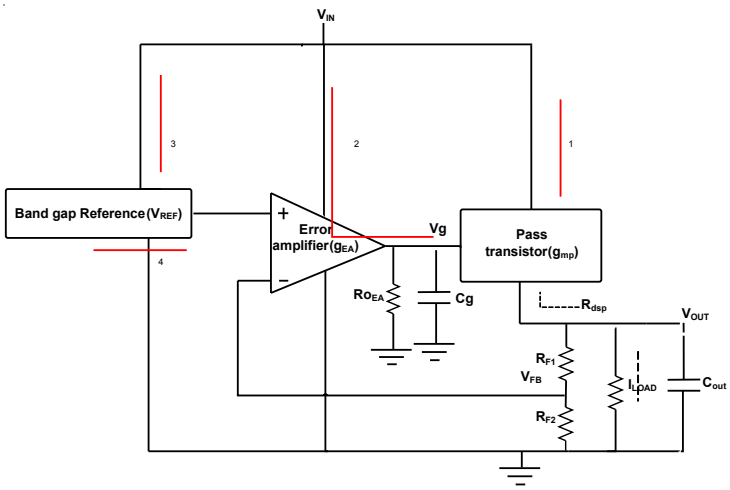

Figure 3.6 Regulator Power Supply Rejection Ratio

Power supply rejection ratio is calculated through two transfer functions $A_s(\omega)$ and $A_{loop}(\omega)$ where $A_s(\omega)$ represents the gain transfer function between supply and output and $A_{loop}(\omega)$ represents the open loop transfer function between input node to the output. The power supply rejection ratio is represented as given in Equation 3.10.

$$PSRR(\omega)= 20 \log[A_{loop}(\omega)/A_s(\omega)] \text{ dB} \quad (3.10)$$

It is discerned from the Equation 3.10 that power supply rejection ratio is increased as the $A_s(\omega)$ decreases and $A_{loop}(\omega)$ increases.

An LDO that has PSRR= -50dB, Frequency= 1MHz, Input ripple = 1mV, it can attenuate a 1mV at this frequency to just 3.16 μV at the output.

3.11 Output current

The output current specifications notify the range of load currents for which the regulation is assured, worst case short circuit current. The suitable conditions under which these ranges are plausible include input voltage, output voltage and the ambient temperature which also determines the regulators break down

Chapter 4

Adaptively Biased Capacitor-less Low Dropout Regulator with Improved Transient Performance

4.1 Introduction

The literature survey reveals that the significant parameters that influence the performance of the LDO regulator used for mobile applications include quick response to fast load transients, regulation and power supply rejection. In this chapter, an improved folded cascode error amplifier-based topology for LDO regulator is analyzed with the help of appropriate transfer function and found that the performance can be improved by making the biasing of error amplifier adaptive to load transients. In this direction, a topology for LDO that employs a modified error amplifier circuit along with quick response augmentation segment to improve transient response as compared to [23] is presented in this chapter.

4.2 LDO Voltage Regulator with Simple Folded Cascode Error Amplifier

~~Topologies of Capacitor Free LDR~~

~~The different possibilities of error amplifier structures that are involved in the capacitor less LDR are examined. The parameters that influence the performance of LDR are explored and analyzed. It is attempted to improve the performance of error amplifier without compromising area and power consumption.~~ The block diagram of LDO voltage regulator with simple folded cascode architecture for error amplifier [44], [49] is shown in Figure 4.1. The error amplifier of the LDO voltage regulator should be designed with sufficiently large gain to meet the regulation requirements. The conventional LDO voltage regulator(CONV_LDO) with simple folded cascode error amplifier topology offers reasonably good gain for better regulation while optimizing the overdrive.

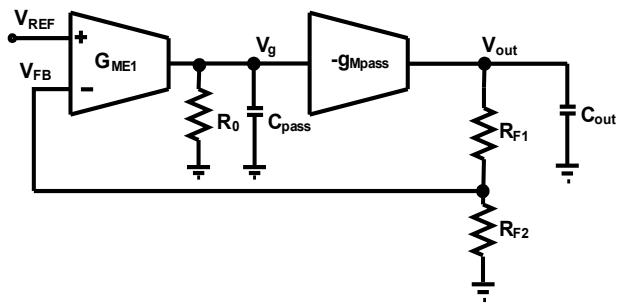

Figure 4.1 Block diagram of CONV_LDO regulator w/o compensation

The following section 4.2.1 reveals the corresponding stability aspects that facilitates to explore further improvement in the performance of LDO voltage regulator for Mobile and DDR3 IO applications.

1.1.1 Stability Analysis of CONV_LDO

The stability of the topology is analyzed with the help of the small signal equivalent circuit shown in Figure 4.2. The dominant pole is formed by error amplifier output node Vg in association with the effective pass transistor gate capacitance C_{pass}. Thus, the LDO regulator output pole becomes non-dominant. At larger load currents output pole moves away from the dominant pole which improves the stability of the system. However, at lower load currents this non-dominant pole moves closer to the dominant pole making the system unstable. This prompts an appropriate compensation for better stability over the load range.

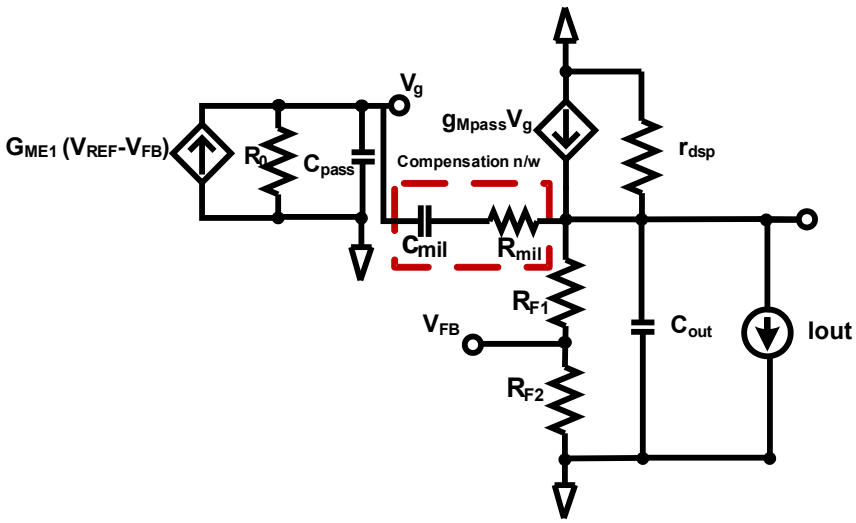

Figure 4.2 Small-signal equivalent circuit of CONV_LDO Regulator

Accordingly pole splitting through compensation network C_{mil} and R_{mil} is shown in the Figure 4.2 that splits the two poles apart while introducing additional zero as given in the Equations 4.1 through 4.3. Figure 4.3 shows the block diagram of LDO voltage regulator with miller compensation [50] and the corresponding schematic is depicted in Figure 4.4. The addition of the miller capacitance effectively pushes the dominant pole further towards the origin increasing the separation between the poles which in turn improves the stability. The corresponding transfer function T(s) and Gain Bandwidth product are given in the Equations 4.4 and 4.5 respectively.

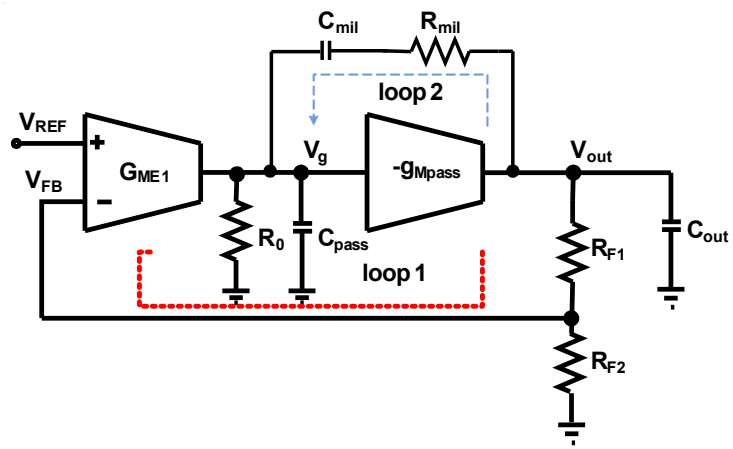

Figure 4.3 Block diagram of CONV_LDO Regulator with compensation

Error amplifier (transconductance G_{ME1}), pass transistor M_{pass} (transconductance g_{Mpass}) and feedback network (R_{F1}, R_{F2}) form loop1 while loop2 constitutes the Miller capacitor (C_{mil}) and Miller resistance (R_{mil}) connected across pass transistor M_{pass}.

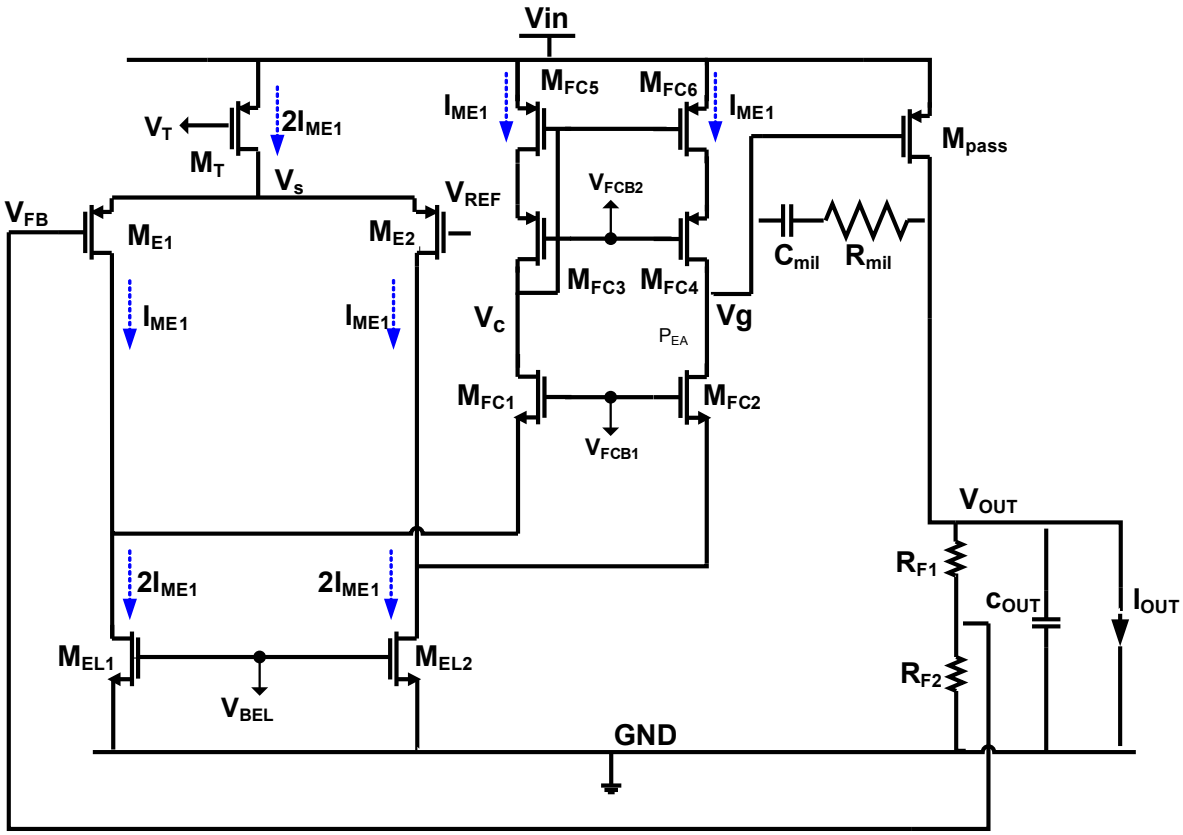

Figure 4.4 Schematic of CONV_LDO regulator

$$P_{EA} = -\frac{1}{R_0\left(C_{pass} + C_{mil} g_{Mpass} R_{out}\right)} \tag{4.1}$$

$$P_{out} = -\frac{g_{Mpass} + \frac{1}{R_{out}}}{C_{out} + C_{pass}} \alpha \sqrt{I_{out}} \tag{4.2}$$

$$z_1 = -\frac{1}{\left(R_{mil} - \frac{1}{g_{Mpass}}\right) C_{mil}} \tag{4.3}$$

$$T(s) = \frac{BG_{ME1} R_0 g_{Mpass} R_{out} \left(1 + \frac{s}{z_1}\right)}{\left(1 + \frac{s}{P_{EA}}\right)\left(1 + \frac{s}{P_{out}}\right)} \tag{4.4}$$

$$GBW = \frac{BG_{ME1}R_0 g_{Mpass}R_{out}}{R_0\left(C_{pass} + C_{mil}g_{Mpass}R_{out}\right)} \tag{4.5}$$

It can be seen from the transfer function *T(s)* that the DC gain i.e. $BG_{ME1}R_0g_{Mpass}R_{out}$ is a function of the transconductance of the error amplifier. Where *B* is the resistive feedback ratio, P_{out} is the output pole, Z_1 is zero and P_{EA} is the pole at the error amplifier output node. G_{ME1} and R_{out} are the transconductance and output resistance of error amplifier respectively. The pass transistor transconductance is g_{Mpass} and R_{out} is the output resistance of the LDO regulator. The requisite compensation capacitance C_{mil} can be obtained from the Equations 4.6 through 4.8. Phase margin(PM) PM is given in Equation 4.6. Where W_u is the unity-gain frequency and P_{nd} is the non-dominant pole. Minimum separation(T_{PM}) between non-dominant pole P_{nd} and unity gain frequency W_u is given by Equation 4.7.

$$PM = 90^0 - \arctan\frac{(w_u)}{(p_{nd})} \tag{4.6}$$

$$T_{PM} = \frac{p_{nd}}{w_u} = \frac{\left(\dfrac{g_{Mpass} + \dfrac{1}{R_{out}}}{C_{out} + C_{pass}}\right)}{\left(BG_{ME1}R_0 g_{Mpass}R_{out}\right).\left(\dfrac{1}{R_0\left(C_{pass} + C_{mil}g_{Mpass}R_{out}\right)}\right)} \tag{4.7}$$

Minimum T_{PM} is obtained by differentiation of Equation 4.7 with $g_{Mpass,}$ resulting in Equation 4.8. The miller capacitance C_{mil} is selected accordingly from the following Equation 4.8.

$$T_{PM\min} = \sqrt{\frac{C_{out}}{C_{mil}}} \times \frac{1}{R_{out}} \tag{4.8}$$

1.1.2 Results and Discussion

The stability of the circuit for a range of load currents is demonstrated in the Figure 4.5. As mentioned earlier the phase margin at high load currents is better than the that of lighter loads. Corresponding transient response is shown in Figure 4.6.

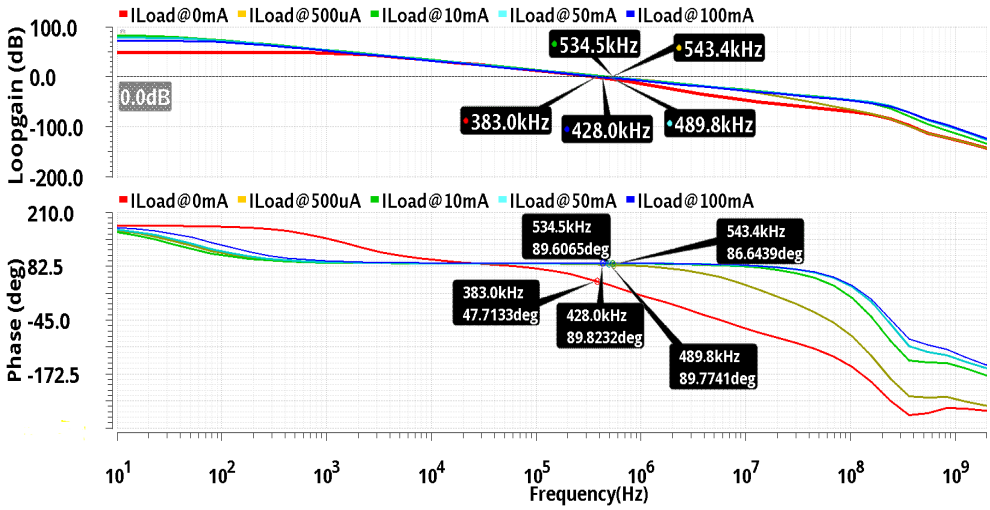

Figure 4.5 Loop Gain and Phase response for load currents from 0 to 100mA for CONV_LDO Regulator

The transient response shown in Figure 4.6 demonstrates the role of compensation network (R_{mil} and C_{mil}) in reducing undershoot to 446.5mV with settling time of 3.03µs from an uncompensated value of 698.1mV with settling time 2.74µs. The slight increase in the settling time in the compensated case is due to the decreased unity gain frequency with miller network.

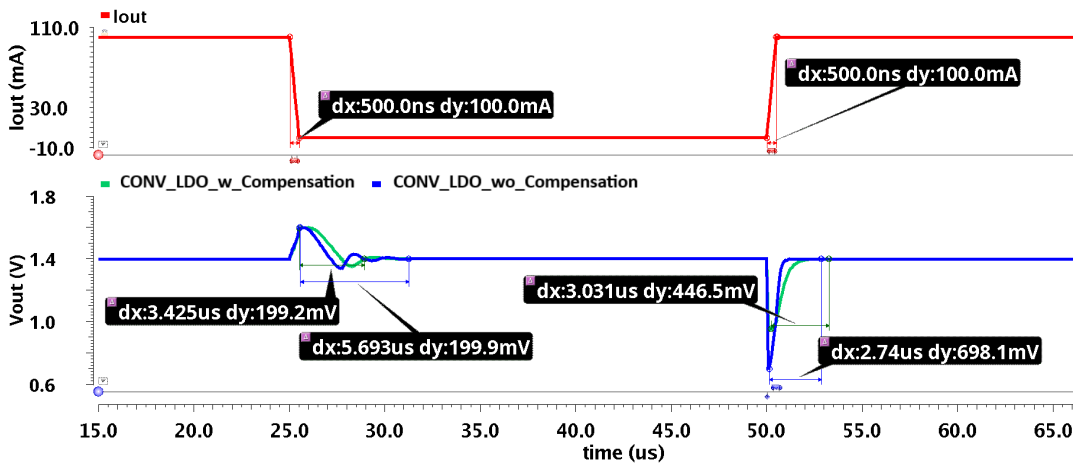

Figure 4.6 Transient response of CONV_LDO regulator

It can be seen from the above observations that there is a trade-off between transient response and stability of the LDO voltage regulator. However, for the portable applications including power supply for DDR3 IO etc. there is a necessity to improve the transient response further. This prompts one to explore the possibility of improving the transient response without compromising much on the stability. This objective can be fulfilled if the error amplifier can be made more sensitive in response to the load transients. Towards this end an appropriate topology is to be chosen for the error amplifier that does the needful with minimal impact on the stability.

4.3 LDO voltage Regulator with Improved Folded Cascode Error Amplifier

The error amplifier based on improved folded cascode structure [51] could be employed in the LDO voltage regulator [52], [53] to improve the performance as compared to that of conventional simple folded cascode amplifier without consuming additional quiescent current but with enhanced transconductance. This section analyzes LDO regulator with more stringent load requirements as compared to [52], [53]. The block diagram and the corresponding schematic are shown in Figure 4.7 and Figure 4.8.

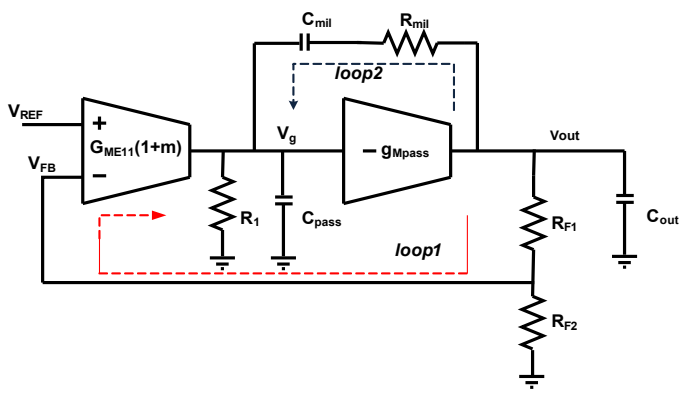

Figure 4.7 Block diagram of IFC_LDO regulator

The improved folded cascode LDO(IFC_LDO) voltage regulator schematic is shown in Figure 4.8. The split driving transistors (M_{E11}, M_{E12}, M_{E21}, M_{E22}) and corresponding disproportionate mirrored load (M_{EL11}, M_{EL12}, M_{EL21}, M_{EL22}) support a large bias current during

DC conditions while act as driving elements for ac signal under transients which lead to improved transconductance as compared to that of simple folded cascode.

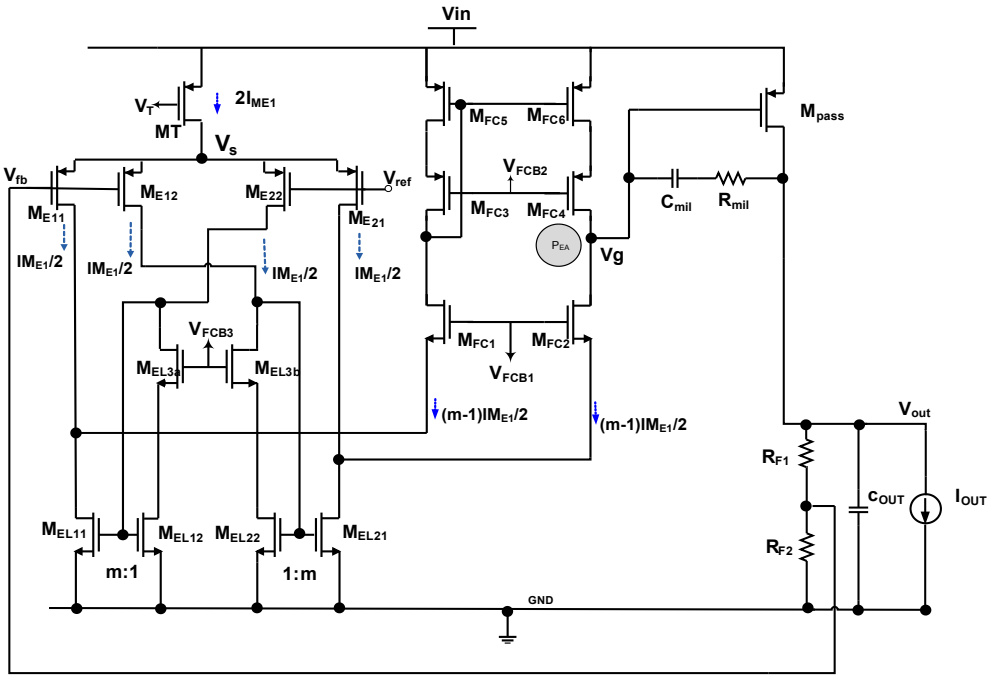

Figure 4.8 Schematic of IFC_LDO regulator

1.1.3 Stability Analysis of IFC_LDO

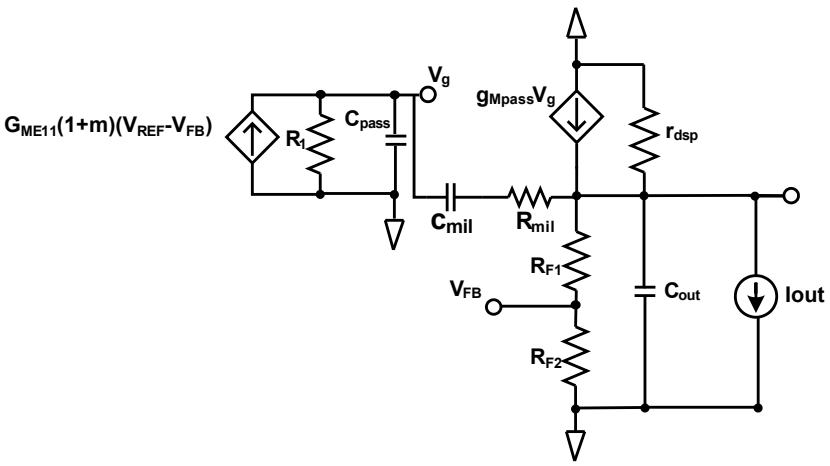

Figure 4.9 Small signal equivalent circuit of IFC_LDO

The stability of IFC_LDO is analyzed by the transfer function *T(s)* given in Equation 4.9 which is derived from the small signal equivalent circuit given in Figure 4.9. By virtue of current mirror transistors effect the transconductance of the error amplifier is (1+m) times the

G_{ME11}. For a suitable selected value of m=3 the resultant transconductance becomes twice (theoretically) to that of error amplifier of conventional simple folded cascode LDO regulator.

$$T(s)=\frac{BG_{ME11}(1+m)R_0 g_{Mpass}R_{out}\left(1+\frac{s}{z_1}\right)}{\left(1+\frac{s}{P_{EA}}\right)\left(1+\frac{s}{P_{out}}\right)} \quad (4.9)$$

1.1.4 Results and Discussion

It is observed from the transfer function Equation 4.9, the gain bandwidth product of IFC_LDO is approximately twice that of CONV_LDO due to increased transconductance obtained through simulation is exhibited from the transconductance plots in Figure 4.10.

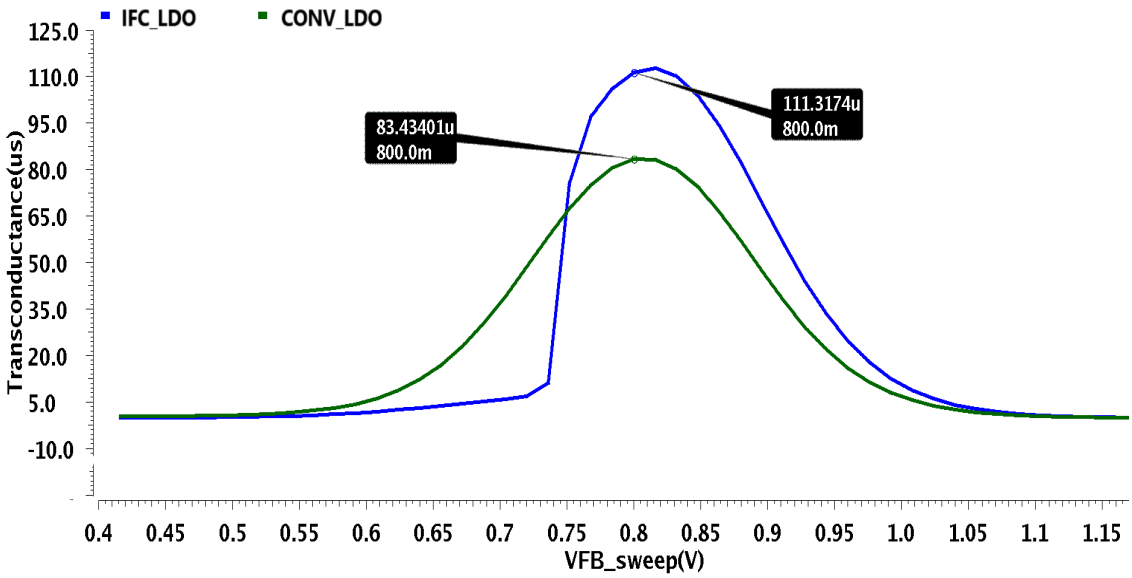

Figure 4.10 Transconductance of CONV_LDO and IFC_LDO

The Frequency response for CONV_LDO and IFC_LDO for a load current variation of 0mA and 100mA is plotted in Figure 4.11. It is observed from the plots that gain has increased from 72.98dB (CONV_LDO) to 79.51dB (IFC_LDO) for the case of 100mA, while unity gain frequency has increased from 428.1kHz to 856.90kHz. This improvement in the unity gain frequency is attributed to the deliberate attempt to improve the transconductance for better transient response as discussed earlier. However, it led to slight degradation in the phase margin at no load(zero) current.

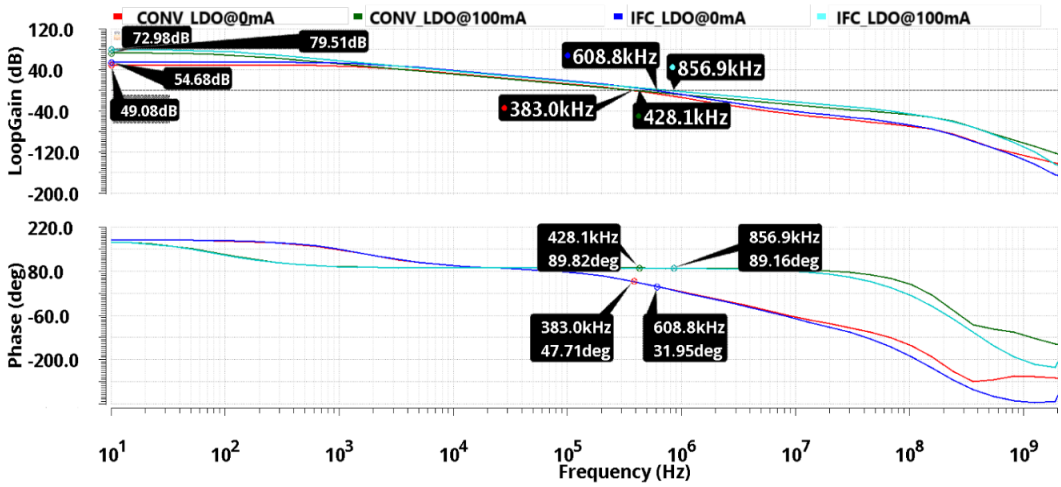

Figure 4.11 Loop gain and phase response of CONV_LDO and IFC_LDO

The stability of the topology is accessed from the loop gain and phase response plot for different load currents viz. 0mA, 500µA, 10mA, 50mA, and 100mA as depicted in Figure 4.12. The phase margin at no load current is 31.95^0 while it is 89.16^0 for 100mA load current.

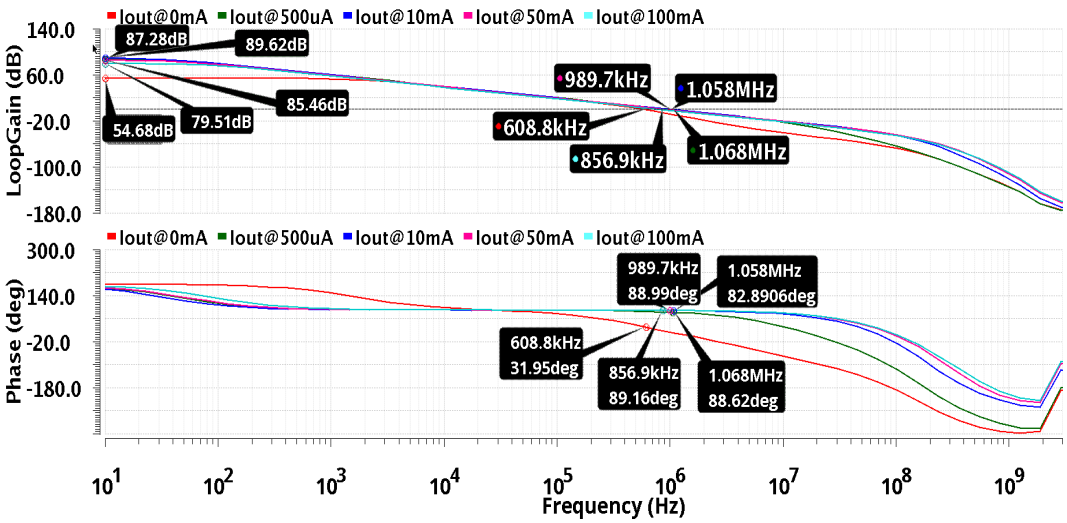

Figure 4.12 Loop gain and phase response of IFC_LDO for load current from 0 to 100mA

The Transient response of IFC_LDO regulator and CONV_LDO regulator is plotted in Figure 4.13 for a load current variation of 0 and 100mA with a rise and fall time of 500ns suiting to the portable applications including DDR3 IO as against 1µs in [52], [53] .

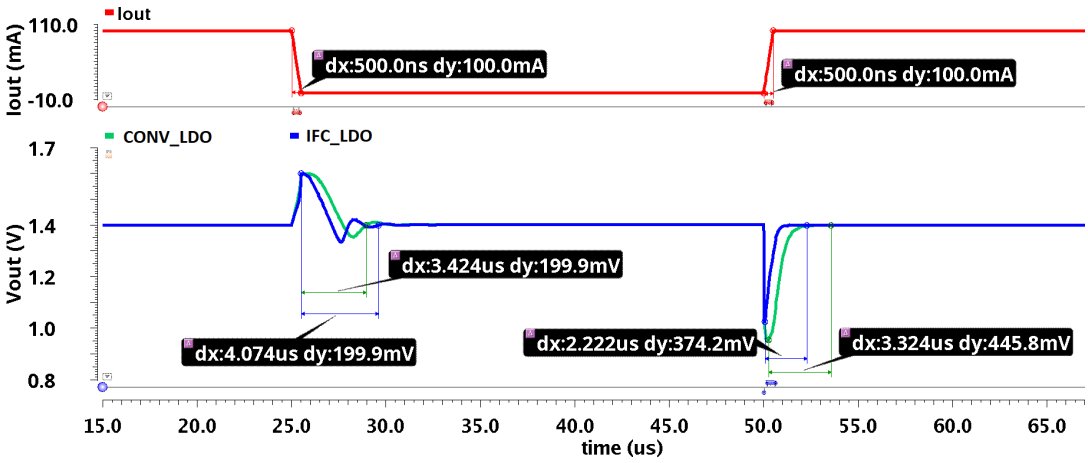

Figure 4.13 Transient response of IFC_LDO and CONV_LDO for 0 to 100mA load transient in 500ns

It is observed that for a load transient of zero to 100mA undershoot reduces from 445.8mV (CONV_LDO) to 374.2mV (IFC_LDO) with a reduced settling time from 3.32µs (CONV_LDO) to 2.22µs (IFC_LDO). The overshoot settling time reduces from 4.07µs(CONV_LDO) to 3.424 µs(IFC_LDO).

The transient currents of error amplifier (I_{MFC4} through transistor M_{FC4}) and the voltage V_g of the pass transistor corresponding to CONV_LDO and that of IFC_LDO are shown in the Figure 4.14. The voltage changes occurring at the gate of pass transistor is attributed to the current transients of error amplifier due to load variations. It can be observed that IFC_LDO could respond quickly to the load changes as compared to that of conventional one.

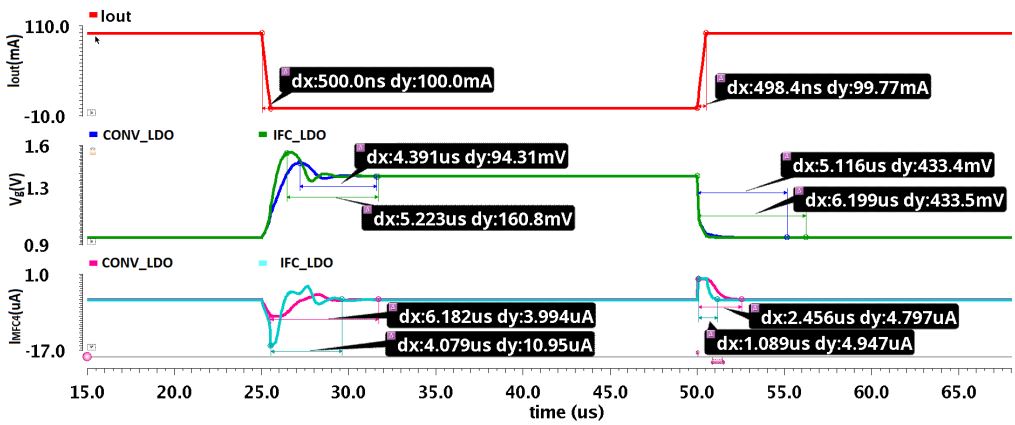

Figure 4.14 Current I_{MFC4} and the voltage V_g at the gate of pass transistor

The improvement in the performance of IFC_LDO as depicted above can be attributed mainly to the deliberate effort made to improve transconductance through appropriate mirroring. An attempt to improve transconductance further by increasing mirror ratio "m" degrades phase margin and hence stability due to the movement of associated parasitic poles inside the unity gain frequency.

Alternately, transconductance can be improved by choosing large bias currents [54] for the error amplifier making it a power monger circuit. In addition, it forces the gate voltage of differential pair to be small, thereby limiting the input common mode range (ICMR).

The other alternative to improve transconductance without increasing the bias current is to use large input PMOS transistors which may drive them into sub-threshold region during transients affecting transient response. This stimulates one to explore alternate solutions to improve performance of the LDO as discussed in the subsequent section.

4.4 LDO Voltage Regulator with Load Tracking Bias

This section deals with an alternate approach to circumvent the limitations of IFC_LDO regulator architecture as observed in the previous section. This work presents an LDO that modifies the improved folded cascode structure with fixed bias discussed above by employing the flipped voltage follower adapting the bias [23] to track the load changes. This adaptation increases the transconductance of the error amplifier improving the overall performance of the LDO than that of IFC_LDO regulator with a marginal penalty of additional bias current.

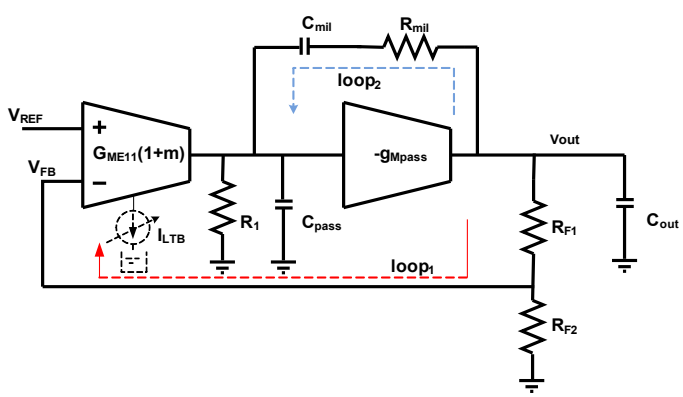

Figure 4.15 Block diagram of Load Tracking Bias LDO regulator

The block diagram of the load tracking bias LDO is shown in Figure 4.15. The load tracking bias current I_{LTB} of the error amplifier as a function of differential voltage (V_{REF}-V_{FB}) enhances transconductance that improves DC gain, gain bandwidth product and transient response of the regulator.

1.1.5 Circuit Design and Analysis

The schematic of Load Tracking Bias LDO regulator(LTB_LDO) is shown in Figure 4.16. The slew rate drive required at the gate of pass transistor is limited by the bias current $2I_{ME1}$ for conventional differential pair. An attempt is made to improve the slew rate by modifying the tail current of the differential amplifier corresponding to the fixed bias IFC_LDO using a flipped voltage follower [55].

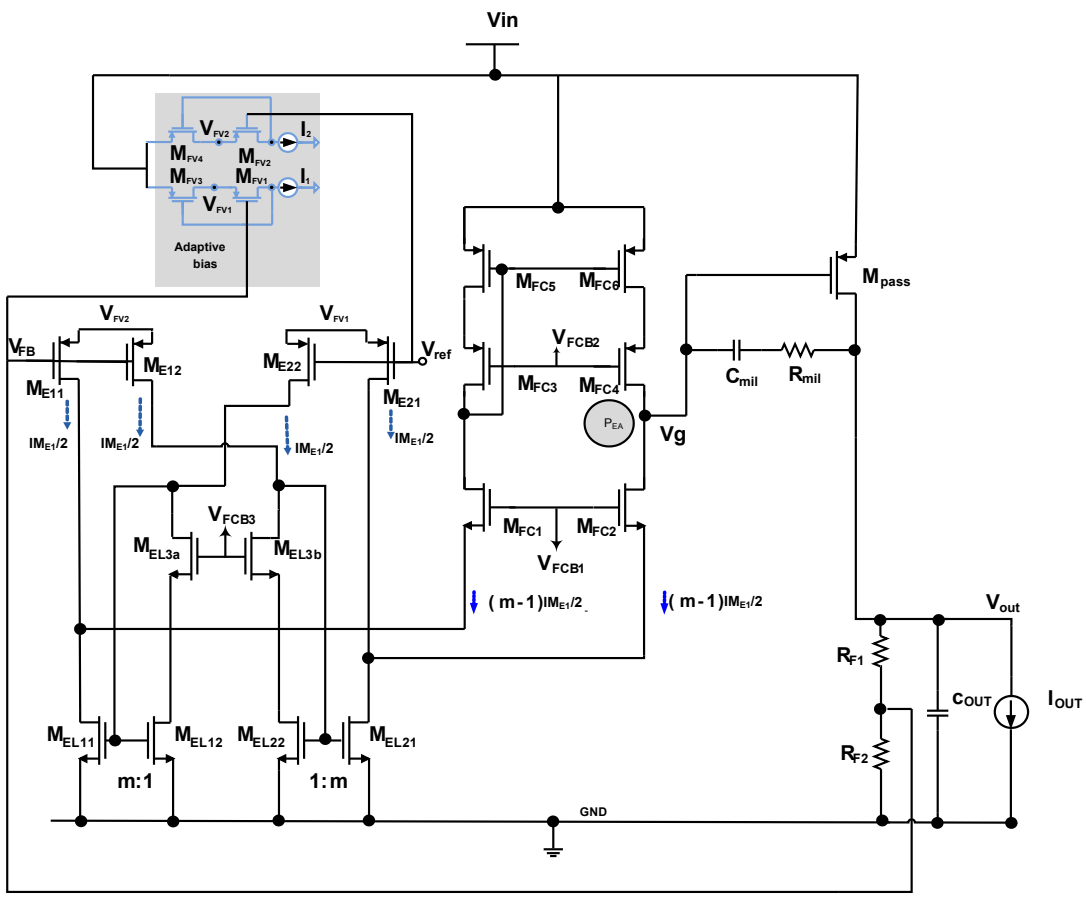

Figure 4.16 Schematic of Load Tracking Bias LDO regulator

The differential pair transistors are cross coupled with level shifters (M_{FV3}, M_{FV1}, I_1) and (M_{VF4}, M_{VF2}, I_2) facilitate load tracking bias. During steady state each transistor of differential pair carries same quiescent current. During load transient, undershoots at the output decrease the feedback voltage applied at the gate of (M_{E11}, M_{E12}) which further decreases the source voltage of (M_{E21}, M_{E22}) while the source voltage of (M_{E11}, M_{E12}) is at a constant value. Therefore, the drain current of (M_{E11}, M_{E12}) increases whereas the current through (M_{E21}, M_{E22}) decreases. The increased drain current is larger than quiescent current [56] exhibiting class AB operation which is proportional to the load transient.

The differential drain currents variation as a function of voltage V_{FB_sweep}(V_{FB}-V_{REF}) for CONV_LDO and LTB_LDO regulator is shown in Figure 4.17. It is observed from the plots that the difference current for LTB_LDO regulator is large thereby contributing to increase in the slew rate at the gate of the pass transistor by an order of two while compared to CONV_LDO and for a same change in the differential voltage applied.

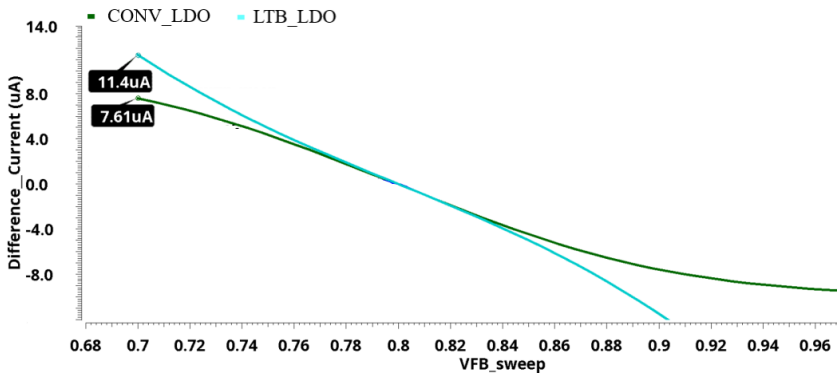

Figure 4.17 Differential currents of LDO regulators with V_{FB_sweep} voltage

Pass Transistor design

A pass transistor is designed using the specifications and process parameters tabulated in the following Table 4.1.

Table 4.1 Circuit and Process parameters

Circuit Parameters	Specification	Process parameter	Value
Input voltage ()	1.6	Threshold Voltage ()	-0.455
Output voltage ()	1.4	PMOS Tansconductance ()	60

Load current ()	100mA	PMOS Length(L)	180nm
Dropout Voltage (	200mV	NMOS Tansconductance ()	300

The PMOS pass transistor M_{Pass} is sized as given by the Equation 4.10.

$$V_{DROPOUT} <*=< 200mV \quad (4.10)$$

>

Length of the pass transistor is chosen minimum i.e. 180nm so that =

Error Amplifier Design

The error amplifier is designed with the following specifications. Circuit parameters are given in the Table 4.2.

Table 4.2 Error amplifier specifications

Circuit parameter	**Specification**	**Circuit parameter**	**Specification**
Input voltage ()	1.6V	Maximum Load current ()	100mA
Output voltage ()	1.4V	Load regulation	<20μV/mA
Dropout voltage ()	0.2V	Power consumption ()	<120μW

Since the reference voltage (V_{REF}) and output voltage(V_{out}) are related to each other by Equation 4.11

$$== \quad (4.11)$$

$$\text{So, } 0.6=0.8 \quad (4.12)$$

The 20μA bias current is chosen for the feedback resistive network such that it ensures a minimum sub-threshold current during worst case conditions and operates under extreme temperature and process corners.

So, = = 70kΩ (4.13)

Solving Equation 4.12 and 4.13 gives

=30k and 40k

The regulator output resistance R_{out} is given by Equation 4.14

R_{out} (4.14)

The load regulation is related to output resistance loop gain and feedback factor β through Equation 4.15.

Load regulation = (4.15)

The drop across the pass transistor is related to the dropout voltage and maximum load current by = =2 Ω.

As the loop gain >> 1 and assuming a worst case of unity feedback and considering the load regulation specification of 0.021 and substituting the values of and we get

Loop gain

The loop gain (comprises of error amplifier loop gain and pass transistor loop gain . So,

100dB= => 100dB= =>

The transient response of the regulator is related to the output voltage by Equation 4.16.

(4.16)

Where [16]

The output is desired to be below 100mV and settle below 1μs. Hence settling time related to the closed loop bandwidth as

i.e >1MHz so a minimum bandwidth of 1MHz is selected.

The unity gain frequency of error amplifier is given by , where C_g is the gate capacitance

=2π23.14=125.6 μA/V

The power consumption, total current and minimum supply voltage are related by

P= * V_{line} < 120μW, < 75μA

Minimum bias current for error amplifier is chosen by taking into account maximum load transient and consequent slewing limit while its maximum is bounded by power dissipation limit.

Accordingly, the quiescent current of 20 μA suffices to meet above limitations. The input differential pair transistor transconductance is obtained by

125.6*= =>

Then the transistors M_{E11} and M_{E12} each have a transconductance of

The length of transistor is selected such that it minimizes short channel and mismatch effects. The transistors M_{EL11}, M_{EL12} and M_{EL21}, M_{EL22} are sized in such a way that mirroring is done three times (2.5μA:7.5μA) in order to obtain the desired transconductance while trading with power consumption and phase margin. The transistor at the output stage of error

amplifier is designed for a good swing at the same time contributing to large output resistance.

The transistors M_{FC4} and M_{FC8} in the folded arm of error amplifier carrying a current of 5µA are applied an appropriate overdrive voltage (150mV) such that maximum possible swing available at the gate of error amplifier i.e V_{in}-0.3V.

Appropriate overdrive voltage of 150mV is applied for the transistors M_{FC4} and M_{FC8} carrying a current of 5µA in the folded arm of error amplifier, ensuring a maximum possible swing (i.e V_{in}-0.3V) at the gate of pass transistor. Transistors M_{FC2} and M_{EL21} are sized in the similar lines which allows a minimum swing of 300mV from ground.

The aspect ratio of transistor M_{FC3}, M_{FC4}, M_{FC5}, M_{FC6} is given by

=150*

= 150* =>

For the transistors M_{FC2} and M_{EL21}

=150*

= 150*=>

The load tracking bias sub section (transistors M_{FV3}, M_{FV1} and I_1) is designed as follows:

The output voltage swing at the node V_{FV1} is bounded by expression

$$V_{SGM_{FV3}}+V_{tp}<V_{FV1} < V_{SGM_{FV3}}+ V_{SDM_{FV1}}$$

Further, the output voltage swing at the node Vab1 is calculated from the difference of the extremes leading to

$$V_{MFV1} =V_{tp}-V_{SDM_{FV1}}$$

In order to increase the output swing, the swing across $V_{SDM_{FV1}}$ should be as small as possible. But, reducing $V_{SGM_{FV1}}$ towards this end pushes M_{FV1} in to sub-threshold region. To avoid it, the following condition must be satisfied

$$V_{SGM_{FV1}} - V_{tp} > nkt/q$$

Where the value of n typically lies in the range 1<n<3 and kt/q is the thermal voltage (26mV at room temperature). An Overdrive voltage ($V_{SGM_{FV1}} - V_{tp}$) is chosen 150mV considering the worst case i.e. n=3 with appropriate margin. A bias current of 2.5µA is considered as the branch current of M_{FV3}-M_{FV1}-I_1 and thus aspect ratio for M_{FV1} is calculated as

$$150mV = => =$$

The transistor M_{FV3} is sized in similar lines whose value is 4. From the adaptive biasing section of load tracking bias LDO regulator

$$V_{SGM_{FV3}} = V_{SDM_{FV3}} + V_{SDM_{FV1}}$$

Under quiescent conditions with no transient currents and considering M_{FV1} in saturation, transistor M_{FV3} will be in saturation if

$$V_{SDM_{FV3}} = V_{IN} - (V_{FB} + |V_{tp}|_{M_{FV1}} +) - V_{FB} >$$

Where V_{FB} is the feedback voltage, I_1 is the quiescent current of the adaptive biasing stage. Similarly, the saturation condition for M_{FV3} is given by

$$V_{SGM_{FV1}} - V_{SDM_{FV1}} = -- <$$

Therefore, limitations on feedback voltage is given by the following Equation 4.17

$$+<-<++ \qquad (4.17)$$

The current I_1 is chosen such that it satisfies the boundary limits of Vin-V_{FB}. Thus the above Equation 4.17 sets limitations on the feedback voltage and hence the permissible load transients.

1.1.6 Stability Analysis

The frequency response of Load Tracking bias LDO regulator is shown in Fig. 4.18 along with that of conventional folded cascade LDO and improved folded cascode LDO regulator. It can be seen from Figure 4.18 that there is an improvement in dc gain i.e. 85.17dB (LTB_LDO) as compared to 72.98dB (CONV_LDO). Also, unity gain frequency is improved to 1.679MHz (LTB_LDO) against the corresponding value of 428.1KHz (CONV_LDO). This facilitates faster response to load transients while maintaining almost nearly same phase margin which ensures stability as non-dominant parasitic poles of adaptive bias structure lie well beyond unity gain frequency.

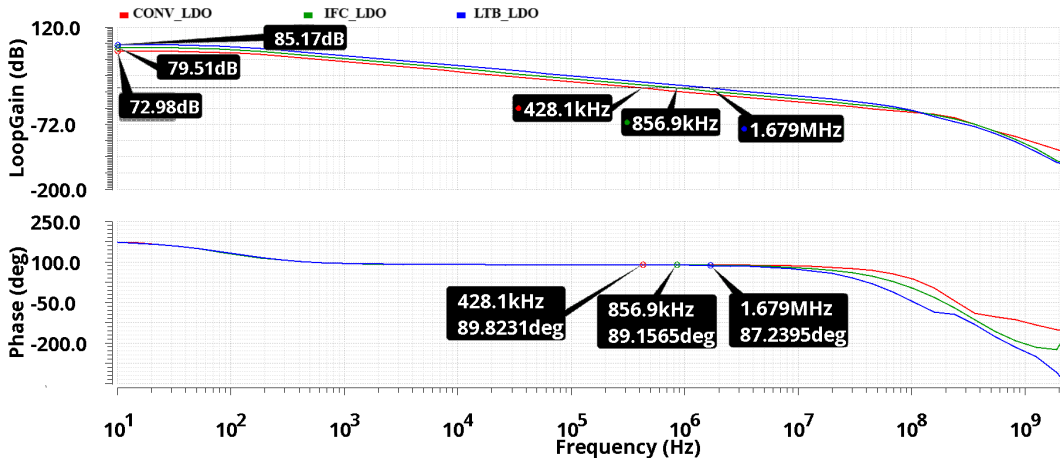

Figure 4.18 Comparison of Loop Gain and Phase responses of CONV_LDO, IFC_LDO and LTB_LDO regulators at load current of 100mA

1.1.7 Results and Discussion

The transient performance of load tracking bias LDO regulator is analyzed with a load transient of zero to 100mA with a rise and fall time of 500ns.

When the load current changes from low to high value, a large undershoot arises in the output voltage which after being sampled by feedback network is applied to the M_{E11}, M_{E12} and

M_{FV1} simultaneously. This varies voltages at the source of M_{E21} and M_{E22} while the flipped voltage follower maintains a constant voltage V_{FV1} at the sources of M_{E11} and M_{E12}. This causes a change in |Vgs| across the M_{E11} and M_{E12} resulting in significant drain current. At the same time |Vgs| of M_{E21} and M_{E22} decrease resulting in smaller currents for M_{E21} and M_{E22}. This current is mirrored to M_{EL11}. The resultant current of M_{EL11} and M_{E11} changes the overdrive of M_{FC1} which in turn gets mirrored through M_{FC3} M_{FC5}-M_{FC6} M_{FC4} pair. Similar action develops current through M_{FC2} which can be expected to be more than that of M_{FC4}. This decreases voltage at node Vg which facilitates pass transistor to source more current as required. Similarly, converse action takes place during load transients from high to low. Corresponding transient response is shown in Figure. 4.19 along with the responses of CONV_LDO and IFC_LDO structures.

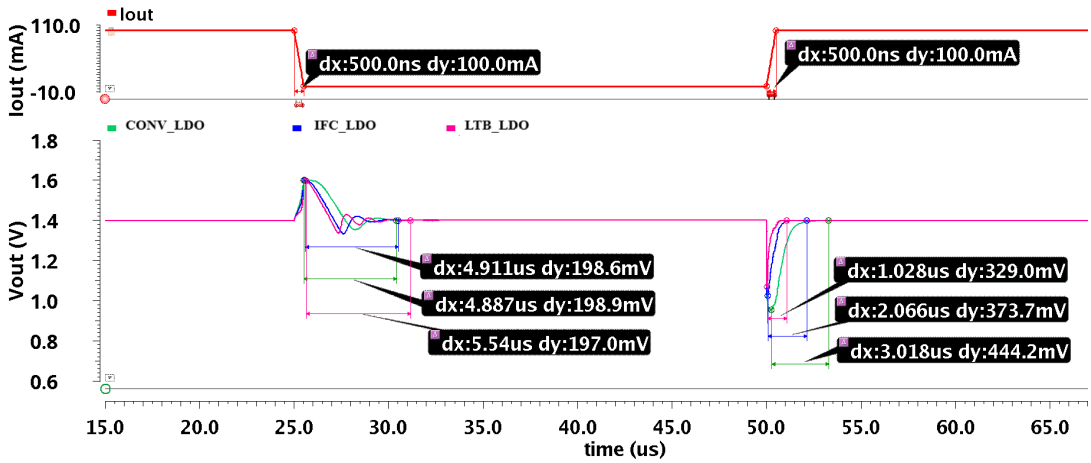

Figure 4.19 CONV_LDO, IFC_LDO and LTB_LDO regulators transient responses for load current variation between 0 and 100mA in 500ns

It is observed from Fig. 4.19 that Load Tracking Bias LDO settles faster within 1.028µs with an undershoot value of 329.0mV while the overshoot reduces to 197mV and settles in 5.54µs. The improvement in transient response for the topology presented is further endorsed by relative comparison of the plots (Figure 4.20) of pass transistor driving current at the output of error amplifier i.e. current (I_{MFC4}) and the corresponding gate voltage Vg for all the three LDO's under consideration. It can be seen that the pass transistor driving current and hence the corresponding gate voltage respond quickly to load transients for the topology presented as compared to the improved folded cascode LDO and conventional simple folded cascode LDO regulator structures.

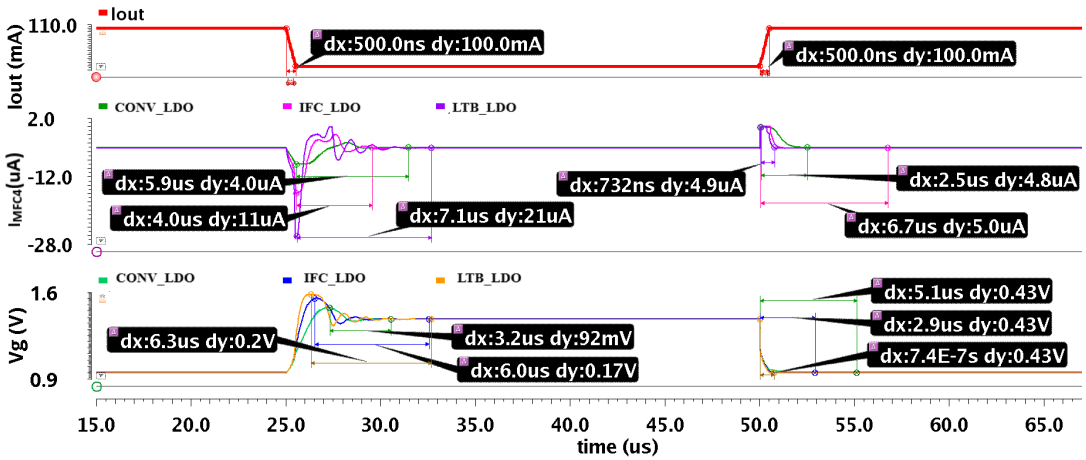

Figure 4.20 Current I_{MFC4} and the voltage Vg at the gate of pass transistor

4.5 Transient Enhanced Load Tracking Bias(TE_LTB) LDO Structure

The transient response improvement due to adaptive biasing is limited by the threshold voltages of the NMOS and PMOS transistors as can be seen from Equation 4.17. Also the latencies involved in the feedback loop further exacerbate the response. To meet the demands of regulation during load transients, a higher value of miller capacitance (C_{mil}) much larger than the gate drain capacitance of pass transistor (M_{Pass}) is required for compensation, so that the coupling between output (V_{out}) and gate of the pass transistor (V_g) is fast. The brute force addition of large capacitor brings RHP zero to lower frequencies degrading stability. So, a solution proposed by [8], [57] is employed as shown in the Figure. 4.21 that provides unidirectional path for quick response without affecting stability at large.

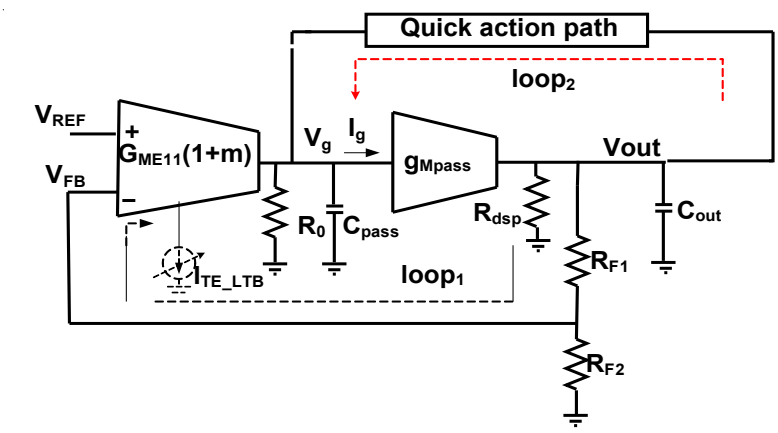

Figure 4.21 Block diagram of TE_LTB LDO voltage regulator

The loop2 in Figure. 4.21 acts as a quick action path such that it facilitates quick change in pass transistor gate voltage (V_g) in response to load transient relative to that of loop1 as required. Care should be taken in such a way that the zeros and poles resulting from additional quick action segment should be kept away from the loop gain bandwidth of main loop so that the stability is not affected.

1.1.8 Circuit Design and Analysis

The Transient enhanced load tracking bias LDO structure have adaptive bias error amplifier and quick action path comprising transistors M_{FP1}, M_{FP2}, M_{FP3} and M_{FP4} along with components R_f and C_f [57] .The quick action path controls the charging and discharging rate of the gate capacitance such that it governs the action of pass transistor M_{pass} to regulate the output voltage (V_{out}). The transient enhanced load tracking bias LDO regulator is shown in Figure. 4.22.

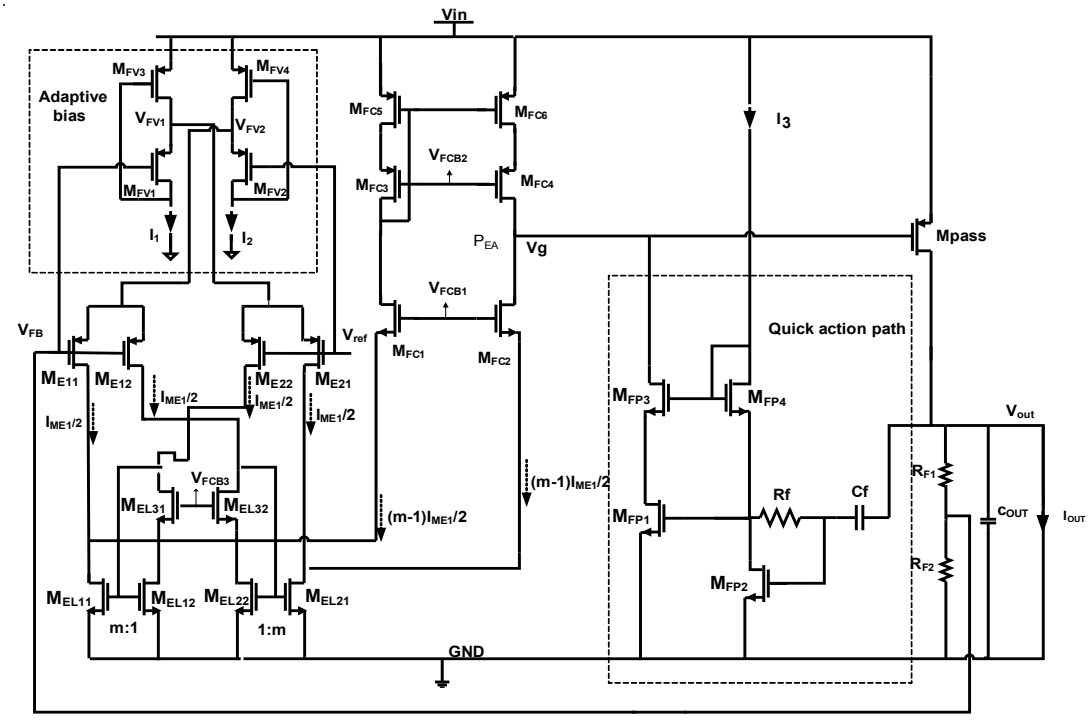

Figure 4.22 Schematic of Transient Enhanced Load Tracking Bias LDO regulator

The quick action path circuit should be designed in such a way that it should replenish the change at the gate of pass transistor (M_{pass}) at a quicker rate. Thus the rate of change of charge at the gate of pass transistor i.e $C_{gs}V_{gs}$ should be equal to the rate of change of charge that

quick action path supplements i.e $C_f dV_{out}$ This amounts to a very large value of the order of 50 nF which can be further scaled down to 500fF by a gain factor of transconductance of quick action path network comprising transistors M_{FP1}- M_{FP4} [57].

1.1.9 Stability Analysis

The transfer function is derived from the small signal equivalent circuit representation of Figure. 4.23.

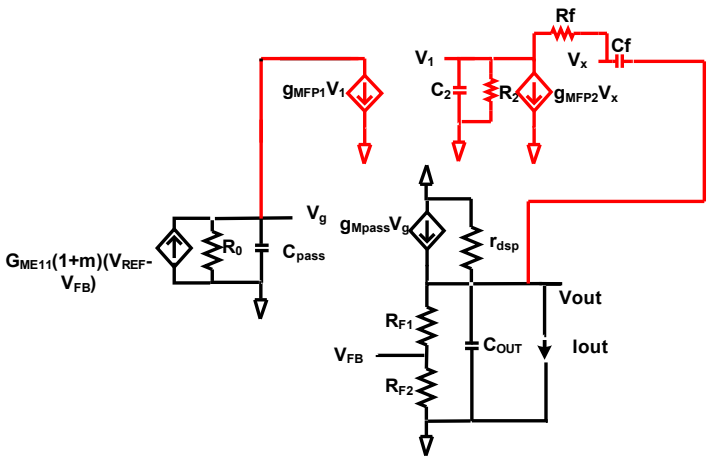

Figure 4.23 Small signal equivalent of TE_LTB LDO regulator

The quick acting path comprises of a RC differentiator that responds swiftly to the load transients and couple of amplifiers for requisite gain and unidirectional response.

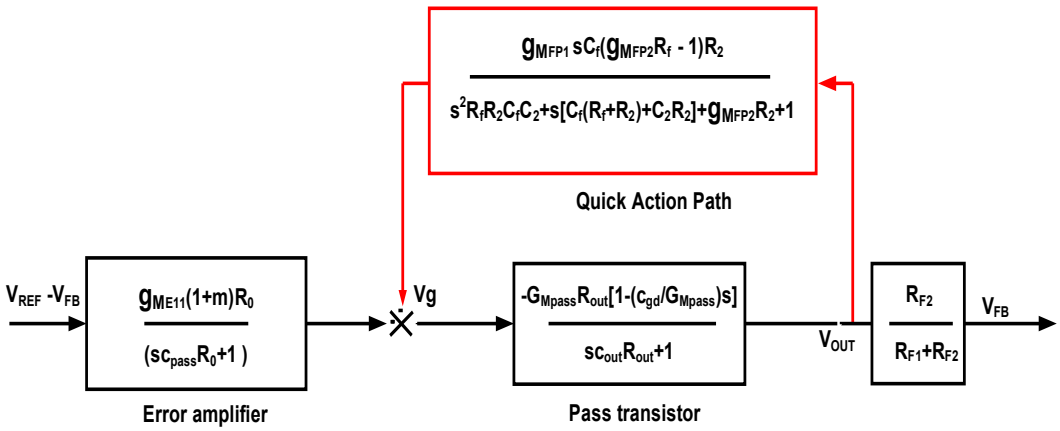

Figure 4.24 Block diagram representation of TE_LTB LDO regulator

It can be seen from Figure 4.24 that the quick action path [57] when applied to the load tracking bias LDO presented earlier results in the following transfer function.

$$T(s)=\frac{G_{ME11}(1+k)R_0G_{Mpass}R_{out}\left(\frac{R_{F2}}{R_{F1}+R_{F2}}\right)\left(1+G_{M_{FP2}}R_2\right)\left(1-\frac{s}{z_1}\right)\left(1+\frac{s}{z_2}\right)\left(1+\frac{s}{z_3}\right)}{\left(1+sc_{pass}R_0\right)\left(\begin{array}{l}s^3\left(C_{out}R_{out}R_fR_2C_fC_2\right)+\\ s^2\left(R_fR_2C_fC_2+\left(C_f\left(R_f+R_2\right)+C_2R_2\right)c_{out}R_{out}+\frac{C_{gd}}{G_{Mpass}}G_{M_{FP1}}R_2C_f\left(G_{M_{FP2}}R_f-1\right)\right)+\\ s\left(C_f\left(R_f+R_2\right)+C_2R_2+GG_{M_{FP2}}R_2c_{out}R_{out}-G_{M_{FP1}}C_f(G_{M_{FP2}}R_f-1)R_2G_{Mpass}R_{out}\right)\right)+G_{M_{FP2}}R_2+1\end{array}\right)}$$

Where z_1 is a Right Half Plane Zero while z_2, z_3 are Left Half Plane Zeros of transfer function. Enough care is taken to push all high frequency zeros and poles to much higher frequency beyond the unity gain frequency while the pole at the pass transistor gate node remains dominant.

$$z1=\frac{g_{Mpass}}{C_{gd}},\ z2=\left[\frac{\left(1+g_{M_{FP2}}R_2\right)}{C_f\left(R_f+R_2\right)+C_2R_2}\right],\ z3=\left[\frac{C_f\left(R_f+R_2\right)+C_2R_2}{R_fR_2C_fC_2}\right]$$

1.1.10 Results and Discussion

Loop gain and phase response of Transient Enhanced Load Tracking Bias LDO regulator for different load currents is shown in Figure 4.25.

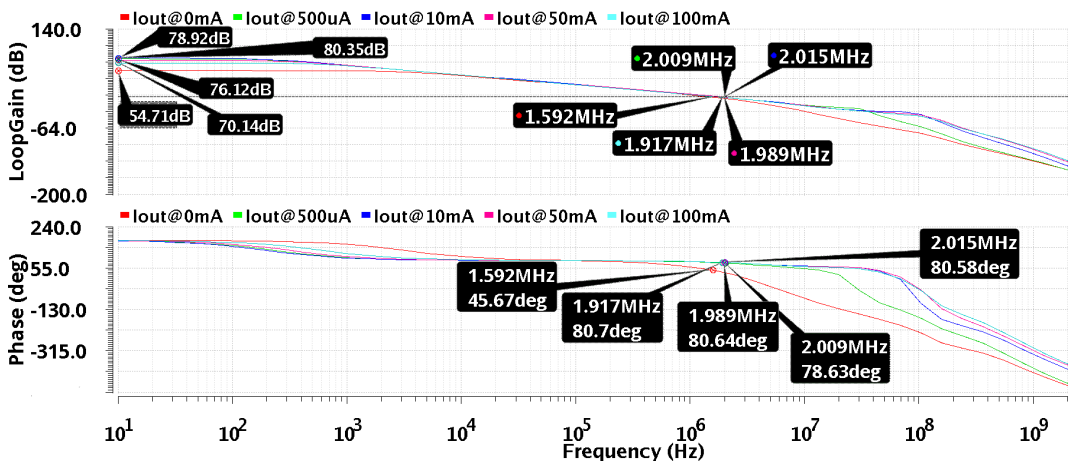

Figure 4.25 Loop gain and phase response of TE_LTB LDO regulator

It is observed from the loop gain and phase response plot that at a load current 100mA the unity gain frequency is 1.917MHz while the phase margin corresponding to it is 80.7^0. The stability of the regulator is critical while operated at lower load currents. At a lower load current of 0mA the phase margin is 45.67^0.

The relative comparison of transient response corresponding to Transient Enhanced Load Tracking Bias LDO regulator against that of the other LDO regulators discussed earlier is depicted in Figure 4.26 which clearly shows the reduction in overshoot/under shoot voltages to 150.1mV/89.95mV along with improvement in the corresponding settling times (1.088µs. and 719ns respectively).

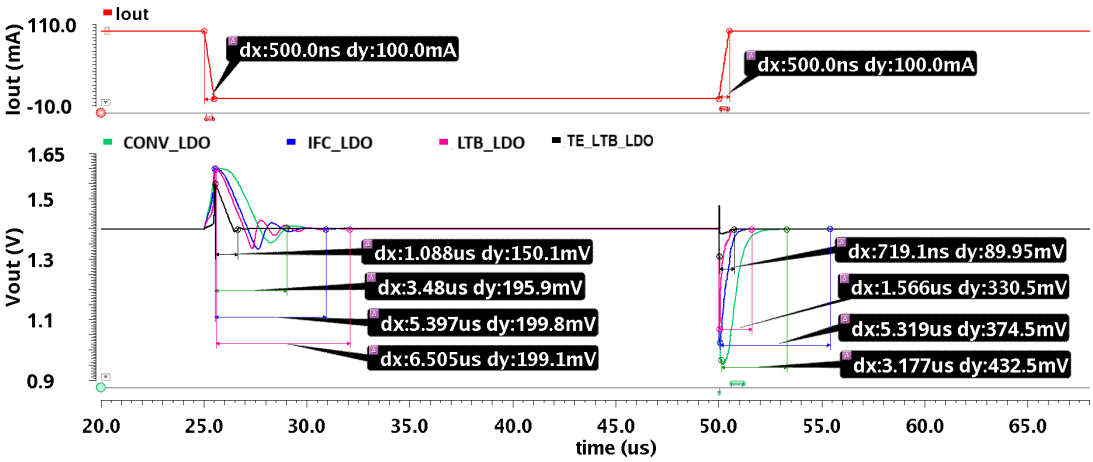

Figure 4.26 Comparison of Transient response of all LDO regulators

The response of the LDO to load transient from 'zero to 100mA' (ΔIout of 100mA) and '1mA to 100mA' (ΔI_{out} of 99mA) reveals the following. Though ΔIout differs by 1 percent only, corresponding transient response varies significantly. This can be attributed to the fact that in case of load changing from 1mA to 100mA, its unity gain bandwidth is large enough to respond relatively faster.

The transient response of the LDO voltage regulator for the load steps of 1mA to 100mA, 10mA to 100mA and 20mA to 100mA with a rise/fall time of 500ns is depicted in Figure 4.27 through Figure 4.29. It can be noted that the performance is relatively poor when the load variation is considered from zero or very low loads.

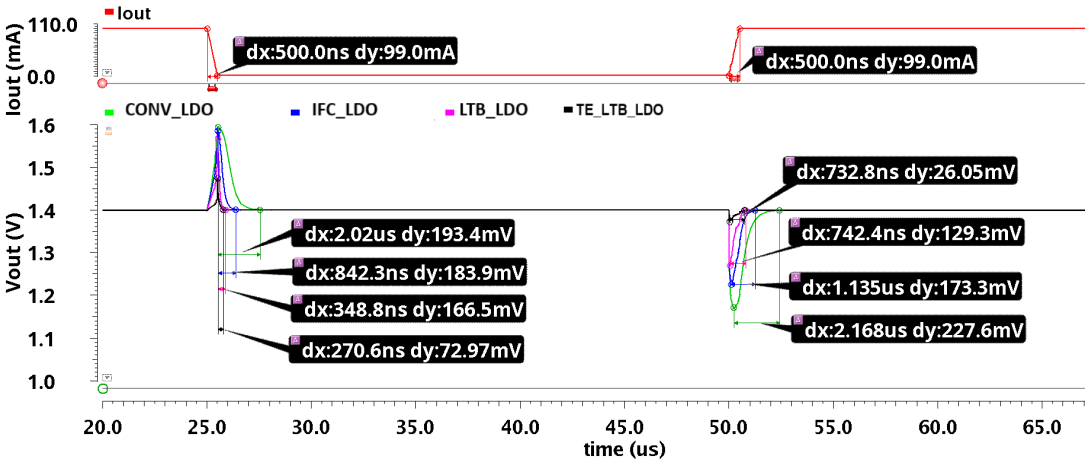

Figure 4.27 Transient response of all LDO regulators for a load change from 1 to 100mA

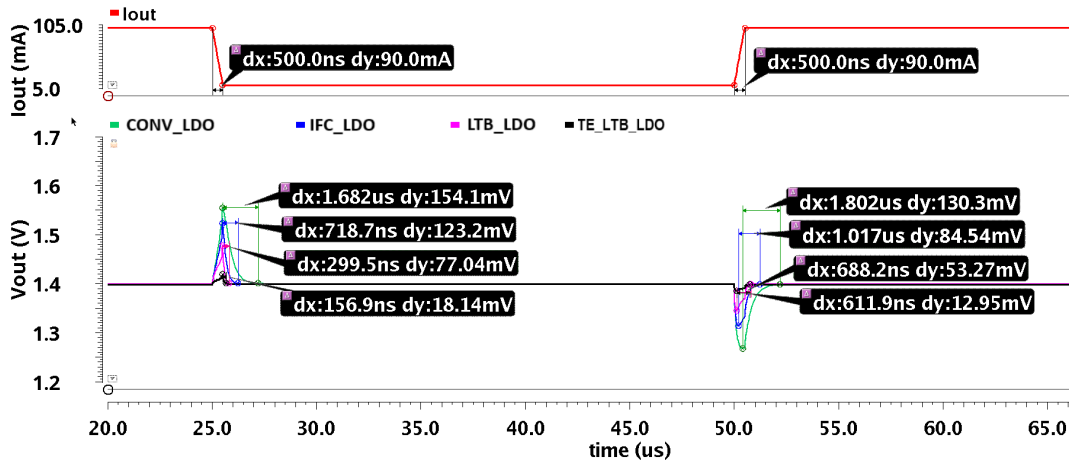

Figure 4.28 Transient response of all LDO regulators for a load change from 10 to 100mA

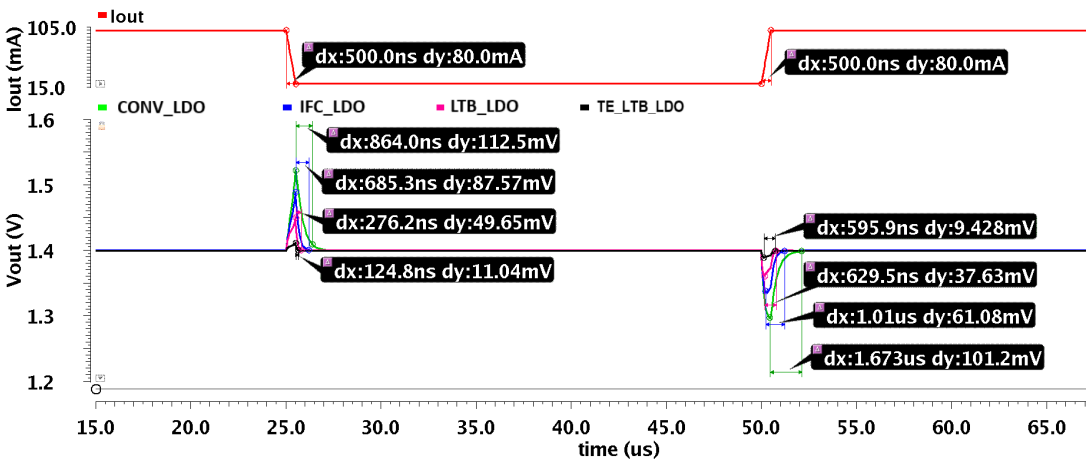

Figure 4.29 Transient response of all LDO regulators for a load change from 20 to 100mA

The load regulation of the LDO presented is shown in Figure 4.30. It is evident from the plot that_TE_LTB LDO regulator_exhibits a load regulation of 20.6µV/mA which is slightly larger than that of load tracking bias LDO regulator with 6.6 µV/mA which can be traded with slight degradation in DC gain.

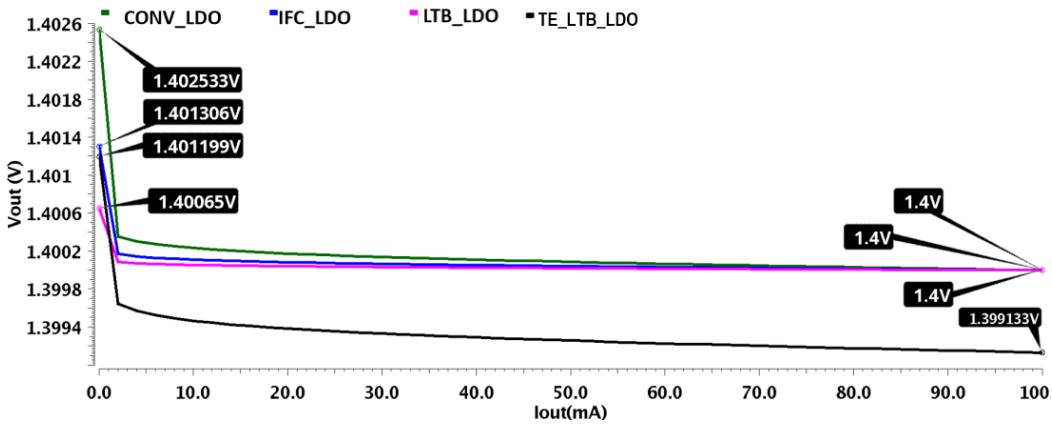

Figure 4.30 Load Regulation for all LDO regulators

The corresponding gain margin, phase margin and unity gain frequency versus the load current of LDO regulators are plotted in Figure 4.31, Figure 4.32 and Figure 4.33 respectively.

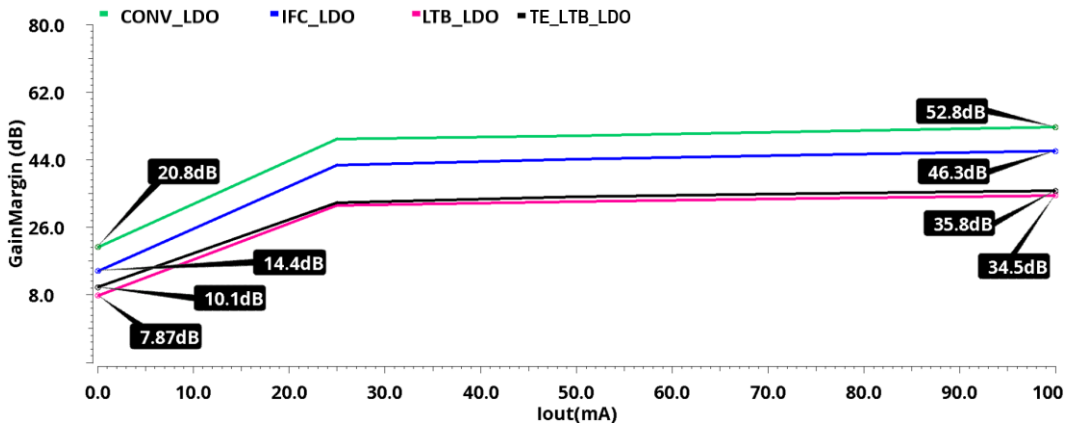

Figure 4.31 Gain Margin (GM) as a function of load current

Referring to Figure. 4.32, it can be seen that the UGF of TE_LTB LDO regulator is 1.58MHz which is relatively larger as compared to the other LDOs under consideration. This improvement can be attributed to the applied transient enhancement, however the price paid

in order to obtain this improvement is negligible since the corresponding degradation in the phase margin is relatively very small (Figure 4.33).

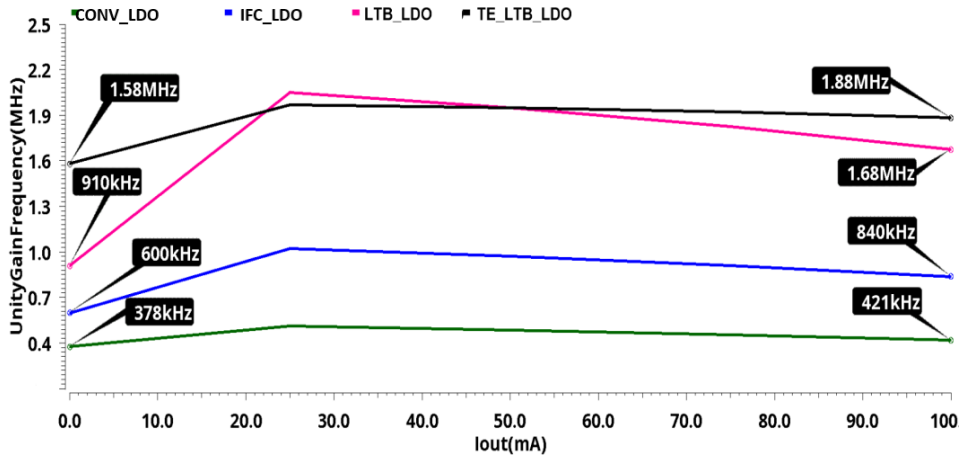

Figure 4.32 Unity Gain Frequency (UGF) as a function of load current

Phase margin as a function of load current is plotted in Figure 4.33. The phase margin is relatively low at lower currents as compared to higher load currents as the pole corresponding to the output node is closer to the first (dominant) pole.

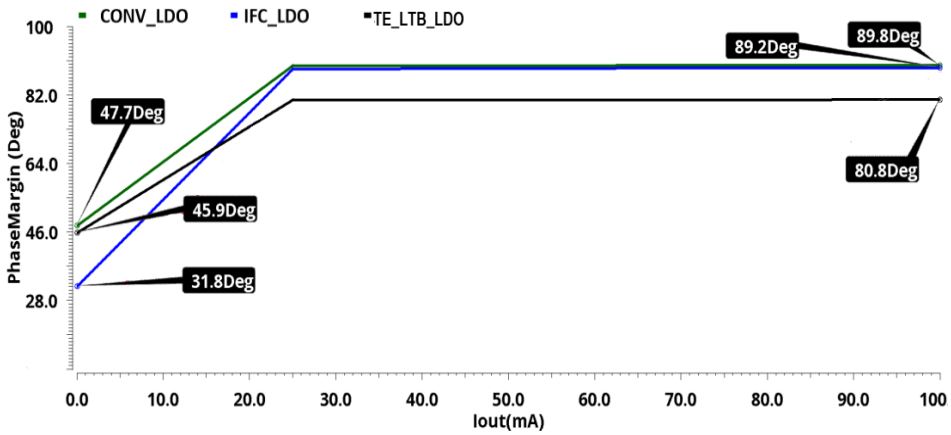

Figure 4.33 Phase Margin (PM) as a function of load current

The zero introduced should be chosen so as to track the non- dominant pole. However, at higher loads, the pole moves farther away from the origin so that phase margin improves without much effort on the compensation front which is evident from the Figure 4.33. The phase margin for TE_LTB LDO regulator is almost closer to that of the conventional one but then it quickly tracks the load changes which can be seen from the slope of the plot.

The power supply rejection is plotted for different LDO regulators which is shown in Figure 4.34. The power supply rejection ratio depends on error amplifier band width, unity gain frequency and output capacitor.

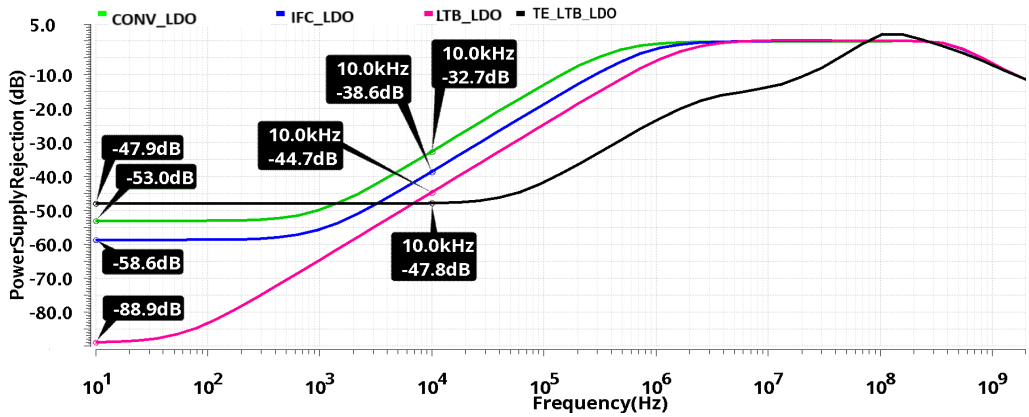

Figure 4.34 Power Supply Rejection Ratio (PSRR) for all LDO regulators

The load tracking bias LDO offers good power supply rejection but only up to 5KHz. However transient enhanced load tracking bias LDO offers a moderate power supply rejection which is relatively constant over wider range of frequencies (almost up to 100 KHz) due to the enhanced frequency response. The transient enhanced load tracking bias LDO regulator offers power supply rejection for a broad frequency range up to 100KHz although with a slight degradation in power supply rejection due to the corresponding decrement in DC gain. This can be attributed to the reduced output impedance of error amplifier due to additional quick path network.

The transient enhanced load tracking bias LDO regulator at no load consumes a quiescent current of 64.4µA, slightly larger relative to the other topologies which is attributed to the additional fast path. The layout of the TE_LTB LDO regulator without output capacitor C_{out} has been shown in Figure 4.35. The largest chip area is occupied by the pass transistor and is exhibited.

Summary

The power requirement of portable SoC demand quick transient response and stability over a range of load currents. The transient response of the LDO can be improved by increasing the unity gain frequency with the help of augmented transconductance of the error

amplifier. However, it trades off with the stability of the LDO especially at low load currents. In this chapter an LDO topology was presented that adapts its bias to the load transients improving the transient response while striking a good trade off with stability over a range of load currents.

Table 4.3 lists the Phase Margin, Gain margin, load regulation, power supply rejection (PSR) and the load transient Responses of TE_LTB_LDO regulator under extreme temperatures and process corners demonstrating the robustness of proposed design.

Table 4.3 Performance Summary of TE_LTB LDO under Process and Temperature Corners

Parameter	**27ºC**	**40ºC**				**90ºC**			
Corner	**TT**	**SS**	**SF**	**FS**	**FF**	**SS**	**SF**	**FS**	**FF**
PM_{min}(Deg.)	45.9	41.37	50.97	35.75	47.60	63.43	83.39	63.43	86.56
GM_{min}(dB)	10.1	10.62	12.64	9.48	12.05	16.08	24.07	16.21	25.90
LoadRegulation (µV/mA)	20.6	32	66	20	77	1.1	3.3	1.1	4
PSR(dB)@ 10k	-47.8	-36.26	-50.09	-45.25	-52.56	-38.27	-49.19	-47.18	-49.98
Undershoot(mV), Sett.(s)@ 0to 100mA	89.95, 719n	89.46, 659n	85.62, 669n	87.62, 850n	83.50, 906n	105.5, 934n	82.09, 1290n	100.70, 973n	71.23, 1100n
$Overshoot_t$(mV), Sett.(s)@ 0 to 100mA	150.1, 1.08u	127.60, 3.1u	125.98, 2.26u	140.5, 2.79u	135.0, 2.97u	140.11, 2.54u	116.83, 3.63u	149.96, 2.75u	123.89, 3.84u
Undershoot(mV), Sett.(s) @1 to100mA	26.05, 732.n	29.39, 1.1u	29.09, 1.48u	29.99, 1.43u	29.51, 1.48u	38.47, 1.88u	36.77, 1.52u	38.25, 1.60u	36.10, 1.52u
Overshoot(mV), sett.(s) @1to 100mA	72.97, 270n	69.52, 0.96n	68.76, 1.14u	77.19,1. 39u	76.91, 1.44u	85.97, 1.12u	83.75, 1.35u	94.74, 2.18u	92.91, 1.35u

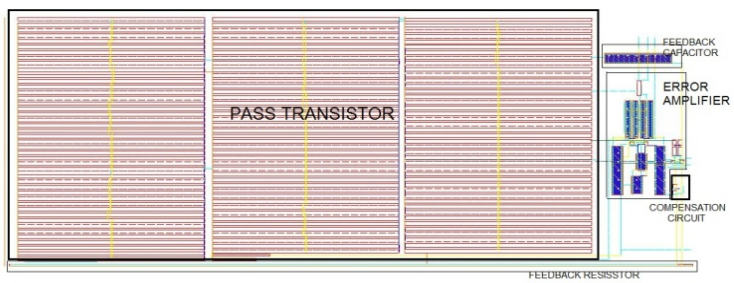

Figure 4.35 Layout of TE_LTB LDO regulator

Relative comparison of the performance of the transient enhanced load tracking bias LDO against the topologies that focused on improving the transient response from literature is

shown in Table 4.4. This work achieves better transient response with moderate quiescent current. In addition, the edge time considered here is 500nsec which is half of that of the other topologies [8] [33] [59] With respect to [34], though edge time considered is 500nsec, the load current variation is taken from100µA to 100mA whereas this work considers load variation from 0 to 100mA which is more stringent constraint since the performance is critical at lower load currents and in particular at no load currents. Edge time of 500nsec was considered for [23] also, but it considers a load variation from 0.5mA to 200mA. It is evident that the proposed TE_LTB LDO regulator has small quiescent power consumption, good regulation accuracy, and high-power supply rejection for the load variation from 0 to 100mA.

Table 4.4 Performance Summary and Comparison with recent Capacitor-less LDOs

	[8]	[58]	[59]	[23]	[60]	[33]	[34]	**This work#**				
Year (20XX)	07	10	10	13	14	12	15	**15**				
Technology(µm)	0.35	0.35	0.35	0.11	0.18	0.35	0.18	**0.18**				
Vsupply(V)	3.0	1.4	1.8	2.2	1.8	1.2	1.4		**1.6**			
V_{DROP}(mV)	200	200	200	200	0.2	0.2	0.2		**0.2**			
V_{OUT}(V)	2.8	1.2	1.6	2	1.6	1.0	1.2		**1.4**			
$I_{loadmax}$ (mA)	50	100	100	200	50	100	100		**100**			
I_Q(µA)@No load	65	43	20	41.5	55	28	0.61		**64.4**			
I_Q(µA) @Full load	65	43	20.9	41.5	80	380.1	141		**64.1**			
ηc@Full load (%)	-	99.96	99.98	99.97	99.8	99.62	99.8		**99.66**			
Load Reg.(µV/mA)	760	400	109	108	140	78.2	270		**20.6**			
C_{out}(pF)	100	100	100	40	100	100	100		**100**			
PSRR(dB) @freq. (Hz)	-57@ 1K	N/A	-40 @ 10K	-	-70 @ 1M	-47.90@10K -31.95@100K -13.15@1M	-26 @1M		**-47.79@10K -40.2@100K -23.05@1M**			
ΔI_{load}(mA)	49.99[1]	99	90	199.5	50	100	99.99	99	**80**	**90**	**99**	**100**

Edgetime(µs)	1	1	1	0.5	0.1	1	1	.5	**~0.5**	**~0.5**	**~0.5**	**~0.5**
Undershoot(mV)	78	70	73	385	80	105	110	5	**9.43**	**13**	**26.5**	**89.9**
Overshoot(mV)	77	70	70	200	120	50	85	34	**11.04**	**18**	**73**	**150**

Chapter 5

Capacitor-less Voltage Regulator with Segmented Pass Transistors

As discussed in the previous chapters, the bulky pass transistor poses impediment for the transient response of the capacitor-less LDO voltage regulator. Pass transistor can be segmented to address this problem [61] which can facilitate quick response of the LDO. Different topologies in this direction are explored in this chapter to improve overall performance of LDO.

5.1 Capacitor-less LDO with Split Drive Error Amplifier using Segmented Pass Transistors

This topology attempts to split the large pass transistor into two segments each driven by individual appropriate error amplifiers. One of the segmented pass transistors is sized to meet the fast load transients while the overall pass transistor addresses the dropout voltage. The error amplifiers are designed to impart the requisite drive quickly to the respective pass transistors to improve transient response while conserving the quiescent current.

A Capacitor-less LDO architecture employing two error amplifiers that drive their corresponding pass transistors to regulate the output is shown in Figure 5.1.

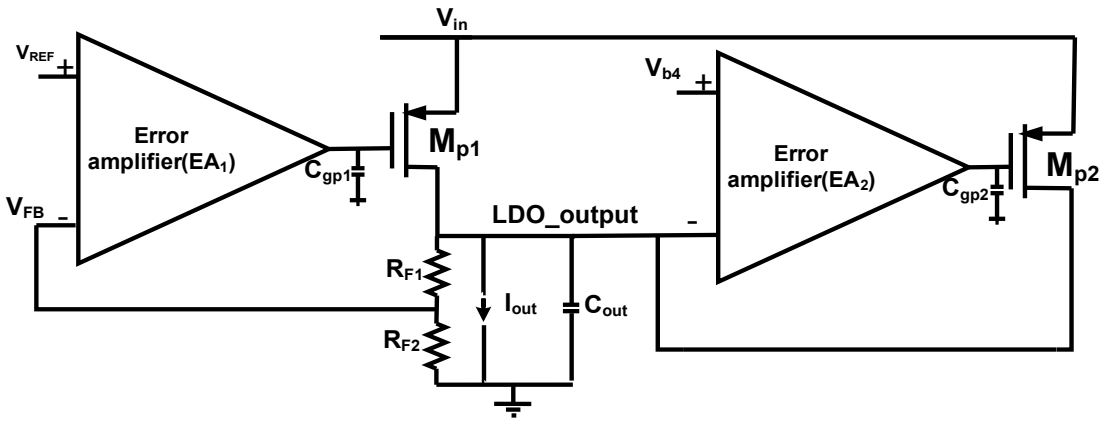

Figure 5.1 Block diagram of the proposed topology

Conventional LDO voltage regulators are designed to support large load currents with a low dropout specification. Consequently, the pass transistor is over sized from the viewpoint of transient response which can be optimized. Accordingly pass transistor is split in such a way that relatively smaller fraction constituent can respond quickly to load transient while overall pass transistor will meet dropout specification as well. This necessitates two separate driving circuits for both the transistors meeting their individual requirements. The LDO employing different drivers [62] with single error amplifier was presented in these lines. In this section a topology is presented that uses two separate error amplifiers to drive the split transistors in order to improve the transient performance.

During load transients from low to high the pass transistor M_{p1} along with its error amplifier EA_1 reacts faster as it is relatively smaller compared to M_{p2}. The total load current is shared by the pass transistors in such a way that the smaller pass transistor takes relatively smaller portion of the current (less than 20mA) while the larger takes the greater share. The

error amplifiers driving the pass transistors are designed suiting the individual requirements of the pass transistors.

1.1.11 Transient Enhanced Loop Operation (Error Amplifier 1 - EA_1)

The schematic corresponding to error amplifier driving the smaller pass transistor is shown in the Figure 5.2. The requirement of this error amplifier is to enable the respective pass transistor to respond quickly whenever load changes from no load (zero) to full load which can be met with larger slew rate drive at the gate of pass transistor without demanding larger quiescent current. At the same time a smaller transconductance under steady state improves phase margin. Hence, an error amplifier with low transconductance and high slew rate is demanded. The topology most suitable for this requirement is a class AB transconductance amplifier. It offers low transconductance and maintains stability at lower load currents along with reasonably good slew rate without consuming significant extra bias current.

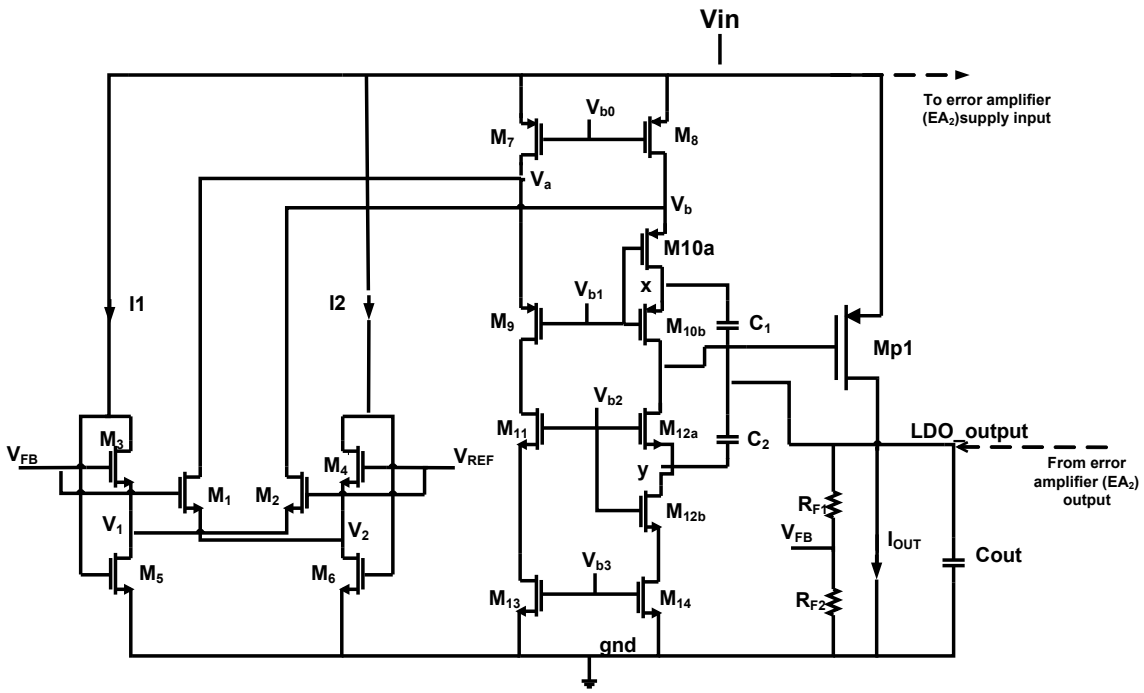

Figure 5.2 The error amplifier (EA_1) employing modified folded cascode architecture along with hybrid cascode compensation

A class AB folded cascode based operational transconductance error amplifier is realized by M1-M14 in which (M3, M5, I1) and (M4, M6, I2) comprise the level shifters while M7-M14 constitute the output stage of the modified folded cascode amplifier with split transistor and hybrid cascode compensation [63][70]. The hybrid cascode compensation is realized by capacitor C1 along with transistors M10a, M10b forming one section of cascode compensation while capacitor C2 with M12a, M12b forming its counterpart. The slew rate drive at the gate of pass transistor of error amplifier EA1 is improved by class AB operation of differential pair input transistors in synergy with hybrid cascode compensation.

In the steady state operation, the gate to source voltages of M1-M4 are forced to be the same by the flipped voltage follower units (M3, M5, I1 and M4, M6, I2). During load transients a sampled voltage VFB of the output is fed back to the gate input of M1, M3. The gate to source voltages of M3 and M4 are maintained constant by negative feedback operation of flipped voltage followers. Consequently, the undershoot voltage increases the gate to source voltage of M2 that results in a large sink of drain current through it, thereby changing the voltage at the folded node V_a of folded cascode amplifier. At the same time the differential operation reduces the current of M1 influencing the other folded node voltage Vb.

The current driving capability of M5 determines the maximum current drive through M2 and its performance is not limited to their bias currents. Analogous behaviour is observed for overshoots. Thus, the response of the differential pair transistors to the load variations affect the current of second wing of folded cascode structure. As this operation involves passing of the signal through large number of transistors it gets delayed. In order to speed up this operation a hybrid cascode compensation scheme is used in which the sudden load transients are coupled to the second wing of folded cascode structure and the gate of pass transistor is controlled much earlier to differential pair operation.

The transistor M_{10} in the folded arm of the error amplifier is fragmented [64] into two transistors M_{10a} (W/L1) and M_{10b} (W/L2) such that total length $L=L_1+L_2$ remains the same. Similar operation is applied for the transistor M_{12}. This leads to two signal feedback paths from the output to the low impedance nodes X and Y through C_1 and C_2 respectively. The undershoot voltages generated at the output is coupled to the source of M_{10b} and M_{12a} instantaneously. This decreases the overdrive of M_{10b} such that its current now is well below

its steady state current. On contrary, the reduced voltage at node Y increases the overdrive voltage of M_{12a} sinking large current through it. This results in current comparator action of M_{10b} and M_{12a} which pulls the gate voltage of the pass transistor M_{p1} low enough to source more current as required. An analogous operation occurs at the instance of overshoot.

1.1.12 Second Error Amplifier (EA_2) Loop

The schematic corresponding to the second error amplifier (EA_2) is shown in Figure 5.3.

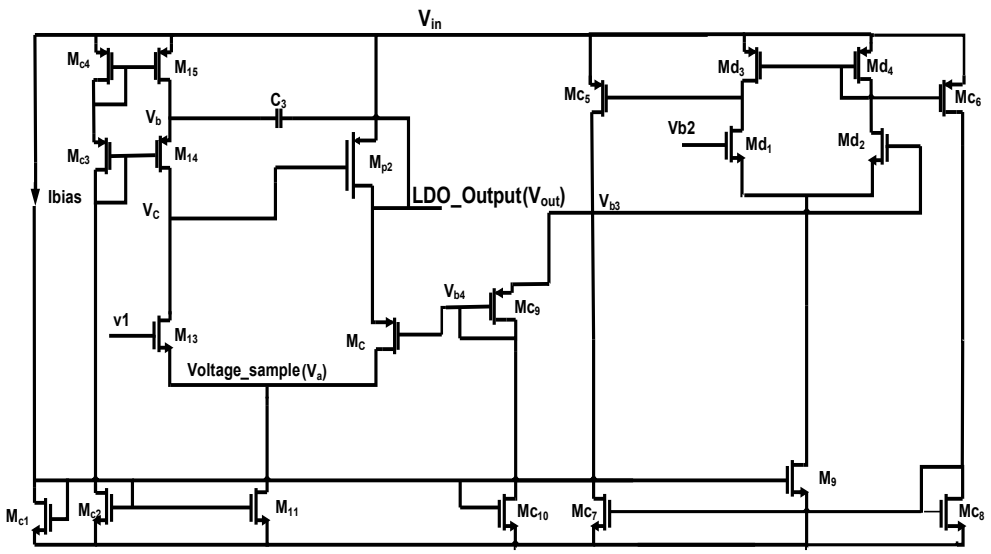

Figure 5.3 The error amplifier (EA_2) with modified folded cascode stage along with miller compensation capacitor.

The pass transistor M_{p2} is relatively bulkier as compared to the first one addressing the dropout specification. The biasing conditions keep the pass transistor M_{p2} in off region till the load current reaches significantly larger value(~20mA). Thus, this error amplifier is relieved from the stringent requirement of responding to zero or low loads while catering to the higher range of loads. Thus, it is designed with relatively higher transconductance meeting the requisite larger load current demands and attempting to mitigate over shoots.

Thus, error amplifier EA_2 of the LDO is designed using cascode current source based flipped voltage followers formed by transistors (M_C, M_{13}, M_{14}, M_{15}) driving pass transistor M_{p2}. Two feedback loops with different speeds are used for this error amplifier in an attempt to

further optimize performance. One loop consists of M_{13}, M_C and M_{p2} while the other loop is formed by cascode compensation capacitor C_3 along with M_{14} and M_{p2}. In the primary loop, the control transistor M_C acts as a variable resistance depending on the output variations and thus supports the regulation. The NMOS transistor M_{13} forms the folded cascode structure. This common gate transistor M_{13} serves dual purpose of providing a loop gain and also an offset voltage generator at the node (voltage_sample) and is large enough to keep the transistor M_C in saturation for the entire range of load currents. This alleviates the minimum biasing current requirement conditions imposed for the general flipped voltage follower based LDOs. The transistor M_{14} along with cascoded stage current source transistor M_{15} increases the resistance at the gate of pass transistor M_{p2} and thus improves the loop gain. The coupling capacitor C_3 forms an auxiliary path to transfer the output voltage variations to the node V_b that charges and discharges the gate of pass transistor M_{p2} in accordance to the load current transitions and provide a quick regulation response.

The small signal equivalent circuit for the error amplifier EA_2 is shown in Figure 5.4. The transfer function of the regulator comprising error amplifier EA_2 along with pass transistor is given in Equation 5.4 [65].

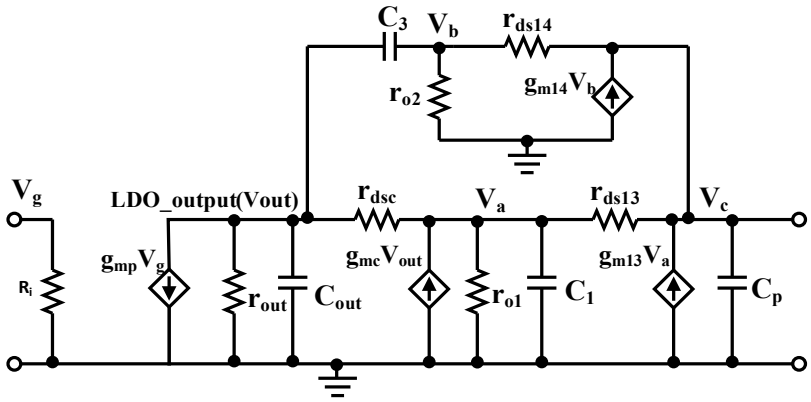

Figure 5.4 Small signal equivalent of error amplifier EA_2

$$r_{out} = r_{dsp} || 1/g_{mc} \tag{5.1}$$

$$r_{01} = r_{ds11} \,||\, 1/g_{m13} \tag{5.2}$$

$$r_{02} = r_{ds15} \,||\, 1/g_{m14} \tag{5.3}$$

Where r_{dsp} is the resistance of transistor M_{p2}, $r_{01}$and r_{02} are resistances at nodes V_a and V_b respectively. Transfer function is given by Equation 5.4.

$$T(s) \approx \frac{A_{DC}(1+\frac{s}{\omega_{z1}})}{[(1+\frac{s}{\omega_{p-3dB}})(1+\frac{s}{\omega_{p2}})]} \tag{5.4}$$

Where A_{DC} is the loop gain, the dominant pole is given by $\omega_{p\text{-}3dB}$, pole ω_{p2} and zero ω_{z1}

$$\omega_{p-3dB} = \frac{g_{m14}r_{bias2}r_{bias1}r_{ds14} + g_{m13}r_{bias1}r_{dsp}r_{ds13} + g_{m14}r_{bias2}r_{dsp}r_{ds14}}{C_p g_{m13}r_{bias2}r_{bias1}r_{ds14}r_{ds13}r_{dsp}} \tag{5.5}$$

$$\omega_{z1} = \frac{g_{mc}g_{m14}}{[(g_{mc}+g_{m14})C_3]} \tag{5.6}$$

$$\omega_{p2} = \frac{g_{m14}}{C_3} \tag{5.7}$$

The transient response of the LDO is further improved by inclusion of overshoot reduction circuit as discussed in the next section.

1.1.13 Overshoot Reduction Circuit

The class A mode operation of error amplifier (EA_2) limits the slew rate drive at the gate of pass transistor during load transients leading to large overshoots with long settling time at the output [66]. In order to reduce the overshoot, an attempt is made to clamp the output to be within the limits using the overshoot reduction circuit shown in Figure 5.5. It comprises of transistors M_{A1}-M_{A6} and capacitor C_m. A current comparator is designed consisting of transistors M_{A1}-M_{A3} forming one wing while M_{A4}-M_{A5}, I_B forming the other. The complete schematic of the topology is shown in Figure 5.6.

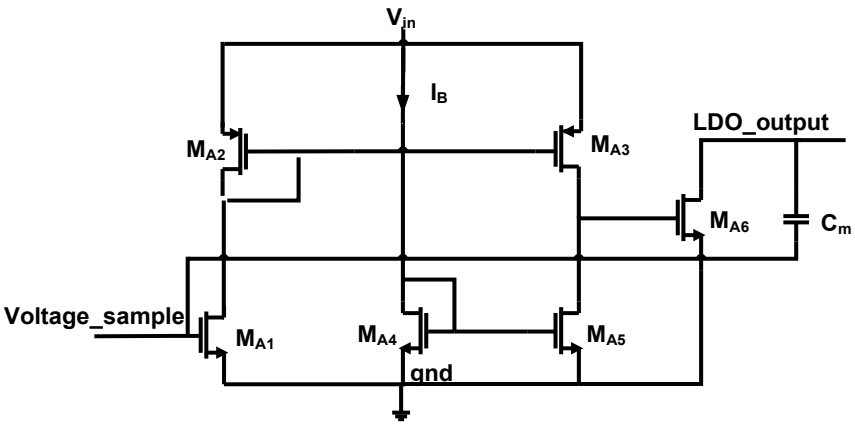

Figure 5.5 Overshoot reduction technique

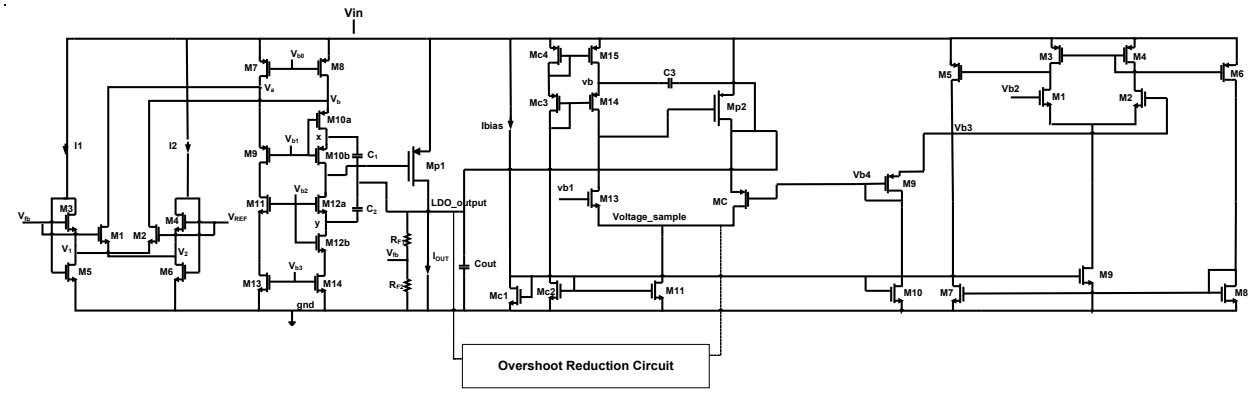

Figure 5.6 Complete schematic of capacitor-less LDO

The aspect ratio of the M_{A5} is chosen to be relatively larger as compared to M_{A3} so as to keep M_{A6} off. The overshoots generated at the output during transients is coupled to M_{A1} through C_m and error amplifier node 'Voltage_sample'. The resulting imbalance in the currents generates large overdrive voltage across M_{A6} such that it sinks large current through it as per the load demand. Thus, output can be quickly recovered back from the transient by judiciously choosing size of M_{A6}.

1.1.14 Results and Discussion

The capacitor-less LDO is designed to deliver 1.6V output with 1.8V input. The total quiescent current is restricted to be within 40µA. A total compensation capacitance of 15pF is used for this topology with a 100pF capacitor at the output. Figure 5.7 shows the transient response for the load current variation between 0 and 100mA for a rise and fall time of 500ns.

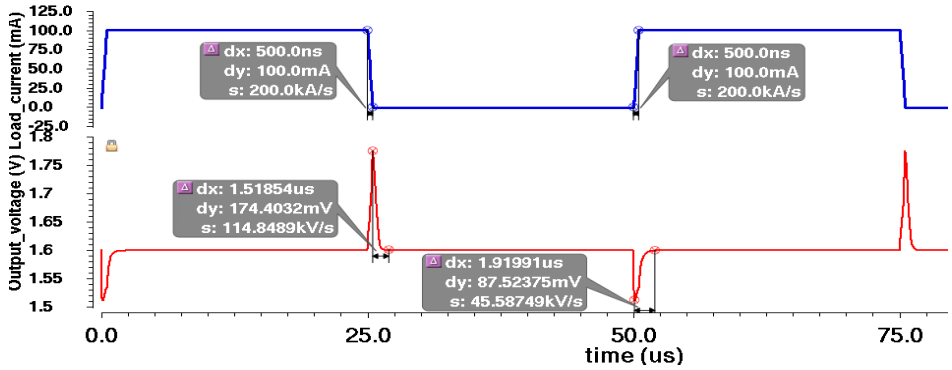

Figure 5.7 Transient response for the load transient from 0 to 100mA with rise and fall time of 500ns

The frequency response corresponding to the two loops with the respective error amplifiers and pass transistors is shown in Figure 5.8. It can be seen that the error amplifier EA_1 exhibits a gain of 61.09dB with a unity gain frequency of 0.6MHz while the other error amplifier EA_2 has a loop gain of 57.76dB and a unity gain frequency of 1.53MHz that helps in quick recovery from high to low load transients.

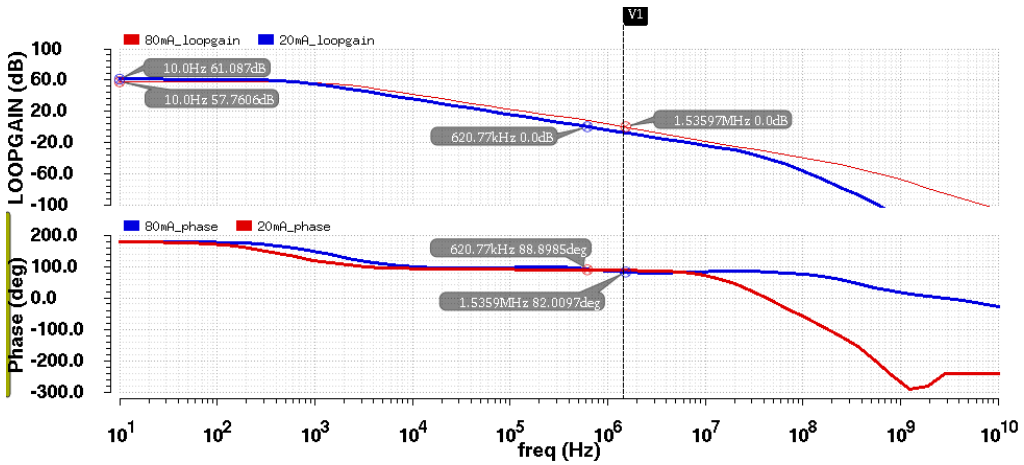

Figure 5.8 The frequency response of the proposed LDO depicting the error amplifiers (EA_1 with 20mA-Mp1 and $EA_2$with 80mA-M_{p2})

At higher load currents the non-dominant pole due to output node moves away from the origin while dominant pole due to larger pass transistor moves towards the origin. Thus, there is room for translating this advantage to improve load transients by increasing the unity gain frequency of the corresponding driving error amplifier EA_2. This in turn facilitates LDO to respond quickly to the load changes during higher load range. Similarly, at lighter loads the

load pole moves towards the origin and lighter pass transistor makes the dominant pole to move away from the origin. Thus, the purpose of choosing smaller pass transistor at lighter loads though serves to respond load changes quickly, it proves counterproductive in terms of stability. Hence EA_1 is judiciously designed to pull the dominant pole towards the origin that improves stability while retaining the advantage of smaller pass transistor at lighter loads. This is evident in the frequency response where unity gain frequency(UGF) of the smaller pass transistor is lower than that of larger transistor.

It can be further endorsed through the Figure 5.9 which demonstrates current through individual pass transistors against the variation of the load current.

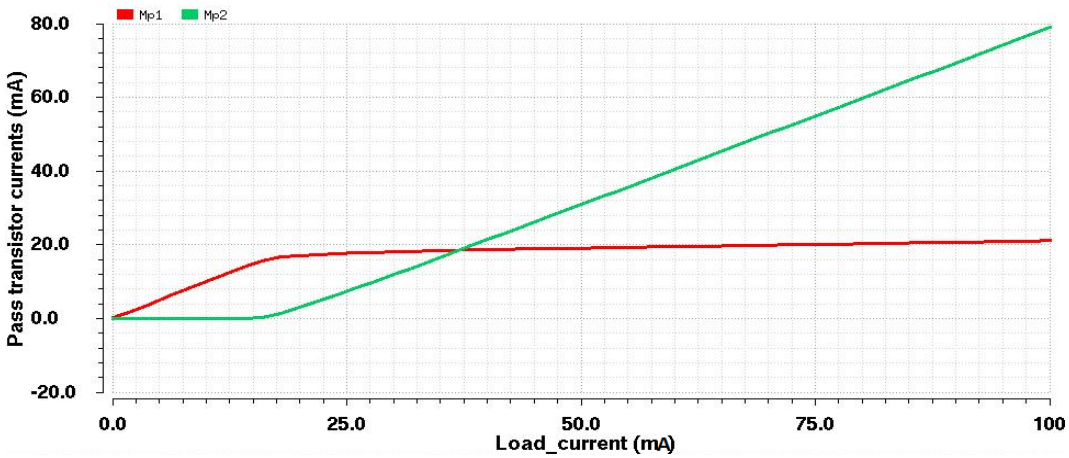

Figure 5.9 The pass transistor currents (M_{p1} and M_{p2}) as a function of load current

The proposed LDO performance in comparison to the state of art capacitor-less LDOs is shown in the Table 5.1. It is noted that the proposed LDO with its less undershoot and overshoot is competitive to the other state of art LDOs and is validated through lowest figure of merit. The FOM is adopted from [36] as a single expression taking into account trade-offs in parameters across the technologies and different load transients corresponding to topologies under consideration that leads to fair comparison which is given in the Equation (5.8)

Table 5.1 Comparison with related work

Parameter	**[33]**	**[23]**	**[35]**	**[34]**	**[36]**	**This work**
Year	2012	2013	2013	2016	2016	**2017**
Tech	0.35	0.11	0.065	0.18	0.18	0.18
Minimum Vin(V)	1.2	2.2	1.2	1.4	1.5	1.8

Nominal V0(V)	1	2	1	1.2	1.2	1.6
Vdropout(mV)	200	200	200	200	300	200
Iq(mIn)µA	28	41.5	0.9	0.61	2.4	40
Iq(max) µA	380	41.5	82.4	141	242	40
ΔI_{load}(mA)	100	199.5	100	99	99.9	100
Edge time(ns)	1000	500	300	500	300	500
K	3.33	1.67	1	1.67	1	1.67
Alpha	5.385	1.693	1	2.77	2.77	2.77
Undershoot (mV)	105	384	68.8	5	125	87.52
Overshoot(mV)	50	200	24.4	34	65	174.4
Vout(pp)mV	155	584	93.2	39	190	261.92
Cout(pF)	100	40	100	100	100	100
FOM	**67.7**	**70.7**	**76.8**	**12.07**	**60.0**	**22.7**

$$FOM = k * \frac{\Delta V_{out}(pp) * I_q(\min)}{\alpha^2 * \Delta I_{load}(\max)} \tag{5.8}$$

Where k = (Δt used for the topology under consideration)/ (smallest Δt among designs for comparison), α= (technology used in the present work)/ (lowest technology used in the previous work). It may be observed that the load current range is from 1mA to 100mA in [34] against zero to 100mA in the current work.

5.2 LDO Regulator with Adaptive Biasing and Bulk Modulation

The work presented so far focused on improving the performance of the LDO by exploiting the adaptive biasing and pass transistor segmentation. The stability of the regulator at lower load currents is addressed by segmentation of pass transistors and adaptively controlling them in accordance to load current demands [25]. However, the adaptive biasing results in nonlinear movement of poles [67] leading to proximity of dominant and non-dominant poles which limits the improvement in transient performance in terms of overshoots and under shoots as well as settling time. This detrimental behaviour can be addressed by controlling the drive strength of pass transistor using bulk modulation [37] along with the benefits of adaptive biasing. The corresponding block level representation of the topology is shown in Figure 5.10.

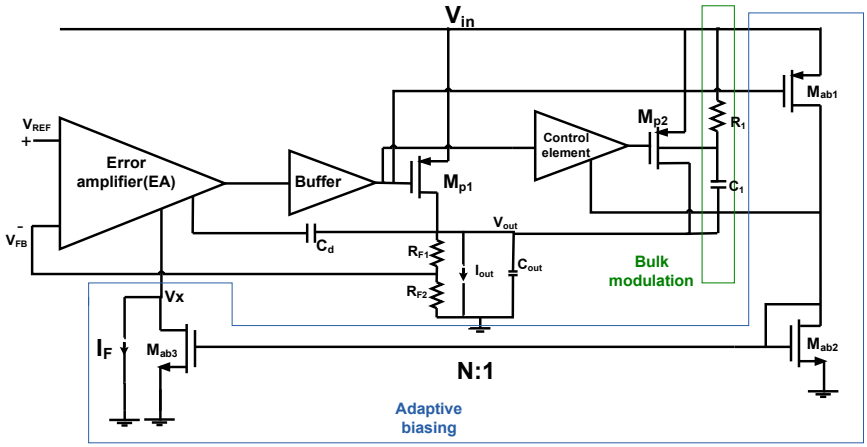

Figure 5.10 Block diagram of the proposed LDO regulator

1.1.15 Bulk Modulated Capacitor-less Low Dropout Regulator

The schematic of bulk modulated adaptively biased capacitor-less LDO voltage regulator is shown in Figure 5.11.

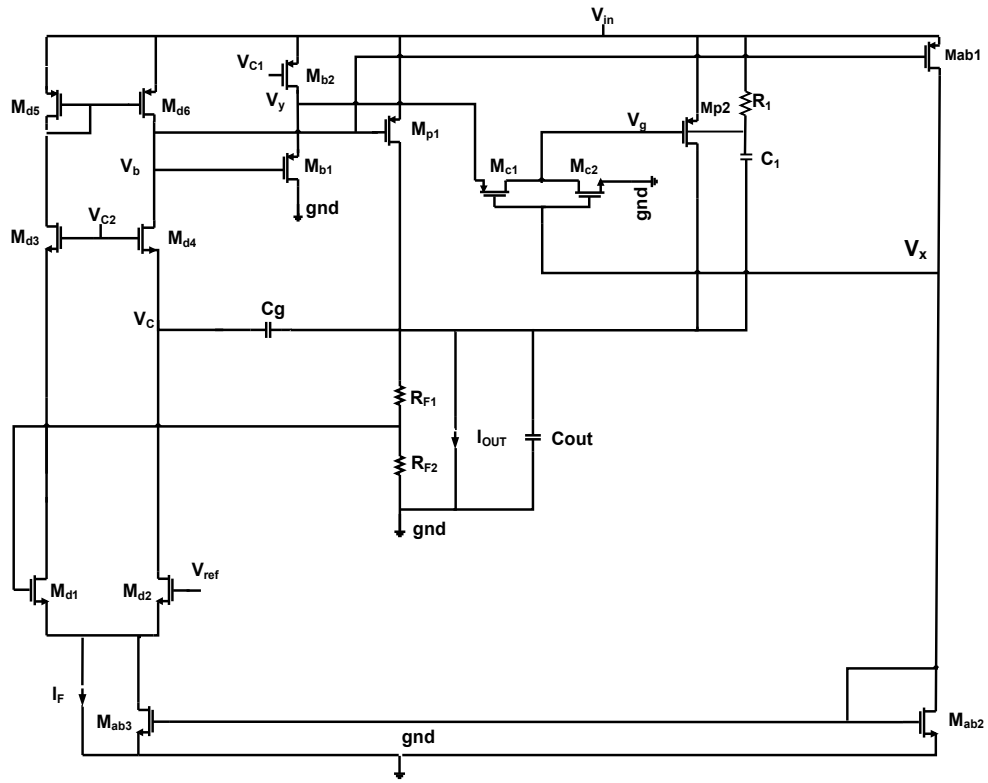

Figure 5.11 The bulk modulated adaptively biased capacitor-less LDO

It can be controlled using back gate drive of the pass transistor. This requirement for extra drain current is supported by modulating the threshold voltage of the bulk terminal of

the pass transistor. Initially during undershoots, the gate voltage is high while the output voltage is low. The capacitor coupled between bulk and output node charges to the supply through resistance R_1 which in turn decreases source to bulk voltage (V_{sb}) as per the relation given by Equation 5.9 [36].

=- (5.9)

Where V_{th} is the threshold voltage of pass transistor M_{p2}, V_{th0} is the nominal threshold voltage, is emission coefficient, and fermi potential. This operation in turn decreases the threshold voltage and augments the increase in the drain current. Thus, it restores the output voltage sooner to its regulated value and pacifying the ringing effect. The bulk terminal of the PMOS pass transistor is biased such that it modulates the threshold voltage of the device only when needed (i.e. during transients) while retaining low leakage currents during steady state. During high to low load transients, an overshoot voltage is generated at the output. The potential at pass transistor bulk terminal raises high from its nominal value through resistor R1. It decreases V_{sb} which in turn increases the threshold voltage. The increased threshold voltage further decreases the pass transistor current precipitating the required changes in the load. This improves the settling time and overshoot.

The entire operation is evident from the waveforms plotted at relevant nodes as shown in Figure 5.12 Similar improvement can be envisaged during the instance of undershoot.

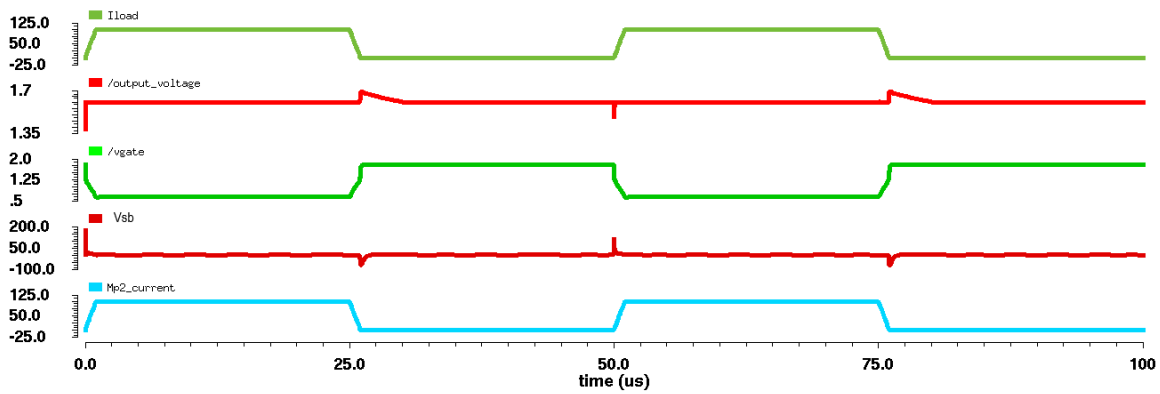

Figure 5.12 The transient response behavior at the nodes of the adaptively biased bulk modulated LDO.

1.1.16 Design and Analysis

Design of bulk modulated adaptively biased capacitor-less LDO

The pass transistor M_{p1} is sized to support lower load currents with a dropout voltage of 200mV as per the following relation.

$$V_{DROPOUT}<*=<200mV \quad (5.10)$$

$$> \quad (5.11)$$

Length of pass transistor is chosen minimum i.e 180nm. Correspondingly, the pass transistor M_{p2} is designed to support the higher load currents. The reference voltage (V_{REF}) and output voltage (V_{OUT}) are related to each other by Equation 5.12.

$$== \quad (5.12)$$

$$\text{So } 0.6 = 0.8 \quad (5.13)$$

The 1µA bias current is chosen for the feedback resistive network such that it ensures a minimum sub-threshold current during worst case conditions and operates under extreme temperature and process corners.

$$\text{So } = = 1600k\Omega \quad (5.14)$$

Solving equation 5.13 and 5.14 gives =700kΩ and 0kΩ

The transistor M_{ab1} and M_{P2} are sized such that they maintain a ratio 1:M between them, where M is selected such that a low quiescent current of 1µA flows through M_{ab1}. The value of M is chosen such that it consumes a low quiescent current for low power consumption. Here, a current of 1µA is chosen, so M=100 as M_{p1} carries 100µA.

(5.15)

An overdrive of 200mV chosen for M_{ab1} such that

(5.16)

3.33 (5.17)

Transistors M_{ab2} and M_{ab3} form a current mirror with a mirror ratio of 1: N between them. Larger mirror ratio N yields better adaptation to loads which is effective during mid load range. However, it trades off with power consumption. Accordingly, a judicious value(N=2) is chosen that strikes balance between power consumption and transient response.

(5.18)

(5.19)

==1.75 (5.20)

= =2 (5.21)

2 (5.22)

The tail current source Mab3 is augmented with an auxiliary current source I_F(1µA) that ensures the error amplifier transistors in saturation even for lower load currents while adaptive biasing is ineffective. The error amplifier transistors M_{d1} and M_{d2} are sized to support a total tail current of 3µA.

(5.23)

=== 1.185 (5.24)

The length of transistors is selected to be 1µm. The same aspect ratio is used for M_{d3} and M_{d4}. The aspect ratio of transistors M_{d5} and M_{d6} are selected such that they carry a current of 1.5µA each with an overdrive voltage of 100mV across it. A length of 1µm is chosen for the transistor M_{d5}, M_{d6}.

(5.25)

==5 (5.26)

The control section consists of transistors M_{c1} and M_{c2} are designed such that they operate with error amplifier output voltage V_y and adaptive bias voltage V_x to conduct quiescent current for a suitable range of load currents beyond which the output of it get clamped. The control section is analysed and designed as follows:

For M_{c2} is off and no current flows through the control section. For the current through control section is zero and M_{c1} is off. Later M_{c1} slowly turns on while M_{c2} continues to be in triode region that results in the following current.

I= (5.27)

The current flowing through M_{c1} follows the above relation till M_{c2} enters saturation, at which instance the current is governed by the following equation.

(5.28)

Solving Equation 5.28, we get

=+ (5.29)

So, for + the current through control section is zero and further conduction in the control section is governed by the following equation.

+ + (5.30)

The dimensions of $M_{c1}$and M_{c2} are selected in accordance with the above equation, whose values decides the quiescent current freezing conditions i.e quiescent current does not change even while the load current changes .The design is done to support the aforementioned criterion as any higher quiescent current chosen corresponding to load current does not improve transient response and taxes power consumption unnecessarily.

Transient response in effect to bulk modulation of pass transistor

This section presents salient features of the design of LDO using bulk modulation of pass transistor. Care should be taken to constrain the leakage currents that may result due to bulk modulation. Towards this end, |Vsb| is constrained to be less than 400mV.

The bulk PN junction current is given by . Considering ,,, Id is calculated as 48nA which is almost insignificant. The static resistance of PN junction diode supporting 48nA current is

$$=8.33M\Omega \quad (5.31)$$

A resistance R1 connected across the bulk to source terminal is designed in such a way that it allows maximum current through it while limiting the current through PN junction to be within the specified range. This transient bulk voltage should be retained over sufficiently large portion of the settling time to allow the pass transistor to respond to the load changes in association with the main loop. Accordingly, R_1C_1 is chosen to be order of the $1/3^{rd}$ of the settling time. s Capacitor C1 is selected as 5pF without demanding larger silicon space, accordingly R_1 is obtained from the Equation 5.32.

$$= R1=> \quad (5.32)$$

1.1.17 Small Signal Analysis

The transfer function for the above circuit is derived from the small signal equivalent in the Figure 5.13.

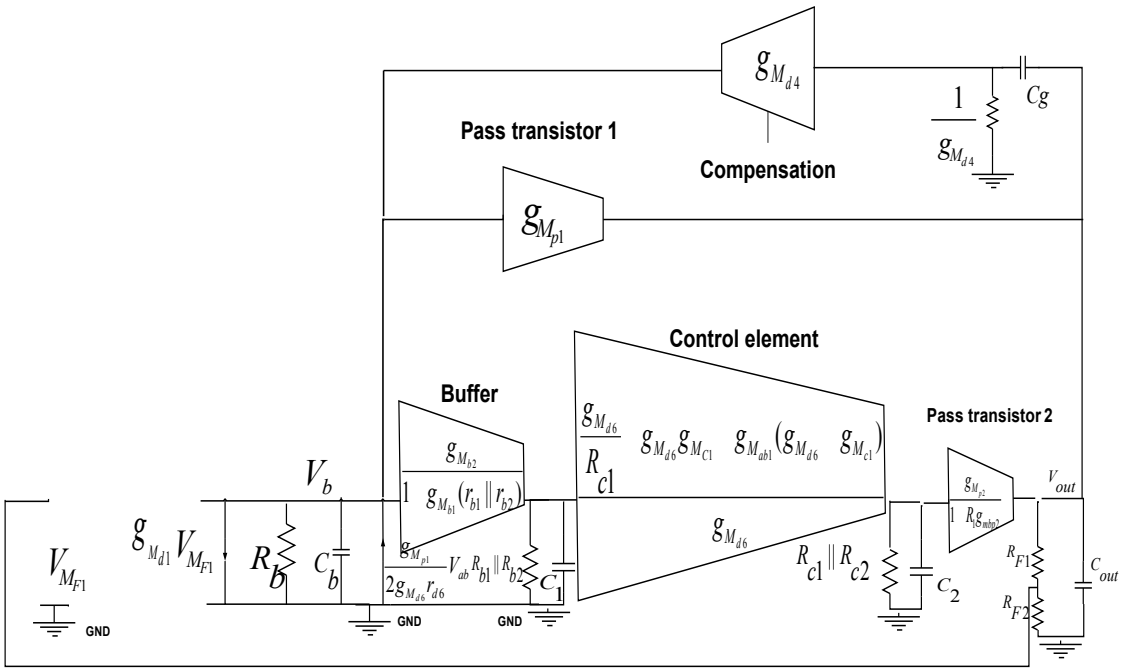

Figure 5.13 Small signal equivalent diagram of proposed regulator

(5.33)

= (5.34)

= (5.35)

==} (5.36)

(5.37)

The buffer and control section are ignored in the small signal analysis as it is judiciously designed in such a way that its output poles lie at far higher frequencies thereby not influencing the dominant pole. The transconductance of pass transistor Mp2 is relatively larger dimension to support higher load currents as compared to the other pass transistor MP1 such that the effective transconductance is that of MP2. The adaptive bias loop transistors are designed such that their poles do not influence the small signal response.

The reduced small signal transfer function is given by

T(s) = (5.38)

Where =

Dominant pole is given by Equation 5.39, Zero is given by Equation 5.40 and the unity gain frequency is given by Equation 5.41

(5.39)

(5.40)

(5.41)

1.1.18 Results and Discussion

The LDO is designed to deliver a nominal regulated output voltage of 1.6 V with a dropout of 200 mV at 100 mA load current using 180nm CMOS technology. This architecture benefits from relatively low quiescent current of 1.5 µA at no load and 20 µA at full load. The frequency response is depicted in Figure 5.14. The LDO uses 40pF capacitance at the output node and 5pF at the bulk terminal. The frequency response plots reveal a dc gain of 71dB and phase margin of 77.42° at full load (100 mA) and 70.03° at no load (0 mA).

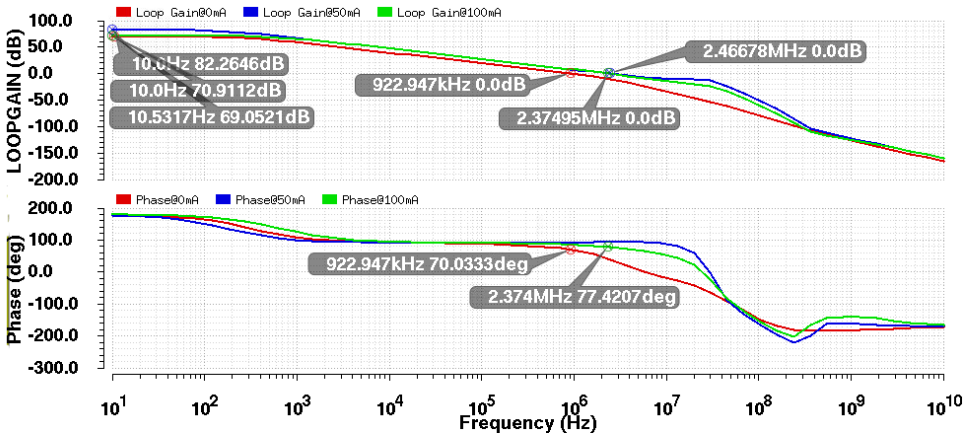

Figure 5.14 Frequency response of LDO at a load current of 0mA, 50mA and 100mA

The transient response of this LDO topology with bulk modulation is shown in Figure 5.15. This plot also includes transient response of LDO using only transistor segmentation but

no bulk modulation and that of conventional LDO i.e. without pass transistor segmentation and bulk modulation.

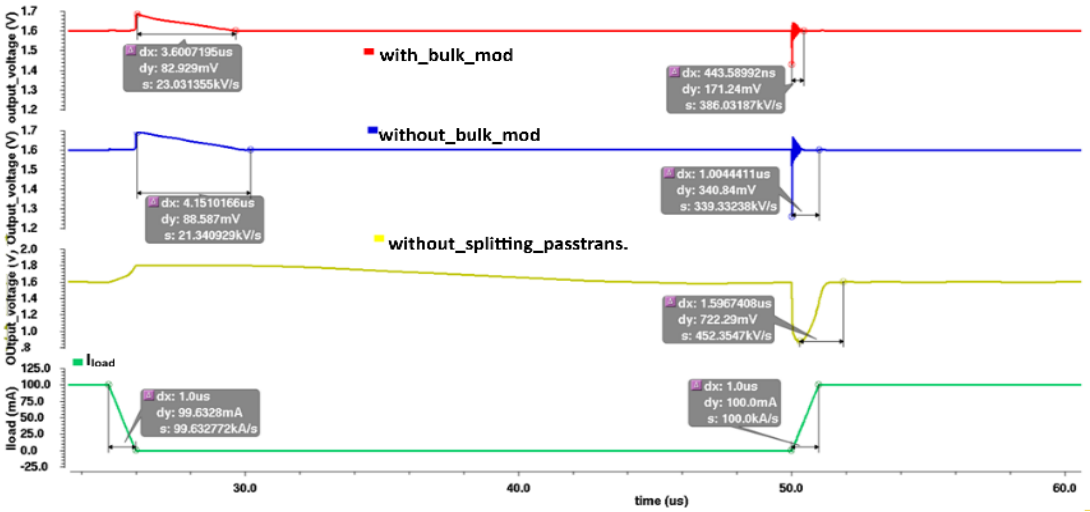

Figure 5.15 Transient responses of LDOs: conventional LDO, segmented pass transistor biased with/without bulk modulation

The impact of pass transistor segmentation and bulk modulation are shown explicitly. An undershoot of 722.29 mV with settling time of 1.59 µs and an overshoot of 200 mV with settling time of almost 10 µs is observed for conventional LDO. Adaptive biasing with pass transistor segmentation reduces undershoot to 340.84 mV and settling time to 1µs. A corresponding reduction in overshoot of 88.58 mV with a settling time of 4.15µs can be observed. The inclusion of bulk modulation further reduces undershoot to 171.24 mV with a settling time of 443.59 ns while restricting the overshoot to 82.92 mV.

The regulator exhibits a load regulation of 0.104 mV/mA as shown in the Figure 5.16. The plot of line regulation is shown in Figure 5.17. It can be seen that it offers a reasonably good regulation of 0.01572 mV/V at full load current.

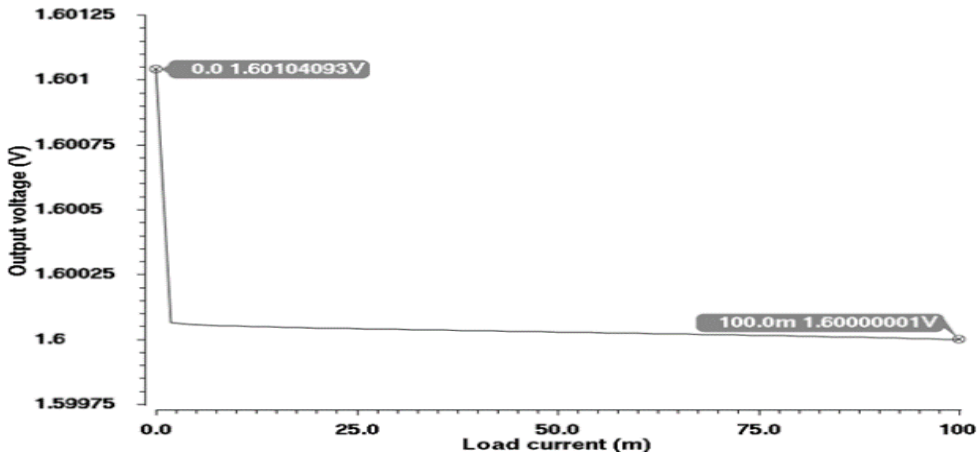

Figure 5.16 Load regulation of the proposed regulator for an input supply voltage of 1.8V

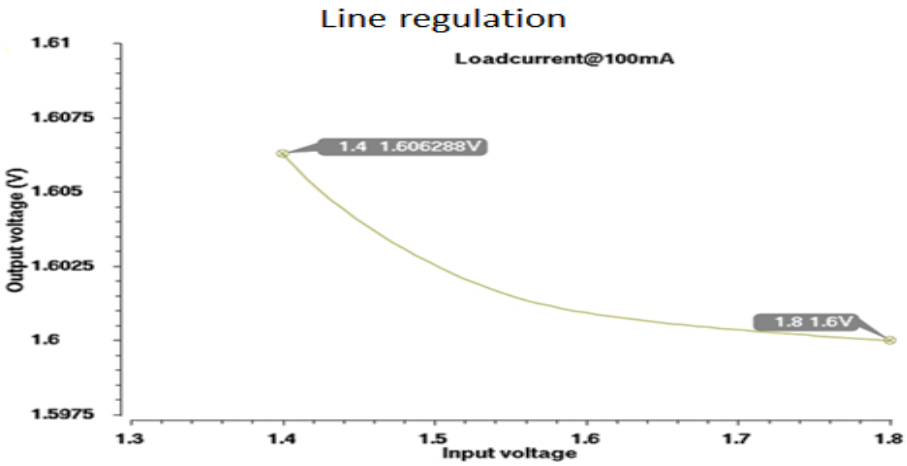

Figure 5.17 Line regulation of proposed regulator at the load current of 100 mA.

The ability of LDO to reject the power supply ripple (PSRR) is demonstrated in the Figure 5.18 by superimposing a 200-mV ripple on the supply. It can be seen that the LDO offers a power supply rejection of -54.53 dB at 10 Hz and -36.18 dB at 1 MHz at full load.

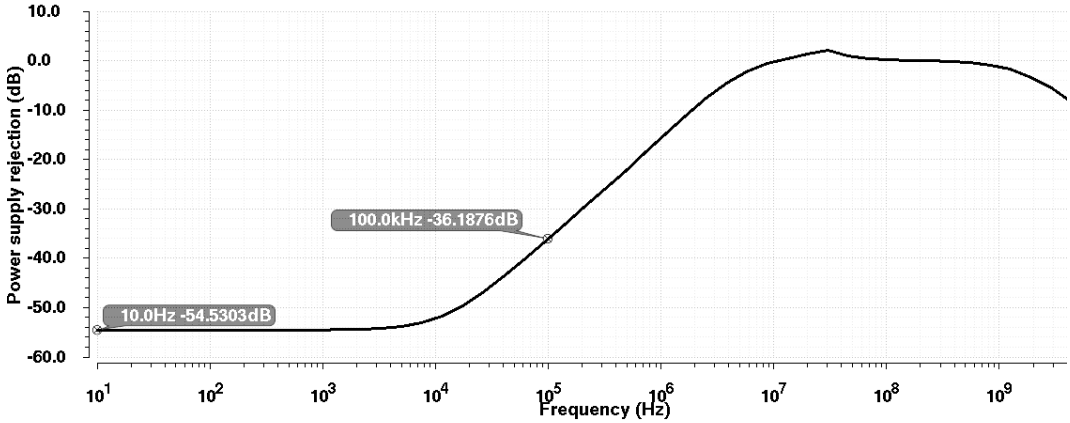

Figure 5.18 Power supply rejection ratio of the proposed regulator at 100mA load current

The variation of quiescent current (I_Q) against the load is plotted in Figure 5.19. The lower load currents up to 2.5mA are supported by the pass transistor M_{p1} while relatively larger load currents are supported by the pass transistor M_{p2} in tandem with M_{p1}.

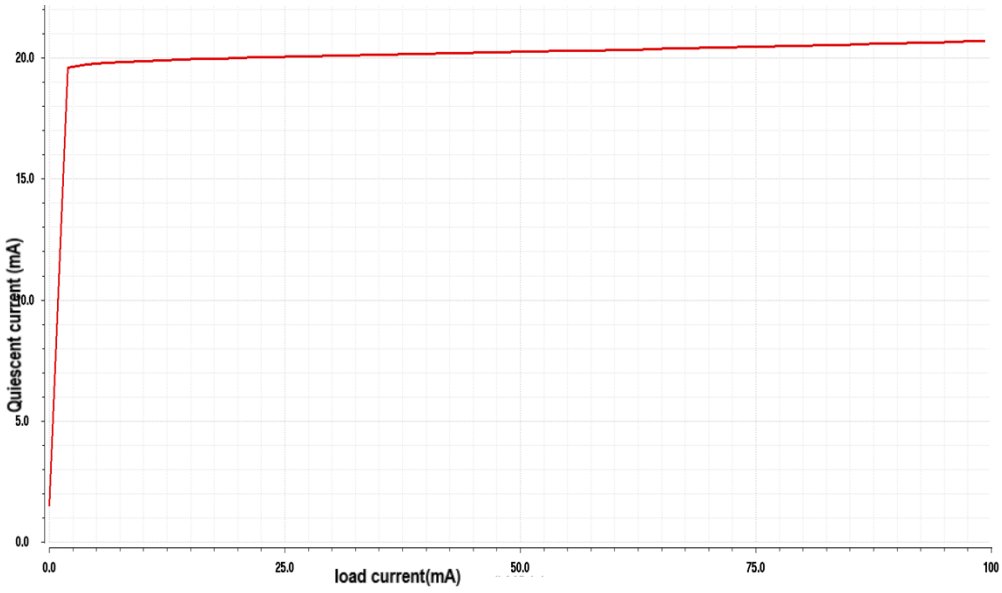

Figure 5.19 Quiescent current consumption as a function of load current

This architecture exhibits a current efficiency η of 99.89% which is evaluated form the following Equation 5.42.

(5.42)

The worst case transient response at different process corners is reported in Table 5.2. It is observed from the tabulated values that the variation in undershoot/overshoot along with settling times is insignificant for the corners TT and FF. However, there is a slight degradation in the performance due to the reduced transconductance of the transistors at the SS corner as shown in the Figure 5.20.

Table 5.2 Tabulated values of transient response at process corners

Process corners	**Undershoot/settling time**	**Overshoot/settling time**
Typical-Typical	162.815mV/427.375ns	84.196mV/4.85µs
Slow-Slow	247.734mV/997.625ns	119.917mV/5.743 µs
Fast-Fast	119.215mV/542.681ns	69.65mV/3.42 µs

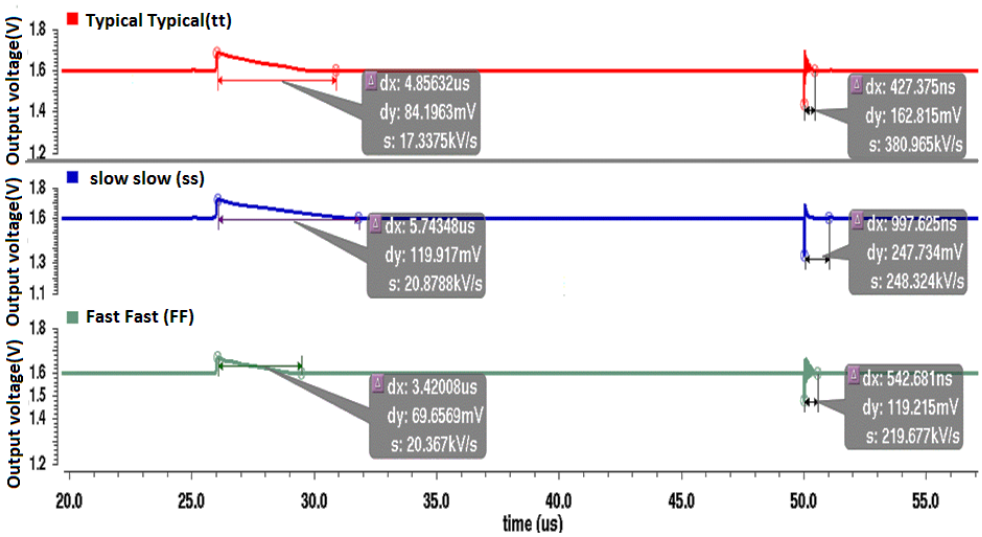

Figure 5.20 Transient response at process corners

The load regulation performance is provided in Table 5.3. It is envisaged from Figure 5.21 that the variation in load regulation is almost negligible with temperature.

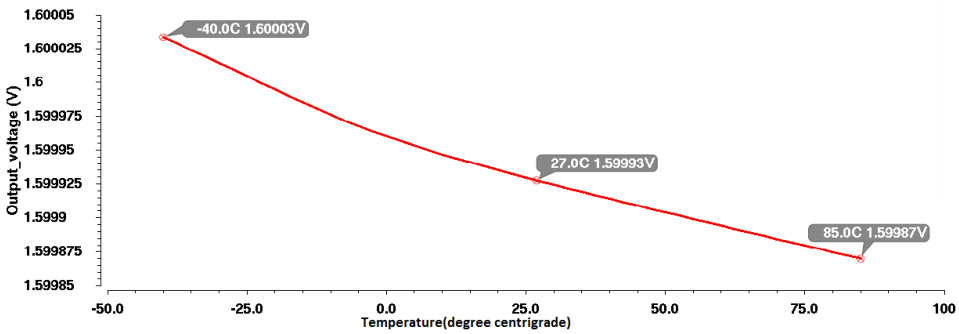

Figure 5.21 Output voltage variation as a function of temperature

Table 5.3 Tabulated values of output voltage as a function of temperature

Temperature(°C)	**Output_voltage(V)**
-40	1.60003
27	1.59993
85	1.59987

The comparison with the latest state of art LDOs is shown in Table 5.4. The architecture presented uses a 40-pF output capacitor similar to that of [25] but consumes a relatively lower quiescent current of 1.5 µA at no load. It can be observed that it improves the transient response by decreasing undershoot and overshoot voltages. Further, an improvement in settling time can be noticed as compared to other state of art LDOs shown in the Table 5.4. Also, an improved load regulation of 0.104 mV/mA can be observed for the LDO presented as compared to its counterparts except [33] which was obtained at the cost of higher quiescent current. The overall performance of architecture is found to be better in terms of figure of merit (FOM) as defined in the Equations 5.39 and 5.40. The improvement in the performance of the LDO is evident from the lowest figures of merit.

$$\text{FOM(settle)}= \tag{5.43}$$

Where T_R is the response time/settling time, I_{Qmin} is the minimum quiescent current and I_{load} is the maximum load current.

$$\text{FOM}_{(alpha)} = \tag{5.44}$$

K= (5.45)

α= (5.46)

Where ΔV_0 is the undershoot voltage, $\Delta I_{0.max}$ corresponds to the maximum load current, and I_Q quiescent current.

Table 5.4 Comparison with related work

Reference	**[68]**	**[58]**	**[31]**	**[33]**	**[25]**	**(This work)**
Year	2007	2010	2010	2012	2016	**2017**
Technology(µm)	0.35	0.35	0.09	0.35	0.18	0.18
Nominal voltage(V)	2.8	1.2	1	1	1.6	1.6
Supply voltage(V)	3	1.4	1.2	1.2	1.8	1.8
Dropout voltage(mV)	200	200	200	200	200	200
Outputcap ()(pF)	100	100	50	100	40	40
Line reg. (mV/V)	23	-	3.78	0.39	-	0.0157
Load reg. (mV/mA)	0.56	0.4	0.1	0.078	4	0.104
Quiescent current ()(µA)	65	43	8	28-380	4.8	1.5
Load current() mA	50	100	100	100	100	100
$\Delta I_{O,max}$ (mA)	50	99	97	100	100	100
Undershoot(mV)	30	70	66	105	170	171.2
Overshoot(mV)	60	40	58	50	200	82.92
Edge time	1000	1000	100	1000	1000	1000
PSRR	< -57 dB@ 1 kHz	-	< -44 dB@ 1 kHz	< -13.15 dB@ 1 MHz	-	< - 36.18 dB@ 100kHz-16dB@ 1 MHz
Current eff@100mA	99.87	99.96	99.98	99.98	99.99	99.89
Vout(pp)(mV)	90	70	124	155	370	254
Cout(pF)	100	100	50	100	40	40
Settling time(µs)	15	4	4	1	4	0.443
FOM(alpha)	77.36	20.10	10.22	28.69	44.4	9.525
FOM(settle)	19.5	1.72	0.32	0.28	0.192	0.0066

To summarize, this topology adapts the biasing to the load conditions in order to improve the transient response. It also exploits the bulk modulation to absorb the load transients swiftly which in turn helps in reduction of over/undershoots. The control section is designed carefully to perform multiple functions. Primarily it serves the purpose of

controlling the switching instance of the segmented pass transistor. Secondly, it improves the slew rate at the gate of pass transistor $M_{p2.}$ In addition, it obviates the quiescent current variation beyond the requisite range of load currents thus conserving the power.

The frequency compensation sustains stability for the entire range of load currents. Although this LDO topology requires slightly higher quiescent at full load as compared to [25], the improved transient response, high current efficiency, and settling time trade off better and is suitable for applications that demand quick response in the order of nanoseconds. The corresponding layout is shown in Figure 5.22.

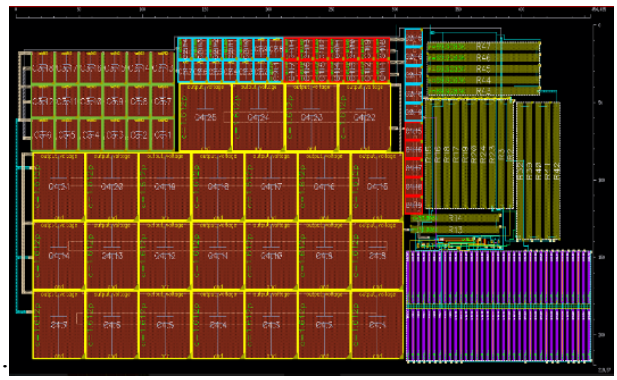

Figure 5.22 Layout of bulk modulated LDO regulator

5.3 Adaptively Biased LDO with Bulk Modulation and Augmented Transient Response

The performance of adaptively biased LDO with pass transistor segmentation and bulk modulation is limited by the maximum leakage current of the pass transistor. On the other hand, enhancing the adaptation of biasing to load current transient's further increases overall

quiescent current. Also, in this topology as the output capacitance is restricted to 40pF to conserve silicon space, it further constrains the transient performance. An alternate approach is explored to improve the performance further without disturbing the adaptive biasing and bulk modulation effects. Thus, an attempt is made to improve the performance further, using a transient supplementing path as shown in Figure 5.23.

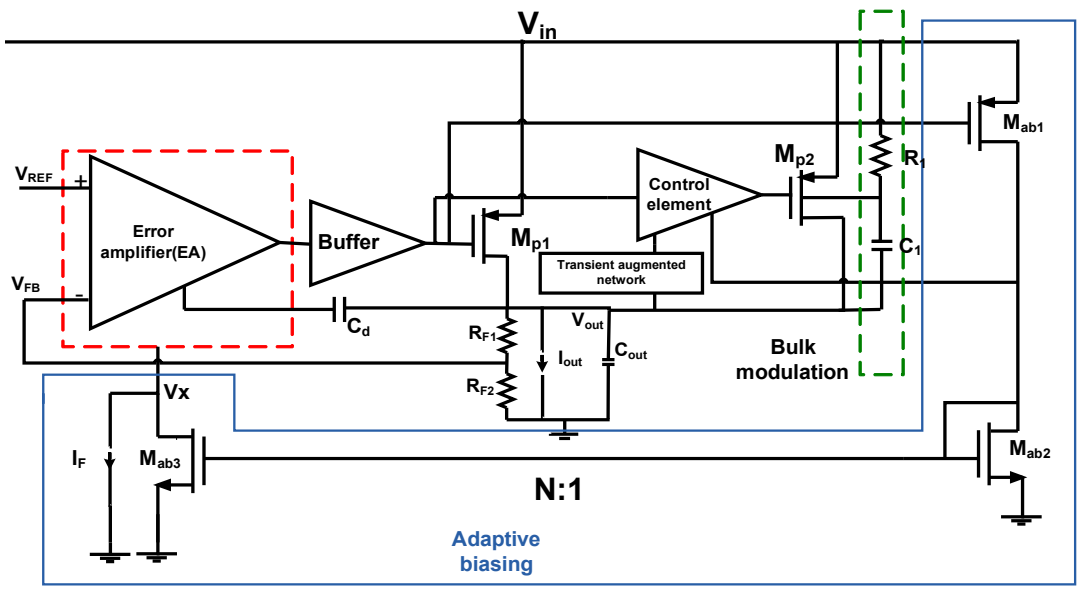

Figure 5.23 Block diagram of adaptively biased LDO with bulk modulation and augmented transient Response

Transient Response Augmentation

The schematic corresponding to adaptively biased LDO with bulk modulation and augmented transient response is shown in the Figure. 5.24. It employs a control section comprising M_{c1}-M_{c2}-R_e-C_e-M_{p2}-V_{out} in the feedback that aids in attaining a fast settling with reduced over/undershoots during load transients. In addition, this optimizes quiescent current in the control section to conserve power. Here an attempt is made to couple the output voltage variations due to the load transients swiftly to the control section in such a way that it hastens the corrective mechanism. In this direction, load transients are quickly transmitted to the source node of the transistor M_{c2} using a capacitor Ce in association with a resistor R_e as shown in Figure 5.24. This configuration forms a transient augmented network coupling the output voltage (V_{out}) variations to the adaptively biased control section thereby improving the slew rate drive at the gate of pass transistor M_{P2}. The output voltage variations are coupled

through the transient augmented network to the source terminal of transistor M_{c2} modifying its overdrive voltage during load transients. This triggers corresponding changes to the gate voltage of the pass transistor M_{p2} leading to a faster control of the regulated output voltage.

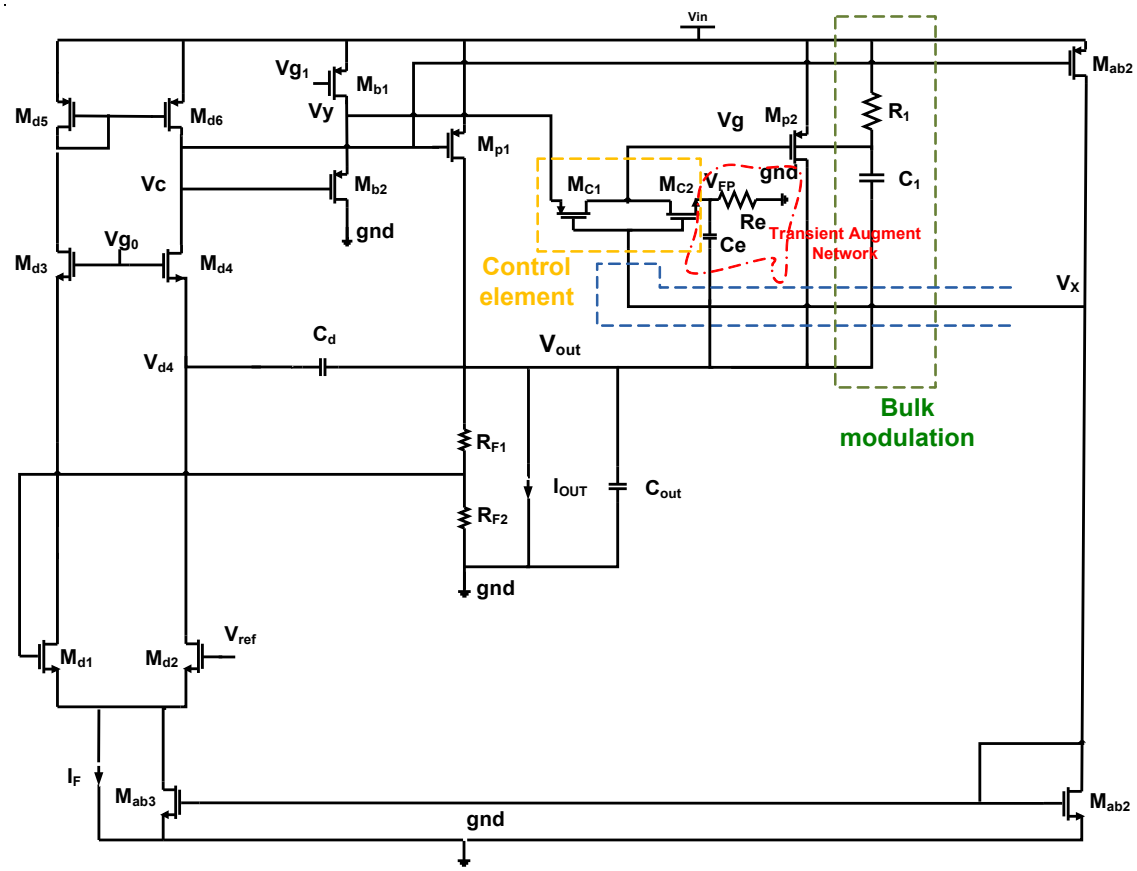

Figure 5.24 Transient augmented network(Tan) based capacitor-less LDO regulator

The voltages and currents at different nodes of control unit during overshoot as a result of load transient from high to low are shown in Figure 5.25. The sequence of waveforms represents the pass transistor (M_{p2}) gate voltage Vg, transistor M_{c2} source voltage V_{FP} and the control element current I_{MC2} with and without transient augment network. It reveals that the corresponding voltages/currents react relatively faster with the application of transient augmented network segment which can be seen from the relatively sharp slope. This facilitates fast charging and discharging of the large value of pass transistor (M_{p2}) gate capacitance leading to improved transient response.

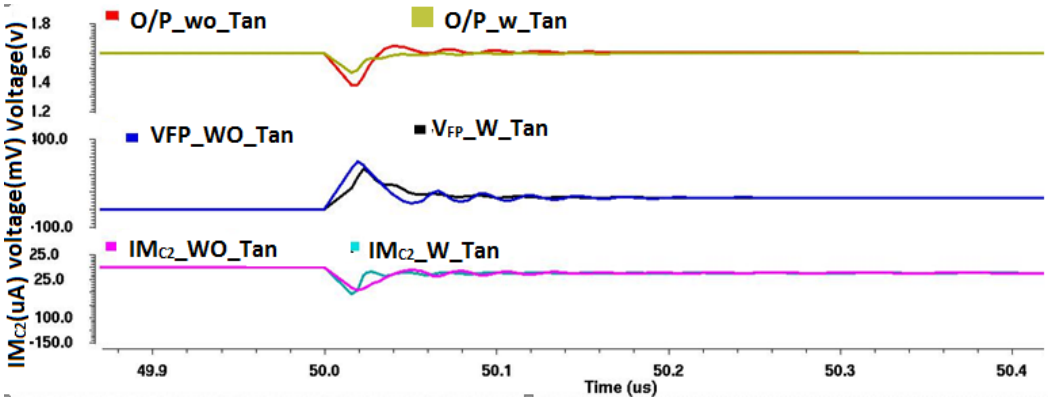

Figure 5.25 Transient voltages and currents of regulator

1.1.19 Design and Analysis

A simple RC network augments the performance by coupling variations at the load to the gate of pass transistor. The corresponding differentiator capacitance can be obtained by equating charge required to change voltage at the gate of pass transistor to that of output. However, this capacitance is relatively large so an R_eC_e network with control section as shown in the Figure 5.24 is used. It facilitates quick response with a small capacitor.

Considering the case of sudden increase in load it pulls source potential of M_{C2} in control section. This in turn increases its V_{gs} thereby sinking more current through it. Consequently, the voltage at the gate of pass transistor is pulled low facilitating the pass transistor M_{p2} to source more current to the output node (V_{out}) as required. During this course of operation, the bulk to source potential (V_{bs})of M_{C2} increases, V_{th} decreases and thereby augmenting the current as per the load demand. The "R_eC_e" time constant should be chosen such that the capacitor should discharge at a relatively slower rate retaining the voltage drop at the gate of pass transistor till it could influence the requisite current changes.

The application demands the regulated voltage to settle within 500ns. The time constant of this circuit is selected such that it maintains V_{FP} for a time period ~~comparable~~of one third of settling time mitigating the possible ringing effect due to ~~Under~~degraded phase margin that may arise by the virtue of pass transistor current enhancement. With these considerations the time constant is calculated as τ_{ReCe}=150ns. Let us consider Re=10k so that,

So, ==15pF

This large value of capacitor is required if the output transitions are to be passed instantly to the gate of pass transistor. However, the control section and pass transistor contributes a gain of 24dB i.e a factor of 20 which facilitates to reduce the capacitance value selection.

=> pF

So, =10K and1pF is selected.

1.1.20 Results and Discussion

The transient augment feedback loop M_{p2}, , should maintain its gain below unity for stability of the regulator. The frequency response of the main feedback loop and transient augment network loop is plotted in the Figure 5.26. It can be seen that the main feedback loop does not interact with the transient augment loop thus sustaining stability.

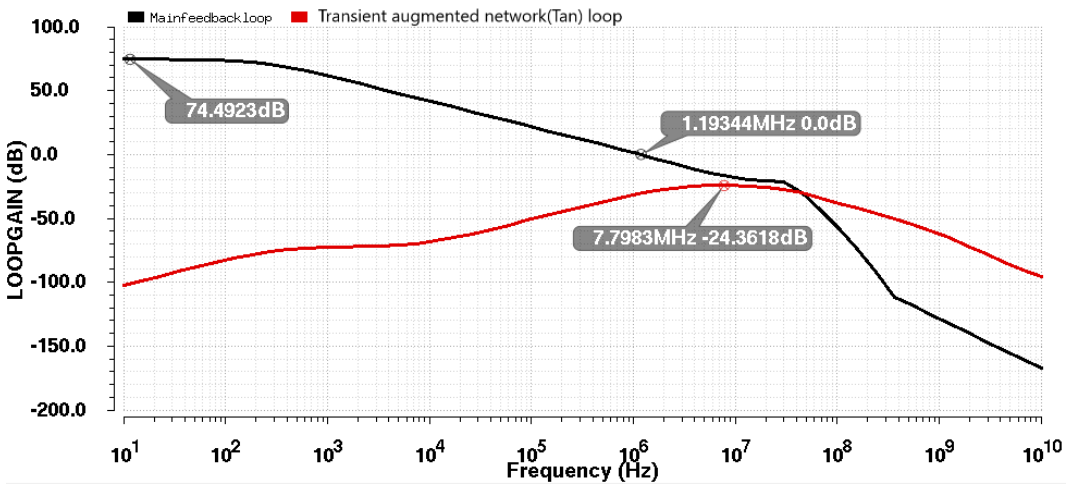

Figure 5.26 Frequency response of the Tan loop and main feedback loop

The frequency response for the LDO regulator is shown in Figure. 5.27. The regulator operates with a dc gain of 69dB at zero load current while it is 78.82dB at 100mA load current with a unity gain frequency of 445kHz at no load while 1.193MHz at full load. The phase margin is 84.10^0 at 1.193MHz.

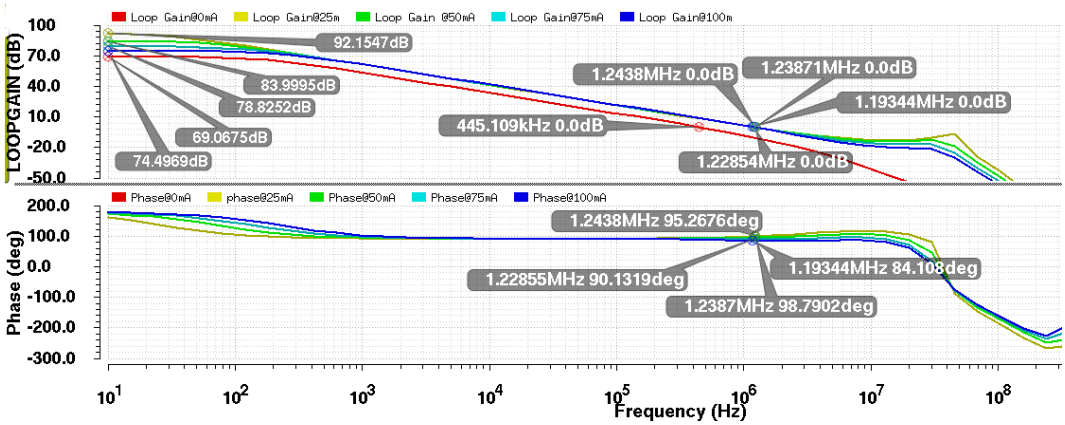

Figure 5.27 Frequency response plot for different load currents

The stability of the LDO regulator topology presented is examined by plotting the variation of phase margin and unity gain frequency over the entire load current range which is shown in Figure. 5.28

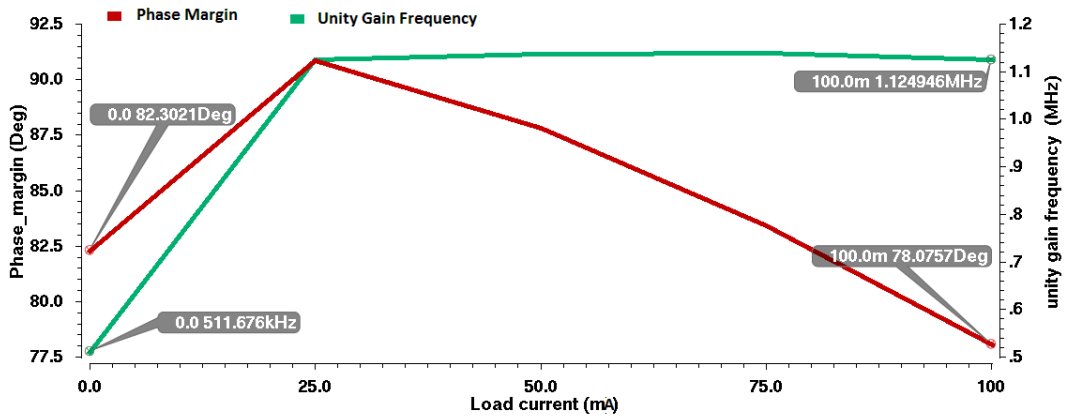

Figure 5.28 Phase margin and unity gain frequency as a function of load current

The adaptive biasing architecture imposes the changes in the unity gain frequency proportional to load current. The pass transistor supporting lower load current below 20mA contributes to a pole whose position relative to the unity gain frequency determines the phase margin. As the load current increases the output pole movement relative to unity gain frequency increases resulting in increase in phase margin. As the second pass transistor comes into action, the adaptive biasing is controlled in such a way that the unity gain frequency changes little and the relative position of second pass transistor pole with unity gain frequency causes phase margin to decrease. At no load/low load currents, the pole at the output (say P_L)

is dominant and pole due to the error amplifier output impedance in association with pass transistor gate capacitance forms non-dominant pole (P_{eapg}) as shown in Figure 5.29.

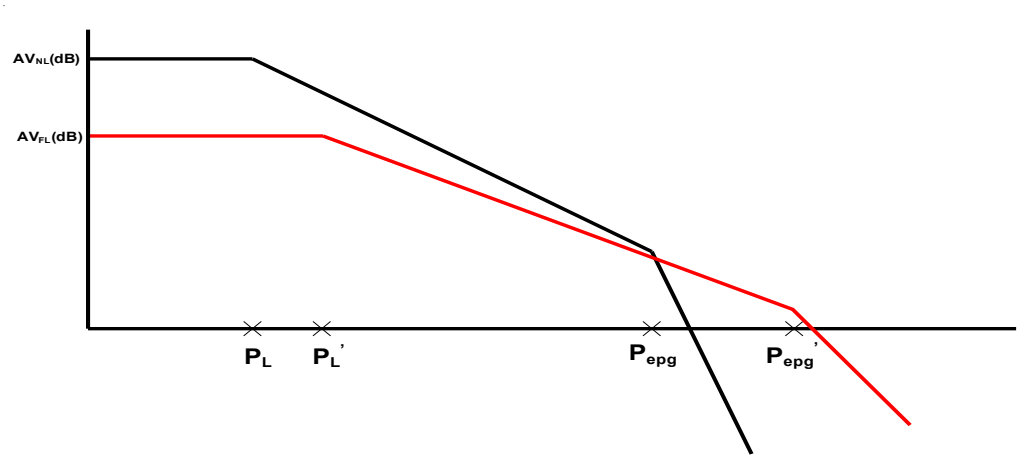

Figure 5.29 Pole movement for different load currents

At this juncture, it is assumed that the overall DC gain is at least 10 (20dB) which ensures almost 90^{o} phase shift due to P_L. Now as I_L increases, P_L moves away from the origin (towards P_L'). Also gain decreases as I_L increases (r_o decreases) which increases UGF though slightly. E.g. I_L is doubled, gain decreases times. Phase margin is completely decided by the ratio of non-dominant pole i.e. P_{eapg} to UGF. Also, as I_L increases, P_{eapg} moves towards high frequencies (towards P_{eapg}') since error amplifier output impedance (r_o) decreases. Adaptive biasing further increases the bias proportionate to load increment which increases phase margin. Once the load reaches sufficiently large value, the pass transistor M_{p2} will be turned on. It makes the non-dominant pole P_{eapg}' to move closer to P_L degrading the phase margin. Under these conditions the adaptive bias is made deliberately less effective which justifies further the decay in phase margin. However, care is taken such that requisite phase margin is maintained throughout the load range.

The transient response plots for adaptive bias with and without bulk modulation and adaptive bias with transient augment network along with bulk modulation is shown in Figure 5.30 and Figure 5.31 for overshoot and undershoot respectively for a load change of 0 to 100mA with a rise and fall time of 1µs. From the plot it can be seen that the overshoot and settling time are 140mV/6.353µs, 101.74mV/4.678µs and 95mV/4.358µs for the three topologies under consideration. Also, the corresponding undershoot can be observed to be

298mV/372ns, 218mV/261ns and 134mV/240ns. Thus, a significant improvement in the performance can be observed across the topologies progressively.

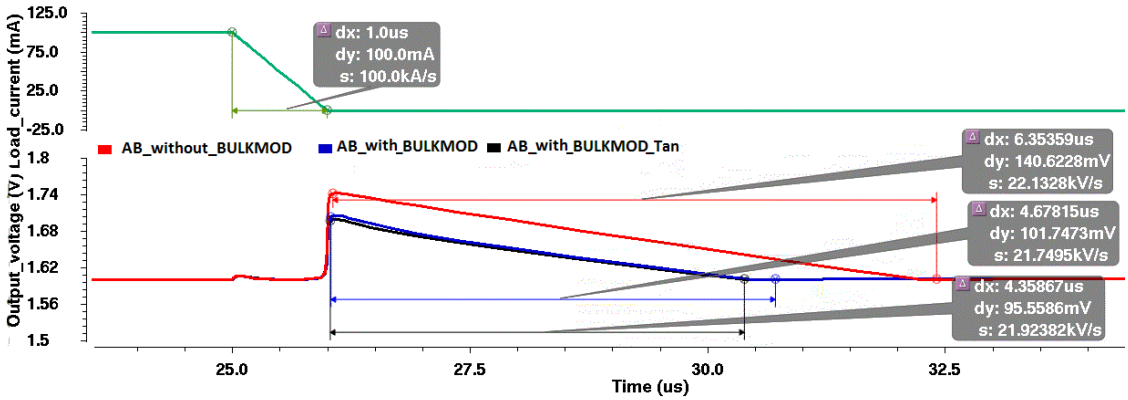

Figure 5.30 Transient response (overshoot) for 100mA to 0mA load

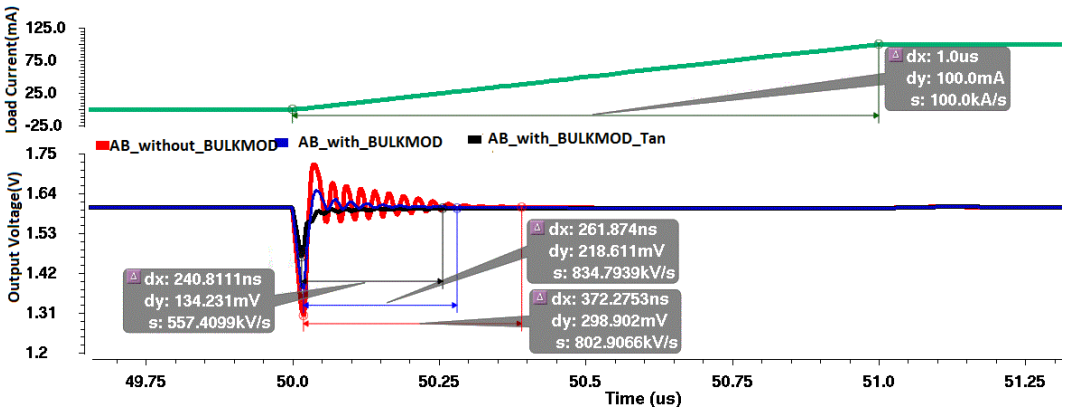

Figure 5.31 Transient response(undershoot) for 0mA to 100mA load

The adaptively biased LDO with segmented pass transistor using augmented transient path consumes a total quiescent current of 16.5µA which is distributed among different stages as 1.5µA for the error amplifier, 6.28µA for the buffer circuit, 5.9µA for the control element while the rest is shared by the current sensing circuit.

The transient response during overshoot/undershoot across the process corners is shown Figure. 5.32 and Figure. 5.33 respectively. It can be observed that the performance is not degraded much from fast to slow corners.

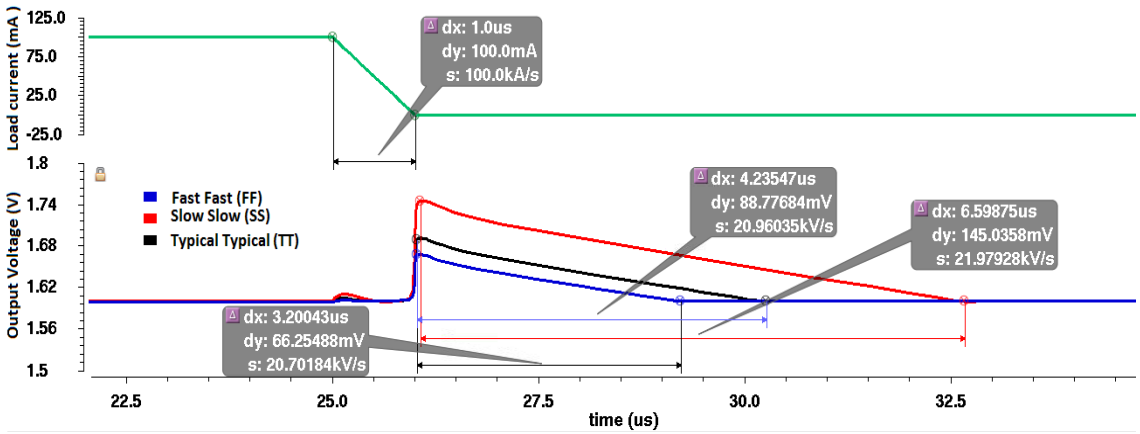

Figure 5.32 Transient response(overshoot) of the regulator @100mA for different process corners (ss- slowslow, ff-fastfast, tt-typicaltypical)

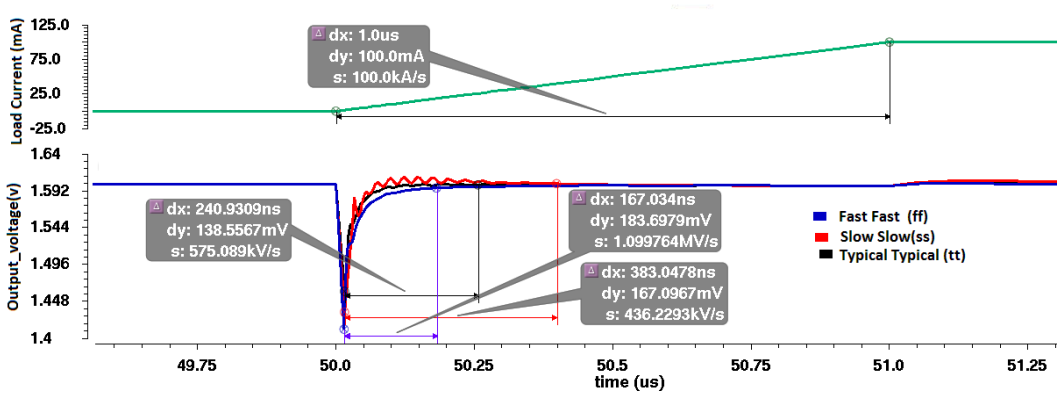

Figure 5.33 Transient response(undershoot) of the regulator @100mA for different process corners (ss- slowslow, ff-fastfast, tt-typicaltypical)

The dc performance metrics load/line regulation determine the ability of a regulator to maintain a constant output voltage against changes in the supply or load. The line regulation is plotted in Figure 5.34 at load currents of 100µA and 100mA for the LDO with transient augmented network.

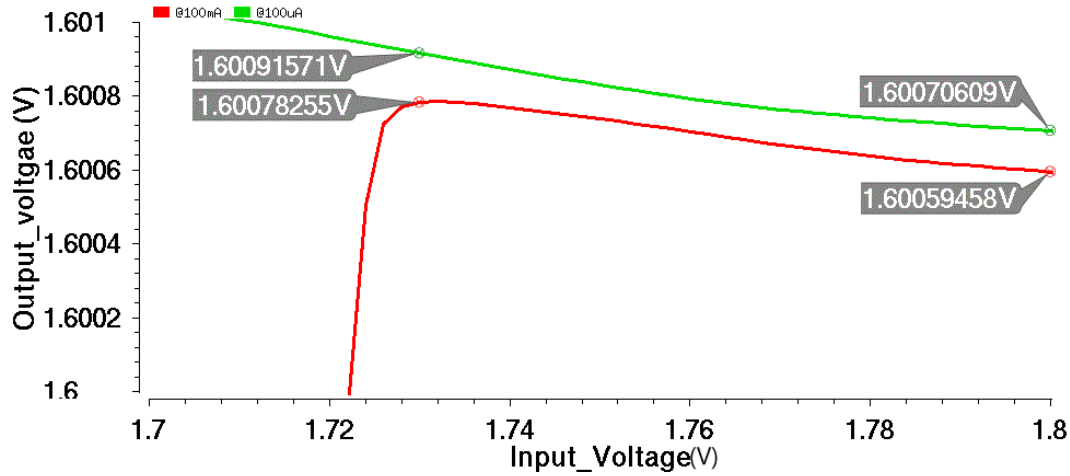

Figure 5.34 Line regulation for load current 100µA and 100mA

With reference to above plot shown in Figure. 5.34, these curves should coincide with each other against the input voltage deviation in case of zero load regulation. However, the gap between them portrays a finite load regulation. It exhibits a load regulation of 2.1mV/V for 100µA and 1.9mV/V at full load of 100mA. The load regulation is plotted by sweeping current from absolutely no load (0mA) to full load (100mA) as shown in Figure. 5.35.

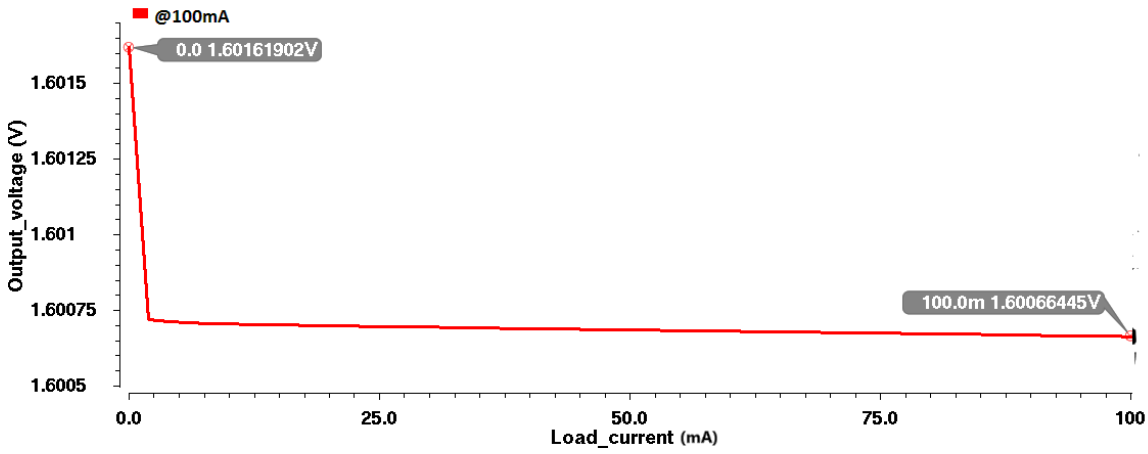

Figure 5.35 Load regulation for load current varying from 0 to 100mA

The change in the output voltage is restricted below 0.95mV over the entire load current range from 0 to 100mA.This translates to a load regulation of 0.095µV/mA. The load regulation across the process corners is plotted in Figure 5.36.

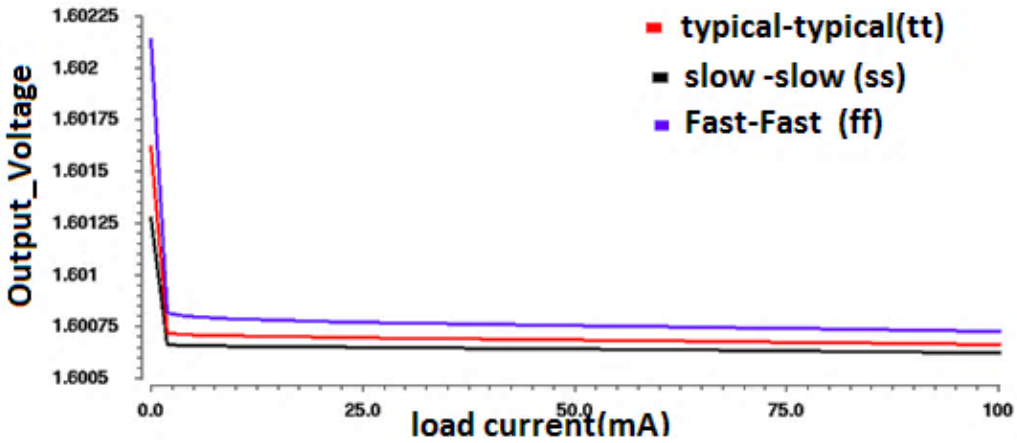

Figure 5.36 Load regulation at different process corners

The performance of the LDO regulator is plotted against temperature variation in Figure 5.37. The output voltage variation is observed to be within 1.663mV/^{0}C at 100µA load current while at 100mA the variation is 1.703 mV/^{0}C.

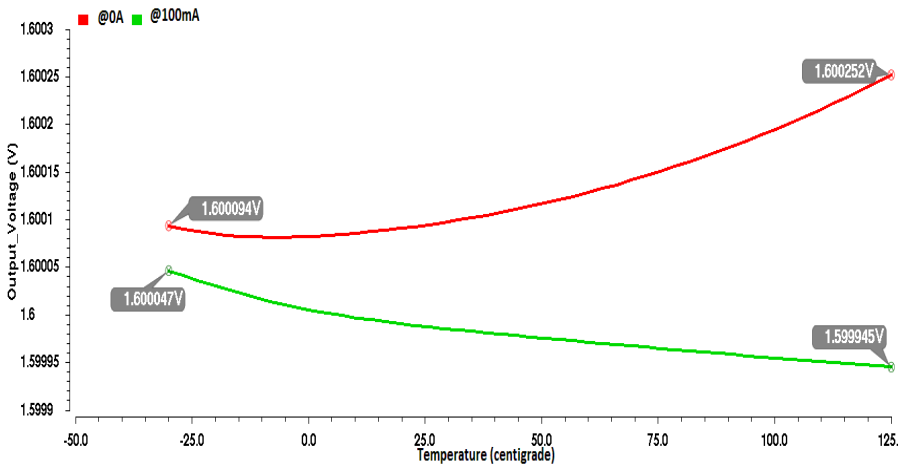

Figure 5.37 LDO response against temperature variation for 100mA load

The output noise power spectral density of the proposed LDO versus frequency is demonstrated in Figure. 5.38

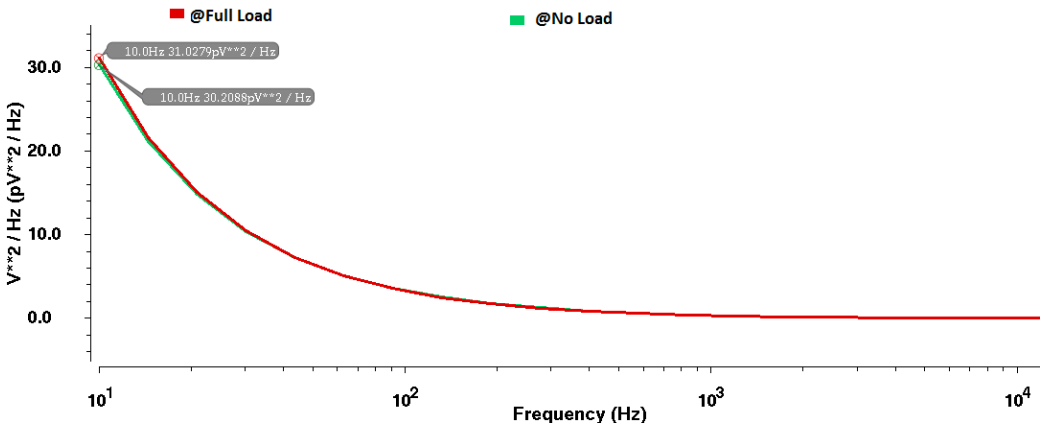

Figure 5.38 Power Spectral Noise density of the proposed LDO

The spot noise at DC frequency is 30.20pV²/Hz and 31.02 pV²/Hz at no-load and full-load conditions. The error amplifier and feedback resistances are the dominant sources of LDO noise. The small feedback resistance reduces its contribution to the noise but unnecessarily increases the LDO quiescent current consumption.

Table 5.5 The performance analysis of state of art capacitor-less LDOs

Parameter	[25]	[34]	[36]	[65]	[28]	[29]	This work
Technology	0.18	0.18	0.18	0.18	0.13	0.35	0.18
V_{in}(V)	1.8	1.4	1.5	1.2	1.2	2.0	1.8
V_{out}(V)	1.6	1.2	1.2	1.0	1.0	1.8	1.6
Dropout(mV)	200	200	300	200	200	200	200
Undershoot(mV)	170	110	125	342	140	89	134.2
Overshoot(mV)	200	85	65	192	90	129	95.5
ΔV_{out}(pp)	370	195	190	534	230	218	229.78
I_{qmin}(µA)	4.8	0.61	2.4	14	27	50	1.5
I_{qmax}(µA)	6	141	242	14	27	50	16
ΔI_{load}(mA)	100	99.99	99.9	100	99.99	100	100
Edgetime(ns)	1000	1000	300	1000	300	1000	1000
I_{load}(mA)	100	100	100	99.95	100	100	100
Cout(pF)	40	100	100	100	80	100	40
Sett.time(µs)	4	2	0.8	1.5	2.5	1.5	0.26
FOM(Alpha)(µV)	38.59	478.09	247	129.98	62.10	50.125	63.92
FOMsettle(µs)	0.192	0.0122	0.0192	0.21	0.675	0.75	0.0039

The performance parameters comparison of the proposed topology with the state of art LDOs is tabulated in Table 5.5. The presented regulator consumes the lowest quiescent

current of 1.5 µA at lower load current, a small output capacitor of 40pF, comparatively lower peak to peak output voltage variation and lowest settling time relative to the similar concern reported in [25]. The LDO reported in [28] have transient response comparable to the presented work but have a large output capacitor(80pF) and settling time (2.5µs). The peak to peak output voltage variation in [34] and [36] have a relatively less peak to peak voltage variation compared to the presented work as the load current is changed from 100µA to 100mA and employed a large output capacitor of 100pF but have a large settling times of 2µs [34] and 0.8µs [36]. A Figure of merit (FOM) that relates response time, minimum load current and dynamic load current is used and the presented work with lowest FOM of 0.0039µs is useful for portable applications. Layout is shown in Figure 5.39.

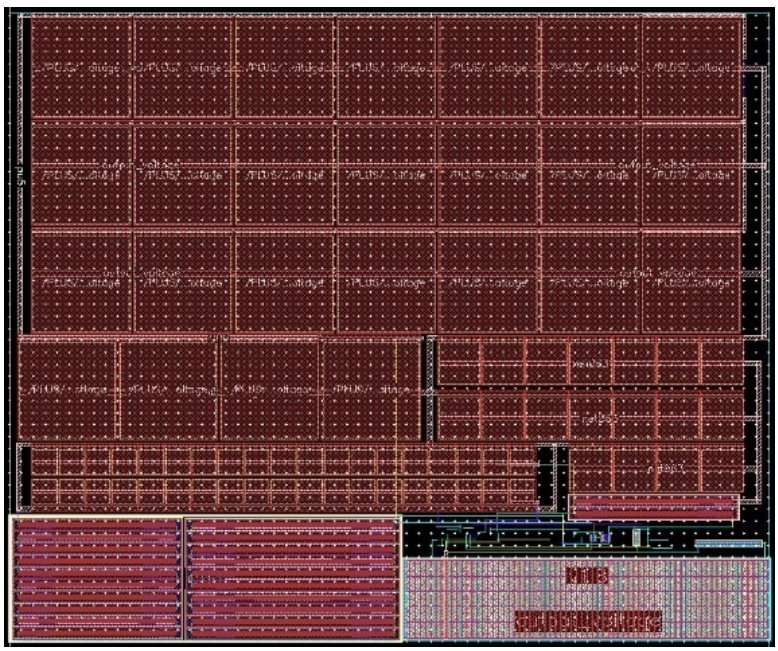

Figure 5.39 Layout of transient augmented LDO regulator

Chapter 6

Conclusions and Future scope

In this thesis an attempt has been made to explore different circuit strategies that will improve performance of on-chip LDO voltage regulator suitable for mobile applications including DDR3 IO circuits. Different circuit topologies are presented that trade off among the corresponding design challenges viz., transient response, stability, area and power consumption using 180nm CMOS technology to deliver nominal output voltages ranging from 1.4 to 1.6V for the load variation of 0 to 100mA with a dropout voltage of 200 mV and a least quiescent current consumption of 1.5µA.

A LDO voltage regulator topology with improved folded cascode error amplifier was presented that enhances trans-conductance improving DC gain and unity gain frequency. This is augmented using an auxiliary loop with a very small compensation capacitor of 500fF achieving a good transient response and load regulation of 20.6µV/mA. This topology achieves current efficiency of 99.66% for a quiescent current of 64.1µA with an undershoot voltage of 89.9mV and a settling time of 719ns. This ensures better stability even at no load currents by pushing the non-dominant poles away from unity gain frequency. LDO based on segmented pass transistors and multiple error amplifiers could improve the current efficiency

by consuming quiescent current of 40μA while saving silicon space. An adaptively biased error amplifier along with segmented pass transistors with bulk modulation could limit quiescent current further to 20μA while providing very good stability with a phase margin of 70.37^0 even at no load current.

LDO regulator based on multiple loop control topology with a simple transient augmented path could strike better trade-off between quiescent current (16μA) and transient response (with a settling time of 260ns and under shoot voltage of 139mV).

It is observed that an attempt to reduce settling time increases overshoot and undershoot. Stability at no load currents requires special attention. LDO topologies biased adaptively to load transients could conserve quiescent current. Also pass transistor segmentation with bulk modulation is found to improve transient response of the on-chip LDO voltage regulators making them suitable for mobile applications.

6.1 Future scope

In this thesis an attempt was made to improve the transient response by segmenting the pass transistor into two transistors only. Multiple segmentation of the pass transistors will facilitate to design a digitally assisted LDO that can exploit usage of state of the art scaled down technologies which offers re-configurability. However, this trades off with the accuracy of the regulator. Power Supply Rejection Ratio can be improved to meet the accuracy demand of the analog front end and sensor applications.

Recent eruption of IoT demand deft power management schemes. DC-DC regulators along with LDO voltage regulators can be designed based on energy harvesting techniques to address ultra-low power needs of IoT applications.

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List of Publications

1. Suresh Alapati, Sreehari Rao Patri & K. S. R. Krishna Prasad, **An adaptively biased capacitor less low dropout regulator with improved transient response**" in *J CIRCUIT SYST COMP* Vol. 26, No. 10, p.p- 1750146-1-35, October 2017. (SCI).

2. Suresh Alapati & Patri Sreehari Rao "**Capacitor less voltage regulator with split drive error amplifier for segmented pass transistors"** in *J. Low Power Electron.* Vol. 14, p.p-1–8, 2018(ESCI).

3. Suresh Alapati & Patri Sreehari Rao "**A low quiescent current fast settling capacitor-less low dropout regulator employing multiple loops**" in *Indonesian Journal of Electrical Engineering and Computer Science* Vol. 10, No. 3, p.p- 1070-1079, June 2018(SCOPUS).

4. Suresh Alapati & Patri Sreehari Rao "**Improved transient response capacitor less low dropout regulator employing adaptive bias and bulk modulation**" in *Turkish Journal of Electrical engineering and Computer science.* (SCI).

Appendix A

Band Gap Reference

The low dropout regulators require a constant reference voltage that is independent of temperature and supply variations. A constant reference voltage is usually achieved by making use of principle of band gap reference. It employs a complementary to absolute temperature(CTAT) generator based on negative temperature coefficient of PN junction and proportional to absolute temperature(PTAT) generator. The schematic is shown in Figure A.1.

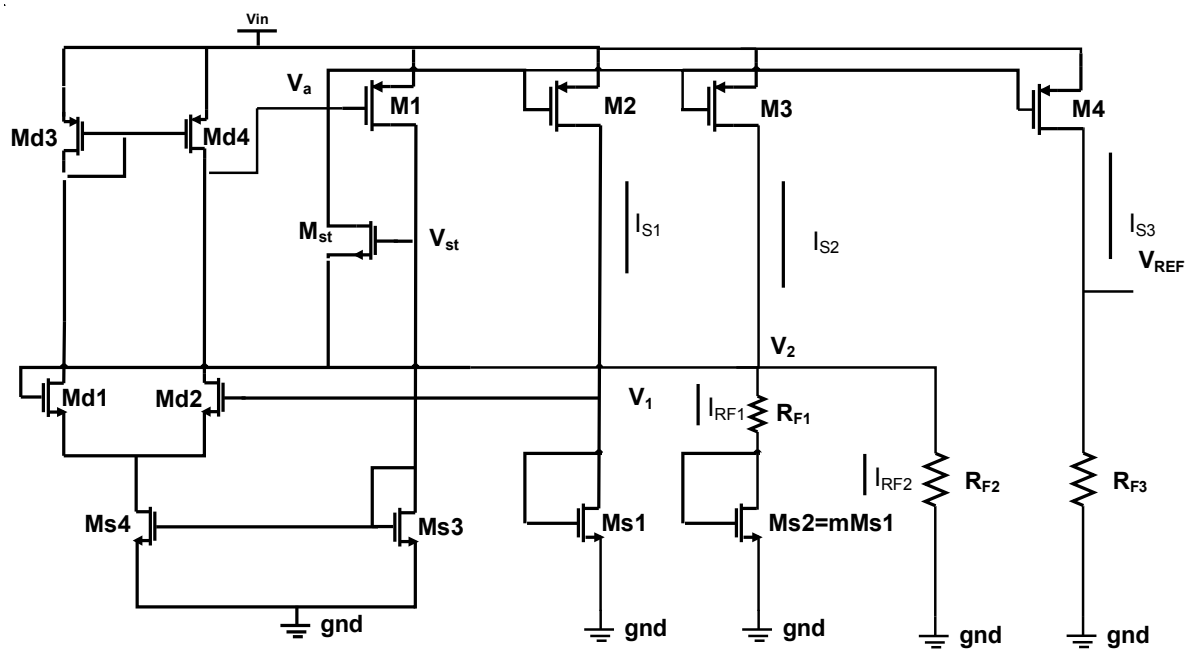

Figure A.1 Schematic of band gap reference

A band gap reference is designed to supply a constant reference voltage of 900mV which is independent of process and temperature variations. This circuit is designed using only MOSFETs operating in subthreshold region to conserve power [69].

Bandgap reference design

The circuit is designed such that $I_{s1}=I_{s2}=I$. The Vgs of M_{s1} and M_{s2} are related to current I_{s1} and I_{s2} as given in the following Equations.

$$= n\ln [\ ]+$$

$$= n\ln[\ ]+$$

Applying KVL around the loop consisting of transistors M_{s1} M_{s2} and resistor $R_{F1,}$ we have

$$=n\ln (m)$$

The current varies proportional to temperature as defined as

$$= n\ln(m)$$

While varies inversely proportional to temperature following the relation as shown below

Finally, and produce voltages that have positive temperature coefficient and negative temperature coefficients respectively satisfying the requirements of bandgap reference. So can be represented as

The desired reference voltage is generated by adjusting R_{F3}. The performance metric used for the BGR i.e temperature coefficient (TC) is given in the following equation

$$TC =$$

The BGR is designed for 900mV with a temperature coefficient of 5.33 ppm/°C over temperature range of -40^0 to 125^0C that consumes 12 µW at room temperature.

Appendix B

Power Supply Rejection Ratio

A general electric circuit consisting of different nodes is characterized by a transfer function between them. However, the transfer function from input node (V_{in}) to the output node (V_{out}) and power supply node(V_{dd}) acquire due importance. Its characterization is done through a suitable block diagram shown in Figure B.1.

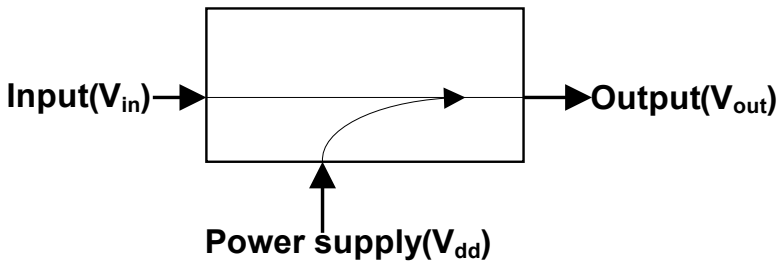

Figure B.1 General electric circuit block diagram

The capability of an electric circuit to suppress any power supply variations to its output signal is power supply rejection ratio(PSRR). The PSRR is defined as ratio that correlates the transfer function of the power supply node(V_{dd}) to the output node (V_{out}) represented by (As (ω)) and the transfer function of the input node(V_{in}) to the output node(V_{out}) represented by open loop transfer function $A_{loop}(\omega)$. The power supply rejection ratio(PSRR) is stated as Equation B.1

$$\text{PSRR }()=20.\ \text{Log} \qquad \text{(B.1)}$$

Where parameter $A_s(\omega)$ is the reciprocal of the power supply gain commonly termed as PSR (Power Supply Rejection), it is distinct from PSRR. It is observed from Equation B.1 that PSRR is proportional to $A_{loop}(\omega)$ and inversely proportional to $A_s(\omega)$, consequently if As(ω) decreases the PSRR is increased and if the open-loop gain $A_{loop}(\omega)$ is increased, the

PSRR is improved. The basic sub-block of LDO that contributes to the improvement of open loop gain is error amplifier.

The Equation B.2 shows the relationship between the parameters output node(V_{out}), input node(V_{in}), power supply node (V_{dd}),open loop transfer function (), and power supply transfer function ().

$$=.V_{dd} + .V_{in} \quad \text{(B.2)}$$

The Equation B.3 reveals the relationship between the output voltage(V_{out}) and reference voltage(V_{REF}) as a function of feedback resistances R_{F1} and R_{F2} . The reference voltage(V_{REF}) is generated by a bandgap reference that is supposed to present low noise characteristics and high immunity to power supply variations.

$$V_{out} = V_{Ref}(1+) \quad \text{(B.3)}$$

The contribution of noise generated in bandgap reference is considered negligible and thus the variations of V_{out} due to supply noise and input for a typical LDO shown in Figure B.2 is given by Equation B.4.

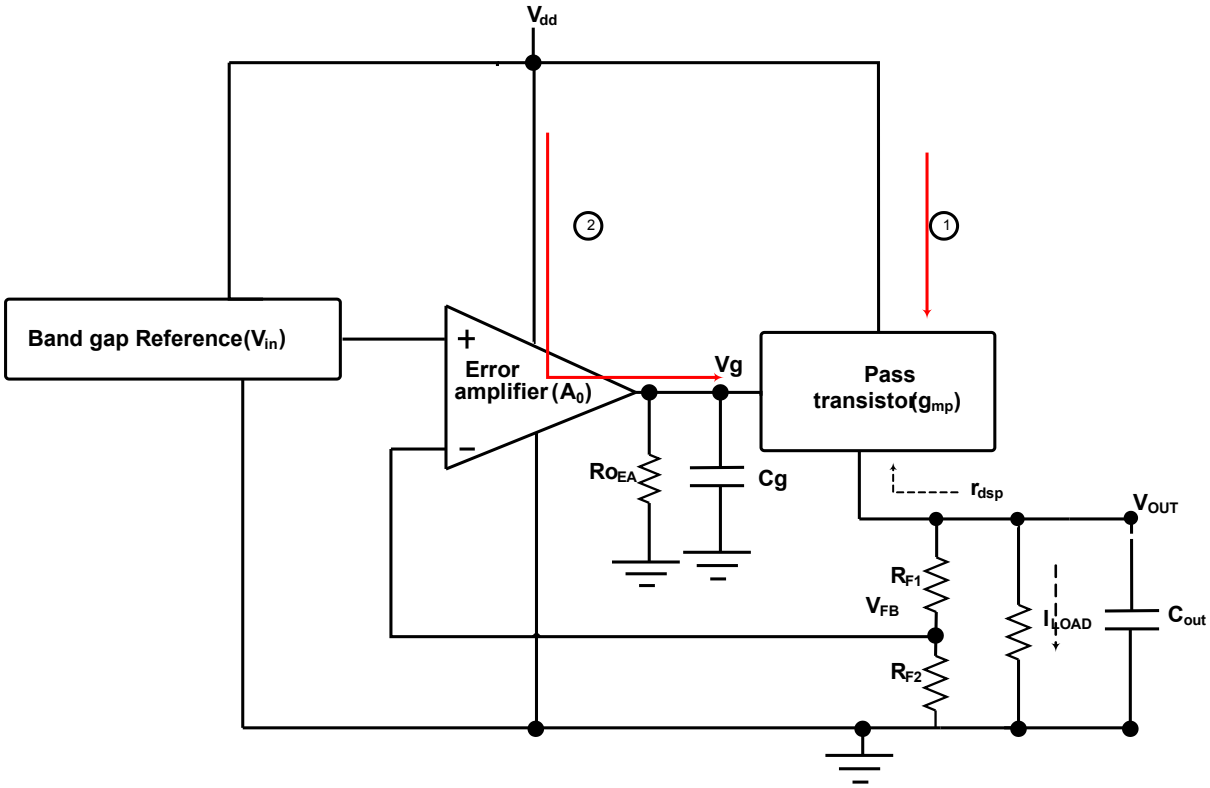

Figure B.2 Power supply rejection ratio of a typical LDO

$$=.V_{dd} + \ .-() \qquad \text{(B.4)}$$

$$V_{dd} \qquad \text{(B.5)}$$

$$\text{So} = \qquad \text{(B.6)}$$

$$\text{PSRR(dB)}=-20\text{Log}_{10}(\text{change in } V_{out}/\text{change in } V_{dd}) \qquad \text{(B.7)}$$

Where the factor in the Equation B.6 corresponds to the open loop gain (A_{loop}),while is the open-loop gain of the error amplifier, β is the feedback factor $R_{F2}/ (R_{F1} + R_{F2})$, and are the transconductance and drain-to-source resistance of the pass device, respectively.

It is observed that the PSRR improvement is possible with an increase in the error amplifier gain or/and reduce the gain factor 1/β which is typically large for low power

consumption. Additionally, the aspect ratio of pass device and the current required for its operation also influence the PSRR and must be given due consideration.

Appendix C

Stability analysis of CONV_LDO

The stability of conventional LDO Regulator (CONV_LDO) is analyzed through a small signal equivalent circuit shown in Figure C.1 is the small signal equivalent circuit diagram representation of the conventional LDO(CONV_LDO).

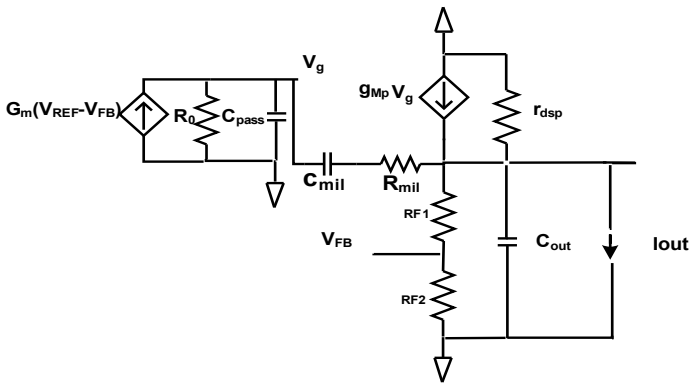

Figure. C.1. Small-signal equivalent circuit of conventional LDO.

The aspect ratio of pass transistor Mp is large, in support of large load current of 100mA. In spite of large gate to source capacitance (C_{gs}) and gate to drain capacitance (C_{gd}) due to Mp's large aspect ratio, the miller effect of Cgd increases the effective capacitance at the gate of the pass transistor (Mp). Thus, the error amplifier pole P_{EA} at Vg forms a dominant pole among all the poles and zeros of conventional LDR. So, the expression for error amplifier pole P_{EA} is given by Equation. C.1.

$$P_{EA} = -\frac{1}{R_0\left(C_{pass} + C_{mil} g_{Mp} R_{out}\right)} \tag{C.1}$$

Where R_{out} is the equivalent error amplifier output resistance, C_{pass} is the pass transistor capacitance, miller capacitance is C_{mil}, g_{Mp} is the pass transistor transconductance and the

output load capacitance is C_{out} and the output equivalent resistance Rout is ($r_{dsp}||R_{F1}||R_{F2}$) where R_{F1} and R_{F2} are feedback resistances and r_{dsp} drain to source resistance of pass transistor. But, as the voltage gain of pass transistor changes with varying load current, P_{EA} shows load dependency. Nevertheless, less sensitive than the output pole P_{out}. The second pole Pout located at the LDR output is given by Equation. C.2

$$P_{out} = -\frac{g_{Mp} + \frac{1}{R_{out}}}{C_{out} + C_{pass}} \alpha \sqrt{I_{out}} \tag{C.2}$$

The P_{out} movement for a large load current change impacts the stability of LDR. The increased load current reduces the output resistance (R_{out}) drastically; in consequence, Pout lies at higher frequencies thus maintaining the stability of the system.

On the contrary, at low load currents, load resistance (R_{out}) increases significantly, bringing the P_{out} to lower frequencies at a close proximity to the error amplifier pole P_{EA} and thus compromising stability.

The commonly used effective compensation scheme is shown in Figure 4.4 of the text and involves generation of zero (z_1). It is a function of miller capacitor C_{mil} that pulls error amplifier pole P_{EA} to lower frequencies and null resistor R_{mil} that pulls power transistor Mp's right-half-plane zero to the left-half-plane, thus sustaining stability.

The corresponding zero is given by Equation C.3.

$$z_1 = -\frac{1}{\left(R_{mil} - \frac{1}{g_{Mp}}\right) C_{mil}} \tag{C.3}$$

Considering the B as feedback factor defined by Equation C.4

$$B = \frac{R_{F2}}{R_{F1} + R_{F2}} \tag{C.4}$$

So, the complete loop gain transfer function is given by C.5

(C.5)

The corresponding Gain bandwidth product is given by Equation (C.6)

$$GBW = \frac{BG_m R_0 g_{Mp} R_{out}}{R_0\left(C_{pass} + C_{mil} g_{Mp} R_{out}\right)} \tag{C.6}$$

The transfer function T(s) determines the worst-case stability for different load currents. The compensation capacitor C_{mil} once determined ensures stability for a wide range of load currents. The worst-case stability occurs for minimum phase margin of second order system.

The phase margin for compensated two pole systems is given by

(C.7)

Where the unit-y-gain frequency and pnd is the non-dominant pole of the second order system. The larger the value of () is the better the phase margin. A factor T_{PM} that defines the separation between and is considered and is represented as

(C.8)

Where DC loop gain given by B $G_m R_0 g_{Mp} R_{out}$ .The value of B=1 is considered for worst case feedback factor for stability.

The larger the value of T_{PM} is the better the phase margin. A factor T_{PM} that defines the separation between P_{nd} and is considered and is represented as

$$T_{PM} = \frac{p_{nd}}{w_u} = \frac{\left(\frac{g_{Mp} + \frac{1}{R_{out}}}{C_{out} + C_{pass}}\right)}{\left(BG_m R_0 g_{Mp} R_{out}\right).\left(\frac{1}{R_0\left(C_{pass} + C_{mil} g_{Mp} R_{out}\right)}\right)} \tag{C.9}$$

The minimum value of T_{PM} at which minimum phase margin occurs is found by differentiating C.9 with g_{Mp}. The resulting minimum T_{PM} is given by

$$T_{PM\min} = \sqrt{\frac{C_{out}}{C_{mil}}} \times \frac{1}{Rout} \tag{C.10}$$

By substituting Equation C.10 into Equation C.7, the minimum phase margin is given in Equation C.11as

$$PM = 90^0 - \arctan\left(\sqrt{\frac{C_{mil}}{C_{out}}}\right) \times R_{out} \tag{C.11}$$

and further from Equation C.11 the compensation capacitor is expressed as

$$C_{mil} = \frac{C_{out}}{R_{out}{}^2 \tan^2\left(90^0 - PM\right)} \tag{C.12}$$

In our design, a C_{mil} of 1.5pF is selected for LDR and found suitable for a full range of load current.

Appendix D

DDR3 Memory

The computing devices uses random access memory (RAM) for its data storage. One such type of RAM is DDR SDRAM (double-data-rate synchronous dynamic random-access memory) which is more suitable for applications that demand memory access with high bandwidth and low latency. The SDRAM memory devices are classified into DDR, DDR2, DDR3 and DDR4 Versions. DDR SDRAM can transfer two chunks of data per clock cycle as depicted in Figure D.1 that achieves double data rate as compared to SDR SDRAM.

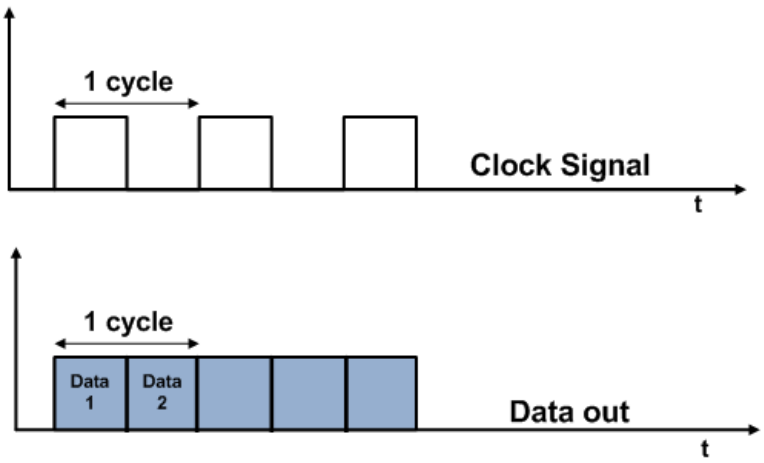

Figure D.1 Operational behavior of DDR mode signal

Such memories are nomenclature with double the real maximum clock rate operation. For example, DDR2-800 memories work at 400 MHz, DDR2-1066 and DDR3-1066 memories work at 533 MHz, DDR3-1333 memories work at 666.6 MHz, and so on.

The clock rates mentioned refer to the clock rates used for the communication between the memory and memory controller. However, the internal operations that are executed in a DDR SDRAM needs special attention which is discussed further in the fore coming paragraphs.

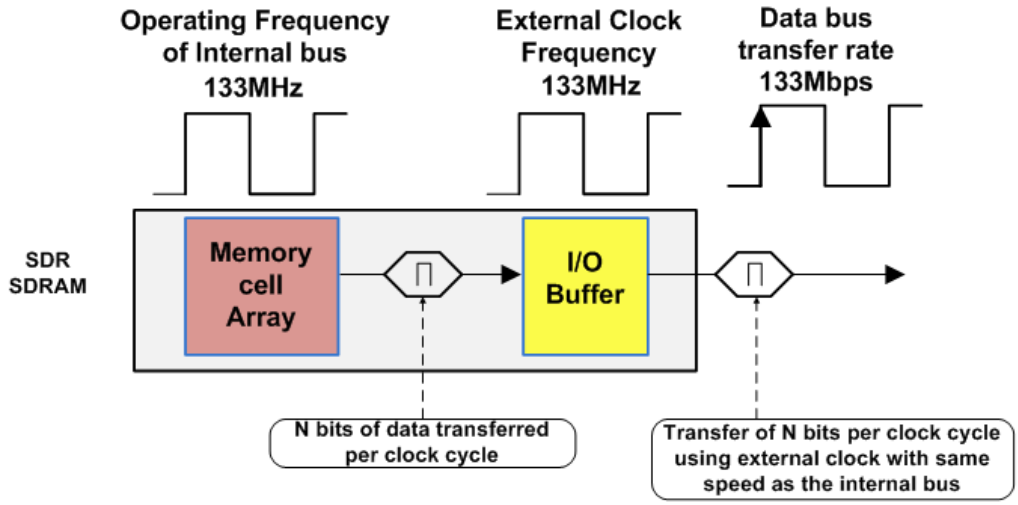

Figure D.2 Demonstration of prefetching operations inside the SDR SDRAM memory IC.

The basic operations that constitute the communication between Memory cell array and Memory controller is shown in Figure D.2. It constitutes the memory cell array that interfaces with the external world (memory controller) through an I/O buffer. It is observed that in the case of SDR SDRAM (single data rate SDRAM) n bit of data per clock cycle are transferred between Memory cell array and I/O buffer (each operating at same clock frequency of 133MHz) which further transfers the data to memory controller through external data bus at the same data rate (133MHz).

The next generation DDR SDRAM transfers the data between Memory cell array and memory controller with double the data transfer rate (266MHz) of the prior architecture as shown in Figure D.3.The memory bus operating frequency is kept at 133MHz by transferring 2N bits of data per clock cycle by sending data at both the edges of clock cycle.

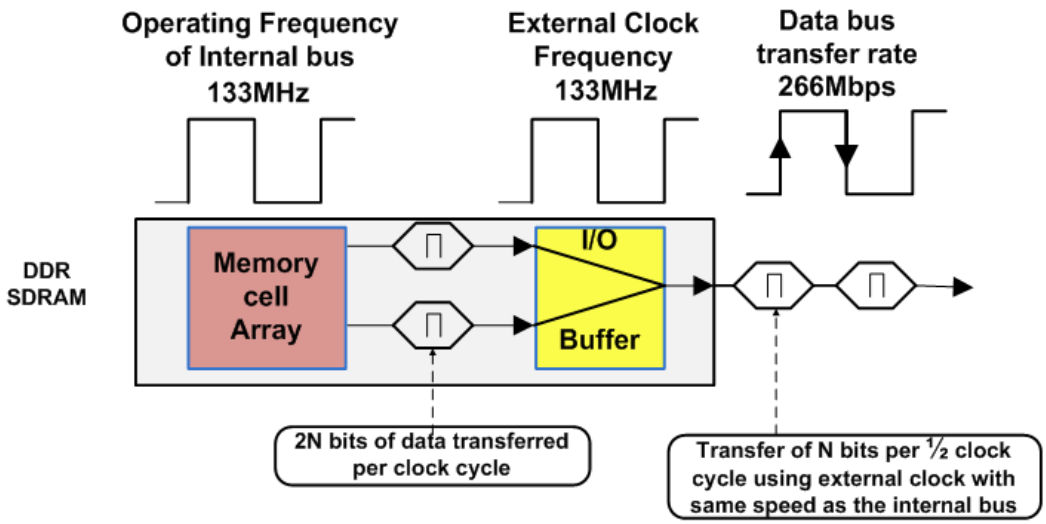

Figure D.3 Demonstration of prefetching operations inside the DDR DDRAM memory IC.

For a change in the generation from DDR to DDR2, the external clock has been doubled to double the Data bus transfer rate but to use the same memory IC at 133 MHz the memory cell array transfers 4bits to the I/O buffer thereby increasing the data bus transfer rate to 4 x 133 MHz = 533 Mhz. The memory fetching operations are shown in Figure D.3.

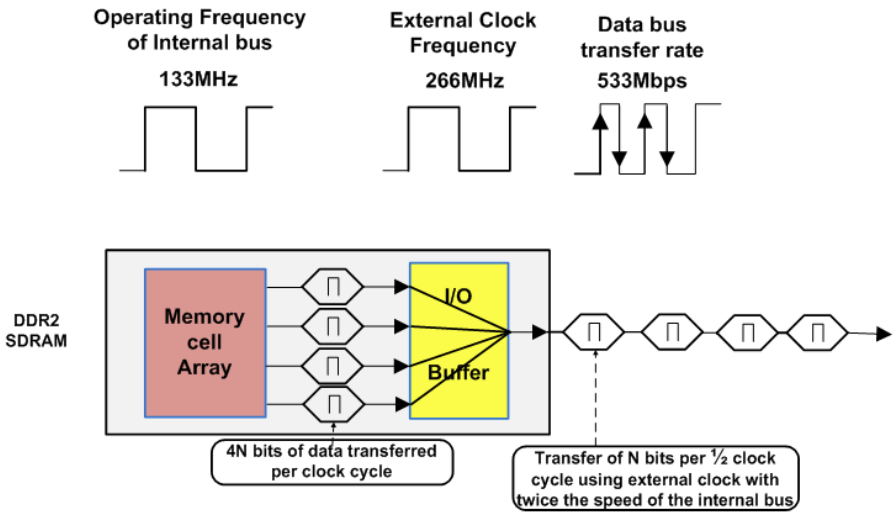

Figure D.3 Demonstration of prefetching operations inside the DDR2 DDRAM memory IC.

The specifications of Different SDRAM architectures are tabulated as below:

DDRSDRAM standard	Internal Rate(MHz)	Bus clock (MHz)	Prefetch	Data rate (MT/s)	Transfer rate (GB/s)	Voltage (V)
SDRAM	100-166	100-166	1n	100-166	0.8-1.3	3.3
DDR	133-200	133-200	2n	266-400	2.1-3.2	2.5/2.6
DDR2	133-200	266-400	4n	533-800	4.2-6.4	1.8
DDR3	133-200	533-800	8n	1066-1600	8.5-14.9	1.35/1.6
DDR4	133-200	1066-1600	8n	2133-3200	17-21.3	1.2

Among the mentioned SDRAM DDRs DDR4 SDRAM is dense, offers high bandwidth, operates with high data rate, and consumes low power relative to earlier generations.

The characterization of power supply system of a DDR3 interface of a single memory cell is as shown in Figure D.4.The power supply design for this interface is challenging due to the high data rate of DDR3 signaling which leaves little margin for the tolerance in the supply ripple magnitude and settling time during sudden load transients. It is therefore necessary to develop a highly optimized power supply system particularly employing low dropout

regulators(LDOs) that offers highly accurate and fast settling transient performance. The characterization of DDR physical signal system is as follows:

A low dropout regulator is required to power up these memories termination rail Vtt which is shown in Figure D.4.

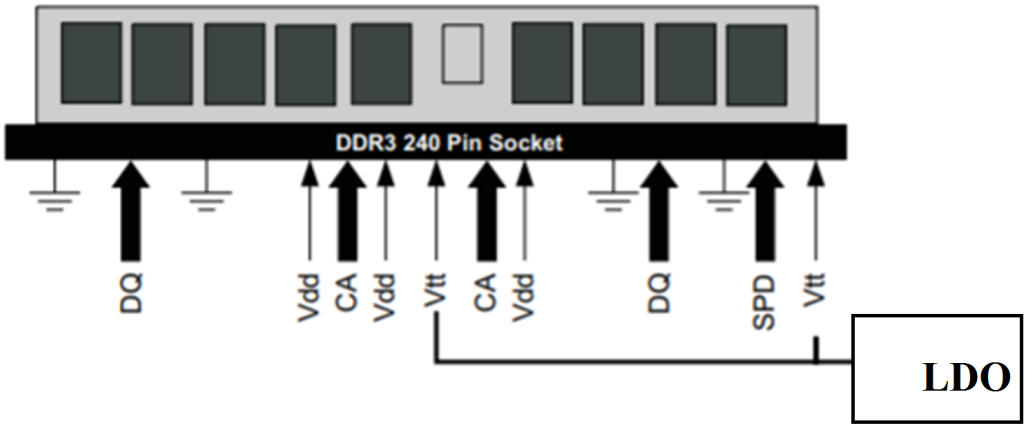

Figure D.4 Typical application diagram for DDR3 VTT DIMM using LDO

The characteristics of Vtt terminal is determined by the DDR memory termination structure that aids in the sourcing and sinking of current without compromising with the transients generated across Vtt.

The single memory cell of DDR physical signal system is shown in Figure D.5

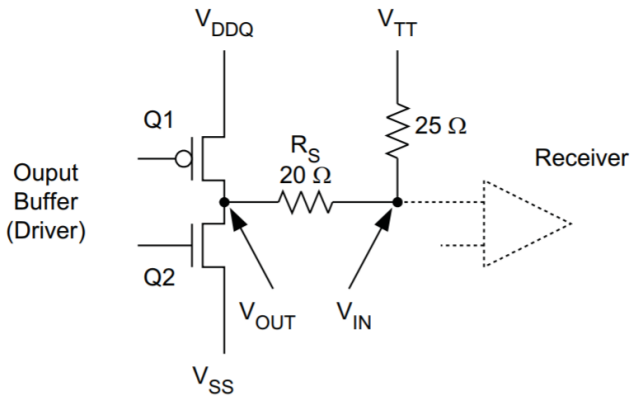

Figure D.5 DDR Physical signal system

The operation of DDR physical signal system is described as follows:

When Q1 is on and Q2 is off current flows from V_{DDQ} via the termination resistor to V_{tt} Thus V_{tt} behaving as sinking device. When Q2 is on and Q1 is off current flows from V_{tt} via termination resistor to ground. Thus V_{tt} is behaving as sourcing device. The accuracy in the V_{tt} voltage decides memory signal integrity. The signal overshoots and undershoots are kept

within 10% to 15% of the supply voltage (V_{tt}=1.6V) which amounts to 200mV. The maximum load that DDR3 memory takes may rise to 100mA as it gets loaded by eight data lines as each data lane that is properly terminated for maximum data transfer rate along with differential clock.

Another parameter that is worth consideration is the transient response (undershoot)settling time for the load current transients from low to high. During this operation the signal swing is minimum and the receiver cannot detect data changes. So, it is imperative that LDO regulator response settles within the duration of preamble sequence. The duration of 500bit preamble sequence can be 500ns with a data rate of 1Gbps demanding undershoot settling time of order of 300ns.