Investigations on Quasi-Z-Source based Multilevel Inverters for Grid-Tied Photovoltaic Systems

Submitted in partial fulfilment of the requirements

for the award of the degree of

Doctor of Philosophy

By

Pasupuleti Manoj

(Roll No. 718019)

Supervisor

Dr. V. T. Somasekhar

Professor (HAG)

DEPARTMENT OF ELECTRICAL ENGINEERING

NATIONAL INSTITUTE OF TECHNOLOGY WARANGAL

WARANGAL – 506004, TELANGANA STATE, INDIA

March-2023

APPROVAL SHEET

This Thesis entitled "**Investigations on Quasi-Z-Source based Multilevel Inverters for Grid-Tied Photovoltaic Systems**" by **Pasupuleti Manoj** is approved for the degree of Doctor of Philosophy.

Examiners

_____

_____

_____

Supervisor

Dr. V. T. Somasekhar
Professor (HAG)
EED, NIT Warangal

Chairman

Dr. S. Srinivasa Rao
Professor
EED, NIT Warangal

Date: _____

DEPARTMENT OF ELECTRICAL ENGINEERING
NATIONAL INSTITUTE OF TECHNOLOGY
WARANGAL – 506 004

DEPARTMENT OF ELECTRICAL ENGINEERING
NATIONAL INSTITUTE OF TECHNOLOGY WARANGAL

CERTIFICATE

This is to certify that the thesis entitled **"Investigations on Quasi-Z-Source based Multilevel Inverters for Grid-Tied Photovoltaic Systems"**, which is being submitted by **Mr. Pasupuleti Manoj** (Roll No. 718019), is a bonafide work submitted to National Institute of Technology, Warangal in partial fulfilment of the requirement for the award of the degree of **Doctor of Philosophy** in Department of Electrical Engineering. To the best of my knowledge, the work incorporated in this thesis has not been submitted elsewhere for the award of any degree.

Dr. V. T. Somasekhar
(Supervisor)
Professor (HAG)
Department of Electrical Engineering
National Institute of Technology
Warangal – 506004

Date:

Place: Warangal

DECLARATION

This is to certify that the work presented in the thesis entitled "**Investigations on Quasi-Z-Source based Multilevel Inverters for Grid-Tied Photovoltaic Systems"** is a bonafide work done by me under the supervision of **Dr . V. T. Somasekhar**, Department of Electrical Engineering, National Institute of Technology, Warangal, India and was not submitted elsewhere for the award of any degree.

I declare that this written submission represents my ideas in my own words and where others ideas or words have been included; I have adequately cited and referenced the original sources. I also declare that I have adhered to all principles of academic honesty and integrity and have not misrepresented or fabricated or falsified any idea/data/fact/source in my submission. I understand that any violation of the above will be a cause for disciplinary action by the institute and can also evoke penal action from the sources which have thus not been properly cited or from whom proper permission has not been taken when needed.

Pasupuleti Manoj
(Roll. No: 718019)

Date:
Place: Warangal

ACKNOWLEDGEMENTS

It gives me immense pleasure to express my heartfelt gratitude to my supervisor **Prof. V. T. Somasekhar** for giving me the opportunity to work under his direction. His knowledge, suggestions, and discussions helped me to overcome difficult situations during my thesis work. Without his scholarly guidance, this thesis could not have been completed. I consider myself very fortunate to have worked with him.

I take the opportunity to thank my Doctoral Scrutiny Committee chairman **Dr. S. Srinivasa Rao**, Professor, Department of Electrical Engineering and all Doctoral Scrutiny Committee members, **Dr. A. Kirubakaran**, Associate Professor, Department of Electrical Engineering, **Dr. G. Siva Kumar,** Associate Professor, Department of Electrical Engineering and **Dr. N. Bheema Rao,** Professor, Department of Electronics and Communication Engineering for their detailed review, constructive suggestions and excellent advice during the progress of this research work.

I am very thankful to **Dr. B. L. Narasimharaju**, Head of Department of Electrical Engineering and **Prof. N.V. Ramana Rao**, Director, NIT Warangal for their support and cooperation.

I am highly grateful to my seniors Dr. Suresh Lakhimsetty, Dr. Sumon Dhara and Dr. Patnana Hema Kumar for their constant support and suggestions during my Ph.D work. I convey my special thanks to my contemporary Research Scholars Mr. K. Hema Sundar, Mr. M. Madhu Babu, Mr. K. Ashok Kumar, Mr. M F Baba, Mr. Chinmay Kumar Das, Mr. C.R. Arun Kumar for constant support throughout my journey. I thank my juniors Mr. K.V.V.S Ramana kumar and Mr. K. Srikanth Reddy for their cooperation and encouragement.

I also appreciate the encouragement from teaching, non-teaching members, and fraternity of Department of Electrical Engineering of NIT Warangal. They have always been encouraging and supportive.

Finally, I would like to thank my parents Shri. Manga Raju, Smt. Rajya Lakshmi and my sister Ms. Vasavi, for their love, patience and moral support during my research work.

Pasupuleti Manoj

ABSTRACT

The importance of renewable energy sources need not be overemphasized in the present scenario of the dwindling resources of conventional energy. The efforts to contain environmental pollution resulted in the emergence of solar photovoltaic (PV) systems. Declining costs, durability, and lower maintenance are the contributing factors to the proliferation of solar energy systems. Solar PV systems are operated in stand-alone mode for water pumping, rural electrification, and street lighting applications. Also, grid-tied PV systems are gaining momentum due to the ever-increasing nature of electrical energy.

Conventionally, in grid-tied PV systems, the objectives of boosting the inadequate PV input voltage and the DC-AC conversion are achieved with a two-staged system, consisting of a boost converter and conventional VSI. These systems display a good maximum power point tracking (MPPT) capability due to the availability of an additional DC/DC boost converter. However, the demerits of these systems are low reliability, less efficiency, and increased complexity. In recent times, quasi-z-source-based solar PV systems attract the attention of researchers. Owing to their single-staged nature, these topologies can accomplish both boosting and inversion with reduced switching resources, smaller sizes of passive components, lower cost, and enhanced efficiency.

In the past two decades, multilevel inverters gained much attention as they are suitable for high power and high voltage applications. With an increased number of voltage levels, multilevel inverters (MLIs) reduce the voltage stress across the power semiconductor switching devices and derive a superior harmonic performance compared to the conventional two-level VSIs. However, owing to their buck-typed nature, conventional multilevel inverters require that the input DC voltage be higher than the desired peak value of the AC output voltage. Therefore single-stage systems aim to overcome this disadvantage by fusing a multilevel inverter with a quasi-z-source network.

This thesis presents the investigation of single-stage quasi-z-source-based multilevel inverter configurations for both multi-string and single-string applications. The thesis attempts to address some major challenges associated with the quasi-z-source-based multilevel inverters which are: (i) achieving higher voltage boosting and inversion simultaneously (ii) the reduction of leakage current, (iii) reactive power capability (iv)

multilevel operation with reduced switching devices, etc. In an attempt to address these challenges, four single-stage multilevel inverter topologies have been proposed in this thesis.

Firstly, a single-stage, four-level, cascaded multilevel inverter is proposed for multi-string photovoltaic applications. The proposed configuration achieves voltage boosting using three quasi-z-source networks, which are fused with the cascaded multilevel configuration. The power converter employs a level-shifted space vector modulation technique. In comparison with the conventional qZS-based cascaded H-bridge and Neutral point clamped inverters, the power converter achieves a 50% higher boost factor. Moreover, compared to the aforementioned configurations, the proposed converter outputs a higher number of voltage levels, resulting in better spectral performance and alleviating the voltage stress across the switches. Further, it is shown that the employed control technique implements the shoot-through without any additional power loss in qZS inverters. Moreover, the performance characteristics of the proposed inverter were compared with existing topologies to highlight its merits. However, the control complexity associated with the MPPT tracking with multiple PV sources, DC-link voltage regulation, and the requirement of a large number of switching devices to synthesize a 4-level output voltage waveform is the major demerits of the topology.

In the second proposal**,** a single-stage seven-level quasi-z-source-based MLI is investigated to minimize the aforementioned drawbacks. The power converter employs only two PV sources and requires a lower number of devices to generate a 7-level output voltage waveform. Further, the power converter employs a modified level-shifted PWM scheme, which achieves the twin objectives of boosting the input voltage and the generation of 7 levels in the output voltage waveform. Moreover, this work aims to minimize the leakage current, which is one of the major issues in transformerless inverters, by reducing the magnitude of voltage transitions in the parasitic capacitor and the suppression of higher-order harmonics in the ground leakage current.

To further, minimize the input PV sources and semiconductor devices a five-level qZS-based PV inverter is proposed. In this topology, two symmetrical qZS networks with a single DC source are fused with a 5-level hybrid inverter. Similar to the aforementioned topology, the proposed power converter employs a modified level-shifted PWM to achieve boosting and five-level operation. When compared to the existing qZS-based 5-level inverters in the literature, the proposed power converter employs fewer semiconductor switching

devices, enhancing its reliability. Further, the power converter also minimizes the leakage current to less than the standards dictated by *VDE-0126-1-1*.

Both the proposed qZS-based seven-level and five-level inverters suffer from high voltage THD and conventional voltage boosting. To minimize these drawbacks a quasi-switched capacitor-based five-level inverter is proposed. The proposed power converter comprises two quasi-z-source networks and switched capacitor-based five-level inverter with a single PV source. With the aid of a modified LSPWM scheme and switched capacitor network the power converter achieves higher voltage boosting and five-level voltage inversion. Further, the power converter minimizes the leakage current without any additional need for filter components.

All the above-mentioned power configurations in this thesis are verified with laboratory prototypes in the stand-alone as well as the grid-tied modes of operation. Experimental studies validate the working principles of the proposed power converter configurations along with the proposed modulation strategies in steady-state as well as dynamic conditions.

Table of Contents

Acknowledgement ..... **i**

Abstract ..... **ii**

Table of Contents ..... **v**

List of Figures ..... **ix**

List of Tables ..... **xv**

Abbreviations ..... **xvi**

List of Symbols ..... **xix**

Chapter-1 Introduction 1-1

1.1 General overview 1-2

1.2 Classification of PV inverters 1-3

1.2.1 Central inverters 1-3

1.2.2 String inverters 1-3

1.2.3 Microinverter 1-3

1.3 Interfacing PV source with grid 1-4

1.3.1 Number of power processing stages 1-4

1.3.2 Isolated/Non-Isolated inverter 1-5

1.4 Leakage current 1-6

1.5 Single-stage non-isolated power converters with voltage boosting 1-7

1.6 PV inverter standards in grid-tied operation 1-8

1.7 Organization of the thesis 1-9

Chapter-2 Literature survey 2-1

2.1 Introduction 2-2

2.2 The Impedance source inverter 2-2

2.3 Classification of impedance source networks 2-5

2.3.1 Non-transformer impedance networks 2-5

2.3.2 Transformer-coupled impedance networks 2-7

2.4 Multilevel Inverters 2-8

2.5 Impedance source Multilevel Inverter 2-9

2.5.1 Three-phase impedance source multilevel inverter topologies 2-9

2.5.2 Single-phase impedance source multilevel inverter topologies 2-12

2.6 Motivations 2-15

2.7 Objectives 2-16

Chapter-3 A Quasi-Z-Source Based Space Vector Modulated Cascaded Four-Level Inverter for Photovoltaic Applications 3-1
3.1 Introduction 3-2
3.2 The proposed Quasi-z-source based four-level cascaded MLI(QZS-FCMI) 3-3
3.2.1 Switching states and the output voltage of the Four-level Inverter 3-4
3.3 Control strategy for the proposed QZS-FCMI 3-5
3.3.1 Implementation of the SVPWM scheme 3-5
3.3.2 Insertion of the shoot-through in the FCMI 3-6
3.3.3 Analysis of the Boost factor of the Quasi-Z-source with the proposed PWM Scheme 3-10
3.4 The control scheme of QZS-FCMI for stand-alone and grid-connected operation 3-12
3.4.1 Standalone mode 3-12
3.4.2 The Grid-connected mode of operation 3-13
3.5 Experimental Results 3-14
3.6 Comparison with the proposed QZS FCMI 3-21
3.7 Power loss analysis for the proposed QZS-FCMI 3-23
3.8 Summary 3-24
Chapter-4 An Asymmetrical Dual Quasi-Z-Source Based 7-Level Inverter for PV Applications 4-1
4.1 Introduction 4-2
4.2 The proposed DQZS-7LI 4-3
4.2.1 Proposed Power converter 4-3
4.2.2 Output voltage levels and corresponding switching states of the power converter 4-3
4.3 The control scheme for the proposed dual QZS 7-level inverter 4-5
4.3.1 Implementation of the MLS-PWM scheme 4-5
4.3.2 Boost factor of the proposed DqZS-5LI 4-7
4.3.3 Design of qZS network of proposed DqZS-7LI 4-8
4.4 Standalone and grid-connected control strategies of DQZS-7LI 4-9
4.4.1 Stand-alone mode 4-9
4.4.2 The Grid-connected mode of operation 4-10
4.5 Reduction of leakage current 4-11
4.6 Experimental Results 4-13
4.7 Comparison with the proposed DQZS-7LI 4-18
4.8 The Loss analysis for the DQZS-7LI 4-20
4.9 Summary 4-21

Chapter-5 A Single-Stage Quasi-Z-Source Based 5-Level Grid-tied PV Inverter with Reduced Leakage Current 5-1
5.1 Introduction 5-2
5.2 The QZS-Based 5-level Hybrid inverter 5-3
5.2.1 Power converter 5-3
5.2.2 Switching states and corresponding output levels of the power converter 5-3
5.2.3 Boost factor 5-5
5.3 Modulation scheme 5-6
5.4 Proposed control strategy for standalone and grid-connected 5L-QZSI 5-7
5.4.1 Standalone mode 5-7
5.4.2 The grid-connected mode of operation 5-8
5.5 Reduction of leakage current 5-9
5.6 Experimental Results 5-12
5.7 Comparison of proposed topology with 5-Level qZSI 5-18
5.8 Power Loss for the 5L-QZSI 5-20
5.9 Summary 5-21
Chapter-6 A Quasi-Switched Capacitor Based Grid-connected PV Inverter with a Reduced Leakage Current 6-1
6.1 Introduction 6-2
6.2 The QSC-Based five-level T-type inverter 6-3
6.2.1 Power Converter 6-3
6.2.2 Switching logic of the qSC-5LI 6-3
6.3 Modulation Technique 6-5
6.3.1 Proposed modulation technique for qSB-5LI 6-5
6.3.2 Analysis of the Boost Factor 6-6
6.4 Proposed closed-loop control schemes for qSB-5LI 6-7
6.4.1 Standalone mode 6-7
6.4.2 Grid-connected mode 6-8
6.5 Reduction of Leakage current 6-9
6.6 Experimental results 6-10
6.7 Comparison between the proposed qSC-5LI and the qZS-based five-level inverter topologies 6-15
6.8 Loss Distribution in qSC-5LI 6-16
6.9 Summary 6-17
Chapter-7 Conclusion and Future Scope 7-1
7.1 Conclusion 7-2
7.2 Future Scope 7-3

Appendix-1 .....A-1

References R-1

Publications.....P-1

List of Figures

Fig. 1.1:	General layout of a grid-tied PV inverter.	1-2
Fig. 1.2:	Overview of PV inverters (a) Central inverter (b) string inverter (c) Microinverter.	1-4
Fig. 1.3:	Block diagram of (a) Two-stage power converter (b) Single-stage power converter.	1-5
Fig. 1.4:	Parasitic capacitances in a typical PV Panel.	1-6
Fig. 2.1:	The Z-source inverter	2-2
Fig. 2.2:	Quasi-Z-source inverter	2-4
Fig. 2.3:	Classification of impedance source networks	2-5
Fig. 2.4:	Embedded Z-source network	2-6
Fig. 2.5:	Switched inductor Z-source network	2-6
Fig. 2.6:	Capacitor/diode assisted qZS network	2-6
Fig. 2.7:	(a) Switch Boost inverter (b) Trans-switch boost inverter	2-7
Fig. 2.8:	(a) Trans. ZSN (b) Trans.QZSN	2-7
Fig. 2.9:	(a) LCCT ZSI (b) LCCT QZSI	2-8
Fig. 2.10:	Z-source NPC three-level inverter	2-9
Fig. 2.11:	(a) Single Z-source NPC three-level inverter (b) Modified Z-source NPC three-level inverter	2-10
Fig. 2.12:	Quasi-Z-source NPC three-level inverter	2-10
Fig. 2.13:	A three-level Quasi-Z-source based T-type inverter.	2-11
Fig. 2.14:	Quasi-Z-source CHB inverter	2-11
Fig. 2.15:	Z-source seven-level inverter	2-12
Fig. 2.16:	Quasi-Z-source single-phase CHB inverter	2-13
Fig. 2.17:	Quasi-switched boost inverter	2-13

Fig. 2.18:	Modified quasi-Z-source five-level inverter	2-14
Fig. 2.19:	Quasi-Z-source with additional switches	2-15
Fig. 2.20:	Quasi-Z-source with AC decoupling switches	2-15
Fig. 3.1:	Proposed qZS-FCMI.	3-3
Fig. 3.2:	Implementation of phase-A switching for qZS-FCMI.	3-6
Fig. 3.3:	Space vector diagram of FCMI.	3-7
Fig. 3.4:	Switching sequence of FCMI when reference phasor is in sector HVW.	3-8
Fig. 3.5:	Circuit diagrams for switching states mentioned in Fig. 3.4 (a) [210] state (b) [310] state (c) [320] state (d)[321] state in a given sample time T_s.	3-9
Fig. 3.6:	Scaling of boost factor by LSPWM technique.	3-10
Fig. 3.7:	DC-link voltage control scheme for the proposed FCMI.	3-12
Fig. 3.8:	Block diagram of the grid control scheme.	3-14
Fig. 3.9:	Experimental results of input voltage (V_{in1}) and DC-link voltages (V_{dc1}, V_{dc2}, V_{dc3}) of FCMI.	3-15
Fig. 3.10:	Experimental results of input voltage (V_{in1}) and DC-link voltages (V_{dc1}, V_{dc2}, V_{dc3}) of FCMI.	3-16
Fig. 3.11:	Experimental results of Pole voltage waveform (V_{BO}), Line voltage (V_{BC}), Phase voltage (V_{BN}), and Phase current (i_B) of FCMI.	3-16
Fig. 3.12:	Harmonic spectrum of the output phase voltage (V_{BN}) and phase current(i_{BN}).	3-17
Fig. 3.13:	Experimental results (a) DC-link voltage waveforms of qZS-FCMI and the load voltage and current in phase C (b) Zoom-in view of the DC-link voltages (C) Zoom-in view of the load voltage and current in phase C.	3-18
Fig. 3.14:	Experimental results (a) DC-link voltages and input voltage waveforms of FCMI during source disturbance (b) Zoom-in view of the DC-link voltages of the FCMI.	3-18
Fig. 3.15:	Experimental results of MPPT control of PV-1	3-19

Fig. 3.16:	Experimental results of MPPT control of PV-2.	3-19
Fig. 3.17:	Experimental results (a) PV current (I_{pv1}), total dc-link voltage ($V_{dctotal}$), grid currents (I_{gabc}) (b) grid voltage and grid current.	3-20
Fig. 3.18:	Experimental result of inverter line voltage (V_{AB}) and grid voltage (V_{ga}) and grid current (i_{ga}) waveforms.	3-21
Fig. 3.19:	Loss distribution in the device for qZS-FCMI.	3-23
Fig. 3.20:	Calculated efficiency of the proposed qZSI-FLI for two different input voltages.	3-24
Fig. 3.21:	Experimental efficiency of the proposed qZSI-FLI	3-24
Fig. 4.1:	Proposed DqZS-7LI.	4-3
Fig. 4.2:	Circuit diagrams for NST and ST states of the power converter.	4-5
Fig. 4.3:	Implementation of modified reference wave (v_m^*) for DqZS-7LI.	4-6
Fig. 4.4:	Implementation of modulation technique.	4-7
Fig. 4.5:	Equivalent circuit of DqZS-7LI during (a) shoot-through state (ST) (b) non-shoot-through (NST) state. (c) Simplified equivalent circuit.	4-8
Fig. 4.6:	Closed-loop DC-link voltage control for the proposed DqZS-7LI.	4-9
Fig. 4.7:	The grid control scheme for DqZS-7LI.	4-10
Fig. 4.8:	(a) DqZS-7LI with leakage ground current path (b) equivalent circuit of the differential-mode model(c) equivalent circuit of the common-mode model.	4-12
Fig. 4.9:	Experimental results of DC-input voltages ($V_{in1,}$ V_{in2}) and DC-link voltages (V_{dc1}, V_{dc2}) of DqZS-7LI.	4-14
Fig. 4.10:	Experimental results of the DC input voltage (V_{in2}), DC-link voltage (V_{dc2}) and inductor current (i_{L4}), and capacitor voltages (V_{c3}, V_{c4}) of the qZS-1 network.	4-15
Fig. 4.11:	Experimental results of (a) Output voltage waveform (V_{AB}), Load voltage (i_{Load}) (b) Parasitic capacitor voltage (V_{cp}), and Leakage current (i_{leak}) of DqZS-7LI.	4-15

Fig. 4.12:	Experimental results of DC-link voltage (V_{dc1}), capacitor voltages (V_{c1}, V_{c2}), output voltage (V_{AB}), and the load current (i_{load}).	4-16
Fig. 4.13:	Experimental results of (a) DC input voltages (V_{in1}, V_{in2}) and DC-link voltages waveforms of DqZS-7LI in the course of source disturbance (b) Zoomed view of the DC-link and DC input voltages of the DqZS-7L	4-17
Fig. 4.14:	Experimental results (a) Capacitor voltage (V_{c3}), Phase voltage (V_{AB}), Inductor current (i_{L3}) Grid voltage (V_g), and Grid current (i_g) (b) Zoom-in view at 300W.	4-17
Fig. 4.15:	(a) Output voltage (V_{AB}), load voltage (V_{out}), and load current (i_{load}) for 0.8 lagging power factor (b) FFT of inverter output voltage 'V_{AB}' (c) FFT of output voltage 'V_{out}'	4-18
Fig. 4.16:	(a). Power Loss distribution in DqZS-7LI at 300W. (b) Experimental efficiency of the proposed DqZS-7LI.	4-21
Fig. 5.1:	The Proposed 5L-qZSI	5-3
Fig. 5.2:	Circuit diagrams for NST and ST states of the power converter.	5-4
Fig. 5.3:	Implementation of the modulation scheme for 5L-qZSI.	5-6
Fig. 5.4:	Implementation of the modulation technique.	5-7
Fig. 5.5:	Indirect DC-link voltage regulation of the proposed 5L-qZSI.	5-8
Fig. 5.6:	The control scheme for grid-tied 5L-qZSI.	5-9
Fig. 5.7:	5L-qZSI with leakage current path.	5-11
Fig. 5.8:	Equivalent circuit of the common-mode model.	5-11
Fig. 5.9:	The simplified equivalent circuit.	5-12
Fig. 5.10:	Experimental results of input voltage (V_{in}) and DC-link voltages V_{dc1} & V_{dc2}.	5-14
Fig. 5.11:	Experimental results of the input voltage (V_{in1}), DC-link voltage (V_{dc1}), inductor current (i_{L1}), and capacitor voltages (V_{c1}, V_{c2}).	5-14
Fig. 5.12:	Experimental waveforms of output voltage (V_{AB}) and load current (i_{load}).	5-15
Fig. 5.13:	Experimental results of parasitic capacitor voltage (V_{cp}), leakage current (i_{leak}) of the PV source, and harmonic spectrum of leakage current.	5-15

Fig. 5.14:	Experimental results of DC-link voltages (V_{dc1} & V_{dc2}), output voltage (V_{AB}) and load current (i_{load}).	5-16
Fig. 5.15:	Experimental results of (a) input voltages (V_{in1}) and DC-link voltages (V_{dc1} & V_{dc2}) (b) Zoomed view of the plot (a).	5-17
Fig. 5.16:	Experimental results of the total DC link voltage, output voltage of the inverter (V_{AB}), grid voltage (V_g), and current (i_g).	5-17
Fig. 5.17:	(a) FFT of inverter output voltage 'V_{AB}' (b) FFT of grid current 'i_g' (c) FFT of output voltage 'V_{out}'(d) output voltage (V_{AB}), load voltage (V_{out}) and load current (i_{load}) for 0.8 lagging power factor.	5-18
Fig. 5.18:	(a) Power Loss distribution in 5L-qZSI.(b) Efficiency comparison with the 5L-qZSI (c) Experimental efficiency of the 5L-qZSI	5-21
Fig. 6.1:	The Proposed qSC-5LI	6-3
Fig. 6.2:	(a) Schematic of qZS network during NST states (b-f) Schematic of MLI during NST-1 to NST-6.	6-4
Fig. 6.3:	(a) Schematic of qZS network during ST states (b-d) Schematic of MLI during ST-1 to ST-3.	6-5
Fig. 6.4:	Implementation of the modulation technique.	6-6
Fig. 6.5:	Implementation of the modulation technique.	6-6
Fig. 6.6:	(a) Control strategy for standalone mode and (b) Control strategy for a grid-connection mode of operation.	6-8
Fig. 6.7:	(a) Common-mode model of qSC-5LI (b) Simplified common-mode model.	6-10
Fig. 6.8:	Input voltage (V_{in}), DC-link voltage (V_{dc1}), capacitor voltages (V_{c1}, V_{c2}), and inductor current (i_{L1}) of the qSC-5LI.	6-12
Fig. 6.9:	Input voltage (V_{in}), DC-link voltage (V_{dc1}), capacitor voltages (V_{c1}, V_{c2}), and inductor current (i_{L1}) of the qSC-5LI.	6-12
Fig. 6.10:	Input voltage (V_{in1}), DC-link voltage (V_{dc1}) and switched capacitor voltages (V_{SC1}, V_{SC2}) of the qSC-5LI.	6-12
Fig. 6.11:	PV capacitor voltage (V_{cp}) and leakage current (i_{leak}) of the qSB-5LI.	6-13
Fig. 6.12:	Input voltage (V_{in}), DC-link voltages (V_{dc1} & V_{dc2}), output voltage (V_{AB}) and load current (i_{load}) during load disturbance.	6-13

Fig. 6.13:	Input voltages (V_{in1}) and DC-link voltages (V_{dc1} & V_{dc2}) and output voltage (V_{AB}) (b) Zoom-in view of the plot (a).	6-14
Fig. 6.14:	Total DC link voltage (V_{dc}), Inverter output voltage (V_{AB}), input voltage (V_{in}), grid voltage (V_g) and grid current (i_g).	6-14
Fig. 6.15:	Efficiency curve of qSC-5LI.	6-17
Fig. 6.16:	Loss distribution in switches, diodes, inductor, and capacitors at 400W in qSC-5LI.	6-17
Fig.A.1:	A view of the fabricated laboratory prototype	A-1

LIST OF TABLES

Table 1.1	Various codes and standards for PV system	1-8
Table 3.1	Pole voltage (V_{AO}) for different switching combinations	3-4
Table 3.2	Hardware Prototype Parameters	3-14
Table 3.3	Comparison of different impedance topologies with the proposed topology	3-22
Table 4.1	switching combinations to achieve 7-level operation	4-4
Table 4.2	Hardware Prototype Specifications	4-14
Table 4.3	Comparison of the proposed power converter with qZS topologies	4-19
Table 5.1	Different switching logic to obtain 5-level operation	5-4
Table 5.2	Effective CMV of the power converter for D=0.25	5-10
Table 5.3	Experimental Specifications	5-13
Table 5.4	Comparison of the proposed power converter with 5-level qZS topologies	5-19
Table 6.1	Switching states to achieve five-level operation	6-4
Table 6.2	Parasitic voltage of the power configuration for D=0.1.	6-10
Table 6.3	Operating parameters of hardware prototype	6-11
Table 6.4	Comparison of the QSC-5LI with five-level quasi-z-source Multilevel inverters	6-16

Abbreviations

FCMI	Four-level CMI
LSPWM	Level-shifted Space Vector PWM
VSIs	voltage source inverters
ZSI	Z-source inverter
qZS	Quasi-Z-source
qZSI	Quasi-Z-source inverter
STI-1	Shoot-Through Inverter-1
STI-2	Shoot-Through Inverter-2
CHB	Cascaded H-Bridge
CHB-MLI	Cascaded H-Bridge Multilevel inverters
CMI	Cascaded Multilevel Inverter
FC	Flying capacitor
SVPWM	Space Vector Pulse Width Modulation
STPWM	sine-triangle PWM
PD	phase disposed
TSV	Total Standing Voltage
NST	Non-shoot-through
ST	Shoot-through
MLSPWM	Modified level-shifted PWM
CMV	Common-mode voltage

PSIM	Powersim
FPGA	Field Programmable Gate Arrays
LSPWM	Level Shifted Pulse Wish Modulation
MATLAB	Matrix Laboratory
MLI	Multilevel Inverter
MOSFET	Metal–oxide semiconductor with field-effect transistor
MPPT	Maximum Power Point Tracking
MPP	Maximum Power Point
NPC	Neutral Point Clamped
P&O	Perturb and Observe
PF	Power Factor
PI	Proportional Integral
PLECS	Piecewise Linear Electrical Circuit Simulation
PLL	Phase Locked Loop
PR	Proportional Resonant
PV	Photovoltaic
PWM	Pulse Width Modulation
RMS	Root Means Squares
SOGI	Second Order Generalized Integrator
SPWM	Sinusoidal Pulse Width Modulation
SVPWM	Space Vector Pulse Width Modulation

SC	Switched Capacitor
THD	Total Harmonic Distortion
UPF	Unity Power Factor
ESR	Equivalent series resistor

List of Symbols

V_{XO}	pole voltage
V_{XN}	Phase voltage
V_{CM}	Common-mode voltage
T^*_{gx}	Normalized modulating signal
T_s	Sampling time period
T_{sh}	Shoot-through time
S_{hx}	Shoot-through pulses
B	Boost factor
M	Modulation index
D	Shoot-through duty ratio
V_{dcx}	DC-link voltages
$V^*_{dctotal}$	Reference total DC-Link voltage
$V_{dctotal}$	Total DC-Link voltage
$S_1, S_2 \ldots S_n$	Switching devices of the inverter.
i^*_d	d-axis reference current
i^*_q	q-axis reference current
V^*_d	d-axis reference voltage
V^*_q	q-axis reference voltage
V_{in}	Input voltage
V_{cx}	Capacitor voltages

I_{L1}	Inductor current
i_x	Phase current.
V_{PV}	PV voltage.
I_{PV}	PV current
V_g	Grid voltage
i_g	Grid current
i^*_g	Reference grid current
V^*_{dc}	reference DC-link voltage
V_{AB}	Load voltage
V_{out}	Output voltage
N_L	No of levels
N_{sw}	No of switches
Psw	Mosfet switching losses
P_{con}	Mosfet conduction losses
P_{sd}	Diode switching losses
P_{cd}	Diode conduction losses
P_{ind}	Inductor conduction loss
P_{cap}	Capacitor ESR loss
v_m	Sinusoidal modulating signal
v^*_m	modified reference signal

C	Carrier signal
V_{Lx}	Inductor voltages
i^*_g	Reference grid current
V_{mcm}	Effective CMV
R_D	Damping resistor
C_p and C_n	Parasitic capacitor
V_{cp}	Voltage of PV parasitic capacitor
Vscx	Switched capacitor voltage
V_{shx}	DC reference signal
i_{leak}	Leakage current
i_{load}	Load current
Scx	Switched capacitor voltages

Chapter 1

Introduction

Chapter 1

Introduction

1.1 General overview

The impending shortage of conventional sources of electric power has accelerated the prominence of research and development of alternative forms of energy. Of the available renewable forms of energy, solar and wind display massive potential to supplement conventional sources of energy. In particular, power generation with solar photovoltaic (PV) panels offers several advantages such as reliability of the source and clean energy. Reduced electricity bills and low maintenance costs are the contributing factors to the proliferation of solar energy systems.

With these benefits, PV-based power generation is increasingly becoming popular around the world, resulting in several large-scale installations with significant investments. Most developed and developing countries have consistently promoted solar PV energy systems through governmental support. Of all the nonconventional energy sources available, PV power occupies 24.3% of the total share [1]. In India, solar power installations have increased from 2.6 GW to more than 61is GW in the last 7 years. India is now in the 4th global Position for overall installed renewable energy capacity [2].

In general, PV systems are configured either as stand-alone systems or grid-connected applications. As the PV power is produced at low DC voltage, there is a need for a power electronic interface between the PV source and load/grid to obtain the AC output voltage of the required magnitude and frequency as shown in Fig .1.1. In this figure, *'C_p'* and *'C_n'* represent the parasitic capacitors of the PV panel, *'L_g'* represents the grid inductance and *'R_g'* represents the ground resistance.

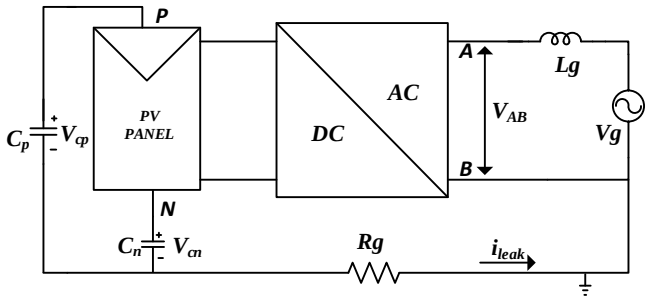

Fig .1.1: General layout of a grid-tied PV inverter.

Further, there are also some disadvantages associated with PV generation. The major drawbacks are the huge installation cost and low conversion efficiency of the PV source. Therefore, the design and selection of the power electronic interface employed in the PV system should offer higher efficiency. Hence, in recent years, researchers have proposed several power configurations to achieve higher efficiency. The following sections discuss the different types of power converters based on the modular structure of the PV source [3-4].

1.2 Classification of PV inverters

The grid-connected PV systems can be classified into the central inverter, string inverter, and microinverter based on the modular structure of the PV panels [5].

1.2.1 Central inverters

The central inverters are the primitive PV inverters that are used in PV farms. A large number of PV panels are interconnected in series and parallel to provide high power level (MW) and DC voltage to avoid further amplification (shown in Fig.1.2 (a)). However, the drawbacks associated with these power converters are: (i) the requirement of high voltage DC cables between inverter and PV modules (ii) higher power loss incurred due to centralized MPPT (iii) the requirement of string diodes (iv) development of hotspots in the PV panels up on the occurrence of significant unequal shading.

1.2.2 String inverters

These inverters are scaled-down versions of centralized inverters. Several PV modules are connected in series to form a string that is directly interfaced with the inverter (shown in Fig.1.2 (b)). There is no need for additional string diodes which improves efficiency. Further, each string of PV panels can be associated with an individual MPPT controller thereby improving the overall efficiency when compared to centralized inverters. However, the following are the drawbacks associated with these converters (i) a higher number of components (ii) each string requires a separate inverter (iii) the shaded PV panel restricts the amount of power the PV string can produce.

1.2.3 Microinverter

The microinverter is an integration of a PV panel and inverter working as a single entity (shown in Fig.1.2 (c)). As each PV panel is associated with an individual inverter, separate

MPPT control can be implemented to improve the effectiveness of the MPPT [6]. Further, the 'plug and play' feature of the microinverter simplifies the tasks of maintenance and installation. The effect of shading is minimized on the overall system as all PV modules are isolated. However, the following are the drawbacks associated with these converters (i) high component count (ii) cost per watt increases (iii) a two-stage system is employed to boost the input DC voltage and invert the DC to AC.

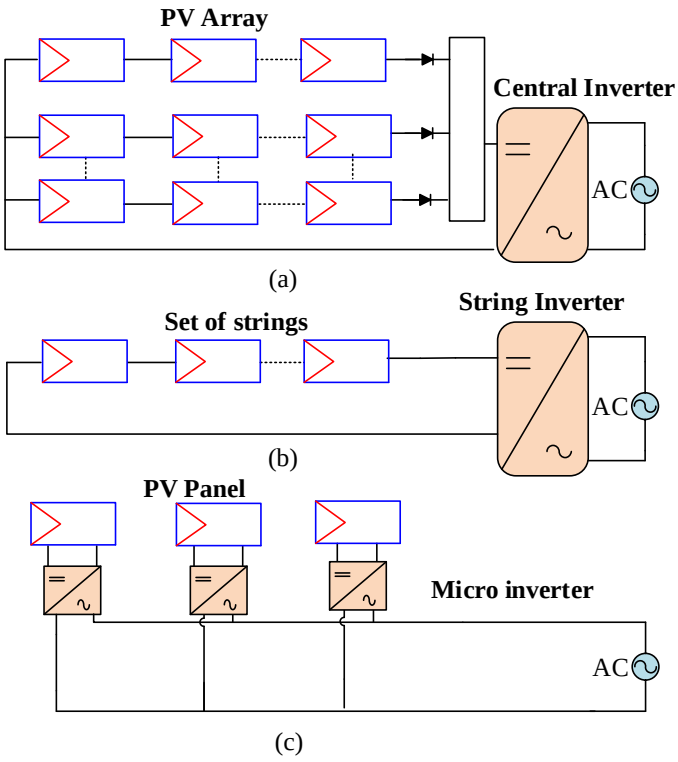

Fig .1.2: Overview of PV inverters (a) Central inverter (b) string inverter (c) Microinverter.

1.3 Interfacing PV source with grid

This section discusses the modifications in the PV inverter topologies based on the number of power processing stages and the employment of a transformer [7].

1.3.1 Number of power processing stages

Solar PV systems often require the conversion of low output voltages of PV panels into AC of required voltage and frequency to cater to the requirements of consumers. In practice, it is often accomplished by a two-stage conversion process. Firstly, the low DC voltage output by the PV panels is boosted to attain the required DC voltage level using a DC-DC boost converter. Apart from voltage boosting, this converter plays the pivotal role of rendering the

maximum power point tracking (MPPT) capability to the solar PV system. The DC voltage, thus boosted, is then converted into AC using a conventional voltage source inverter (VSI) to deliver AC power of the required voltage and frequency to the end-users (as shown in Fig.1.3(a)). Despite its popularity, the two-stage conversion system increases the cost and complexity, taxing the efficiency and reliability of the power circuit.

The improvement of system efficiency, decreasing the cost and increasing the power density demands for the reduction of power stages of the converter. In contrast to the two-stage conversion, the PV power is directly processed to load/grid through the inverter in the single-stage conversion. A single-stage inverter executes both maximum power tracking and grid current control through a single-power processing stage (as shown in Fig.1.3 (b)). These incorporate advantages such as good MPP tracking, high efficiency, low component requirement, compact design, and high reliability when compared to the two-stage inverter.

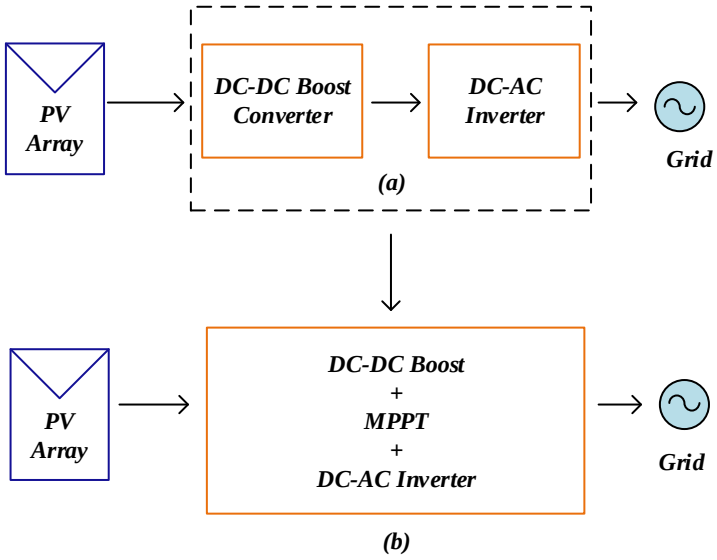

Fig .1.3: Block diagram of (a) Two-stage power converter (b) Single-stage power converter.

1.3.2 Isolated/Non-Isolated inverter

The aforementioned single-stage and double-stage inverters are further classified into isolated and non-isolated inverters. In isolated inverters, a high-frequency transformer is employed in a DC-DC converter, or a line-frequency transformer is connected across the grid. Galvanic isolation can be provided by both high-frequency and low-frequency transformers, which eliminates the flow of leakage current. However, the utilization of a low-frequency transformer increases the overall cost and makes the system bulky. Further,

the inclusion of the high-frequency DC-DC isolation stage increases the number of power processing stages in the system, which results in reduced efficiency.

In non-isolated power converters, due to the absence of a transformer, the power converter becomes lighter, has a higher power density, and is more efficient. However, the absence of galvanic isolation creates a resonant path that generates leakage current.

From the aforementioned discussion, it can be concluded that a single-stage non-isolated power converter is the most viable solution to achieve high efficiency with less component count. Therefore, the problem of leakage current should be addressed by modulation techniques and semiconductor rearrangement.

1.4 Leakage current

Fig.1.1 shows the single-stage non-isolated inverter for a grid-connected PV system. It may be noticed that, without the isolation transformer, there exists a direct ground current path between the PV panel and the grid [8]. As PV cells accumulate a considerable charge on their surfaces, parasitic capacitances are formed between the cell-to-frame (C_{p1}), cell-to-rack (C_{p2}), and cell-to-ground (C_{p3}) as shown in Fig 1.4. These capacitances depend on the physical dimensions of the panel and atmospheric conditions. In a practical PV system, the frame of the PV panel, and the mounting rack are grounded. Hence they assume equal potential. Therefore, all three parasitic capacitances are connected in parallel and the equivalent value of the parasitic capacitance is the summation of all partial capacitances (C_{p1}, C_{p2}, and C_{p3}).

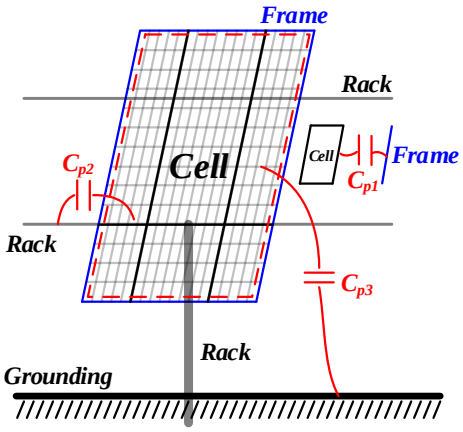

Fig 1.4: Parasitic capacitances in a typical PV Panel.

Further, the common-mode voltage of the power converter results in high-frequency voltage transitions across this parasitic capacitor. In the absence of galvanic isolation, this capacitive coupling facilitates the flow of leakage current from the PV panel to the ground. This leakage current is constituted by both low-frequency and high-frequency switching components which injects harmonics into the grid. This results in an increased power loss in the system, reduced longevity of PV panels, and a compromise in the safety issues to operating personnel [9].

Therefore, to ensure the safety of the operating personnel, this leakage current should be limited to less than 300mA as per the stipulation laid out by the standard VDE0126-1-1[10]. Since the parasitic capacitance varies greatly depending on atmospheric conditions and construction, a lumped equivalent value of 100nF/kW was chosen for the experimental studies of the proposed power converters in this thesis.

1.5 Single-stage non-isolated power converters with voltage boosting

In the last two decades, considerable research work has been carried out in the area of *single-stage non-isolated boost inverters* to circumvent the disadvantages associated with the traditional two-stage inverter topologies. The motivation behind this research is to improve the performance of the single-stage power converter regardless of its efficiency, size, and complexity.

These single-stage boost topologies are categorized into the following topologies (i) current source inverters (ii) active buck-boost inverters (iii) impedance inverters [11]. The current source inverter is inherently a single-stage boosting converter. However, it requires a bulky inductor at the input. The buck-boost functionality can be derived with the employment of an additional *Active Boost Network* to buck-boost inverter. These power converters typically employ an inverter that is cascaded to an AC/AC boosting network. These power converters avail AC/AC boosting at an expense of additional active switches. The disadvantages of bulky inductors and an excess number of switching devices for boosting are overcome with the impedance source inverters. They are capable of handling low PV voltages with a wide variation in voltage while providing inherent protection from shoot-through faults [12-13]. In the year 2003, *Peng* introduced the first impedance power converter namely the Z-source inverter (ZSI). This converter is capable of achieving the twin objectives of boosting and inversion simultaneously. These impedance-based power

converter has been extensively researched in the past two decades. Subsequently, researchers have suggested various topological and modulation-based modifications to improve the performance of the conventional ZSI. Among these, the quasi-Z-source inverters are the most prominent. The disadvantage associated with the conventional ZSI, namely the discontinuous input current, is successfully overcome with the quasi-Z-source (qZS) inverters [14]. Furthermore, the voltage rating of one of the capacitors is significantly reduced in qZSIs, compared to the conventional ZSIs.

Based on the limitations of various transformerless power circuit configurations and their modulation schemes reported in the earlier literature, this thesis investigates different qZS-based topologies to improve their performance.

1.6 PV inverter standards in grid-tied operation

The PV inverters should be designed to comply with various international standards [15-19] while injecting power into the grid. The following is the list of important parameters, which should be considered for grid-tied operation (i) grid current THD (ii) injected direct current (iii) range of grid frequency (iv) power factor (v) leakage current.

As per the PV standards (IEEE 1547, AS4777, EN 61000-3-2), the maximum THD allowable in the grid current should be restricted to 5%. This improves the power quality at the distribution feeder. Further, the injected DC into the grid is limited to 0.22% to 1% of the rated output current. The range of grid frequency varies with different countries as shown in Table 1.1. According to the standard stipulated by VDE-AR-N-4105, the inverter should be capable of delivering reactive power within the power factor range of 0.8 to 0.95. Finally, the leakage current should be limited to less than 300mA (RMS) according to the standard stipulated by VDE 0126-1-1. Further, the circuit should be opened within 0.3sec when the RMS current is higher than 300mA.

TABLE 1.1 VARIOUS CODES AND STANDARDS FOR PV SYSTEM

	THD	**DC current injected**	**Grid frequency(Hz)**	**Power factor**
IEEE 1547	< 5%	<0.5% of rated output power	57 -60.5	0.9 to 0.97
AS4777	< 5%	<0.5% of rated output power	48-52	0.8-0.95
EN 61000-3-2	< 5%	<0.5% of rated output power	47.5-50.2	NA

1.7 Organization of the thesis

This thesis is structured into seven chapters, which are summarized as follows:

Chapter 2 presents a comprehensive review of several Z-source and quasi-Z-source three-phase and single-phase topologies. The motivation for the problem formulation and objectives of the thesis are also presented in this chapter.

Chapter 3, presents a three-phase quasi-Z-source based four-level cascaded MLI for Photovoltaic application. In this chapter, a detailed view of the working principle of the power converter along with the proposed modulation scheme is presented. Further, the improved boost factor of the four level inverter is obtained using mathematical analysis. It is shown that in the stand-alone mode of operation, the output voltage can be regulated by controlling the shoot-through duty ratio of the quasi-Z-sources networks. In addition, it is also shown that, during grid-tied mode of operation the twin objectives of MPPT and active power injection into the grid is achieved by controlling the shoot-through duty ratio and modulation index.Further, the experimental studies validates the concept and performance of the proposed inverter. Finally, the proposed configuration is compared with the existing multilevel inverter configurations to emphasize its features and merits.

Chapter 4, presents a single-stage dual quasi-Z-source 7-level inverter along with its PWM technique. The working principle and various modes of operation of the proposed seven-level inverter are presented. Further, the implementation of the proposed PWM scheme, analysis of the boost factor, and design of the qZS network of the power converter are presented. In addition, it is also shown that the proposed topology can regulate the output voltage in the stand-alone mode, and can inject active power into the grid in the grid-tied mode of operation. This chapter also addresses how to minimise high-frequency voltage transitions across the parasitic capacitor to reduce leakage current. The experimental studies are presented to validate the operation of the power converter. Finally, the comparison of the proposed power converter with the other existing qZS inverter is presented to highlight its benefits.

Chapter 5, proposes a single-staged quasi-Z-source-based five-level inverter topology, as well as a modulation technique. The working principle and different modes of operation of the proposed power converter are presented. Analysis of leakage current is also presented for

the proposed inverter. Furthermore, in this chapter, the performance of closed-loop control schemes for the proposed power converter in both stand-alone and grid-tied modes of operation is assessed. Experimental results are presented to validate the operation of the proposed power converter. Finally, the benefits obtained by the proposed power converter, compared to the other converters reported in the literature are presented.

Chapter 6, presents a single-stage quasi-switched capacitor-based five-level inverter for PV systems. Various modes of operation of the proposed configuration are presented along with its proposed PWM scheme. Also, the reduction of the leakage current in the proposed power converter is analyzed with common mode and differential mode analyses of the power converter. Experimental results are presented to validate the proposed configuration. Further, a comparison with existing qZS-5LI is presented to highlight the features of the proposed configuration.

Chapter 7, summarizes the important findings of the research work reported in this thesis and suggests possible extensions for future work.

Chapter 2

Literature survey

Chapter 2

Literature survey on Impedance source inverters

2.1 Introduction

As mentioned in the preceding chapter, impedance-source inverters belong to the category of single-stage power converters. Power converters belonging to this class are capable of deriving the twin objectives of voltage boosting as well as inversion from a single entity. Two-stage power converters are currently being used required for low or variable-voltage renewable energy sources. In such a scenario, it makes an interesting study as to how the impedance-source inverters compare vis-à-vis the two-stage converters.

This chapter comprehensively reviews various impedance source networks and different single-phase and three-phase impedance source inverters for PV systems.

2.2 The Impedance source inverter

The first impedance source inverter namely the "Z-source inverter" was introduced in 2002[12]. This power converter consists of the impedance network, which is made up of inductors, capacitors, and diodes to boost or buck the voltage. The impedance network employs two inductors (L_1 and L_2) and two capacitors (C_1 and C_2) connected in an X shape to interface the inverter to the DC source as shown in Fig.2.1.

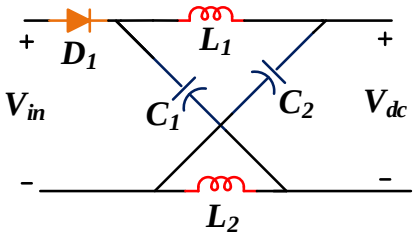

Fig 2.1: The Z-source inverter

To illustrate the operating principle of the Z-source inverter a three-phase voltage-fed Z-source inverter is used as an example. In a conventional three-phase inverter we have six active states and two zero states. In addition to these states, the Z-source inverter has a state known as the "shoot-through state" where a single leg or multiple legs of the inverter are short-circuited in an instant. The shoot-through states are forbidden in conventional VSIs as it leads to the short-circuiting of the input source and damage the switches.

It should be noted that the conventional VSIs and CSIs are capable of operating as buck and boost converters respectively. The shoot-through state is strictly forbidden for a VSI making it work exclusively as a buck-type converter. On the other hand, the CSI uses the shoot-through states to obtain the boost capability. In contrast, the impedance-source inverters, with the shoot-through states can provide the buck-boost capability, which is unique to this class of converters.

To analyze the voltage gain offered by the Z-source inverter, a brief mathematical analysis regarding the operation of the power converter is presented below.

Z-source inverter operates in two modes namely, (i) shoot-through mode and (ii) non-shoot-through mode. During the shoot-through mode, the inverter output terminals are short-circuited and no energy is transferred from source to load. Further, the input source is disconnected from the inverter, and both the inductors store energy from the capacitors. This stored energy along with the input DC supply is fed to the load during the non-shoot-through state.

Applying voltage sec balance during shoot-through and non-shoot-through states, and considering the symmetry of the Z-source network the following voltage equations are derived.

During Non-shoot-through

$$V_L = V_{in} - V_C \tag{2.1}$$

$$V_{dc} = (2V_C) - (V_{in}) \tag{2.2}$$

During Shoot-through

$$V_L = V_C \tag{2.3}$$

$$V_{dc} = 0 \tag{2.4}$$

Application of the volt-sec balance to all of the inductor voltages over one switching time period paves the way to the derivation of the boost factor obtained with the Z-source inverter. Each switching time period consists of one of the NST modes (equations 2.1-2.2) & the ST mode (equations 2.3-2.4). It may be noted that the symmetry of the Z-source networks results in $V_{C1}=V_{C2}=V_C$ and $V_{L1}=V_{L2}=V_L$.

The voltages across the capacitors are expressed as:

$$V_{C1}=V_{C2}=\frac{(1-D)}{(1-2D)}V_{in} \tag{2.5}$$

Where 'D' is the shoot-through duty ratio, defined as T_{sh}/T_s. (where T_{sh} and T_s respectively denote the shoot-through time and the time period of the switching cycle).

Hence, the boosted DC-link voltage from equation (2.2) is expressed as:

$$V_{dc}=\frac{1}{(1-2D)}V_{in} \tag{2.6}$$

Where $B=\frac{1}{(1-2D)}$ is the boost factor of ZSI.

Therefore, the peak fundamental output phase voltage of the inverter is expressed as:

$$\hat{V}=\frac{1}{2}*M*B*V_{in} \tag{2.7}$$

Where 'M' is the modulation index and 'B' is the boost factor.

Despite these advantages of boosting, inherit shoot-through immunity, and single-stage conversion, the ZSI also suffers from the following drawbacks (i) discontinues input current due to the presence of input diode (ii) huge component size (iii) no common ground. Therefore to address these drawbacks a modified ZSI known as a quasi-Z-source inverter (qZSI) is proposed in [14]. Fig. 2.2 shows the schematic of the qZSI, it may be observed that an input inductor is always in connection with the source which results in continuous input current waveform. Further, the voltage rating of one of the capacitors is decreased in comparison with ZSI which leads to reduce the size of the capacitor.

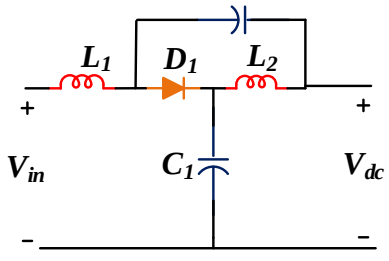

Fig .2.2: Quasi-Z-source inverter

Hence, it can be inferred that qZSI provides higher benefits like reduced component rating, continuous input current, and common ground feature than ZSI with the same boost factor.

2.3 Classification of impedance source networks

To further minimize the drawback associated with the Z-source and the qZS inverter topologies, several impedance networks are developed. These developments are primarily classified into three types [20] (i) non-transformer (ii) Active switch (iii) Transformer coupled impedance networks. Fig 2.3 presents different topologies associated with these three different types of impedance networks. These new topologies are mainly developed to reduce the ratings and quantity of passive components and to improve the boost factor when compared to the Z-source network. These three classifications are further discussed in detail in the following subsections.

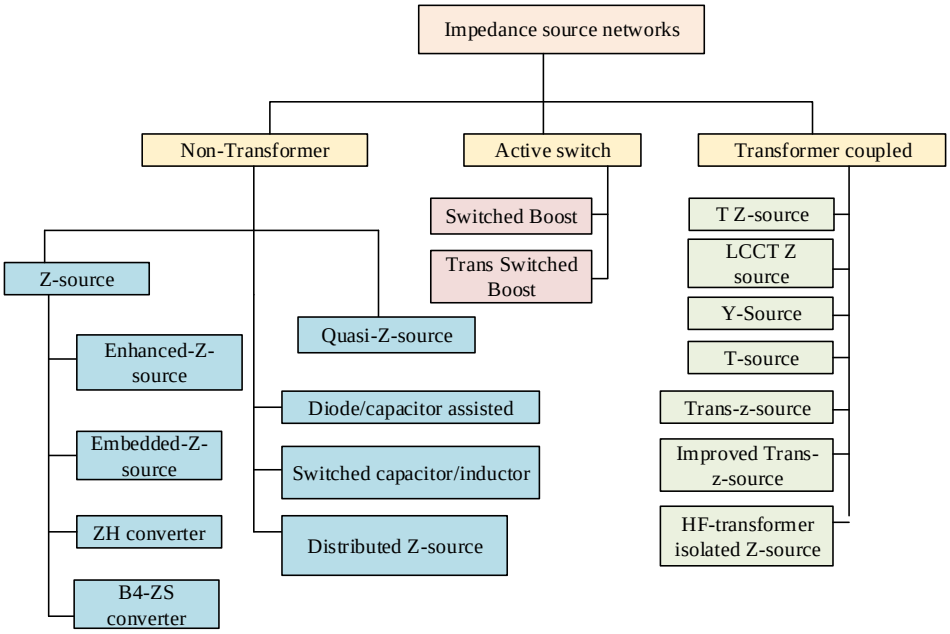

Fig. 2.3: Classification of impedance source networks

2.3.1Non-transformer impedance networks

2.3.1.1 Embedded Z-source

Fig. 2.4 shows the schematic of the embedded Z-source network [21-22]. This impedance network provides continuous input current and has low capacitor voltage. Therefore, it is suitable for PV applications. Further, this topology employs two DC sources which reduce the voltage and current ripple. However, these two input sources operate asymmetrically which is the major disadvantage. Further, this increases the cost and no of components.

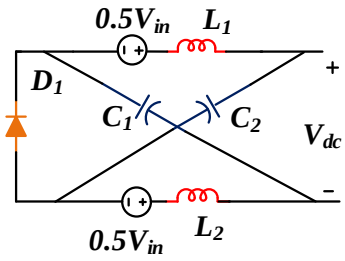

Fig. 2.4: Embedded Z-source network

2.3.1.2 Switched inductor/capacitor network

To improve the boost factor of the Z-source network and reduce the stress on passive elements, inductors are replaced with switched inductors in this topology (as shown in Fig 2.5). This topology provides continuous input current with lower voltage stress. However, these advantages are obtained at an expense of increased passive device count and cost [23-25].

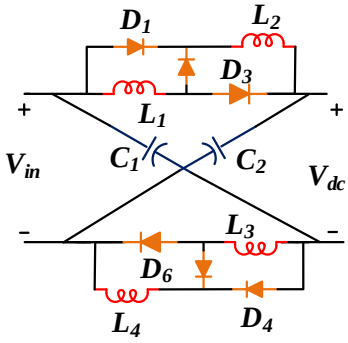

Fig. 2.5: Switched inductor Z-source network

2.3.1.3 Capacitor/Diode assisted network

Similar to the above-mentioned topologies, the capacitor/Diode assisted networks are formed by the addition of some diodes and capacitors to the qZS network. These modifications are implemented to increase the voltage gain of the qZS network. Fig.2.6 shows the different possible extended boost qZS topologies [26-27]. Similar to the above impedance network, the voltage gain is obtained at the expense of increased passive devices.

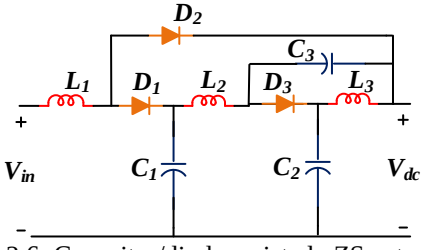

Fig. 2.6: Capacitor/diode assisted qZS network

2.3.2 Active switch impedance networks

The main aim of these active switch impedance networks is to achieve the advantages of ZSI topology with only half of the number of passive components. These topologies namely "switched inductor networks" consists of one inductor, capacitor, diode, and an active switch as shown in Fig 2.7[28]. However, these networks could not overcome the drawbacks of ZSI such as discontinuous input current, low boost, and high voltage stress on the capacitor. Further, these topologies are extended by adding an inductor in the input to make the current continuous as shown in Fig 2.7(b).

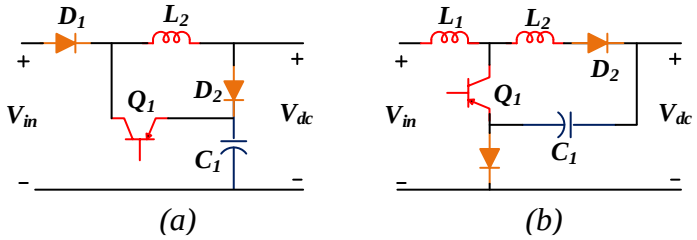

Fig. 2.7: (a) Switch Boost inverter (b) Trans-switch boost inverter

2.3.3 Transformer-coupled impedance networks

To improve the power density and overall system cost, coupled inductors and transformers are employed in the Z-source and quasi-Z-source networks. The following topologies are based on coupled or transformer impedance networks.

2.3.3.1 Trans-Z-source/Trans-QZ-source topologies

In topologies like ZS, qZS, and embedded Z-source inverters the gain offered by the impedance network could be even infinity. However, when the gain is greater than '3' the voltage stress across the switches is high. Trans-Z-source and Trans-QZ-source with the discontinuous and continuous operation have been proposed in [29-31]. These topologies achieve higher voltage boosting, and lesser voltage stress by employing only one coupled inductor, one diode, and one capacitor as shown in Fig .2.8.

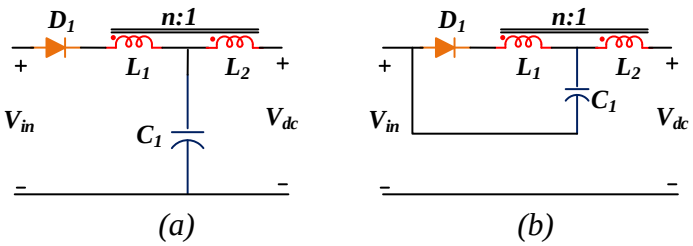

Fig. 2.8: (a) Trans. ZSN (b) Trans.QZSN

Further based on the no of coupled inductor winding and their arrangement in Trans-Z-source topologies the following impedance networks are derived (i) Y-source (ii) T-source

and (iii) TZ-source. These topologies achieve a higher boost factor by changing the turns-ratio of the coupled inductor. The drawbacks associated with these topologies are the presence of leakage inductance. Furthermore, the coupled inductor in trans-Z-source topology is replaced by a high-frequency transformer to derive an LCCT-Z-source topology [32]. It employs an inductor-capacitor-capacitor-transformer as shown in Fig 2.9. The structures for LCCTZSN and quasi-LCCTZSN are provided in Fig. 2.9(a) and Fig. 2.9(b) respectively. The presence of the quasi counterpart makes the converter draw a smooth input current from the source, which is essential for PV power generation.

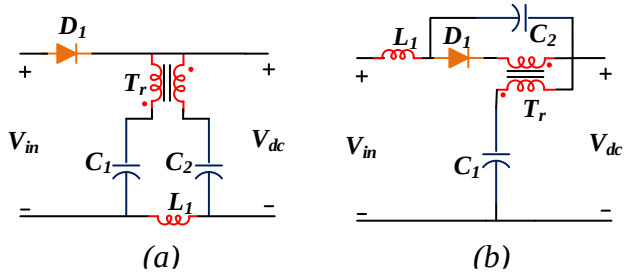

Fig. 2.9: (a) LCCT ZSI (b) LCCT QZSI

To address the shortcomings of the conventional ZSI and enhance its performance, several changes and improvements have been proposed for the original ZSI. Some were able to enhance the capacity more effectively, while others were able to lower the capacitor voltage and the start-up inrush current. The aforementioned impedance network can be integrated with existing MLI structures to form a single-stage boosting inverter based on the application.

2.4 Multilevel Inverters

MLIs have recently received a lot of attention, both from the research community and from industry, as they are emerging as a viable technology for a wide range of applications. Baker and Bannister produced the first patent in the middle of the 1970s that described a converter architecture capable of generating multilevel voltage from independent DC voltage sources [33]. This power converter namely the “Cascaded H-Bridge inverter” consists of a series of single-phase inverters connected to an isolated DC source. Further, this power converter is modified to produce a multilevel output voltage from a single DC source and with extra diodes connected to the neutral point. This topology is well known as “Neutral point clamped MLI” [34]. Further, a flying-capacitor-based MLI is proposed in [35], which was widely used for three-level and five-level applications.

All the aforementioned MLI have several attractive features as follows (i) lower output voltage THD waveform (ii) less dv/dt stress on the switches (iii) reduced filter size, and (iv) electromagnetic interface. However, the requirement for more components, balancing capacitor voltages, and increased control complexity limits the use of MLIs for higher-level operations. In addition, MLIs are essentially buck-type power converters. Therefore, they require a higher input DC voltage to achieve the desired output voltage. This necessitates a boosting stage to increase the output voltage between PV and MLIs. Thus, the amalgamation of impedance-network with multilevel inverters can inherit the benefits associated with both of these topologies [37-39] for photovoltaic applications.

2.5 Impedance source Multilevel Inverter

In this section, the proposed impedance source multilevel inverter topologies in the literature for both three-phase and single-phase systems are presented. Furthermore, a brief description of their benefits and drawbacks is provided.

2.5.1 Three-phase impedance source multilevel inverter topologies

Most of the research work regarding the integration of Z-source and multilevel inverters is carried out considering the conventional NPC and CHB converter topologies. In the work reported in [40-41], two isolated DC sources are connected to two Z-sources to obtain the required buck-boost capability. The boosted DC-link is connected to a three-level NPC MLI at the back-end (shown in Fig.2.10). The resulting system is a typical single-stage system as the shoot-through time period required for the Z-source is provided by the back-end three-level inverter. However, it is an expensive proposition due to the additional clamping diodes and the requirement of a complex modulation technique for proper balancing of the shoot-though in Z-source network.

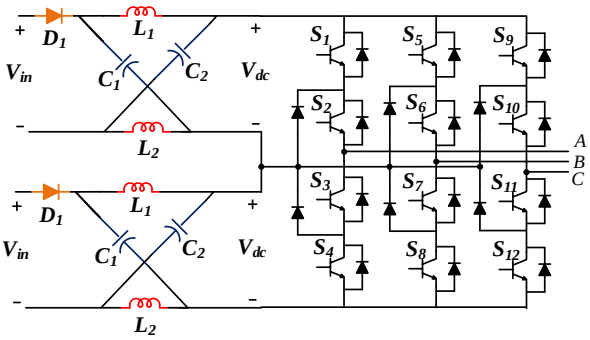

Fig. 2.10: Z-source NPC three-level inverter

The single Z-source topology, reported in [42], also requires two DC sources. Compared to [9], it needs only one impedance network(shown in Fig 2.11(a)). However, the cost of the system is not reduced, as the size and component ratings of the passive elements are doubled. Following these developments, a few more power circuit configurations have been proposed, which employ a single DC source and a single Z-source [43] (shown in Fig 2.11(b)). However, the main disadvantage of these topologies is the discontinuous input current, which should be avoided in PV applications. The requirement of achieving a continuous input current led to the development of three-level qZS-NPC topologies [44] shown in Fig. 2.12. An early topology belonging to this category consists of a symmetrical combination of two qZS networks, which form a T-type structure with a common neutral point.

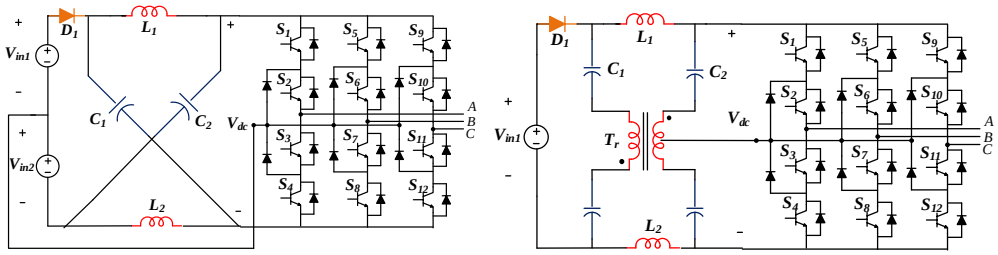

Fig. 2.11: (a) Single Z-source NPC three-level inverter (b) Modified Z-source NPC three-level inverter

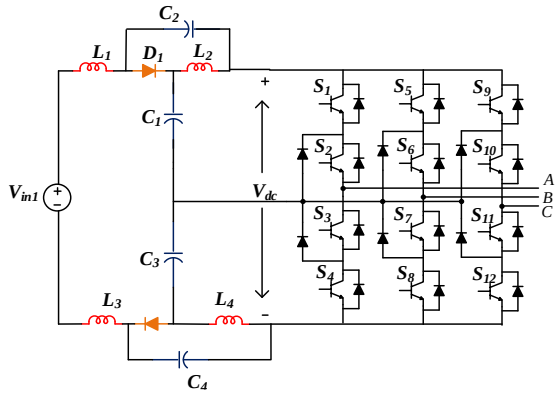

Fig. 2.12: Quasi-Z-source NPC three-level inverter

A modified qZS-based power circuit configuration is proposed in [45], which needs fewer switching devices. In this power converter, two qZS networks are connected to a 3-level T-type inverter as shown in Fig. 2.13. Both of these topologies display drawbacks such as (i) deviation of the neutral point voltage due to the unbalancing of the capacitor voltages (ii) additional clamping diodes and (iii) the non-improvement of boost factor compared to the traditional qZSI [44][45].

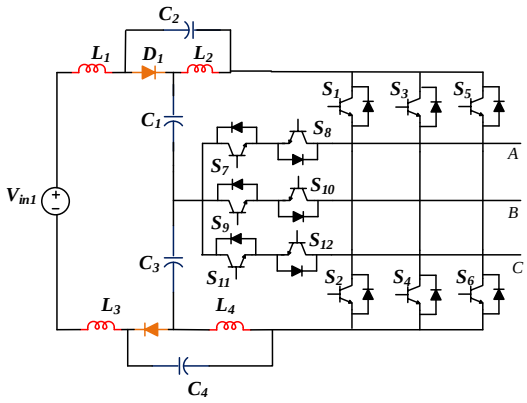

Fig. 2.13: A three-level Quasi-Z-source based T-type inverter.

Cascaded H-Bridge Multilevel inverters (CHB-MLI) are comprised of multiple units of H-bridge inverters, which reduce the requirement of the DC-link voltage for each inverter. They also provide an output voltage waveform with much lesser THD and *dv/dt* [46-48]. Recently, a combination of qZS and CHB-MLI is proposed, which combines the advantages of both CHB-MLIs and the quasi-Z sources [49-50]. In these configurations, individual qZS networks are connected to each H-bridge inverter to obtain the required voltage boosting. However, these systems require individual MPPT and DC-link voltage [51-52].

Figure 2.14 shows a single-stage, three-phase qZS-CHB MLI [51] that requires nine isolated PV sources, 36 semiconductor switching devices, and the associated gate-drive circuitry. Though the qZS-CHB MLI converter displays a higher efficiency, the cost, and complexity of control increase with the number of levels in the output voltage. This is due to the requirement of implementing MPPT individually for each qZS and controlling its dc-link voltage.

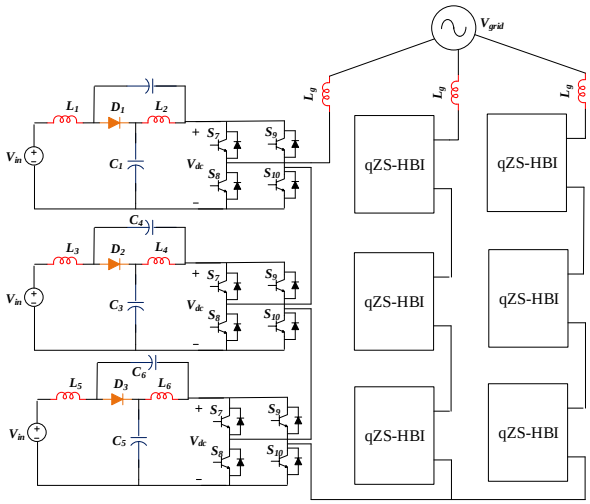

Fig. 2.14: Quasi-Z-source CHB inverter

2.5.2 Single-phase impedance source multilevel inverter topologies

Initial investigations of single-stage systems were confined to the Z-source-based CHB and the NPC systems. Fig 2.15 displays a seven-level inverter topology reported in [53], wherein a cascaded Z-source network with two switches is connected to an H-bridge inverter. This power converter requires fewer semiconductor switches compared to the ZS-NPC topologies. However, this topology needs three isolated Z-source networks, which increases the number of passive components. The drawback of discontinuous input current associated with the Z-source-MLIs is overcome by fusing the NPC and CHB topologies with a quasi-Z-source.

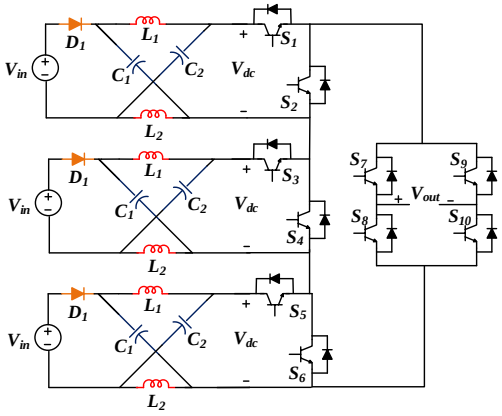

Fig. 2.15: Z-source seven-level inverter

A 3-level qZS-NPC topology was reported in [54], wherein two symmetrical qZS networks are interfaced with an NPC inverter. This topology suffers from the drawbacks associated with the conventional NPC such as additional clamping diodes and neutral-point deviation [55-56]. In qZS-CHB topologies [57-58], each unit of the H-bridge inverters is interfaced with a qZS network to boost the voltage of an isolated PV panel(as shown in Fig.2.16). However, the extension of CHB topologies to a higher number of voltage levels involves a corresponding increase in the number of qZS networks (and the associated passive components). Other complexities associated with the qZS-based CHB inverters are: (i) distributed MPPT control, and (ii) individual DC-link voltage regulation [59].

Fig. 2.17 presents a 5-level inverter [60], which employs only one inductor and one capacitor in each qZS, halving the number of passive components, compared to the earlier topologies. However, two diodes and two switches are additionally needed in this topology to provide the boosting capability, increasing the switching power losses in semiconductors. All of the aforementioned topologies [56-60] require more than one PV source.

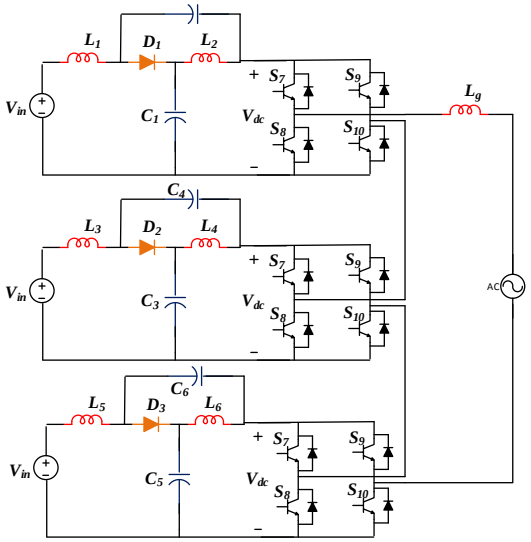

Fig. 2.16: Quasi-Z-source single-phase CHB inverter

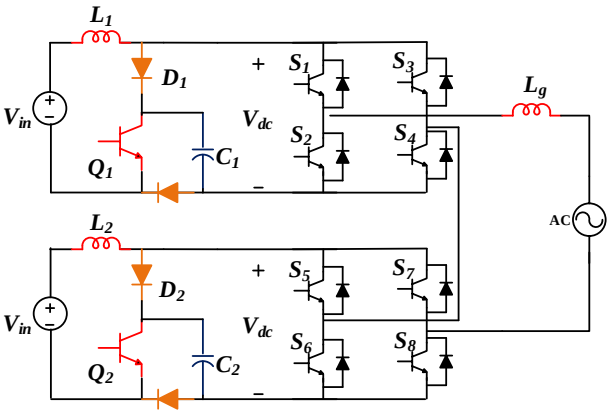

Fig. 2.17: Quasi-switched boost inverter

In an attempt to minimize the number of input sources and inductors, a modified power converter is proposed in [61]. As shown in Fig. 2.18, the power converter employs eight switching devices, two inductors, and one PV source to produce a 5-level output voltage waveform. However, this topology results in increased voltage and current stresses in the devices when compared to the multiple-source qZS-CHB topologies. Furthermore, the input current from the DC source is discontinuous., which doesn't auger well for PV applications.

The qZS-based 5-level topology presented in [62] employs eight switching devices and is a combination of NPC and T-type inverters. This topology suffers from the drawbacks of additional clamping diodes which are required for freewheeling operation.

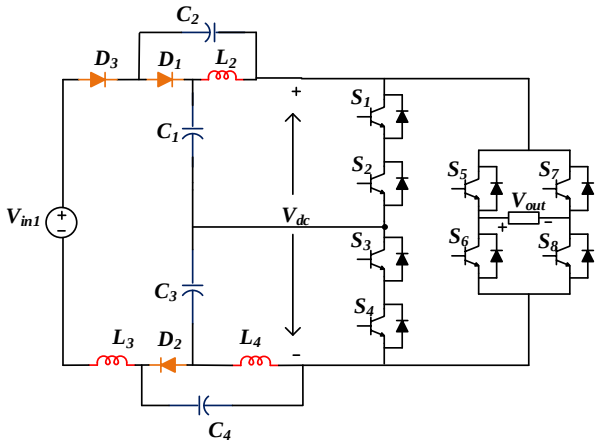

Fig. 2.18: Modified quasi-Z-source five-level inverter

Leakage current is another major issue in PV-fed grid-connected transformerless inverters [68-69]. High-frequency transitions in the Common mode voltage (CMV) of the MLI charge the parasitic capacitance of the PV panel, facilitating the flow of leakage current. If this leakage current is not restricted to the prescribed limits, the safety of the PV system could be compromised. Apart from the regular switching transitions, the shoot-through states (which are deliberately introduced in ZS / qZS-based MLIs to achieve the required voltage boosting) also contribute to the high-frequency transitions in CMV.

In conventional single-phase inverters, the CMV is reduced either with modulation schemes of inverters or by devising newer topologies. In modulation methods, appropriate voltage vectors are employed to reduce the CMV [63-64]. Alternatively, additional semiconductors are used to decouple AC and DC sides to eliminate the leakage current [65]. For three-phase qZSI topologies, the CMV is reduced by the modification of SVPWM [66-67] and the addition of a fast recovery diode in the negative path of the PV panel [68].

To minimize the high-frequency voltage transitions in CMV for a single-phase qZSI, a modified PWM technique is suggested in [69], which chooses appropriate zero states. The power converter topology described in [70] employs two additional switches to create an alternative path between the negative DC terminal of the PV panel to the grid (as shown in Fig 2.19). These switches are operated at the grid frequency to clamp the parasitic voltage across the capacitor either to zero or to the grid voltage. The proposed power converter in [71], connects two extra switches and diodes across the grid terminals (shown in Fig. 2.20). These additional devices are switched during the zero states to isolate the PV source from the grid, paving the way to the minimization of voltage transitions in the CMV. However, the

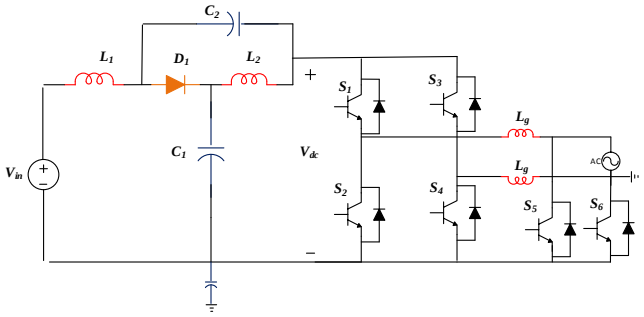

Fig. 2.19: Quasi-Z-source with additional switches

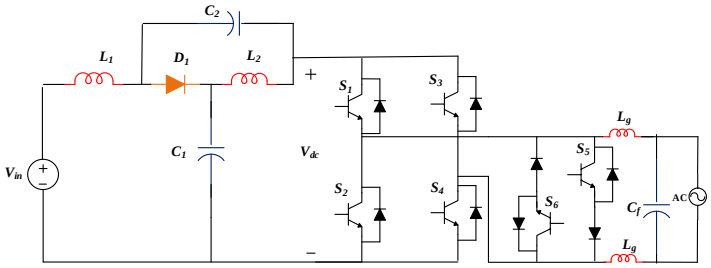

Fig. 2.20: Quasi-Z-source with AC decoupling switches

aforementioned literature [69-71] is limited to the minimization of leakage current in qZS-based single-phase 2-level inverter topologies.

2.6 Motivations

Based on the above literature review, the following observations were made w.r.t the existing Impedance source Multilevel inverter topologies:

1. In three-phase impedance source MLI, the majority of the literature is confined to only three-level systems. Further, these investigations are carried out with conventional CHB and NPC-based topologies. Therefore, the drawbacks associated with the conventional CHB and NPC are also manifested in these topologies.
2. In the three-phase Z-source MLI, the single-stage operation with voltage boosting and multilevel output is achieved with the expense of large voltage stress across the switching devices and discontinuous input current which is not favorable for PV applications.
3. The three-phase qZS-CHB topology achieves low switching stress across switches with a continuous input current. However, the complexity of MPPT control and DC-link voltage regulation increases with an increase in voltage levels.
4. Further, most of the existing three-phase impedance source MLI have the conventional boosting of ZS / qZSI. Therefore, a higher shoot-through duty ratio ‘D’ is implemented which limits the modulation index ‘M’ to a lower value.

5. The 5-level and 7-level single-phase impedance source inverters have some drawbacks such as the employment of multiple DC sources, increased switch count, and discontinuous input current.
6. In addition, the leakage current minimization in ZS/qZS inverters is only confined to the two-level inverters.

The above-mentioned limitations of the three-phase and single-phase ZS/qZSI are the motivations for the research carried out in this thesis.

2.7 Objectives

The research work presented in this thesis puts an effort to fulfill the following objectives:

1. Development of three-phase and single-phase impedance source multilevel inverter configurations with high gain for multiple and single string PV modules with minimum switching devices and continuous input current.
2. Propose new modulation techniques to simultaneously achieve higher voltage boosting with output voltage inversion.
3. To minimize the high-frequency voltage transition across the parasitic capacitor of the PV panel thereby reducing the leakage current within the stipulated limit set by the VDE0126-1-1 standard.
4. Analyses of the steady-state and dynamic performances of the quasi-z-source multilevel inverter during the stand-alone and the grid-tied modes of operation.

Chapter 3

A Quasi-Z-Source Based Space Vector Modulated Cascaded Four-Level Inverter for Photovoltaic Applications

Chapter 3

A Quasi-Z-Source Based Space Vector Modulated Cascaded Four-Level Inverter for Photovoltaic Applications

3.1 Introduction

In Chapter 1 it is stated that the qZS based NPC topologies suffer from the drawbacks such as (i) deviation of the neutral point voltage due to the unbalancing of the capacitor voltages (ii) additional clamping diodes and (iii) the non-improvement of boost factor compared to the traditional qZS. The qZS-based CHB topologies also incur a higher cost and complexity of control with the number of levels in the output voltage. This is due to the requirement of individual MPPT for each qZS network and the regulation of its DC-link voltages.

In general, multi-level inversion can be obtained with a relatively new topology known as the Cascaded Multilevel Inverter (CMI) [72]. This topology brings in a considerable reduction in the number of DC sources and switching devices compared to the CHB-MLI configuration. Unlike the NPC and the flying capacitor (FC) MLI topologies, the CMI doesn't require clamping diodes/capacitors. For a comparable number of voltage levels in the output (phase voltage) waveform, CMIs require fewer DC input power supplies and power semiconductor switching devices. Owing to the reduced number of components, the reliability of a CMI would be higher compared to the aforementioned power converter configurations.

Therefore, this chapter proposes a new power converter configuration, which is obtained by the amalgamation of qZS networks with a Four-level CMI (FCMI) to achieve single-stage conversion. It is shown that, when the proposed power converter is modulated with a carrier-based Level-shifted Space Vector PWM (LSPWM) scheme, it would result in 50% higher boosting capability compared to the NPC 3-level and the CHB-based systems. Furthermore, better spectral performance is obtained by the proposed converter as it outputs more voltage levels, compared to the aforementioned topologies. It is also shown that the proposed LSPWM scheme implements the shoot-through state, required for the qZS, using the FCMI without any additional power loss in the semiconductor switching devices. The principles of the proposed power converter topology, as well as the PWM technique are experimentally verified with a laboratory prototype.

3.2 The proposed Quasi-z-source based four-level cascaded MLI(QZS-FCMI)

The proposed PV fed qZS based four-level cascaded multilevel inverter (qZS-FCMI) is shown in Fig.3.1. In this circuit configuration, four-level inversion is achieved by the cascaded connection of three basic 2-level voltage source inverters (VSIs). Two of these inverters are pivotal in implementing the shoot-through mode, which is essential for the operation of the qZS networks. Thus, these are named as Shoot-Through Inverter-1 (STI-1) and Shoot-Through Inverter-2 (STI-2) respectively. The output terminals of STI-1 (A_1, B_1, C_1) and STI-2 (A_2, B_2, C_2) are connected to the DC input terminals of the third VSI (Fig. 3.1), which steers the output of these two shoot-through inverters to the load/grid. Hence, it is named the Output Inverter.

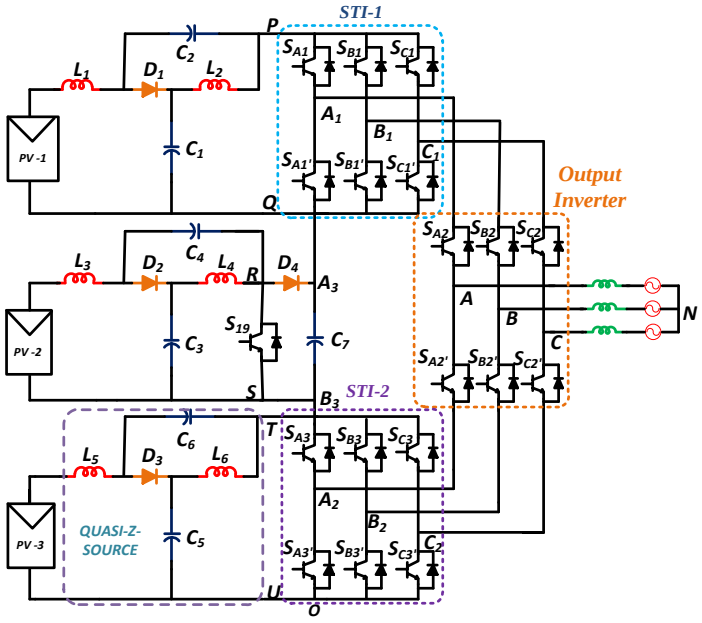

Fig. 3.1: Proposed qZS-FCMI.

These VSIs are fed with three identical qZS networks, which boost the low input voltages of isolated PV panels to the desired levels. The middle qZS network is accompanied by a switch (S_{19}), a DC-link capacitor (C_7), and a diode (D_4). These components provide a constant DC-link voltage at terminal points (A_3, B_3).

Similar to the conventional Z-source inverter the qZSI operates in two modes, namely: (i) the shoot-through mode and, (ii) the non-shoot-through mode. In the shoot-through mode, energy from the PV source as well as the capacitors (C_1, C_2) is stored in the inductors (L_1, L_2) by turning on the switches in each phase of the inverter. This stored energy in the inductors is

then transferred to the load during the non-shoot-through mode of the qZSI. The presence of the impedance networks before the inverters avoids the requirement of the dead-band circuitry for protection against the shoot-through fault. This topology consists of 19 power semiconductor switching devices (S_1-S_{19}). The shoot-through mode is inserted for the top and the bottom quasi-Z sources through the phase-legs of the STI-1 and the STI-2 Inverters. A separate switch (S_{19}) is used to introduce the shoot-through mode in the middle qZS.

3.2.1 Switching states and the output voltage of the Four-level Inverter

The pole voltages (the voltages of the 'A', 'B', and 'C' points shown in Fig. 3.2 w.r.t the point 'O') of the qZS four-level inverter are denoted as V_{AO}, V_{BO}, and V_{CO} respectively. Table 3.1 shows the details regarding the switching states of the individual devices pertaining to the A-phase of the proposed FCMI and the pole voltage (V_{AO}). In Table 3.1 and for the rest of the work, the logic levels '1' and '0' respectively indicate the 'on' and the 'off' states of the switching devices present in the proposed power converter. From Table 3.1, it is evident that each pole voltage of the proposed converter is capable of assuming four levels, thus making it a four-level VSI.

TABLE 3.1: POLE VOLTAGE (V_{AO}) FOR DIFFERENT SWITCHING COMBINATIONS

State type	Pole Voltage (V_{AO})	Level No	Pole (A) terminal connection (See Fig.3.1)	Switching states (1-ON, 0-OFF)					
				S_{A1}	$S_{A1'}$	S_{A2}	$S_{A2'}$	S_{A3}	$S_{A3'}$
NST	V_{DC}	3	P	1	0	1	0	0	0
NST	$\frac{2V_{DC}}{3}$	2	Q	0	1	1	0	0	0
UST				1	1	1	0	1	0
NST	$\frac{V_{DC}}{3}$	1	T	0	0	0	1	1	0
NST	0	0	U	0	0	0	1	0	1
LST				0	1	0	1	1	1

NST**-Non shoot-through,UST**-Upper shoot-through,***LST**-Lower shoot-through.

The shoot-through switching states for phase-A of the STI-1 and STI-2 Inverters are also shown in Table 3.1. From this table, it may be noted that whenever a shoot-through state is inserted in any given phase in the STI-1, the pole voltage of that phase falls from a level of 'V_{DC}' to a level of '$2V_{DC}/3$'. Similarly, whenever a shoot-through state is inserted in any given phase-leg in the STI-2, the pole voltage of that phase becomes 0 V.

The pole voltages of the cascaded qZS four-level inverter can be expressed as:

$$V_{AO} = S_{A2} * S_{A1} + \frac{(S_{A2'} * S_{A3})}{3} + \frac{(S_{A1'} * S_{A2}) * 2}{3} \tag{3.1}$$

$$V_{BO} = S_{B2} * S_{B1} + \frac{(S_{B2'} * S_{B3})}{3} + \frac{(S_{B1'} * S_{B2}) * 2}{3} \tag{3.2}$$

$$V_{CO} = S_{C2} * S_{C1} + \frac{(S_{C2'} * S_{C3})}{3} + \frac{(S_{C1'} * S_{C2}) * 2}{3} \tag{3.3}$$

Common mode voltage will be the average of three-pole voltages as shown

$$V_{CM} = (V_{AO} + V_{BO} + V_{CO})/3 \tag{3.4}$$

Phase voltage of the inverter using the above equations

$$V_{AN} = V_{AO} - V_{CM} \tag{3.5}$$

$$V_{BN} = V_{BO} - V_{CM} \tag{3.6}$$

$$V_{CN} = V_{CO} - V_{CM} \tag{3.7}$$

Thus, the phase voltages are expressed as:

$$V_{AN} = (2 * V_{AO})/3 - (V_{BO}/3) - (V_{CO}/3) \tag{3.8}$$

$$V_{BN} = (2 * V_{BO})/3 - (V_{CO}/3) - (V_{AO}/3) \tag{3.9}$$

$$V_{CN} = (2 * V_{CO})/3 - (V_{BO}/3) - (V_{CO}/3) \tag{3.10}$$

3.3 Control strategy for the proposed QZS-FCMI

3.3.1 Implementation of the SVPWM scheme

In general, the Space Vector Pulse Width Modulation (SVPWM) is preferred as it results in 15% more utilization of the DC-link voltage compared to the sine-triangle PWM (STPWM). In this work, the SVPWM is implemented by adopting the switching scheme described in [73], wherein the concept of imaginary switching time periods is introduced. Operating only on the references (denoted by v_a^*, v_b^* and v_c^*), this scheme directly outputs the gating waveforms for a two-level VSI. The on-time periods of the gating signals pertaining to the top switching devices in a two-level VSI (i.e. devices connected to the positive DC rail) are denoted by the time periods T_{ga}, T_{gb} and T_{gc}.These time periods replicate the waveforms of the references (i.e. $v_a^*, v_b^*,$ and v_c^*). This work uses the normalized modulating signals denoted as T_{ga}^*, T_{gb}^* and T_{gc}^*, which are the per-unit values, obtained on the base value of the sampling time period of T_s.

In general, the implementation of SVPWM can be either sample-based or carrier-based. This work uses the latter, as it is more convenient to implement for the present system. Of the several variants of the carrier-based implementations, the Level-Shifted PWM (LSPWM) is

selected to implement the SVPWM scheme, as it offers advantages such as ease of implementation. In the LSPWM technique, phase-disposed (PD) carrier waveforms are used, where the three triangular carrier waves are in phase and are displaced vertically by an equal amount of 1/3. These reference waves (T_{ga}^{*}, T_{gb}^{*} and T_{gc}^{*}) are compared with the top, middle, and bottom carrier waves to produce the switching signals for the three two-level inverters shown in Fig. 3.2.

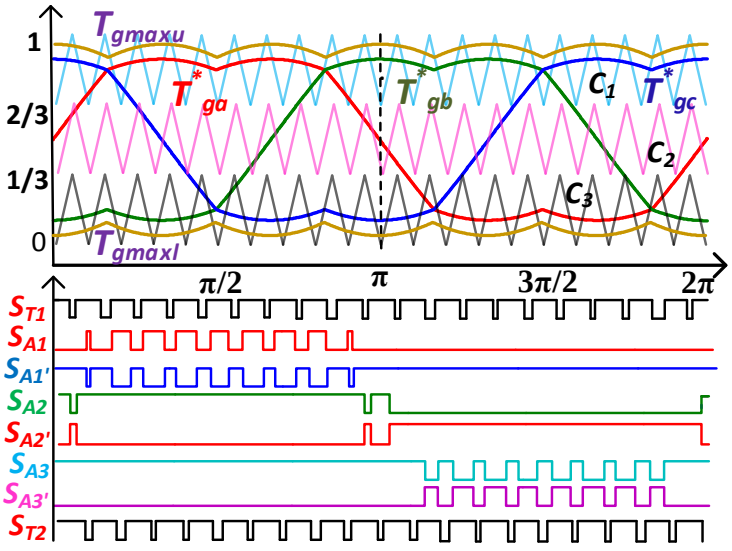

Fig. 3.2: Implementation of phase-A switching for qZS-FCMI.

3.3.2 Insertion of the shoot-through in the FCMI

In order to introduce the shoot-though, the maximum and minimum envelope of the reference waves are generated using equations (3.11) & (3.12).

$$T_{g\max} = MAX\left(T_{ga}^{*}, T_{gb}^{*}, T_{gc}^{*}\right) \tag{3.11}$$

$$T_{g\min} = MIN\left(T_{ga}^{*}, T_{gb}^{*}, T_{gc}^{*}\right) \tag{3.12}$$

These envelopes ((T_{gmax}) and(T_{gmin}) are modified by shifting them in opposite directions by half of the required shoot-through time (denoted as T_{sh}). The modified references are respectively denoted as (T_{gmaxu}) and(T_{gminl}) which are given in the following expressions (13) & (14).

$$T_{g\max u} = T_{g\max} + (D/2) \tag{3.13}$$

$$T_{g\min l} = 1 - T_{g\min} - (D/2) \tag{3.14}$$

The shoot-through duty factor 'D' is defined as $D = \frac{T_{sh}}{T_s}$

The modified envelopes given by equations (3.13) & (3.14) are compared with the respective carriers to obtain the *shoot-through pulses* for the STI-1 and STI-2 as shown in Fig. 3.2. To obtain the desired gating signals to implement the required shoot-through time period, a logical 'OR' operation is performed between the shoot-through pulses (S_{T1}, S_{T2}) and the original gating signals (which are produced by the comparison of the original references T_{ga}^*, T_{gb}^* and T_{gc}^* and the carrier waveforms). Thus, the required voltage boosting is obtained.

The implementation of shoot-through for the proposed converter is explained with the space vector diagram of the FCMI, which consists of three concentric hexagons (Fig.3.3) which consist of three concentric hexagons. While the tip of the reference vector is located in the innermost hexagon for the 2-level operation, it is located in the middle and the outer layers respectively for three-level- and four-level operations. From Table 3.1, it is evident that each pole-voltage assumes four switching states independent of the other two, resulting in a total of 64 (4^3) useful switching states for the four-level FCMI. These (64) switching states result in 37 voltage space vectors. It may be noted from Fig. 3.3, that the entire space-vector diagram is divided into 54 sectors.

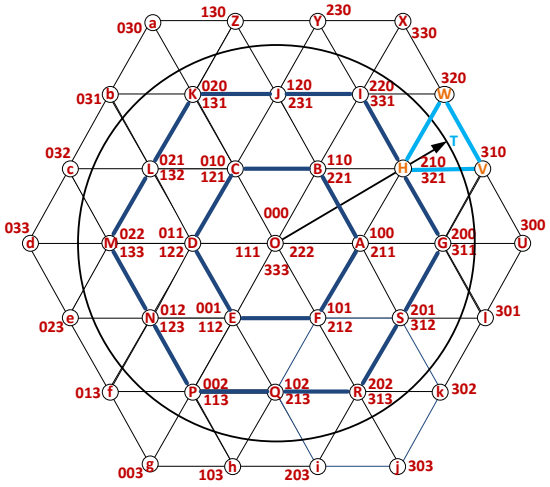

Fig. 3.3: Space vector diagram of FCMI.

Let an instant be considered, wherein the reference voltage vector ($\overrightarrow{OT}$) is situated in the sector 'HVW' as shown in Fig. 3.3. The objective of the LSPWM scheme is to synthesize this reference voltage vector in the average sense, over the sampling time period (denoted as $'T_s'$). The switching sequence required to synthesize this reference voltage is given by: [210]-[310]-[320]-[321] as shown in Fig. 3.4. The phase-disposition (PD) strategy ensures that the nearest vectors, which are situated in the closest proximity to the reference voltage vector, are switched while allowing only one transition between the switching of the successive vectors.

A typical sequence [210] denotes that pole-A is connected to point 'Q', pole-B is connected to point 'T' and pole-C is connected to point -U as shown in Fig. 3.5(a). It may be noted that all three output points of the STI-1 (A_1, B_1, C_1) are clamped to the negative rail of the top qZS network when the vector [210] is switched (i.e. the STI-1 is operated with a null-vector. This facilitates the introduction of the shoot-through state in the STI-1, by turning on switch S_{A1}) as shown in Fig. 3.5(a). The implementation of the shoot-through state in the [210] state is shown in Fig. 3.4 (the region in red color).

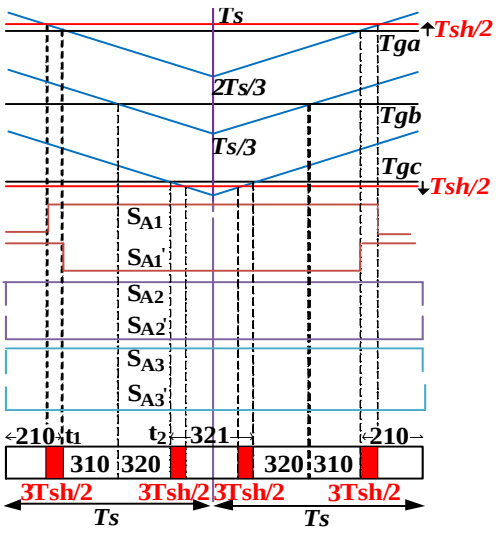

Fig. 3.4: Switching sequence of FCMI when reference phasor is in sector HVW.

When a transition occurs from the vector [210] to the vector [310], as shown in Fig. 3.5(b) the rising edge of the gating signal to the top-device S_{A1} is advanced by a duration of $3T_{sh}/2$, while the turn-off of the bottom-device $S_{A1'}$ remains unaltered (i.e. it occurs at 't_1' as before). Thus, the insertion of the shoot-through state does not incur additional switching power loss. In the state [310], it may be noted that: (i) the pole-A is connected to the point 'P' of STI-1 (ii) the pole-B is connected to the point 'T' of STI-2 and (iii) the pole-C is connected to the terminal 'U' of the STI-2 (as shown in Fig. 3.5(b)). Consequently, both STI-1 and STI-2 are in their active states, and power is transferred from their respective quasi-Z-sources to the load through the output inverter. When the proposed converter is switched to the [320] state, the poles A, B, and C are connected to the 'P', 'Q', and 'U' terminals as shown in Fig.3.5(c). Thus, both STI-1 and STI-2 are in their active states as in the case of the state [310].

The occurrence of shoot-through in the A-phase of the STI-1 leads to the boosting of the DC-link of the top qZS network. To ensure a balanced operation between the top- and the bottom-qZS networks, the shoot-through time is equally distributed in the STI-1 and STI-2 in a given sample time period (T_s). When the vector [321] is switched, the STI-2 is operated

with a null-vector. All three output points of the STI-2 (A_2, B_2, and C2) are clamped to the positive rail of the bottom qZS network, as shown in Fig.3.5 (d). Thus, this state is also amenable for the introduction of the shoot-through state by turning on the switch $S_{C3'}$.

When the proposed converter is switched to the [320] state, the poles A, B, and C are connected to the 'P', 'Q', and 'U' terminals as shown in Fig.3.5(c). Thus, both STI-1 and STI-2 are in their active states as in the case of the state [310].

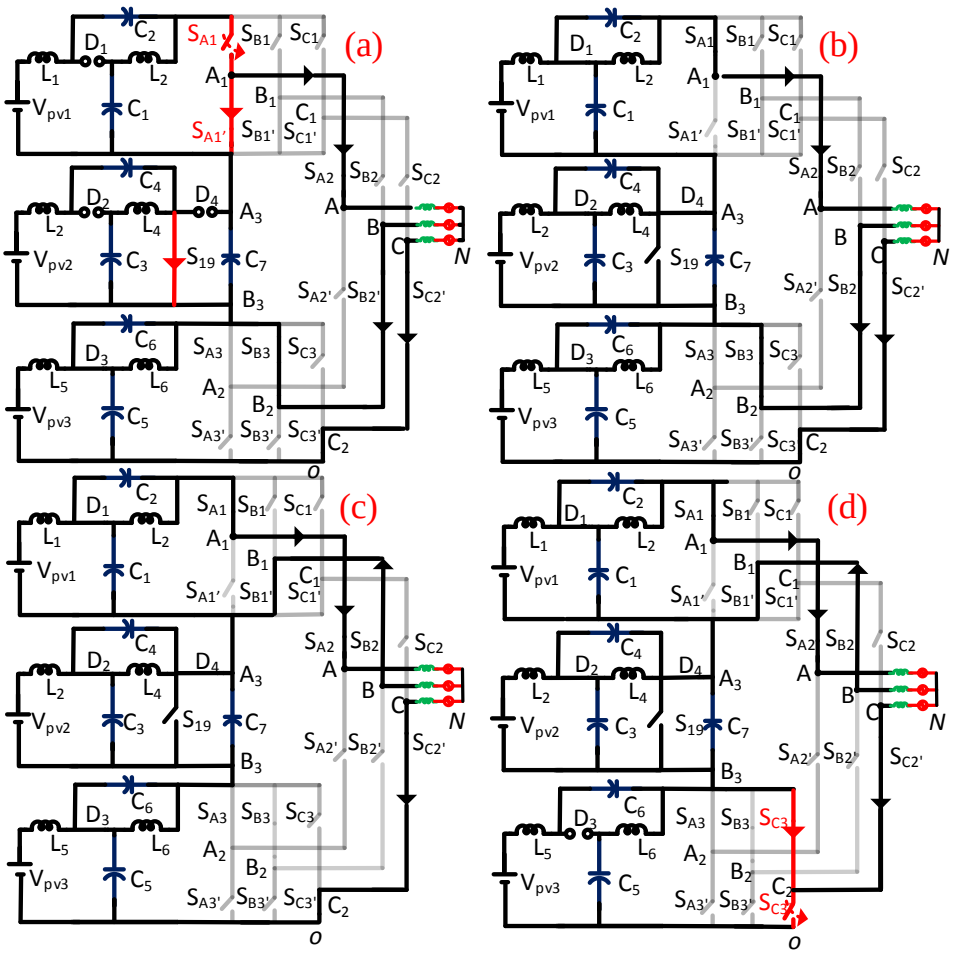

Fig. 3.5: Circuit diagrams for switching states mentioned in Fig. 3.4 (a) [210] state (b) [310] state (c) [320] state (d)[321] state in a given sample time T_s.

The occurrence of shoot-through in the A-phase of the STI-1 leads to the boosting of the DC-link of the top qZS network. To ensure a balanced operation between the top- and the bottom-qZS networks, the shoot-through time is equally distributed in the STI-1 and STI-2 in a given sample time period(T_s). When the vector [321] is switched, the STI-2 is operated with a null-vector. All three output points of the STI-2 (A_2, B_2, and C2) are clamped to the positive rail of the bottom qZS network, as shown in Fig.3.5 (d). Thus, this state is also amenable for the introduction of the shoot-through state by turning on the switch $S_{C3'}$.

From the foregoing discussion, it is obvious that there is no mechanism to introduce the shoot-through state in the middle qZS. Hence, an additional switch is provided (S_{19}, Fig. 3.1) to implement the shoot-through state and boost the low voltage output by the middle string of the PV panels.

3.3.3 Analysis of the Boost factor of the Quasi-Z-source with the proposed PWM Scheme

The references and the carrier signals corresponding to STI-1 are shown in Fig. 3.6.

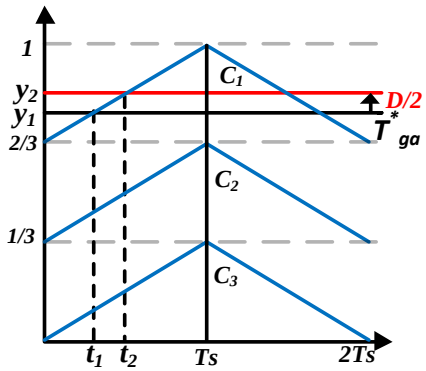

Fig. 3.6: Scaling of boost factor by LSPWM technique.

This diagram is drawn for a period, wherein the maximum value amongst the three references is assumed by the A-phase. This diagram helps to evaluate the modified boost factor in the proposed power converter. It may be observed that the slope of the top carrier wave (C_1) is 1/3.

From Fig. 3.6, the point of intersection between the upper carrier wave and the reference occurs at (t_1, y_1).The coordinates t_1 and $y_1$are related by the following expression:

$$y_1 = \frac{1}{3}t_1 + \frac{2}{3} \tag{3.15}$$

$$y_2 = \frac{1}{3}t_2 + \frac{2}{3} \tag{3.16}$$

The difference in eq (3.16) and eq (3.15) results in

$$y_2 - y_1 = \frac{1}{3}(t_2 - t_1) \tag{3.17}$$

From Fig. 3.6, it may be noted that

$$y_2 - y_1 = (D/2)$$

Hence,

$$t_2 - t_1 = (3D/2) \tag{3.18}$$

From the above equations, it is evident that an increment of (D/2) to the modulating signal 'T_{ga}^{*}' manifests as an increase in the shoot-through time period of (3D/2) (introduced in phase-A) for STI-1. Thus, it can be stated that the LSPWM results in the scaling-up of the shoot-through time period by a factor of 3, when compared to the shoot-through time period of a Z-source or a quasi-Z-source fed two-level inverter (which is equal to *'D'*). A similar conclusion can be drawn for the STI-2 as well by decrementing the reference signal $T_{gc}^{*}$by D/2 on the *lower* carrier wave (Fig.3.6).

The increment in the shoot-through time period increases the boosting capability of the inverter. As the shoot-through duty factor is modified to (3D/2), the equation governing the relationship between the shoot-through duty period (*D) a*nd the boost factor (*B*) is also modified. The relationship between the shoot-through duty (*D)* and the boost factor (*B*) for the conventional Z-source or quasi-Z-source fed inverter proposed in [14] is given by:

$$B_{conv} = \frac{1}{1-2D} \tag{3.19}$$

The boost factor for the proposed converter operated with the proposed control scheme is obtained by simply replacing the shoot-through duty (*D)* with (3D/2).

$$B_{new} = \frac{1}{1-2(\frac{3D}{2})} = \frac{1}{1-(3D)} \tag{3.20}$$

Equation (3.20) suggests that there is a considerable improvement in the boost factor with the proposed control strategy, compared to the conventional scheme. For example, when *D* = 0.2, the boost factor in the conventional scheme is given by 1.667. For the same shoot-through duty, the boost factor increases to 2.5 with the proposed power converter (an increase of 50%).

$$\hat{V} = \frac{1}{\sqrt{3}} * M * B_{new} * V_{input} \tag{3.21}$$

Equation (3.21) express the peak fundamental output phase voltage ('$\hat{V}$') of the qZS four-level inverter.

3.4 The control scheme of QZS-FCMI for stand-alone and grid-connected operation

3.4.1 Stand-alone mode

The overall gain of the proposed converter is given by the product of the boost factor (*B*) of the front-end qZS section and the modulation index (*m*) of the back-end 4-level inverter. It is evident that both of these sub-sections are mutually dependent on each other. While the front-end qZS provides the DC-link for the 4-level inverter, the latter facilitates the much-required shoot-through state for the former. As the shoot-through state is inserted in the zero (null) state, the momentary short-circuiting of the DC-link (due to the insertion of the shoot-through state) doesn't affect the waveform of the output voltage of the 4-level inverter. Generally, the modulation index (*m*) that controls the output voltage of the 4-level inverter is held constant in the stand-alone mode.

As the DC-link voltage of the 4-level inverter varies due to the fluctuations in the PV voltage, the boost factor (*B*) of the qZS is adjusted to regulate the DC-link voltage with closed-loop control and also to regulate the output voltage of the 4-level inverter at the required voltage level. As the boost factor (*B*) depends on the shoot-through duty factor (*D*, Eqn. 3.20), the output voltage is regulated simply by controlling the shoot-through duty ratio '*D*'. Fig. 3.7 shows the control scheme for the regulation of the DC-link voltage for the 4-level inverter using the shoot-through duty ratio. As the DC-links of STI-1 and STI-2 are fed from qZS networks, a pulsating voltage waveform is produced at the terminals of the DC-links (terminals P, Q, R, S, and T, U as marked in Fig. 3.1) when the shoot-through mode is inserted in each phase leg.

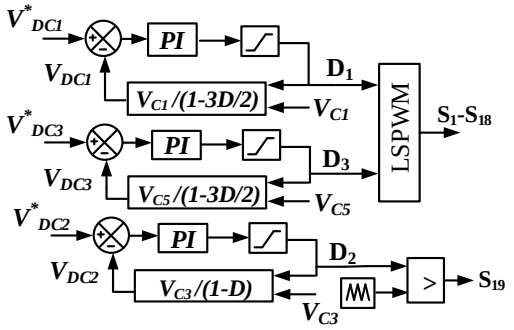

Fig.3.7: DC-link voltage control scheme for the proposed FCMI.

This pulsating waveform, such as the voltage across the points 'P' and 'Q' (Fig. 3.1), can neither be sensed directly nor can it be used as the feedback signal to regulate the DC-link

voltage. Hence the actual DC-link voltage is estimated by sensing the capacitor voltage and the shoot-through duty ratio (*D*) of the individual inverters.

The DC-link voltages V_{DC1} and V_{DC3} are compared with the references V^*_{DC1} and V^*_{DC3} respectively and the corresponding errors are input to the individual PI controllers. The PI controllers then produce the control signals, which control the shoot-through duty ratios *'D_1'* and *'D_3'*. These duty ratio signals are then utilized to generate the gating signals for STI-1 and STI-2, using the LSPWM scheme, as explained in the earlier section. As the shoot-through state for the middle qZS is inserted using the switch (S_{19}), the DC-link voltage of the Output Inverter is regulated by controlling its duty-ratio *'D_2'*(Fig. 3.7). Thus, the three peak DC-link voltages (V_{DC1}, $V_{DC2,}$ and V_{DC3}) of the inverters are regulated using the closed-loop feedback control to obtain a regulated output voltage at the consumer end.

3.4.2 The Grid-connected mode of operation

The following objectives should be fulfilled by the FCMI for grid connectivity: (i) independent MPPT control for the three qZS networks (ii) voltage control of the DC-link (iii) maintaining UPF with the grid. As the proposed converter is operated with two control parameters, namely, the shoot-through duty ratio (D) and the modulation index (m), the first of these three objectives is achieved by the exclusive control of the shoot-through duty ratio 'D', while the latter two objectives are realized by the exclusive control of 'm'.

Fig. 3.8 shows the block diagram to implement the grid control for the proposed converter. To extract the maximum power from the PV panels, the well-known Perturb & Observe algorithm is adopted. The respective voltages and currents of the three isolated PV sources are sensed and fed to the individual MPPT controllers to generate the required shoot-through duty ratio signals 'D_1', 'D_2', and 'D_3'. To track the maximum power from the top and bottom PV sources the shoot-through duty ratios 'D_1' and 'D_3' (which are equal to 'D' in steady state conditions as shown in Fig. 3.4) are fed to the LSPWM scheme to implement the shoot-through in STI-1 and STI-2 respectively. The shoot-through time period of the middle qZS network is controlled by an individual switch S_{19}. Consequently, the MPPT for PV-2 is implemented by controlling the duty ratio of the switch 'S_{19}'.

To control the total DC-link voltage ($V_{dctotal}$) of the FCMI, each DC-link voltage 'V_{DC1}', 'V_{DC2}', and 'V_{DC3}' are to be estimated. As in the case of stand-alone operation explained earlier, the total DC-link voltage ($V_{dctotal}$) is the sum of V_{DC1}, V_{DC2}, and V_{DC3}, which are

estimated by sensing the capacitor voltages and duty ratios. The PI controller, which is present in the outer voltage loop compares the actual DC-link voltage ($V_{dctotal}$) with its reference ($V^*_{dctotal}$) and outputs the d-axis reference current (i^*_d) to the inner current loop. However, the q-axis component (i^*_q) is set to zero to achieve the UPF operation. These current references (i_d^*, i_q^*) are compared with the actual d- & q-components of the grid currents (which are obtained by using Park's transformation to the measured 3-phase currents) to generate the d- and the q-axis references voltages (V^*_d, V^*_q) which determine the required modulation index [74].

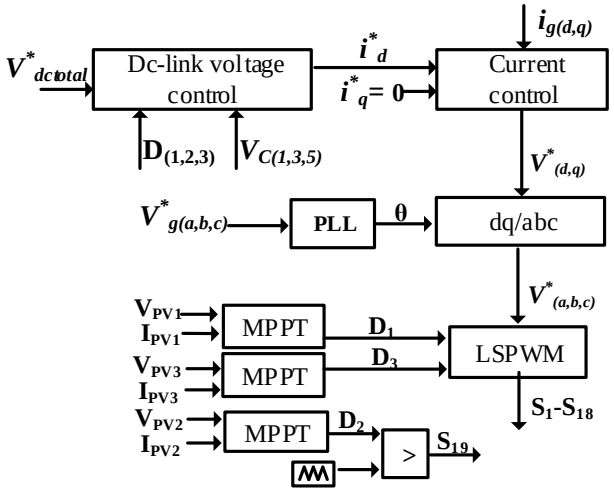

Fig. 3.8: Block diagram of the grid control scheme.

3.5 Experimental Results

A scaled-down experimental prototype of the proposed power converter has been developed to validate the working principle of the power converter (Fig. A.1). The details regarding the hardware components and the operating parameters are summarized in Table 3.2.

TABLE 3.2: HARDWARE PROTOTYPE PARAMETERS

Parameters	Values
DC input voltage(V_{in})	210V
Total boosted DC-link voltage	420 V
Rated power	870W
Nominal output phase voltage	135V (RMS)/50Hz
Switching frequency	10kHz
Modulation Index (m)	0.77
Inductors	3mH, EE65 CORE
Electrolytic Capacitors	400µF,300V
Fast recovery diode	MUR1560CT

Three programmable DC sources with CV-CC characteristics are employed to emulate the PV supply. The DC-link voltage control of the proposed four-level inverter is implemented with an SPARTAN-6 FPGA. The proposed modulation technique has been implemented using the Xilinx block set available with the MATLAB & Simulink environment. The code is deployed to the Spartan-6 FPGA module. The DL850E Yokogawa power oscilloscope is used for capturing the hardware results.

The top trace of Fig. 3.9 shows the input voltage (V_{in1}) applied to all three qZS networks, each of which is equal to 70 V. It may be observed that the DC-link voltages (V_{dc1}, V_{dc2}, V_{dc3}) of all three inverters are boosted to 140V. Thus, the boost factor of 2 is obtained with experimentation, which is in agreement with the analytical results (Eqn. 3.20). From Fig. 3.9, it is also evident that the DC-link voltages of STI-1 and STI-2 pulsate between the levels of 0 and 140V as the shoot-through time period is inserted in each phase leg of these inverters. In contrast, the DC-link voltage of the output inverter is regulated at a constant voltage of 140V by the qZSI network and the capacitor C_7.

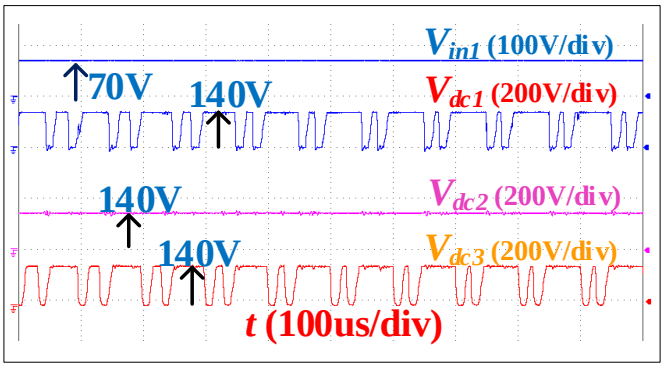

Fig. 3.9: Experimental results of input voltage (V_{in1}) and DC-link voltages (V_{dc1}, V_{dc2}, V_{dc3}) of FCMI.

The benefit obtained with the qZS in terms of the alleviation of voltage stresses across the capacitors is demonstrated in the experimental result presented in Fig. 3.10(a). With an input DC voltage of 70V (top trace) and a shoot-through duty factor (*D*) of 0.166, a pulsating DC-link voltage of 140V is obtained (second trace). The voltage of the DC-link (140 V) is distributed in the ratio of 1-3D/2: 3D/2 in the capacitors C_1 and C_2. The lower two traces of Fig. 3.10(a), which present these voltages verify these results experimentally, as the voltages across these two capacitors are 105 V and 35 V respectively. Fig. 3.10(b) shows the DC link voltage(V_{dc1}) and inductor current(i_{L1}) of the qZS network. It may be noted that an average current of 3.75A flows through the qZS inductors. These experimental waveforms clearly show the effect of the

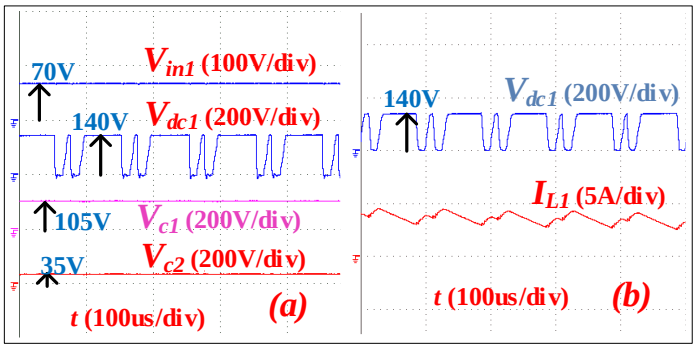

Fig. 3.10: Experimental results of (a) input voltage (V_{in1}),DC-link voltage (V_{dc1})and capacitor voltages(V_{c1},V_{c2}) of top qZS network (b) DC-link voltage (V_{dc1}) and inductor current (I_{L1})

the shoot-through time period on these inductor currents, as they increase linearly during these time periods. During the non-shoot-through states, these currents decrease linearly.

The output of the back-end 4-level inverter is presented in Fig. 3.11 when the modulation index (m) is set to a value of 0.77, as indicated in Table 3.2. The pole voltage of the A-phase (V_{BO} in Fig. 3.11), presented as the top trace, displays four distinct levels ranging from 0 V to 420 V in steps of 140V. The line and phase voltages (V_{BN} and V_{BC} in Fig. 3.11) are presented in the middle and the bottom traces in this figure respectively.

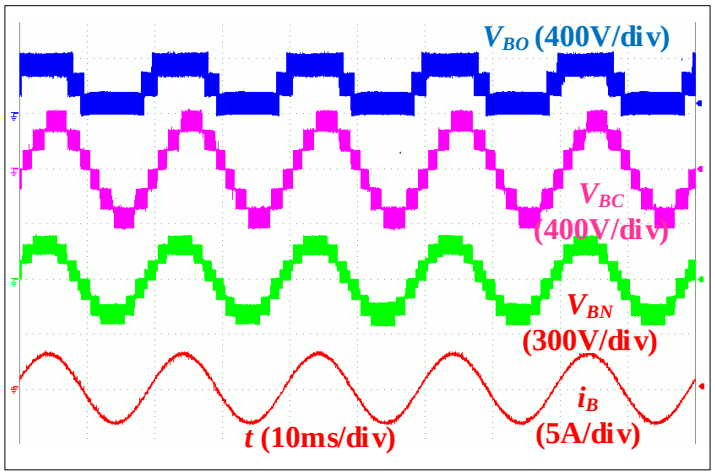

Fig. 3.11: Experimental results of Pole voltage waveform (V_{BO}), Line voltage (V_{BC}), Phase voltage (V_{BN}), and Phase current (i_B) of FCMI.

Fig. 3.12 shows the harmonic spectrum of the output phase voltage, and the phase current wherein the RMS value of the fundamental component is 135V (RMS) and 2.19A. The fundamental output voltage is in agreement with the theoretical value calculated based on the overall gain of the proposed converter, which is given by the product of the modulation index (m) and the boost factor (B) derived in Eqn. 3.21. For an input voltage of 70V, modulation index (m) of 0.77, and the shoot-through duty factor (D) of 0.166, the theoretical

value of the output phase voltage would be 135 V (RMS). Thus, the practically obtained phase voltage is concurrent with the theoretically obtained value.

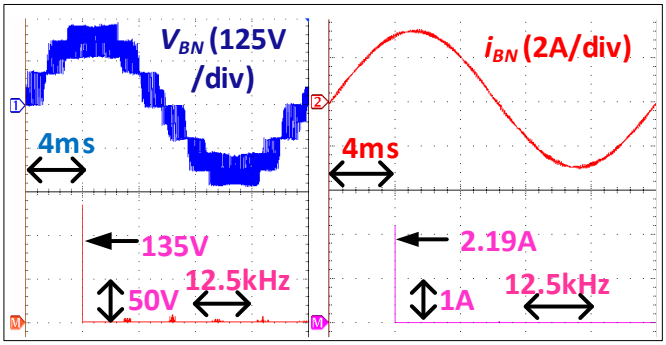

Fig. 3.12: Harmonic spectrum of the output phase voltage (V_{BN}) and phase current(i_{BN}).

Fig. 3.13 shows the effectiveness of the closed-loop control scheme (shown in Fig. 3.7) for the proposed power converter against the load disturbance while operating in the stand-alone mode. The top three traces of Fig. 3.13(a) show the DC-links voltages (V_{dc1}, V_{dc2}, and V_{dc3}). The bottom trace of this figure shows the voltage and current in one of the load phases. To study the effect of the load disturbance, the load current is suddenly doubled (from 0.67 A to 1.35 A) and is then restored to the pre-disturbance value. Figures 3.13(b) and 3.13(c) display the zoomed pictures of the DC-link voltage, the output phase voltage, and the output phase current. From Fig. 3.13(a), it is evident that sudden changes in the load current disturb the DC-link voltages momentarily and the closed-loop controller effectively regulates the DC-links against the load disturbances.

Fig. 3.14 demonstrates the regulation of the DC-link voltages against the supply disturbance with the closed-loop controller. In this experiment, all three DC inputs (V_{in1}, V_{in2}, V_{in3}, Fig. 3.14(a)) are initialized to 50 V. Then, each input is disturbed by about 25%. Firstly, the input voltage V_{in1} is decreased by 10 V and then the other two input voltages are increased by 10 V. It may be observed that the corresponding DC-link voltages, which are displayed below their respective input voltages show momentary changes; they are quickly regulated by the closed-loop action of the controller. As in the case of the load disturbance, the controller automatically adjusts the respective shoot-through duty ratios to regulate the DC-link voltages.

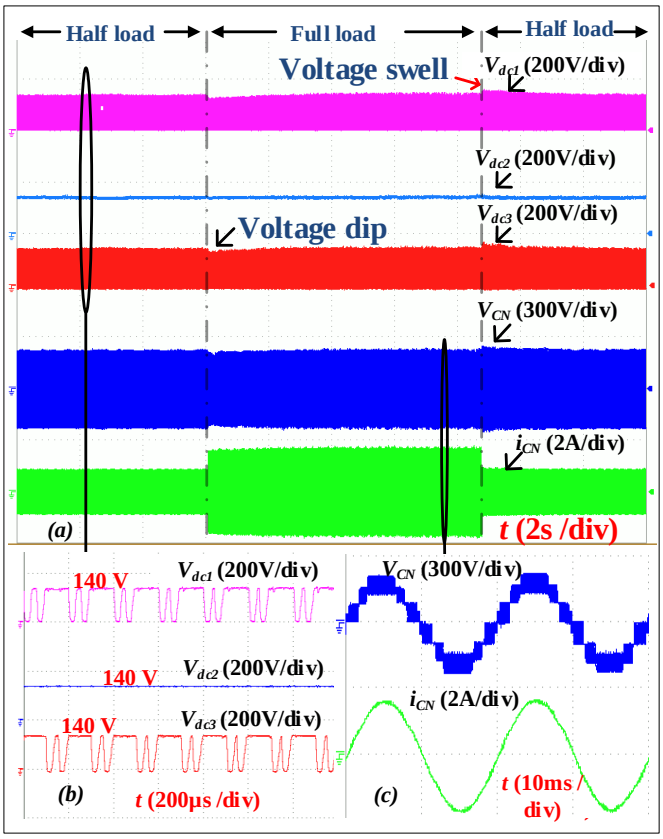

Fig. 3.13: Experimental results (a) DC-link voltage waveforms of qZS-FCMI and the load voltage and current in phase C (b) Zoom-in view of the DC-link voltages (C) Zoom-in view of the load voltage and current in phase C.

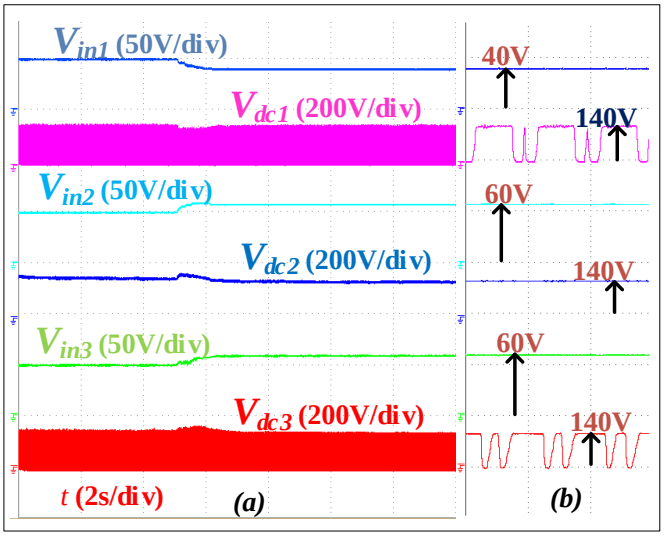

Fig. 3.14: Experimental results (a) DC-link voltages and input voltage waveforms of FCMI during source disturbance (b) Zoom-in view of the DC-link voltages of the FCMI.

To evaluate the dynamic performance of the MPPT controller of the qZS converters, programmable DC sources are used to emulate the P_{PV} vs V_{PV} characteristics of the PV panels [79-80]. The Programmable DC sources are operated in the constant voltage mode with a variable current limit. Fig.3.15 and Fig.3.16 show the experimental validation of MPPT

control for the top and middle PV sources. The top traces in Fig.3.15 and Fig.3.16 show the power, while the middle and the bottom traces respectively show the voltage and the current of the PV source.

To verify the dynamics of MPPT, the source current limit is first decreased and is then restored to its pre-disturbance value to emulate varying irradiation as shown in Fig.3.15 and Fig.3.16. When the change in irradiation is detected by the respective MPPT controllers, they immediately control the shoot-through duty ratio, thereby extracting the maximum power from the PV sources. Fig. 3.15 and Fig. 3.16 clearly demonstrate the tracking capability of the MPPT controllers corresponding to the top and the middle PV sources. The MPPT algorithms for both of the sources are run at a sampling frequency of 1 kHz. Since in the day-to-day experience, the change in irradiation is a slow phenomenon, it is evident that the dynamic response of the MPPT controller is satisfactory for the bandwidth corresponding to the chosen sampling frequency.

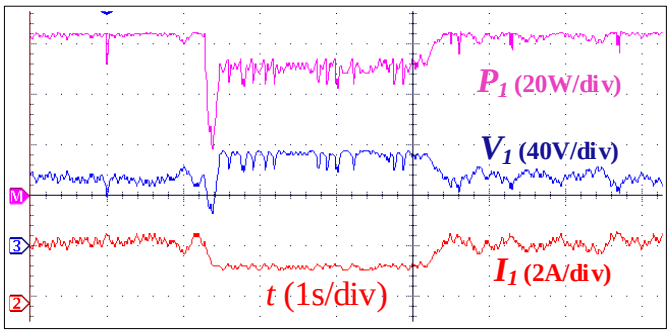

Fig.3.15: Experimental results of MPPT control of PV-1

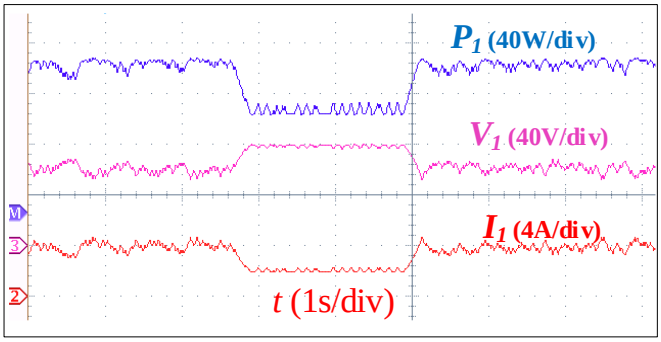

Fig.3.16: Experimental results of MPPT control of PV-2.

Fig. 3.17 shows the real-time simulation results pertaining to the synchronization of the proposed converter with the grid. These simulations are carried out using the OPAL-RT simulator (OP4500) [75]. OP4500 is equipped with a high-end Intel multicore processor, Xilinx kintex 7 FPGA with analog and digital channels. Thus, the RT-Lab environment

enables parallel processing and provides real-time simulation results, which are often considered equivalent to the experimental results obtained with a hardware prototype [76]. From Fig. 3.17, it is evident that, when the insolation level is suddenly decreased and then increased (from 1000W/m2 to 700W/m2 and vice versa), the PV current also changes correspondingly (from 3.5A to 2.1A, as shown in the top trace). It may be observed that the DC-link voltage is regulated at 770 V (middle trace) despite a change in insolation as explained in the previous section (Fig. 3.8). Also, the 3-phase currents injected into the grid undergo a corresponding variation (bottom trace) depending on the maximum power extracted from the PV sources using the MPPT algorithm explained earlier. Figure 3.17(b) shows the grid voltage (V_{ga}) and grid current (i_{ga}) of phase-A. The effectiveness of the proposed control method is evident as the converter injects active power into the grid at UPF. Fig. 3.18 demonstrates the capability of the proposed power converter to inject power into the grid in the grid-tied mode of operation.

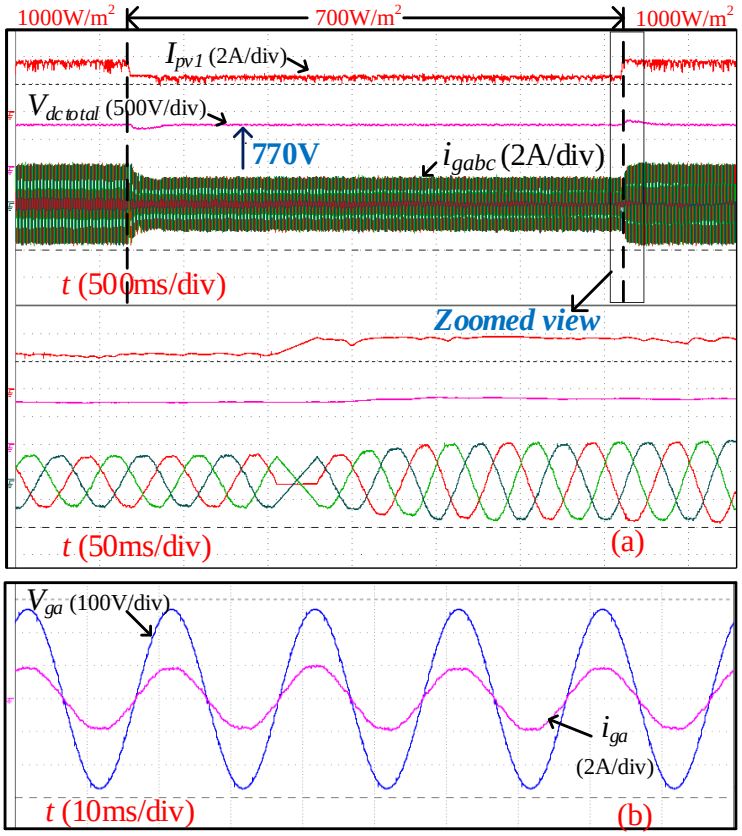

Fig. 3.17: Experimental results (a) PV current (I_{pv1}), total dc-link voltage ($V_{dctotal}$), grid currents (I_{gabc}) (b) grid voltage and grid current.

The qZS-FLI injects a current (per phase) of 1.34 A (RMS) at UPF while the grid voltage (per phase) is maintained at 115V (RMS). The inverter line-to-line voltage (V_{AB}) is also shown in Fig. 3.18 to validate the operation of the proposed qZS-FLI during the grid connection mode.

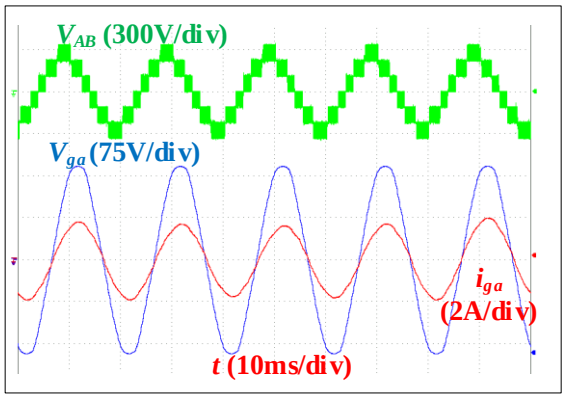

Fig. 3.18: Experimental result of inverter line voltage (V_{AB}) and grid voltage (V_{ga}) and grid current (i_{ga}) waveforms.

To summarize, the experimental results serve as the proof-of-concept for the proposed power converter and its control scheme.

3.6 Comparison with the proposed QZS FCMI

To show the advantages of the proposed topology, comparative analyses have been carried out, which are summarized in Table 3.3. As there are no impedance-source-based four-level topologies available in the literature, all the recent three-level topologies along with a seven-level topology are considered for comparison. Table 3.3 presents the component count of passive and active elements and compares the boost factor, voltage stress, gain, and inductor current ripple for these converters. The proposed converter produces a higher number of voltage levels when compared to all the topologies except qZS-CHB [51]. Except for the topologies described in [45] and [82], the proposed FLI uses an equal or lesser number of power diodes. As the number of voltage levels (N_L) is not identical across the compared topologies, the number of switches (N_{sw}) and the Total Standing Voltage (TSV) (the sum of blocking voltages of all the switches and diodes w.r.t the peak voltage value) is calculated [84]. The ratio (N_{sw}/N_L) is a figure of merit, which quantifies the switching resources required per voltage level. In this aspect, the proposed topology works out to be better than the one described in [51] and almost equivalent to the topologies described in [81-83]. Similarly, the ratio (TSV/N_L) is another holistic figure of merit, which quantifies the specific blocking voltage of any given topology.

The proposed topology registers a lower (TSV/N_L) ratio compared to the other MLI topologies. This signifies that even though the switch count is higher in the proposed converter, the blocking voltages are lower when compared to other MLI configurations. As seen in Table 3.3, the gain and the boost factor of the proposed four-level inverter are

Table 3.3: Comparison of different impedance topologies with the proposed topology

	ZS-NPC[41]	qZS-CHB [51]	LC-NPC[81]	qZS-3LT[45]	qSB-3LT[82]	AI-3LT[83]	Proposed
Levels(N_L)	Three	Seven	Three	Three	Three	Three	Four
Sources	2	9	2	1	1	1	3
Capacitors	4	18	2	4	2	2	7
Inductors	4	18	2	4	1	1	6
N_{SW}/N_L	4	5.1	4.66	4	4.66	4.33	4.75
Diodes	8	9	8	2	4	2	4
TSV/N_L	3.32	2.16	4	3.33	3	2.5	1.91
Boost	$\frac{1}{(1-2D)}$	$\frac{1}{(1-2D)}$	$\frac{1}{(1-2D)}$	$\frac{1}{(1-2D)}$	$\frac{1}{(1-2D)}$	$\frac{2}{(1-2D)}$	$\frac{1}{(1-3D)}$
Gain	$\frac{M}{(2M-1)}$	$\frac{M}{(2M-1)}$	$\frac{M}{(2M-1)}$	$\frac{M}{(2M-1)}$	$\frac{M}{(2M-1)}$	$\frac{2M}{(2M-1)}$	$\frac{M}{(3M-2)}$
Switch voltage stress	$\frac{1}{(1-2D)2}$	$\frac{1}{(1-2D)3}$	$\frac{1}{(1-2D)2}$	$\frac{1}{(1-2D)2}, \frac{1}{(1-2D)}$	$\frac{1}{(1-2D)2}$	$\frac{1}{(1-2D)}$	$\frac{1}{(1-3D)3}$
Capacitor voltage stress	$\frac{(1-D)}{(1-2D)2}$	$\frac{(1-D)}{(1-2D)3}$ for C_1 $\frac{(D)}{(1-2D)3}$ for C_2	$\frac{1}{(1-2D)2}$	$\frac{(1-D)}{(1-2D)2}$ for C_2,C_3 $\frac{(D)}{(1-2D)2}$ for C_1,C_4	$\frac{1}{(1-2D)2}$	$\frac{1}{(1-2D)}$	$\frac{(1-3D/2)}{(1-3D)3}$ for C_1 $\frac{(3D/2)}{(1-3D)3}$ for C_2
Diode voltage stress	$\frac{1}{(1-2D)2}$	$\frac{1}{(1-2D)3}$	$\frac{1}{(1-2D)2}$	$\frac{1}{(1-2D)2}$	$\frac{1}{(1-2D)2}$	$\frac{1}{(1-2D)}$	$\frac{1}{(1-3D)3}$
Inductor current ripple	$\frac{(1-D)DT}{(1-2D)2L}$	$\frac{(1-D)DT}{(1-2D)3L}$	$\frac{(1-D)DT}{(1-2D)L}$	$\frac{(1-D)DT}{(1-2D)2L}$	$\frac{DT}{2L}$	$\frac{2D(1-D)T}{(1-2D)L}$	$\frac{(1-D)DT}{(1-2D)3L}$

dependent on the shoot-through duty ratio and vary exponentially with D. When D > 0.25, the proposed MLI displays a higher boosting factor and gain when compared to all other topologies. For D < 0.25 the proposed MLI shows a better-boosting factor and gain than all other topologies except [83]. For all of the seven power converters, voltage stresses across the devices and the passive elements are calculated based on the *per-unit* basis, with V_{dc} (the total DC-input voltage) as the base value. All the topologies are evaluated for a total input voltage of 300 V DC from the PV source so that the desired phase voltage of 230 V (RMS) is output by them. The proposed topology results in lesser voltage stress across the switches, capacitor, and diodes except [51], as all the three-level topologies require a higher boost factor to derive the required output voltage of 230V/Ph (RMS) for the input of 300V DC. Assuming identical values for switching frequency, duty ratio, and inductors, the value of the ripple current in the inductors is minimum for the proposed topology when compared to the topologies reported in [41][81][45][83], which lowers the size of the inductor. From the above comparison, it is evident that, despite the higher number of components, the proposed four-level inverter results in lower voltage stress on the switches, diodes, and capacitors, which leads to the lower ratings of the devices compared to the three-level topologies. The proposed FCMI shows a better boost factor when compared to all other topologies for higher duty ratios. Also, the inductors have a lower current ripple, which leads to a lower value of inductors.

3.7 Power loss analysis for the proposed QZS-FCMI

In this section, the power losses incurred in the power semiconductor devices and the passive components are assessed for the proposed configuration. In order to evaluate these power losses, the proposed configuration is simulated with the thermal models of the semiconductor devices for a power output of 1kW in the PLECS software. A reference power model of IGBT along with body diode (*IKW30N60T*) is considered for simulation. The following power loss components are considered while analyzing the converter loss: (i) switching and conduction losses in the IGBTs (denoted by P_{SW} and P_{CON}), (ii) diode switching and conduction losses (denoted by P_{SD} and P_{CD}) (iii) inductor conduction loss (P_{ind}) (iv) Capacitor ESR loss (P_{cap}). Apart from these losses, the conduction losses in the inductors and the ESR losses in the capacitors are calculated based on the equivalent parasitic resistance [77]. These losses have been evaluated at M = 0.77, D=0.2, V_{in1} = V_{in2}= V_{in3}=100 V, V_{dc1} =243V, fs =10 kHz, Po =1kW, PF = 1, Vo (ph-RMS) = 230V. The summary of the losses is presented in Fig.3.19.

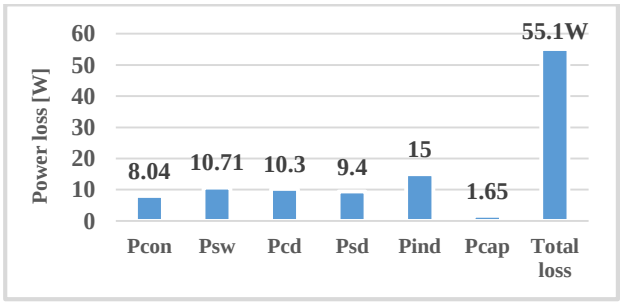

Fig .3.19: Loss distribution in the device for qZS-FCMI.

Such data are generated for various values of the output power ranging from 0.5-2.5 kW for the input voltages of 100 V and 120 V. The data so generated is plotted in Fig. 3.20. These data suggest that the efficiency curve is practically flat with average efficiencies of 93% and 94% respectively for the aforementioned values of the input voltages.

These data further suggest that the efficiency of the proposed power converter increases as the input voltages increase. This is because, an increased input voltage results in the decrease of the boosting factors, leading to the reduction of the power loss. It may be observed from Fig.3.20 that at a dc input voltage of 120V, we require a shoot-through duty ratio of 0.17 to achieve the desired output voltage of (230V). This requires a lower voltage boosting, which helps in the reduction of the inductor losses thereby increasing the efficiency when compared to the lower input voltage of 100V.

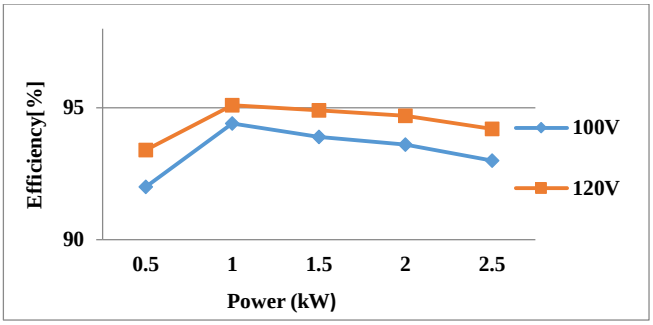

Fig. 3.20: Calculated efficiency of the proposed qZSI-FLI for two different input voltages.

To validate the hardware efficiency of the prototype a precision digital power meter (Yokogawa WT332E) is used to measure the input power of the proposed qZS-FLI and a power analyzer (UNI-T UT283A) is used to measure the output power. The experiment is conducted for a step change of 100W ranging from 400W to 870W. Fig. 3.21 shows the experimental efficiency curve of the qZS-FLI. From the plot, it may be noted that the average experimental efficiency of the prototype hovers around 92%. It may be observed that the experimental efficiency is in close approximation to the simulated efficiency (shown in Fig. 3.20), which is around 93% to 94%.

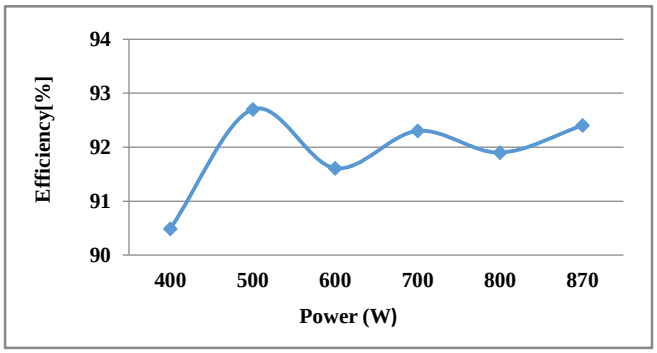

Fig. 3.21: Experimental efficiency of the proposed qZSI-FLI.

3.8 Summary

This chapter reports the research work investigated in the *single-stage* solar PV power conversion systems with 3-phase output for stand-alone and grid-connected applications. Single-stage power conversion is obtained by the amalgamation of two mutually interdependent sub-systems, namely, the front-end qZS networks and the back-end FCMI. It is shown that the LSPWM technique increases the boost-factor by 50% when compared to the power circuit configurations reported in the earlier literature. Also, this power circuit configuration is structurally simpler and requires fewer components compared to the NPC or the CHB-based systems. The steady-state and the dynamic performance of the proposed four-level inverter in the stand-alone mode have been verified with experimental validation. The

experimental results indicate that the DC-links of the proposed power converter are regulated by the adjustment of the shoot-through duty factor. This feature makes the proposed four-level inverter suitable for stand-alone applications. Further, real-time simulations and experimentation validates the performance of the proposed four-level inverter in grid-connected mode of operation. It is shown that it is possible to implement the MPPT by varying the shoot-through duty factor, while the output of the FCMI is controlled by varying the modulation index. It is also shown that the proposed four-level inverter, injects active power into the grid with the help of a PLL. The power loss analysis, carried out with simulation studies, reveals that the proposed converter is capable of achieving an efficiency of 94%.

Chapter 4

An Asymmetrical Dual Quasi-Z-Source Based 7-Level Inverter for PV Applications

Chapter 4

An Asymmetrical Dual Quasi-Z-Source Based 7-Level Inverter for PV Applications

4.1 Introduction

In the previous chapter, a single-stage four-level qZS-based cascaded MLI has been investigated to reduce the complexity associated with NPC and CHB topologies. The proposed power converter achieves a higher boost factor, and lesser voltage stress across the switches, diodes, and capacitors, which leads to lower ratings of the devices compared to the three-level NPC and CHB topologies. Further, the closed-loop control schemes in stand-alone mode and grid-connected mode of operation are investigated and validated experimentally.

However, the control complexity associated with the MPPT tracking with multiple PV sources, DC-link voltage regulation, and the requirement of a large number of switching devices to synthesize a 4-level output voltage waveform are the major demerits of the topology. Further, as the proposed power converter in chapter 1 avoids galvanic isolation between the PV panel and the grid there would be a flow of leakage current. This leakage current contains components corresponding to the switching frequency, which inject harmonics into the grid current. Some of the well-known ill-effects of the leakage current are: increased power loss, poor electromagnetic compatibility, and decreased operational safety (possible electric shock).

These shortcomings are the impetus for the development of the single-stage dual quasi-z-source 7-level inverter (DqZS-7LI) topology proposed in this chapter. This power converter configuration, which utilizes a lower number of devices, is obtained by combining two antiparallel qZS networks with a cascaded 7-level H-bridge circuit. This chapter also proposes a modified level-shifted PWM scheme, which achieves the twin objectives of input voltage boosting and generation of 7 levels in the output voltage. Along with the proposed PWM technique, an LCL filter is used to reduce the high-frequency voltage transitions across the parasitic capacitance. This restricts the leakage current within the safety standards stipulated by the VDE0126-1-1[10]. Steady-state and dynamic performances of the power converter are experimentally verified both in stand-alone and grid-connected modes with the aid of a hardware prototype.

4.2 The proposed DQZS-7LI

4.2.1 Proposed Power converter

The proposed PV fed dual- quasi-z-source 7-level inverter (DqZS-7LI) topology is shown in Fig. 4.1. This configuration employs two PV sources, PV-1, and PV-2, with an unequal voltage ratio of 1:2 respectively. Also, this power converter consists of two quasi-z-source networks and a cascaded 7-level H-bridge inverter. The outputs of the PV sources are input to the quasi-z-source networks as shown in Fig. 4.1. The qZS networks boost the input PV voltage to suit the requirements of the 7-level inverter. The top qZS network (qZS-1) employs switches S_1 and S_2 to obtain the required shoot-through. Similarly, switches S_3 and S_4 are used to obtain the shoot-through for the bottom qZS network (qZS-2). As shown in Fig. 4.1, the midpoints of switches S_1, S_2, and S_3, S_4 respectively serve as the positive and negative DC rails for the output H-bridge inverter, which is constituted by switches S_5-S_8. The midpoints A and B of the H-bridge are interfaced with the grid with a symmetrical LCL filter. The detailed description of the parameters C_p, C_n, R_D, and R_G are explained in section 4.5.

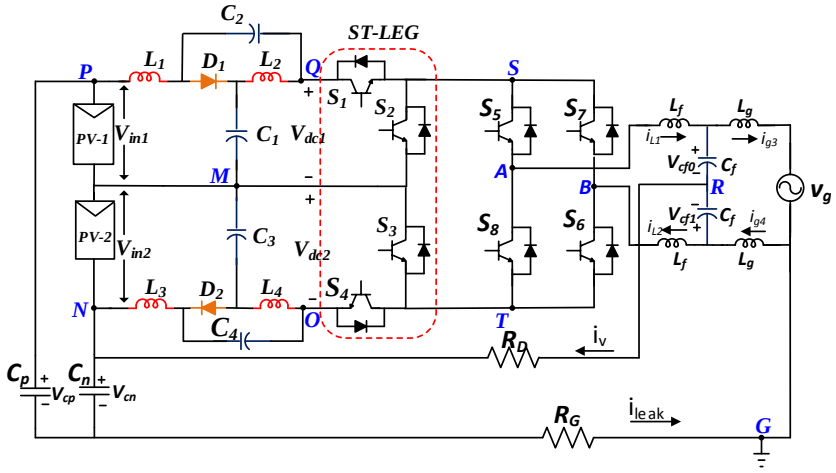

Fig. 4.1: Proposed DqZS-7LI.

4.2.2 Output voltage levels and corresponding switching states of the power converter

The proposed configuration is capable of generating seven levels in the output phase voltage waveform V_{AB} (see Column-2, Table 4.1). In Table 4.1, the 'on' and the 'off' states of the semiconductor devices are indicated as logic '1' and '0' respectively. These switching states are classified into two types namely, the non-shoot-through states (NST), and the shoot-through states (ST). The NST states are further subdivided into six active states and two zero states. These active -states generate six distinct voltage levels $\pm$V, $\pm$2V, and $\pm$3V in the output voltage waveform (considering Vin = V).

TABLE 4.1 SWITCHING COMBINATIONS TO ACHIEVE 7-LEVEL OPERATION

State type	Voltage (V_{AB}) for *Vin1 = V & Vin2 =2V*	Switching states (1-ON, 0-OFF)							
		S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
NST	$3V$	1	0	0	1	1	1	0	0
NST	$2V$	0	1	0	1	1	1	0	0
NST	V	1	0	1	0	1	1	0	0
NST	0	0	0	0	0	1	0	1	0
NST	0	0	0	0	0	0	1	0	1
NST	$-V$	1	0	1	0	0	0	1	1
NST	$-2V$	0	1	0	1	0	0	1	1
NST	$-3V$	1	0	0	1	0	0	1	1
ST	0	1	1	0	0	1	0	1	0
ST	0	0	0	1	1	1	0	1	0
ST	0	1	1	1	1	1	0	1	0

Fig. 4.2 presents the operating modes of the proposed converter during the NST and the ST states. While Fig. 4.2(a) - Fig. 4.2(e) represent the NST modes of the power converter, Fig. 4.2(f) - Fig. 4.2(h) represents the ST mode. From Fig. 4.2(a), it may be noticed that by turning on S_1 and S_4, the combined DC-link voltage (V_{dc1}+V_{dc2}, Fig. 4.1) is equal to +3V, which is applied to the H- bridge inverter terminals. Fig. 4.2(b) shows the operating mode to synthesize the voltage level of +2V, wherein the switches S_2 and S_4 are turned on. The operating mode to generate the level of +V is demonstrated in Fig. 4.2(c), wherein the switches S_1 and S_3 are turned on (Table 4.1 and Fig. 4.2(c)). It may be noted that the switches S_5 and S_8 are turned on in all these three modes to connect the rails of the H-bridge to the outputs of the qZS networks. The method of synthesizing the three negative levels (-V, -2V, and -3V) can readily be deduced with the aid of Table 4.1. In the zero states, the H-bridge is completely isolated from the qZS networks by turning off all four switches S_1 - S_4 as shown in Fig. 4.2(d) and Fig. 4.2(e). During these two states, there is no power transfer between the PV source and the load. Thus, it is evident that the shoot-through (ST) mode of operation can be inserted in the zero-state.

In the proposed topology, the shoot-through mode of operation can be implemented in three different ways. These are: (i) qZS-1 shoot-through (Fig. 4.2(f)) (ii) qZS-2 shoot-through (Fig. 4.2(g)) (iii) both qZS-1 and qZS-2 shoot-through (Fig. 4.2(h)). In (i) and (ii) shoot-through modes of operation the respective DC-link voltages (V_{dc1}, V_{dc2}) of the qZS networks drop to zero, and in (iii) the total DC-link voltage (V_{dc1}+V_{dc2}) of the power converter drop to zero.

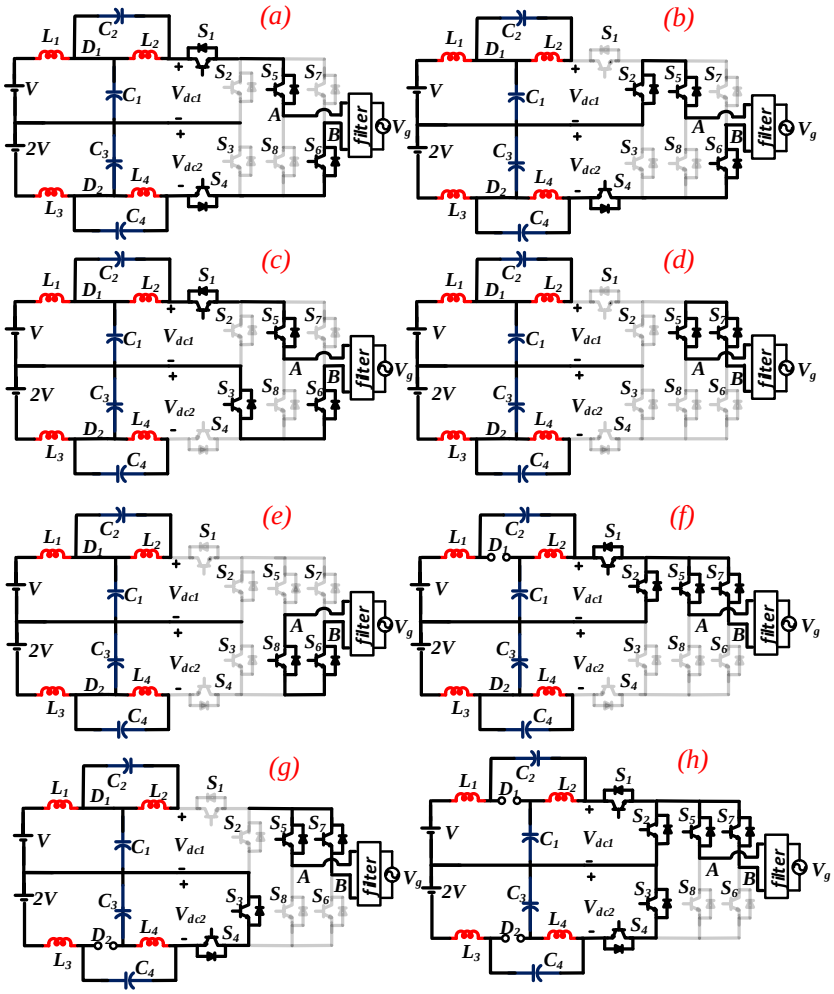

Fig. 4.2: Circuit diagrams for NST and ST states of the power converter.

In this configuration, the zero-state (which includes the ST state) is inserted in all 7 levels of operation to obtain the required boosting of the DC-link voltage. Consequently, the output voltage displays pulsation (from zero to the synthesized voltage level) in any given time period.

4.3 The control scheme for the proposed dual QZS 7-level inverter

4.3.1 Implementation of the MLS-PWM scheme

Generally, two control techniques are commonly employed to obtain a multilevel output waveform: (i) level-shifted PWM (LSPWM) and, (ii) phase-shifted PWM. In this work, a modified level-shifted PWM (MLSPWM) is implemented to synthesize the desired 7-level phase voltage waveform with input voltage boosting. To synthesize the required 7-level output voltage waveform despite the asymmetry in the input voltages, the sinusoidal modulating signal ($v_m = m\,sin(\omega t)$) should be modified to v_m^* as shown in Fig. 4.3. The PWM scheme

is implemented by comparing a modified reference signal (v_m^*) with a single carrier signal. Initially, the modulated sine wave (v_m) is divided into three regions of operation Z_{n1}, Z_{n2}, and Z_{n3} (shown in Fig. 4.3) based on the value of modulation index (m) and 'R_1', 'R_2', where 'R_1' and 'R_2' are defined as the multiplication factors which are taken into consideration for asymmetry of the input voltages. The multiplication factors 'R_1' and 'R_2' are expressed as:

$$R_1 = {V_{in1}}/{V_{in1} + V_{in2}}\,,\; R_2 = {V_{in2}}/{V_{in1} + V_{in2}} \tag{4.1}$$

In region-1, wherein $0 < v_m < (R_1.m)$, the modulated sine wave (v_m) is not modified. In region-2 ($R_1.m < v_m < R_2.m$), the sine wave (v_m) is scaled down to $v_m/2$ and in region-3 ($R_2.m < v_m < m$), it is scaled down to $v_m/3$. The summation of the references in regions 1, 2 & 3 synthesizes the modified reference wave (v_m^*) as shown in Fig. 4.3. The modified reference wave (v_m^*), shown in Fig. 4.3, is plotted considering the voltage ratio of the input PV sources (1:2). Hence R_1 and R_2 are selected as 1/3 and 2/3.

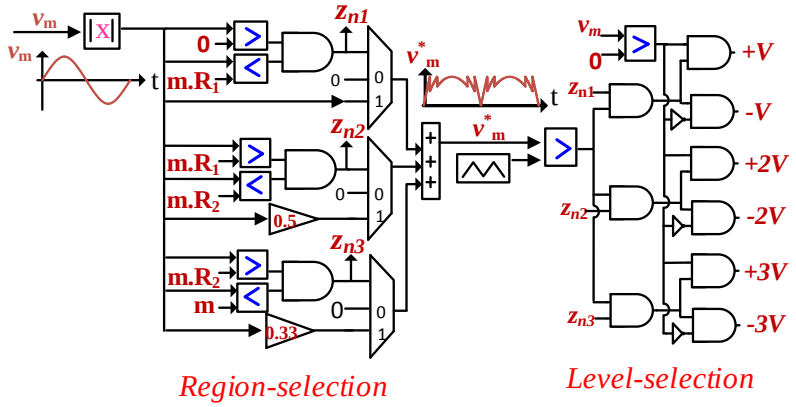

Fig. 4.3: Implementation of modified reference wave (v_m^*) for DqZS-7LI.

The modified reference wave (v_m^*) is compared with the carrier wave (C) in the three regions mentioned above, for both positive and negative half-cycles. The voltage level in the output is determined by the output of the comparator and the region of operation (Z_{n1}, Z_{n2}, and Z_{n3}) as shown in Fig. 4.3. Table 4.2 shows the generation of gating signals for the power devices to synthesize various voltage levels. Fig. 4.4 presents the PWM pulses (S_1'-S_8') required to synthesize the 7-level output voltage waveform. Further, to implement voltage boosting in qZS networks, two shoot-through pulses S_{h1} and S_{h2} are generated by comparing the DC references v_{sh1}, v_{sh2} with the carrier signal (C). To facilitate the boosting operation with qZS-1 and qZS-2, logical 'OR' operations are respectively performed between the shoot-through pulse train (S_{h1}) and the signals (S_1'-S_2'), the shoot-through pulse train (S_{h2}), and the signals (S_3'-S_4'). The signals obtained after these logical 'OR' operations are employed to gate the

switches S_1-S_4. It may be noted that the gating signals (S_5'-S_8') are directly used to gate the switches S_5-S_8 to generate polarity in the output voltage.

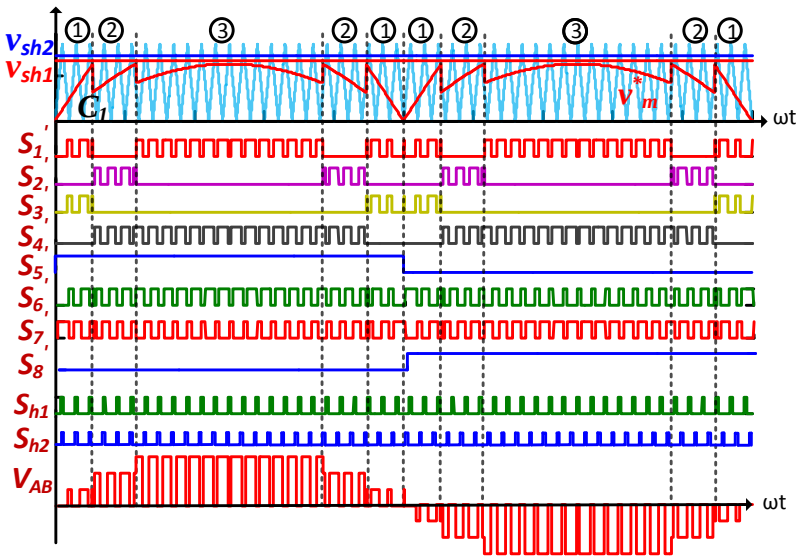

Fig. 4.4: Implementation of modulation technique.

4.3.2 Boost factor of the proposed DqZS-5LI

Fig. 4.5 shows the equivalent circuit for the proposed DqZS-7LI during shoot-through (ST) and non-shoot-through (NST) states of operation.

During the ST, the inductor voltages (V_{L1}, V_{L2}) and DC-link voltages are presented in equations (4.2), (4.3) & (4.4):

$$V_{L1} = V_{in1} + V_{c2}, V_{L2} = V_{c1} \quad (4.2)$$

$$V_{L3} = V_{in2} + V_{c4}, V_{L4} = V_{c3} \quad (4.3)$$

$$V_{dc1} = 0, V_{dc2} = 0 \quad (4.4)$$

Similarly, in the NST state, these are given by:

$$V_{L1} = V_{in1} - V_{c1}, V_{L2} = -V_{c2} \quad (4.5)$$

$$V_{L3} = V_{in2} - V_{c3}, V_{L4} = -V_{c4} \quad (4.6)$$

$$V_{dc1} = V_{c1} + V_{c2}, V_{dc2} = V_{c3} + V_{c4} \quad (4.7)$$

Applying the volt-sec balance to the inductors (equations 4.2, 4.5, 4.3 & 4.6) over one switching time-period (T_s) the following equations are derived:

$$V_{C1} = \frac{1-D_1}{1-2D_1} V_{in1}, V_{C2} = \frac{D_2}{1-2D_2} V_{in1} \quad (4.8)$$

$$V_{C3} = \frac{1-D_1}{1-2D_1} V_{in2}, V_{C4} = \frac{D_2}{1-2D_2} V_{in2} \quad (4.9)$$

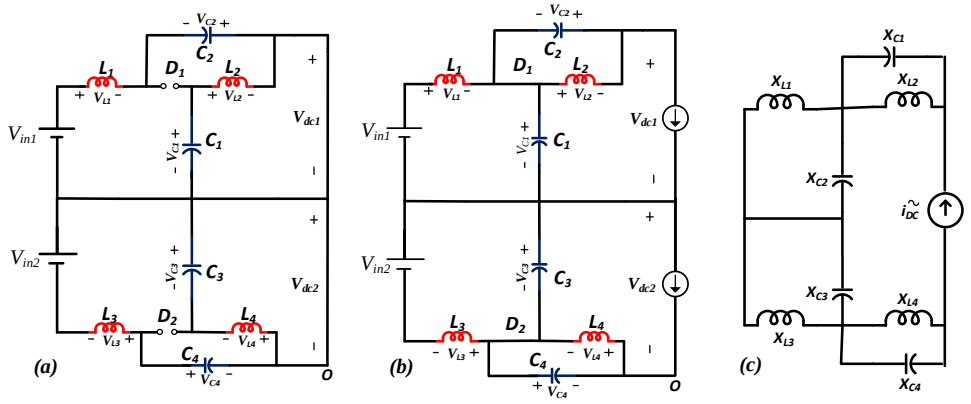

Fig. 4.5: Equivalent circuit of DqZS-7LI during (a) shoot-through state (ST) (b) non-shoot-through (NST) state. (c) Simplified equivalent circuit.

where 'D_1 & D_2' are the shoot-through (ST) duty ratios, which are expressed as T_{sh}/T_s; where T_{sh} is the ST time.

From equations (4.7), (4.8) & (4.9), the boosted DC-link voltages are expressed as:

$$V_{dc1} = \frac{1}{1-2D_1}\ V_{in1},\ V_{dc2} = \frac{1}{1-2D_2}\ V_{in2} \tag{4.10}$$

4.3.3 Design of qZS network of proposed DqZS-7LI

In the proposed power converter the design of the quasi-z-source inductors and capacitors are derived based on the allowable low frequency current ripple of the inductor and DC-link voltage ripple of the inverter. This low-frequency ripple is caused by the second harmonic component of the output power. Further, to simplify the design equations only the low-frequency ripple component is considered neglecting the switching frequency ripple of the inductor current. The simplified equivalent circuit of the power converter is shown in Fig. 4.5(c). The current source $i_{DC}^{\sim}$ shown in Fig. 4.5(c), represents the fundamental component of the DC-link current and $X_{l(1-4)}$ to $X_{c(1-4)}$ represent the reactive components of the quasi-z-source network.

From the equivalent circuit, the low-frequency component of i_{L1} is derived as:

$$i_{L1}^{\sim} = \frac{4\sqrt{2}}{3\pi}.\frac{k(P_{OUT})}{V_{OUT}}.\sin(\frac{4.\pi.t}{T} - \frac{\pi}{2}).\frac{x_{C2}}{x_{L1}+x_{C2}} \tag{4.11}$$

Where the variable 'k' represents the percentage of the power delivered by the PV-1. From equation (4.11) and the power balance of the power converter the low-frequency inductor ripple 'x' is expressed as

$$x = \frac{4\sqrt{2}}{3\pi}\frac{V_{in1}}{V_{OUT}}\frac{T^2}{(16\pi^2 L_1 C_2 - T^2)} \tag{4.12}$$

Similarly, the low-frequency voltage across the capacitor 'C_1' is given by

$$v_{C1}^{\sim} = \frac{4\sqrt{2}}{3\pi}\frac{k(P_{OUT})}{V_{OUT}}\sin(\frac{4.\pi.t}{T} - \frac{\pi}{2}).\frac{x_{L2}.x_{C1}}{x_{L2}+x_{C1}} \quad (4.13)$$

From equation (4.13) the low-frequency voltage ripple 'y' across the capacitor 'C_1' is expressed as:

$$y = \frac{4\sqrt{2}}{3\pi}\frac{k(P_{OUT}).(D)}{V_{OUT}.(1-2D)V_{in1}}\frac{4\pi TL_2}{(16\pi^2 L_2C_1 - T^2)} \quad (4.14)$$

Solving the equations (4.12) and (4.14) and considering L_1=L_2 and C_1=C_2 the inductor and capacitor values of qZS-1 are obtained. A similar analysis is applied to the inductor and capacitor of qZS-2 to derive L_3, L_4, and C_3, C_4 parameters.

4.4 Stand-alone and grid-connected control strategies of DQZS-7LI

4.4.1 Stand-alone mode

It is well known that the output voltage of the quasi-z-source MLI is determined by the gain, which is the product of the boost factor 'B' and modulation index 'm' and obtained by the qZS network. In the stand-alone mode of operation, the modulation index (m) is held constant while controlling the output voltage. In such a situation, the gain of the power converter is solely determined by the boosting factor (B), which needs to be controlled to regulate the output voltage against the load and source disturbances.

In the proposed topology, a pulsating DC-link is produced across the qZS-1 and qZS-2 networks, when shoot-through (ST) is inserted in the shoot-through leg constituted by S_1, S_2, S_3, and S_4 (Fig. 4.1). An indirect measurement of the DC-link voltage is required as the pulsating DC voltage cannot be measured directly or it can be used as a feedback signal. In the present work, the DC-link voltage V_{dc1} and V_{dc2} of the 7-level inverter are estimated using shoot-through duty ratios (D_1, D_2) and the capacitor voltages (V_{c1}, V_{c3}) (Eqn. 4.8&4.9). Fig. 4.6 presents the closed-loop control scheme to control the DC-link voltages (V_{dc1} and V_{dc2}) of the proposed converter.

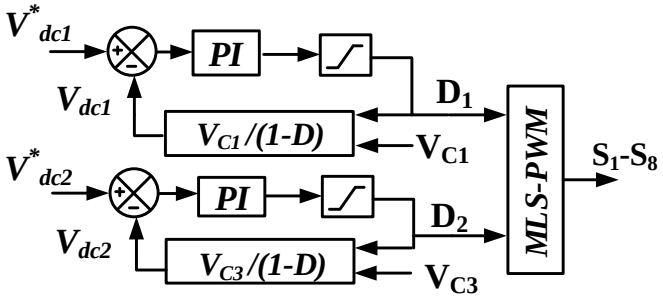

Fig. 4.6: Closed-loop DC-link voltage control for the proposed DqZS-7LI.

The estimated DC-link voltages V_{dc1} and V_{dc2} are then compared with the reference voltages V^*_{dc1}, and V^*_{dc2} respectively, and the error generated is compensated by the PI controllers. The outputs of the PI controllers determine the required shoot-through duty ratios (D_1, D_2). These duty ratios are translated into the reference signals *'V_{sh1}* and *V_{sh2}'* (Fig. 4.6), which are compared with the carrier signal to implement the shoot-through mode as discussed in Section 4.3. Thus, the output voltage of the DqZS-7LI is regulated solely with the closed-loop feedback control of DC-link voltages (V_{dc1}, V_{dc2}).

4.4.2 The Grid-connected mode of operation

The grid-connected mode of operation requires the fulfilment of three objectives: (i) DC-link voltage regulation (ii) Injection of power into the grid at unity power factor (iii) Independent MPPT control of the two quasi-z-source networks. The two degrees of freedom offered by the qZS converter namely, the shoot-through duty ratio 'D' and the modulation index 'm' and are utilized to control these three objectives. Fig. 4.7 shows the control scheme for the closed-loop control of the proposed DqZS-7LI in the grid connection mode.

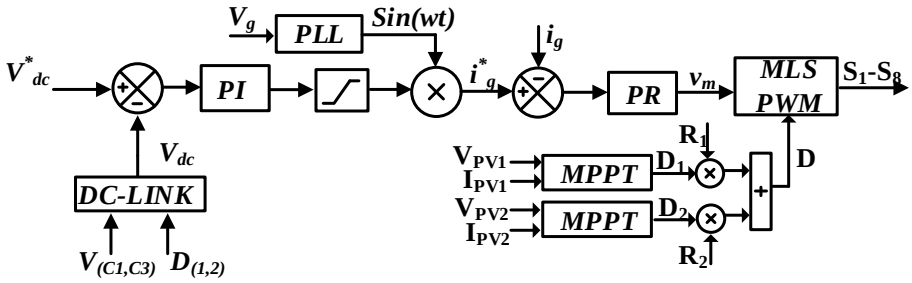

Fig.4.7: The grid control scheme for DqZS-7LI.

Perturb & Observe MPPT algorithm is employed to extract the maximum power from the PV panels. The currents (I_{PV1}, I_{PV2}) and voltages (V_{PV1}, V_{PV2}) of the PV panels are sensed and fed to the respective MPPT controllers. These controllers generate the required duty ratios (D_1 and D_2), which are multiplied by R_1 and R_2 (equation 4.1) to generate the shoot-through duty ratio (D)[87]. Further, the duty ratio is fed to the MLS-PWM to implement the ST mode with the help of the shoot-through leg.

As stated in the previous section, the total DC-link voltage is assessed by sensing the voltages across capacitors and the duty ratios of the qZS-1 and qZS-2 networks. The error between the reference DC-link voltage (V^*_{dc}) and the estimated value (V_{dc1}+V_{dc2}) is compensated by the PI controller that is present in the outer voltage loop. The control signal generated by the PI controller is multiplied with a unit-sine signal ($\sin \omega t$) to generate the

reference value for the inner current loop (i^*_g) which is synchronized to the grid using a PLL. The reference grid current (i^*_g) is then compared to the actual grid current (i_g) and the resultant error is compensated by a PR controller. The output of the PR controller then generates the required modulation signal v_m, which is employed by the MLS-PWM control scheme to control the magnitude of the active power injected into the grid. [86].

4.5 Reduction of leakage current

In transformerless PV systems, due to the absence of galvanic isolation, the leakage current flows through the path that is formed by the frame of the PV panel, the parasitic capacitance, and the common ground. The VDE0126-1-1 standard [10] specifies that the maximum leakage current is limited to 300mA. As mentioned earlier, quasi-z-source multilevel inverters boost the input voltage with the insertion of the shoot-through mode in the zero states of the switching period. Although PV sources are isolated from the grid during the zero-states (Fig. 4.2 (d) and 4.2(e)), the addition of the shoot-through state introduces high-frequency transitions in the voltage impressed across the parasitic capacitor. These high-frequency transitions generate the leakage current, which flows from the PV source to the ground. Thus, it stands to reason that maintenance of a constant voltage across the parasitic capacitance eliminates the leakage current. Though it is generally desirable to eliminate the leakage current, it is not possible in qZS-based multilevel inverters owing to the insertion of the shoot-through in the zero-states. In such a scenario, the leakage current is reduced by reducing the magnitude of high-frequency transitions in the voltage, which is impressed across the parasitic capacitor. It is well known that the magnitude of these high-frequency transitions is determined by the common-mode voltage (CMV), which is defined as follows:

$$V_{cm} = \frac{V_{AO}+V_{BO}}{2} \tag{4.15}$$

As shown in Fig. 4.1 the qZS-2 network is connected with a reversed orientation compared to the qZS-1 network (Fig. 4.1). This facilitates the inclusion of inductor L_3 and the capacitor C_4 between inverter negative terminal ‘O’ and negative terminal of PV panels ‘N’ throughout the shoot-through (ST) as well as the non-shoot-through (NST) states. Hence, the effective CMV (V_{mcm}) is represented as:

$$V_{mcm} = V_{cm} + V_{L3} - V_{C4} \tag{4.16}$$

Furthermore, an LCL filter is connected across the inverter output terminals (AB), as shown in Fig. 4.8(a), to achieve the dual objectives of (i) reducing higher-order current harmonic

components in the leakage current induced by the effective CMV (V_{mcm}) and (ii) filtering the output voltage of the inverter. To damp out the oscillations in the leakage current, a damping resistor (R_D) is connected between the midpoint of the filter capacitor and the negative terminal of the PV source (N) as shown in Fig. 4.8(a). In Fig. 4.8(a), C_p and C_n respectively represent the parasitic capacitance formed between the PV cells and their metallic frame, while R_G represents the ground resistance [85].

The mathematical model of the system shown in Fig. 4.8(a) may be resolved into the differential-mode and the common-mode models.

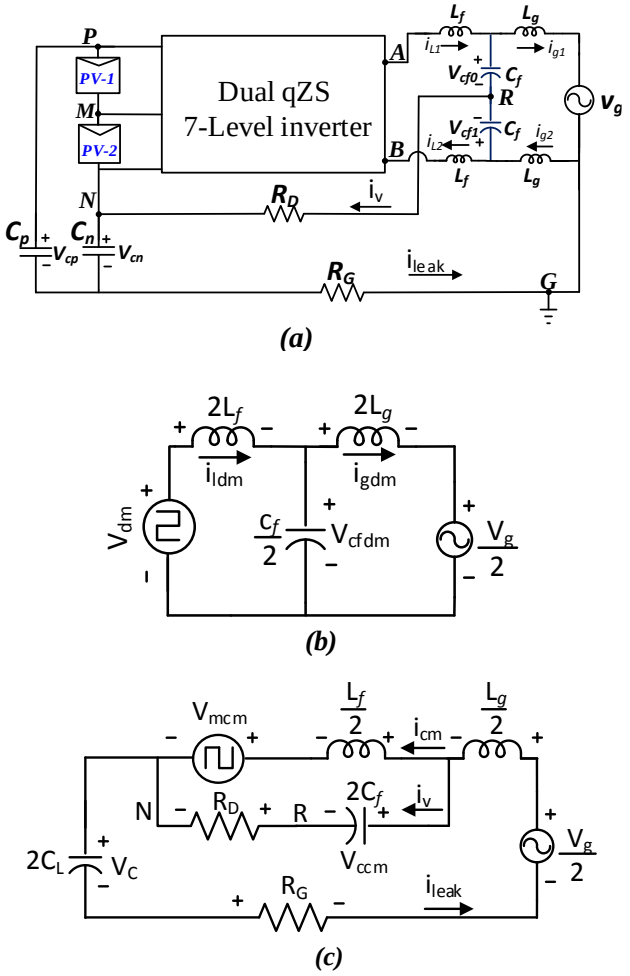

Fig. 4.8: (a) DqZS-7LI with leakage ground current path (b) equivalent circuit of the differential-mode model(c) equivalent circuit of the common-mode model.

The equations corresponding to the differential-mode model are given by:

$$2L_f \, \hat{i}_{ldm} = V_{dm} - V_{cfdm} \tag{4.17}$$

$$2L_g \, \hat{i}_{gdm} = V_{cfdm} - V_g \tag{4.18}$$

$$\frac{C_f}{2}\hat{V}_{cfdm} = i_{ldm} - i_{gdm} \tag{4.19}$$

where the symbols i_{ldm}, i_{gdm}, $V_{dm,}$ and V_{cfdm} respectively denote the differential-mode inverter current ((i_{l1}+i_{l2})/2), differential-mode grid current ((i_{g1}+i_{g2})/2), differential-mode inverter voltage (V_{AN}-V_{BN}) and the differential-mode filter voltage (V_{cf0} +V_{cf1}). A pictorial representation of equations (4.17-4.19) results in the differential-mode equivalent circuit presented in Fig. 4.8(b).

On the other hand, the equations corresponding to the common-mode model are given by:

$$\frac{L_f}{2}\hat{\imath}_{lcm} = \frac{V_g}{2} - i_{leak}R_G - V_c - V_{mcm} - \frac{L_g}{2}\hat{\imath}_{leak} \tag{4.20}$$

$$\frac{L_f}{2}\hat{\imath}_{lcm} = V_{mcm} - V_{cfcm} + i_v R_D \tag{4.21}$$

$$2C_L\,\hat{V}_c = i_{leak} \tag{4.22}$$

$$2C_f\,\hat{V}_{cfcm} = i_{leak} - i_{lcm} \tag{4.23}$$

where the symbols i_{lcm} and V_{cfcm} respectively denote the common-mode inverter current ((i_{l2}-i_{l1})) and the common-mode voltage of the filter ((V_{cf0} -V_{cf1})/2).

A pictorial representation of equations (4.20-4.23) results in the common-mode equivalent circuit presented in Fig. 4.8(c). In this analysis, it is assumed that both PV parasitic capacitors have the same value of capacitance (i.e. C_P=C_N=C_L).

From Fig. 4.8(c), it may be noted that the leakage current (i_{leak}) is split into two components i_{lcm} and i_v (the high-frequency current flowing through the midpoint of capacitors 'R' and the 'N' terminal, Fig. 4.8(a)). This mid-point connection creates an alternate path to the current produced by the high-frequency voltage transitions in V_{mcm}. This branch bypasses higher-order components of leakage current (on account of the presence of the capacitor $2C_f$) and allows only lower-order components of currents to flow through the ground path. From this analysis, it is evident that the LCL filter reduces the leakage current significantly.

4.6 Experimental Results

A low-scale hardware prototype of the proposed DqZS-7LI is fabricated to verify the MATLAB-Simulink results. Fig.A.1 shows the fabricated hardware prototype.

To emulate the PV source two programmable DC power supplies with CC-CV characteristics are employed. The PWM scheme is implemented with a Spartan-6 FPGA board, which outputs gating pulses that are employed to drive the switches S_1-S_8 (power MOSFETs). A Yokogawa DL850 power oscilloscope is utilized to capture the experimental waveforms. Table 4.2 presents the details of the component and the specifications of the hardware prototype.

TABLE 4.2 HARDWARE PROTOTYPE SPECIFICATIONS

Parameters	Values
Input DC voltage(V_{DC})	105V
Total boosted voltage	210V
output voltage	110V (RMS)-50Hz
Switching-frequency(fs)	20kHz
Modulation-Index (m)	0.75
Inductors	EE65CORE, 3-mH
Capacitors (Electrolytic)	1400µF,300V
Ultra-Fast rectifier diode	MUR1560CT
Parasitic capacitor C_p	100nF
R_D, L_f, C_f,, Lg	1ohm,1mH, 6uf, 2.5mH
Power	300W

Fig. 4.9 demonstrates the applied input voltages (V_{in1}, V_{in2}) and boosted DC-link voltages (V_{dc1}, V_{dc2}) of the 7-level inverter. As shown in the figure the input voltages of 35 V (V_{in1}) and 70V (V_{in2}) are input to the top and bottom qZS networks respectively. As stated in the earlier sections, the proposed converter utilizes dual-quasi-Z source networks to achieve the required voltage boosting. In the present experimental studies, a shoot-through duty ratio (D) of 0.25 to achieve a boosting factor of 2 (Eqn. 4.10). A modulation index (m) of 0.75 is chosen to obtain the required output voltage (110 V). From Fig. 4.9 it may be observed that the input voltages are boosted to 70 and 140V as indicated by the traces of V_{dc1} and V_{dc2}. It may also be noted that the waveforms of the DC-link voltages are typically pulsating, as they drop to a value of zero whenever a shoot-through mode is inserted.

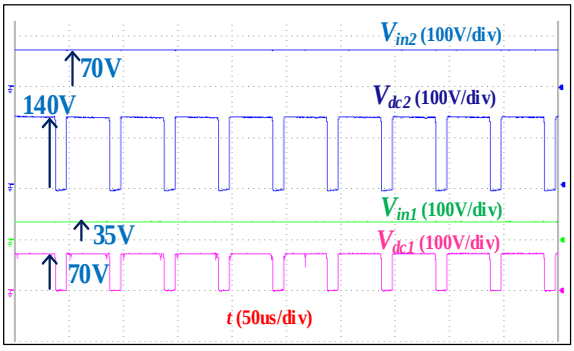

Fig. 4.9: Experimental results of DC-input voltages ($V_{in1,}$ V_{in2}) and DC-link voltages (V_{dc1}, V_{dc2}) of DqZS-7LI.

The experimental waveforms of inductor current (i_{L4}) and the capacitor voltages (V_{c3}) and (V_{c4}) of the qZS-2 are shown in Fig. 4.10. For a shoot-through (ST) duty ratio (D) of 0.25, the input voltage (top trace) of 70V is boosted to 140V DC-link (second trace). From the figure it is evident that the boosted DC-link voltage of 140V is distributed across the capacitors C_3 and C_4 in the ratio of (1-D): (D). Fig. 4.10 also shows that the voltages across the capacitors (C_3, C_4) attain steady-state values of 105 and 35V respectively. It may be observed that whenever the DC-link voltage drops to a value of zero (during the ST time period), the inductor current (i_{L4}) (third trace) increases linearly. During the non-shoot-through time period, the inductor current decreases linearly.

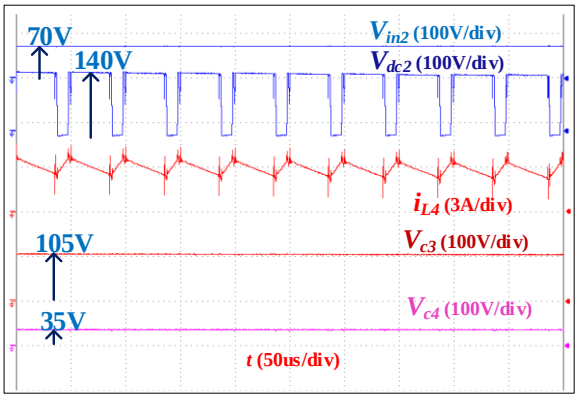

Fig. 4.10: Experimental results of the DC input voltage (V_{in2}), DC-link voltage (V_{dc2}) and inductor current (i_{L4}), and capacitor voltages (V_{c3}, V_{c4}) of the qZS-1 network.

Fig. 4.11(a) presents the output voltage and the load current of the proposed DqZS-7LI in the stand-alone mode of operation. The output voltage displays seven distinct levels between its negative and positive peak values (-210V to +210V). It may be noted that the phase voltage is a pulsating waveform that drops to a value of zero during the shoot-through period. The terminal voltage of the PV parasitic capacitor (V_{cp}) and leakage current (i_{leak}) are shown in Fig. 4.11(b).

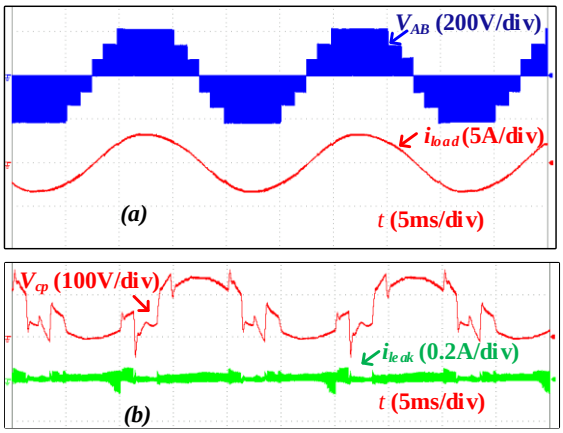

Fig. 4.11: Experimental results of (a) Output voltage waveform (V_{AB}), Load voltage (i_{Load}) (b) Parasitic capacitor voltage (V_{cp}), and Leakage current (i_{leak}) of DqZS-7LI.

It may be observed that all high-frequency voltage transitions in the terminal voltage of the parasitic capacitor (V_{cp}) are filtered out, resulting in a low leakage current (i_{leak}) of 11.97mA (RMS). This leakage current, which flows between the PV source and the ground, is well within the limits of 300mA stipulated by VDE0126-1-1.

The dynamic performance of the power converter with closed-loop control in the stand-alone mode of operation is shown in Fig. 4.12. The control scheme shown in Fig. 4.6, which regulates the DC-link voltage, is employed for experimentation. The top three traces of this figure show the DC-link voltage of the top qZS (V_{dc1}) and the capacitor voltages (V_{C1}, V_{C2}) of the corresponding qZS network. The bottom two traces show the output voltage (V_{AB}) and the load current (i_{load}) of the power converter. The load on the proposed converter is suddenly reduced (2.2 A to 1.4A) to evaluate its dynamic response against load disturbances. Fig. 4.12 reveals that neither the DC-link voltage (V_{dc1}) nor the capacitor voltages (which add up to the DC-link voltage) show any noticeable change despite a sudden change in the load. It may also be noted that the output voltage (V_{AB}) remains unperturbed as its magnitude is solely determined by the DC-link voltage in the stand-alone mode of operation.

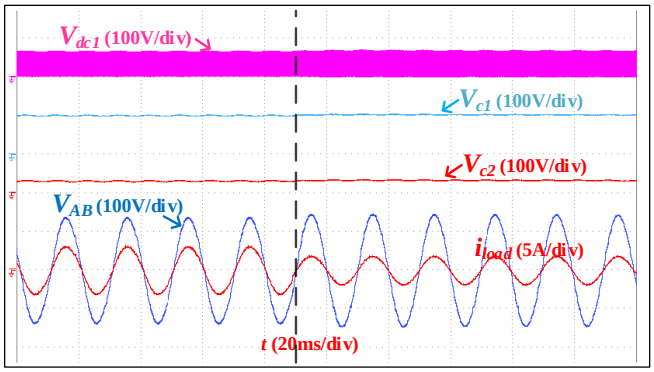

Fig. 4.12: Experimental results of DC-link voltage (V_{dc1}), capacitor voltages (V_{c1}, V_{c2}), output voltage (V_{AB}), and the load current (i_{load}).

Further, the dynamic response of the power converter against the source disturbance is assessed. In this experiment (Fig. 4.13), V_{in1} and $V_{in2,}$ which are initially maintained at 70V and 45 V respectively, are suddenly changed to 80V and 35 V. It may be noted that the second and the last traces of Fig. 4.13, which respectively show the two DC-link voltages, do not show any appreciable transients following the source disturbance.

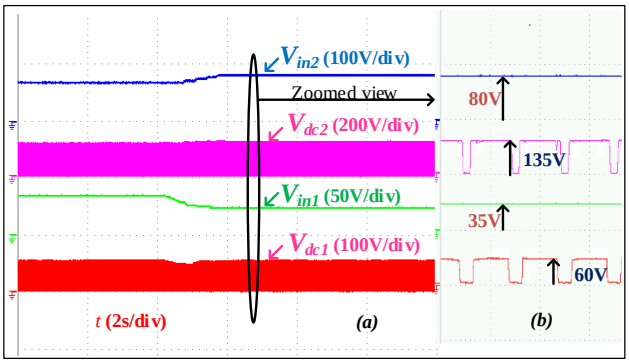

Fig. 4.13: Experimental results of (a) DC input voltages (V_{in1}, V_{in2}) and DC-link voltages waveforms of DqZS-7LI in the course of source disturbance (b) Zoomed view of the DC-link and DC input voltages of the DqZS-7L

Fig. 4.14 demonstrates the dynamic behavior of the proposed power converter while it feeds the grid. In this experiment, the active power of 135 W is fed into the grid initially. The shoot-through duty factor (D), which is automatically adjusted by the controller (Fig. 4.7) based on the insolation, is then increased to inject higher power into the grid. This action momentarily disturbs the DC-link voltage, which is quickly regulated by the action of the outer loop PI controller. This increases the reference grid current, which determines the magnitude of the current which should be fed into the grid to maintain the DC-link voltage and the output voltage. The PR regulator injects the required current into the grid by adjusting the modulation index.

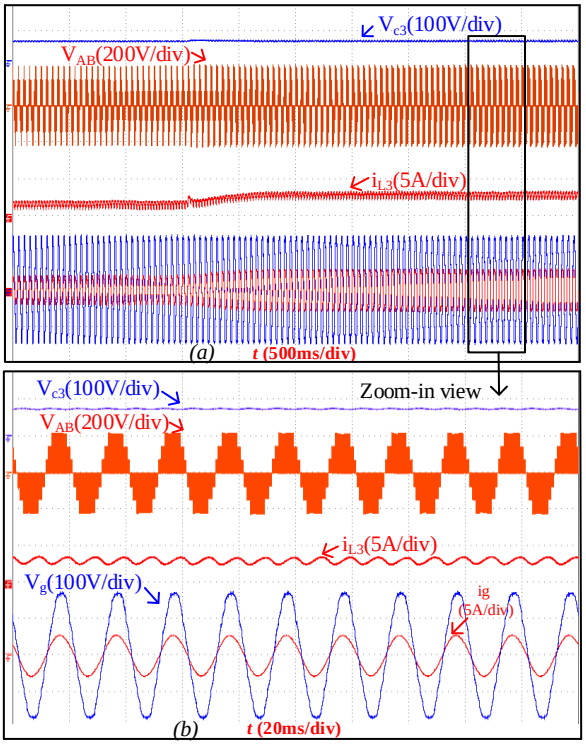

Fig. 4.14: Experimental results (a) Capacitor voltage (V_{c3}), Phase voltage (V_{AB}), Inductor current (i_{L3}) Grid voltage (V_g), and Grid current (i_g) (b) Zoom-in view at 300W.

Fig. 4.14 clearly shows the action of the controller, which automatically adjusts the modulation index. The adjustment of the modulation index results in (a) restoration of the DC-link voltage, which is evident from the first and second traces (b) an increase in the source current iL3 (from 1.3 A to 3 A, third trace), and (c) increase in the power injected into the grid (fourth trace, wherein the grid current increases from 1.23 to 2.2 A, RMS). The zoomed picture of the aforementioned quantities and waveforms clearly shows the power injection into the grid at UPF.

Fig. 4.15(a) demonstrates the reactive power capability of the power converter. The power converter is tested for a 0.8 lagging (R=40Ω, L=95mH) power factor. From Fig. 4.15(a) it may be noted that, load current 'i_{load}' is lagging w.r.t to load voltage 'V_{out}' which displays the reactive power capability of the proposed power converter.

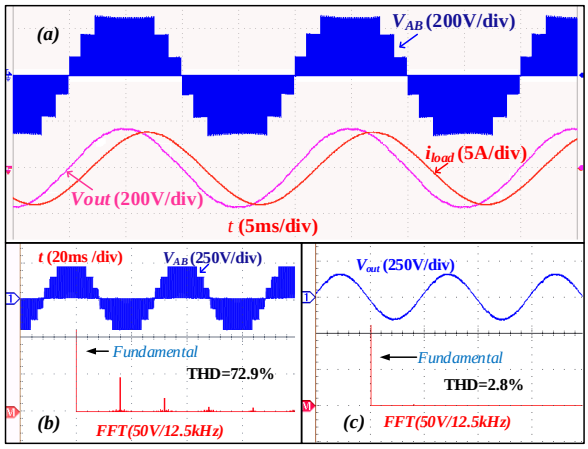

Fig.4.15: (a) Output voltage (V_{AB}), load voltage (V_{out}), and load current (i_{load}) for 0.8 lagging power factor (b) FFT of inverter output voltage 'V_{AB}' (c) FFT of output voltage 'V_{out}'

4.7 Comparison with the proposed DQZS-7LI

This section summarizes the merits of the proposed topology over the other impedance-source-based topologies, which have been reported so far in the literature. As qZS-based 7-level inverters available in the literature are scanty, a comparison with recent 5-level inverters is also considered. Table 4.3 presents the comparison of the number of components required, boost, and voltage stress across the devices in these topologies.

The proposed power converter (DqZS-7LI) requires a lesser number of capacitors, inductors, and switches when compared to the seven-level topologies presented in [53] and [59]. It may be observed that the proposed power converter requires an equal number of passive components and switches when compared to the 5-level topologies described in [54], [62]. Further, it is seen that the proposed power converter requires a lesser number of power diodes.

TABLE 4.3 COMPARISON OF THE PROPOSED POWER CONVERTER WITH QZS TOPOLOGIES

Parameters	**ZS- 7L[53]**	**qZS-NPC[54]**	**qZS-CHB[59]**	**MqZS[61]**	**qZS-5L [62]**	**Proposed**
Levels(N_L)	7	5	7	5	5	7
Sources	3	1	3	1	1	2
Capacitors	6	4	6	4	4	4
Inductors	6	4	6	2	4	4
N_{SW}	10	8	12	8	8	8
Diodes	3	6	3	3	4	2
Input current	discontinuous	continuous	continuous	discontinuous	continuous	continuous
Boost	$1/(1-2D)$	$1/(1-2D)$	$1/(1-2D)$	$2/(1-2D)$	$1/(1-2D)$	$1/(1-2D)$
Switch voltage stress	$(x\sqrt{2})/3$ $(x/\sqrt{2})$	$(x/\sqrt{2})$	$(x\sqrt{2})/3$	$(x/\sqrt{2})$	$(x/\sqrt{2})$	$x\sqrt{2}\ for\ S_1, S_2$ $(x\sqrt{2})/3\ for\ S_3, S_4$ $(x.2\sqrt{2})/3\ for\ S_5 to S_8$
Capacitor voltage stress	$\sqrt{2}/3$	$1/\sqrt{2}\ for\ C_1$	$\sqrt{2}/3\ for\ C_1$	$1/\sqrt{2}\ for\ C_1$	$1/\sqrt{2}$ $for\ C_1, C_3$	$\sqrt{2}/3\ for\ C_1$ $(x.D.\sqrt{2})/3\ for\ C_2$
		$(x.D)/\sqrt{2}$ $for\ C_2$	$(x.D.\sqrt{2})/3\ for$	$(x.D)/\sqrt{2}\ for\ C$	$(x.D)/\sqrt{2}$ $for\ C_2, C_4$	$(2\sqrt{2})/3\ for\ C_3$ $(x.D.2\sqrt{2})/3\ for\ C_4$
Diode voltage stress	$(x\sqrt{2})/3$	$(x/\sqrt{2})$	$(x\sqrt{2})/3$	$(x/\sqrt{2})$	$(x/\sqrt{2})$	$(x\sqrt{2})/3\ for\ D_1$ $(x.2\sqrt{2})/3\ for\ D_2$
TSV/N_L	1	1.4	0.71	1.5	1.2	1
Voltage THD	23.3%	76.4%	29.3%	38.2%	73.2%	72.9%
Nsw* cost of the high-side driver	10*263= Rs.2630/-	8*263= Rs.2104/-	6*263= Rs.1578/- 6*117= Rs.702/- Total = 2280/-	8*263= Rs.2104/-	8*263= Rs.2104/-	8*263= Rs.2104/-

$* x = 1/(1-D)\ where\ D\ is\ shoot-through\ duty\ ratio;\ \ cost\ of\ high\ side\ driver(\text{1EDF5673K}) = Rs.263\ ;$
$cost\ of\ low\ side\ driver(\text{IED44173NO1B3K}) = Rs.117$

compared to all of these topologies. It may be noted that the voltage stress in [59] is lower when compared to all other topologies.

However, this advantage is overshadowed by the increased number of switches, diodes, and passive components needed in this topology. As seen from the Table, it may be noted that all these power converters have the same boost factors for a given shoot-thorough duty ratio 'D' except [61]. The voltage stresses on the capacitors, diodes, and switches in all these topologies are calculated on a per-unit basis, taking the output voltage (RMS) value as the base value. It may be observed that the voltage stress in [59] is lower when compared to all other topologies. However, this advantage is overshadowed by the increased number of switches, diodes, and passive components needed in this topology. As the numbers of diodes, switches, and the voltage levels of the compared topologies are unequal, the Total Standing Voltage (TSV) (the sum of blocking voltages of all the switches and diodes w.r.t the peak

voltage value) per number of voltage levels (N_L) is calculated [71]. It may be noted that the proposed power converter registers a lower (TSV/ N_L) ratio when compared to the topologies [53], [54], [61], and [62].

The proposed power converter has a higher voltage THD when compared to [53], [59], and [61] as the zero-level is inserted in each level of operation to boost the input voltage, achieve 7-level operation, and minimize the leakage current. However, the inverter output voltage is filtered by the LCL filter to provide a sinusoidal output voltage with a THD of 2.8% (as shown in Fig. 4.15(c)) to load/grid.

All the topologies compared in Table 4.3 except [59], requires high-side drivers for multilevel operation. All the topologies are evaluated for M = 0.75, P_o =1kW, and Vo (RMS) = 230V. The minimum available high side gate driver is rated for 600V, hence cost of the 600V high side gate driver is considered for all the topologies. As the number of switches is equal in the topologies presented in [54], [61], [62], and the proposed power converter, the cost (w.r.t high side driver) is also equal. Further, the proposed power converter incurs a lower cost (w.r.t to high side gate driver) when compared to topologies [53], as the number of switches is less. The power converter [59] has 6 low-side drivers, however, this advantage is offset by an equal number of high-side switches.

4.8 The Loss analysis for the DQZS-7LI

The efficiency of the proposed power converter is assessed by evaluating the following losses (i) switching loss (P_{sw}) and conduction power losses (P_{con}) occurring in the semiconductor switches $S_1 – S_8$ (ii) switching loss (P_{sd}) and conduction losses (P_{cd}) in anti-parallel and quasi-z-source diodes (Fig. 4.1). To this end, the Powersim (PSIM) software is employed, which possesses thermal models of several popular switching devices. These simulation studies are carried out by employing MOSFET IRFP460 and the power diode 150EBU04 to construct the power converter. Further, the ESR losses (P_{cap}) in the capacitors and the conduction losses (P_{ind}) in the inductors are calculated using the method described in [77]. The loss distribution for the proposed converter for 300W power output is shown in Fig. 4.16(a). From Fig. 4.16(a) it may be noted that the simulated efficiency of the converter is around 94% at 300W output power. These losses have been evaluated assuming V_{in1} = 35V, V_{in2}= 70V, f_s =20 kHz, M = 0.75, D=0.25, Vo (ph-RMS) = 110V, PF = 1.

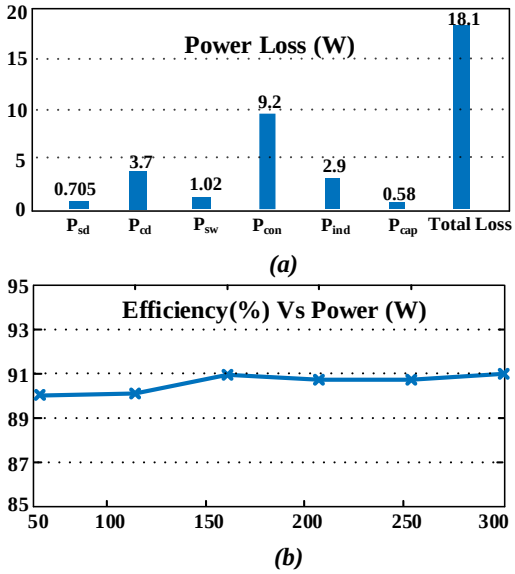

Fig. 4.16: (a). Power Loss distribution in DqZS-7LI at 300W. (b) Experimental efficiency of the proposed DqZS-7LI.

Fig. 4.16(b) shows the experimental efficiency of the power converter for a step change of power ranging from 50W to 300W. To validate the efficiency of the power converter, a power analyser (UNI-T UT283A) is employed to measure the output power. The input power is measured by a digital power meter (Yokogawa WT332E). From Fig. 4.16(b), it may be observed that the efficiency of the prototype reaches 91 % at 300W output.

4.9 Summary

This chapter proposes a single-stage dual-quasi-z-source 7-level inverter (DqZS-7LI), which is suitable for stand-alone as well as grid-connected PV applications. In this single-stage power converter, a modified LSPWM achieves the twin objectives of boosting the input PV voltages (using dual-qZS networks) and synthesizing the 7-level output voltage waveform (using the 7-level output inverter). Being a seamless structure, this power converter requires fewer semiconductor switching devices, compared to the other qZS and ZS-based seven-level topologies reported in earlier literature. Experimental studies are carried out to assess the steady-state and dynamic performances of the proposed power converter in the stand-alone mode as well as the grid-connected modes of operation. It is also shown that the leakage current is minimized by the combined effort of the modulation technique and the symmetrical LCL filter. Experimentation results demonstrate that the leakage current is well within the limits of the standards set by the *VDE 0126-1-1*. Based on the experimental results, it can be concluded that the proposed power converter could be effective for solar PV applications.

Chapter 5

A Single-Stage Quasi-Z-Source Based 5-Level Grid-tied PV Inverter with Reduced Leakage Current

Chapter 5

A Single-Stage Quasi-Z-Source Based 5-Level Grid-tied PV Inverter with Reduced Leakage Current

5.1 Introduction

The proposed power converter in chapter 4 achieves seven-level operation and voltage boosting with fewer semiconductor devices when compared to existing qZS and ZS 7-level inverter topologies. Further, the power converter is capable of operating in both stand-alone and grid-connected modes of operation with reactive power support. However, the following limitations are the demerits of the power converter: (i) The asymmetrical distribution of PV sources in the ratio 1:2 which increases the complexity of the closed control technique (ii) a higher THD in the output voltage (iii) conventional boosting factor of qZS inverter (iv) decrease in efficiency due to increased conduction losses of power diodes and switches.

These shortcomings are the motivating factors for the proposal of a 5-level, qZS-based PV inverter (5L-qZSI) in this chapter. In this topology, two symmetrical qZS networks with a single DC source are fused with a 5-level hybrid inverter. When compared to the existing qZS-based 5-level inverters in the literature, the proposed power converter employs fewer semiconductor switching devices, enhancing its reliability. The objectives of boosting the voltage of the input PV source, as well as the synthesis of a 5-level output voltage, are achieved with a modified level-shifted PWM scheme.

This chapter also discusses the closed-loop control schemes for the proposed power converter in both stand-alone and grid-tied modes of operation. It is shown that during the stand-alone mode of operation, the output voltage of the inverter is regulated for both source and load disturbances. Also, it is demonstrated that with the aid of a PLL, the grid-tied current control injects active power into the grid. It is also shown that the proposed topology is capable of reducing the leakage current, which is one of the major safety concerns in transformerless PV systems. The experimentally obtained steady-state and dynamic performances of the proposed power converter in both the stand-alone and the grid-tied modes of operation are presented in this chapter. Finally, the loss distribution among the switching devices of the power converter is simulated using PSIM software.

4.2The QZS-Based 5-level Hybrid inverter

4.2.1 Power converter

Fig. 5.1 shows the proposed single-stage PV-fed qZS-based 5-level hybrid inverter. This converter employs a single PV source, two quasi-z-source networks (qZS-1 & qZS-2), and a hybrid 5-level inverter. The output terminals of the PV source are input to the qZS networks, which boosts the low voltage of the PV source. The hybrid 5-level inverter consists of three independent legs (S_1, S_2), (S_3, S_4) & (S_5, S_6). The switching legs (S_1, S_2) & (S_3, S_4) are connected in cascade, which serves to provide a short circuit path to the quasi-z-source networks when they are operated in the shoot-through mode. A separate switching leg (S_5, S_6) is connected across the positive terminal of the top qZS network (shown as 'Q' in Fig. 5.1) and the negative terminal of the bottom qZS network (shown as 'O' in Fig. 5.1). This facilitates five-level inversion across the output terminals 'A' and 'B'. The 5-level inverter is interfaced with the grid through a symmetrical LCL filter.The role of the circuit components R_D, R_G, Cp, and Cn are discussed in detail in the section pertaining to the leakage current.

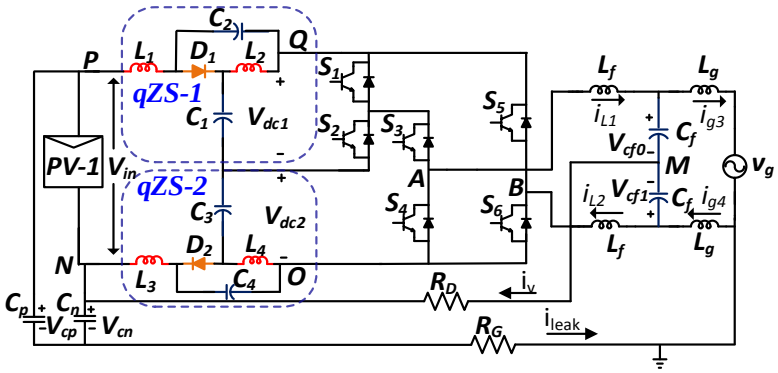

Fig. 5.1.The Proposed 5L-qZSI.

4.2.2 Switching states and corresponding output levels of the power converter

The switching combinations of the proposed power converter, along with the corresponding voltage levels which reveals that it can achieve 5-level inversion are presented in Table 5.1. Of the six switching states shown in Table 5.1, five correspond to the *non-shoot-through* (NST) states. These NST states synthesize the required voltage levels from the inverter. The remaining state, which is known as the *shoot-through* (ST) state, is used to boost the voltage of the input PV source. Fig. 5.2 shows the operational modes (NST and ST) of the proposed power converter corresponding to the switching states shown in Table 5.1. From Fig. 5.2(a),

TABLE 5.1 DIFFERENT SWITCHING LOGIC TO OBTAIN 5-LEVEL OPERATION

State-type	Switching states (1-ON, 0-OFF)						Output Voltage 'V_{AB}'	V_{AB} for (V_{dc1}= V_{dc2}=0.5V_{dc})
	S_1	S_2	S_3	S_4	S_5	S_6		
NST-1	1	0	1	0	0	1	V_{dc1}+ V_{dc2}	V_{dc}
NST-2	0	1	1	0	0	1	V_{dc2}	0.5V_{dc}
NST-3	0	1	0	1	0	1	0	0
NST-4	0	1	1	0	1	0	-V_{dc1}	-0.5V_{dc}
NST-5	0	1	0	1	1	0	-(V_{dc1} +V_{dc2})	-V_{dc}
ST-1	1	1	1	1	0	1	0	0

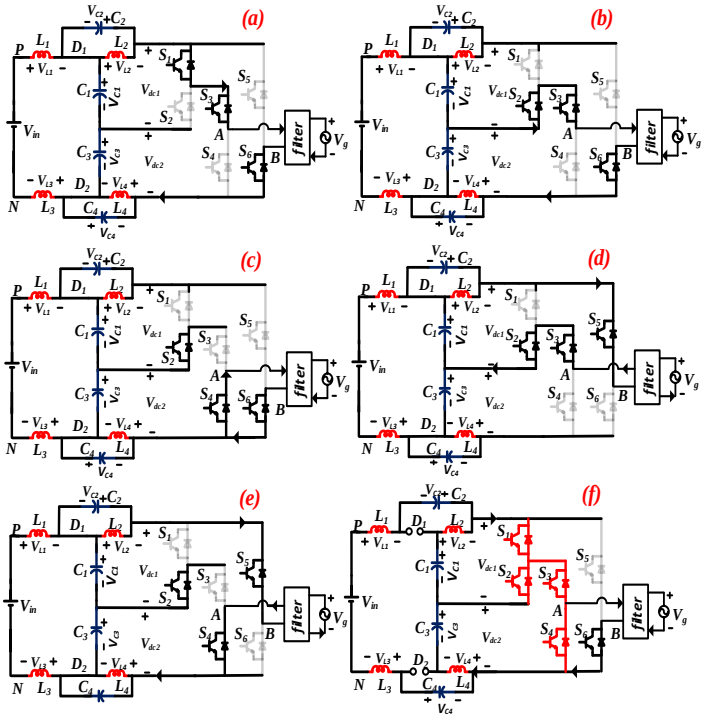

Fig. 5.2. Circuit diagrams for NST and ST states of the power converter.

it may be observed that switches S_1, S_3 & S_6 are turned on to apply the total DC-link voltage of 'V_{dc1}+V_{dc2}' across the load. When switches S_2, S_3 & S_6 are turned on, only half the total DC-link voltage 'V_{dc2}' is applied across the load terminals as shown in Fig. 5.2(b). Fig. 5.2(c) demonstrates the zero state where only two switches S_4 and S_6 are turned on to produce the freewheeling path. Similarly, the corresponding operational modes, which produce the negative voltage levels in the output voltage across the load are shown in Fig. 5.2(d),(e).

During the NST state, the voltages across the four inductors and the total DC-link voltage are expressed as :

$$V_{L1} + V_{L3} = V_{in} - V_{C3} - V_{C1} \quad (5.1)$$

$$V_{L2} = -V_{C2} \quad (5.2)$$

$$V_{L4} = -V_{C4} \quad (5.3)$$

$$V_{dc} = V_{dc1} + V_{dc2} = (V_{C1} + V_{C2}) + (V_{C3} + V_{C4}) \quad (5.4)$$

It may be observed that during the zero-state, there is no power transfer between the PV source and the load. A fraction of the zero-state (Fig. 5.2(c)) is allocated to insert the ST state, which is pivotal to the implementation of the boosting operation, wherein all four switches S_1-S_4 are turned on to provide the short circuit path to qZS networks (Fig. 5.2(f)).

The PWM scheme adopted in this work attaches a zero-state to all of the NST states. As an ST state is inserted in every zero-state, the DC-link voltage falls periodically to a value of zero, making it appear as a pulsed waveform. The pulsation in the DC-link voltage causes a corresponding pulsation in the output voltage. Thus, the instantaneous value of the output voltage falls to a value of zero at all voltage levels.

During the ST state, the voltages across the inductors and the total DC-link voltage are expressed as:

$$V_{L1} + V_{L3} = V_{in} + V_{C2} + V_{C4} \quad (5.5)$$

$$V_{L2} = V_{C1} \quad (5.6)$$

$$V_{L4} = -V_{C3} \quad (5.7)$$

$$V_{dc} = V_{dc1} + V_{dc2} = 0 \quad (5.8)$$

4.2.3 Boost factor

Application of the volt-sec balance to all of the inductor voltages over one switching time period paves the way to the derivation of the boost factor obtained with the proposed power converter. Each switching time period consists of one of the NST modes (equations 5.1-5.3) & the ST mode (equations 5.5-5.7). It may be noted that the symmetry of the qZS networks results in V_{C1}=V_{C3} and V_{C2}=V_{C4}.

The voltages across the capacitors are expressed as:

$$V_{C1}=V_{C3} = \frac{(1-D)}{(1-2D)}\frac{V_{in}}{2} \quad (5.9)$$

$$V_{C2}=V_{C4}=\frac{(D)}{(1-2D)}\frac{V_{in}}{2} \tag{5.10}$$

Where 'D' is the shoot-through duty ratio, defined as T_{sh}/T_s. (where T_{sh} and T_s respectively denote the shoot-through time and the time period of the switching cycle).

Hence, the total boosted DC-link voltage from equation (5.4) is expressed as :

$$V_{dc}=V_{dc1}+V_{dc2}=\frac{1}{(1-2D)}V_{in} \tag{5.11}$$

5.3 Modulation scheme

The proposed power converter is modulated with a level-shifted PWM technique, which is capable of achieving the twin objectives of boosting the PV voltage as well as the generation of a 5-level output voltage waveform. Fig. 5.3 presents the schematic diagram of the modulator, which generates the modulation signal v^*_m which is compared with the carrier C_1 to synthesize the gating signals for the power semiconductor switching devices. The modulator (Fig. 5.3) performs two tasks namely, (i) zone selection (ii) level selection. In Zone selection, the sinusoidal control signal 'v_m' is divided into two zones (z_1 & z_2) based on the value of the modulation index 'm' as shown in Fig. 5.3. In zone-1 ($0 < v_m < m/2$), the modulating signal doesn't undergo any change. In zone-2 ($m/2 < v_m < m$), the modulating signal v_m is scaled down to $v_m/2$. The summation of the references generated in zone-1 & 2 synthesizes the modulation signal v^*_m as shown in Fig. 5.3.

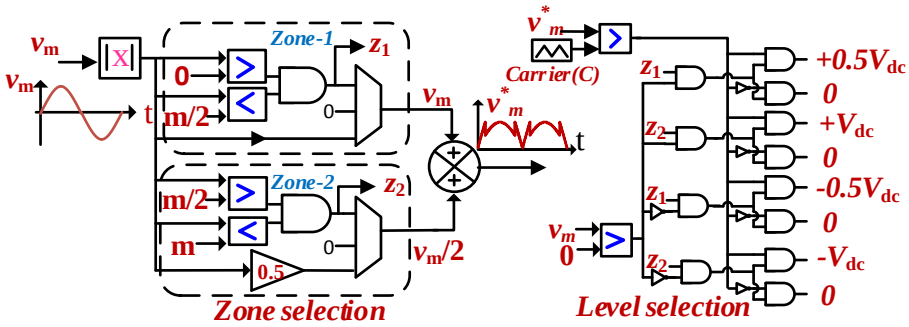

Fig. 5.3. Implementation of the modulation scheme for 5L-qZSI.

In level selection**,** the required output level is selected based on the following factors (i) polarity of the control signal 'v_m' (ii) zone of operation (z_1 & z_2) (iii) comparison output of v^*_m' and carrier signal 'C'. For example, if the control signal $v_m > 0$ and it is in zone-1 ($0 < v_m < m/2$) of operation, then the output voltage is switched to zero volts when $v^*_m <$ carrier(C) and switched to '$+0.5V_{dc}$' when $v^*_m >$ carrier(C). Further, the required gating sequence of the selected level is chosen from Table 5.1 (NST-1 to NST-5).

To augment the functionality of shoot-through to the generation of voltage levels described above, the power devices corresponding to the ST state should also be turned on (see the last row of Table 5.1). The generation of the shoot-through signal (S_T) is accomplished by the comparison of a DC reference signal (v_{sh}) with the carrier wave (C, Fig. 5.4). Thus, it is evident that the actual gating signals to the power devices S_1-S_4 are obtained by the logical OR operation of the level-generating gating signals ($S_{11} - S_{44}$, Fig. 5.4) with the shoot-through-generating gating signals (S_T, Fig. 5.4). It should be noted that the switching devices S_5 and S_6 are low-frequency signal operated at grid frequency (Fig. 5.4). These signals are generated based on the polarity of the control signal 'v_m' (Fig. 5.3).

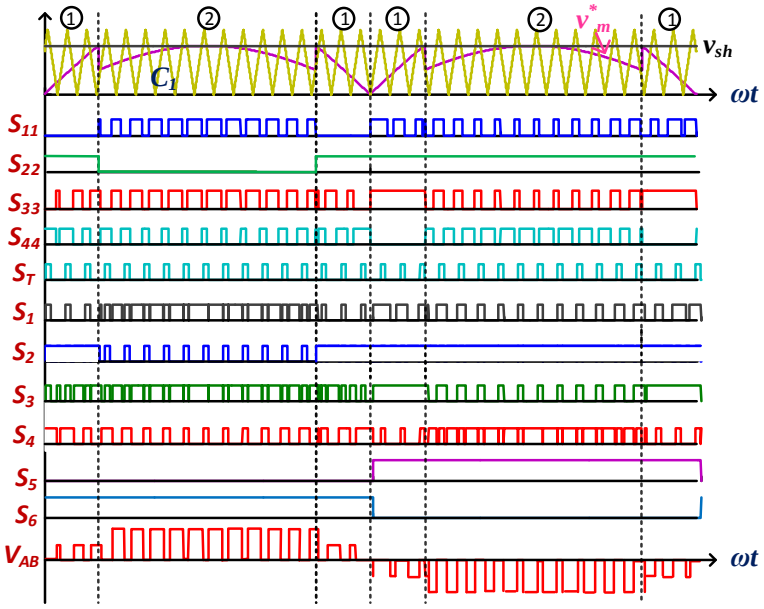

Fig. 5.4. Implementation of the modulation technique.

5.4 Proposed control strategy for stand-alone and grid-connected 5L-QZSI

The controllers used in the stand-alone and grid-connected mode which are introduced in chapter 4 are reproduced here for ready reference.

5.4.1 Stand-alone mode

The proposed power converter offers two degrees of freedom to regulate the output voltage to the desired RMS value (i) modulation index 'm' (ii) shoot-thorough duty ratio 'D'. Generally, in the stand-alone mode of operation, the output voltage is regulated with exclusive control of the ST duty ratio 'D' while keeping the modulation index 'm' constant. By

controlling the duty ratio '*D*' the DC-link voltage of the converter is regulated to a constant value, irrespective of the source and load disturbances.

In the proposed 5L-qZSI, the total DC-link voltage (V_{dc1}+V_{dc2}) drops to a value of zero whenever a shoot-thorough state is inserted in the zero-state (shown in Fig. 5.2(f)) and assumes the value of the boosted DC-link during the non-shoot-through (NST) states. This results in a pulsating signal, which cannot be directly used as a feedback signal to the PI controller. Hence an indirect closed-loop control of the DC-link voltage of the proposed power converter is shown in Fig. 5.5.

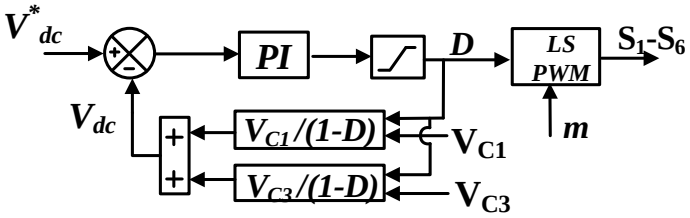

Fig. 5.5. Indirect DC-link voltage regulation of the proposed 5L-qZSI.

As shown in Fig.5.5. the total DC-link voltage (V_{dc}) is estimated by sensing the voltage across the capacitors *'V_{c1}, V_{c3}'* and '*D*'. This estimated DC-link voltage (V_{dc}) is then compared with the reference DC-link voltage (V^*_{dc}) and the error generated is compensated by the PI controller. The duty ratio '*D*' is generated by comparing the output of the PI controller (the DC reference signal V_{sh} shown in Fig. 5.4) with the carrier *C* to introduce the shoot-through state in the switches S_1-S_4.

5.4.2 Grid-tied mode of operation

Fig. 5.6 presents the control scheme for the proposed power converter to inject active power into the grid. This control scheme has an independent MPPT control (to extract the maximum power from the PV source), an outer voltage loop to regulate total DC-link voltage, and an inner current control loop to inject active power at UPF. As discussed earlier, the two degrees of freedom, namely the modulation index (*m*) and the shoot-through duty factor (*D*) are utilized to achieve these objectives.

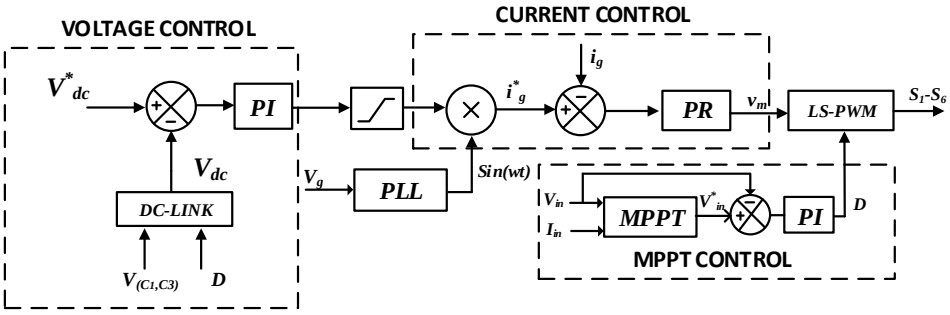

Fig. 5.6. The control scheme for grid-tied 5L-qZSI.

To track the maximum power point of the PV panel, a simple P&O algorithm is implemented. The Voltage (V_{in}) and current (I_{in}) of the PV source are sensed and fed to the P&O algorithm. The MPPT tracks the maximum power, by generating the reference input voltage (V^*_{in}). Further, the reference input voltage (V^*_{in}) is compared with the actual input voltage of the PV panel (V_{in}). The resultant error is compensated by the PI controller by controlling the shoot-through duty ratio 'D' of the power converter, which directly controls the total DC-link voltage (V_{dc}) of the proposed power converter.

As mentioned earlier, the DC-link voltage is indirectly estimated by the capacitor voltages (V_{C1}, V_{C3}) and the shoot-through duty ratio (D). The outer voltage loop regulates the total DC-link voltage (V_{dc}) to its reference value (V^*_{dc}). The control signal generated by the PI controller is multiplied by a unit-sine, which is synchronized to the grid using a single-phase SOGI-PLL. The synchronized reference current (i^*_g) is then compared with the grid current and the error is compensated by a PR controller. The output of the PR controller is a sinusoidal control signal (v_m), which is further modified to v^*_m as discussed in section III. This modulation signal v^*_m is compared with the carrier 'C' to produce the PWM for the switches S_1-S_6 thereby, controlling the active power injected into the grid [86],[88].

5.5 Reduction of leakage current

Leakage current is an issue of paramount interest in transformerless PV systems. The ill effects of leakage current are well-researched and documented. It leads to the distortion of grid voltage, electromagnetic interference, and safety issues [90]. The VDE0126-1-1 standard stipulates that the maximum value of current be limited to 300mA (RMS) [10].

Additional shoot-through pulses, which are inserted in qZS inverters to boost the input PV voltage, result in high-frequency voltage transitions across the parasitic capacitor formed between the PV array and the ground. This capacitive coupling induces leakage current when galvanic isolation is absent.Therefore, it is desirable to maintain a constant voltage across the

parasitic capacitor to eliminate the leakage current. Nevertheless, in qZS-based multilevel inverters, it is not possible to eliminate the leakage current owing to the insertion of shoot-through in the zero-state. Hence, in the proposed power converter, the leakage current is reduced by limiting the magnitude of the high-frequency voltage transition across the parasitic capacitor.

In the proposed power converter, these high-frequency voltage transitions are determined by the effective CMV (v_{ecm}), which is defined as:

$$v_{ecm} = v_{cmv} + v_{L3} - v_{C4} \tag{5.12}$$

Where v_{cmv}, is the common-mode voltage which is expressed as :

$$v_{cmv} = \frac{v_{AO}+v_{BO}}{2} \tag{5.13}$$

The difference between inductor voltage 'v_{L3}' and the capacitor voltage 'v_{C4}' during shoot-through (ST) and non-shoot-through (NST) states are expressed as:

$$v_{L3} - v_{C4} = 0.25V_{dc} \quad \text{for the ST state} \tag{5.14}$$

$$v_{L3} - v_{C4} = \frac{-(D)}{(1-2D)}\frac{V_{dc}}{2} \quad \text{for the NST state} \tag{5.15}$$

Table 5.2 presents the pole voltages (v_{AO},v_{BO}), CMV (v_{cmv}), and the effective CMV (v_{ecm}) of the power converter in the non-shoot-through (NST) and the shoot-through (ST) states. As an illustration, the effective CMV is calculated based on the equations (5.12) when the shoot-through duty ratio '*D*' is equal to 0.25. It may be noted that the voltages across L_3 and C_4 of the qZS-2 network reduce the effective CMV in the range of 0 to 0.5 V_{dc} (eqn.5.12).

TABLE 5.2 EFFECTIVE CMV OF THE POWER CONVERTER FOR D=0.25

State-type	Output voltage	v_{AO}	v_{BO}	v_{cmv}	v_{ecm}
NST-1	V_{dc}	V_{dc}	0	0.5 V_{dc}	0.25 V_{dc}
NST-2	0.5V_{dc}	0.5 V_{dc}	0	0.25 V_{dc}	0
NST-3	0	0	0	0	0.25 V_{dc}
NST-4	-0.5V_{dc}	0.5 V_{dc}	V_{dc}	0.75V_{dc}	0.5 V_{dc}
NST-5	-V_{dc}	0	V_{dc}	0.5V_{dc}	0.25 V_{dc}
ST-1	0	0	0	0	0.25 V_{dc}

As mentioned above, the effective CMV (v_{ecm}) of the power converter introduces current harmonics of higher order in the leakage current. To minimize these higher-order harmonics, a symmetrical LCL filter is connected across the output terminal of the inverter '*A' & 'B'* as shown in Fig. 5.7. A damping resistor (R_D) is connected between the negative

terminal of the PV source '*N*' and the midpoint of the filter capacitors '*M*' to dampen the oscillations in leakage current, which arise due to the ringing of the LC components. In Fig. 5.7, the symbols 'R_G', 'C_p', and 'C_n' respectively denote the ground resistance, and the parasitic capacitances formed between the PV panel and the ground. Both of the parasitic capacitors of the PV panel are assumed to have the same capacitance value ($C_p = C_v = C$) [85].

The common-mode model of the power converter shown in Fig. 5.7 is assessed to evaluate the effect of the LCL filter on the leakage current.

The common-mode model equations are expressed as:

$$\frac{L_f}{2}\hat{\imath}_{cmi} = \frac{v_g}{2} - \frac{L_g}{2}\hat{\imath}_{leak} - i_{leak}R_G - v_c - v_{ecm} \tag{5.16}$$

$$\frac{L_f}{2}\hat{\imath}_{cmi} = v_{cmf} - v_{ecm} + i_v R_D \tag{5.17}$$

$$2C\hat{v}_c = i_{leak} \tag{5.18}$$

$$2C_f\,\hat{v}_{cmf} = i_{leak} - i_{cmi} \tag{5.19}$$

where, v_{cmf} represents the common-mode filter voltage ($(v_{cf0} - v_{cf1})/2$) and i_{cmi} denotes the common-mode inverter current ($i_{L2} - i_{L1}$).

The equivalent circuit shown in Fig. 5.8 presents the pictorial representation of the common-mode equations (5.16-5.19). The simplified equivalent circuit of the Common mode model of the filter is shown in Fig. 5.9.

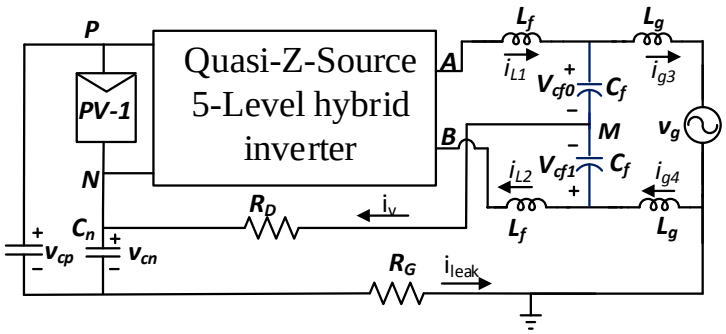

Fig. 5.7. 5L-qZSI with leakage current path.

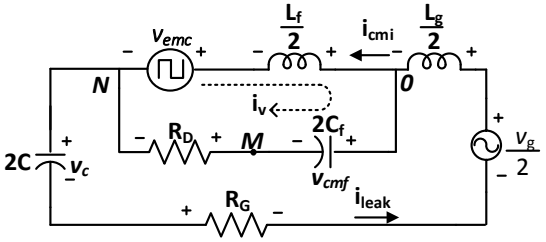

Fig. 5.8. Equivalent circuit of the common-mode model.

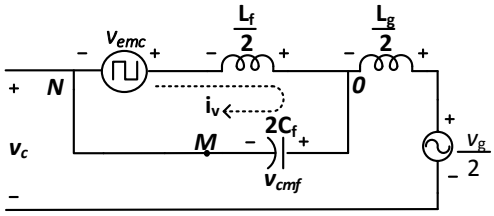

Fig. 5.9. The simplified equivalent circuit.

From the simplified equivalent circuit (Fig. 5.9) the voltage 'v_c' induced across the parasitic capacitor is expressed as follows:

$$v_c = \frac{-v_{emc}(\omega)}{1-\omega^2 L_f C_f} + \frac{v_g}{2} \tag{5.20}$$

$$v_c = \frac{-v_{emc}(\omega)}{1-\frac{\omega^2}{\omega_r^2}} + \frac{v_g}{2} \tag{5.21}$$

Where 'ω_r' is the resonance frequency of the filter ($(L_f/2)$,$2C_f$) and 'ω' is the switching frequency of the inverter.

From equation (21) it may be observed that an extra term of -1/($1 - \frac{\omega^2}{\omega_r^2}$) is multiplied by the effective CMV(v_{emc}). Hence, the attenuation gain(dB) of 20 log $\left|1 - \frac{\omega^2}{\omega_r^2}\right|$ is applied to v_{emc} which increases with lesser resonance frequency 'ω_r'. Thus, the main contribution of the high-frequency component in the parasitic capacitor 'v_{emc}' is attenuated by 20 log $\left|1 - \frac{\omega^2}{\omega_r^2}\right|$. This leaves only the grid frequency component to be present across the parasitic capacitor which reduces the leakage current to be within the grid standards. As the AC filter ($(L_f/2)$,$2C_f$) forms a closed path, a current i_v circulates in the closed loop as shown in Fig. 5.8. From the Fig. 5.9 the current i_v is expressed as follows:

$$i_v = \frac{v_{emc}(\omega).\omega}{1-\frac{\omega^2}{\omega_r^2}} \tag{5.22}$$

As the resonance frequency 'ω_r' is far less than switching frequency 'ω' the magnitude of the circulating current'i_v' in the LC filter is very small. Hence, there is no need for a damping resistor in the LC filter.

5.6 Experimental Results

The proposed power converter is experimentally validated with the laboratory prototype shown in Fig. A.1

In this system, a programmable DC source is employed to emulate the CC-CV characteristics of the PV source. A *SPARTAN-6* FPGA board is used as the digital control platform, which outputs the required gating signals to the power semiconductor switching devices S_1-S_6 (Fig.1). Table 5.3 presents the specifications of the parameters considered for hardware experimentation.

TABLE 5.3 EXPERIMENTAL SPECIFICATIONS

Operational Parameters	**Values**	**System Parameters**	**Values**
Input voltage (V_{in})	105V	Inductors (EE65CORE)	3mH
Total DC-link voltage	210V	Capacitors (Electrolytic)	300V,1000µF
Output RMS voltage	110V	Ultra-Fast rectifier diode	MUR1560CT
Modulation-Index (m)	0.75	MOSFETs	IRFP460
Output Power (P_o)	400W	Parasitic capacitor (C_p)	100nF
Switching frequency(f_{sw})	20kHz	R_D, L_f, C_f,, L_g	1ohm,1mH,6uf, 2.5mH

As shown in Fig. 5.1, the qZS networks are fed by the emulated PV source with an input voltage (V_{in}) of 105V. As this voltage is inadequate to obtain the output voltage of the required magnitude (110 V (RMS)), the input voltage is boosted to the required magnitude (which is *twice* that of the input voltage) by implementing a shoot-through duty ratio of 0.25 (Eqn. 5.9). The input voltage (V_{in}) and the DC-link voltages (V_{dc1} & V_{dc2}), i.e. the outputs of the qZS networks of the power converter, are shown in Fig. 5.10. It may be observed that the voltage of each DC-link is boosted to 105V resulting in a total DC-link voltage of 210 V (i.e $V_{dc} = V_{dc1} + V_{dc2}$). As shown in Fig. 5.10, the DC-link voltages 'V_{dc1}, V_{dc2}' are pulsating waveforms, which drop to a value of zero whenever the shoot-through mode is switched using the devices S_1- S_4 (Fig 5.2(f))). The voltage of each DC-link is boosted to 105V resulting in a total DC-link voltage of 210 V (i.e $V_{dc} = V_{dc1} + V_{dc2}$). As shown in Fig. 5.10, the DC-link voltages 'V_{dc1}, V_{dc2}' are pulsating waveforms, which drop to a value of zero whenever the shoot-through mode is switched using the devices S_1- S_4 (Fig. 5.2(f))).

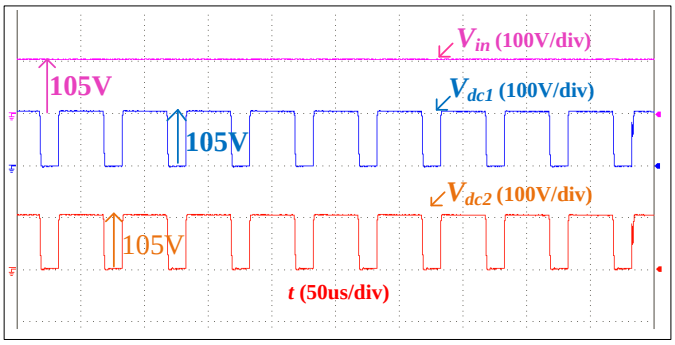

Fig. 5.10. Experimental results of input voltage (V_{in}) and DC-link voltages V_{dc1} & V_{dc2}.

Fig. 5.11 presents the experimental waveforms of input voltage (V_{in}), DC-link voltage (V_{dc1}), inductor current (i_{L1}), and the capacitor voltages (V_{c1} & V_{c2}) of the power converter (Fig. 5.1). It may be observed that, when the shoot-through-mode (ST-mode) is inserted into the power converter, the DC-link voltage drops to a value of zero. During the ST-mode, the inductor current (i_{L1}) increases linearly and stores energy from the input source. In contrast, during the non-shoot-through-mode (NST-mode), i.e. when the DC-link voltage assumes a value of 105V as shown in Fig. 5.11, the inductor current (i_{L1}) decreases linearly while discharging its energy into the load. Theoretically, the capacitors 'C_1' and 'C_2' of the qZS network-1 should share the DC-link voltage (V_{dc1}) in the ratio of (*1-D*): *D*. The traces of the capacitor voltages, presented in Fig. 5.11, confirm that the DC-link voltage output by the qZS network-1 (105V) is distributed in the ratio of 0.75:0.25 across these two capacitors (78 V and 26 V respectively).

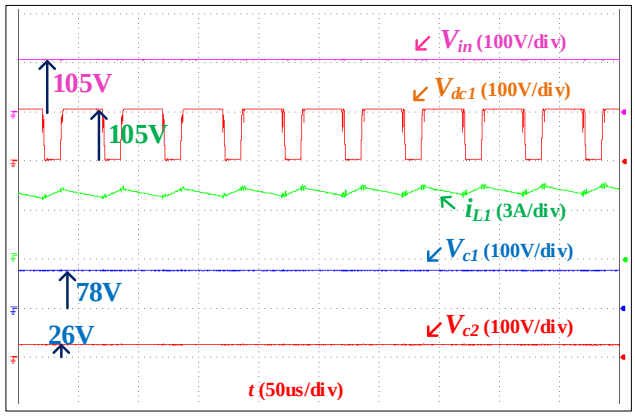

Fig. 5.11. Experimental results of the input voltage (V_{in1}), DC-link voltage (V_{dc1}), inductor current (i_{L1}), and capacitor voltages (V_{c1}, V_{c2}).

The proposed power converter is operated with a modulation index of 0.75 and a shoot-through duty ratio of 0.25 to obtain the required output voltage of 110V (RMS) at the output. The waveforms of the output voltage (V_{AB}) and the load current (i_{load}) are shown in Fig. 5.12. The experimental result of the output voltage clearly shows 5 distinct voltage levels namely, 0V, ±105V, and ±210V. The magnified view clearly reveals that the output voltage pulsates between the values of zero and the current-voltage level output by the converter (Fig . 5.12).

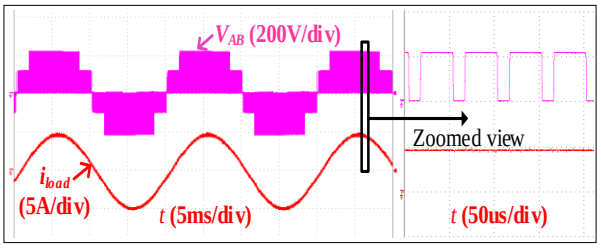

Fig. 5.12. Experimental waveforms of output voltage (V_{AB}) and load current (i_{load}).

Fig. 5.13 provides the zoomed view of (i) voltage across the parasitic capacitor 'V_{cp}' (ii) leakage current 'i_{leak}' and (iii) FFT spectrum of the leakage current. It may be noted that the high-frequency voltage transitions across the parasitic capacitor are effectively bypassed with the use of the LCL filter and the additional path 'MN' (Fig. 5.7). Consequently, the parasitic capacitor is exposed only to the low-frequency content in the voltage transitions, leading to an effective reduction in the leakage current. It may be noted that the leakage current with the proposed power converter is 10.15mA (RMS), which is well within the limits of 300mA stipulated by VDE0126-1-1.

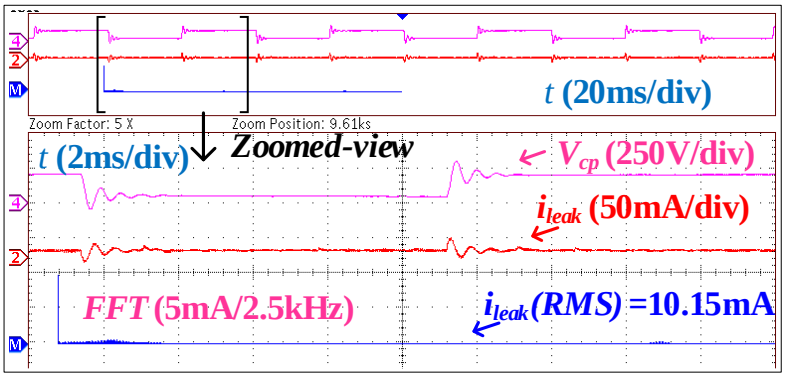

Fig. 5.13. Experimental results of parasitic capacitor voltage (V_{cp}), leakage current (i_{leak}) of the PV source, and harmonic spectrum of leakage current.

The DC-link voltage regulation of the power converter in stand-alone mode of operation is demonstrated in Fig. 5.14 & Fig. 5.15.The dynamic performance of the proposed 5L-qZSI (with the controller shown in Fig. 5.5) against the load disturbance is presented in Fig. 5.14. The top two traces in Fig. 5.14 present the DC-link voltages (V_{dc1}&V_{dc2}), while the bottom

two traces show the output voltage and the load current waveforms. Initially, both the DC-link voltages are boosted to 105V (peak) by maintaining a shoot-through duty ratio (D) of 0.25, while delivering a load current of 1.76A. Then, the load current is suddenly increased to 3.53A and is then decreased back to 1.76A. With this change in the load current, the disturbance in the DC-link voltage is sensed and the closed-loop DC-link controller automatically adjusts the shoot-through duty ratio to maintain the DC-link voltage at 105V. It may also be noticed that both DC-link voltages are regulated at 105V despite the load disturbances (Fig. 5.14). The settling time of the DC-link voltage after the load disturbance is less than 2 fundamental cycles. As the output voltage (V_{AB}) is solely dependent on the DC-link voltages of the power converter in the stand-alone mode of operation, it is regulated at the set value of the reference (i.e.110V (RMS)) despite the load disturbances (Fig. 5.14).

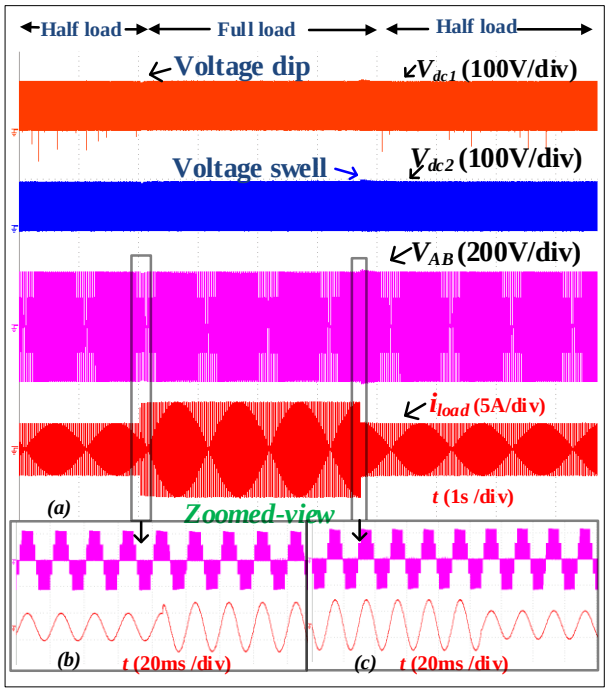

Fig. 5.14. Experimental results of DC-link voltages (V_{dc1} & V_{dc2}), output voltage (V_{AB}) and load current (i_{load}).

Fig. 5.15 shows the dynamic response of the proposed power converter against supply disturbances. In this experiment, the input voltage (V_{in}), which is initially maintained at 100V is subjected to a quick disturbance of 30V. It may be observed that the DC-link voltages (bottom two traces) are well regulated at a constant value of 105V with a quick dynamic response. Thus, it may be concluded that the closed-loop controller (Fig. 5.14) effectively regulates the DC-link voltages for both source and load variations.

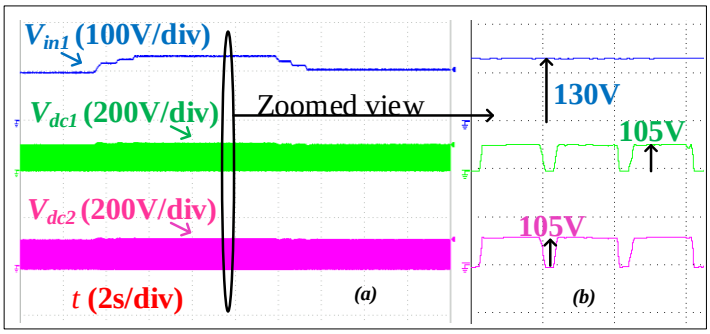

Fig. 5.15. Experimental results of (a) input voltages (V_{in1}) and DC-link voltages (V_{dc1} & V_{dc2}) (b) Zoomed view of the plot (a).

Fig. 5.16 presents the behavior of the proposed power converter in the grid-tied mode of operation. With the controller shown in Fig. 5.6, the active power of 230W is initially injected into the grid. As mentioned earlier, the value of irradiation determines the value of the shoot-through duty ratio '*D*'. To emulate the behavior of the PV source, which increases the output power with an increase in the value of irradiation, a step change is introduced in the value of the shoot-through duty ratio 'D' (0.18 to 0.21). The corresponding increase in the input power can be noticed from the change in the input current (I_{in}) from 2.4A to 3.8A RMS (third trace). This momentarily increases the DC-link voltage (second trace). However, the error between the reference and the actual (feedback) values of the DC-link voltage is compensated by the PI controller (Fig. 5.6), which increases the reference value of the grid current. The PR controller, which is present in the inner current loop compensates for the current error by readjusting the modulation index '*m*' to increase the current injected into the grid. This automatically restores the value of the DC-link voltage (V_{dc}) and the output voltage (V_{AB}) of the inverter. Fig. 5.16 clearly shows the increase in the value of the grid current from 2.11A to 3.56 (RMS) at UPF.

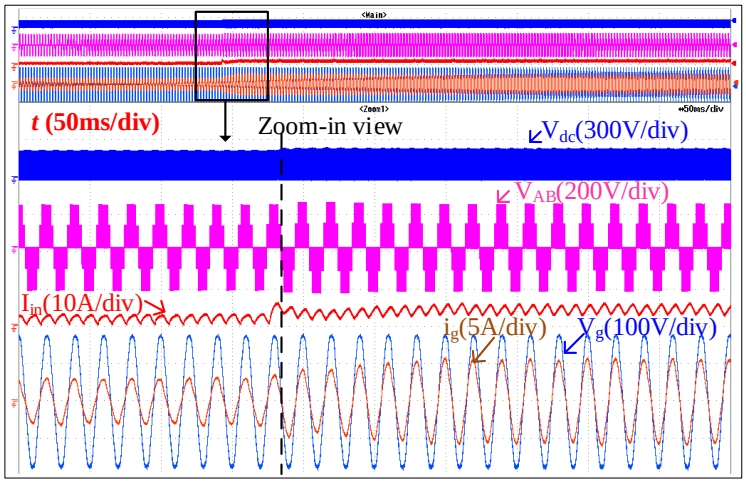

Fig. 5.16. Experimental results of the total DC link voltage, output voltage of the inverter (V_{AB}), grid voltage (V_g), and current (i_g).

Fig. 5.17 (a) and Fig. 5.17(b) show the harmonic spectrum of the inverter voltage 'V_{AB}', and grid current 'i_g' wherein the RMS value of the fundamental component is 110V (RMS) and 3.6A. The voltage THD and current THD obtained are 75.5% and 3.65%. The measured voltage THD of the power converter is on the higher side due to the insertion of a zero-state in each voltage level of operation to boost the input voltage. However, the inverter voltage 'V_{AB}' is filtered by the LCL filter to provide sinusoidal output voltage 'V_{out}' of THD 1.8% to load/grid (as shown in Fig. 5.17(c)).

To validate the reactive power capability, the power converter is tested for a 0.8 lagging (R=26Ω, L=61mH) power factor. Fig .5.17(d) demonstrates the experimental waveforms of inverter output voltage 'V_{AB}', load voltage 'V_{out}', and load current 'i_{load}'. It may be observed that the load current is lagging w.r.t to load voltage (V_{out}) which shows the reactive power capability of the power converter.

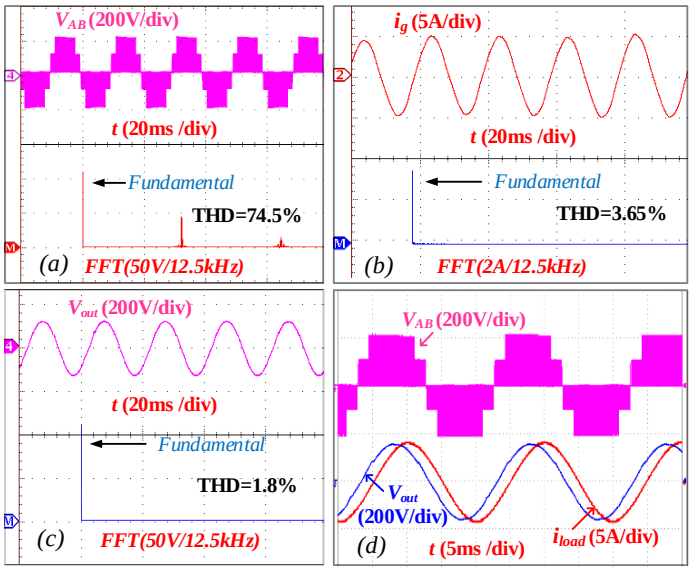

Fig .5.17 (a) FFT of inverter output voltage 'V_{AB}' (b) FFT of grid current 'i_g' (c) FFT of output voltage 'V_{out}'(d) output voltage (V_{AB}), load voltage (V_{out}) and load current (i_{load}) for 0.8 lagging power factor.

5.7 Comparison of proposed topology with 5-Level qZSI

This section critically compares the proposed power converter vis-à-vis the previously available topologies in literature, which are based on the 5-level-qZS inverter. This comparison is based on the number of semiconductor switching devices and passive components and summarizes the voltage stress across devices for all of the five topologies. From Table 5.4, it may be observed that the proposed topology (5L-qZSI) has a lower number of semiconductor switches, compared to other 5-level qZS inverters. It may also be

noted that, while the proposed power converter uses fewer power diodes when compared to the topologies [54], [61], and [62]. The proposed topology 5L-qZSI is on par with the other quasi-z-source converters, in terms of the number of capacitors. While it appears that the MqZS-5LI [61] has an advantage w.r.t the proposed power converter in terms of inductors, it results in a discontinuous input current which is not favorable for PV applications. The RMS value of the output voltage is the base value for the calculation of the *per-unit* voltage stress across the switching devices as well as the passive components It may be observed that all five topologies have equal voltage stress across the capacitor and diodes. Even though the voltage stresses on the diodes and active switches are comparable in all of the five topologies, the requirement of a higher number of diodes/switches in the compared topologies leads to lower reliability [54], [59], [61] and [62]. As the number of switches and diodes are unequal across the compared topologies, the Total Standing Voltage (TSV) of the power converters is calculated [89].

TABLE 5.4 COMPARISON OF THE PROPOSED POWER CONVERTER WITH 5-LEVEL QZS TOPOLOGIES

	qZS-NPC[54]	**qCHB-FLBI[59]**	**Mqzs- 5LI[61]**	**qZS-5L[62]**	**Proposed**
Levels	5	5	5	5	5
Sources	1	2	1	1	1
Capacitors	4	2	4	4	4
Inductors	4	2	2	4	4
Active Switches	8	8	8	8	6
Diodes	6	4	3	4	2
Input current	continuous	continuous	discontinuous	continuous	continuous
Capacitor voltage stress	$1/\sqrt{2}$ C_1,C_2	$1/\sqrt{2}(1-D)$ C_1	$1/\sqrt{2}$ C_1,C_2	$1/\sqrt{2}$ C_1,C_3	$1/\sqrt{2}$ C_1,C_3
	$D/\sqrt{2}(1-D)$ C_3,C_4	$1/\sqrt{2}(1-D)$ C_2	$D/\sqrt{2}(1-D)$ C_3,C_4	$D/\sqrt{2}(1-D)$ C_2,C_4	$D/\sqrt{2}(1-D)$ C_2,C_4
Diode voltage stress	$1/\sqrt{2}(1-D)$	$1/\sqrt{2}(1-D)$	$1/\sqrt{2}(1-D)$	$1/\sqrt{2}(1-D)$	$1/\sqrt{2}(1-D)$
Switch voltage stress	$1/\sqrt{2}(1-D)$	$1/\sqrt{2}(1-D)$	$\frac{1}{\sqrt{2}(1-D)}$ for S_1-S_4	$1/\sqrt{2}(1-D)$	$1/\sqrt{2}(1-D)$for S_1-S_3
			$\sqrt{2}/(1-D)$for S_5-S_8		$1/\sqrt{2}(1-D)$ for S_4-S_6
TSV	7	5	7.5	6	5.5
Voltage THD	76.4%	42.73%	38.2%	75.2%	75.5%
Leakage current Without filter	720mA	1.1A	590mA	325mA	210mA
Leakage current With filter	520mA	Not applicable	70mA	22mA	12mA

It may be noted that the proposed power converter (5L-qZSI) registers a lower TSV when compared to qZS-NPC [54], MqZS-5LI [61], and qZS-5L [62] topologies. From Table 5.4, it may be observed that the proposed topology results in a lower leakage current of 210mA (which is under the stipulated limit of 300mA) when compared to topologies [54], [59], [61] and [62] even without the filter. This is because the proposed modulation technique applies a zero-state in each level of operation. Further, with the employment of the 'LCL' filter and with the additional path 'MN', the leakage current of the proposed topology drops to 12 mA. It may be noted that the points 'M' and 'N' cannot be connected in a cascaded H- bridge topology with an LCL filter and isolated PV sources due to the lack of a common point (Fig. 5.1) [59]. The proposed power converter has a higher voltage THD when compared to [59],[61] as zero level is inserted in each level of operation to boost the input voltage. However, the inverter output voltage is filtered by the LCL filter to provide a sinusoidal output voltage to the load/grid.

5.8 Power Loss for the 5L-QZSI

The power loss of the proposed 5L-qZSI is assessed by evaluating it using the Powersim (PSIM) software, at 400W. Thermal models of the MOSFET-IRFP460 and the power diode-ISL9R3060G2 are employed to evaluate power loss incurred in semiconductor switches (S1-S6), and power diodes (D1-D2). Further, conduction losses in the inductor (P_{ind}) and the ESR losses (P_{cap}) in the capacitors are estimated using the method described in [77]. These losses are evaluated with (i) input voltage (Vin) of 105V (ii) output voltage of 110V (RMS) (iii) switching frequency (fs) of 20kHz (iv) shoot-through duty ratio (D) of 0.25 and, (v) the modulation index (m) of 0.75. Fig. 5.19 (a) displays the power loss incurred in switching devices and passive components at 400W.

Fig. 5.19(b) presents the efficiency curves of the topologies compared in Table 5.4. The efficiencies of the power converters are assessed by evaluating the power loss incurred in it using the Powersim (PSIM) software, in the output range of 0-400W. Thermal models of the MOSFET-IRFP460 and the power diodeISL9R3060G2 are employed to evaluate the losses. It may be observed that the proposed power converter (5L-qZSI) registers a higher efficiency when compared to all of the compared topologies due to lower semiconductor switch and diode count. It may be noted that the average efficiency of the proposed power converter is about 95%.

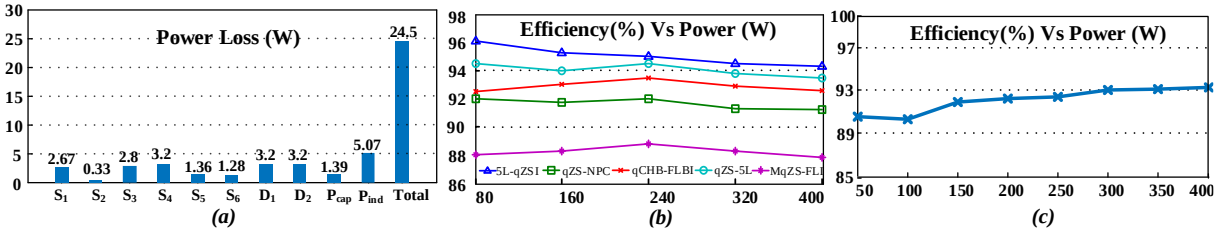

Fig. 5.18 (a) Power Loss distribution in 5L-qZSI.(b) Efficiency comparison with the 5L-qZSI (c) Experimental efficiency of the 5L-qZSI

The experimental efficiency of the power converter is validated by using a precision digital power meter (Yokogawa WT332E) to measure the input power and output power is measured by a power analyzer (UNI-T UT283A). The experimentation is implemented for a step change of 50W ranging from 50W to 400W. The hardware efficiency curve of the 5L-qZSI is shown in Fig. 5.18(c). From Fig. 5.18(c) it may be noted that the experimental efficiency of the prototype achieves 93% at 400W output.It may be observed that the hardware efficiency is in close approximation to the simulated efficiency(shown in Fig. 5.18(b)), which is about 95%. In addition to this, the CEC efficiency of the proposed power converter is also estimated using the method shown in [91]. The CEC efficiency is found to be 92 %.

5.9 Summary

This chapter proposes a single-stage, 5-level quasi-z-source-based hybrid inverter (5L-qZSI) for stand-alone, as well as grid-tied PV applications. The voltage boosting as well as 5-level inversion are simultaneously achieved with the proposed single-stage converter and the associated modulation technique. When compared to the existing qZS 5-level inverter topologies, the proposed power converter employs fewer switching devices to synthesize the 5-level output voltage waveform. It is shown that the use of an LCL filter reduces the leakage current. It is also demonstrated that, due to the combined efforts of the filter and the PWM strategy, the leakage current is suppressed to 10mA which is well within the stipulated limit of 300 mA by the *VDE 0126-1-1* standard. The steady-state and dynamic performances of the power converter in the stand-alone mode and the grid-tied mode are experimentally demonstrated. It is shown that in the stand-alone mode of operation, the output voltage of the power converter is solely regulated with the control of the shoot-through duty ratio against the source and load disturbances. Further, the dynamic performance of the current controller in the grid-tied mode of operation is demonstrated experimentally. It is shown that the current control strategy achieves the injection of active power into the grid at UPF. The power loss analysis of the proposed power converter, evaluated using the PSIM software, reveals that the efficiency of the proposed power converter is around 95%.

Chapter 6

A Quasi-Switched Capacitor Based Grid-connected PV Inverter with a Reduced Leakage Current

Chapter 6

A Quasi-Switched Capacitor Based Grid-connected PV Inverter with a Reduced Leakage Current

6.1 Introduction

In the previous chapter, a single-stage, 5-level quasi-z-source-based hybrid inverter (5L-qZSI) with only six switching devices is investigated. When compared to existing qZS-based 5-level inverter topologies in the literature, the power converter achieves 5-level operation with fewer switches devices. In addition to this, the power converter minimizes the leakage current to less than 300mA with the help of both modulation techniques and a symmetrical LCL filter connected across the load/grid. Despite these advantages, the power converter also suffers from the following drawbacks: (i) higher voltage THD (ii) conventional voltage boosting of qZS inverter (iii) utilization of additional LCL filter for leakage current minimization.

To overcome these limitations a quasi-switched capacitor-based five-level inverter (qSC-5LI) is proposed in this chapter. The power converter operates with a single DC source and draws continuous current from the input supply. Further, the power converter simultaneously achieves higher voltage boosting capability and five-level voltage inversion with the aid of a modified LSPWM scheme. In addition, the power converter minimizes the high-frequency voltage variations across the stray capacitance thereby minimizing the leakage current without any additional filter. The measured leakage current is determined to be substantially within the VDE0126-1-1-specified limit. [10].

Furthermore, it is demonstrated that the power converter's output voltage is solely regulated against source and load disturbances when operating in stand-alone mode. It is also shown that the closed-loop current control strategy injects active power into the grid at UPF. In addition to this, the loss analysis of the power converter is evaluated using thermal modules in PSIM software. Additionally, the experimental results pertaining to the dynamic performance of the five-level inverter in both stand-alone and grid-connection operations are presented in this chapter.

6.2 The QSC-Based five-level T-type inverter

6.2.1 Power Converter

The proposed quasi-switched capacitor-based five-level inverter (qSC-5LI) is shown in Fig. 6.1. The power converter comprises two quasi-z-source networks (qZS-1 and qZS-2) with a single PV source and a switched capacitor-based five-level inverter. To boost the input voltage to the desired DC-link voltage, the output terminals of the quasi-z-source networks 'Q' and 'O' are short-circuited by turning on the switches (S_1-S_4). Further, two switched capacitor units 'S_1, D_3, S_{C1}' and 'S_4, S_{C2}, D_4' are used to synthesize five levels in output voltage waveform. The load/grid is interfaced to the inverter to the mid-points of switches S_5, S_6, and the ground.

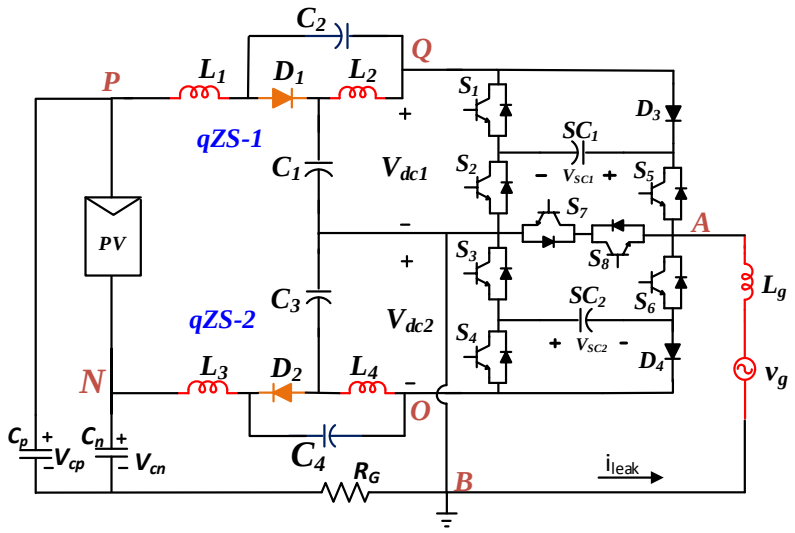

Fig. 6.1.The Proposed qSC-5LI

6.2.2 Switching logic of the qSC-5LI

The voltage levels obtained with the proposed qSC-5LI, along with their corresponding switching logics are shown in Table 6.1. Among the 8 states presented in Table 6.1, states *NST-1* to *NST-5* are the *non-shoot-through states* which synthesize 5 output levels, and states ST-1 to ST-3 represent different *shoot-through states* to obtain boosting in qZS networks. Fig. 6.2 displays the circuit diagram of the proposed topology during the non-shoot-through mode of operation. From Fig. 6.2 (a) it may be noticed that both the qZS diodes (D_1 and D_2) are forward-biased to provide a total DC-link voltage of 'V_{dc1}+V_{dc2}' across the inverter input terminals (Q, O). Further, Fig. 6.2(b) to Fig. 6.2(e) show the non-shoot-through states *NST-1*

TABLE 6.1 SWITCHING STATES TO ACHIEVE FIVE-LEVEL OPERATION

State-type	Switching logic (0-OFF,1-ON)								Output Voltage 'V_{AB}' (V_{dc1}= V_{dc2}= V_{sc1}= V_{sc2}=0.5V_{dc})	
NST-1	1	0	1	0	1	0	0	0	(V_{dc1}+ V_{SC1})	V_{dc}
NST-2	0	1	1	0	1	0	0	0	V_{dc1}	0.5V_{dc}
NST-3	0	1	1	0	0	0	1	1	0	0
NST-4	0	1	1	0	1	1	0	0	-V_{dc2}	-0.5V_{dc}
NST-5	0	1	0	1	0	1	0	0	-(V_{dc2} +V_{SC2})	-V_{dc}
ST-1	1	1	1	1	1	0	0	0	V_{SC1}	0.5V_{dc}
ST-2	1	1	1	1	0	1	0	0	-V_{SC2}	-0.5V_{dc}
ST-3	1	1	1	1	0	0	1	1	0	0

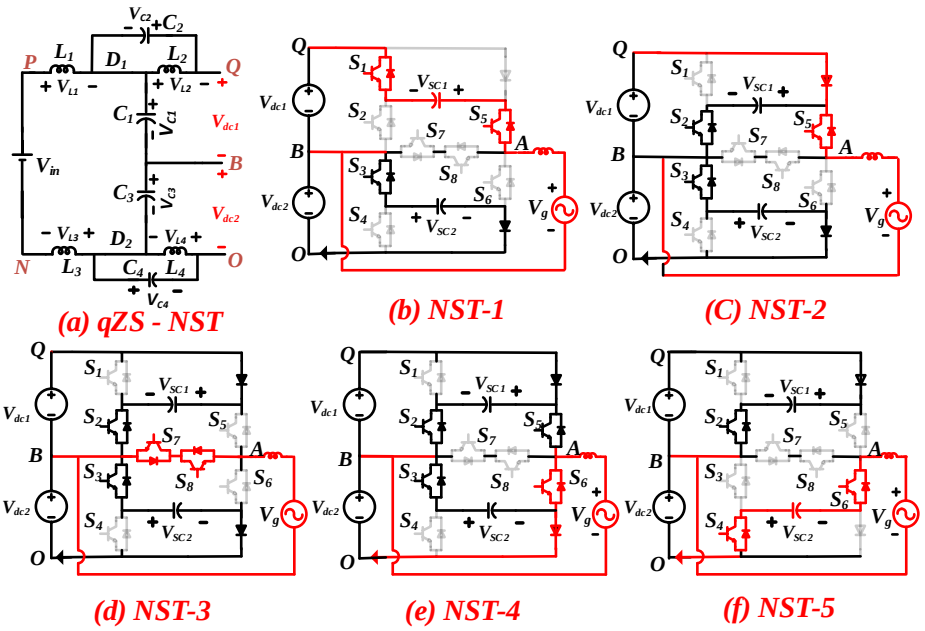

Fig. 6.2. (a) Schematic of qZS network during NST states (b-f) Schematic of MLI during NST-1 to NST-6.

to *NST-5* shown in Table 6.1 to generate $\pm V_{dc}$, $\pm 0.5V_{dc}, 0$ voltage levels. During the NST states, it may be observed that the charging currents of the switched capacitor (S_{C1}, S_{C2}) are provided by the inductors of the quasi-z-source network. Therefore the inrush charging currents of the switched capacitors are reduced to a lower value.

During the Non-shoot-through state, the voltages across the inductors (L_1-L_4) and the total DC-link voltage(V_{dc}) are stated as:

$$V_{L1} + V_{L3} = V_{in} - V_{C3} - V_{C1} \quad (6.1)$$

$$V_{L2} = -V_{C2} \quad (6.2)$$

$$V_{L4} = -V_{C4} \quad (6.3)$$

$$V_{dc} = V_{dc1} + V_{dc2} = (V_{C1} + V_{C2}) + (V_{C3} + V_{C3}) \quad (6.4)$$

Fig. 6.3 presents the different shoot-through states (*ST-1* to *ST-3*) of the qSC-5LI shown in Table 6.1. From Fig. 6.3(a) it may be noticed that the terminals 'Q and O' of the power converter are short-circuited by turning on the switches 'S_1 to S_4' thereby storing energy in the quasi-z-source inductors. This shoot-through can be implemented in three different ways in the proposed power converter as shown in Fig. 6.3(b), Fig. 6.3(c), and Fig. 6.3(d). During *ST-1* and *ST-2* the power converter outputs $+0.5V_{dc}$ and $-0.5V_{dc}$ across the grid, as shown in Fig. 6.3(b) and Fig. 6.3(c). Further, during ST-3 the switches S_7 and S_8 are turned on to output 0 V across the grid as shown in Fig. 6.3(c).

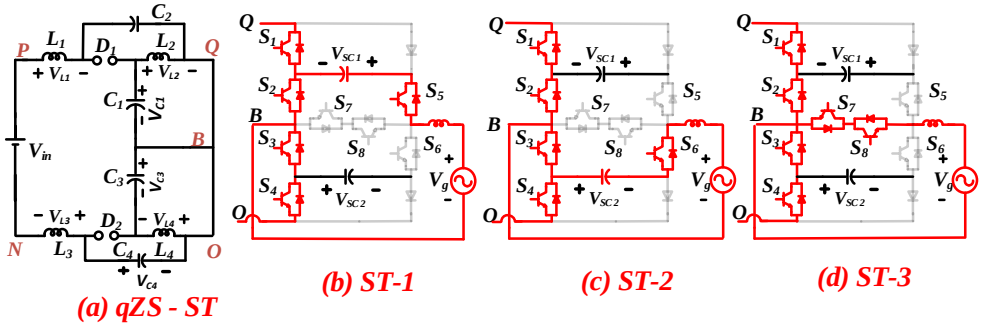

Fig. 6.3. (a) Schematic of qZS network during ST states (b-d) Schematic of MLI during ST-1 to ST-3.

During the Shoot-through state, the voltages across the inductors (L_1-L_4) and the total DC-link voltage (V_{dc}) are expressed as:

$$V_{L1} + V_{L3} = V_{in} + V_{C2} + V_{C4} \tag{6.5}$$

$$V_{L2} = V_{C1} \tag{6.6}$$

$$V_{L4} = -V_{C3} \tag{6.7}$$

$$V_{dc} = V_{dc1} + V_{dc2} = 0 \tag{6.8}$$

6.3 Modulation Technique

6.3.1 Proposed modulation technique for qSB-5LI

For the proposed topology, the level-shifted PWM technique is implemented to perform the following operations: (i) boost the input PV voltage and (ii) five-level output voltage inversion. From Fig. 6.4(a) it may be noticed that the modulating signal 'V_m' is compared with the carriers C_1- C_4 to produce the level-generating signals S_{11}-S_{44} and S_5-S_8. Further, to generate shoot-through pulses 'Sh_1 and Sh_2', two DC reference signals 'V_{sh1} and V_{sh2}' are compared with carriers 'C_4'and 'C_1'.Moreover, the modulation signal 'V_m' is divided into four equal zones 'z_1,z_2,z_3, *and* z_4'. To implement boosting, logical operations are performed between the shoot-through pulses 'Sh_1 and Sh_2' and level-generating pulses 'S_{11}-

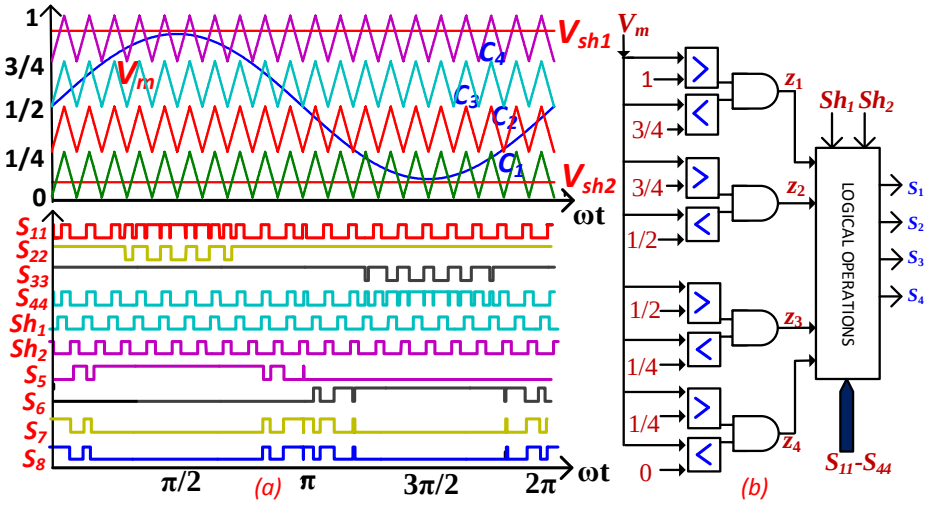

Fig. 6.4. Implementation of the modulation technique.

S_{44}' based on the zone of operation as shown in Fig. 6.4(b). Finally, the desired PWM signals 'S_1-S_4' is obtained from the logical operations and are fed to the power converter.

Fig. 6.5 presents the switching states of the power converter during the positive and negative half-cycles of the output voltage waveform. As shown in Fig. 6.5(a) the modulation signal 'V_m' is compared to carrier 'C_3' to generate voltage levels 0 and 0.5V. It may be observed that the DC reference signal (V_{sh2}) is incremented by 'D' (where *'D'* is defined as the ratio of shoot-through time and sample time) and is compared with carrier 'C_1' to insert a shoot-through pulse in 'S_1' and 'S_4'.From Fig. 6.5(a) it is evident that the shoot-through duty ratio 'D' is scaled up by a factor of 4 (shown in red color) by the level-shifted PWM. The implementation of shoot-through in voltage level 0.5V to V is shown in Fig. 6.5(b). In contrast to Fig 6.5(a), the shoot-through is generated by a decrement of the DC-reference (V_{sh1}) by D. The DC-reference signal (V_{sh1}) is compared with carrier 'C_4' to insert shoot-through pulse in 'S_1' and 'S_4'. A similar conclusion can be drawn from Fig. 6.5(c) and Fig. 6.5(d), where V_{sh1} and V_{sh2} are utilized to insert shoot-through in voltage levels from (0 to -0.5V) and (-0.5V to -V).

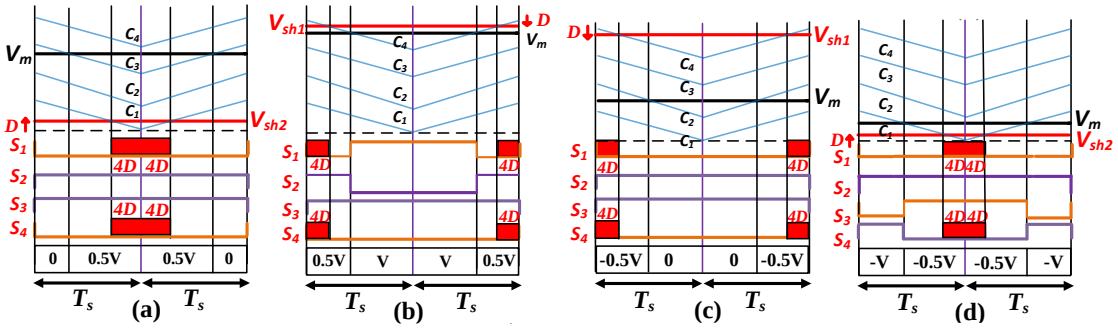

Fig. 6.5. Generation of switching states in positive and negative half cycles.

6.3.2 Analysis of the Boost Factor

To derive the boost factor of the power converter, volt-second balance is applied to inductor voltage equations during non-shoot-through (equations 6.1-6.3) and shoot-through states (equations 6.5-6.7).

From the volt-sec balance, the voltage across the qZS capacitors is expressed as:

$$V_{C1}=V_{C3} = V_{in} \tag{6.9}$$

$$V_{C2}=V_{C4} = \frac{(4D)}{(1-4D)} V_{in} \tag{6.10}$$

Where the shoot-through duty ratio (*D*) is defined as the ratio of shoot-through time (T_{sh}) and sample time (T_s).

The total DC-link voltage (V_{dc}) of the power configuration during the *NST* state is expressed as:

$$V_{dc} = V_{dc1} + V_{dc2} = V_{c1} + V_{c2} + V_{c3} + V_{c4} = \frac{2}{(1-4D)} V_{in} \tag{6.11}$$

6.4 Proposed closed-loop control schemes for qSB-5LI

To facilitate an easy reference, the controllers for stand-alone and grid-connected modes are reproduced from the earlier chapter.

6.4.1 Stand-alone mode

The primary goal of the power configuration in stand-alone mode is to maintain the output voltage at its rated value against load and source disturbances. To this end, the closed-loop control scheme (shown in Fig. 6.6(a)) is implemented to regulate the output voltage at the desired RMS value. In general, the output voltage of the inverter ($m.V_{dc}$) is controlled by regulating the total DC-link voltage ($V_{dc} = V_{dc1} + V_{dc2}$) at a constant value of the modulation index. It may be noticed that the DC-link voltage pulsates from a value of zero to the boosted DC voltage as a consequence of inserting the shoot-through mode of operation using the inverter switches (S_1-S_4). As the direct measurement of DC-link voltage is not feasible, it is estimated with an indirect measurement as shown in Fig. 6.6(a).As shown in the figure the total DC-link voltage 'V_{dc}' is estimated by sensing the voltage across the capactors 'V_{c1}, V_{c3}' and shoot-through duty ratio '*D*'.

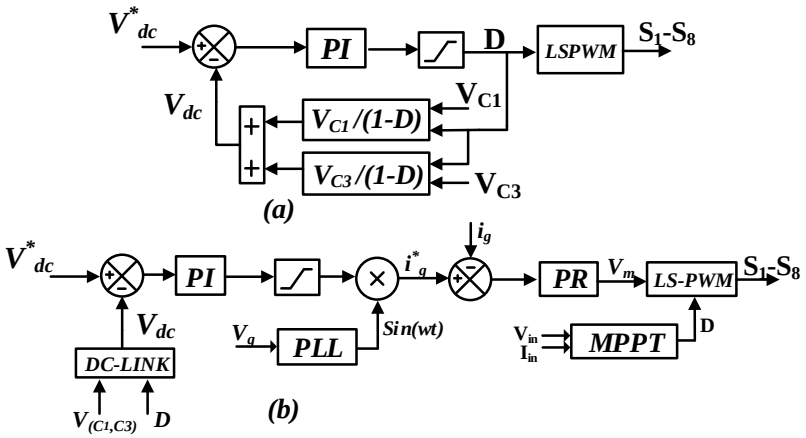

Fig. 6.6. (a) Control strategy for stand-alone mode and (b) Control strategy for a grid-connection mode of operation.

The error generated by the comparison of V_{dc}^{*} and V_{dc} is compensated by the PI controller.The PI controller generates a DC signal, corresponding to the duty ratio '*D*', which in turn determines the shoot-through DC-reference signals '$V_{sh1,}$ V_{sh2}', which are needed to implement the *LSPWM*. These DC-reference signals are compared with carrier signals 'C_1, C_4' to generate the shoot-through signals 'Sh_1 and *Sh2'* (as discussed in section III (a)).

6.4.2 Grid-connected mode

The closed-loop control scheme for the grid-connection mode of operation is presented in Fig. 6.6(b). This scheme enables the controller to inject active power into the grid. In this control scheme, an outer voltage loop is employed to control the DC-link voltage, while an inner current loop injects current into the grid. Further, an independent MPPT control is implemented to extract the peak power from the PV source.

The *perturb & observe* (*P&O*) MPPT algorithm is employed to track the peak power of the PV source. Both PV voltage (V_{in}) and current (I_{in}) are sensed and are input to the *P&O* algorithm. The algorithm generates the required shoot-through (*ST*) duty ratio '*D*' to track the maximum power point of the PV source. The change in duty ratio 'D' results in the change in the total DC-link voltage 'V_{dc}' of the 5-level inverter. The assessed DC-link voltage 'V_{dc}' is compared with the reference DC-link voltage (V^{*}_{dc}) and the produced error is compensated by the output loop PI controller. The PI controller generates the current reference (i^{*}_{g}), which is in sync with the grid employing a PLL. The difference in the current reference (i^{*}_{g}) and the actual grid current is compensated by a PR controller by varying the modulation signal (v_m). The change in modulation signal (v_m) results in a change in the current inigjected into the grid

[86], [88]. Thus, in the grid-connection mode, both degrees of freedom offered by the power converter namely, the shoot-through duty ratio (D) and the modulation index (m) are effectively utilized to realize the objectives of MPPT and injection of current into the grid respectively.

6.5 Reduction of Leakage current

Transformerless inverter configurations are widely reported in the literature for grid-connection applications. They offer advantages such as higher power density, and higher efficiency. However, the elimination of the transformer results in the flow of leakage current, which is highly undesirable. In general, high-frequency voltage variations across the stray capacitance formed due to the grounded frame of the PV panel paves the way to the genesis of the leakage current.

The harmful effects of the leakage current in terms of performance and safety are well documented [90]. The standard *VDE0126-1-1* [10] specifies that the maximum leakage current is restricted to 300mA (RMS). The most popular strategies to minimize/restrict the leakage current include clamping the voltage across the stray capacitance to a constant value or reducing the high-frequency voltage content across it.

This high-frequency voltage content is caused by the common-mode voltage of the multilevel inverter. This calls for the assessment of high-frequency voltage content applied across the stray capacitance. To realize this objective, a common-mode model of the power converter is developed, which is shown in Fig. 6.7(a). Further, the common-mode voltage is resolved into the common-mode and the differential mode components as shown in Fig 6.7(b).

From Fig. 6.7(b) the parasitic voltage (v_{cp}) across the PV capacitor is determined by the following expression:

$$v_{cp} = v_{L3} + v_{C4} + v_{tcmv} \tag{6.12}$$

Where the effective common mode voltage is defined as $v_{tcmv} = v_{cmv} - 0.5v_{dm}$

The sum of inductor and capacitor voltages '$v_{L3} + v_{C4}$' during the non-shoot-through (NST) and shoot-through (ST) states are stated as:

$$v_{L3} + v_{C4} = \frac{-(1+4D)}{4} V_{dc} \quad \text{for the } NST \text{ state} \tag{6.13}$$

$$v_{L3} + v_{C4} = \frac{(1-4D)}{4} V_{dc} \quad \text{for the } ST \text{ state} \tag{6.14}$$

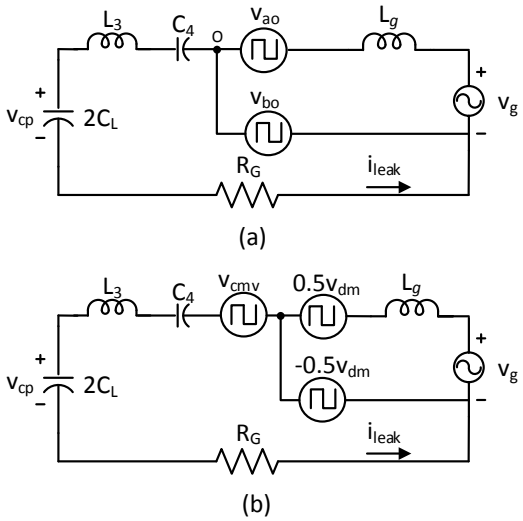

Fig. 6.7 (a) Common-mode model of qSC-5LI (b) Simplified common-mode model.

The pole voltages (v_{AO},v_{BO}), effective common mode voltage (v_{tcmv}), the sum of voltages $v_{L3} + v_{C4}$ and the parasitic voltage across the PV capacitor (v_{cp}) during *ST* and *NST* states are shown in Table 6.2. For example, the 'v_{cp}' is calculated for a shoot-through duty ratio of 0.1. It may be observed that, the 'v_{cp}' remains to be constant at a value of $0.15V_{dc}$ for both *ST* and *NST* states. As the parasitic voltage 'v_{cp}' across the PV capacitor remains constant, the leakage current which flows from the PV source to the grid is minimized.

TABLE 6.2 PARASITIC VOLTAGE OF THE POWER CONFIGURATION FOR D=0.1.

State-type	v_{AB}	v_{AO}	v_{BO}	v_{tcmv}	$v_{L3} + v_{C4}$	v_{cp}
NST-1	V_{dc}	$1.5V_{dc}$	$0.5V_{dc}$	$0.5V_{dc}$	$-0.35V_{dc}$	$0.15V_{dc}$
NST-2	$0.5V_{dc}$	V_{dc}	$0.5V_{dc}$	$0.5V_{dc}$	$-0.35V_{dc}$	$0.15V_{dc}$
NST-3	0	$0.5V_{dc}$	$0.5V_{dc}$	$0.5V_{dc}$	$-0.35V_{dc}$	$0.15V_{dc}$
NST-4	$-0.5V_{dc}$	0	$0.5V_{dc}$	$0.5V_{dc}$	$-0.35V_{dc}$	$0.15V_{dc}$
NST-5	$-V_{dc}$	$-0.5V_{dc}$	$0.5V_{dc}$	$0.5V_{dc}$	$-0.35V_{dc}$	$0.15V_{dc}$
ST-1	$0.5V_{dc}$	$0.5\ V_{dc}$	0	0	$0.15V_{dc}$	$0.15V_{dc}$
ST-2	$-0.5V_{dc}$	$-0.5\ V_{dc}$	0	0	$0.15V_{dc}$	$0.15V_{dc}$
ST-3	0	0	0	0	$0.15V_{dc}$	$0.15V_{dc}$

6.6 Reduction of Leakage Current

The operating principles of the proposed power configuration are validated with a scaled-down prototype which is shown in Fig .A.1. A programmable DC power supply is utilized to replicate the CC-CV behavior of the PV panel and FPGA (Spartan-6) is utilized to output the gating pulses for the power converter. Table 6.3 displays the hardware specifications as well as the experiment's operational settings. In this experimental setup, an input voltage (V_{in}) of

TABLE 6.3 OPERATING PARAMETERS OF HARDWARE PROTOTYPE

Operational conditions	**Values**	**Components**	**Values**
Input voltage (V_{in})	70V	EE65CORE Inductors	3mH
Total DC-link voltage	200V	Capacitors (C_1-C_4)	300V,1300µF
Switching frequency	20kHz	Switched capacitors (SC_1, SC_2)	200V,400 µF
Output voltage(RMS)	110V	Fast recovery diode	MUR1560CT
Modulation Index (m)	0.8	MOSFETs	IRFP460
Output Power (P_o)	400W	PV capacitor (C_p)	100nF

70V is applied across the qZS networks to acquire the output voltage of 110 V (RMS). However, this input voltage (70V) is not adequate to achieve 110 V (RMS). Therefore, the input voltage (V_{in}) is boosted to obtain the required magnitude, by inserting an ST duty ratio of 0.08, which realizes a boost factor of 2.83 (Eqn. 6.11).

The experimental waveforms of the input voltage (V_{in}) and the boosted DC-link voltages (V_{dc1} & V_{dc2}) of the qSC-LI are shown in Fig. 6.8. It may be noticed that the DC-link voltage (V_{dc1} & V_{dc2}), are pulsating waveforms which switch between the voltage levels of 100 V during the *NST* state and 0 V during the *ST* state. Thus, the total DC-link is boosted to 200V (i.e. $V_{dc} = V_{dc1} + V_{dc2}$) indicating that a boost factor of 2.83 is obtained. Further, the last two traces of Fig. 9 present the output voltage (V_{AB}) and the load current (i_{load}). It may be noticed that the output voltage has 5 distinct voltage levels namely 0V, ±100V, and ±200V. The zoomed view of Fig. 9 clearly shows the voltage transitions in the DC-link voltages and output voltage of the power converter.

Fig. 6.9 presents the inductor current (i_{L1}) and capacitor voltages (V_{c1} & V_{c2}) of the top quasi-z-source network-1 of the power converter (Fig. 6.1). Theoretically, in qZS -1 the boosted DC-link voltage (V_{dc1}), is distributed in the ratio (1-4D: 4D) across the quasi-z-source capacitors 'C_1' and 'C_2'. It may be noted from Fig. 6.9 that the capacitors 'C_1' and 'C_2' respectively support the voltages 70V and 30V, which add up to the total DC-link voltage (V_{dc1}) of 100V. The experimental values are in close agreement with the theoretical values of 68V and 32V. Further, the last trace shows the rise and fall of the inductor current (i_{L1}) during the shoot-through and the non-shoot-through modes of operation.

The input voltage (V_{in1}), the DC-link voltage $V_{dc1,}$ and the voltage across the switched capacitors (V_{SC1} and V_{SC2} are presented in Fig. 6.10. In the proposed power converter, both

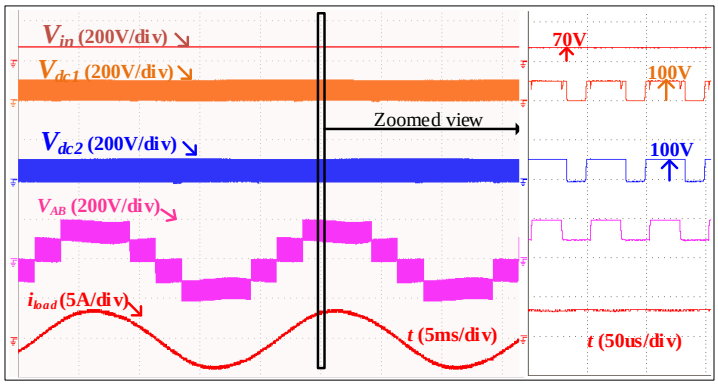

Fig. 6.8. Input voltage (V_{in}), DC-link voltages (V_{dc1} & V_{dc2}), Output voltage (V_{AB}), and load current (i_{load}) of the qSC-5LI.

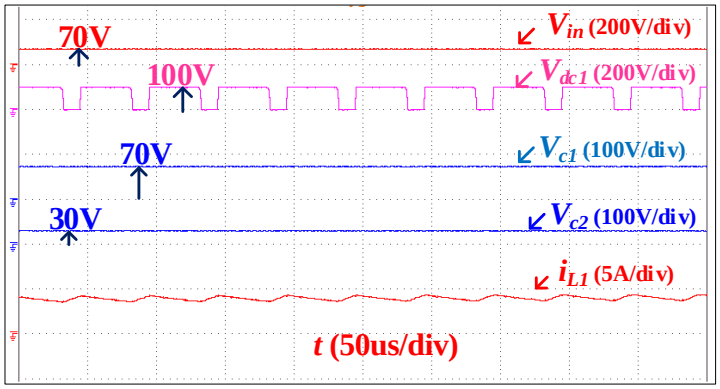

Fig. 6.9. Input voltage (V_{in}), DC-link voltage (V_{dc1}), capacitor voltages (V_{c1}, V_{c2}), and inductor current (i_{L1}) of the qSC-5LI.

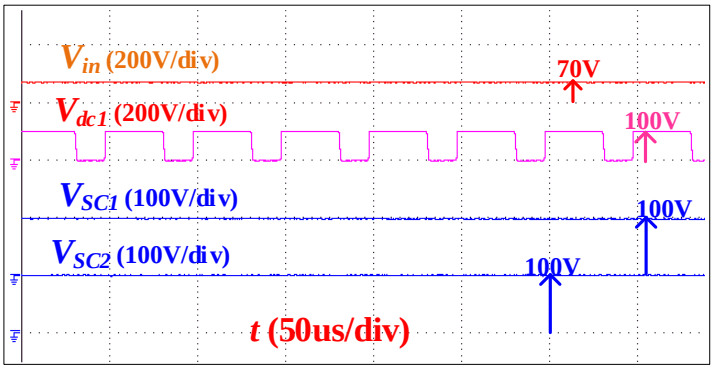

Fig. 6.10. Input voltage (V_{in1}), DC-link voltage (V_{dc1}) and switched capacitor voltages (V_{SC1}, V_{SC2}) of the qSC-5LI.

switched capacitors (SC_1, SC_2) are charged to half the total DC-link voltage to obtain the five-level output voltage waveform. It may be observed that the switched capacitors are charged to 100V each which is half of the total DC link voltage of 200V. The experimentally obtained parasitic voltage (V_{cp}) and the leakage current (i_{leak}) are shown in Fig. 6.11. It may be observed that the parasitic voltage is constant at 31V with only the switching frequency ripple present in it. It is evident that the induced leakage current is minimized due to the absence of high-frequency voltage transitions in 'V_{cp}'. The experimentally measured leakage current is 8.1mA (RMS), which falls within the standard VDE0126-1-1 limit of 300mA (RMS) [10].

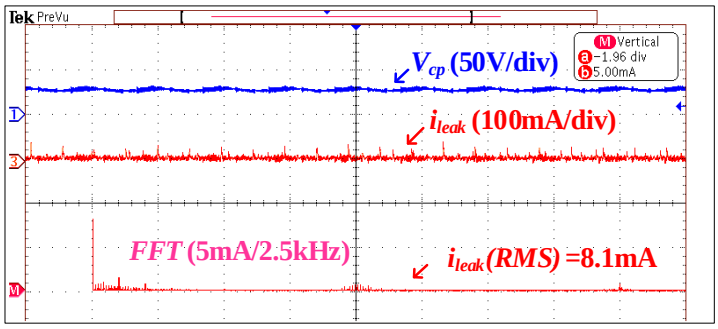

Fig. 6.11. PV capacitor voltage (V_{cp}) and leakage current (i_{leak}) of the qSB-5LI.

Fig. 6.12 depicts the dynamic response of the power converter in the stand-alone mode of operation against the load disturbance. In this experiment, both the DC-link voltages (V_{dc1}&V_{dc2}) of the power converter, are regulated at 100V (peak) to generate an output voltage of 110V (RMS). Initially, the power converter is loaded to 1.4 A, which is half of its full-load value. When the converter is suddenly loaded to its rated value of load current (2.82 A), the DC-link voltages (V_{dc1}&V_{dc2}) remain practically unperturbed (Fig. 6.12) due to the control action exerted by the closed-loop controller shown in Fig. 6.6(a). This regulatory action also manifests at the output, as the output voltage of the proposed power converter is solely dependent on the DC-link voltages (V_{dc1}&V_{dc2}).

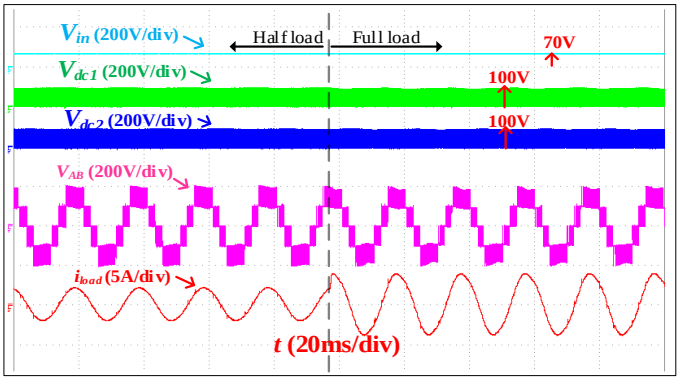

Fig. 6.12. Input voltage (V_{in}), DC-link voltages (V_{dc1} & V_{dc2}), output voltage (V_{AB}) and load current (i_{load}) during load disturbance.

The dynamic response of the proposed topology to source disturbances is shown in Fig. 6.13. In the experimental result presented in Fig. 6.13, the input voltage (V_{in}) is initially maintained at 70V with a total DC-link voltage of 200V (i.e. 100 V per each qZS) and a quick disturbance of 30 V is created in the supply voltage. From Fig. 6.13, it may be observed that both DC-links (V_{dc1}&V_{dc2}) are maintained at 100V irrespective of the changes in the supply voltage. Thus, it is experimentally verified that the closed-loop controller shown in Fig. 6.6(a) is capable of regulating the DC-link voltages against the supply disturbances as well.

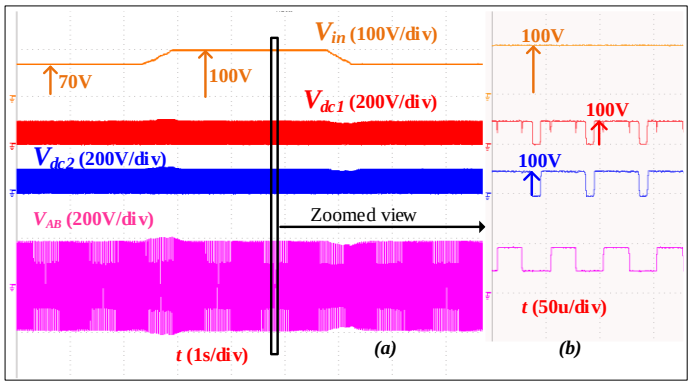

Fig. 6.13. Input voltages (V_{in1}) and DC-link voltages (V_{dc1} & V_{dc2}) and output voltage (V_{AB}) (b) Zoom-in view of the plot (a).

Fig. 6.14 presents the experimental result pertaining to the grid-connection mode of operation. In this mode, the controller shown in Fig. 6.6(b) is employed. Initially, the active power of 250W is injected into the grid by the controller. As mentioned in section V, the controller dynamically adjusts the value of the shoot-through duty ratio '*D*' based on the insolation level on PV panels. As the insolation of the PV panel increases the output power injected into the grid also increases. When a quick increase of the shoot-through duty ratio 'D' is introduced (which follows an increase in the insolation level), the input current (I_{in}, third trace) is correspondingly increased from 2.7A to 4A (RMS), in turn increasing the DC-link voltages. The outer loop PI controller (Fig. 6.6(b)) responds to this disturbance by increasing the reference value of the grid current. The inner current loop's PR controller compensates for the difference between the reference and actual grid current values by increasing the modulation index '*m*'. This increases the grid current thereby increasing the active power pumped into the grid. In consequence, the DC-link voltage automatically returns to its actual value. The corresponding increase of grid current (i_g) is clearly visible in Fig. 6.14 (from 2.26A RMS to 3.39A RMS at UPF).

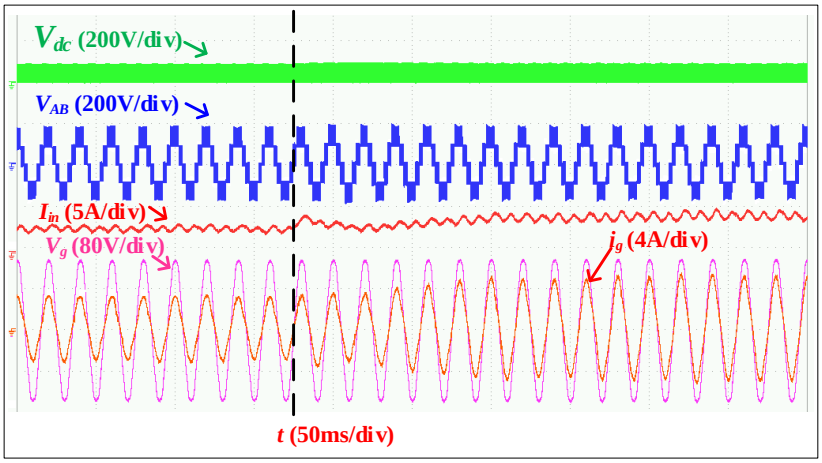

Fig. 6.14. Total DC link voltage (V_{dc}), Inverter output voltage (V_{AB}), input voltage (V_{in}), grid voltage (V_g) and grid current (i_g).

6.7 Comparison between the proposed qSC-5LI and the qZS-based five-level inverter topologies

In this section, the proposed power converter (qSC-5LI) is compared with the previously reported 5-level qZS inverters. In Table 6.4 all of the 5-level qZS inverters are compared in terms of device count, boost factor, voltage stress, voltage THD, and leakage current.

It may be noticed that the proposed qSC-5LI employs an equal number of switches but requires two additional capacitors when compared to the other quasi-z-source topologies. The topology reported in [61] needs fewer inductors when compared to the proposed power converter. However, the input current drawn by this power converter is discontinuous which is not ideal for Photovoltaic applications. It may also be observed that the proposed topology results in a higher boost factor when compared to the other five-level quasi-z-source topologies. The voltage stress across the switches, diode, and capacitors is calculated on a *per-unit* (p.u.) basis. For these computations, the output voltage (RMS) is considered to be the base value. It may be noticed that the proposed topology and converters [54], [59], and [62] have equal voltage stress across the switches and diodes. It may be noted that the quasi-z-source capacitors of the proposed topology are subject to higher voltage stress when compared to the other qZS topologies. However, this may not be a disadvantage as the power converter (qSC-5LI) results in a higher boost factor. As the total switching device count is unequal in the topologies presented in Table 6.4, the Total Standing Voltage (TSV) is calculated [88].

In comparison with topologies [54] and [61] the proposed converter has a minimum TSV value as shown in Table 6.4. Further, the voltage THD and the leakage current of all topologies listed in Table 6.4 are analyzed. It may be noted that the proposed converter registers lower voltage THD when compared to topologies [54], [59], and [62]. The topologies presented in references [54], [59], and [61] do not address the issue of leakage current. Hence, to compare the leakage current, these topologies are simulated with the parasitic capacitor 'C_p' of value 100nF. It may be noted that, when compared to the other four topologies, the proposed power converter has a lower leakage current (10.02 mA).

TABLE 6.4 COMPARISON OF THE QSC-5LI WITH 5-LEVEL QZS MLIS

	qZS-NPC[54]	qCHB-FLBI[59]	Mqzs- 5LI[61]	qZS-5L[62]	qSC-5LI (proposed)
N_{Levels}	Five	Five	Five	Five	Five
$N_{sources}$	One	Two	One	One	One
$N_{inductors}$	Four	Four	Two	Four	Four
$N_{capacitors}$	Four	Four	Four	Four	Six
N_{diodes}	Six	Two	Three	Four	Four
$N_{switches}$	Eight	Eight	Eight	Eight	Eight
Boost	$1/(1-2D)$	$1/(1-2D)$	$2/(1-2D)$	$1/(1-2D)$	$2/(1-4D)$
continuous input current	Yes	Yes	No	Yes	Yes
voltage stress across the capacitor	$1/\sqrt{2}$ (C_1,C_2)	$1/\sqrt{2}$ (C_1,C_2)	$1/\sqrt{2}$ (C_1,C_2)	$1/\sqrt{2}$ (C_1,C_3)	$(1-4D)/\sqrt{2}(1-D)$ (C_1,C_3)
	$\frac{D}{\sqrt{2}(1-D)}$ (C_3,C_4)	$\frac{D}{\sqrt{2}(1-D)}$ (C_3,C_4)	$\frac{D}{\sqrt{2}(1-D)}$ (C_3,C_4)	$\frac{D}{\sqrt{2}(1-D)}$ (C_2,C_4)	$(4D)/\sqrt{2}(1-D)$ (C_2,C_4)
					$\sqrt{2}/(1-D)$ (SC_1, SC_2)
voltage stress across Diode	$\frac{D}{\sqrt{2}(1-D)}$	$\frac{D}{\sqrt{2}(1-D)}$	$\frac{D}{\sqrt{2}(1-D)}$	$\frac{D}{\sqrt{2}(1-D)}$	$\frac{D}{\sqrt{2}(1-D)}$
voltage stress across the Switch	$\frac{D}{\sqrt{2}(1-D)}$	$\frac{D}{\sqrt{2}(1-D)}$	$1/\sqrt{2}(1-D)$ for S_1-S_4	$\frac{D}{\sqrt{2}(1-D)}$	$\frac{D}{\sqrt{2}(1-D)}$
			$\sqrt{2}/(1-D)$for S_5-S_8		
TSV	7	5	7.5	6	6
THD (Voltage)	75.4%	42.73%	38.2%	74.2%	38.2%
Leakage Current	720mA	1.1A	590mA	325mA	10.02mA

6.8 Loss Distribution in qSC-5LI

In this section, the power loss analysis of the proposed power converter has been performed in *Powersim (PSIM)* software to estimate the efficiency. The power converter is simulated by employing the thermal models of the power diode (ISL9R3060G2) and semiconductor switch (MOSFET-IRFP460). The switching losses (P_{sd}, P_{sw}) and conduction (P_{cd}, P_{con}) losses incurred

in the diodes and the switches (S_1-S_8) are evaluated for output power in the range of 0-400W. Further, the ESR losses in the capacitors (P_{cap}) and conduction losses in the inductors (P_{ind}) are estimated using equations given in [77]. From Fig. 6.15 it may be observed that the power converter displays an average efficiency of 95 %. Furthermore, at 400W, the power loss in switches (S_1-S_8) and passive components is depicted in Fig. 6.15.

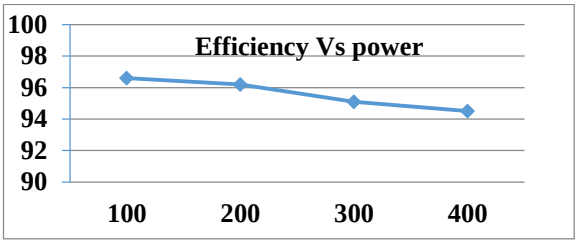

Fig. 6.15. Efficiency curve of qSC-5LI.

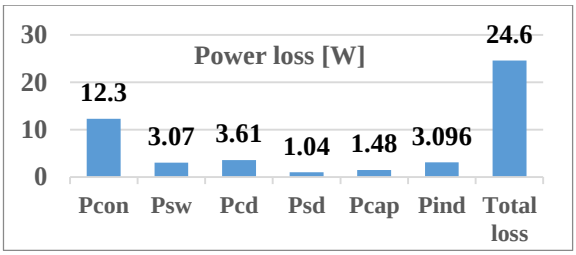

Fig. 6.16. Loss distribution in switches, diodes, inductor, and capacitors at 400W in qSC-5LI.

6.9 Summary

In this chapter, a single-stage quasi-switched capacitor-based five-level inverter (qSC-5LI) is investigated for PV applications. The proposed topology, along with its modulation scheme, simultaneously achieves voltage boosting and five-level operation. The power converter offers a higher boost factor when compared to other quasi-z-source-based five-level topologies in the literature. In addition to this, the proposed topology reduces the leakage current to 8.01mA, which is far lower than the stipulated limit set by the *VDE 0126-1-1* standard (300mA RMS) [10]. In stand-alone mode, a closed-loop DC-link control system is employed to regulate the output voltage by controlling the shoot-through duty ratio '*D*'. It is also shown that in the grid-connection mode of operation, the control is decoupled in that the objective of MPPT is addressed with the shoot-through duty factor while the control of grid current requires that the modulation index be controlled. Finally, experimentation is carried out to evaluate the dynamic performance of the proposed system in both stand-alone and grid-connected modes.

Chapter 7

Conclusion and Future Scope

Chapter 7

Conclusion and Future Scope

7.1 Conclusion

The principal focus of this thesis is to investigate different single-stage quasi- z-source based multilevel inverter configurations for multi-string and single-string Photovoltaic applications. The thesis consists of six chapters of which, the first is introductory and the rest are contributory in nature.

Chapter 2 reviews the available impedance source multilevel configurations in both single- and three-phase and further specifies the major demerits of these topologies. These disadvantages are the impetus to embark on the research problem in this thesis.

Important contributions of this thesis are summarized as follows:

1. A single-stage, qZS-based cascaded four-level inverter with a space-vector modulation technique is presented in Chapter 3. The power converter is a fusion of three quasi-z-source networks and a cascaded four-level inverter. The proposed configuration with the aid of implemented modulation scheme achieves 50% higher voltage boosting in comparison with the conventional qZS-CHB and qZS-NPC topologies. Furthermore, the power converter achieves higher voltage levels, which reduces voltage stress across the switches. It is shown that the output voltage can be controlled in stand-alone mode using shoot-through duty ratio control of qZS networks. Further, the power converter is also capable of injecting power into the grid at UPF.
2. A single-stage qZS-based seven-level inverter is presented in chapter 4. This power converter is a fusion of asymmetrical dual quasi-z-source networks with 7-level cascaded MLI. This power converter achieves boosting and seven-level output voltage waveform with less no of switching devices when compared to existing qZS and ZS-seven level topologies in the literature. Further, with the assistance of the modulation technique and symmetrical LCL filter, the high-frequency transitions across the parasitic capacitor are reduced. This paves the way for the flow of low leakage current and from experimentation, it is shown that the RMS value of the leakage current is well below the German standard DIN VDE 0126-1-1.

3. To remove the asymmetry and to reduce the no of input sources, a seamless 5-level, single-stage qZS-based MLI is presented in chapter 5. In this power converter, a single DC source is interfaced to two symmetrical quasi-Z-sources networks which are amalgamated with a five-level hybrid inverter. The power converter employs only six semiconductor switches to simultaneously achieve boosting and 5-level output voltage inversion.The proposed topology employs fewer semiconductor devices in comparison with the existing qZS-based five-level inverters in the literature. With the aid of a modified level-shifted PWM scheme and LCL filter the power converter minimizes the leakage current to less than 300mA. Further, the performance of the closed-loop operation of the proposed topology in stand-alone mode and grid-tied mode is assessed and validated with hardware experimentation.
4. To improve the boosting capability and achieve less voltage THD output voltage waveform a single-stage 5-level qZS based switched capacitor MLI is proposed in chapter 6. The proposed power converter comprises dual quasi-z-source (qZS) networks and switched capacitor based 5-level inverter with a single PV source. The power converter achieves higher voltage boosting with the modified LSPWM scheme. Further, the power converter minimizes the high-frequency oscillation across the parasitic capacitor of the PV panel without any additional requirement of a filter. This minimizes the leakage current to be less than 300mA complying with the VDE0126-1-1 standards. The principle of the proposed topology is verified with an experimental prototype in both stand-alone and grid-connection modes of operation.

7.2 Future Scope

Based on the research done in this thesis, the recommendations for future work are as follows:

i) Investigation on high-frequency transformer-based impedance networks with new MLI topologies for PV-grid connected system.

ii) Further investigation on quasi-switched capacitor-based MLI topologies with less component count and leakage current minimization.

iii)As shoot-through implementation in the switching cycle results in additional switching losses, it would be an interesting proposition to implement soft switching to improve efficiency.

iv) Implementation of advanced predictive algorithms and advanced control schemes at various platforms for efficient tracking in PV systems.

Appendix-I

Description of the Experimental Prototype

Figure A.1 presents the photograph of the experimental prototype, which was developed to validate the proposed qZS based multilevel inverter configurations in this thesis.

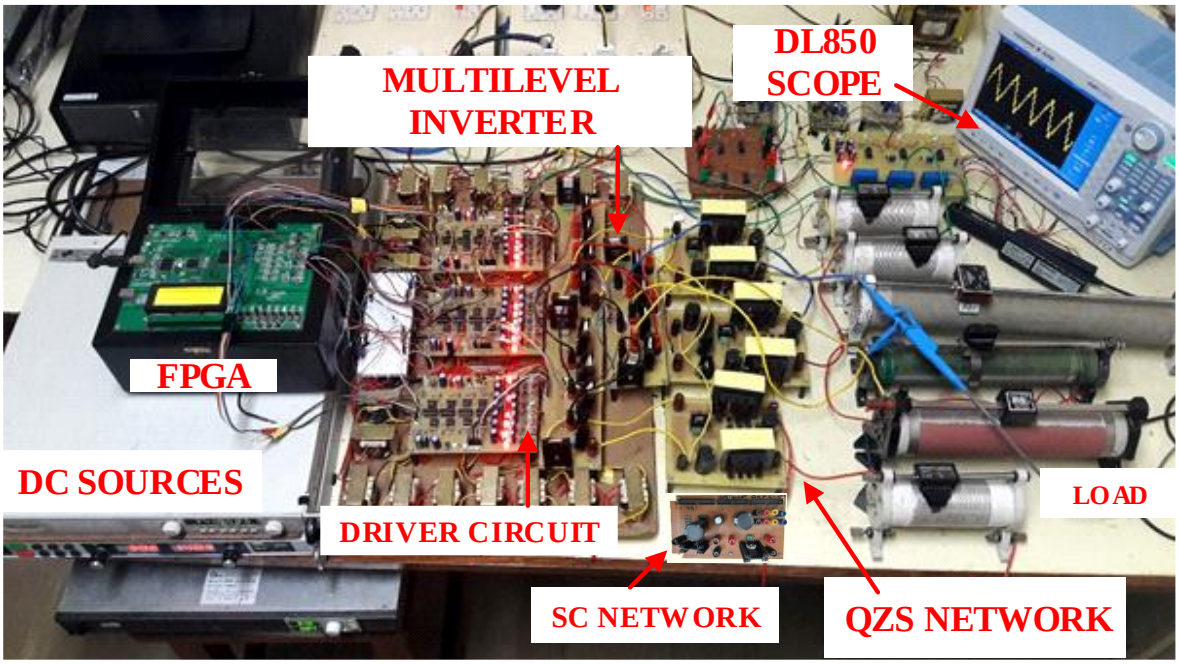

Fig. A.1: A view of the fabricated laboratory prototype

References

[1] RENEWABLES 2021 GLOBAL STATUS REPORT

[2] Indian Renewable Energy Industry Report (November, 2021), https://www.ibef.org/industry/renewableenergy.aspx

[3] Kim, Yong Sin, and Roland Winston. "Power conversion in concentrating photovoltaic systems: central, string, and micro-inverters." Progress in Photovoltaics: Research and Applications 22, no. 9 (2014): 984-992.

[4] S. B. Kjaer, J. K. Pedersen and F. Blaabjerg, "A review of single-phase grid-connected inverters for photovoltaic modules," in IEEE Transactions on Industry Applications, vol. 41, no. 5, pp. 1292-1306, Sept.-Oct. 2005, doi: 10.1109/TIA.2005.853371.

[5] K. Alluhaybi, I. Batarseh and H. Hu, "Comprehensive Review and Comparison of Single-Phase Grid-Tied Photovoltaic Microinverters," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 8, no. 2, pp. 1310-1329, June 2020, doi: 10.1109/JESTPE.2019.2900413.

[6] Y. Zhou and H. Li, "Analysis and Suppression of Leakage Current in Cascaded-Multilevel-Inverter-Based PV Systems," in IEEE Transactions on Power Electronics, vol. 29, no. 10, pp. 5265-5277, Oct. 2014, doi:10.1109/TPEL.2013.2289939.

[7] D. Meneses, F. Blaabjerg, Ó. García and J. A. Cobos, "Review and Comparison of Step-Up Transformerless Topologies for Photovoltaic AC-Module Application," in IEEE Transactions on Power Electronics, vol. 28, no. 6, pp. 2649-2663, June 2013, doi: 10.1109/TPEL.2012.2227820.

[8] M. N. H. Khan, M. Forouzesh, Y. P. Siwakoti, L. Li, T. Kerekes and F. Blaabjerg, "Transformerless Inverter Topologies for Single-Phase Photovoltaic Systems: A Comparative Review," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 8, no. 1, pp. 805-835, March 2020, doi: 10.1109/JESTPE.2019.2908672.

[9] Hernández, J. C., P. G. Vidal, and A. J. R. E. Medina. "Characterization of the insulation and leakage currents of PV generators: Relevance for human safety." Renewable Energy 35, no. 3 (2010): 593-601.

[10] W. Li, Y. Gu, H. Luo, W. Cui, X. He and C. Xia, "Topology Review and Derivation Methodology of Single-Phase Transformerless Photovoltaic Inverters for Leakage Current Suppression," in IEEE Transactions on Industrial Electronics, vol. 62, no. 7, pp. 4537-4551, July 2015.

[11] F. Akbar, H. Cha, H. F. Ahmed and A. A. Khan, "A Family of Single-Stage High-Gain Dual-Buck Split-Source Inverters," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 2, pp. 1701-1713, June 2020, doi: 10.1109/JESTPE.2019.2894384.

[12] F. Z. Peng, "Z-source inverter," IEEE Transactions on Industry Applications, vol. 39, no. 2, pp.504–510, Mar. 2003, doi: 10.1109/TIA.2003.808920.

[13] Fang Zheng Peng et al., "Z-source inverter for motor drives," in IEEE Transactions on Power Electronics, vol. 20, no. 4, pp. 857-863, July 2005.

[14] J. Anderson and F. Z. Peng, "A Class of Quasi-Z-Source Inverters," 2008 IEEE Industry Applications Society Annual Meeting, Edmonton, AB, pp. 1-7, 2008.

[15] Sahoo, Sarat Kumar, Sukruedee Sukchai, and Franco Fernando Yanine. "Review and comparative study of single-stage inverters for a PV system." Renewable and Sustainable Energy Reviews 91 (2018): 962-986.

[16] Automatic Disconnection Device Between a Generator and the Public Low-Voltage Grid, DIN VDE V 0126-1-1, 2006.

[17] Islam, Monirul, Saad Mekhilef, and Mahamudul Hasan. "Single phase transformerless inverter topologies for grid-tied photovoltaic system: A review." Renewable and Sustainable Energy Reviews 45 (2015): 69-86.

[18] Figueira, Henrique Horst, et al. "Brazilian grid-connected photovoltaic inverters standards: A comparison with IEC and IEEE." 2015 IEEE 24th International Symposium on Industrial Electronics (ISIE). IEEE, 2015.

[19] Schwartfeger, Luke, et al. "Review of distributed generation interconnection standards." EEA Conference & Exhibition. 2014.

[20] I. Jamal, M. F. Elmorshedy, S. M. Dabour, E. M. Rashad, W. Xu and D. J. Almakhles, "A Comprehensive Review of Grid-Connected PV Systems Based on Impedance Source Inverter," in IEEE Access, vol. 10, pp. 89101-89123, 2022.

[21] P. C. Loh, F. Gao, and F. Blaabjerg, ‘‘Embedded EZ-source inverters,’’IEEE Trans. Ind. Appl., vol. 46, no. 1, pp. 256–267, Jan. 2010.

[22] Y. P. Siwakoti, F. Z. Peng, F. Blaabjerg, P. C. Loh, and G. E. Town, ‘‘Impedance-source networks for electric power conversion. Part II:A topological review,’’ IEEE Trans. Power Electron., vol. 30, no. 2,pp. 699–716, Mar. 2015.

[23] M. Chuang and L. Hong, ‘‘Research on photovoltaic grid-connected control of Z source inverter based on active disturbance rejection technology,’’ in Proc. IEEE 4th Adv. Inf. Technol., Electron. Automat. ControlConf. (IAEAC), Dec. 2019, vol. 6, no. 2, pp. 2648–2652

[24] N. Subhani, R. Kannan, A. Mahmud, and F. Bleiberg, ‘‘Z-source inverter topologies with switched Z-impedance networks: A review,’’ IET Power Electron., vol. 14, no. 4, pp. 1–24, Sep. 2020, doi: 10.1049/pel2.12064.

[25] M. Hasan, B. Nozadian, E. Babies, S. H. Hosseini, and E. S. As,‘‘Switched Z-source networks: A review,’’ IET Power Electron., vol. 12,no. 7, pp. 1616–1633, Feb. 2019.

[26] T. Li and Q. Cheng, ‘‘A comparative study of Z-source inverter and enhanced topologies,’’ CES Trans. Electr. Mach. Syst., vol. 2, no. 3,pp. 284–288, Sep. 2018.

[27] Y. P. Siwakoti, P. C. Loh, F. Blaabjerg, and G. E. Town, ‘‘Y-source impedance network,’’ IEEE Trans. Power Electron., vol. 29, no. 7, pp. 3250–3254, Jul. 2014.

[28] A. H. Rajaei, S. Kaboli, and A. Emadi, ‘‘Sliding-mode control of Z-source inverter,’’ in Proc. 34th Annu. Conf. IEEE Ind. Electron., Nov. 2008, pp. 947–952.

[29] W. Qian, F. Z. Peng, and H. Cha, ‘‘Trans-Z-source inverters,’’ IEEE Trans. Power Electron., vol. 26, no. 12, pp. 3453–3463, Dec. 2011.

[30] T. Li and Q. Cheng, ‘‘A comparative study of Z-source inverter and enhanced topologies,’’ CES Trans. Electr. Mach. Syst., vol. 2, no. 3,pp. 284–288, Sep. 2018.

[31] Y. P. Siwakoti, P. C. Loh, F. Blaabjerg, and G. E. Town, ‘‘Y-source impedance network,’’ IEEE Trans. Power Electron., vol. 29, no. 7,pp. 3250–3254, Jul. 2014

[32] M. Adamowicz, R. Strzelecki, F. Z. Peng, J. Guzinski, and H. A. Rub,‘‘New type LCCT-Z-source inverters,’’ in Proc. EPE, Sep. 2011, pp. 1–10.

[33] R. H. Baker and L. H. Bannister, “Electric power converter,” U.S. Patent3 867 643, 1975.

[34] R. H. Baker, “Switching circuit,” U.S.Patent 4210826, 1980.

[35] T. A. Meynard and H. Foch, “Multi-level conversion: High voltage choppers and voltage-source inverters,” in Proc. IEEE Power Electron. Spec. Conf., 1992, pp. 397–403.

[36] J. P. Lavieville, P. Carrere, and T. Meynard, “Electronic circuit for converting electrical energy and a power supply installation making use thereof,” U.S. Patent 5 668 711, 1997.

[37] K. Zeb et al., “A comprehensive review on inverter topologies and control strategies for grid-connected photovoltaic system,” Renewable and Sustainable Energy Reviews, vol. 94. Elsevier Ltd, pp. 1120–1141, Oct. 01, 2018. doi: 10.1016/j.rser.2018.06.053.

[38] S. Busquets-Monge, J. Rocabert, P. Rodriguez, S. Alepuz and J. Bordonau, "Multilevel Diode-Clamped Converter for Photovoltaic Generators With Independent Voltage Control of Each Solar Array," in IEEE Transactions on Industrial Electronics, vol. 55, no. 7, pp. 2713-2723, July 2008.

[39] P. K. Kar, A. Priyadarshi, S. B. Karanki and A. Ruderman, "Voltage and Current THD Minimization of a Single-phase Multilevel Inverter with an Arbitrary RL-load Using a Time-domain Approach," in IEEE Journal of Emerging and Selected Topics in Power Electronics, doi: 10.1109/JESTPE.2021.3050787.

[40] P. C. Loh, F. Blaabjerg and C. P. Wong, "Comparative Evaluation of Pulsewidth Modulation Strategies for Z-Source Neutral-Point-Clamped Inverter," in IEEE Transactions on Power Electronics, vol. 22, no. 3, pp. 1005-1013, May 2007.

[41] P. C. Loh, F. Gao, F. Blaabjerg, S. Y. C. Feng and K. N. J. Soon, "Pulsewidth-Modulated Z-Source Neutral-Point-Clamped Inverter," in IEEE Transactions on Industry Applications, vol. 43, no. 5, pp. 1295-1308, Sept.-Oct. 2007.

[42] P. C. Loh, S. W. Lim, F. Gao and F. Blaabjerg, "Three-Level Z-Source Inverters Using a Single LC Impedance Network," in IEEE Transactions on Power Electronics, vol. 22, no. 2, pp. 706-711, March 2007.

[43] S. M. Dehghan, M. Mohamadian, A. Yazdian and F. Ashrafzadeh, "Dual-input dual-output z-source inverter," 2009 IEEE Energy Conversion Congress and Exposition, USA, pp. 3668-3674, 2009.

[44] O. Husev, C. Roncero-Clemente, E. Romero-Cadaval, D. Vinnikov and T. Jalakas, Threelevel three-phase quasi Z-source neutral-point-clamped inverter with novel modulation technique for photovoltaic application, Electr. Power Syst. Res. 130 (2016) 10–21.

[45] C. Qin, C. Zhang, A. Chen, X. Xing and G. Zhang, "A Space Vector Modulation Scheme of the Quasi-Z-Source Three-Level T-Type Inverter for Common-Mode Voltage Reduction," in IEEE Transactions on Industrial Electronics, vol. 65, no. 10, pp. 8340-8350, Oct. 2018.

[46] S. K. Chattopadhyay and C. Chakraborty, "Three-Phase Hybrid Cascaded Multilevel Inverter Using Topological Modules With 1:7 Ratio of Asymmetry," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 6, no. 4, pp. 2302-2314, Dec. 2018

[47] Q. Huang and A. Q. Huang, "Feedforward Proportional Carrier-Based PWM for Cascaded H-Bridge PV Inverter," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 6, no. 4, pp. 2192-2205, Dec. 2018.

[48] T. Zhao et al., "Harmonic Compensation Strategy for Extending the Operating Range of Cascaded H-Bridge PV Inverter," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 8, no. 2, pp. 1341-1350, June 2020.

[49] Dongsen Sun, Baoming Ge, F. Z. Peng, A. R. Haitham, Daqiang Bi and Yushan Liu, "A new grid-connected PV system based on cascaded H-bridge quasi-Z-source inverter," 2012 IEEE International Symposium on Industrial Electronics, Hangzhou, pp. 951-956, 2012.

[50] Y. Zhou, L. Liu and H. Li, "A High-Performance Photovoltaic Module-Integrated Converter (MIC) Based on Cascaded Quasi-Z-Source Inverters (qZSI) Using eGaN FETs," in IEEE Transactions on Power Electronics, vol. 28, no. 6, pp. 2727-2738, June 2013.

[51] Y. Liu, B. Ge, H. Abu-Rub and F. Z. Peng, "An Effective Control Method for Three-Phase Quasi-Z-Source Cascaded Multilevel Inverter Based Grid-Tie Photovoltaic Power System," in IEEE Transactions on Industrial Electronics, vol. 61, no. 12, pp. 6794-6802, Dec. 2014.

[52] Y. Liu, H. Abu-Rub, B. Ge and F. Z. Peng, "An effective control method for quasi-Z-source cascade multilevel three-phase grid-tie photovoltaic power system," 2014 IEEE Applied Power Electronics Conference and Exposition - APEC , Fort Worth, TX, 2014, pp. 1733-1737,2014.

[53] M. R. Banaei, A. R. Dehghanzadeh, E. Salary, H. Khounjahan, and R. Alizadeh, "Z-source-based multilevel inverter with reduction of switches," IET Power Electronics, vol.5, no.3, pp.385-392, May 2012.

[54] O.Husev, C. Roncero-Clemente, E. Romero-Cadaval, D.Vinnikov, and S. Stepenko, "Single phase three-level neutral-point-clamped quasi-Z-source inverter', IET Power Electronics, 8, (1), pp. 1–10, 2015.

[55] P. Roncero-Sanchez, C. Roncero-Clemente, E. Romero-Cadaval,O. Husev, and E. Makovenko, "Control scheme of a three-phase three-level NPC qZ-source inverter with LCL filter for RES applications," in Proc. 42nd Annu. Comf. IEEE Ind. Electron. Soc., 2016, pp. 6540-6547.

[56] S. Bayhan, M. Trabelsi, O. Ellabban, H. Abu-Rub, and R. S. Balog, "A five-level neutral-point-clamped/H-bridge quasi-impedance source inverter for grid-connected PV system," in Proc. 42nd Annu. Conf. IEEE Ind. Electron.Soc., 2015, pp. 2502-2507.

[57] Dongsen Sun, Baoming Ge, F. Z. Peng, A. R. Haitham, Daqiang Bi and Yushan Liu, "A new grid-connected PV system based on cascaded H- bridge quasi-Z-source inverter," 2012 IEEE International Symposium on Industrial Electronics, Hangzhou, pp. 951-956, 2012.

[58] Y. Zhou, L. Liu and H. Li, "A High-Performance Photovoltaic Module-Integrated Converter (MIC) Based on Cascaded Quasi-Z-Source Inverters (qZSI) Using eGaN FETs," in IEEE Transactions on Power Electronics, vol. 28, no. 6, pp. 2727-2738, June 2013.

[59] B. Ge, Y. Liu, H. Abu-Rub and F. Z. Peng, "State-of-Charge Balancing Control for a Battery-Energy-Stored Quasi-Z-Source Cascaded-Multilevel-Inverter-Based Photovoltaic Power System," in IEEE Transactions on Industrial Electronics, vol. 65, no. 3, pp. 2268-2279, March 2018.

[60] Tan-Tai Tran, Minh-Khai Nguyen, "Cascaded five-level quasi-switched-boost inverter for single-phase grid-connected system" IET Power Electron, vol. 10, no. 14, pp.1896-1903, November 2017.

[61] A. Ho and T. Chun, "Single-Phase Modified Quasi-Z-Source Cascaded Hybrid Five-Level Inverter," in IEEE Transactions on Industrial Electronics, vol. 65, no. 6, pp. 5125-5134, June 2018.

[62] C. K. Das, K. Annamalai and S. Veeramraju Tirumala, "A Quasi-Z-Source-Based Five-Level PV Inverter With Leakage Current Reduction," in IEEE Transactions on Industry Applications, vol. 58, no. 1, pp. 400-412, Jan.-Feb. 2022.

[63] X. Guo, "Three-Phase CH7 Inverter With a New Space Vector Modulation to Reduce Leakage Current for Transformerless Photovoltaic Systems," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 5, no. 2, pp. 708-712, June 2017.

[64] W. Li, Y. Wang, J. Hu, H. Yang, C. Li and X. He, "Common-Mode Current Suppression of Transformerless Nested Five-Level Converter With Zero Common-Mode Vectors," in IEEE Transactions on Power Electronics, vol. 34, no. 5, pp. 4249-4258, May 2019.

[65] R. Rahimi, S. Farhangi, B. Farhangi, G. R. Moradi, E. Afshari and F. Blaabjerg, "H8 Inverter to Reduce Leakage Current in Transformerless Three-Phase Grid-Connected Photovoltaic systems," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 6, no. 2, pp. 910-918, June 2018.

[66] N. Noroozi and M. R. Zolghadri, "Three-phase quasi-Z-source inverter with constant common-mode voltage for photovoltaic application," IEEE Trans. Ind. Electron., vol. 65, no. 6, pp. 4790-4798, Jun. 2018

[67] Y. P. Siwakoti and G. E. Town, "Common-mode voltage reduction techniques of three-phase quasi Z-source inverter for AC drives," in Proc. 28th Annu. IEEE Appl. Power Electron. Conf. Exposit. (APEC), Mar. 2013,pp. 2247-2252.

[68] F. Bradaschia, M. C. Cavalcanti, P. E. P. Ferraz, F. A. S. Neves, E. C. dos Santos, and J. H. G. M. da Silva, "Modulation for three-phase transformerless Z-source inverter to reduce leakage currents in photovoltaic systems," IEEE Trans. Ind. Electron., vol. 58, no. 12, pp. 5385-5395, Dec. 2011.

[69] Y. Liu, B. Ge, X. Li and Y. Xue, "Common Mode Voltage Reduction of Single-Phase Quasi-Z-Source Inverter-Based Photovoltaic System," IEEE Access, vol. 7, pp. 154572-154580, 2019.

[70] W. Y. Choi, M. K. Yang, "Transformerless Quasi-Z-Source Inverter to Reduce Leakage Current for Single-Phase Grid-Tied Applications," Electronics, vol. 8, no. 3, pp. 312, March 2019.

[71] M. Meraj, S. Rahman, A. Iqbal and L. Ben-Brahim, "Common Mode Voltage Reduction in a Single-Phase Quasi Z-Source Inverter for Transformerless Grid-Connected Solar PV Applications," in IEEE Journal Emerg. Sel. Topics Power Electron, vol. 7, no. 2, pp. 1352-1363, June 2019.

[72] V. T. Somasekhar, K. Gopakumar, M. R. Baiju, K. K. Mohapatra and L. Umanand, "A multilevel inverter system for an induction motor with open-end windings," in IEEE Transactions on Industrial Electronics, vol. 52, no. 3, pp. 824-836, June 2005.

[73] Joohn-Sheok Kim and Seung-Ki Sul, "A Novel Voltage Modulation Technique of the space vector PWM," The Transactions of the Institute of Electrical Engineers of Japan, vol.116-D, pp. 820-825.

[74] B. Li, X. Tian and H. Zeng, "A grid-connection control scheme of PV system with fluctuant reactive load," 2011 4th International Conference on Electric Utility Deregulation and Restructuring and Power Technologies (DRPT), Weihai, China, pp. 786-790, 2011.

[75] G. Eshwar Gowd, P. C. Sekhar and D. Sreenivasarao, "Real-Time Validation of a Sliding Mode Controller for Closed-Loop Operation of Reduced Switch Count Multilevel Inverters," in IEEE Systems Journal, vol.13, no.1, pp.1042-1051, March 2019.

[76] J. Belanger, P.Venne, and J.N Paquin, "The what, where and why of real-time simulation," Planet Rt., pp.25-29, 2010.

[77] D. Sun et al., "Modeling, Impedance Design, and Efficiency Analysis of Quasi- Z Source Module in Cascaded Multilevel Photovoltaic Power System," in IEEE Transactions on Industrial Electronics, vol. 61, no. 11, pp. 6108-6117, Nov. 2014.

[78] P. Manoj, V.T. Somasekhar, and A. Kirubakaran, "A Space Vector Modulated Quasi-Z-Source Based Four-Level VSI for PV Application," IEEE EEEIC 2019, pp. 1-5, 2019.

[79] S. Jain, R. Karampuri and V. T. Somasekhar, "An Integrated Control Algorithm for a Single-Stage PV Pumping System Using an Open-End Winding Induction Motor," in IEEE Transactions on Industrial Electronics, vol. 63, no. 2, pp. 956-965, Feb. 2016.

[80] S. Jain, S. Dhara and V. Agarwal, "A Voltage-Zone Based Power Management Scheme With Seamless Power Transfer Between PV-Battery for OFF-Grid Stand-Alone System," in IEEE Transactions on Industry Applications, vol. 57, no. 1, pp. 754-763, Feb. 2021.

[81] M. Sahoo and S. Keerthipati, "A three-level LC-switching-based voltage boost NPC inverter," IEEE Trans. Ind. Electron., vol. 64, no.4,pp. 2876-2883, Apr. 2017.

[82] D. Do and M. Nguyen, "Three-Level Quasi-Switched Boost T-Type Inverter: Analysis, PWM Control, and Verification," in IEEE Transactions on Industrial Electronics, vol. 65, no. 10, pp. 8320-8329, Oct. 2018.

[83] M. -K. Nguyen, T. -T. Tran and F. Zare, "An Active Impedance-Source Three-Level T-Type Inverter With Reduced Device Count," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 8, no. 3, pp. 2966-2976, Sept. 2020.

[84] S. Majumdar, B. Mahato and K. C. Jana, "Implementation of an Optimum Reduced Components Multicell Multilevel Inverter (MC-MLI) for Lower Standing Voltage," in IEEE Transactions on Industrial Electronics, vol. 67, no. 4, pp. 2765-2775, April 2020.

[85] G. Escobar, P. R. Martinez-Rodriguez, S. Iturriaga-Medina, J. C. Mayo-Maldonado, J. Lopez-Sarabia and O. M. Micheloud-Vernackt, "Mitigation of Leakage-Ground Currents in Transformerless Grid-Tied Inverters via Virtual-Ground Connection," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 8, no. 3, pp. 3111-3123, Sept. 2020.

[86] Yulin Yang, Guihua Liu, Hongpeng Liu and Wei Wang, "A single-phase grid synchronization method based on frequency locked loop for PV grid-connected inverter under weak grid," Proceeding of the 11th World Congress on Intelligent Control and Automation, 2014, pp. 5453-5456.

[87] V. Sonti, S. Jain and S. Bhattacharya, "Analysis of the Modulation Strategy for the Minimization of the Leakage Current in the PV Grid-Connected Cascaded Multilevel Inverter," in IEEE Transactions on Power Electronics, vol. 32, no. 2, pp. 1156-1169, Feb. 2017.

[88] R. Teodorescu, F. Blaabjerg, U. Borup and M. Liserre, "A new control structure for grid-connected LCL PV inverters with zero steady-state error and selective harmonic compensation," Nineteenth Annual IEEE Applied Power Electronics Conference and Exposition, 2004. APEC '04., 2004, Vol.1,pp. 580-586.

[89] S. Majumdar, B. Mahato and K. C. Jana, "Implementation of an Optimum Reduced Components Multicell Multilevel Inverter (MCMLI) for Lower Standing Voltage," in IEEE Transactions on Industrial Electronics, vol. 67, no. 4, pp. 2765-2775, April 2020.

[90] X. Guo, Y. Yang, R. He, B. Wang and F. Blaabjerg, "Transformerless Z-Source Four-Leg PV Inverter With Leakage Current Reduction," in IEEE Transactions on Power Electronics, vol. 34, no. 5, pp. 4343-4352, May 2019.

[91] S. Krauter and J. Bendfeld, "Comparison of Microinverters: Update on conversion efficiencies and energy yields," 2020 47th IEEE Photovoltaic Specialists Conference (PVSC), 2020, pp. 1429.

Publications

Journals

1. P.Manoj, K. Annamalai, S. Dhara and V. T. Somasekhar, "A Quasi-Z-Source-Based Space-Vector-Modulated Cascaded Four-Level Inverter for Photovoltaic Applications," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol.10, no.4, pp.4749-4762, Aug.2022, doi:10.1109/JESTPE.2021.3125695.
2. P. Manoj, A. Kirubakaran, V. T. Somasekhar, "An Asymmetrical Dual Quasi-Z-Source Based 7-Level Inverter for PV Applications," *in IEEE Transaction on Energy conversion*,2022 doi : 10.1109/TEC.2022.3222498.
3. P. Manoj, A. Kirubakaran and V. T. Somasekhar, "A Single-Stage Quasi-Z-Source-Based 5-Level Grid-Tied PV Inverter With Reduced Leakage Current," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 11, no. 1, pp. 826-835, Feb. 2023, doi: 10.1109/JESTPE.2022.3201566.
4. P. Manoj, A. Kirubakaran, V. T. Somasekhar, "A Quasi-Switched Capacitor Based Grid-connected PV Inverter with minimum Leakage current," (*in draft*)

Conference

1. P. Manoj, V. T. Somasekhar and A. Kirubakaran, "A Space Vector Modulated Quasi-Z-Source Based Four-Level VSI for PV Application," *2019 IEEE International Conference on Environment and Electrical Engineering and 2019 IEEE Industrial and Commercial Power Systems Europe (EEEIC / I&CPS Europe)*, Genova, Italy, 2019, pp. 1-5, doi: 10.1109/EEEIC.2019.8783748.