DESIGN AND CIRCUIT PERFORMANCE ANALYSIS OF ENCLOSED CIRCULAR DOUBLE GATE MOSFETS

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Doctor of Philosophy

by

Kallepelli Sagar

(Roll No. 718142)

Supervisor

Dr. Maheshwaram Satish

Assistant Professor

Department of Electronics and Communication Engineering

Department of Electronics & Communication Engineering

NATIONAL INSTITUTE OF TECHNOLOGY WARANGAL – 506004, T.S, INDIA

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APPROVAL SHEET

This thesis entitled "**Design and Circuit Performance Analysis of Enclosed Circular Double Gate MOSFETs"** by Mr. **Kallepelli Sagar** is approved for the degree of **Doctor of Philosophy**.

Examiners

_____

_____

Supervisor

_____

Dr. Maheshwaram Satish

Assistant Professor, Department of Electronics & Communication Engineering,

NIT WARANGAL

Chairman

_____

Prof. D. Vakula

Head, Department of Electronics & Communication Engineering,

NIT WARANGAL

Date: 07-08-2023

Place: Warangal

DECLARATION

I hereby declare that the matter embodied in this thesis entitled "**Design and Circuit Performance Analysis of Enclosed Circular Double Gate MOSFETs**" is based entirely on the result of the investigation and research work carried out by me under the supervision of **Dr. Maheshwaram Satish**, Department of Electronics and Communication Engineering, National Institute of Technology, Warangal. I declare that this work is original and has not been submitted in part or full, for any degree or diploma to this or any other university and was not submitted elsewhere for the award of any degree.

I also declare that this written submission represents my ideas in my own words and where others' ideas or words have been included, I have adequately cited and referenced the original sources. I have adhered to all principles of academic honesty and integrity and have not misrepresented or fabricated or falsified any idea/date/fact/source in my submission. I understand that any violation of the above will cause disciplinary action by the institute and can also evoke penal action from the sources which have thus not been properly cited or from whom proper permission has not been taken when needed.

Kallepelli Sagar
Roll No: 718142

Date: 07-08-2023
Place: Warangal

Department of Electronics and Communication Engineering
National Institute of Technology
Warangal – 506 004, Telangana, India

CERTIFICATE

This is to certify that the thesis work entitled **"Design and Circuit Performance Analysis of Enclosed Circular Double Gate MOSFETs"**, which is being submitted by Mr. Kallepelli Sagar (Roll No.718142), is a bonafide work submitted to National Institute of Technology Warangal in partial fulfilment of the requirement for the award of the degree of *Doctor of Philosophy in Electronics and Communication Engineering of National Institute of Technology, Warangal* is a record of bonafide research work carried out by him under my supervision.

To the best of our knowledge, the work incorporated in this thesis has not been submitted elsewhere for the award of any degree.

Dr. Maheshwaram Satish
Supervisor
Department of ECE
National Institute of Technology
Warangal – 506004

This Thesis is Dedicated to My

Family, Gurus, & Friends

Contents

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ABSTRACT

Over the last decade, the migration of commercial planar CMOS technology to multigate technologies has enabled continuing scaling of feature size to below 20 nm gate length while controlling short channel effects (SCEs) & reducing the leakage current. To address SCEs, multigate MOSFET architectures like FinFETs, gate-all-around (GAA) FETs, nanowire (NW) FETs, and Nanosheet (NS) FETs have been proposed. The multigate FETs with rectangular structure suffer from the corner effect (CE) problem, which is responsible for lowering the threshold voltage (V_{TH}) at the channel corners due to a decrease in the longitudinal electric field (LEF). One more issue with multigate rectangular MOSFETs is, they suffer from radiation effects like Total Ionizing dose (TID) and Single event effects (SEE).

To overcome these limitations, alternative solutions have been explored with respect to the device's layout geometry (circular, octagonal, and hexagonal, etc.). The circular gate transistor (CGT) is one such layout based solution that can extend the traditional CMOS process while using less silicon area. Owing to the circular structure they are immune to CE and radiation effects. Due to their asymmetric enclosed design, the inner/outer silicon pad can be configured as Source/Drain or Drain/Source. With the internal drain configuration these CGTs can enhance the LEF along the channel and improve the device performance.

In this thesis, initially, the performance of a novel circular double gate (CDGT) silicon on insulator (SOI) metal oxide semiconductor field effect transistor (MOSFET) to mitigate the SCEs is presented and the compared with existing circular single gate (CSGT) device at 30 nm technology node by using fully calibrated TCAD. In addition, the effects of various device configurations, such as raised S/D topologies and junctionless mode analysis, on CDGT device performance have been investigated.

At sub 10 nm technology nodes a similar comparison is performed between CSGT and CDGT for Low power (LP) and High performance (HP) applications. Among these two, the best device i.e., CDGT is benchmarked against popular multigate architectures. The proposed CDGT device is a suitable substitute for the NS FET in HP applications by offering a higher ON-current (I_{ON}) for future technology nodes. The investigation of various CDGT architectures has been carried out further. Among all architectures, the HfO_2 based CDGT architecture with 2 nm of underlap length provides good electrical properties, with an I_{ON}/I_{OFF}

ratio greater than 10^7, near-ideal subthreshold slope (SS), and reduced drain induced barrier lowering (DIBL).

CDGT is further optimized for ON current, by increasing the device area(inner drain radius). Using this concept, increasing the device area by 25% and 50% improves the total ON current by 19% and 39%, respectively. Further, similar analysis is performed at lower nodes 7 nm & 5 nm. The findings indicate that a similar improvement in ON current is observed for future scaling. The influence of source/drain doping concentration is also been investigated on proposed CDGT device.

Furthermore, novel NSFETs with circular layout geometry, i.e., Circular Nanosheet MOSFETs (C-NSFETs) are proposed for HP applications at 10 nm gate length. Further, the C-NSFETs performance by vertically stacking the circular sheets (2-sheet, 3-sheet, and 4-sheet) are explored and named them as Stacked Circular NSFETs (SC-NSFETs) and analyzed the variations of their device performance. It is observed that the device drive current is further improved by stacking multiple nanosheets within the same footprint.

Circuit performance is estimated on different circular MOSFETs using the effective current method at the 30 nm technology node, and then detailed analysis is performed using transient simulations at the 10 nm technology node.

Finally, analyzed the effects of radiation such as TID and SEEs, on electrical characteristics of the enclosed circular layout transistors like CSGT and CDGT, at 10 nm gate length (L_G). The results show that TID has minimal effect on the electrical properties of enclosed circular layout transistors and is insignificant in the case of CDGT. During the SEEs simulation, the alpha particles with low energy of 1.5 MeV- cm^2/mg Linear energy transfer (LET) and heavy ion particles with the high energy of 35 MeV-cm^2/mg LET are employed. The CDGT devices are less sensitive to the Single event transient (SET) in the inverter analysis due to their strong gate controllability by two gates and enclosed circular geometry. These circular FETs show superior immunity to radiation effects due to the enclosed layout. The CDGT outperforms the CSGT in terms of electrical performance and is less sensitive to the TID effect and SEEs. This TCAD based simulation study proves the suitability of CDGT devices in aerospace and military applications.

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Nomenclature

2D	Two-Dimensional
3D	Three-Dimensional
BOX	Buried Oxide
CDGT	Circular Double Gate Transistor
CE	Corner Effects
CGT	Circular Gate Transistor
CMOS	Complementary Metal Oxide Semiconductor
C-NSFETs	Circular Nanosheet FETs
CSGT	Circular Single Gate Transistor
DIBL	Drain Induced Barrier Lowering
DG	Double Gate
EOT	Equivalent Oxide Thickness
FoM	Figures of Merit
GAA	Gate-All-Around
GDSII	Geometric Data Stream for Information Interchange
GDML	Geometry Description Markup Language
g_d	Output Conductance
g_m	Transconductance
GSeat	Genius Single Event Analysis Tool
GUI	Graphical User Interface
HCEs	Hot Carrier Effects
HfO_2	Hafnium Oxide
HP	High-Performance
IC	Integrated Circuit
IGFET	Insulated-Gate Field-Effect Transistor
I_{OFF}	OFF/Leakage Current
I_{ON}	ON/Drive Current
IRDS	International Roadmap for Devices and Systems
ITRS	International Technology Roadmap for Semiconductors
JL	Junctionless
L or L_G	Channel/Gate Length
LET	Linear Energy Transfer
LP	Low power
MOSFETs	Metal Oxide Semiconductor Field Effect Transistors

MuGFET	Multiple-Gate Field-Effect Transistors
NM_H	Noise Margin High
NM_L	Noise Margin Low
NSFETs	Nanosheet Field-Effect Transistors
NTRS	National Technology Roadmap for Semiconductors
NW	Nanowire
PEF	Perpendicular Electric Field
RGTs	Rectangular-Gate Transistors
RIE	Reactive Ion Etching
SCEs	Short Channel Effects
SC-NSFETs	Stacked Circular NSFETs
SEEs	Single Event Effects
SET	Single Event Transient
SNM	Static Noise Margin
SOI	Silicon-On-Insulator
SS	Subthreshold Slope
TCAD	Technology Computer Aided Design
T_d	Propagation Delay/ Delay Time
TGF	Transconductance Generation Factor
T_f	Falling Edge Time Constant
TID	Total Ionizing Dose
T_{ox}	Gate Oxide
T_r	The Rising Edge Time Constant
V_{EA}	Early Voltage
VeSFET	Vertical Slit Field Effect Transistors
VeSTICs	Vertical Slit Transistor-based ICs
VLSI	Very Large-Scale Integration
V_{TH}	Threshold Voltage
W_{EFF}	Effective Width

Chapter-1

1. Introduction

1.1. History

The Semiconductor industry has expanded significantly in recent decades, owing to the micro/nano electronics revolution. Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) have been a major element in the semiconductor industry due to their higher package density, low power dissipation, and superior performance for industrial and commercial applications. Complex circuits that have billions of transistors functioning as switches are now integrated on a single chip. This progress in the semiconductor industry has led to the invention of novel electronic circuits and advanced processors for a variety of applications [1].

The concept of semiconductor devices being embedded in a thin silicon film that is supported mechanically by an insulating substrate has been around for decades. Historically, the first transistor was found in the patent of Lilienfeld dating 1926 and named it as Insulated-Gate Field-Effect Transistor (IGFET). The active section of this device is made of a thin semiconductor film placed on top of an insulator. Thus, the silicon-on-insulator (SOI) device can be said to as the first MOSFET. Unfortunately, the technology at that time was incapable of creating the device. Lilienfeld IGFET technology was forgotten and totally ignored & overshadowed for a period by the introduction of the bipolar transistor in 1947 and its major success. A few years later, advancements in technology led to the production of high-quality Gate Oxides (T_{OX}). In 1960, Kahng and Atalla created the first operational MOSFET based on Lilienfield's IGFET. MOSFET technology became more essential as monolithic integrated circuits improved, and Complementary Metal Oxide Semiconductor (CMOS) technology is still the leading technology in the nanotechnology industry.

Over the last 60 years, specialists have put a lot of attention into research and development since the introduction of the first electronic integrated circuit (IC) built by Jack St. Claire Kilby at Texas Instruments in 1958. For his efforts, he received the Nobel Prize in

Physics in the year 2000. Following the development of the first planar IC, the Gordon Moore proposed the Moore's law in 1965, which is still in use today. Moore revised his prediction in 1975, that the numbers of transistors should double every two years. Moore's law projected that the number of transistors per integrated circuit will increase exponentially with CMOS technology, resulting in increased density, speed, and power improvement [2] [3].

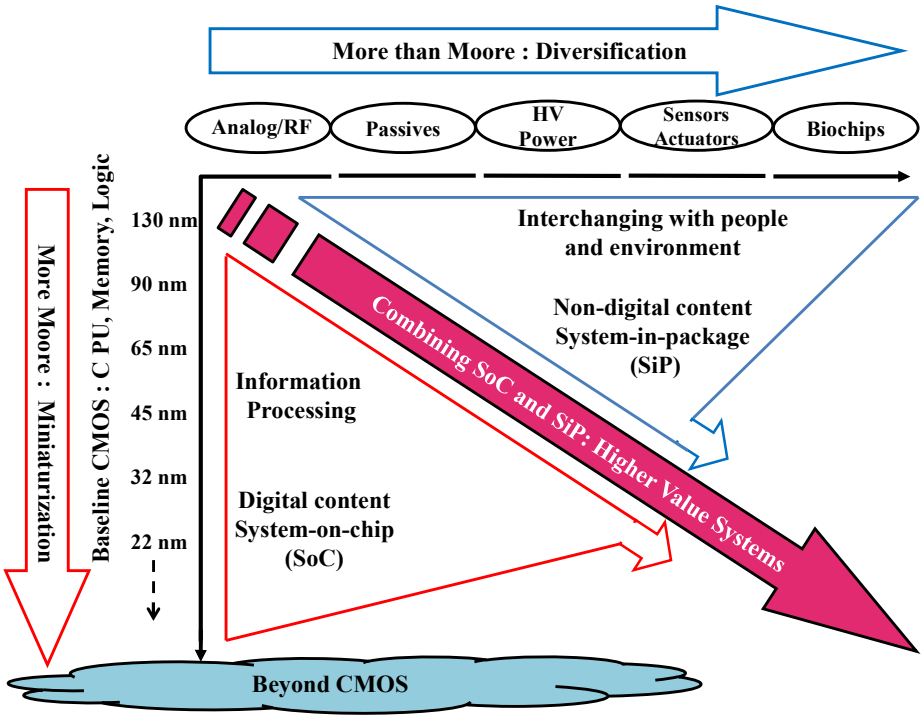


Fig. 1.1: Moore's Law and More [4].

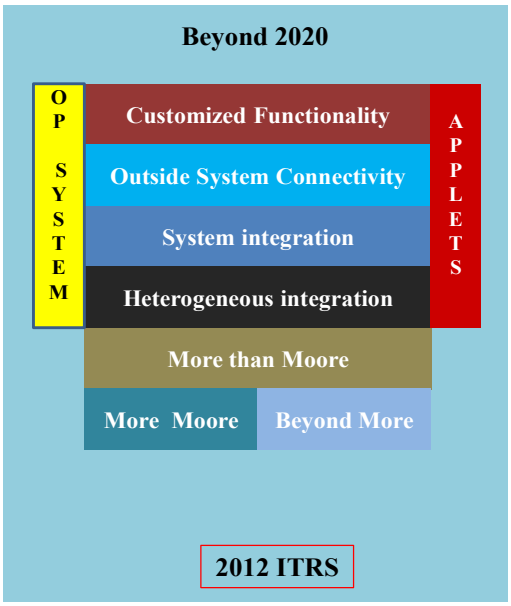


Fig. 1.2: The New Ecosystem of the Electronics Industry [5].

The Semiconductor Industry Association issued the "National Technology Roadmap for Semiconductors (NTRS)" in 1992, which presented a 15-year forecast on important semiconductor industry trends. The roadmap was a useful reference guide for semiconductor production companies, with expectations on materials and software projections, and provides clear goals for researchers in the coming years. The NTRS was upgraded in 1994 and 1997 with alternative solutions and possible requirements. To take advantage of contributions from across the world, the NTRS was modified in 1998 to "International Technology Roadmap for Semiconductors (ITRS)". Since 1998, ITRS has published or revised roadmaps annually till 2015.

As illustrated in Fig. 1.1, the ITRS issued the first white paper in 2005, in which the keywords "More than Moore" and "More Moore" [4] were introduced for the first time. This announcement promised the invention of the iPhone and iPad in later years. Therefore, the ITRS agreed to restructure in December 2012, during its annual meeting in Taiwan, to address the rebuilt ecosystem of the microelectronics sector. In May 2016, the transition and growth of the roadmap from the ITRS to the International Roadmap for Devices and Systems (IRDS) resulted in significant attention to systems [5]. As shown in the Fig. 1.2, priority has been given to architectures and applications that vary from the conventional model of device → circuit → logic gate → functional block → system. All of these efforts have resulted in the evolution of MOSFET dimensions from millimeter to nanometer scale, i.e., a change of six orders of magnitude in roughly 60 years, or almost one order of magnitude of MOSFET dimension decrease every decade.

1.2. Developments of MOS Technologies

In general, the primary goals of research & development were to shrink the dimensions and improve the electrical performance of MOSFETs and hence improve their ICs performance [6]. The scaling down of the size of transistors has followed Moore's law, and due to shrinking of the device, the electronic industry has benefited significantly over the last 4 to 5 decades in terms of increasing data throughput per chip. Long channel MOSFETs virtually has ideal characteristics, but as device geometries shrink, they deviate significantly from ideal characteristics. When the device's channel length is limited to depletion widths of source and drains junctions, several Short Channel Effects (SCEs) [7], including Drain Induced Barrier Lowering (DIBL), Threshold voltage (V_{TH}) roll-off, mobility reduction, and bulk punch

through, degrade the device performance [8]. To overcome the SCEs while maintaining device length as short as possible, for many years, research & development in micro/nano electronics has been divided into three broad groups.

i) New manufacturing techniques to implement MOSFETs (nanoimprint photolithography [9], plasma deposition [10], lightly doped drain [11], elevated or raised source/drain [12] etc.),

ii) New materials (High-k material [13], metal gate [14], Germanium [15], SOI [16], Silicon-on-Sapphire [17], Silicon-Germanium [18], Ferroelectric materials [19], etc.), and

iii) Advanced innovative architectures (Double gate (DG) MOSFET [20], Ultra-thin body [21], FinFET [22], Multiple-Gate Field-Effect Transistors (MuGFET) [23], Gate-All-Around (GAA) or Nanowire (NW) [24][25] , Junctionless (JL) [26], Tunnel FET [27], and Nanosheet [28], VeSFET [29] [30] etc.).

The developments in the manufacturing process and the use of new materials gave the freedom to the researchers to scale down the transistors up to the 100 nm technology node while keeping SCEs under control. Traditional planar MOSFETs, on the other hand, suffer greatly from SCEs at technology nodes less than 50 nm and beyond [31]. Thus, to overcome SCEs, advanced novel structures are being used with multiple gates.

To expand CMOS technology beyond sub 45 nm, SOI MOSFETs are a potential candidate to replace traditional planar MOSFETs [32]. However, SOI MOSFETs are not immune to SCEs when further scaled down to sub 30 nm technology nodes [33]. Due to their enhanced performance and superior electrostatic gate control over the conduction channel, DG MOSFETs [34] are an alternative design for replacing planar MOSFETs in sub 20 nm technology nodes. Because of misalignment and the complex manufacturing process, a new structure known as FinFET has emerged as a suitable device in High-Performance (HP) applications. FinFETs, on the other hand, have several difficulties in designing, functionality, layout, and cost for subsequent scaling [35] [36]. However, in order to maintain SCE control, the fin thickness and gate length must be scaled, which can lead to V_{TH} variation [37]. Because of their enhanced short-channel control and high current density, GAA/NW MOSFETs are expected to provide even further device scalability [38]. Meanwhile, as compared to the standard GAA structure, Nanosheet field-effect transistors (NSFETs) display improved performance, higher drive currents, and better process efficiency due to the stacking process. As a result, the NSFET is gaining popularity as the most promising candidate for

future devices [39]. The Vertical Slit Field Effect Transistors (VeSFET) is another intriguing novel device that has been suggested in the literature to replace the conventional MOSFET [40]. It is an unconventional device with a non-standard layout that offers low power (LP) consumption and high package density for analog and digital applications [41].

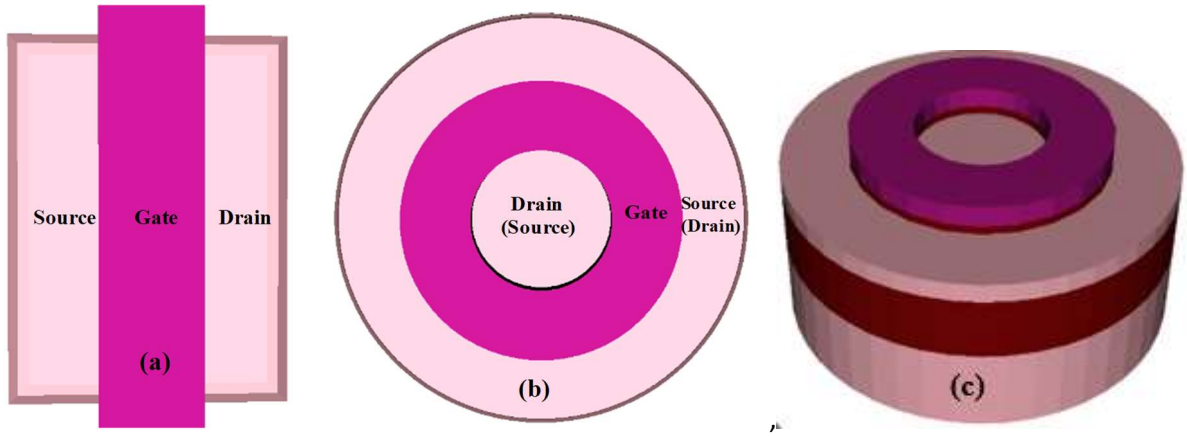


Fig. 1.3: (a) Rectangular MOSFET layout (b) Circular MOSFET layout, (c) Structure of Circular MOSFET.

Apart from these various non-planar devices (novel advanced innovative architectures), reduction in leakage currents & SCEs can also be achieved from non-standard enclosed geometries (circular, hexagonal, octagonal, and ellipsoidal, etc.) [42]. These are developed based on the layout of the device. These non-standard layout devices can improve electrical performance, reducing the longitudinal corner effects, and boosting tolerance towards ionizing radiation. The circular/ring/annular gate MOSFET is one of the most popular non-standard layouts. Fig. 1.3 depicts traditional rectangular MOSFET and circular edgeless MOSFET. It has a circular gate layout, which provides higher immunity to SCEs than traditional planar MOSFETs, owing to the absence of side interface areas, which cause trap-induced leakages. Three Dimensional (3D) view of the Circular gate MOSFET is shown in Fig. 1(c). The structural difference between circular gate MOSFET with other existing technologies is discussed in Chapter 2.

This thesis investigates the enclosed circular layout transistor based on both structural and material variations. Further, it analyzes the behaviour of circuit level performance and also radiation effects.

1.3. Motivation

Naturally, the developments of advanced CMOS (novel advanced innovative architectures) have led to a desire to utilize the technology in a range of applications, including military, aerospace, and terrestrial [43]. One of the most typical issues that ICs encounter in the space environment is the TID effect, which is the accumulation of the ionizing dose over time. The influence of total ionizing dose (TID) on device performance is a major problem for space-based applications, as it can affect crucial device operating parameters such as shift in V_{TH}, off-state leakage, mobility, subthreshold slope (SS), and transconductance (g_m) [44]. One more major issue is corner effects (CE), which is prominent in MuGFETs with three or more gates. The gate voltage in MuGFETs causes the CE to increase the resultant electric field in the areas close to the vertices of the junctions of two different gate regions. This effect lowers the V_{TH} of multigate FETs in these gate regions and consequently, it reduces the electrostatic controllability of the gate of the transistor (undesired effect). Because of these reliability issues like TID and CE effects in non-planar multigate devices, we need to innovate new fabrication processes, techniques, devices, and materials that can mitigate the degradation of ionizing radiation (protons, heavy ions, and electromagnetic waves) in semiconductor device parameters and avoid potential electrical failures [45]. These effects can be eliminated/minimized using enclosed layout transistors. One such layout is the non-standard enclosed circular geometry (circular gate transistor (CGT)), which has the added advantage of an increase in the effective width of a transistor for a given silicon area [46]. CGTs are capable of improving the Longitudinal electric field along a channel that reduces the CE and enhances radiation hardening [47]. Therefore, with these advantages, the circular layout has been used with the multiple gates concept to create ICs at lower technology nodes and investigate their radiation hardness analysis.

1.4. Problem Statement

The primary goal of this thesis is to perform a detailed simulation-based analysis of circular double gate transistors (CDGT) SOI MOSFETs for LP and HP applications to mitigate the SCEs, as well as their radiation-hardness analysis. Also, the impact of various device-level variations such as raised topologies, Junctionless mode, and high-k materials on CDGT device behavior. Further the design of stacked nanosheet MOSFETs in a circular geometry for building high-current-rate integrated circuits.

1.5. Research Objectives

To mitigate the SCEs along with CE and TID effects and implement radiation tolerance circuits for space and military applications, we have considered several objectives, which are mentioned below during the period of research.

1. Implementation of CSGT and CDGT SOI MOSFET devices and analyze the DC performance with several device level variations such as raised source/drain topologies, Junctionless mode analysis at 30 nm technology node.
2. Implementation of CDGT SOI MOSFET with under lap and high-k dielectric material concepts and analyze the Analog/RF performance.
3. Benchmarking, optimization, and scaling of CDGT SOI MOSFET at sub 10 nm technology nodes.
4. Design and analysis of circular nanosheet MOSFETs and stacking of circular nanosheet MOSFETs.
5. Design and analysis of inverter to analyze the circuit level performance of circular MOSFETs.
6. Analysis of radiation effects (TID effects on device performance and SEEs on circuit performance) of different circular MOSFETs.

1.6. Thesis Organization

The thesis presents circular single and double gate MOSFETs device design and radiation hardened analysis for use in aerospace and military applications. The thesis is organized into seven chapters. The following section gives the summary of the chapters.

Chapter 1 presents an introduction to the work, motivation, reasons for choosing the problem and contributions of the thesis.

Chapter 2 This chapter deals with a detailed literature review of circular layout transistors with a notable amount of most recent literature. It covers the history of circular layout transistors, as well as their evolution in the semiconductor industry. It also discusses several viable solutions for SCEs. Finally, this chapter concludes with a discussion of research gaps in the available literature.

Chapter 3 In this chapter, A well-calibrated TCAD setup with various simulated physical models is established to implement the circular layout transistors are discussed. To validate

the models used for the device simulation studies at different technology nodes, device structures identical to the reported experimental devices [48] & [49] were created, and matching their V-I characteristics. Further, detailed information about relevant physics models is provided for carrier generation, carrier recombination, band-to-band tunneling, and velocity saturation along with density gradient for quantum corrections. This chapter also contains details of simulation setup requirements for TID effects on device performance as well as SEE (Single event effects) on circuit transient simulations.

Chapter 4 This chapter describes the detailed implementation of SOI circular layout transistors such as circular single gate transistors (CSGT) and CDGT MOSFETs at 30 nm technology node. Analyzes the performance of these devices in terms of the device-level figures of merit (FoM) such as device ON current (I_{ON}), leakage current (I_{OFF}), I_{ON}/I_{OFF} current ratio, SS, and DIBL. It also contains device level variations like raised source/drain topologies and JL behavior on CDGT devices. This study provides the need of use of multiple gates concept in circular geometry (CDGT devices) to improve the device electrical performance. Finally, this chapter ends with the performance analysis of CSGT and CDGT devices at 10 nm technology node.

Chapter 5 This chapter mainly discusses the CDGT device at the 10 nm node with the impact of its device-level & material variations such as underlap concept, and high-k dielectric materials on device performance. Furthermore, the CDGT device is benchmarked against advanced novel structures and CDGT's device optimization and scaling are discussed. Finally, this chapter concludes with a discussion of the novel implementation of a stacked nanosheet MOSFET in circular geometry. This study of stacked circular nanosheet MOSFET gives the guidelines for building high-current-rate integrated circuits, such as current drivers and power stages.

Chapter 6 This chapter discusses a detailed circuit analysis of various circular layout transistors by analyzing the CMOS inverter. Further, the radiation effects such as TID effects on device performance of both CSGT and CDGT devices, as well as SEEs on their circuit performance are analyzed. Because of its high radiation tolerance, this study can provide guidelines to researchers to use circular layout transistors in radiation environments such as military and aerospace applications.

Chapter 7 This chapter summarizes the overall work done in this thesis and proposes some potential future work trends to take this research to the next level.

Chapter-2

2. Literature Survey

CMOS devices have been progressively scaled down, together with breakthroughs in CMOS processing technology, resulting in advancements in Very Large Scale Integration (VLSI) design methodologies. By using advanced CMOS VLSI technology and high density novel architectures, high performance computer system chips are integrated with proper functionality at a low cost. Due to the downsizing of CMOS devices, the related power consumption has been reduced. However, the issues associated with MOSFET scaling, such as SCEs, are becoming more prevalent. As discussed in Chapter 1, several solutions were deployed to address the SCEs due to scaling.

2.1. Review on Possible Solutions

SOI MOSFETs are one of the first alternative solutions to replace conventional rectangular MOSFETs to further expand CMOS technology by controlling SCEs. SOI technology has major advantages over planar MOS technology [50][32]. These benefits include low leakage current, faster switching speed, reduced subthreshold swing, better isolation, decreased latch-up, and improved short channel immunity [51]. However, SOI MOSFETs are not immune to short channel effects when further scaled down [33]. Several issues need to be solved to produce high performance SOI devices. Oxide leakage and high series resistance are two of the most significant problems [52].

The SOI MOSFET performance is limited due to the source and drain contact resistances in the sub 32 nm regime. This is because while contact resistance increases with the scaling of the contact area, the on-state resistance of a MOSFET decreases with the scaling of the transistor. One common method for reducing the series resistance component is by raised S/D engineering [53]. Raised S/D structures have shown promise in mitigating the parasitic resistances associated with the source and drain, improving ON current, reducing the lateral electric field, controlling hot carrier effects, and improving device performance [12].

Modifying the doping concentration and obtaining high quality junctions is difficult in thin SOI layers when the device is scaled down to sub 30 nm nodes [54]. Hence, the JL

concept, which is a better doping choice for short channel devices. The JL concept has gained much attention in recent years, using high and uniform doping in the channel and S/D regions. This has several benefits over traditional planar MOSFETs, such as enhanced performance against SCEs, high scalability, a low thermal budget, and a simplified fabrication process [55] [56]. Such gains are only achieved because of the high current drive with no barrier in JL devices.

One of the methods to reduce SCEs and leakage currents is the use of gate source/drain underlap concept. Because of the underlap concept, the series resistance will increase, resulting in a reduction in total device current (both I_{ON} & I_{OFF}). It offers an optimum I_{ON}/I_{OFF} ratio [57][58]. It offers desirable characteristics like greater break-down voltage, decreased electric field at the drain and source regions, smaller gate leakage current, and so on, making it better suited for limiting the influence of drain potential on source barrier (DIBL effect) and reducing hot carrier effect.

The biggest advancement in transistor technology since the invention of polysilicon-gate MOS transistors has been the using of high-k and metal materials. The various High-k gate dielectric materials such as (Al_2O_3, La_2O_3, HfO_2, etc.) have attracted the interest of many researchers over the last two decades due to their significant potential for maintaining further downscaling in Equivalent Oxide Thickness (EOT) with a physically thicker film and a lower gate leakage current [13]. All these approaches are related to the process variations (raised source/drain, Underlap, JL), and new materials (SOI, high – k). Along with these solutions, to reduce SCEs, advanced novel devices are proposed with multiple gates.

2.1.1. Review on Advanced Structures

In recent years, the microelectronics sector has made huge investments in revolutionary technologies aimed at the production of devices with exceedingly small dimensions [59]. The lack of gate control over the channel in very short channel devices (owing to the closeness of the source and drain regions) makes the usage of traditional MOSFETs in ultra-scaled transistors difficult. As a result, alternative technologies like multigate architectures are explored and reported in the literature [60].

The continuous scaling of planar MOSFETs to sub 30 nm ranges drastically degrades device performance, resulting in increased leakage currents & off-state power, both of which

are critical design criteria for next-generation CMOS [61]. The mitigation of off-state leakage current and SCEs in the conventional planar transistor becomes complicated technological challenge as the MOSFET channel length is shortened. The SCEs including SS deterioration, V_{TH} roll-off, and high DIBL restricts the device performance for smaller channel lengths. Various advanced MOSFET designs [62][63][64][65] and better quality channel materials are now in demand [18] [22] to overcome the scaling limits. In recent years, modern architectures such as multigate devices like DG [20], FinFET [66], GAA FETs [67] [68], and NSFETs [69][70] have gained popularity, which lowers drain-to-source leakage currents [71] and improves device performance with some fabrication complexity.

DG MOSFETs is an alternate structure for replacing planar MOSFETs in sub 30 nm technology nodes, due to their high performance and enhanced electrostatic gate control over the conduction channel as shown in Fig. 2.1. It also exhibits reduced SCEs and provides an improved drive current because, in DG MOSFETs, two gates control the channel [72].

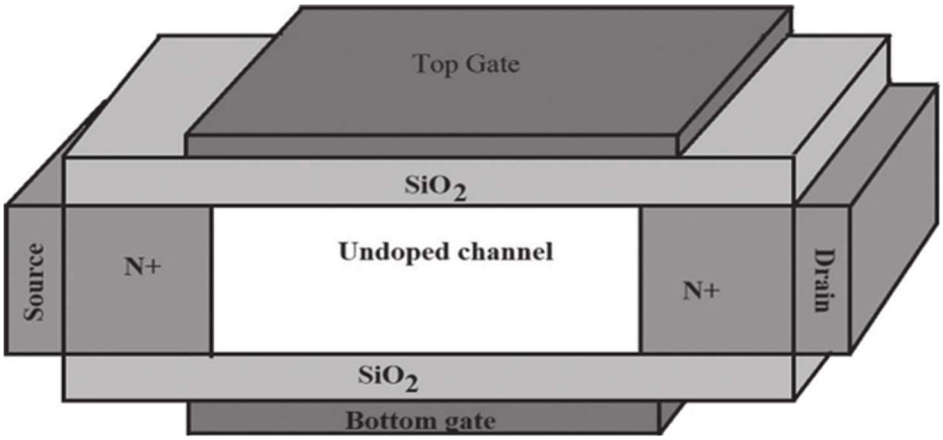


Fig. 2.1: Structure of Double gate MOSFET [72].

FinFETs have effectively enabled continuous technological scaling from conventional devices by increasing additional gate controllability over the channel at lower technology nodes, leading to an enhanced performance at lower supply voltages [66]. Due to complex fabrication and alignment in DG MOSFETs, this new structure such as FinFET is developed to lower SCEs with better gate controllability on three sides by three gates as shown in Fig. 2.2. FinFET technology has many advantages over bulk CMOS, including high drive current for a given similar footprint, resulting in high speed, low leakage, low power consumption, no random dopant fluctuations, resulting in better mobility and transistor scaling beyond 20 nm.

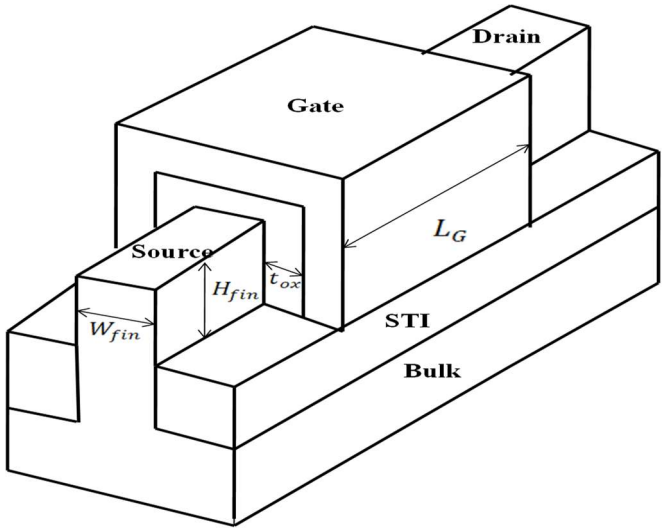


Fig. 2.2: Structure of FinFET.

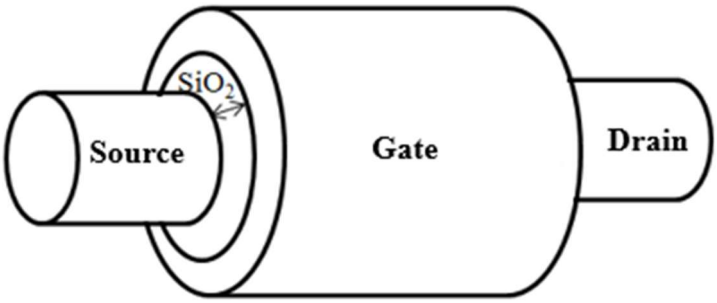


Fig. 2.3: Structure of NWFET.

FinFETs, on the other hand, have several difficulties in designing, functionality, layout, and cost for subsequent scaling [35][36]. However, in order to limit SCEs, the fin thickness and gate length must be scaled, which can lead to high V_{TH} variation [37]. Because of their enhanced short-channel control with the surrounding gate as shown in Fig. 2.3, and high current density, GAA/ NWFETs are expected to provide even further device scalability [38][73][74]. Modern device topologies have progressed from planar to multigate and finally to the ultimate GAA to improve electrostatic gate control and reduce SCE [75]. Even with an improved channel structure, the standard lateral NW device's cell width is severely constrained by the source/drain contact size, spacer thickness, and gate length [76]. Vertical nanowire FETs have a lower layout footprint than lateral nanowire FETs and can have a more flexible gate length, contact size, and spacer width [77]. As a result, the Vertical nanowire FET was conceived and developed to increase scalability by manufacturing the channel in the

vertical direction, with the source and drain on the bottom and top of the gate [78]. These NWFETs have been used in a variety of applications, namely biosensors, non-volatile memories, solar cells, pressure sensors [79]. Meanwhile, as compared to the standard GAA structure, GAA-NSFETs display improved performance, higher drive currents, and better process efficiency due to the stacking process. As a result, the NSFET is gaining popularity as the most promising candidate for future devices [39][80].

NSFETs have recently been proposed as a way to continue scaling as shown in Fig. 2.4 [81]. In NSFETs, the width of the silicon film (NS width) is not restricted by fin quantization & fin pitch, allowing for greater flexibility in producing sufficient effective width (W_{EFF}). However, the larger cross section influences drive current, parasitic components, and electrostatics all at the same time. As a result, it is critical to evaluate device design alternatives for NSFETs. Meanwhile, horizontally- stacked NSFETs have been presented with significant promise to replace fin structure by achieving improved electrostatics and higher drive currents with large W_{EFF} within the same footprint [28].

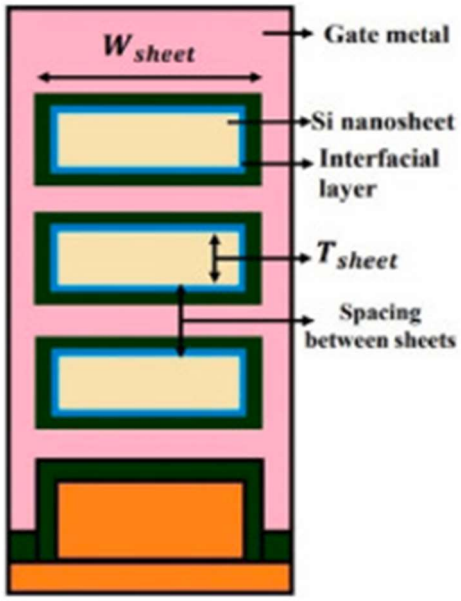


Fig. 2.4: Structure of NSFET.

The issues with CMOS scaling can be effectively resolved by the multigate devices which are discussed above. These devices are capable of much more than just better electrostatic control if the gates are managed independently [82]. In addition to increasing the functionality of a single device, independent gate control also offers opportunities for device circuit co-design, which may be an alternative to scaling in terms of increasing the functional density for a

given silicon area. VeSFET is a non-standard layout device as shown in Fig. 2.5, which symmetrically has two independent gates, will allow engineers to create innovative circuits and improve performance, particularly in the low power domain [83]. These devices offer very high I_{ON}/I_{OFF} ratios, low drain leakage currents, and nearly ideal subthreshold slope. With the help of twin independent gates in VeSFET structure both AND & OR operations are implemented using a single transistor, increasing logic density per area while consuming less power. VeSFETs are elementary components of Vertical Slit Transistor-based ICs (VeSTICs) [30]. Due to the special 3D geometry of VeSFETs, complementary pairs of devices can be produced on SOI substrates using the same techniques as in conventional CMOS process [41].

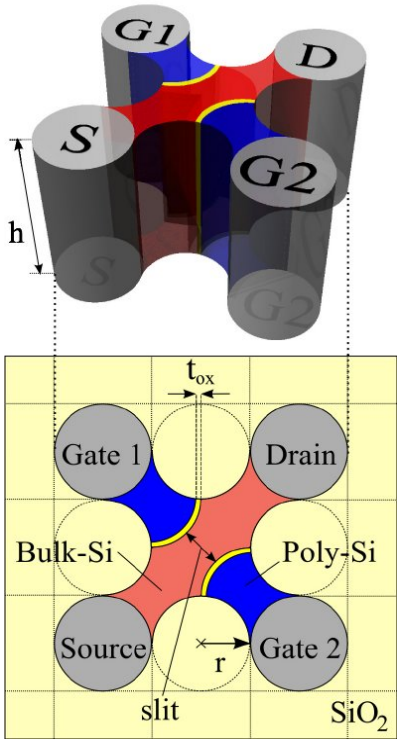


Fig. 2.5: Structure of VeSFET [30].

2.1.2. Review on Non-standard Devices

In addition to these solutions for overcoming SCEs, there is another category that semiconductor and ICs companies have yet to investigate, which is regarding the layout of the device. By changing the conventional rectangular gate layout to non-standard enclosed layouts [42] such as circular [46], diamond (hexagonal) [84], fish [85], elliptical [86], octagonal [87], etc. These non-rectangular (non-standard) gate layout designs for MOSFETs can improve electrical performance as well as ionizing radiation tolerance.

The major issue in rectangular layout MOSFETs (multiple gates) is the corner effect (CE). Let's consider a standard GAA MOSFET (rectangular-section) [88], the Perpendicular Electric Field (PEF) near the devices gate corners is high (due to two field components ($\overrightarrow{\varepsilon_T} = \overrightarrow{\varepsilon_2} + \overrightarrow{\varepsilon_1}$)), while PEF in the rest of the silicon channel is low (due to only single PEF ($\overrightarrow{\varepsilon_1} = \overrightarrow{\varepsilon_2}$)) as shown in the Fig. 2.6. This high PEF is responsible for lowering the device V_{TH} at the corners of the device channel region and this effect is called CE. Due to this reduction in V_{TH}, leakage currents increase, this is an unwanted effect in 3D devices and tends to weaken electrostatic controllability. To reduce the CE, and extend the planar CMOS technology process, circular layout geometry is used. This revolutionary layout style for MOSFETs helps to enhance their electrical performance and ionizing radiation tolerance.

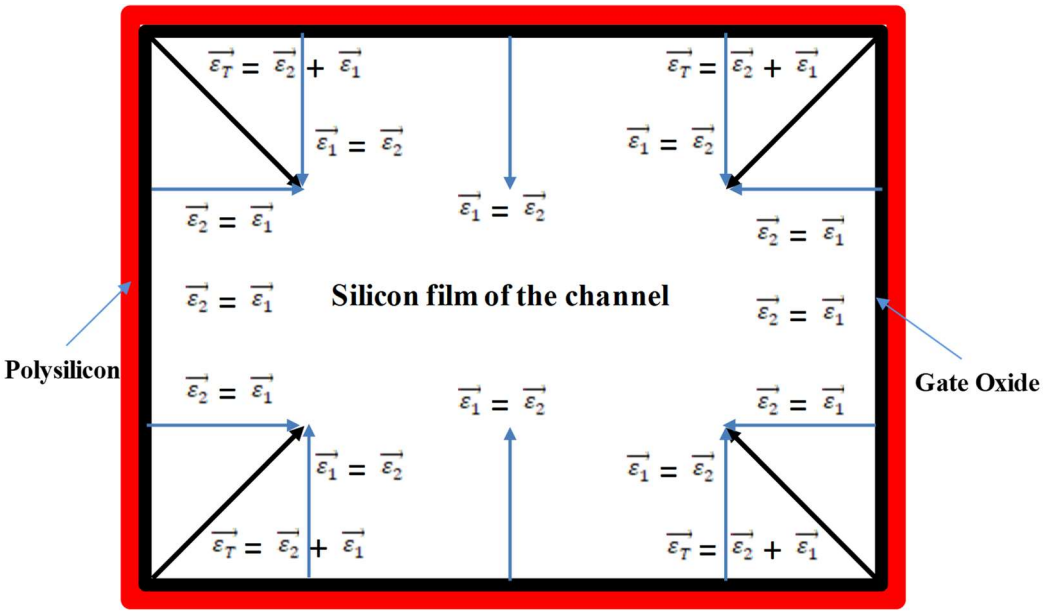


Fig. 2.6: The PEF vector components ($\overrightarrow{\varepsilon_1}$ and $\overrightarrow{\varepsilon_2}$) and their outcomes.

2.1.3. Review on Circular MOSFETs

CMOS technology scaling follows Moore's Law in terms of both decreasing feature size of the transistor and increasing data throughput per chip. However, the threshold voltage required to control leakage currents does not result in a proper scaling of the power supply. This results in significant increases in electric fields between channels and oxide layers of the MOSFET, and it finally leads to an impact on reliability [89]. The introduction of the lightly doped drain regions decreases the channel electric field and increases reliability, but it is ineffective for lower technologies. In radiation conditions, this is a major problem. To create radiation-hardened systems, enclosed CGTs have been designed. These CGTs do not have

edges (edgeless) that are known to create leakage paths in NMOS transistors. These CGTs are employed in Radiation hardened (Rad-hard) applications such as aerospace, military, and terrestrial because they perform more correctly and consistently in areas that may be exposed to radiations. The complexity of the unique Rad-hard technology, limited volume demand, and space efficiency are all reasons why this technology is not extensively employed.

De Lima and Gimenez [90] proposed the circular gate non-standard layout geometrical device to improve the short-channel immunity for high-frequency ICs. CGTs are commonly used in the design of integrated circuits. CGTs have been used in high-frequency amplifiers in common-source differential pairs to extend the amplifier bandwidth by minimizing stray capacitances associated with drain-substrate junctions [91]. CGTs have a greater breakdown voltage than traditional Rectangular Gate Transistors (RGTs) due to the absence of sharp contours on p/n junctions. As a result, they are attractive as building blocks for a wide range of high current-rate switching drivers, such as linear regulators and power transistors [92].

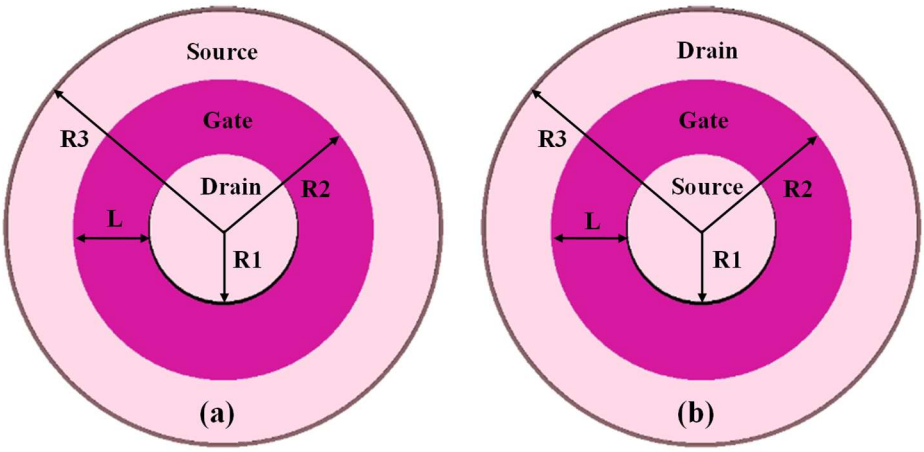


Fig. 2.7: CGT MOSFETs which is operating in a) Internal drain configuration, b) External drain configuration.

CGTs are asymmetric devices; they can be operated in both internal drain configuration and external drain configuration as shown in the Fig. 2.7. This is one more advantage of CGTs. Since the longitudinal electric field in the channel close to the drain area is greater than the longitudinal electric field in the channel close to the source area, the circular gate transistor with an inner silicon pad functioning as a drain has superior electrical characteristics [46]. Because of its enclosed asymmetrical layout topology, the CGTs enhance longitudinal electric field along the channel, mitigate CE effects, and finally improve radiation sensitivity. CGTs

are preferred in analog circuits, since they occupy a lower silicon area [93]. In Fig. 2.7, R1 and R2 are the internal and external radii of the channel, respectively, and R3 is the radius that defines the external edges of the device. Here, the channel length (L or L_G) is equal to R2 - R1.

To further improve the layout packaging, an overlapping CGT architecture has been introduced with excellent thermal stability for aerospace applications as shown in the Fig. 2.8 [47]. As the gate overlaps between adjacent unit cells in overlapping CGT structures, the area of the drain and source junctions decreases, resulting in quicker transients. This new structure is also more efficient in terms of area than RGTs. Owing to its layout compactness, overlapping CGTs are an excellent alternative technology for building high-current-rate integrated circuits, such as current drivers and power stages, while reducing the die size and chip cost for future scalability [94].

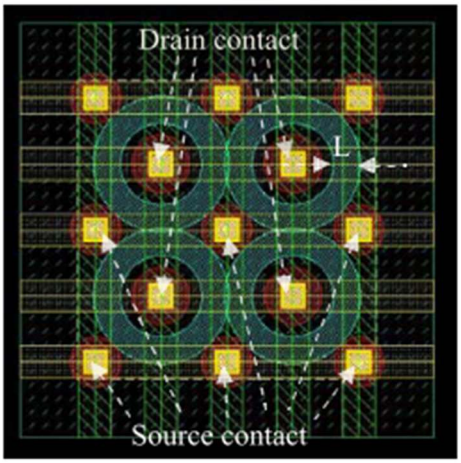


Fig. 2.8: 2×2 array of O-CGT [94].

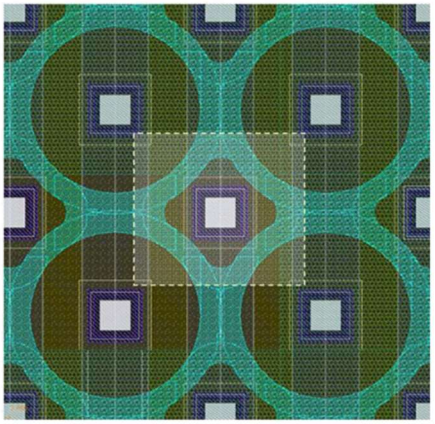


Fig. 2.9: Alternative overlapping CGT structure [95].

The analytical modelling of a circular MOSFET with a larger channel length was introduced [95]. In this work, alternative overlapping CGT layout is proposed with rounded source edges to improve the FOM as compared to conventional overlapping CGTs and RGTs as shown in Fig. 2.9. Here, FOM defined as $\eta = (W/L)/A$, where W is defined as the effective width of the channel, L is defined as the length of the channel, and A is defined as the transistor layout area.

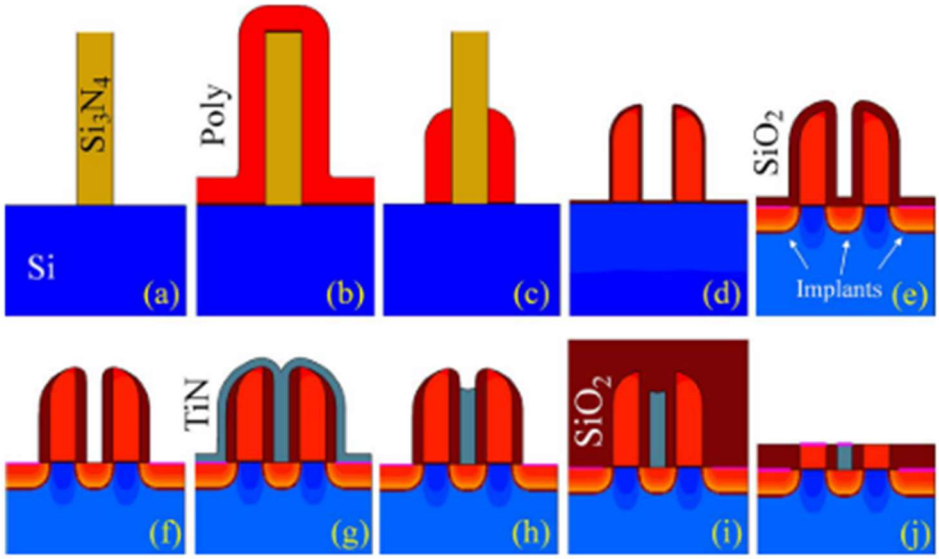


Fig. 2.10: Process setups (a) Lithography Reactive Ion Etch (RIE) Si_3N_4, (b) Deposit SiO_2/poly, (c) RIE poly/SiO_2, (d) Grow SiO_2, (e) Implant, deposit, SiO_2, (f) RIE SiO_2, (g) Deposit metal, (h) Etch metal, (i) Deposit SiO_2, (j) Chemical Mechanical Polishing.

Williams et al. [96], extended the same technique to a shorter channel length, naming the device as Ring FET at sub 45 nm technology node. The fabrication process of Ring FETs is compatible with the conventional planar rectangular gate transistor fabrication process as shown in the Fig. 2.10. Because the Ring FET channel is totally self-contained within the device, impact ionization is reduced, the hot-carrier effect is reduced, and drain-to-source leakage is removed, which improves the device's hot-carrier reliability [97]. The simulation findings demonstrate that using the internal silicon region as the drain reduces the influence of the drain fields on the source barrier as the Gate Length (L or L_G) is scaled below 45 nm.

Kumar et al. [98], for the first time developed an analytical drain current model for nanoscale Ring FET design. While developing the model, major short-channel effects such as channel length modulation, drain-induced barrier lowering and velocity scattering, were

taken into account. Model results were compared with simulation results and found to be in good agreement. The suitability of CGT/ Ring FETs for digital and high-frequency applications, as well as the reliability issues, have been discussed and compared with planar MOSFETs [99]. Shobhana et al. [57], used lightly doped drain concept to further improve device performance. The addition of lightly doped drain regions reduces both OFF current (increased series resistance and reduced DIBL) and ON current (due to an increase in series resistance).

The 3D curvature effect caused by the circular layout of a practical SOI lateral power device often limits its breakdown properties [100]. A 3D variation of lateral doping approach is proposed in this work to reduce the electric field crowding of the SOI lateral double diffused metal oxide semiconductor with a circular layout. As a result, the layout's 3D curvature effect is completely eliminated, and the breakdown voltage is improved. Moreover, lateral double diffused metal oxide semiconductor with the innovative drift doping profile displays better ON-state performances, such as higher ON-state breakdown voltage, decreased specific on-resistance, larger saturation current, reduced quasi-saturation effect, enhanced g_m, and thus a large Baliga's figure of merits [101].

2.2. Review on Radiation Effects

Most electronic circuits nowadays are made up of MOSFETs and bipolar devices. Ionizing radiation can cause significant charge accumulation in insulators and oxides, which can lead to the degradation and failure of the device. The TID effect [102] is one of many radiation-induced defects. This effect, caused by long-term accumulated radiation damage, generally worsens the performance of CMOS ICs by altering the characteristics of MOSFET devices, specifically n-MOSFETs contained in the circuits. As a result, TID has an impact on long-term missions, satellite lifetimes, and any other electronic circuit used in a radiation environment [103].

SEE is a soft error that causes critical reliability concerns in a semiconductor circuit during dynamic operation. A soft error is more frequent in commercial terrestrial applications than hard error, which are more common in military and space electronics [104]. A soft error occurs when a radiation incident deposits sufficient charge in a logic circuit to invert a node voltage or flip the data state of a memory cell. Because the radiation does not severely affect

the circuit or device, this error is referred to as "soft," because it may be rectified by writing updated data [105].

The radiation effects (TID and SEE) have been investigated using on various device architectures such as planar, SOI, FinFET, NW, and NSFET [106][107][108][109]. The TID response of a bulk and SOI FinFETs were compared at 14 nm node [110][111]. The influence of SEEs was examined in NSFETs and FinFETs [105][112]. The TID effects with an in depth study of the device-level response of a bulk FinFET at 14 nm process node, as well as the impact of process parameters, transistor layout, device threshold voltage, and irradiation bias configuration is investigated [43][113]. The effect of radiation on FinFET and stacked NW, as well as the effect of SEE on static random-access memory cells, has been examined at 20 nm L_G [114]. Radiation effects on 7-layer stacked GAA NSFET were also investigated [115]. All these reports are related to advanced novel structures and are unable to tolerate the radiation effects completely due to their non-enclosed geometry. From the limited data on circular layout transistors (CSGT/CDGT) and due to their advantage of enclosed circular design, these are capable of decreasing CE effects and are better suitable for radiation hardened applications [98][89]. Because radiation facilities are usually limited and experiment costs are expensive, 3D- TCAD (Technology Computer Aided Design) simulators have been frequently employed to give insight into physical mechanisms and the effects of ionizing radiation[116]. Thus, the Visual TCAD (Genius 3D by Cogenda) [117] simulator is utilized in this work.

2.3. Research Gaps

Based on the literature survey it is observed those CGTs are one of the promising devices to replace conventional planar transistors for lower nanometer technology nodes. Because of advantage of their enclosed layout design, these are well suited for operation in radiation environments. Hence, it is necessary to analyze the radiation effects such as TID effects on device performance and SEE effects on circuit performance. The following research gaps are addressed:

- Many reports are related to circular single gate transistors [46], [97], [98], [101]. To control the SCEs the concept of circular gate transistors with multiple gates is not reported.

- The impact of device level variations such as raised source/drain topologies and junctionless behaviour on circular MOSFETs has not been reported.
- The impact of device scaling, use of high-k dielectric materials and underlap concepts on device performance are not studied extensively.
- The implementation of stacked nanosheet MOSFETs with circular geometry to build high current integrated circuits has not been reported.
- Design and analysis of circular layout-based inverter cell and radiation effects on electrical performance is not reported.

Chapter-3

3. TCAD Calibration and Simulation Setups

The significance of this study using Visual TCAD [117] semiconductor simulator tool is explained in this chapter. Here, two well calibrated TCAD simulation setups are established as part of the thesis for different technology nodes. These calibration setups are included with suitable physical models related to mobility, carrier recombination, and bandgap narrowing effects along with quantization effects. The validation of simulation setups is achieved by simulating equivalent devices' reported structures (30 nm node [48] & 10 nm node [49]) and also matching their V-I characteristics. Further, this chapter consists of complete details of various model parameters used in the different simulation frameworks. Finally, it concludes with simulation setups related to the radiation effects such as TID and SEE effects [118][119].

3.1. Visual Technology Computer Aided Design: Visual TCAD

Cogenda's semiconductor simulation software consists of several sub tools. Some of the sub-tools used during this thesis work include Visual TCAD, Genius, Gds2Mesh, and VisualParticle.

Visual TCAD tool is a graphical user interface for carrying out device and circuit simulations. It is an electronic design automation tool that simulates the fabrication and operation of semiconductor devices. By incorporating several physical effects on device structures, the tool solves equations such as drift-diffusion, energy balance, and transport equations. It supports Two Dimensional (2D) and Three Dimensional (3D) device simulation, SPICE circuit simulation, and device/circuit mixed simulation. It consists of the following modules.

- Device structure drawing package for 2D devices.
- Circuit schematic capturing package for circuit simulations.
- Visualization package to examine the simulation output file generated by Genius.
- Spreadsheet package to view the data obtained from the simulation
- X-Y plotting package to plot the results obtained from the simulation.

Genius Simulator

Cogenda software includes a 'Genius' parallel 3D device simulator. It delivers unprecedented capacity and performance by using state-of-the-art parallel computing technologies that have become very affordable. This is a commercial device TCAD simulator that is scaled beyond the 10-transistor limit. The parallel computation in Genius can reduce simulation time by approximately ten times. Genius can simulate large device architectures as well as small circuit blocks containing many devices at the same time. In the Fig. 3.1, as the number of cores increases the simulation time reduces, and the simulation time is reduced by approximately 90 % when 32 core processor is used [120].

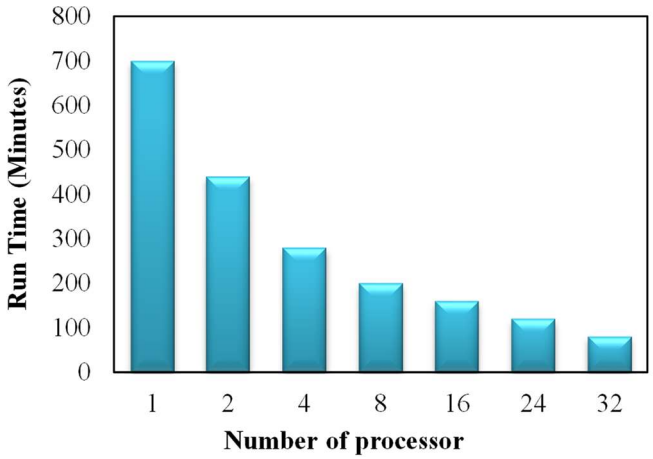


Fig. 3.1: Processor core (vs) Simulation time in minutes of a CMOS inverter in Genius [120].

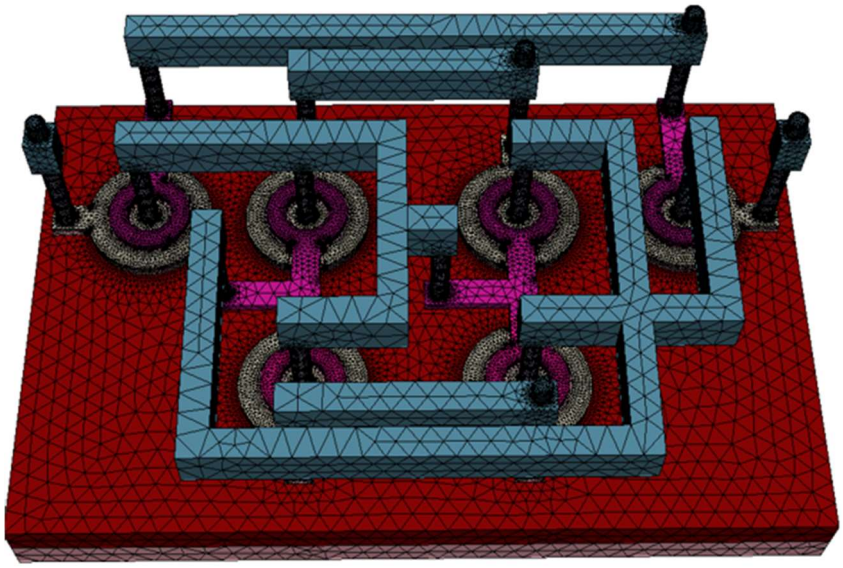


Fig. 3.2: Device modeling and mesh generation during Genius simulation.

Genius Simulator has many features which depend on device requirements & some other conditions. It includes a wide range of mobility models, Quantum model, Energy balance model, Impact ionization model, Lattice heating model, band-to-band tunnelling model, 3D TID model, device model generation from Geometric Database for Information Interchange (GDSII) mask layout etc. To extract the currents, it solves the Continuity and Poisson equations with one of the transport models (drift-diffusion model, Monte Carlo, etc.). Fig. 3.2 shows an example of a Genius parallel 3D device simulator. This diagram illustrates how devices are modelled (created) and meshes are generated during simulation.

Gds2Mesh

Gds2Mesh sub tool is an application for creating 3D TCAD models. It uses predefined and programmable process rules to build the device model using the GDSII mask layout as input [119]. i.e., it constructs 3D device models from planar mask layouts, according to a set of process rules and process parameters, by extruding 2D graphs into 3D objects. It is having some features such as python program interface, customized process rules with scripting, and high quality meshing, etc. For accurate simulation, the mesh has been fine tuned in the channel and junction regions after being automatically generated. To simulate the device, it can be imported into Genius [121].

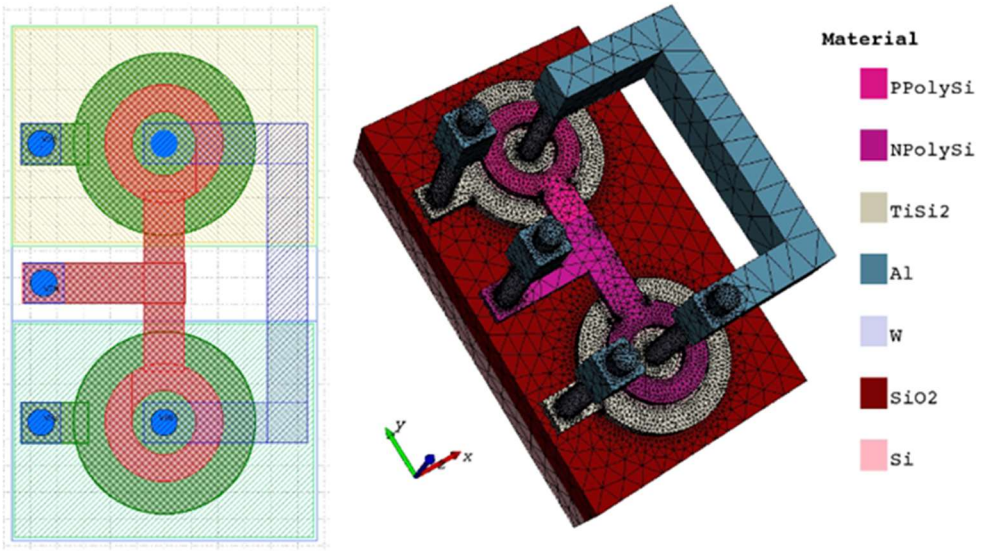


Fig. 3.3: (a) Layout of inverter, (b) corresponding 3D inverter.

Fig. 3.3 shows the CMOS inverter generated by using Gds2mesh. Mask layout of a CMOS inverter standard cell (left), and the TCAD model 3D inverter structure generated with

Gds2Mesh (right). Extrusion and other geometric operations are used in a properly defined process rule to extract the various layers from the mask set and construct the device geometry objects. Additionally, the positioning of doping profiles is determined by the mask layouts. One more feature of Gds2Mesh is the creation of Geometry Description Markup Language (GDML) files for VisualParticle/GSeat to analyze radiation effects. The major advantage of Gds2Mesh is that only one process file is required to create the individual devices (nmos or pmos) and circuits (inverter or SRAM, etc.).

VisualParticle/GSeat

Cogenda software has another attractive option to analyze the radiation effects known as the 'VisualParticle/GSeat' simulator. The graphical user interface for GSeat (Genius Single Event Analysis Tool) is called VisualParticle. The incident particle and simulation parameters can be set up by the user in the GUI, and they can also explore the simulated particle trajectory visually as shown in Fig. 3.4.

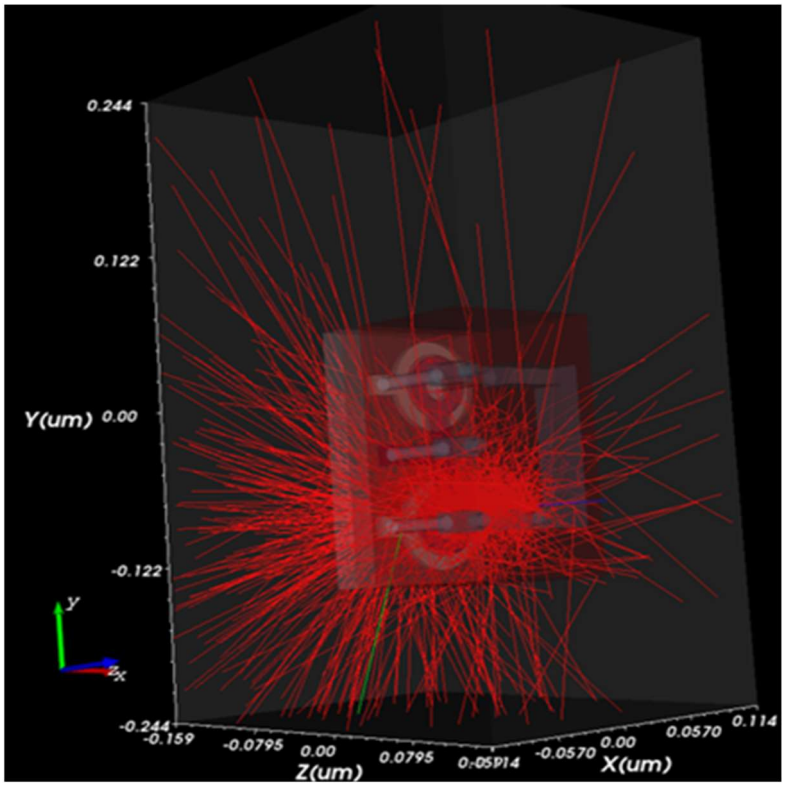


Fig. 3.4: Radiation tracks due to incident particles.

As a component of Cogenda's SEEs solution, GSeat is a Monte Carlo simulator for analyzing high-energy particles that are passing through semiconductors [122]. It is a well-known

custom-made simulator for high-energy space, physics, medical and radiation applications based on the Geant4 code. GSeat contains physics based models and databases related to SEEs. It is intended to be used in conjunction with the Genius 3D device simulator and Gds2Mesh model builder. These three tools serve as the foundation for Cogenda's SEE analysis package. GSeat produces particle trajectories and energy deposits along the trajectories, which causes carrier generation in the Genius TCAD simulation. GSeat's geometry is modelled in Geant4's GDML format. GDSII and process rules files can be used to generate a GDML format file using Gds2Mesh.

GSeat supports simulation of SEE caused by various particles such as alpha, heavy ion, proton, and neutron and for a wide energy range. Realistic physical models of the particles mentioned above have been implemented. The total energy deposit of the radiation event can be exported as plain text or in eXtensible Markup Language format. The energy deposit can then be used in conjunction with Genius tool to forecast the SEE of the device.

In addition to these, the following sub-tools that are not used during the simulation are given here.

Genes: It is a smart 2D process simulator for Silicon/Silicon Carbide devices. It simulates standard process simulation steps such as oxidation, epitaxial growth, deposition, silicidation, diffusion, etching, and ion implantation.

CRad: It is a tool for estimating the Total Displacement Dose, rate of SEE, and TID of semiconductor devices in space orbits.

VisualFab: It is a workbench that integrates process simulation experiments. It uses fab engineering concepts such as split, split table, wafer, and process module. It also enables users to visualize these experiments and design concepts in an easy-to-use graphical user interface (GUI).

3.2. Calibration Setup

In this thesis, the proposed different circular MOSFETs are implemented by using either Genius 3D device simulator or Gds2Mesh. To validate the simulation setup used in this thesis work, the simulated work is calibrated with the experimental work at both 30 nm and 10 nm

technology nodes. During the calibration, creating the experimental device with identical geometry, and also match their characteristic with the fine tune of appropriate physics models. The quantum confinement effect and scattering effects are considered during both calibrations.

3.2.1. 30 nm Technology Node

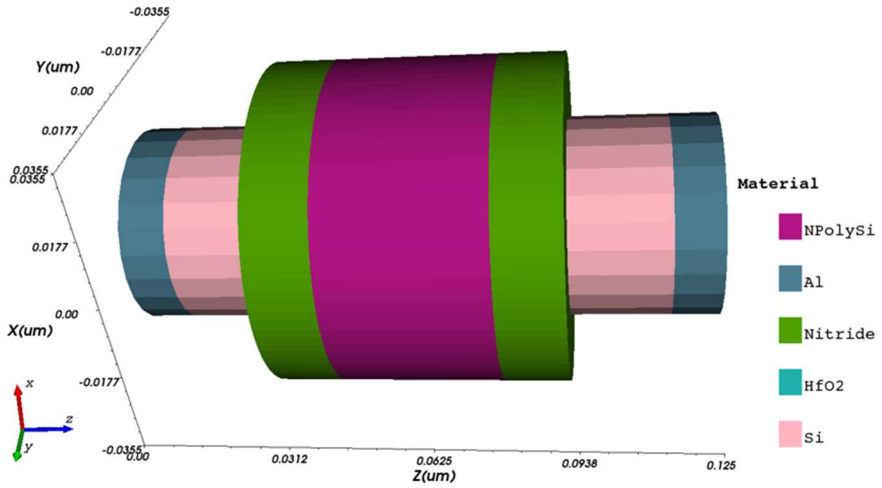


Fig. 3.5: 3D schematic view of calibrated NWFET structure at 30 nm node.

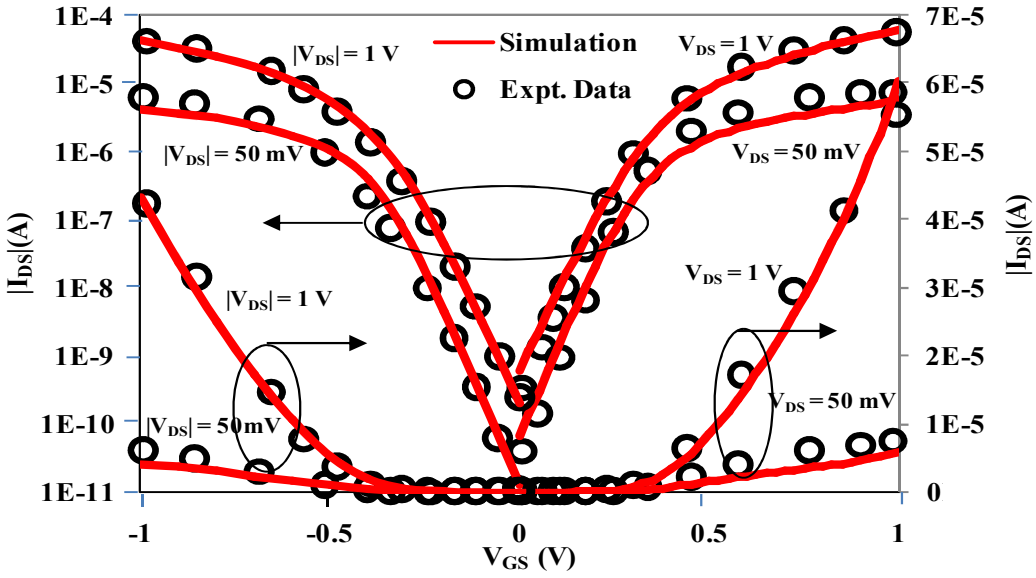


Fig. 3.6: Calibration with an experimental nanowire FET [48] at 30 nm.

Initially, the different circular MOSFETs are designed and simulated at 30 nm technology node. To validate the physical models that are employed for the device simulations, a

multigate NW FET matching the experimental device in [48] is designed, simulated and calibrated at 30 nm technology node.

According to geometrical parameters reported in [48] [123], NW FETs structures are created initially for NMOS (L or L_G = 35 nm, width of the NW = 13.3 nm, height of the NW = 20.4 nm, diameter of NW = 21.45 nm, Hf based dielectric (EOT) = 1.5 nm), and for PMOS (L or L_G = 25 nm, width of the NW = 9 nm, height of the NW = 13.9 nm, diameter of NW = 14.6 nm, Hf –based dielectric (EOT) = 1.5 nm). When the device structure matches the reported NW FET as shown in the Fig. 3.5, it is simulated with appropriate physical models to calibrate the experimental results. The simulation results are a good match with the experimental results for both NMOS and PMOS devices as shown in the Fig. 3.6. The linear characteristics are plotted by converting the log curve to ensure better calibration for above threshold region.

The following physics models are included in the simulation setup. The Quantum transport drift-diffusion correction model as given below is used in the simulation setup to account for quantum confinement effects. The quantum- corrected equation for electron and hole can be written as:

$$\Lambda n = - \frac{\hbar^2 \Upsilon_n \nabla^2 \sqrt{n}}{6 q m_n^* \sqrt{n}} \tag{3.1}$$

$$\Lambda p = \frac{\hbar^2 \Upsilon_p \nabla^2 \sqrt{p}}{6 q m_p^* \sqrt{p}} \tag{3.2}$$

Where, $\Upsilon_n = 3.6$ and $\Upsilon_p = 5.6$ are the correction of variation of effective mass. These two parameters ensure that these results are agree with those from Poisson-Schrödinger method and are obtained from Fermi-statistics. p and n are the hole and electron concentration, q represents the charge of an electron, m_p^* and m_n^* are the effective mass of hole and electron, and ħ is Planck's constant.

The Lucent high field mobility model considers the large field effects. This model uses the Caughey–Thomas model for the carrier velocity saturation (v_{sat0}) calculation. The v_{sat0} is adjusted to 1.6×10^7 cm.s^{-1} for NMOS device, and 1.4×10^7 cm.s^{-1} for PMOS device. The maximum mobility value (μ_{max}) was adjusted to 130 & 80 cm^2.V^{-1}.s^{-1} for both NMOS & PMOS devices respectively during calibration to match the ON current. The mobility degradation in the inversion layer due to acoustic phonon scattering and surface roughness scattering is considered to calculate carrier mobility.

For narrow bandgap effects caused by heavy doping, Schenk's bandgap narrowing model is used. The most important and fundamental physical parameters for a semiconductor material are the band structure parameters, which include effective density of states in the valence band Nv and conduction band Nc, bandgap Eg, and intrinsic carrier concentration n_{ie}. The following is the definition of the effective density of states in valence and conduction bands:

$$N_v = 2\left(\frac{m_p{}^* k_b T}{2\pi\hbar^2}\right)^{3/2} \tag{3.3}$$

$$N_c = 2\left(\frac{m_n{}^* k_b T}{2\pi\hbar^2}\right)^{3/2} \tag{3.4}$$

High carrier lifetimes are taken into account in Shockley-Read-Hall recombination, while high current densities are taken into account in Auger recombination. The Selberherr impact ionization model is employed for the generation rate of the electron–hole pair due to the carrier Impact Ionization. The Fermi–Dirac statistics are included because the source/drain is heavily doped. The direct tunneling model to account for gate tunneling currents, and WKB was used to calculate the electron/hole tunneling currents.

Finally, to match the threshold voltage of the experimental device, the metal gate work function was adjusted to 4.46 eV for NMOS and 4.7 eV for PMOS respectively. The surface interface effects are not considered during the simulations.

3.2.2. 10 nm Technology Node

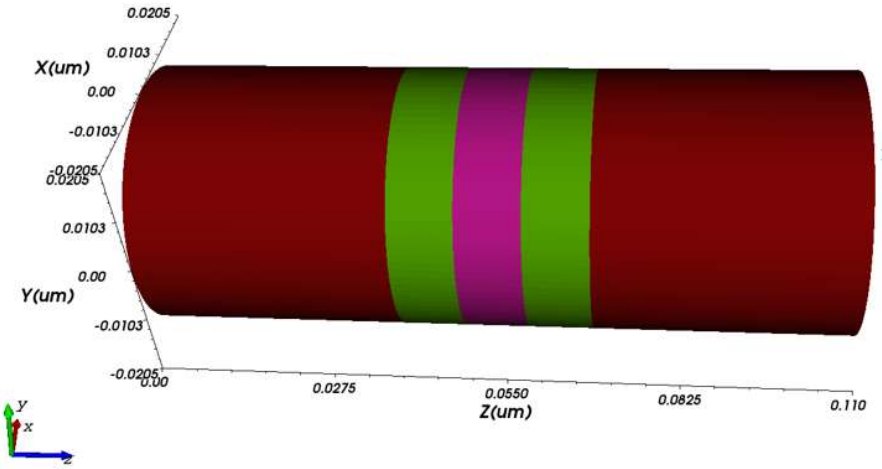


Fig. 3.7: 3D schematic view of calibrated NWFET structure at 10 nm node.

As the advanced technology node has entered the sub 10 nm regime & the thesis work is mainly focused on the analysis of the proposed circular MOSFETs at the lower sub 10 nm nodes, the setup was further calibrated at a shorter L_G of 10 nm. During this, experimental work (a multigate nanowire FET) Ming et al.[49] was used for calibration.

Initially, according to geometrical parameters reported in [49], NW FETs structures are created for NMOS (L_G = 10 nm, diameter of NW = 16 nm, T_{ox} = 2.5 nm), and for PMOS (L_G = 10 nm, diameter of NW = 13 nm, T_{ox} = 2.5 nm). When the device structure matches the reported NW FET [49] as shown in the Fig. 3.7, it is simulated with appropriate physical models to calibrate the experimental results.

The simulation results are a good match with the experimental results for both NMOS and PMOS devices as shown in the Fig. 3.8. The linear characteristics are plotted by converting the log curve to ensure better calibration for above threshold region.

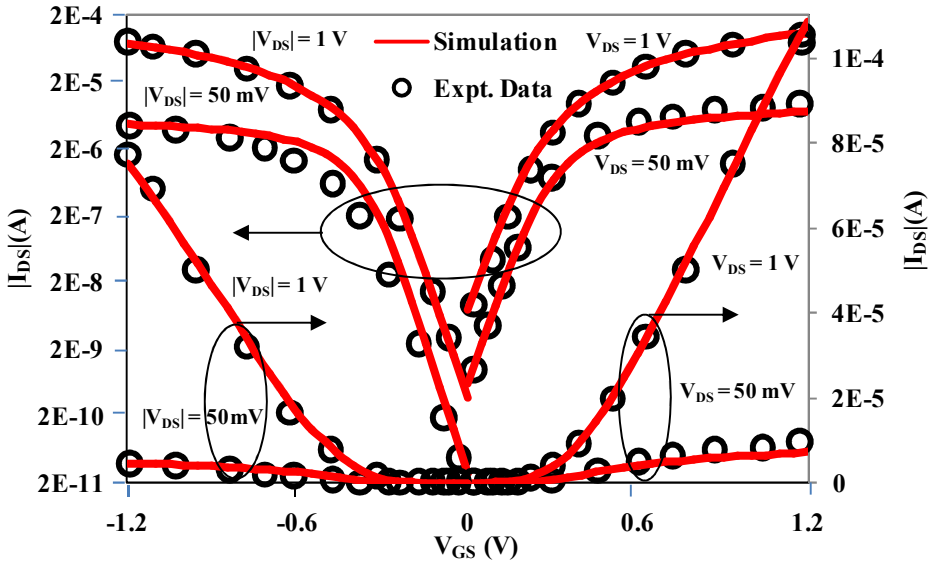


Fig. 3.8: Calibration with an experimental nanowire FET [49] at 10 nm.

The setup also includes some other or additional models in addition to the physical models mentioned in section 3.2.1. The quantum density gradient model is included for quantum correction effects. The Lombardi surface mobility model is used to describe the carrier mobility in the MOSFET inversion layer. To calculate the carrier mobility, the mobility degradation in the inversion layer due to acoustic phonon scattering and surface roughness scattering, as well as doping-dependent bulk mobility for ionized impurity scattering, are considered. The carrier velocity saturation (v_{sat0}) is adjusted to 2.2 × 10^7 cm.s^{-1} for NMOS

device, and 2.1 × 10^7 cm.s^{-1} for PMOS device. The maximum mobility value (μ_{max}) was adjusted to 830 & 400 $cm^2.V^{-1}.s^{-1}$ for both NMOS & PMOS devices respectively during calibration to match the ON current.

Because the channel length is 10 nm, Kane's band-to-band tunneling model is used to account for band-band tunneling [124][125], and it is expressed as follows,

$$G^{BB} = D \times A.BTBT.\frac{E^{BBT.GAMMA}}{\sqrt{E_g}} \times exp\left(-B.BTBT \times \frac{{E_g}^{3/2}}{E}\right) \quad (3.5)$$

Where E denotes the magnitude of the electrical field, E_g denotes the material's band gap, and A.BTBT and B.BTBT are the empirical fitting parameters. The statistical factor is denoted by D. The value of D is one or the eq. 3.6 as suggested by Hurkx.

$$D_{Hurkx} = \frac{n_{ie} - np}{(n + n_{ie})(p + n_{ie})} \quad (3.6)$$

Finally, to match the threshold voltage of the experimental device, the metal gate work function was adjusted to 4.5 eV for NMOS and 4.72 eV for PMOS, respectively.

3.3. Simulation Setups for Radiation Effects Analysis

3.3.1. Simulation Setup for TID Effect in Semiconductor Devices

One of the most noticeable effects on irradiated semiconductor devices is the TID. MOS devices historically were considered robust specifically to the TID effects. This viewpoint has shifted drastically since deep-submicron CMOS technologies have become mainstream. TID effects in CMOS thin gate oxides are significantly reduced for thicknesses less than 10 nm. However, in modern CMOS technologies, the thick oxide layer in shallow trench isolation does not scale down. As a result, source-drain and inter-diffusion leakage currents are the primary TID concerns in deep-submicron CMOS technologies [126].

The dose for this TID process simulation is defined by the totaldose (rad) parameter, the dose rate by the dose rate parameter (rad/s), and the step size of increasing dose by the dose step parameter (rad). To achieve stable convergence in TID simulation, gradually increase the dose and perform a global potential update every 0.5 Krads. The TID command flow chart is shown in Fig. 3.9.

The example of the TID command is given as follows.

TID type=advanced totaldose=100 × 10^6 doserate=10 dosestep=0.5 × 10^3

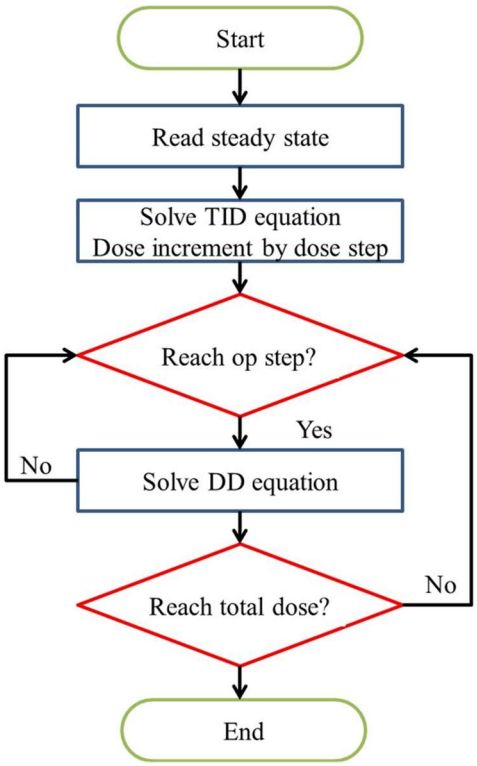


Fig. 3.9: TID command flow chart [126].

Cogenda TCAD employs Rowsey's doctoral thesis [127] physical model of TID in SiO_2 layer, which estimates carrier transport, recombination, generation, and trapping. The 'TID' command in Genius instructs the simulator to solve the required equations such as electron continuity equation, hole continuity equation, Poisson equation, and the trap-de trap equation to calculate the fixed-charge generation as listed below [128].

$$\frac{d^2\emptyset}{dx^2} = -\frac{\rho}{\varepsilon_s} = -\frac{q}{\varepsilon_s}(p + N_a - n) \tag{3.7}$$

$$\frac{dn}{dt} = \nabla f_n + G_n - R_n \tag{3.8}$$

$$\frac{dp}{dt} = \nabla f_p + G_p - R_p \tag{3.9}$$

$$\frac{dT_p}{dt} = R_p - R_n = \sigma_{pta}|f_p|T_a - \sigma_{nta}|f_p|(T_a - T_b) \tag{3.10}$$

Where $\boldsymbol{f_n} = \boldsymbol{\mu_n nE} + \boldsymbol{D_n \nabla_n}$, and $\boldsymbol{f_p} = \boldsymbol{\mu_p pE} + \boldsymbol{D_p \nabla_p}$

G and R = Generation and Recombination of charge carriers

f_n and f_p = The local electrons and holes current density respectively,

σ_{pta} = Hole capture rate at neutral trap A (cm^2),

σ_{nta} = Electron capture rate at positively charged trap A (cm^2),

T_a = Density of trap A (cm^{-3}).

Genius provides various TID models, like basic, advanced, and full models. The basic type of TID solver only calculates the bulk trap density in oxide region. This basic type of solver is suitable for TID effect simulation of CMOS up to 1×10^6 rad. Furthermore, the advanced type TID solver also considers the interface trap density and stores the result as interface charge profile. In most cases, a relatively simple model that describes the generation of fixed charge in the oxide is sufficient for CMOS devices subjected to a moderate amount of dose. The total ionizing dose and dose rate can be entered directly by the user, and Genius will calculate the oxide charge density produced in the insulators.

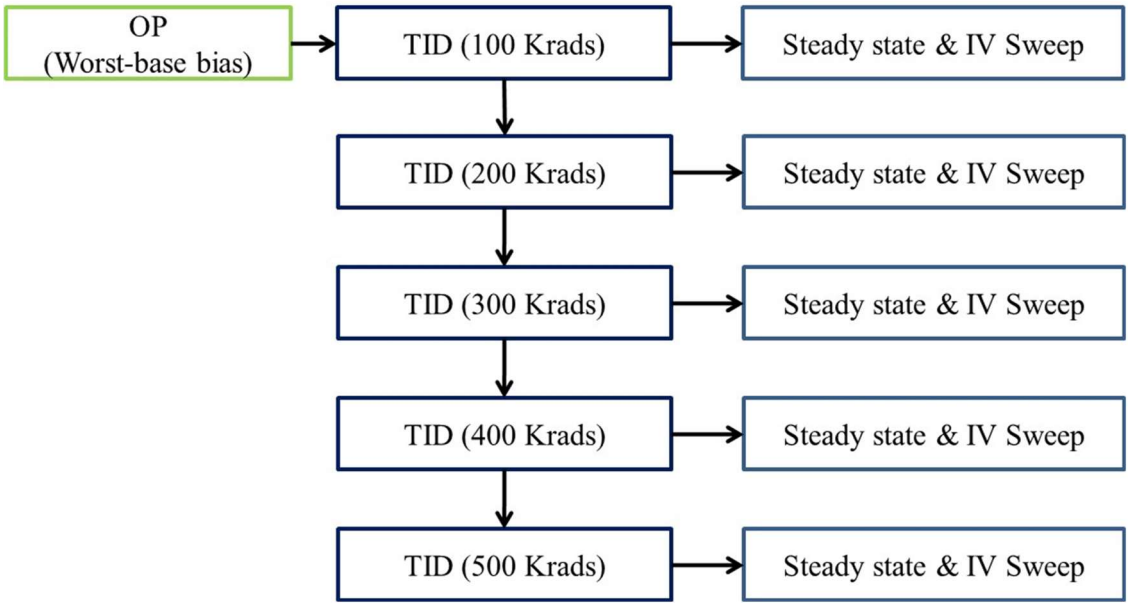


Fig. 3.10: TID simulation flow chart [126].

To avoid underestimating the device's damage, the device is biased in the OP simulation prior to the TID simulation. For CMOS bulk devices, the "worst-case" bias is to ground all terminals except the gate, which is held at supply voltage (V_{DD}). Fig. 3.10 depicts the simulation flow of TID effects. It is intended to simulate the MOSFET IV curves under different doses. As a result, prepare five irradiated device states for doses ranging from 100 to 500 Krad, and then begin an IV sweep simulation from each state.

3.3.2. Simulation Setup for Single Event Effects (SEE) in CMOS Circuits

GSEAT & Visual Particle sub tools provided by Cogenda software to analyze the radiation effects (SEEs) [129]. The Geant4-based GSeat is a computer program that can be used to investigate the SEE effects of microelectronics in radiation environments. The detailed 3D structure of the device is required for SEE simulation. The device structure generated by the Gds2Mesh tool in GDML format can be loaded into GSeat.

The GDML file containing the geometry and material details of the device as well as information about the particles, including particle type, energy, and track, are included in the GSeat input along with a few control arguments.

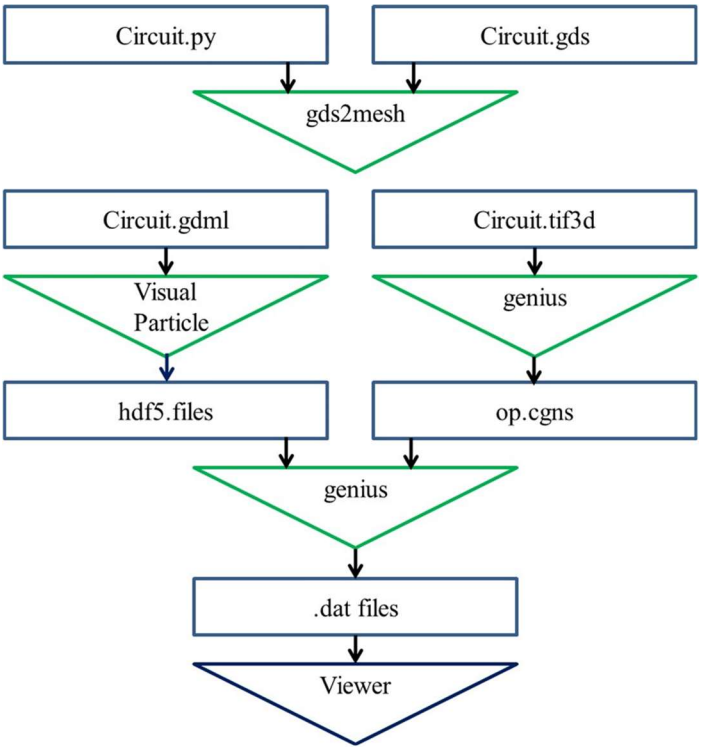


Fig. 3.11: Modeling flow (steps and tools) [130].

Cogenda provides an intuitive GUI called VisualParticle. This GUI makes it easier for the user to see the structure of the device, incident particle setting and run time parameters, and complete GSeat simulation post-processing.

The flow chart shown in Fig. 3.11 is followed to analyze the radiation effects in Cogenda Visual TCAD software. The flowchart in Fig. 3.10 lists the steps and tools used. Note that the rectangular represent input/output files and the triangles represent simulation tools.

Chapter-4

4. Design of Circular MOSFETs

As mentioned in Chapter 1 and 2, the circular MOSFET is one of the alternative devices to mitigate SCEs. These circular MOSFETs are better immune to corner effects and radiation due to their enclosed circular gate layout. As mentioned in Chapter 2, the circular MOSFETs with internal drain configuration are considered throughout the work due to the performance advantage. To further extend the life of planar and SOI technology based devices, in this work, single circular gate SOI MOSFET is analyzed and proposed double circular gate SOI MOSFETs at lower technology nodes with an internal silicon pad acting as a drain.

4.1. Circular Single Gate Transistor (CSGT)

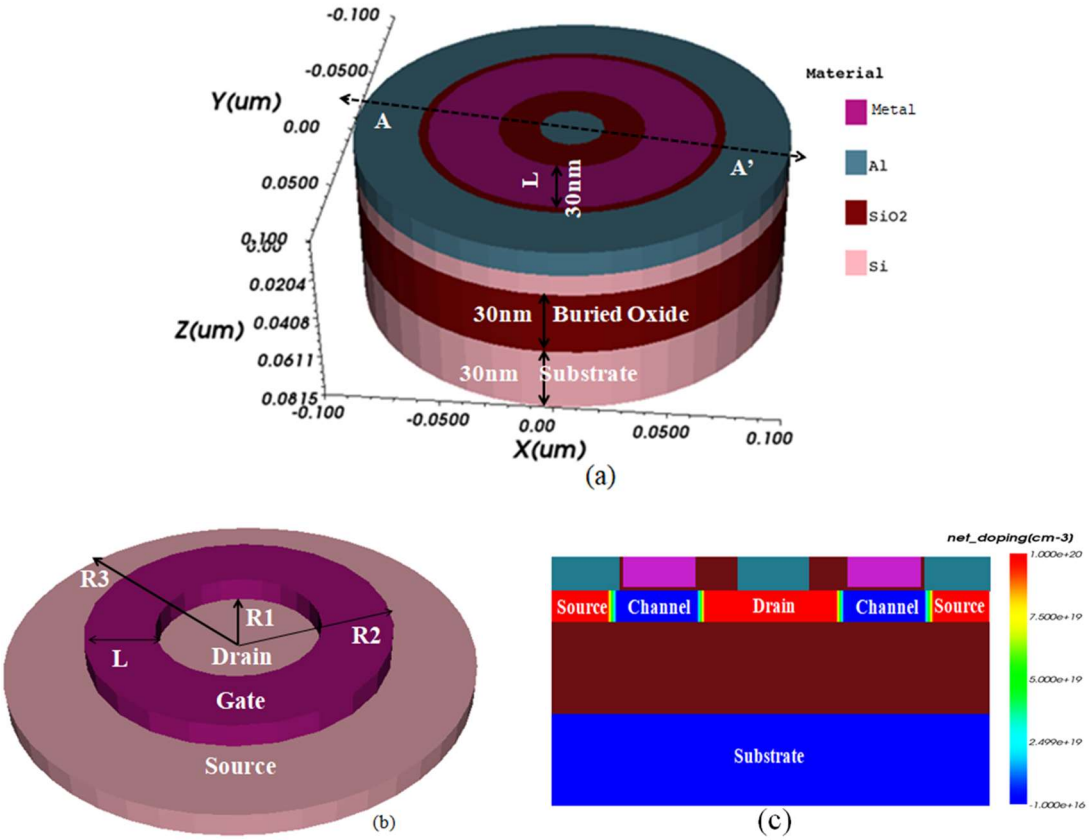


Fig. 4.1: (a) 3D view of a circular gate SOI MOSFET, (b) 3D-CSGT, (c) 2D-CSGT with doping profiles.

A 3D isometric view of CSGT SOI MOSFET with geometric details is shown in Fig. 4.1(a); after removing the oxide and substrate layers, 3D view of the CSGT structure is shown in Fig. 4.1(b). Fig. 4.1(c) depicts the corresponding 2D cross-sectional view across the cutline A-A′ with doping profiles. The region defined by the circle with the radius R1 is assigned as the drain, the region defined by the ring between R2 and R1 represents the channel or gate, and the outer ring between R3 and R2 is assigned as the source. Hence, the technology node or the channel length of CSGT can be defined as L = R1 – R2. Furthermore, the important dimensions in terms of the technology node are defined as R1 = L, R2 = 2L, and R3 = 3L. The CSGT fabrication process is compatible with traditional planar rectangular gate transistor fabrication [95][45].

4.2. Circular Double Gate Transistor (CDGT)

4.2.1. CDGT Device Structure

The 3D view of CDGT SOI MOSFETs is similar to the CSGT device as shown in Fig. 4.1(a); after removing the oxide and substrate layers, 3D view of the CDGT device is shown in Fig. 4.2(a). The corresponding 2D cross-sectional view across the cutline A–A′ with doping profiles is shown in Fig. 4.2 (b). The CSGT fabrication process is compatible with traditional planar rectangular gate transistor fabrication [95][45].

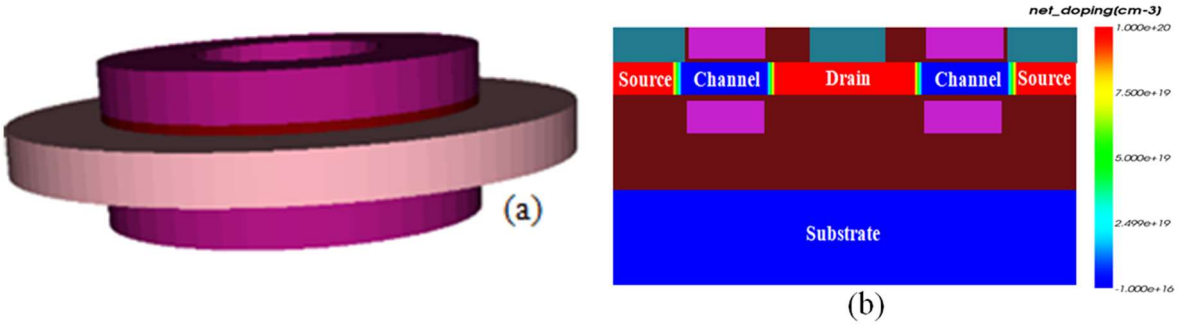


Fig. 4.2: (a) 3D view of a circular double gate SOI MOSFET, (b) 2D-CSGT with doping profiles.

4.2.2. CDGT Fabrication Process

The 3D view of the fabrication process of the proposed CDGT SOI MOSFET is shown in Fig. 4.3. Similar to CSGT, the CDGT SOI fabrication process is compatible with the planar double-gate SOI fabrication process [131].

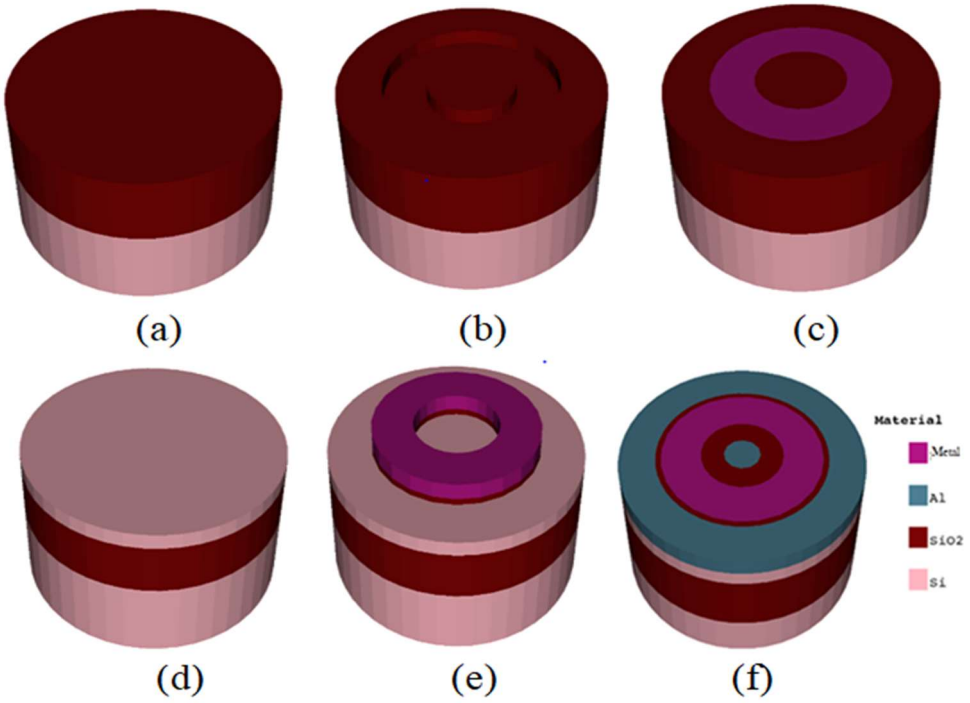


Fig. 4.3: Fabrication process of the CDGT SOI MOSFET. (a) Bulk silicon wafer is thermally oxidized, (b) Lithography and patterning the bottom gate cavities, (c) bottom metal gate deposition and patterning, (d) deposition of active silicon and patterning, (e) top gate oxidation, metal gate deposition, patterning, and doping, (f) metallization.

The fabrication process of CDGT starts with the bulk silicon wafer which is first thermally oxidized to obtain the structure shown in Fig. 4.3 (a). The bottom gate cavities are then patterned using a sulfur hexafluoride based RIE plasma to obtain the structure shown in Fig. 4.3 (b). The cavities are then filled with the metal gate using chemical vapor deposition, which is followed by RIE [131] and chemical mechanical polishing resulting in Fig 4.3. (c). In the next step, deposition of the silicon layer through epitaxy (which inherently includes the active silicon oxidation when deposited on metal [132][133] is followed by active island patterning, resulting in the structure shown in Fig 4.3. (d). After this, thermal oxidation is performed to obtain the top gate oxide which is followed by metal filling and patterning to form the top gate as shown in Fig 4.3. (e). The Source/Drain (S/D) doping is then done with the top gate protecting the channel region. In the last step, metallization and isolation are performed, as shown in Fig. 4.3. (f).

4.3. Simulation Methodology of CSGT and CDGT Devices

The performance analysis of CSGT and CDGT SOI MOSFETs is carried with identical geometrical parameters. Some of the essential device parameters used in the simulation study of the CSGT and the CDGT are given in Table 4.1.

Table 4.1: Geometrical details of CSGT and CDGT devices used in the simulation.

Device type	**CSGT**		**CDGT**	
Parameter	**NMOS**	**PMOS**	**NMOS**	**PMOS**
L_G or L	30 nm			
Buried Oxide (BOX)	30 nm			
T_{OX}	1.5 nm			
S/D and Channel thickness	10 nm			
Gate thickness	10 nm			
Source/ Drain doping (cm^{-3})	1×10^{20}			
Channel doping (cm^{-3})	1×10^{16}			
Substrate doping (cm^{-3})	1×10^{15}			
$\lvert V_{DD} \rvert$ (V)	0.9			

The calibrated simulation setup described in Chapter 3 is used in this analysis [48] [123]. Initially, during the simulation process, to match the device $V_{TH} \sim |0.25|$ V) for both NMOS and PMOS devices with the ITRS 2013 projections [134] (using the constant current method), adjustments are done to the device parameters such as the gate work function (n-CSGT: Φ_m = 4.54 eV; p-CSGT: Φ_m = 4.72 eV; n-CDGT: Φ_m = 4.48 eV; p-CDGT: Φ_m = 4.76 eV), and the channel doping is set to 1×10^{16} cm^{-3} for both CSGT and CDGT. The threshold voltage is obtained using the constant current method, i.e., V_{TH} is taken from the curve of the drain current (I_{DS}) versus V_{GS} by considering the value of V_{GS} at a drain current $I_{DS} = (W/L) \times 10^{-7}$ A μm^{-1}.

Where, W is the effective width of the channel, and L is the channel length. The Circular MOSFET's device geometrical factor in terms of effective channel width (W_{Rect}) and channel/gate length (L) of the conventional rectangular gate transistor is given by Eq. (1) [46],

$$\left[\frac{2\pi}{\ln(R2/R1)}\right]_{Circular} = \left(\frac{W}{L}\right)_{Rectangular} \tag{4.1}$$

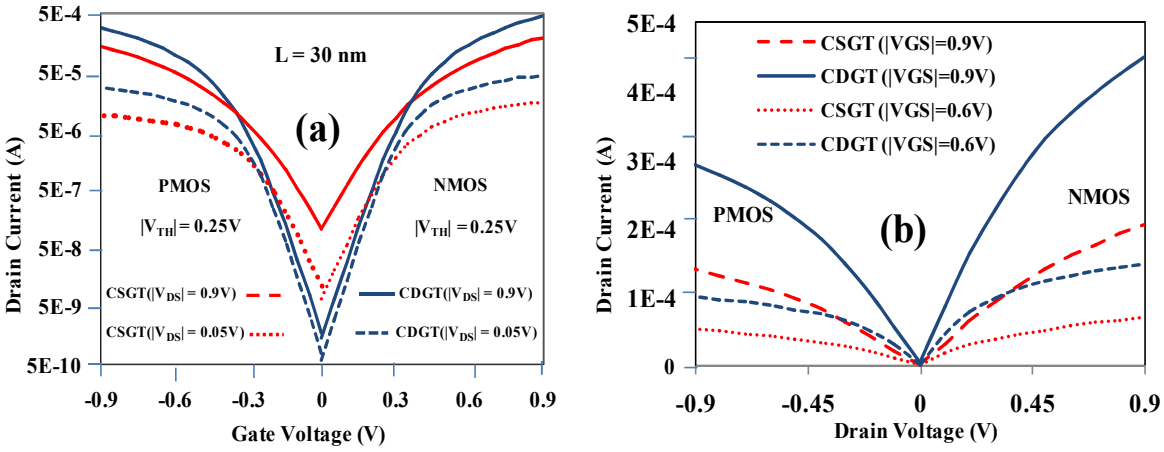


Fig. 4.4: (a) I_{DS}–V_{GS} of the CSGT and the CDGT for both NMOS and PMOS devices with L and V_{TH} values shown inset, (b) I_{DS}–V_{DS} of the CSGT and the CDGT devices.

Fig. 4.4 presents the simulation results of the CSGT and CDGT for both NMOS and PMOS devices using the calibrated setup. Fig. 4.4 (a) shows the I_{DS}–V_{GS} characteristics for low and high V_{DS} of both the CSGT and the CDGT after tuning the work function to match the V_{TH} (~|250 mV|). Fig. 4.4 (b) shows the corresponding I_{DS}–V_{DS} characteristics. In Fig. 4.4, it can be observed that the proposed CDGT shows better results compared to the CSGT in terms of I_{ON}/I_{OFF} ratio that is close to 10^6 (n-CDGT: 6.75×10^5; p-CDGT: 3.16×10^5), near ideal SS (n-CDGT: 70.2 mV dec^{-1}; p-CDGT: 70.6 mV dec^{-1}), and smaller DIBL (n-CDGT: 42.9 mV V^{-1}; p-CDGT: 46.7 mV V^{-1}). Here, DIBL is defined as the difference in threshold voltage between V_{DS} (low) = 0.05 V and V_{DS} (high) = 0.9 V with respect to a change in V_{DS}. All the relevant numerical values are summarized in Table 4.2. The important characteristics are highlighted in bold font.

Table 4.2: Performance Comparison of CSGT & CDGT SOI MOSFETs.

Device type	**CSGT**		**CDGT**	
Parameter	**NMOS**	**PMOS**	**NMOS**	**PMOS**
Work function (eV)	4.54	4.72	4.48	4.76
I_{ON} (mA)	0.27	0.2	**0.52**	**0.33**
I_{OFF} (nA)	88.1	133	**0.77**	**1.06**
I_{ON}/I_{OFF} ($\times 10^3$)	3.06	1.51	**675**	**316**
SS (mV/dec)	98	101	**70.2**	**70.6**
DIBL (mV/V)	162	181.5	**42.9**	**46.7**
C_{gg} (F)	3×10^{-16}	3.1×10^{-16}	3.7×10^{-16}	4.1×10^{-16}
Intrinsic delay (s)	1×10^{-12}	1.4×10^{-12}	6.4×10^{-13}	1.1×10^{-12}

4.4. Raised Source/Drain CDGT Structures

From the results of the previous analysis, the CDGT shows better electrical properties when compared to the CSGT. The SOI MOSFET performance is limited due to the source and drain contact resistances in the sub 32 nm regime. This is due to the fact that while contact resistance increases with contact area scaling, the ON-state resistance of a MOSFET decreases with the scaling of the transistor. One common method for reducing the series resistance component is by raised S/D engineering [53].

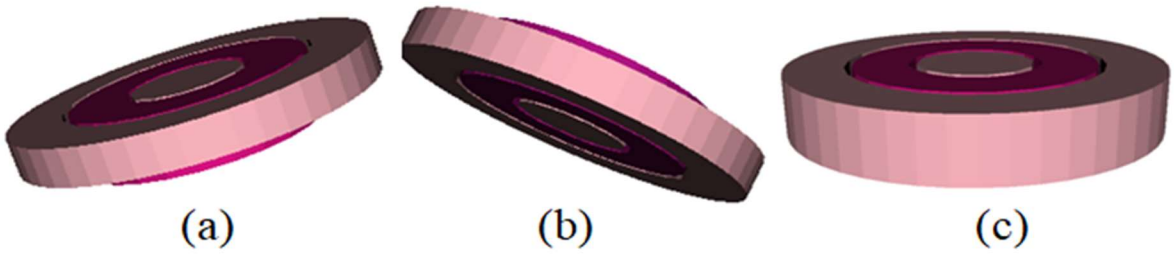


Fig. 4.5: 3D view of CDGT SOI MOSFET with Source/Drain (a) raised top, (b) raised bottom, (c) raised top and bottom ('both') structures.

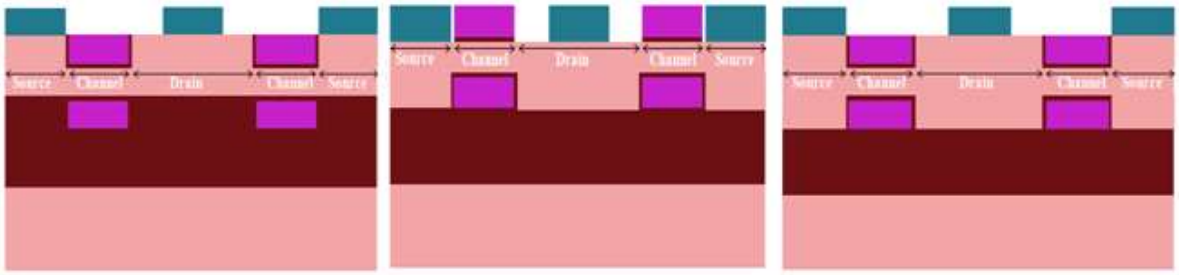


Fig. 4.6: 2D cut view of raised top, raised bottom, and raised 'both' CDGT SOI MOSFETs.

Raised S/D structures have shown promise in mitigating the parasitic resistances associated with the source and drain, improving ON current, reducing the lateral electric field, controlling hot carrier effects, and improving device performance [12]. Hence, the authors propose to extend the performance of the CDGT SOI MOSFETs using a raised structure and to find the best configuration among them. Fig. 4.5 shows a 3D schematic view of a CDGT with various raised S/D structures such as a raised top (Fig. 4.5 (a)), a raised bottom (Fig. 4.5 (b)), and a raised top and bottom, known here as 'both' (Fig. 4.5 (c)). The corresponding 2D views are shown in Fig. 4.6.

Fig. 4.7 shows the surface potential and electric field characteristics along the channel length from the left side (Drain edge) to the right side (Source edge) of various raised

structures. In this Fig. 4.7, it is evident that the surface potential is higher, and the electric field is lower for 'both' raised CDGT structures compared to a regular CDGT at the drain/channel interface. Due to its higher barrier potential, and electric field lower at drain/channel interface, the hot carrier effects (HCEs) and off-state leakages are reduced for 'both' raised CDGT structures and improve the device performance.

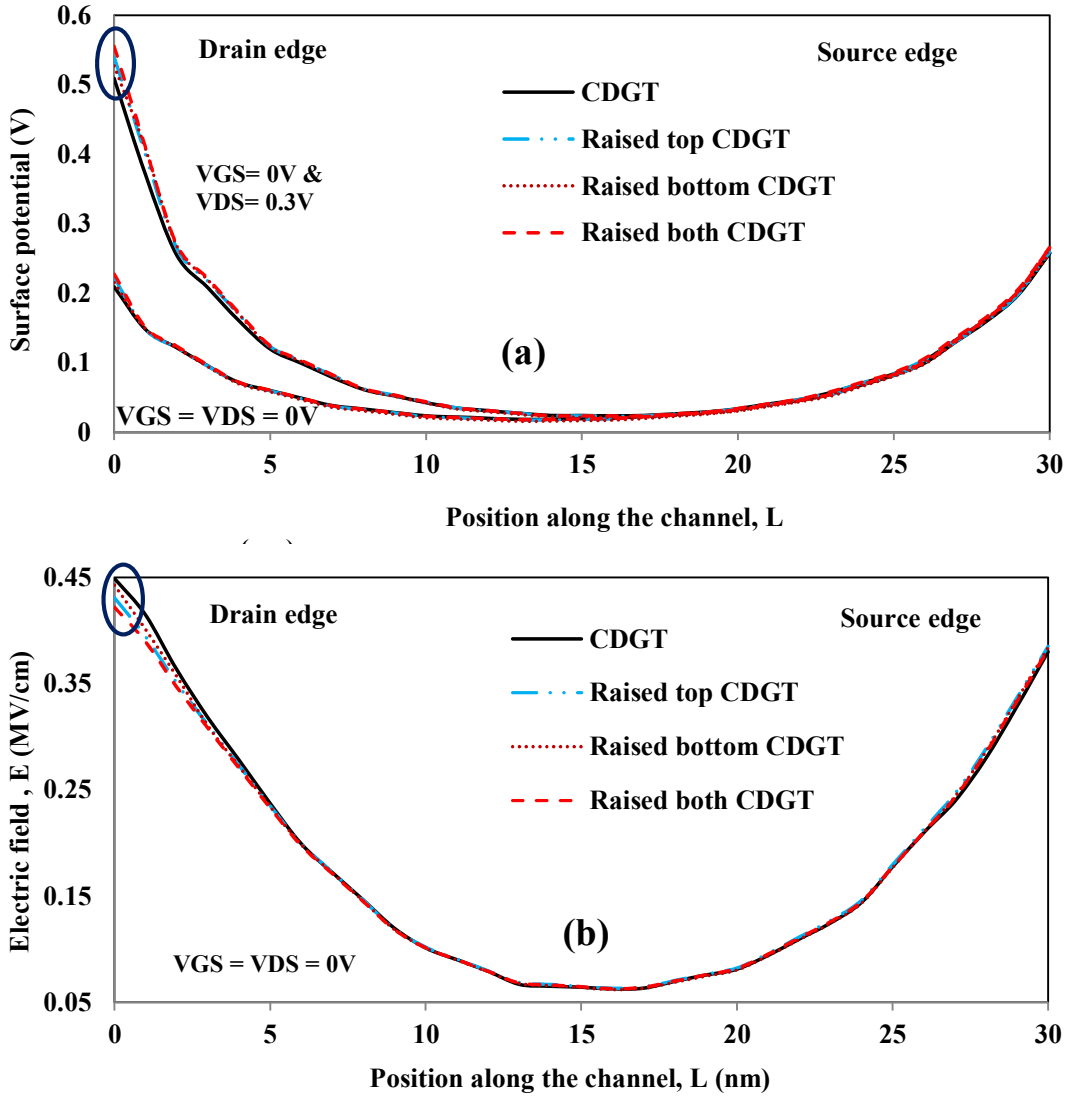


Fig. 4.7: (a) Surface Potential, (b) Electric field along the channel for various raised structures.

Fig. 4.8 shows the effective mobility at different gate voltages, V_{GS}= 0V, 0.3V, 0.6V, 0.9V, and V_{DS}=0.9 V for the structures for the different raised CDGT structures. In the Fig. 4.8, at high gate voltage, the mobility in raised both is higher which is attributed to the higher area on drain/channel & source/channel interfaces of raised both structures. Further, the spreading

resistance associated with the source/channel edge & drain/channel edge reduces and the sheet resistance of the source, drain region also reduces, thus increasing the drain current.

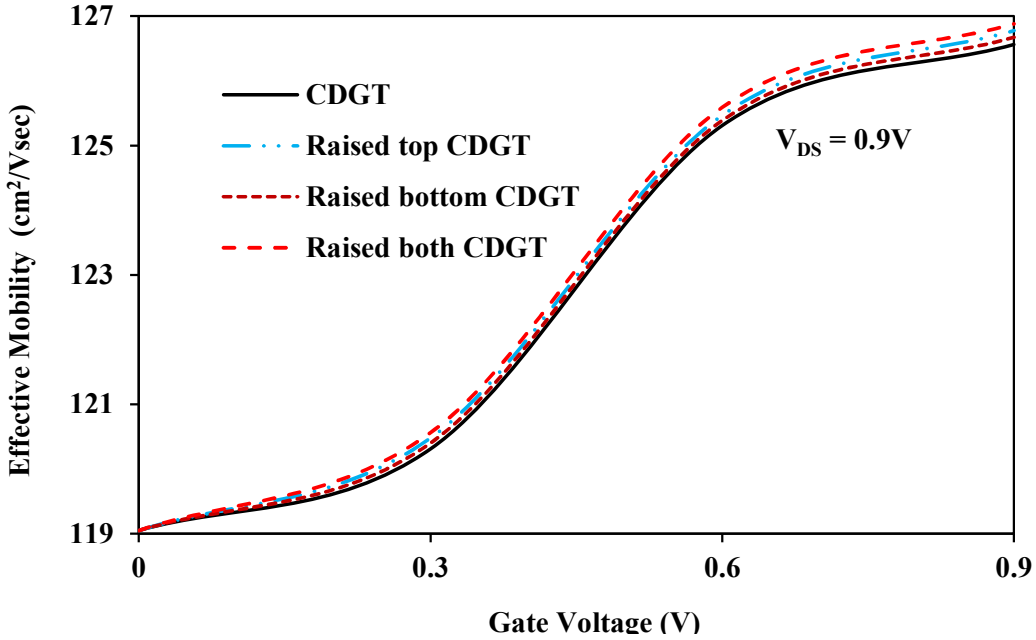


Fig. 4.8: Effective mobility (vs) V_{GS} for different raised CDGT structures.

The calibrated simulation setup presented in previous section is used for all these different raised structures (Fig. 4.5). To understand the advantage of raised structures, the authors compare these devices in terms of the device level FoM. Here, the FoM, such as I_{ON}, I_{ON}/I_{OFF}, SS, and DIBL are compared. In the proposed NMOS raised top, bottom, and 'both' CDGT SOI MOSFETs, the I_{ON} values (V_{GS} = 0.9 V, V_{DS} = 0.9 V) are 0.54, 0.53, and 0.56 mA, respectively, and for the PMOS raised top, bottom, and 'both' CDGTs, they are 0.35, 0.34, and 0.36 mA, respectively. The I_{ON}/I_{OFF} ratios for the NMOS raised top, bottom, and 'both' CDGTs are, respectively, 7.15×10^5, 7.02×10^5, and 7.47×10^5. The I_{ON}/I_{OFF} values for the PMOS raised top, bottom, and 'both' CDGTs are, respectively, 3.45×10^5, 3.38×10^5, and 3.56×10^5. The SSs for the NMOS raised top, bottom, and 'both' CDGTs are, respectively, 69.4, 69.5, and 69.3 mV dec^{-1}. The DIBLs for the NMOS raised top, bottom, and 'both' CDGTs equal 43.1, 42.7, and 43.2 mV V^{-1}, respectively. Finally, the DIBLs for the PMOS raised top, bottom, and 'both' CDGT SOI MOSFETs are 47.1, 46.6, and 47.2 mV V^{-1}, respectively.

The extracted SCE parameters for different raised S/D structures (NMOS and PMOS devices) are given in Table 4.3. The 'both' raised SOI CDGT exhibits better electrical properties compared to all other structures. Because its structure is raised on both sides, the parasitic series resistance associated with the S/D is reduced, thus the device's ON current

improves by 7%, and the overall I_{ON}/I_{OFF} is improved by 11% compared to the CDGT SOI MOSFET.

Table 4.3: Important simulated numerical values for 30 nm gate length CDGT SOI MOSFETs with normal and raised S/D structures (raised top, raised bottom and both raised).

Device type	**CDGT**		**Raised top CDGT**		**Raised bottom CDGT**		**Raised both CDGT**	
Parameter	**NMOS**	**PMOS**	**NMOS**	**PMOS**	**NMOS**	**PMOS**	**NMOS**	**PMOS**
Work function (eV)	4.48	4.76	4.48	4.76	4.48	4.76	4.48	4.76
I_{ON} (mA)	0.52	0.33	0.54	0.35	0.53	0.34	**0.56**	**0.36**
I_{OFF} (nA)	0.77	1.06	0.75	1.03	0.76	1.04	**0.75**	**1.01**
I_{ON}/I_{OFF} ($\times 10^5$)	6.75	3.16	7.15	3.45	7.02	3.38	**7.47**	**3.56**
SS (mV/dec)	70.2	70.6	68.3	69.4	68.4	69.5	68.2	69.3
DIBL (mV/V)	42.9	46.7	43.1	47.1	42.7	46.6	43.2	47.2

4.5. JL Mode Analysis of Raised 'both' CDGT MOSFETs

Since our previous analysis of different raised CDGT topologies revealed that the 'both' raised CDGT provides better performance than the other two, this device's performance is further analyzed by employing the JL concept, which is a better doping option for short-channel devices.

This work is mainly focused on the sub 30 nm technology node, and at these nodes, it is difficult to modify the doping concentration and obtain high-quality junctions in thin SOI layers. Hence, JL transistors have uniform doping in the entire silicon film (channel, source, and drain regions) [54].

The JL mode has gained much attraction in recent years, and has several benefits over traditional planar MOSFETs, such as enhanced performance against SCEs, high scalability, a low thermal budget, and a simplified fabrication process [55]. The lower electric field in the channel also decreases the degradation of field mobility compared with conventional junction-based transistors [56]. Such gains are only achieved because of the high current drive with no barrier in JL devices.

The same simulation setup is used for a JL raised 'both' CDGT with different doping profiles such as 1×10^{17} cm^{-3}, 5×10^{17} cm^{-3}, 1×10^{18} cm^{-3}, 5×10^{18} cm^{-3}, and 1×10^{19} cm^{-3}. Here, these various JL devices are adjusted to the ($|V_{TH}| \sim 0.25$ V) by tuning the metal gate's work function to find the optimum doping.

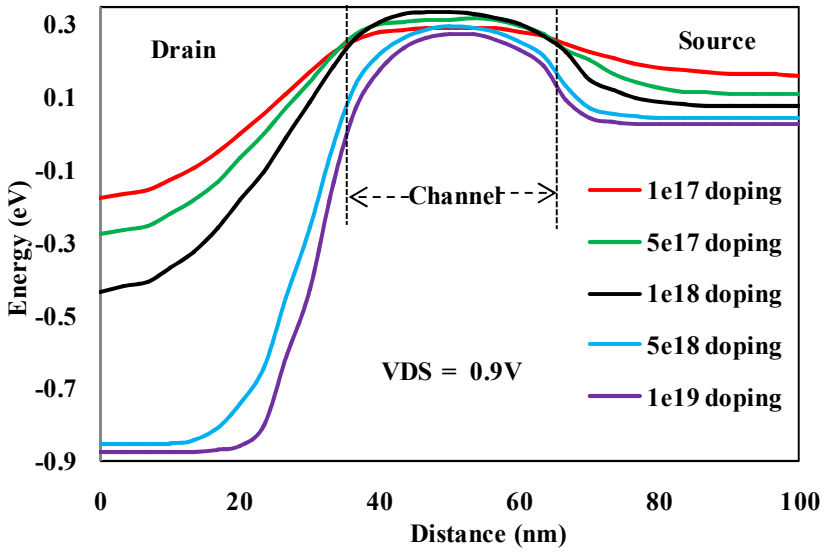


Fig. 4.9: Conduction band energy in the lateral direction for various doping concentrations.

Fig. 4.9 shows the conduction band in the lateral direction of the device in the OFF state for a JL analysis of the raised 'both' CDGT structure. In this Fig. 4.9, it can be observed that (a) the conduction energy at the drain/channel interface is reduced more for higher doping concentrations (5×10^{18} cm^{-3} and 1×10^{19} cm^{-3}). Therefore, for these doping concentrations, gate controllability over the channel decreases, HCEs are higher and thus subthreshold leakages increase. (b) The barrier height at the source/channel interface is very low for lower doping concentrations (1×10^{17} cm^{-3} 5×10^{17} cm^{-3}). Therefore, for these doping concentrations and at V_{DS} = 0.9 V, the carriers can easily move from the source to the drain with higher velocities; thus, the HCEs are greater [135]. Because of the above reasons, for an increase in doping, there is an increase in I_{ON} (increase in carriers), the overall trend of I_{ON}/I_{OFF} increases for doping levels of up to 1×10^{18} cm^{-3} and then decreases as doping increases further. Similarly, DIBL decreases for doping levels of up to 1×10^{18} cm^{-3} and further increases as doping increases. As the doping is increased, SS increases within a range of 65 to 74 mV dec^{-1} as shown in Fig.4.10 (a). The corresponding SS values are given in Table 4.4.

In Fig. 4.10 (b), the JL raised 'both' CDGT with moderate doping 1×10^{18} cm^{-3} provides optimum performance in terms of better electrical properties, such as a good I_{ON}/I_{OFF} ratio of about 3.75×10^{5}, a near ideal SS of 66.9 mV dec^{-1}, and a lower DIBL of about 35.1 mV V^{-1}. The extracted SCE parameters for different doping concentrations of the raised 'both' S/D structures (NMOS and PMOS devices) are given in Table 4.4.

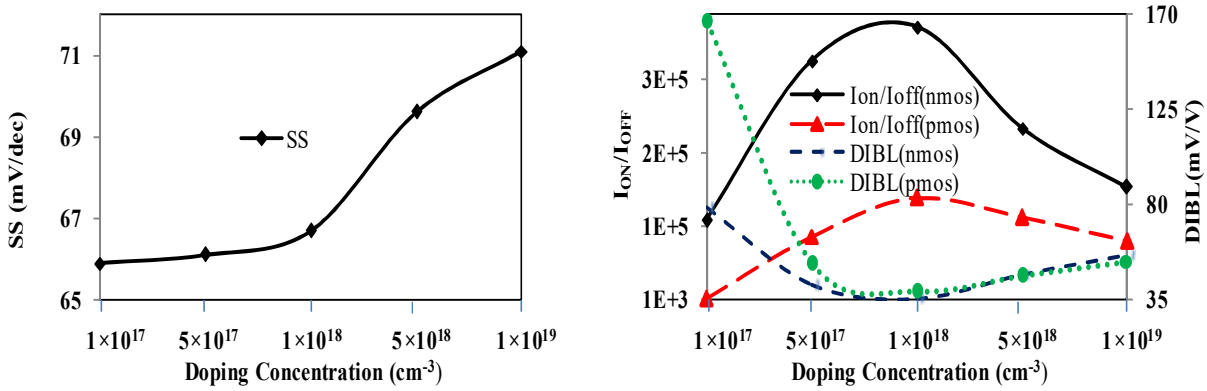


Fig. 4.10: Variation of (a) SS, and (b) I_{ON}/I_{OFF} and DIBL versus various doping concentrations.

Table 4.4: Performance Comparison of Raised both CDGT SOI MOSFET with various Doping Concentrations.

Doping Concentration	**1 × 10^{17} (cm^{-3})**		**5 × 10^{17} (cm^{-3})**		**1 × 10^{18} (cm^{-3})**		**5 × 10^{18} (cm^{-3})**		**1 × 10^{19} (cm^{-3})**	
Parameter	**NMOS**	**PMOS**	**NMOS**	**PMOS**	**NMOS**	**PMOS**	**NMOS**	**PMOS**	**NMOS**	**PMOS**
Work function (eV)	4.35	4.97	4.41	4.83	4.44	4.79	4.64	4.57	4.89	4.31
I_{ON} (mA)	0.14	0.04	0.14	0.07	0.15	0.09	0.2	0.14	0.22	0.17
I_{OFF} (nA)	1.2	36.3	0.43	0.84	**0.41**	**0.65**	0.88	1.24	1.38	2.1
I_{ON}/I_{OFF} (× 10^{4})	10.96	0.11	32.64	8.78	**37.26**	**13.98**	23.41	11.3	15.43	8.02
SS (mV/dec)	65.9	68.9	66.1	68.3	66.9	69.8	69.6	72.2	71.1	74.3
DIBL (mV/V)	78.7	166	42.3	51.8	**35.1**	**38.9**	46.8	45.8	55.9	53.2

In above sections, the device level performance of different types of circular MOSFETs is discussed. The impact of CSGT, CDGT, raised 'both' CDGT and raised 'both' CDGT JL devices (1 ×10^{18} cm^{-3}) on circuit performance is further analyzed for dynamic CMOS inverter behaviour. The results suggest that the proposed CDGT device provides smallest delay among all and outperforms all other devices in terms of circuit performance (see more detailed explanation in chapter 6).

4.6. Performance Analysis of CSGT/CDGT Devices at Sub 10 nm Node

In the previous analysis, the authors discussed about circular MOSFETs such as CSGT and CDGT devices at a gate length of 30 nm. The results suggest that CDGT has better electrical performance than CSGT due to two gates shielding the channel. Further, to improve the

device performance the raised S/D topologies and junctionless mode analysis were implemented on the CDGT device. All these structures are created by 'Genius' 3D parallel simulator provided by Cogenda Visual TCAD at a 30 nm technology node.

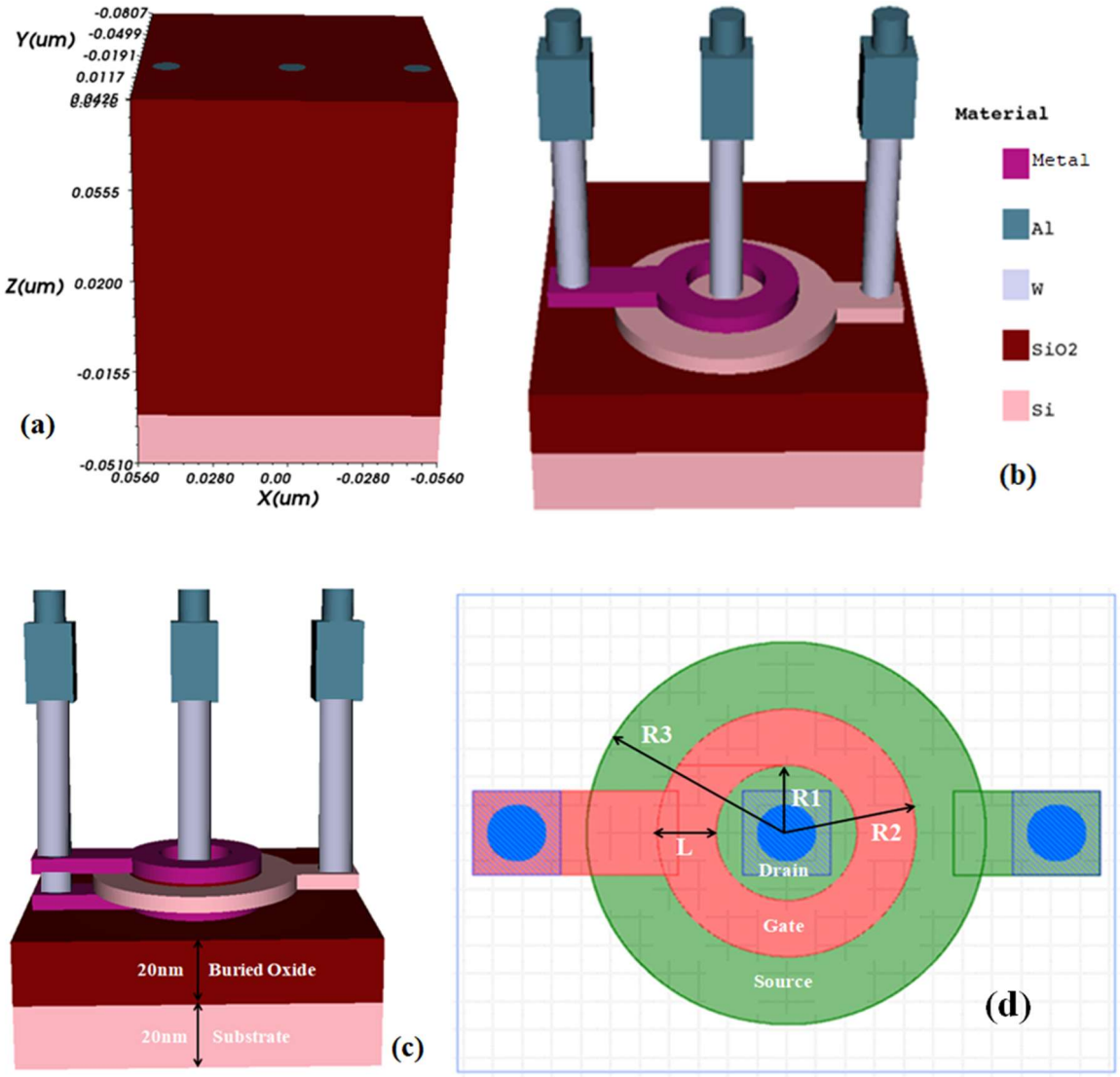


Fig. 4.11: (a) 3-D design view of Circular SOI MOSFET, (b) & (c) CSGT and CDGT after removing passivation oxide layer respectively, (d) proposed layout of Circular MOSFET.

As the technology entered a sub 10 nm nodes, a similar comparison analysis is performed on circular devices (CSGT and CDGT) at this node. Fig. 4.11 depicts the structure of 3D CSGT and CDGT SOI MOSFETs with essential dimensional parameters. Fig. 4.11 (b) and 4.11 (c) shows the equivalent 3D views of proposed CSGT and CDGT devices after removing the passivation oxide layer from Fig. 4.11 (a) respectively. All of these structures, doping

profiles, contacts definition, and mesh generation for device simulation are generated by applying process rules on GDSII of layout (layout and process flow files are used as input to Gds2Mesh), and the related layout is given in Fig. 4.11 (d). The same layout (Fig. 4.11 (d)) is used to design CSGT and CDGT devices with different process flow.

Some of the key device parameters utilized in the device creation are R1 = L = 10 nm, R2 = 2 × L = 20 nm, and R3 = 3 × L = 30 nm. Along with these dimensions, the gate/channel thickness is 5 nm, BOX thickness is 20 nm, the substrate thickness is 20 nm, and active silicon film thickness is 5 nm, thickness of Source/Drain (S/D) is 5 nm, and Tox thickness is 1 nm. The doping profiles are as follows: substrate doping concentration of 1×10^{15} cm^{-3}, the channel doping concentration of 1×10^{15} cm^{-3} and S/D doping concentration of 1×10^{20} cm^{-3}. Finally, supply voltage is 0.75 V considered. Genius 3D device simulator is used for all device simulations.

During the performance analysis of CSGT and CDGT devices at the 10 nm technology node, the calibrated simulation setup described in Chapter 3 is used in this analysis [49], and the authors followed IRDS 2017 projections for LP and HP applications. To match the threshold voltage for both NMOS & PMOS devices with IRDS 2017 projections [28] (using the constant current technique), we modified the metal gate work function. During the calibration we have used 4.5 eV for NMOS and 4.72 eV for P-MOS metal gate work functions respectively. Further, the work function is tuned around the values cited above for the HP applications ($|V_{TH}| \sim 0.19$ V) and LP applications ($|V_{TH}| \sim 0.32$ V) for all devices throughout the simulations.

Fig. 4.12 shows the DC characteristics of the CSGT and CDGT for both NMOS & PMOS devices with the calibrated setup. Fig. 4.12 shows the performance comparison of both devices for HP applications, and Fig. 4.13 shows the performance comparison for LP applications. At this node, Fig. 4.12, it can be seen that the CDGT device outperforms the CSGT device in terms of higher ON current (CSGT: 9.85×10^{-5} amps; CDGT: 3.1×10^{-4} amps), and better I_{ON}/I_{OFF} ratio (CSGT: 1.26×10^{4}; CDGT: 1.73×10^{6}) for LP applications (NMOS devices), this is similar to a 30 nm technology node. In comparison to CSGT, two gates electrically protect the channel on each side (front side and backside) from the drain voltage, allowing control over the silicon layer and strong electrostatic control over the channel. As a result, the CDGT reduces SCE, decreases leakage currents, and improves the I_{ON}/I_{OFF} ratio [136]. Further, the detailed electrical performance comparison (device-level FoM) of both devices (CSGT and CDGT) is given in Table 4.5 for LP and HP applications.

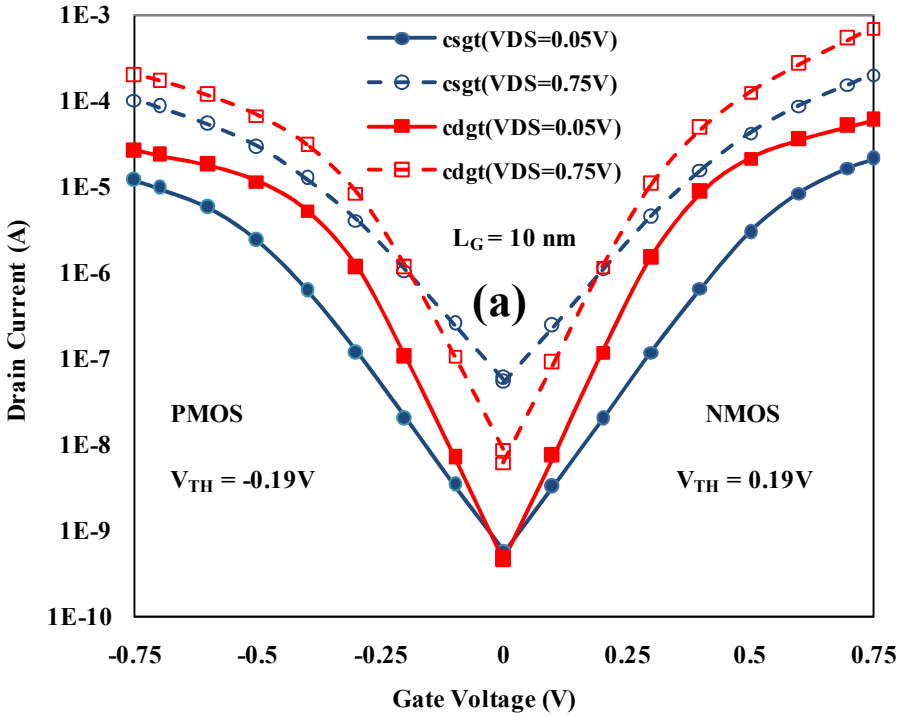


Fig. 4.12: I_{DS}–V_{GS} characteristics of both CSGT and CDGT SOI MOSFETs for HP applications.

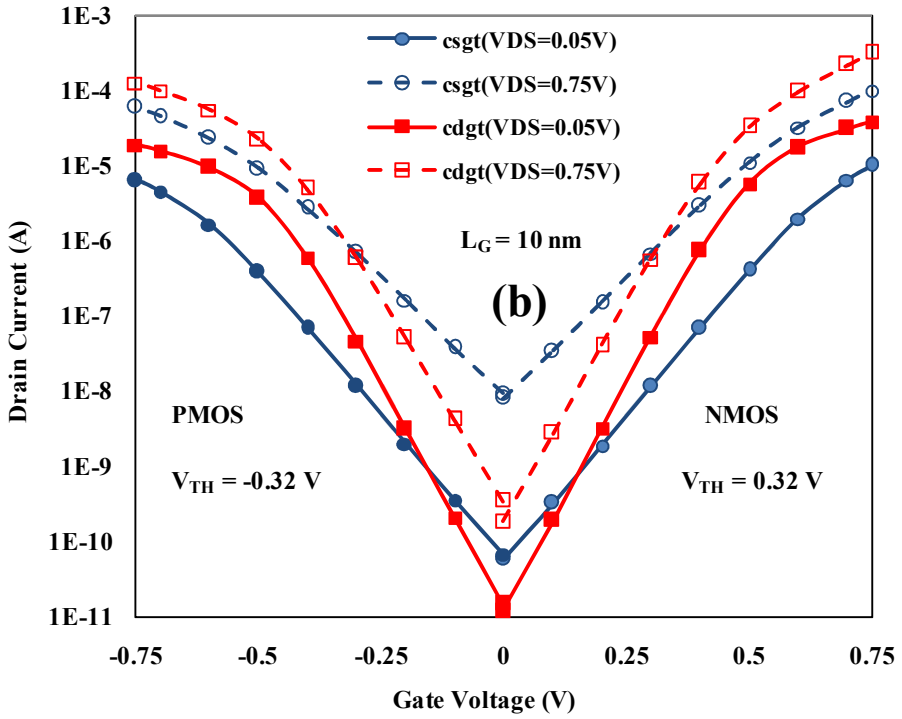


Fig. 4.13: I_{DS}–V_{GS} characteristics of both CSGT and CDGT SOI MOSFETs for LP applications.

Table 4.5: FoM comparison of both CSGT and CDGT SOI MOSFETs for LP and HP applications.

Device type	**CSGT**		**CDGT**		**CSGT**		**CDGT**	
Parameter	**NMOS**	**PMOS**	**NMOS**	**PMOS**	**NMOS**	**PMOS**	**NMOS**	**PMOS**
Threshold Voltage ($\|V_{TH}\|$)	0.19 V (HP)				0.32 V (LP)			
I_{ON} (mA)	0.2	0.1	**0.7**	**0.2**	0.1	0.06	**0.31**	**0.13**
I_{OFF} (nA)	52.5	57.2	**6.04**	**8.7**	7.9	9.1	**0.18**	**0.3 4**
I_{ON}/I_{OFF} ($\times 10^4$)	0.38	0.18	**11.5**	**2.3**	1.25	0.65	**172**	**36.8**
DIBL (mV/V)	328	337	**127**	**141**	328	337	**127**	**141**
SS (mV/dec)	153	157	**86**	**93**	151	154	**84**	**91**

The proposed CDGT device ON current is about 0.31 mA (~ 3290 µA/µm), and which is five times more than IRDS projections (~ 597 µA/µm) at 10 nm technology node for LP applications [28].

4.7. Summary

From the performance analysis of Circular SOI MOSFETs, we observe that the proposed CDGT SOI MOSFET provides better electrical characteristics than CSGT at a 30 nm technology node with an ON current (I_{ON}) of approximately 0.52 mA, and I_{ON}/I_{OFF} ratio of about 6.75×10^5. To improve the device ON current further, different raised Source/Drain (S/D) topologies are implemented on the CDGT device, among these the 'both' raised S/D CDGT device provides better performance than others. Furthermore, we also analyzed the behaviour of the best device of all, i.e., the raised 'both' topology device in junctionless mode. The optimum performance of the device is observed at uniform doping of 1×10^{18} cm^{-3}. Finally, similar analysis at a lower technology node (10 nm) is performed on circular MOSFETs. In this chapter, it is showed that traditional planar CMOS SOI technology performance can be improved upon by use of the CDGT SOI MOSFET.

Chapter-5

5. CDGT Device Optimization and Scaling Performance

Circular MOSFETs are another class of enclosed devices to extend the life of traditional planar CMOS SOI technology by overcoming the SCEs. As discussed in Chapter 4, the CDGT device provides better performance than CSGT at 10 nm technology node. In this chapter, a detailed analysis of optimizing CDGT device performance, and the impact of both underlap and high - k dielectric concepts on CDGT devices by extracting the DC, analog/RF parameters is presented. Next, the proposed CDGT device is benchmarked with existing novel structures like FinFET, NWFET and NSFET. Furthermore, the impact of scaling on CDGT performance is analyzed. Finally, this chapter ends with a discussion of the novel implementation of the stacking of nanosheets in a circular geometry.

5.1. CDGT Device Optimization

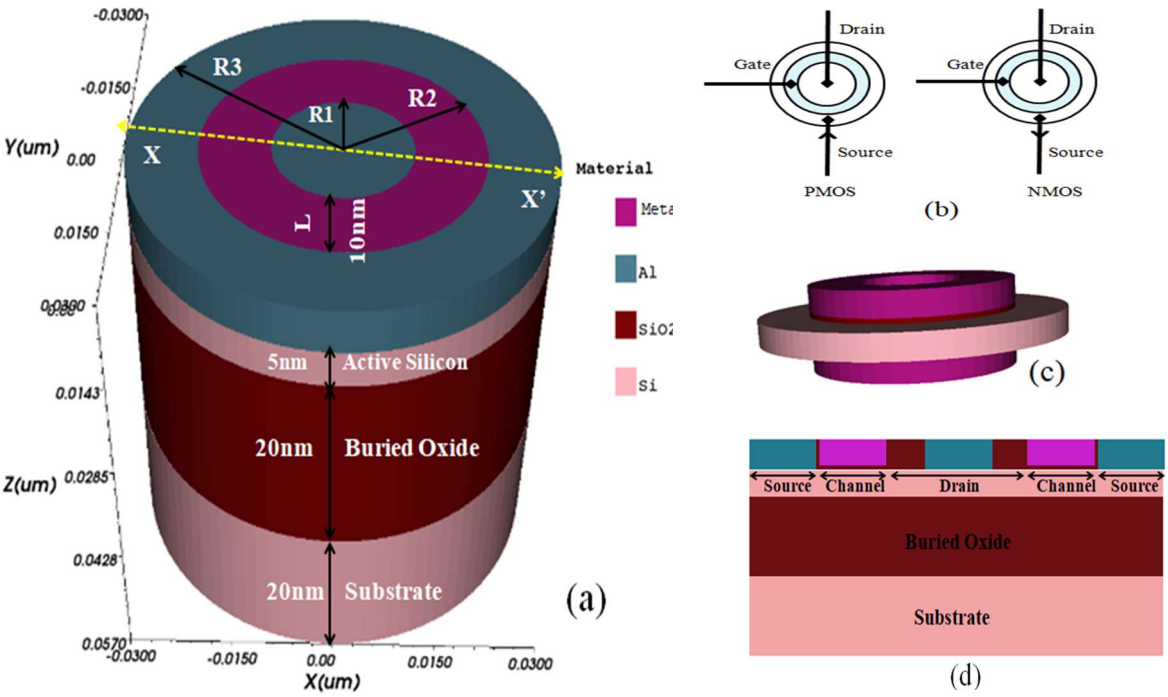


Fig. 5.1: (a) 3-D schematic view of CDGT, (b) Symbol of Circular MOSFET, (c) 3D - CDGT, (d) 2D - CDGT.

The 3D schematic view of CDGT & corresponding proposed symbols (PMOS & NMOS) are shown in Fig. 5.1 (a) and (b) respectively. The 3D view of the CDGT architecture after the substrate and oxide layers have been removed is shown in Fig. 5.1 (c). The 2D cross-sectional image of CDGT across the cutline XX' is shown in Fig. 5.1 (d). The essential dimensional parameters are also shown in Fig. 5.1 (a).

During device creation, the authors considered R1= L= 10 nm, R2= R1 + L = 20 nm, and R3= 3L = 30 nm. In addition to these parameters, we also considered metal gate thickness of 5 nm, BOX & substrate thickness of 20 nm, active silicon film thickness of 5 nm, and T_{OX} of 1 nm (SiO_2). The length of the channel is set as 10 nm with the doping concentration of 1×10^{15} cm^{-3}. The doping concentration in the source and drain regions is 1×10^{20} cm^{-3}, and the substrate doping concentration of 1×10^{15} cm^{-3}. These are the important device dimensions for the 10 nm technology node. Visual TCAD 3D Genius simulator is used to create device structures, doping profiles, contacts definition, and mesh generations for device simulations.

According to [46], the geometric factor of the circular MOSFET is defined by equation (5.1), with respect to the traditional planar rectangular MOSFET.

$$\left(\frac{W_{Rect}}{L}\right)_{Rectangular} = \left[\frac{2\pi}{\ln(R2/R1)}\right]_{Circular} \tag{5.1}$$

In the CDGT, the effective width of the channel W is defined as,

$$W = 2\pi \times \frac{[R1 + R2]}{2} \tag{5.2}$$

or substitute R2 = R1 + L in equation (5.2) to obtain W as follows:

$$W = 2\pi \times [R1 + 0.5 \times L] \tag{5.3}$$

Scaling of the device to sub 10 nm (L < 10 nm) will reduce the effective width of the channel, thus decreasing the ON current. The above effect is compensated by increasing R1. From equation (5.3), we can say that (i) For LP applications, the device ON current will improve by increasing R1 at a given technology node. (ii) When the technology is scaled down further, the device ON current will be reduced, it can be compensated by increasing R1. In these two

cases, as R1 increases, the device effective width (area) will increase which will enhance the device ON current.

Initially, the drain radius is considered as R1= L = 10 nm. During this analysis, to further improve the ON current, the inner drain radius R1 is increased from 10 nm to 20 nm. To differentiate the structure with these two radiuses, they are approximately named as R10nmSiO_2 (R1 = 10 nm) and R20nmSiO_2 (R1 = 20 nm).

As discussed in Chapter 4, here, the metal gate work function is adjusted to match the threshold voltage of about ($|V_{TH}|$ ~ 0.19 V) for HP applications, and the threshold voltage of about ($|V_{TH}|$ ~ 0.32 V) for LP applications for all NMOS & PMOS devices throughout the simulations.

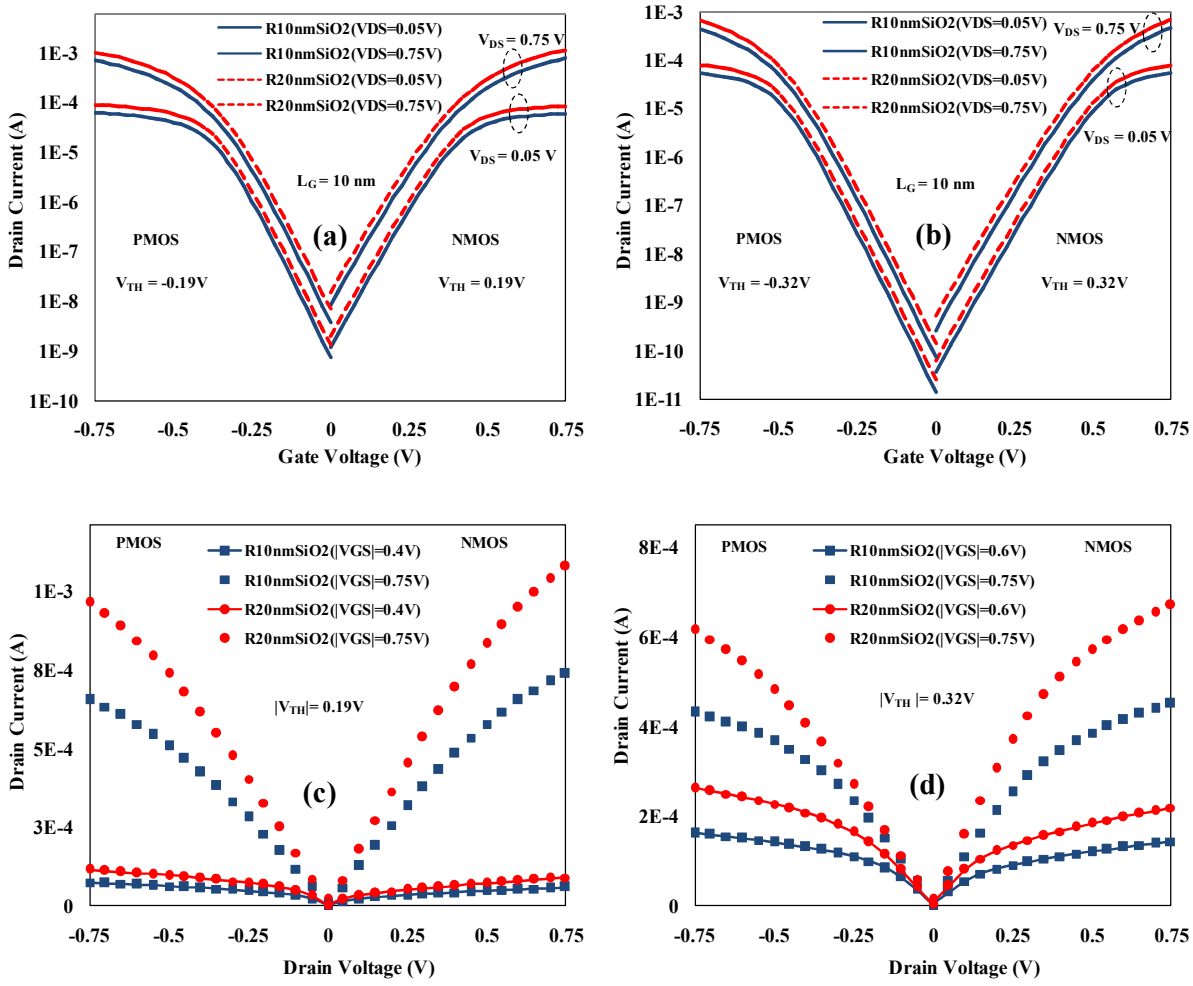


Fig. 5.2: (a), (b) I_{DS}-V_{GS} of CDGT with R1=10 nm & 20 nm for both NMOS&PMOS devices. (c), (d) I_{DS} -V_{DS} of CDGT with R1=10 nm & 20 nm for both NMOS&PMOS devices & corresponding V_{TH} values given inset.

Fig. 5.2 (a) & 5.2 (b) illustrates I_{DS}–V_{GS} electrical characteristics for low V_{DS} (0.05V) & high V_{DS} (0.75V) of the CDGT device for HP and LP applications respectively. Fig. 5.2 (c) & 5.2 (d) shows the corresponding I_{DS} - V_{DS} characteristics. In Fig. 5.2, it can be seen that because of the increase in the effective channel width & the average circumference, the CDGT device architecture with R1= 20 nm provides more ON current (≥ 1 mA). However, due to the smaller drain region with R1 = 10 nm, the off-state current is less when compared to R1= 20 nm. When the R1 increases from 10 nm to 20 nm the ON-current of the CDGT device increases by 46%. The comparison of the CDGT architectures with R1= 10 nm & 20 nm (@V_{TH}= 0.19V & @V_{TH} = 0.32 V) in terms of electrical parameters such as device I_{ON}, the device I_{OFF}, the overall I_{ON}/I_{OFF} ratio, SS, and DIBL are tabulated in Table 5.1. From Table 5.1, we can observe that the CDGT device architecture with R1 = 20 nm provides a better ON current than the other one.

Table 5.1: Performance analysis of CDGT with R1=10 nm & R1=20 nm.

Device type	**R10nmSiO₂**		**R20nmSiO₂**		**R10nmSiO₂**		**R20nmSiO₂**	
Parameter	**NMOS**	**PMOS**	**NMOS**	**PMOS**	**NMOS**	**PMOS**	**NMOS**	**PMOS**
Threshold Voltage (V_{TH})	0.19 (HP)				0.32 (LP)			
I_{ON} (mA)	0.77	0.68	**1.12**	**0.99**	0.45	0.43	**0.67**	**0.64**
I_{OFF} (nA)	8.1	3.8	14.7	6.9	0.26	0.073	0.51	0.14
I_{ON}/I_{OFF} ($\times 10^5$)	0.95	1.8	0.76	1.43	17.3	58.9	13.4	45.7
SS (mV/dec)	86	76	90	79	84	73	87	75
DIBL (mV/V)	105	77	110	82	105	77	110	82

In Table 5.1, it is evident that devices with the threshold voltage (|V_{TH}|~ 0.19 V) provide better device I_{ON} in the order of mA. Hence these low threshold devices are used for HP applications. Whereas the devices with a threshold voltage (|V_{TH}|~ 0.32 V) provide lower I_{OFF} in the order of pA. Hence these high threshold devices are used for LP applications.

5.2. Performance Analysis of Underlap (UL)

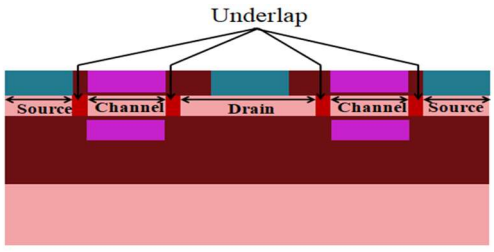


Fig. 5.3: 2D – CDGT with underlap.

From the previous section, it is found that CDGT architecture with increased inner radius (R1) from 10 nm to 20 nm gives better ON current at the cost of an increase in leakage. Further investigated the R20nmSiO_2 device with underlap concept to minimize these leakage currents.

Underlap has been considered to improve device performance. It offers desirable characteristics like greater breakdown voltage, decreased electric field at the drain and source regions, smaller gate leakage current, and so on, making it better suited for limiting the influence of drain potential on source barrier (DIBL effect) and reducing hot carrier effects [57]. Because of underlapping, the device's series resistance increases, resulting in a reduction in total device current (both I_{ON} & I_{OFF}). It offers an optimum I_{ON}/I_{OFF} ratio [57].

Fig. 5.3 depicts the 2D cross sectional view of the double gate circular MOSFET with underlap regions. The CDGT device R20nmSiO_2 with different underlap lengths (on both sides of the gate) of 1nm (UL1nmSiO_2), 2nm (UL2nmSiO_2), and 3nm (UL3nmSiO_2) with underlap doping concentration of 1×10^{18} cm^{-3} are simulated &compared interms of I_{ON}, I_{ON}/I_{OFF}.

Table 5.2: Performance analysis of R20nmSiO2 with different underlap lengths for HP applications.

Device type	**UL1nmSiO_2**		**UL2nmSiO_2**		**UL3nmSiO_2**	
Parameter	**NMOS**	**PMOS**	**NMOS**	**PMOS**	**NMOS**	**PMOS**
Threshold Voltage (V)	0.19(HP)					
I_{ON} (mA)	1.04	0.96	**0.98**	**0.89**	0.93	0.82
I_{OFF} (nA)	8.9	4	**6.5**	**3.2**	5.3	2.7
I_{ON}/I_{OFF} ($\times 10^5$)	1.2	2.4	**1.5**	**2.8**	1.8	3.1

Table 5.3: Performance analysis of R20nmSiO2 with different underlap lengths LP applications.

Device type	**UL1nmSiO_2**		**UL2nmSiO_2**		**UL3nmSiO_2**	
Parameter	**NMOS**	**PMOS**	**NMOS**	**PMOS**	**NMOS**	**PMOS**
Threshold Voltage (V)	0.32(LP)					
I_{ON} (mA)	0.64	0.6	**0.6**	**0.57**	0.57	0.54
I_{OFF} (nA)	0.17	0.07	**0.12**	**0.05**	0.09	0.043
I_{ON}/I_{OFF} ($\times 10^5$)	37.6	85.7	**50**	**114**	64	126

Table 5.2 shows the comparison of the underlap structures for HP applications. From Table 5.2, we can say that, as the underlap length increases both ON and OFF currents are reduced. The optimum performance can be obtained for the device R20nmSiO_2 with a minimum of 2nm underlap length as compared to the device R10nmSiO_2 without underlap concept (from Table 5.1). Similar findings are observed for LP applications as shown in Table 5.3.

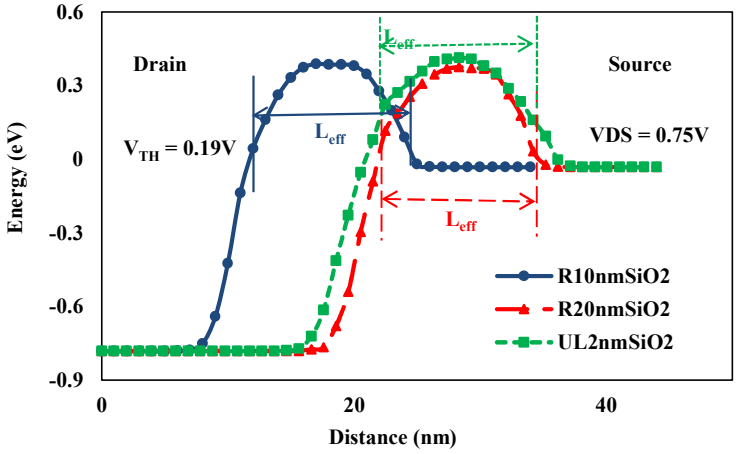


Fig. 5.4: Conduction energy band profiles along the lateral direction for different CDGT devices.

For the NMOS device OFF-state operation at a lower threshold voltage of 0.19V, Fig. 5.4 presents the edge of the conduction band in the lateral direction at the center of the active silicon film layer. From Fig. 5.4, it can be seen that the device with an underlap of 2 nm has a higher barrier height at the source/channel interface. As a result, despite having a high velocity at a high V_{DS}, the carriers cannot easily flow from source to drain in this device. Thus, HCEs are reduced, thereby reducing subthreshold leakages as well. Because of the above reason, the overall ON to OFF ratio is higher for this device only.

Further the DC performance (I_{ON}, I_{ON}/I_{OFF}, DIBL & SS), and analog/RF performance (Transconductance generation factor (TGF), g_m, Early voltage (V_{EA}), & Output conductance (g_d)) of different CDGT devices (R10nmSiO_2, R20nmSiO_2 & UL2nmSiO_2) are investigated. The TGF is defined as the g_m/I_{DS} ratio, which represents the conversion of DC power to AC frequency. The variation in drain current to change in gate voltage is referred to as the g_m. The parameter g_m is critical in the design of op-amps. It denotes a device's gate transport efficiency. In general, g_m indicates a device's gain, while I_{DS} is the power dissipation required to attain that gain. The V_{EA} is the ratio of I_{DS} to g_d. The g_d is the ratio of the drain current

change to the drain voltage change. To achieve better analog performance, g_d should be low & V_{EA} should be high.

$$Transconductance\ (g_m) = \frac{\partial I_D}{\partial V_{GS}} \tag{5.4}$$

$$Transconductance\ generation\ factor\ (TGF) = \frac{g_m}{I_{DS}} \tag{5.5}$$

$$Transconductance\ (g_d) = \frac{\partial I_D}{\partial V_{DS}} \tag{5.6}$$

$$Early\ Voltage\ (V_{EA}) = \frac{I_d}{g_d} \tag{5.7}$$

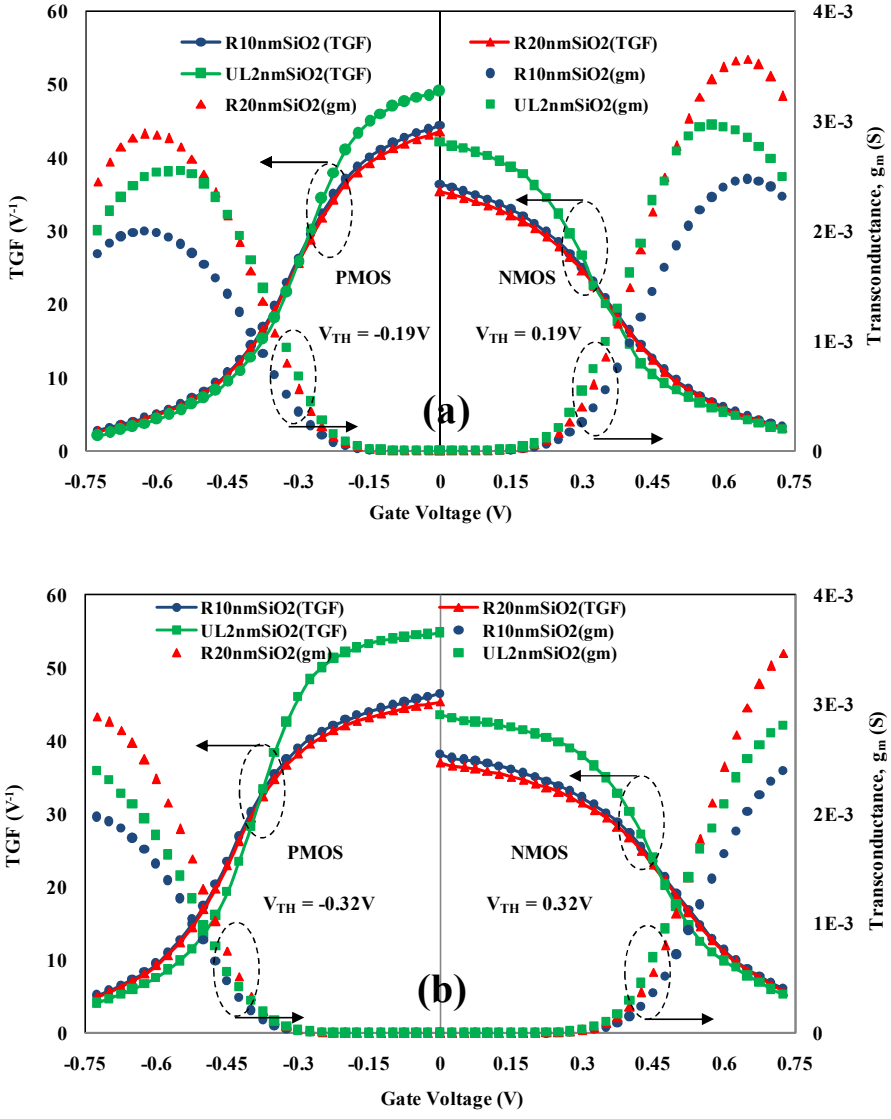
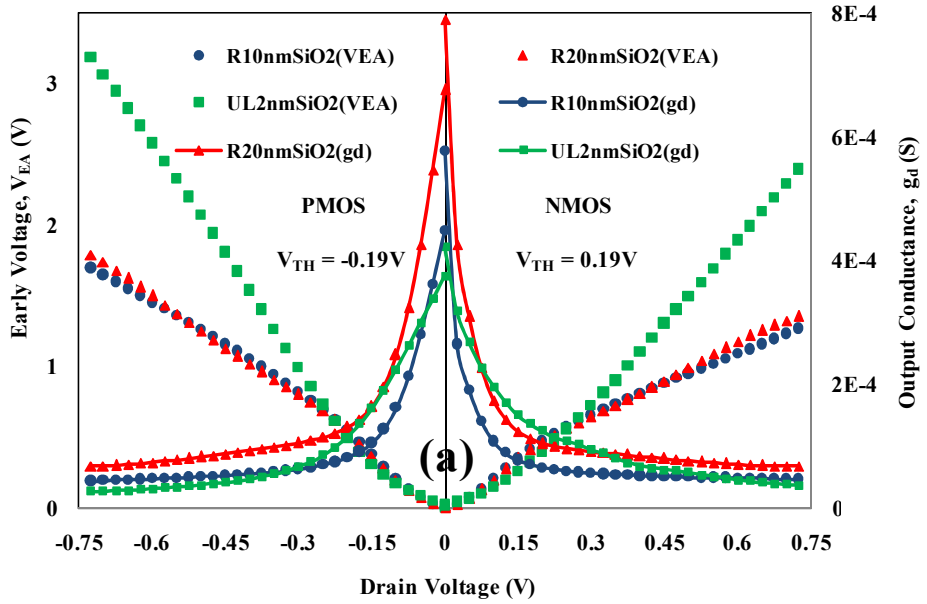


Fig. 5.5: (a), (b) g_m & TGF of CDGT with R1=10 nm, 20 nm, & UL2nm for both NMOS&PMOS devices, corresponding V_{TH} values shown inset.

Fig. 5.5 compares the TGF and g_m levels of the various CDGT devices (R10nmSiO_2, R20nmSiO_2 & UL2nmSiO_2) devices at a lower V_{TH} of 0.19V (HP) & higher V_{TH} of 0.32 V (LP) for both NMOS & PMOS devices. Fig. 5.5 shows that the CDGT device (R20nmSiO2) provides greater g_m with a higher drive current. However, the CDGT device with underlap (UL2nmSiO_2) provides a superior TGF because of its lower leakage current. The UL2nmSiO2 device enhances the signal because of its high TGF.



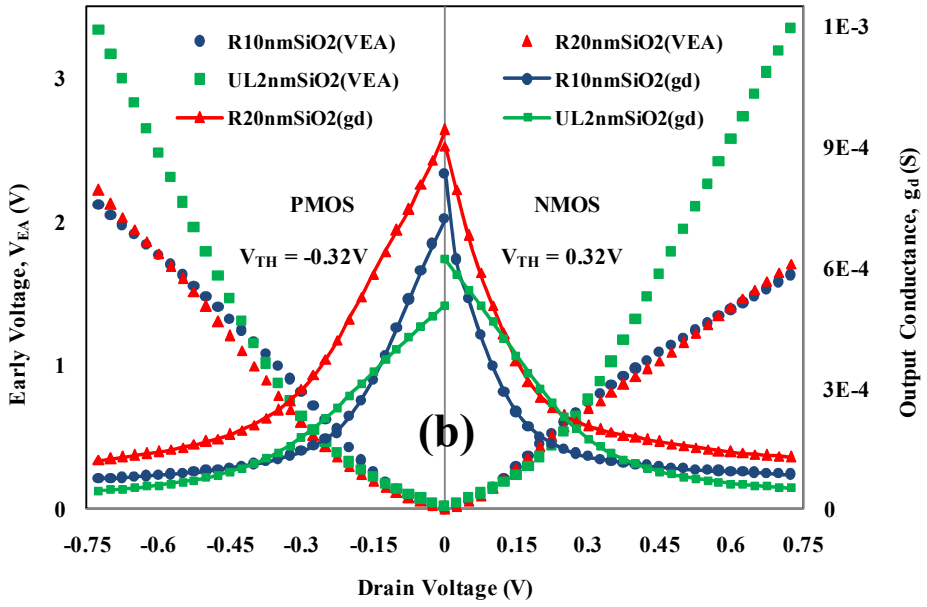


Fig. 5.6: (a), (b) g_d &V_{EA} of CDGT with R1=10 nm, 20 nm, & UL2nm for both NMOS & PMOS devices, corresponding V_{TH} values shown inset.

Fig. 5.6 compares the V_{EA} and g_d of the above-mentioned devices at a lower V_{TH} of 0.19V (HP) and a higher V_{TH} of 0.32V (LP) for both NMOS and PMOS devices. In this result the CDGT device with underlap ($UL2nmSiO_2$) has a larger V_{EA} and a lower g_d due to its lower OFF current. With the above advantages, the CDGT with underlap of 2 nm ($UL2nmSiO_2$) device improves analog performance. Among the mentioned 3 different architectures, the $UL2nmSiO_2$ architecture outperforms the others in terms of electrical performance. This architecture provides a better I_{ON}/I_{OFF} ratio of ~ 1.14×10^7, a lower DIBL of ~ 69 mV/V, and a near-ideal SS of ~ 69.6mV/dec. In addition, Table 5.4 & Table 5.5 summarize all the essential numerical data.

Table 5.4: Overall Performance analysis of different CDGT architectures for HP applications.

Device type	**$R10nmSiO_2$**		**$R20nmSiO_2$**		**$UL2nmSiO_2$**	
Parameter	**NMOS**	**PMOS**	**NMOS**	**PMOS**	**NMOS**	**PMOS**
V_{TH} (V)	0.19 (HP)					
I_{ON} (mA)	0.77	0.68	**1.12**	**0.99**	0.98	0.89
I_{OFF} (nA)	8.1	3.8	14.7	6.9	**6.5**	**3.2**
I_{ON}/I_{OFF} ($\times 10^5$)	0.95	1.8	0.76	1.43	**1.5**	**2.8**
SS (mV/dec)	86	76	90	79	**79**	**71**
DIBL (mV/V)	105	77	110	82	**84**	**69**
TGF(V^{-1})	36.4	44.4	35.4	43.6	**42**	**49**
V_{EA} (V)	1.27	1.7	1.36	1.79	**2.4**	**3.18**

Table 5.5: Overall Performance analysis of different CDGT architectures for LP applications.

Device type	**$R10nmSiO_2$**		**$R20nmSiO_2$**		**$UL2nmSiO_2$**	
Parameter	**NMOS**	**PMOS**	**NMOS**	**PMOS**	**NMOS**	**PMOS**
V_{TH} (V)	0.32 (LP)					
I_{ON} (mA)	0.45	0.43	**0.67**	**0.64**	0.6	0.57
I_{OFF} (nA)	0.26	0.073	0.51	0.14	**0.12**	**0.05**
I_{ON}/I_{OFF} ($\times 10^5$)	17.3	58.9	13.4	45.7	**50**	**114**
SS (mV/dec)	84	73	87	75	**77**	**69.6**
DIBL (mV/V)	105	77	110	82	**84**	**69**
TGF(V^{-1})	38.3	46.5	37	45.3	**43.5**	**54.8**
V_{EA} (V)	1.63	2.12	1.71	2.22	**3.33**	**3.35**

5.3. Performance Enhancement with High-k Dielectric

The study of the above-mentioned devices ($R10nmSiO_2$, $R20nmSiO_2$ & $UL2nmSiO_2$) is extended by using a high-k dielectric gate material stack. The various high-k dielectric gate materials such as (Al_2O_3, La_2O_3, HfO_2, etc.) have attracted the interest of many researchers

over the last two decades due to their significant potential for maintaining further downscaling in EOT (equivalent oxide thickness) with a physically thicker film and a lower gate leakage current [13]. In this study, Hf-based dielectric (HfO_2) of 0.4 nm with relative dielectric constant (K) = 26 as gate dielectric (EOT = 1nm) is used. Hafnium Oxide (HfO_2) dielectric gate material offers greater thermal stability, a higher recrystallization temperature, and an enhanced interface characteristic when compared to other gate insulator materials [137]. The Hf-based dielectric architectures are defined with R10nmHfO_2 (R1 = 10 nm), R20nmHfO_2 (R1 = 20 nm), and UL2nmHfO_2 (UL = 2 nm).

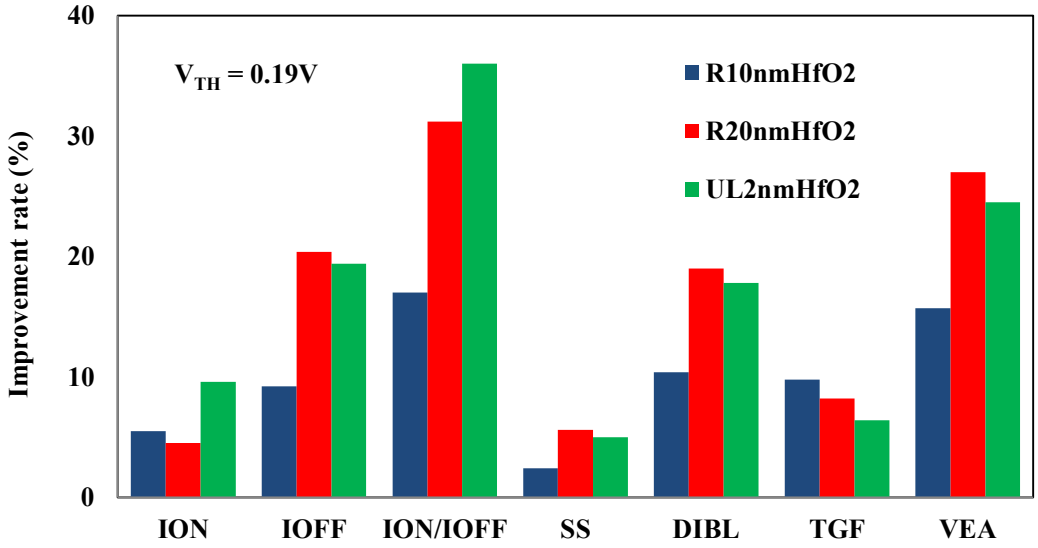


Fig. 5.7: Percentage improvement in performance (%) using high-k dielectric on various device metrics.

Fig. 5.7 shows the percentage of performance improvement rate for the various electrical parameters for the HfO_2 based architectures when compared with their SiO_2 counterparts. With the use of high-k dielectric (HfO_2), the gate oxide thickness increases, which reduces the gate leakage currents, thereby improving the overall device performance. Fig. 5.7 clearly shows that utilizing high-k material as a gate stack enhanced the performance of various circular double gate devices. In the case of UL devices with Hf-based dielectric, the device ON current increases by about 10%, the OFF current improves by about 20%, and the I_{ON}/I_{OFF} improves by about 36% when compared to CDGT devices without high-k. Electrical characteristics such as SS and DIBL have been enhanced by 5% and 18%, respectively. Similarly, analog/RF metrics such as TGF & V_{EA} are enhanced by 7% and 25%, respectively.

5.4. Benchmarking of CDGT device

In this section, the proposed CDGT device is benchmarked to that of existing advanced novel devices such as FinFET, NWFET, and NSFET [138]. Table 5.6 compares the performance of the proposed CDGT with the existing advanced novel devices (NMOS) at the sub 10 nm technology node. All these novel devices have identical device parameters such as gate length, doping concentrations ($N_{S/D}$ = 5 × 10^{19} cm^{-3}), supply voltage, and V_{TH} as given in Table 5.6 [138]**.** In this benchmarking, to make our proposed CDGT device identical with these novel structures, we adjusted the parameters to similar values.

Table 5.6: A comparison of the proposed CDGT's performance with advanced novel devices.

Device (NMOS)	**FINFET** [138]	**NWFET** [138]	**Nanosheet** [138]	**Proposed device (CDGT)**
Gate length	~ 12 nm	~ 12 nm	~ 12 nm	~ 12 nm
Perimeter	35.8 nm	20.29 nm	110 nm	~113 nm
NS or Si thickness			5 nm	5 nm
W_{fin}&H_{fin}	5.8 nm & 15 nm	-		-
NW diameter	-	6.46 nm	-	-
$N_{S/D}$ doping	5 × 10^{19} cm^{-3}	5 × 10^{19} cm^{-3}	5 × 10^{19} cm^{-3}	5 × 10^{19} cm^{-3}
Threshold voltage (V)	~ 0.185	~ 0.185	~ 0.185	~ 0.185
I_{ON} (µA/µm)	~612	~568	~699	**~4923**
I_{OFF} (nA/µm)	~7	~3	~5.7	~32
I_{ON}/I_{OFF} (× 10^5)	~ 0.87	~1.9	~1.2	~1.5
SS (mV/dec)	~74	~65	~71	~74

In Table 5.6, the NW FET has the least I_{OFF} and SS, indicating excellent gate control among all four structures. According to Table 5.6, the proposed device CDGT has the highest normalized I_{ON} in the ON-state region compared to all other structures, which is approximately 7 times greater than the next best device i.e., NSFET. In the subthreshold region, the CDGT device has the highest I_{OFF} of the four devices compared. Despite this, the proposed CDGT device still delivers the 2nd highest I_{ON}/I_{OFF} ratio. The I_{ON}/I_{OFF} ratio of the CDGT device is 18% lower than that of the NWFET, delivering better performance and outperforming all other devices in the ON- region. Hence the proposed CDGT device is a suitable alternative for NSFET in HP applications due to its superior drive current.

Table 5.7 displays the impact of S/D doping concentration on the performance of the aforementioned devices. By increasing the S/D doping from from 5 × 10^{19} cm^{-3} to 1.5 × 10^{20} cm^{-3}, the device ON-current can be increased, but this has an adverse influence on the sub-

threshold region. As the doping increases from 5×10^{19} cm^{-3} to 1.5×10^{20} cm^{-3} results in a rise in ON current by 27%, 44%, 28%, and 135% for the FinFET, NWFET, NSFET, and CDGT, respectively. The subthreshold characteristics such as I_{OFF} is increased by approximately 5.2 times, 2.1 times, 4.1 times, and 3.8 times for the FinFET, NWFET, NSFET, and CDGT, respectively. The same doping change results in V_{TH} reduction by 45 (−24%), 16 (−8.6%), 36 (−19.5%), and 39 (−21%) mV for FinFET, NWFET, NSFET, and CDGT, respectively. Similarly, the SS is increased by 8%, 3%, 7% and 8% for the FinFET, NWFET, NSFET, and CDGT, respectively.

Table 5.7: Performance comparison of CDGT device with existing novel devices at different doping concentrations.

Device (NMOS)	**$N_{S/D} = 1 \times 10^{20}$ cm^{-3}**				**$N_{S/D} = 1.5 \times 10^{20}$ cm^{-3}**			
	FinFET [138]	NW [138]	NS [138]	**CDGT**	FinFET [138]	NW [138]	NS [138]	**CDGT**
V_{TH} (V)	0.158	0.176	0.164	**0.160**	0.14	0.169	0.149	**0.146**
I_{ON} (µA/µm)	724	732	832	**8070**	777	819	893	**11592**
I_{OFF} (nA/µm)	19	4.6	13.3	**76.5**	36.1	6.2	23.5	**121**
I_{ON}/I_{OFF} ($\times 10^5$)	0.38	1.6	0.63	**1.06**	0.21	1.3	0.38	**0.96**
SS (mV/dec)	77	66	74	**77**	80	67	76	**79**

From Tables 5.6 & 5.7, the device ON current is increased with increasing in S/D doping concentration (due to increase in carriers), and the proposed CDGT device provides better ON current among all. The overall device performance is compared using the ON/OFF current ratio (I_{ON}/I_{OFF}), which reduces by -76%, -32%, -68%, and -38% for the FinFET, NWFET, NSFET, and CDGT, respectively, as the S/D doping is increased from 5×10^{19} cm^{-3} to 1.5×10^{20} cm^{-3}.

5.5. CDGT Device Scaling Performance

In the previous sections, the CDGT device performance (in terms of ON current) is optimized by increasing the inner drain radius (R1). In this scaling analysis, instead of increasing R1 to a random value, the authors increased the inner drain radius R1 of the device by considering a

25% and 50% increase in the total device area. i.e., here, optimizing the device performance by increasing the effective width of the device (area) for LP applications.

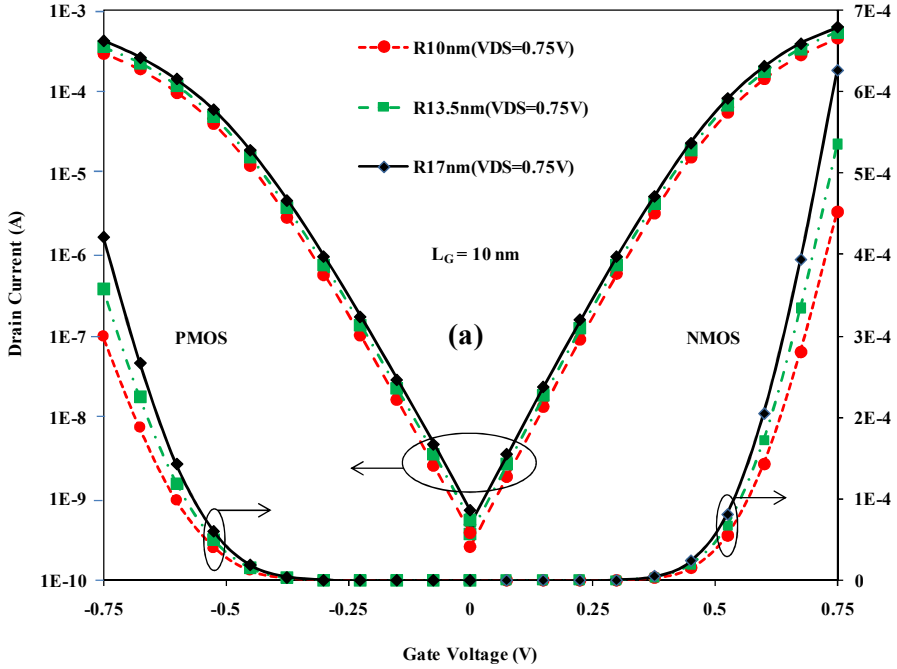


Fig. 5.8: I_{DS}-V_{GS} characteristics for the 10 nm gate length with different inner radiuses R1 = 10 nm, 13.5 nm, and 17 nm, on both linear (right) and logarithmic (left) scales, at high V_{DS} = 0.75 V.

Initially, the drain radius is considered as R1= L = 10 nm. It is increased to ~ 13.5 nm (by considering 25 % area increment), and it is further increased to ~ 17 nm (by considering 50 % area increment). Fig. 5.8 shows the I_{DS}–V_{GS} characteristics for V_{DS} = 0.75 V of both NMOS and NMOS devices with three different inner drain radiuses. Fig. 5.9 shows both ON current and I_{ON}/I_{OFF} comparison of CDGT devices at different inner drain radiuses.

From Fig. 5.9, as the inner drain radius (R1) increased from 10 nm to 13.5 nm, the device ON current will increase from ~ 0.453 mA to ~ 0.535 mA. Further, it will be increased to ~ 0.626 mA, when R1 is increased to 17 nm. This is due to the increase in device effective width & average circumference as R1 increases. i.e., as the device area is increased by 25 %, the ON current is improved by ~19 percent, and further, it is improved by 39 percent when the area is increased by 50 %, along with keeping subthreshold characteristics in the same order. However, there is a marginal decrement in the overall I_{ON} / I_{OFF} ratio as the drain radius is increased from 10 nm to 17 nm which follows the same trend as given by the reference [97].

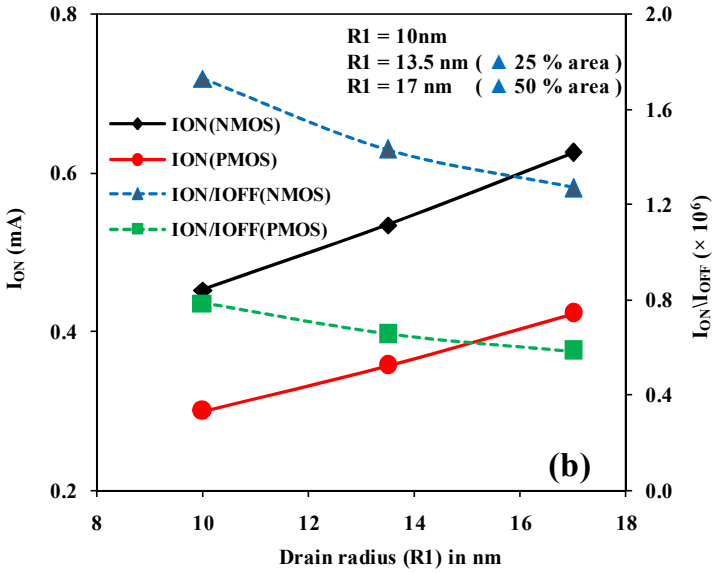


Fig. 5.9: Comparison of ON current and I_{ON}/I_{OFF} ratios at 10 nm node.

Further, the comparison of the CDGT device with different inner drain radiuses, R1= 10 nm, 13.5 nm & 17 nm in terms of electrical parameters such as variation in V_{TH}, device I_{ON}, I_{OFF}, the overall I_{ON}/I_{OFF} ratio, DIBL, and SS are tabulated in Table 5.8. From the Table 5.8, it is noticed that, as the drain radius increases from 10 nm to 17 nm, the OFF state leakage current slightly increases, which is still under the acceptable range of less than 1 nA [139] [140] and also provides improved ON current for LP applications. It can be compensated by using the underlap concept, as discussed in an earlier section.

Table 5.8: Electrical characteristics comparison of CDGT with different inner radiuses at 10 nm node.

Device type	**R1 = 10 nm**		**R1 = 13.5 nm (▲ 25% area)**		**R1 = 17 nm (▲ 50 % area)**	
Parameter	**NMOS**	**PMOS**	**NMOS**	**PMOS**	**NMOS**	**PMOS**
Threshold Voltage (V_{TH})	0.32	-0.32	0.317	-0.3184	0.3153	-0.3166
I_{ON} (mA)	0.452	0.3	0.535	0.357	**0.626**	**0.423**
I_{OFF} (nA)	0.262	0.38	0.374	0.546	0.493	0.73
I_{ON}/I_{OFF} ($\times 10^6$)	1.73	0.786	1.43	0.654	1.27	0.584
DIBL (mV/V)	~ 105	~ 114	~ 108	~116.9	~ 112	~ 120.5
SS (mV/dec)	~ 85	~ 88	~ 86	~ 89	~ 87	~ 90

5.5.1. Technology Node (7 nm)

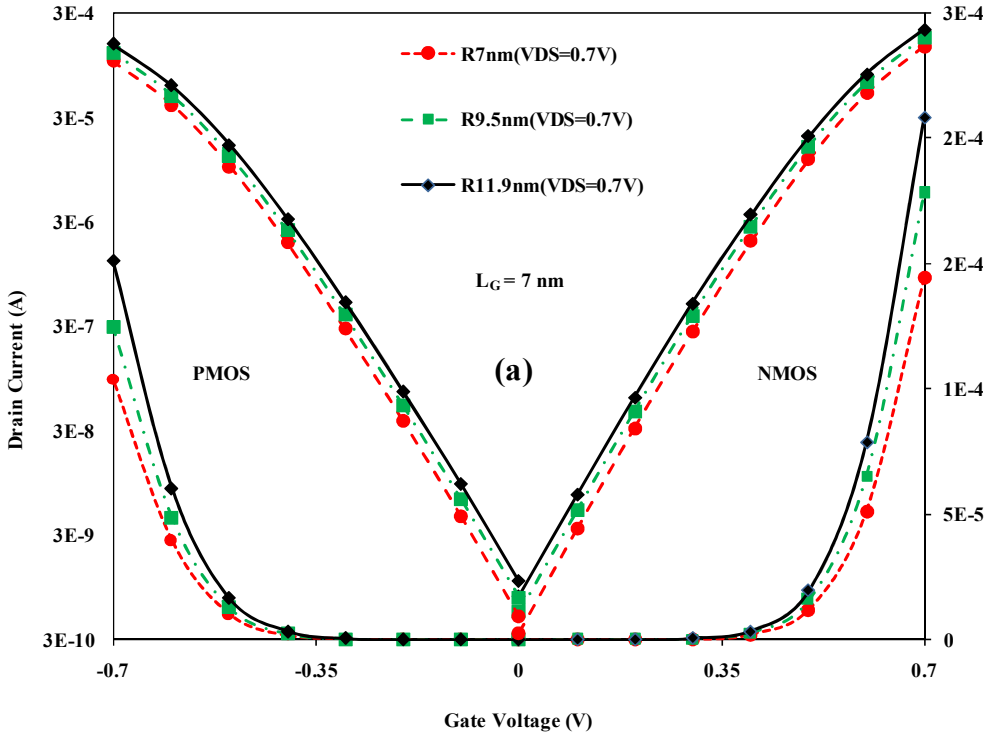


Fig. 5.10: I_{DS}-V_{GS} characteristics for the 10 nm gate length with different inner radiuses R1 = 7 nm, 9.5 nm, and 11.9 nm, on both linear (right) and logarithmic (left) scales, at high V_{DS} = 0.7 V.

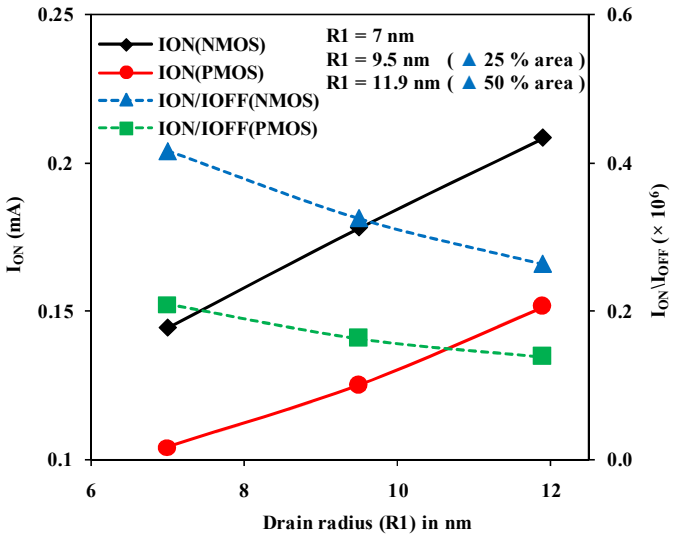


Fig. 5.11: Comparison of ON current and I_{ON}/I_{OFF} ratios at 7 nm node.

The analysis is extended to future technology nodes such as 7 nm and 5 nm using the same concept and followed the IRDS rules. According to IRDS regulations [139], considered a V_{TH} of around (|360 mV|) and a supply voltage of about 0.7 V at the 7 nm technology node. Similarly, at the 5 nm technology node, these values are (|324 mV|) and 0.65 V respectively. To match these threshold voltages at different technology nodes, the metal gate work function is tuned accordingly. However, EOT is considered to be 1 nm at both technology nodes.

At this node, initially, considered the drain radius as R1= L = 7 nm. It is increased to ~ 9.5 nm (by considering 25 % area increment), and it is further increased to ~ 11.9 nm (by considering 50 % area increment). Fig. 5.10 displays the I_{DS}–V_{GS} characteristics for a high drain to source voltage (V_{DS} = 0.7 V) of both NMOS and NMOS devices with three different inner drain radiuses. Fig. 5.11 shows both ON current and I_{ON}/I_{OFF} comparison of CDGT devices at different inner drain radiuses.

Similar to the 10 nm node from Fig. 5.11, as the inner drain radius (R1) is increased from 7 nm to 9.5 nm, the device ON current will increase from ~ 0.145 mA to ~ 0.178 mA. Further, it will be increased to ~ 0.208 mA, when R1 is increased to 17 nm. i.e., as the device area increased to 25 % (R1 = 9.5 nm), the ON current improved by ~22 %, and further it is improved by 43 % when the area is increased by 50 % (R1 = 11.9 nm).

Table 5.9: Electrical comparison of CDGT with different inner radiuses at 7 nm node.

Device type	**R1 = 7 nm**		**R1 = 9.5 nm (▲ 25% area)**		**R1 = 11.9 nm (▲ 50 % area)**	
Parameter	**NMOS**	**PMOS**	**NMOS**	**PMOS**	**NMOS**	**PMOS**
Threshold Voltage (V_{TH})	0.36	-0.36	0.355	-0.357	0.351	-0.352
I_{ON} (mA)	0.145	0.104	0.178	0.125	**0.208**	**0.151**
I_{OFF} (nA)	0.347	0.498	0.547	0.767	0.792	1.1
I_{ON}/I_{OFF} ($\times 10^6$)	0.417	0.21	0.326	0.163	0.263	0.137
DIBL (mV/V)	~166	~173	~175	~179	~183	~187
SS (mV/dec)	~ 100	~ 105	~ 102	~ 106.7	~ 103.3	~ 108

The comparison of the CDGT device with different inner drain radiuses, R1= 7 nm, 9.5 nm & 11.9 nm in terms of electrical parameters such as variation in V_{TH}, I_{ON}, I_{OFF}, the overall I_{ON}/I_{OFF} ratio, DIBL, and SS are tabulated in Table 5.9. From Table 5.9, can be said that as inner drain radius increases the device threshold voltage reduces thus increasing both ON and OFF current.

5.5.2. Technology Node (5 nm)

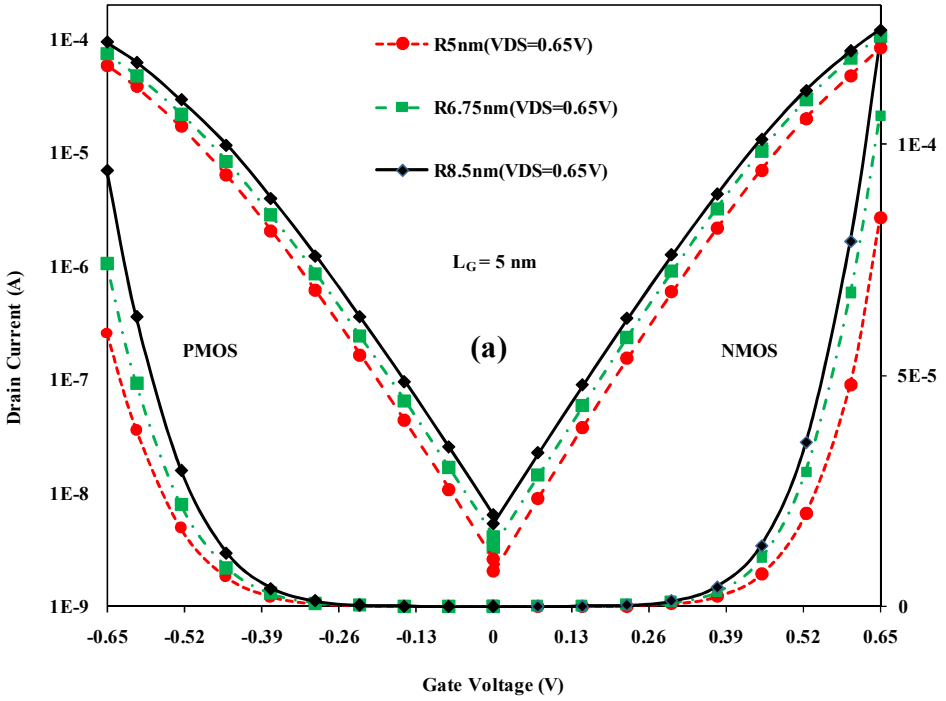


Fig. 5.12: I_{DS}-V_{GS} characteristics for the 10 nm gate length with different inner radiuses R1 = 5 nm, 6.5 nm, and 8.75 nm, on both logarithmic (left) and linear (right) scales, at high V_{DS} = 0.65 V.

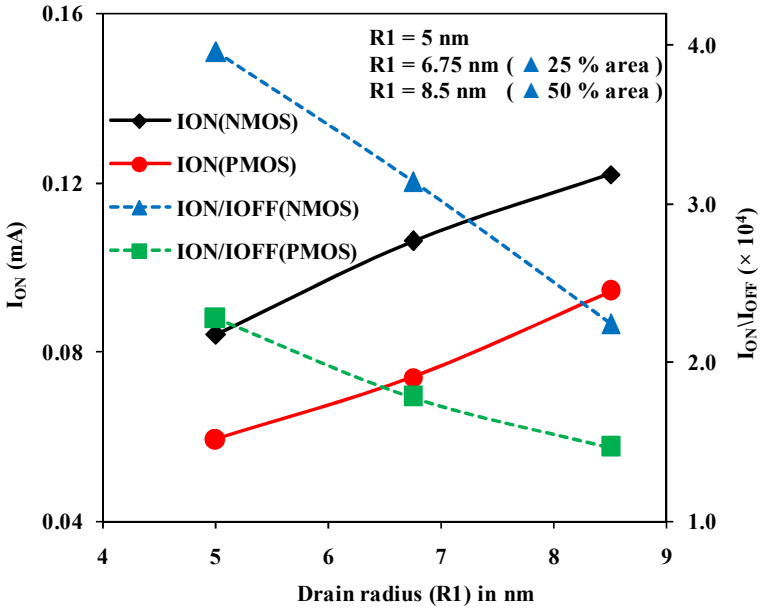


Fig. 5.13: Comparison of ON current and I_{ON}/I_{OFF} ratios at 5 nm node.

At this node, initially, considered the drain radius as R1= L = 5 nm. It is increased to ~ 6.75 nm (by considering 25 % area increment), and it is further increased to ~ 8.5 nm (by considering 50 % area increment). Fig. 5.12 shows the I_{DS}–V_{GS} characteristics for a high drain to source voltage (V_{DS} = 0.65 V) of both NMOS and PMOS devices with three different inner drain radiuses. Fig. 5.13 shows both ON current and I_{ON}/I_{OFF} comparison of CDGT devices at different inner drain radiuses.

Similar to the 10 nm node from Fig. 5.13, as the inner drain radius (R1) increased from 5 nm to 6.75 nm, the device ON current will increase from ~ 8.4×10^5 to ~ 10.6×10^5. Further, it will be increased to ~ 12.2×10^5, when R1 is increased to 8.5 nm. i.e., as the device area increased to 25 % (R1 = 9.5 nm), the ON current improved by ~26 %, and further, it is improved by 45 % when the area is increased by 50 % (R1 = 8.5 nm).

The comparison of the CDGT device with different inner drain radiuses, R1= 5 nm, 6.75 nm & 8.5 nm in terms of electrical parameters such as variation in V_{TH}, I_{ON}, I_{OFF}, the overall I_{ON}/I_{OFF} ratio, DIBL, and SS are tabulated in Table 5.10. From Table 5.10, as inner drain radius increases the device threshold voltage reduces and thus increasing both ON and OFF current.

Table 5.10: Electrical characteristics comparison of CDGT with different inner radiuses at 5 nm node.

Device type	**R1 = 5 nm**		**R1 = 6.75 nm (▲ 25% area)**		**R1 = 8.5 nm (▲ 50 % area)**	
Parameter	**NMOS**	**PMOS**	**NMOS**	**PMOS**	**NMOS**	**PMOS**
Threshold Voltage (V_{TH}) (V)	0.324	-0.324	0.313	-0.3164	0.3046	-0.306
I_{ON} (mA)	0.084	0.059	0.106	0.074	**0.122**	**0.094**
I_{OFF} (nA)	2.12	2.6	3.38	4.15	5.43	6.43
I_{ON}/I_{OFF} ($\times 10^4$)	3.96	2.28	3.14	1.79	2.244	1.47
DIBL (mV/V)	~ 224	~ 227	~ 238	~ 241	~ 251	~ 254
SS (mV/dec)	~ 116.6	~ 120.5	~ 118.2	~ 123	~ 120	~ 124.2

With the above analysis, we can say that the device performance is improved further in terms of ON current by increasing inner drain radius, when the device is further scaled down to future technology nodes such as 7 nm and 5 nm.

5.6. Impact of Geometrical Variations on CDGT Performance

The performance of CDGT is analyzed further by changing the CDGT physical dimensions such as gate length and thickness of the active silicon film. The length of the gate scaled from 20 nm to 10 nm and silicon film thickness increased from 5 nm to 8 nm during this analysis.

5.6.1. Gate Length (L)

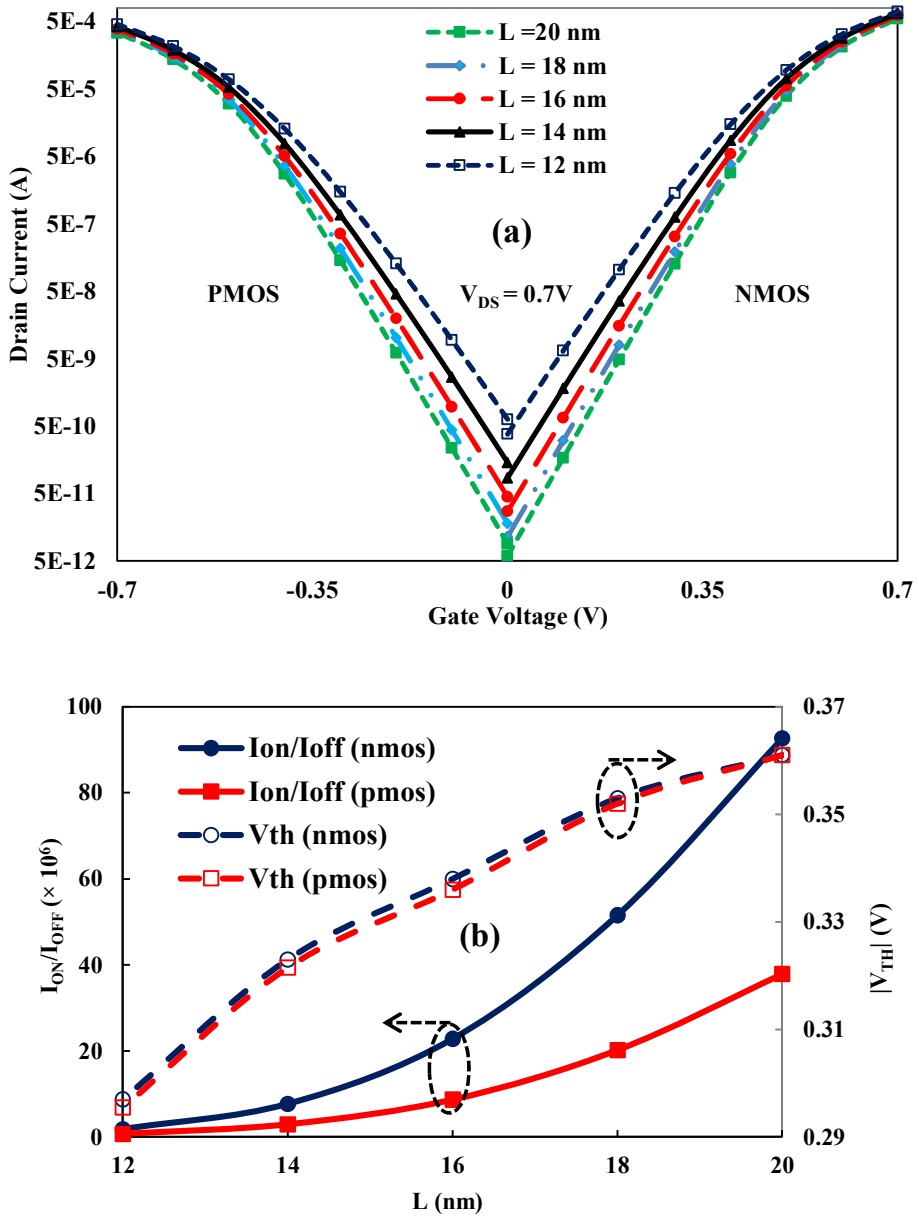


Fig. 5.14: Electrical behavior of CDGT for various gate lengths, (a) ON current (b) Switching ratio and V_{TH} of proposed CDGT devices.

During this gate length variation analysis, the drain length (R1) of 20 nm, and source length (R3 – R2) of 20 nm have been considered throughout this analysis. During this study, we have considered IRDS 2017 projections [27] for various specifications such as the gate length (L), device threshold voltage (V_{TH}), and supply voltage (V_{DD}) for LP applications. As per the variation in gate length the device area has been changed in terms of radiuses as R2 = R1 + L and R3 = R2 + L = R1 + 2L.

Fig. 5.14 shows electrical characteristics of proposed CDGT device with variation in gate length (L) at 7 nm technology node. From Fig. 5.14 (a) it is found that as the L is scaled down from 20 nm to 12 nm the device leakage current (I_{OFF}) increases because of less controllability of the gate over the channel. The decrease in gate length the SCEs dominates due to several factors such as charge sharing mechanisms, etc. However, the ON current (I_{ON}) increases with scaling effect due to decreased effective gate length leading to less electron tunneling distance from source to drain.

Fig. 5.14 (b) shows variations in both ON to OFF current ratio (I_{ON}/I_{OFF}) and threshold voltage (V_{TH}) with gate length scaling of a proposed CDGT device. As the device is scaled down (gate length is reducing), the V_{TH} of the device decreases due to the dominant SCEs as shown in Fig. 5.14(b). The V_{TH} roll-off of 17.7% observed for the proposed device when the L is scaled down from 20 nm to 12 nm. The I_{ON}/I_{OFF} ratio falls with scaling of gate length in Fig. 5.14 (b) due to less gate control over the channel. The I_{ON}/I_{OFF} ratio determines the performance capability of the device as well as the possibility of future scaling for lower technology nodes. In Fig. 5.14 (b) it is clearly visible that as the device gate length is scaled down from 20 nm to 10 nm, the I_{ON}/I_{OFF} ratio is still greater than 10^6. Further, the impact of device scaling on CDGT device electrical performance is shown in Table 5.11 in detail.

Table 5.11: Performance comparison of proposed CDGT with different gate lengths.

Gate Length (L)	**20 nm**		**18 nm**		**14 nm**		**12 nm**	
	NMOS	**PMOS**	**NMOS**	**PMOS**	**NMOS**	**PMOS**	**NMOS**	**PMOS**
V_{TH} (V)	0.36	036	0.352	0.351	0.322	0.32	0.296	0.295
I_{ON} (mA)	0.56	0.341	0.59	0.362	0.66	0.422	0.71	0.454
I_{OFF} (pA)	5.97	9	11.4	17.9	85.6	144	380	630
I_{ON}/I_{OFF} ($\times 10^6$)	92.7	37.9	51.5	20.2	7.7	2.94	1.86	0.72
SS (mV/dec)	68.4	69.6	69.4	71.3	75.2	78.2	79.9	84.4
DIBL (mV/V)	38.8	43.7	45.8	51.3	70.7	79.7	92.8	104.3

5.6.2. Silicon film thickness (T_{si})

In this analysis, we have extracted the electrical characteristics by varying the thickness of the active silicon film while keeping other parameters at identical values. Fig. 5.15 shows electrical characteristics of proposed CDGT device with variation in Silicon film thickness (T_{si}) at 7 nm technology node.

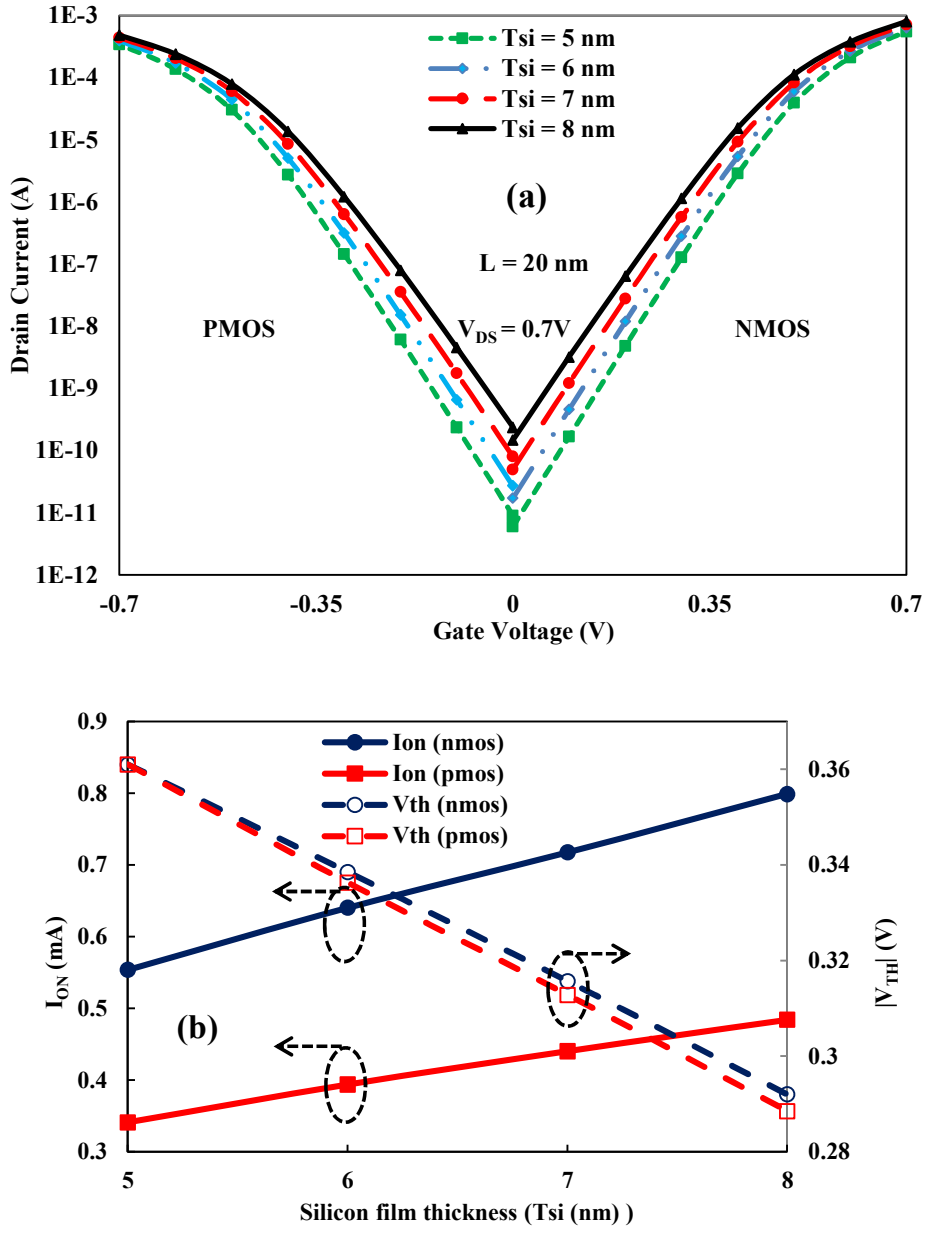


Fig. 5.15: Electrical behavior of CDGT with Tsi variations, (a) I_{DS} - V_{GS} (b) ON current and V_{TH} (c) SS of proposed CDGT devices.

From Fig. 5.15 (a), it can be observed that an increase in Tsi from 5 nm to 8 nm leads to an increase in the I_{ON} of the proposed CDGT due to the increase in the effective channel width. Similar to the ON current, an increase in the OFF current is also noticed because the gate loses its control over the channel when the channel thickness increases, leading to more leakages in the device. These leakages increase the I_{OFF} of the device.

Fig. 5.15 (b) shows variations in both I_{ON} and threshold voltage (V_{TH}) with variation in T_{si} of a proposed CDGT device. As the T_{si} increases, from Fig. 5.15 (b), it can be seen that the threshold voltage decreases as the gate loses control over the channel. The V_{TH} roll-off of 19% is noticed for the proposed device when the T_{si} is increased from 5 nm to 8 nm. From Fig. 5.15 (b), the I_{ON} increases more than 40 % as the T_{si} is changed from 5 nm to 8 nm due to increment in effective width of the channel. Further, the impact of variation in thickness on proposed CDGT device electrical performance is shown in Table 5.12 in detail. In Table 5.12, it is clearly visible that as the T_{si} increased from 5 nm to 8 nm, the I_{ON}/I_{OFF} ratio is still greater than 10^6. An I_{ON}/I_{OFF} ratio greater than 10^6 is observed in both Table 5.11 and Table 5.12, which is within an acceptable range, that is, the scaling effect of variation in L and Tsi is minimal. Hence the proposed CDGT device is well suited for low technology nodes with high ON current for LP applications.

Table 5.12: A comparative analysis of proposed CDGT for various thicknesses (T_{si}).

Silicon film thickness (T_{si})	**5 nm**		**6 nm**		**7 nm**		**8 nm**	
	NMOS	**PMOS**	**NMOS**	**PMOS**	**NMOS**	**PMOS**	**NMOS**	**PMOS**
V_{TH} (V)	0.36	036	0.338	0.336	0.315	0.312	0.29	0.288
I_{ON} (mA)	0.56	0.341	0.64	0.394	0.72	0.44	0.8	0.484
I_{OFF} (pA)	5.97	9	17.1	27	49.7	80.1	147	236
I_{ON}/I_{OFF} ($\times 10^6$)	92.7	37.9	37.5	14.6	14.5	5.5	5.4	2.06
SS (mV/dec)	68.4	69.6	69.5	71.5	71.4	73.9	74	77
DIBL (mV/V)	38.8	43.7	49	54.3	60.8	67.3	74.9	82.1

5.7. Circular Nanosheet MOSFETs (C- NSFETs)

Over the past few decades, semiconductor technology has emerged as the driving force behind computing hardware. Further, over the past decade, the FinFET technology has gradually come to dominate the semiconductor market [141]. The power, density, and performance requirements for this technology continue to scale, but not quickly enough. New advancements are still needed to create faster more potent artificial intelligence hardware.

For more than a decade, researchers have been working on GAA transistors, and the device structure has emerged from a single nanowire to a stacked nanosheet (NS). Because of the stacking process, NSFETs outperform standard GAA structures in terms of performance, drive currents, and process efficiency. As a result, NSFET is becoming the most popular candidate for future devices [39][80].

The increased W_{EFF} in NSFETs enables greater current drivability in a similar footprint while maintaining superior electrostatics. The NSFETs can also vary the drain currents by changing the NS width, enabling the design of CMOS-compatible layouts. Similar to an NW, but with a wider width, NSFETs exhibit improved device performance levels and better control over leakage current [142]. Because of its higher footprint density and improved electrostatic control in GAA, NS offers a better power-performance design point [143].

With the advantages of both NSFETs and Circular geometry, in this section, a new structure called Circular NSFETs (C-NSFETs) is proposed at sub 10 nm technology node with an internal silicon pad as a drain. Further, extended this work in terms of stacked C-NSFETs like 2 sheets, 3 sheets, and 4 sheets and compare their electrical performance for both N-type & P-type MOSFETs.

5.7.1. Device Structure and Fabrication Process

The concept of 3-D C-NSFETs with relevant dimensional parameters is shown in Fig. 5.16. After removing the passivation oxide layer from Fig. 5.16 (a), the corresponding 3D view of the proposed C-NSFET is shown in Fig. 5.16 (b) along with the relevant layers. Here, all these structures are created by Gds2mesh (layout & process flow files as input), and the corresponding layout structure is shown in Fig. 5.16 (c). In Fig. 5.16 (c), the area of circular sheet with radius R1 is defined as drain region, the area between R2 and R1 is defined as gate or channel region, and finally the area with outer ring between R3 and R2 is defined as the

source region. As a result, the C-NSFETs technology node or gate length is L = R2 − R1. The 2D view of C-NSFET with doping profiles is shown in Fig. 5.16 (d) obtained across the cutline AA' of Fig. 5.16 (c). Some of the essential device parameters used in the device creation and simulation study of the C-NSFETs is given in Table 5.13.

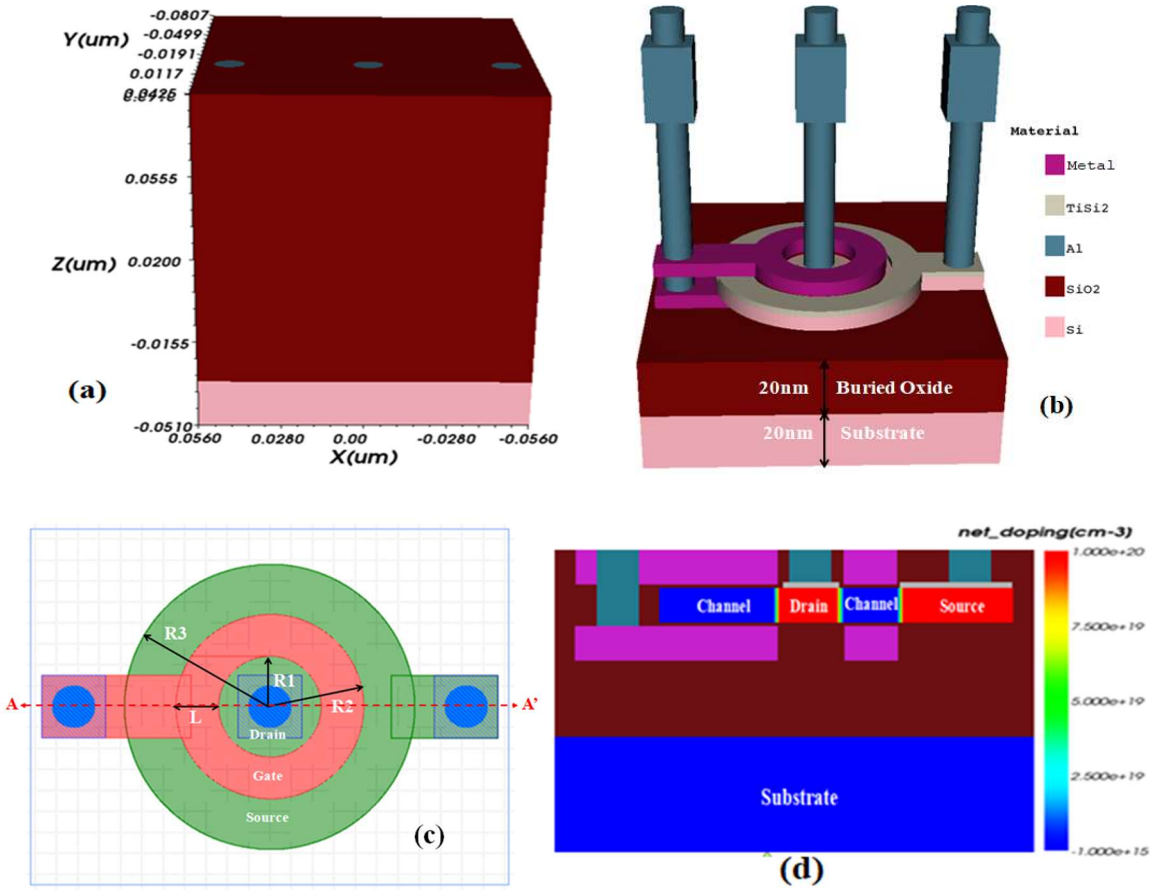


Fig. 5.16: (a) 3-D design view of Circular Nanosheet FET, (b) C-NSFET after removing passivation layer, (c) layout of C-NSFET, (d) 2D cut view of C-NSFET across the AA' cutline with doping profiles.

Table 5.13: Geometrical details of C-NSFETs devices used in the simulation.

Device type	**C-NSFET**	
Parameter	**NMOS**	**PMOS**
Gate Length (L or L_G)	10 nm	
T_{OX}	1 nm	
S/D thickness	5 nm	
Gate thickness	5 nm	
Nanosheet film thickness (T_{ch})	5 nm	
Source/ Drain doping (cm^{-3})	1×10^{20}	
$\|V_{DD}\|$ (V)	0.75	

The 2D view of the fabrication process of the proposed C-NSFET is shown in Fig. 5.17. To attain greater package densities, the C-NSFET fabrication technique, as shown in Fig. 5.17, utilizes a self-aligned fabrication procedure similar to the CDGT fabrication process discussed in Chapter 4. In this fabrication process, to achieve high performance, the alternative wafer bonding technique [144] can be used in step (d) of the fabrication process. In Fig. 5.17, the isolation oxide is shown up to the top metal gate.

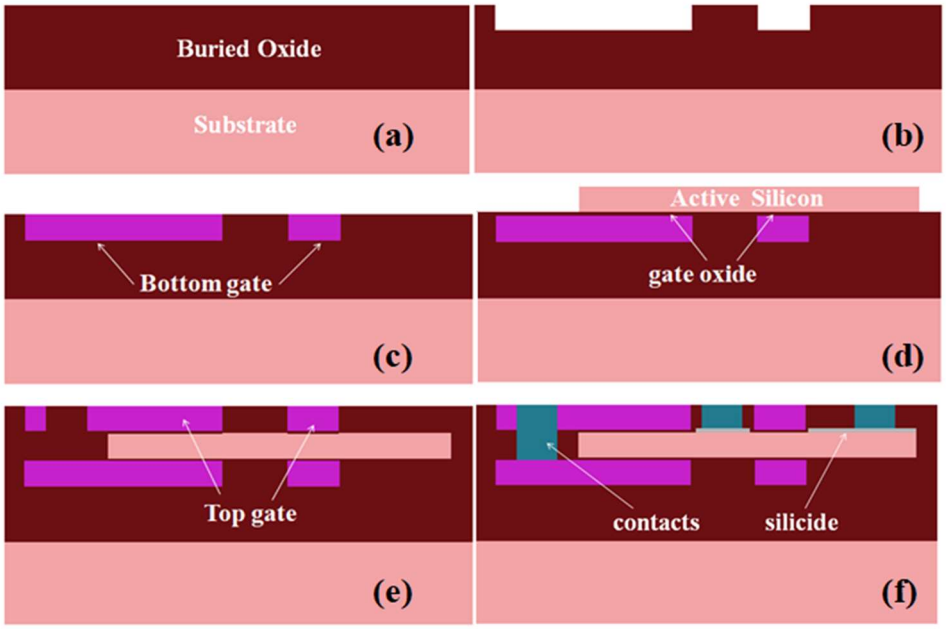
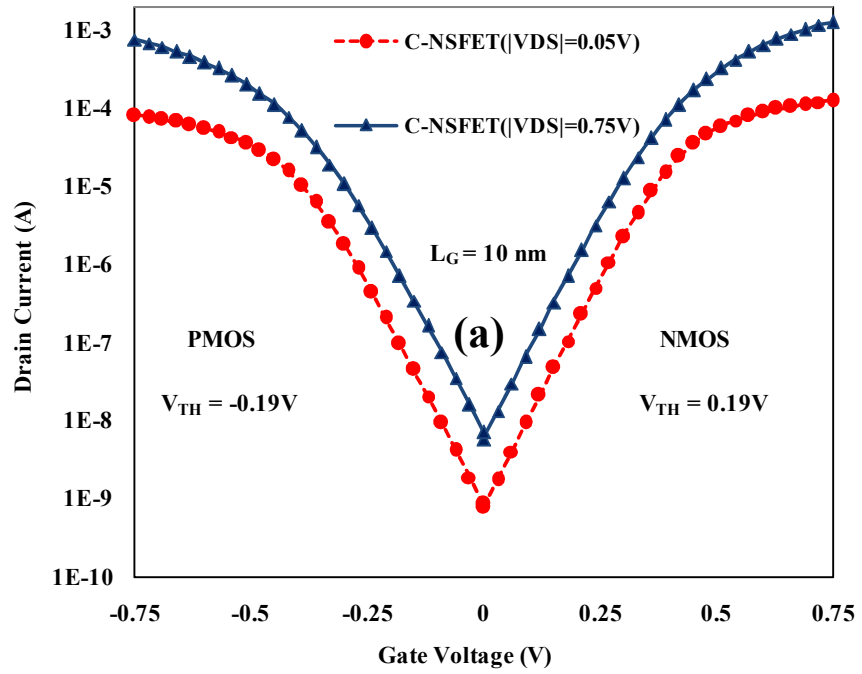


Fig. 5.17: Fabrication process of proposed C-NSFET in 2D view, (a) Thermal oxidation of bulk silicon, (b) lithography & RIE bottom gate cavities, (c) Deposition of bottom metal gate& RIE, (d) Active Silicon island deposition &patterning, (e) Oxidation of the top gate, metal gate deposition and doping (f) Silicidation, deposit metal and RIE etch.

5.7.2. Simulation Methodology

C-NSFETs were designed using Gds2mesh and simulated using Genius 3D device simulator at a 10 nm technology node. During the performance analysis of the C-NSFET device at the 10 nm technology node, the same simulation setup which is discussed in Chapter 3 for HP applications is used. In this work, to match the threshold voltage for both NMOS & PMOS devices with IRDS 2017 projections [139] (using the constant-current technique), the authors modified the metal gate work function. To maintain the device threshold voltage to 0.19 V for HP applications, the authors adjusted the metal gate work function to 4.53 eV for the NMOS device & 4.71 eV for the PMOS device.



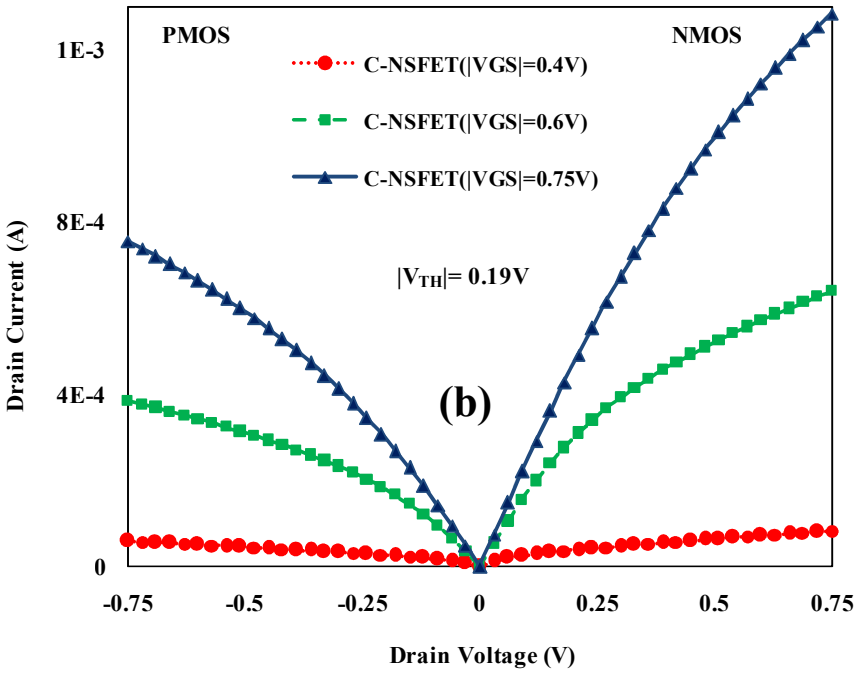


Fig. 5.18: (a) I_{DS}-V_{GS} of C-NSFETs for both N-type & P-type devices for L_G=10 nm, corresponding V_{TH} values given in legend, (b) I_{DS} -V_{DS} of C-NSFETs for both NMOS & PMOS devices.

Fig. 5.18 shows the simulation results of the C-NSFET for both NMOS & PMOS devices with the calibrated setup. Fig. 5.18 (a) shows I_{DS}–V_{GS} characteristics of C-NSFET after tuning the metal gate work function to match the V_{TH} (~|0.19V|) at higher drain-to-source voltage

V_{DS}=0.75V. Fig. 5.18 (b) shows the corresponding I_{DS} - V_{DS} characteristics. In Fig. 5.18, it can be observed that the proposed C-NSFET shows good electrical characteristics in terms of device ON current in the order of mA (NMOS: ~1.26 mA; PMOS: ~ 0.75 mA), device leakage currents in the order of nanoamps (NMOS: ~5.7 nA; P-type: ~7.1 nA), I_{ON}/I_{OFF} ratio greater than 10^5 (NMOS: ~2.2 × 10^5; PMOS: ~1.06 × 10^5), SS of about (NMOS: ~ 82 mV/dec; PMOS: ~ 86 mV/dec), and DIBL of about (NMOS: ~105 mV/V; PMOS: ~113 mV/V).

Table 5.14 shows the performance comparison of the proposed C-NSFET with the existing advanced novel structures, such as FINFET, NWFET, and NSFET [138] at sub 10 nm technology node for NMOS devices. All these devices have identical doping concentrations, EOT, and supply voltages**.** The doping concentration in source/drain regions is 1 × 10^{20} cm^{-3}, and the channel/substrate doping concentration is 1 × 10^{15} cm^{-3}, EOT of 1 nm (SiO_2) and supply voltage of 0.7V have been considered. During this analysis, the device parameters are adjusted to similar values to make an identical comparison with these novel structures. The I_{OFF} is taken at V_{GS} = 0 V, and the device I_{ON} at V_{GS} = V_{DS} = 0.7 V. From Table 5.14, it can be noticed that the proposed device C-NSFET provides the highest normalized drive current compared to all other structures, and which is about approximately 14 times more than the next best NSFET. Because of its superior drive current, it is benchmarked for HP applications.

Table 5.14: Performance analysis of proposed C-NSFET with existing novel structures.

Device (NMOS)	**Simulated FINFET** [138]	**Simulated NWFET** [138]	**Simulated Nanosheet** [138]	**Proposed C-NSFET**
Gate length	~ 12 nm	~ 12 nm	~ 12 nm	~ 10 nm
Threshold voltage (V)	~ 0.158	~ 0.176	~ 0.164	~ 0.176
I_{ON} (µA/µm)	~724	~732	~832	**~11648**
I_{OFF} (nA/µm)	~19	~4.6	~13.3	~88.3
I_{ON}/I_{OFF} (× 10^5)	~ 0.38	~1.6	~0.63	~1.32
SS (mV/dec)	~77	~66	~74	~84.7

5.8. Stacked Circular Nanosheet MOSFET (SC-NSFETs)

To further improve the device drive current for HP applications, a novel circular stacked Nanosheet concept, i.e., stacking of NSs (2-sheet, 3-sheet, and 4-sheet) with circular layout geometry is proposed. Fig. 5.19 shows the stacked circular NSFETs (SC-NSFETs). In this

Fig. 5.19, the thickness of each Nanosheet is considered as 5 nm. In these SC-NSFETs, all Nanosheets are stacked vertically with 7 nm spacing between them (1nm SiO_2 + 5nm gate thickness +1nm SiO_2). Table 5.15 summarizes all the geometrical parameters of the SC-NSFETs during the device creation & simulation. All these stacked structures are likewise formed using the same layout (Fig. 5.16 (c)), along with a modified process file to account for multiple Nanosheets.

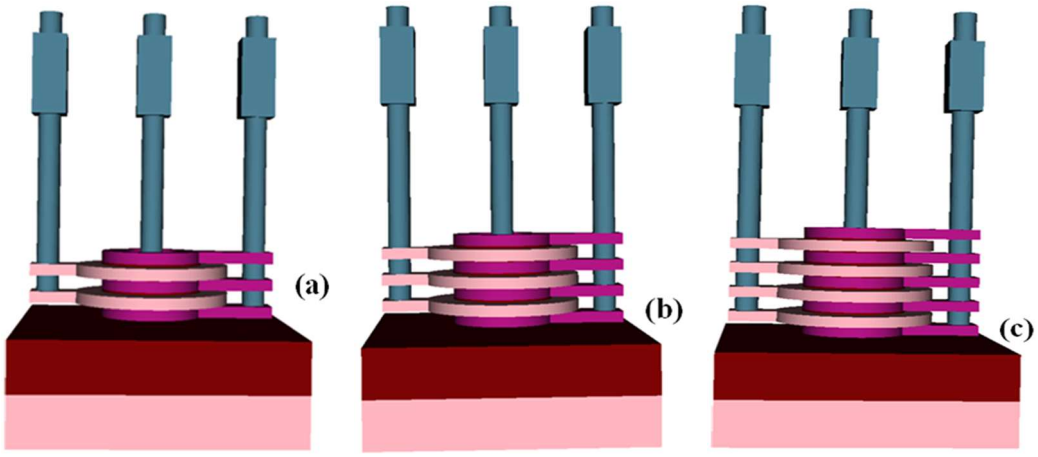


Fig. 5.19: 3-D schematic view of stacked Circular Nanosheet FET, (a) 2-sheet (b) 3-sheet, (c) 4-sheet C-NSFETs.

Table 5.15: Geometrical parameters for 10-nm node SC-NSFETs.

Geometrical parameters	**NMOS**	**PMOS**
Gate length (L_G)	10 nm	
No. of Nanosheets (NS)	2, 3, 4	
NS thickness (T_{ch})	5 nm	
NS spacing (T_{sp})	7 nm	
Gate thickness (T_G)	5 nm	
Gate dielectric thickness (T_{ox})	1 nm	
Source/Drain doping	1×10^{20} cm^{-3}	
Channel doping	1×10^{15} cm^{-3}	

For these multiple stacked circular Nanosheets (Fig. 5.19), the calibrated simulation setup given in section 3 is utilized. To further understand the benefits of stacked structures, examined these stacked devices in terms of device-level FoM, such as device I_{ON}, I_{OFF}, and I_{ON}/I_{OFF} ratio. These multiple stacked circular NS devices were employed with the same work functions (NMOS: 4.53 eV; PMOS: 4.71 eV) that were given in section 5.7.2. The constant current approach is used to extract the device V_{TH} at I_{DS}= NS × (W/L_G) × 10^{-7} A. Where NS = number of Nanosheets.

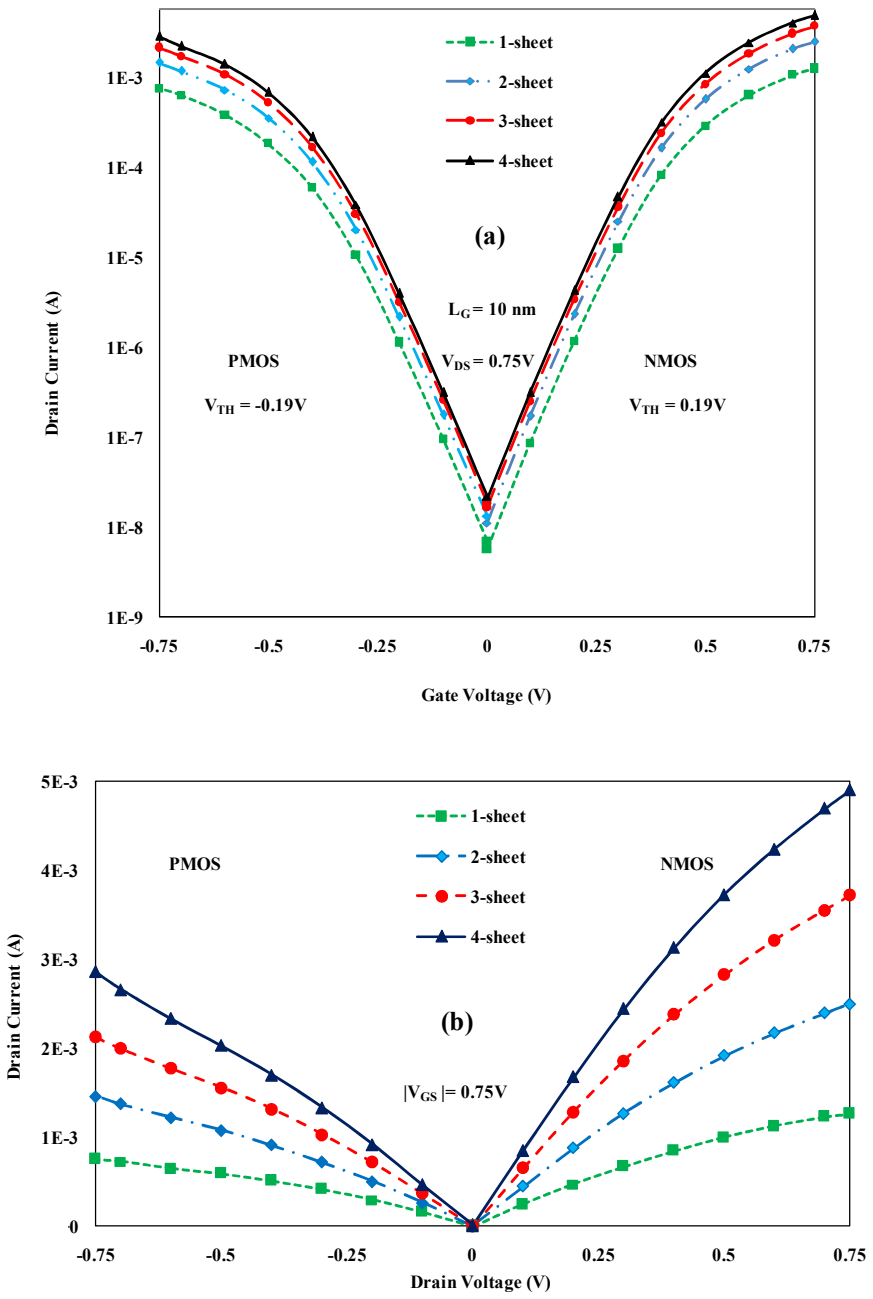


Fig. 5.20: (a) I_{DS}-V_{GS} of stacked C-NSFETs, (b) I_{DS} -V_{DS} of stacked C-NSFETs ON current comparison of different stacked C-NSFETs for both NMOS &PMOS devices.

Fig. 5.20 shows the electrical characteristics of different SC-NSFETs for both NMOS & PMOS devices. Fig. 5.20 (a) depicts the change in transfer characteristics as the number of Nanosheets increases from one to four at high V_{DS} = 0.75 V. Fig. 5.20 (b) shows the output characteristics I_{DS} – V_{DS} curves of stacked (1 to 4) circular NSFETs at V_{GS} = 0.75 V. From Fig. 5.20, it can be said the drive current in the four sheets circular MOSFET is nearly four

times that of the single sheet circular MOSFET. i.e., as the number of sheets increases, the effective width increases with the same footprint, thus improving device drive current.

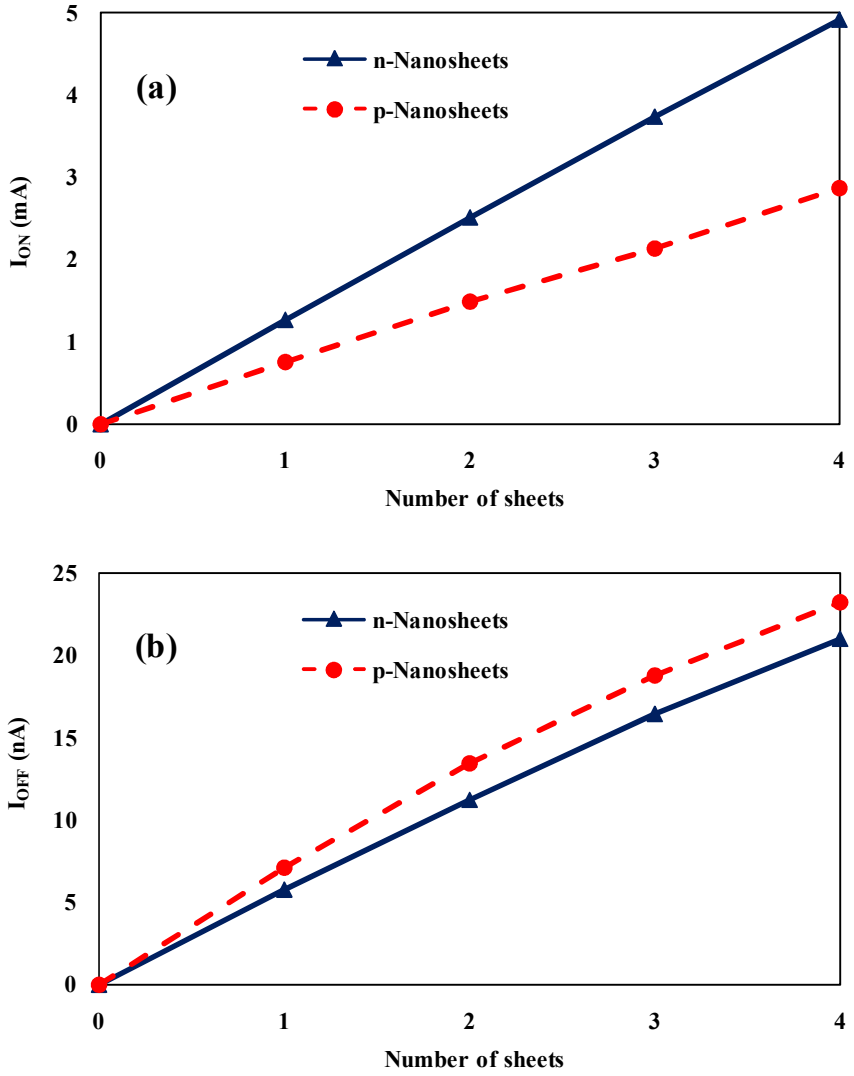


Fig. 5.21: (a) ON current comparison of different stacked C-NSFETs, (b) OFF current comparison of different stacked C-NSFETs for both NMOS & PMOS devices.

Other key metrics derived from electrical characteristics include I_{ON}, I_{OFF}, SS, DIBL, and V_{TH}. Fig. 5.21 shows device ON & OFF current comparison of different SC-NSFETs for both NMOS & PMOS FETs. It should be noted that the I_{ON} and I_{OFF} currents increase as the number of circular nanosheets increases although the I_{ON} / I_{OFF} ratio is almost constant (NMOS: ~2.3×10^5; PMOS: ~1.2×10^5) at high V_{DS} = 0.75 V. The stacked C-NSFET has a larger saturation current than a single C-NSFET because it has more electron conducting channels, greater mobility, and reduced S/D parasitic resistance. Similarly, C-NSFETs have greater I_{OFF} owing to their higher effective width due to multiple sheets. With this new

concept like stacking of circular nanosheets, a very high drive current is achieved. As the stacking of sheets increased from one to four, the device ON current is increased from ~1.26 mA to ~ 4.9 mA for N-type devices. Further, the comparison of different SC-NSFETs is tabulated in Table 5.16. Even when the number of nanosheets is increased to four, the SS, DIBL, and V_{TH} are found to be almost same. For NMOS devices, these values are respectively ~ 82 mV/dec, ~ 105 mV/V, and ~ |0.19V|. Similarly, for PMOS devices ~ 86 mV/dec, ~ 113 mV/V, and ~ |-0.19V| respectively.

Table 5.16: Performance analysis of SC-NSFETs.

Device type	**1-sheet**		**2-sheet**		**3-sheet**		**4-sheet**	
Parameter	**NMOS**	**PMOS**	**NMOS**	**PMOS**	**NMOS**	**PMOS**	**NMOS**	**PMOS**
V_{TH} (V)	0.19 (HP)							
I_{ON} (mA)	1.26	0.75	2.5	1.47	3.72	2.12	4.9	2.86
I_{OFF} (nA)	5.7	7.1	1.12	1.34	1.64	1.87	2.1	2.33
I_{ON}/I_{OFF} ($\times 10^5$)	2.21	1.06	2.23	1.09	2.27	1.13	2.33	1.22
SS (mV/dec)	85	86	84	85.3	83.6	84.7	83.2	84
DIBL (mV/V)	105	115.3	104.8	112.7	104.6	111.7	103.8	110.6

The above analysis shows that SC-NSFETs give improved electrical performance, with an ON/OFF current ratio of more than10^5, and a very excellent drive current of nearly 5 mA with similar foot-print. These novel SC-NSFETs are a suitable alternative technology for building high-current-rate integrated circuits, such as current drivers and power stages, while reducing the die size and chip cost for future scalability.

5.9. Summary

In this chapter, the CDGT with inner radius R1= 10 nm & 20 nm are proposed at the sub 10 nm technology node for LP & HP applications and extracted the DC, analog/RF parameters. Among these, the CDGT device with R1 = 20 nm provides a better ON current. These architectures have a significant DIBL, which results in a low I_{ON}/I_{OFF} ratio. To optimize the performance of the CDGT device underlap structures are explored. The introduction of the underlapping concept to the CDGT device with inner radius R1 = 20nm lowers leakage currents. CDGT with both R1= 20 nm & underlap length of 2nm has the best I_{ON}/I_{OFF} ratio. In addition, the behavior of several CDGT architectures with high –k dielectric used as a gate stack are investigated. It enhances the overall electrical characteristics of the device as well as the analog/RF performance. Benchmarked the CDGT device's ON current relative to its area

to provide suggestions for the future development of multi-gate silicon technology nodes. Finally, the proposed C-NSFETs at 10 nm gate length for both NMOS & PMOS devices are analyzed for their electrical performance for HP applications. Furthermore, a novel device is proposed with the stacking of multiple Nanosheets in circular layout geometry.

Chapter-6

6. Circuit Performance and Radiation Effects analysis of Circular MOSFETs

In Chapter 4 and 5, the detailed device level performance analysis of different circular MOSFETs is presented. Several design metrics such as DC characteristics (I_{ON}, I_{OFF}, I_{ON}/I_{OFF} ratio, DIBL, and SS), and analog/RF characteristics (TGF, g_m, V_{EA}, and g_d) were considered during this analysis. The impact of different device, process, and material level variations such as raised S/D topologies, junctionless mode of operation, underlap concept, and use of high - k dielectric materials are analyzed on the best device (CDGT).

The detailed circuit performance analysis of different circular MOSFETs are explored in this chapter. Initially, the circuit performances of several circular MOSFETs which are already described in Chapter 4 at the 30 nm technology node are investigated by analyzing the dynamic CMOS inverter behaviour. In the analysis of CMOS inverter performance, the propagation delays of different circular MOSFETs are estimated with the help of parasitic capacitances by using the effective current model [145] [146] [147]. Furthermore, at the sub 10 nm technology nodes, the inverter circuit performance of CSGT and CDGT devices is analyzed using the transient simulation. The Static Noise Margin (SNM) levels, DC response, transient response, and propagation delays are under consideration during the comparison of these circular MOSFETs. Additionally, this chapter explores the impact of radiation on the device and circuit performance, including TID effects and SEE effects.

6.1. Circuit Performance Analysis of Circular MOSFETs

6.1.1. Inverter Performance Analysis at 30 nm Technology Node

In Chapter 4, the performance of different circular MOSFETs at 30 nm technology node are evaluated. The circuit performance of these circular MOSFETs such as CSGT, CDGT, raised 'both' CDGT and raised 'both' CDGT JL device (1×10^{18} cm^{-3}) are examined in this analysis. Here, the authors investigated the propagation delay (T_d or t_p) performance of the above-mentioned structures using a two-stage inverter with FO1 delay, as shown in Fig. 6.1.

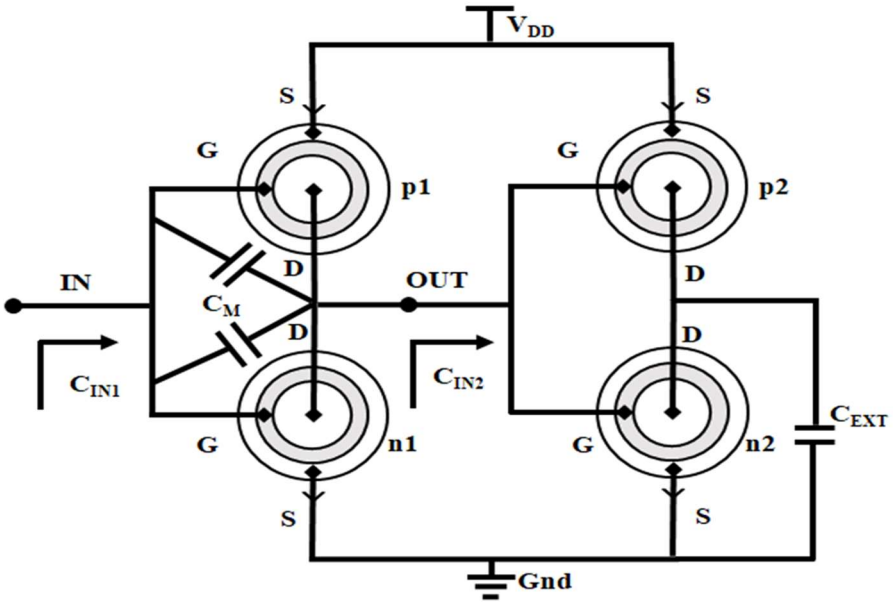


Fig. 6.1: Schematic view of a two-stage inverter.

The inverter delay of the CMOS is extracted from transient simulations or obtained using the effective drive current model given by eq. (6.1) [145], where V_{DD} is the supply voltage.

$$T_d = 0.5\, C_L \times {}^{V_{DD}}\!/_{I_{eff}} \tag{6.1}$$

Where, I_{eff} is the effective drive current and it is defined as by eq. (6.2) [146],

$$I_{eff} = {}^{(I_H + I_M + I_L)}\!/_{3} \tag{6.2}$$

Here, I_H is the drain current (I_{DS}) when the supply voltage of V_{DS}= 0.5V_{DD} and V_{GS} =V_{DD}. I_M is the drain current (I_{DS}) when the supply voltage of V_{DS} = 0.75V_{DD} and V_{GS} = 0.75V_{DD}. I_L is the drain current (I_{DS}) when the supply voltage of V_{DS}=V_{DD} and V_{GS} = 0.5V_{DD} [146]. These currents are extracted from the respective voltage-current characteristics. C_L is the load capacitance of the first-stage inverter at the node denoted by 'OUT.' The value of C_L is evaluated from the parasitic first-stage (Miller-amplified) output and the input capacitance of the second stage according to eq. (6.3), where M is Miller's coefficient and is considered to be 1.5 [73].

$$C_L = MC_M + C_{IN} \tag{6.3}$$

C_{IN2} is determined from the weighted distribution of PMOS and NMOS during the input transitions of the ON- and OFF-state capacitances. For example, during the output fall

transition to 0.5V_{DD}, the transistor p2 remains in the ON state, and n2 changes from OFF to ON. Similar to this, the transistor p2 turns on during the output-rise transition to 50% of V_{DD} while n2 stays in the ON state position. Thus, in both cases, the OFF to ON ratio 0.25:0.75 [146] [73] [148] can be used to obtain C_{IN2}, as described in eq. (6.4).

$$C_{IN2} = 0.25C_{G\_OFF} + 0.75C_{G\_ON} \tag{6.4}$$

Here, C_M , C_{G_OFF}, and C_{G_ON} are expressed as follows.

$$C_M = C_{GD\_OFF}(PMOS) + C_{GD\_OFF}(NMOS) \tag{6.5}$$

$$C_{G\_OFF} = C_{G\_OFF}(PMOS) + C_{G\_OFF}(NMOS) \tag{6.6}$$

$$C_{G\_ON} = C_{G\_ON}(PMOS) + C_{G\_ON}(NMOS) \tag{6.7}$$

As per the eq. (6.1), the propagation delays of high-to-low transition (t_{pHL}) and low-to-high transition (t_{pLH}) are expressed as follows.

$$t_{pHL} = 0.5\, C_L \times {V_{DD}}/{I_{eff\ (NMOS)}} \tag{6.8}$$

$$t_{pLH} = 0.5\, C_L \times {V_{DD}}/{I_{eff\ (PMOS)}} \tag{6.9}$$

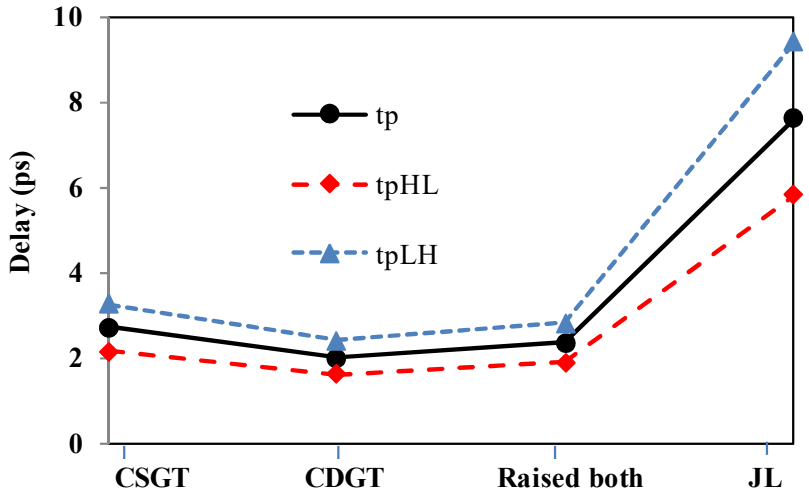


Fig. 6.2: Delay characteristics of different circular MOSFETs.

In Fig. 6.2, the authors show the calculated inverter delay for the several types of circular MOSFET mentioned above. Among these circular MOSFETs, the CDGT SOI MOSFET structure provides the smallest delay, with a value of 2 ps, whereas the raised 'both' JL (1 ×

10^{18} cm^{-3}) structure yields the highest delay of all, with a value of 7.6 ps. This is due to a lower I_{eff} current with moderate doping of 1×10^{18} cm^{-3}. Even though the JL mode of operation provides more delay, it reduces the SCE, thermal budget, and fabrication complexity when scaling technology down to nodes below 30 nm.

6.1.2. Inverter Performance Analysis at 10 nm Technology Node

In Chapter 4, the performance of different circular MOSFETs such as CSGT and CDGT devices at a 10 nm technology node is evaluated. In this section, the circuit-level performance of both CSGT and CDGT devices at this node is done by implementing a CMOS inverter by using the same Gds2mesh tool (described in Chapter 3) and analyzed its transient and DC characteristics for HP and LP applications. The same device level process flow (described in Chapter 4) is utilized to build both CSGT and CDGT CMOS inverters, with the only difference being that the device layout is changed to the inverter layout. The layout based metal interconnect lines and other inter device effects have been included during the design of a complete inverter cell.

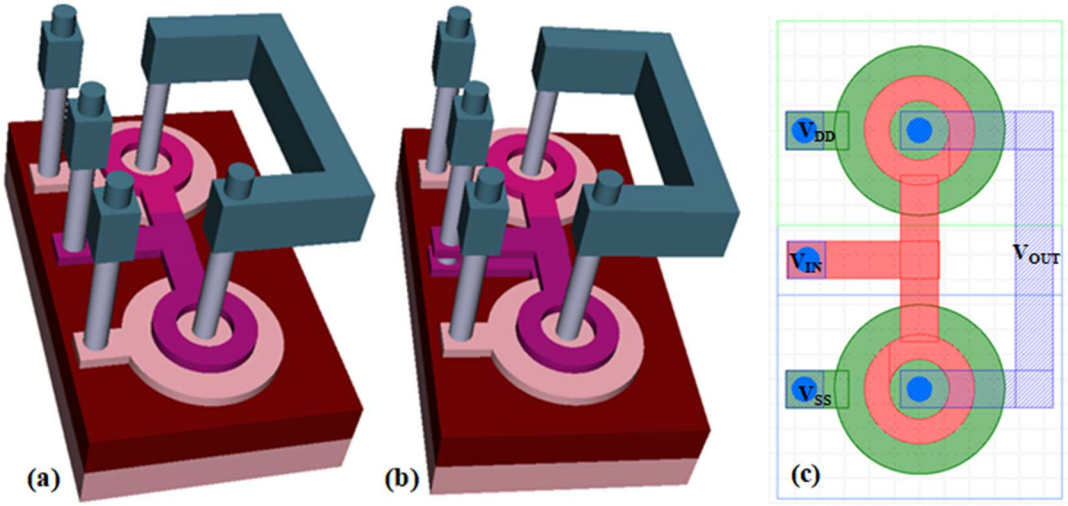


Fig. 6.3: (a) & (b) CSGT and CDGT inverters respectively, (c) corresponding layout.

Fig. 6.3 shows the schematic view of the CMOS inverter. Fig. 6.3 (a) and 6.3 (b) shows the equivalent 3D views of proposed CSGT and CDGT CMOS inverters respectively, and the corresponding layout used to create these inverter structures is also shown in Fig. 6.3 (c). During the analysis of proposed CSGT/CDGT inverters, the authors followed IRDS 2017 projections [139] for dimensions and supply voltages. As per IRDS rules, we have considered gate oxide (SiO_2) thickness of 1 nm, the supply voltage of 0.75V, and the V_{TH} of 0.19 V for

HP & 0.32V LP applications. The metal gate work function is tuned to maintain the same threshold voltage for HP and LP applications during the simulation.

In the CMOS inverter, Supply voltage (V_{DD}) is chosen as 0.75 V. The rising edge time constant (T_r), falling edge time constant (T_f), and delay time (T_d) have all been set at 100 ps for the CMOS inverter's transient response. Pulse width and the repeating period of the pulse train of the input signal (V_{IN} (t)) are chosen as 400 ps, and 1ns, respectively.

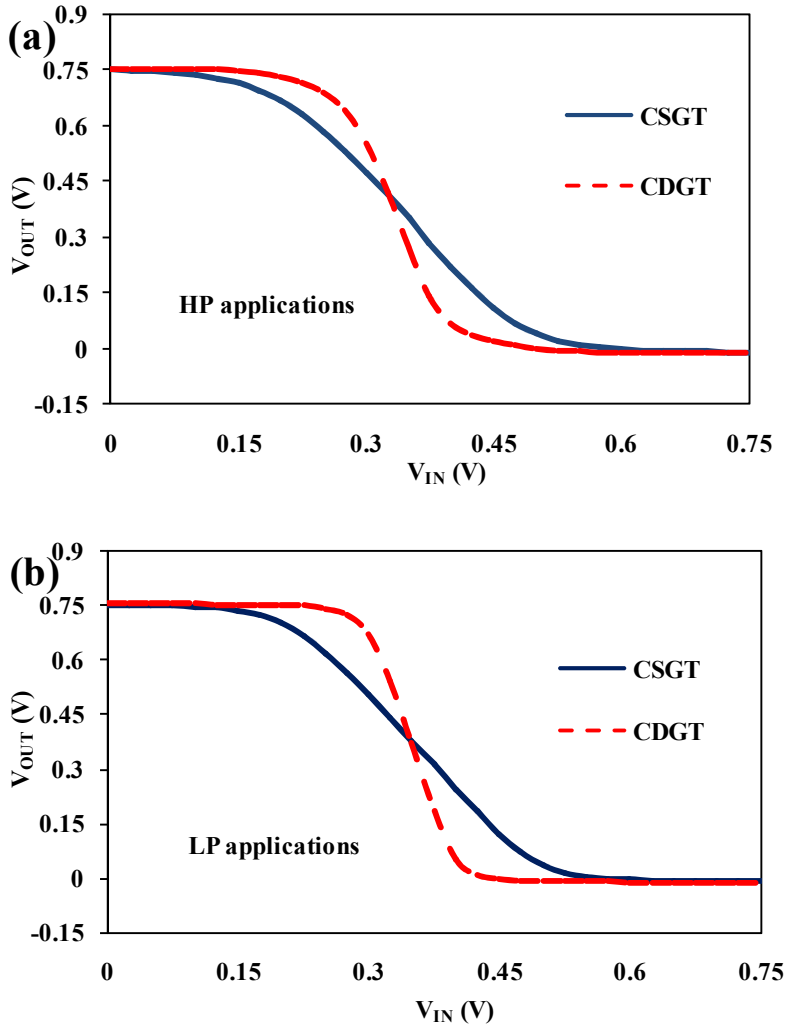


Fig. 6.4: DC characteristics of CSGT and CDGT CMOS inverters, (a) HP, (b) LP applications.

Fig. 6.4 shows the DC characteristics of the CSGT and CDGT SOI CMOS inverter for HP (Fig.6.4 (a)) and LP (Fig. 6.4 (b)) applications. From this Fig. 6.4, the proposed CDGT inverter has a better switching speed compared to the CSGT inverter. The corresponding SNM butterfly diagrams are shown in Fig. 6.5. From these figures, we can observe that the

noise margin is improved by increasing the threshold voltage, and the CDGT CMOS inverter has a better noise margin compared to CSGT CMOS inverter. The noise margin values of CSGT and CDGT CMOS inverters are given in Table 6.1. In this Table 6.1, the noise margin levels are improved by 50 % in the case of CDGT compared to the CSGT inverter.

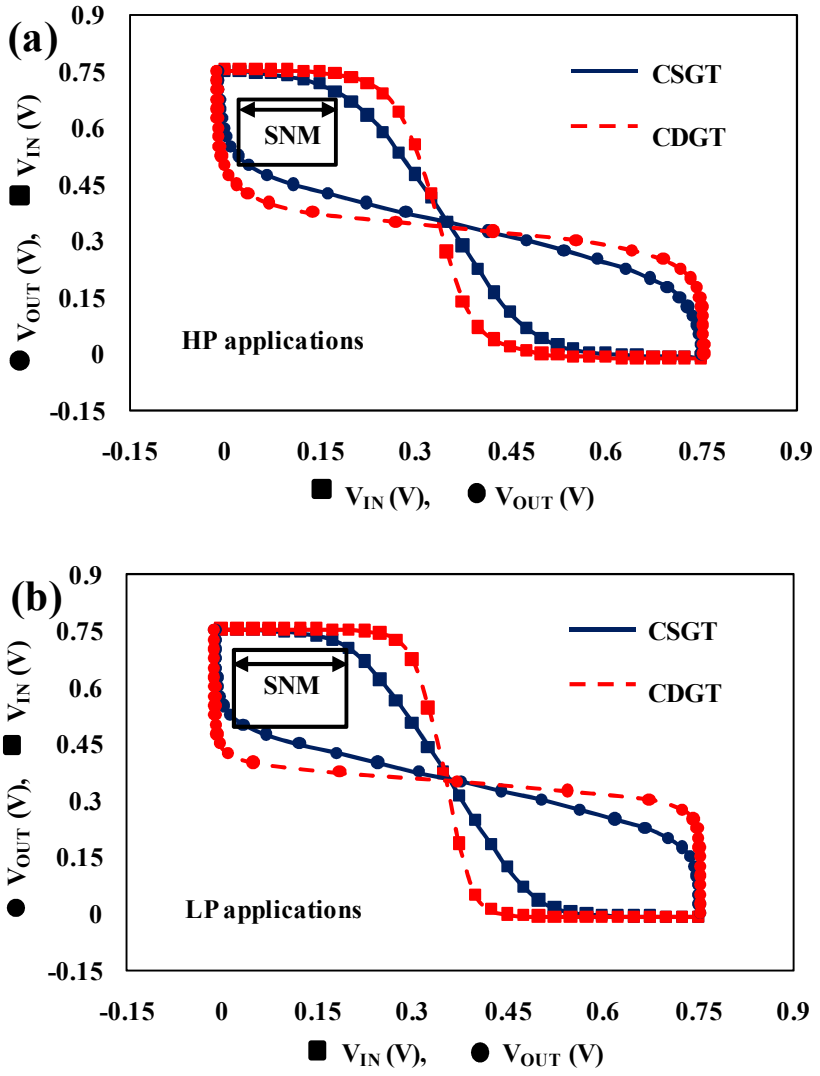


Fig. 6.5: Butterfly curves and SNMs of CSGT and CDGT CMOS inverters, (a) HP, (b) LP applications.

Table 6.1: Noise margin of CSGT and CDGT CMOS inverters for HP and LP applications.

Parameters	V_{TH} (V)	V_{IL} (V)	V_{IH} (V)	V_{OL} (V)	V_{OH} (V)	NM_L (V) = V_{IL}-V_{OL}	NM_H (V) = V_{OH}-V_{IH}
CSGT (HP)	0.19	0.181	0.493	0.0463	0.692	0.1346	0.199
CDGT (HP)	0.19	**0.234**	**0.422**	**0.0403**	**0.7103**	**0.1936**	**0.2883**
CSGT (LP)	0.32	0.193	0.503	0.0302	0.7105	0.1627	0.2075
CDGT (LP)	0.32	**0.273**	**0.419**	**0.0154**	**0.7281**	**0.2576**	**0.309**

Table 6.1 demonstrates that, in comparison to HP applications, an increase in the threshold voltage for LP applications causes an increase in the noise margin low (NM_L) and noise margin high (NM_H) levels of both CSGT and CDGT inverters. Because of its better controllability, i.e., by shielding the channel with two gates the proposed CDGT CMOS inverter has higher noise margin levels (less sensitive to noise) compared to the CSGT CMOS inverter.

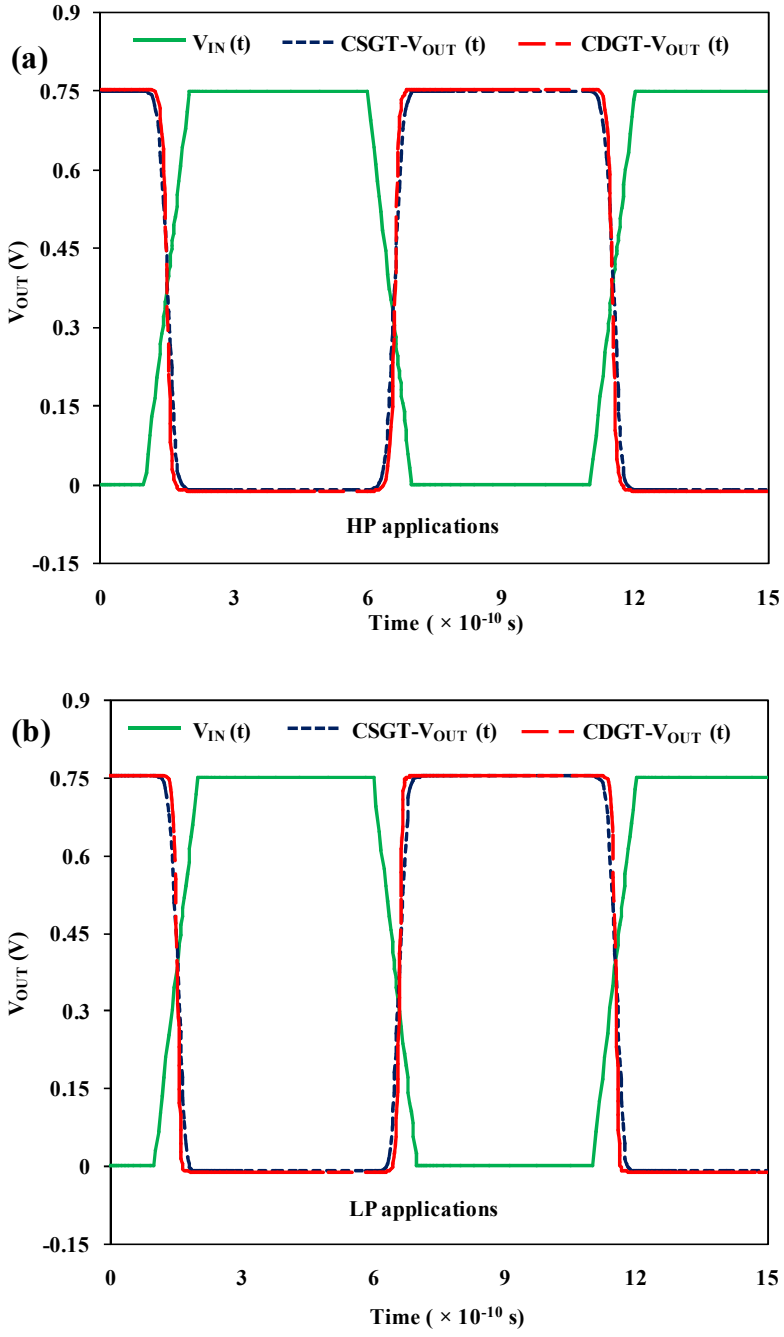


Fig. 6.6: Transient responses (V_{OUT} (t)) of CSGT and CDGT CMOS inverters, (a) HP, (b) LP applications.

The transient output voltage (V_{OUT} (t)) response of the CMOS inverter for both CSGT and CDGT devices is depicted in Fig. 6.6. The transient response for HP applications is shown in Fig. 6.6 (a), the transient response for LP applications is shown in Fig. 6.6 (b). From Fig. 6.6, it is evident that the T_f and T_r of CDGT CMOS inverter output voltage V_{OUT} (t) is less compared to CSGT CMOS inverter. Because of higher I_p(t) and I_n(t) of CDGT CMOS inverter, the fall and rise times of the inverter are reduced. Here, I_p(t) and I_n(t) are the currents flowing through the PMOS and NMOS of the CMOS inverter, respectively as shown in Fig. 6.7. Since both devices have higher threshold voltages for LP applications than HP applications, it is clear from Fig. 6.7 that these two current component values are lower for LP applications.

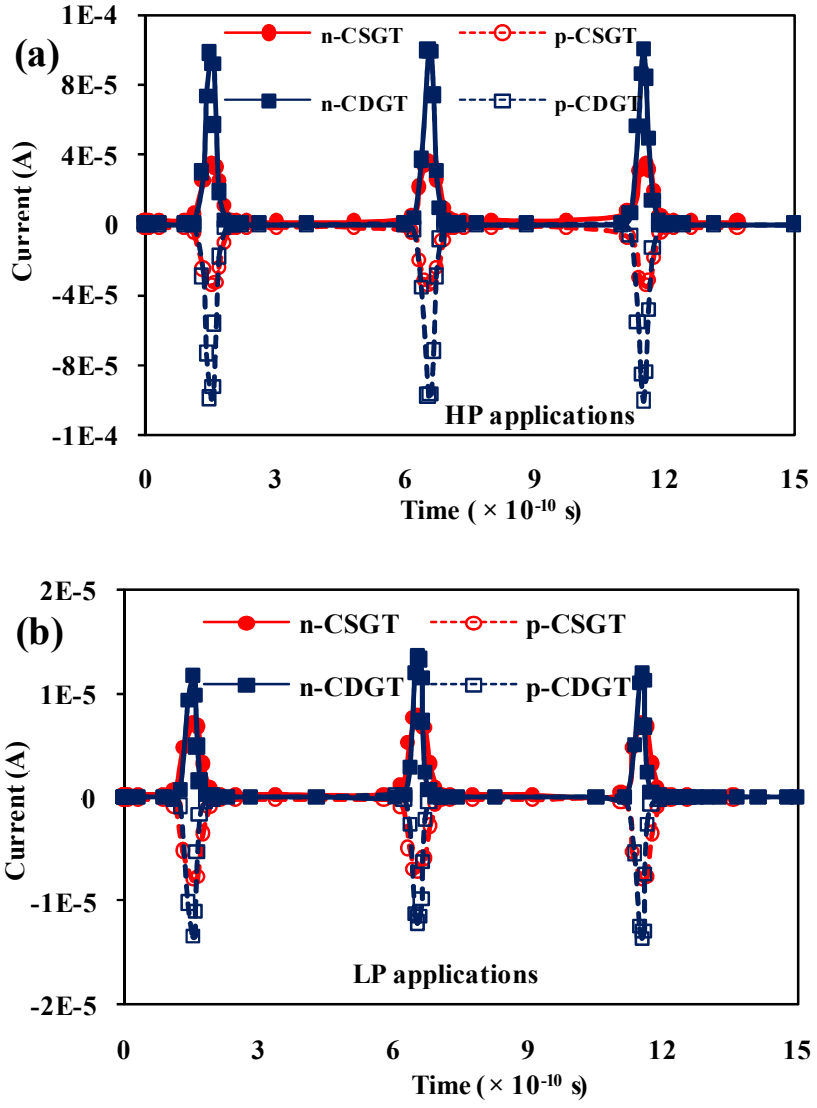


Fig. 6.7: Transient response of currents (Ip (t) and In (t)) in CSGT and CDGT CMOS inverters, (a) HP, (b) LP applications.

6.2. Radiation Effects in Circular MOSFETs

6.2.1. Radiation Basics

The entire world is covered and surrounded by microelectronics, and a number of them are launched into space on a regular basis. There are over 5400 active satellites orbiting the Earth, according to Ref. [149]. From an electronics perspective, the radiation environment in which these systems must operate is much more hostile than the ground level.

The effects of radiation are not just limited to space. It was already proven in 1976 that bit errors are caused by atmospheric neutrons in computers used at the Los Alamos National Laboratory in the United States [150]. In the 1960s, it was believed that radiation caused displacement damage dose and TID in electronics. The first prediction on the increasing risk of failure in electronics with technological revolution was made by Wallmark and Marcus [151] in 1962. As technology advances toward the nano scale and our dependence on electronics in daily life activities (international and national security, communication, transport, etc.) increases, this makes us vulnerable to malfunctions. Even at ground level, it is impossible to completely avoid cosmic radiation, but the effects can be minimized. Understanding how radiation and matter interact as well as the mechanisms that affect electronics is essential for this. In this section, the physical principles that go on when energetic heavy-ions interact with matter and have an impact on silicon-based devices and materials is discussed.

When an energetically charged particle passes through matter, it loses energy through various mechanisms. According to [152], the various energy loss mechanisms are listed as follows. Here, the ionizing radiation is defined as radiation with enough energy to remove electrons from atoms and create ions.

1. Projectile excitation and ionization
2. Excitation and ionization of target atoms
3. Electron capture
4. Electromagnetic radiation
5. Recoil loss (nuclear stopping)

In addition, the following reactions may also contribute to the energy loss:

6. Chemical reactions
7. Nuclear reactions

Most of the energy loss is typically caused by mechanisms 1 and 2. The physical characteristics of the target material are permanently or temporarily altered by particle irradiation. Since ionizing radiation (mechanisms 1-3) primarily breaks covalent bonds only in the target material, it is generally considered non-destructive. Depending on the substance, these broken bonds either immediately reassemble themselves or can be repaired by high temperature annealing. In truth, heavy ions alter the target permanently. One reason is that material modification happens as a result of the high density of ionization caused by the high energy atomic number ions. On the other hand, the nuclear stopping (mechanism 5) causes the energetic target to recoil, which could cause the target's atomic structure to change.

6.2.2. Types of Radiation Effects in Electronics

In electronics, a wide range of various effects is produced by each of the aforementioned mechanisms of energy deposition for heavy ions. Typically, there are two main categories for these effects: Cumulative effects and SEEs.

6.2.2.1. Cumulative Effects

Cumulative effects are divided into two types: Displacement Damage Dose (DDD) and TID. This cumulative stress of radiation over time can gradually alter the characteristics of microelectronics, such as shifting the V_{TH} and reducing the minority carrier lifetimes.

Displacement Damage Dose

Displacement damage dose effects in electronics are induced by Non Ionizing Energy Loss associated with the particle radiation [153] [154]. The Non Ionizing Energy Loss is defined as the portion of the energy deposited by an ion in the target that does not form electron-hole pairs. Due to the ion hit, the atoms are knocked out of their lattice sites and resulting in an interstitial vacancy pair known as a Frenkel pair or defect. This loss has been used to describe displacement damage's effects on electronic devices, such as dark current in solar cells and reduction in minority carrier lifetimes in bipolar devices. Generally, a reduction in the current gain of dark currents in BJT or charge-couple devices is attributed to these defects.

Total Ionizing Dose (TID) effects

TID effects are driven by radiation induced charge carriers that survive recombination and are not swept away by electric fields [106]. Because holes are the least mobile of the charge carriers, recombination is considered to be significant especially in dielectrics like SiO_2. These effects can happen in both bipolar and MOS devices [128]. The TID effects are characterized by Linear Energy Transfer (LET) [155]. The term "LET" refers to the typical energy deposited by striking the particle per unit length. Generally, it can be expressed in terms of MeV-cm2/mg.

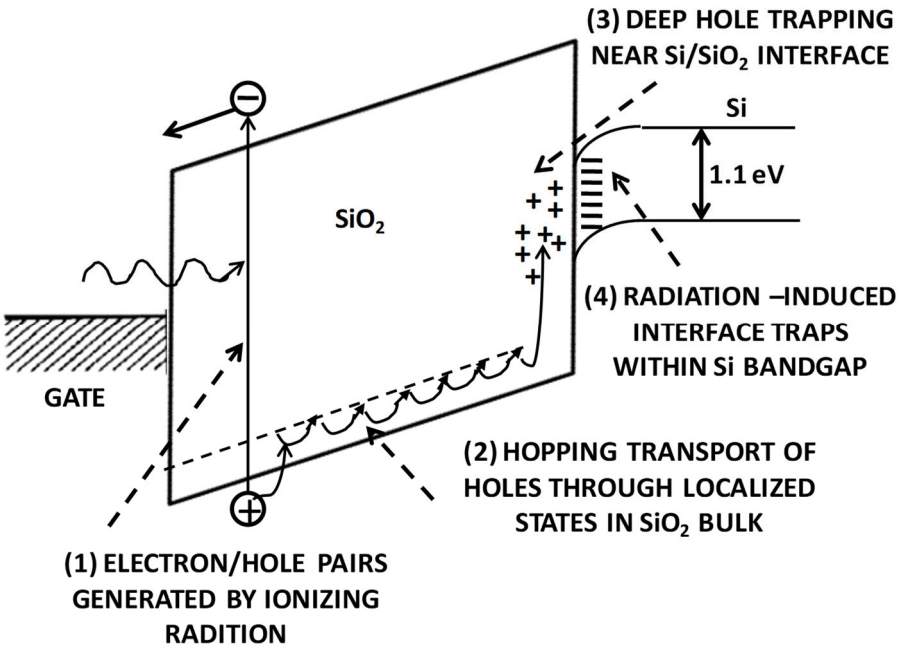


Fig. 6.8: An illustration of a MOS structure's energy band diagram, highlighting the primary physical mechanisms underpinning the radiation response [106].

Fig. 6.8 displays the schematic MOS structure's schematic energy band diagram, which depicts the fundamental physical radiation response [106]. In Fig. 6.8, the gate is subjected to positive bias, causing electrons to flow in its direction and holes to move to the Si substrate. The gate insulator, which is the most radiation-sensitive component of a MOS system, requires consideration of four major physical processes. Radiation that penetrates the gate oxide produces electron/hole pairs in the valence and conduction bands of SiO_2. In SiO_2, the electrons are swept out of the oxide much faster than the holes because the electrons are much more mobile [156]. A certain percentage of the electrons and holes will combine again. A massive portion of the holes that manage to avoid the initial recombination are relatively

immobile and remain close to where they were created. When they are present, a MOS transistor experiences a negative threshold voltage shift. The first processes shown in Fig.6.8 are the generation of electron/hole pairs and recombination.

The transport of the holes to the Si/SiO_2 interface is shown as the second process in Fig. 6.8. This process is complex, dispersive, and highly dependent on the temperature, oxide thickness, and applied electric field. The third process in Fig. 6.8 is that a portion of the transporting holes enter a relatively deep, long-lasting trap state when they come into contact with the Si interface. These trapped holes, also known as fixed-charge, result in a residual negative voltage shift. The radiation-induced accumulation of interface traps directly at the Si/SiO_2 interface is the fourth important factor in the MOS radiation response. These traps are localized states with Si band gap energy levels. There is a voltage-dependent threshold shift as a result of the occupancy of these particles being controlled by the Fermi level (or by the applied voltage). The processing of the oxide and other factors (such as temperature and applied field) has a significant impact on interface traps [156].

Many studies have been conducted over the last three decades in an attempt to develop a model of the SiO_2 total dose effect. The scientist Rowsey developed a self-contained physical model to estimate the TID effects in SiO_2 layers.

6.2.2.2. Single Event Effects (SEEs)

SEEs are the instantaneous responses of electronics to ionization events caused by a single energetically charged particle. These charged particles have the ability to ionize materials, which causes the formation of e-h pairs in dielectrics and semiconductor. These SEEs are classified into two types: soft errors (non-destructive) and hard errors (destructive).

Soft Errors

A "soft error" is the term used to describe an ion's temporary disruption of an electronic circuit that can be fixed by reprogramming the hardware. These soft errors are divided into several types as follows [157].

Single Event Upset: Single event upset is an event that occurs when a memory bit (or bits) is flipped from 1 to 0 or 0 to 1. “Single Bit Upset” is the term used to describe an effect where only one bit is changed at a time. When multiple bits are corrupted, the event is known as

“Multiple Bit Upset,” can occur in highly scaled memories because of ion hits with high grazing angles. The single event upset is the oldest type of SEE [158].

Single Event Transient (SET): The consequences of a SET are influenced by factors such as the operating frequency of the circuit. The consequences of a SET are affected by factors such as the circuit's operating frequency. If a SET is latched, it can become a single event upset. An "Analog Single Event Transient” is the term used to describe the transient disturbance brought on by an ion hit in analog devices (such as operational amplifiers, comparators, and voltage regulators). Analog single event transients can produce faulty signals that can spread throughout an integrated circuit and cause serious anomalies, like system failure or data corruption [159].

Single Event Functional Interrupt: Device functionality is lost as a result of single event functional interrupt. When this occurs, the device malfunction can be resolved without having to restart (power cycling) the device. In a control bit or in a register, these events are commonly associated with single event upsets.

Due to advancements in technology, it is now more crucial than ever to prevent the soft errors mentioned above in both general commercial electronics and space electronics [158]. Modern microelectronics has already developed a number of mitigation techniques that can be used on either the circuit level or the software level to reduce soft errors [160].

Hard Errors

In some circumstances, a device's current may peak due to a particle-induced "cloud" of e-h pairs, resulting in high currents that ultimately lead to destructive failure. Compared to the soft errors mentioned above, these irreversible hard errors typically happen less frequently. Since these hard errors cause the device to be partially or entirely inoperable (out of service), they play a significant role in the radiation reliability of electronics. These typical destructive hard errors are divided into several types as follows [161].

Single Event Latchup: In a device, single event latchup is a potentially destructive condition where a single ion strike establishes a conductive path between the device powers rails (V_{DD} and the ground). Only by turning off the power supply can the current in this path be stopped. If the supply’s current is not restricted and/or the device's power cycling is not carried out quickly enough after the current increase, this event may destroy the device.

Single Event Gate Rupture: In MOS devices, single event gate rupture refers to the breakdown of the gate oxide, which is attributed to the ion-induced conductive path. The material melts down due to thermal runaway caused by the excessive current through the dielectric. Since the event occurs quickly and makes it difficult to measure the current spikes accurately, the fundamental physical mechanisms underlying single event gate rupture is still unknown. There are only a few semi-empirical or qualitative models that can predict this event.

Single Event Burnout: In MOSFET or bipolar power devices, single event burnout is a common failure. Lightly doped epitaxial layer creates a highly conductive path through which high current flows during this event, eventually causing thermal runaway and irreversible damage. In many instances, power MOSFETs experience both single event burnout and single event gate rupture simultaneously.

By restricting the supply current, single event latchup and single event burnout can be minimized. The SEL can also be avoided using SOI technology [162]. However, once the threshold conditions (energy deposition density and oxide electric field) are exceeded, single event gate rupture can't be avoided [161].

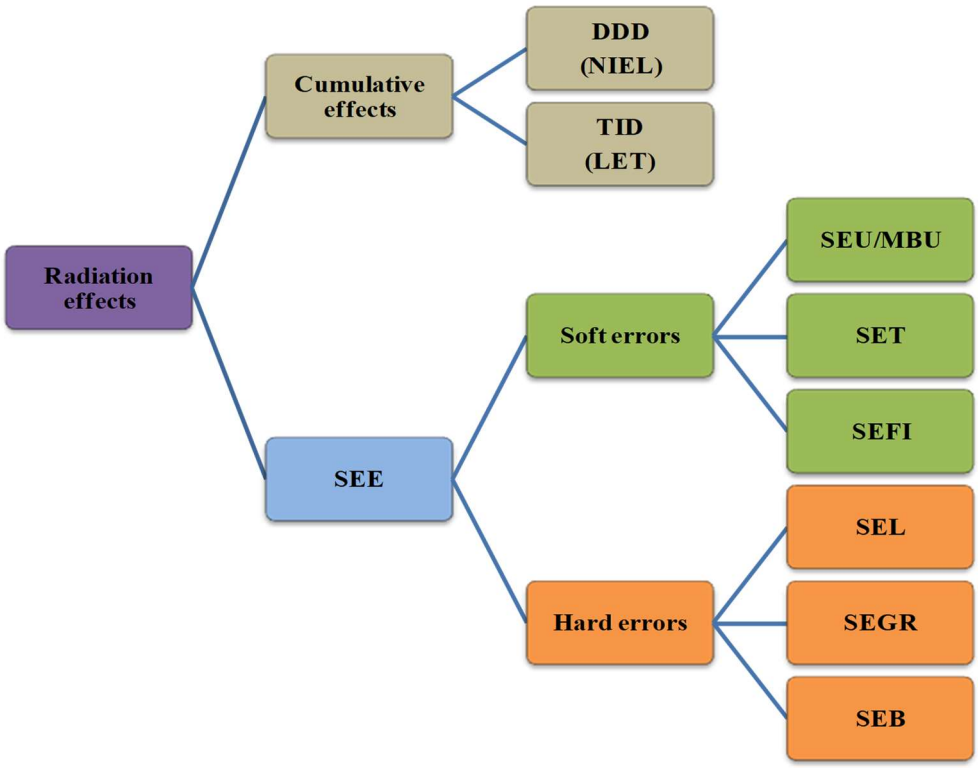


Fig. 6.9: Radiation effect classification.

As this thesis is more focused on fundamental mechanisms such as TID effects and SET responses, thus the different radiation effects in detail further are not discussed in detail further. Fig. 6.9 shows the complete radiation effects classification. Many of these radiation effects in advanced novel structures like FinFET, NW, and NSFETs are already discussed in Chapter 2.

6.2.3. Analysis of TID Effects on Circular MOSFETs

In the previous section, the authors discussed the basics of radiation and the several types of radiation effects in electronics. This section discusses the impact of TID effects on the electrical characteristics of both CSGT and CDGT devices (circular MOSFETs). As mentioned in the previous section, Cogenda TCAD employs Rowsey's doctoral thesis [127] physical model of TID in the SiO_2 layer, which estimates carrier transport, recombination, generation, and trapping. Here, the mobile uncharged particle is described with the diffusion model, and the drift-diffusion model is used for the mobile charged particle. The trap inside SiO_2 is also taken into account while simulating the trapping of holes [115]. The amount of trapped charge carriers is calculated in terms of interface trap charge density. The 3D device model is created based on process rules and layout using the Gds2mesh tool. The radiation effects are generated via the visual particle tool and then applied to the 3D device model. Further, the genius tool is utilized for simulation. This software can be programmed to simulate different radiation doses. The effects in the buried oxide layer are also considered.

The Genius simulator solves the various equations to evaluate the charge generation by using the TID command (as shown in Fig.3.9 from Chapter 3) as an input. Prior to TID simulation, operating point simulation is performed using the device's worst-case biasing. In the worst-case scenario, all CMOS device terminals other than the gate should be grounded. The goal of this simulation is to model the V-I characteristics of MOS under various dose scenarios. In the TID simulation flow (as shown in Fig.3.10 from Chapter 3), different dose steps from 0 Krad to 500 Krad are developed and the V-I characteristic curve for each step is analyzed.

During irradiation, the devices under test were deployed in a static working environment that is representative of both CSGT and CDGT NMOS devices operating at (drain voltage (V_d) = gate voltage (V_g) = 0.75 V, and source voltage (V_s) = 0 V). The analysis of TID effects on DC characteristics of both CSGT and CDGT devices were simulated

without radiation (0 Krad: pre-radiation) and with radiation dosage ranging from 100 Krad (Rad: Radiation absorbed dose) to 500 Krad.

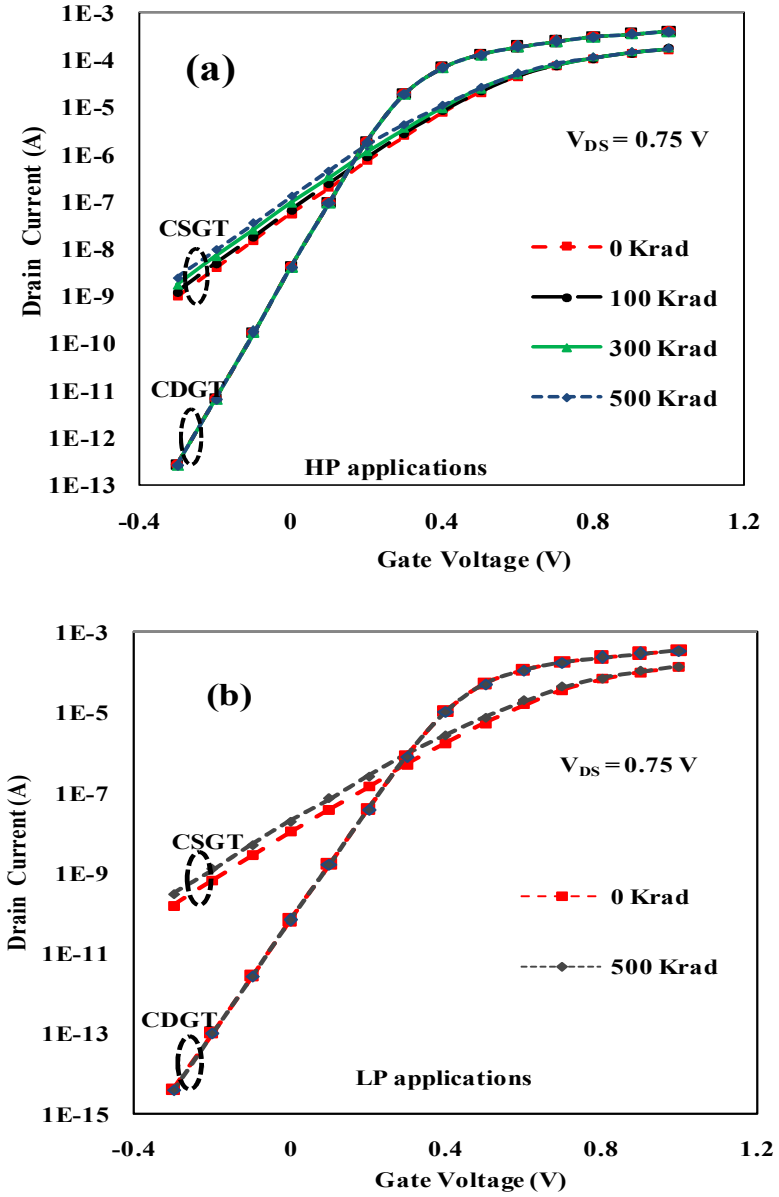


Fig. 6.10: Effect of radiation dose on device characteristics of CSGT and CDGT, (a) HP, (b) LP applications (NMOS devices).

Fig. 6.10 shows the influence of TID effects on I_{DS}-V_{GS} characteristics of CSGT and CDGT NMOS devices at V_{DS} = 0.75 V. Fig. 6.10 (a) depicts the I_{DS}-V_{GS} characteristics of both devices for HP applications under various radiation doses ranging from 0 Krad to 500 Krad. Fig.6.10 (b) represents electrical characteristics for LP applications. To visualize the impact of TID effect on device leakage current easily, the high dose (500 Krad) and a low dose (0 Krad) curves are shown in Fig. 6.10 (b). In Fig. 6.10, the OFF state leakage currents increase

slightly with an increase in radiation dose, because of their enclosed circular gate structures, the impact of TID effects is minimum in both CSGT and CDGT devices when compared to advanced novel structures like FinFET, NW, and NSFETs. In Fig. 6.10, it can be observed that the OFF current is increased by 2 times with an increase in radiation dose up to 500 Krad in the case of CSGT devices, and there is negligible change in the case of CDGT devices. At the same dosage of 500 Krad (post-radiation), the above mentioned advanced novel structures have 3 to 4 decades increment in leakage currents [43][114]. This is attributed to the circular gate and double gate structure in the CDGT device.

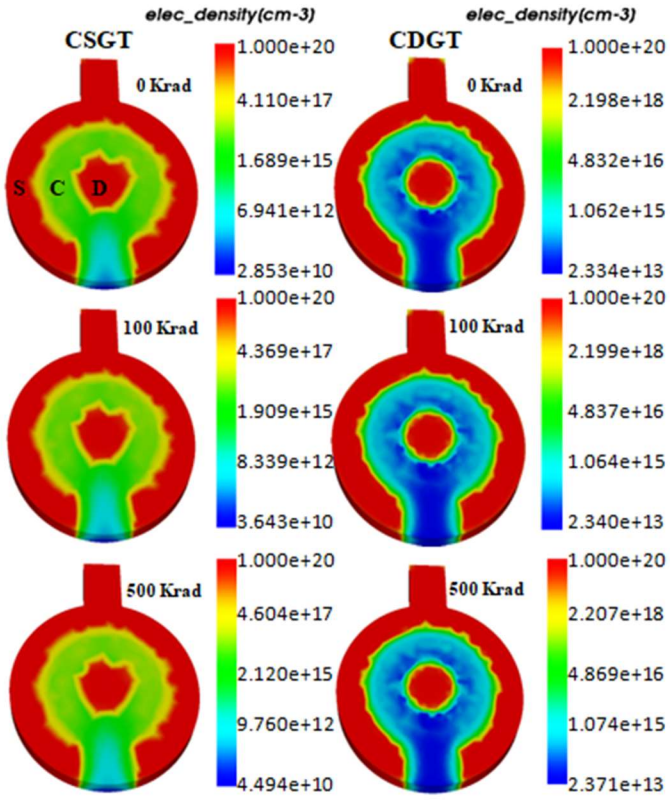


Fig. 6.11: Charge density distributions under the TID effect with different doses.

To get further clarity on TID effects, the electron density of the devices at different radiation doses is shown in Fig. 6.11. In Fig.6.11, 'S' indicates the source region, 'C' indicates the channel region, and 'D' indicates the drain region. In general, when the radiation dose increases, the fixed charge in the oxide region increases which leads to increase in the electron density near the interface between the channel and the buried oxide layer, resulting in a sub-threshold current. According to Fig. 6.11, the electron density increases from 1.69×10^{15} cm^{-3} to 2.12×10^{15} cm^{-3} in the case of the CSGT device as the radiation dosage increases to 500 K, while it remains nearly constant (~ 4.8×10^{16} cm^{-3}) in the case of the CDG device.

As a result, the sub-threshold leakage currents of the CSGT device have increased with the TID effects, whereas there is almost no change in the sub-threshold leakage currents for the CDGT device.

Table 6.2: Impact of TID effects on device threshold voltage and leakage currents.

Device (NMOS)	**CSGT**		**CDGT**	
Parameters	**V_{TH} (V)**	**I_{OFF} (A)**	**V_{TH} (V)**	**I_{OFF} (A)**
0 Krad	0.2185	5.58×10^{-8}	0.175	4.15×10^{-9}
100 Krad	0.205	6.73×10^{-8}	0.175	4.15×10^{-9}
300 Krad	0.18	9.41×10^{-8}	0.175	4.16×10^{-9}
500 Krad	0.1575	1.28×10^{-7}	0.175	4.17×10^{-9}

Table 6.2 shows the effect of radiation dose on both device threshold voltage & leakage currents. The threshold voltage (V_{TH}) of the device shifts after it is exposed to radiation. The threshold voltage shift is caused by the combined effect of threshold shift of trapped hole in silicon dioxide (SiO_2) and in the interface [128]. Table 6.2 shows that when the radiation dosage is raised to 500k, the leakage current increase by more than 50% in the case of the CSGT device, but it is nearly constant in the case of the CDGT. With this analysis, it can be said that the impact of TID effects on CDGT devices is negligible compared to CSGT. Because of its high radiation tolerance, the proposed CDGT device is the optimum solution for Military and Aerospace applications.

6.2.4. Analysis of SEEs on Inverter Performance of Circular MOSFETs

In the earlier sections, the circuit performance analysis of different circular MOSFETs such as CSGT and CDGT devices is analyzed by implementing the CMOS inverter and discussed the basics of radiation effects (TID and SEEs). Here, in this section, the impact of SEE effects such as SET on the transient response characteristics of both CSGT and CDGT inverters is presented.

The inverter circuit design employed in the SEE simulation is depicted in Fig. 6.12. During this radiation analysis, the layout based metal interconnects lines and other inter device effects have been included in the design of the complete inverter cell. The ionizing alpha particle is assumed to strike the drain of a CDGT NMOS device (Fig. 6.12). Ionizing radiation causes the NMOS device to turn on abnormally and flip the output in transient time as the inverter is pulled up. During the process of SEEs simulation, the low and high energy particles with LETs of 1.5 MeV-cm^2/mg and of 35 MeV-cm^2/mg, respectively are considered.

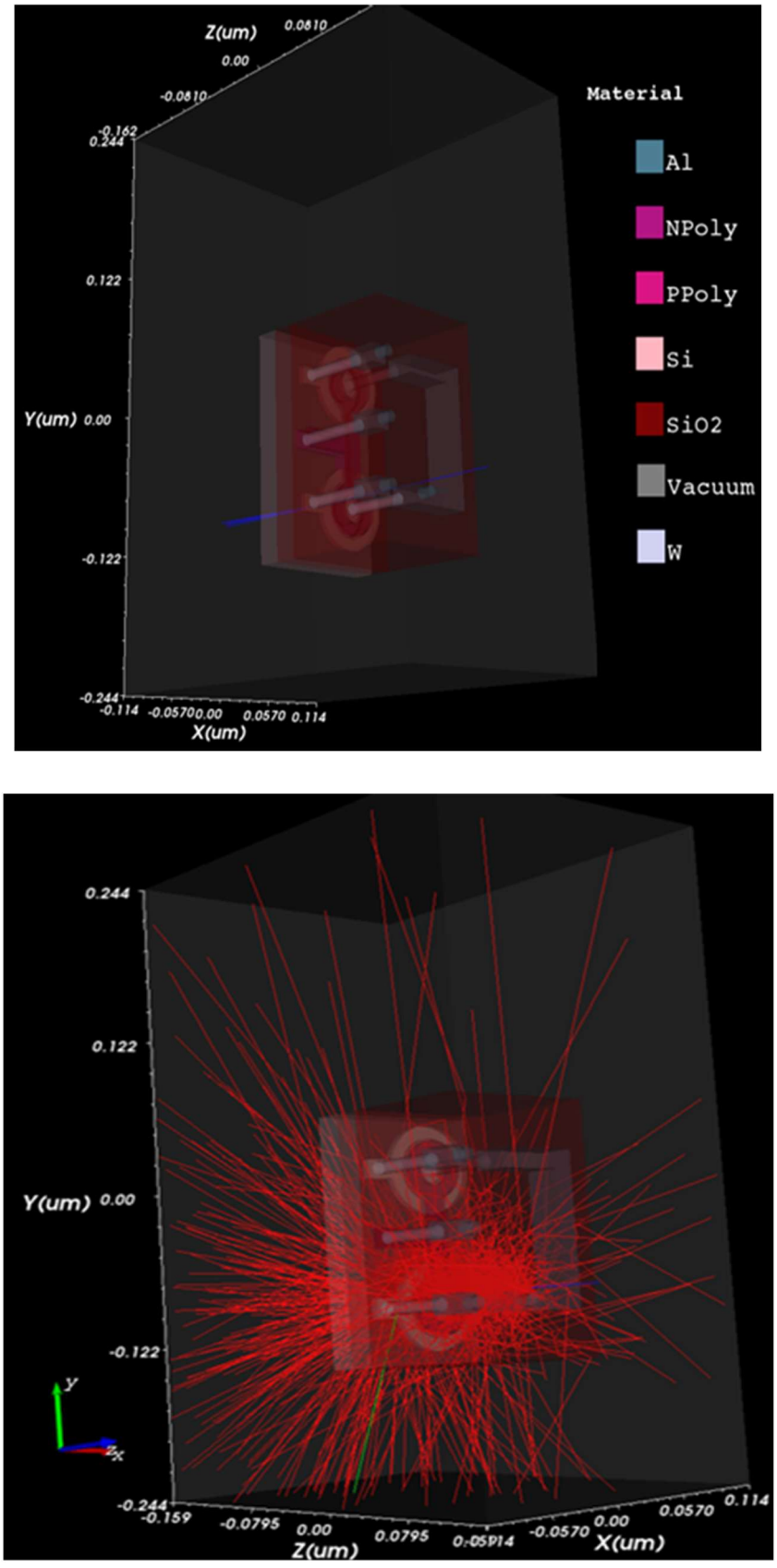


Fig. 6.12: 3D-view of CDGT CMOS inverter with particle strike on the drain of an NMOS device for SEE simulation a) low-energy particle (top) b) high-energy particle (bottom).

In this analysis, 1.5 MeV-cm^2/mg LET is assumed to represent the worst-case scenario of the alpha particle effect, whereas 35 MeV-cm^2/mg LET is intended to represent a heavy ion (iron) strike in space. Here, the same biasing conditions are used defined in section 6.1.2 (Inverter performance analysis). From Fig.12 (b), it is observed that the particle penetrates deeper in the X- direction, showing the worst SET case.

Fig. 6.13 shows the single event transient response of both CSGT and CDGT CMOS inverters with incident radiation energy particles. The influence of the energy particle at the drain junction is extremely significant, as illustrated in Fig. 6.13 (a), because the produced electrons near the drain side may be directly collected as the drain current, turning on the NMOS device in both CSGT and CDGT. As the LET is higher for high energy heavy ion, the influence of SET becomes higher as illustrated in Fig. 6.13 (b). However, the SET of the CDGT MOSFET is significantly smaller than that of the CSGT because the CDGT has better gate controllability due to two gates, which reduces the undesired flow of generated free carriers. Despite the energy particle strike, the CDGT device's strong gate field due to circular layout can maintain the off state well, thus allowing the transient value on the output node to quickly revert to its original output level. With the benefit of circular layout in both CSGT and CDGT, as shown in Fig 6.13 (a), the maximum node potential drop is still less than 150 mV V for CSGT and less than 50 mV for CDGT. It is indicating that low-energy particles with LET of 1.5 MeV-cm^2/mg will not flip the output in both cases.

It is found that both CSGT and CDGT are highly immune to low-energy particles, and the LET is increased to 35 MeV-cm^2/mg to analyze the transient effect of high-energy particles. The largest transient is detected when ionizing radiation penetrates in the Z-direction, as illustrated in Fig. 6.12 (a). The accumulation of charge becomes significant because not only does the particle penetrate in all directions, but radiation ionization happens in the bulk region in both inverters. Similar to low energy particle analysis, with high energy particle striking, the maximum node potential drop is approximately 0.65 V for CSGT, and it is approximately 0.55 V for CDGT inverters, as shown in Fig. 6.13 (b). i.e., with the advantage of circular layout, though the LET is increased to 35 MeV-cm^2/mg, still output will not flip completely, and the output node quickly reverts to its original output level. From Fig. 6.13 (c) (SET pulses) and with the above analysis, CDGT has stronger SET immunity than CSGT. From Fig. 6.13 (c), it is evident that the output voltage quickly gets back to its original value within 10 ps in the case of both lower and higher energy particles. A similar analysis is

reported in literature with identical energy particles for advanced novel structures such as FinFET and Nanosheet [105]. The output voltage flipped completely, and the time taken for the output voltage to get back to its previous value is nearly 150 ps for the FinFET device, and 30 ps for the nanosheet device.

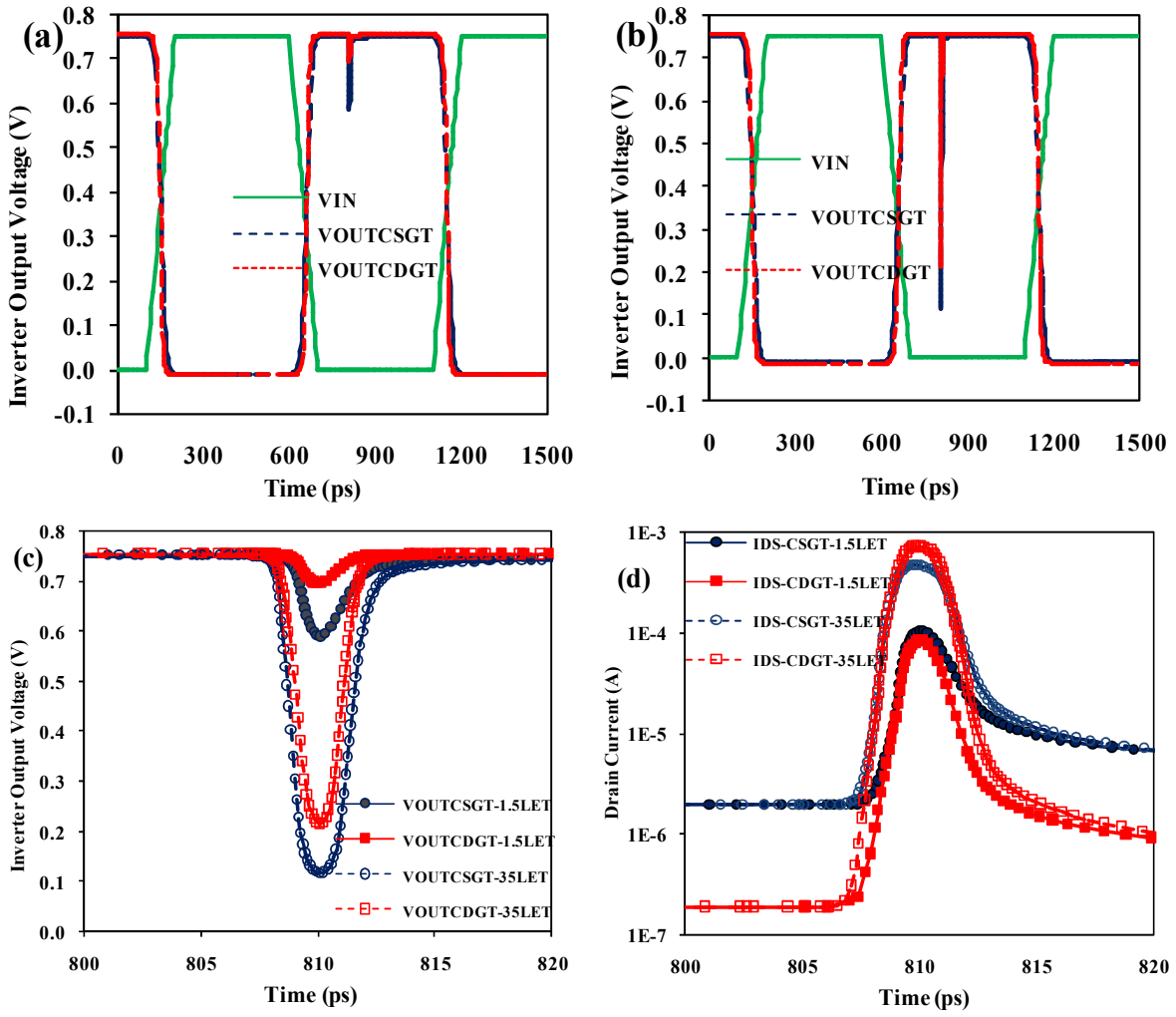


Fig. 6.13: Transient responses of CSGT and CDGT CMOS inverters with SEEs, a) transient response due to incident of low-energy particle, b) transient response due to incident of high-energy particle, c) SET pulses, d) drain current transients due to both low and high LETs.

Fig. 6.13 (d) shows the simulated drain current transient of 10 nm gate length CSGT and CDGT NMOS devices due to both LETs (1.5 MeV-cm^2/mg & 35 MeV-cm^2/mg) striking at the drain side. As displayed in Fig. 6.13 (d), the CDGT device quenches the transient response faster than the CSGT device, indicating that the CDGT has superior gate controllability due to the two gates (front and backside). Moreover, the leakage currents are at lower levels compared to CSGT. The transient at a low leakage level lasts shorter for both

CSGT and CDGT devices due to the fact that having the advantage of circular gate layout geometry in both structures. From this analysis, the proposed circular layout transistors such as CSGT and CDGT devices have better radiation immunity compared to advanced innovative structures such as FinFETs and Nanosheet MOSFETs as given in the reference with a similar analysis [105].

6.3. Summary

In this chapter, the circuit level performance of different circular MOSFETs such as CSGT, CDGT, raised 'both' CDGT, and JL CDGT SOI MOSFETs by examining a two-stage inverter with FO1 delay performance at 30 nm technology node is investigated. Among these, the CDGT device provides least delay of 2 ps. This delay analysis has been performed by using an effective current method and found that CDGT gives the lowest delay of 2 ps among all structures. Further, at the sub 10 nm technology node, investigation at the circuit level performance for CSGT and CDGT SOI MOSFETs is done by designing an inverter circuit using the Gds2mesh tool, analyzing the noise margins from DC simulations & delay form transient simulations. Among them, CDGT provides better inverter performance with higher noise margin levels. Next, the influence of total ionizing dose effects caused by different radiation doses is studied on the CSGT and CDGT FETs. The findings show that TID effects have less influence on the electrical properties of CDGT devices when compared to CSGT devices, particularly in the sub-threshold region. When the radiation dose increases from 0 K to 500 K, the leakage current does not change much in the case of the CDGT device, whereas it is increased approximately 2.3 times in the CSGT device. Further, the impact of single event transient effects due to low energy alpha particles and high energy heavy ion particles are investigated. Though heavy ion striking, the output voltage drop is observed at 0.55 V for CDGT and 0.65 V for CSGT inverters and reverts the voltage to its original value within 10 ps. Because of the advantage of their circular layout geometry, both proposed CSGT and CDGT devices have better immunity to radiation compared to advanced novel structures like FinFET and Nanosheet FETs. However, compared with CSGT, the CDGT shows excellent immunity to ionizing radiation because of better gate controllability with two gates in the structure, and it is better suitable for military and aerospace applications.

Chapter-7

7. Conclusions and Future Scope

In this chapter, the authors summarize the key findings of the research on different circular MOSFETs that was done for this thesis. Further, the authors also offer ideas for providing suggestions that could be conducted to examine a circular MOSFET's complete radiation analysis and potentially use it as a radiation-hardened device.

7.1. Conclusions

The CGT, which is a non-standard enclosed gate transistor, is one of the alternative solutions to the traditional planar transistor. In this thesis, to extend the life of traditional planar CMOS SOI technology for lower sub 10 nm nodes while keeping the SCEs under control, the authors proposed a novel Circular Double Gate Transistor (CDGT) with an internal silicon pad used as drain. Initially, circular MOSFETs such as CSGT and CDGT SOI MOSFETs have been implemented as compatible with SOI CMOS technology at 30 nm technology node and compared their performance with device-level FoM. Here, the FoM such as I_{ON}, I_{OFF}, I_{ON}/I_{OFF} current ratio, SS, and DIBL are compared. When compared to CSGT, CDGT offers better electrostatic controllability over the channel and offers control over the silicon film because two gates electrically shield the channel from the drain voltage on either side (front or back). As a result, the CDGT improves the I_{ON}/I_{OFF} ratio, lowers leakage, and controls SCE.

Further, at the same node, the raised S/D topologies such as raised top, raised bottom, and raised both have been implemented on the CDGT devices to improve the device ON current. To make the fabrication process easier along with control of the SCEs, the JL mode of analysis has been performed on the CDGT device by varying the doping concentration from 1×10^{17} cm^{-3} to 1×10^{19} cm^{-3}. The optimum performance has been observed at 1×10^{18} cm^{-3} with better electrical performance.

Next, the performance of both CSGT and CDGT SOI devices has been analyzed at lower sub 10 nm technology node for LP and HP applications. Among the best device, i.e., CDGT devices, performance is optimized by varying the inner drain radius and the use of underlap concept. With a 20 nm inner drain radius and a 2 nm underlap length, the CDGT device offers the best performance in terms of a higher I_{ON}/I_{OFF} ratio while controlling SCEs.

On these various CDGT devices, the impact of high-k dielectric material (HfO_2) used as a gate stack is also examined. The analog/RF performance and DC characteristics have been taken into consideration during the comparison. With the use of HfO_2, the device has provided better performance in terms of improvement in device ON current, I_{ON}/I_{OFF} ratio, TGF, and V_{EA}. Additionally, the performance of the proposed CDGT device is also compared with that of existing novel structures such as FinFET, nanowire, and nanosheet MOSFETs.

Furthermore, a novel concept known as C-NSFETs at a 10 nm gate length has been proposed for HP applications, by combining the advantages of the nanosheet concept and the circular geometry. To improve the device's performance, the stacking of multiple nanosheets (2 –sheets, three, and four) has been used in circular layout geometry and naming them as SC-NSFETs. The suggested SC-NSFETs with the stacking of four sheets have a high ON current in the order of mA and are more appropriate for building high-current-rate integrated circuits.

Next, the circuit analysis has been performed on various circular MOSFETs by implementing the two-stage CMOS inverter and evaluating the performance at the 30 nm technology node using the effective drive current model. The CDGT-based CMOS inverter with FO1 delay has a better performance compared to all other structure-based CMOS inverters. Using the Gds2mesh tool and transient simulations, a similar analysis has been performed on the DC characteristics, noise margin levels, and transient response of CSGT and CDGT inverter circuits at lower sub 10 nm technology nodes. It has been concluded that the CDGT-based inverter circuit has better DC, transient responses, and higher noise margin levels compared to the CSGT-based inverter.

Finally, to evaluate the influence of TID and SEE effects the radiation analysis has also been performed on different circular MOSFETs. The impact of TID effects on device performance has been evaluated from without radiation (pre-radiation) to with up to a radiation dosage of 500 Krad in a range of 100 Krad. The device threshold voltage and OFF-state leakage currents are the parameters analyzed during this TID analysis. Due to the benefit of circular layout geometry, these circular MOSFETs are less affected by TID effects in sub-threshold regions, and they have no effect (insignificant) at all on CDGT devices. The impact of SEE effects on circuit performance has been evaluated by striking the drain of the NMOS transistor of the CMOS inverter with low and high-energy particles. Here, the worst-case low energy alpha particle with the LET of 1.5 MeV-cm^2/mg, high energy heavy iron ion with LET

of 35 MeV-cm^2/mg, and transient response of the CMOS inverter have been considered during SEE simulations. Like TID effects, because of their enclosed circular layout geometry, both proposed CSGT and CDGT devices are better immune to radiation compared to advanced novel structures like FinFET and NSFETs. However, compared with CSGT, the CDGT exhibits superior immunity to ionizing radiation because of better gate controllability with two gates in the structure, and it is better suitable for radiation environment applications such as military, terrestrial, and aerospace.

Hence, with the detailed analysis on the CDGT device, the scaling performance of the device at lower sub 10 nm technology nodes, circuit performance analysis, and radiation effects analysis, it is concluded that the proposed CDGT device is an alternative solution for high current rate integrated circuits and also an optimum solution for radiation hardened environments for future technology nodes.

7.2. Future Scope

In this thesis, the design of circular MOSFETs such as circular double gate transistors (CDGT) and circular nanosheet FETs has been presented for radiation environment applications. This work can be carried out further based on this thesis as follows.

- It is possible to design universal logic gates (NAND, NOR), ring oscillators, memory cells (SRAM), etc. using circular MOSFETs.
- The detailed analysis of CDGT MOSFET can be carried out in the design of different analog circuits such as current mirrors and differential amplifiers etc.
- The complete radiation analysis can be done on circular MOSFETs. i.e., the analysis of radiation effect such as Single Event Upset on a typical 6T SRAM cell.
- The mathematical analytical model can be developed for the proposed CDGT device.
- The impact of the negative capacitance effect could be analyzed on the different circular MOSFETs.
- Implementation of 2D material based circular MOSFETs, and their performance analysis.

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International Journals

1. S. Kallepelli and S. Maheshwaram, "A novel circular double gate with raised source/drain SOI MOSFET," *Semicond. Sci. Technol.*, vol. 36, no. 6, p. 65009, 2021, https://doi.org/10.1088/1361-6641/abf0e6. **(SCI)**
2. K. Sagar and S. Maheshwaram, "Performance analysis of sub 10nm double gate Circular / Ring MOSFET," *Silicon*, pp. 1–9, 2022, https://doi.org/10.1007/s12633-022-01668-w. **(SCI)**
3. K. Sagar and S. Maheshwaram, "A Novel Vertically Stacked Circular Nanosheet FET for High Performance Applications," *ECS J. Solid State Sci. Technol.***,** https://doi.org/10.1149/2162-8777/ac71c9. **(SCI)**
4. K. Sagar and S. Maheshwaram, "Benchmarking and Optimization of Circular Double Gate MOSFET (CDGT) for Sub 10 nm Nodes," *Silicon***,** 2023, https://doi.org/10.1007/s12633-022-02282-6 . **(SCI)**
5. K. Sagar and S. Maheshwaram, "Radiation Hardness Analysis in Advanced Enclosed Layout Circular MOSFET at L_G = 10 nm," *IEEE Trans. NanoTech.* **(SCI Journal) (Under Review).**

International Conferences

1. K. Sagar and M. Satish, "Performance Comparison of Circular Double Gate Transistor (CDGT) with Novel Architectures for High-Performance Applications," *2022 IEEE International Symposium on Smart Electronic Systems (iSES)*, Warangal, India, 2022, pp. 148-152, https://doi.org/10.1109/iSES54909.2022.00039. **(IEEE)**

Appendix

This appendix presents device structure code of a SC-NSFET (2-sheet) with typical dimensions used in Gds2mesh tool:

L = 10 nm, T_{ox} = 1 nm, NS thickness = 5nm, S/D doping = 1×10^{20} cm^{-3}, channel doping = 1×10^{15} cm^{-3}.

```
__all__=['MosisCMOSMask', 'CMOSProcess']

from ProcessDesc import *

# {{{ MosisCMOSMask

class MosisCMOSMask(GdsiiMask):

    # {{{ map

    map = {

        'N_WELL':          42,

        'P_WELL':          41,

        'CAP_WELL':        59,

        'ACTIVE':          43,

        'THICK_ACTIVE':    60,

        'PBASE':           58,

        'POLY_CAP1':       28,

        'POLY':            46,

        'SILICIDE_BLOCK':  29,

        'N_PLUS_SELECT':   45,

        'P_PLUS_SELECT':   44,

        'POLY2':           56,

        'HI_RES_IMPLANT':  34,

        'CONTACT':         25,

        'POLY_CONTACT':    47,

        'ACTIVE_CONTACT':  48,
```

```
        'POLY2_CONTACT':    55,
        'METAL1':           49,
        'VIA':              50,
        'METAL2':           51,
        'VIA2':             61,
        'METAL3':           62,
        'VIA3':             30,
        'METAL4':           31,
        'CAP_TOP_METAL':    35,
        'VIA4':             32,
        'METAL5':           33,
        'VIA5':             36,
        'METAL6':           37,
        'DEEP_N_WELL':      38,
        'GLASS':            52,
        'PADS':             26,
        'ROUTE_PORT':       24          # Port for routing
      }
  # }}}
  def __init__(self, fname, params=GdsiiMask.Params(), top_level_struct=None):
    super(MosisCMOSMask, self).__init__(fname, params=params,
top_level_struct=top_level_struct)
  # {{{ getLayerList()
  def getLayerList(self):
    return [
      'BBOX',
      ('N_WELL',          0x80ff8d, 0),
      ('P_WELL',          0x80a8ff, 0),
      'CAP_WELL',
```

('ACTIVE', 0x008000, 5),

'THICK_ACTIVE',

'PBASE',

'POLY_CAP1',

('POLY', 0xff0000, 4),

'SILICIDE_BLOCK',

('N_PLUS_SELECT', 0x01ff6b, 12),

('P_PLUS_SELECT', 0xfbe328, 13),

'POLY2',

'HI_RES_IMPLANT',

('CONTACT', 0x0080ff, 1),

'POLY_CONTACT',

'ACTIVE_CONTACT',

'POLY2_CONTACT',

('METAL1', 0x0000ff, 12),

'VIA',

'METAL2',

'VIA2',

'METAL3',

'VIA3',

'METAL4',

'CAP_TOP_METAL',

'VIA4',

'METAL5',

'VIA5',

'METAL6',

'DEEP_N_WELL',

'GLASS',

'PADS',

```
            'ROUTE_PORT']
    # }}}

    # {{{ getLayer()
    def getLayer(self, layer):
        if layer=='BBOX':
            return self.getBoundbox()
        else:
            return super(MosisCMOSMask, self).getLayer(layer)
    def getLabels(self, layer):
        if layer=='BBOX':
            return []
        else:
            return super(MosisCMOSMask, self).getLabels(layer)
    # }}}
# }}}
# {{{ CMOSParams
class CMOSParams(ParameterSet):
    '''Parameters for Generic Deep Submicron CMOS Process'''
    def __init__(self):
        super(CMOSParams, self).__init__()
        self.params = [
        ('lmd',         0.005,       'Design rule length unit lambda (um)')    # layer thickness
        ('Tsub',        0.02,        'Thickness of the substrate region (um)'),
        ('TSTI',        0.005,       'Depth of the STI trench (um)'),
        ('TBOX',        0.02,        'Thickness of the BOX region (um)'),
        ('Tox',         0.001,        'Thickness of the gate oxide'),
        ('Tpoly',       0.005,       'Thickness of the poly-silicon gate'),
        ('TILD',        0.06,        'Thickness of the ILD dielectric (um) '),
```

```
    ('TM1',         0.035,      'Thickness of Metal 1 (um)'),  # offset length
    ('off_spc',     0.002,      'offset for deep S/D implant, measured from poly edge (um)'),
    ('off_pkt',     0.0,        'offset for pocket implant, measured from poly edge (um)'),
    ('off_ply_cnt', 0.00,       'offset of poly contact holes (um)'),
    ('off_act_cnt', 0.00,       'offset of active contact holes (um)'),   # sub doping
    ('Nsub',        1e15,       'Doping concentration in p substrate (cm^-3)'),  # well doping
    ('Nwel_n',      1e15,       'Well doping concentration (acceptor) for nMOS (cm^-3)'),
    ('Rmax_wel_n',  0.00,       'Rmax of well doping for nMOS (um)'),
    ('Rmin_wel_n',  0.00,       'Rmin of well doping for nMOS (um)'),
    ('Ll_wel_n',    0.0001,     'Lateral characteristic length of well doping for nMOS (um)'),
#active thickness
    ('Lr_wel_n',    0.0001,     'Vertical characteristic length of well doping for nMOS (um)'),
    ('Nwel_p',      1e15,       'Well doping concentration (donor) for pMOS (cm^-3)'),
    ('Rmax_wel_p',  0.00,       'Rmax of well doping for pMOS (um)'),
    ('Rmin_wel_p',  0.00,       'Rmin of well doping for pMOS (um)'),
    ('Ll_wel_p',    0.0001,     'Lateral characteristic length of well doping for pMOS (um)'),
    ('Lr_wel_p',    0.0001,     'Vertical characteristic length of well doping for pMOS (um)'),
       # channel doping
    ('Nchn_n',      1e15,       'Channel doping concentration (acceptor) for nMOS (cm^-3)'),
    ('Rmax_chn_n',  0.00,       'Rmax of channel doping for nMOS (um)'),
    ('Rmin_chn_n',  0.00,       'Rmin of channel doping for nMOS (um)'),
    ('Ll_chn_n', 0.0001,        'Lateral characteristic length of channel doping for nMOS
(um)'),
    ('Lr_chn_n',    0.0001,     'Vertical characteristic length of channel doping for nMOS
(um)'),
    ('Nchn_p',      1e15,       'Channel doping concentration (donor) for pMOS (cm^-3)'),
    ('Rmax_chn_p',  0.00,       'Rmax of channel doping for pMOS (um)'),
    ('Rmin_chn_p',  0.00,       'Rmin of channel doping for pMOS (um)'),
    ('Ll_chn_p', 0.0001,      'Lateral characteristic length of channel doping for pMOS (um)'),
    ('Lr_chn_p', 0.0001,      'Vertical characteristic length of channel doping for pMOS (um)'),
```

```
    # pocket doping
    ('theta_pkt',   45,          'Tilt angle for pkt doping'),
    ('Npkt_n',      2.0e18,      'Pocket doping concentration (acceptor) for nMOS (cm^-3)'),
    ('Rmax_pkt_n',  0.0064,    'Rmax of pocket doping for nMOS (um)'),
    ('Rmin_pkt_n',  0.0064,    'Rmin of pocket doping for nMOS (um)'),
   ('Ll_pkt_n',    0.0001,     'Lateral characteristic length of pocket doping for nMOS (um)'),
   ('Lr_pkt_n',    0.005,      'Vertical characteristic length of pocket doping for nMOS (um)'),
    ('Npkt_p',      2.0e18,      'Pocket doping concentration (donor) for pMOS (cm^-3)'),
    ('Rmax_pkt_p',  0.0064,  'Rmax of pocket doping for pMOS (um)'),
    ('Rmin_pkt_p',  0.0064,   'Rmin of pocket doping for pMOS (um)'),
    ('Ll_pkt_p',    0.0001,     'Lateral characteristic length of pocket doping for pMOS (um)'),
    ('Lr_pkt_p',    0.005,      'Vertical characteristic length of pocket doping for pMOS (um)'),
    # S/D extension doping
    ('Nsde_n',      1e18,       'S/D extension doping concentration (donor) for nMOS (cm^-3)'),
    ('Rmax_sde_n',  0.005,   'Rmax of S/D extension doping for nMOS (um)'),
    ('Rmin_sde_n',  0.00,     'Rmin of S/D extension doping for nMOS (um)'),
    ('Ll_sde_n',    0.0001,    'Lateral characteristic length of S/D extension doping for nMOS
(um)'),
    ('Lr_sde_n',    0.0001,    'Vertical characteristic length of S/D extension doping for nMOS
(um)'),
    ('Nsde_p',      1e18,        'S/D extension doping concentration (acceptor) for pMOS (cm^-
3)'),
    ('Rmax_sde_p',  0.005,    'Rmax of S/D extension doping for pMOS (um)'),
    ('Rmin_sde_p',  0.00,     'Rmin of S/D extension doping for pMOS (um)'),
    ('Ll_sde_p',    0.00005,   'Lateral characteristic length of S/D extension doping for pMOS
(um)'),
    ('Lr_sde_p',    0.00005,   'Vertical characteristic length of S/D extension doping for pMOS
(um)'),
    # Deep S/D doping
    ('Nsd_n',       1e20,      'S/D doping concentration (donor) for nMOS (cm^-3)'),
    ('Rmax_sd_n',   0.005,  'Rmax of S/D doping for nMOS (um)'),
```

```
        ('Rmin_sd_n',   0.00,     'Rmin of S/D doping for nMOS (um)'),
        ('Ll_sd_n',     0.00005,  'Lateral characteristic length of S/D doping for nMOS (um)'),
        ('Lr_sd_n',     0.005,    'Vertical characteristic length of S/D doping for nMOS (um)'),
        ('Nsd_p',       1e20,     'S/D doping concentration (acceptor) for pMOS (cm^-3)'),
        ('Rmax_sd_p',   0.005,    'Rmax of S/D doping for pMOS (um)'),
        ('Rmin_sd_p',   0.00,     'Rmin of S/D doping for pMOS (um)'),
        ('Ll_sd_p',     0.00005,   'Lateral characteristic length of S/D doping for pMOS (um)'),
        ('Lr_sd_p',     0.005,    'Vertical characteristic length of S/D doping for pMOS (um)'),

        # Mesh size control
        ('msz_sub',      0.01,          'Mesh size constraint in the substrate region (um)'),
        ('msz_active',   0.005,         'Mesh size constraint in the active region (um)'),
        ('msz_active1',  0.005,         'Mesh size constraint in the active region (um)'),
        ('msz_ext',      0.005,         'Mesh size constraint in the active region (um)'),
        ('msz_chn',      0.001,         'Mesh size constraint in the transistor channel (um)'),
        ('msz_chn1',     0.001,         'Mesh size constraint in the transistor channel (um)'),
        ('msz_ox',       0.01,          'Mesh size constraint in the oxide region (um)'),
        ('msz_ox1',      0.01,          'Mesh size constraint in the oxide region (um)'),
    ]
# }}}
# {{{ CMOSProcess
class CMOSProcess(ProcessBase):
    '''Generic Deep Submicron CMOS Process'''
    Params = CMOSParams
    # {{{ __init__()
    def __init__(self, params):
        super(CMOSProcess, self).__init__(params)
        self.IOPadList = None  # default=None. We build every IO pad in this case
```

```
        Tsub, TSTI, TBOX, Tox, Tpoly, TILD, TM1, lmd =
self.params.getParams(['Tsub','TSTI', 'TBOX', 'Tox', 'Tpoly', 'TILD', 'TM1', 'lmd'])
            self.z0        = 0.0
            self.zSTI      = self.z0 -  TSTI
            self.zox1      = self.zSTI - Tox
            self.zSilic1   = self.zox1 - 4*Tox
            self.zpoly1    = self.zox1 - Tpoly

            self.zox2      = self.zpoly1 - Tox
            self.zSTI1     = self.zox2 -  TSTI
            self.zox3      = self.zSTI1 - Tox
            self.zpoly2    = self.zox3 - Tpoly
            self.zbox      = self.zpoly2 -  TBOX
            self.zbottom = self.zbox - Tsub
            self.zox       = self.z0 + Tox
            self.zSilic    = self.zox + Tox
            self.zpoly     = self.zox + Tpoly
            self.zM1b      = self.z0 + Tox + Tpoly + TILD
            self.zM1t      = self.z0 + Tox + Tpoly + TILD + TM1
          self.zmax      = self.zM1t + 2*lmd  # top of oxide
          self.zpad      = self.zmax + 0*lmd  # top of pad
        self.materials = {
                        'npoly':          'NPoly',
                        'ppoly':          'PPoly',
                        'active_contact':  'Al',
                        'poly_contact':    'Al',
                        'metal1':          'Al',
                                'via2':           'TiSi2',
                       }
```

```
# }}}

# {{{ buildSubstrate()
def buildSubstrate(self):
    if self.refine:
        msz_sub = self.params.getParams('msz_sub')
    else: msz_sub = 1e3
    g = self.mask.getBoundbox()
    obj = Extrusion(g, self.zbottom, self.zbox)
    self.device.add_object(obj, "sub", "Si", "", "sub", msz_sub)  # bottom surface with label
# }}}

def buildBuriedOxide(self):
    if self.refine:
        msz_ox = self.params.getParams('msz_ox')
    else: msz_ox = 1e3
    obj = Extrusion(self.mask.getBoundbox(), self.zbox, self.zpoly2)
    self.device.set_fill_object(obj, "BOX", "SiO2", msz_ox)

 # {{{ buildActive()
def buildActive(self):

    msz_active, msz_chn = self.params.getParams(['msz_active', 'msz_chn']
    g_active = self.mask.getLayer('ACTIVE')
        g_metal2 = self.mask.getLayer('VIA4')
        g_metal3 = self.mask.getLayer('METAL3')
        g_active1 = Polygon.subtract(g_active, g_metal3)
        g_active_nonmetal2 = Polygon.subtract(g_active1, g_metal2)
        g_active_metal2 = Polygon.intersect(g_active, g_metal2)
```

```
    obj = Extrusion(g_active_metal2, self.zSTI, self.z0)
        self.device.add_object(obj, "active_channel", "Si", "", "", msz_chn)
    pad = Extrusion(g_active_nonmetal2, self.zSTI, self.z0)
    self.device.add_object(pad, "active_pad", "Si", "", "", msz_active)
# }}}
 # {{{ buildActive1()
def buildActive1(self)
    msz_active1, msz_chn1 = self.params.getParams(['msz_active1', 'msz_chn1']
        g_active  = self.mask.getLayer('ACTIVE')
        g_metal2 = self.mask.getLayer('VIA4')
        g_active_nonmetal2 = Polygon.subtract(g_active, g_metal2)
        g_active_metal2 = Polygon.intersect(g_active, g_metal2)
        obj1 = Extrusion(g_active_metal2, self.zSTI1, self.zox2)
        self.device.add_object(obj1, "active_channel1", "Si", "", "", msz_chn1)
       pad1 = Extrusion(g_active_nonmetal2, self.zSTI1, self.zox2)
      self.device.add_object(pad1, "active_pad1", "Si", "", "", msz_active1)
# }}}
def getIOPadList(self):
    return self.padList


   def setIOPadList(self, padList):
    self.IOPadList = padList
   # {{{ buildPoly()
   def buildPoly(self):
    lmd = self.params.getParams('lmd')
    if self.refine: msz=lmd
    else:           msz=1e3
    g_contact = self.mask.getLayer('CONTACT')
```

```
    g_poly   = self.mask.getLayer('POLY')
    g_p_plus = self.mask.getLayer('P_PLUS_SELECT')
    g_p_poly = Polygon.intersect(g_poly, g_p_plus)
    g_n_poly = Polygon.subtract(g_poly, g_p_plus)
    g_p_poly11 = Polygon.subtract(g_p_poly, g_contact)
    g_n_poly11 = Polygon.subtract(g_n_poly, g_contact)
    npoly = Extrusion(g_n_poly11, self.zox, self.zpoly)
    self.device.add_object(npoly, 'npoly', self.materials['npoly'],  '', '', msz)
    ppoly = Extrusion(g_p_poly11, self.zox, self.zpoly)
    self.device.add_object(ppoly, 'ppoly', self.materials['ppoly'],  '', '', msz)
# }}}
  # {{{ buildPoly1()
def buildPoly1(self):
    lmd = self.params.getParams('lmd')
    if self.refine: msz=lmd
    else:           msz=1e3
    g_contact = self.mask.getLayer('CONTACT')
    g_poly   = self.mask.getLayer('POLY')
    g_p_plus = self.mask.getLayer('P_PLUS_SELECT')
    g_p_poly = Polygon.intersect(g_poly, g_p_plus)
    g_n_poly = Polygon.subtract(g_poly, g_p_plus)
    g_p_poly11 = Polygon.subtract(g_p_poly, g_contact)
    g_n_poly11 = Polygon.subtract(g_n_poly, g_contact)

    npoly1 = Extrusion(g_n_poly11, self.zpoly1, self.zox1)
    self.device.add_object(npoly1, 'npoly1', self.materials['npoly'],  '', '', msz)
    ppoly1 = Extrusion(g_p_poly11, self.zpoly1, self.zox1)
    self.device.add_object(ppoly1, 'ppoly1', self.materials['ppoly'],  '', '', msz)
# }}}
```

```
 # {{{ buildPoly2()
 def buildPoly2(self):
    lmd = self.params.getParams('lmd')
    if self.refine: msz=lmd
    else:           msz=1e3
    g_poly1   = self.mask.getLayer('POLY')
    g_p_plus = self.mask.getLayer('P_PLUS_SELECT')
    g_p_poly2 = Polygon.intersect(g_poly1, g_p_plus)
    g_n_poly2 = Polygon.subtract(g_poly1, g_p_plus)
    npoly2 = Extrusion(g_n_poly2, self.zpoly2, self.zox3)
    self.device.add_object(npoly2, 'npoly2', self.materials['npoly'],  '', '', msz)
    ppoly2 = Extrusion(g_p_poly2, self.zpoly2, self.zox3)
    self.device.add_object(ppoly2, 'ppoly2', self.materials['ppoly'],  '', '', msz)
 # }}}
# {{{ buildsilicide()
 def buildsilicide(self):
    lmd = self.params.getParams('lmd')
    if self.refine: msz=lmd
    else:           msz=1e3
    g_via2   = self.mask.getLayer('VIA2')
    g_metal4 = self.mask.getLayer('METAL4')

    g_sil = Polygon.subtract(g_via2, g_metal4)
    obj10 = Extrusion(g_sil, self.z0, self.zSilic)
    self.device.add_object(obj10, "silicide", self.materials['via2'],  '', '', msz)
 # }}}
# {{{ buildsilicide1()
 def buildsilicide1(self):
    lmd = self.params.getParams('lmd')
```

```
        if self.refine: msz=lmd
        else:           msz=1e3
        g_via2   = self.mask.getLayer('VIA2')
        g_metal4 = self.mask.getLayer('METAL4')
        g_sil1 = Polygon.subtract(g_via2, g_metal4)
        obj101 = Extrusion(g_sil1, self.zox2, self.zSilic1)
        self.device.add_object(obj101, "silicide1", self.materials['via2'],  '', '', msz)
    # }}}
# {{{ buildContact()
    def buildContact(self):
        lmd = self.params.getParams('lmd')
        if self.refine: msz=lmd
        else:           msz=1e3
        g_poly    = self.mask.getLayer('POLY')
        g_contact = self.mask.getLayer('CONTACT')
        g_poly_contact   = Polygon.intersect(g_contact, g_poly)
        g_active_contact = Polygon.subtract(g_contact, g_poly)


        active_contact = Extrusion(g_active_contact, self.zox2, self.zM1b)
        self.device.add_object(active_contact, 'active_contact',
                               self.materials['active_contact'],  '', '', msz)
        poly_contact = Extrusion(g_poly_contact, self.zox3, self.zM1b )
        self.device.add_object(poly_contact, 'poly_contact',
                               self.materials['poly_contact'],  '', '', msz)
    # }}}
    # {{{ buildMetal1()
    def buildMetal1(self):
        lmd = self.params.getParams('lmd')
```

```
    if self.refine: msz=1.5*lmd
    else:           msz=1e3
    obj = Extrusion(self.mask.getLayer('METAL1'), self.zM1b, self.zM1t)
    self.device.add_object(obj,     'metal',
                           self.materials["metal1"],  '', '', msz)
# }}}
def buildGateOxide(self):
    if self.refine:
        msz_ox1 = self.params.getParams('msz_ox')
    else: msz_ox1 = 1e3
    g_poly2   = self.mask.getLayer('POLY')
    g_metal2 = self.mask.getLayer('METAL2')
    g_ox = Polygon.intersect(g_metal2, g_poly2)
    obj4 = Extrusion(g_ox, self.z0, self.zox)
    self.device.add_object(obj4, "gox", "SiO2",  '', '', msz_ox1)
def buildGateOxide1(self):
    if self.refine:
        msz_ox1 = self.params.getParams('msz_ox')
    else: msz_ox1 = 1e3
    g_poly2   = self.mask.getLayer('POLY')
    g_metal2 = self.mask.getLayer('METAL2')
    g_ox1 = Polygon.intersect(g_metal2, g_poly2)
    obj5 = Extrusion(g_ox1, self.zox1, self.zSTI)
    self.device.add_object(obj5, "gox1", "SiO2",  '', '', msz_ox1)
def buildGateOxide2(self):
    if self.refine:
        msz_ox1 = self.params.getParams('msz_ox')
    else: msz_ox1 = 1e3
    g_poly2   = self.mask.getLayer('POLY')
```

```
    g_metal2 = self.mask.getLayer('METAL2')
    g_ox2 = Polygon.intersect(g_metal2, g_poly2)
    obj6 = Extrusion(g_ox2, self.zox2, self.zpoly1)
    self.device.add_object(obj6, "gox2", "SiO2",  '', '', msz_ox1)
def buildGateOxide3(self):
    if self.refine:
       msz_ox1 = self.params.getParams('msz_ox')
    else: msz_ox1 = 1e3
    g_poly2   = self.mask.getLayer('POLY')
    g_metal2 = self.mask.getLayer('METAL2')
    g_ox3 = Polygon.intersect(g_metal2, g_poly2)
    obj7 = Extrusion(g_ox3, self.zox3, self.zSTI1)
    self.device.add_object(obj7, "gox3", "SiO2",  '', '', msz_ox1)
def buildFillOxide(self):
    if self.refine:
       msz_ox = self.params.getParams('msz_ox')
    else: msz_ox = 1e3
    obj = Extrusion(self.mask.getBoundbox(), self.zpoly2, self.zmax)
    self.device.set_fill_object(obj, "ox", "SiO2", msz_ox)
# {{{ buildPowerPad()
def buildPowerPad(self):
    lmd = self.params.getParams('lmd')
    if self.refine: msz=lmd
    else:           msz=1e3
    g_vdd = self.mask.getPad('METAL1', 'vdd')
    g_vss = self.mask.getPad('METAL1', 'vss')
    if g_vdd:
      obj = Extrusion(g_vdd, self.zM1t, self.zpad)
      self.device.add_object(obj,     'vdd',    'Al',  'vdd', '', msz)
```

```
    if g_vss:
      obj = Extrusion(g_vss, self.zM1t, self.zpad)
      self.device.add_object(obj,     'vss',    'Al',  'vss', '', msz)
# }}}
# {{{ getIOPadList()
def getIOPadList(self):
    if self.IOPadList==None:
        return self.mask.getLabels('ROUTE_PORT')
    else:
      return self.IOPadList
# }}}
# {{{ buildIOPad()
def buildIOPad(self):
    padList = list(set(self.getIOPadList())) ## remove duplicates
    lmd = self.params.getParams('lmd')
    if self.refine: msz=lmd
    else:           msz=1e3
    for pad in padList:
        g = self.mask.getPad('ROUTE_PORT', pad)
        if g==None:
          print 'IO pad "%s" not found' % pad
          raise ValueError
        obj = Extrusion(g, self.zM1t, self.zpad)
        self.device.add_object(obj,  pad, 'Al', pad, '', msz)
# }}}
# {{{ placeWaferDoping()
def placeWaferDoping(self):
    Nsub = self.params.getParams('Nsub')
    # substrate doping
```

```
        g_sub = Polygon.offsetted(self.mask.getBoundbox(), 0.1)
        if Nsub>0:
            s = "Acceptor"
        else:
            Nsub *= -1
            s = "Donor"
        self.device.add_profile(PlanarUniformProfile(g_sub, self.zbottom, self.z0, s, Nsub))
    # }}}
    # }}}
    # {{{ placeSDDoping()
    def placeSDDoping(self):
        off_spc = self.params.getParams('off_spc')
        g_n_plus  = self.mask.getLayer('N_PLUS_SELECT')
        g_p_plus  = self.mask.getLayer('P_PLUS_SELECT')
        g_metal2  = self.mask.getLayer('METAL2')
        g_off_spc = Polygon.offsetted(g_metal2, off_spc)
        g_sde_n = Polygon.subtract(g_n_plus, g_metal2)
        g_sde_p = Polygon.subtract(g_p_plus, g_metal2)
        g_sd_n  = Polygon.subtract(g_n_plus, g_off_spc)
        g_sd_p  = Polygon.subtract(g_p_plus, g_off_spc)
        # deep s/d
        N_n, Rmax_n, Rmin_n, Ll_n, Lr_n,Nsd_n,Nsd_p = self.params.getParams(['Nsd_n',
'Rmax_sd_n', 'Rmin_sd_n', 'Ll_sd_n', 'Lr_sd_n','Nsd_n','Nsd_p'])
        #self.device.add_profile(PlanarAnalyticProfile(g_sd_n, self.z0, Rmin_n, Rmax_n,
"Donor", N_n, Lr_n, Ll_n, PlanarAnalyticProfile.GAUSSIAN))
            self.device.add_profile(PlanarUniformProfile(g_sd_n,
self.zSTI,self.z0,"Donor",Nsd_n)
        N_p, Rmax_p, Rmin_p, Ll_p, Lr_p = self.params.getParams(['Nsd_p', 'Rmax_sd_p',
'Rmin_sd_p', 'Ll_sd_p', 'Lr_sd_p'])
        #self.device.add_profile(PlanarAnalyticProfile(g_sd_p, self.z0, Rmin_p, Rmax_p,
"Acceptor", N_p, Lr_p, Ll_p, PlanarAnalyticProfile.GAUSSIAN))
```

```
            self.device.add_profile(PlanarUniformProfile(g_sd_p,
self.zSTI,self.z0,"Acceptor",Nsd_p))


        N_n, Rmax_n, Rmin_n, Ll_n, Lr_n,Nsd_n,Nsd_p = self.params.getParams(['Nsd_n',
'Rmax_sd_n', 'Rmin_sd_n', 'Ll_sd_n', 'Lr_sd_n','Nsd_n','Nsd_p'])

        #self.device.add_profile(PlanarAnalyticProfile(g_sd_n, self.zox2, Rmin_n, Rmax_n,
"Donor", N_n, Lr_n, Ll_n, PlanarAnalyticProfile.GAUSSIAN))

            self.device.add_profile(PlanarUniformProfile(g_sd_n,
self.zSTI1,self.zpoly1,"Donor",Nsd_n))

        N_p, Rmax_p, Rmin_p, Ll_p, Lr_p = self.params.getParams(['Nsd_p', 'Rmax_sd_p',
'Rmin_sd_p', 'Ll_sd_p', 'Lr_sd_p'])

        #self.device.add_profile(PlanarAnalyticProfile(g_sd_p, self.zox2, Rmin_p, Rmax_p,
"Acceptor", N_p, Lr_p, Ll_p, PlanarAnalyticProfile.GAUSSIAN))

            self.device.add_profile(PlanarUniformProfile(g_sd_p,
self.zSTI1,self.zpoly1,"Acceptor",Nsd_p))

    # }}}

    def meshSizeControl(self):

        pass

    # {{{ buildDevice()

    def buildDevice(self):

        if self.mask==None:

            raise ValueError

        self.buildSubstrate()

        self.buildActive()

        self.buildActive1()

        self.buildGateOxide()

        self.buildGateOxide1()

        self.buildGateOxide2()

        self.buildGateOxide3()

        self.buildPoly()

        self.buildPoly1()

        self.buildPoly2()
```

```
    self.buildsilicide()
    self.buildsilicide1()
    self.buildContact()
    self.buildMetal1()
    self.buildPowerPad()
    self.buildIOPad()
    self.buildFillOxide()
    self.buildBuriedOxide()
    self.placeWaferDoping()
    self.placeSDDoping()
    self.device.finalize()
    if self.refine:
    self.meshSizeControl()
# {{{ buildCAD()
def buildCAD(self):
    if self.mask==None:
       raise ValueError
    self.buildSubstrate()
    self.buildActive()
    self.buildActive1()
    self.buildGateOxide()
    self.buildGateOxide1()
    self.buildGateOxide2()
    self.buildGateOxide3()
    self.buildPoly()
    self.buildPoly1()
    self.buildPoly2()
    self.buildsilicide()
    self.buildsilicide1()
```

```
        self.buildContact()
        self.buildMetal1()
        self.buildPowerPad()
        self.buildIOPad()
        self.buildFillOxide()
        self.buildBuriedOxide()
        self.device.finalize()
    # }}}
# }}}
```