Design and Analysis of Dual Material Gate Junctionless FinFET for Analog IC Applications

Submitted in partial fulfilment of the requirements

for the award of the degree of

Doctor of Philosophy

by

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APPROVAL SHEET

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Dedicated

To

My Family,

Teachers & Friends

Declaration

This is to certify that the work presented in the thesis entitled **Design And Analysis Of Dual Material Gate Junctionless FinFET For Analog IC Applications** is a bonafide work done by me under the supervision of **Prof. T.V.K Hanumantha Rao**, Professor, Department of Electronics and Communication Engineering, National Institute of Technology Warangal, India and was not submitted elsewhere for the award of any degree.

I declare that this written submission represents my ideas in my own words and where others' ideas or words have been included, I have adequately cited and referenced the original sources. I also declare that I have adhered to all principles of academic honesty and integrity and have not misrepresented or fabricated or falsified any idea / data / fact / source in my submission. I understand that any violation of the above will be a cause for disciplinary action by the Institute and can also evoke penal action from the sources which have thus not been properly cited or from whom proper permission has not been taken when needed

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CERTIFICATE

This is to certify that the thesis work entitled **Design And Analysis Of Dual Material Gate Junctionless FinFET For Analog IC Applications** is a bonafide record of work carried out by **Rambabu Kusuma** submitted to the faculty of **Electronics & Communication Engineering** department, in partial fulfilment of the requirements for the award of the degree of **Doctor of Philosophy** in **Electronics and Communication Engineering, National Institute of Technology Warangal, India-506004**. The contributions embodied in this thesis have not been submitted to any other university or institute for the award of any degree.

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Rambabu Kusuma

Abstract

The era of Internet of Things (IoT) and Big data are the major driving forces to develop intelleigent systems. Specifically, these systems are designed by Complementary Metal Oxide Semiconductor (CMOS) technology with proper scaling of the device ratios. Eventhough, the CMOS scaling trend has reached its atomistic limit the short channel effects and fabrication difficulty have worsened the MOS devices' aggressive scaling. Junctionless (JL) technology has been suggested as one of the likely methods to get around this scaling barrier. Homogeneous doping concentration is used in all three regions by JL-based FETs. This idea not only makes manufacturing simpler and less expensive, but it also exhibits better short channel behaviour than typical junction-based devices. Due to their promising attributes, JL based FinFETs are chosen for this research work.

However, due to the high electric field in the nano-scaled device, the electrical characteristics deteriorate due to the short channel effects (SCEs). Moreover, channel potential, position of minimum threshold voltage, and subthreshold characteristics of the FinFET are altered because of SCEs. To reduce this SCEs problem, the gate material engineering, such as dual metal gate structure are incorporated into the FinFET. To further reduce SCEs, the gate stack engineering is employed into the dual material gate JL FinFET.

The main objective of the thesis is to design and simulation analysis of the dual material gate junctionless FinFET (DMG JLFinFET). In this thesis, the DC performance parameters of DMG JLFinFET i.e. Ion, Ioff, Ion/Ioff ratio, subthreshold swing (SS) and drain induced barrier lowering(DIBL) is presented. Besides, the analog/RF figures of merit of the proposed DMG JLFinFET, including the transconductance, transconductance generation factor, The Cut-off frequency, Intrinsic delay , Transconductance frequency product , Gain bandwidth product are evaluated for different values of device parameters. Also, the linearity performance metrics such as second order transconductance coefficient (g_{m2}), third order transconductance coefficient (g_{m3}), second and third-

order voltage intercept points VIP2, VIP3, third-order power intercept point (IIP3), and 1-dB compression point of the proposed DMG JLFinFET are evaluated for different values of device parameters. Furthermore, temperature variability analysis of DMG JLFinFET analyzed. It is investigated that the proposed DMG JLFinFET has better performance than SMG JLFinFET. The proposed device verified against numerical results obtained from TCAD simulations obtained from Visual TCAD, which is a device simulator from Cogenda.

Contents

List of Figures

List of Tables

List of Abbreviations

2D	Two Dimensional
BJT	Bipolar Junction Transistor
CMOS	Complementary Metal Oxide Semiconductor
DIBL	Drain-Induced Barrier-Lowering
DMG	Dual-Material-Gate
FD	Fully-Depleted
FOM	Figure Of Merit
Ge	Germanium
HCEs	Hot-Carrier Effects
IC	Integrated Circuit
ITRS	International Technology Roadmap for Semiconductors
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MuGFETs	Multi-Gate Field Effect Transistors
PD	Partially Depleted
QMEs	Quantum Mechanical Effects
RF	Radio Frequency
SCEs	Short-Channel Effects
Si	Silicon
SOI	Silicon-On-Insulator
SoC	System On-Chip
VLSI	Very Large Scale Integration
ULSI	Ultra-Large Scale Integration
UTB	Ultra-Thin Body

Chapter 1

Introduction

FinFET (Fin Field-Effect Transistor) is a type of transistor technology that has become popular in recent years for use in integrated circuits. It is a three-dimensional transistor architecture that is designed to provide improved performance, power efficiency, and transistor density over traditional planar transistors. In a FinFET, the gate of the transistor wraps around a vertical silicon "fin," which protrudes from the surface of the silicon wafer. This three-dimensional design allows the gate to control the flow of current on three sides of the fin, providing improved performance and control over the flow of electrons. FinFETs are commonly used in modern microprocessors, memory chips, and other high-performance digital circuits. They are also used in radio-frequency (RF) and analog circuits, where their low power consumption and high switching speeds make them an attractive option. Overall, FinFET technology has played a crucial role in enabling the continued progress of Moore's Law, which states that the number of transistors on a chip will double every two years, by allowing for the creation of smaller and more efficient transistors.

1.1 Evolution of Transistors

The transistor is a significant invention that fundamentally altered the development of computers. Vacuum tubes were employed in the first generation of computers; transistors in the second generation; integrated circuits in the third generation; and microprocessors in the fourth generation. In an effort to replace vacuum tubes as mechanical relays

in telecommunications, scientists John Bardeen, William Shockley, and Walter Brattain at the Bell Telephone Laboratories in Murray Hill, New Jersey, studied the behaviour of crystals (germanium) as semiconductors. The vacuum tube, which was used to amplify music and voice and enabled long-distance calling, consumed electricity, produced heat, and burned out quickly, necessitating heavy maintenance. When a final attempt to use a purer substance as a contact point resulted in the creation of the "point-contact" transistor amplifier, the team's research was about to come to a fruitless end. The group won the Nobel Prize in Physics in 1956 for inventing the transistor.

A semiconductor material, such as silicon and germanium, that has the ability to conduct electricity and act as insulation, is used to make transistors. Electronic current is modulated and switched by transistors. Digital circuits previously used vacuum tubes before transistors. Discover all the drawbacks of vacuum tubes in computers by reading the tale of the ENIAC(Electronic Numerical Integrator And Computer). The transistor was the first gadget made to function as both a resistor and a transmitter, transforming sound waves into electronic waves and managing electronic current respectively. Transistor is used as transmitter and also used to transfer the resistance. For their transistor, John Bardeen and Walter Brattain filed a patent. The transistor effect and a transistor amplifier were both the subject of William Shockley's patent application. The computer architecture had a significant effect by the revolution of transistors. Semiconductor-based transistors replaced tubes leading to improved computer design. Same task could be done by transistors, which use less power and space than large and unstable vacuum tubes.

The first functional silicon insulated-gate field effect transistor, or MOSFET as it is called today, was created by Atalla and Kahng in 1960, which had been long expected by Lilienfeld [1]. The device's three main layers - silicon semiconductor as the base material, thermally generated native oxide as an insulator, and the metallic gate electrode serving as the controlling terminal - are stacked one on top of the other to form the overall structure. Because they discovered that silicon's oxidation process is more comfortable than germanium's, they used silicon crystals. Since that time, silicon has dominated the semiconductor industry [2]. By utilizing the Schottky theory, which clarified the rectification between the semiconductor and metal junction [3], Mead proposed the construction of the metal-semiconductor field effect transistor (MESFET) in 1966. Finally, employing

an n-type gallium arsenide (GaAs) epitaxial layer on a semi-insulating GaAs substrate, Hooper and Lehrer created the first MESFET prototype [4]. The historical development of electronic devices from the invention of vacuum tubes to the start of the nanoscale period is summarized in Figure 1.1 [6].

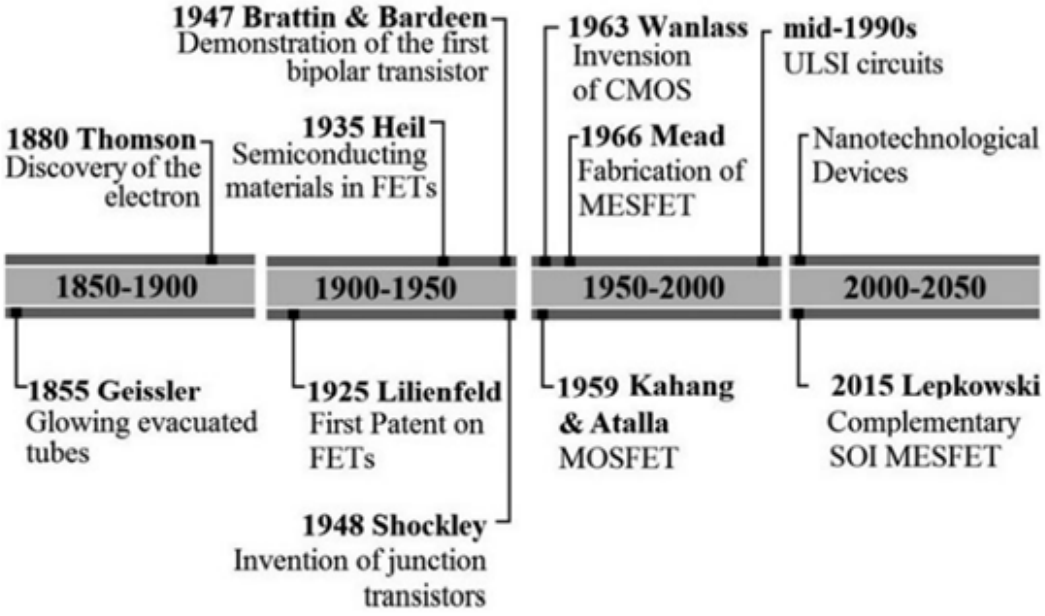


Figure 1.1 Historical growth of the electronic devices [6]

1.1.1 Integrated Circuits (ICs)

Jack Kilby proposed in 1958 that transistors and other electronic components may be produced simultaneously on a single semiconductor chip as opposed to separately. This concept made it possible to build electronic components using the same method and supplies. In this method, the p-n junction and bulk semiconductor could both be used to make capacitors and resistors. Kilby was able to construct a flipflop using two transistors and a germanium wafer. Integrated circuits were created in this way [5]. Inventing integrated circuits six months after Kilby, Robert Noyce overcame a number of Kilby's circuit's real-world challenges, including as the issue of interconnectivity between the chip's components. This improved the integrated circuits' ability to be produced in large quantities.

The number of IC components has increased to hundreds of millions as a result of

Wanlass and Sah's invention of Complementary Metal Oxide Semiconductor (CMOS). Since then, chips' component counts have started to rise and integrated circuits have progressively grown in complexity. Gordon Moore made a forecast about the development of integrated circuits in 1965 that became known as Moore's law. According to Moore's law, an integrated chip would have twice as many transistors per square inch every two years. According to Moore's law, the transistor geometry must be reduced every 18 to 24 months. Strong process technology and significant investment in semiconductor foundry R&D are needed for this. VLSI technology has mostly followed Moore's law during the past 50 years as a result of the quick advancements in photolithography techniques, tools, pattern transfer procedures, and equipment.

Over the past few decades, increased complexity, faster production, and lower cost of integrated circuits have been pursued to satisfy the never-ending demand for improved device performance. The smallest feature size in an IC surpassed the submicron dimension in the early 1980s, and Intel debuted its microprocessor that featured transistors manufactured using 14nm technology in 2015. Today's microprocessors have about a billion transistors, while a 256 GB Secure Digital (SD) memory card, which weighs less than a gram has 10^{12} transistors, assuming each transistor can store two bits [6].

1.2 MOSFET Scaling

The electronic industry has been extremely benefiting from scaling down the dimensions of MOSFET for the last four decades. The shrinking of MOSFETs to sub-nano meter scale enables integration of the billions of the components on a small substrate area. Initially, the constant electric field scaling theory was introduced in 1974 [7]. In this theory, the scaling was done to the dimensions and voltage of the device with same scaling factor S while keeping electric field constant. Hence, the speed of device increases by a factor S and the power dissipation of the device decreases by a factor of S^2 The other major scaling is constant voltage scaling. In this theory, the operating voltage of the device is unchanged and scaling is applied to all other parameters of the device.

In 2015, International Technology Roadmap for Semiconductors (ITRS) presented that the scaling of the MOSFET more than Moore beyond CMOS technology node could

be a challenging task, since the planar MOSFET has already reached its scaling limited [8]. Moreover, more Moore beyond CMOS is further continuing the scaling of MOSFETs leads to high hot carrier effects (HCEs) and short channel effects (SCEs) such as subthreshold swing, drain induced barrier lowering (DIBL), threshold voltage roll-off, and interface charges[9].

1.2.1 Scaling challenges

Modern devices and circuits have emerged in recent years as a result of advancements in semiconductor materials and device architecture. A lot of these become workhorses in the mainstream, albeit just a few are still in their infancy. According to the International Technology Roadmap for Semiconductors (ITRS) trends, transistor gates currently measure 14–10 nm [10-11] and are expected to get smaller to 7 nm in the upcoming years. Beyond the 20 nm technological node, the semiconductor industry faces a number of issues that need to be resolved. Reduced transistor size lead to faster switching, lower power dissipation, lower fabrication costs, and an increase in package density.

1.2.2 Drain-Induced Barrier Lowering (DIBL)

The source and drain regions of a transistor get closer to one another as it is downscaled. As a result, the potential barrier between the source and channel region is lowered, and the drain voltage begins to dominate the electrostatic potential of the channel. As a result, it raises the sub-threshold leakages, which raise the transistor's static power requirement. This result restricts transistor scaling [12].

1.2.3 Punch through

A sudden increase in device current due to avalanche multiplication occurs when two depletion zones spanning the source-channel junction and drain-channel junction touch and cause the punch through effect leading to permanent damage of the device.

1.2.4 Carrier mobility degradation

Carrier mobility is one of the most crucial elements that affects the device's present performance. Mobility is described in the definition as the relationship between drift velocity and electric field. As a result, for short channel devices, the drift velocity and ON-current performance are eventually saturated by the lateral field across the channel. Scaling causes a rise in the normal electric field, which worsens carrier mobility due to increased impurity scattering in the channel region [12-13]. To counteract current leakage, which worsens the scattering phenomena, the channel doping is enhanced for scaled devices [14].

1.2.5 Threshold voltage roll-off

The electrostatic potential profile of the channel in highly scaled MOSFET designs depends on the vertical and lateral fields, which are controlled by the gate and drain voltages, respectively. Therefore, as the influence of the drain electric field on the channel increases, the gate voltage necessary for channel inversion decreases. Threshold voltage roll-off, which results in the reduction of threshold voltage, rises with channel length scaling.

1.3 CMOS boosters

As explained in preceding section, a major challenging task in nano-scaled CMOS scaling is eliminating the SCEs and HCEs. To suppress SCEs and HCEs, CMOS boosters are incorporated into the nano-scaled device. They are strained-silicon (s-Si), channel engineering, gate material engineering, high-k dielectric material, non-conventional MOSFET structures, etc. Some of them are illustrated below.

1.3.1 Gate material engineering

Dual-Metal-Gate (DMG) structure, which is one of the notable CMOS technology boosters, was proposed by Long et al.[15]. The gate material of the DMG MOSFET

consists of control gate work function as ϕ_{m1} and screen gate work function as ϕ_{m2}, where $\phi_{m1} > \phi_{m2}$ for n-type device, and vice versa for p-type device. Consequently, the step-equivalent curve is attained in the channel potential. When device operates in the saturation region, the channel region under control gate layer is screened from a drain to source voltage (V_{DS}) as the channel region under screening gate layer absorbs any excess V_{DS}. Therefore, the SCEs and HCEs of the MOSFET are suppressed by employing DMG structure.

1.3.2 Graded channel engineering

If the doping profile in the Silicon channel decreases uniformly in a stepwise manner from the source/channel interface to the drain/channel interface then it is considered as graded channel (GC) structure [16]. By employing GC structure in the MOSFET, high threshold voltages and low SCEs are obtained. Moreover, the HCEs are also reduced due to the lower built-in potential at the drain/channel interface

1.3.3 High-k insulating material

In a process of scaling CMOS devices, the thickness of the dielectric material has reached 10 Angstrom. With the reduction of channel length below 32nm, the gate dielectric thickness has to be scaled down to an ultra-thin size (i.e., less than 1 nm approximately, which is equivalent to five atomic layers). This very thin dielectric layer results in a huge amount of OFF current, thereby increasing the standby power consumption. Therefore, a need of thick dielectric material is required in order to prevent electrons tunnelling through gate oxide[17] i.e the physical thickness of the dielectric material has to be high, whereas its electrical thickness has to be low. Hence, high-k dielectric materials could be one of the best solutions for the issues discussed. The effective oxide thickness of the high-k dielectric material is given as $t_{eff} = t_{high-k}[\epsilon_{SiO2} \ / \ \epsilon_{high-k}]$, where ϵ_{SiO2} and ϵ_{high-k} are permitivities of silicon dioxide material and high-k dielectric layer, respectively and t_{high-k} hickness of high-k dielectric layer.

1.3.4 Non-conventional MOSFETs

The multiple-gate (MuG) MOSFETs are categorized as the double gate (DG) conventional SOI MOSFET, DG non-conventional FinFET, Tri-gate MOSFET, Quadruple Gate MOSFET, surrounding gate MOSFET, and Nanowire MOSFET. The MuG-MOSFET structures can have high gate control over the silicon channel. Consequently, reduction of leakage current and SCEs of the device can be attained. Nevertheless, several process flow issues of MuG-MOSFETs must be resolved before using the MuG-MOSFETs in VLSI systems. Moreover, MuG-MOSFETs require modern fabrication methods such as enhanced etching accuracy, corner effects, reliability, and ultra-thin fin effects, etc.

1.4 Motivation

In nano-scaled regime, MOSFETs suffer from SCEs and HCEs. To suppress SCEs and HCEs, both DMG with GC engineering and gate stack structure are employed in DMG JL FinFET. In the light of above discussion, an effort is done to investigate the subthreshold performance of DMG JL FinFET. Moreover, the effect of various device parameters on the subthreshold characteristics of DMG JL FinFET is investigated .Besides, CMOS technology boosters like DMG with GC engineering and high-k dielectric material help to enhance ON current of DMG JL FinFET. Therefore, these techniques are employed in the DMG JL FinFET to examine their effects on subthreshold behavior of the DMG JL FinFET

1. In nano scale regime CMOS technology is suffering from SCEs like Subthreshold slope, drain induced barrier lowering and facing problem in analog and RF analysis while moving to subthreshold scaling.

2. To avoid these problems dual material gate concept is employed in FinFET to investigate the SCEs effect.

1.5 Problem Statement

The objective is to present a detailed simulation based study of the subthreshold characteristics of dual material gate junctionless FinFET with Gate Oxide, Work Function, and Dimensional Effect, and to analyze Analog RF and Linearity Performance.

1.6 Research Objectives

- Design and Optimization of Dual Material Gate Junctionless FinFET Using Dimensional Effect, Gate Oxide and Work function Engineering at 7 nm Technology Node.
- Study of DMG JL FinFET: Analog/RF Perspective at 7nm Technology Node
- Design and Temperature assessment of Analog/RF and Linearity parameters on Dual Material Gate Junctionless FinFET at 7nm Technology node for nanoscale Applications

1.7 Thesis Organization

The main aim of this thesis is to demonstrate a simulation based analysis of the subthreshold performance of DMG JL FinFET with DC, Anlog and RF performance and temperature variability analysis. The thesis comprises six chapters containing the present Chapter. The contents of other chapters of the thesis are outlined as follows:

Chapter 2 reviews the notable amount of most updated literature of the modeling and simulation of MOSFET and FinFETs with junction and junctionless and DMG JL FinFET in detail.

Chapter 3 deals with the simulation of DMG JL FinFET with dimensional effects and evaluating the performance parameters SS, DIBL, I_{ON}, I_{OFF}, I_{ON}/I_{OFF}.

Chapter 4 presents a detailed analysis of analog/RF performance DMG JL FinFET.

Chapter 5 presents a detailed study of temperature variability analysis DMG JL FinFET with DC, analog/RF and linearity characteristics performance.

Chapter 6 gives conclusions of the work done and provides direction for the upcoming work.

The thesis organization is shown in Figure 1.2

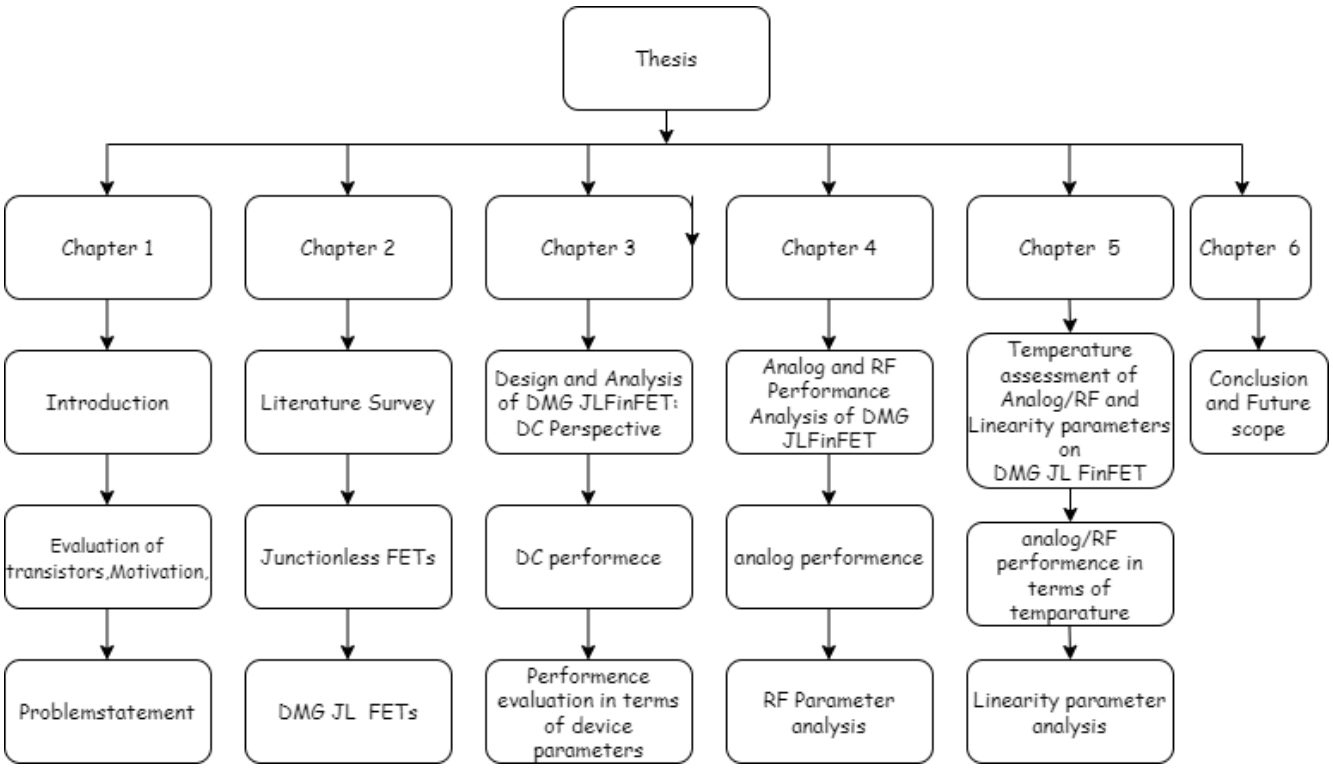


Figure 1.2 Thesis organaization in pictorial representation

Chapter 2

Literature Survey

2.1 Introduction

Very Large Scale Integration (VLSI) technology has advanced significantly over the past two decades, paving the path for a new era in human civilization. Continuous device downscaling has provided great chip density, multi-functionality, and high speed for electronic systems, as anticipated by G. Moore [18]. It is now clear that the usual scaling trend cannot last indefinitely, making it exceedingly difficult for device developers to continue improving device performance and reliability. For deeply scaled devices, generating ultra-sharp junctions proves to be a serious challenge in addition to short channel effects (SCE) degradation, which calls for the development of complex fabrication and process approaches. Recently, "Junctionless (JL) technology" a very efficient and dependable solution has been discovered. This technology is compatible with the CMOS process. This innovative idea eliminates the necessity for the source/drain (S/D) implantation phase during fabrication, relaxing the thermal budget and simplifying the fabrication process.[19–21].

The JL concept is based on a straightforward idea that was patented in 1925 by well-known physicist J. E. Lilienfeld. Numerous research groups' interest in Junctionless FETs (JL FETs) has recently been rekindled. To address current fabrication issues and SCEs, extensive research is currently being done on various JL device architectures. These include bulk junctionless transistors (JLTs)[22], Junctionless nanowire transistors (JNTs) [23], gate all around (GAA) JNTs [24], vertically stacked JNTs [25], JL FinFETs[26], JL

Tunnel FETs [27], JL Vertical slit FET (VesFETs) [28], and more. This chapter provides a thorough overview of the research work done thus far on JL devices by highlighting its potential and problems.

2.2 Junctionless technology beyond CMOS

Despite the fact that several device architectures have been proposed in the literature, many of them remain restricted to the theoretical realm and are not yet ready for mass production due to the complexity and cost of fabrication [14]. A brand-new idea for a Junctionless Field Effect Transistor (JL FET) has been put out in this context of device engineering [29]. J.P. Colinge and his group at Tyndall National Institute in Ireland created and described a tri-gate JL FET in 2010[20]. These special devices use ultra-thin silicon channels with homogenous doping concentration in the source, drain, and channel regions. This significantly lowers the cost of manufacture and streamlines the fabrication process [8]. An overview of the working theory and the benefits and drawbacks are provided in the following subsections.

2.3 Features of Junctionless technology

1. Ease of fabrication: JL FETs' very simplified device architecture is its main benefit [19]. From a manufacturing standpoint, it can be difficult to create a high-quality, ultra-shallow p-n junction at a deep nanoscale level for typical MOSFETs. It calls for a brief transition between n-type doping concentrations of the order of 10^{19} cm^{-3} and p-type doping concentrations of the order of $10^{18}cm^{-3}$ This has a lot of drawbacks, including a large heat budget and pricy annealing methods [21]. JL design does away with the requirement for a S/D diffusion stage during fabrication, which naturally simplifies and lowers the cost of manufacture[26].

2. Design constraint: A high work function gate material (>5.0 eV) and strongly doped ultra-thin silicon sheet (10^{19}–10^{20} cm^{-3}) are needed for the JL device to operate well [19,20,29]. Even if the JL idea made the production process simpler, producing a material with such a high work function is difficult from a fabrication standpoint.

Additionally, it is challenging to maintain the evenly doped ultrathin silicon-on-insulator substrate.

3. Bulk conduction mechanism: JL FETs function in partial depletion mode, which differs from Inversion Mode (IM) MOSFETs in that the conduction channel forms at the bulk of the silicon film, which is separated from the surface by a depletion area. Because of this, JL FETs exhibit completely different performance than IM MOSFETs. JL FETs are less impacted by silicon/oxide interface traps because the bulk area of the device receives the majority of the charge carriers [26]. Ionized impurity scattering, however, unquestionably becomes the predominant mobility degradation mechanism that impacts the ON-current performance of JL FETs because of the high doping concentration needed in JL devices [27]. The vertical electric field at the silicon/oxide interface of the JL devices, which mostly operate in partial depletion mode [25]. Furthermore, the vertical electric field at the silicon/oxide interface is minimal since the JL devices mostly function in partial depletion mode. As a result, they are less vulnerable to BTI (Bias Temperature Instability) and reliability problems [30].

4. Improved short channel and noise behavior: The interaction between source and drain areas is reduced in the absence of depletion regions. As a result, JL FETs have a much enhanced DIBL [20]. In addition, as compared to IM MOSFETs, the bulk conduction mechanism in JL FETs minimizes the electric field at the silicon/oxide and channel/drain interfaces. As a result, the JL FETs are more resistant to the impacts of hot electrons [22]. The JL FETs also outperform MOSFETs in terms of noise performance. When compared to IM MOSFETs, JL FETs have been shown to have reduced 1/f noise and Random Telegraph Noise (RTN) [31–33]. This is brought on by the JL device's bulk channel's low field lines, which noticeably lengthen the average time it takes to catch mobile carriers in traps, close to the gate electrode.

5. Enhanced carrier ballisticity: Without any barrier height, JL FETs offer a seamless transition from the source to the drain area. In JL FETs, the possibility of carrier back scattering is eliminated by the lack of a source to channel barrier height in the ON-state. As a result, JL devices have improved carrier ballisticity when compared to IM devices in the ON-state [34].

2.4 Review of various Junctionless FETs

The Lilienfield's first transistor principle, which was proposed by Lee et al. in 2009 [29], is the foundation of the JL structure idea. Excellent switching ability and superior short channel behaviour have been reported for multi-gate JL FET in comparison to conventional multi-gate FET. Although the results were very encouraging, there was still some uncertainty regarding device variability. Later in 2010, Lee et al. [35] looked at how high temperatures affected the electrical characteristics of multi-gate JL FETs. When compared to multi-gate transistors, operating in accumulation mode (AM) or inversion mode (IM), the effect of JL FETs on threshold voltage (VTH) is shown to be two times greater. In addition, a very little decrease in channel mobility is seen in the JL device. In turn, this causes the constant increase in current drive with temperature. The defect density around the drain-channel junction is also decreased by the lack of S/D implantation, which lowers the total gate-induced drain leakage currents.

The enhanced electrical properties of JL FETs over traditional MOSFETs with gate lengths down to 20 nm have been demonstrated in several research publications that are available in the literature [22,26,36]. In the year 2010 [20], Colinge et al. of Tyndall National Institute carried out the first experimental investigation on 1 nm tri-gate JNT in response to these simulation studies. The reported long channel JL device has demonstrated full CMOS capability, good $I_{ON}/I_{OFF}(>10^6)$, near-ideal sub-threshold swing (SS) at room temperature (64 mV/dec), and extremely low leakage current. Additionally, JL FET has been discovered to have less mobility deterioration with temperature than IM FET. However, it has also been shown that the V_{TH} variability in JL devices is two times worse than that in IM devices. Later, Lee et al. produced short channel (50 nm) JNT using a similar process flow, and the measured findings revealed very modest SCEs (SS 60 mV/dec and DIBL 7 mV/V).

The analogue performance of JL and IM multi-gate transistors was compared by Doria et al. in 2011 [37]. They offered a physical explanation of the analogue behaviour of the JL devices as well as information on how temperature affected it. When comparing the electrical properties of JL and IM devices, it was found that the JL structure had a lower drain current, which is connected to the JLT's poor field channel mobility due to its

heavy doping. Additionally, due to heavy doping, JL devices were shown to have a more significant effect of fin width variation on early voltage ($V_{EA} = I_D/G_D$) and intrinsic voltage gain ($A_V = G_m/G_D$) than IM devices. However, JL FETs have demonstrated to have superior VEA and greater AV than IM devices for all fin widths evaluated. Additionally, because JL devices lack the Zero Temperature Coefficient (ZTC) point (a bias point in the IV curve at which MOSFETs cease to be temperature-dependent), they behave analogically significantly differently from IM devices.

JL FETs, in contrast to IM devices, can sustain a steady drain current across a wide temperature range. However, the JL FET's reduced bulk mobility causes its drain output conductance (G_D) and transconductance values to be lower (G_m). Both junction-based and JL devices showed G_D deterioration as the temperature dropped. But the temperature dependency in the JL device has been shown to be weaker than in IM FETs. As a result, the JL device has demonstrated that V_{EA} and A_V are linearly dependent on temperature. However, these IM device performance measures saturate at about 300 K. For the JL device, it was demonstrated that the performance measure G_m/I_{DS} represents the efficiency of the transistor to convert drain current into transconductance and is nearly independent of temperature (between 223 K and 473 K) in the ON-state. This is quite beneficial for many analogue applications. Of contrast to IM devices, the unity-gain frequency in JL devices was shown to be lower. As a result, JL devices may have restrictions when used to RF applications. By using highly doped S/D extension areas in JL structures, the analogue and RF performance metrics including G_m, A_V cut off frequency, and current drivability may be further enhanced. The authors of this study did not take into account how the device's noise behaviour would be impacted by its only concentration on analogue characteristics.

The behaviour of JL devices in Low Frequency (LF) and Random Telegraph Noise (RTN) has received little attention in recent years [31–33,38]. According to a 2011 study by Nazarov et al. [31], the JL structure has a lesser RTN amplitude than IM devices. This is based on by the JL FET's bulk channel's low field lines, which noticeably lengthen the average time it takes for mobile carriers to be captured in traps close to the gate electrode. The JL multi-gate structure's LF noise behaviour was studied by Jang et al. the same year [33]. The findings showed that, in spite of the bulk conduction mechanism, the

Carrier Number Fluctuation (CNF) model provides a satisfactory explanation for the LF noise behaviour of the JL structure. The two types of noise sources that the CNF model is concerned with are: the first is variations in channel thickness brought on by a reduction in depletion width during partial depletion mode operation and the second is variations in carrier concentration at the silicon-oxide interface during accumulation mode operation. The JL devices' extracted trap density was observed to be nearly identical to IM devices. Degraded channel mobility caused by increased ionized-impurity scattering becomes a severe concern since the JL devices need a high doping concentration for effective device functioning. Lou et al. [39] have proven the JL structure with dual material gate (DMG) to enhance mobility degradation. They suggested a design, with two gates made of materials, with various work functions. According to reports, the usage of DMG was more successful in reducing the hot carrier effect and SCEs. Additionally, it has been demonstrated that DMG structures have lower Gm below V_{TH} and greater Gm in the ON-state compared to traditional single material gate JL structures, which is extremely helpful for quicker turn-off and higher ON-state speeds of the electronics devices.

The maximum oscillation frequency (f_{max}) and unity-gain cutoff frequency (f_T) may both be increased with the suggested structure while maintaining low gate bias, which is advantageous for high frequency applications. The optimization of numerous physical parameters, such as the size of two separate gate materials and their respective work functions, is necessary for such a structure. In several recent papers, Band To Band Tunneling (BTBT) between the drain and channel regions, which causes the parasitic bipolar junction effect in JL devices and considerably raises the OFF-state leakage current to an unbearable level, was also raised as a serious issue [40,41]. Additionally, the performance of the BTBT current was examined for the DMG structure [42]. By using DMG design in JNT, it was discovered that OFF state current may be enhanced by approximately two orders of magnitude. Although the exhibited results showed the DMG structure's great potential, it is highly difficult and demanding to produce DMG structures at the nanoscale size. Therefore, to lessen the complexity associated in the construction of DMG structures, new fabrication technologies must be developed. For the first time, Gnudi et al. evaluated the V_{TH} variability of JL devices [43]. Under the assumption of constant mobility, they developed an analytical model for V_{TH} variability in JL cylindrical silicon

nanowire (SiNW) and planar DG transistors. In highly scaled 20 nm JL SiNW FETs, it has been demonstrated that discrete dopant variations may induce V_{TH} variability to reach roughly 115 mV.

In JL devices, discrete dopant variation has become a significant issue. They did not, however, investigate the JL transistor's drain current variability or the effects of other causes of variability. Aldegunde et al. used 3D non-equilibrium Green's function simulations in 2012 to analyse the variability of the JL GAA SiNW transistor [44]. Along with V_{TH}, they also took into account I_{OFF}, I_{ON}, and SS variation brought on by random dopant fluctuations (RDF). It has been noted that JL structure exhibits more sub-threshold variability than their IM counterparts. Later, using the Impedance Field Method (IFM), Giusi et al. examined the fluctuation of the drain current caused by RDF in the JL DG structure [45]. They claimed that compared to the OFF regime, the current dispersion in the ON regime is significantly smaller. Additionally, it has been discovered that scaling—caused by rising SCEs—increases the variability of both the current and the V_{TH}. Additionally, they have created a mathematical link between the unpredictability of drain current and V_{TH} variability, also takes into account SCE and carrier degeneration corrections. They did, however, presuppose that RDF is the only source of variability.

The simulation analysis was carried out in 2013 by Parihar et al. to evaluate the potential of DG JLTs for ultra-low power (ULP) applications [46]. According to reports, DG JL devices can perform better than traditional DG MOSFETs in ULP (ultra-low power) applications. They also demonstrated that the JL device had the lowest sensitivity to gate length and the highest sensitivity to doping concentration. It has been suggested that using JL devices will make exact V_{TH} matching challenging. Choi et al. [47] also published a comparable study for the GAA JL structure. The GAA JL device has been discovered to be more vulnerable to V_{TH} variations brought on by width change than its IM equivalents. A modified JLT structure with moderate doping (10^{18} cm^{-3}) in the channel was proposed by Parihar et al. in 2014 [48]. Improved sub-threshold features have been seen in the simulation findings, however simultaneously, current performance is also impacted. They also noted a reduction in gate work function requirements and an improvement in V_{TH} variability (between 70% to 90%). The disadvantage of lowering channel doping is surface roughness scattering, which happens as a result of the silicon

body's conduction channel moving from the bulk area to the surface (accumulation mode), and a reduced drive current, which restricts its use to the ultra-low power domain.

In order to address the V_{TH} variability and impact ionization issue of heavily doped JL FET, Sahu et al. evaluated the performance of doping-less JLT in 2014 [49]. It has been discovered that undoped silicon channel JLTs are more resistant to RDF and process fluctuations. Additionally, the channel mobility has been much enhanced. The contact characteristics of metal/undoped-silicon must be difficult to manage throughout the production of doping-less JLT, nevertheless. In order to improve JL FET's current performance, materials other than silicon channel material have also been investigated. Germanium (Ge), a high mobility channel material, has
the following significant flaws:
1) It is challenging to manufacture high-quality gate oxide (GeO_2);
2) there is more tunneling leakage because the direct bandgap is narrower; and
3) low resistance contacts can emerge on n-type Ge substrates.
However, in the case of the JL structure, it is anticipated that oxide tunnelling, surface imperfections, and gate oxide thickness will have less of an impact on carrier transport dynamics. The effectiveness of multi-gate Ge JNTs was assessed by Yu et al. [50]. The findings showed that the Ge bulk JNT offered competitive ON-state current similar to its counterparts, simpler production, and enhanced electrostatic gate control. Bulk Ge JNT exhibit a little deterioration in gate control when compared to silicon, but an increase in ON-current performance is more important for enhancing gate responsiveness. Guo et al. [51] have also investigated Indium Gallium Arsenide, another high mobility material. The results of the experimental measurements have demonstrated good electrical properties for the suggested device design and the efficiency of the Indium Gallium Arsenide channel in lowering external resistance and therefore boosting driving current. Song et al. experimentally proved the effectiveness of III-V JNT in 2014 [52]. In order to prevent mobility deterioration and produce low S/D resistance, the device used in their study was constructed using an implantation-free method in which the S/D area was grown again, using Metal Organic Chemical Vapor Deposition (MOCVD).

In the III-IV JNT structure, high linearity has been reported with minimal bias dependency. This indicated that it was a good candidate for low power, high linearity

RF applications. Several analytical models for better understanding JL FETs' electrical behaviour have been presented in the literature. In the recent years, a number of analytical methods have been put out to address the channel potential distribution among JL DG FETs, including the variable separation methodology [53,54], parabolic approximation [55,56], Schwarz-Christoffel transformation [57], and series expansion method [58]. Asymmetric DG JL structures have also been modelled by Jin et al. [53,59] and Jazaeri et al. [60]. Using the conformal mapping approach, Kumari et al. published an enhanced 2D analytical model for DG JL FETs in 2015 [61]. The source and drain regions were assumed to be completely isolated when the concept was introduced.i.e., when the simulation is going on to focus mainly on channel region source and drain regions are kept in isolate position. Trevisoli et al. devoted their studies towards modeling JNTs [62,63] The drain current model for tri-gate JNTs was put out in[62] . For long channel devices, they solved the 2D Poisson equation to get the surface potential distribution, which was then utilized to calculate the charge density along the channel and the drain current. The 3D Laplace equation solution has been added to the 2D model, which also takes into account the effects of SCEs. They suggested a method to extract the V_{TH} of JNT and a physically based definition for it in [64]. On the basis of the same concept, an analytical model for the V_{TH} has also been created. The proposed methodology, however, was only applicable to long channel devices.

An intriguing investigation of planar SOI JLTs with non-uniform vertical channel doping was conducted by Mondal et al. [65]. This improved structure has been seen as being closer to a real-world device where the vertical distribution of impurities implanted with ions is not uniform. And the Gaussian distribution function has been used to describe this non-uniformity in the doping profile. The suggested structure improves leakage current, increasing I_{ON}/I_{OFF} ratio. The same group later conducted a similar study for non-planar structure in 2015 [66]. However, the Gaussian factors, namely segregation length (σ) and projection range (RP), on which the doping distribution depends heavily, were not taken into account in any of the publications.

The effect of temperature on the DC and AC performance of DG JL FETs with vertical Gaussian doping profiles at temperatures between 200 K and 400 K was examined by B. Singh et al. in 2016 [67]. It has been demonstrated that the ON-state current

increases approximately linearly with temperature whereas the OFF current of the suggested structure significantly reduces at 200 K in contrast to a uniformly doped structure. Additionally, it was discovered that between 200 K and 400 K, the influence of temperature on SCEs such as threshold voltage roll off, subthreshold swing, and DIBL of Gaussian doped DG JL FETs was less pronounced than that of their uniformly doped counterparts. At all temperatures, the suggested structure was also shown to perform better in terms of AC performance parameters such as total gate capacitance, transconductance, transconductance generation efficiency, and cutoff frequency.

In a recent study, Ferhati et al. [68] looked at the durability of Gaussian-doped DG JL MOSFETs against Self Heating Effects (SHEs). According to reports, the Gaussian profile has a significant impact on the I_{ON}/I_{OFF} ratio, the device immunity to SHEs, and the lattice temperature. This suggested design has demonstrated to have a greater capacity to close the gap between high electrical performances and higher device dependability, making it a potential replacement for dependable nano electronic applications. For the first time, B. Singh et al. established an analytical 2D model for channel potential and V_{TH} of DG JL FETs with vertical Gaussian doping distribution [69], in consideration of the benefits provided by Gaussian doped structure.

The 2D Poisson equation was solved using the evanescent mode analysis, and the electrostatic potential distribution throughout the channel was obtained. Instead of using a true non-analytic Gaussian function, they used a Gaussian-like function to make the derivation simpler. Additionally, they ignored the source/drain (S/D) depletion width by assuming the S/D length to be zero, which undoubtedly produced incorrect results for devices with shorter gate lengths.

Later, utilizing the superposition approach, Kumari et al. provided an analytical model of Gaussian doped DG JL FETs taking into account the S/D area [70]. The suggested model, however, was predicated on the supposition that the S/D area was entirely depleted, which is not necessarily true. They have also demonstrated how altering non-uniform doping profile parameters may optimize the leakage current and SCEs in DG JL FETs.

2.5 Review of various Dual Material Gate Junctionless FETs

In [15], W. Long et al. suggested Dual material gate (DMG) FETs as a general new form of field effect transistor (FET). The threshold voltage near the source is higher than that near the drain in this innovative gate arrangement because of the material work function difference (for n-channel FETs, the opposite is true for p-channel FETs). Charge carriers consequently move more quickly through the channel, and a screening effect is created to lessen short-channel effects. The theory, computer simulation findings, design recommendations, processing, and characterization of the DMGFET are thoroughly presented using the hetero structure FET as a vehicle.

In [71] Wei Long et al. the dual material gate field effect transistor (DMGFET), a brand-new category of device, is introduced. Two laterally contacting materials with various work functions make up the DMGFET's gate. In order to accelerate charge carriers in the channel more quickly and decrease short channel effects, this new gate construction takes use of the difference in material work functions by making the threshold voltage near the source more positive than that near the drain.

In [72], G. Venkateshwar Reddy et al, describe the special characteristics of a modified asymmetrical double-gate (DG) silicon-on-insulator (SOI) MOSFET. The front gate is made of two different materials, unlike the asymmetrical DG SOI MOSFET, which has a similar structure. When compared to the DG SOI MOSFET, the improved structure that is the dual-material double-gate (DMDG) SOI MOSFET displays much less short-channel effects (SCEs). This structure's SCEs have been investigated through the development of an analytical model. The surface potential, electric field, threshold voltage, and drain-induced barrier lowering are all calculated using the model. Also included is a model for the voltage gain, drain conductance, transconductance, and current drain.

The perceptible step in the surface-potential profile, which filters the drain potential, is observed to inhibit SCEs in this configuration. Demonstrated that, in comparison to the DG structure, the DMDG structure offers a simultaneous gain in transconductance and a drop in the drain conductance. To check the correctness of the analytical model, the results acquired via two-dimensional simulation are compared with those predicted by the model. In [73]. T. K. Chiang et al. a new two-dimensional model for asymmetrical dual

gate material double-gate (ADMDG) MOSFETs has been created, which includes surface channel potential, subthreshold swing, and threshold voltage. The simulation results that closely match those of the two-dimensional numerical simulator serve as proof that the model is accurate. The model offers fundamental ADMDG MOSFET designing guidelines in addition to providing physical insight into device physics.

In [74], T. K. Chiang et al. A novel two-dimensional model including channel potential, threshold voltage, and subthreshold swing for the dual material surrounding-gate (DMSG) MOSFETs is successfully created on the basis of the solution of the two-dimensional Poisson's equation. The simulation results that closely match those of the two-dimensional numerical simulator serve as proof that the model is accurate. The model offers fundamental designing guidelines for the DMSG MOSFETs in addition to providing physical insight into device physics.

In [75], Ravneet Kaur et al. suggested Dual Material Gate Insulated Shallow Extension Gate Stack (DMG ISEGaS) MOSFET structural design, combining the integration of Dielectric Pocket (DP) and Dual Material Gate (DMG) onto the traditional MOSFET which has been researched for increasing the analogue performance of scaled MOS devices. According to simulation studies, dual material gate engineering improves the analogue performance of the design in terms of intrinsic gain (g_m/g_d), early voltage (V_{EA}), and g_m/i_d.

In [76], Muhammad Mustafa Hussain et al. the integration complexity has been addressed for the first time by integrating a group of complementary metal oxide semiconductor (CMOS) FinFET devices with two separate high-k/metal gate stacks with dual work function on the same wafer. In a procedure that also involves dual metal gate etching and gate stack integration, two entirely distinct metals that were created by atomic layer deposition have been combined. With reasonably symmetric V_{TH}, excellent short channel characteristics with minimal drain induced barrier lowering (DIBL) and subthreshold swing SS have been seen.

In [77], Pedram Razavi et al. using two-dimensional (2-D) simulation, the short channel effects of a modified symmetric double-gate MOSFET made of dual material gates and an oxide stack with high-k material on top of a SiO2 layer were evaluated and compared to those of a standard symmetric double-gate MOSFET. Comparing this

structure to the traditional double-gate MOSFET, it has improved current characteristics and decreases short channel effects (SCEs) such as drain-induced barrier lowering (DIBL), the hot electron effect, and threshold voltage roll-off.

In [78], R. S. Saxena et al. presented a new dual-material-gate-trench power MOSFET which shows a notable increase in transconductance and breakdown voltage without suffering any on-resistance deterioration. The gate of a typical trench MOSFET is divided into two pieces, in this arrangement for work-function engineering. The inversion charge in the channel is shared between the two gates. The device performance was demonstrated using 2-D numerical simulation by changing the lengths of the two gates to permit an equal proportion of the inversion charge. The peak transconductance and breakdown voltage of the novel device improved by around 44% and 20%, respectively, in comparison to the traditional trench MOSFET, respectively, by employing N+ poly-Si as a lower gate material and P+ poly-Si as an upper gate material.

In [79], the advantages of double-gate and dual-material-gate architectures are combined and proposed a dual-material double-gate (DMDG) silicon-on-insulator (SOI) metal-oxide-semiconductor field-effect transistor (MOSFET) for sub-100 nm devices. The alignment of the top and bottom gates, which has a significant impact on the performance of the DMDG-MOSFET, is one of the main problems. In this, the consequences of gate misalignment in the DMDG SOI n-MOSFET were examined. The impacts of gate misalignment on device performance, such as surface potential, electric field, threshold voltage, subthreshold slope, drain-induced barrier lowering, drain current, and transconductance, have been examined in this respect through analytical modelling and in-depth simulations. Both source and drain side misalignments have been considered since gate misalignment can happen on any side of the gate.

In [80], for the advanced nanoscale technology, a novel device configuration known as the dual-material gate SOI MOSFET (DMG SOI MOSFET) is proposed to prevent drain-induced barrier lowering (DIBL) and the short-channel effects (SCEs). Analyzing the electrical properties, the analytical threshold voltage model of the innovative structural device is proposed. Compared to the traditional SOI MOSFET, the DMG SOI MOSFET with high-k dielectric performs better in suppressing DIBL and improving carrier transport efficiency. The DIBL decreases as the dielectric constant rises. The

analytical threshold voltage model and the two-dimensional device simulations have a fair level of agreement.

In [81], explore in 16nm MOSFET devices, the dual material gate (DMG) and inverse DMG devices are used to reduce characteristics variation brought on by random dopant fluctuation (RDF). Researchers have looked at and examined the physical mechanisms used by DMG devices to inhibit RDF. DMG has improved by 28%, 12.3%, and 59% for controlling the RDF-induced V_{TH}, I_{ON}, and I_{OFF} fluctuation, respectively. In [82], examines four common instances of how to reduce short-channel effects using dual-material gate MOSFETs. The double doping gate (DDG) Lightly-doped-Drain (LDD) MOSFET is then introduced as a unique device construction. This new gate design makes use of the material work function. A 2-D device simulator called MEDICI is used to mimic the model. The simulation's outcome demonstrates that by varying the polysilicon's doping concentration, a suitable threshold voltage may be obtained. In the meanwhile, the driving capability has been significantly increased over that of a normal MOSFET. The construction procedure is not difficult and is currently readily accomplished.

In [39], It is suggested to use a dual-material-gate junctionless nanowire transistor (DMG-JNT). Using 3-D numerical simulations, its characteristics are shown and contrasted with a typical single-material-gate JNT. The findings demonstrate that the DMG-JNT has several advantageous characteristics, including a high ON-state current, a high I_{ON}/I_{OFF} current ratio, improved transconductance g_m, a high unity-gain frequency f_T, a high maximum oscillation frequency f_{max}, and a reduced drain-induced barrier lowering. The consequences of various work-function disparities between the two gates and various control gate ratios are investigated. Finally, the work-function difference optimization for the DMG-JNT is shown.

In [83], the superiority of silicon-on-nothing (SON) over silicon-on-insulator MOSFET is established analytically due to SON's greater resistance to various short-channel effects and enhanced current driving capacity. Additionally, it has been demonstrated that the analytical model accords with a variety of simulation findings from MEDICI, ATLAS 2-D, and other sources. Classical models are insufficient to effectively predict the potential profile, threshold voltage, or charge inversion events for dual-material double-gate (DMDG) SON MOSFETs due to the ultrathin device structure.Under the dual-material

front gate, the 2-D Poisson and 1-D Schrodinger equations have been solved to determine the overall potential and inversion charge profile. Calculated and combined with the classical threshold voltage to produce its quantum equivalent is the quantum threshold voltage's variation from the classical one. Additionally, the suggested model has been examined using the numerical device simulator ATLAS 2-D.

In [84], performed a simulation investigation of the performance characteristics of an analogue circuit for a symmetric double-gate junctionless transistor (DGJLT) employing a dual-material gate and high-k spacer dielectric (DMG-SP) on both sides of the device's gate oxides. The parameters are illustrated and contrasted with single-material (conventional) gate (SMG) and DMG DGJLT. In comparison to the SMG DGJLT, the DMG DGJLT offers better intrinsic gain (G_m/R_o), early voltage (V_{EA}), and transconductance (g_m). The high-k spacer boosts the fringing electric fields through the spacer, significantly enhancing the values for DMG-SP DGJLT.

In [85], It is suggested to use a bulk-FinFET with a dual material gate, or DMG-Bulk-FinFET. Using 3-D simulations, its features are contrasted with those of the typical bulk-FinFET. It is shown that the novel structure possesses characteristics that inhibit short channel effects, enhance transconductance, and increase carrier transport effectiveness. Additionally, the work function differential and gate length ratio may be engineered to enhance these aspects. This paper proposes an optimization plan for the DMG structure and demonstrates how the DMG-Bulk-FinFET performs better than its predecessor with a single material gate.

In [86], presented the asymmetric dual material (DM) junctionless double gate transistor 2-D drain current model. Transconductance and its higher order derivatives are computed based on channel potential and validated using the output of the ATLAS 3-D device simulator. The created model may be used to examine how well the device performs digitally in terms of the nMOS inverter circuit's voltage transfer characteristics. Analog performance and the length of the control gate studied. Through thorough circuit modelling, the results further demonstrate the benefit of the DM gate over the single material gate for digital and analogue applications employing CMOS inverters and common source amplifiers.

In [87], in the subthreshold region of operation, the analogue performance of 100

nm dual-material gate complementary metal oxide semiconductor (DMG CMOS) devices is presented. With the aid of thorough device simulations, the analogue performance parameters for the DMG nMOS (metal oxide semiconductor) devices transconductance gm, transconductance generation factor g_m / I_D, Early voltage V_{EA}, output resistance R_o, and intrinsic gain as well as V_{EA} and R_o for the DMG pMOS devices are systematically investigated. Study is also done on how various capacitances affect the unity-gain frequency f_T. It is discovered that the DMG CMOS devices perform noticeably better than their single-material gate (SMG) equivalents. When DMG is utilized for both the n- and p-channel devices, a voltage gain enhancement of more than 70% is shown for the CMOS amplifier.

In [88], It is suggested to use a dual material gate silicon on insulator junctionless transistor (DMG SOI JLT). Using simulation tools from EDA, its properties are shown and contrasted with those of a single Material gate Silicon-On-Insulator Junctionless Transistor (SMG SOI JLT). The outcome demonstrates that the single Material Gate Silicon on Insulator Junctionless Transistor cannot drive as much current as the DMG-SOI JLT. The transition of two gates is abruptly altered by the potential distribution of DMG SOI JLT, which also strengthens the electric field in the channel. In comparison to SMG SOI JLT, when the channel length reduces, DIBL and sub threshold slope change is less in DMG SOI JLT. SMG SOI JLT transconductance is 0.25mS for a channel length of 20nm.

In [89] The rate of technological scaling was slowed down significantly by leakage effects in planar transistors; however, these effects may be mitigated by non-planar transistors. The contribution of two configurations of fin-shaped field effect transistors with dual materials for the gate and gate dielectric but different active fin region materials has been examined. Using the TCAD simulator, both architectures with 14nm gate lengths were designed and simulated. On-off current ratio, subthreshold swing, and the effect of integrating two materials in the active fin area on performance characteristics have been determined. Leakage current of $1.99\text{x}10^{-16}$A has been recorded in heterojunction structures, demonstrating their superiority to homo junction structures and making them a very viable option for integrated circuits with low power dissipation.

In [90], investigated a gate-normal tunnelling field-effect transistor (TFET) built

on SiGe/Si with pillar-shaped contacts to the tunnelling junction offers two important benefits. The first is enhanced electrostatics at the tunnelling junction's edge, which serves to lessen the impact of unfavorable tunnelling routes and, as a result, significantly speeds up device activation. The second involves a self-aligned procedure for the streamlined manufacture of a dual-metal gate.The study offers broad recommendations for enhancing the subthreshold swing in gate-normal TFETs that are not constrained by the material system.

In [91] a generalized analytical subthreshold behaviour model for dual-material gate (DMG) and junctionless omega-gate (JLG) MOSFETs is developed. To build a model based on the effective conducting central potential, acquired by the quasi-3D potential approach.It results in a better prediction of subthreshold behaviour and offers a more precise definition of the scaling equation for JL GFETs. In order to improve immunity to short channel effects, dual materials were used, taking into account both the renewed potential and the present models. Other multiple-gate (MG) nano-transistors can also be effectively modelled.

In [92], the operation of devices for the DMG SOI structure has been shown to be impacted by the gate oxide material. The DMG silicon on insulator metal oxide field effect transistor has been shown to be superior to the planar one because it lessens a variety of short channel effects. With the use of the 2-D Poisson equation, a 2-D analytical model of the dual material gate SOI structure is created in order to compute different device parameters, including the minimum surface potential, electric field, surface potential, and threshold voltage, among others. Different gate oxide materials, such as SiO_2, and HfO_2 with varying relative permittivity are included into the DMG-SOI MOSFET structure, and comparative research has been conducted to assess the effects of these materials on the performance of the device. HfO_2, which has a greater gate dielectric constant than other gate dielectric materials, has been found to exhibit improved device performance.

2.6 Summary

Based on literature survey discussed in above sections, Chapter 2 can be concluded with a few major observations as follows: The Dual Material Gate (DMG) Junctionless

FinFET is a transistor architecture that combines the benefits of a junctionless design and a dual material gate structure.
Here is a summary of its key features and advantages: Unlike traditional MOSFETs, which rely on a pn-junction to control current flow, the DMG JL FinFET is junctionless. It eliminates the need for precise doping profiles and simplifies the manufacturing process, reducing threshold voltage variations and improving device uniformity. The DMG JL FinFET features a dual material gate, composed of two different materials with contrasting properties. This structure enhances the transistor's electrostatic control and improves its performance.
The DMG JL FinFET enables threshold voltage tuning by adjusting the relative work functions of the two gate materials. This feature provides flexibility in optimizing transistor characteristics and adapting to different circuit requirements. The junctionless design and dual material gate structure of the DMG JL FinFET make it highly scalable. It can be fabricated with smaller dimensions, allowing for higher transistor densities and improved integration in advanced semiconductor technologies.

Due to its impressive characteristics, including strong SCEs immunity, high drive current capability, high effective carrier mobility, and high transconductance, the DMG JL FinFET can surpass planar MOSFET. As a result, it is suitable for a wide range of applications, including low-power circuits, radio frequency, memory, and systems-on-chip. Therefore, there is a lot of scope for improvement in the simulation of the oxide engineering and gate material engineering of DMG JL FinFET. The aforementioned literature review provides information on the thesis's purview, which is stated in Chapter 1.

Chapter 3

Design and Analysis of DMG JLFinFET: DC Perspective

3.1 Introduction

The possibility of scaling of MOS (metal oxide semiconductor) devices has made the Complementary CMOS technology commercially successful[93]. As CMOS devices are scaled into deep sub-micrometer regimes, power dissipation increases dramatically due to an increase in leakage current (caused mostly by threshold voltage lowering) and other factors like drain-induced barrier lowering (DIBL), temperature effect, narrow width effect, gate-induced drain leakage (GIDL)[94]. Furthermore, due to direct scaling, conventional MOSFETs have issues such as excessive parasitic capacitance, and surface mobility deterioration. Two solutions were proposed: the first was to operate the device at low temperatures, and the second was Fully Depleted Silicon on Insulator (FDSOI)[95–97].

Thin-film SOI MOSFETs have enhanced short channel effects (SCEs), have excellent latch-up immunity, and have a lower DIBL impact[98]. But SOI devices has lower carrier transport with high electric field near drain, causes hot-carrier effect[99]. To overcome these issues double-gate devices were proposed [100][101]. The overlap capacitances are the major problem in double-gate devices due to miss alignment of gates [102]. To alleviate above problems self-aligned FinFETs were proposed where gate is self-aligned to reduce parasitic resistance and it is effectively controlling SCEs [103–105]. Bulk and SOI technologies are the two ways for designing FinFETs. The advantage of bulk tech-

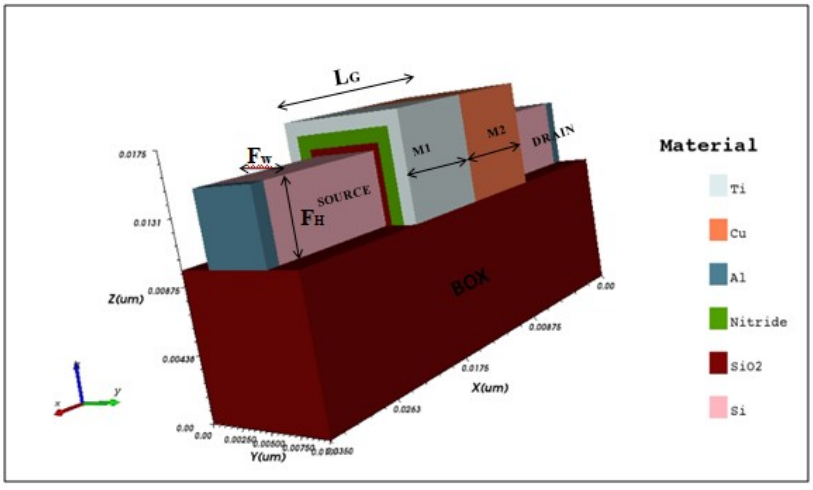
nology was low self-heating and wafers at a reasonable cost are available [106][107], on other hand SOI FinFETs have more saturation current and low leakage current and low parasitic capacitances [108–110].

The gate material engineering was proposed [15,111–113] with two different work function materials are used for gate structures to increase the efficiency of carrier transportation which suppresses the SCEs [114–118]. FinFETs are suitable devices to control the leakage current. FinFETs are front runners of current nanometer technology. Dual material bottom spacer ground plane FinFET performance was analyzed and shows that dual material improves Ion/Ioff ratio and ground plane reduces the DIBL [119]. Different structures are proposed in literature like Teeth Junctionless Gate All around Field Effect Transistor[120] and Ion Sensitive Field Effect Transistors (ISFET)[121]. To the best of authors knowledge in the literature very few dual material gate FETs were designed but, not dual material gate junctionless FinFET.
The design and analysis of DMG JL FinFETs from a DC perspective are motivated by the goals of improving transistor characteristics, optimizing off current,sunthreshold swing and DIBL, enabling enhanced scaling, providing circuit design flexibility, and ensuring process simplicity and compatibility. In this chapter, we proposed Dual Material Gate JLFinFET to reduce SCEs. The organization of the chapter as follows. Section 3.2 describes the device structure, section 3.3 results and discussion with I_{on}/I_{off} current ratio, SS, and DIBL included and section 3.4 concludes the chapter with summary.

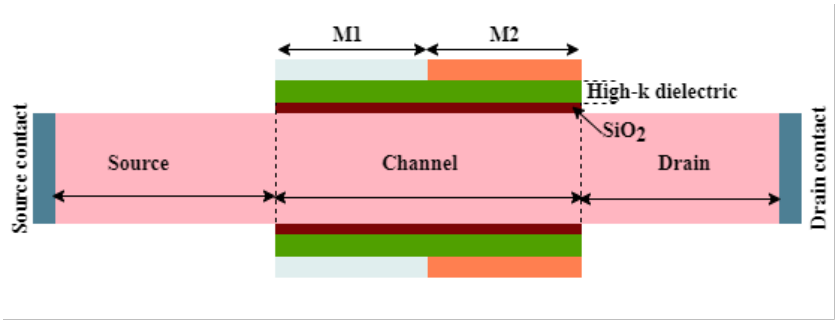
3.2 Device Structure and Simulation Setup

The DMG JLFinFET 3D schematic is shown in Fig 3.1(a) and 2D X-Y cut of DMG JLFinFET shown in Fig 3.1 (b). The gate length (L_G) is 14nm, fin height (F_H) is varied from 10nm to 30nm, fin width (F_H) is varied from 4nm to 6nm. To avoid junction formation at nanoscale, uniform doping is used. Si_3N_4 and HfO_2 are used as high-k materials. All simulations using Visual TCAD are carried out at T=300K.

The mid-gap metals are used as gate materials. The metal gate work function for M1 is 4.9eV and M2 is 4.3eV to 4.7eV which are placed at source side and drain side, respectively. The gate stack is made of SiO_2, Si_3N_4 and HfO_2 with thickness of 0.5nm,



(a) Three-dimensional view of DMG JLFinFET



(b) 2D X-Y cut view of DMG JLFinFET

Figure 3.1 Structure of DMG JLFinFET

0.96nm and 3.07nm respectively.The gate metals are with 1nm thickness. All contacts are made with aluminum. The physical models: band gap narrowing and dopant dependent models are used as the doping concentration is uniform from source to drain. Fermi Dirac distribution model is used to get good accuracy and SRH model is used to estimate generation and recombination effects. Lombardi mobility model is invoked to find mobility degradation. Gummel and Newton numerical methods are invoked to attain good results. Quantum drift-diffusion model invoked for the quantum confinement effect. To validate the simulation results we calibrated the experimental data [122] shown in Fig 3.2. The device dimensions and parameters used in this work are given in Table 3.1.

Table 3.1 Device dimensions and parameters used

Parameter	Value
Gate length	14nm
Fin width	(4-6) nm
Fin height	(10-30) nm
Interfacial Layer SiO_2	0.5nm
High-k dielectric thickness	Variable (Si_3N_4 - 0.96nm, HfO_2 - 3.07nm)
EOT (Equivalent Oxide Thickness)	1nm
Supply Voltage	0.8V
Work function of M1	4.9eV
Work function of M2	4.3eV- 4.7eV

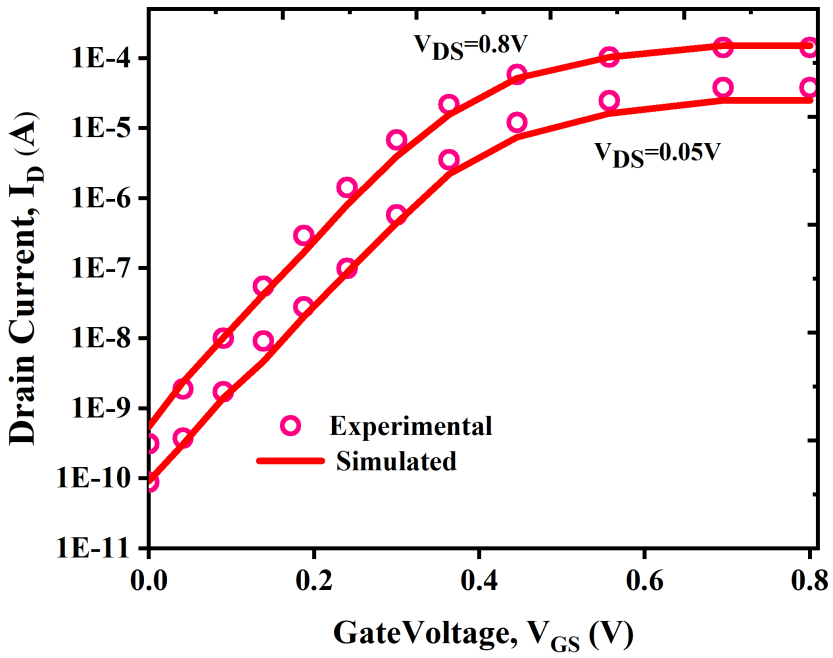


Figure 3.2 Calibrated Drain Characteristics of DMG JLFinFET [122]

3.3 Results And Discussions

The drain characteristics of the DMG JLFinFET simulated in two groups. First one used different single dielectric material as gate oxide and second one by various Gate

Stack(GS) configurations to investigate the effect of GS on 14nm gate length. We used single dielectric materials SiO_2, Si_3N_4 and HfO_2 with thickness of 0.5nm, 0.96nm and 3.07nm respectively. For GS configuration SiO_2+Si_3N_4, SiO_2+ HfO_2, Si_3N_4+ HfO_2 are used. Figure 3 shows I_{ON}/I_{OFF} ratio while varying workfunction of M2 with single gate oxide i.e SiO_2 for different doping concentration levels (5E17 cm^{-3} to 5E19 cm^{-3}). Fig. 3.4 shows the effect of doping variation on drain current with single gate oxide i.e SiO_2, Si_3N_4 and HfO_2. In single gate oxide the DMG JLFinFET with HfO_2 as gate oxide has less leakage current due to high dielectric constant of HfO_2.

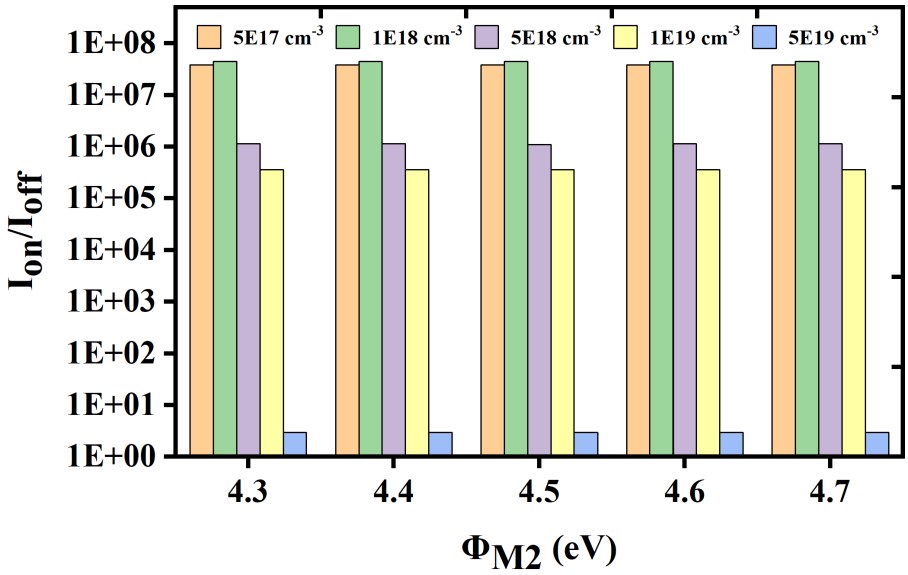


Figure 3.3 ϕM2 Vs Ion/Ioff with SiO2 as gate oxide at constant ϕM1=4.9eV

3.3.1 Gate Oxide Engineering

SiO_2, Si_3N_4 and HfO_2 are taken as gate oxides individuvally with dielectric constant 3.9 ,9 and 24, respectively. SiO_2 with 0.5nm considered as interfacial layer, Si_3N_4 and HfO_2 is 0.96nm and 3.07nm, respectively to get EOT=1nm considered as per IRDS[123]. In each case Ioff was extracted. work function of M1 is fixed. i.e. ϕ_{M1}=4.9 eV and vary the workfunction of M2 i.e. ϕ_{M2} from 4.3 eV to 4.7 eV. The doping concentration of source , drain and channel are taken as uniform because simultaions are performed for JLFinFET. The I_{ON}/I_{OFF} variation is observed by taking different doping levels. The doping concentration is varying from 5x$10^{17}$$cm^{-3}$ to 5x$10^{19}$$cm^{-3}$. From below Fig.3.3 it is evident that I_{ON}/I_{OFF} ratio is good for doping concentration of 1x$10^{18}$$cm^{-3}$ compared to

other doping concentration levels. However, with increasing the workfunction of M2, the off state current gradually increases and it is more for doping concentration $5x10^{19}cm^{-3}$ hence the I_{ON}/I_{OFF} ratio is very low for doping $5x10^{19}cm^{-3}$. It is observed from Fig 3.3 the variarion of ϕ_{M2} is less effect on I_{ON}/I_{OFF} but the variation of I_{ON}/I_{OFF} is more in doping concentration. The slight variation of I_{ON}/I_{OFF} has observed at ϕ_{M2}=4.5eV. Fig 3.4 shows the I_{ON}/I_{OFF} ratio with doping variation with fixed ϕ_{M1}=4.9eV and ϕ_{M2}=4.5eV. it is evident from Fig 3.4 that Compared to SiO_2 and Si_3N_4 gate oxides, HfO_2 has less leakage current because the dielectric constant of HfO_2 is higher than SiO_2 and Si_3N_4. Hence the I_{ON}/I_{OFF} ratio is also high for HfO_2.

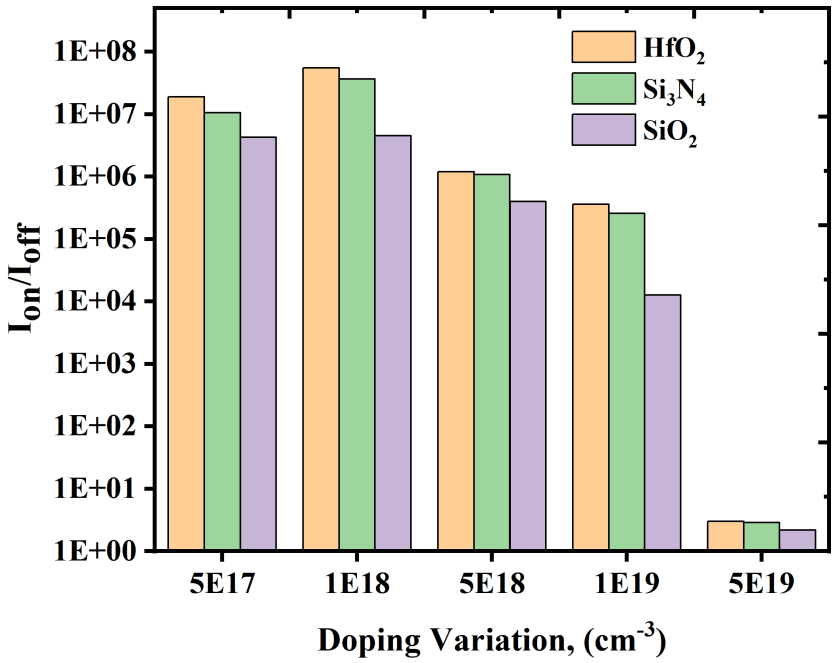
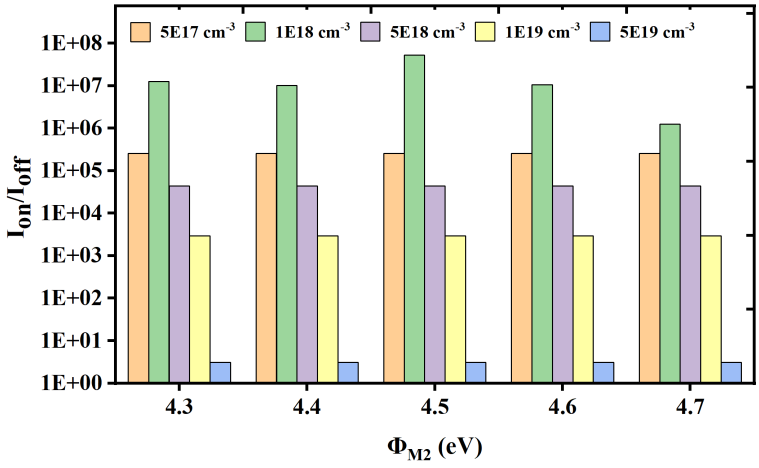
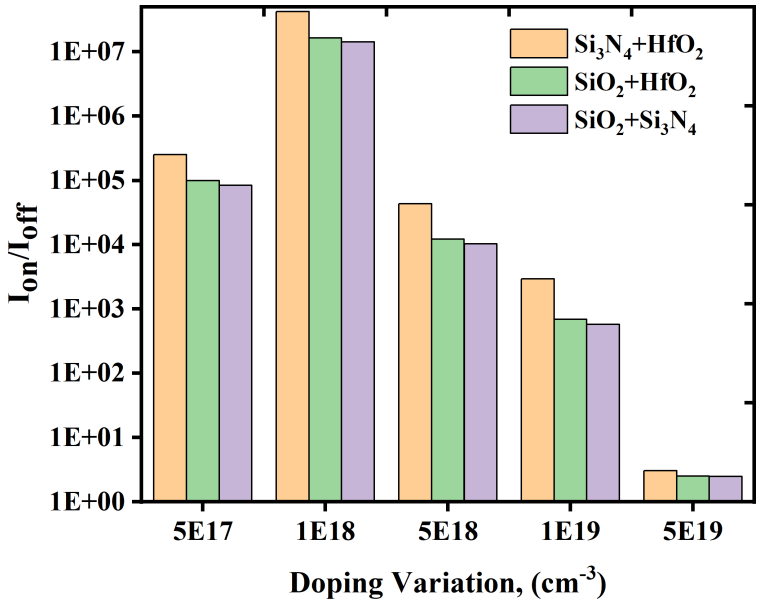


Figure 3.4 I_{ON}/I_{OFF} Vs Doping Variation with fixed ϕM1=4.9eV and ϕM2=4.5eV for different single gate oxides



(a) ϕM2 Vs I_{ON}/I_{OFF} with SiO2+Si3N4 as gate oxide at constant ϕM1=4.9eV

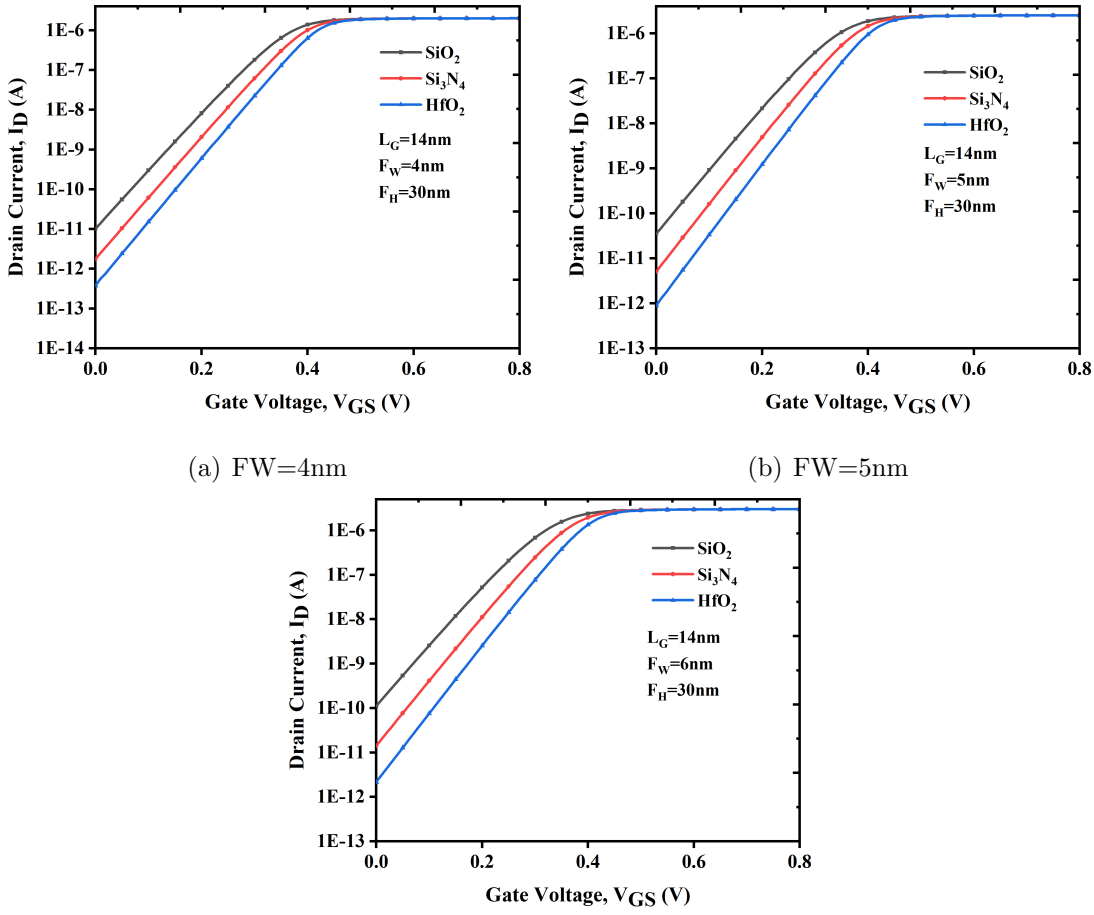


(b) I_{ON}/I_{OFF} Vs doping variation with fixed ϕM1=4.9eV and ϕM2=4.5eV for different dual gate oxides

Figure 3.5 Doping concentration levels

From above Fig 3.4 and 3.5(b) it is observed that doping concentration $1x10^{18}cm^{-3}$ at work function ϕ_{M1}= 4.9eV and ϕ_{M2}=4.5eV, The I_{ON}/I_{OFF} is good compared to all other doping concentrations. The rest of simulations for fin width and fin height variation, doping concentration $1x10^{18}cm^{-3}$ and work function ϕ_{M1}= 4.9eV and ϕ_{M2}=4.5eV are considered.

3.3.2 Fin Width Variation



(a) FW=4nm

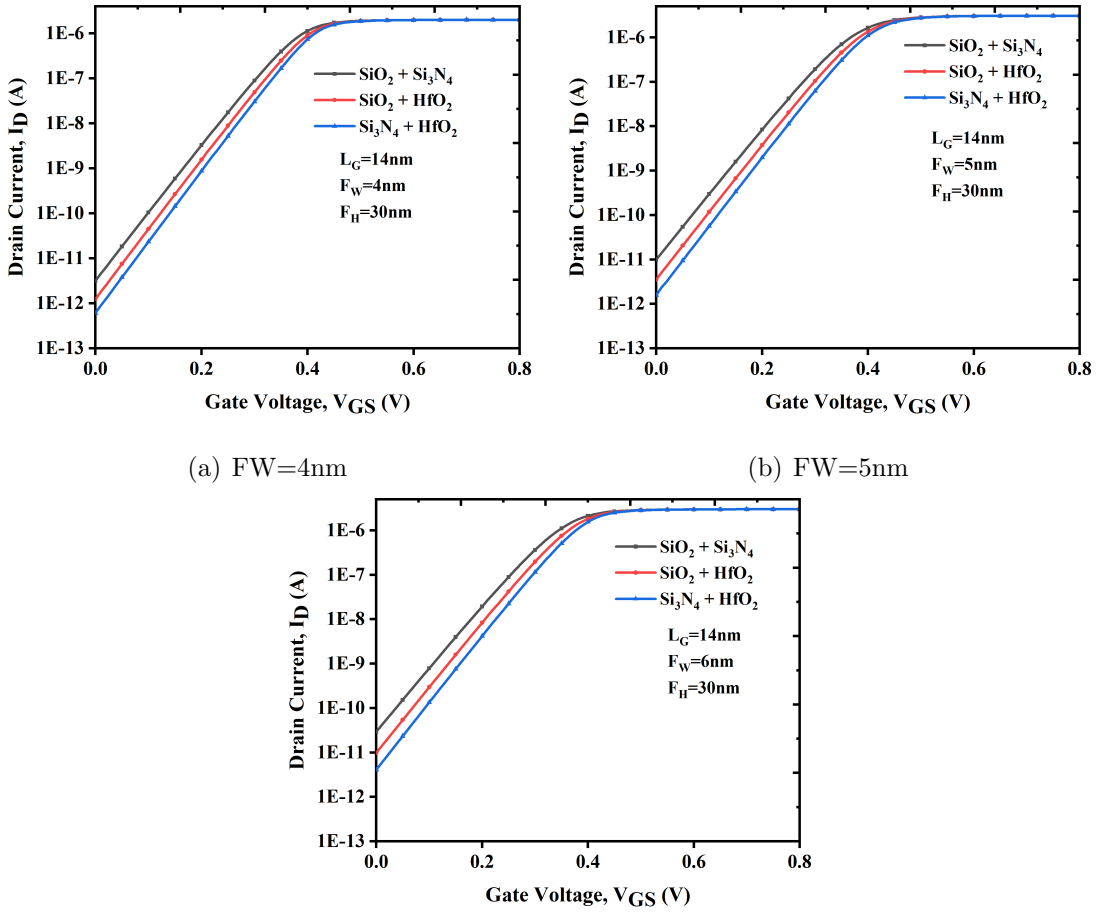
(b) FW=5nm

(c) FW=6nm

Figure 3.6 Fin width variation of DMG JLFinFET with single gate oxides

The drain current versus gate voltage for different fin widths with single gate oxides are shown in Fig 3.6. The gate length (L_G) and fin height (F_H) are fixed at 14nm and 30nm with fin width (F_W) varying from 4nm to 6nm. The drain current variation was observed for single gate oxides SiO_2, Si_3N_4 and HfO_2 with thickness of 0.5nm,0.96nm and 3.07nm respectively. By increasing the F_W off current also increased slightly because it loses the gate control over the channel[124]. Among the F_W variation lowest F_W 4nm has less I_{OFF} and I_{ON}/I_{OFF} ratio is $>10^6$ for the same. The drain current dependence on fin widths with dual gate oxides are shown in Fig 3.7. The gate length (L_G) and fin height (F_H) are fixed at 14nm and 30nm, fin width (F_W) varying from 4nm to 6nm. SiO_2+Si_3N_4, SiO_2+HfO_2 and Si_3N_4+HfO_2 are used as dual gate oxides with thickness of 1.46nm,3.57nm and 4.06nm respectively. While F_W is increasing I_{OFF} also increased

where the control action of gate is less. SiO_2+ HfO_2 gate stack configuration with F_W 4nm has less I_{OFF} with value of 5.79 x10^{-13}(A). The I_{ON}/I_{OFF} ratio is 1.71× 10^6far better for dual gate oxide than single gate oxide configuration.



(a) FW=4nm

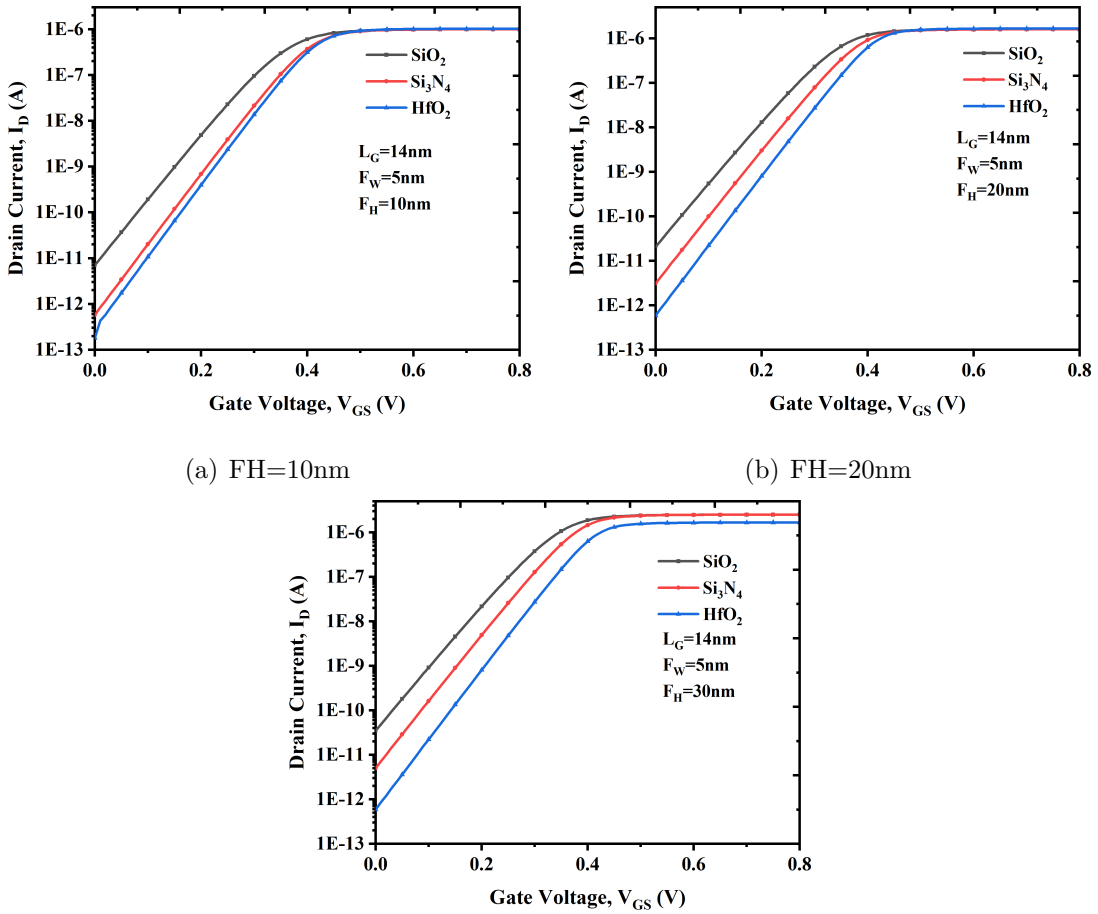
(b) FW=5nm

(c) FW=6nm

Figure 3.7 Fin width variation of DMG JLFinFET with dual gate oxides

3.3.3 Fin Height Variation

The effect of Fin height variation using single gate oxides on drain current is shown in Fig 3.8. L_G and F_W are fixed to 14nm and 5nm. Fin height (F_H) is varied from 10nm to 30nm. By increasing the F_H, the I_{OFF} also increasing. For higher F_H 30nm the I_{OFF} is more due to side wall fringing fields at high fin height.



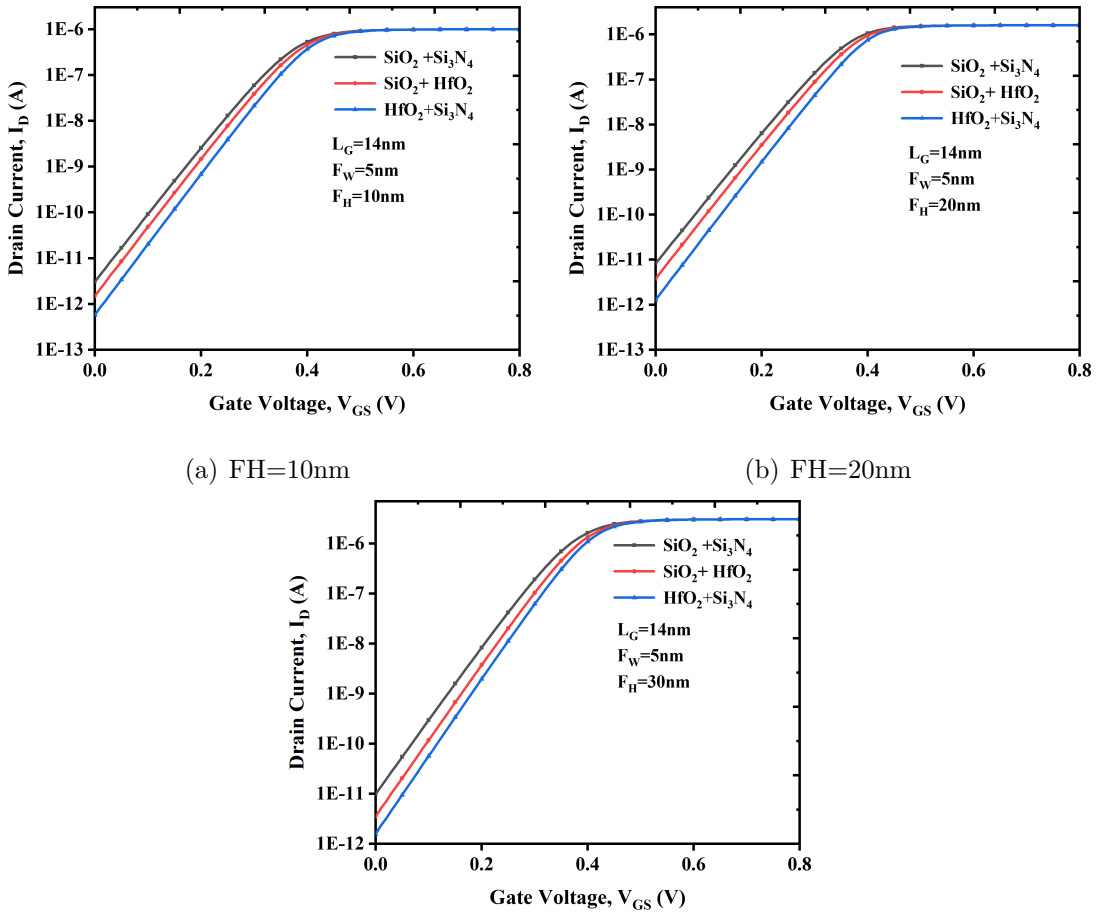
(a) FH=10nm

(b) FH=20nm

(c) FH=30nm

Figure 3.8 Fin height variation of DMG JLFinFET with single gate oxides

The effect F_H variation using dual gate oxides on drain current is shown in Fig 3.9. L_G and F_W are fixed to 14nm and 5nm F_H is varied from 10m to 30nm. An increase in F_H alters device design, resulting in a decrease in aspect ratio (F_W/F_H). The I_{ON}/I_{OFF} ratio should increase with F_H, however it falls with decreased sensitivity owing to quantum confinement phenomenon[124]. The I_{ON}/I_{OFF} ratio exceeding 10^6 at the lowest F_H of 10nm and I_{OFF} staying <pA assures continued down scaling. An increasing the F_H , I_{OFF} also increasing. For higher F_H 30nm the I_{OFF} is more due to less electrostatic integrity at high F_H.



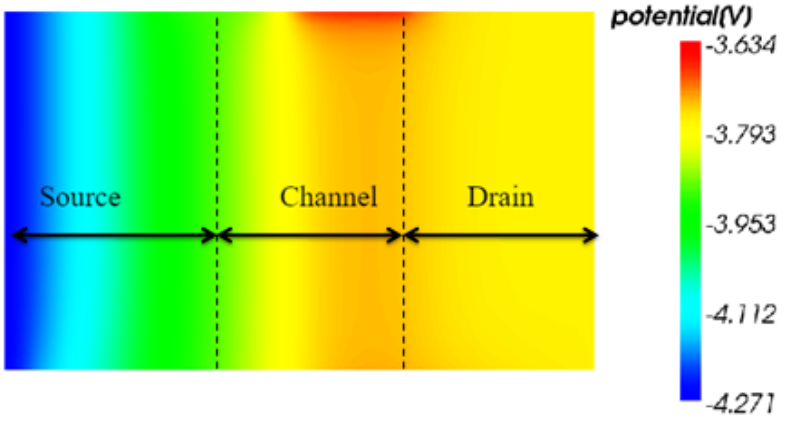
(a) FH=10nm

(b) FH=20nm

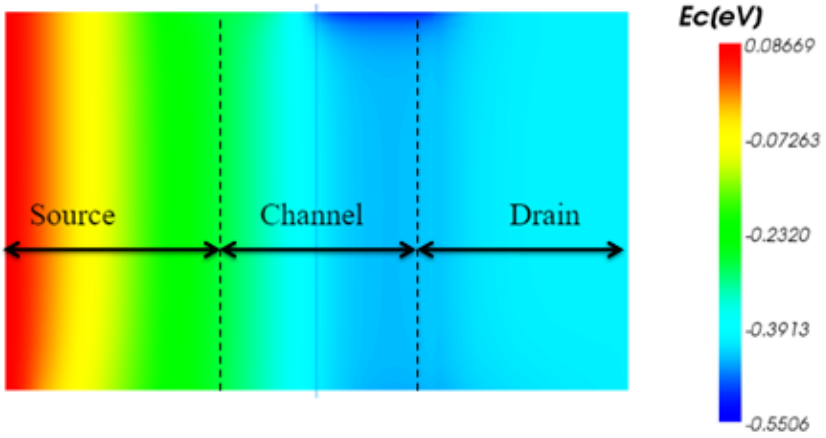
(c) FH=30nm

Figure 3.9 Fin height variation of DMG JLFinFET with dual gate oxides

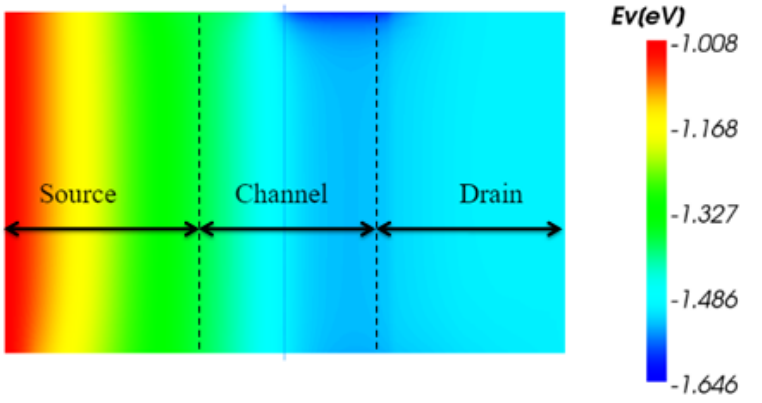
Figure 3.10(a) shows how the distribution of potential occurred in DMG JLFinFET. At the drain side the potential distribution is high and it is less in source and channel thus reducing SCEs. figure 3.10(b) and (c) shows the contour plots of conduction band energy and valence band energy. In both the energy level is more at source side and low at drain side because of band bending.



(a) Horizontal X-Ycut contour plots of potential distribution



(b) Conduction band energy



(c) Valence band energy of DMG JLFinFET with VGS=0.8V and VDS=0.8V at 300K

Figure 3.10 Distribution of potential occurred in DMG JLFinFET

Table 3.2 Performance Parameters of DMG JLFinFET with L_G=14nm, F_H=30nm, F_W=6nm

Configuration	Gate oxide	I_{ON} (A)	I_{OFF} (A)	I_{ON}/I_{OFF}	SS (mV/dec)	DIBL (mV/V)
Single Gate oxide	SiO_2	2.99×10^{-5}	1.11×10^{-11}	2.69×10^{6}	72.48	50.56
	Si_3N_4	2.99×10^{-5}	1.42×10^{-11}	2.11×10^{6}	67.53	33.60
	HfO_2	2.99×10^{-5}	2.17×10^{-11}	1.38×10^{6}	62.90	22.33
Dual Gate oxide	SiO_2+Si_3N_4	2.99×10^{-5}	2.92×10^{-11}	1.02×10^{6}	69.23	38.80
	SiO_2+HfO_2	2.99×10^{-5}	9.81×10^{-11}	3.05×10^{6}	66.79	31.07
	Si_3N_4+HfO_2	2.99×10^{-5}	4.07×10^{-12}	7.34×10^{6}	64.14	25.98

Table 3.3 Performance Parameters of DMG JLFinFET with L_G=14nm, F_H=30nm, F_W=5nm

Configuration	Gate oxide	I_{ON} (A)	I_{OFF} (A)	I_{ON}/I_{OFF}	SS (mV/dec)	DIBL (mV/V)
Single Gate oxide	SiO_2	2.52×10^{-5}	3.52×10^{-11}	7.16×10^{5}	69.83	42.79
	Si_3N_4	2.52×10^{-5}	8.94×10^{-13}	2.82×10^{6}	65.29	28.95
	HfO_2	2.52×10^{-5}	5.08×10^{-12}	4.96×10^{6}	62.41	19.01
Dual Gate oxide	SiO_2+Si_3N_4	3.06×10^{-5}	9.89×10^{-12}	3.09×10^{6}	66.10	33.15
	SiO_2+HfO_2	3.06×10^{-5}	3.54×10^{-12}	8.64×10^{6}	62.14	26.55
	Si_3N_4+HfO_2	3.06×10^{-5}	1.58×10^{-12}	1.93×10^{7}	61.22	22.18

The I_{ON}/I_{OFF} ratio is a significant electrical performance characteristic of the device, and it is intended to be high. The on-state (I_{ON}) current is obtained as the drain current at gate voltage (V_{GS}) = 0.8 V and V_{DS} = 0.8 V. High-k gate dielectrics can improve the I_{ON}/I_{OFF} ratio but mobility deterioration is a serious issue with high-k gate dielectrics owing to the scattering effect. The GS high-k metal gate technology has been utilized to control the mobility degradation problem.

The performance parameters I_{ON}/I_{OFF}, SS and DIBL are calculated with F_W variations and tabulated in Tables 3.2, 3.3, and 3.4. As depicted in the tables single gate oxide configuration with HfO_2 is giving good I_{ON}/I_{OFF} ratio for all F_W variations. In dual gate configuration Si_3N_4 +HfO_2 has better I_{ON}/I_{OFF} ratio and it is maximum at F_W=5nm, approximately 1.93 x10^7. SS and DIBL are two important characteristics to study in

Table 3.4 Performance Parameters of DMG JLFinFET with L_G=14nm, F_H=30nm, F_W=4nm

Configuration	Gate oxide	I_{ON} (A)	I_{OFF} (A)	I_{ON}/I_{OFF}	SS (mV/dec)	DIBL (mV/V)
Single Gate oxide	SiO_2	2.01×10^{-6}	1.02×10^{-11}	1.97×10^{5}	67.35	35.99
	Si_3N_4	2.01×10^{-6}	1.76×10^{-12}	1.14×10^{6}	62.99	24.59
	HfO_2	2.01×10^{-6}	3.78×10^{-13}	5.31×10^{6}	61.29	16.03
Dual Gate oxide	SiO_2+Si_3N_4	2.01×10^{-6}	1.18×10^{-12}	1.70×10^{6}	64.65	28.07
	SiO_2+HfO_2	2.01×10^{-6}	1.24×10^{-12}	1.62×10^{6}	62.92	22.23
	Si_3N_4+HfO_2	2.01×10^{-6}	1.07×10^{-13}	1.88×10^{7}	62.74	18.49

Table 3.5 Performance Parameters of DMG JLFinFET with L_G=14nm, F_W=5nm, F_H=20nm

Configuration	Gate oxide	I_{ON} (A)	I_{OFF} (A)	I_{ON}/I_{OFF}	SS (mV/dec)	DIBL (mV/V)
Single Gate oxide	SiO_2	1.60×10^{-6}	2.09×10^{-11}	0.54×10^{6}	69.83	46.60
	Si_3N_4	1.60×10^{-6}	3.12×10^{-12}	1.96×10^{6}	65.48	31.91
	HfO_2	1.60×10^{-6}	5.90×10^{-13}	0.78×10^{7}	63.41	27.11
Dual Gate oxide	SiO_2+Si_3N_4	1.25×10^{-6}	8.26×10^{-12}	1.70×10^{6}	67.75	39.13
	SiO_2+HfO_2	1.60×10^{-6}	3.83×10^{-12}	2.66×10^{6}	65.97	33.53
	Si_3N_4+HfO_2	1.60×10^{-6}	1.29×10^{-12}	1.25×10^{7}	63.18	26.05

Table 3.6 Performance Parameters of DMG JLFinFET with L_G=14nm, F_W=5nm, F_H=10nm

Configuration	Gate oxide	I_{ON} (A)	I_{OFF} (A)	I_{ON}/I_{OFF}	SS (mV/dec)	DIBL (mV/V)
Single Gate oxide	SiO_2	9.90×10^{-7}	7.04×10^{-12}	1.41×10^{5}	68.70	50.84
	Si_3N_4	9.90×10^{-7}	5.79×10^{-13}	1.71×10^{6}	63.58	36.45
	HfO_2	1.02×10^{-6}	1.81×10^{-13}	5.64×10^{6}	63.04	36.45
Dual Gate oxide	SiO_2+Si_3N_4	9.90×10^{-7}	3.07×10^{-12}	3.23×10^{5}	66.49	43.55
	SiO_2+HfO_2	9.90×10^{-7}	1.50×10^{-12}	6.58×10^{5}	64.17	37.51
	Si_3N_4+HfO_2	9.90×10^{-7}	5.79×10^{-13}	1.71×10^{6}	62.57	29.90

Table 3.7 Performance Comparison of Single Metal and Dual Metal Gate JLFinFET

Parameter	**Single Metal Gate JLFinFET**	**Dual Metal Gate JLFinFET**
I_{ON} (A)	3.73x10^{-7}	9.90 x10^{-7}
I_{OFF} (A)	1.01x10^{-12}	5.79 x10^{-13}
SS (mV/dec)	71.92	62.57
DIBL (mV/V)	35.72	29.90

nanoscale devices. The SS and DIBL are computed separately using below equations [110]

$$DIBL(mV/V) = \frac{V_{T1} - V_{T2}}{V_{D1} - V_{D2}} \tag{3.1}$$

$$SS(mV/dec) = \frac{\partial V_{GS}}{\partial log_{10}(I_D)} \tag{3.2}$$

where V_{T1} andbV_{T2} are threshold voltages calculated at V_{D1}=0.05V and V_{D2}=0.8V respectively. From Table 3.2. SS and DIBL are decreased from 72.48 mV/dec to 62.90 mV/dec and 50.56 mV/V to 22.33 mV/V respectively. From Table 3.3 it is evident that SS and DIBL are reduced from 69.83 mV/dec to 62.41 mV/dec and 42.79 mV/V to 19.01 mV/V. We observe that from Table 3.4 SS and DIBL are minimized from 67.35 mV/dec to 62.92 mV/dec and 35.99 mV/V to 16.03 mV/V. The overall comparison from Tables 3.2, 3.3, 3.4 is that by using high-k materials as GS the performance parameters such as I_{ON}/I_{OFF}, SS, and DIBL are improved. Among the different configurations, single gate oxide HfO_2 giving good I_{ON}/I_{OFF} ratio, in dual gate oxide Si_3N_4 +HfO_2 has superior I_{ON}/I_{OFF}.

The I_{ON}/I_{OFF} ratio with F_H variation is shown in tables 3.5, and 3.6. It is observed that in single gate oxide combination HfO_2 is giving good I_{ON}/I_{OFF} ratio. An ameliorated I_{ON}/I_{OFF} ratio observed in dual gate oxide combination Si_3N_4+HfO_2 because increasing the gate dielectric reduces the leakage current thereby increasing I_{ON}/I_{OFF} ratio. The high-k dielectrics increases capacitance between gate and channel so less leakage current thereby improved I_{ON}/I_{OFF}, SS, and DIBL. The electrical performance parameters with L_G=14nm, F_W=5nm, F_H=20nm are shown in Table 3.5. As moving on from single gate oxide to double gate oxide I_{ON}/I_{OFF} ratio was improved to 1.25 x10^7, SS, and DIBL are

Table 3.8 Comparison of proposed device DC parameters with existing results

Ref	**I_{ON}/I_{OFF}**	**SS (mV/dec)**	**DIBL (mV/V)**
[153]	1.82x10^6	68.78	56.03
[135]	7.20x10^3	90.88	76.30
[179]	1.10x10^6	55.28	–
[182]	1.2x10^6	65	60
[Proposed]	1.87x10^7	61.22	22.18

reduced to 63.18 mV/dec, 26.05 mV/V respectively. It is obvious from table 3.6 that, as we are decreasing F_H to 10 nm, I_{ON}/I_{OFF} ratio fall down to 1.71 x10^6, SS, and DIBL 62.57 mV/dec, 29.90 mV/V respectively. Further reduction of fin height creates process complexity. Reducing the F_H is improving the SS but with cost of DIBL. The overall comparison from tables 5, and 6 is that, among all gate oxide combinations Si_3N_3+HfO_2 have better I_{ON}/I_{OFF} ratio and the optimized F_H is 20nm. As Si_3N_4+HfO_2 have better results, comparison is made for this combination. From table 3.7 it is evident that compare to Single Metal Gate JLFinFET, Dual Metal Gate JLFinFET is giving good performance. The comparision of device parameters with existing literature is shown in Table 3.8.

3.4 Conclusions

Comparative analysis of DMG JLFinFET has been done using oxide and work function engineering. The device performance parameters I_{ON}/I_{OFF}, SS, and DIBL are extracted. In single gate oxide HfO_2 gives improved electrical characteristics. In dual gate oxide Si_3N_4+HfO_2 has controlled SCEs due to reduced parasitic capacitances. Further, the same investigations are carried out for F_W variations. At fin width (F_W) of 5nm better I_{ON}/I_{OFF} ratio and SS are obtained with values 1.93 x10^7 and 62.41mV/dec respectively. At 4nm F_W an excellent DIBL value of 16.03mV/V was found. Similarly for fin height (F_H) variations we calculated electrical performance parameters. At lowest F_H 10nm we got good performance in terms of SS but at the cost of DIBL and I_{ON}/I_{OFF}. From work function and gate oxide engineering with all different combinations, the comparative analysis with Si_3N_4+HfO_2 has an excellent electrical performance. Result analysis shows

that proper choosing of device dimensions gives good electrical performance for nanoscale applications.As a continuation of this chapter, the analysis of analog/RF parameters of DMG JL FinFET with fin width and fin height variations will be presented in the next chapter

Chapter 4

Analog and RF Performance Analysis of DMG JLFinFET

4.1 Introduction

MOSFET is one of the device structures which changed the semiconductor industry into more economical but over the years due to continuous scaling the gate loses its control of the channel. With the advancement from micro to nano regime, it is very difficult to control the channel by single gate. The gate controllability in CMOS technologies at sub-nanometre technology decreases due to the short channel effects (SCE's)[20,125]. These SCEs (Subthreshold Swing (SS), Drain Induced Barrier Lowering (DIBL), Vth roll-off, velocity saturation, hot carriers) are the main cause of degrading the device performance. To overcome these SCE's so many structural developments came in literature and FinFET is one of the new structure, but beyond 22nm technology DIBL has adverse effect which can't control by FinFET. As an alternative, multigate devices came into the picture such as double gate, trigate, and gate all around structures [126–128]. Unlike conventional MOSFETs double gate MOSFETS contains two gates, one is the top gate and another is the bottom gate where misalignment [103,119,129] of gates is the main problem. In trigate FinFET the channel is wrapped by the gate on three sides which have effective control of the gate over the channel resulting in the reduction of subthreshold swing (SS) and drain induced barrier lowering (DIBL) [130,131].

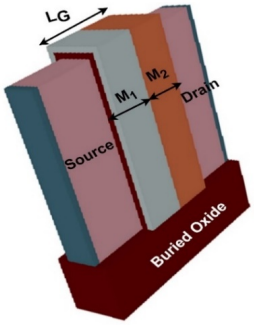
Since 2011, TSMC and Intel adopted FinFETs into their sub-22 nm manufacturing

process as they have well-established fabrication plants. [132–134]. FinFETs are made in two methods, bulk technology and silicon on insulator (SOI) technology [95,135–141]. SOI technology was adopted in this work due to low power consumption, high switching speed, and fewer parasitic capacitances. FinFETs performance further improved by using a high-k gate stack, where leakage current is greatly controllable [109,110,142,143]. However making high-quality junctions is tedious and fabrication is very difficult at sub-22nm, so junction less (JL) transistors came into the picture. For highly scaled devices JLFinFET was proposed [29]. The fabrication of JL transistors is compatible with the CMOS process. High doping is necessary for JL transistors and uniform doping entire silicon region. JL FinFETs are usually in ON mode [19]. A work function with high value fully depletes the channel leading to a complete turn OFF of the device. At present high-k dielectrics are used which show good electrical properties, stability concerning temperature, and quality of interface [144]. The miniaturization of transistor-based systems forced, RF-based blocks into integration as it is cost-effective. Selecting silicon-based designs are a very good choice to implement RF systems. In RF designs cut-off frequency and intrinsic delay are the key parameters where FinFETs show good performance compared to MOSFETs [145].

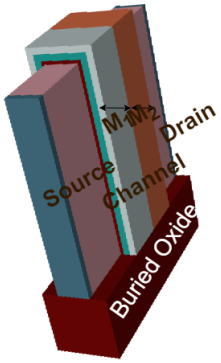
In RF domain FinFETs are potential candidates due to their optimization process techniques like oxide engineering, work function engineering, and metal gate engineering [146]. Linearity is another important metric in RF systems to ensure minimum higher-order harmonics and intermodulation distortion at the system output. Noise is the key parameter for nonlinear distortion in RF wireless systems [147]. To overcome these disadvantages high device performance is needed in terms of linearity, distortion, and transconductance to improving the performance of RF systems [148,149]. In this context linearity, and analog/RF distortion metrics of the junction less transistor are needed. Several works are proposed in the literature on junction less transistors, however, the dimensional effect on linearity and analog/RF parameters of dual material gate junction less FinFET are not yet performed. The chapter is organized as follows: Section 4.2 is device structure and simulation framework, section 4.3 is results and discussions with analog/RF parameters and linearity metrics, the chapter concludes with section 4.4 as conclusion.

4.2 Device Srtructure And Simulation Frame Work

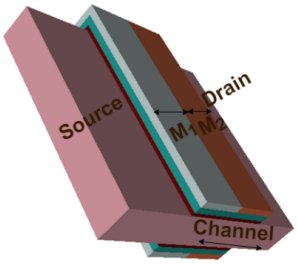
The visual TCAD generated 3D DMG JLFinFET and the 2D structure in X-Y cut are shown in Fig 4.1(a) to 4.1(f) respectively.



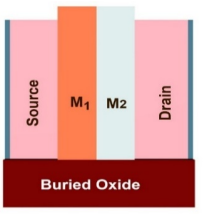
(a) Single gate oxide SiO2



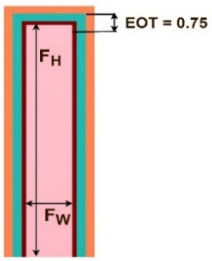
(b) With SiO2 and HfO2 as gate dielectric



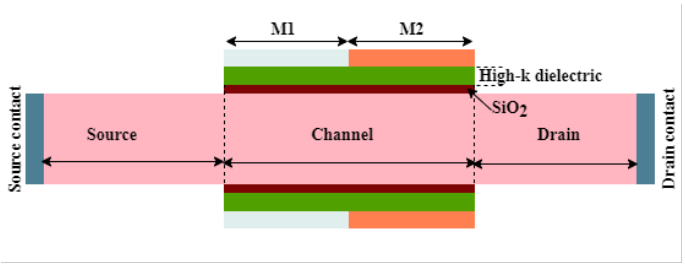
(c) DMG JLFinFET without BOX



(d) Front view of DMG JLFinFET



(e) FH=20nm Fw=5nm with EOT=0.75nm



(f) 2D view of horizontal X-Y cut

Figure 4.1 3D schematic view of DMG JLFinFET

The device dimensions are gate length as 14nm, fin height, and fin width are varied from 10nm to 30nm and 4nm to 6nm respectively. The device parameters used in this

work are depicted in table. The gate stack is made by the combination of high-k materials Si_3N_4 and HfO_2. EOT (Equivalent Oxide Thickness) is 1nm as per IRDS (International Roadmap for Devices and Systems) [8].The simulations are carried out at 300 K using Visual TCAD [150].

The mid-gap metals M1 and M2 are used for gate material with work function 4.9eV and 4.5eV respectively.The metals are titanium and copper respectively. The higher work function metal M1 is placed at the source side lower work function metal M2 is placed at the drain side. The contacts are made with aluminium. The models used in device simulations: drift-diffusion models are used for carrier transport. To observe the generation and recombination phenomena Shockley-Read-Hall (SRH) model is being incorporated. To obtain scattering phenomena Lombardi mobility model is used. This model is also utilized to get the dependency of electric field and surface roughness. As doping concentration is high bandgap narrowing model and band to band tunnelling models are incorporated. To observe the carrier distribution fermi Dirac distribution model was invoked. To estimate the quantum confinement effect quantum model is inserted. We calibrated the experimental data [122] to validate simulation results as shown in Fig 4.2.

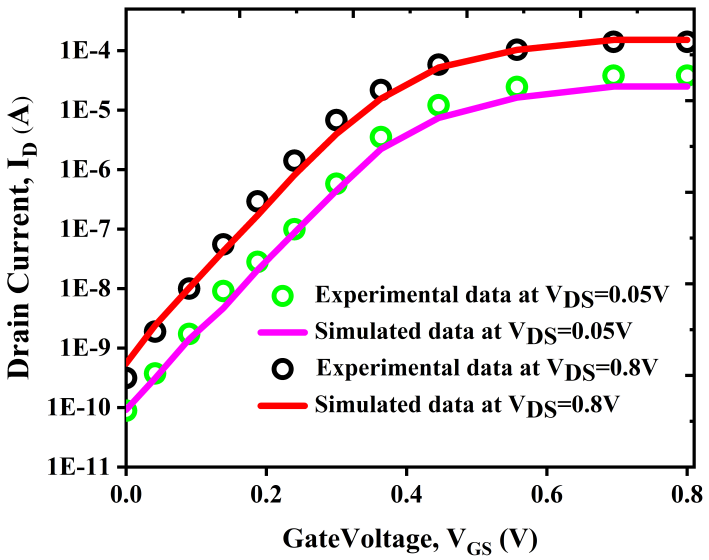


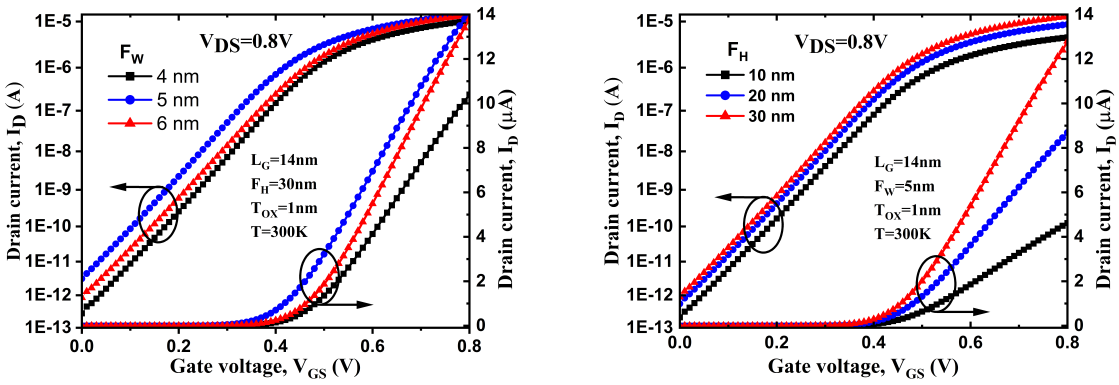
Figure 4.2 Calibration of ID-VGS characteristics of DMG JLFinFET [122]

Table 4.1 Device dimensions and parameters used

Parameter	Value
Gate length (L_G)	14nm
Fin width (F_W)	(4-5) nm
Fin height (F_H)	(10-30) nm
Interfacial Layer SiO_2	0.5nm
High-k dielectric thickness	Variable (Si_3N_4 - 0.96nm, HfO_2 - 3.07nm)
EOT (Equivalent Oxide Thickness)	1nm
Supply Voltage	0.8V
Metal1 Work function (M1)	4.9eV
Metal2 Work function (M2)	4.5eV

4.2.1 Results And Discussion

The drain characteristic of DMG JLFinFET has been plotted for variation in two parameters, the first one with fin width and the second one by fin height. Here we fixed gate length (L_G) = 14nm and varied fin height (F_H) =10nm to 30nm, fin width (F_W) = (4-5) nm. The drain characteristics are plotted in both linear and log scales shown in Fig. 4.3. Fig 4.3(a) and 4.3(b) shows drain characteristics with fin width variation and fin height variation respectively.

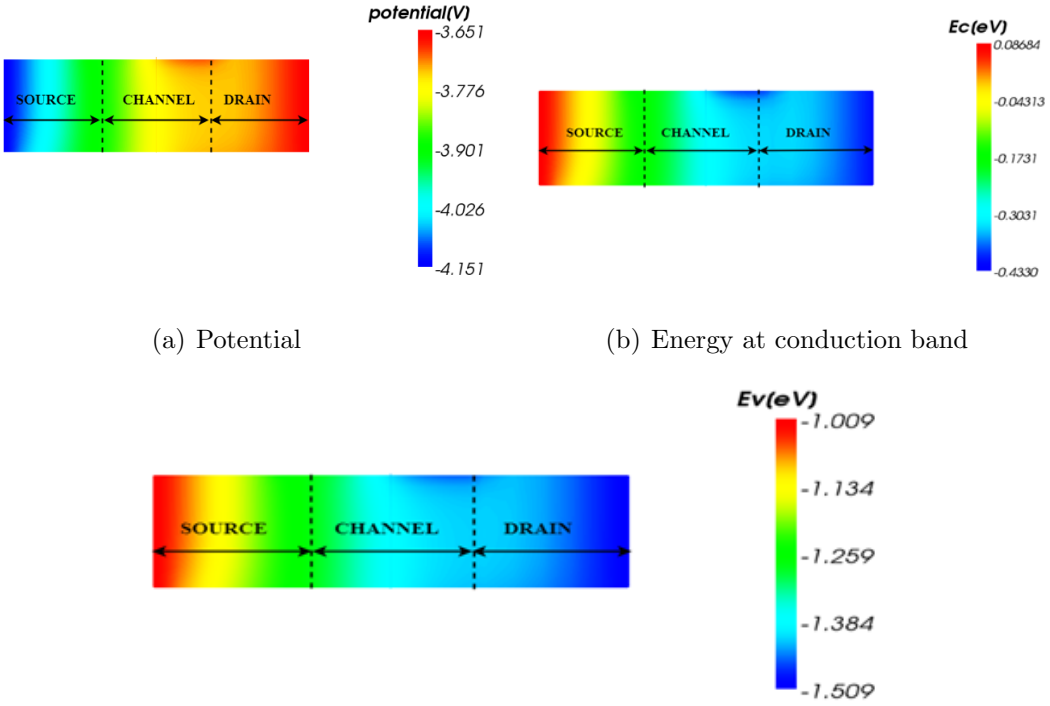


(a) Fin width variation

(b) Fin height variation

Figure 4.3 Drain characteristics

Figure 4.4a shows how the potential distribution is varying from source to drain. The potential is high on the drain side and it's slowly decreasing from channel to source side. Figures 4.4(b) and 4.4(c) show conduction and valence band energies respectively. Here, energy is high at the source end and it becomes low at the drain end as a result of band bending.

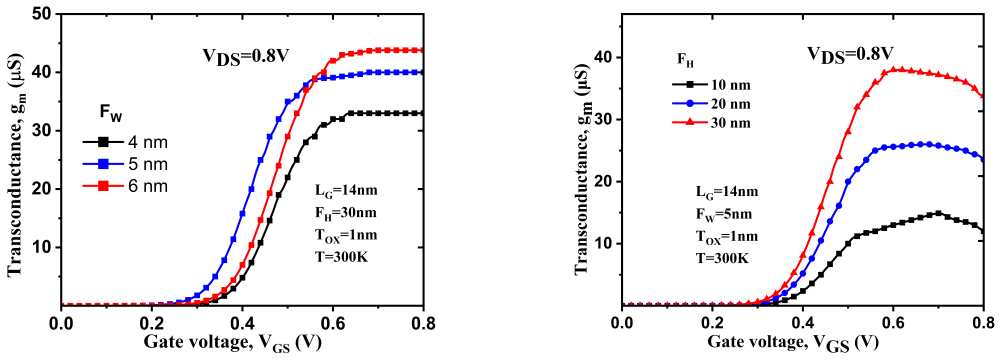


(a) Potential

(b) Energy at conduction band

(c) Energy at valence band for VGS=0.8V, VDS=0.8V

Figure 4.4 Contour plots of DMG JLFinFET



(a) Fin width variation

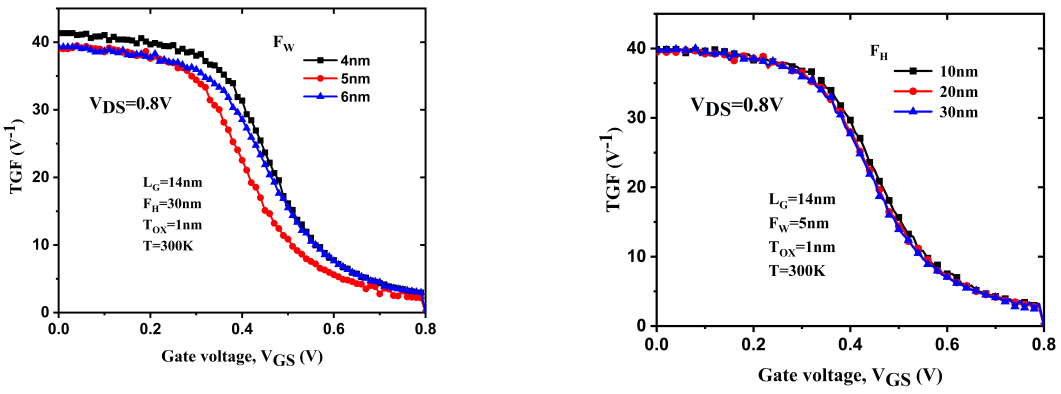
(b) Fin height variation

Figure 4.5 Transconductance

4.2.2 Analog/RF Performance

As the device dimensions are shrinking day by day in integrated circuits and making the systems on single-chip drives to the concept called system on chip (SOC). The SOC is built by using both analog and RF circuits so the study of analog and RF performance metrics is necessary. An essential parameter to evaluate analog performance is transconductance and it is represented as gm, a higher value of gm indicates high-speed operation. The gm is calculated by using the expressions (4.1) [151]

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \tag{4.1}$$



(a) Fin width variation

(b) Fin height variation

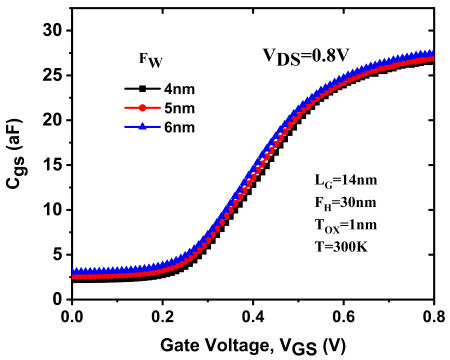
Figure 4.6 TGF

Transconductance generation factor (TGF) is another important parameter to amplify the signal at required power dissipation. The TGF is given by (4.2) [152]

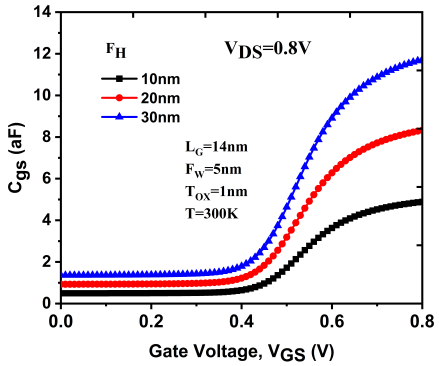
$$TGF = \frac{g_m}{I_D} \tag{4.2}$$

A good gm indicates better TGF and the better TGF gives a good analog performance. A higher value of TGF is required for analog ICs for less linearity distortion and good thermal stability. The minimized coulomb impurity scattering and minimized surface roughness make TGF should below. For RF applications the main key parameters are capacitances encountered between gate and source terminal as well as gate and drain terminal, cut-off frequency, and time delay. To obtain AC small-signal analysis DC voltage of 0.8V with

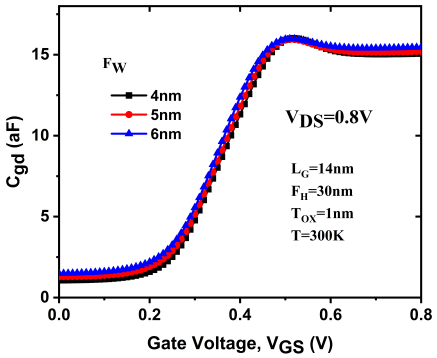
step 0.01V at 1MHz frequency was applied. The capacitance is shown in Fig 4.7. The total gate capacitance constitutes both the source and drain capacitances i.e. $C_{gg} = C_{gs} + C_{gd}$.



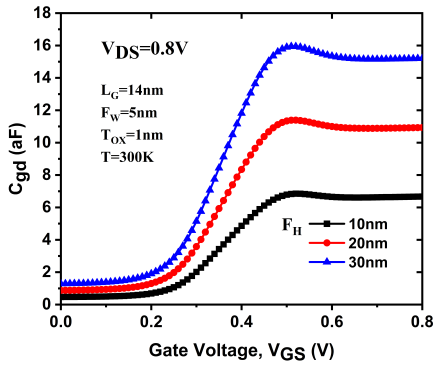
(a) C_{gs} with Fin width variation



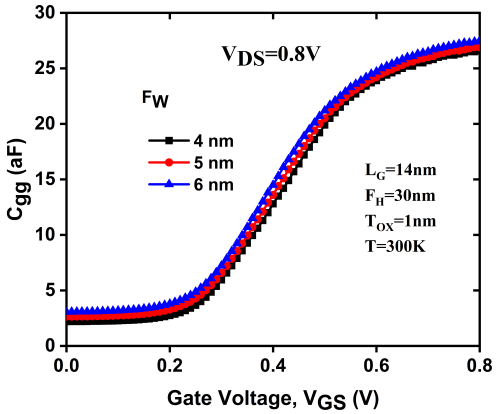
(b) C_{gs} Fin height variation



(c) C_{gd} with Fin width variation



(d) C_{gd} Fin height variation



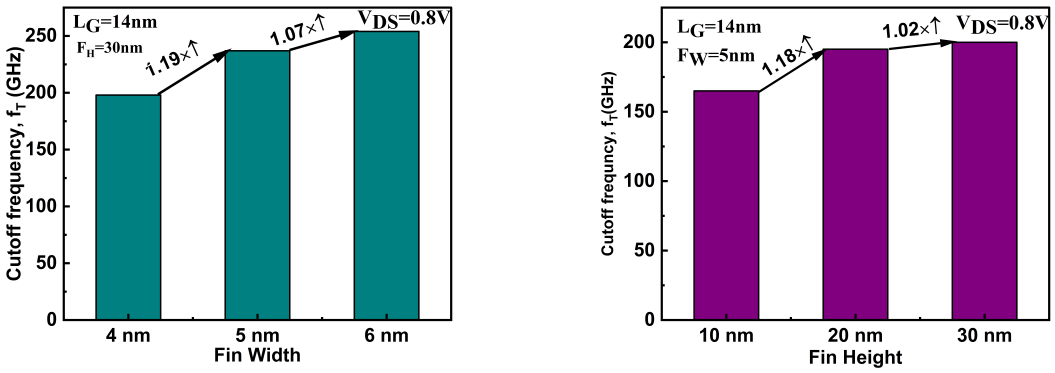
(e) C_{gg} with Fin width variation

Figure 4.7 Effect of Fin width and height variation

Figure 4.7 shows The fin width also affects the effective capacitance but to a smaller extent due to the fact the fin width is changed from 4 to 6 nm as compared to fin height change from 10 to 30 nm. The larger capacitance change observed due to change in fin height could be mainly because of the magnitude of change.

The Cut-off frequency plays an important role to analyze the RF performance of the circuit. It is defined as the frequency at which short-circuit current gain is unity. f_T is given by (4.3) [147]

$$f_T = \frac{g_m}{2\pi(c_{gs} + c_{gd})} \tag{4.3}$$

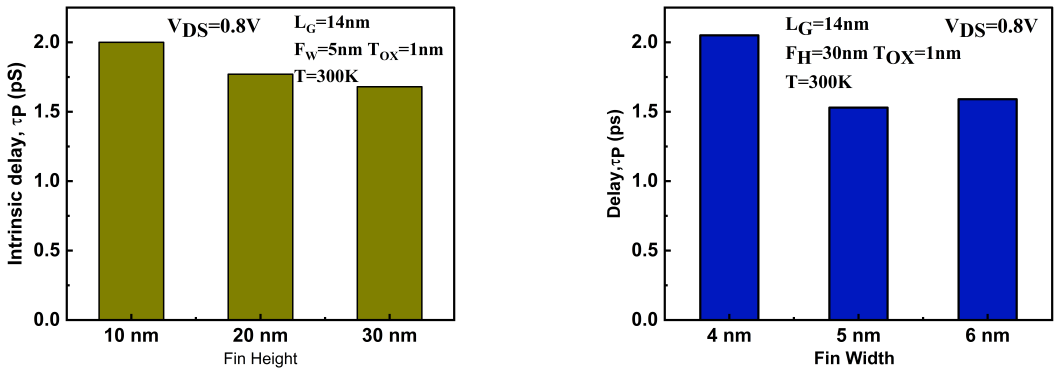


(a) Fin width variation

(b) Fin height variation

Figure 4.8 Cut-off frequency

It is visualized in Fig. 4.8 and it increases with an increase in both fin height and width because with increasing fin height and width gm increases. In F_W variation it's increased by 1.19 times from 4nm to 5nm, 1.07 times from 5nm to 6nm respectively. Similarly for F_H variation 1.18 times from 10nm to 20nm and 1.02 times from 20nm to 30nm respectively.

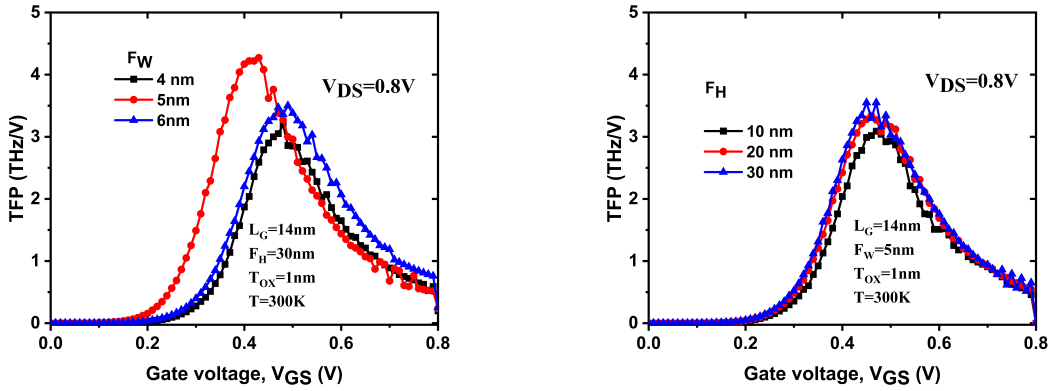


(a) Fin height variation (b) Fin width variation

Figure 4.9 Intrinsic delay

The intrinsic delay is the parameter that specifies the speed of operation. The effect of F_H and F_W variation is shown in Fig 4.9. It is calculated by using the below expression (4.4) [41]

$$\tau = \frac{C_{gg} V_{DD}}{I_{ON}} \tag{4.4}$$



(a) Fin width variation (b) Fin height variation

Figure 4.10 Transconductance frequency product

It varies directly with both V_{DD} and C_{gg} and inversely with I_{ON}. With an increase F_W, C_{gg} increases thereby increasing delay. Compare to F_H variation, F_W variation is more affected delay and the delay is high for F_W=4nm and F_H=10nm. Transconductance

frequency product (TFP) is a significant parameter for high-speed applications (4.5) [152].

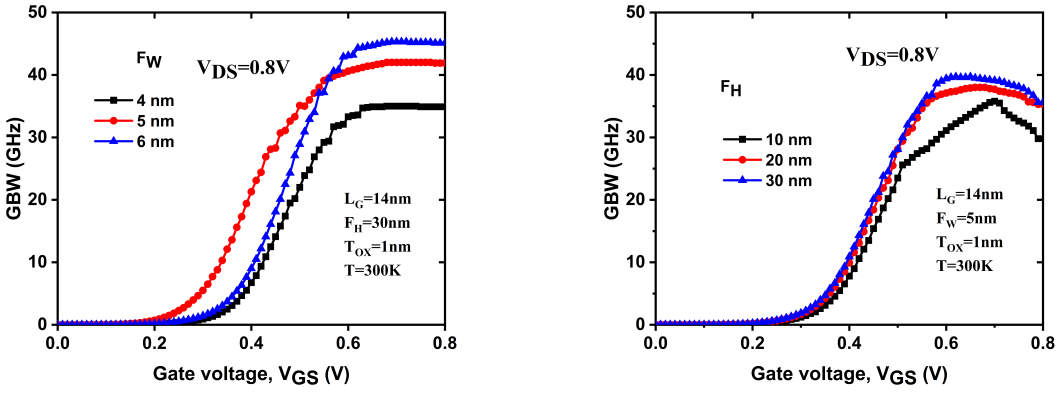
$$TFP = \frac{g_m f_T}{I_D} \tag{4.5}$$

Figure 4.10 shows the impact of F_W and F_H variation on TFP. Here around 0.5V gate voltage Reaches peak value and falls while increasing gate bias, due to mobility degradation.The drain current is higher value for 5nm compared to 4nm and 6nm. As TFP is proportional to drain current TFP is more for 5nm fin width. When the gate voltage increasing i.e., V_{GS} >0.4V the device is saturated, so TFP is lower.

Gain bandwidth product (GBW) is one of the important FOM (Figure of Merit) to evaluate the performance at Radio Frequency. GBW is mathematically calculated using the bellow expression (4.6) [152,153]

$$GBW = \frac{g_m}{2\pi 10 C_{gd}} \tag{4.6}$$

GBW varies directly with g_m and inversely with C_{gd}. Fig 4.11 depicts how the F_W and F_H variation affects GBW. Due to higher increment of C_{gd} and g_m at F_W=6nm, and F_H=30nm the same monotonic increment happens for GBW also.The transconductance is higher value for 5nm compared to 4nm and 6nm for below V_{GS}=0.5V. As GBW is proportional to transconductance, GBW is more for 5nm fin width. When the gate voltage increasing i.e., V_{GS} > 0.5V the transconductance lower so GBW is lower.



(a) Fin width variation

(b) Fin height variation

Figure 4.11 Gain bandwidth product(GBW)

The obtained results are compared with existing literature and shown in Table 4.2

Table 4.2 Comparison of proposed device analog parameters with existing results

Ref	**g_m max (μS)**	**TGF max (V^{-1})**	**C_{gg} (fF)**	**f_t max (GHz)**
[41]	60	–	0.04	150
[151]	35	150	0.024	50
[153]	58	40	0.5	385
[Proposed]	65	68	26	400

4.3 Conclusions

In this chapter, we demonstrated the analog and radio frequency parameter analysis of DMG JLFinFET at a 7nm technology node. The transconductance and transconductance generation factors are good at F_W=6nm and F_H=30nm. The capacitances C_{gs}, C_{gd}, and C_{gg} are extracted. The cut-off frequency is good at F_W=5nm, F_H=20nm, and intrinsic delay is less at F_W=5nm, F_H=30nm.TFP has better values at F_W=5nm and F_H=20nm. GBW is good at F_W=5nm and F_H=30nm. So the proper selection of device dimensions makes the device good behaviour in analog/RF performance. The results show that at the sub-nanometre regime, DMG JLFinFET is a suitable candidate for analog/RF High frequency applications.

The further part of this contribution, i.e., the temperature variability analysis of DMG JL FinFET with analog, RF and linearity parameters analysis will be presented in the next chapter.

Chapter 5

Temperature assessment of Analog/RF and Linearity parameters on DMG JL FinFET

5.1 Introduction

The simulation study of subthreshold characteristics of DMG JL FinFET with DC performence, the analog/RF performance of DMG JL FinFET with fin width and fin height variations have been presented in Chapters 3 and 4, respectively. In this present chapter the temperature variability analysis of DMG JL FinFET was presented.

As depicted in for ITRS (International Technology Roadmap Semiconductor) recent devices of interest are proceeding towards nanoscale regime [154]. However, with reduction in the size of MOSFET, short channel effects (SCEs) such as sub-threshold swing (SS), threshold voltage reduction, channel length modulation, velocity saturation, and hot carrier effects comes into the picture [94]. Electronic domains have such a diverse range of uses, such as car, infrared detectors, military, nuclear, terrestrial systems, space and satellite communication that are extremely temperature dependent [155–157]. However the logic gates, operational amplifiers and static RAM cells are the most important building blocks throughout many applications. CMOS transistors must be scaled to get higher density and performance.

On the other hand, deep scaling effects the performance of CMOS in the form of SCEs. To overcome these problems multi-gate transistors are best options [158,159]. Consequently, FinFET is such a device to control SCEs where the channel is wrapped by

gate in three sides, so gate control is more effective compared to conventional MOSFETs, but making junctions at low technology node is difficult [160]. To overcome these manufacturing challenges, junctionless FinFETs are required at the nano regime. Uniform doping over the silicon fins creates junctionless structures [161]. Due to uniform doping the device behaves as a resistor and the resistivity of the device can be controlled by the gate bias. Furthermore, the technology must be fully depleted in order to fulfill industry requirements and to get the benefits at lower technology nodes. SOI (silicon-on-insulator) is a manufacturing technology that meets all objectives while optimizing the procedure.

In the comparison with other technologies, this does not change the transistor's fundamental dimensions. As the result, we choose DMG JLFinFETs, and also they have smaller parasitic capacitances, consume less power and has higher switching rates [162]. Moreover, in this nano era as the number of transistors on a die is rapidly increasing, the effect of temperature on the characteristics of transistors is main point for consideration with respect to power consumption. To analyse temperature effects so many designs are proposed in the literature. The radiation effect is one of the major considerations while temperature increases rapidly. The temperature variations are extremely sensitive in nanoscale devices and their performance is significantly affected by temperature variation. In the literature survey, a very few designs are investigated with the effect of temperature in the literature to best of authors knowledge.

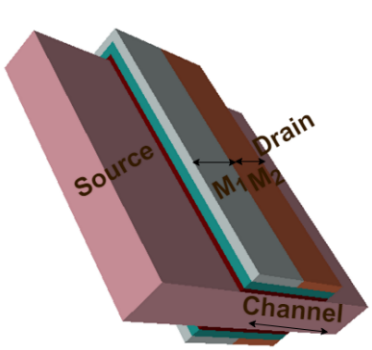
A comparative study of the analog performance, linearity and harmonic distortion characteristics between junctionless (JL) and conventional silicon-on-insulator (SOI) fin-type field-effect transistors (FinFETs) at elevated temperatures (300–500K) is explored in [163]. In [164] the impact of variation in temperature on electrical parameters for a dual material gate (DMG) FinFET reported. In [165] a Study of Negative-Bias Temperature Instability of SOI and Body-Tied FinFETs was reported. Effects of temperature on electrical parameters in GaAs SOI FinFET are studied in [166]. The impact of temperature variation on drain current, gate leakage current, and transconductance from room temperature to high temperature (150 °C) is shown in [167]. A new Germanium based FinFET structure with dual material gate and underlap region between gate region and drain region is shown in [168]. The temperature dependent study of FinFET drain current, through optimization of gate parameters and dielectric material reported in [169]. The

temperature analysis of double gate and ultra-thin SOI transistor is reported in [170,171]. However, with dual material gate (DMG) JLFinFETs, the influence of temperature on radio frequency (RF) performance and linearity metrics has yet to be investigated.

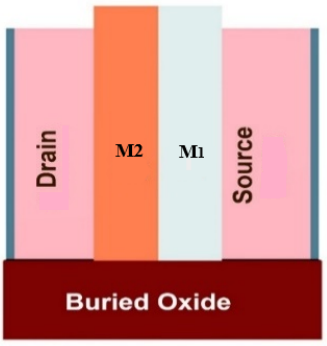
In this work, the influence of temperature on analogue figure of merits of Fin-FET devices such as trans-conductance (g_m), trans-conductance generation factor (g_m/I_D), has been investigated. In addition, we perform several RF characteristics such as gate capacitance (C_{gg}), cut-off frequency (f_T), intrinsic delay, gain frequency product (GFP), and trans-conductance frequency product (TFP). We also examined their variations for different linearity metrics like higher-order derivatives of transconductance (g_{m2}, g_{m3}), voltage intercept point, and 1-dB compression point with operating temperature from 200K to 400K. This chapter is organized as follows: Section 5.2 describes device structure and simulation setup, section 5.3 describes simulated results and discusses the analog/RF performance and linearity metrics and section 5.4 concludes the chapter.

5.2 Device structure and simulation setup

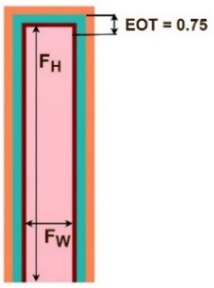
Figure 5.1 (a), 5.1(b) shows a proposed structure of the DMG JLFinFET, and two-dimensional horizontal X-Y cut respectively. In this work, we considered the device dimensions as gate length (L_G) of 14nm, the fin height (F_H) of 30nm and fin width (F_W) of 5nm. Uniform doping is utilized to keep away from junction formation at the nano-scale. Mid-gap metals are employed a as gate materials. M1 has a metal gate work function of 4.9eV, whereas M2 has a work function of 4.5eV and are located on the source and drain sides individually. We used Si_3N_4 and HfO_2 as the gate dielectric materials to make the gate stack. All of the contacts are built by Aluminum. Table 5.1 shows the device dimensions utilized in this investigation. The simulations are being carried out using Visual TCAD tool [150]. As the doping concentration is uniform in entire silicon, the physical models such as doping dependent models and band gap narrowing models are applied. To achieve good accuracy, Fermi Dirac distribution model is used and to determine mobility deterioration, the Lombardi mobility model was applied. The numerical methods of Gummel and Newton are applied to produce good results.



(a) With SiO2 and HfO2 as gate dielectric

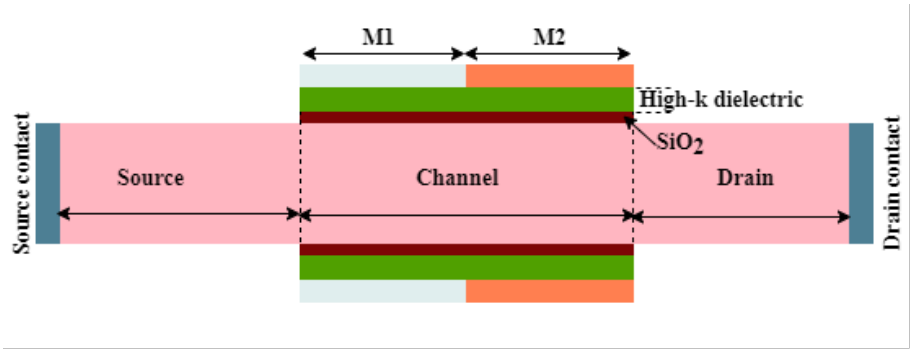


(b) Front view of DMG JLFinFET

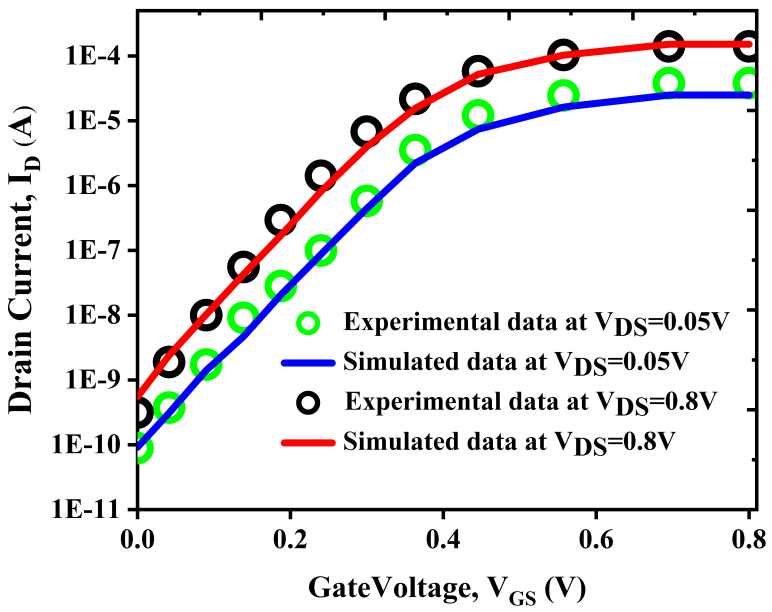


(c) FH=20nm Fw=5nm with EOT=0.75nm

(d) Material



(e) 2D view of horizontal X-Y cut



(f) Calibration with experimental data

Figure 5.1 3D schematic view of DMG JLFinFET

To explain the quantum confinement effect, quantum drift-diffusion model was used. Generation and Recombination effects are being estimated by the SRH model. The experimental data is calibrated [122] as given in Fig 5.1(e) to confirm the simulation model.

Table 5.1 Device parameters used for simulation

Parameter	Value
Gate length (L_G)	14nm
Fin width (F_W)	5nm
Fin height (F_H)	30nm
Interfacial Layer SiO_2	0.5nm
High-k dielectric thickness	Variable (Si_3N_4 - 0.96nm, HfO_2 - 3.07nm)
EOT (Equivalent Oxide Thickness)	1nm
Supply Voltage	0.8V
Metal1 Work function (M1)	4.9eV
Metal2 Work function (M2)	4.5eV

5.3 Simulation results and discussion

5.3.1 Comparison behavior of SMG JLFinFET with DMG JLFinFET

The comparison of drain currents of Single material gate (SMG) and Dual material gate (DMG) Junctionless FinFET shown in above Fig 5.2. Presence of two different work functions [151] in the gate region in DMG reduces the impact of drain bias, which leads to improvement in DIBL effect. The drain characteristics of SMG and DMG are shown in Fig 5.2. It is evident from above figure that improvement of I_{ON} and I_{OFF} is observed for DMG JLFinFET. Furthermore SS and DIBL values obtained for SMG and DMG are 69.83mV/dec,46.60mV/V and 63.27mV/dec, 39.13mV/V respectively. Because of these advantages, an analysis of the effect of temperature on DC, RF/ analog, and linearity have been presented for the DMG JLFinFET.

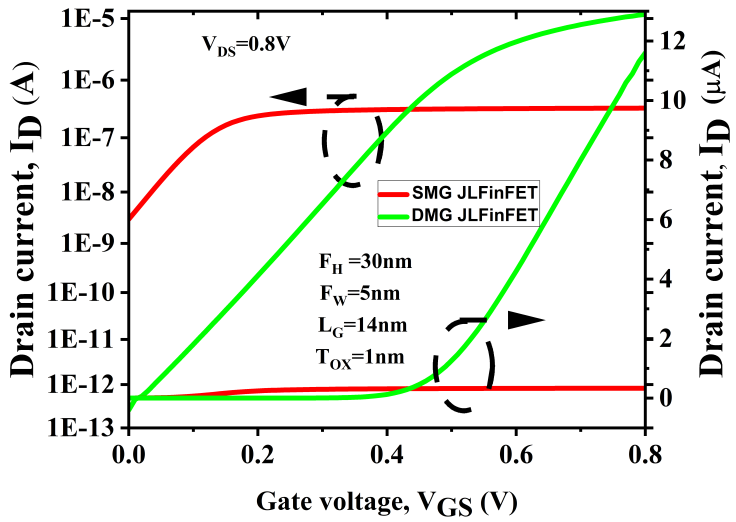


Figure 5.2 Comparison between SMG JLFinFET and DMG JLFinFETs

5.3.2 Impact of Temperature on DC Parameter

DMG JLFinFET transfer characteristics are depicted in Fig 5.3, with log scale, at various temperatures. With temperature, both the OFF-state current (I_{OFF}) and the marginal variation in I_{ON} increases. This rise in I_{OFF} is caused by temperature-dependent processes such as diffusion current and SRH recombination.

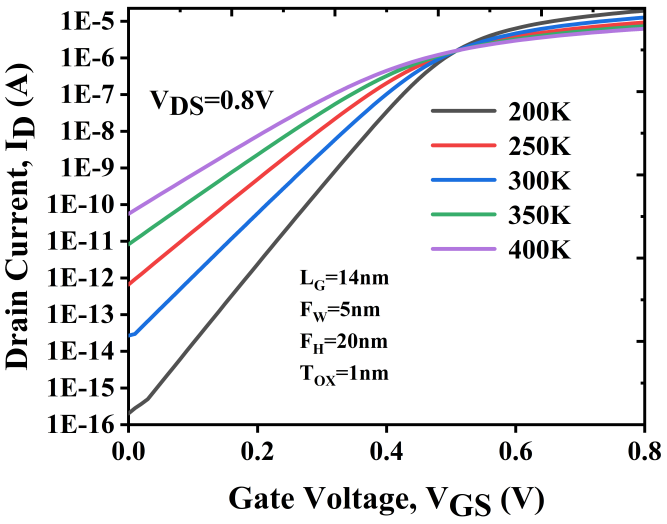


Figure 5.3 Transfer characteristics of DMG JLFinFET with temperature variation

Different physical and transport parameters of MOS devices, such as band-gap, carrier mobility, drift velocity etc., must be accurately calculated to capture temperature variations for accurate and reliable modelling. The empirical relationship between band-gap (E_g) and temperature (T) is given as

$$E_g(T) = E_g(300) - \frac{\alpha T^2}{T + \beta} \tag{5.1}$$

where α=4.73x10^{-4}eV/K, β=636 K, and E_g (300) =1.1 eV are used to calculate (5.1) using measured experimental data for Silicon [172]. The low field mobility model which is extensively used in device simulation [173] is not useful for temperature analysis because it is valid only for room temperature simulation and failed to capture temperature variations. In this work, we have used a mobility model reported in [174] which shows good agreement with measured mobility data and valid for a wide temperature range (up to 673°K). The temperature dependent part of low field mobility is expressed as

$$\mu_L(T) = \mu_{max} \left(\frac{T}{300K} \right)^{-\gamma + c(T/300K)} \tag{5.2}$$

where μ_L(T) is the temperature dependent lattice mobility of Silicon, μ_{max}= 1441cm^{2}V^{-1}S^{-1} is the mobility at T=300°K, γ=2.45 and c=-0.11 are the model parameters used to calculate mobility at higher temperature. We incorporated one mobility degradation model reported in [175] to account for mobility degradation effect due to different scattering phenomena such as Coulomb scattering, phonon scattering and interface roughness scattering. Those mobility components are combined together using Matthiessen's rule denoted as:

$$1/\mu = 1/\mu_{bcs} + 1/\mu_{ac} + 1/\mu_{sr} \tag{5.3}$$

where μ is the effective mobility, μ_{bcs} is the mobility component due to coulomb scattering combined with bulk mobility, μ_{ac} and μ_{sr} are the mobility component due to surface phonon and surface roughness scattering. The intrinsic carrier concentration (n_i) is a temperature-dependent quantity that may be stated mathematically as [163]

$$n_i = exp(-E_g/2kT) \tag{5.4}$$

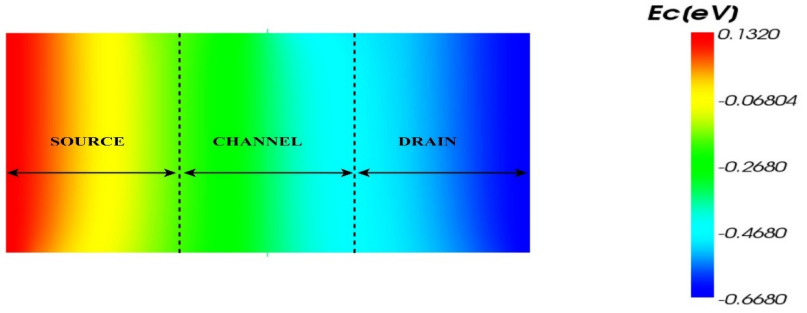
where the absolute temperature is denoted by 'T' and the 'k' denotes Boltzmann constant. From Fig 5.3 it is clear that the temperature change is remarkably negligible at V_{GS}= 0.6 V, which signifies zero temperature coefficient (TC). As the temperature rises, leakage

Table 5.2 Extracted parameters with variation in Temperature

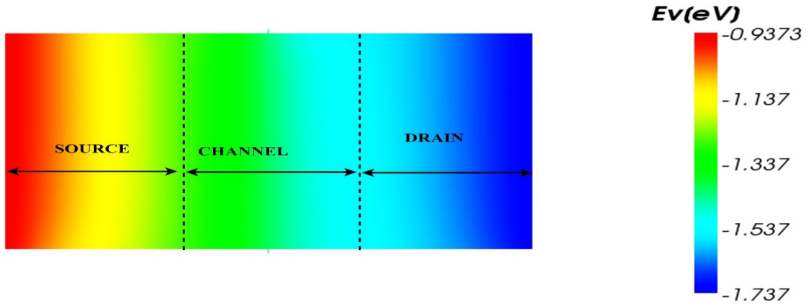
Temperature (K)	**SS (mV/decade)**	**DIBL (mV/V)**	**I_{ON} (A)**	**I_{OFF} (A)**	**Switching Ratio (I_{ON}/I_{OFF})**
200	52.65	68.19	$1.94x10^{-5}$	$7.12x10^{-16}$	$0.27x10^{11}$
250	58.25	72.75	$1.26x10^{-6}$	$6.59x10^{-13}$	$1.41x10^{7}$
300	67.14	87.38	$1.26x10^{-5}$	$2.68x10^{-14}$	$0.47x10^{8}$
350	74.49	108.69	$7.38x10^{-6}$	$8.21x10^{-12}$	$0.89x10^{6}$
400	92.13	136.75	$6.25x10^{-6}$	$5.59x10^{-11}$	$1.11x10^{5}$

current decreases owing to decrease in V_{TH}. However, due to the channel heavy doping in the junction less system, ionized impurity scattering and lattice scattering influences mobility. Mobility varies as $T^{3/2}$, which is being restricted by scattering phenomenon due to presence of ionized impurities [176]. As a result, these impacts partially offset one another to a greater extent. As a result, in the junctionless device the consequent mobility of carriers becomes nearly constant, regardless of temperature [177].It demonstrates I_D increases monotonically with V_{GS}, which is practically temperature dependent for the junctionless device. One key parameter is SS, which is given in terms of temperature in Kelvin as SS=60T/300. As seen in table 5.2, as the temperature rises, the SS rises resulting in a decrease in device performance. DIBL is more affected at 400K and it decreases gradually when device temperature reaches to 200K. I_{ON}/I_{OFF} ratio decreases because I_{OFF} is increasing with temperature but because of the flat band voltage, I_{ON} is relatively constant i.e. when no vertical electrical field is there [178].

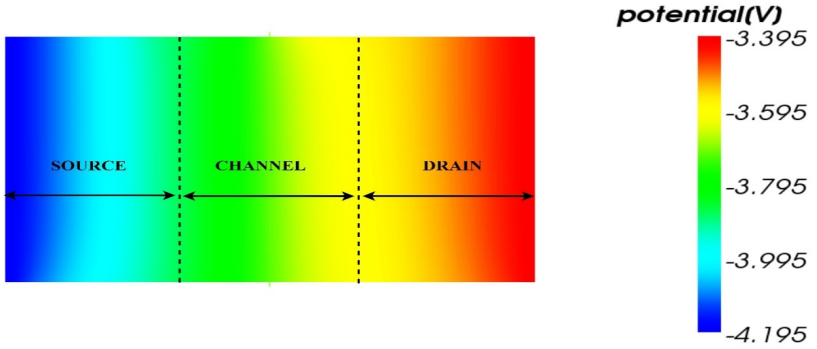
Conduction band and valance band energy contour plots are shown in Fig. 5.4 (a) and 5.4(b) respectively at 400K. Energy is high near the source due to band bending and falls in the channel and drain areas. The potential distribution is shown in Fig. 5.4 (c) which is high at drain side and low at source side, so SCEs are reduced.



(a) Energy of Conduction Band



(b) Energy of Valence Band



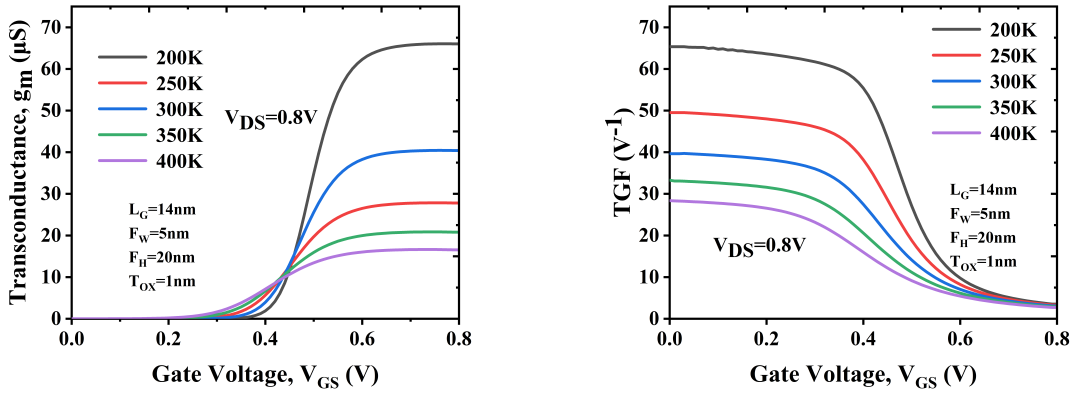
(c) Potential Distribution

Figure 5.4 Contour plots of DMG JLFinFET with VGS=0.8V and VDS=0.8V at 400K in horizontal X-Y cut

Figure 5.4 are contour plots directly taken from tool. The tool is giving in negative format but for calculation we are adding work function to get positive values while calculating the parameters.

5.3.3 Impact of Temperature on Analog/RF Parameter

The g_m is a critical parameter in the design of operational amplifiers. The g_m also specifies an amplifier's bandwidth, DC gain and noise performance. To calculate g_m, use the mathematical expression gm= I_D/V_{GS} [138] keeping V_{DS} as constant. The temperature variability of transconductance (g_m) is related to gate bias as shown in Fig 5.5(a). When the temperature drops, the g_m value rises due to an increase in drain current. The g_m is increased in the weak inversion area, and it diminishes as gate bias increases, because of reduced mobility. At 200K, the g_m reaches its highest peak value of 65µS, and as the temperature rises, the g_m decreases as a result of fall in I_D. At lower temperatures improvement of g_m is owing to increased conduction band energy and also improves the device's gain. The g_m depicts a minimal increase with temperature for DMG JLFinFETs.



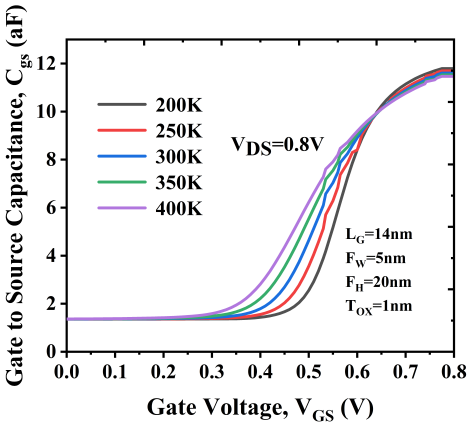
(a) g_m (b) TGF with temperature variation

Figure 5.5 DMG JLFinFET analog/RF characteristics

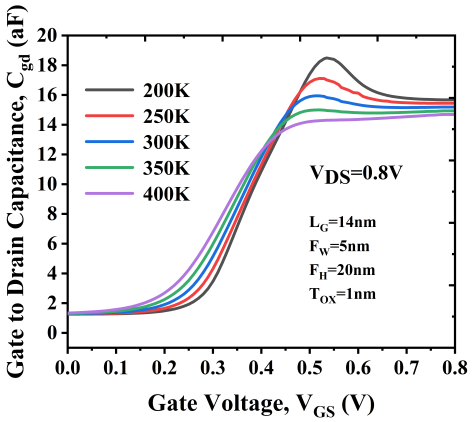
The TGF (Transconductance Generation Factor) is the device property that transforms direct current (DC) power to alternating current (AC). The TGF of a device is proportional to its g_m, a higher TGF for a device indicates strong analog/RF performance. TGF is determined using the equation TGF = g_m/I_D [179]. The change in TGF with V_{GS} is shown in Fig 5.5(b). The TGF value rises as the temperature falls and falls as the temperature rises. The g_m/I_D ratio improves in the weak inversion zone because the decrease in I_D is larger than the increase in g_m with temperature. Furthermore, Temperature has minor influence on TGF, as expected with increased V_{GS}. In the subthreshold

area, a device's capacitance is low, and in the inversion zone, it steadily rises. Gate-to-source capacitance (C_{gs}) and gate-to-drain capacitance (C_{gd}) both increase when the temperature value increases because on both source and drain sides where gate generated fringing fields boost the associated charges.

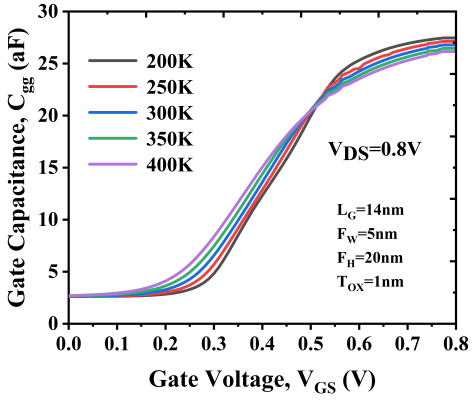
At V_{DS}=0.8V, Fig. 5.6 (a) and 5.6(b) demonstrates the effect of V_{GS} variation on C_{gs} and C_{gd}. With high temperatures, the device shows increased C_{gs} and C_{gd}. The gate capacitance (C_{gg}) is the sum of the capacitances at the drain and source terminals i.e C_{gg}= C_{gs} + C_{gd} [135]. Fig. 5.6 (c) depicts the response of C_{gg} to various temperatures as a function of V_{GS}.



(a) Gate to source capacitance (Cgs)



(b) Gate to drain capacitance (Cgd)



(c) Total gate capacitance (Cgg)

Figure 5.6 The temperature effect

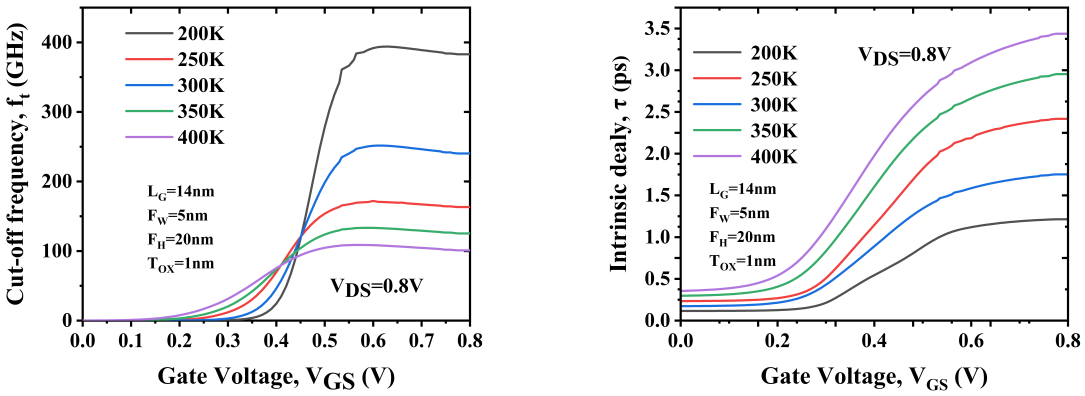
The results show that when the temperature rises, the C_{gg} values rises, because increase in temperature lowers the energy barrier, which concurrently raises the channel

charge carriers under gate area , so total gate Capacitance increases [164].Please note that in Fig. 5.6(c), the C_{gg} decreases with temperature after $V_{GS} = 0.5V$. The cut-off frequency (f_T) is determined by unity short-circuit gain. Fig 5.7 (a) show the effect of temperature on f_T. The value of f_T is increasing with decrease in temperature due to C_{gg} is decreasing and g_m increasing with decrease in temperature only for $V_{GS} > 0.45$ V [180].

$$f_T = \frac{g_m}{2\pi(c_{gs} + c_{gd})} \tag{5.5}$$

Intrinsic delay (τ) is a critical metric that indicates the device's speed. Figure 5.7(b) depicts the temperature dependency of intrinsic delay. It is directly proportional to C_{gg} and inversely proportional to I_{ON} [181]. As the temperature rises, C_{gg} rises and I_{ON} falls therefore increasing the intrinsic delay.

$$\tau = \frac{C_{gg} V_{DD}}{I_{ON}} \tag{5.6}$$



(a) Cut-off frequency

(b) Intrinsic delay

Figure 5.7 Impact of temperature

For high-speed applications, the transconductance frequency product (TFP) is an important metric. It is calculated as:

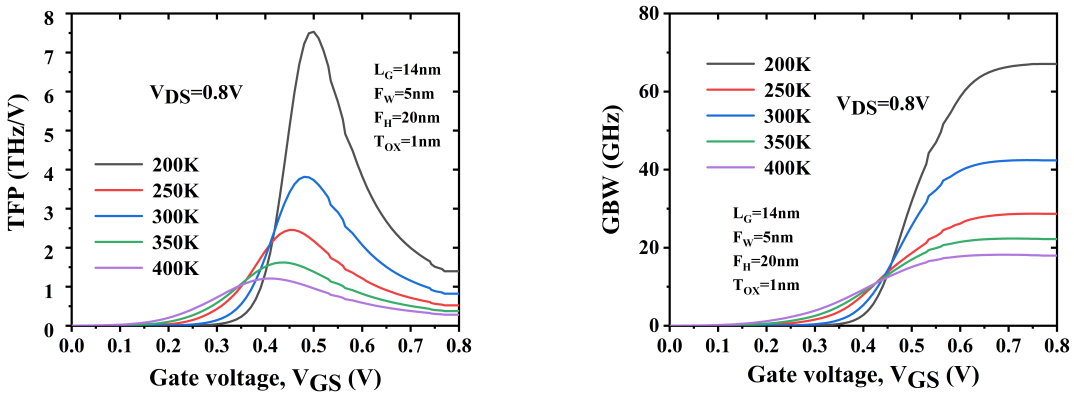
$$TFP = \frac{g_m f_T}{I_D} \tag{5.7}$$

Figure 5.8 (a) depicts the influence of temperature on TFP. TFP, like f_T and g_m, increases when the temperature drops. TFP is found to be elevated at low temperatures due to

mobility degradation. The gain bandwidth product (GBW) is a metric that is used to assess a device's performance at high frequencies. The formula for GBW is as follows

$$GBW = \frac{g_m}{2\pi 10 C_{gd}} \tag{5.8}$$

As depicted in Fig 5.8 (b), it is observed that GBW is high at low temperature and low at higher temperature. A higher value of GBW indicates good performance of the device [182].



(a) TFP (b) GBW

Figure 5.8 The change with the variation of temperature

The obtained results are compared with existing literature and shown in Table 5.3

Table 5.3 Comparison of proposed device analog parameters while varying temperature with existing results

Ref	g_m max (μS)	TGF max (V^{-1})	C_{gg} (fF)	f_t max (GHz)	GBW (GHz)
[138]	12	–	0.08	5	0.79
[179]	6.11	–	4.5	2.51	0.86
[180]	56.29	24.36	24.5	290.4	82.17
[182]	27.5	27	0.6	50	–
[Proposed]	65	68	26	400	65

5.3.4 Impact of Temperature on Linearity Parameter

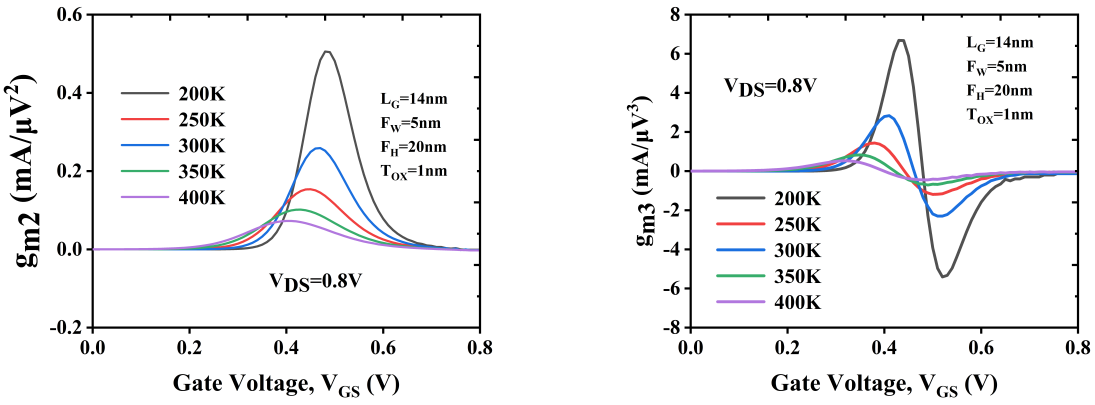
Linearity metric is critical in RF applications and also various mobile communication systems applications. In communication systems, harmonic distortion is a problem, and knowing the effects of higher order harmonics is crucial. Generally, the value of g_{m2} and g_{m3} are calculated as: [152]

$$g_{m2} = \frac{\partial^2 I_D}{\partial V_{GS}^2} \tag{5.9}$$

$$g_{m3} = \frac{\partial^3 I_D}{\partial V_{GS}^3} \tag{5.10}$$

Lower distortion at the output terminals is critical for improved linearity performance. For enhanced linearity, with respect to V_{GS}, transconductance should be constant. Because FinFETs exhibit nonlinearity as a result of mobility deterioration, it's important to investigate the device's behavior at various voltages. As illustrated in Fig. 5.9 (a) and 5.9(b), the second order transconductance coefficient (g_{m2}) and third order transconductance coefficient (g_{m3}) are higher order derivatives of I_D with respect to V_{GS} and can be used to evaluate device nonlinearity.

To get the optimal direct current for a device, use the early zero-crossing point (ZCP) of g_{m2} and g_{m3} in a circuit. The negative peaks in g_{m3} are caused by mobility degradation when gate bias increases. The ZCP, which should be as low as feasible, also shows the biasing voltage's optimal suitability. Because of the less amplitude harmonics at high V_{GS} and early ZCP, it proves its advantage in producing better linearity, demonstrating its acceleration to flatness.



(a) gm2 with various temperatures

(b) gm3 with various temperatures

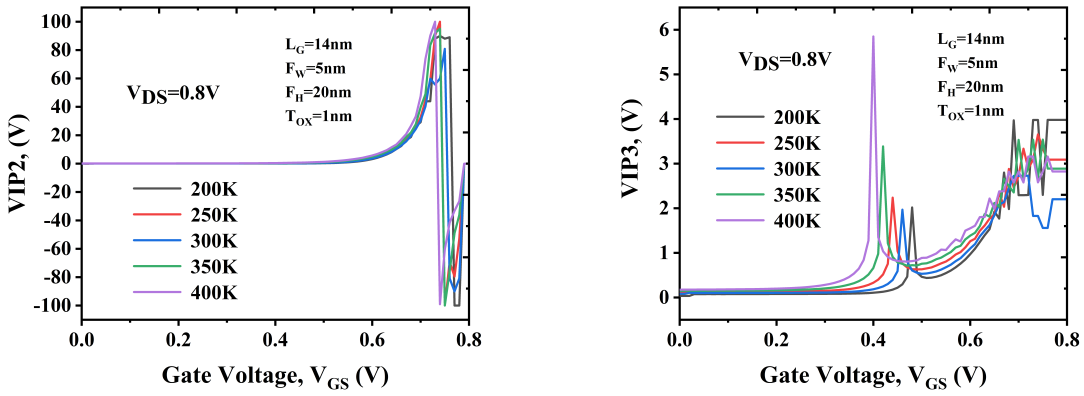
Figure 5.9 The variation of on higher-order harmonics

The g_{m3} has a negative peak and a positive peak, as seen in Fig 5.9 (b). Because g_{m3} is a derivative of g_{m2}, the device produces a negative peak for g_{m3} at the ZCP of g_{m2} and a 2nd positive peak for g_{m3} at the same V_{GS}. Because device features are reaching saturation at high V_{GS}, the peak of g_{m3} is greater in magnitude compared to g_{m2}. Although a balanced modulator [152] can reduce g_{m2}, g_{m3} is more harmful and is the source of distortion in device analysis. The second and third-order voltage intercept points VIP2 and VIP3 are represented by the equations [183].

$$VIP2 = 4\left(\frac{g_m}{g_{m2}}\right) \tag{5.11}$$

$$VIP3 = \sqrt{24\left(\frac{g_m}{g_{m3}}\right)} \tag{5.12}$$

The voltage intercept points VIP2 and VIP3 are, where the fundamental tone amplitude meets 2nd and 3rd order harmonics, and both VIP2 and VIP3 have the units of Volt. The VIP2 and VIP3 with more amplitude have better linearity and less distortion. The transconductance and carrier velocity of the device are likewise affected by the VIP2 and VIP3 parameters. According to Fig 5.10 (a) and 5.10 (b), at high temperature greater amplitudes for both VIP2 and VIP3, indicating stronger linearity and less distortion. The input power where first and third-order harmonic powers are equal, is defined as third-order power intercept point (IIP3).



(a) VIP2 at V_{DS} =0.8 V

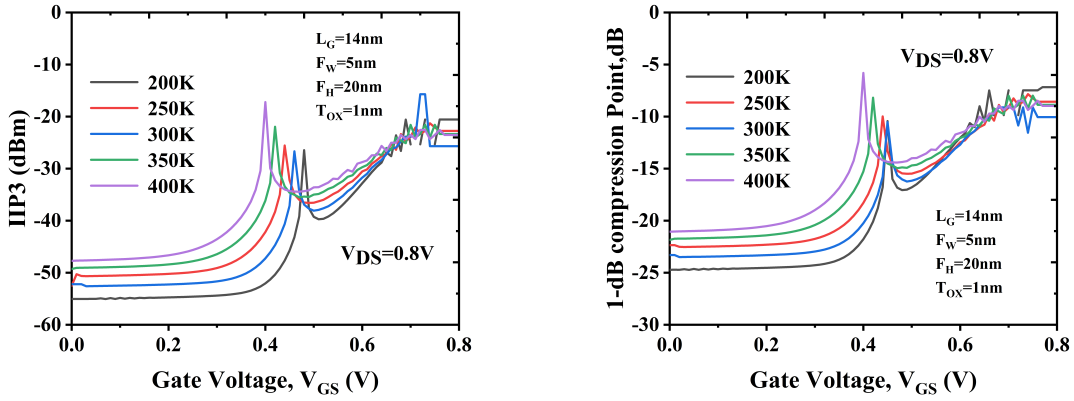
(b) VIP3 at VDS =0.8 V

Figure 5.10 The temperature dependency on Voltage Intercept Points

The IIP3 with series resistance fixed to 50Ω given as

$$IIP3 = \frac{2}{3}\left(\frac{g_m}{g_{m3}R_s}\right) \tag{5.13}$$

A higher IIP3 indicates more linearity. The effect of temperature on IIP3 is shown in Fig 5.11(a). From Fig 5.11(b), it is evident that at 400K temperature, 1-dB compression point rises quickly to reach its peak amongst all temperature combinations, which shows its higher linearity i.e. input power and output power are proportional to each other as same as VIP3, and thus 400K exhibits strong linearity and minimal distortion.



(a) third-order power intercept point (IIP3) at VDS=0.8 V

(b) 1-dB Compression Point at VDS =0.8 V

Figure 5.11 The temperature dependency

A higher peak value with increased temperature i.e. at 400K with -25dBm shows that linearity is improved with increasing temperature. The 1-dB compression point is a significant FOM for determining the maximum limit for linear operation. The 1-dB compression point is defined as the point where input power changes 1-dB from linearity as compared to output power. The 1-dB compression point is calculated as [164].

$$1 - dBcompressionpoint = 0.22\sqrt{\frac{g_m}{g_{m3}}} \tag{5.14}$$

Table 5.4 Summary performance of DMG JLFinFET in the comparison with T=300K

Parameter	**200K**	**250K**	**350K**	**400K**
I_D (A)	6.8↑	3.34↑	5.22↓	6.35↓
DIBL (mV/V)	19.19↑	14.63↑	21.31↑	49.37↑
SS (mV/decade)	12↓	11↓	13↑	21↑
V_t (V)	0.06↑	0.03↑	0.01↓	0.02↓
g_m max (µS)	0.26↑	0.13↑	0.07↓	0.1↓
TGF max (V^{-1})	12↑	5↑	6↓	18↑
f_t max (THz)	2.51↓	2.35↓	2.49↓	2.49↓
Delay (fsec)	0.6↓	0.7↑	1.2↑	1.6↑
GBW max (GHz)	24.7↑	19.53↓	20.1↑	24.2↑
TFP max (THz)	3.53↑	1.5↑	2.5↓	3↓
g_{m2} max (mA/V^2)	0.2↑	0.12↑	0.18↑	0.25↑
g_{m2} min ((mA/V^2))	0.7↑	0.3↑	0.1↓	0.5↓
g_{m3} max (mA/V^2)	4↑	1.8↑	2.25↓	2.99↓
g_{m3} min (mA/V^2)	3↓	1.8	2.96↓	2.95↓
VIP2 max (V)	20↑	40↑	30↑	40↑
VIP2 min (V)	20↑	10↑	30↑	30↑
VIP3 max (V)	1.1↑	0.2↑	1.2↑	4.1↑
IIP 3 max (dBm)	7.63↑	1.71↑	4.93↓	6.5↓
IIP 3 min (dBm)	11.16↑	13.62↑	5.88↑	7.22↑
1db-compression max (dB)	0.41↑	0.06↑	2.46↓	3.25↓

The performance and their variations with temperatures (200K to 400K) are compared with 300K temperature and shown in table 3. We observed that with increasing the temperature, DC parameters like drain current and threshold voltage are decreasing while SS and DIBL are increasing. The analog parameters g_m, f_T, GBW are decreased whereas delay and TFP increased. The linearity parameters g_{m2}, VIP2, VIP3 and IIP3 are increased while g_{m3} and 1-dB compression point are decreased. The obtained results are compared with existing literature and shown in Table 5.5

Table 5.5 Comparison of proposed device linear parameters with existing results

Ref	g_{m2} (mA/V^2)	g_{m3} (mA/V^2)	VIP2 (V)	VIP3 (V)	IIP3 (dBm)	1-dB Compression point (dB)
[152]	0.03	0.05	0.5	8	3	5
[153]	4	4	12	3	10	3
[164]	0.9	5	4	2.5	18	10
[183]	1	7.8	50	3	3	–
[Proposed]	0.2	2	80	4	20	10

5.4 Conclusion

In this work, the temperature analysis of DC, analog/RF and linearity metrics in DMG JLFinFET are carried out using TCAD tool. Results show SS and DIBL increasing, I_{ON}/I_{OFF} is decreasing when increased temperature. Analog/RF properties such as transconductance (g_m) and TGF are decreasing, while C_{gs} and C_{gd} are increasing with increased temperature. The total gate capacitance is monotonically increased with increasing temperature. The cut-off frequency, TFP, GBW are decreasing, on the other hand intrinsic delay is increasing with increase in temperature. The analog/RF properties of DMG JLFinFET are minimally temperature dependent. The higher order harmonics g_{m2} and g_{m3} have high values at 200K temperature. On the contrary, the voltage intercept points VIP2 and VIP3 have high values at 400K temperature. On overall, the linearity parameters achieved superior performance. From the above results we conclude that the temperature dependence has a substantial impact on analog/RF parameters and linearity metrics of DMG JLFinFET, and the study reveals that this device is a potential candidate for nano scale applications in Analog/RF domain.

Chapter 6

Conclusion and Future scope

6.1 Conclusions

The thesis mainly reports on the simulation of subthreshold characteristics DMG JL FinFET. Initially, calibration of 10nm FinFET was done. A detailed analysis has been performed on DMG JL FinFET to explore the effects of various device parameters on the potential, electric field, Ion, Ioff, Ion/Ioff, DIBL, subthreshold current and swing. From the proposed model, Ion/Ioff, subthreshold swing and DIBL is improved. The detailed Anlog and RF performance analysis was done with dimensional effects and with temperature variations by selecting optimum values of fin height (FH) and fin width (FW) and using the DMG structure with GS engineering.

It is observed that DMG JL FinFET has better immunity against SCEs and HCEs compare to SMG JL FinFET. The structure has been validated using TCAD and the results are observed to be in good agreement with those from the experimental data.

Oxide and work function engineering have been used to analyze DMG JLFinFET designs. HfO2 provides enhanced electrical properties in single gate oxide. Due to lower parasitic capacitances, Si3N4+HfO2 has controlled SCEs in dual gate oxide. Additionally, the same study is done for FW variations. Ion/Ioff ratio and SS are improved at a fin width (FW) of 5 nm, with values of 1.93 x 107 and 62.41 mV/dec, respectively. An excellent DIBL value of 16.03mV/V was found at 4nm FW. At the lowest FH 10nm, we achieved good SS performance at the expense of DIBL and Ion/Ioff. The study of the results

reveals that selecting device dimensions properly results in high electrical performance for nanoscale applications.

The analog/RF performance analysis of proposed DMG JLFinFET with dimensional effect has been evaluated using the TCAD simulator. From the result analysis, it has been concluded that the proposed DMG JLFinFET has better analog/RF performance. The transconductance and transconductance generation factors are good at FW=6nm and FH=30nm. The capacitances Cgs, Cgd, and Cgg are extracted. The cut-off frequency is good at FW=5nm, FH=20nm, and intrinsic delay is less at FW=5nm, FH=30nm.TFP has better values at FW=5nm and FH=20nm. GBW is good at FW=5nm and FH=30nm. So the proper selection of device dimensions makes the device good behavior in analog/RF performance. Moreover, the analog/RF performance of DMG JLFinFET is improved by using the DMG structure with the GS engineering technique.

DC, analog/RF, and linearity metric temperature analyses for DMG JLFinFET are done. The results indicate that when the temperature rises, SS and DIBL increase while ION/IOFF decrease. As temperature rises, Cgs and Cgd increase while analog/RF properties like transconductance (gm) and TGF decrease. As the temperature rises, the overall gate capacitance increases monotonically. While the inherent delay is growing with a rise in temperature, the cut-off frequency, TFP, and GBW are all decreasing. Temperature has a negligible impact on the analog/RF characteristics of DMG JLFinFET. At a temperature of 200K, the higher order harmonics gm2 and gm3 exhibit large values. In contrast, at 400 K, the voltage intercept points VIP2 and VIP3 have large values.

6.2 Future Scope

This thesis presents the simulation of DMG JL FinFET subthreshold characteristics. The following are other areas in which this work can be extended.

• By using negative capacitance concept in DMG JL FinFET the performance analysis have to be studied.

• The characteristics of DMG JL FinFET below 7nm node have to study.

• DMG JL FinFETs are expected to continue scaling down to smaller technology nodes, such as 7nm, 5nm, and beyond.

• The radiation problems of DMG JL FinFET have to be studied.

• The fin variation effects of DMG JL FinFET need to be studied.

• Researchers and industry players are exploring novel materials to enhance the performance of DMG JL FinFETs. This includes investigating alternative channel materials (e.g., germanium, III-V compounds) and new dielectric materials with higher dielectric constant (high-k) to further enhance device performance and reduce power consumption.

Publications

List of International Journals:

1. Rambabu Kusuma and TVK Hanumantha Rao, "Design and Optimization of Dual Material Gate Junctionless FinFET Using Dimensional Effect, Gate Oxide and Work function Engineering at 7 nm Technology Node," *Silicon*, Volume 14, issue 16, November 2022. **(SCI-Indexed, Springer)**

2. Rambabu Kusuma and TVK Hanumantha Rao, "Study of DMG JL FinFET: Analog/RF Perspective at 7nm Technology Node" *High Technology Letters*, Volume 28, Issue X, 2022. **(SCOPUS)**

3. Rambabu Kusuma and TVK Hanumantha Rao, "Design and Temperature assessment of Analog/RF and Linearity parameters on Dual Material Gate Junctionless FinFET at 7nm Technology node for nano scale Applications", *Journal of Circuits, Systems and Computers*. **(SCI-Indexed - Under Review)**

4. Rambabu Kusuma and TVK Hanumantha Rao, "Impact of high-k gate dielectric on analog and RF performance of nanoscale Dual Material Gate Junctionless FinFET at 7nm Technology Node", *Electronic Materials Letters*. **(SCI-Indexed - Under Review)**

List of International Conferences:

1. Rambabu Kusuma and TVK Hanumantha Rao, "Recent Trends in FinFET Technology: A Review," in *IC2SV2019, IEEE, NIT Warangal.*

2. Rambabu Kusuma and TVK Hanumantha Rao, "Performance analysis of FinFET using gate stack and work function Engineering in 14 nm technology," in *IEEE 2nd International Conference of emerging technologies 2021, India.*

Patents:

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1. Design and Optimization of Dual Material Gate Junctionless FinFET to reduce SS and DIBL for high switching speed applications at 7nm Technology Node," Patent application no: 202241066584 A. Published on: 25/11/2022

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