DEVELOPMENT OF QUASI Z-SOURCE BASED MULTILEVEL INVERTERS FOR PHOTOVOLTAIC APPLICATIONS WITH LOW LEAKAGE CURRENT

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Electrical Engineering

By

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CERTIFICATE

This is to certify that the work presented in the thesis entitled **Development of Quasi Z-Source based Multilevel Inverters for Photovoltaic Applications with Low Leakage Current** which is being submitted by **Chinmay Kumar Das (Roll no. 719033),** is a bonafide work submitted to National Institute of Technology Warangal in partial fulfilment of the requirement for the award of the degree Doctor of Philosophy in Department of Electrical Engineering. To best of my knowledge the work incorporated in this thesis has not been submitted elsewhere for award of any degree.

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DECLARATION

This is to certify that the work presented in the thesis entitled **Development of Quasi Z-Source based Multilevel Inverters for Photovoltaic Applications with Low Leakage Current** is a bonafide work done by me under the supervision of **Dr. A. Kirubakaran,** Associate Professor, Department of Electrical Engineering National Institute of Technology Warangal and was not submitted elsewhere for the award of any degree.

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ABSTRACT

Contemporary research is directed towards the promotion of Renewable Energy Sources (RES) to counter the harmful effects of fossil fuels. Solar Photovoltaic (PV), Wind, and Fuel cell are some of the popular RESs to generate clean power. PV power has seen a huge growth in terms of installation capacity in the last decade due to availability and decreasing production cost. With a worldwide installed capacity of 710GW and having a growth rate of 24% in 2021, it is poised to become the major source of energy in the foreseeable future. However, the main drawback of PV systems is that they produce DC power, requiring a power conversion system to convert it into AC form, either to be consumed in standalone networks or to inject generated power into the grid. Therefore, development of power electronic interface plays a vital role for standalone/grid connected photovoltaic operations.

This is achieved by traditional two-level inverters either with direct DC/AC single-stage operation or in combination of front-end DC/DC boost converter cascaded with DC/AC inverter i.e., two-stage operations for PV applications. Contemporary, multilevel inverters (MLIs) have often accomplished this objective in the past few decades due to (1) operability of high DC input voltages with power semiconductor switching devices of low-voltage ratings, (2) low total harmonic distortion in the output voltage, (3) low filter requirements for grid interfacing, and (4) lower electromagnetic interference. Numerous topologies have been reported in the literature pertaining to MLIs of which generic topologies of MLI's are mainly divided into three categories, namely: (a) neutral point clamped (NPC-MLI), (b) flying capacitor (FC-MLI), and (c) cascaded H-bridge (CHB-MLI); the rest of the topologies are derived from three basic configurations. All of these inverters have a common drawback in that, they all belong to the "buck" category. Consequently, they require a large number of PV panels to be connected in series and parallel to obtain the required power at the required voltage level. In the past, two-stage topologies have been suggested to circumvent this problem. These systems display a good maximum power point tracking (MPPT) capability due the availability of an additional DC/DC boost converter. The other attractive features of the two-stage systems include reactive power capability, lower leakage current, constant common mode voltage (CMV) and unity power factor (UPF) grid current control. However, the demerits of these systems are low reliability, less efficiency and increased complexity.

To address the above-said issue, single-stage boosting and inverting (SSBI) system are becoming popular in PV power systems. A Z-source inverter acts as an SSBI that performs boosting and inverting in a single stage. A Z-source (ZS) is an impedance network, which is constituted by the combination of inductors and capacitors. Conventional Z-sources are not suitable for PV applications as they suffer from the problem of discontinuous input current. A quasi-Z source (qZS) network is an improved version of the Z-source network, which provides an inductor after the input source, resulting in continuous input current, ease of integration of RES and low component ratings. Therefore, one might expect they inherit both the merits of qZSs and MLIs for PV applications.

Suppression of the leakage current is one of the important requirements while connecting an RES to the grid. The leakage current is principally caused by the time-variant nature of the CMV across the load terminals with respect to source ground. The conventional approach to avoid the leakage current is to provide galvanic isolation (by using a transformer either on the low-frequency side or on the high-frequency side) between the RES and the grid. Placing an isolation transformer on the AC-side would invite drawbacks of increased cost, increased volume, and reduced efficiency. This short coming may be addressed by designing a system, which places a high frequency transformer (HFT) on the DC-side. Even though PV systems with DC-side HFTs achieve lower volumes, they still demand improvements in aspects of efficiency and cost.

Thus, this situation encourages pushing research towards the development of transformerless PV inverters, which aims to reduce size, cost, and leakage current while improving efficiency. However, the removal of transformer causes direct contact between PV panels and grid. A resonant circuit is formed due to parasitic capacitance of PV panels, filter inductors and grid impedances. The aforesaid fluctuation in CMV excites the resonant circuit and cause flow of leakage current from the grid to PV panels via parasitic capacitances. This is achieved by 1) separation of AC and DC sides, 2) connecting the grid neutral to negative terminal of the input, and 3) connecting the midpoint of the DC-link to the grid neutral. These methods were used either to make the CMV constant or allow only a slow (i.e., low frequency) variation in it to reduce the leakage current. The non galvanic isolation techniques are primarily categorized based on 1) the carrier, 2) topology, and 3) modulation technique. Moreover, considerable research works has been carried out in the area of transformerless inverters for single-phase PV applications.

Several new circuit topologies and modulation schemes have been explored to suppress leakage current. However, most of the PV systems described are two-stage systems, which are complex and loss incurring.

Hence, there is wide scope for further research in the area of transformerless single phase quasi Z-Source based Multilevel Inverters for PV applications. Moreover, to address the aforesaid issues, namely (a) operability with a single source, (b) single-stage boosting and inverting, (c) reduced switch count, (d) improved efficiency, (e) reactive power capability and (f) reduced leakage current, this research focuses on the development of single-phase qZS based MLI topologies for stand-alone/grid-connected PV applications. In this context, three new configurations have been proposed in this thesis.

In the first proposal, a quasi Z-source NPC based T-type inverter (Fig. 3.1) was proposed for both stand-alone and grid-connected mode. The proposed improved modulation scheme enables the converter to handle wide input voltage variations, supply reactive power and provide a single stage boosting with inversion. The filter structure and mid-point clamp technique used eliminates high frequency variations across the parasitic capacitor. The proposed converter was tested in MATLAB for various steady-state and dynamic behaviour and further justified with experimental prototype. Moreover, the performance characteristics of the proposed inverter were compared with existing topologies to highlight its merits.

In the second proposal, a single-stage inverter with the amalgamation of dual qZS network and improved T-Type H5 inverter (Fig. 4.1) with the benefits of a single-stage boost, reactive power capability and reduced leakage current was introduced for a PV system. A hybrid method of DC decoupling and Mid-point voltage clamping was utilized for the reduction in leakage current. Furthermore, this converter employs minimum number of switches to operate at any mode, i.e., active, zero and shoot through mode of operation compared to existing inverter topologies.

In the third proposal, a seamless structure of qZS network, T-type inverter and improved Highly Efficient and Reliable Inverter Configuration (HERIC) structure (Fig. 5.1) was integrated and proposed for grid-connected PV system. Further, the modulation scheme was modified to incorporate various active, zero and shoot-through states and enable reactive power support. The shoot-through states were chosen in such a way that

voltage stress was reduced. Both Mid-point clamping technique and AC based decoupling were used to reduce leakage current under the standards dictated by *VDE-0126-1-1*.

In order to evaluate both steady-state and dynamic performance of the proposed topologies, simulations were performed in MATLAB/Simulink environment and then validated through experimental prototype. The experimental setup was built using IRFP460 MOSFET switches, MURS1560 diodes, TLP250 opto-coupler driver ICs and programmable DC supply. The control algorithm was implemented in Xilinx Spartan 6 platform and Real-time studies were performed using Opal-RT 4500 module for all three proposed topologies. Moreover, in this study, an exhaustive comparison of various five-level qZs based MLIs was done to highlight the merits of the proposed topologies. Finally, the performance of inverters was evaluated using PSIM thermal module which records a maximum efficiency of 92-95%. Thus, the proposed topologies are ideal for standalone/grid connected PV applications.

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ABBREVIATIONS

AC	Alternating Current
ADC	Analog to Digital Converter
CCM	Continuous Conduction Mode
CHB	Cascaded H Bridge
CMV	Common Mode Voltage
CMF	Common Mode Filter
CMI	Cascaded Multilevel Inverter
CST	Complete Shoot Through
DCM	Discontinuous Conduction Mode
DC	Direct Current
EMI	Electro Magnetic Interference
FC	Flying Capacitor
FFT	Fast Fourier Transform
FPGA	Field Programmable Gate Array
FB-NPC	Full Bridge Neutral Point Clamped
HFT	High Frequency Transformer
HERIC	Highly Efficient and Reliable Inverter Configuration
HBZVR	Half Bridge Zero Voltage Rectifier
HBZVR-D	Half Bridge Zero Voltage Rectifier with Diode
IS	Impedance Source
IRENA	International Renewable Energy Agency
IEEE	Institute of Electrical and Electronics Engineers
IEC	International Electro technical Commission
LCCT	Inductor-Capacitor-Capacitor-Transformer
LSPWM	Level Shifted Pulse Width Modulation
LFT	Low Frequency Transformer
LST	Lower Shoot Through
MPPT	Maximum Power Point Tracking
MLI	Multilevel Inverter
NPC	Neutral Point Clamped
PV	Photovoltaic

PF	Power Factor
PLL	Phase Locked Loop
P	Proportional
PI	Proportional-Integrator
PR	Proportional-Resonant
PWM	Pulse Width Modulation
PSIM	Power Simulation
PCB	Printed Circuit Board
P & O	Perturb and Observe Method
qZS	Quasi Z-Source
RES	Renewable Energy Sources
SPWM	Sinusoidal Pulse Width Modulation
ST	Shoot Through
SVM	Space Vector Modulation
THD	Total Harmonic Distortion
UPF	Unity Power Factor
UST	Upper Shoot Through
VSI	Voltage Source Inverter
VDE	*Verband der Elektrotechnik, Elektronik undInformationstechnik*
ZS	Z-Source
ZSI	Z-Source Inverter

LIST OF SYMBOLS

B	Boost Factor
C_1	Capacitor 1 of the Impedance network
C_2	Capacitor 2 of the Impedance network
C_3	Capacitor 3 of the Impedance network
C_4	Capacitor 4 of the Impedance network
C_f	Output Filter Capacitor
C_{PAR}	Parasitic Capacitance of the PV panel
C_{PV}	Input capacitor after PV panel
D_{SH}	Shoot-through Duty cycle
D_1, D_2	Diodes of Impedance network
f_s	Switching frequency
f_o	Output frequency
I_O	Output current
I_{grid_act}	Sensed Grid Current
I^*_{grid}	Reference grid current
i_L	Inductor current
I_{PV}	Photovoltaic Current
$i_{LEAKAGE}$	Leakage current
K_p	Proportional constant
K_i	Integrator constant
K_r	Resonant constant
k_{C1}	Ripple factor for capacitor 1 voltage
k_{C2}	Ripple factor for capacitor 2 voltage
K_L	Ripple factor for inductor current
L_1-L_4	Inductances of qZS network
L_f	Filter inductance
m	Modulation index
P_{out}	Output Power
P_{IN}	Input Power

R_g	Ground Resistance
V_{pv}	Input PV voltage
V_{AN}	Voltage across inverter terminal A and negative terminal of PV source
V_{BN}	Voltage across inverter terminal B and negative terminal of PV source
V_{CMV}	Common mode voltage
V_g	Grid Voltage
V_{out}	Output Voltage
V_L	Voltage across inductor of impedance source
V_C	Voltage across capacitor of impedance source
V_{DC}	DC-Link Voltage
V_{DC_act}	Sensed DC-link Voltage
V^*_{DC}	Reference DC-Link Voltage
V_{CPV}	Voltage across parasitic capacitance

Chapter 1

INTRODUCTION

Chapter 1

Introduction

1.1. Background

Renewable energy sources are steadily establishing themselves as promising energy sources to substitute fossil fuels over the last few decades. They have the potential to counter the harmful effects produced by fossil fuels by providing cleaner energy. Non-conventional energy sources like solar, wind and fuel cell are emerging as alternate power generating systems, which could reduce the dependence on conventional energy sources. Of these, solar photovoltaic (SPV) systems are poised to be the most dominant sources due to their abundance, zero-carbon emission, reducing cost of panels, absence of moving parts and advancements in power semiconductor switching device technology and inverter topologies. According to international agencies like IRENA, PV power system holds 24.3% amongst all non-conventional energy sources installed across the globe. With a worldwide installed capacity of 709GW [1] (Fig. 1.1) and an unprecedented growth rate of 24%, solar photovoltaic systems are poised to become a major source of energy generation in the foreseeable future.

In general, PV sources produce DC power and need to be interfaced with the utility/load. The development of power electronic interface is quite an important part in PV power system as shown in Fig. 1.2. The operation of PV systems can be classified in to 2 modes (i) Stand-alone mode, (ii) Grid connected mode [2]. In stand-alone mode of operation, the power processed from the PV source is directly fed to load and stored in batteries for further use. This operating mode is most effective in providing electricity to remote areas where both forms of power (AC and DC) could be utilised. Batteries are the primal source of energy storage in this mode of operation which increases the overall control complexity of the system. Whereas, in grid-connected mode of operation, the power is injected to utility and residential loads based on the requirement[3]. These systems do not need energy storage devices and hence, are a more popular form of PV power generation. More than 90% of worlds PV systems are grid connected due to advantages like low cost, limited storage requirement and negligible maintenance[4]. However, variations in PV output, improved efficiency, reduced count of power semiconductor devices, improved control structure, common mode voltage (CMV) and leakage current due to parasitic capacitance have impelled

the researchers for further development of new Power Conditioners for PV applications in the present scenario.

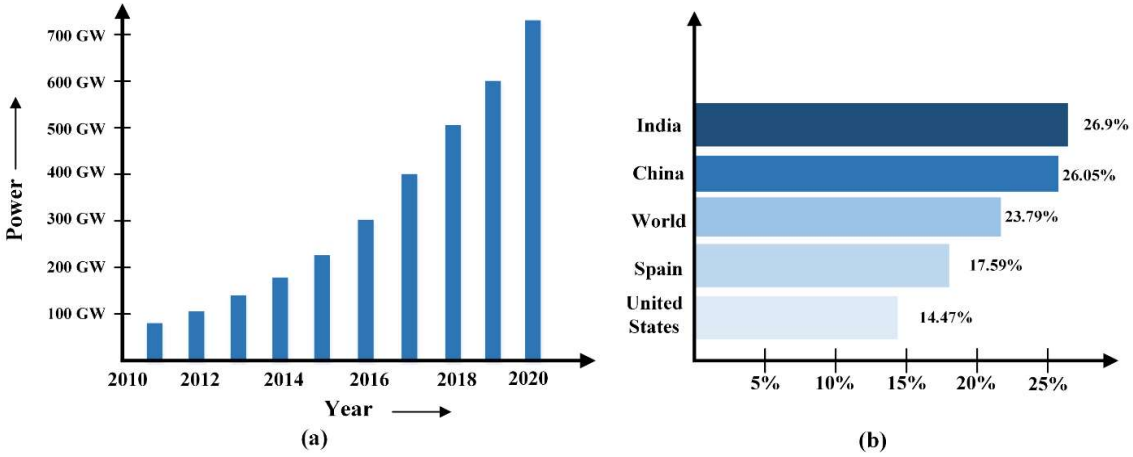


Figure 1.1 Solar PV trends. (a) Increasing trend of PV installation, (b) percentage change in solar energy with respect to 2020

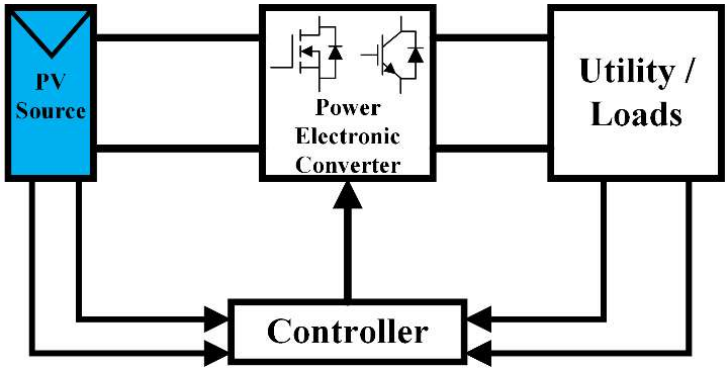


Figure 1.2 Basic Power Electronics interface

1.2. Photovoltaic Technology

In general, PV cells produce an open cell voltage of 0.6V. Therefore, many cells are needed in series and parallel combinations for the desired output voltage. Further, photovoltaic technology can be classified into four categories *viz.* module, string, multi-string, and central inverters based on their output power rating and PV module arrangement. A brief discussion of the types of inverter configuration is provided below[5]–[7].

1.2.1. AC Module Inverters

They are formed with an amalgamation of micro inverter and PV panels as shown in Fig. 1.3(a). They are the 'plug-and-play' type and typically output low power as they are connected to single PV panels. Module inverters are best known for accurately tracking maximum power point (MPPT) in mismatch conditions (partial shading). These kinds of

inverter may have additional DC-DC converter stage and transformer to provide galvanic isolation.

1.2.2. String Inverters

The string inverter depicted in Fig. 1.3(b) shows the string configuration where the inverter is fed from a series of PV panels. The total number of strings connected depends on the load requirement and thus, a DC-DC converter can also be interfaced. String inverters have lower efficiency in achieving MPPT during partial shading conditions than modular inverters. These are typically used in residential applications due to medium output power level and they lack galvanic isolation.

1.2.3. Multi-String Inverters

The multi-string concept is an expanded form of the string inverter to improve power level and flexibility. As shown in Fig. 1.3(c), each PV string is provided with its own DC-DC converter which functions as an MPPT tracker, voltage booster and feed power to DC bus bar. An inverter processes this power from the DC bus bar to utility/load. This concept makes the system more reliable and efficient during partial shading conditions. These are used for medium and large power applications like residential or commercial purposes.

1.2.4. Central Inverters

Central inverter configuration depicted in Fig. 1.3(d) shows how power from the PV array is fed to utility through a single inverter system. In this configuration, PV panels are connected in series and parallel to obtain large power output. The strings are connected in a parallel manner through diodes to avoid reverse current flow. These inverters are highly reliable and have maximum operating life compared to all other configurations but they suffer from lowest energy extraction (MPPT) and are inefficient to overcome mismatch problems. Central inverters are typically used for large power commercial applications.

1.3. Power Electronics Interfaces

Based on power processing stages, the PV inverters can be divided into 2 types: double-stage inverters and single-stage stage inverters[5], [7], [8].

1.3.1. Double-Stage Inverters

Most of the PV modules generate low output voltage hence, it becomes essential to boost input voltage based on requirement. Fig. 1.4 shows the basic configuration of double-stage inverters where the configuration consists of 2 power processing stages, the first of which is voltage boosting and the second is voltage inversion. Voltage boosting is achieved

by a DC-DC converter which operates at high frequency, and then boosted DC voltage goes through inversion to feed the load. Due to additional boosting stage, they require lesser number of PV panels than single stage inverters and also provide excellent MPPT during partial shading conditions. However, the additional power processing stage and requirement of higher components increases the size, cost and deteriorates its efficiency.

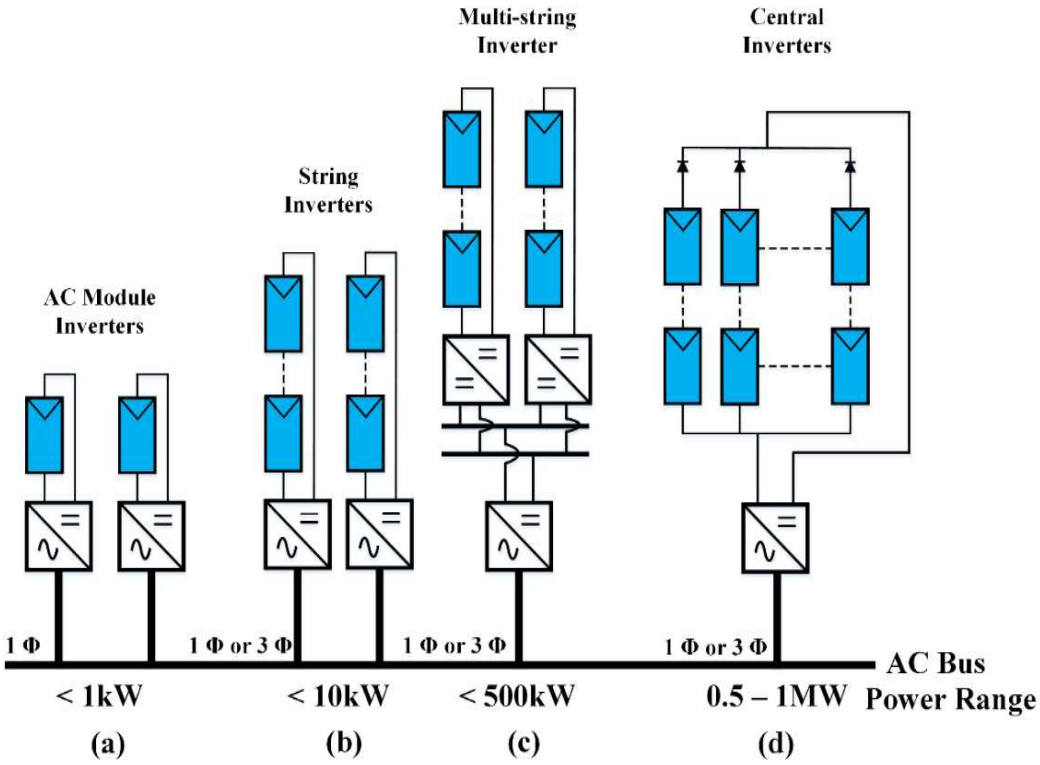


Figure 1.3 PV configurations based on module arrangement and power handling capability

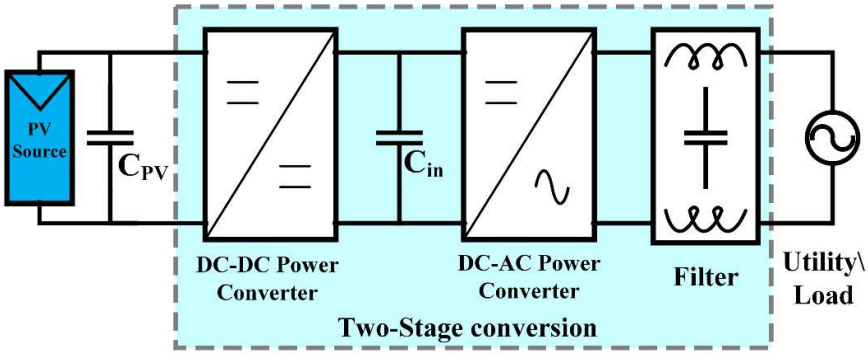


Figure 1.4 Typical Two-Stage Power Converter Topology

1.3.2. Single-Stage Inverters

The power is processed in a single-stage in such types of inverters. They don't require additional boosting stage and can be further classified into two types, namely, simple single-

stage inverters (Fig. 1.5(a)) and SSBI (Fig. 1.5(b)). Simple single-stage inverters are just like multi-string inverters or central inverter where inverters are fed directly from PV panels. They have low efficiency in extracting maximum power and require a larger number of PV panels. However, SSBIs integrate boosting and inverting stage to a single seamless configuration and incorporate advantages like good MPP tracking, high efficiency, low component requirement and high reliability. Furthermore, these systems need to interfaced with the grid in order to supply into excess power to grid. Based on the type of connection with grid, they can be further classified in to two sub categories which are isolated and non-isolated connections.

1.3.2.1 Isolated Topologies

Isolated topologies provide galvanic isolation between the PV source and the utility. Mostly, galvanic isolation is provided by the presence of transformer in the system which eliminates leakage current and DC current injection into utility. The placement of transformer can be done in 2 ways: (i) placing the transformer between inverter and utility (Fig. 1.6(a)), (ii) placing the transformer between source and inverter (Fig. 1.6(b)). The former one is a low frequency transformer (50/60 Hz) and the latter one is high frequency transformer and, in both the cases it degrades the system efficiency, increases the cost and makes it bulky.

1.3.2.2 Non-Isolated Topologies

Non-isolated topologies alternatively known as transformerless topologies, are shown in Fig. 1.5, these are topologies which do not provide galvanic isolation between source and utility. Though the system becomes lighter and more efficient, absence of galvanic isolation creates a resonant path that triggers leakage current. The prime motive of the topologies is to suppress the leakage current flowing from utility to PV source with various modulation techniques and power semiconductor device rearrangement.

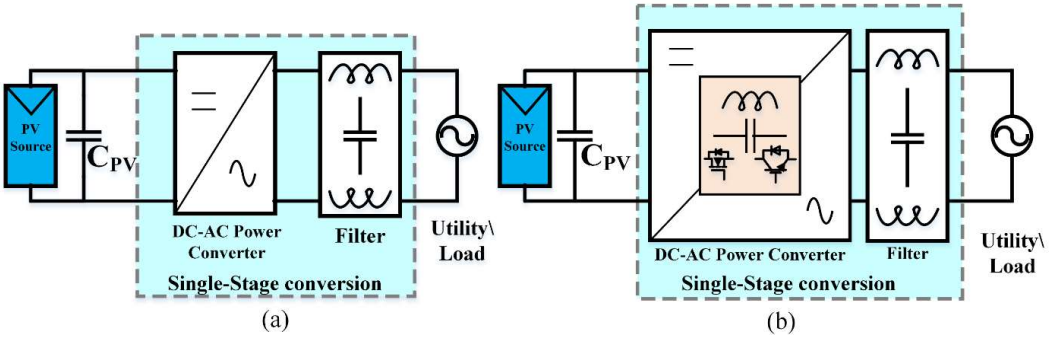


Figure 1.5 Single stage topologies; (a) Buck type single stage topology, (b) Single stage boost type topology

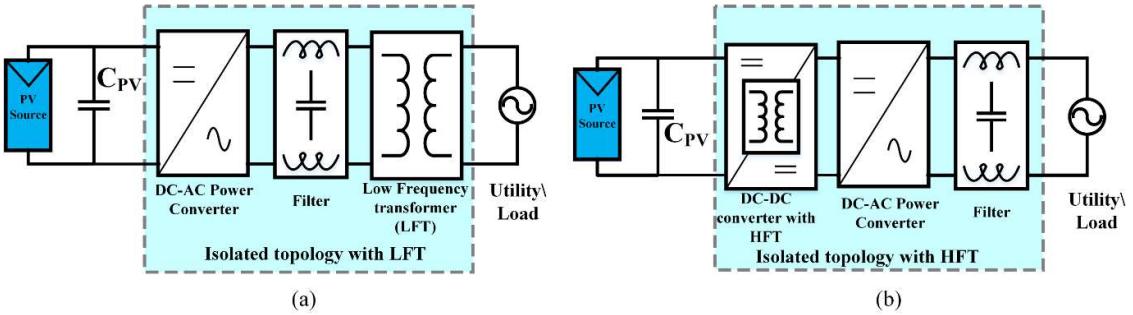


Figure 1.6 Typical scheme for Isolated based topologies; (a) Isolated topologies with LFT, (b) Isolated topologies with HFT.

1.4 The Impedance Source Inverter

From the above discussion, it is clear that the inverter configuration can be classified into various categories based on power levels, power processing stages and interconnection with grid. However, for medium and large power applications, multi-string and central inverters are suitable, and these can be further connected in either two-stage or single-stage system. Due to the presence of additional DC-DC converter, two-stage systems provide good maximum power extraction and require fewer PV panels in series. Further, the presence of additional active and passive components makes the two-stage system bulky, less efficient and less reliable. Hence, single-stage systems which are capable of achieving boosting and inverting are best suited for PV generating system.

The concept of SSBI was first introduced by F.Z. Peng as "Impedance Source Inverter" in 2008[9]. In this inverter an impedance network is sandwiched between a voltage source and a three-phase inverter to obtain single stage boosting and inverting. The impedance network which consists of 2 capacitors and inductors is connected in X fashion at the front-end of an inverter. These inverters commonly known as Z-Source inverters (ZSI) (as shown in Fig. 1.7) have been proven to overcome limitations of traditional inverters (Voltage Source Inverter) because of the following characteristics:

(i) Lower requirement of PV panels.

(ii) Single-stage power conversion with buck-boost capability.

(iii) Inherent shoot-through immunity.

(iv) Better input voltage regulation ratio

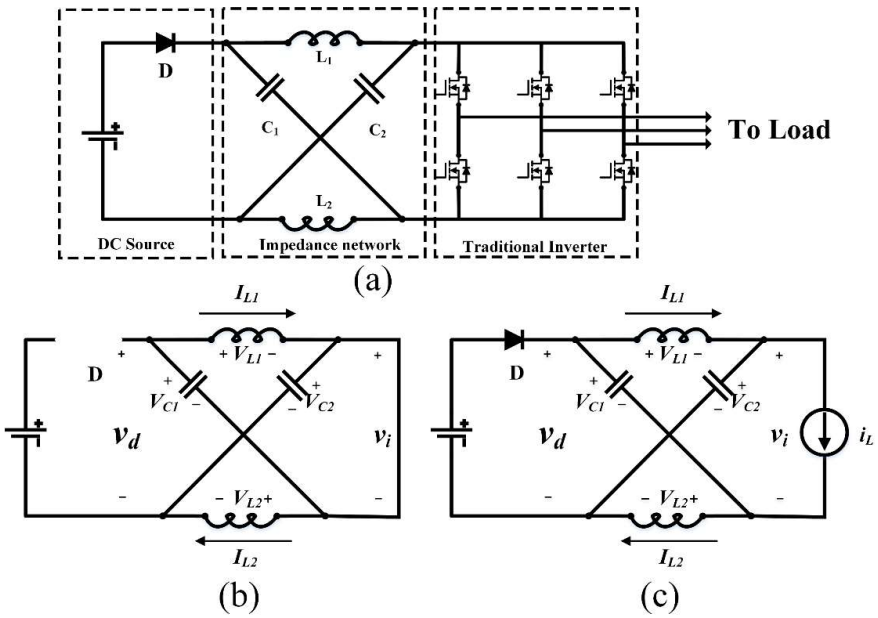


Figure 1.7 Z-Source Inverter; (a) ZSI, (b) Shoot-through Mode, (c) Non-Shoot-Through Mode.

ZSI operates in two modes, namely, Shoot-through Mode (STM) and Non-Shoot-Through Mode (NSTM). As shown in Fig. 1.7(b), during the STM (DT_0) the output terminals are short circuited and no energy is transferred to load. Due to circuit conditions, the diode gets reversed biased and inductors get charged from the capacitors during this mode. Assuming the symmetrical behaviour of the impedance network it may be noted that:

$$V_{C1} = V_{C2} = V_C v_{L1} = v_{L2} = v_L \tag{1.1}$$

Applying KVL to the circuit shown in Fig. 1.7,

$$During\ \ DT_0 \begin{cases} v_i = 0 \\ v_d = 2V_C \\ v_L = V_C \end{cases} \tag{1.2}$$

where, *D* denote the shoot-through duty ratio for a switching cycle of T_0.

NSTM as shown in Fig. 1.7(c) basically consists of all active operating modes for a traditional inverter. During this mode, the diode is forward biased and carries the input current while the capacitor gets charged. However, the combined energy of source and impedance network is delivered to the load though inverter section. Applying KVL during this mode, the values for capacitor and DC-Link becomes:

$$During\ (1-D)T_0 \begin{cases} v_L = V_{in} - V_C \\ v_i = 2V_C - V_{in} \end{cases} \tag{1.3}$$

Applying Volt-sec balance to the inductor during STM and NSTM it was found that:

$$V_C(D)T_0 + (V_{in} - V_C)(1-D)T_0 = 0 \tag{1.4}$$

Rearranging the equation, the capacitor voltage became:

$$V_C = \frac{V_{in}(1-D)}{(1-2D)} \tag{1.5}$$

Substituting the value of V_C in equation 1.3, the DC-Link value v_i is:

$$v_i = \frac{V_{in}}{(1-2D)} = BV_{in} \tag{1.6}$$

Where, '*B*' is the boost factor of ZSI.

However, ZSI has a limitation of discontinuous input current due to the presence of input diode which impedes its application in PV systems. This drawback was addressed by a new configuration, namely, '*quasi-Z-Source Inverter*' (qZSI) by placing the inductor in series with input source and rearranging passive elements[10]. This arrangement has advantages such as:

(i) Continuous input current.

(ii) Reduced component rating and size.

(iii) Availability of common ground between source and load.

The qZSI is shown in Fig.1.8(a), where it can be observed that inductor (L_1) is placed in input side which makes the current continuous. The STM and NSTM are represented by figs.1.8(b) and fig 1.8(c) respectively. During the STM, the governing equations are:

$$During\ DT_0 \begin{cases} V_{L1} = V_{in} + V_{C1} \\ V_{L2} = V_{C2} \\ V_D = V_{C1} + V_{C2} \end{cases} \tag{1.7}$$

Where, it can be clearly seen that the diode blocks completely DC-Link voltage.

Similarly, during NSTM, the corresponding equations are:

$$During\ (1-D)T_0 \begin{cases} V_{L1} = V_{in} - V_{C2} \\ V_{L2} = -V_{C1} \\ V_{dc} = V_{C1} + V_{C2} \end{cases} \tag{1.8}$$

Applying volt-sec balance for inductor L_1 gives

$$(V_{in} + V_{C1})DT_0 + (V_{in} - V_{C2})(1-D)T_0 = 0 \tag{1.9}$$

Similarly, applying volt-sec balance for inductor L_2 gives:

$$V_{C2}DT_0 - V_{C1}(1-D)T_0 = 0 \tag{1.10}$$

Solving 1.9 and 1.10 voltages across capacitors are:

$$V_{C1} = V_{in}\frac{D}{1-2D}\ and\ V_{C2} = V_{in}\frac{(1-D)}{1-2D} \tag{1.11}$$

Hence, the DC-Link voltage of qZSI is:

$$V_{dc} = V_{in}\frac{1}{1-2D} = BV_{in} \tag{1.12}$$

Where, the term '*B*' the boost factor of the system. It may be noted that the boost factor is same as ZSI[11]. Hence, it can be inferred that qZSI provides higher benefits like reduced component rating, continuous input current and common ground feature than ZSI with same boost factor.

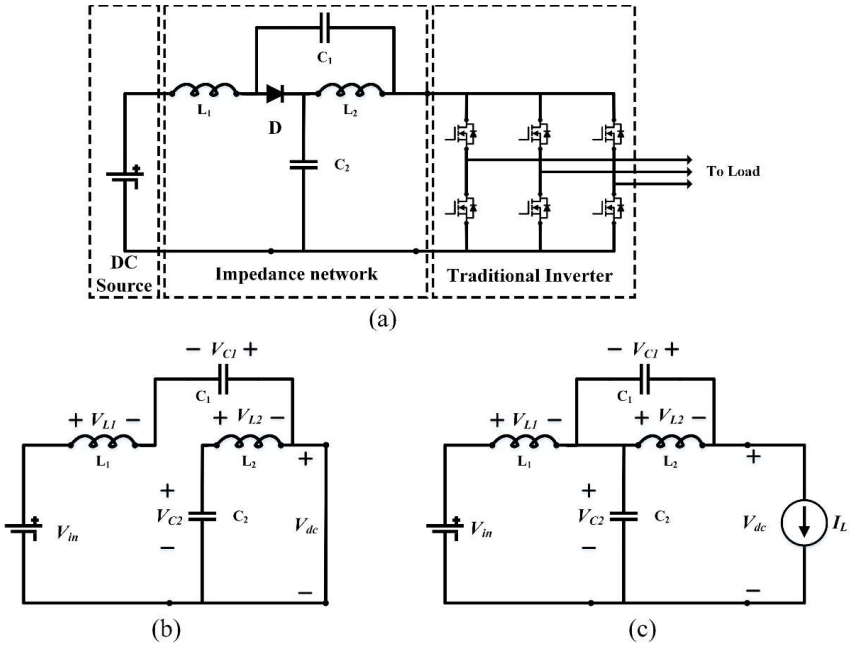


Figure 1.8 Quasi-Z-Source Inverter; (a) 3-Phase qZSI, (b) STM, (c) NSTM

1.5 Multilevel Inverters

All the above topologies were discussed for two-level operations. Whereas in the present scenario, Multilevel Inverters with reduced device count are gaining popularity due to the merits of reduced dv/dt, driver circuits, size, cost and efficiency[12], [13]. It is capable of synthesizing the output voltage waveform close to sinusoidal for increased levels and also minimises the total harmonic distortion (THD). Even though the concept was formulated in 1975, the three traditional MLIs - Neutral point clamped (NPC), flying capacitor (FC) and Cascaded H-Bridge (CHB) MLIs (Fig. 1.9) are highly popular for industrial applications. However, the requirement of more components, balancing capacitor voltages and increased control complexity limits the use of MLIs for higher level operations[14]. In additions, MLIs are buck in nature, reduce output voltage regulation and deteriorates the output voltage waveform at lower modulation index. This necessitates a boosting stage to increase the output voltage between PV and MLIs. Hence, the research is aimed to develop impedance source based MLIs imposing benefits of both impedance source and reduced device count MLIs for Photovoltaic Applications.

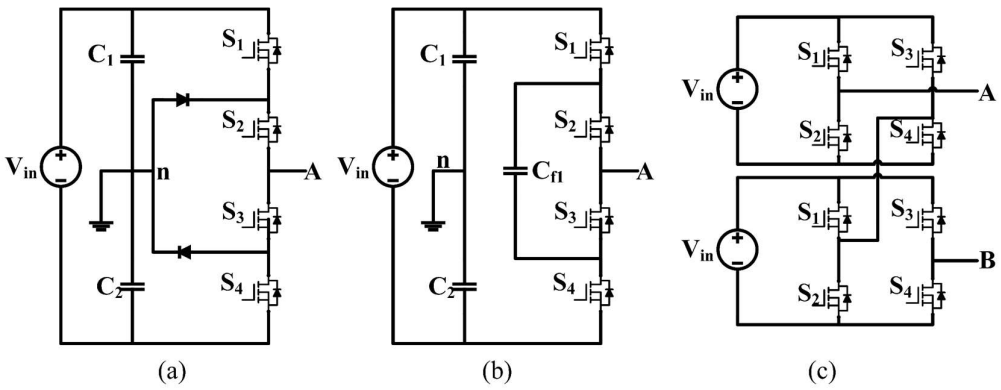


Figure1.9 Traditional MLI. (a) Diode-Clamped Topology, (b) Flying Capacitor (FC) Topology and (c) Cascaded H-Bridge (CHB) Topology

1.6 Analysis of Leakage Current

As discussed in earlier sections isolated based topologies help in providing galvanic isolation and restricts DC current injection, thereby improving the quality of power injecting to utility. However, their bulkiness and reduced efficiency has directed the contemporary research towards development of non-isolated based topologies. These transformerless inverters have high efficiency and reliability with PV system but due to lack of galvanic isolation, they suffer from the issue of common mode current[15]. A typical non-isolated system is shown in Fig. 1.10. Due to the existence of direct path between PV panels and utility, there exists a resonant path between various passive elements that triggers the leakage current. Some of the issues related to leakage current are potential induced degradation of PV panels, significant conducted and radiated electromagnetic interferences (EMI), grid current distortion and operational insecurity[16].

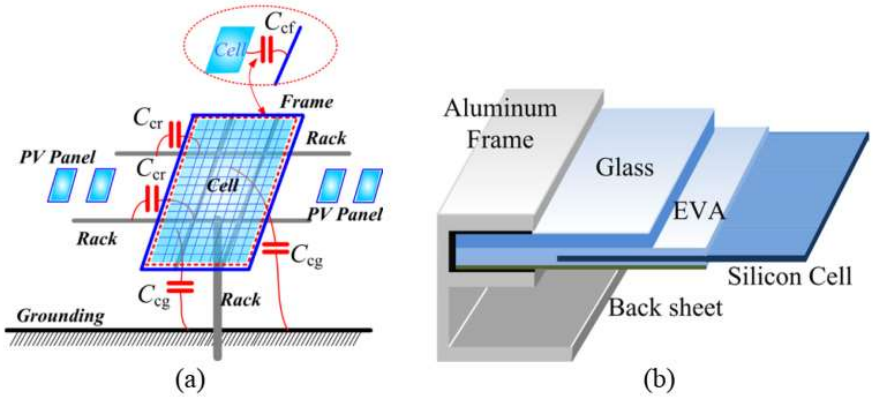


Figure 1.10 PV panels with various parasitic (a) Parasitic capacitance across various PV elements, (b) Internal structure of PV panel

The parasitic element that contributes most to leakage current is the parasitic capacitance formed between PV panels and the ground. The primary factors contributing to the formation of parasitic capacitance are PV panel physical parameters, mounting methods, solar cell types, dielectric permittivity of the encapsulated material and relative humidity of air. The value of the leakage current greatly depends on the value of the parasitic capacitance which is a variable quantity as per above-said factors and common mode voltage (CMV). Most commonly used single-capacitor model predicts the parasitic capacitance to have a value between 7nF/kW to 220nF/kW[17]. The relation between the leakage current (i_{LEAK}), parasitic capacitor (C_{PAR}) and CMV is given by:

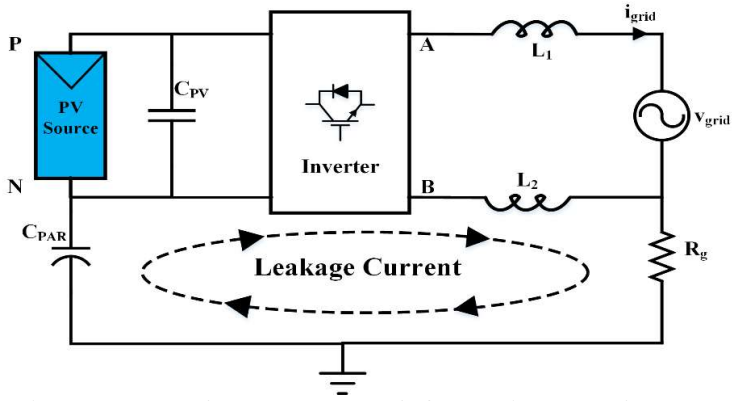


Figure 1.11 Leakage current path for PV integrated system

$$i_{LEAK} = C_{PAR} \frac{V_{CMV}}{dt} \tag{1.13}$$

For a typical transformerless system, as shown in Fig 1.11, the leakage current i_{LEAK} flows through the loop consisting of the parasitic capacitances (C_{PAR}), bridge, filters (L_1 and L_2), utility grid, and ground impedance R_g. The leakage current path is equivalent to an LC resonant circuit in series with the CM voltage and the CM voltage v_{CM} is defined as:

$$v_{CM} \quad \frac{V_{AN}+V_{BN}}{2} + V_{AN} - V_{BN} \frac{L_2-L_1}{2(L_2+L_1)} \tag{1.14}$$

For an asymmetrical filter condition ($L_1 \neq L_2$), the above equation holds good for CMV calculation. However, for symmetrical filter condition ($L_1 = L_2$) the above equation becomes:

$$v_{CMV} = \frac{V_{AN}+V_{BN}}{2} \tag{1.15}$$

From (1.13) and (1.15) it is evident that CMV triggers leakage current. Hence, to reduce leakage current, symmetrical filter condition becomes a primary requirement. Further, based on topological structure, PWM scheme and loading conditions, there exists high frequency variations in CMV. Hence, it becomes the prime aim of the transformerless inverter system to either eliminate high frequency transition or allow a variation of frequency of 50Hz/60Hz in CMV.

Table 1.1 Grid Codes for PV Inverters

<table>
<tr><th colspan="2">Issue</th><th colspan="2">VDE 0126-1-1</th><th>VDE-AR-N 4105</th></tr>
<tr><td colspan="2" rowspan="5">Leakage current</td><td>RMS Value</td><td>Break time</td><td rowspan="5">The use of the leakage current protection devices is inevitable. The standard IEC 60755 defines the detail requirements for the leakage current protection devices.</td></tr>
<tr><td>i > 300mA</td><td>0.3s</td></tr>
<tr><td>Δi > 30mA</td><td>0.3s</td></tr>
<tr><td>Δi > 60mA</td><td>0.15s</td></tr>
<tr><td>Δi > 150mA</td><td>0.04s</td></tr>
<tr><td rowspan="2">Grid frequency monitor</td><td>50.2 < f < 51.5</td><td colspan="2">Disconnected from the grid within 0.2s</td><td>Adjustable generation systems shall reduce (for f increase) or increase (for f decrease) the active power P_M generated instantaneously with a gradient of 40% of P_M per Hertz</td></tr>
<tr><td>f > 51.5 or f < 47.5</td><td colspan="3">Disconnected from the grid within 0.2s</td></tr>
<tr><td colspan="2">Active power</td><td colspan="2">None</td><td>The generation systems (>100kW) could reduce their active power to a set point provided by the network operator.</td></tr>
<tr><td colspan="2">Reactive power</td><td colspan="2">None</td><td>The generation systems should output required reactive power in accordance with the characteristic curve provide by network operator.</td></tr>
</table>

1.7 Grid Standard

Most of the PV systems around the world are grid-connected systems which decrease the burden on conventional energy sources. The penetration of RES into the grid without proper code can make the grid unstable. Hence, it is important to operate existing systems and interconnect new systems with these codes. Table 1.1 provides various codes and their rationale for connection of PV systems and modes of grid operation.

1.8 Summary

From the above discussion, it is apparent that contemporary research is focused on the development of new configurations of Impedance Source based MLIs with the features of reduced device count, improved waveform quality, easy control scheme, single stage boosting, high efficiency and reliability for Photovoltaic applications. To contribute to the current research area, this thesis aims to investigate new single-stage boosting and inverting topologies to harness power from PV panels and successfully feed to grid without isolation transformer. The works presented addresses the issue of leakage current and measures to keep it well within the limit. Modified modulation scheme was also presented to insert shoot-though at various instants of time. The dynamic behaviour of the proposed configurations is presented and analysed under standalone mode and grid connected mode. Finally, a comprehensive comparison was made with existing impedance source based MLIs available in the literature to highlight the merits of the proposed configurations.

Chapter 2

LITERATURE REVIEW

Chapter 2

Literature Review

2.1. Introduction

The rise in carbon emission, global warming and shortage of fossil fuel-based power generation has compelled the growth of RES based on Solar, Wind, Fuel-Cell, etc. Among these, photovoltaic technology shows potential to meet the energy requirements as discussed in previous chapter. With improvement in this technology PV panels are becoming more cheaper, which makes the integration PV technology with grid achievable. Nevertheless, with low panel efficiency (15% for poly-crystalline and 18% for mono-crystalline) and variable weather conditions like solar insolation, temperature, partial shading and grounding issues, it becomes important to extract maximum power. Moreover, due to low voltage output of PV panels they are connected in series-parallel combination to meet power requirement. A lot of investigations have been going on with regards to PV material design, power electronics interface and control schemes. Finding solutions to achieve minimum device count, low leakage current, voltage boosting and reduced control complexity improves the performance of PV inverters and enhances the longevity of PV panels. Therefore, inverters play a pivotal role in extracting maximum power from PV and feeding it into utility.

Grid-connected inverter can be classified in two categories based on (a) type of interconnection and (b) power processing stage. Based on the type of interconnection, it can be further classified into isolated type and non-isolated type. Topologies that provide galvanic isolation between PV source and utility are called Isolated topologies. The galvanic isolation can be provided either on low frequency side or high frequency side based on location of transformer. However, this makes the system less efficient, bulky and costly[18]. Non-isolated inverters or transformerless inverter addresses this issue by eliminating transformer present in the circuit. They have the advantageous in terms of efficiency, cost and modularity but due to the absence of galvanic isolation there is a direct path between source and utility which paves way for flow of leakage current. This flow of leakage current can cause various issues like EMI, reduces the life span of PV panels, create operational insecurity and decrease reliability. Therefore, in non-isolated topologies, it important to reduce leakage current by denying path to it.

The voltage source inverter (VSI), based on power processing stage can be classified into two-stage type and single-stage type. Two-stage system use additional DC-DC power

converter at front-end of VSI to boost the PV voltage. Due to additional DC-DC stage they achieve excellent MPPT tracking and high boost; on the flip side these systems have lower efficiency[19]. Single-stage boosting with inverting system alleviates the above said issue by integrating boost network into traditional VSIs and hence, eliminates two-stage power processing[20]. These systems are beneficial and best applicable to module-based inverters for low power applications. Therefore, non-isolated based Single-stage boosting with inverting system is an advantageous proposition of PV application.

In this context, this chapter presents a comprehensive review of existing impedance source networks for single stage boosting feature. Further, a detailed review of various single-phase transformerless topologies is carried out based reduction in leakage current. A thorough review with comparative assessment of existing three-level and five-level impedance source based MLI is also presented for PV-grid connected system. For simplicity PV sources has been modelled here as DC source.

2.2. Overview of Various Types of Impedance Networks

The solar PV modules have very low output voltage which necessitates the requirement of boosting network based on the applications. Impedance source networks plays a pivotal role in boosting the input voltage without needing any additional semiconductor devices[20]–[22]. Impedance network can be basically classified into 2 sections i.e., non-Transformer based and Transformer/Coupled inductor based. Fig 2.1 shows the basic impedance sources available in literature, the other impedance sources being extension of these networks to improve gain and reduce stress.

The Z-source inverter (Fig. 2.1(a)) was proposed by F.Z. Peng in 2002 which was integrated with 3-phase voltage source inverter in order to obtain single-stage boosting and inverting. However, the traditional Z-source networks have the following limitations: discontinuous input currents, high switching stresses during high boost operations, poor power quality during high boost operations, high start-up inrush currents, inability to share the neutral with load (or) non-availability of joint earthing, and high capacitor voltage stresses. These disadvantages paved way for the development of quasi-Z-source (qZS) network shown in Fig. 2(b) and 2(c). The abovesaid issues were addressed through qZS network which has the same boost factor as of Z-source. A theoretical study was performed by taking parasitic nature of transmission line as distributed Z-source parameters, as shown Fig. 2.1(d)[23], [24]. This network performs shoot-through network in the front-end of distribution network.

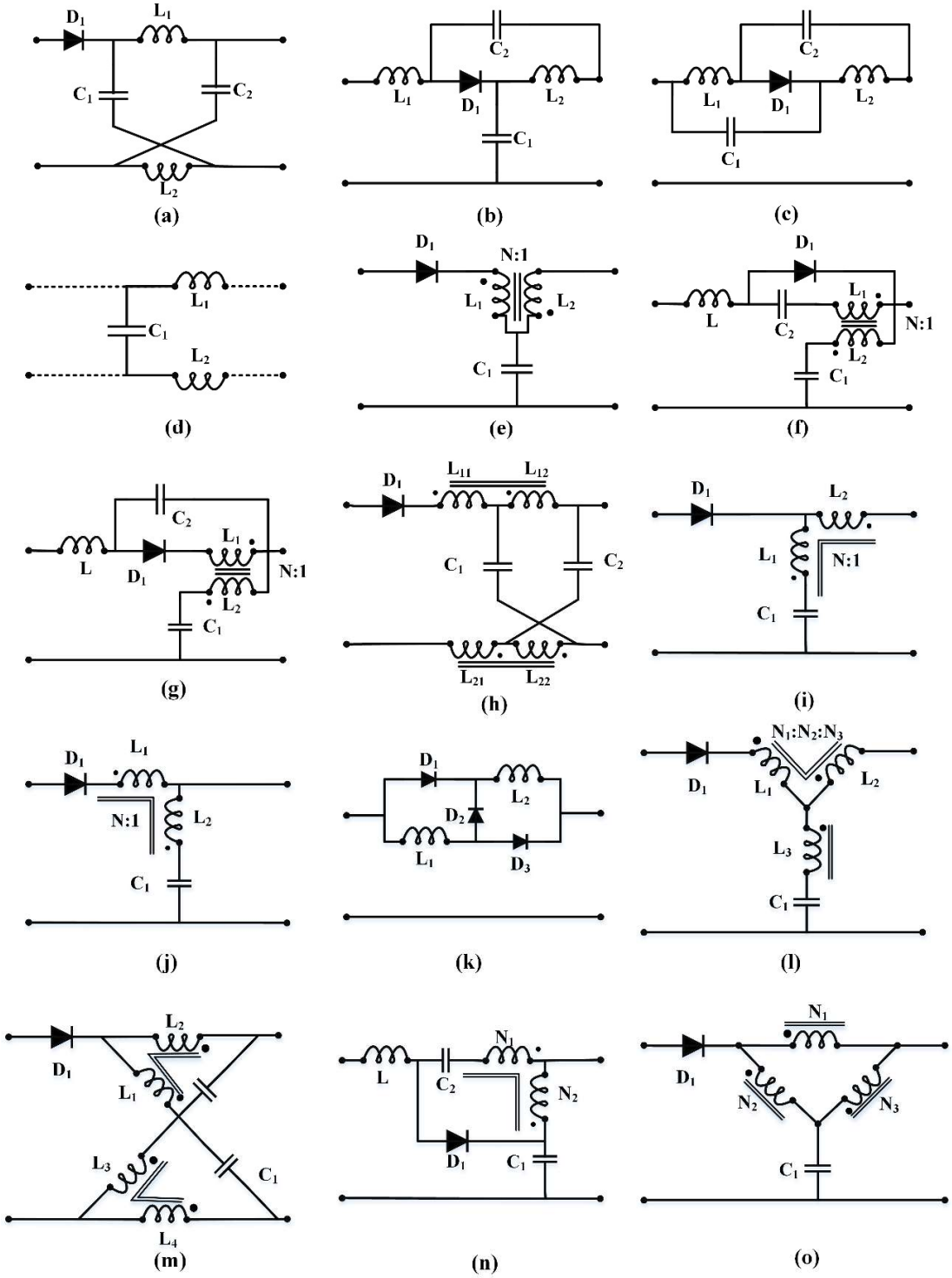


Figure 2.1 Basic impedance source networks. (a) ZSN, (b) QZSN, (c) d-QZSN, (d) DZSN, (e) Trans-ZSN (or) TSN, (f) LCCT-ZSN, (g) QLCCT-ZSN, (h) TZSN, (i) Γ-SN, (j) FΓ-SN, (k) LSN, (l) YSN, (m) Σ-SN, (n) ASN, and (o) Δ-SN

A transformer-based Z-source was introduced in[25]–[27], which improved gain by modifying the turns ratio provided as shown in Fig. 2(e). This structure reduced the voltage

stress significantly. Inductor-Capacitor-Capacitor-Transformer Z-source Network (LCCTZSN) was introduced in 2011 with 2 different structures[28], [29]. The structures for LCCTZSN and quasi-LCCTZSN are provided in Figs. 2(f) and 2(g) respectively. The quasi counterpart proved to be advantageous as it drew smooth input current from source and hence, ideal for PV power generation. A transformer Z source (TSN) was introduced in 2009 by M. K. Naguyen *et al.*[30] which achieved high boost using transformer ratio of more than 1. As shown in Fig. 2.1(h) TSN utilised 2 pairs of coupled inductors, a pair of capacitors and a diode to form the network. P.C. Loy *et al.*[31]proposed a gamma source network (ΓSN) which utilised transformer-based coupling to achieve high boost factor and gain. The network is connected in Γ shape (Fig 2.1(i)) and achieves boosting by maintaining a low turns ratio[32]–[34]. Many improved versions of ΓSN are also available in literature incorporating advantages like continuous input current, no start-up inrush current, reduced leakage inductance and reduced voltage spikes. A flipped gamma source network (FΓSN) was introduced [34], [35]for current source inverter application to achieve high gain with higher turns ratio (Fig 2.1(j)).

A new solution to reduce high start-up inrush current was proposed in [36] as L-Source network (LSN). This network presented in Fig. 2.1(k) utilises only inductors and diode to achieve boosting capability. To operate in wide voltage ranges, Y-Source network (YSN) was introduced in 2014 [37], [38]. This network as shown in Fig 2.1(l) has 3 coupled inductors and 1 capacitor (visible like Y network) provides 3 degrees of control to achieve voltage boost. Two ΓSN was connected to form a Σ-Source network (ΣSN) which is shown in Fig. 2.1(m) to achieve voltage boosting with changing turns ratio and varying duty cycle[39]. The main advantage of this converter is that it increases voltage gain, reduces size, and significantly reduces leakage inductance. Replacing the coupled inductor by auto-transformer, A-Source network (ASN) was proposed [40]which draws continuous input current as shown on Fig. 2.1(n). As shown in Fig. 2.1(o) 3 tightly coupled inductors in Δ fashion were proposed in 2017 as Δ-Source network[41]. This network offered low magnetising transformer current and provided better transient effect due to leakage inductance. The above said impedance network can be integrated with existing MLI structures to form single stage boosting inverter based on requirement.

Table 2.1 Comparison of Various Impedance Source Networks

Type of impedance source	Boost factor	Type of input current	Component count				Remarks ++ Pros and -- Cons
			L	C	D	CCI/TR	
Z Source (Fig. 2.1(a))	$\frac{1}{1-2D}$	Discontinuous	2	2	1	0	++ inherent shoot through protection ++ single stage boosting and inverting -- start-up inrush current
Quasi Z Source (Fig. 2.1(b) and (c))	$\frac{1}{1-2D}$	Continuous	2	2	1	0	++ common ground between input and output ++ reduced capacitor voltage -- no change in diode and voltage stress
T Z-source (Fig. 2.1(e))	$\frac{1}{1-(1+k)D}$	Discontinuous	0	1	1	1	++switching stresses compare to ZSN, QZSN ++voltage gain and modulation index can increase simultaneously ++common ground with a load --high turns requirement for high boost gains --suffers from the leakage inductance
LCCT-ZN (Fig. 2.1(f) and 2.1(g))	$\frac{1}{1-(1+k)D}$	Continuous	1	2	1	1	++ high gains by changing turns ratio ++ high frequency ripples -- suffers from leakage inductance
TZN (Fig. 2.1(h))	$\frac{1}{1-(1+k)D}$	Discontinuous	0	2	1	2	++ lower voltage stress ++ simultaneous increment of shoot through and modulation index -- Absence of common ground
Γ-source (Fig. 2.1(i))	$\frac{1}{1-(1+\frac{1}{k-1})D}$	Discontinuous	0	1	1	1	++ higher boost capability ++ common ground with load ++ simultaneous increment of shoot through and modulation index -- suffers from the leakage inductance
Flipped Γ-source (Fig. 2.1(j))	$\frac{1}{1-(1+k)D}$	Discontinuous	0	1	1	1	

Type of impedance source	Boost factor	Type of input current	Component count				Remarks ++ Pros and -- Cons
			L	C	D	CCI/TR	
LSN (Fig. 2.1(k))	$\frac{1+D}{1-D}$	Continuous	2	0	3	0	++ reduced passive component count ++ no start-up inrush current -- low boost factor compared to ZSN
YSN (Fig. 2.1(l))	$\frac{1}{1-(\frac{N_3+N_1}{N_3-N_2})D}$	Discontinuous	0	1	1	1	++ high Gain at low shoot through ++ high degree of control -- suffers from leakage inductance
Σ-SN (Fig. 1(m))	$\frac{1}{1-(k)D}$	Discontinuous	0	2	1	2	++ low switching stress compared to ZSN ++ simultaneous increment of shoot through and modulation index -- absence of common ground -- suffers from leakage inductance
A-SN (Fig. 1(n))	$\frac{1}{1-(2+k)D}$	Continuous	1	2	1	1	++ high gains by changing turns ratio ++ common ground -- suffers from leakage inductance
Δ-SN (Fig. 1(o))	$\frac{1}{1-(k)D}$	Discontinuous	0	1	1	1	++ highest degree of voltage boosting ++ low leakage inductance effect compared to YSN ++absence of common ground -- discontinuous input current

L= Inductors, C= Capacitors, D=Diodes, CCI=Coupled Inductors an TR=Transformers

2.3. Overview of Single Phase Transformerless Inverters

As discussed in previous chapter, single-phase transformerless inverters are getting popular for PV applications due to low cost, compact size and higher efficiency. The common mode voltage developed in circuit triggers the resonant path of parasitic elements which causes the leakage current damages the semiconductor devices, shortens life of PV panels and causes EMI issues. However, the problems are addressed in two ways; first method is to deny any path between source and utility and second is to reduce high frequency transitions in CMV[42], [43]. Based on this idea, the configurations in the literature can be divided in 3 types: (a) DC decoupling based, (b) AC decoupling based and (c) Mid-point clamped based. Fig 2.2 shows the basic circuitry to achieve various transformerless inverters (TLI).

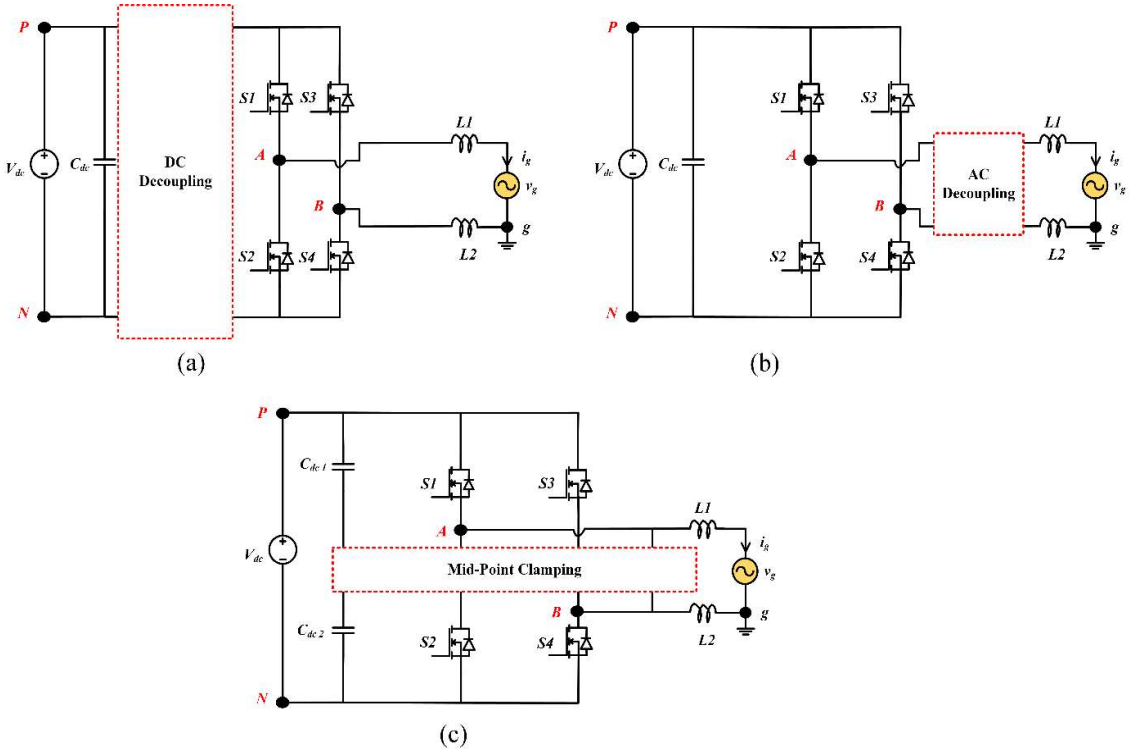


Figure 2.2 Basic classifications of transformerless inverters. (a) DC decoupling based, (b) AC decoupling based and (c) Mid-point clamping based.

2.3.1 DC Decoupling Based Topologies

These topologies use the technique of isolating source and utility side by providing additional power semiconductor devices on DC side[44], [45]. This method effectively keeps leakage current under the German standard *VDE-0126-1-1*. Some topologies that provide this feature are explained below and these includeH5 [46], H6 dc side [15], H6 dc side-1 [47], and H6 dc side-2 [47]topologies.

Fig 2.3(a) presents the circuitry of H5 inverter proposed in [46], [48] and patented by well-known solar inverter producers SMA solar technology. An additional switch S_5 is placed between source and a full bridge inverter (FBI), which acts as DC decoupling switch. The operation of this inverter is same as that of FBI except during zero state, wherein switch S_5 is turned off to decouples PV source during freewheeling period. Though this provides lower leakage current, this topology suffers from higher conduction losses which reduce power density. To reduce the leakage current further, a H6 based topology (Fig. 2.3(b)) was proposed in [49], where one more switch (S_6) was added in negative terminal to deny any path to parasitic resonant circuit. Due to the operation of 4 switches at a time, the converter incurred huge losses during power transferring mode. To counter power loss, two H6 based dc side topologies were presented in [47] which can be seen in fig. 2.3(c) and 2.3(d). Their operations are similar while achieving higher efficiency than H5 or H6 circuits. However, DC-decoupling based topology reports higher losses and unbalanced switching due to the presence of power semiconductor devices on DC side. Therefore, DC-decoupling circuit alone cannot achieve low leakage current keeping power losses low.

2.3.2 AC Decoupling Based Topologies

AC decoupling-based topologies provide segregation of PV and utility side by placing power converting devices on AC side. They provide balanced power output with low THD and constant CMV. HERIC and extended H6 based topologies are mostly used to provide AC based segregation[50]–[58].

HERIC topology introduced in[50] is well known to achieve a high efficiency of 98%. They are applicable to string inverters and recommended by German manufacturer sunways solar inverters[51]. As illustrated in Fig. 2.4(a) this topology provides decoupling of PV side during freewheeling period by activating switches S_5 and S_6. A similar kind of topology is present in [58] and shown in fig. 2.4(b), wherein two more additional diodes are used in series with decoupling switches. This circuitry avoids the conduction of body diode of decoupling switches, which improves the efficiency and reliability of the converter. In both the cases, a constant CMV, low leakage current and low output ripple are achieved.

The extended form of H6 topologies is also utilised for AC decoupling. The 2 topologies presented in [52]and [53] use 2 pairs of switches and diode to freewheel the output current during the zero state and thus, provide decoupling. As shown in Fig. 2.4(c) and 2.4(d), the power delivering switches operate in full bridge mode and they achieve constant CMV. These topologies have major disadvantage of higher conduction losses as a greater number of

switches conduct in power delivering mode. An extended form of H6 topology was proposed in[54] wherein the cross connected diodes and switches are replaced with IGBTs as shown in Fig. 2.4(e). This demonstrated a better reactive power handling capability than MOSFET driven circuits. Fig. 2.4(f) displays a mid-switch based H6 transformerless inverter[55] which used switch S_6 to complete the freewheeling path of output current. Another interesting topology derived from H5 circuitry [56], [57]is shown in Fig. 2.4(g) where 2 switches are added to top and bottom between arms of FBI. Additional diodes are used for freewheeling load current which decouples the PV with the utility grid to achieve low leakage current. However, this comes with disadvantage of fixed dead time for all power semiconductor devices.

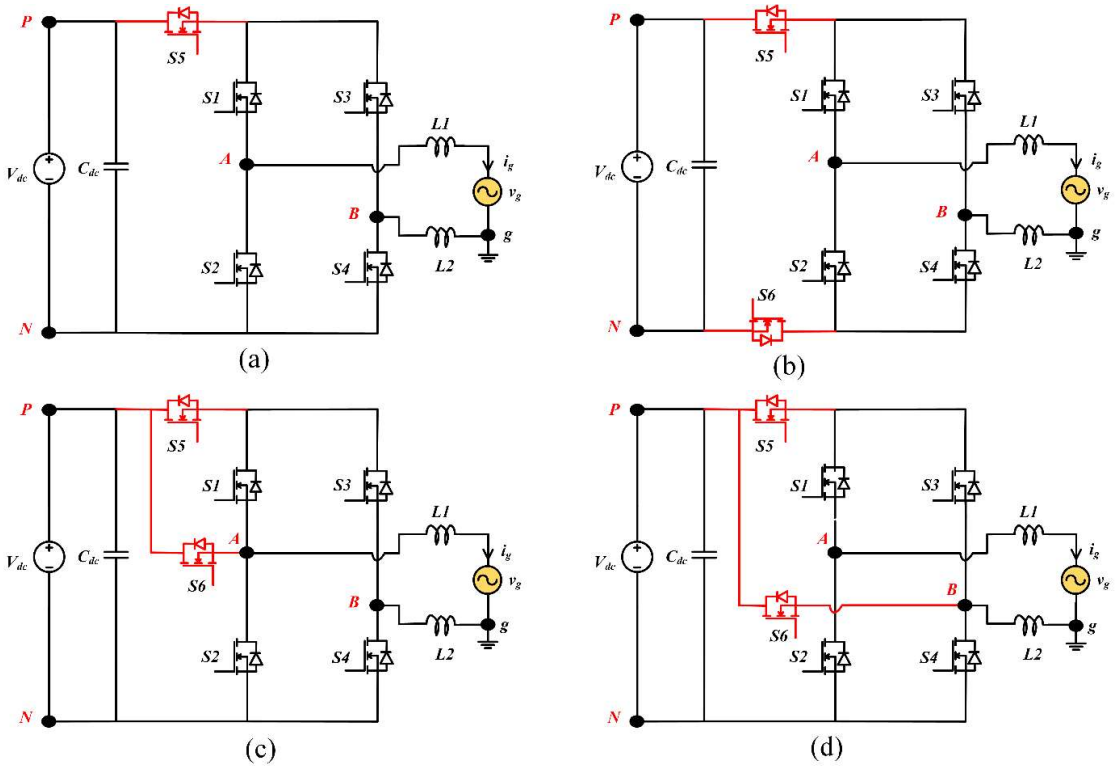


Figure 2.3 DC decoupling-based circuits. (a) H5 inverter, (b) H6 inverter, (c) H6-dc-side-1 topology and (d) H6-dc-side-2 topology.

2.3.3 Mid-Point Clamped Topologies

Topologies that use additional power semiconductor devices on either AC or DC to clamp the voltage are classified as mid-point clamped topologies. These are extended versions of full bridge topology with advantages like lower ripple in leakage current and constant CMV. The midpoint clamping topologies, such as HB-ZVR [59], HB-ZVR-D[60], H5-D [48],

HERIC-Active-1 [43], HERIC-Active-2 [43],HERIC-Active-3 [43], PN-NPC [61], [62], iH5/oH5 [63], oH5-1 [64], and oH5-2 [64], are explained in following sections.

Fig 2.5(a) presents H-bridge zero voltage rectifier (HB-ZVR) which operates exactly as a full bridge inverter but uses bidirectional switch and rectifier circuit to clamp the mid-point of dc link voltage to output during freewheeling period[65]. H-bridge-ZVR-diode (HB-ZVR-D) is illustrated in fig 2.5(b); it achieves zero leakage current and constant CMV by using fast recovery diode. Fig. 2.5(c) presents an improved H5 topology that uses a diode and switch S_5 to clamp the mid-point voltage during freewheeling period. Using this topology, a constant CMV is achieved and leakage current reduces to one-third of H5 inverter. However, it suffers from high THD which requires a bulky filter.

Based on active clamping of HERIC structure, 3 topologies are proposed in [43]are presented in Fig. 2.5(d)-(f). These topologies clamp the mid-point of dc-link voltage to the mid-point of HERIC structure to make CMV constant. Though these topological schemes achieve low leakage current, but they suffer from dead time issue. An interesting transformerless circuit is proposed in[61], [62] utilises cells of positive NPC and negative NPC. The topology shown in Fig. 2.5(g) uses 4 power semiconductor devices during freewheeling period to achieve constant CMV and low leakage current.

Topology illustrated in Fig. 2.5(h) shows an improved version of H5 inverter where 2 switches are added to DC side. One of the switches decouples the PV while another clamps the mid-point voltage during freewheeling period[63], [66]. The main advantage of this topology is achieving good differential mode characteristics with constant CMV. Two oH5 inverters (oH5-1 and oH5-2) proposed in [64]are again extended versions of traditional H5 inverter circuitry. The topologies in Fig. 2.5(i) and 2.5(j) respectively achieves low leakage current by eliminating high frequency transitions in CMV. The circuit uses 2 switches and 2 diodes to clamp the mid-point voltage during freewheeling period. Eventually, the three-level operation described for the above topologies requires a bulky filter to lower the THD. Due to the buck nature, these topologies require larger input voltage, which required a greater number of PV panels[67] in series, thereby, contributing to strengthening of leakage current.

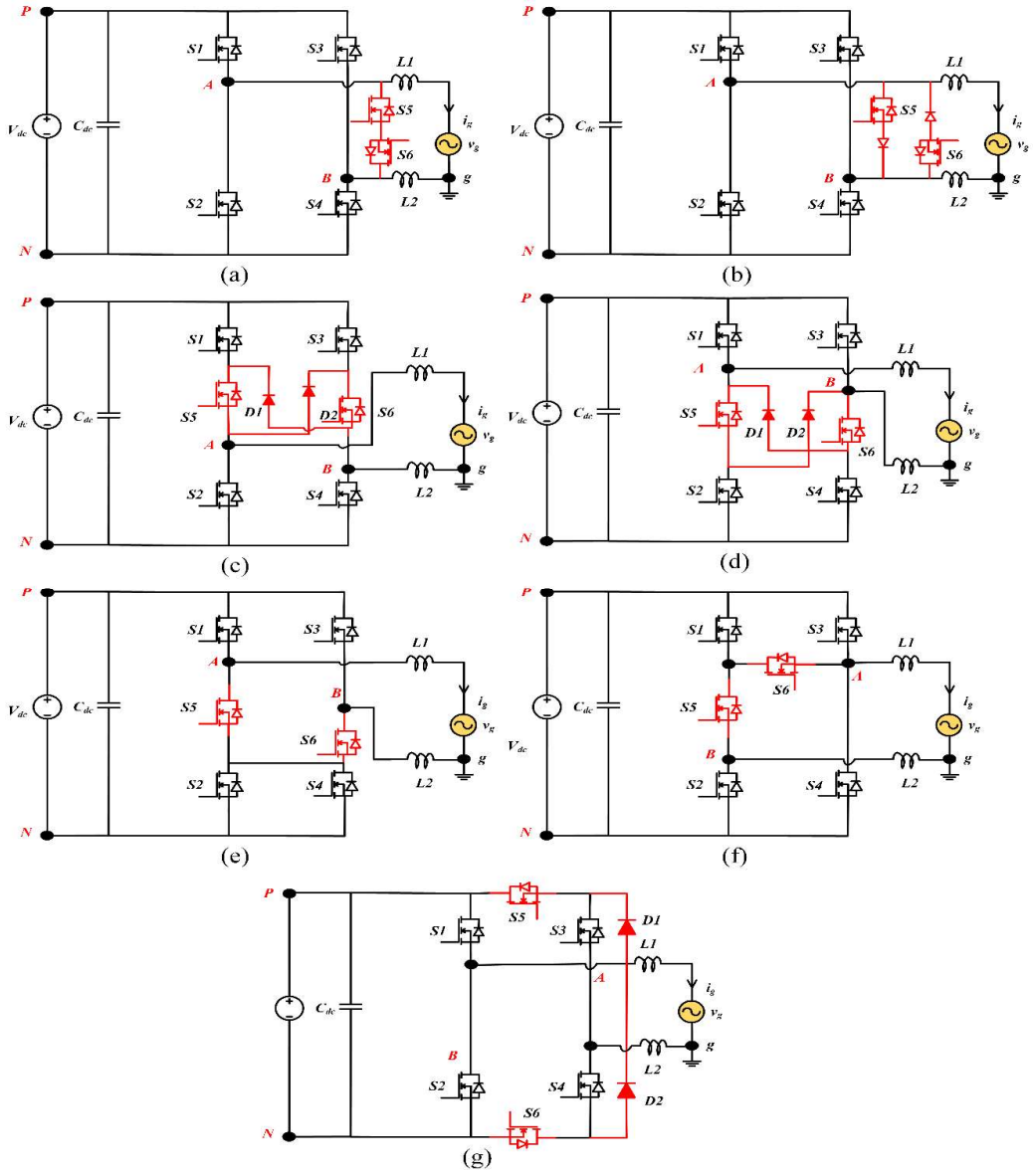


Figure 2.4 AC decoupling-based topologies. (a) HERIC structure, (b) HERIC ac-based structure, (c) H6 with diodes-1 inverter, (d) H6 with diodes-2 inverter, (e) H6-1 inverter, (f) H6 with mid-switch inverter and (g) Full-bridge inverter with mid-point switches and diodes.

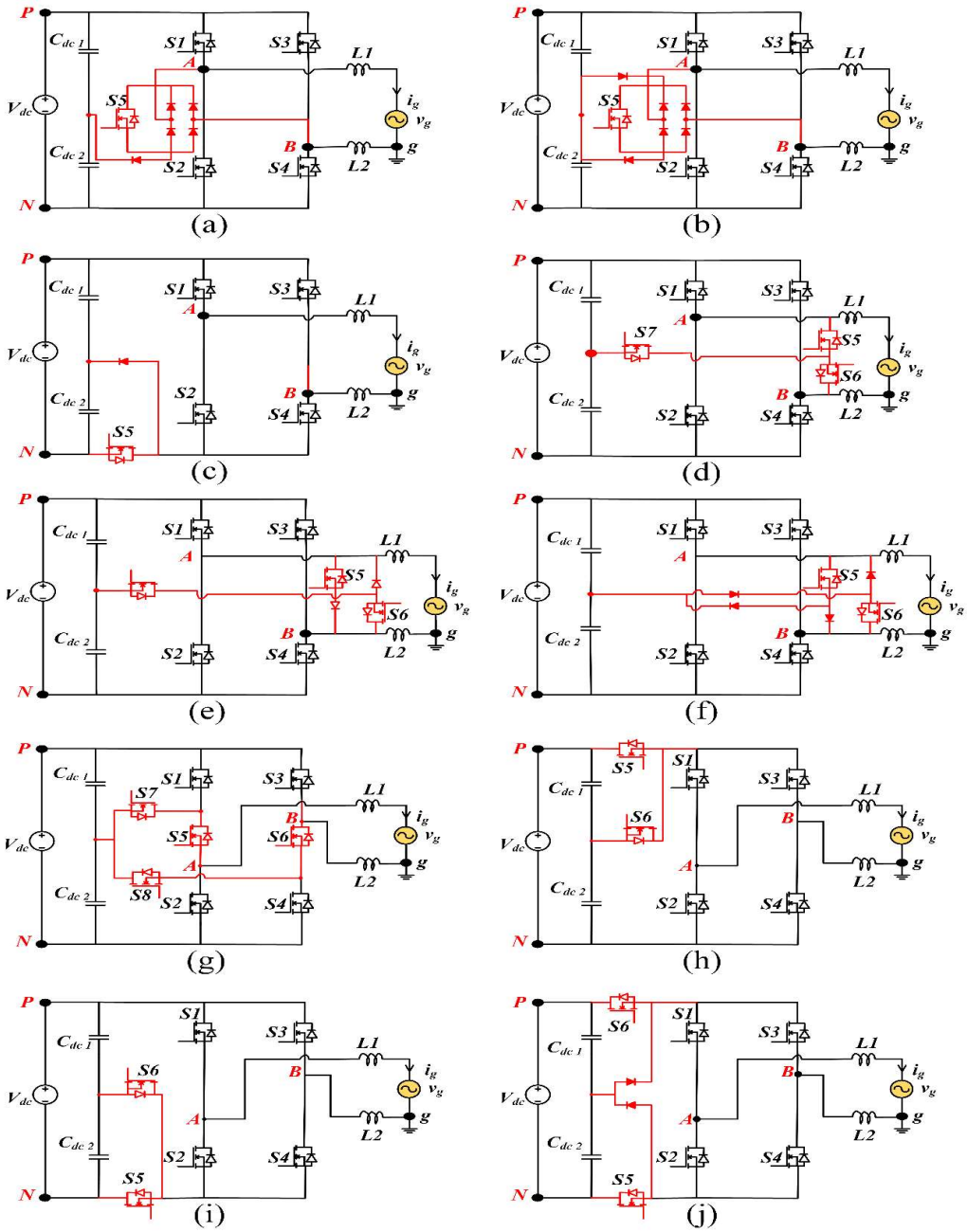


Figure 2.5 Mid-point clamped topologies. (a)HB-ZVR topology, (b) HB-ZVR-D topology, (c) H5-D topology, (d) HERIC-Active-1 topology, (e) HERIC-Active-2 topology, (f)HERIC-Active-3 topology, (g) PN-NPC topology, (h) iH5/oH5 topology, (i) oH5-1 and oH5-2 circuitry.

2.4. Overview of qZS/ZS Based Single Phase Transformerless Inverters

As the demand for PV based power generation is increasing every year and with more than 90% of world PV system are grid connected, the PV system is becoming the most dependable source of distributed generation. In section 2.2 various impedance sources were classified and studied. It was inferred that the impedance source networks with continuous input current are best suited for RES like PV. Section 2.3 provided insights into various methods to provide transformerless operation and a thorough explanation of existing topologies was presented. Although these topologies reduce leakage current, their buck nature demands greater number of PV panels to achieve grid voltage. The amalgamation of impedance source network and transformerless inverter integrates advantages like single-stage boosting, DC-AC conversion, low leakage current, low requirement of PV panels and high reliability against shoot-through.

A symmetric Z-Source integrated with HERIC structure was proposed in [68] to achieve low leakage current. As presented in Fig 2.6(a) this circuitry uses 2 diodes at positive and negative rail to form a symmetric structure and denies path to leakage current. The HERIC structure provides the freewheeling path and decouples the PV from the grid. A ZS based active and passive clamped HERIC topology shown in Fig 2.6(b) and 2.6(c) was introduced in [68], [69]. However, ZS based passive clamping circuit proved to be more efficient and more robust than ZS based active clamped topology. Fig. 2.6(d) presents a symmetric Z-source network with H5 topology to achieve constant CMV and low leakage current[70]. Well-known H5 circuit provides the decoupling of source and utility side by using additional power semiconductor devices on DC side[46]. Although ZS based transformerless topologies provided low leakage current, they still suffer from discontinuous input current[71], so the use of qZS network is encouraged for PV applications.

Fig. 2.7(a) shows the amalgamation of qZS network and HERIC based AC topology. The qZS network has benefits over ZS networks in terms of continuous input current, common ground between PV and utility, and lower voltage stress on capacitor. This proposed topology employs well-known HERIC based AC topology to decouple PV panel and grid which lowers leakage current[72]. A modified PWM scheme was also proposed in this to incorporate shoot-through technique to achieve single-stage boosting and inversion. This qZS based HERIC structure shows high efficiency and reliability due to non-conducting of body diodes of power semiconductor devices during freewheeling period and thus, providing

reactive power support. The modulation technique provided for this inverter has freewheeling period after each powering and shoot-through period which increases switching losses. To counter this, [73] proposes a qZS based transformerless inverter with modified modulation scheme to eliminate leakage current and reduce the number of switching times per cycle. Fig 2.7(b) demonstrates the topology that utilises a bidirectional branch which operates at grid frequency, providing a current path for clamping the common-mode voltage v_p to the neutral and the grid voltage v_g, for positive and negative grid cycles, respectively. Apart from reducing the leakage current the inverter achieves maximum efficiency of 95.1% which makes it most eligible option for PV based distributed system.

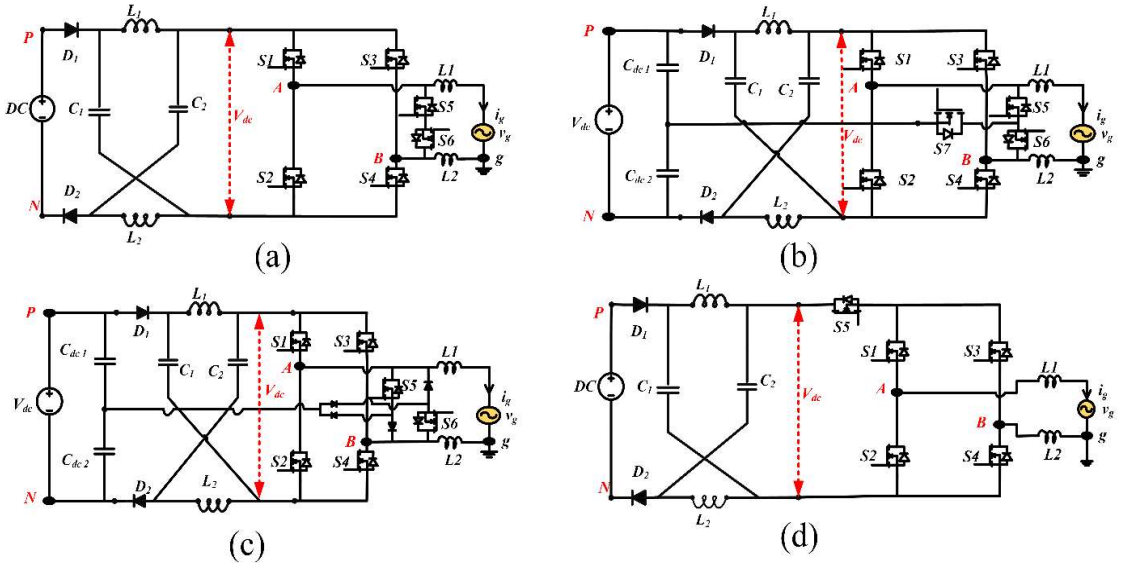


Figure 2.6 Z-source based transformerless inverters. (a) ZS-HERIC topology, (b) ZS-Active clamping HERIC, (c) ZS- Passive clamping HERIC and (d) ZS-H5 topology.

Even though the abovesaid topologies supress leakage current, there still exist double-line frequency (2ω) voltage variations in dc-link voltage[74]. To supress this [75] proposes an Active Power Filter (APF) based qZS inverter (qZSI) that compensates the dc-side double-line frequency and reduces CMV to half of the value through traditional SPWM methods. As shown in Fig 2.8, the APF circuit is made from additional LC tank circuit (L_3C_3) connected to half-bridge branch. To reduce CMV variations due to shoot-through, one of the zero-states is eliminated; this results in half reduction of CMV amplitude and nearly three-quarter decrease of leakage current.

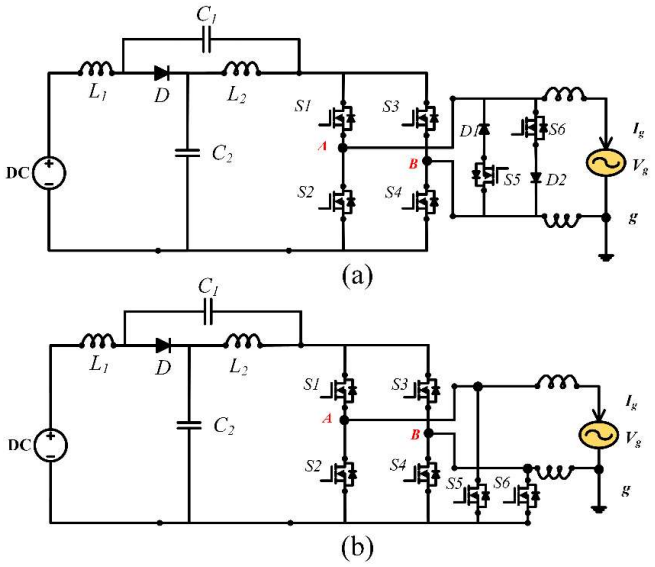


Figure 2.7 qZS based Transformerless topologies. (a) qZS based HERIC and (b) qZS based HERIC-1 topology.

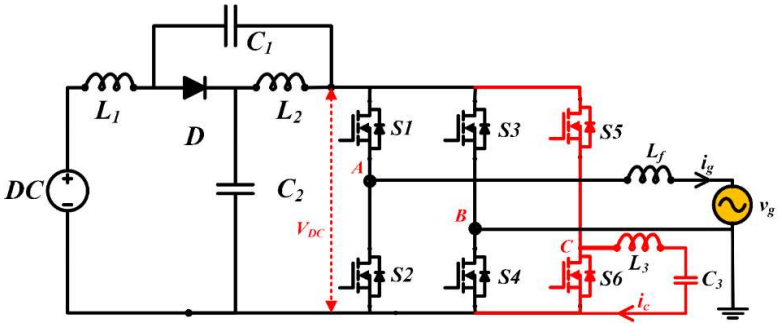


Figure 2.8 APF based qZSI topology.

2.5.Overview of qZS Based Five-Level Inverter

Recently, module and string type PV systems have become popular throughout the world due to high PV power extraction, low PV system installation effort, easy monitoring and rapid failure detection[42], [60], [76]. The conventional single-stage boost and inverting system are quite effective in achieving the advantages of above said system. However, they still require a bulky filter to feed high quality power to grid. Impedance Source based Multilevel inverters (MLI) provide appropriate boosting and inverting with stepped waveform that reduces filter size[77].

Initially, *Banaei et al* [78]introduced ZS based MLI which integrates 2 modules of ZS network and half bridge inverter to produce multilevel voltage. As shown in Fig. 2.9(a) this topology uses FB for polarity reversal and has an additional feature of modularity. The same topology can be modified using quasi-Z-source network to realize five-level output using two

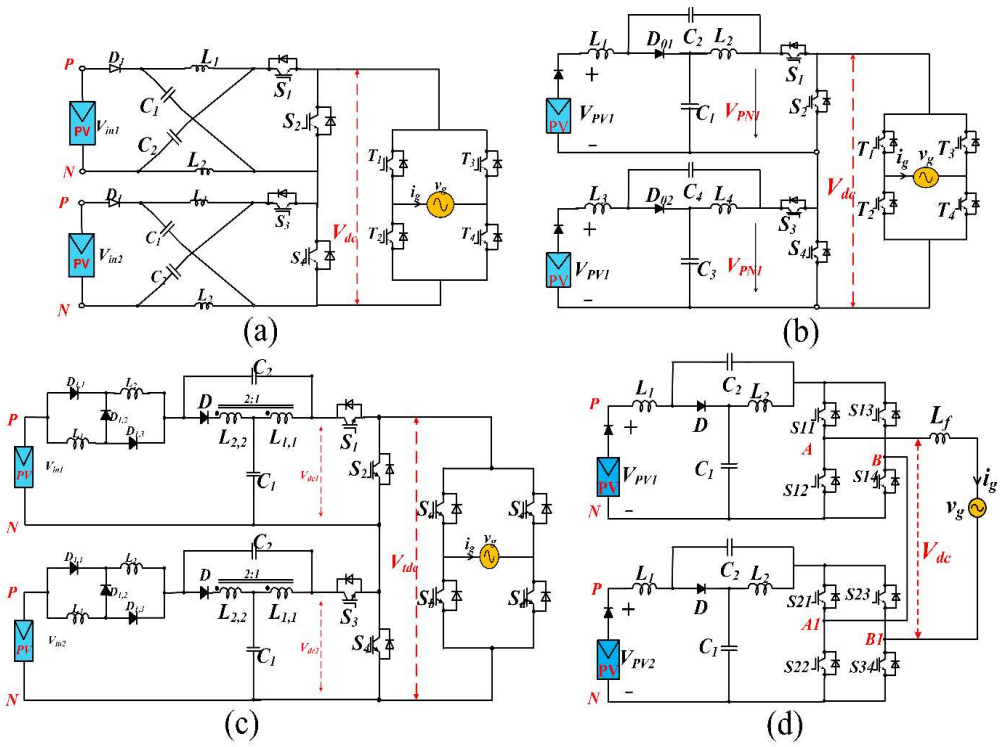


Figure 2.9 Cascaded based qZSI. (a) ZS-HBI topology, (b) qZS-HBI topology, (c) SL-qZS based HBI topology and (d) qZS-CMI topology.

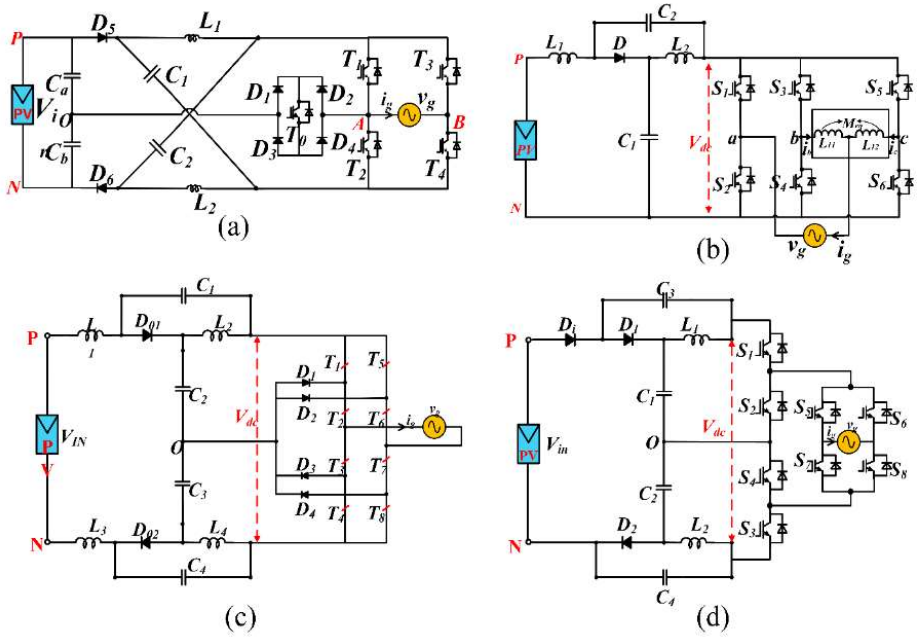


Figure 2.10 Single source based qZS-MLI (a) ZS with T-type inverter, (b) qZS with coupled inductor topology, (c) qZS-NPC topology and (d) MqZS topology.

Table 2.2 Comparative Assessment of qZS Based Five-Level Topologies

Features		MqZS	qZS-NPC	qZS with CI*	ZS-T-type	qZS-CMI	SL-qZS-HBI	qZS-HBI	ZS-HBI
Components	S	8	8	6	5	8	8	8	8
	D	3	2	1	6	2	8	2	2
	L	2	4	4	2	4	8	4	4
	C	4	4	2	2	4	4	4	4
Sources required		1	1	1	1	2	2	2	2
Remarks	Pros	High gain, Low inductor count	Lower filter requirement	High gain	Lower filter requirement	Modular	High Gain	Modular	Modular
	Cons	Discontinuous input current.	High semiconductor device count	High passive component count	Discontinuous input current.	Requires 2 sources	High Passive component count	Unbalanced Switching	Discontinuous input current.

S= Switches, D= Diodes, L= Inductors and C= Capacitors

basic units[79]. It offers CIC (continuous input current) and can be employed for PV applications, as shown in Fig. 2.9(b). The same topology is extended with replacement of one of the inductors with a switched inductor and another with coupled inductor as shown in Fig. 2.9(c)[80].

Fig. 2.9(d) illustrates a qZS based five-level inverter which utilises two basic modules of qZS with H-bridge inverter to produce the required voltage[81]–[83]. This topology achieves modularity and also facilitates independent dc-link voltage balancing by incorporating distributed maximum power point tracking which makes it a viable solution for string and multi-string PV structures.

However, the above said topologies still require two PV sources to output a five-level voltage. To address this issue a single source-based solution was provided by [84], [85]. Fig. 2.10(a) presents an ZS network with T-type inverter that produces a five-level boosted output having similar gain as traditional ZSI. A coupled inductor based qZSI proposed in [86] is presented in Fig 2.10(b). The coupled inductors are clubbed with a three-phase voltage source inverter and utilise a qZS network to achieve boosted five-level output voltage. The demerit of this topology is requirement of complex circuitry and control algorithms to drive it. Fig. 2.10(c) illustrates qZS based NPC inverter formed by front-end two back-to-back connected qZS network with traditional NPC inverter[87], [88]. The boost factor obtained is same of traditional qZS network but the use of diodes in power circuit makes it prone to damage. To reduce the component count of passive elements [89] proposed modified qZS (MqZS) inverter. This topology utilizes a lower number of passive elements to achieve similar boost as traditional qZS network. However, due to presence of diode in the input this topology is not suitable for PV applications.

A brief assessment of existing ZS/qZS based five-level inverter was performed considering their merits and demerits (see Table 2.2). All the abovesaid topologies have not considered the high frequency variations of CMV and associated leakage current. Hence, they require additional isolation transformer on grid side to provide isolation which increases the size, cost and losses of overall power system.

2.6. Problem Formulation

After reviewing various impedance source networks and impedance source based multilevel inverters following observations have been derived:

a) The use of greater number of DC sources and passive components to increase the output voltage level increases the size, cost and weight while achieving low reliability.
b) Recent research has focus on developing novel topologies that should feed the grid with reduced semiconductor devices and promise higher efficacy and reliability.
c) Impedance networks with discontinuous input current are not applicable for PV based power generation.
d) Impedance source based multilevel inverters are good solutions for PV based system due to their single stage boosting and inverting capability.
e) Reactive power support and Elimination of high frequency transitions with suitable decoupling methods for transformerless Impedance Source based MLIs will be a better proposition for PV systems.

Hence, there is still adequate scope for further research in the area of impedance source based multilevel inverters for PV based grid connected power system. The proposed research work focuses on the development of novel topologies based on the amalgamation of impedance source network and multilevel inverters for single-phase PV applications. The aim of these inverters is to provide high efficiency, single stage boosting with inversion, shoot-through immunity, reactive power support and reduced leakage current. Improved modulation scheme has also been investigated to incorporate shoot-through pulses in right amount with lower transitions and lower switching losses.

2.7. Objective of the Thesis

Based on the literature review the main objectives of the thesis are the following –

a) To minimize the number of DC sources to weaken the parasitic capacitance.
b) Keep the leakage current well below the standards.
c) To develop new power converter having features like
    i. Single stage boosting
    ii. Reactive power support
    iii. Lower power semiconductor count
    iv. High efficiency and
    v. High reliability
d) Integrate PV and Grid using proposed power converters to feed the grid.
e) Develop control strategy to make the system resistance to disturbances.

2.8. Organisation of the Thesis

This thesis is organised into six chapters. The work presented in each chapter is outlined as follows:

Chapter 1 describes the importance of renewable energy sources-based power supply system and pertinent background to the development of impedance source based multilevel inverter topologies for PV applications with reduced leakage current.

In **Chapter 2**, an exhaustive literature review based on impedance networks, single-phase transformerless topologies and impedance source based MLIs has been presented. The literature also gives insight of various methods to deny path for the leakage current and to avoid high frequency transitions across parasitic capacitance. A brief overview of existing impedance source-based inverters is also presented that reduces leakage current. Further this chapter sets the tone for the development of quasi-Z source based single-phase inverter topologies for PV based grid connected power system.

Chapter 3 investigates a qZS based new topology that outputs a five-level voltage waveform for photovoltaic applications. The inverter achieves transformerless operation and provides reactive power to the load based on its demands with modified modulation technique. The simulations and a laboratory prototype were developed to access it steady state and dynamic behaviour. A detailed comparison is also presented with existing topologies to highlight its merits.

Chapter 4 introduces a five-level qZS based H5 inverter for photovoltaic system with reduced leakage current. The inverter provides DC decoupling during zero state. The system description, various modes of operation and common mode voltage analysis are presented thoroughly. The simulations carried out and a laboratory prototype was developed to access it steady state and dynamic behaviour are discussed. A detailed comparison is also presented with existing topologies to highlight its merits.

Chapter 5 introduces a five-level qZS inverter based on improved HERIC structure for photovoltaic system with reduced leakage current. The inverter provides AC decoupling during zero state and clamps the mid-point voltage during freewheeling period. System description, various modes of operation and common mode voltage analysis are presented thoroughly. Simulations were carried out and a laboratory prototype was developed to access it steady state and dynamic behaviour. A detailed comparison is also presented with existing topologies to highlight its merits.

Chapter 6 presents a detailed comparison of qZS source based five-level inverters existing in the literature with the proposed topologies.

Finally, **Chapter 7** concludes the thesis by summarizing the contributions and indicates the direction of further research in PV based grid connected power system.

Chapter 3

QUASI Z-SOURCE BASED NPC T-TYPE INVERTER

Chapter 3

Quasi Z-Source Based NPC T-Type Inverter

3.1 Introduction

From the previous chapters, it is apparent that identifying the benefits of impedance source and multilevel inverters will enhance the performance of the photovoltaic system because of reduced device count, low cost, better efficiency and low leakage current. Therefore, in this chapter, a new configuration of NPC based qZS T-type inverter (qZS-NPC-T^2I) that outputs a five-level voltage with a reduced leakage current is proposed. A modified modulation technique has also been proposed to achieve the desired output voltage waveform. The leakage current is reduced by decoupling the DC side from the AC side to deny a path to it. A modified shoot-through technique has also been introduced for proper boosting of DC-link voltage. The modified modulation scheme not only reduces the leakage current but also balances the neutral point voltage. Also, the proposed converter possesses the ability to supply reactive power to the grid / stand-alone system. Therefore, in this chapter, design, operation and analysis of proposed configuration have been presented based on simulation and an experimental prototype model.

3.2 Operation of the Proposed NPC Based qZS T-Type Inverter

3.2.1 Proposed Topology

The schematic arrangement of the proposed configuration of an improved NPC based qZSI for single –phase applications is shown in Fig. 3.1. It comprises of an NPC arm and a T-type arm. The proposed configuration contains eight switches (S_1-S_8), four inductors (L_1-L_4), four capacitors (C_1-C_4) and four diodes (D_1-D_4). Of these, devices S_1 and S_2 constitute a bidirectional switch. The junction of the inner capacitors of the two qZS networks forms the neural point 'O'. The load is connected between the midpoint of T-type arm (which is connected to the junction of the clamping diodes of the NPC arm) and the midpoint of the NPC arms. This modification facilitates power circulation during the freewheeling period while disconnecting the load side from the source side. This converter can produce 5 voltage levels viz. 0, $\pm V_{DC}/2$ and $\pm V_{DC}$. The total dc-link voltage V_{DC} is the sum of all four capacitor voltages. The working principle of the proposed power converter and the modified modulation scheme are explained in detail in the subsequent sections. A new hybrid shoot-through

technique has been implemented to obtain the required voltage boosting and to ensure effective utilization of all components. This method also helps in balancing the neutral point 'O'.

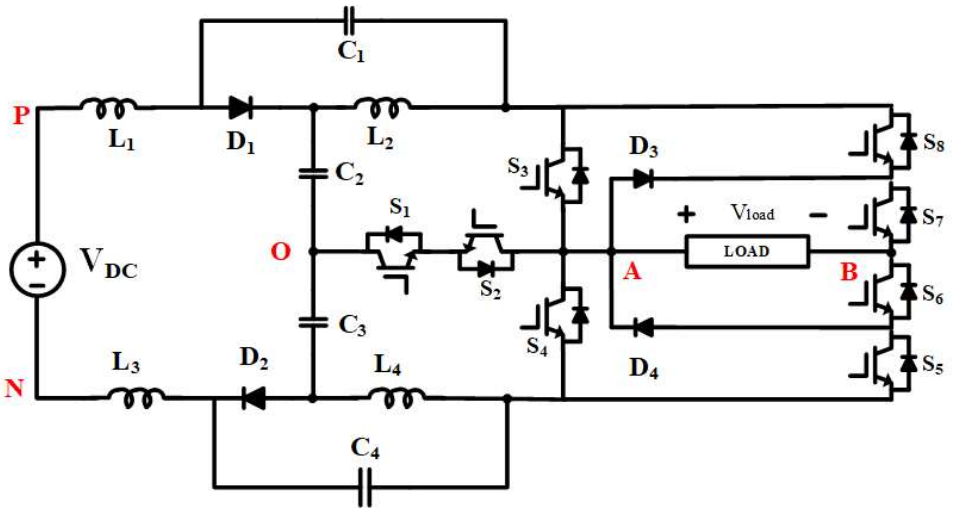


Figure 4.1 Proposed qZS based NPC inverter.

3.2.2 Working Principle

The working principle of the proposed converter is explained in detail covering the aspects of: (i) generation of output levels (ii) operation in freewheeling states (iii) operation in the shoot-through states.

Firstly, the output levels of $\pm V_{DC}/2$ and $\pm V_{DC}$ (which are the active states) may be realized in two alternative ways, accounting for 4 modes of operation. Secondly, there exist three types of shoot-through modes for the proposed converter namely: (i) the upper-half shoot-through mode (ii) the lower-half shoot-through mode and (iii) the complete shoot-through mode. Lastly, there exists a zero (i.e., a null) mode, which provides the freewheeling of power. With the aid of Fig. 3.2, these 8 modes of operation are described below:

Mode 1:- The Positive Powering Mode-1

This mode produces the voltage level of $+V_{DC}/2$. Switches S_1, S_2, S_5 and S_6 are utilized while other devices are turned off. Fig. 3.2(a) shows the direction of the current in this mode. The power is positive as both voltage and current are in the same direction.

Mode 2:- The Positive Powering Mode-2

The voltage level of $+V_{DC}$ is obtained by turning on switches S_3, S_5 and S_6. The path of current is shown in Fig. 3.2(b).

Mode 3:- The Negative Powering Mode-1

Fig. 3.2(c) shows the method of developing the voltage level of $-V_{DC}/2$. The Switching devices S_7, S_8 and the bidirectional switches are used to generate this voltage level.

Mode 4:- The Negative Powering Mode-2

Switches S_4, S_7 and S_8 are used to realize the voltage level of $-V_{DC}$. Direction of the current for positive power is shown in Fig. 3.2(d).

Mode 5:- The Freewheeling (Zero or Null) Mode

The freewheeling modes are applied at the beginning and at the end of any half period. Fig. 3.2(e) shows the details pertaining to this operation.

Mode 6:- The Complete Shoot-Through Mode

The complete shoot through (CST) mode is achieved by short-circuiting both qZS networks. The path of current for this method is shown in Fig. 3.2(f). Switches S_3 and S_4 are used to obtain this mode of operation.

Mode 7:- The Upper Shoot-Through Mode

The upper shoot-through (UST) mode utilizes only the upper qZS part to achieve the voltage boosting. This shoot-through mode is created by turning on switches S_1, S_2 and S_3 (Fig. 3.2(h)). During this time, the inductors of the upper qZS network get charged and supply power during the active mode.

Mode 8:- The Lower Shoot-Through Mode

The lower shoot-through (LST) mode is shown in Fig. 3.2(g). The path for current during the LST mode traverses through S_1, S_2 and S_4 pertaining to lower qZS.

Modes 1-4 are active states, which produce the required voltage levels, while modes 6-8 are the shoot-though states used for single-stage boosting. Assuming identical parameters for passive elements ($L_1=L_2=L_3=L_4=L$ and $C_1=C_2=C_3=C_4=C$), the following equations can be derived. The equations applicable for UST and LST are the subsets of the equations applicable for CST. The total DC-link voltage of this qZSI[87] is:

$$V_{DC} = V_{C1} + V_{C2} + V_{C3} + V_{C4} \tag{3.1}$$

The capacitor voltages of the proposed inverter assuming symmetrical characteristics can be expressed as:

$$V_{C1} = V_{C4} = \frac{D_{SH} * V_{IN}}{(1-2D_{SH})} \tag{3.2}$$

$$V_{C2} = V_{C3} = \frac{(1-D_{SH}) * V_{IN}}{(1-2D_{SH})} \tag{3.3}$$

$$B = \frac{1}{1-2*D_{SH}} \tag{3.4}$$

In eqn.3.4, the term "*B*" represents the boost factor obtained by the proposed converter, which is the same as that of conventional qZSI. The symbol D_{SH} represents the shoot-through duty cycle needed to achieve the required boosting level.

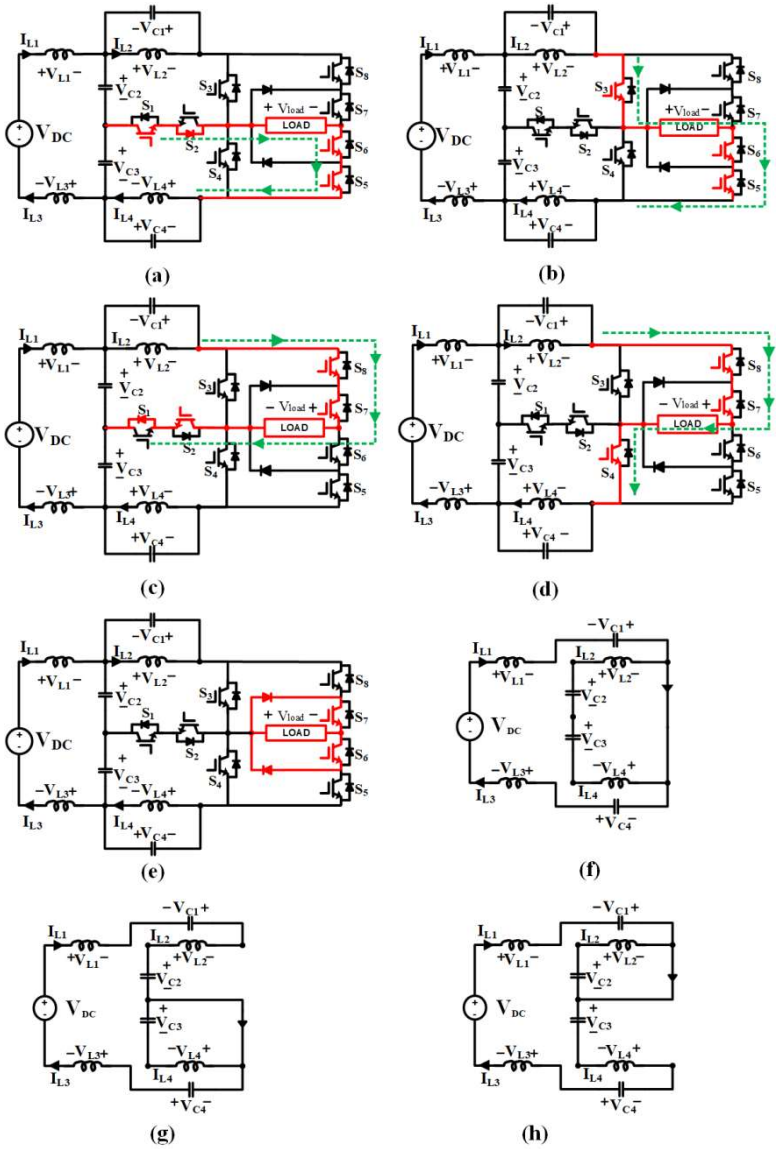


Figure 3.2 Various operating modes of the proposed converter. Fig (a)-(d) active modes, Fig (e) freewheeling mode and Fig (f)-(h) various shoot through modes.

3.2.3 Modified Modulation Scheme

In this work, a hybrid modulation technique is presented, which is derived from the sine pulse width modulation (SPWM). Phase disposition level-shift carrier waves are utilized to develop this modulation scheme for the switching devices. Table 3.1 provides details regarding the switching devices, which are required to be turned on (denoted by '1') to realize the five voltage levels, and the three shoot-through states for the proposed converter. Fig. 3.3 shows the level-shifting carrier PWM technique, which presents four carrier signals (C_1-C_4) and the sine modulating signal. Signals *A, B, C, D* are obtained by comparing modulating signal with four carrier waveforms. The signal 'G' is obtained by comparing modulating signal with zero and signal H is logical inversion of G. All of these signals are further decoded to generate the required gating signals for all the switching devices, which constitute the proposed converter.

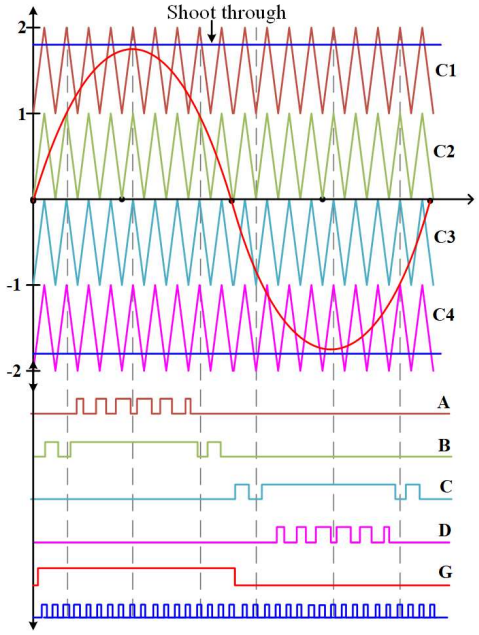


Figure 3.3 LSPWM and corresponding signals.

Based on the switching table provided below (Table 3.1), the modulating signal for each switch can be defined as:

$$\boldsymbol{S_1} = \boldsymbol{S_2} = A \oplus B + C \oplus D\ , \boldsymbol{S_3} = B, \boldsymbol{S_4} = D\ , \boldsymbol{S_5} = A\ , \boldsymbol{S_6} = G + \bar{C}G, \boldsymbol{S_7} = \bar{A}G + \bar{G}\ , \boldsymbol{S_8} = C \quad (3.5)$$

Moreover, a hybrid-shoot through technique has been applied to achieve appropriate voltage boosting, which employs three types of shoot-through modes viz. the LST, the UST and CST (the circuits for these shoot-through modes have been presented in the previous

section)[90]. LST and UST are respectively applied in the positive and negative half cycles while realizing $+V_{DC}/2$ and $-V_{DC}/2$ levels. In contrast, CST is applied while switching $+V_{DC}$ and $-V_{DC}$ levels (i.e., during both positive and negative half cycles).

Table 3.1 Switching States of the qZS-NPC-T²I

Output Levels	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	Switching State
V_{DC}	0	0	1	0	1	1	0	0	Active
$V_{DC}/2$	1	1	0	0	1	1	0	0	Active
0	1	1	0	0	0	1	1	0	Zero
$-V_{DC}/2$	1	1	0	0	0	0	1	1	Active
$-V_{DC}$	0	0	0	1	0	0	1	1	Active
0	0	1	1	0	0	0	0	0	Upper Shoot through
0	1	0	0	1	0	0	0	0	Lower Shoot through
0	0	0	1	1	0	0	0	0	Complete Shoot through

3.3 Passive Component Selection

In a symmetrical dual-quasi structure, all passive components have similar values. One of the important factors in the calculation of the ratings of the passive components is the addition of low frequency ripple (at a frequency of '2ω') to high frequency ripple[91]. Of these two ripple components, the low frequency ripple component is typically caused by the circulation of double frequency component between the source and the load, while the high-frequency component is caused by shoot-through states. The inductance (3.6) and the capacitance values (3.7) and (3.8) are calculated using these formulae[88]:

$$L = \frac{4*V_O^2*(1-2D_{SH})*T_S*D_{SH}}{(1-D_{SH})*K_L*P_O} \tag{3.6}$$

$$C_1 = C_4 = \frac{T_S*P_O*(1-D_{SH})^2}{4*k_{C1}V_O^2(1-2D_{SH})} \tag{3.7}$$

$$C_2 = C_3 = \frac{T_S*P_O*(1-D_{SH})*D_{SH}}{4*k_{C1}V_O^2(1-2D_{SH})} \tag{3.8}$$

In the above formulae, the symbols K_L, k_{C1} *and* k_{C2} denote the ripple factors of the inductors and the capacitors respectively. A clear boundary between continuous conduction mode (CCM) and the discontinuous conduction mode (DCM) is established in [87], [88].

3.4 Control Structure

In this work, two types of control structures are considered, namely, the standalone system and grid connected system. They are described in detail in the following paragraphs.

3.4.1 Stand-Alone System

A closed-loop control system consisting of two-loops is used in the stand-alone control structure (Fig. 3.4). The objective of this control system is to maintain the dc-link voltage constant during the load and source disturbances[92]. From Fig. 3.1, it may be noted that the DC-link voltage is the sum of all 4 capacitor voltages. Hence four voltage sensors are needed to measure the peak value of the DC-link voltage. However, exploiting the symmetric nature of the proposed back-to-back qZS networks to advantage, only two capacitor voltages (V_{C1} and V_{C2}) are sensed using two voltage sensors. The sum of these two voltages is then multiplied by a factor of 2 to estimate the peak dc-link voltage. Thus, the closed-loop system uses 3 sensors in all; two for sensing the capacitor voltages and one for sensing the inductor current.

The outer loop consists of a PI controller, while the inner loop consists of a simple proportional (P) controller. In the outer loop, the measured value of the peak DC-link voltage is compared with its reference value. To compensate the error (if any) between the desired and the actual values of the DC-link voltage, the PI controller determines the required inductor current and sets this value as the reference for inner controller, which controls the inductor current. This reference inductor current is then compared with the actual (i.e., the sensed) inductor to determine the required value of the shoot-through duty cycle.

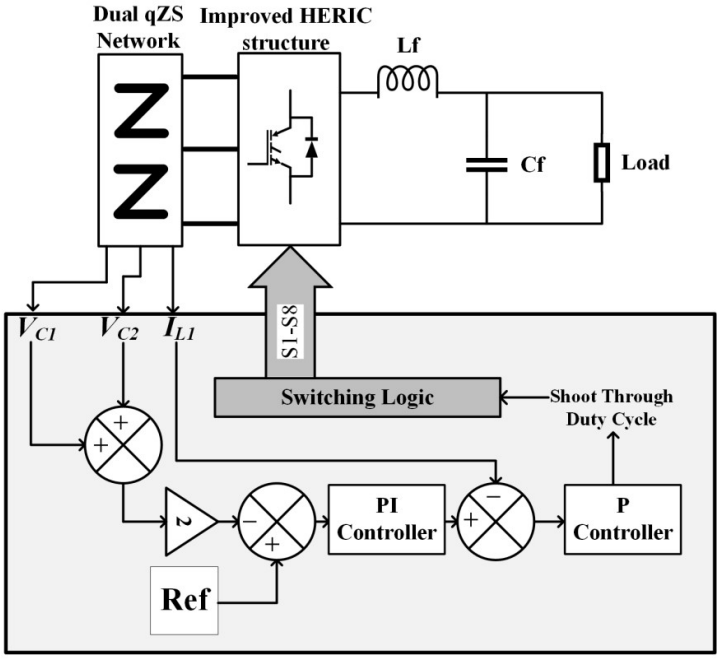


Figure 3.4 Closed loop control scheme for standalone system.

3.4.2 Grid-Connected System

The performance of the proposed power converter has also been studied in the grid connected mode. In this mode of operation, there are two objectives: (i) maximum power point tracking (MPPT) (ii) realization of unity power factor (UPF).

In this work, MPPT for a given value of irradiance is accomplished by controlling the shoot-through duty cycle (denoted by the symbol 'D_{sh}')[93]. Perturb and Observe (P&O) method is implemented to obtain the required value of reference, which is then compared with the top and bottom carrier waves (Fig. 3.3) to generate the shoot-though pulse. The shoot-through pulse is then logically manipulated to create the upper, lower and full shoot-through modes in the inverter.

Fig. 3.5 presents the control structure to realize the objective of controlling the grid current to achieve optimal injection of active power into the grid, which requires UPF operation[94]. The actual DC-link voltage is obtained by the addition of the capacitor voltages V_{C1} and V_{C2}, which are sensed and multiplied by a factor of '2' (as the total DC-link voltage is the sum of two identical back-to-back connected qZS network). The actual DC-link voltage is then compared with the reference value and the error between them is compensated by a PI regulator. The output of the PI regulator represents the regulated error which is expected to be zero. The output signal of the PI controller is then subtracted from the value obtained by dividing PV power by peak grid voltage to obtain the magnitude of the peak current, which needs to be injected into the grid to regulate the DC-link voltage and to achieve MPPT.

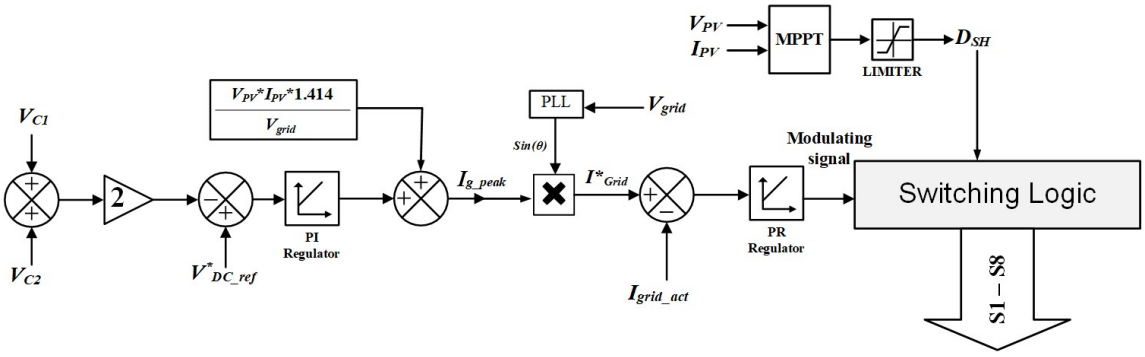


Figure 3.5 Closed loop control scheme for PV-grid connected system.

To achieve the UPF operation, a PLL is employed to synchronize the grid current with the grid voltage. The generated waveform template is multiplied with the magnitude of the peak value of the reference current to generate the sinusoidal reference for grid current[95]. The reference grid current is then compared with the actual (i.e., the sensed) grid current and

the resultant error is fed to a Proportional - Resonant (PR) controller to generate the modulation signal. The modulation signal is then compared with the carrier signals to implement LSPWM scheme (Fig.3.3).

3.5 Leakage Current Analysis

The equivalent common mode model of the proposed qZS-NPC based PV system and its simplified version are presented in Figs. 3.6(a) and 3.6(b) respectively[75]. The parameters R_g and R_f respectively represent the average ground impedance and the internal resistance of the filter. From Fig.3.6(a), the common mode voltage for the inverter can be estimated as:

$$V_{CMV} = \frac{V_{An}+V_{Bn}}{2} \tag{3.9}$$

where V_{AN} and V_{BN} respectively denote the phase-leg voltages of the inverter with respect to ground (Fig. 3.1)[15].

The common mode current (CMC) or the leakage current flows from the PV panel to the ground (N) due to the time-variant nature of the common mode voltage. The leakage current is related to the parasitic capacitor by:

$$i_{leakage} = C_{PV}\frac{dV_{CPV}}{dt} \tag{3.10}$$

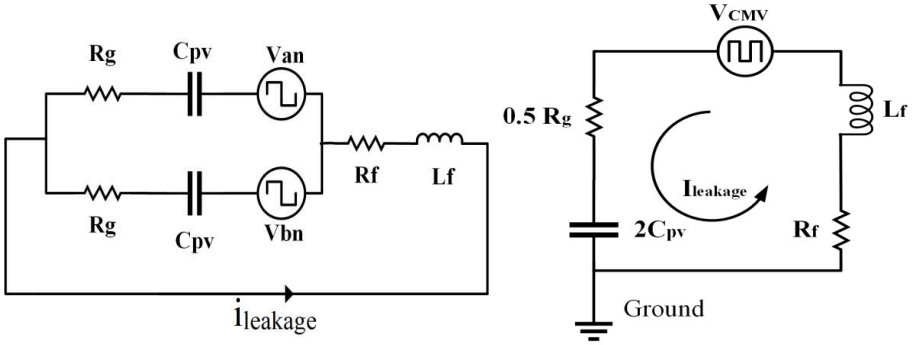
Where, $i_{leakage}$ is the leakage current in ground and C_{PV} and V_{CPV} are the capacitance and the voltage across the parasitic capacitor found from the PV panels to the ground.

As the leakage current is caused mainly due to variation in CMV, the high frequency components in CMV strongly influence it. Thus, the CMC can be suppressed by:

i. Making CMV constant
ii. Reducing the high frequency variation
iii. Reducing CMV

Following the operating principle presented in Section-3.2, it may be observed that the inverter has 3 principal working modes, namely, active-, zero- and shoot-through modes. The shoot-though mode, which is inserted between the active and the zero state, mainly contributes to variation of CMV. As three different types of shoot-through are inserted to get the required boosting factor, CMV also varies based on which type of shoot-though is applied, causing the voltage across the parasitic capacitor to vary. The proposed topology employs an active filter (Fig. 3.7), which accomplishes the tasks of both filtering the output voltage and suppressing CMV. An active LCL filter is obtained by splitting the filter capacitor into 2 equal parts and connecting the mid-point of these capacitors to the negative rail of the input DC source[96]. This type of structure not only filters out the high frequency components in

the output voltage, but also checks the high frequency variation in voltage across the parasitic capacitor, thereby reducing the leakage current significantly.



(a) (b)

Figure 3.6 Common Mode circuit representation of the inverter. (a) Equivalent circuit, (b) Exact equivalent circuit.

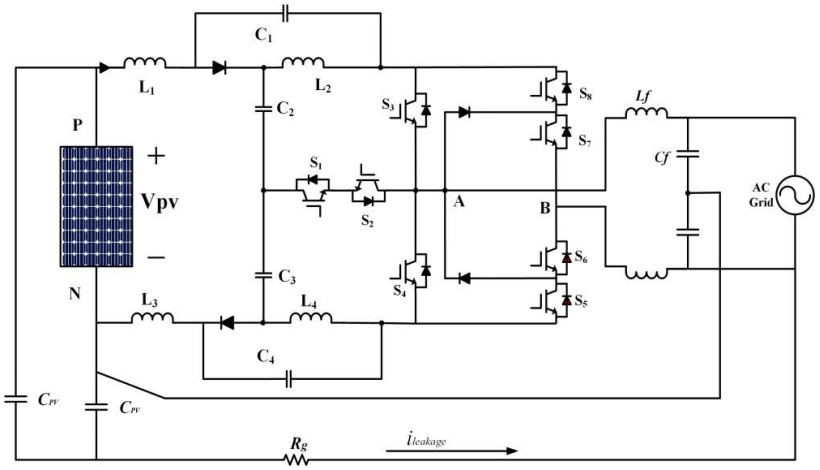


Figure 3.7 Proposed topology with split LCL filters to reduce high frequency variation in CMV.

3.6 Results and Discussions

3.6.1 Simulation Results

The working principle of the proposed power circuit was verified with simulation studies using MATLAB/Simulink and experimentally validated with a scaled down prototype. The operating conditions and the converter parameters are enumerated in Table 3.2. The values of passive components were calculated using equations (3.6)-(3.8). Fig. 3.8(a) shows all of the five voltage levels produced by the proposed inverter. Fig. 3.8(b) shows the fluctuating DC-link voltage. It is evident that whenever the shoot-through state is switched, the DC-link is short circuited and its voltage is brought down to zero. While the application of LST or UST

the voltage floats at $0.5V_{DC}$. It may also be noted that the complete shoot-through (CST) mode is employed while operating at the voltage level of V_{DC}.

Table 3.2 Simulation and Experimental Parameters

Parameters	Values
Power	500 watts
Input voltage	100 V
Grid Voltage (rms)	110 V
Inductor L_1-L_4, L_f	1mH, 4mH
Capacitor C_1-C_4, C_f	1000µF, 2µF
Switching Frequency	10kHz
Controller	Xilinx Spartan 6 FPGA
Switches (S_1-S_8)	STGB20H60DF
Diodes(D_1-D_4)	MURS1560

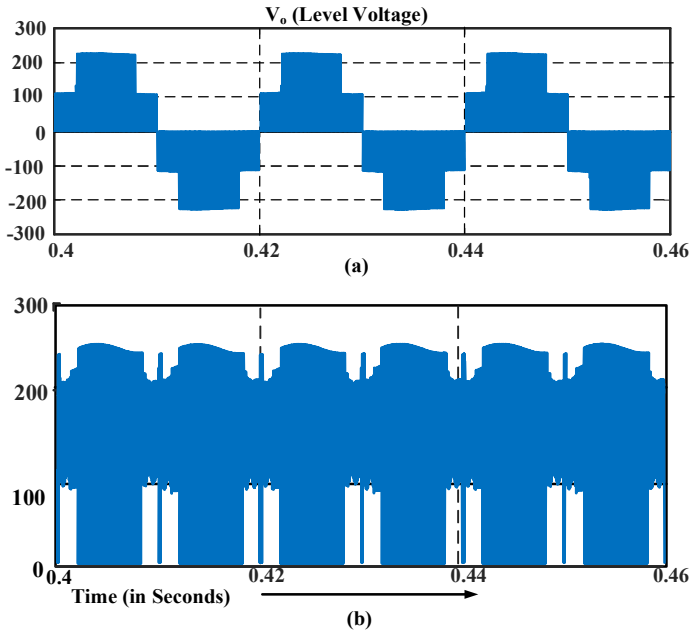


Figure 3.8 Simulation results for proposed inverter. (a) Output level voltage; (b) DC-link voltage.

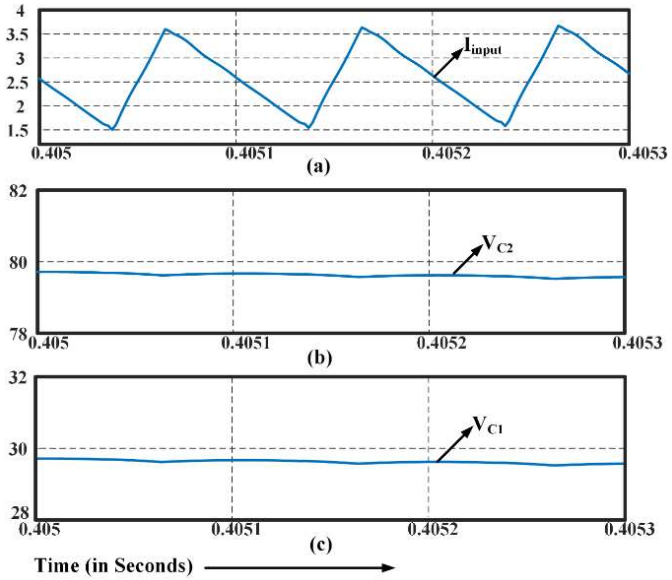


Figure 3.9 Dynamics of passive components. (a) Inductor current for L_1. (b) Voltage across capacitor C_2. (c) Voltage across capacitor C_1.

In this simulation study, the input voltage was 100V and the AC output RMS voltage 110V (or a peak value of 155V). When the qZS networks were operated with a shoot-through duty ratio of 0.27, a boost factor of 2.2 (app.) was obtained (eqn.3.4). By noting the peak value of the DC-link voltage (Fig. 3.8(b)), it is evident that the required boost factor was obtained. From the circuit diagram of the proposed power converter (Fig. 3.1), it may be noted that the boosted DC-link voltage was obtained by summing up all the four capacitor voltages. Accordingly, Fig. 3.8(b) shows that the peak value of the boosted DC-link voltage is the sum of the four capacitor voltages.

Further, Fig. 3.9(a) shows the inductor current of the inverter. The inductor is energized during the shoot-through mode and its current increases. During the non-shoot-through modes the inductor current decreases. Figs. 3.9(b) & 3.9(c) respectively show the voltages across capacitors C_2 and C_1 (79.6V and 29.8V). The voltages across the other two capacitors (C_3 and C_4) would be identical to the ones shown owing to topological symmetry of the back-to-back connected qZS networks (Fig. 3.1). The capacitor voltages are very close to theoretically computed values given by eqns. 3.2 &3.3 (81.6 V and 30.18 V respectively). Thus, the simulated results support the theoretical analyses presented in the earlier sections.

The capability of providing a free-wheeling path during zero-period renders the reactive power handling capability to the proposed converter. This feature is demonstrated with the simulation results shown in Fig. 3.10. Figures 3.10 (a), 3.10(b) and 3.10 (c) respectively

show the voltage (blue trace) and the current (red trace) across the load for UPF, 0.8 (lag) and 0.8 (lead) respectively.

As stated earlier, the modulation scheme adopted in this work not only provides the reactive power capability to the converter but also helps in the suppression of leakage current. As explained in the previous section, the split filter provided at the output reduces the high frequency variation in CMV appearing across the parasitic capacitor. Fig. 3.11 shows the simulation results pertaining to the suppression of CMC. The CMV and the voltage across the parasitic coupling capacitor are shown in Figs 3.11(a) & (b) respectively. Fig. 3.11(c) displays the leakage current flowing from the source to the load. With a peak value of less than 20mA, the proposed power converter complies with VDE 0126-1-1 grid standards.

The dynamic performance of the proposed converter against both source and load disturbances for a stand-alone system is presented in Fig. 3.12 and 3.13 respectively. The closed loop control system aims to regulate the dc-link voltage to a constant value by controlling the shoot-through duty cycle. The reference value for the dc-link voltage (peak value) was kept at 220V. Fig 3.12 shows the dynamic response of the proposed converter for the source disturbance, wherein the source voltage was suddenly varied from 100V to 120V. The corresponding change in the shoot-through duty is presented in Figs 3.12 (b). From Fig. 3.12 (c), it may be noted that the peak value of the DC-link voltage was regulated by the closed-loop controller (Fig. 3.4), as it gets back to its original value following the disturbance. The impact of the source disturbance on the load voltage and the current is shown in Fig. 3.12 (d), in which it is evident that the load voltage (and hence the load current for a constant load impedance) is practically immune to source disturbance. This is attributed to the electrical inertia introduced by the filtering elements.

The dynamic response of the proposed converter against a sudden load disturbance is presented in Fig. 3.13. Despite a sudden change in the load current from 2A to 5A (due to the reduction of the load impedance), the output voltage doesn't show any significant difference. The reason for this is: (i) modulation index is kept constant (ii) DC-link voltage is regulated with a fast closed-loop controller (iii) there is a large electrical inertia at the output stage.

Fig. 3.14 shows the characteristics of the PV panels used to assess the performance of the proposed converter using both off-line and real-time simulation studies. Fig. 3.15 shows off-line simulation results for the grid connected system. The dynamic behavior of the proposed converter is studied when irradiation decreases, while the temperature is constant.

Fig. 3.15(a) shows the change in irradiance from 900 watts/m^2 to 700 watts/m^2, which is applied at 1 sec of simulation. The corresponding change in power can be observed in Fig. 3.15(b). The change in irradiation forces P & O algorithm to adjust the shoot-through duty factor to re-attain MPP.

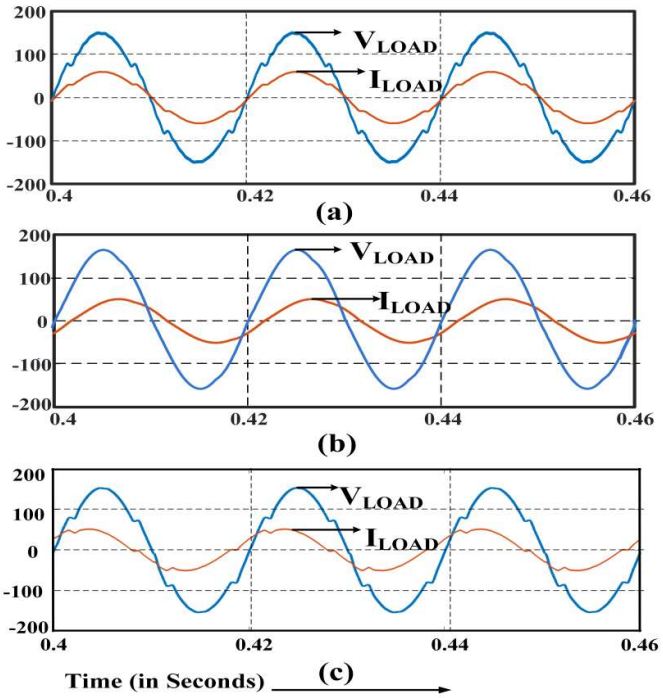


Figure 3.10 Reactive power capability of converter. Output of converter for various load pf (a) UPF; (b) 0.8 Lagging PF and (c) 0.8 Leading PF.

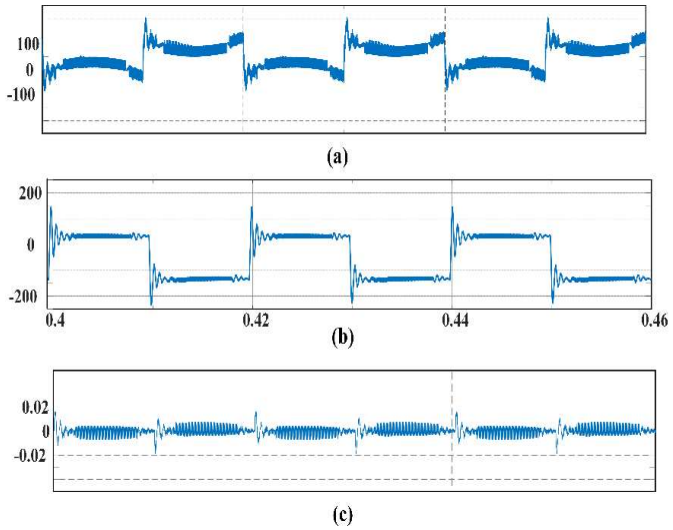


Figure 3.11 Common mode parameters of the inverter (a) CMV; (b) Voltage across parasitic capacitor and (c) Leakage current.

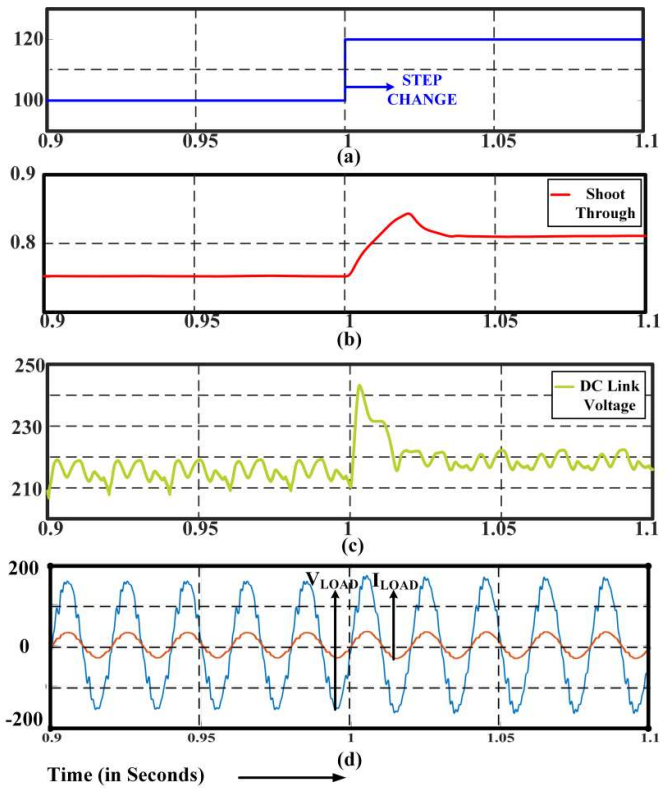


Figure 3.12 Transient response of system for disturbances on source side. (a) Step change in input voltage; (b) Change in shoot though duty cycle; (c) Peak DC link voltage and (d) Output voltage and current.

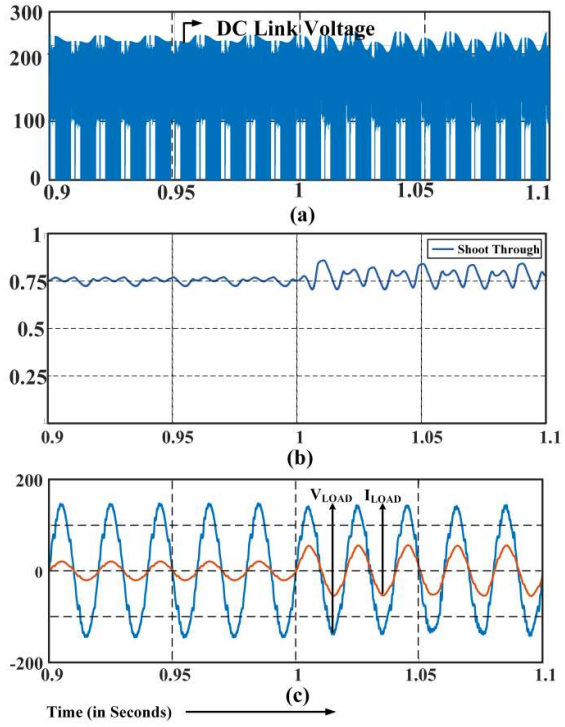


Figure 3.13 Transient performance of the system for step change in load. (a) DC-link voltage; (b) Shoot through duty cycle and (c) Output voltage and current

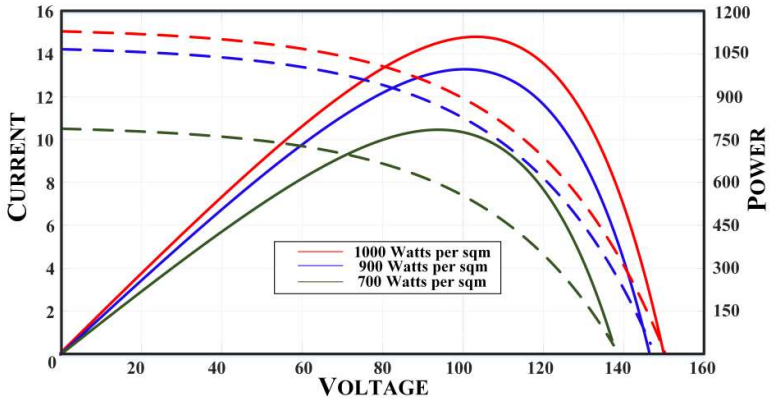


Figure 3.14 P-V and I-V curve of the PV array.

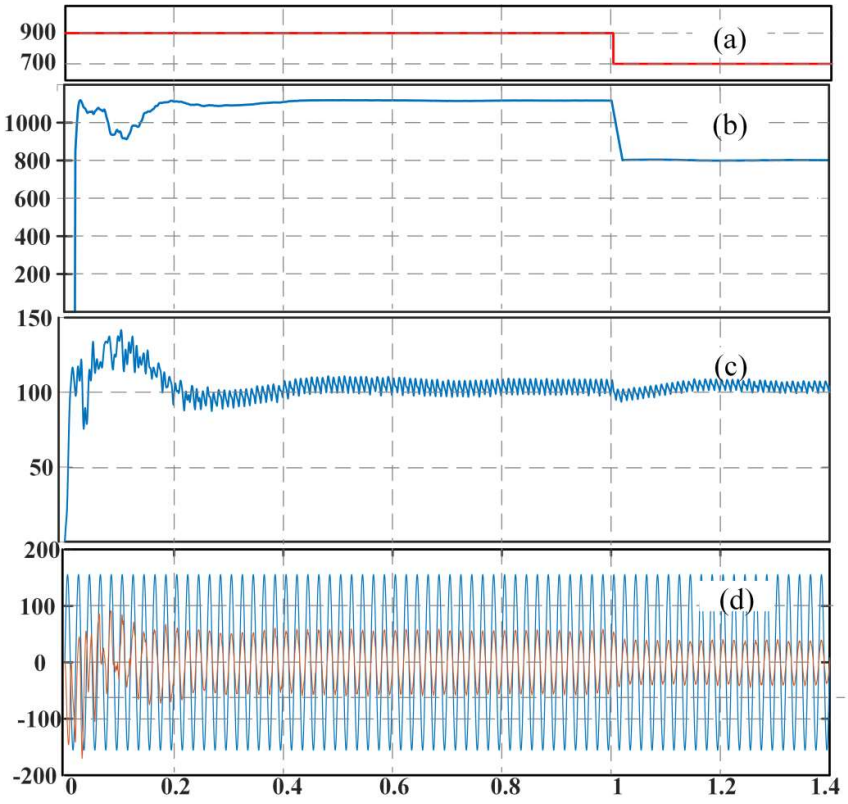


Figure 3.15 Grid based simulation for step change in irradiance (a) Change in irradiance; (b) Change in PV array's power level; (c) PV voltage and (d) Grid voltage and current.

The PV voltage and the PV current clearly indicate the effect of re-adjusting the shoot-through duty factor and the subsequent re-attainment of MPP with changed irradiation. The decreased PV current (due to the decrease of irradiation) manifests as a decrease in the grid current, as the grid voltage is regulated by the regulation of the DC-link current (at a constant modulation index). The waveforms of the grid voltage and the grid current are presented in

Fig. 3.15(d). It may be observed that following the environmental disturbance, the grid current decreases. It may also be observed that, owing to the control effort put in by the control system shown in Fig. 3.5, the grid current is always in phase with grid voltage resulting in the UPF operation.

The PV panels used for simulation are rated for 95 watts with the open-circuit voltage (V_{OC}) 25.9V and the short-circuit current (I_{SC}) of 3.36A. A total number of 12 panels were utilized. Six of them were connected in series to obtain the required voltage rating and 2 such strings connected in parallel to obtain a total power rating of approximately 1150 watts. The P-V characteristics for the array can be seen in Fig. 3.14 for various irradiance conditions at a temperature of 25ºC. Perturb and observe algorithm (P&O) was used to reach the maximum power point (MPP). This algorithm is widely used because of its simplicity and ease of implementation. The algorithm is evaluated for every 1 millisecond and outputs the shoot through duty cycle value.

3.6.2 Experimental Results

To validate the theoretical analyses and the simulation results a 500 W laboratory prototype was developed and tested. The experimental setup of the proposed inverter is shown in Fig. 3.16. The passive components were designed using the formulae presented in equations (3.6)-(3.8). The power converter was realized with the IGBT switching devices (STGB20H60DF) while the controller and the PWM scheme were implemented with FPGA Spartan 6 by Xilinx. Fig. 3.17 (a) shows the experimental results pertaining to the steady state performance of the dc-link voltage and the output voltage, while Fig. 3.17(b) presents the current flowing through the inductor (L_1) and the voltage waveforms across the capacitors C_1 and C_2 in steady state (Fig. 3.1). The waveforms of the output voltage and the load current in steady-state condition and the reactive power handling capability of the converter are illustrated in Fig. 3.18. The figure shows the converter output for resistive and lagging power factor loads. There is a slight dip or flatness in the output voltage of the converter. This is due to the occurrence of the shoot-through mode along with the active voltage vector around transition periods.

The performance of the converter in terms of suppressing leakage current is shown in Fig. 3.19. The top and bottom traces respectively show leakage current and CMV across the parasitic branch. It is evident that the proposed modulation technique is capable of suppressing leakage current and reducing high frequency variation in CMV. It may also be noted that the

maximum value of the leakage current is only 20 mA, which is well below the German VDE 0126-1-1 grid standards[43].

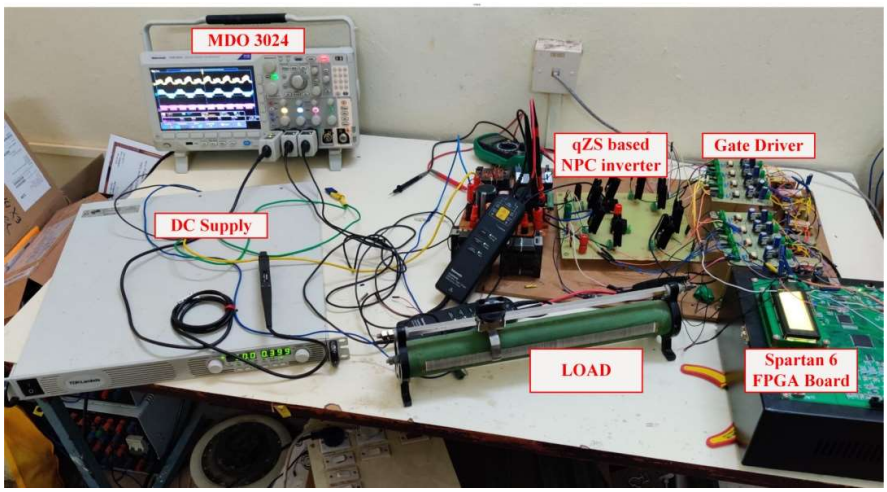
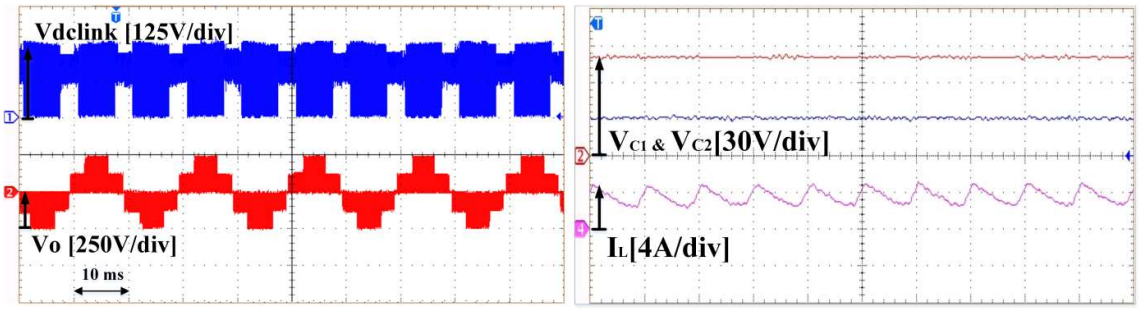
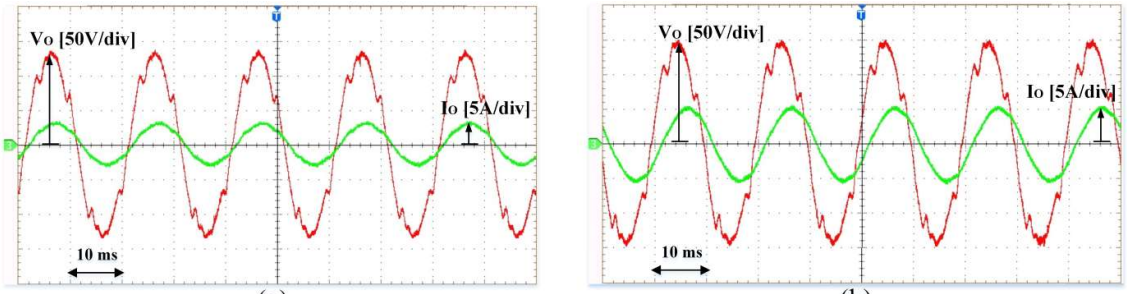


Figure 3.16 Hardware setup of the proposed inverter.



(a) (b)

Figure 3.17 Experimental results for proposed system in steady state. (a) DC link Voltage and Output level voltage; (b) Capacitor voltages and inductor current.



(a) (b)

Figure 3.18 Experimental waveform demonstrating reactive power capability of the inverter (a) UPF; (b) 0.8 Lagging PF.

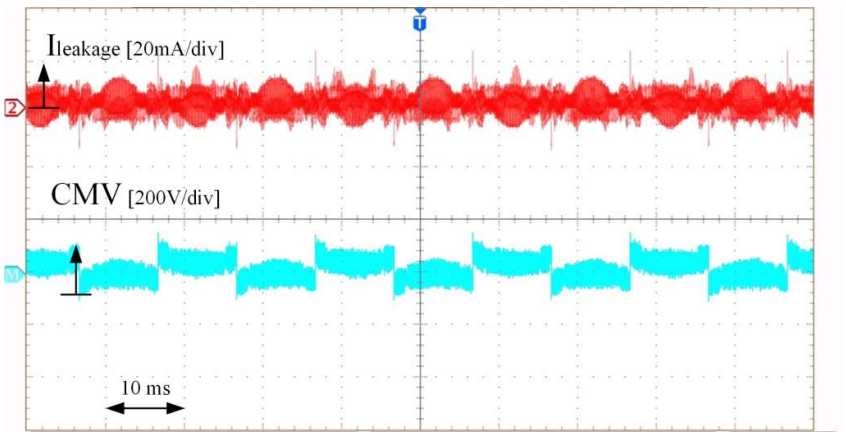


Figure 3.19 Experimental results for leakage current and common mode voltage

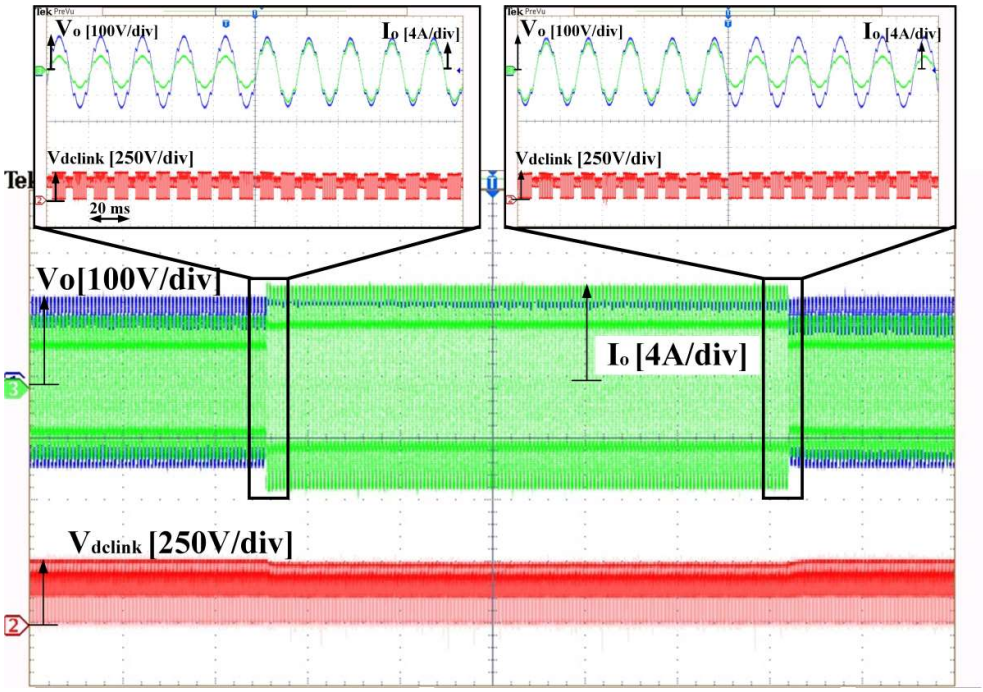


Figure 3.20 Experimental results for transient response of system for step change in load.

The dynamic performance of the proposed power converter is presented in Figs. 3.20 and 3.21. Fig. 3.20 shows the dynamic behavior of the system against a sudden load disturbance. The load current is suddenly increased from 2A to 4A, and then back to 2 A after a while. It can be observed that, when the load is changed, the dc-link of the converter is regulated at the desired value by the control system shown in Fig. 3.4. Fig. 3.21 shows the dynamic response of the converter, when it is subjected to a sudden source disturbance. The control system (Fig. 3.4) maintains the DC-link voltage at the desired value when the input voltage is suddenly changed from 100V to 120V. Thus, the steady-state and the dynamic

performance of the proposed converter are verified experimentally in the standalone mode of operation.

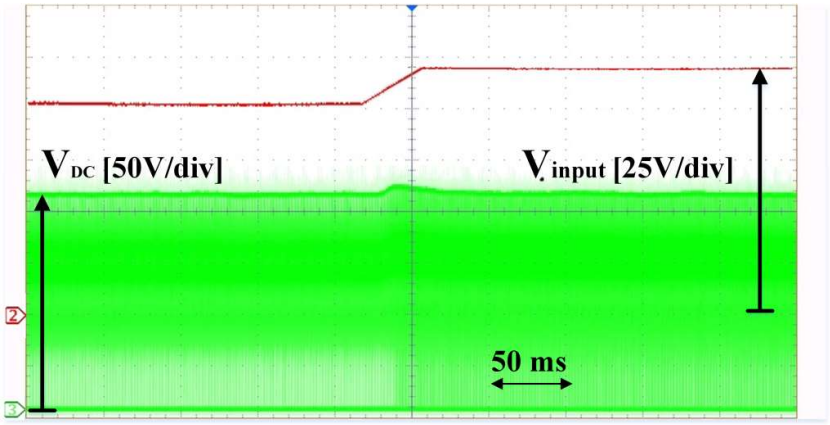
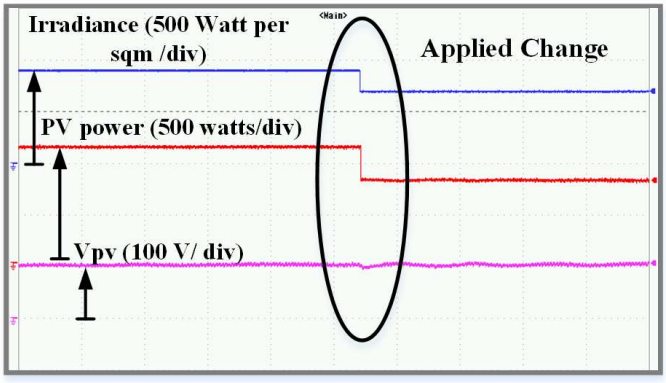
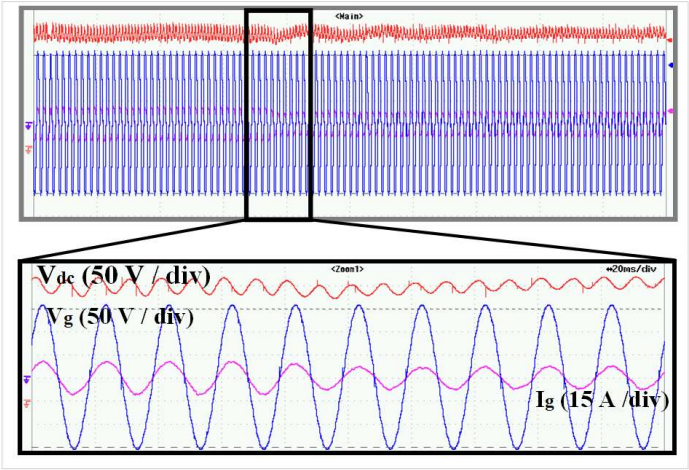


Figure 3.21 Experimental result demonstrating transient response of system for change in source voltage.



(a)



(b)

Figure 3.22 Results for the grid connected PV system. (a) Dynamics of input side parameters irradiance, PV array power and Voltage across PV array; (b) Dynamics of output side parameters peak dc link voltage, grid voltage and current respectively.

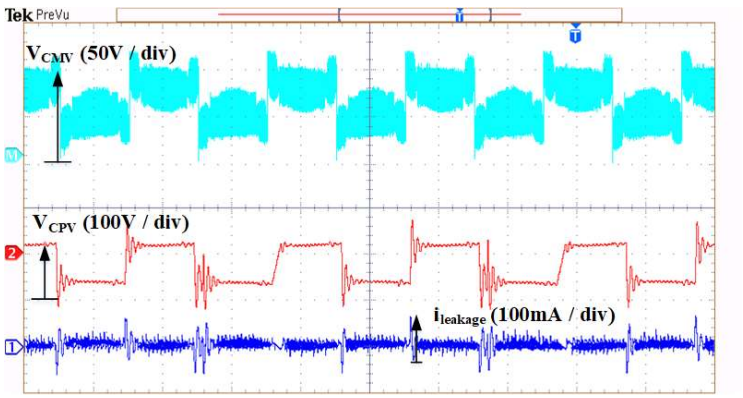


Figure 3.23 Results for common mode properties during grid connected mode.

Further, as reported in[97], the performance of the proposed converter in the grid-connected mode is assessed using real-time simulation studies using Opal-RT 4500 real-time simulator platform. The real-time simulation results are presented in Fig. 3.22. Fig. 3.22(a) shows that, following a change in irradiance (from 900 watts/m^2 to 700 watts/m^2), both PV power and PV voltage change. The MPPT algorithm then quickly restores the PV voltage by adjusting the shoot-through time. This action regulates the DC-link voltage as shown in the top trace of Fig. 3.22 (b). The decrease in PV current causes a corresponding change in the current injected by the converter into the grid. These real-time simulation results reinforce the results obtained with off-line simulations in demonstrating the effectiveness of the proposed topology for standalone/grid connected PV applications.

The common mode parameters of the system in grid connected mode are shown in Fig. 3.23. The waveforms of common mode voltage (V_{CMV}), Voltage across parasitic capacitor (V_{CPV}) and the leakage current ($i_{leakage}$) can be observed. It may be noted that the proposed control scheme works well in grid connected mode keeping the leakage current ($i_{leakage,\ RMS} = 22mA$) of proposed converter well under the German standards VDE-0126-1-1($i_{leakage,\ RMS} \leq 300mA$).

3.6.3 Efficiency Curve

The power-efficiency curves for the converter topologies considered in the previous section for comparative analyses are presented in Fig. 3.24(a). It is observed that the maximum efficiency of around 95.3% can be achieved by the proposed topology. The efficiencies of all of the power converters, which are being compared, are estimated using the thermal module of Powersim (PSIM) software which imports the real characteristics of switches and the passive components as described in [98]. The performance of these converters was evaluated at various loads keeping the input voltage (V_{in} = 100 V), modulation

index (m = 0.7) and shoot-through duty factor (D_{sh} = 0.27) constant. The losses of the converter were calculated using the method provided in [75], [83]. From Fig. 3.24(b) it is evident that the calculated and simulated loss values agree well with each other which proves the validity of the efficiency curve. Though the numbers of the passive components are the same for all of these single-phase topologies (Table 3.2), the proposed power converter displays higher efficiency due to reduced number of switching devices and the non-conduction of the internal diodes during the free-wheeling period.

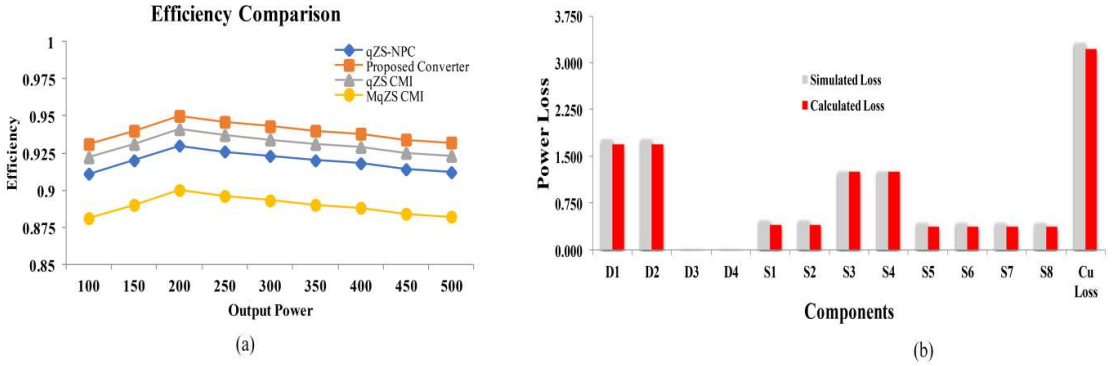


Figure 3.24 Efficiency comparisons of various qZS based inverters. (a) Efficiency vs. Power output for various converter; (b) Comparison graph between calculated loss and simulated loss.

3.7 Comparison with Existing Topologies

This section reports about the performance of the proposed qZS-NPC-T2I vis-à-vis the existing qZS based single-phase topologies reported in the literature. Three five-level topologies were considered for the comparative evaluation, namely (i) qZS-NPC[87], (ii) single phase qZS based CMI [83] and (iii) Modified qZS (MqZS)[89].

Table 3.3 presents the number of passive elements, switching devices and the source requirement of the proposed topology with the topologies mentioned above. It may be noted that the proposed topology requires the same number of passive elements, compared to qZS-NPC and qZS-CMI. However, it requires 2 more inductors, compared to MqZS. While the proposed topology requires fewer number of diodes than qZS-NPC, it needs one and two more diodes compared to qZS-CMI and MqZS respectively. Though the proposed topology needs a higher number of diodes, only 2 of them were used during the zero-period. Also, the proposed topology requires only one voltage source to generate the five-level output voltage waveform, putting it on par to other topologies except qZS-CMI (which needs two sources).

Table 3.3 Component Comparison of Proposed Topology with Existing Topologies

Components	qZS-NPCT^{2}I	MqZS modified hybrid inverter	qZS-CMI	qZS-NPC
Inductors	4	2	4	4
Capacitors	4	4	4	4
Diodes	4	3	2	6
Switches	8	8	8	8
DC sources	1	1	2	1
Boost Factor	$1/1-2D_{SH}$	$2/1-2D_{SH}$	$1/1-2D_{SH}$	$1/1-2D_{SH}$

From Table 3.3, it is evident that the boost-factor obtained by the proposed inverter is the same as that of qZS-NPC and a single module of qZS-CMI. However, it is lower than the boost-factor obtained with MqZS base inverter by a factor of 0.5.

Table 3.4 compares all of the aforementioned topologies with respect to voltage stress (which determines the voltage rating) across each component, taking AC output RMS voltage as the base value. It may be noted that, similar to the topologies qZS-CMI and qZS-NPC, all of the switching devices of the proposed inverter are subjected to equal voltage stress. In the MqZS topology, some of the switches are required to handle a higher voltage stress (double compared to three previous topologies). The capacitors and diodes are required to handle the same voltage stress in all of the four topologies.

Table 3.4 Voltage Stress Comparison

Components	qZS-NPCT^{2}I		MqZS modified hybrid inverter		qZS-CMI		qZS-NPC	
Switches	$\frac{1}{\sqrt{2}(1-D)}$		$\frac{1}{\sqrt{2}(1-D)}, \frac{\sqrt{2}}{(1-D)}$		$\frac{1}{\sqrt{2}(1-D)}$		$\frac{1}{\sqrt{2}(1-D)}$	
Capacitor	C_2, C_3	$\frac{1}{\sqrt{2}}$	C_1, C_2	$\frac{1}{\sqrt{2}}$	C_2, C_3	$\frac{1}{\sqrt{2}}$	C_1	$\frac{1}{\sqrt{2}}$
	C_1, C_4	$\frac{1}{\sqrt{2}}\frac{D}{1-D}$	C_3, C_4	$\frac{1}{\sqrt{2}}\frac{D}{1-D}$	C_1, C_4	$\frac{1}{\sqrt{2}}\frac{D}{1-D}$	C_2	$\frac{1}{\sqrt{2}}\frac{D}{1-D}$
Diodes	$\frac{1}{\sqrt{2}(1-D)}$		$\frac{1}{\sqrt{2}(1-D)}$		$\frac{1}{\sqrt{2}(1-D)}$		$\frac{1}{\sqrt{2}(1-D)}$	

3.8 Summary

This chapter proposed a new qZS based five-level inverter topology for photovoltaic applications. The proposed converter is essentially a single-stage boost converter, consisting

of a dual-qZS structure at the input side, and the connection of an NPC arm and T-type arm at the output side. It supports the freewheeling of power without using any of the anti-parallel diodes of the active switches. This feature, along with its single-stage boosting capability, improves the efficiency and the reliability of the converter. The modulation technique adopted in this work, along with the split filter at the output, reduces leakage current by reducing high-frequency variation across the parasitic coupling capacitance. Simulation and experimental results indicate that the leakage current is well within the limits stipulated by VDE 0126-1-1 grid standards.

The steady-state and the dynamic performances of the proposed power converter, in the stand-alone mode of operation, are assessed by carrying out off-line simulation studies and experimentally verifying them with the aid of a laboratory prototype. For the grid-connected mode of operation, real-time simulation studies were carried out to validate the same.

To sum up, it is shown that the proposed single-phase, five-level inverter topology displays the features of: (i) single stage boosting, (ii) reactive power handling capability, (iii) low leakage current and, (iv) higher efficiency compared to the other comparable topologies. Owing to these advantages, it is envisaged that this converter could be an attractive proposition for PV generation in the years to come.

Chapter 4

DUAL QUASI Z-SOURCE BASED IMPROVED H5 INVERTER

Chapter 4

Dual Quasi Z-Source Based Improved H5 Inverter

4.1. Introduction

The configuration proposed in the previous chapter incorporates benefits like single-stage boosting, reduce device count, low voltage stress and low leakage current. However, the presence of diodes makes the system less reliable and lacks modularity. To address the above said issues, a new configuration based on dual qZS network integrated with modified H5 inverter is investigated. The leakage current that flows through the resonant circuit formed due to lack of galvanic isolation mustn't be denied any path. Modified H5 inverter adds additional power semiconductor device on the positive rail of DC side that turns off during freewheeling period while clamping the mid-point voltage, thereby restricting the circulation of leakage current. This power circuit configuration is constituted by two mutually dependent sub-converters, in that a front-end quasi-Z-source (qZS) part is integrated to a back-end multilevel inverter (MLI). The MLI provides the shoot-through state to qZS, while qZS provides pulsating DC input to MLI. In this chapter, a modified modulation scheme, which is based on the employment of phase-disposed and level-shifted carrier signals, has been employed to reduce leakage current. To reduce the leakage current further, a passive filter is employed to eliminate high frequency variations across parasitic capacitance. The working principle of the proposed power converter and the effectiveness of the modulation scheme have been validated with simulation studies in both standalone and the grid-connected mode. Therefore, in this chapter, design, operation and analysis of proposed configuration have been presented based on simulation and an experimental prototype.

4.2 Dual Quasi Z-Source Based Improved H5 Inverter

The proposed qZS based transformerless 5-level inverter is presented in Fig. 4.1, which consists of 3 parts. The first part is the dual quasi-Z source, comprising four inductors (L_1-L_4), four capacitors (C_1-C_4) and two diodes (D_1, D_2). The dual quasi-Z source network is formed by connecting two conventional quasi-Z sources[88]. The junction of the inner capacitors of the two quasi Z-sources forms the neutral point of the dc-link, as shown in Fig. 4.1. The quasi-Z source impedance network has an advantage over traditional Z source inverter in that it results in a continuous input current and a reduced capacitor rating, making it suitable for PV systems. The second part consists of 5-level inverter, which is capable of the

following features: (i) single stage boosting, (ii) reactive power control, (iii) isolation of the source and grid sides, (iv) clamping of neutral point voltage to load and (v) provision of freewheeling paths for various loads. The 5-level inverter itself is obtained by integrating a H-bridge (S_1-S_4), an additional switch connected to positive rail (S_5) and a bidirectional switch (S_6 and S_7). There are two purposes to the bidirectional switch. Firstly, it helps in producing an extra voltage level by connecting the point- *A* to the midpoint of the dual qZS structure (point *O*, Fig. 4.1). Secondly, it helps in clamping the midpoint voltage to the load/ grid in order to avoid variations in CMV during zero periods. Finally, part 3 consists of a notch filter, which consists of 4 filter inductors and 2 capacitors where the midpoint of the connection is clamped to the negative rail of the source[99]. This type of connection not only filter the stepped output voltage of 5-level inverter; it also filters high frequency variations in voltage across the parasitic PV capacitor, which in turn reduces leakage current.

This basic topology can easily be extended to realize cascaded operations. The basic unit of a cascaded structure are shown in Fig. 4.2(a) and 4.2(b) respectively. The details of the operation and various working modes are explained in the following sections.

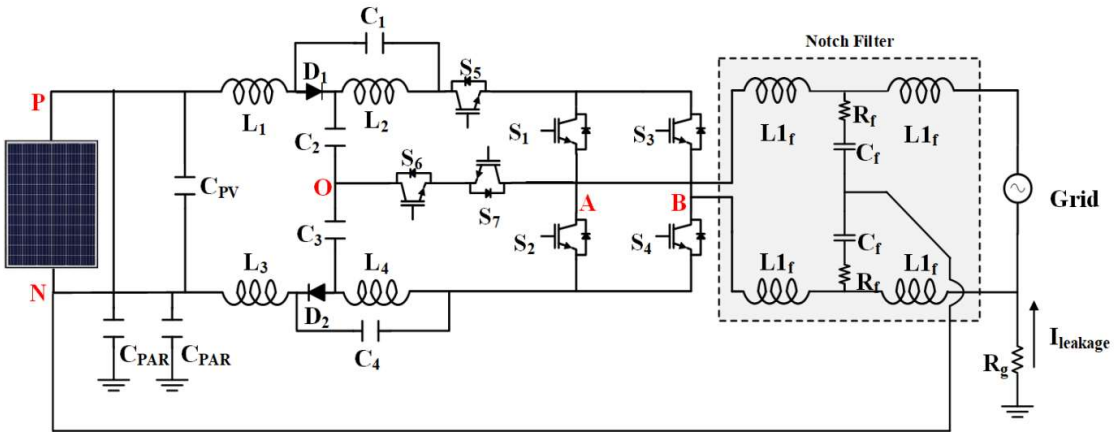


Figure 4.1 Proposed dual qZS based improved H5 inverter.

4.3. Operating Modes and Modified Modulation Scheme

As mentioned in the earlier section, a modification is proposed to an existing switching scheme for the proposed power converter to realize the advantages. Four level-shifted and phase disposed carrier signals along with one modulating signal are used to generate the switching signals that determine the level of operation for the proposed 5-level inverter (Fig. 4.3).

The working modes of the proposed power converter are divided into three categories, namely, active, shoot though and free-wheeling modes. While the active states produce the

required voltage levels, the shoot- through and the free-wheeling modes are used for boosting the input voltage and supporting the non-unity PF loads.

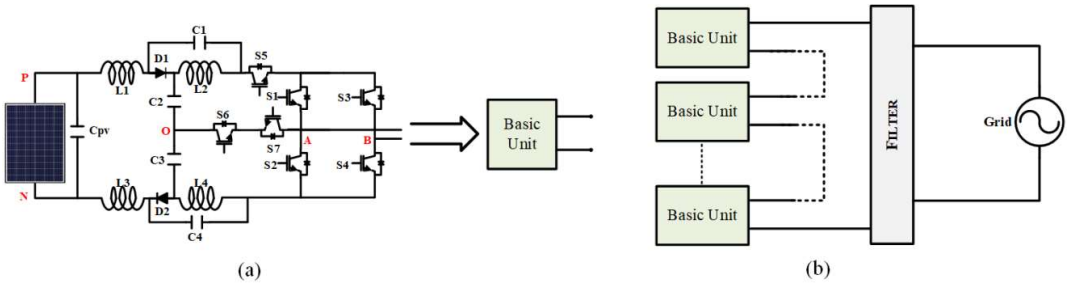


Figure 4.2 Generalised form (a) Basic unit; (b) Generalized structure for N-level inverter.

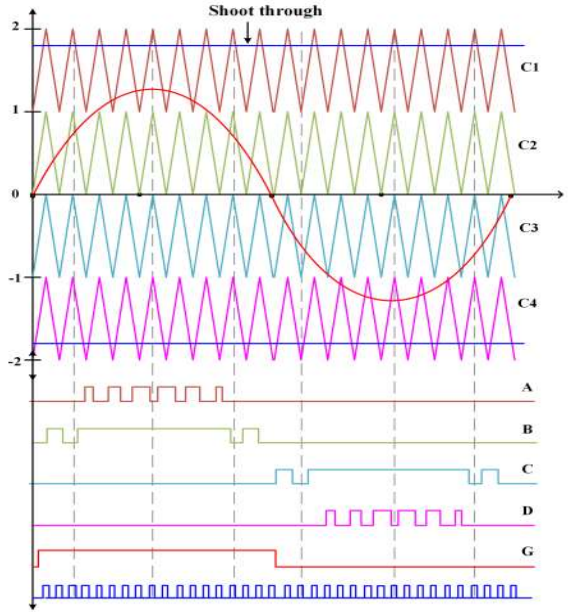


Figure 4.3 Level shift pulse width modulation scheme.

The active states are divided into 4 parts, which produce four voltage levels, namely, $\pm V_{dc}/2$ *and* $\pm V_{dc}$. The method of generating the voltage level of $+V_{dc}/2$ is shown in Fig. 4. 4(a). In this mode, switches S_4, S_6 and S_7 belonging to the lower qZS network are turned on to produce the required voltage level. Similarly, switches S_1, S_4 and S_5 are turned on to generate the voltage level of $+V_{dc}$ as shown in Fig. 4.4(b). On the negative side, the voltage level of $-V_{dc}/2$ is obtained by turning on switches S_3, S_5, S_6 and S_7 (Fig. 4.4(c)). In order to generate the voltage level of $-V_{dc}$, the devices S_2, S_3 and S_5 are turned on, as shown in Fig. 4.4(d).

The shoot through states, which render the feature of voltage boosting, are categorized into two types; the Upper Shoot Through (UST) and the Lower Shoot Though (LST) states. The UST (Fig. 4.4(e)) and LST (Fig. 4.4(f)) are applied to the converter during the positive

and the negative values of the voltage levels respectively. The modified implementation of the shoot through mode avoids the problem of switching the voltage level to zero, while switching between the levels of $+V_{dc}/2$ and $+V_{dc}$.

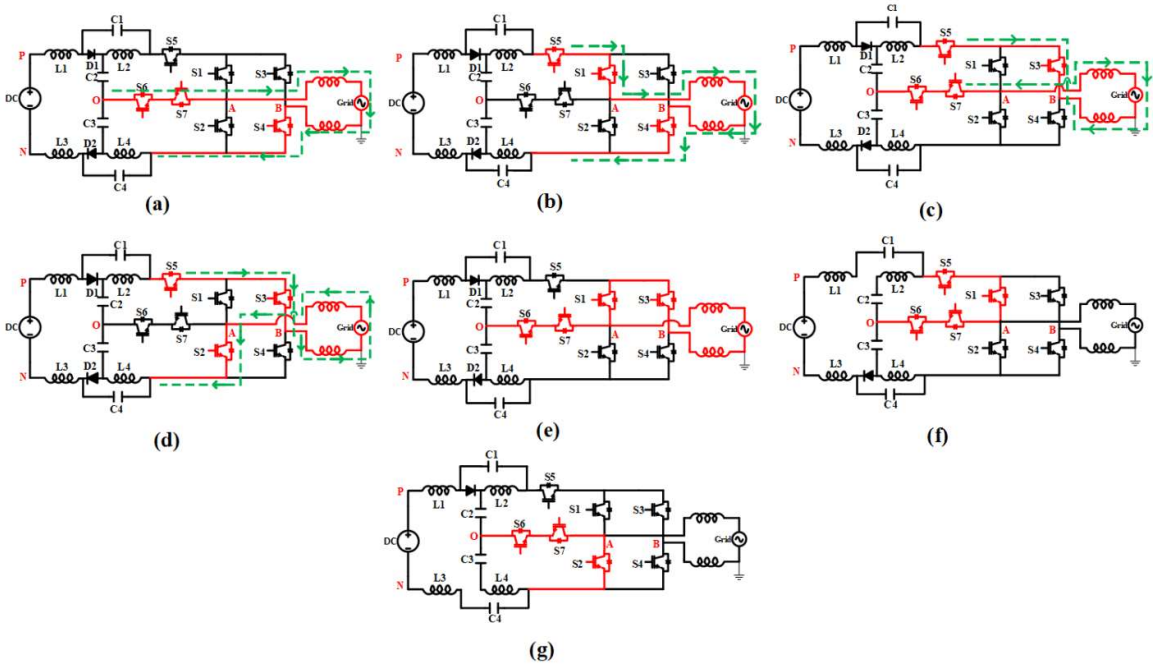


Figure 4.4 Working modes of the proposed inverter: (a) active switches for generating$+V_{dc}/2$; (b) active switches for generating $+V_{dc}$; (c), active switches for generating$-V_{dc}/2$; (d) active switches for generating $+V_{dc}$; (e) active switches for generating zero state; (f) active switches for generating upper shoot though; (g) active switches for generating lower shoot through.

Analysis of the working modes presented in Fig. 4.4 and Table-4.1 paves way to devise an improved switching scheme. It may be noted from Fig. 4.1 that the branch, constituted by S_6 and S_7, can conduct bidirectionally in a controlled manner. When allowed to conduct, this branch connects point A (Fig. 4.1) to the midpoint of two capacitors ($C_2$and C_3), facilitating the generation of voltage levels ($\pm V_{dc}/2$). Also, this branch clamps the neutral point voltage to the load in the free-wheeling period to keep the CMV as low as possible (Fig. 4.4(f)). During the free-wheeling period, switches S_1 and S_3 are turned ON and switch S_5 is turned off to isolate the grid side from the source side. This method of isolation helps in reducing the leakage current in inverter[51]. The free-wheeling state facilitates reactive power compensation for both leading and lagging loads. Whenever the output voltage and the output current do not have the same zero-crossing instants, switches S_1 and S_3 conduct, providing a path for the freewheeling current during the time-gap between two zero-crossing events. At

appropriate intervals, the shoot through is inserted using the switches S_1, $S_2$and S_5 to obtain the required voltage boosting. The five basic PWM signals *A*, *B*, *C*, *D* and *G* (Fig. 4.3) are logically manipulated to derive the gating signals for individual switching devices of the proposed converter.

Table 4.1. Switching Table for Proposed Converter

S1	S2	S3	S4	S5	S6	S7	Output Voltage	Switching State
0	0	1	0	0	1	1	$0.5V_{DC}$	Active
1	0	1	0	1	0	0	V_{DC}	Active
0	0	0	1	1	1	1	$-0.5V_{DC}$	Active
0	1	0	1	1	0	0	$-V_{DC}$	Active
1	0	0	1	0	1	1	0	Zero
1	0	0	0	1	1	1	0	UST
0	1	0	0	0	1	1	0	LST

The switching logic to derive the gating signals of all switching devices is provided in (4.1).

$$S_1 = B + \bar{A}G + \bar{C}\bar{G} + UST,$$
$$S_2 = D + LST,$$
$$S_3 = A,$$
$$S_4 = C + \bar{A}G + \bar{C}\bar{G},$$
$$S_5 = B + C + UST,$$
$$S_6 = S_7 = (A \oplus B) + (C \oplus D) + \bar{A}G + \bar{C}\bar{G} \quad (4.1)$$

The condition to apply the shoot through state is given by:

$$D_s + m \leq 1 \quad (4.2)$$

where D_s and m respectively denote the values of the shoot-through duty cycle and the peak modulation index. Assuming symmetrical values of passive components ($L_1=L_2=L_3=L_4$ *and* $C_1=C_2=C_3=C_4$) the peak dc-link value is given by:

$$\hat{V}_{DC} = V_{C1} + V_{C2} + V_{C3} + V_{C4} \quad (4.3)$$

where, $V_{C1}, V_{C2}, V_{C3}, V_{C4}$ represent the average capacitor voltages of qZS capacitors. The capacitor voltages and the boost factor can be determined using the voltage balance

equations for inductors over one switching period[83]. The voltages across the capacitors and the boost factors are obtained as follows:

$$V_{C1} = V_{C4} = \frac{D_S V_{IN}}{(2-4D_S)} \tag{4.4}$$

$$V_{C2} = V_{C3} = \frac{(1-D_S)V_{IN}}{(2-4D_S)} \tag{4.5}$$

$$B = \frac{V_{DC}}{V_{IN}} = \frac{1}{1-2D_S} \tag{4.6}$$

where B is the boost factor of the proposed converter, which is the same as the one obtained for conventional qZS structure. The symbols V_{IN} and V_{DC} respectively denote the voltage input to converter and peak dc-link voltage.

4.4 Passive Components Selection

The values of the inductors and the capacitors of qZS network are estimated based on the switching frequency and the allowable ripple content for them. The average input current can be estimated using the power balance equation:

$$P_{IN} = P_{OUT} \tag{4.7}$$

Insertion of the shoot through time period causes high frequency ripple in the inductor current. The inductor current increases during the shoot through period and decreases during the active period[21]. The estimated rise in current in this time interval is as follows:

$$\Delta I_{L1} = \int_0^{TD_S} \frac{dI_{L1}}{dt}\, dt = \frac{V_{IN}+V_{C1}+V_{C4}}{2L} TD_S \tag{4.8}$$

From the above equation, the minimum value of inductor can be estimated as:

$$L = \frac{4V_O^2(1-2D_S)TD_S}{(1-D_S)K_L P_{OUT}} \tag{4.9}$$

where, V_O is the output voltage, K_L is the allowable ripple though inductor current. A similar expression can be used to estimate the values of the capacitors.

$$C_1 = C_4 = \frac{TP_{OUT}(1-D_S)^2}{4k_{C1}V_O^2(1-2D_S)} \tag{4.10}$$

$$C_2 = C_3 = \frac{TP_O(1-D_S)D_S}{4k_{C2}V_O^2(1-2D_S)} \tag{4.11}$$

Where, K_{C1} and K_{C2} represent the allowable ripple voltage across the capacitor. From these equations it is evident that the shoot-through duty and the values of the passive components can be estimated[20] based on the required boost factor and the output power.

4.5. Control Scheme

Fig. 4.5 shows the closed loop controller, which regulates dc-link (and hence the output voltage) of the proposed power converter against source and load disturbances. This control scheme consists of a two-loop structure. In this scheme, the outer loop regulates the dc-link voltage. The inner loop, which is appreciably faster than the outer loop, regulates the output current of the PV source. Firstly, the peak dc-link voltage is obtained by summing up the physically measured voltages, which appear across capacitors C_1 and C_2 (Fig. 4.1) and multiplying this value by a factor of 2. Generally, the reference peak dc-link voltage is determined by MPPT controller, though it can also be set manually. The voltage error is processed through a proportional integral (PI) controller, which generates the reference value for the PV output current (which flows through inductor i_{L1}). The actual inductor current (i_{L1}) is then measured and compared with this reference value and the error is then compensated with a proportional controller, which generates the signal to obtain the shoot-through duty cycle. In this work, this controller is implemented digitally using Xilinx -Spartan 6 FPGA board.

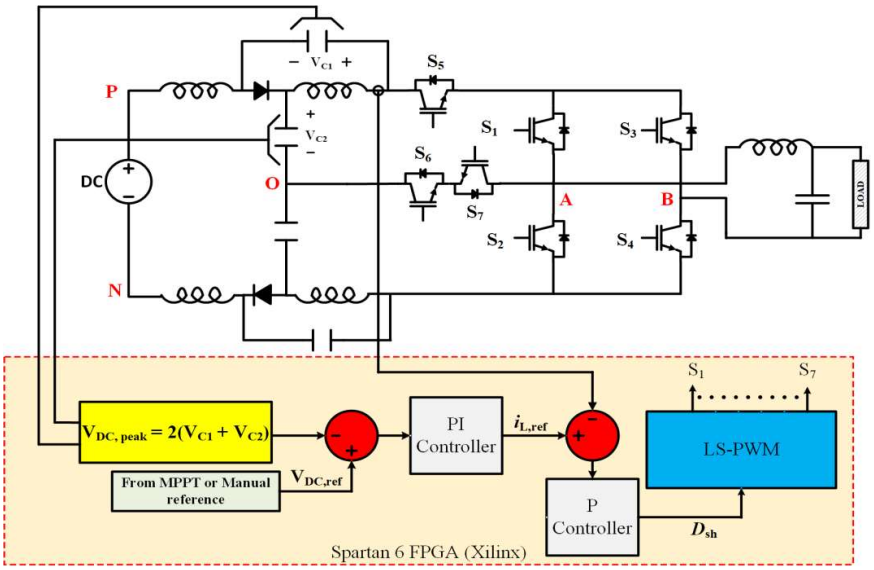


Figure 4.5 Closed loop scheme.

4.6. Leakage Current Analysis

In a solar inverter, the parasitic/stray capacitance is formed between PV terminals and the ground (Fig. 4.6(a)), which provides the path for the common mode current (popularly called as the leakage current)[15]. This leakage current flowing from PV terminals can be measured establishing an RC circuit between point N and load negative. The common mode

voltage is defined as the average voltage between inverter terminals to the negative rail of the source. The CMV of the system can be defined as[18]:

$$V_{CMV} = \frac{V_{AN}+V_{BN}}{2} \tag{4.12}$$

where, V_{AN} and V_{BN} are inverter terminal voltages with respect to point N (Fig. 4.1).

The common-mode equivalent circuit for the proposed inverter is shown in Fig. 4.6. The current flowing through this circuit represents the leakage current, which primarily depends on ground resistance and the value of the parasitic capacitances (Fig. 4.6(b))[16]. The exact equivalent circuit of the whole system where V_{CMV} acts as a source presented in Fig. 4.6(c). Fig. 4.7 shows the variation of the leakage current (RMS value) with respect to the aforementioned circuit parameters for a CMV of 50. From this, it may be noted that the RMS value of the leakage current is directly proportional to the parasitic capacitance but is inversely proportional to ground impedance. Hence an increased ground resistance results in a decrease of the leakage current.

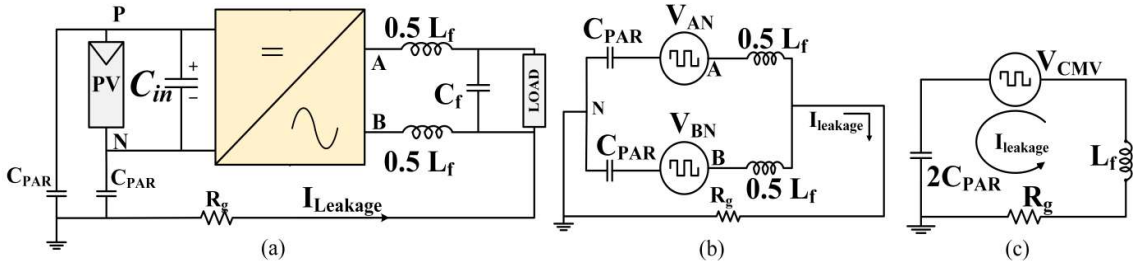


Figure 4.6 Common mode circuit (a) Overall system representing parasitic elements and leakage current. (b) Total circuit for leakage current flow; (c) Equivalent circuit form source to load side.

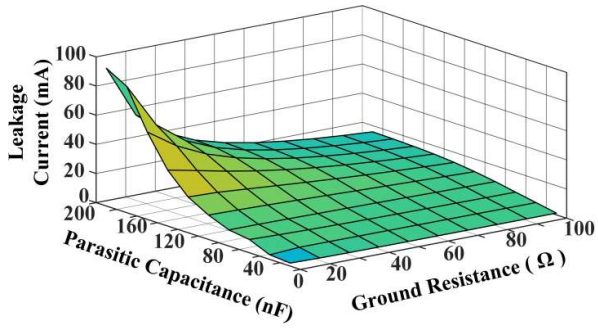


Figure 4.7 Variation of leakage current with respect to ground resistance and parasitic capacitance (CMV=50V)

Also, the leakage current that flows through the ground is directly proportional to the rate change of the voltage across the parasitic capacitance. Therefore, leakage current can be reduced by reducing the variation of voltage across the stray capacitance. The proposed

modulation scheme ensures that the mid-point voltage of the inverter is clamped to the load terminals during the freewheeling period clamping the CMV to zero and reducing the voltage variation across the parasitic capacitor.

The shoot through mode in qZS networks, which is inserted to obtain the required voltage boosting, results in the presence of CMV as well as its high frequency variation across the stray capacitance paving way for the circulation of leakage current. However, the notch filter, which is an LCL filter kept at the output, reduces both the magnitude of CMV and its high-frequency variation[99], [100]. In LCL filter, the inductors and the capacitor are split as shown in Fig. 4.1. The midpoint of the split capacitor is connected to the negative rail of the source (point N, Fig. 4.1). This connection reduces the leakage current by making the high frequency voltage waveform assume a trapezoidal shape (which is impressed across the parasitic capacitance).

4.7. Results and Discussions

The performance of the proposed converter has been verified using simulation studies through MATLAB/Simulink tools and the experimental validation has been carried out with a scaled down laboratory prototype. Both simulation and experimental studies have been performed at a power level of 500W with similar parameters as enumerated in Table 4.3.

4.7.1. Simulation Results

Fig. 4.8 shows the simulated steady-state performance of the proposed converter. The formula for the boost factor obtained with this converter is given by (Table 4.2):

$$B = \frac{1}{1-2D_S} \tag{4.13}$$

The above equation suggests that a boost factor of 2.2 is obtained with a shoot through duty $\boldsymbol{D_S} = 0.27$.

As shown in Fig. 4.8(a), an input voltage of 100V and a shoot through duty cycle of $\boldsymbol{D_S} = 0.27$ result in a boosted dc-link of 220V (with a 10V ripple). This complies with the above expression, as a boost factor of 2.2 is obtained. The modified modulation scheme and the shoot though insertion technique avoid the dc-link value to fall to zero every time. The steady-state waveforms of the output voltage of the 5-level inverter, the load voltage and current waveforms (with a multiplication factor of 10) are shown in Fig. 4.8(b) and 8(c) respectively. Fig. 4.8(d) presents the current through inductor L_1, which increases during the

shoot-through mode of qZS network. Owing to the symmetry of qZS network and identical values of inductances, all other inductor currents show identical waveforms.

Table 4.2. Simulation and Experimental Parameters

Parameters		Values
Output Power		500W
Input Voltage		100V
Output Voltage (RMS)		110V
Inductors	L_1-L_4	1mH
	L_f	4mH
Capacitors	C_1-C_4	1000µF
	C_f	4µF
Switches (S_1-S_7)		IRFP460
Diodes (D_1, D_2)		MURS1560

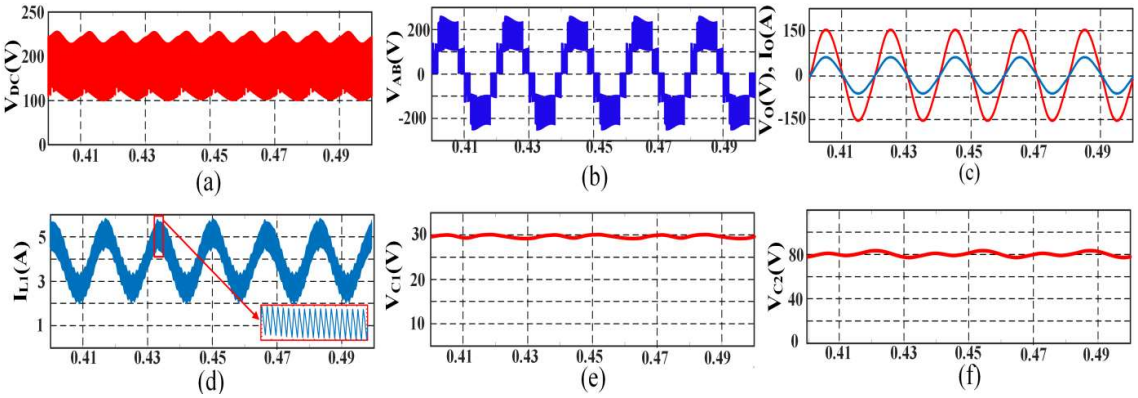


Figure 4.8 Simulation results (a) Boosted DC link voltage; (b) Inverter terminal level voltage; (c) Output Voltage and Current; (d) Inductor current for L_1; (e) V_{C1}; (f) V_{C2}

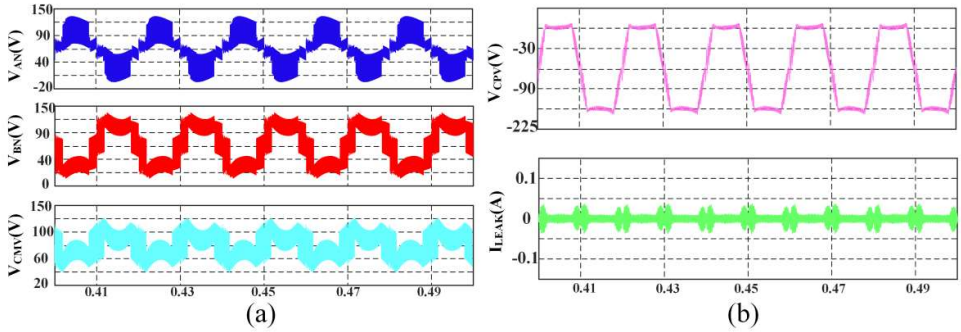


Figure 4.9 Simulation results (a) Common Mode Characteristics V_{AN}, V_{BN} and V_{CMV} respectively; (b) Voltage across parasitic capacitor and Leakage current.

Due to the symmetry of qZS network, C_1=$C_4$and C_2=C_3. Fig. 4.8(e) and 8(f) present the voltages across capacitors C_1 and C_2. The average values of these capacitor voltages comply with equations (4) and (5).

The common mode characteristics of the proposed power converter are presented in Fig. 4.9. The CMV (V_{CMV}) is calculated using V_{AN} and V_{BN} (equation 4.12). The steady-state waveforms of these three voltages (V_{AN}, V_{BN} and V_{CMV}) are presented in Fig. 4.9(a). The shoot through mode inserted in every switching cycle manifests as high-frequency content in these waveforms.

The top waveform of Fig. 4.9(b) shows the voltage across the stray capacitance, wherein the high-frequency content is absent. This shows the effectiveness of the proposed modulation scheme and the filter arrangement. The second waveform in Fig. 4.9(b) is the leakage current that flows from the source to the load. Due to the trapezoidal nature of the voltage across stray capacitor, the peak value of leakage current is restricted to 20mA which is well below the German standard VDE 0126-1-1 (which specifies that the leakage current be within ≤ 300 mA).

As explained in the earlier section, the modulation scheme, besides suppressing the leakage current in the proposed converter, provides it the capability to support reactive power. The proposed converter achieves this feature by providing a path for the free-wheeling current for lagging or leading loads. Fig. 4.10 demonstrates the reactive power capability of the converter, wherein the load is changed from UPF to 0.9 lagging power factor. This capability is achieved by turning on switches S_1 and S_3 during the zero-period as shown in Fig. 4.4(e). During this period the CMV is clamped to a value of zero, which is achieved by turning on the devices S_6, S_7 (connecting the point "A" to the midpoint of NPC structure, i.e., "O") and turning off device S_5 (which isolates the source-side and the load-side) as shown in Fig. 4.4(e).

The dynamic performance of the proposed converter under load disturbance is demonstrated in Fig. 4.11. The control scheme, shown in Fig. 4.7, aims to maintain a constant dc-link voltage by regulating the shoot-through duty cycle. In the simulation result shown in Fig. 4.11(a), the load on the converter is removed at *t=2sec* and is again applied at *t=4sec.* Zoomed views of all quantities, namely output voltage, output current, peak dc-link voltage and the shoot-through duty cycle are shown in Fig. 4.11(b)-4.11(d). It can be observed that the shoot-through duty cycle is automatically adjusted by the controller to maintain the peak dc-link value at its reference value.

Fig. 4.12 shows the dynamic response of the proposed converter against source disturbance. In this simulation study, the input voltage is ramped up from 80V to 100V, starting at *t=1sec*. The input voltage is then ramped down to 80V at *t = 3.5 sec.* Both of these changes are affected gradually (i.e., as a ramp) to simulate the real-world condition (Top trace, Fig. 4.12). The middle and bottom traces of Fig. 4.12 present the responses of the peak dc-link voltage and the shoot-through duty respectively. It can be observed that the peak dc-link voltage changes due to change in input voltage. The controller then springs into action and adjusts the shoot-through duty cycle to regulate the peak dc-link voltage at its reference value.

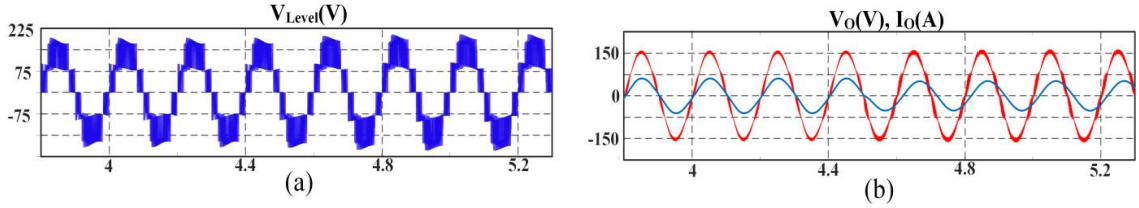


Figure 4.10 Reactive power capability of the converter (a) Inverter terminal voltage during load change from UPF to 0.9 Lag PF; (b) Output Voltage and Current

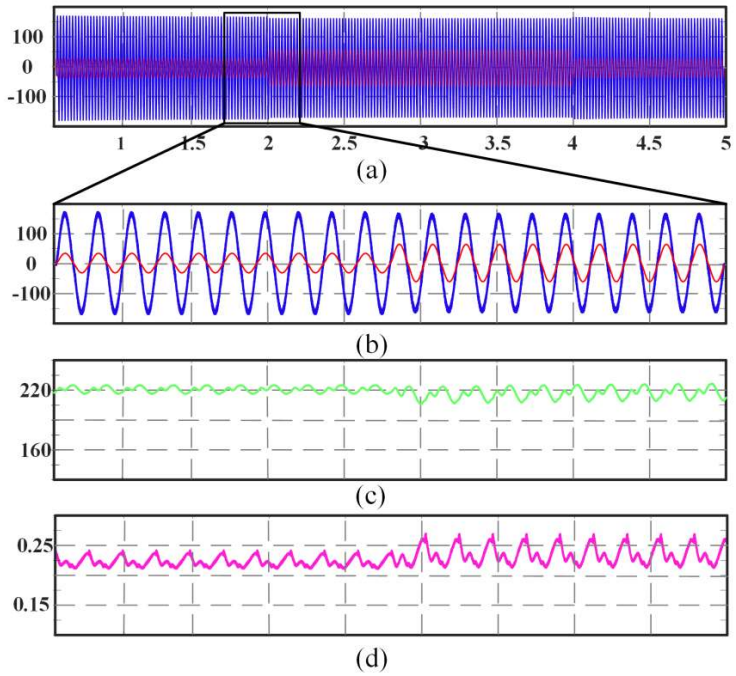


Figure 4.11 Simulation results for closed loop control during change in load : (a) Complete simulation results with output voltage and current; (b) Zommed version of load voltage and cuurent during release of load at *t=2 secs*; (c) Peak DC link voltage; (d) Shoot-through duty cycle.

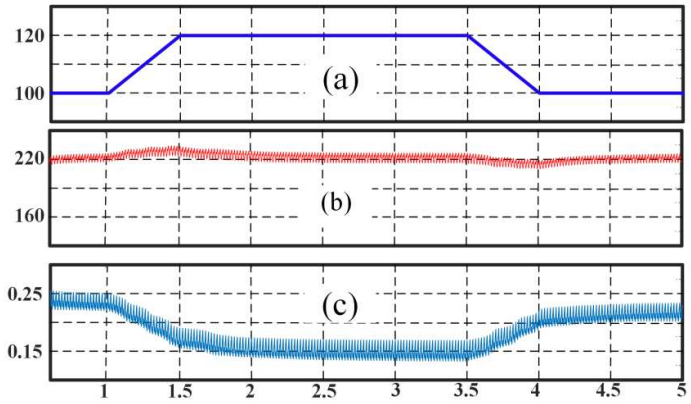


Figure 4.12 Simulation results for closed loop control during change in input voltage: (a) Ramp change in input voltage from 100V to 120V at t=1 sec and 120V to 100V at t=3.5 secs; (b) Regulated DC link voltage; (c) Change in shoot-through duty cycle.

4.7.2. Experimental Results

In order to validate the simulation results presented in the above section, an experimental prototype is developed, which is rated for a power rating of 500 W (Fig. 4.13). The parasitic elements that trigger the leakage current is emulated by connecting a resistance (R_g) and a capacitance (C_{PAR}) in series, which is connected between the negative terminal of the source output and load as shown in Fig. 4.1. The inductors and capacitors of the qZS, which are calculated using (4.9)-(4.11), are used for the realization of the physical prototype (the same component values are used in simulation studies too). IRFP460 power-MOSFETs and MURS1560 diodes (for qZS) were employed to construct the power converter. The PWM scheme and the controller were implemented with Spartan 6 series FPGA.

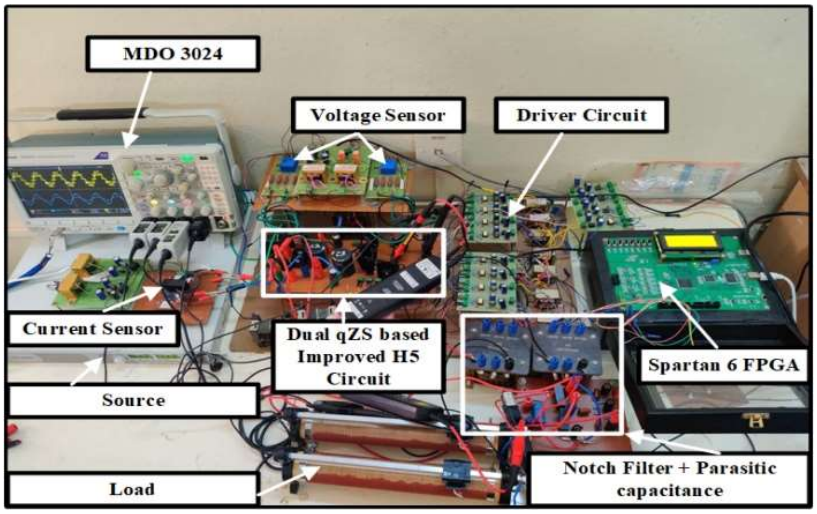


Figure 4.13 Hardware setup of proposed inverter.

The steady-state performance of the converter is presented in Fig. 4.14. The dc-link voltage and the terminal voltage of the 5-level inverter are presented in Fig. 4.14(a). Fig. 4.14(b) presents the inverter terminal voltage, output voltage (after filtering) and load current. The current flowing through the inductor L_1 and the voltages across the two capacitors C_1 and C_2 are presented Fig. 4.14 (c). The FFT of the inverter terminal voltage, output voltage and output current are presented in Fig. 4.14(d)-(f). The THD of output voltage and current have a value of 2.98% and 2.05% respectively which are well within IEEE standard.

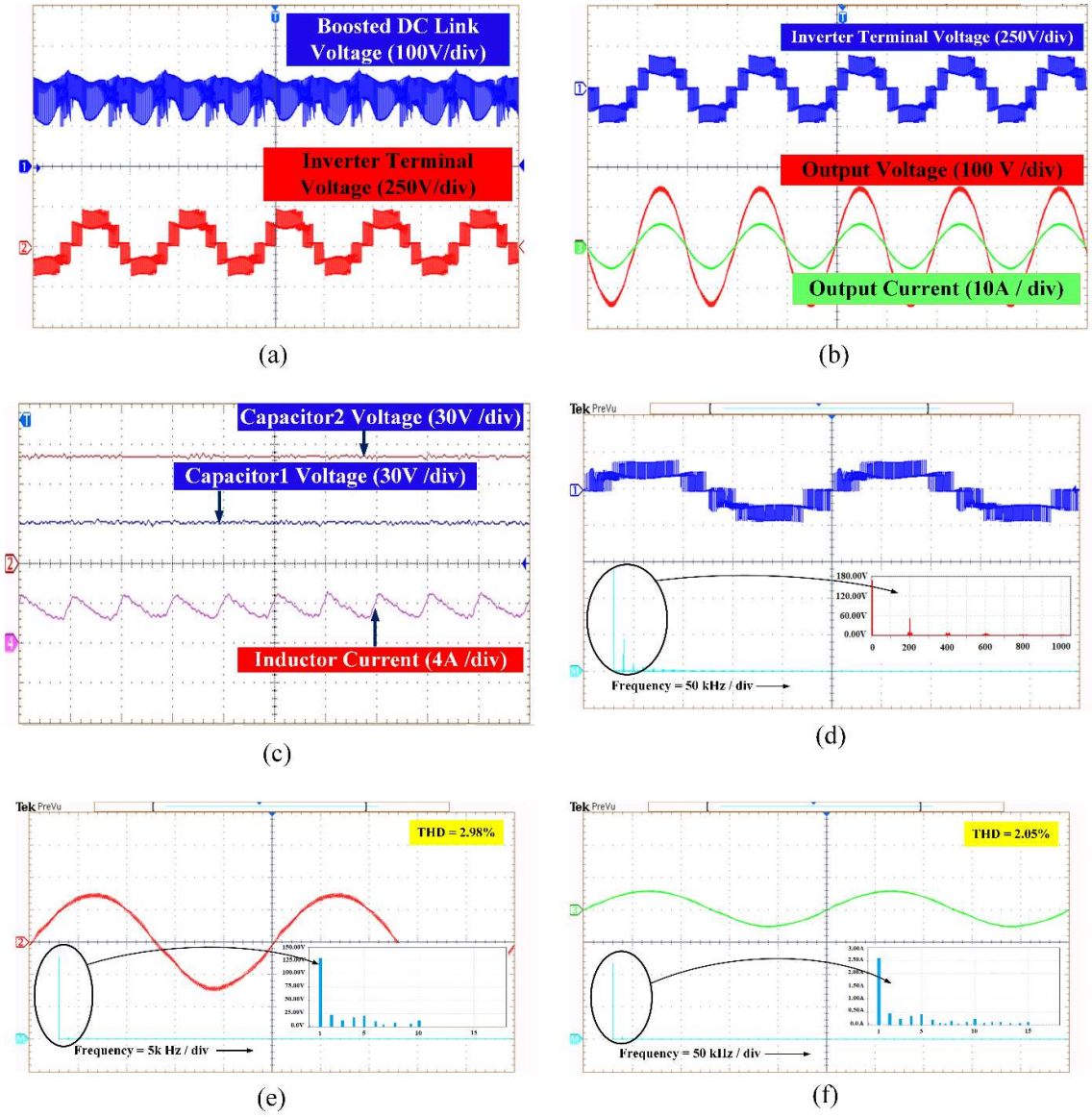


Figure 4.14 Steady State performance of the proposed converter: (a) Boosted dc link voltage, Inverter terminal voltage; (b) Inverter terminal voltage, output voltage and current; (c) i_{L1}, v_{C1} and v_{C2} (d) FFT of inverter terminal voltage; (e) FFT of inverter output voltage; (f) FFT of inverter output current.

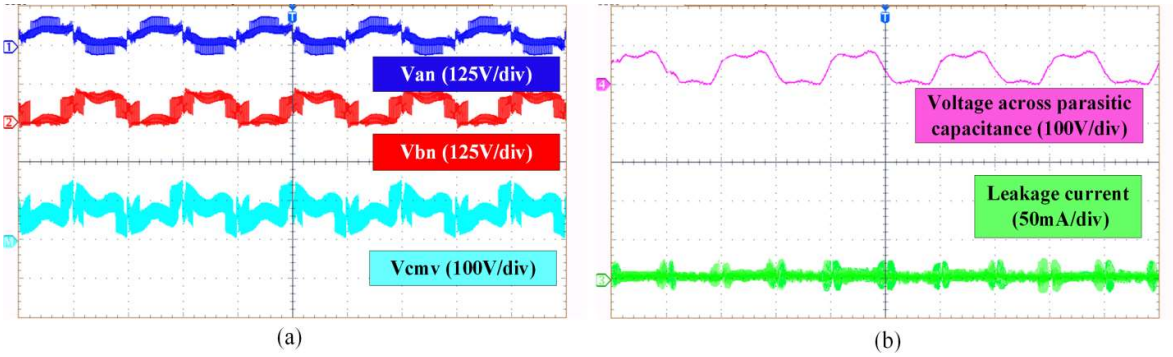


Figure 4.15 Common mode characteristics of inverter: (a) V_{AN}, V_{BN} and V_{CMV}; (b) Voltage across parasitic capacitance and leakage current.

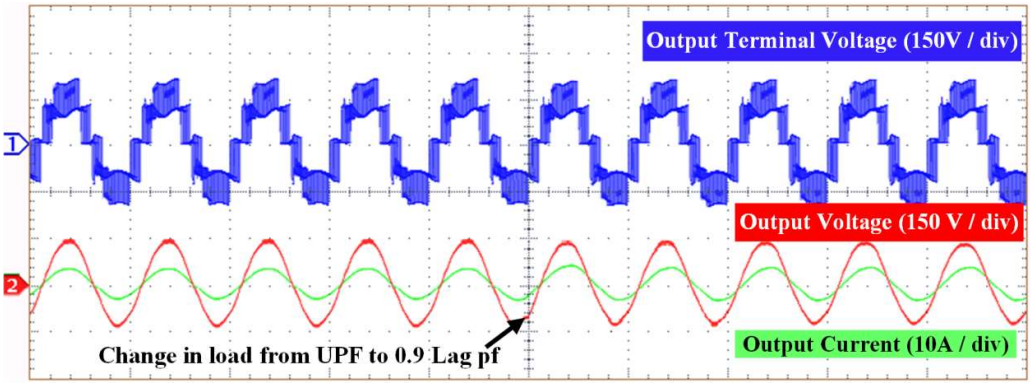


Figure 4.16 Experimental waveform demonstrating the reactive power capability of converter.

Fig. 4.15 describes the common mode characteristics of the proposed inverter. The inverter terminal voltages (V_{AN}, V_{BN}) and the CMV (V_{CMV}) are shown in Fig. 4.15(a). Fig. 4.15(b) presents the voltage across the parasitic capacitance and the leakage current. It is evident form Fig. 4.15(b) that the proposed PWM scheme and the notch filter succeed in suppressing leakage current. It may be noted that the resulting leakage current is 20 mA (RMS), which is well within the value stipulated by German VDE 0126-1-1 standard ($\leq$ 300 mA).

The experimental result presented in Fig. 4.16 validates the reactive power capability of the converter. It may be noted that, despite the change in the nature of the load (UPF to 0.9 lag), the terminal voltage of the inverter remains undistorted. As explained earlier, this reactive power handling capability is attributed to the availability of the free-wheeling paths for the inverter current during the time-gap between the positive zero-crossing instants of output voltage and output current.

Fig. 4.17 shows the dynamic performance of the proposed converter against the source disturbance. It may be observed that despite a gradual change in input voltage (90V to 105V and then 105V to 80V), the dc-link voltage is regulated at the reference value by the controller

in both the conditions. The dynamic response of the system against the load disturbance is presented in Fig. 4.18. It is evident that the control system (Fig. 4.7) can also tackle load disturbance. Fig. 4.18 reveals that the dc-link voltage of the converter is regulated by the controller effectively as the load is changed from 5A to 4A and vice-versa. Fig 4.19 shows the system in grid-connected mode while 4.19(a) shows the input parameters to inverter and 4.19(b) shows DC-link, grid voltage and grid current.

4.7.3. Efficiency and Loss Analysis

The section presents a comparative study of the efficiencies displayed by various single-phase five-level inverter topologies compared in literature. Efficiencies of these inverters were estimated using the thermal models of the switching devices available with PSIM software[98]. While performing these efficiency calculations, identical parametric values were used across all of the converters ($V_{IN} = 100V$, $D_S = 0.27$, $m = 0.7$).

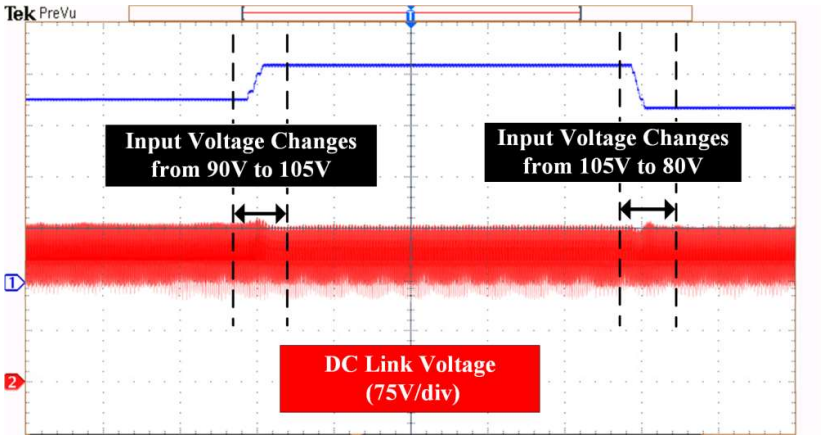


Figure 4.17 Closed loop results for change in input voltage.

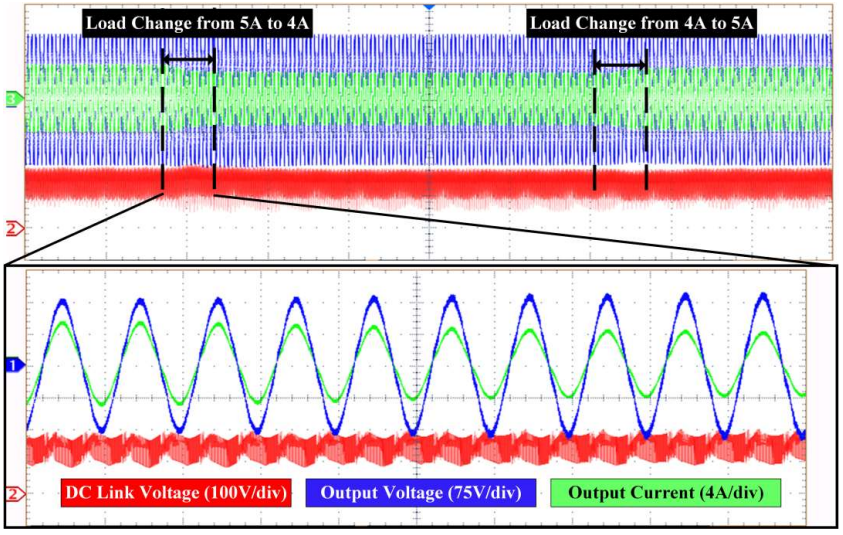
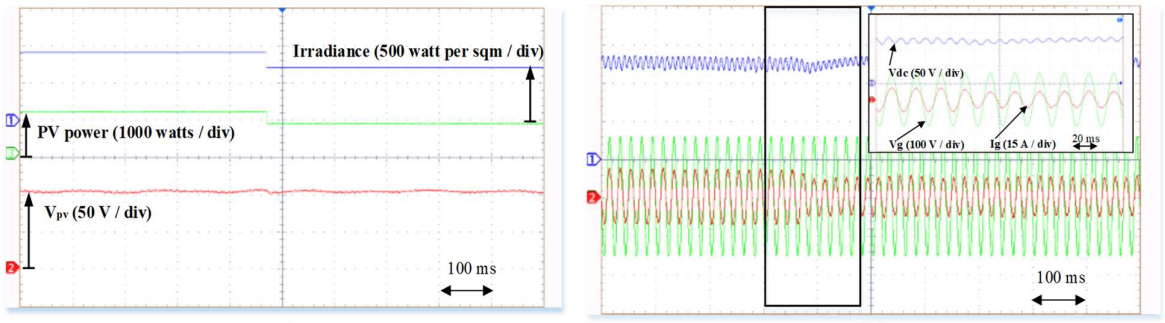
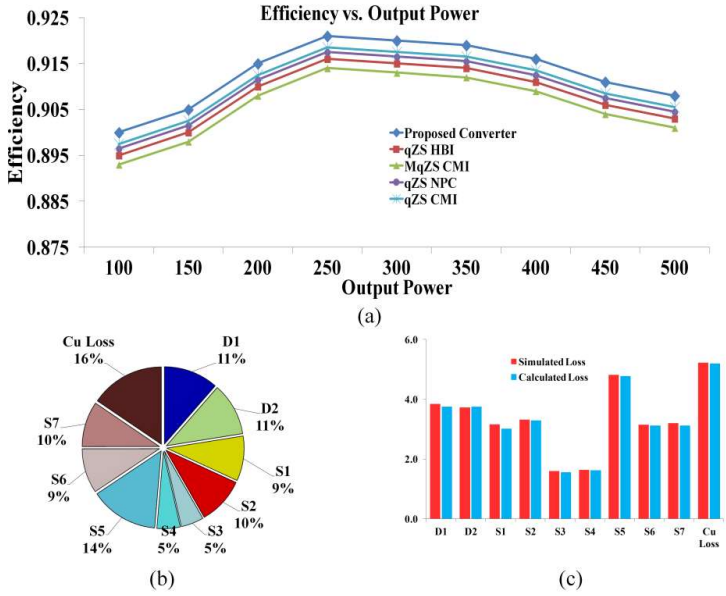


Figure 4.18 Closed loop results for change in load.



(a) (b)

Figure 4.19 Grid-connected mode (a) Variation in input, (b) Variation in output due to change in irradiance.



(a) (b) (c)

Figure 4.20 Efficiency comparison (a) Efficiency of various qZSI, (b) Loss distribution among elements, (c) comparison between calculated and simulated loss.

Fig. 4.20 (a) presents the efficiencies of existing qZS based five-level topologies. It is evident that the proposed converter exhibits higher efficiency compared to other converters (described in Table-2) throughout the operating range of the converter. It may also be noted from Fig. 4.20 (a) that the proposed converter achieves a maximum efficiency of 92% at around 250W. Higher efficiency of the proposed power converter is attributed to the employment of fewer switching devices and a suitable modulating technique. The loss distributions in various active and passive devices are shown in Fig. 4.20(b). It can be observed that copper losses take top most position followed by the losses in switch S_5 and diode (D_1 and D_2). Among the switches, S_5 incurs the highest amount of loss from remaining in conduction state for most of time in the whole cycle. However, based on the formulas provided, the losses are calculated and compared with the simulated losses as seen in Fig.

4.20(c). It can be verified that simulated loss (blue bar) and calculated losses (red bar) have almost same values, which attests to the effectiveness of efficiency curves. Efficiency of the converter can still be improved by replacing the conventional silicon devices with SiC or GAn counterparts.

4.8. Comparison with Existing Topologies

A detailed comparison of the proposed converter with existing literature is provided in Table 4.2. Amongst the existing PV based inverter in [79], [83], [87], [89], [101]–[106] the proposed inverter has lowest switches count to provide five-level output except [102] which has the same count but suffers from single stage boosting and shoot-through problem. DMSC5L-TL [103] and 5L-CGBT-ANPC[104] have the ability to supress leakage current suppression due to the common ground feature. DMSC5L-TL[103] requires a higher active device count to produce the same level and moreover, it also requires a boosting stage to incorporate variable boosting feature. The 5L-CGBT-ANPC[104]has similar device count and variable single stage boosting like the proposed inverter but higher amount of semiconductor devices needs to be conducting to produce voltage while operating. Moreover, if V_{DC} is considered as input to the inverter [101]–[106] requires higher capacitor rating than the proposed one.

The Total Blocking Voltage (TBV), which is the sum of voltages blocked by individual devices of a given power converter[19], is also lowest for the proposed converter compared to all other topologies except qZS-CMI[83] and ref[105]. However, the proposed topology requires only one input dc power source, compared to two in the case of the qZS-CMI topology; this advantage outweighs the disadvantage associated with the TBV. The higher requirement of diode and shoot though problem in ref[105] makes it less reliable than the proposed one. The presence of clamping diodes in qZS-NPC[88] makes it prone to failure and losses. Hence, it can be inferred that the proposed topology could be more efficient than the other topologies of this genre. However, unlike the proposed power converter, MqZS[89] doesn't addresses the issues of reactive power handling capability and leakage current. Furthermore, owing to the absence of an inductor at the input, the input current is discontinuous in MqZS. Hence, it is not suitable for PV applications. To summarize, the proposed converter has features like lowest switch count, single stage boosting, no shoot though risk, low total blocking voltage, reactive power capability, low capacitor rating and reduced leakage current; these traits makes it ideal for PV applications.

Table 4.3 Complete Comparisons with Existing Topologies

Features	Shoot though risk	Voltage across each capacitor	Maximum no. of switch conducting	leakage Current	Reactive Power Capability	Sources required	Boosting	TBV	D	C	L	No. of Switches (BDC*)	Levels
[87]	No	$V_{C1}=\frac{D_S V_{DC}}{2}, V_{C2}=\frac{(1-D_S)V_{DC}}{2}$	4	Not Addressed	No	1	Yes, Variable	$6V_{DC}$	6	4	4	8(0)	5
[83]	No	$V_{C1}= D_S V_{DC}, V_{C2}=(1-D_S)V_{DC}$	4	Not Addressed	No	2	Yes, Variable	$4V_{DC}$	2	4	4	8(0)	5
[89]	No	$V_{C3}=\frac{D_S V_{DC}}{2}$ $V_{C2}=V_{C1}=\frac{(1-D_S)V_{DC}}{2}$	4	Not Addressed	No	1	Yes, Variable	$6V_{DC}$	3	4	2	8(0)	5
[79]	No	$V_{C1}= D_S V_{DC}$ $V_{C2}=V_{C3}=$ $(1-D_S)V_{DC}$	3	Not Addressed	No	2	Yes, Variable	$6V_{DC}$	2	4	4	8(0)	5
[101]	Yes	$V_{C1}=V_{DC}$ $V_{C2}=2V_{DC}$	3	Zero	Yes	1	Yes, Fixed	$10V_{DC}$	1	2	0	6(1)	3
[102]	Yes	$V_{C1}=V_{DC}$ $V_{C2}=2V_{DC}$	3	Zero	Yes	1	Yes, Fixed	$10V_{DC}$	1	2	0	6(1)	5
[103]	Yes	$V_{C1}= V_{C2}=V_{DC}$ $V_{C1}=2V_{DC}$	4	Zero	Yes	1	Yes, Fixed	$10V_{DC}$	1	3	0	7(2)	5
[104]	No	$V_{C1}=2V_{DC}$ $V_{C2}=V_{DC}$	4	Zero	Yes	1	Yes, Variable	$12V_{DC}$	0	2	1	7(0)	5
[105]	No	$V_{C1}=V_{DC}$	3	Zero	Yes	1	Yes, Variable	$5V_{DC}$	5	2	4	5(0)	3
[106]	Yes	$V_{C1}=V_{DC}$	3	Zero	Yes	1	Yes, Variable	$6V_{DC}$	2	1	1	5(1)	3
[110]	No	$V_{C1}=V_{DC}$	2	Zero	Yes	1	Yes, Variable	$4V_{DC}$	2	1	3	4(0)	3
qZS-IH5	No	$V_{C1}=\frac{D_S V_{DC}}{2} V_{C2}=\frac{(1-D_S)V_{DC}}{2}$	3	Addressed, 20 mA	Yes	1	Yes, Variable	$5.5V_{DC}$	2	4	4	6(1)	5

4.8. Summary

This chapter proposes a new power circuit configuration for single-phase, single-stage PV systems. The proposed power converter is designed by fusing a qZS network with a 5-level voltage source inverter. The 5-level inverter is synthesized by augmenting an *H5-inverrter* with a bi-directional clamping branch. This bi-directional clamping branch, besides obtaining the clamping of the mid-point voltage, produces an additional level in the output voltage waveform.

The qZS network is formed by connecting two symmetrical quasi-Z-sources in a back-to-back manner. Such a network results in a neutral point clamped structure with single-stage boosting. The modulation technique employed for this power converter aims to achieve: (i) five voltage levels (ii) reactive power handling capability, and (iii) confining of leakage current to well within the standards of VDE 0126-1-1.

The effectiveness of the adopted modulation strategy and the control scheme are assessed with simulation studies. These simulation studies reveal that both steady-state and dynamic performances of the proposed converter are satisfactory. Simulations studies clearly show that the controller regulates the peak value of the dc-link voltage against the source and load disturbances by adjusting shoot-through duty cycle.

These simulations are then experimentally validated on a 500 W laboratory prototype using Spartan 6 FPGA control platform. Experimental results, which agree with simulation results validate the working principle of the proposed converter and the adopted modulation scheme.

A comparative study of the proposed power converter with other comparable topologies reported in literature so far reveals that the proposed converter yields better performance in aspects such as switch count, reliability, efficiency, leakage current and reactive power handling capability. Based on these advantages, it appears that this power converter is a viable proposition for PV applications and merits further exploration.

Chapter 5

DUAL QUASI Z-SOURCE BASED T-TYPE INVERTER WITH IMPROVED HERIC STRUCTURE

Chapter 5

Dual Quasi Z-Source Based T-Type Inverter With Improved HERIC Structure

5.1 Introduction

In chapter 4, a dual quasi Z-source based H5 inverter configuration was proposed with the merits of single-stage boosting and reduce the leakage of the system. In this chapter, a new configuration of dual quasi Z-source based T-type five-level inverter with improved HERIC structure is proposed to address the problems associated with the two-stage systems, which are bulky and expensive, and have leakage current issues for grid-connected applications.

Therefore, this chapter presents the operating principle of the proposed topology based on output voltage level generation. Modified PWM and a passive filter were introduced to eliminate high frequency transitions across the parasitic capacitance to effectively suppress leakage current. It has the merits of single-stage conversion and reactive power support, which is the essential requirement for present PV inverters. Complete design and analysis of CMV have been described to minimize the leakage current. MATLAB simulation work is carried out for the proposed configuration to address the dynamic performance of the system under stand-alone and grid connected modes of operation. In addition, a laboratory prototype was used to validate the results. Finally, a comprehensive comparison is made with existing quasi Z-source based inverters to highlight the advantages of the proposed configuration.

5.2 System Description

5.2.1 Proposed Topology

Fig. 5.1 depicts the proposed single-phase dual-qZS-T-type inverter with an improved HERIC structure. This converter outputs a five-level output voltage waveform and is applicable for photovoltaic applications. The proposed power converter appears as a continuous structure consisting of a dual qZS network and a T-type five-level inverter with an improved HERIC arm as shown in Fig. 5.1. The qZS boosting network consists of two conventional qZS networks, which are connected to the positive and the negative terminals of the PV source as shown in Fig. 5.1. With the orientations of qZS networks as shown in Fig. 5.1, it is possible to create a DC neutral point (the point ‘O’ in Fig. 5.1).

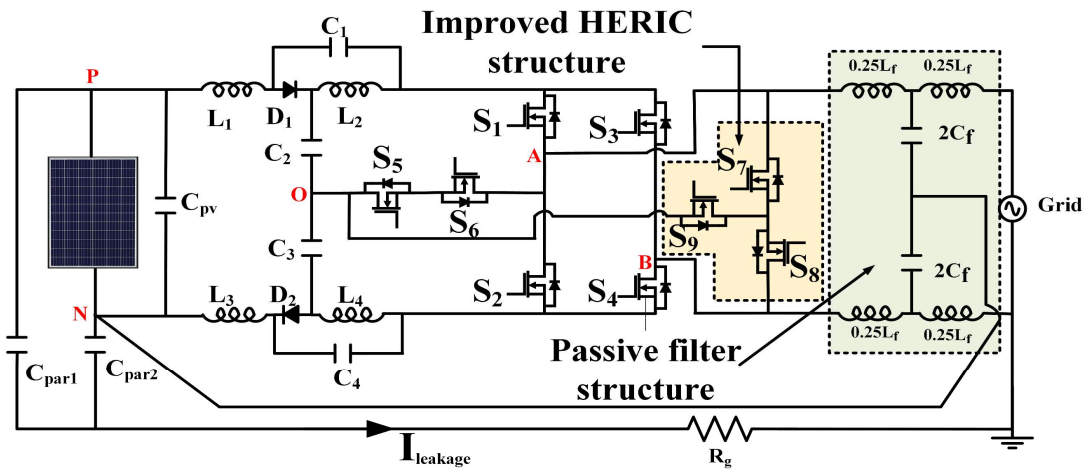


Figure 5.1 Dual qZS based improved HERIC structure.

Owing to the structural symmetry of the proposed topology, the neutral point 'O' is balanced naturally. It is evident the proposed topology is an amalgamation of a T-type arm, the HERIC structure and a switch that helps in clamping the mid-point 'O'. Bidirectional switches (S_5, S_6), which constitute the T-type arm facilitate the generation of the voltage level $\pm V_{DC}/2$. Further, bidirectional switches (S_7, S_8) form the HERIC structure, which offers a freewheeling path for the grid current, while isolating the AC side and the DC side. In the improved HERIC structure, switch S_9 is utilized to clamp the mid-point 'O' to the mid-point of the bidirectional switches (S_7, S_8) during the freewheeling period, which forces CMV to attain a value of zero. This topology uses a modified modulation scheme, which is employed to generate gating signals for the switches to suppress of CMV while synthesizing the five-level voltage waveform across the load. The working modes and the control structure are explained in the following sections.

5.2.2 Operating Modes

The operating modes of the inverter are shown in Fig. 5.2. These operating modes are broadly classified into 2 categories, namely, non-shoot-though modes and shoot-through modes. The non-shoot-through mode consists of 5 states of which 4 states correspond to the active mode and the remaining one state corresponds to the zero mode. The shoot-though mode consists of 2 states, namely, Upper Shoot-Through mode (UST) and Lower-Shoot-Through mode (LST). Table 5.1 enumerates the voltage levels and the switching scheme to realize these levels along with the auxiliary information.

As stated earlier, the implementation of shoot-though modes (UST and the LST) are pivotal to obtain the required voltage boosting. In this context, the UST mode is employed to

realize the objective of voltage boosting during the positive half cycle using top-qZS. Similarly, the LST mode is applied during the negative half-cycle of the output voltage to short-circuit the bottom qZS.

The non-shoot through zero-vector mode, which is shown in Fig. 5.2(g), clamps the mid-point 'O' to the junction of the bidirectional switches, while forcing CMV to zero. Also, this mode offers an additional advantage of improving the reliability of the converter, as it facilitates the freewheeling of the grid current without utilising the level-generating switching devices.

Table 5.1 Switching Sequence

Voltage level obtained	Turned-on Switches	Nature of the switching state	Reference to figure
$+V_{DC}/2$	S_4, S_5 and S_6	Active, Non-shoot-through	2(a)
$+V_{DC}$	S_1 and S_4	Active, Non-shoot-through	2(b)
$-V_{DC}/2$	S_3, S_5 and S_6	Active, Non-shoot-through	2(c)
$-V_{DC}$	S_2 and S_3	Active, Non-shoot-through	2(d)
0	S_1, S_5 and S_6	Upper Shoot-through	2(e)
0	S_2, S_5 and S_6	Lower shoot-through	2(f)
0	S_7, S_8 and S_9	Zero-state	2(g)

Modulation index (m) is defined as the ratio of the amplitudes of carrier wave and the modulating (reference) wave; it determines the amplitude of the fundamental component of the output voltage. The conditions to be fulfilled for achieving the shoot though-duty (D_S) is related to the peak modulation index (m) as follows:

$$D_S + m \leq 1 \tag{5.1}$$

Applying volt-sec balance to the inductors over one switching cycle, the boost factor and various capacitor voltage values are obtained as follows[83], [87]:

$$V_{C1} = V_{C4} = \frac{D_S V_{IN}}{(2-4D_S)} \tag{5.2}$$

$$V_{C2} = V_{C3} = \frac{(1-D_S)V_{IN}}{(2-4D_S)} \tag{5.3}$$

$$B = \frac{V_{DC}}{V_{IN}} = \frac{1}{1-2D_S} \tag{5.4}$$

$$V_{out} = mBV_{in} \tag{5.5}$$

In equations (5.4) and (5.5), symbol *'B'* represents the boost factor of the proposed converter, which is the same as the one obtained for conventional qZS converter. The symbols V_{IN} and V_{DC} respectively denote the input voltage to the converter (PV source in the present case) and the peak value of boosted dc-link voltage. Similarly, the symbols $V_{C1}, V_{C2}, V_{C3}, V_{C4}$ respectively represent the average capacitor voltages of qZS capacitors. The total peak DC-

link voltage output by the dual-qZS is obtained by adding up the average voltages across all the four capacitors ($V_{C1}, V_{C2}, V_{C3}, V_{C4}$):

$$\hat{V}_{DC} = V_{C1} + V_{C2} + V_{C3} + V_{C4} \tag{5.6}$$

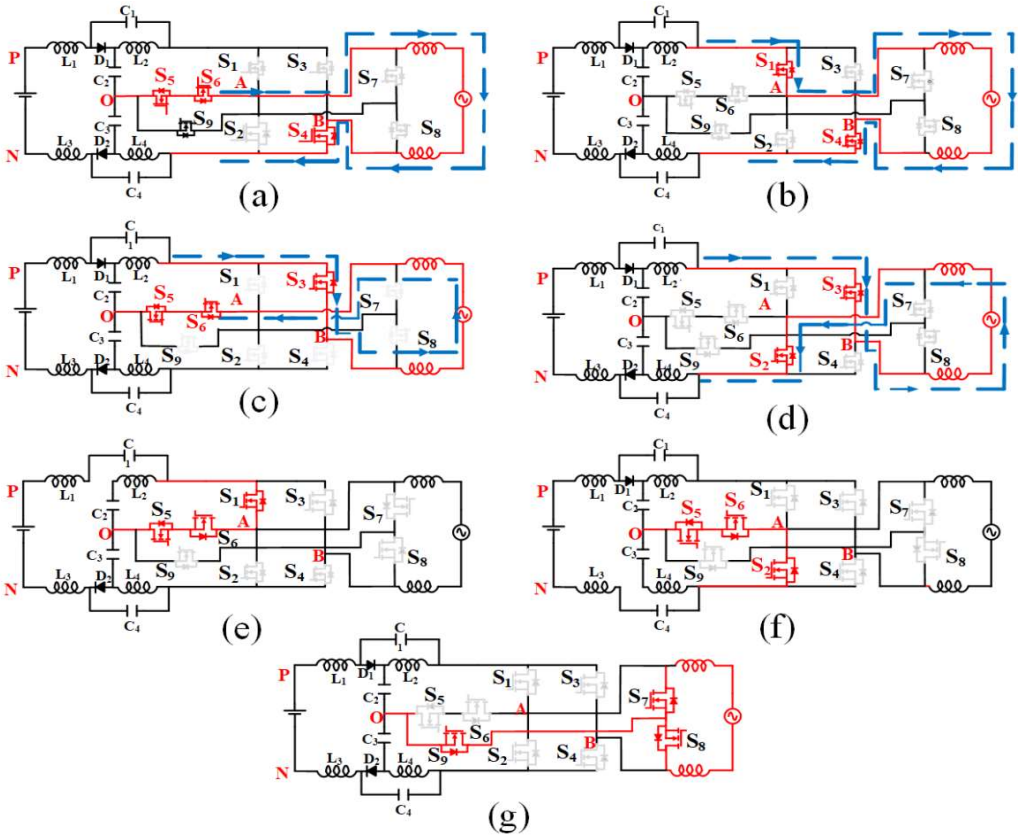
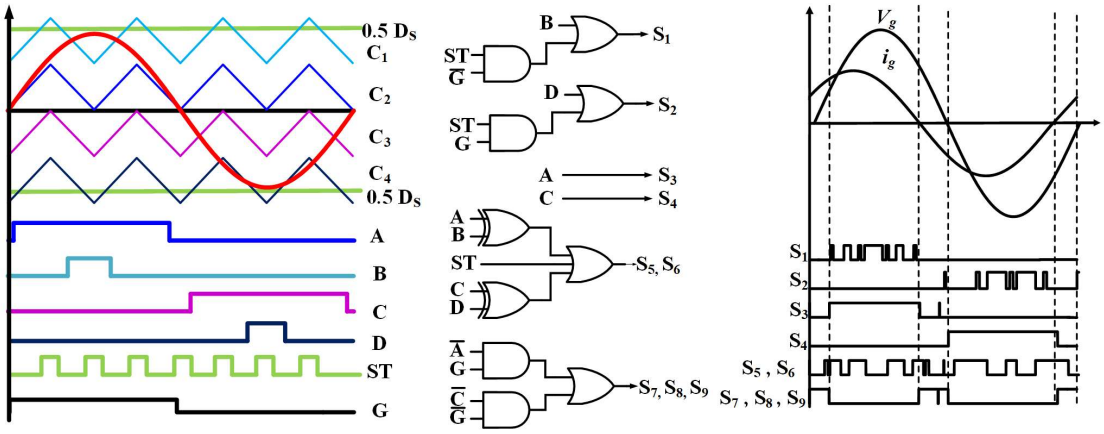


Figure 5.2 Operating modes of the proposed inverter that include active states ((a)-(d)), shoot though states ((e)-(f)) and zero state (g).

5.2.3 Modified Modulation Scheme

The Level-Shifted PWM (LSPWM) scheme is employed in this work to generate gating signals to the devices, which constitute the proposed power converter. Four level-shifted carrier waveforms (Fig. 5.3(a)) are compared with a sinusoidal modulating signal to produce signals *A-D*. Two DC references are compared with the top- as well as the bottom triangular carrier waves and are combined through an 'OR' gate to produce the shoot-through pulse trains *ST*. Also, signal '*G*' is generated by comparing the modulating signal with a value of zero. By processing these signals through combinational logic scheme, shown in Fig. 5.3(b), the gating signals are generated for all of switching devices. Fig. 5.3(c) shows the gating signals generated, when the load is reactive in nature. It may be noted from Fig. 5.3(c) that, during the time-period between the negative zero-crossing instants of the output voltage

and current, the modulation scheme provides the free-wheeling path by activating switches S_7, S_8 and S_9.



(a) (b) (c)

Figure 5.3 Modified PWM Scheme implementation; (a) LSPWM scheme and corresponding signals. (b) Logic for generation of switching signals for S_1-S_8. (c) Switching signals during reactive loads.

5.3 Passive Component Selections

5.3.1 qZS Passive Component Calculations

From Fig. 5.1, it may be noted that the proposed converter requires 8 passive components, *viz.* four inductors and four capacitors. Due to the symmetrical nature of the top and bottom qZS networks, it is obvious that the parametric values of all inductors (L_1 - L_4) and capacitors (C_1, C_4 and C_2, C_3) should be the same. The values of these components can be found using two parameters: operating frequency and ripple content. Assuming a lossless system, the input power (P_{IN}) and output power (P_{OUT}) are equal, i.e.:

$$P_{IN} = P_{OUT} \tag{5.7}$$

and,

$$I_{IN} = \frac{P_{OUT}}{V_{IN}} \tag{5.8}$$

In (5.8), I_{IN} denotes the average input current, which is the same as the average current flowing through the inductor L_1 (I_{IN}=I_{L1}). The ripple in the inductor current is primarily due to the employment of shoot-through (ST) and non-shoot-through (NST) modes of operation in a switching cycle. The ripple in the inductor current can be found by applying KVL during the ST mode as follows[20], [21]:

$$\Delta I_{L1} = \int_0^{TD_S} \frac{dI_{L1}}{dt} dt = \frac{V_{IN}+V_{C1}+V_{C4}}{2L} TD_S \tag{5.9}$$

Where from the minimum value of the inductor current to obtain the continuous conduction mode (CCM) [31] is given by:

$$L = \frac{4V_O^2(1-2D_S)TD_S}{(1-D_S)K_L P_{OUT}} \tag{5.10}$$

where, the term K_L represents the allowable ripple content through the inductor and V_O is the output voltage.

Similarly, the values of outer capacitors (C_1, C_4) and inner capacitors (C_2, C_3) are calculated as:

$$C_1 = C_4 = \frac{TP_{OUT}(1-D_S)^2}{4k_{C1}V_O^2(1-2D_S)} \tag{5.11}$$

$$C_2 = C_3 = \frac{TP_O(1-D_S)D_S}{4k_{C2}V_O^2(1-2D_S)} \tag{5.12}$$

Where K_{C1} and K_{C2}respectively denote the allowable ripple content in these capacitors. It may be noted from the above equations that the values of passive components of qZS network are determined by the desired ripple content, switching frequency, ST duty cycle, output voltage and the output power.

5.3.2 Input Filter Calculations

It is a well-known fact that 1-Ph inverters cause a ripple in the source current. This ripple corresponds to a frequency that is twice that of output frequency. In conventional 1-Ph inverters, a capacitor, which is provided at the dc input terminals, facilitates the circulation of this ripple current by providing a path of low impedance to it. Generally, a PV source is also equipped with such a capacitor [91] to circulate the ripple current. The value of the capacitor, denoted as C_{PV} is given by:

$$C_{PV} = \frac{P_{PV}}{2\omega_g V_{PV}\Delta V_{PV}} \tag{5.13}$$

Where P_{PV} is the power rating of the PV panel, ΔV_{PV} is the allowable ripple content in the PV voltage and ω_g is the fundamental value of the grid frequency.

5.3.3 Output Filter Calculations

The primary function of the output filter (Fig. 5.1) is to eliminate high frequency content in the output voltage (V_{AB}). The ST and the NST modes cause high frequency transitions in the output voltage as well as the CMV. The modulation scheme, explained in the earlier section, clamps the CMV to a value of zero during the zero-period. However, CMV still contains high frequency transitions due to ST mode of operation. The output filter, apart from providing a purely sinusoidal output voltage, is instrumental in attenuating the high-frequency transition across the parasitic capacitor (which is the root cause of leakage current).

As seen in Fig. 5.1 the filter structure is a modified form of the conventional LC filter, wherein the filter inductor is split into 4 parts. Similarly, the filter capacitor is split into two halves with their mid-point connected to point '*N*'. The lumped value of the LC-filter is given by[100]:

$$f_{LC} = \frac{1}{2\pi\sqrt{L_f C_f}} \tag{5.14}$$

5.4 Control Schemes for the Proposed Topology

As stated earlier, the proposed power converter is capable of two modes of operation namely, the standalone mode and the grid-connected mode. Two separate controllers have been developed to control it in these two modes of operation, which are described in detail in the sub-sections that follow.

5.4.1 Standalone Mode

Fig. 5.4(a) shows a detailed schematic diagram of the control system, which is used in the standalone mode. This control system employs a two-loop control structure to obtain fast dynamic response. It regulates the DC-link voltage with its outer loop, while the inner loop controls the input current (i_{LI}). The outer loop regulates the peak value of the dc-link voltage (V_{DC}) by controlling the ST duty ratio (D_s). For the proposed PV converter, MPPT is obtained with well-known perturb and observe (*P&O*) method[60]. Based on the voltage (V_{PV}) and current (I_{PV}) of the PV panels, the MPPT algorithm provides the reference (required) value of the input voltage V_{PV}^*. The error between the required and the actual values of the input voltage is compensated by a PI controller, which outputs the reference value for the peak dc-link voltage (V_{DC}^*). This reference is then compared with the peak value of the DC-link voltage, which is measured by exploiting the symmetrical nature of the qZS networks (Fig. 5.1).

Exploiting the symmetrical nature of the qZS networks, eqn. 6 becomes:

$$\hat{V}_{DC} = 2(V_{C1} + V_{C2}) \tag{5.15}$$

The measured and the reference values of the peak dc-link voltages are then compared and their difference is compensated with the aid of another PI controller. The output of the PI controller provides the reference value of the input current i_{L1}^*. The error between the reference and actual values of the input current ($i.e. i_{L1}^* - i_{L1}$) is compensated by a Proportional (P) controller, which outputs the signal that controls the ST duty ratio (D_s). It should be noted that the DC-link voltage is affected by both source and load disturbances. As

the modulation index is held constant, the regulation of the DC-link voltage paves way to the regulation of the output voltage as well.

5.4.2 Grid Connected Mode

In this mode of operation, both the ST duty ratio and the modulation index are controlled. Thus, the controller shown in Fig. 5.4 is augmented with the one shown in Fig. 5.4, which determines the modulation index. Apart from the regulation of the DC-link voltage, this control system tries to inject active power into the grid at UPF. These objectives are fulfilled by processing the PV voltage (V_{PV}), PV current (I_{PV}) and the grid voltage (V_g) with a *reference generation block* that generates the reference signal for the peak value of the grid current (denoted as $I_{grid,peak}$ in Fig. 5.4), which is given by:

$$I_{Grid,peak} = \frac{\sqrt{2}\, V_{PV} I_{PV}}{V_{grid}} \tag{5.16}$$

The reference value of the peak grid current is then multiplied with a unit-sine wave, which is synchronized to the mains using a PLL. This signal serves as the instantaneous reference waveform for the grid current. The error between the instantaneous reference and the actual grid currents is then compensated with a PR controller, which outputs a signal that determines the modulation index (m). This modulation signal is employed to generate the gating signals as described in the earlier section.

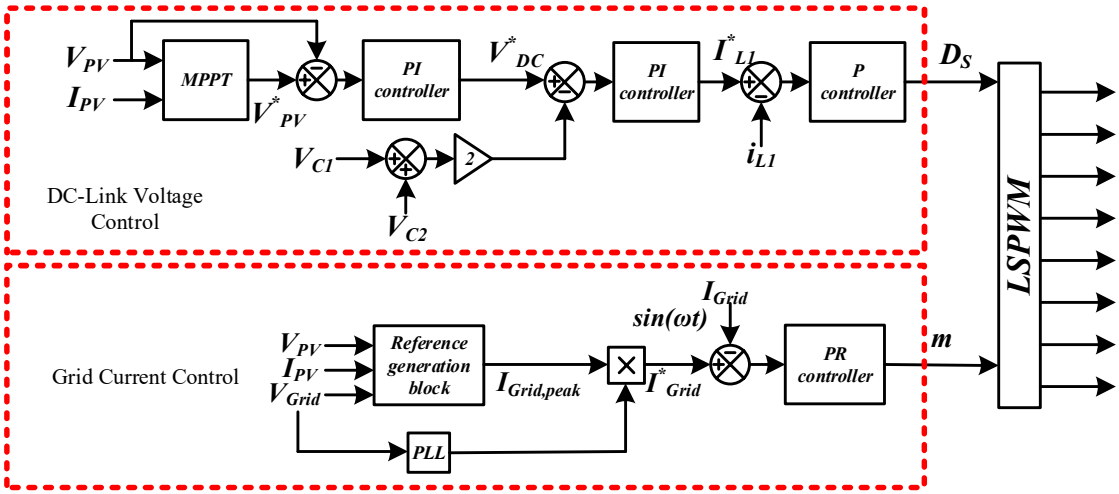


Figure 5.4 Control schematic for the proposed Power converter (DC-link control and grid current control).

5.5 Leakage Current Analysis

The leakage current that flows between PV panels and load is mainly due to CMV and interaction among various components such as junction capacitance of power semiconductor switching devices, parasitic elements of the filter, parasitic elements in the leakage path, and

passive components of the quasi-Z-sources (Fig. 5.5(a)). The CMV of the proposed power converter (Fig. 5.1) is given by [91], [107]

$$V_{CMV} = \frac{V_{AN}+V_{BN}}{2} \tag{5.17}$$

The terms V_{AN}, V_{BN} and V_{CMV} can be represented in terms of switching functions [107] by:

$$V_{AN} = [0.5\{S_3S_5S_6\} + \{S_1S_3\} + 0.5]V_{DC} \tag{5.18}$$

$$V_{BN} = [0.5\{S_4S_5S_6\} + \{S_2S_4\} + 0.5]V_{DC} \tag{5.19}$$

$$V_{CMV} = 0.25\,V_{DC}\,[\{S_5S_6S_3\} + 2\{S_1S_3\} + \{S_5S_6S_4\} + 2\{S_2S_4\} + 2] \tag{5.20}$$

The equivalent circuit of the proposed converter with respect to sources V_{AN} and V_{BN} is shown in Fig 5.5(b), from which it is evident that the leakage current is caused by the potential difference between point *A* and *B* w.r.t point *N* Fig. 5.5(c) shows the common-mode equivalent circuit which shows that the common-mode voltage (V_{CMV}) causes leakage current. The magnitude of the leakage current is principally determined by the values of ground resistance (R_g) and the parasitic capacitance (C_{PAR}). From Fig. 5.5(c) the leakage current (i_{LEAK}) is given by:

$$i_{LEAK} = C_{PAR}\frac{dV_{PAR}}{dt} + \frac{V_{CMV}}{R_g} \tag{5.21}$$

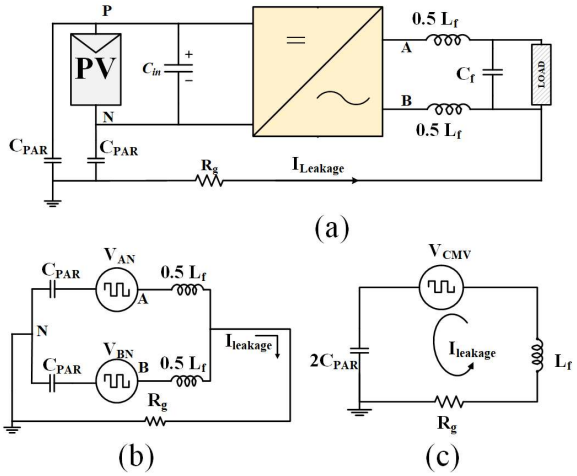


Figure 5.5 Representation of circuit with parasitic elements; (a) Entire system with parasitic elements. (b) Equivalent circuit of the proposed converter in terms of terminal voltage V_{AN} and V_{BN}. (c) Common Mode equivalent circuit.

Where, V_{PAR} represents the voltage across the parasitic capacitance. From eqn. 5.21, it is evident that the leakage current is directly proportional to the value of the parasitic capacitance (C_{PAR}) and is inversely proportional to the ground resistance (R_g). As stated earlier, the value of the parasitic capacitance varies in the range of (7nF - 220nF) /kW [16],

[17] depending upon numerous factors such as the type of panels, distance between frame and ground, weather and aging conditions.

Fig. 5.6 shows the relationship between the estimated leakage current for the proposed converter w.r.t the values of C_{PAR} and R_g, assuming that the average value of CMV is 50V. This plot reveals that the leakage current is reduced at low values of parasitic capacitance and high values of ground impedance.

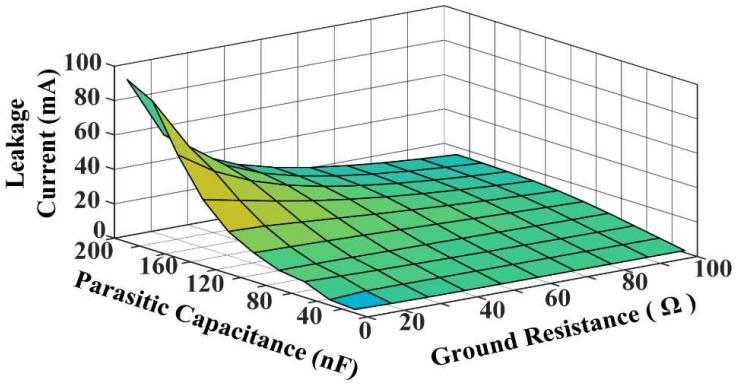


Figure 5.6 Variation of leakage current with respect to ground resistance and parasitic capacitance.

5.6 Results and Discussions

The performance of the proposed power converter assessed with simulation studies using the MATLAB/Simulink platform, assuming that the power semiconductor switching devices and the diodes are ideal. Table 5.2 provides the values of various passive elements, which are used for both simulation studies and experimental verification. An input PV voltage (V_{in}) of 100 V, output voltage ($V_{o,rms}$) of 110 V (RMS) and modulation index (m) of 0.7 were employed during simulation as well as experimentation. With the selected ST duty ratio of 0.27, a boost factor of 2.2 is obtained (eqn. 5.4 and 5.5).

5.6.1 Simulation Results

The steady state performance of the proposed converter is shown in Fig. 5.7. The pulsating dc-link voltage waveform is presented in Fig. 5.7(a), which clearly demonstrates the voltage boosting capability of qZS network by a factor of 2.2 (100V to 220V). The output of the inverter is shown in Fig. 5.7(b), which clearly shows 5 voltage levels ($\pm V_{DC}/2$, $\pm V_{DC}$and zero, Fig. 5.2). The filtered voltage and the load current (scaled to match the plot) are shown in Fig. 5.7(c). It may be noted that the waveforms of the output voltage and current are sinusoidal showing the effectiveness of the filter.

Table 5.2 Simulation and Experimental Parameters

Parameters		Values
P_O		500 W
V_{in}		100 V
V_{out} *(rms)*		110 V
Inductors	L_1-L_4	1 mH
	L_f	4 mH
Capacitors	C_1-C_4	1000 µF
	C_f	2 µF
	C_{PAR}	100 nF
Frequency	f_s	10 kHz
	f_o	50 Hz
R_g		10 Ω

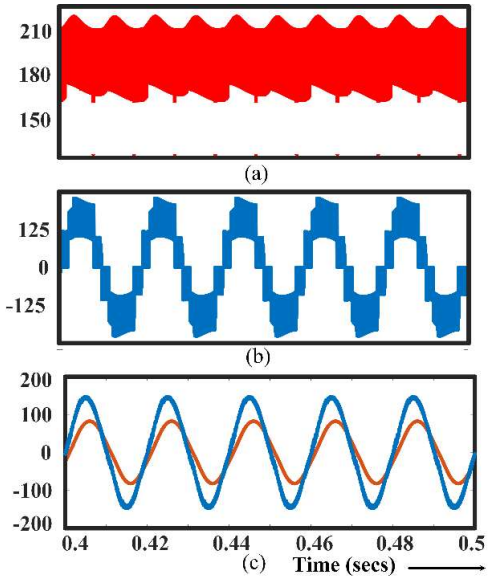


Figure 5.7 Simulated waveform of the converter in steady state. (a) Boosted dc-link. (b) Level voltage across output terminals. (c) Output voltage and current.

As explained in the earlier section, the combined effort of the modified switching scheme and the filter suppresses the high frequency transitions across the parasitic capacitance, which consequently reduces the leakage current. This fact is demonstrated in the simulation results shown in Fig. 5.8. The waveforms of the voltages V_{AN}, V_{BN} and V_{CMV} are shown in Fig. 5.8(a). The voltage across the parasitic capacitance and the corresponding leakage current are provided in Fig. 5.8(b). It is important to note that high frequency transitions are eliminated in the voltage across the parasitic capacitance and it becomes trapezoidal. As this trapezoidal waveform lacks sudden spikes and the attendant leakage current becomes low in magnitude.

As shown in Fig. 5.2(g) & Fig. 5.3(b), the modified PWM scheme turns on the switches S_7 and S_8 during the zero-state, providing a path for the circulation of the load current, which manifests as the reactive power supporting the capability of the converter. The reactive power supporting the capability of the proposed converter is shown in Fig. 5.9, wherein the phase difference between the output voltage and current waveforms is clearly visible, when the resistive load is changed to the reactive load at t = 0.8 sec. It can be also noted that the CMV of the converter drops down to a value of zero when the switch S_9 is turned on (Fig. 5.2(g)).

The dynamic performance of the proposed converter in the standalone mode is presented in Figs. 5.10 and 5.11. When the converter is subjected to a source disturbance (100 V – 120 V, Fig. 5.10), the DC-link voltage is momentarily disturbed. The control system shown in Fig. 5.4(a) readjusts the ST duty ratio to restore the DC-link voltage. A similar control action against the load disturbance is shown in Fig. 5.11.

Fig. 5.12 shows the behaviour of the proposed system for grid-tied applications. As stated earlier, the controller (shown in Fig. 5.4 (a) and 5.4 (b)) regulates both ST duty factor and the modulation index in operating mode while realizing UPF. To assess the performance of the converter in this mode, it is subjected to a disturbance in the irradiance at *t=0.8 secs* (1000W/m^2 to 700W/m^2) and at *t=1.4 secs* (700W/m^2 to 900W/m^2) and the corresponding changes in the PV power and the PV voltage are respectively shown in Fig 5.12(a). The fluctuations in PV power due to changes in irradiance manifest in grid current as shown in Fig. 5.12(a) (lower trace). The control scheme shown in Fig. 5.4 not only regulates the dc-link voltage (Fig 5.12(b)) but also maintains unity power factor operation of the grid. Fig. 5.12 (c) illustrate the voltage across the parasitic capacitor (V_{PAR}) and the leakage current (i_{LEAK}) in the grid-tied operation. It can be observed that both the quantities are immune to the disturbance in irradiance. Further, the magnitude of the leakage current is 17mA (RMS), which is significantly lower than the limit (300 mA) imposed by the *VDE-0126-1-1*.

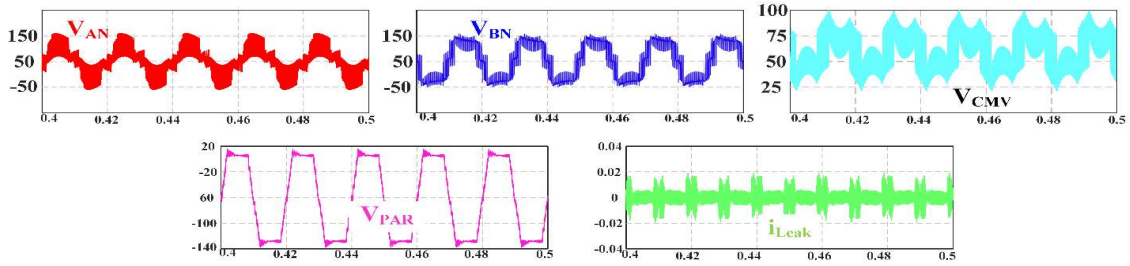


Figure 5.8 Simulation results for parasitic elements; (a) Voltages across V_{AN}, V_{BN} and V_{CMV} respectively. (b) Voltage across parasitic capacitance and leakage current.

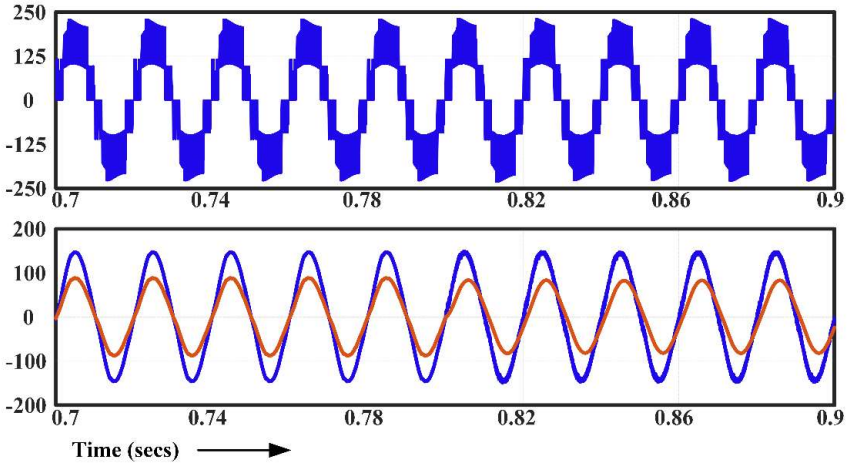


Figure 5.9 Simulated waveform demonstrating reactive power capability. (a) Level voltage of the converter. (b) Output voltage and current.

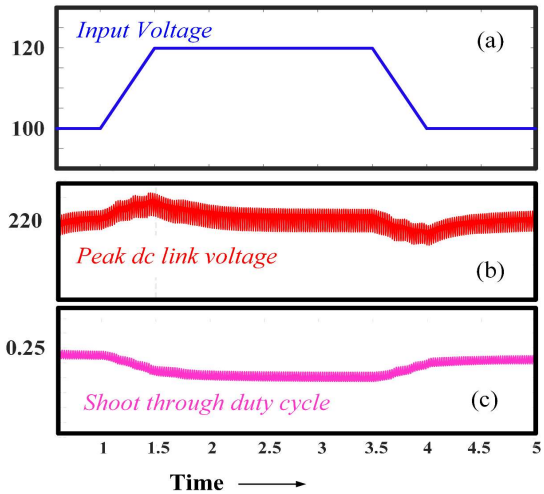


Figure 5.10 Dynamic response of the converter for change in source. (a) Change in input voltage. (b) Peak dc-link voltage variation. (c) Change in shoot though duty cycle value.

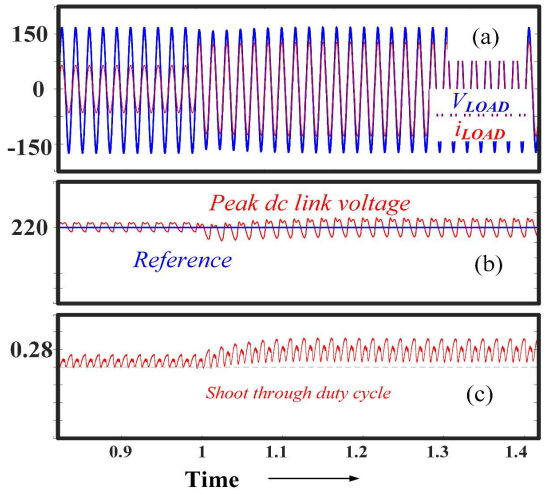


Figure 5.11 Dynamic response of system subjected to load change. (a) Simulated waveform of load voltage and current during change. (b) Reference and Peak dc-link voltage. (c) shoot through duty cycle.

5.6.2 Experimental Results

Fig. 5.13 shows the picture of a 500 W laboratory prototype, which was developed to validate the simulation studies. The prototype was built with power MOSFETs (IRFP460) and fast recovery diodes (MURS1560). The modulation scheme and the closed loop control system were implemented with Spartan 6 FPGA digital control platform. The steady-state performance of the converter in the standalone mode is presented in Fig. 5.14(a). This figure shows the plots of dc-link voltage, output voltage of the inverter, filtered output voltage and the load current respectively.

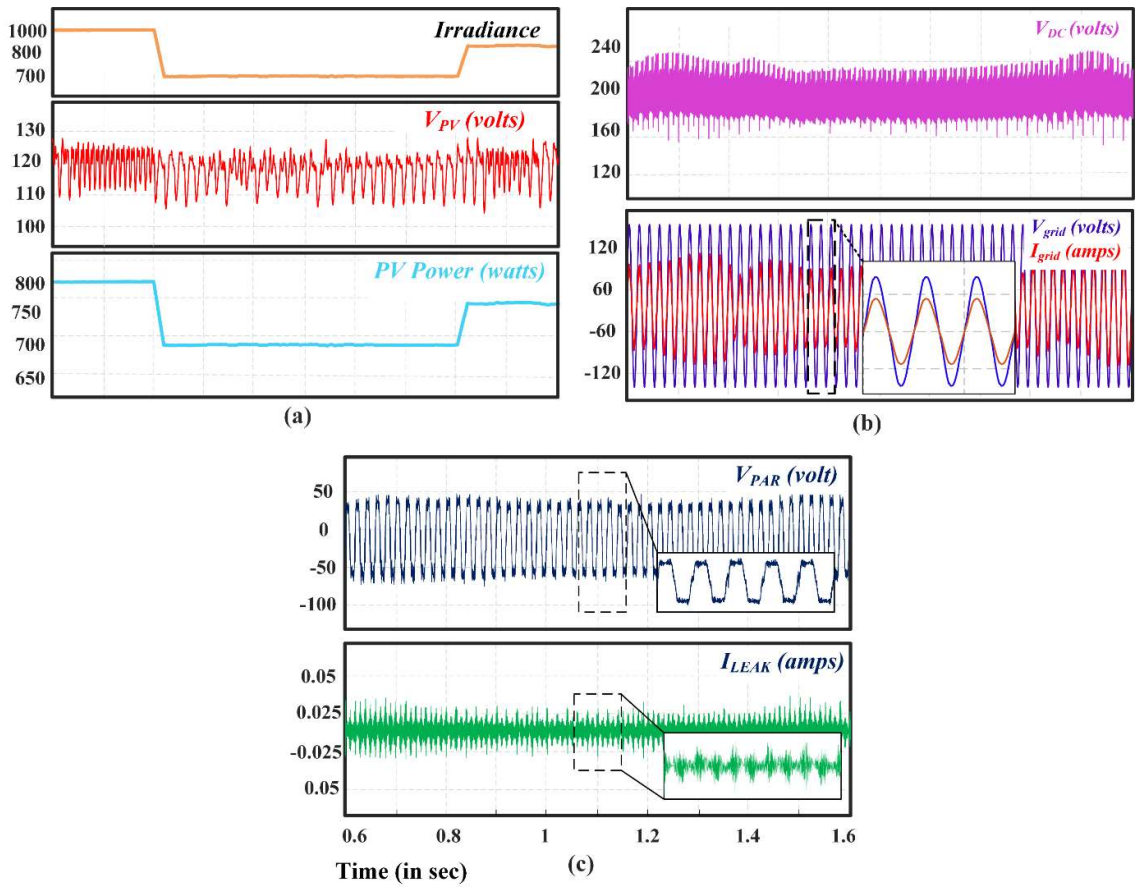


Figure 5.12 Simulation results during grid-tied mode. (a) Solar irradiance, PV Voltage and PV power. (b) Peak dc-link voltage, grid voltage and grid current. (c) Voltage across PV parasitic capacitor and Leakage current.

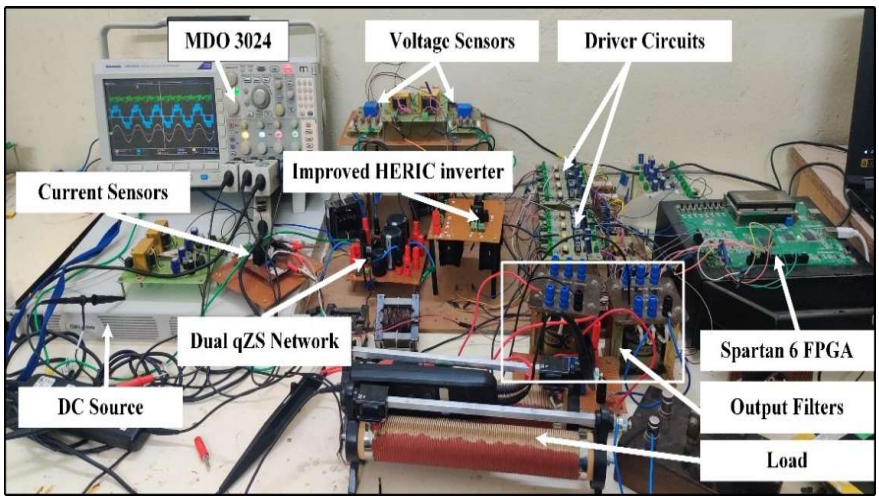


Figure 5.13 Experimental prototype of the proposed converter.

The waveforms pertaining to common mode parameters can be seen in Fig. 5.15. The top and middle traces of this figure respectively present the terminal voltages V_{AN} and V_{BN}. The CMV is shown in the bottom trace, which is calculated using (5.17). It can be observed that the shoot-through period, introduced in the zero-period of *every switching cycle*, contributes to high-frequency transitions in the CMV. As stated earlier, the combined effort of the modulation scheme and the output filter suppresses high-frequency variations. Consequently, the voltage across the parasitic capacitor (V_{PAR}, left trace of Fig. 5.8(b)), which is shown in the upper trace of Fig. 5.15(b), is rid of high-frequency transitions. This causes a reduced leakage current, which is shown in the bottom trace of Fig. 5.15 (b). The measured RMS value of this current is 15 mA, which is significantly lower than 300 mA, which is the stipulated value as per German standard *VDE 0126-1-1*.

Apart from reducing the leakage current, the modulation scheme achieves the capability of supporting reactive power, which is demonstrated in Fig. 5.16. This experiment clearly shows that the proposed power converter comfortably negotiates a sudden changeover from an initial UPF load to a 0.9 PF (lagging) load.

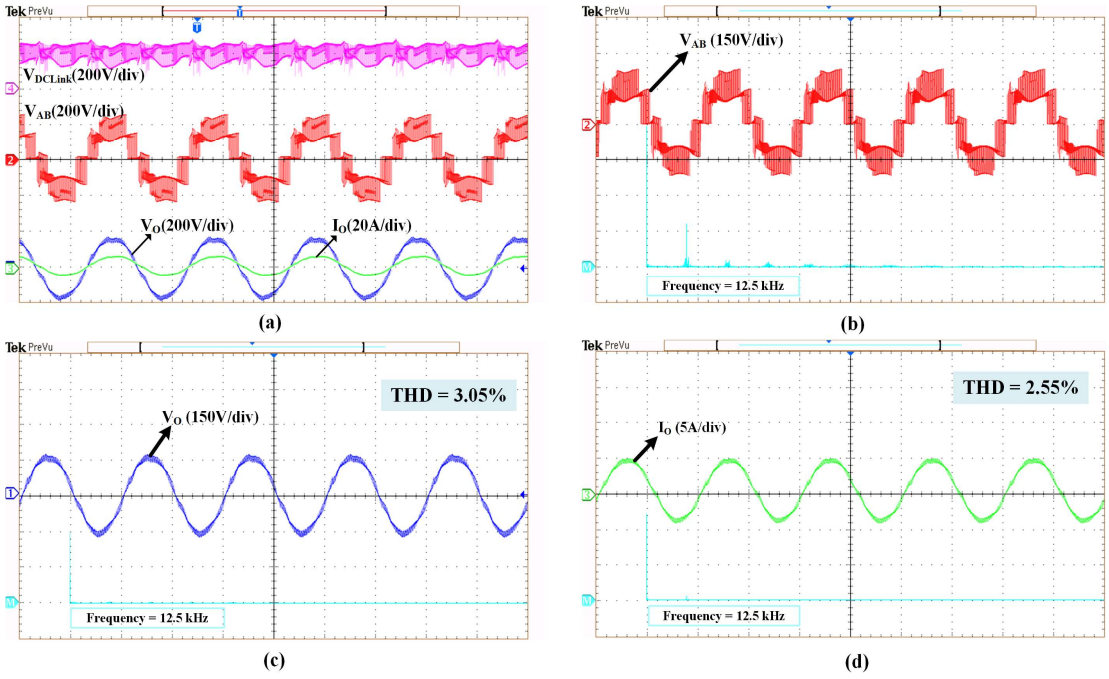


Figure 5.14 Experimental waveform of the proposed converter in steady state (a) Steady state waveform dc-link voltage, level voltage, output voltage and output current. (b) FFT of level voltage (V_{AB}). (c) FFT of output filtered voltage (V_O). (d) FFT of output current (I_O).

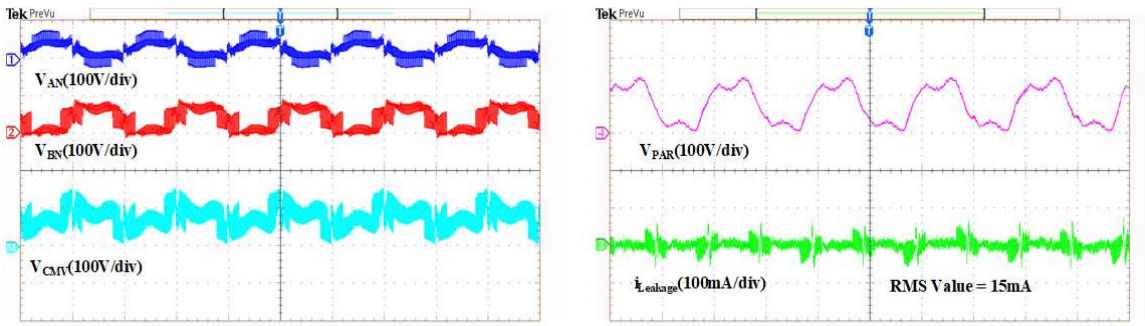


Figure 5.15 Experimental waveform for common mode parameters. (a) Waveform of V_{AN}, V_{BN} and V_{CMV}. (b) Waveforms of voltage across parasitic capacitor (V_{PAR}) and leakage current ($i_{Leakage}$).

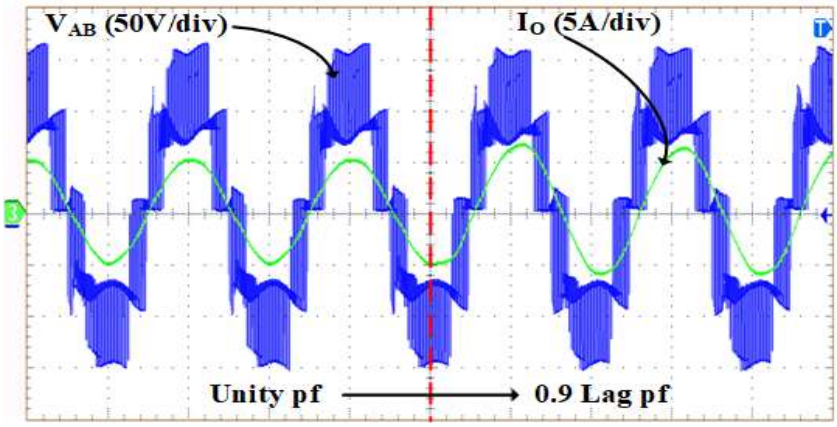


Figure 5.16 Waveform showing reactive power capability of converter.

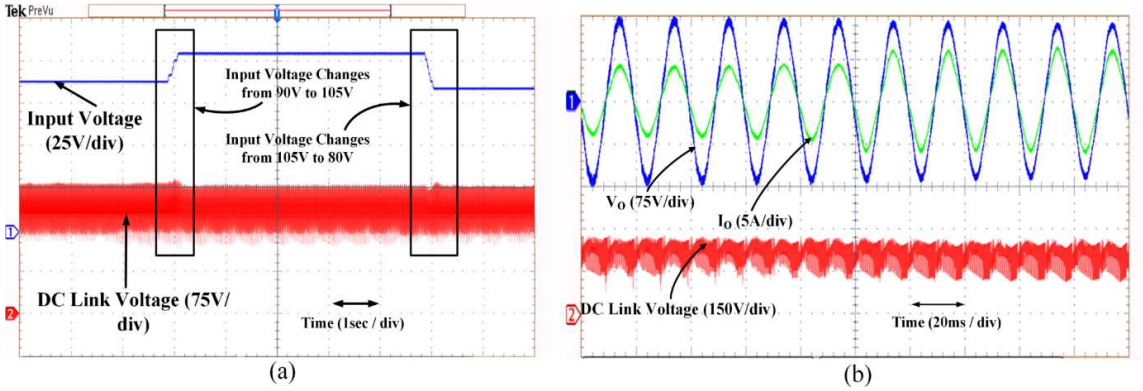
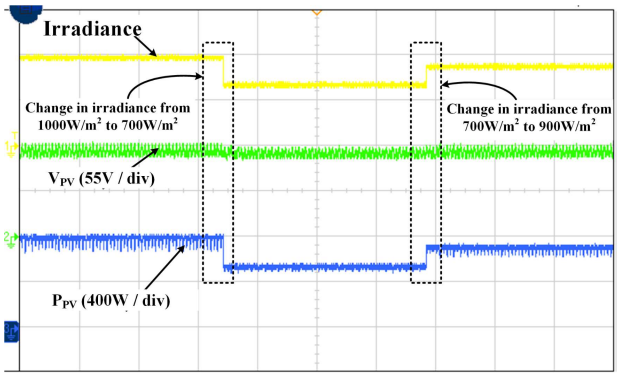
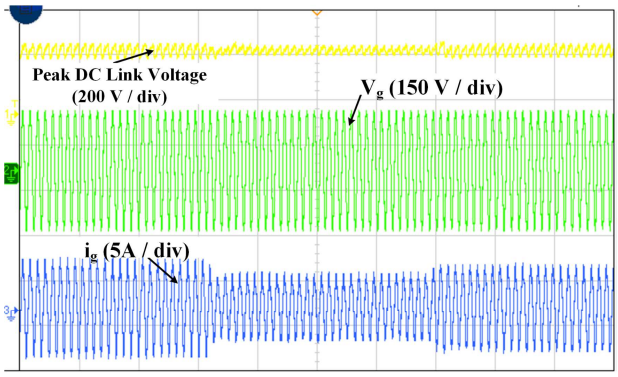


Figure 5.17 Experimental waveform for dynamic performances. (a) Dynamic performance of converter subjected to input voltage change (90V to 105 and 105 to 90V). (b) Dynamic response of the system for load changes from 2.5A to 4A.

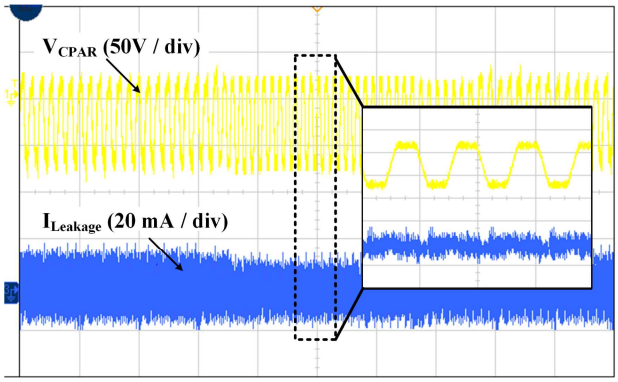
The dynamic response of the system against the source and load disturbance is shown in Fig 5.17. This experimental result clearly demonstrates the capability of the controller to regulate the DC-link voltage against source disturbances (90V to 105V and vice versa, Fig. 5.17(a)) and load disturbance (2.5A - 4A, Fig. 5.17(b)).



(a)



(b)



(c)

Figure 5.18 Results during grid-tied mode. (a) Input side parameters irradiance, PV Voltage, PV power. (b) Output side parameters Peak dc-link voltage, grid voltage and grid current. (c) Voltage across parasitic capacitor and Leakage current.

Fig. 5.18 shows the performance of the proposed power converter in the grid-tied mode of operation, which is assessed using the real-time simulator Opal-RT (OP4510) [97], [108]. In this study, irradiance is changed; firstly from 1000 W/m^2 to 700 W/m^2, and then to 900 W/m^2 (top trace, Fig. 5.18(a)). Following the first change, a drop occurs in the PV power (bottom trace) with an associated drop in PV voltage (second trace). However, the MPPT algorithm restores the PV voltage to its original value. The corresponding changes to this

disturbance in the output (peak dc-link voltage, grid voltage and grid current) are shown in Fig. 5.18(b). Due to the change in the PV power, a slight disturbance occurs in the peak value of the dc-link voltage (top-trace I Fig. 5.18(b)), which is eventually regulated by the controller (Fig 5.4(a)). The fluctuations in the irradiance (and therefore the PV power) cause the corresponding fluctuations in the grid current as shown in the bottom trace of Fig. 5.18 (b). However, the controller (Fig 5.4(b)) ensures that the power converter injects active power into the grid at UPF, despite disturbances in irradiance.

The waveforms pertaining to leakage current and the voltage across parasitic capacitor (V_{PAR}) in the grid-tied operation are shown in Fig 5.18(c). It is observed that neither this voltage(top trace) nor the leakage current (bottom trace) shows any appreciable change despite change in irradiance. Further, the RMS value of the leakage current in grid-tied operation is 17mA, which is far lower than the value stipulated by *VDE-0126-1-1*.

The experimental and real-time simulation results (Fig. 5.14 – Fig. 5.18) adequately validate the simulation results, which were presented in earlier sections for the proposed power converter.

5.6.3 Efficiency and Loss Analysis

Efficiency curves of the proposed converter at various values of output power and ST duty factors are provided in Fig. 5.19. Fig. 5.19(a) shows the efficiency obtained with PSIM simulator, which is capable of importing actual characteristics of various active devices and passive components to the power converter that is simulated [98], [109].It may be noted that the proposed converter obtains a maximum efficiency of 93% at an output power of 400 W (app.). Fig. 5.19 (b) shows the dependence of efficiency on ST duty ratio. This plot shows that the efficiency deceases (as total power loss increases), when ST duty ratio is increased. This phenomenon is attributed to increased conduction loss in ST devices (S_1, S_2, S_5 and S_6) and the qZS inductors.

Fig. 5.19(c) presents the loss distribution chart, which shows the percentage division of power loss in various active and passive elements. The copper loss incurred in the inductors is about 21% while the losses in diodes (D_1 and D_2) add up to 24% of the total loss. Out of the 9-power semiconductor switching devices, most of the losses occurs in 6 switches (S_1-S_6) while the other three switches (S_7- S_9) incur relatively low power loss. Though the proposed topology uses one more switching device compared to most of the other topologies reported in literature, the negligible power loss in 3 switches offsets this drawback.

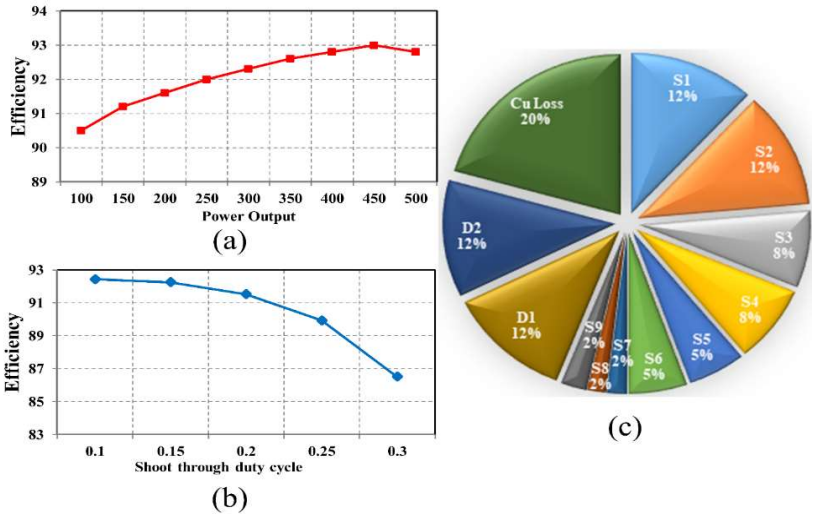


Figure 5.19 Efficiency and loss distribution; (a) Efficiency vs. output power the proposed converter, (b)Efficiency vs. shoot through duty cycle, (c) Loss distribution among various elements.

5.7. Comparison with Existing Topologies

Table 5.3 presents the comparison of the proposed topology with similar power converter configurations reported in the literature. From Table 5.3, it may be noted that the proposed converter requires the fewest conducting switches for the generation of voltage levels and ST modes, making it more reliable and efficient. Though the common ground-based topologies [101], [103], [104]display excellent suppression of leakage current, they require an additional voltage boosting stage. Also, they have a higher total blocking voltage (TBV), which is defined as the sum of the blocking voltages of individual switches. Despite the ability of variable boosting, the 5L-CGBT-ANPC converter[104] requires a high TBV and a floating capacitor. The converter reported in [101]needs an identical number of conducting switches; but it outputs only a three-level waveform. On the other hand, the qZS five-level inverters reported in[79], [83], [87], [89], result in higher leakage current.

The qZS-CMI[83]has a similar passive component count as that of the proposed converter. However, higher losses are incurred in this converter as it needs more conducting switches to generate the output voltage while requiring double the number of PV sources to feed the converter. The MqZS, reported in[89], needs a lower number of switching devices and passive components compared to the proposed power converter. However, this advantage is outweighed by the requirement of an additional input diode, which results in discontinuous input current.

Table 5.3 Complete Comparison of Proposed Topology with Existing Topologies

Type of converter		Proposed	[104]	[103]	[101]	[73]	[68]	[72]	[75]	[89]	[79]	[83]	[87]
Levels		5	5	5	3	3	3	3	3	5	5	5	5
Components Count	S*	9	7	9	7	6	6	6	6	8	8	8	8
	D*	2	0	1	1	1	2	3	1	3	2	2	6
	L*	4	1	0	0	2	2	2	3	2	4	4	4
	C*	4	2	3	2	2	2	2	3	4	4	4	4
Total Blocking Voltage		$7.5*V_{DC}$	$12*V_{DC}$	$10*V_{DC}$	$10*V_{DC}$	$6*V_{DC}$	$6*V_{DC}$	$6*V_{DC}$	$6*V_{DC}$	$6*V_{DC}$	$6*V_{DC}$	$4*V_{DC}$	$6*V_{DC}$
Sources required		1	1	1	1	1	1	1	1	1	2	2	1
PWM		Unipolar	Unipolar	Unipolar	Unipolar	Unipolar	Unipolar	Unipolar	Unipolar	Unipolar	Unipolar	Unipolar	Unipolar
Maximum conducting switches		3	4	4	3	3	6	5	4	4	3	4	4
Variable Boosting Feature		Yes	Yes	No	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Reactive power support		Yes	Yes	Yes	Yes	No	Yes	Yes	No	No	No	No	No
Capacitor charge balancing		Not Needed	Inherent	Inherent	Inherent	Not Needed	Not Needed	Not Needed	Not Needed	Not Needed	Not Needed	Not Needed	Not Needed
Leakage current		Low	Zero	Zero	Zero	Low	Low	Low	Low	NA	NA	NA	NA
Source Shoot through risk		No	No	Yes	Yes	No	No	No	No	No	No	No	No

* S=Switches, D=Diodes, L=inductors, C=Capacitors

Table 5.4 Voltage Stress Comparison

Components	Diodes	Capacitor	Switches
[87]	$\frac{1}{\sqrt{2(1-D)}}$	$\frac{1}{\sqrt{2}}, \quad \frac{1}{\sqrt{2}}\frac{D}{1-D}$	$\frac{1}{\sqrt{2(1-D)}}$
[83]	$\frac{1}{\sqrt{2(1-D)}}$	$\frac{1}{\sqrt{2}}, \quad \frac{1}{\sqrt{2}}\frac{D}{1-D}$	$\frac{1}{\sqrt{2(1-D)}}$
[79]	$\frac{1}{\sqrt{2(1-D)}}$	$\frac{1}{\sqrt{2}}, \quad \frac{1}{\sqrt{2}}\frac{D}{1-D}$	$\frac{1}{\sqrt{2(1-D)}}, \quad \frac{\sqrt{2}}{(1-D)}$
[89]	$\frac{1}{\sqrt{2(1-D)}}$	$\frac{1}{\sqrt{2}}, \quad \frac{1}{\sqrt{2}}\frac{D}{1-D}$	$\frac{1}{\sqrt{2(1-D)}}, \quad \frac{\sqrt{2}}{(1-D)}$
[75]	$\frac{1}{\sqrt{2(1-D)}}$	$\frac{1}{\sqrt{2}}, \quad \frac{1}{\sqrt{2}}\frac{D}{1-D}$	$\frac{\sqrt{2}}{(1-D)}$
[72]	$\frac{1}{\sqrt{2(1-D)}}$	$\frac{1}{\sqrt{2}}, \quad \frac{1}{\sqrt{2}}\frac{D}{1-D}$	$\frac{\sqrt{2}}{(1-D)}$
[68]	$\frac{1}{\sqrt{2(1-D)}}$	$\frac{1}{\sqrt{2}}$	$\frac{\sqrt{2}}{(1-D)}$
[73]	$\frac{1}{\sqrt{2(1-D)}}$	$\frac{1}{\sqrt{2}}, \quad \frac{1}{\sqrt{2}}\frac{D}{1-D}$	$\frac{\sqrt{2}}{(1-D)}$
[101]	$\frac{\sqrt{2}}{m}$	$\frac{\sqrt{2}}{m}, \quad \frac{2\sqrt{2}}{m}$	$\frac{\sqrt{2}}{m}$
[103]	$\frac{2\sqrt{2}}{m}$	$\frac{\sqrt{2}}{m}, \quad \frac{2\sqrt{2}}{m}$	$\frac{\sqrt{2}}{m}$
[104]	----	$\frac{\sqrt{2}}{m}, \quad \frac{2\sqrt{2}}{m}$	$\frac{\sqrt{2}}{m}$
Proposed	$\frac{1}{\sqrt{2(1-D)}}$	$\frac{1}{\sqrt{2}}, \quad \frac{1}{\sqrt{2}}\frac{D}{1-D}$	$\frac{1}{\sqrt{2(1-D)}}, \quad \frac{\sqrt{2}}{(1-D)}$

Table 5.4 shows the voltage stresses (defined as the ratio of the blocking voltage across the device / component to the RMS value of the output voltage) borne by the switching devices in these converters. Due to their higher TBVs, the common ground-based topologies need to handle higher voltage stress, making them vulnerable. The voltage stresses on the capacitors of qZS based topologies[79], [83], [87], [89] are the same. For qZS-NPC[87]and qZS-CMI[83] topologies, the voltage stresses for all the switches are the same, as they block half of the boosted dc-link voltage. In contrast, some the switches of the proposed power converter are constrained to support the complete dc-link voltage, doubling the stress on them.

5.8 Summary

In this chapter, a dual-quasi-Z-source based single-stage, single-phase, five-level inverter for PV applications was presented. The proposed converter employs two back-to-back connected conventional qZS networks to boost input PV voltage. A T-type arm is fused with an improved HERIC network to obtain the output, which derives the following benefits: (i) freewheeling of load current is accomplished without the aid of the level generating switches (ii) isolation of AC and DC sides and, (iii) achievement of a CMV of zero by clamping neutral point during the zero-state.

A modified modulation scheme is employed for the proposed converter, which achieves the twin objectives of deriving a five-level boosted output and reactive power capability. A modified filter structure is used to attenuate high frequency transitions in CMV to keep the leakage current well within the standards specified by *VDE 0126-1-1*.

Simulation studies validate the operating principle of the proposed converter and its performance in both steady-state and dynamic conditions. The simulation results are then validated with the aid of a laboratory prototype. Both simulation and experimental results demonstrate the effectiveness of the combination of modulation scheme and the filter structure to suppress the leakage current.

Furthermore, the proposed converter is compared with various qZS based five-level inverter topologies in terms of the number of active switches and passive components, voltage stresses and the TBV. This comparison reveals that the proposed converter incurs the lowest power loss. With these features and advantages, it is envisaged that the proposed single-stage power converter could be useful for PV generation.

Chapter 6

COMPARATIVE ASSESSMENT

Chapter 6

Comparative Assessment

In this chapter, for better understanding the merits of the proposed topology, a detailed comparison of existing qZS based single-phase 5-level topologies [79], [83], [87], [89] with the proposed topologies is presented in Table 6.1. From the table it can be observed that the proposed topologies have fewer number of power semiconductor devices than the existing topologies. The bidirectional clamped switches help in clamping the midpoint of IS structure which provides an additional voltage level while clamping clamps the CMV to a voltage level of zero. The proposed topology-1 and 2 have the lowest TBV which makes the voltage stress lowest. However, in the proposed work 2 and 3 has the lowest number of diodes in the structure which makes the system less prone to failure. The proposed topologies require a fewer number of sources than the existing one which makes them advantageous for PV applications. It can be well observed that the proposed topologies have a definitive advantage over the existing topologies in terms of reactive power support and utilises a fewer number of power semiconductor devices to generate output voltage levels. Moreover, the leakage current issue is discussed in the proposed work which makes the topology a viable solution for PV applications.

Similarly, this table also provides a clear insight of comparisons among the proposed topologies which have their own advantages and drawbacks. The proposed topology-1 performs better in terms of TBV and efficiency, but the presence of higher number of diodes in the structure makes it more prone to failure and requires more number of conducting devices in a cycle. The proposed topology-2 is advantageous in terms of the lower number of power semiconductor devices and utilises fewer devices to produce output voltage. The DC bypass switch present in the structure to reduce the leakage current is in a conduction state in most of the time, which makes its efficiency lower than the other two topologies. However, the proposed topology-3 outperforms the other 2 in terms of leakage current reduction. It achieves the lowest leakage current in AC decoupling method while efficiency is similar to that of topology-1. This topology suffers from some drawbacks such as higher requirement of switching devices which in return increases the total blocking voltage of the system. Evaluating in terms of leakage current the German standard VDE-0126-1-1 suggests that it should less than 300mA. All the proposed inverter keeps the leakage current under 20mA

which is around 90% reduction in leakage current. Evaluated in terms of efficiency existing qZS based inverters achieves an efficiency of around 94%, but the proposed converter attains around 95% of maximum efficiency.

Table 6.1. Comparative Analysis of Proposed Topologies with Existing qZS based Five-Level Topologies

Features	qZS NPC	qZS-CMI	MqZS	qZS-HBI	Proposed work-1	Proposed work-2	Proposed work-3
Levels	5	5	5	5	5	5	5
No. of Switches(BDC*)	8(0)	8(0)	8(0)	8(0)	6(1)	5(1)	5(2)
No. of Inductors	4	4	2	4	4	4	4
No. of Capacitors	4	4	4	4	4	4	4
No. of Diodes	6	2	3	2	4	2	2
Total blocking voltage	$6V_{DC}$	$4V_{DC}$	$6V_{DC}$	$6V_{DC}$	$5V_{DC}$	$5.5V_{DC}$	$7.5V_{DC}$
Type of PWM scheme	Unipolar	Unipolar	Unipolar	Unipolar	Unipolar	Unipolar	Unipolar
Boosting	Yes, Variable	Yes, Variable	Yes, Variable	Yes, Variable	Yes, Variable	Yes, Variable	Yes, Variable
No. of Sources	1	2	1	2	1	1	1
Reactive Power Capability	No	No	No	No	Yes	Yes	Yes
Leakage Current	Not Addressed	Not Addressed	Not Addressed	Not Addressed	Addressed, 20 mA	Addressed, 20 mA	Addressed, 15 mA
Maximum no. of switch conducting at a time	4	4	4	3	4	3	3
Reported Efficiency (%)	94	90	91	91	95	92	94

*BDC Bidirectional Clamped

Chapter 7

CONCLUSION AND FUTURE SCOPE

Chapter 7

Conclusion and Future Scope

7.1. Conclusion

RES based power supply system is getting popular due to its availability, economic feasibility and eco-friendly nature. PV is treated as primary source due to the advantage of lower investment, absence of rotating parts, low carbon emission, low maintenance and installation cost. However, development of power conditioners plays a vital role to interface the PV modules for standalone and grid connection operations. The use of conventional single-stage and two-stage system has its own merits and demerits and the placement of transformer either on the low frequency side or high-frequency side has its own limitations of size, cost, reliability and low efficiency. Owing to the aforesaid problems, transformerless single stage boost inverters are becoming popular in the present scenario due to their compactness and higher efficiency. Quasi Z-Source inverter has emerged as an attractive solution with the merits of buck-boost capability with a single-stage operation, continuous input current, low component size, high efficiency and reliability.

In contemporary times, multilevel inverters are gaining attention due to reduced part count, low voltage stress across the devices, low total harmonic distortion and reduced filter size. However, it demands more PV panels being buck in nature. Therefore, imposing the benefits of both impedance source and MLIs will be a better solution for PV applications. However, leakage current issue is a major concern in transformerless inverters due to the direct connection between PV panels and grid. The leakage current value is greatly dependent on value of parasitic capacitance and voltage variation across parasitic capacitance. This flow of leakage current can cause various issues like EMI, reduces the life span of PV panels, operational insecurity and decreases the reliability. Due to inverter switching action there exists high frequency variations on common mode voltage (CMV) which excite the resonant circuit amongst various parasitic of the circuit for the flow of leakage current. To overcome the issue of leakage current, various topologies have been identified in literature based on DC based decoupling, AC based decoupling and Mid-point clamping. Therefore, for successful reduction in leakage current a hybrid method must be investigated.

To address the aforesaid problems, in this thesis, a detailed literature review was carried out based on impedance source inverters, transformerless inverters and impedance source based multilevel inverters. After reviewing various topologies, the following objectives have been derived for investigations:

- Comprehensive literature review on impedance source (IS) networks, transformerless topologies and IS based transformerless topologies for PV-grid connected system.
- Development of new single-phase single-stage inverter topologies with the features of reduced switch count, reactive power capability, single-stage boosting, high efficiency and lower THD.
- Operation, Simulation and Validation of proposed topologies under steady state and dynamic conditions.
- Development of experimental prototype for verification in stand-alone and grid-connected mode.

To address the above-said issue, this thesis proposed three novel quasi Z-Source based Multilevel Inverter topologies incorporating feature like (i) reduced switch count, (ii) reduced leakage current, (iii) high efficiency, (iv) reactive power capability and (v) single stage boosting with inversion.

Mindful of these objectives, in the first proposal a quasi Z-Source based NPC T-type inverter was proposed for achieving benefits like single-stage boosting with inverting, reactive power capability and reduced leakage current. A hybrid method of AC decoupling and Mid-point clamping was utilized to reduce high frequency voltage transition across CMV which in return reduces leakage current. Improved PWM scheme was presented using level shift PWM and simple shoot-through method to handle a wide range of input voltage.

In the second proposal, a single-stage inverter was presented with the amalgamation of dual qZS network, T-type arm and H5 inverter topology with the benefits of a single-stage boost, reactive power capability and reduced leakage current for a PV system. A hybrid method of DC decoupling and Mid-point voltage clamping was utilized for reduction of leakage current. Furthermore, this converter employed minimum number of switches to operate at any mode, i.e., active, zero and shoot through mode of operation compared to existing inverter topologies.

In the third proposal, a seamless structure of qZS network, T-type inverter and improved HERIC structure was integrated and proposed for PV-grid-connected system.

The modulation scheme was modified to incorporate various active, zero and shoot-through states. The shoot-through states were chosen in such a way that it reduces voltage stress. Both Mid-point clamping technique and AC based decoupling was used to reduce the leakage current under the standards dictated by *VDE-0126-1-1*.

In order to evaluate the steady-state and the dynamic performances of the proposed topologies, simulation studies were performed in MATLAB/ Simulink environment and then experimentally verifying them with the aid of a laboratory prototype. The experimental setup was built using IRFP460 MOSFET switches, MURS1560 diodes, TLP250 Opto-coupler driver ICs and programmable DC supply. The control algorithm was implemented in Xilinx Spartan 6 FPGA platform. For the grid-connected mode of operation, real-time simulation studies using Opal-RT 4500 module was performed for all three proposed topologies to validate the model. To sum up, it is shown that the proposed single-phase, five-level inverter topologies has of 1) single-stage boosting, 2) reactive power handling capability, 3) low leakage current, and 4) higher efficiency of 92-95% compared to other comparable topologies. Owing to these advantages, it is envisaged that the proposed topologies could be an attractive proposition for PV generation.

7.2. Future Scope

The proposed research can be extended further in the following areas: -

- Investigations of the proposed configurations for three-phase systems.
- Investigation on other impedance source networks compatible with new MLI topologies for PV-grid connected system.
- Investigation of other single-stage and two-stage multilevel inverter topologies with reduced switch count, low leakage current, and reactive power control capability.
- Implementation of advanced predictive algorithms and advanced control schemes at various platforms for efficient tracking in PV systems.

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LIST OF PUBLICATIONS

International Journals:

1.Chinmay Kumar Das, A. Kirubakaran, V.T. Somasekhar, "**A Quasi Z-Source Based Five-Level PV Inverter with Leakage Current Reduction**," *IEEE Transactions on Industry Applications*, Vol.58, No.1, pp.400-412, 2022.

2.Chinmay Kumar Das, A. Kirubakaran, V.T. Somasekhar, K. Sateesh Kumar, "**An Improved Quasi Z-Source Based H5 Inverter with Low Leakage Current for Photovoltaic Applications**," *International Transactions on Electrical Energy Systems*, Wiley, Vol.31, No.12, pp.1-19, 2021.

International Conferences:

3. Chinmay Kumar Das, A. Kirubakaran, V.T. Somasekhar, and K. Sateesh Kumar "**A New Dual Quasi Z-Source Based T-Type Five-Level Inverter with HERIC Structure for PV System,"** *IEEE SEFET 2022, GRIET Hyderabad,* pp.1-5, 2022.

4. Chinmay Kumar Das, A. Kirubakaran, and V.T. Somasekhar, "**Improved H5 Circuit Based Five-Level Quasi Z-Source Inverter with Reduced Leakage Current**," *PEDES 2020, MNIT Jaipur*, pp.1-6, 2020.

5. Chinmay Kumar Das, A. Kirubakaran, and V.T. Somasekhar, "**A Five-Level Quasi Z-Source Based NPC Inverter for PV Applications**," *EEEIC 2019*, *Italy*, pp.1-5, 2019.

Under Review:

6. Chinmay Kumar Das, A. Kirubakaran, V.T. Somasekhar, and K. Sateesh Kumar "**A Dual Quasi-Z Source Based T-Type Five-Level Inverter with Improved HERIC Structure for Photovoltaic Applications**" *IEEE Transactions on Industry Applications***.**

Appendix-A

Simulink models for proposed topology-I

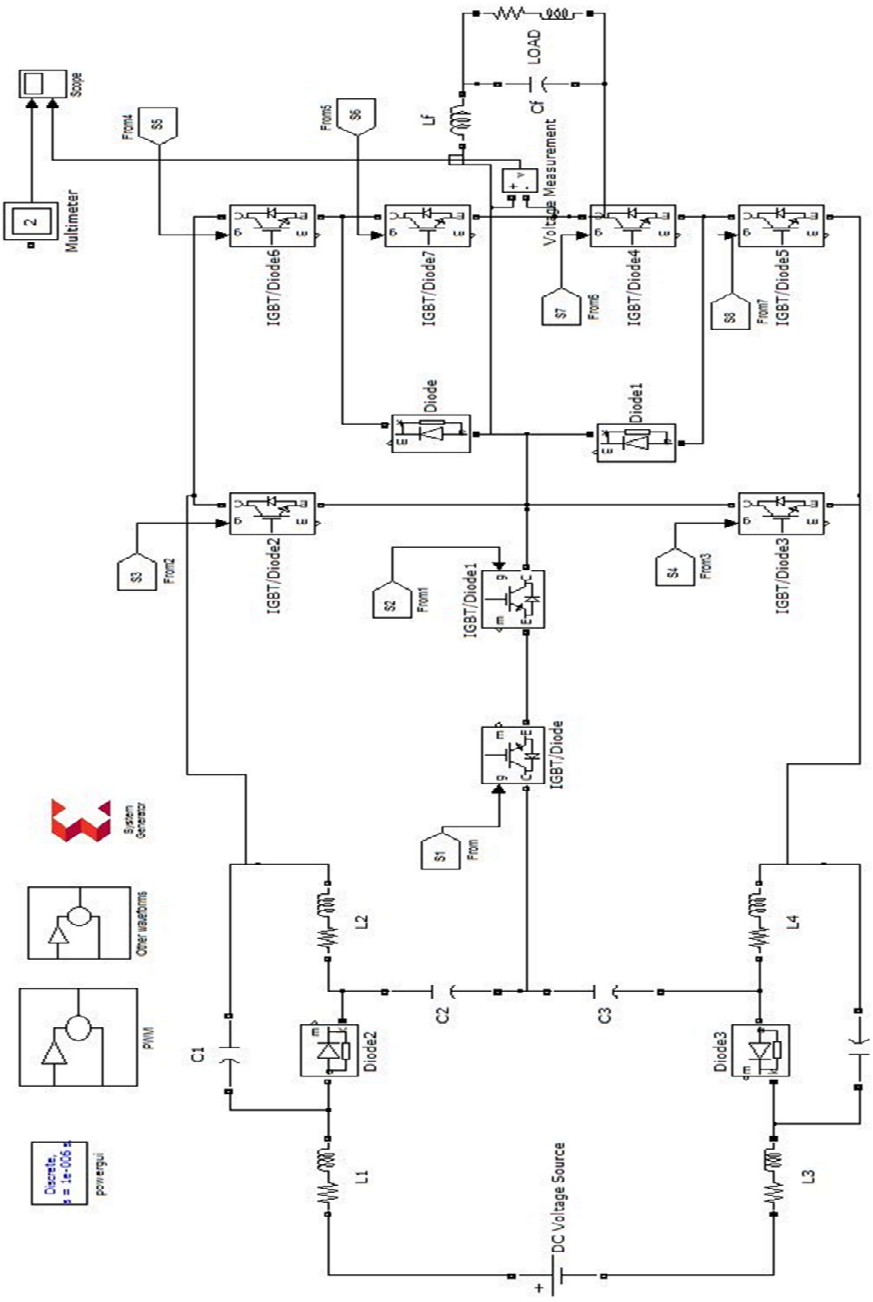

Fig. A1. Simulink model for qZS based NPC T-type inverter.

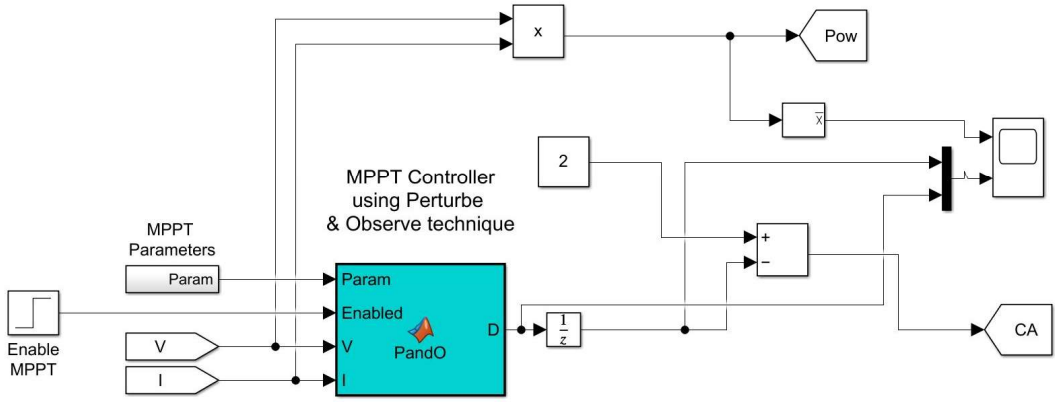

Fig. A2. Simulink model of MPPT based DC-link voltage control.

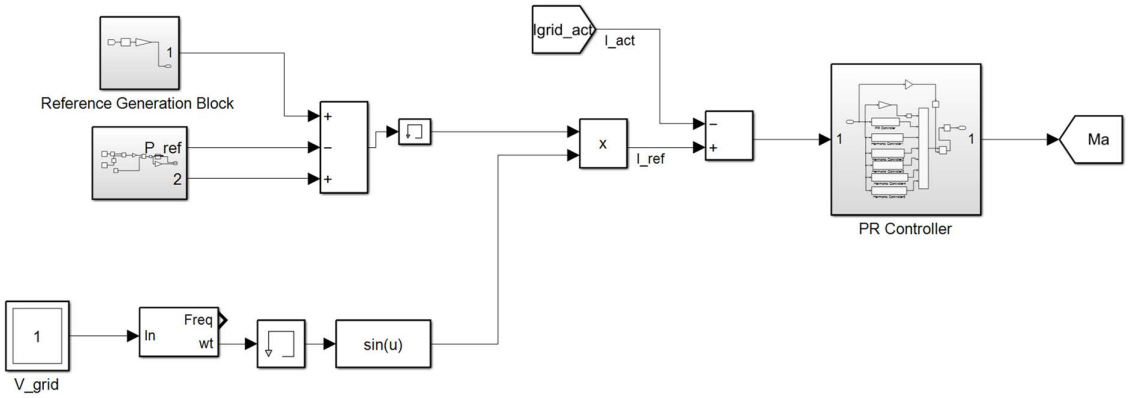

Fig. A3. Simulink model for grid current control.

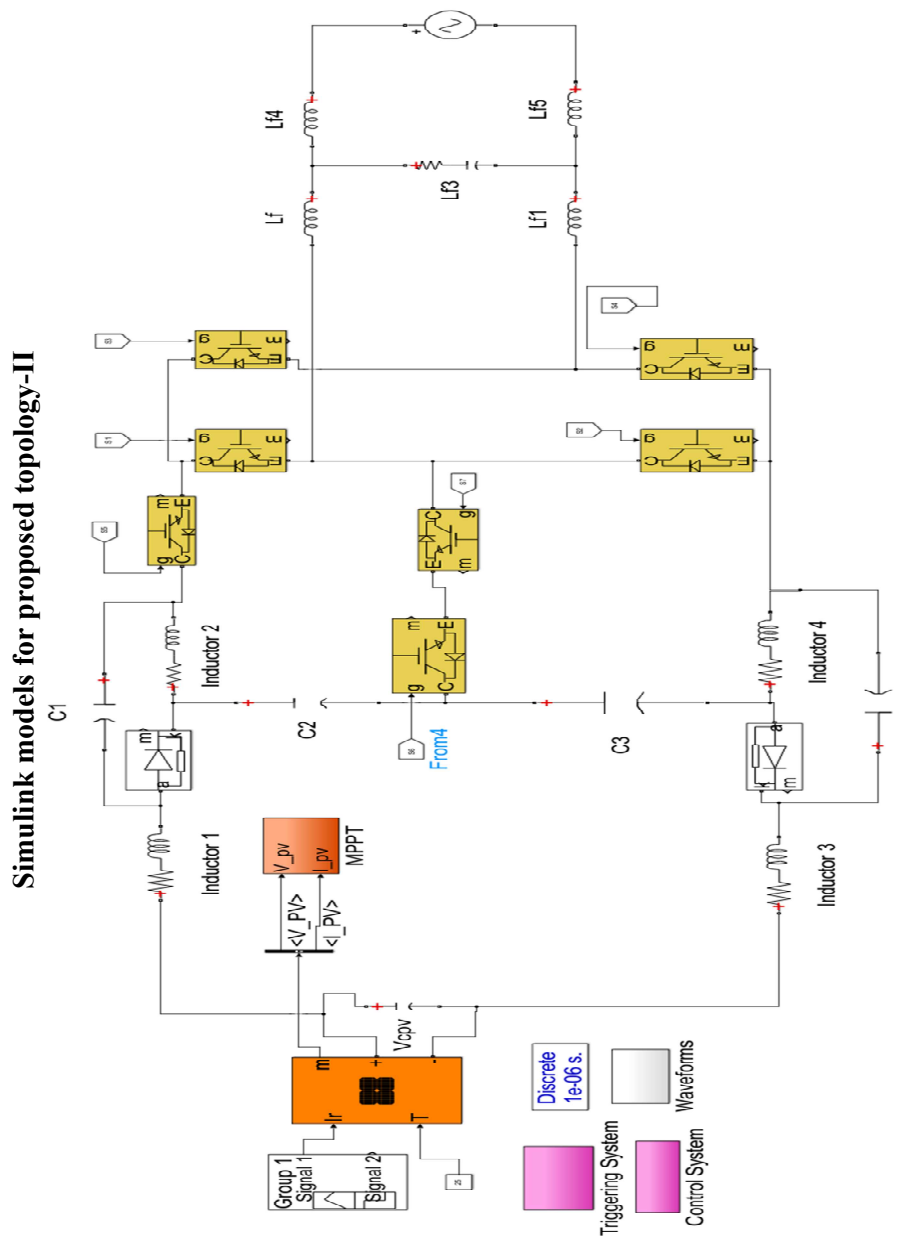

Fig. A4. Simulink model for Dual qZS based improved H5 inverter.

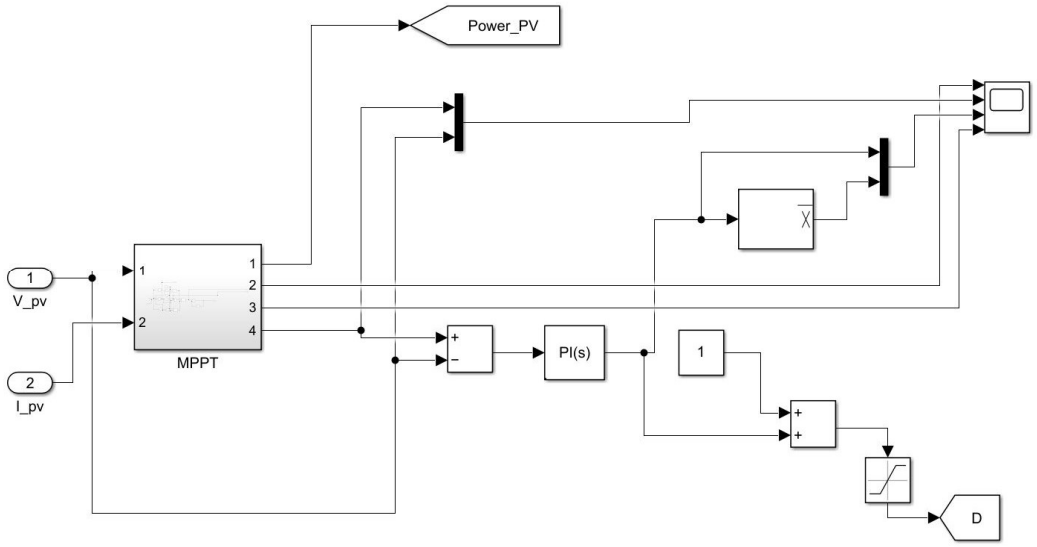

Fig. A5. Simulink model of MPPT based DC-link voltage control.

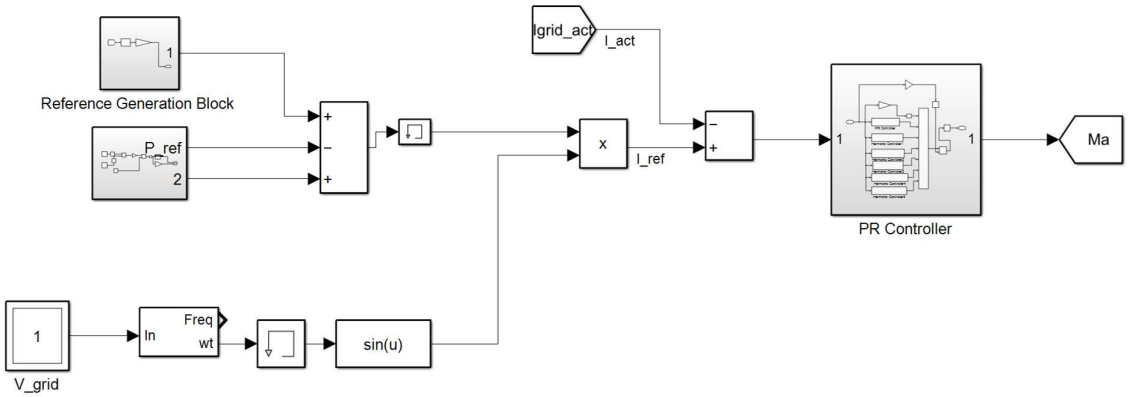

Fig. A6. Simulink model of grid current control.

Simulink models for proposed topology-III

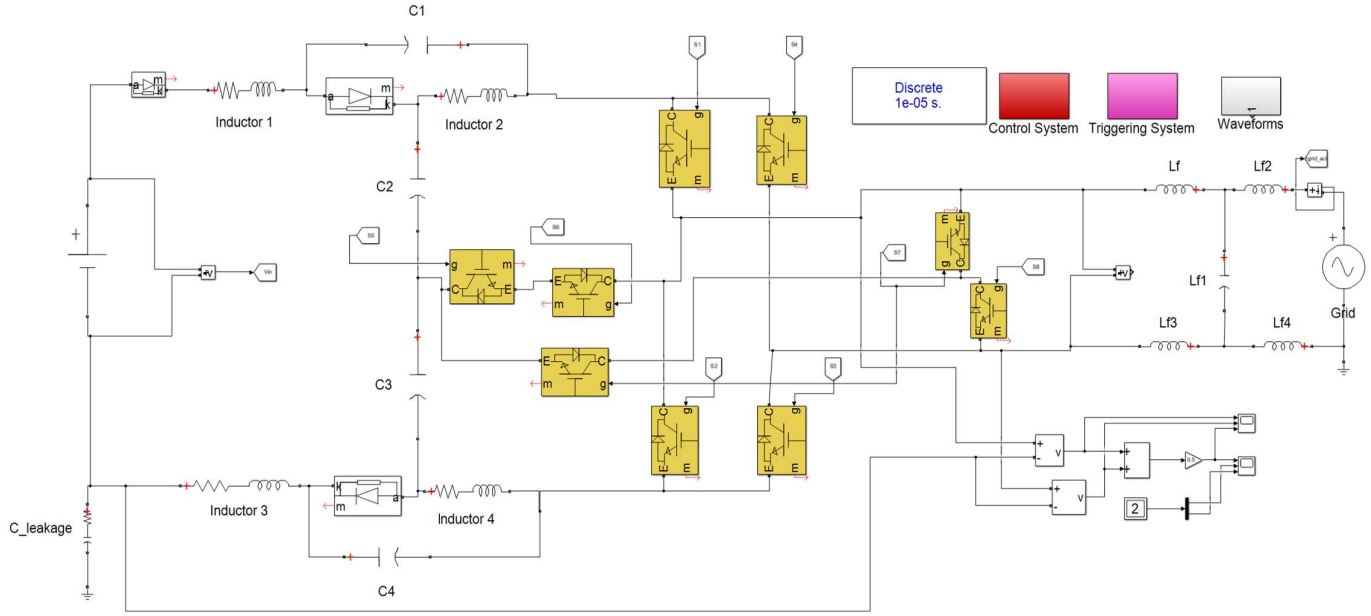

Fig. A7. Simulink model for Dual qZS based improved HERIC inverter.

Appendix-B

Procedure for generation of control pulses using XILINX tools are follows: -

1. Develop control scheme in MATLAB using Xilinx block sets.
2. Use Xilinx system generator to build the model and generate .bit file.
3. Use iMPACT software to load the generate file into flash memory of the FPGA.
4. Observe the pulses using digital oscilloscope before giving to gate driver circuit.

Generation of control pulses using Xilinx-MATLAB block sets.

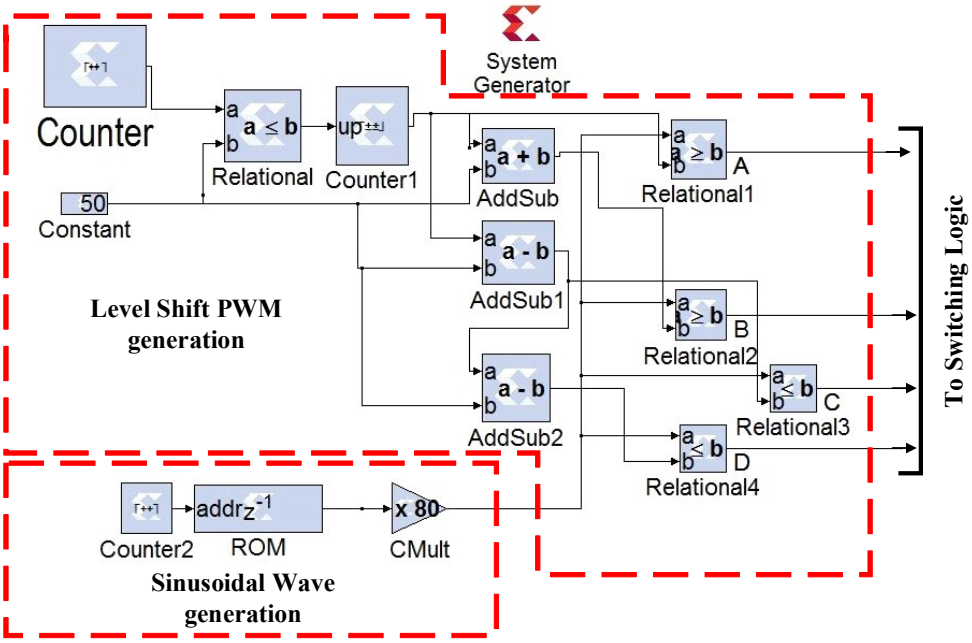

Fig. B1. FPGA-Simulink model to generate pulses using LSPWM.

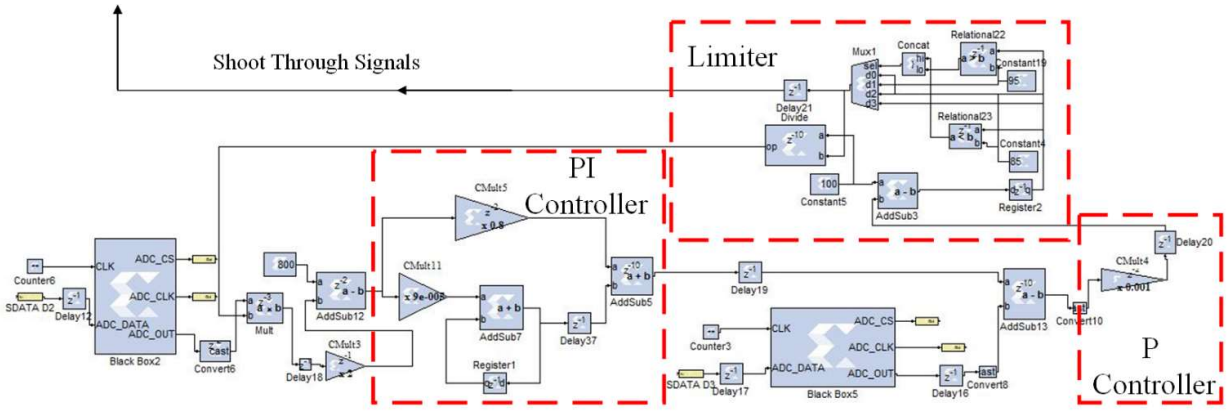

Fig. B2. FPGA-Simulink model to control DC-link voltage.

Bio-data

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Educational Qualifications

- Doctorate of Philosophy — 2019- 2022
  National Institute of Technology Warangal, Telangana.
- Master in Engineering (Power Electronics) – CGPA-8.39/10 — 2015-2017
  Birla Institute of Technology Mesra, Ranchi.
- Bachelor of Technology (Electrical Engineering)- CGPA- 7.5/10. — 2010-2014
  Parala Maharaja Engineering College, Berhampur.

Academic Achievements: -

- Qualified Olychem-2009 and attended chemistry Olympiad.
- Qualified Gate-2015 with a gate score of 443.
- Served as technical advisor to team PEAC during masters.