FAULT-TOLERANT BLDC MOTOR DRIVE CONFIGURATIONS FOR LOW-POWER ELECTRIC VEHICLE APPLICATIONS

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DOCTOR OF PHILOSOPHY

By

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CERTIFICATE

This is to certify that the thesis entitled **"Fault-Tolerant BLDC Motor Drive Configurations for Low-Power Electric Vehicle Applications"**, which is being submitted by **Mr. Patnana Hema Kumar** (Roll No. 717114), is a bonafide work submitted to National Institute of Technology, Warangal in partial fulfilment of the requirement for the award of the degree of **Doctor of Philosophy** in Department of Electrical Engineering. To the best of my knowledge, the work incorporated in this thesis has not been submitted elsewhere for the award of any degree.

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DECLARATION

This is to certify that the work presented in the thesis entitled "**Fault-Tolerant BLDC Motor Drive Configurations for Low-Power Electric Vehicle Applications"** is a bonafide work done by me under the supervision of **Dr. V. T. Somasekhar**, Department of Electrical Engineering, National Institute of Technology, Warangal, India and was not submitted elsewhere for the award of any degree.

I declare that this written submission represents my ideas in my own words and where others' ideas or words have been included; I have adequately cited and referenced the original sources. I also declare that I have adhered to all principles of academic honesty and integrity and have not misrepresented or fabricated or falsified any idea/data/fact/source in my submission. I understand that any violation of the above will be a cause for disciplinary action by the institute and can also evoke penal action from the sources which have thus not been properly cited or from whom proper permission has not been taken when needed.

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Patnana Hema Kumar

ABSTRACT

Fault tolerance is a very important aspect of design from the standpoint of reliability for electric vehicles (EVs). Propulsion motors in EVs are typically controlled by voltage source inverters (VSIs). Thus, achieving fault tolerance against faults occurring in switching devices is of paramount interest. Prior research shows that faulty power semi-conductor devices contribute to a significant portion of the total fault conditions in drive configurations. The semi-conductor switch faults are of two types, namely, open-circuit faults (OCF) and short-circuit faults (SCF).

A dual-inverter fed dynamically reconfigurable OEWBLDCM drive is proposed which can provide fault tolerance against a single-switch OCF as well as SCF in power semiconductor switching devices. Diagnosing algorithms for single-switch OC and SC faults are presented. In particular, the handling of SCF is essentially pre-emptive in nature in that detection and subsequent circuit reconfiguration are carried out before the SC fault can cause over-currents in the remaining healthy switching devices and damage them. The SCF is sensed with simple analog circuitry, without compromising on the issues of electrical isolation and bandwidth. A simple method of reconfiguring the power circuit is described in this work, in which the faulty inverter is reconnected to provide a switched neutral point. Further, the post-fault reconnection of the battery ensures that the healthy battery bank that is connected to the faulty inverter is also utilized, which enhances the reliability of the drive. In this drive configuration, it is possible to deliver the rated torque at half of the rated power following the occurrence of either of these two faults. While semiconductors are used to control the power flow into the motor in this drive configuration, the switchgear (two DPDT relays) is used to reconnect the batteries after the occurrence of a fault.

The second contribution of the thesis is another dynamically reconfigurable OEWBLDCM drive topology that can deliver *rated power to the motor even after* the occurrence of either an OCF or an SCF. In this drive configuration, the batteries are reconnected *in series*, unlike the aforementioned power circuit configuration, wherein the batteries are connected in parallel. This configuration uses two more DPDT relays to connect the batteries in series, compared to the previous drive configuration.

The next contribution is the development of an improved drive configuration, which can provide fault tolerance against a single switch OCF or SCF. As in the case of the

configuration described in contribution-2, this topology can deliver the *rated power* to the motor with the *same* number of semiconductors but with a *lower* requirement of supporting switchgear (only two SPDT relays) and sensors. This topology employs 3 bi-directional power devices, which are not exposed to the network in the pre-fault conditions and are therefore not susceptible to failures in the pre-fault conditions. This feature enhances the reliability of this drive configuration.

The previous three drive configurations obtain fault tolerance of a BLDC motor drive only against a single-device fault. Unlike these three, the drive configuration proposed as the fourth contribution can achieve fault tolerance against multiple switch OCF and SCF. It can achieve fault tolerance against all the 15 (i.e. ${}^{6}C_{2}$) combinations of 2-switch OC and SC faults and 20 (i.e. ${}^{6}C_{3}$) combinations of 3-switch faults (except the shoot-through fault). Furthermore, it can even handle the simultaneous as well as the sequential occurrences of OC and SC faults while achieving fault tolerance. This drive configuration can also deliver the *rated power* to the BLDC motor even after the occurrence of *multiple* OC and SC faults. In this fault-tolerant drive configuration, the additional switching resources, which are pivotal to the implementation of fault tolerance are not included in the pre-fault power circuit, enhancing its reliability.

To verify the economic feasibility of the proposed drive configurations, cost-analysis is carried out for the proposed drive configurations. The cost analysis reveals that, compared to the conventional BLDC motor drives, the proposed fault-tolerant systems incur affordable additional raw material costs. All the fault-tolerant circuit topologies proposed in this thesis are first simulated using *MATLAB/SIMULINK* and the results are verified by implementing these schemes on a three-phase, 250 Watt, 48 Volts, and 3200 RPM BLDC motor using *dSPACE1104* as the control platform.

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Abbreviations

ICE	Internal Combustion Engine
IEA	International Energy Agency
EV	Electrical Vehicle
BEV	Battery Electric Vehicle
HEV	Hybrid Electric Vehicle
PHEV	Plug-in Hybrid Electric Vehicle
FCEV	Fuel-Cell Electric Vehicle
DC	Direct Current
IM	Induction Motor
PMM	Permanent Magnet Motor
SRM	Switched Reluctance Motor
PF	Power Factor
PMSM	Permanent Magnet Synchronous Motor
BLDC	Brushless Direct Current
EMF	Electromotive Force
KW	Kilo Watt
HP	Horse Power
IGBT	Insulated Gate Bipolar Transistors
PWM	Pulse Width Modulation
VSI	Voltage Source Inverter
OCF	Open-Circuit Fault
SCF	Short-Circuit Fault
TRIAC	Triode for Alternating Current

OEWBLDCMD	Open-End Winding Brushless DC Motor Drive
MSCMG	Magnetically Suspended Control Moment Gyro
MATLAB	Matrix Laboratory
dSPACE	Digital Signal Processing and Control Engineering
DPDT	Double Pole Double Throw
SPDT	Single Pole Double Throw
NC	Normally Closed Terminal of the Relay
NO	Normally Open Terminal of the Relay
ISO	Isolation Amplifier

List of Symbols

V_{DC}	Input DC link voltage
I_S	Input DC link current
I_{SD}	Input DC link current of dual inverter
i_a	A-phase motor current
i_b	B-phase motor current
i_c	C-phase motor current
e_a	A-phase back EMF
e_b	B-phase back EMF
e_c	C-phase back EMF
B_1	Supply battery input-1
B_2	Supply battery input-2
H_a/ H_b / H_c	Hall-effect position sensors
I_{th}	Threshold value of current
I_{ref}	Reference current
R_f ; D_{sf}	Safety factors for the fault-diagnosis
T_{fault}	Critical-time-period
T_e	Error-time-period
T_{sector}	Time period of one sector
ω_{el}	Electrical angular velocity
ω_{me}	Mechanical angular velocity
f_{el}	Electrical frequency
t_{el}	Period for one electrical cycle
P	Number of poles

S_f	Sensitivity factor
T_{invchk}, T_{drelay}	Delay time periods
v_l	Line voltage matrix
v_{ab} / v_{bc} / v_{ca} / $v_{a'b'}$ / $v_{b'c'}$ / $v_{c'a'}$	Line-Line voltages
$v_{th,sc}$	Threshold value of voltage
v_{ref}	Rated line-line voltage
FDF1/FDF2	Fault-detection-flags
OCFSEC	Sector in which the OC fault first identified
FINV	Flag to identify the faulty inverter
OCFSW1/2/3	Flags to store the OC fault switch number
SCFSEC	Sector in which the SC fault first identified
SCF_l	SC flag matrix
SCFSW	Flag to store the SC fault switch number
ROCFSW1/2/3	Flags to store the reliable OC fault switch number
CNT	Error counter
CNT_{cr}	Critical count value
S	Column matrix denoting sector information
$T_{e,n}$	Error-time-period accumulators dedicated to each sector
$F_{s,n}$	Fault sector flags
F_s	Matrix corresponding to fault sector flags
T_{fc}	Electrical-fault-cycle flag
F_{fs}	First-fault-sector
TR_{fault}	Recheck-critical-time-period
Nzel	Number of zero transisitions in an electrical cycle

N_{zts}	Number of sectors in which OC fault continuously diagnosed
Relay-A/B/C	Relay actuating signals

Chapter 1

Introduction

Chapter 1

Introduction

1.1 Background

Unrestrained consumption of fossil fuels ever since the invention of internal combustion engines (ICEs) resulted in a continuous decay of the environment and destruction of echo systems, questioning the very survivability of humankind. According to a recent IEA (International Energy Agency) survey, the transportation sector holds 20% of the world's energy consumption [ref is needed]. This prompted a paradigm change in the transportation sector, as electric vehicles (EVs) are poised to replace ICEs, which untiringly rotated the wheels of civilization in the past two centuries.

The reasons for choosing EVs over ICEs in the transportation sector are, reduction of greenhouse gas emissions and increased oil prices. Apart from the low emission of greenhouse gases, EVs also offer higher efficiencies and noiseless operation. It is predicted that by the end of the present decade, a major share of road transportation is borne by EVs. The penetration of EVs is further hastened by the recent developments in supportive technologies such as lightweight and high energy density batteries, efficient power semiconductor switching devices, high energy permanent magnets, and high-speed digital control platforms. In general, EVs found applications in various modes of transport such as aircraft, ships, trains & road transport (2-wheeler, 3-wheeler & 4-wheeler). In this thesis, the term EV particularly refers to ground transport vehicles.

EVs employ electric motors as their propulsion units, which are controlled by power electronic inverters. Electric motors used in EVs are expected to possess the qualities of greater torque to weight ratio, high torque at starting and low-speed operation, good dynamic response, good reliability, higher efficiency, easier controllability, robustness, low acoustic noise, and low maintenance requirements. Desirable features of EVs encompass high efficiency, fast battery charging, high acceleration, autonomy, environment friendliness, and safety.

EVs are divided into four major categories based on their architecture as shown in Fig. 1.1).

i) **Battery Electric Vehicles (BEVs):** BEVs are also referred to as All-Electric Vehicles (AEVs). These EVs run entirely on electric drives powered by batteries. These batteries are charged externally by plugging into the electric grid.

ii) **Hybrid Electric Vehicles (HEVs):** HEVs use both Internal Combustion (IC) engines and battery-powered electric drives. The IC engine is used for both driving and battery charging purposes. The transmission system which drives the wheels is driven simultaneously by both the IC engines and electric motors

iii) **Plug-in Hybrid Electric Vehicles (PHEVs):** PHEVs use both IC engines and battery-powered electric drives. The batteries can derive charge externally using a plug socket.

iv) **Fuel-Cell Electric Vehicles (FCEVs):** FCEVS are also referred to as zero-emission vehicles. They employ 'fuel-cell technology', which converts chemical energy into electric energy required to power the vehicle.

Of all these types of EVs, BEVs are the most efficient. The efficiency of PHEVs lies in between the BEVs and HEVs.

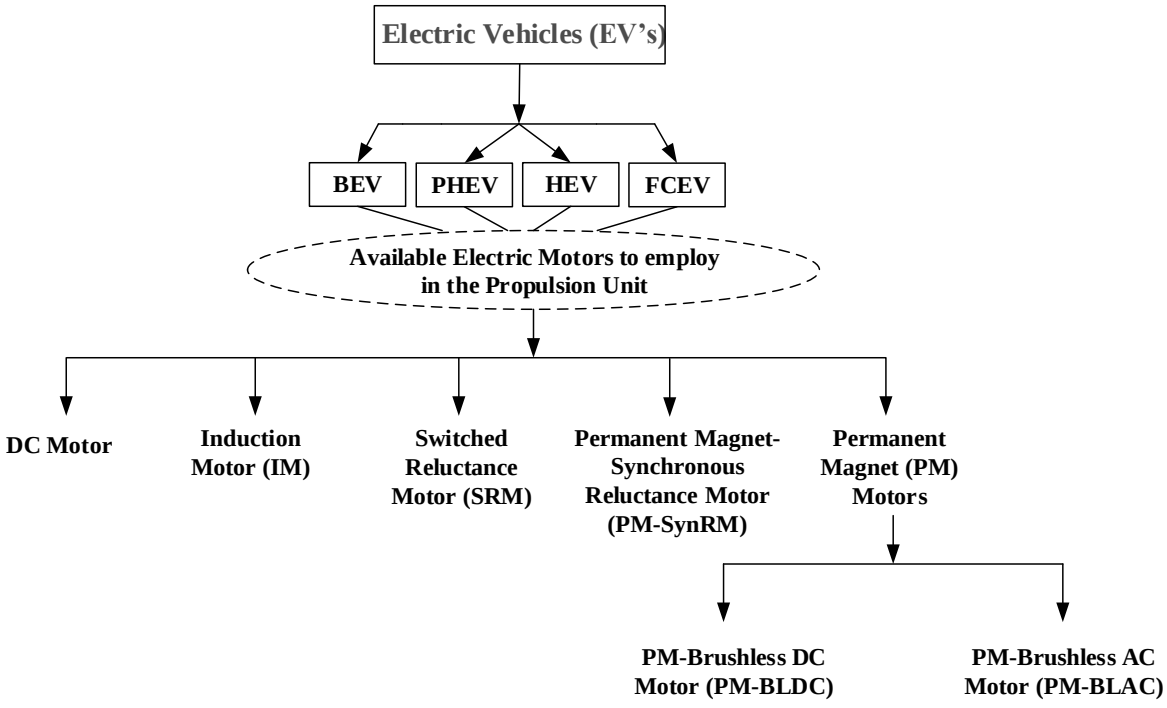


Fig. 1.1: List of available Electric motors to employ in the propulsion unit of EV applications

As mentioned earlier, EVs derive their tractive power from electric motors. These motors could be of the following type; (i) Brushed DC Motors (ii) Induction Motor (IM) (iii) Switched Reluctance Motors (SRM), (iv) Permanent Magnet- Synchronous Reluctance Motor (PM-SynRM) and (v) Permanent Magnet Motors (PMMs). Of these, the traditional DC motors, owing to their well-known inherent weaknesses, have become obsolete and are not being considered in contemporary designs.

Induction Motors offer the advantages of lower maintenance, robustness, and lower costs. However, they are plagued with weaknesses such as lower torque, higher starting currents, and vibrations at starting conditions, moderate efficiencies, and moderate speeds. Switched Reluctance Motors display the features of simple construction and the consequent ruggedness, requiring lower maintenance. They are also capable of running at higher speeds. Despite these advantages, they could not penetrate the field of EVs owing to their drawbacks such as lower P.F operation, lower dynamic response, and higher acoustic noise.

The Permanent Magnet Synchronous Reluctance Motor (PM-SynRM) offers the features of higher operating efficiency and PF. However, the stack length of the PM-SynRM is more compared to PMMs for the same power rating.

The shortcomings of the aforementioned motors forced designers around the globe to consider Permanent Magnet Motors (PMMs) for EV applications. PMMs are capable of displaying the features of better dynamic response, higher efficiency, greater operating speeds, higher PFs, higher torque to weight ratios, lower maintenance, and lower acoustic noise.

In the category of PMMs, two principal variants exist namely, Permanent Magnet Synchronous Motors (PMSMs) and the Brushless Direct Current (BLDC) Motors. BLDC motors offer advantages such as higher power density (by about 15%), lower switching and conduction losses, enhanced thermal reliability, simpler control, and the use of inexpensive sensors compared to PMSMs [1-11].

Fig. 1.2 shows BLDC motor drives, which are employed in various low-power EV applications. Fig. 1.2a shows a foldable electric wheelchair application, which employs a 24 V, 250W BLDC motor [74]. An electric bicycle is shown in Fig.1.2b, which is designed with a 36 V, 250W BLDC motor [75]. A 3-seater application is shown in Fig. 1.2c that uses a 48 V, 2 HP BLDC motor [76]. A 48 Volt, 4 KW BLDC motor-based electric ambulance car is

shown in Fig. 1.2d [77]. Furthermore, BLDC motors can find applications in EVs with higher power ratings also as indicated in [10], [11] & [78].

Fig. 1.2: BLDC motor in various low-power EV applications: (a) Electric Wheelchair [74] (b) Electric Cycle [75] (c) Mahindra Treo 3-seater/HRT/SFT [76] (d) Electric Ambulance Car [77]

Fig. 1.3 shows the basic 3-phase 2-level VSI fed BLDC motor drive configuration. The VSI consists of six power semiconductor switching devices, which achieve electronic commutation for the BLDC motor. These switches also control the phase voltage applied to the motor with suitable modulation techniques, paving the way to the speed control of the motor. The gating signals for the inverters are determined by the position of the rotor, which is sensed by three Hall-effect sensor signals (H_a, H_b & H_c). Based on the information available from the three Hall-effect sensor signals, the electrical cycle is divided into six sectors of operation (Sector-1 to Sector-6). The back EMFs developed in the motor phases and the corresponding gating signals of dual-inverter configuration are shown in Fig. 1.4. The speed of the motor can also be estimated by calculating the time taken for each sector of operation. The speed of the motor can be controlled by varying the phase voltage appearing across the

motor terminals. The phase voltage can be varied by controlling the gate signal of the VSI switches using pulse width modulation (PWM) techniques.

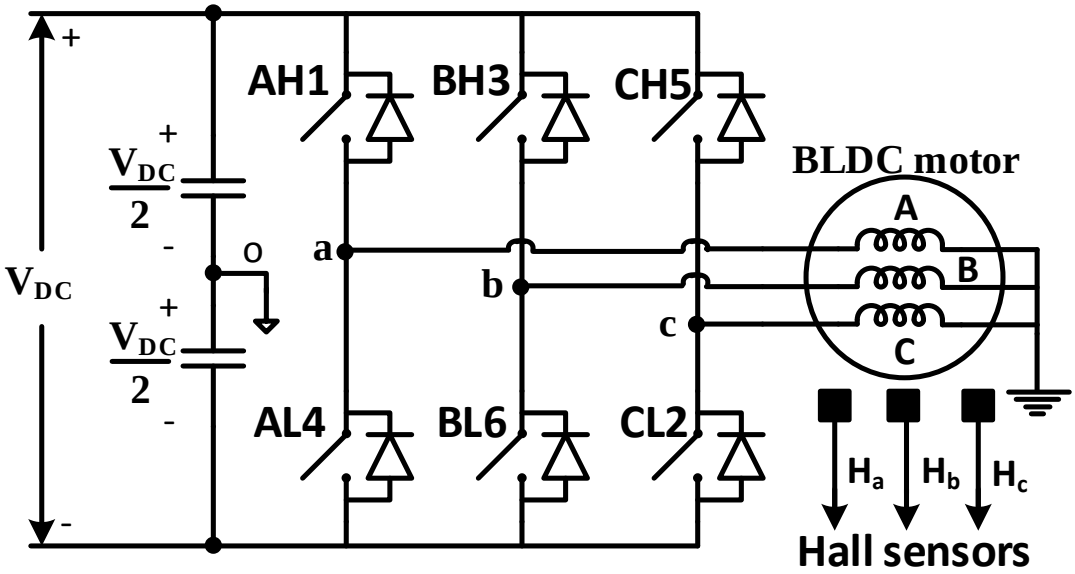
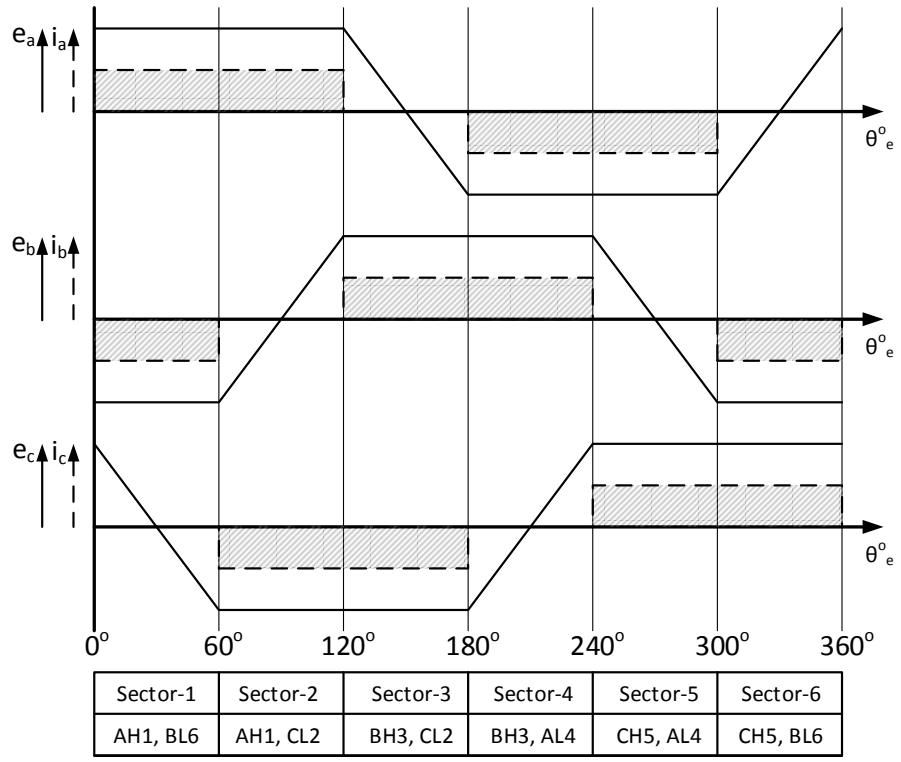


Fig. 1.3: Conventional 3-Phase, 2-Level VSI fed BLDC Motor Drive Configuration



Sector-1	Sector-2	Sector-3	Sector-4	Sector-5	Sector-6
AH1, BL6	AH1, CL2	BH3, CL2	BH3, AL4	CH5, AL4	CH5, BL6

Fig. 1.4: Back EMF and motor phase current waveforms with switching logic for the conventional BLDC motor drive topology

The reliability of the power supply to the propulsion motor drive configuration is a crucial factor in EVs. In general, electric drives could fail due to faults occurring either in their motors or in their power electronic controllers. Faults that generally occur in motors include the defects developed in their stator windings, bearings, and rotor. Power converter faults generally comprise the defects developed in their power semiconductor switching devices, gate drive circuits, sensors, and controllers [12-23]. According to the Electronic Power Research Institute (EPRI) survey [13]-[14], the stator winding faults are estimated as 36% of total motor faults, which include phase-to-ground faults, phase-to-phase faults, open-coil faults or inter-turn short-circuit faults. Bearing faults are about 41% of motor faults, which occur because of improper maintenance, fast switching occurrence in PWM techniques, etc. Rotor faults are about 9% of motor faults that occur because of aging effect/manufacturing defects, frequent starting operations, thermal and mechanical stress, etc.

A survey on the possibility of the faults in the variable speed drives in the industry is given in [15]-[18]. From this survey it is observed that 38% of drive failures are attributed to the faults in power switches, 53% of failures are related to the control circuits and 7.7% are in the external auxiliaries.

Power semiconductor switching devices fail either due to open-circuit (OC) faults (OCF) or short-circuit (SC) faults (SCFs). OC faults in power devices cause pulsating currents, which lead to pulsating torques. OC faults also lead to the reduction of the average torque produced by the motor and result in unbalanced stresses amongst the switching devices of the VSI. Even though OC faults do not require immediate intervention, they often result in secondary faults in the VSI, motor, and load if they are allowed to persist for longer periods. In contrast, SCFs need immediate attention and shut down as they cause large fault currents [19]–[23].

Thus, it is very important to ensure the reliability of electric drives used in EV applications despite failures in power semiconductor switching devices. To this end, it is needed to conceive fault-tolerant drive configurations, and diagnosing algorithms to detect the OC and SC faults.

1.2 Literature Review

The problem of enhancing the reliability of EVs by addressing the issue of fault tolerance has attracted the attention of researchers around the globe and consequently, considerable research has been carried out in the areas of fault-tolerant power converter topologies, diagnosis of OC and SC faults, and post-fault configuration of power converters.

Fig. 1.5 represents the block diagram representation of prior art literature corresponding to the fault-diagnosis and fault-tolerant operations of the IM, PMSM & BLDC drive configurations.

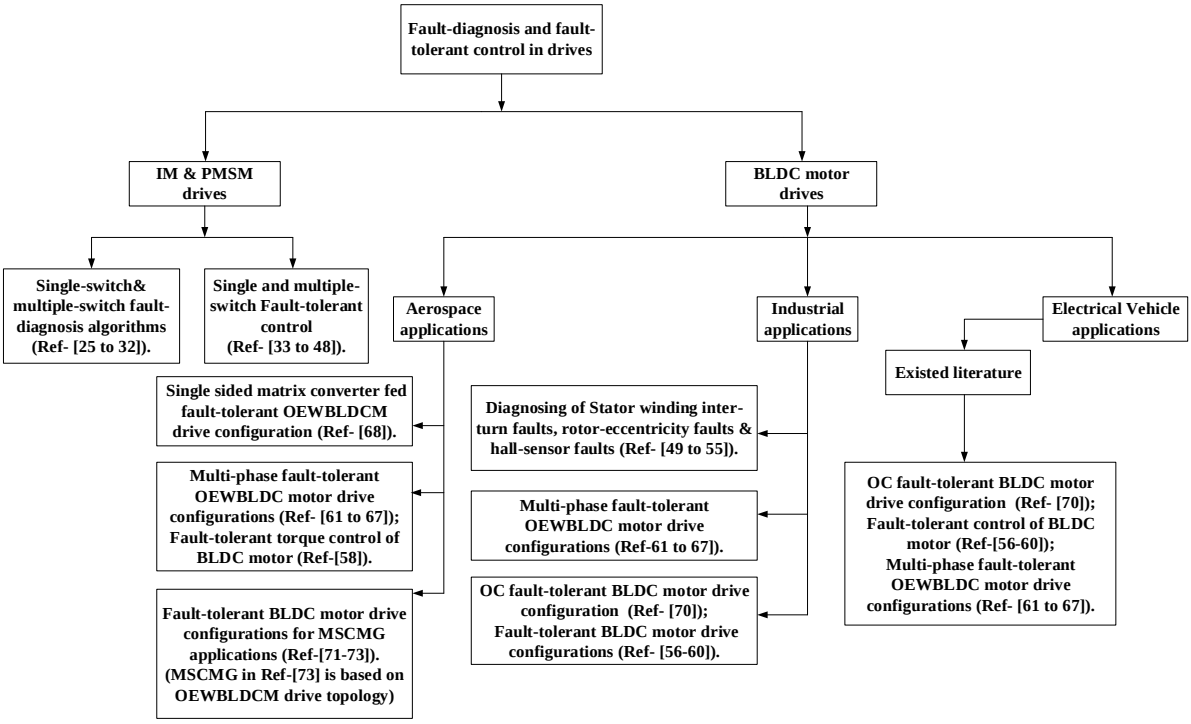


Fig. 1.5: Block diagram representation of fault-diagnosis & fault-tolerant drive configurations existed in the prior art literature

The research work reported in [24] describes the diagnosis of the OC/SC faults occurring in the switching devices of the VSI based on the behaviour of the gate-to-emitter voltages of IGBTs within 3μs. However, this method applies only to IGBT-based converters and requires auxiliary inductors and gate-to-emitter voltage measurement circuitry for the fault-diagnosis.

Two methods for single-switch OC fault detection are described in [25]. The first method is based on the analysis of the current vector trajectory and the second one is based on the determination of the instantaneous frequency of the current vector. In the work

presented in [26], single-switch fault detection and diagnosis of switching devices are carried out, using the Concordia frame of reference. However, this approach involves complex computations and pattern recognition algorithms. It is shown in [27] that, by using the Park's vector corresponding to the average stator current, the single-switch OC and SC faults in the power switching devices can be identified.

In the research work reported in [28], an algorithm is presented to diagnose the multiple OC faults in the switches of the VSI based on the normalized average motor phase currents. A multiple-switch OC fault-diagnosis algorithm for the VSI fed PWM operated motor drives, which is based on the errors in reference currents is presented in the research work reported in [29]. In the work [30], a multiple-switch OC fault-diagnosis algorithm is presented for a closed-loop vector-controlled VSI-fed motor drive. A model-based fault-diagnosis and fault-isolation procedure for multiple-switch OC fault conditions in the IM drives is presented in the research work [31]. Based on the park's vector information of the motor phase currents, a real-time multiple-switch fault-diagnosis and isolation procedure for the VSI fed drive configuration is presented in the work [32].

Parallel redundancy, conservative design techniques and multiphase PWM drive configurations have been proposed to improve the fault tolerance. The trade-off lies in the increased system cost and size of such systems [33]-[35]. In general, the provision of redundancy increases the costs of electric drives. Intelligent fault mitigation control methods, along with appropriate hardware modifications to the conventional three-phase adjustable-speed PWM drives, were also reported to minimize cost [36-39]. To explore the possibility of cost reduction further, various reduced switch-count converter topologies for three-phase AC motor-drive systems have been developed [40]-[41]. A survey on fault tolerance techniques for three-phase voltage source inverters is presented in [42]-[43].

The analyses of the pre-fault and post-fault operations for multilevel open-end winding IM drive topologies, which are capable of handling both OC fault and SC fault, are presented in the works [44]-[47]. However, the method of diagnosing the OC & SC faults is not presented in these works [44]-[47]. With the fault-tolerant topologies mentioned in [44]-[47], the DC-source (battery in the context of EVs) present on the faulty inverter is unused, causing a reduction in the on-road endurance of the drive after the occurrence of the fault. The work reported in [48] presents the OCF diagnosis algorithm for a multi-level dual-inverter fed open-end winding IM drive.

Despite the availability of a rich repertoire of fault-diagnosis methods and post-fault drive configuration strategies in the area of induction motor drives, they do not apply to BLDC motor drives, due to the discontinuous current and trapezoidal back EMF of the BLDC motors. However, this literature forms the basis to develop fault-diagnosis and reconfiguration strategies for BLDC drives.

The fault-tolerant control for the rotor-eccentricity faults in PM-BLDC motors has been suggested in the works [49]-[50]. The stator winding inter-turn fault-diagnosis of PM-BLDC motor drive, based on the strategy of model current control, has been presented in the works [51]-[52]. In the research works reported in [53-55], fault-tolerant operations have been proposed for BLDC motor drives for the faulty condition in any one of the Hall-Effect sensors.

The research work presented in [56] describes failure diagnostics and the corresponding remedial control strategies for BLDC motor drives. For OC failures, a technique to maintain the rated output torque for a permanent magnet hybrid BLDC motor drive configuration, using field-reconstruction strategies and boosting of filed-excitation, is investigated in [57]. Fault-tolerant torque control for a BLDC motor that can facilitate a precise torque control with a reduced power dissipation despite the failure of one of its phase winding is described in [58].

Fast-changing and soft commutation between the main, and redundant branches of a VSI using a combination of rugged mechanical commutators and semiconductors are reported in [59]. The fault-tolerant analysis described in [59] reveals that even though mechanical commutators are slow compared to power semiconductor switches, they provide the advantages of low losses, electrical isolation, and stress elimination for the parallel redundant branches.

In the research work presented in [60], a single-switch OC (or) SC fault-tolerant drive topology for EV applications is described, which uses six TRIACs and one actuator leg additionally. However, fault-diagnosis algorithms were not described in this literature.

The literature [61-67] presents open switch/phase fault-tolerant control strategies for multi-phase Open-End Winding Brushless DC (OEWBLDC) Motor Drives. These drives could be useful in applications such as EVs, military, manufacturing firms & aerospace applications.

The work reported in [61] shows that the motor would be able to operate with reduced torque and increased torque ripple despite the open-circuit fault either in the switching devices of the converter or the motor phase windings. The research work presented in [62-64] also discusses various fault-tolerant control strategies and compensation methods for controlling the torque ripple during the open-switch/phase fault conditions. Also, the work presented in [64] describes the fault-diagnosis procedure for the OC fault in a multi-phase BLDC drive. This work emphasizes the advantage of employing the open-end winding topology of the motor from the standpoint of fault tolerance.

A fault-tolerant OEWBLDC Motor Drive (OEWBLDCMD) with a multiphase single-sided matrix converter has been proposed in work [68], which is capable of handling open-circuited faults in the phase windings of the motor. However, in this work [68], the pertinent fault-diagnosis algorithms are not provided. In the work [69], an OC/SC fault-diagnosis algorithm based on pattern recognition of line-line voltages using discrete Fourier transform analysis for the in-wheel brushless DC motor used in EV applications is proposed.

A fault-tolerant BLDC motor drive is reported in [70], in which the faulty phase is connected to the midpoint of the dc-link using a bidirectional switch (shown in Fig. 1.6). However, fault detection is only limited to the OC fault-diagnosis. The fault-tolerant BLDC drive topology presented in [70] requires six additional fuses for achieving SC fault tolerance.

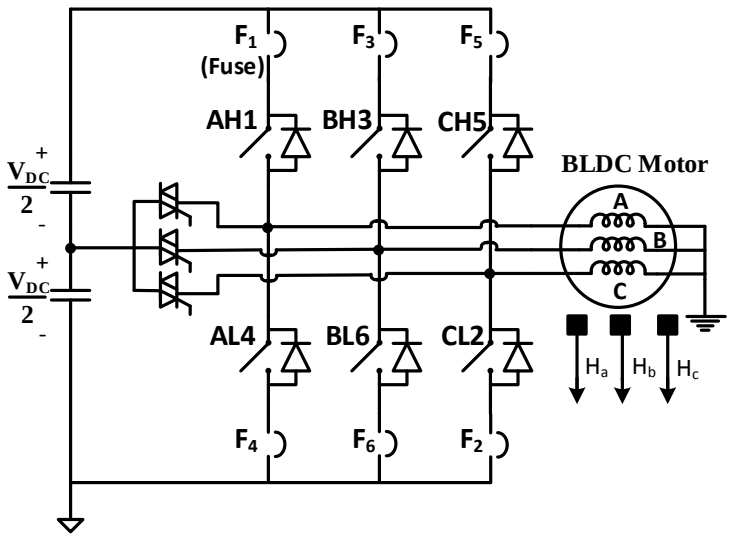


Fig. 1.6: Fault-tolerant BLDC motor drive topology proposed in Reference-[70]

Fault-tolerant control moment gyros (CMGs), which are used in attitude control of space stations, are described in [71]–[73]. Buck converter fed inverter drive control is used for magnetically suspended CMG (MSCMG). OCF and SCF diagnosis for MSCMG was discussed in [71]. The scope of this work [71], however, is limited to the diagnosis of the fault.

The work reported in [72] achieves fault tolerance against both the OC fault and the SC fault occurring in the buck converter as well as the inverter switches (shown in Fig. 1.7). A fault-diagnosis algorithm has been described in this work, which is capable of detecting a single switch OC/SC fault in the overall power circuit. In this drive, the fault-tolerant operation is obtained by the placement of triacs in series and parallel to the converter leg. However, these triacs are constrained to conduct even during the normal (i.e. fault-free) operating conditions, making them vulnerable to the development of additional faults. The fault-diagnosis algorithm presented in [72] doesn't address the faults developed in these additional triacs.

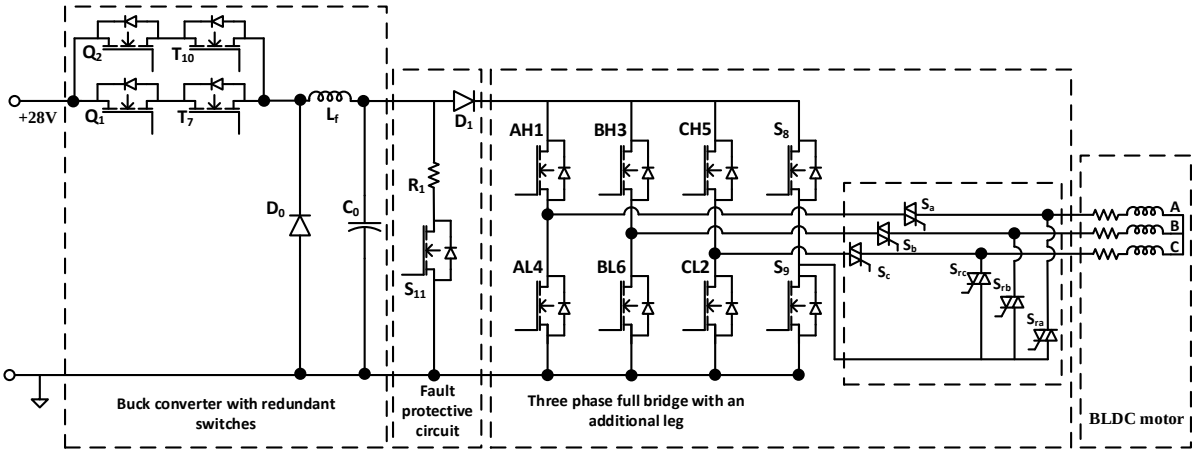


Fig. 1.7: Fault-tolerant BLDC motor drive configuration for MSMCG applications proposed in Reference-[72]

A dual-inverter fed OEWBLDCMD is proposed in [73], which is aimed for the MSCMG applications (shown in Fig. 1.8). In this topology, a front-end dc‑dc buck converter provides a ripple-free dc input to the dual-inverter fed OEWBLDCMD. As in [73], the output voltage of the dc-dc converter is varied to control torque of the BLDC motor. In other words, the dual-inverter configuration reported in [73] is not modulated and is operated in the conventional six-step commutation mode. The diagnosis algorithm described in this paper is capable of detecting an OC/SC fault in any one of the twelve semiconductor switching devices present in the drive. However, the motor in this scheme is constrained to handle twice its rated

current in four modes of operation (out of six modes) after diagnosing the fault. This calls for the oversizing of the motor.

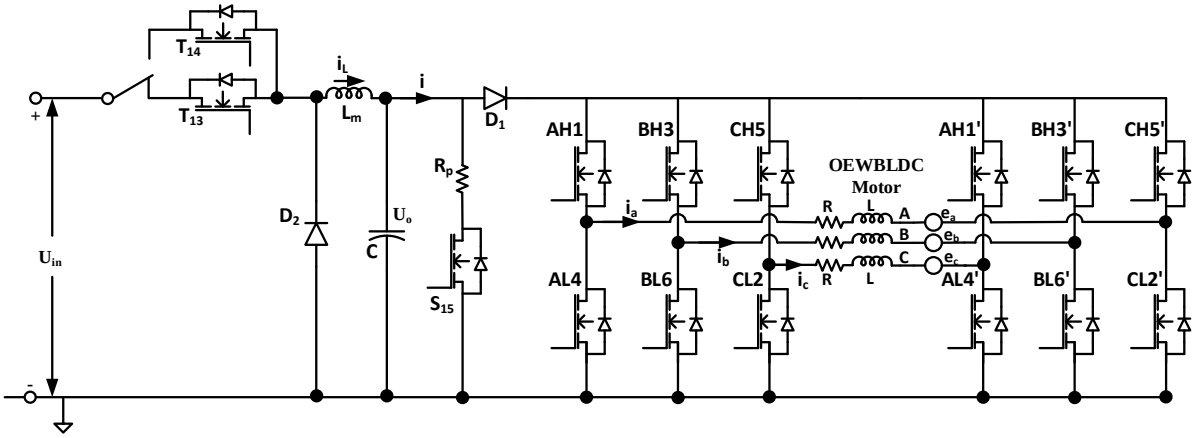


Fig. 1.8: Fault-tolerant OEWBLDC motor drive configuration for MSMCG applications proposed in Reference-[73]

Furthermore, the fault-diagnosis schemes in [71]-[73] are applicable only for the MSCMG drive operated by a buck converter fed inverter, as the fault-diagnosis is based on the sensing of the output voltage and the dc-link current of the buck converter. Hence, this method cannot be applied to the conventional inverter fed BLDC motor drives.

1.3 Motivation

The following observations are made on the fault-tolerant BLDC Motor Drive configurations from the literature review:

i) BLDC motors are promising for EV applications due to features of having (i) higher torque-to-volume ratio; (ii) higher efficiency; (iii) ease of control; and (iv) better dynamic response.

ii) A considerable portion of the total faults developed in motor drives are due to the failure of power semiconductor switches. Hence, researchers are attracted to design fault-tolerant topologies against the failure of power semiconductor switching devices. Designing fault-tolerant drive configurations help in enhancing the reliability, safety, and robustness of the EV.

iii) Literature survey suggests the possibility of designing dynamically reconfigurable fault-tolerant drive configurations with interesting possibilities in terms of utilizing

the battery effectively while delivering rated power (complete fault tolerance) to the load even under faulty conditions.

iv) For BLDC motors, it is worth investigating if pre-emptive fault-diagnosis and circuit reconfiguration strategies can be devised when power semiconductor switching devices develop short-circuit faults. If it is manageable, it avoids the flow of SC fault currents through the faulty switching devices.

v) Literature on the fault-tolerant operation of multiple-switch OC/SC fault conditions for BLDC motor drives is scanty. This gap was addressed in this research work.

vi) Complete fault tolerance demands additional switching resources and sensors. It could be beneficial to explore the possibilities of reducing additional components.

vii) Vulnerability issues pertaining to the power steering components (which are often semiconductors) should be addressed in fault-tolerant drives. It could be worth exploring if rugged electromechanical devices (such as relays) can replace power semiconductors for steering power.

viii) In the scenario of ever-decreasing costs of semiconductors, it is interesting to evaluate, as to what extent the cost incurred due to the employment of additional switching resources are offset by the reduced number of sensors, which are relatively more expensive.

1.4 Thesis Objectives

Following the motivation described earlier, the focus of this research work is to design fault-tolerant BLDC motor drive configurations used in EV applications. The objectives of the research work are as follows:

i) Development of fault-tolerant topologies, which can withstand a single-switch OC/SC fault condition in the power converter using a reduced number of additional components.

ii) Development of diagnostic algorithms to detect OC/SC fault conditions in the switching devices of the power converter.

iii) Development of low-cost sensors, which are required to diagnose the switch faults.

iv) Development of operational procedures for the dynamic circuit reconfiguration to achieve effective utilization of DC sources and reliable and continuous post-fault operation.

v) Development of a multiple-switch fault-tolerant topology that can withstand multiple-switch OC/SC fault conditions in the power converter with a reduced number of additional components.

vi) Reduction of the additional raw material cost (RMC) of a fault-tolerant BLDC motor drive to suit EV applications.

1.5 Organization of the Thesis

The organization of the thesis work on fault-tolerant BLDC motor drive configurations for low-power electric vehicle applications is made into overall six chapters and each chapter's brief outlook is provided below:

Chapter 1 gives the background and literature survey on the existing fault-tolerant drive configurations and their merits and demerits. The motivation for the problem formulation, objectives and thesis structure are also presented in this chapter.

Chapter 2 presents a dynamically reconfigurable open-end winding brush-less DC motor (OEWBLDCM) drive topology which is capable of handling single-switch OC/SC faulty conditions. The pre-fault and post-fault circuit reconfiguration strategies for the fault-tolerant drive operation is illustrated. The algorithms corresponding to the diagnosis of single-switch OC as well as SC faulty conditions are discussed. The pre-emptive nature of SC fault-diagnosis, which can avoid over currents in healthy switching devices is illustrated. The design of cost-effective analog-based voltage sensors for diagnosing SC fault is presented. The effectiveness of the proposed power circuit, fault-diagnosis algorithms, and reconfiguration strategies are assessed with simulation studies and is validated experimentally. The features of the proposed fault-tolerant drive topology are compared with the previously reported topologies in literature. A cost analysis is carried out to determine the additional raw material cost (RMC) required for imparting the feature of fault tolerance compared to the conventional BLDC motor drive configuration.

Chapter 3 presents a dynamically reconfigurable single-switch OC/SC fault-tolerant OEWBLDCM drive topology that can deliver rated (i.e., 100%) post-fault output power. The dynamic circuit reconfiguration and battery reconnection procedure for the fault tolerance feature are explained. Simulation studies and experimental verification are carried out to validate the fault-tolerant feature of the proposed drive configuration. Cost-analysis is carried out to determine the economic feasibility of the proposed drive configuration.

Chapter 4 presents a single-switch OC/SC fault-tolerant BLDC motor drive topology for low-power EV applications. This power converter uses 3 bi-directional power devices, which are inactive in the normal mode of operation, enhancing its reliability. The proposed fault-tolerant BLDC motor drive requires fewer additional components and sensors compared to the fault-tolerant power converters, which are reported in chapters 2 and 3. The proposed drive configuration can deliver the rated power in the post-fault conditions (i.e., single-switch OC/SC fault conditions) similar to the topology presented in chapter 3. Experimental results are presented for validating the fault-tolerant feature of the proposed drive configuration. The economic feasibility of the proposed drive configuration is verified using cost analysis.

Chapter 5 presents a multi-switch fault-tolerant and auto-reconfigurable BLDC motor drive configuration, suitable for EV applications, owing to its enhanced reliability. The proposed power circuit configuration, along with its fault diagnostic algorithm, is capable of achieving fault tolerance against multiple OC and SC faults. The proposed drive configuration is capable of delivering rated power to the BLDC motor even after the development of several faults in the power semiconductor switching devices. Simulation and experimental studies validate the concept of the proposed drive topologies. This chapter also presents an analysis that assesses the cost-effectiveness of the proposed drive configuration.

Finally, **Chapter 6** gives a summary of key achievements illustrated in the thesis along with the scope for future research.

All the fault-tolerant circuit topologies proposed in this thesis are first simulated using MATLAB/SIMULINK and the results are verified by implementing these schemes on a three-phase, 250 Watt, 48 Volts, and 3200 RPM BLDC motor using dSPACE1104 as the control platform.

1.6 Summary

This chapter presents an introduction to the research work undertaken in this doctoral thesis. The motivation and objectives are spelled out after the introduction of pertinent literature available on this topic, which includes various fault-tolerant drive configurations. Finally, this chapter presents the organization of this thesis.

Chapter 2

An Open-End Winding BLDC Motor Drive with Fault-diagnosis and Auto-Reconfiguration

Chapter 2

An Open-End Winding BLDC Motor Drive with Fault-diagnosis and Auto-Reconfiguration

2.1 Introduction

As stated in Chapter-1, power semiconductor switches account for about 38% of the total faults developed in the motor drives [15-18]. This is the impetus for the development of auto-reconfigurable fault-tolerant topologies, which can withstand OC/SC fault conditions in any of the power semiconductor switching devices. This would help in enhancing the reliability, robustness & safety of the BLDC motor drives used in Electric Vehicle (EV) applications.

Literature survey reveals that, in the research works reported in [44-48], the pre-fault and post-fault operations of multilevel open-end winding IM drive topologies that are capable of handling both OC and SC faults are presented.

The power circuit configurations reported in [61-67] present multi-phase open-end winding-based fault-tolerant BLDC motor (OEWBLDCM) drive configurations that can withstand OC faults in switch as well as motor phase windings.

A fault-tolerant OEWBLDC Motor Drive (OEWBLDCMD) with a multiphase single-sided matrix converter has been proposed in work [68], which is capable of handling open-circuited faults in the phase windings of the motor. However, in this work [68], the pertinent fault-diagnosis algorithms are not provided.

A dual-inverter fed OEWBLDCM drive for MSC moment gyro applications has been proposed in [73], which can achieve fault tolerance to a single switch OC/SC fault. However, this fault-tolerant scheme presented in [73] requires that the motor phases carry double the rated current following either of these faults.

These works exploit the inherent advantage associated with the open-end winding configuration of the motor from the standpoint of fault tolerance.

Motivated by the aforementioned literature, an improved fault-tolerant Open-end Winding BLDC (OEWBLDC) Motor Drive configuration for EV applications is presented in this chapter. This OEWBLDC motor drive is powered by two battery banks of equal voltage and power rating from either side of the open-ended stator windings. This drive is capable of exhibiting tolerance against both OC and SC faults in any one of the twelve switching devices of the dual-inverter system.

This chapter also proposes new algorithms for OC and SC fault-diagnosis for all of the switching devices of the OEWBLDC motor drive. In particular, the SC fault is identified by sensing the line voltages before a short-circuited semiconductor device causes overcurrent through the device. To make the fault-diagnosis cost-effective and practicable, inexpensive and readily available current sensors and analog isolators are employed, without compromising on bandwidth.

Upon the identification of fault, the power circuit is automatically reconfigured to supply reduced power to the motor, enhancing the reliability of the drive. With the help of appropriate switchgear, one can reconnect the battery of the faulted inverter side in parallel to the battery of the operating inverter.

To assess the effectiveness of the proposed algorithms for OC and SC fault-diagnosis, the OEWBLDC motor drive is operated in both open-loop as well as in closed-loop. It is shown that the drive is capable of delivering full load torque, even when OC and SC faults occur, making it suitable for electric vehicle applications. Furthermore, the topology presented also results in lesser (dv/dt) stress across the switching devices, enhancing the longevity of the drive compared to the conventional BLDC drive.

The effectiveness of the proposed power circuit, fault-diagnosis algorithms, and reconfiguration strategies is assessed with simulation studies, which are validated experimentally.

2.2 The Open-End Winding Brush-Less Dc Motor Drives

Figure 2.1 shows the circuit diagram of the fault-tolerant Open-End Winding Brush-Less DC (OEWBLDC) Motor Drive configuration. A dual-inverter system consisting of Inverter-1 (INV-1 for short) and Inverter-2 (INV-2). These inverters derive their DC inputs from two electrically isolated battery banks ('B_1' & 'B_2') through two DPDT relays. The nomenclature of various components and terminals of the power circuit are as follows: terminals of motor phase windings (A), (B) & (C) are: (a, a'), (b, b') & (c ,c'); positive terminals of respective DC-links of inverters: P_1 (for INV-1) & P_2 (for INV-2)); negative terminals of respective DC links of inverters: N_1 (for INV-1) & N_2 (for INV-2)); three legs of (INV-1) and (INV-2) are: (LEG-A, LEG-B & LEG-C) and (LEG-A', LEG-B' & LEG-C'); midpoint of inverter legs: u (for LEG-A), v (for LEG-B), w (for LEG-C), u' (for LEG-A'), v' (for LEG-B') & w (for LEG-C); INV location of switching devices: upper banks of inverters (H); lower banks of inverters (L); power switch identification numbers for INV-1: (1-6); for INV-2: (1'-6') ; positive and negative terminals of the DC source B_1: S_1 & S_2; B_2: S_3 & S_4. For example, the switch CH5' pertains to the switching device present in the C-phase of the upper bank of the Inverter-2, which bears the number 5 (see Fig. 2.1).

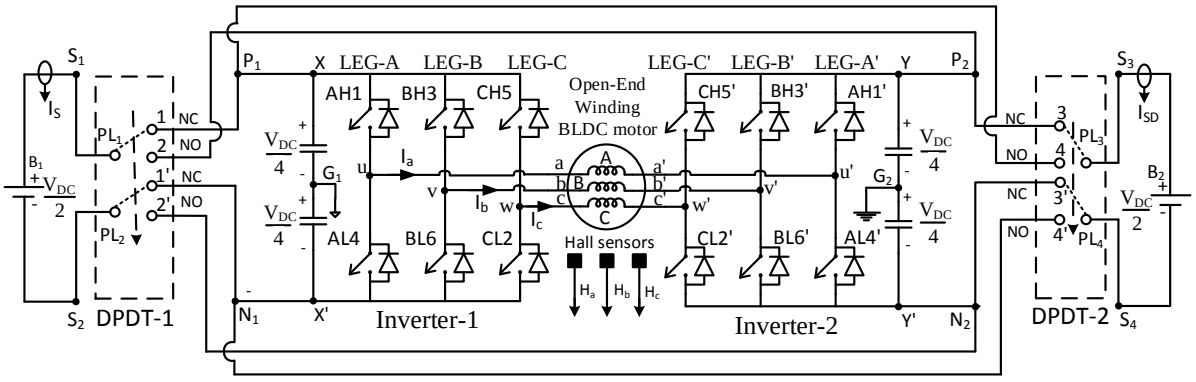
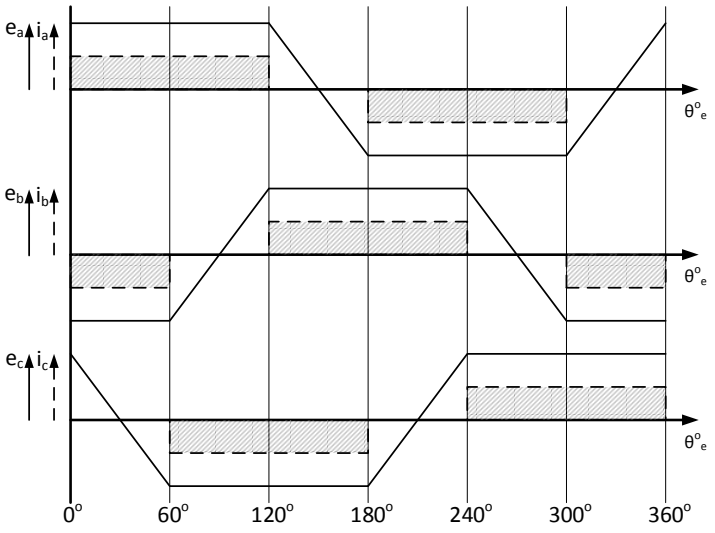


Fig. 2.1: Circuit Configuration of OEWBLDC Motor Drive

The discussion on the role of the DPDT relays is deferred to section-2.3. The batteries, by default, are connected to the Normally Closed (NC) terminals (11' for INV-1 and 33' for INV-2). Fig. 2.2 presents the Back-EMF waveforms across the phase windings of the OEWBLDCMD, the operating sectors, and the switching regimes of the power switching devices of the dual-inverter system. Similar to the conventional Brushless DC Motor drive, there exist six sectors of operation (represented as Sector-1 to Sector-6). Also, the devices to be switched are identified by the three Hall-Effect position sensors, namely H_a, H_b & H_C as shown in Fig. 2.1.



Mode	Sector-1	Sector-2	Sector-3	Sector-4	Sector-5	Sector-6
INV1	AH1, BL6	AH1, CL2	BH3, CL2	BH3, AL4	CH5, AL4	CH5, BL6
INV2	AL4', BH3'	AL4', CH5'	BL6', CH5'	BL6', AH1'	CL2', AH1'	CL2', BH3'

Fig. 2.2: Back EMF and Motor phase current waveforms with switching logic

The equivalent circuit diagrams for Sector-1 and Sector-2 are shown in Fig. 2.3a and Fig. 2.3b respectively. From Fig. 2.3a it may be noted that the conducting phase windings are **aa'** and **bb'** while the phase **cc'** is left floating. The winding bb' provides the return path for the current flowing through **aa'** (and vice-versa). Furthermore, if the top switch of INV-1 for a given phase winding is turned on (AH1 in this case), the bottom switch of INV-2 is also turned on (AL4' in this case).

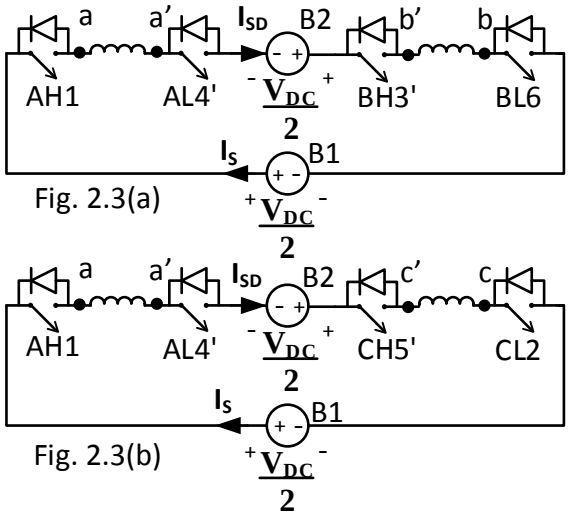


Fig. 2.3: Electrical equivalent of the fault-tolerant OEWBLDCM drive: (a) Sector-1 operation, (b) Sector-2 operation

2.3 The necessity of Additional Switchgear

After the diagnosis of either an OC or an SC fault, the following strategies should be followed to render the capability of fault tolerance to the drive. It is also important to redeploy the healthy battery connected to the faulty inverter to enhance the utilization of the battery and the reliability of the drive.

2.3.1 Reconfiguration of the Circuit for OC/SC Fault

The reconfiguration of the circuit is achieved by creating a switched neutral point by gating either all of the switching devices connected to the positive or negative DC rail, depending upon the type of fault developed in the faulty inverter.

For example, if an OC fault is developed in any one of the three switches connected to the positive DC rail of INV-1, say AH1, then all of the switching devices of INV-1, which are connected to the negative DC rail (AL4, BL6, and CL2) are simultaneously gated to create a switched neutral point on the negative DC rail of that inverter. The other two healthy switches, namely BH3 and CH5 are never gated to avoid shoot-through faults in the 'B' and 'C' phase legs of INV-1. A similar reconfiguration strategy is adopted for the other switching devices as well.

On the other hand, if an SC fault occurs in AH1, then the other two healthy devices connected to the positive DC rail of INV-1 (BH3 and CH5) are continuously gated, so that, the switched neutral point is created, this time on the positive DC rail of INV-1. In this case, the switching devices AL4, BL6, and CL2 are never gated to avoid the occurrence of the shoot-through fault.

2.3.2 Reconnection of the Healthy Battery Bank using DPDT Relays

It is obvious that with the aforementioned maneuvers, the faulty inverter is isolated and the OEWBLDC motor is operated as a conventional BLDC motor with only one battery bank with half of the rated voltage. However, this move deprives the service of the healthy battery bank (connected to the faulty inverter) to the resulting system.

Thus, to salvage this situation, there is a necessity to connect the healthy battery bank in parallel to the existing battery bank associated with the healthy inverter. The employment

of the two DPDT relays, shown in Fig. 2.1, would accomplish this task. Under normal conditions, the battery is connected to 'Normally Closed' (NC) terminals (11' for INV-1 and 33' for INV-2), thereby INV-1 and INV-2 derive their DC inputs from batteries 'B_1' and 'B_2'. When a fault (either OC fault or SC fault) is detected and the faulty inverter is identified and reconfigured, the battery bank of the faulted inverter is connected in parallel to its counterpart through the 'Normally Open' (NO) terminals (22' of INV-1 and 44' of INV-2).

Detailed strategies for triggering these relays after diagnosing OC and SC faults are described in sections-2.4 and 2.5 respectively. The method of energizing the relay coils is described in section-2.6.

2.4 Fault-Diagnosis and Control for Open-Circuit Fault

This chapter proposes a method to extend the strategy described in [70] for the identification of the Open-Circuit Fault (OCF) for the Open-end Winding Brushless DC (OEWBLDC) motor drive. The procedure is described in the following paragraphs:

The OC fault-diagnosis algorithm always (i.e. by default) assumes that the OC fault occurs in INV-1 (Fig. 2.1) and then proceeds to test whether it is true. If this test asserts that this assumption is false, then it is identified that the OC fault has occurred in INV-2. To optimize the number of current sensors, Hall CTs are placed in the DC-links of respective inverters. The symbols 'I_S*'* and 'I_{SD}' respectively denote the DC-link currents of INV-1 and INV-2. Thus, when an OC fault occurs due to the failure of anyone switching device in Sector-1 (Fig. 2.3a), both DC-link currents drop down to zero. Thus, as far as INV-1 is concerned (as by default it is assumed that INV-1 is faulty), either an OC fault has occurred for AH1 or BL6. The exact identification of the OC fault consists of the following sections. The proposed OC fault-diagnosis algorithms work for the 120^0 mode of operation.

2.4.1 Diagnosis of the Open-Circuit fault

The process of diagnosing the open-circuit fault consists of three stages namely, (i) fault identification, (ii) fault assertion, and (iii) fault localization. These three stages are described elaborately in the following sections.

A. Fault Identification

In this stage, it is monitored, whether or not the DC-link current of INV-1 drops below a certain critical threshold value of current 'I_{th}'. This threshold value is an appropriate fraction (R_f) of the reference current ('I_{ref}'), which is output by the speed controller when the BLDC Motor is operated in a closed loop. In the present work, a value of 0.1 is employed for 'R_f'. However, if the motor is operated in an open loop, a small current value such as 50mA is used as the critical threshold. It is evident that a lower value of 'R_f' ensures more reliable identification of the fault. Thus,

$$I_{th} = R_f * I_{ref} \tag{2.1}$$

$$\begin{cases} I_S < I_{th}, & \text{fault condition is indicated} \\ I_S \geq I_{th}, & \text{normal condition} \end{cases} \tag{2.2}$$

B. Fault Assertion

Part 1:

A mere Identification of OC fault is not adequate to assert that it has really occurred, as the DC-link current of INV-1 can momentarily drop below the value of the critical threshold due to disturbances. To conclusively assert that an OC fault has occurred, it should last longer than a predetermined 'critical-time-period', denoted as 'T_{fault}'. Whenever $I_S < I_{th}$, a timer is triggered and the time period for which the above condition prevails is monitored. This time period is named the 'error-time-period' and is denoted as 'T_e'. The error-time-period 'T_e' is accumulated in terms of the current sampling period 'T_s' as:

$$T_e(n) = T_e(n-1) + T_s \tag{2.3}$$

Where 'T_s' denotes the sampling period of 'I_S' with $T_e(-1)=0$. In this present work sampling period is 70μS.

In the process of the fault-detection, the error period '$T_e(n)$' is compared with the critical-time-period 'T_{fault}', which depends on the actual speed of the motor. Thus, the calculation of the critical-time-period ('T_{fault}') requires the knowledge of the period of one sector of operation 'T_{sector}'. The relationship between electrical angular velocity 'ω_{el}' and the mechanical angular velocity 'ω_{me}' is given by:

$$\omega_{me} = \frac{2}{P} * \omega_{el} \tag{2.4}$$

$$f_{el} = \frac{\omega_{el}}{2*\pi} \; ; t_{el} = \frac{1}{f_{el}} \tag{2.5}$$

Where 'P' denotes the number of poles, 'f_{el}' denotes electrical frequency, and 't_{el}' denotes the period for one electrical cycle.

As there exist 6 operational sectors (Fig. 2.2) in one electrical cycle of operation, 'T_{sector}' is (1/6) of the time for one electrical cycle (t_{el}).

$$T_{sector} = \frac{1}{6*f_{el}} \tag{2.6}$$

From eq. (2.5), eq. (2.6) can be rewritten as:

$$T_{sector} = \frac{4*\pi}{P*\omega_{me}*6} \tag{2.7}$$

The critical-time-period 'T_{fault}' is given by

$$T_{fault} = S_f \; * \; T_{sector} \tag{2.8}$$

Where 'S_f' is a fraction called *sensitivity factor* (i.e. $0 < S_f < 1$). It is obvious that a low value of 'S_f' leads to fast detection of OC fault at the expense of accuracy and vice-versa. A digital signal named 'Fault-Detection-Flag-1' (FDF1) is set to a value '1' when an OC fault is detected.

$$\begin{cases} FDF1 = 1, OCFSEC = m; \text{if } T_e(n) > T_{fault} \\ FDF1 = 0, OCFSEC = 0; \text{if } T_e(n) < T_{fault} \end{cases} \tag{2.9}$$

(For sector-(m), where $(1 \leq m \leq 6)$)

The sector number in which the OC fault is detected is stored in the flag 'OCFSEC' (i.e. $1 \leq OCFSEC \leq 6$).

Part 2:

Once an OC fault is detected in sector-m, the DC-link current of INV-1 (i.e., I_S), sampled in the next sector (i.e. Sector-2, Fig. 2.3b) would facilitate the identification of the switching device which causes OC fault. By adopting a similar procedure as described above

in sector-2 (or sector-(m+1) in general), another digital signal called 'Fault-Detection-Flag-2' (FDF2) is set to a value of '1' i.e.

$$\begin{cases} \text{FDF2} = 1 \ \text{ if } \ T_e(n) > T_{\text{fault}} \\ \text{FDF2} = 0 \ \text{ if } T_e(n) < T_{\text{fault}} \end{cases} \left(\begin{matrix} \text{for sector}-(m+1) \\ \text{where } (1 \le m \le 6) \end{matrix} \right) \qquad (2.10)$$

At the end of this stage, the switch that causes the OC fault (assuming that the fault occurs in INV-1) is determined. The flag 'OCFSW' stores the device number i.e. OCFSW ϵ (AH1, AL4, BH3, BL6, CH5, CL2) depending on the status flags 'FDF1', 'FDF2' & 'OCFSEC'.

C. Fault Localization

Till this stage, it is assumed that the OC fault always occurs in INV-1. As the top switch of INV-1 (AH1 in the present example, see Fig. 2.3a) is connected in series to the bottom switch of INV-2 (AL4' in the present example, see Fig. 2.3a), for a given phase winding (phase aa' in the present example) a detection of OC fault could be due to the failure of either AH1 or AL4'. To identify if AL4' has failed instead of AH1, the following procedure is adopted:

Step 1:

The gating signals of all of the top devices of INV-1 (i.e. AH1, BH3, and CH5) are disabled and the gating signals of all the bottom devices of INV-1 (AL4, BL6, CL2) are continuously fired. This would create an isolated electrical switched neutral as the points 'a', 'b', and 'c' are connected to the negative terminal of the DC-link of INV-1 (Fig. 2.1). The resulting system would therefore be identical to the conventional BLDC drive with a single DC power supply (with voltage '$V_{DC}/2$').

Step 2:

The gating signals are then applied exclusively to INV-2. Based on the DC-link current of INV-2 (i.e. I_{SD}) the procedure described in the previous section is repeated for INV-2 (till part-1 of the 'Fault-assertion' stage). If the fault persists, then it is obvious that the OC fault has occurred in INV-2 (meaning that AL4' has failed instead of AH1, contrary to the initial assumption). To rule out false detection of OC fault in INV-2, the aforementioned procedure is initiated after a safe period of 'T_{invchk}' from the time instant at which the OC fault was first asserted. An additional flag 'FINV' is used to denote the faulted inverter. If the OC fault occurs

in INV-1, then 'FINV' is set to '0'. On the other hand, if the OC fault occurs in INV-2, then 'FINV' is set to '1'.

2.4.2 Control for the Open-Circuit fault

A. Reconfiguration of the Faulted Inverter

As mentioned in Section-2.3, based on the information obtained w.r.t the OC fault, the inverter which develops the OC fault switch is clamped to a neutral state by applying an appropriate null vector (i.e. - - - or + + +). The type of the null vector is determined by the position of the faulted switch. For example, if any switch connected to the positive DC-rail fails, then all the three bottom switches are gated continuously, clamping that inverter to the state (- - -) and vice-versa.

It is evident that the topology presented for the OEWBLDC motor drive is capable of handling multiple OC faults, so long as they occur at one side (i.e. one or more among AH1, BH3, and CH5) and the switches on the other side are healthy (AL4, BL6, and CL2).

Table-2.1 summarizes the details regarding the reconfiguration of the system based on the status flags 'FDF1', 'FDF2', 'OCDMOD' and 'FINV'.

B. Reconnection of the Healthy Battery Bank

After the reconfiguration of the inverter, the healthy battery connected to the faulty inverter is redeployed to enhance the reliability of the drive. This task is accomplished with the aid of the DPDT relays, using the procedure described in the following paragraphs:

If FINV=0, then INV-1 has developed the OC fault and its battery bank is connected in parallel to its counterpart by energizing the relay coil of the DPDT-1 (Fig. 2.1). Similarly if FINV=1, then INV-2 has developed the OC fault, and its battery bank is connected in parallel to its counterpart by energizing the relay coil of the DPDT-2 (Fig. 2.1).

A simple transistor-based relay coil circuit, triggered by the 'FINV' signal under OC fault conditions, is employed to facilitate the reconnection of the battery bank To facilitate a safe reconnection, the battery of the faulted inverter is connected to its counterpart (in parallel) after a delay of 'T_{drelay}'. Fig. 2.4 shows the flowchart of fault-diagnosis and reconfiguration for OC fault.

Table 2.1: Information on the OC Fault-Diagnosis

(FDF1,FDF2,OCFSEC)	FINV	OCFSW	Clamped switches
(1,1,1) or (1,0,2)	0	AH1	AL4,BL6,CL2
	1	AL4'	AH1',BH3',CH5'
(1,1,3) or (1,0,4)	0	BH3	AL4,BL6,CL2
	1	BL6'	AH1',BH3',CH5'
(1,1,5) or (1,0,6)	0	CH5	AL4,BL6,CL2
	1	CL2'	AH1',BH3',CH5'
(1,1,4) or (1,0,5)	0	AL4	AH1,BH3,CH5
	1	AH1'	AL4',BL6',CL2'
(1,1,6) or (1,0,1)	0	BL6	AH1,BH3,CH5
	1	BH3'	AL4',BL6',CL2'
(1,1,2) or (1,0,3)	0	CL2	AH1,BH3,CH5
	1	CH5'	AL4',BL6',CL2'

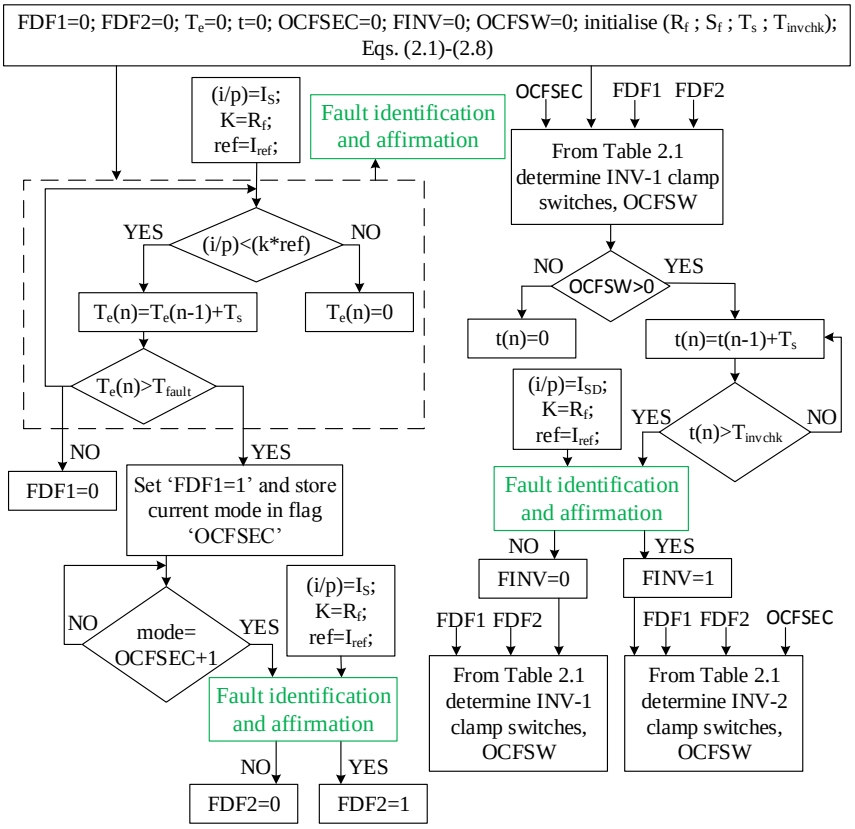


Fig. 2.4: Flowchart representing the fault-diagnosis and reconfiguration for OC fault

2.5 Fault-Diagnosis and Control for Short-Circuit Fault

The proposed SC fault-detection method is based on the measurement of the instantaneous line-line voltages (v_{ab}, v_{bc}, v_{ca}, $v_{a'b'}$, $v_{b'c'}$, $v_{c'a'}$). The matrix 'v_l' represents the line voltages, i.e.

$$v_l = [v_{ab} \quad v_{bc} \quad v_{ca} \quad v_{a'b'} \quad v_{b'c'} \quad v_{c'a'}]^T \tag{2.11}$$

The proposed SC fault-diagnosis algorithms work for the 120^0 mode of operation. The method of diagnosing and controlling the SCF is explained in the following paragraphs:

2.5.1 Diagnosis of the Short-Circuit Fault

If the SC fault takes place in switch AL4 during its conduction in Sector-4, then it won't affect its normal operation of Sector-4 and Sector-5. However, it must be detected during Sector-6 (i.e. before entering Sector-1, to avoid the shoot-through of DC supply as AH1 is scheduled to turn on in Sector-1). It may be noted that in Sector-6 the switches CH5 and BL6 are in conduction. Development of SC fault due to the failure of AL4 would cause the line-line voltage 'v_{ab}' to drop to zero in Sector-6, which can easily be detected by monitoring all the six line-line voltages mentioned in eq. (2.11). Thus, there exists a respectable period corresponding to 60^o (electrical) to detect if v_{ab} =0 (where it should not be equal to zero if AL4 is healthy).

In practice, a threshold '$v_{th,sc}$' is used to detect the SC fault, which is typically 5% (say 'k') of the peak of rated line-line voltage ('v_{ref}').

$$v_{th,sc} = k * v_{ref} \tag{2.11}$$

If any one of the absolute values of the measured line-line voltages (say $|v_{xy}|$; {(x, y) ϵ (a, b, c, a', b', c')}) is lesser than '$v_{th,sc}$', then error-time-period '$T_e(n)$' starts accumulating according to the following difference equation:

$$\begin{cases} T_e(n) = T_e(n-1) + Ts, & |v_{xy}| < v_{th,sc} \\ T_e(n) = 0, & |v_{xy}| > v_{th,sc} \end{cases} \tag{2.12}$$

Where (x) ϵ (a, b, c, a', b', c') & (y) ϵ (b, c, a, b', c', a')

When the count accumulated in '$T_e(n)$' is more than critical-time-period 'T_{fault}', then the corresponding flag 'SCF_{ab}' is set to '1'. Another flag named 'SCFSEC' is used to identify the sector number in which the fault is detected. For example, the flag 'SCF_{ab}' can be set to '1' either in Sector-3 (due to the failure of AH1) or Sector-6 (due to the failure of AL4). Consequently, the flag 'SCFSEC' can have a value of either '3' (if AH1 fails) or '6' (if AL4 fails). The generalized procedure of setting the flags 'SCF_{xy}' and 'SCFSEC' are represented by the following equations:

$$\begin{cases} SCF_{xy} = 1;\ SCFSEC = m & \text{if } T_e(n) > T_{fault} \\ SCF_{xy} = 0;\ SCFSEC = 0 & \text{if } T_e(n) < T_{fault} \end{cases} \tag{2.13}$$

(For sector-(m), where $(1 \leq m \leq 6)$)

Where (x) ϵ (a, b, c, a', b', c') & (y) ϵ (b, c, a, b', c', a')

The matrix 'SCF_l' contains all the six short-circuit flags i.e.

$$SCF_l = [SCF_{ab} \quad SCF_{bc} \quad SCF_{ca} \quad SCF_{a'b'} \quad SCF_{b'c'} \quad SCF_{c'a'}]^T \tag{2.14}$$

Table-2.2 summarizes all possibilities of SC fault and the status of the corresponding flags i.e., SCF_{xy} where {(x, y) ϵ (a, b, c, a', b', c')} and the corresponding values of 'SCFSEC'. The device, which is identified to be the source of SCF is also stored in an additional flag named 'SCFSW'.

2.5.2 Control for the Short-Circuit Fault

A. Reconfiguration of the Faulted Inverter

As in the case of OC fault, an appropriate null vector (i.e. - - - or + + +) is employed in this case also, to provide a switched neutral point by the faulty inverter. Here also, the type of the null vector is determined by the position of the faulted switch. In this case, if any switch connected to the positive DC-rail develops an SC fault, then the remaining switches connected to the positive DC rail are gated continuously, clamping that inverter to the state (+ + +) and vice-versa.

Upon the identification of the faulted switch (say AH1), all of the switches connected to the positive DC terminal of INV-1 (BH3, CH5) in this case are continuously gated, creating a switched neutral at point 'X' (Fig. 2.1). In other words, the gating signals corresponding to the lower switches (AL4, BL6, and CL2) are withdrawn, reconfiguring the power circuit. A

similar action is adopted if the SC fault is identified in INV-2. Table-2.2 (Last Column) also summarizes as to which switches are turned on for all the possible SC faults.

Table 2.2: Information on the SC Fault-Diagnosis

Fault Identification	Fault Assertion ($T_e > T_{fault}$)	SCF_l	SCFSEC	SCFSW	Clamped switches
$\|v_{ab}\| < v_{th,sc}$	Yes	$SCF_{ab} = 1$	3	AH1	AH1, BH3, CH5
			6	AL4	AL4, BL6, CL2
	No	$SCF_{ab} = 0$	-	-	-
$\|v_{bc}\| < v_{th,sc}$	Yes	$SCF_{bc} = 1$	5	BH3	AH1, BH3, CH5
			2	BL6	AL4, BL6, CL2
	No	$SCF_{bc} = 0$	-	-	-
$\|v_{ca}\| < v_{th,sc}$	Yes	$SCF_{ca} = 1$	1	CH5	AH1, BH3, CH5
			4	CL2	AL4, BL6, CL2
	No	$SCF_{ca} = 0$	-	-	-
$\|v_{a'b'}\| < v_{th,sc}$	Yes	$SCF_{a'b'} = 1$	6	AH1'	AH1', BH3', CH5'
			3	AL4'	AL4', BL6', CL2'
	No	$SCF_{a'b'} = 0$	-	-	-
$\|v_{b'c'}\| < v_{th,sc}$	Yes	$SCF_{b'c'} = 1$	2	BH3'	AH1', BH3', CH5'
			5	BL6'	AL4', BL6', CL2'
	No	$SCF_{b'c'} = 0$	-	-	-
$\|v_{c'a'}\| < v_{th,sc}$	Yes	$SCF_{c'a'} = 1$	4	CH5'	AH1', BH3', CH5'
			1	CL2'	AL4', BL6', CL2'
	No	$SCF_{c'a'} = 0$	-	-	-

B. Reconnection of the Healthy Battery Bank

The process of triggering the DPDT relays after the reconfiguration of the faulty inverter is described in the following paragraph:

If the SC fault is developed in INV-1, then one of the flags SCF_{ab}, SCF_{bc}, and SCF_{ca} is set to a logic level of '1'. These flags are input to an *OR* operation to derive the trigger signal to the relay coil of DPDT-1 (Fig. 2.1). A similar procedure is adopted for the reconnection of the battery bank connected to INV-2, wherein the flags ($SCF_{a'b'}$, $SCF_{b'c'}$, $SCF_{c'a'}$) are used to derive the trigger signal for DPDT-2.

Fig. 2.5 shows the flowchart of fault-diagnosis and reconfiguration for SC fault. The principal advantages of the proposed fault-detection schemes are:

1. The SC fault detection is essentially pre-emptive in nature as the acts of detection and the subsequent circuit reconfiguration are carried out before the SC fault can cause over-currents in healthy switching devices and damage them.

2. It uses simple, cheap, and easily available analog devices to achieve electrical isolation between the power circuit and control platform, avoiding the high-cost Hall voltage sensors.

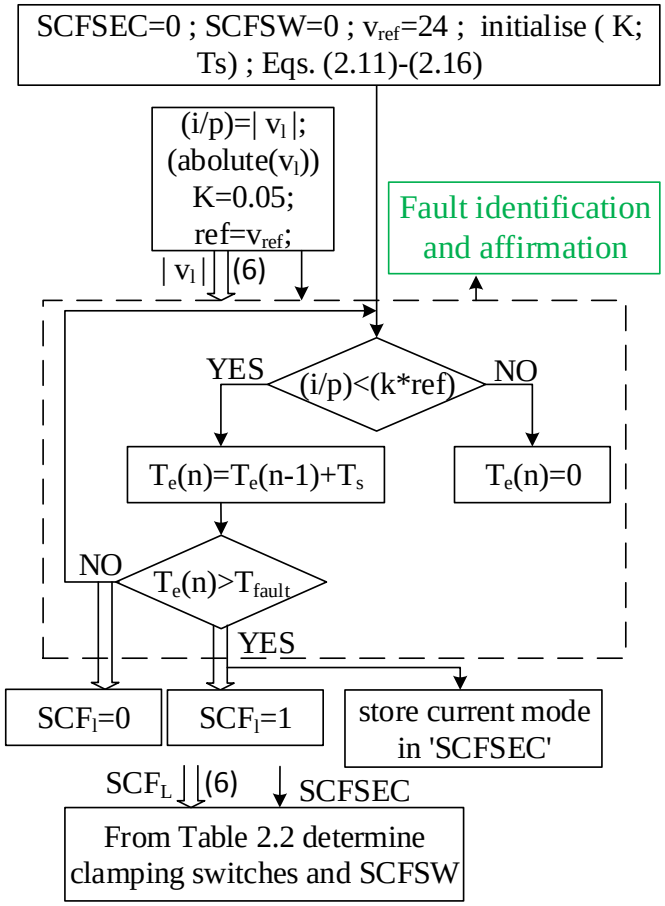


Fig. 2.5: Flowchart representing the fault-diagnosis and reconfiguration for SC fault

The OC/SC fault diagnosis can also be carried out by sensing the collector-to-emitter voltage of the individual switching devices. However, the proposed way of measuring DC-line currents for fault diagnosis facilitates the control of the BLDC motor drive. It also facilitates monitoring the condition of motor phase windings in addition to the diagnosis of the OC faults. The proposed line-line voltage monitoring to diagnose the SC fault obtains the required electrical isolation between the power circuit and the control platform.

2.6 Sensing and Interfacing Circuitry

2.6.1 Description of Hardware Circuit used for Fault-diagnosis

From the description of OC fault presented in section-2.4, it is obvious that the detection of OC fault requires the sensing of the two DC link currents. Similarly the diagnosis of SC fault requires the measurement of all six line voltages (v_{ab}, v_{bc}, v_{ca}, $v_{a'b'}$, $v_{b'c'}$, $v_{c'a'}$) present on either side of the motor, with open-ended stator windings. All of these line-line voltages need to be electrically isolated w.r.t the ground-point of the control platform (i.e. dSPACE in the present case).

2.6.2 Design of Low-Cost Analog Voltage Sensor with Electrical Isolation

As mentioned above, the sensing of SC fault involves the measurement of six-line voltages. The line-line voltages are measured using differential amplifiers (shown at extreme-left and at extreme-right of Block-1 and Block-2 in Fig. 2.6). Though Fig. 2.6 shows the sensing of the line voltages 'v_{ab}' (Block-1) and '$v_{a'b'}$' (Block-2) only, such circuits are replicated for the sensing of the other line-line voltages as well (Blocks 4-6, Fig. 2.6). The DC-link voltages of INV-1 and INV-2 are each equal to 24 V (Table-A.1). These DC-link voltages are split equally using capacitors (Fig. 2.6) and two isolated ground points 'G_1' and 'G_2' are derived.

The operational amplifiers derive their power supplies from the X & X' points, and Y & Y' points, to sense the line voltages on INV-1 and INV-2 sides respectively ($v_{XG_1} = v_{YG_2} = 12$ V and $v_{X'G_1} = v_{Y'G_2} = 12$ V). In other words, the voltage sensing circuitry derives its power supplies directly from the vehicle battery. Precision Isolation Amplifiers (ISO124), which are of unity gain, are employed to achieve electrical isolation, However, this device needs another isolated power supply to obtain electrical isolation between the grounds 'G_1', 'G_2' and the ground of the control platform 'G_3'. The outputs of all of the measured line-line voltages obtained at the outputs of the isolation amplifiers, which are electrically isolated are represented by a matrix 'v_{lc}' i.e.

$$v_{lc} = [vc_{ab} \quad vc_{bc} \quad vc_{ca} \quad vc_{a'b'} \quad vc_{b'c'} \quad vc_{c'a'}]^T \tag{2.15}$$

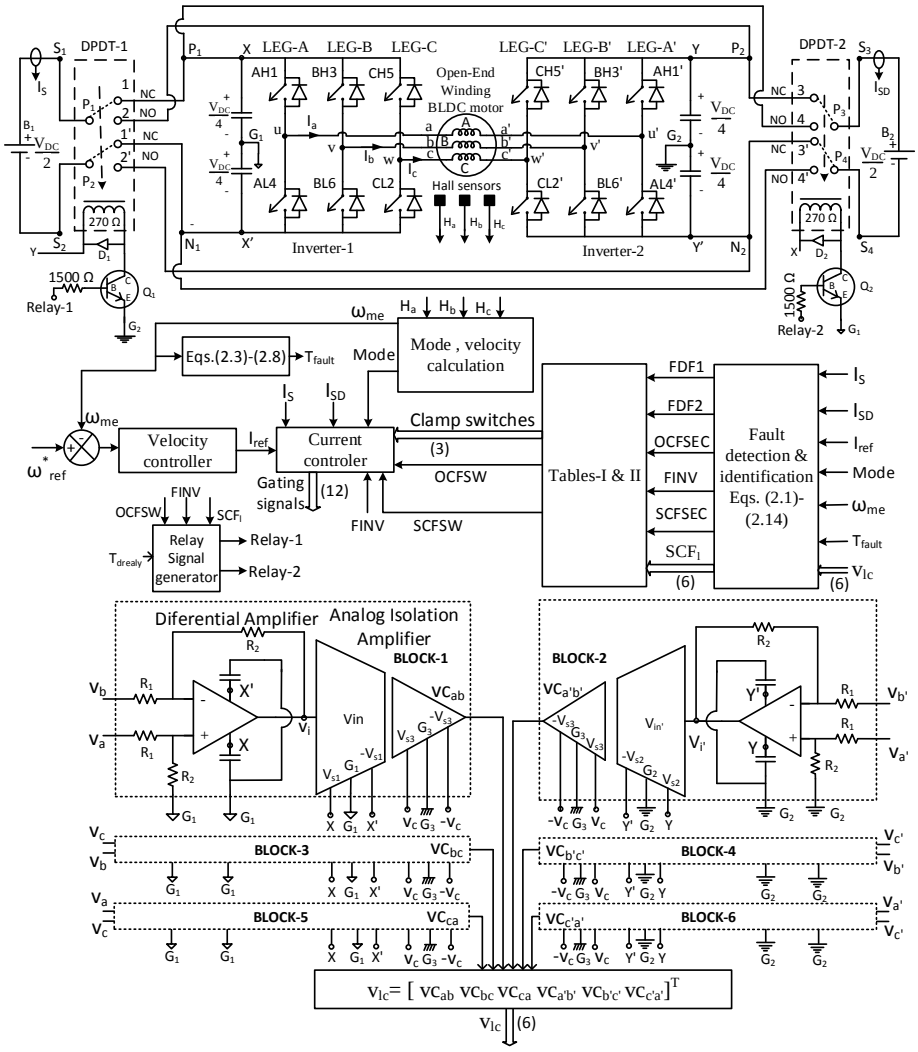


Fig. 2.6: Overall Configuration of Fault-Tolerant BLDC Motor Drive Configuration

These control voltages are restored to the original value by multiplying with the appropriate scale factor (i.e. depending on differential amplifier gain) in the control platform. Alternatively, all isolated power supplies can be derived directly from the vehicle battery using an appropriate Switch Mode Power Supply. The developed analog voltage sensor results in a lower cost compared to the Hall-voltage sensors. However, the algorithm proposed for the diagnosis of the SC fault doesn't require the magnitudes of the line-line motor terminal voltages. It needs only a level signal which is indicative of the occurrence of the SC fault. Thus, further cost reduction can be obtained by processing the level detection signal on the high voltage side through an opto-isolator for diagnosing the SC fault conditions.

As stated earlier, two DPDT switches are used in this system to connect the battery bank of the faulted inverter in parallel to its counterpart. The operating voltage of the DPDT relay coil is 12 V. After the diagnosis of the fault (i.e. OC fault or SC fault) and the subsequent

reconfiguration of the power circuit, one of the relay coils is energized through a transistor, which derives its base signal (Relay-1/2 signal) from the control platform (i.e. dSPACE-1104 in the present work). The transistors 'Q_1' and 'Q_2' control the relay coils of the DPDT-1 and DPDT-2 relay respectively (see Fig. 2.6). It can easily be verified that the power supplies for these transistors must be cross-connected for an appropriate reconnection of the healthy battery corresponding to the faulted inverter. For example, when INV-2 fails, the battery bank 'B_2' must be reconnected in parallel to its counterpart (i.e. 'B_1'). It can be easily verified that this objective is achieved only when the relay transistor, which reconnects the battery 'B_2' derives its power supply from 'B_1' (and vice-versa).

The performance of the proposed diagnosis algorithms is experimentally verified with both open-loop and closed-loop operation of the drive. The closed-loop operation of the drive is based on the classical structure, wherein the outer speed loop specifies the reference for the inner current loop. Fig. 2.6 presents the overall control scheme, including the generation of the gating signals needed for the switching devices of the dual-inverter scheme for both healthy and faulty conditions.

2.7 Results and Discussion

The behaviour of the fault-tolerant OEWBLDC motor drive under OC fault & SC fault is first assessed with simulation studies using MATLAB/Simulink and then are experimentally validated using the dSPACE-1104 control platform. For verification, the experimental setup of fault-tolerant BLDC motor drive configuration (shown in Fig. 2.6) has been built in the laboratory and its physical layout is shown in Fig. A1. Table-A.1 presents the motor parameters used for simulation as well as experimentation. The experimental setup consists of power semiconductor inverter switches along with the driver circuitry, proposed analog-based voltage sensors, current sensors, relay circuitry, battery power supply, BLDC motor (which can be operated as a conventional star connected BLDC motor or OEWBLDC motor), hall-effect sensor input driver circuitry, and a *dSPACE-1104* control platform with host PC to produce the gating signals for fault-tolerant drive operation.

Simulation and experimental results for OC fault are studied by opening the switching devices CH5 & CL2' for INV-1 and INV-2 respectively. During experimentation, the OC fault condition is enforced on the inverters by withdrawing the gating pulses to them. Similarly to enforce the SC fault conditions, the gating pulses for AL4 and AL4' are applied continuously.

As mentioned in the previous sections, two flags (namely OCFSW and SCFSW) are employed to identify and indicate the faulted switching device. As stated earlier, it is assumed that OC fault takes place in INV-1 by default. OC fault is identified in INV-2 only when it is identified that it didn't take place in INV-1.

2.7.1 Simulation Results

Figs. 2.7 & 2.8 show the simulation results to detect the OC fault in INV-1. The sector number (1-6) of conduction is identified by monitoring the pattern of the Hall Position sensors placed on the shaft of the motor. Thus, the signal which identifies the sector of operation starts at '1' and is incremented by '1', whenever a change in the sector of conduction is identified by monitoring the Hall-sensor signals. It rolls back to '1' again from Sector '6', as each sector of operation lasts for 60 electrical degrees (Fig. 2.7 (a)). Thus, when the DC-link current falls to zero following the development of an OC fault (Fig. 2.7 (b)), the sector of conduction in which the OC fault occurs is identified and is registered in the flag 'OCFSEC' (Fig. 2.7 (c)). Based on the statuses of the internal flags 'FDF1', 'FDF2' & 'OCFSEC' (Figs. 2.7 & 2.8) the faulted switch is identified as CH5 in the present case (from Table-2.1) and is stored in the flag 'OCFSW' (at 'tz', Fig. 2.7 (d)) with its device number.

Fig. 2.8 shows the internal process of setting the flags 'FDF1' & 'FDF2'. When the DC-link current of INV-1 drops to a value, which is lesser than the threshold current (at the instant 'tf', see in Figs. 2.7 (b) & 2.8 (a)) an accumulator is initiated (eq. (2.3)). When the count accumulated is more than the critical-time-period ('T_{fault}'), the flag 'FDF1' is set (at the instant 'tx', in Fig. 2.8 (b)). This means that at the instant 'tx', it is identified that, so far as INV-1 is concerned, the faulted switch could be either CH5 or AL4. To further identify which of these two switches has failed, another accumulator is initiated at the beginning of the next sector (instant 'ty', Fig. 2.8 (c)). When the count accumulated is greater than the 'T_{fault}', the flag FDF2 is set to '1' (at 'tz', Fig. 2.8 (d)). Based on the statuses of flags 'FDF1', 'FDF2' and 'OCFSEC', the faulted device is identified using Table-2.1.

Fig. 2.9 shows the simulation results for the identification of OC fault in INV-2. The device CL2' is in series with CH5 under normal operation and it is initially assumed that the OC fault occurs in INV-1. Thus, the OC fault is initially attributed to CH5 at a time 'tp' (Fig. 2.9 (d)) and only INV-2 is operated by clamping INV-1 (i.e. a switched neutral point is created by turning on the switching devices connected to the negative DC rail of INV-1). However, if

the OC fault exists in INV-2, then it is observed that the DC current I_{SD} is discontinuous in nature. This situation is presented in Fig. 2.9 (b), wherein a pulsating current waveform (zoomed version of Fig. 2.9 (b)) is observed as I_{SD} can exist in only four sectors out of the six possible sectors of conduction, confirming that the OC fault has occurred in INV-2. To rule out false-positive identification (i.e. a spurious detection), the process of fault detection is initiated at the time instant 'tq' (Fig. 2.9 (d)) and is diagnosed at a time 'tr' and thereby 'FINV' flag is set to high (at instant 'tr', in Fig. 2.9 (a)). Upon the active high identification of flag 'FINV', the flag 'OCFSW' is updated with the actual faulty switch number corresponding to switch CL2' (i.e. '2', see Fig. 2.9(d)). When it is identified that the OC fault has occurred in INV-2, the switched neutral is created by INV-2, and INV-1 is operated normally.

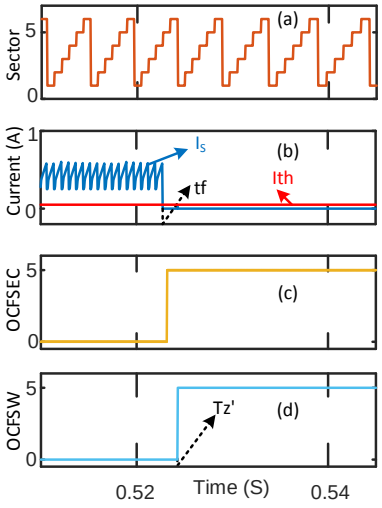


Fig. 2.7: Simulation results for OC fault in INV-1 (i.e., switch CH5): (a) sector of operation (b) I_S, I_{th} (c) OCFSEC (d) OCFSW

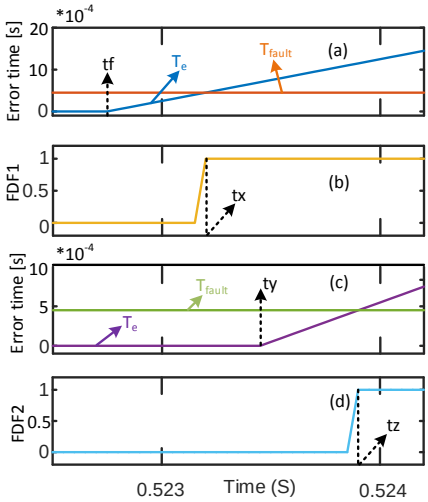


Fig. 2.8: Simulation results representing statuses of flags for OC fault in INV-1 (i.e., switch CH5): (a) T_e, T_{fault} (Sector-5) (b) FDF1 (c) T_e, T_{fault} (Sector-6) (d) FDF2

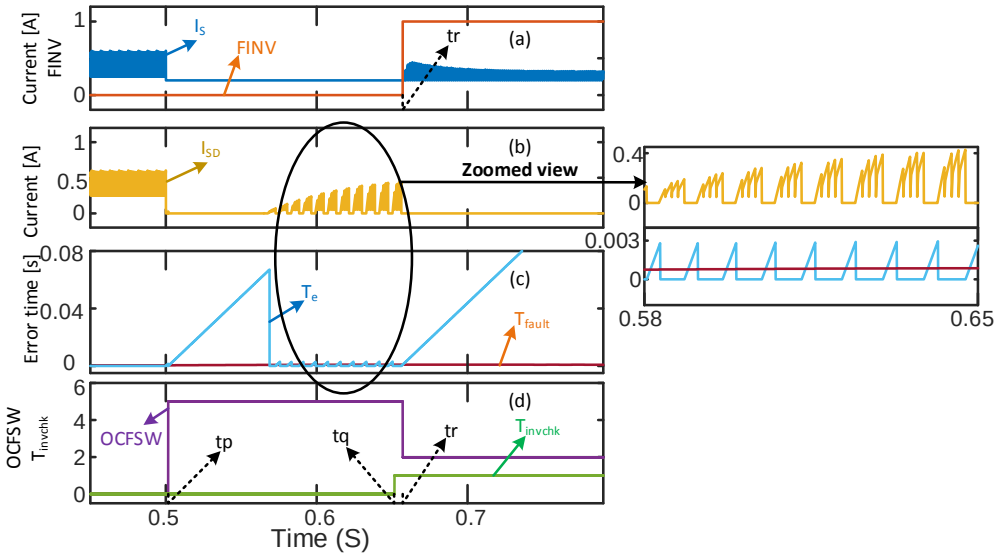


Fig. 2.9: Simulation results representing fault-diagnosis of OC fault in INV-2 (i.e., switch CL2'): (a) I_S, FINV (b) I_{SD} (c)T_e, T_{fault} (d) OCFSW, T_{invchk} (Left : Normal view; Right : Zoomed view of encircled portion)

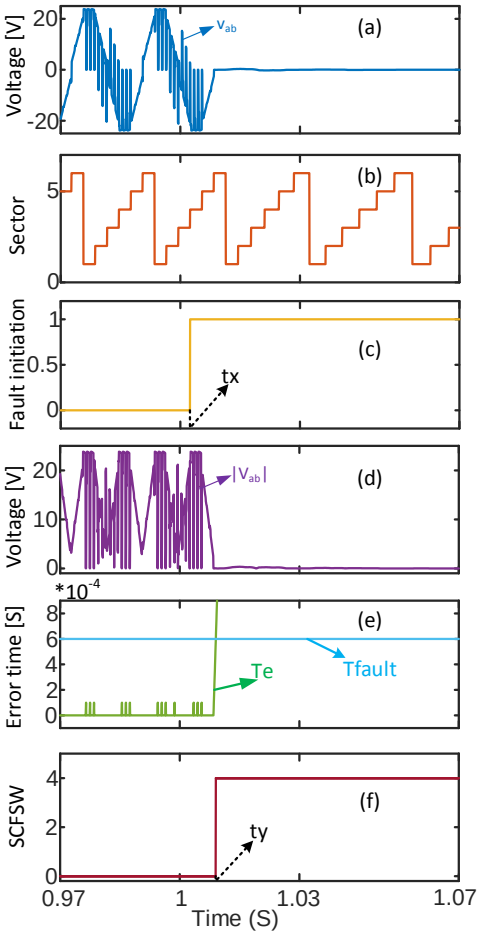


Fig. 2.10: Simulation Results showing SC fault-diagnosis for INV-1 (i.e., switch AL4): (a) v_{ab} (b) operating sector (c) fault initiation (d) $|v_{ab}|$ (e) T_e, T_{fault} (f) SCFSW

The simulation result, which demonstrates the SC fault-diagnosis process is presented in Fig. 2.10. The SC fault was induced in AL4 by gating it continuously. However, as AL4 is expected to conduct normally during Sector-4 and Sector-5 (Fig. 2.2), the effect of SC fault is not visible immediately during these two sectors of operation. It would be visible only in Sector-6 and the circuit reconfiguration must take place within this sector of operation; otherwise, as described earlier, a shoot-through fault would occur. Figs. 2.10 (a) & 2.10 (b) shows the line voltage 'v_{ab}' and the signal corresponding to the sector of operation. The SC fault is induced into the system at the instant 'tx' (Fig. 2.10 (c)). Fig. 2.10d shows the $|v_{ab}|$, which is compared with 'v_{th}' (see Table-2.2), which is selected to be 5% of the peak value of the line voltage (i.e. 0.05*24=1.2 V). As mentioned in the earlier section if $|v_{ab}| < v_{th}$ for a time-period of 'T_{fault}' (Fig. 2.10 (e)), then the occurrence of SC fault is confirmed in INV-1. Fig. 2.10 (f) shows the switching device in which short-circuit fault is identified (switch '4' in INV-1 in this case, which is AL4).

2.7.2 Experimental Results

To validate the proposed diagnosis and reconfiguration of the dual-inverter fed OEWBLDC motor drive, the dSPACE-1104 hardware control platform is used and the corresponding experimental setup is shown in Fig. A.1.

Figs. 2.11 & 2.12 show the process of fault-diagnosis and circuit reconfiguration when the drive is operated in open-loop and an OC fault is deliberately induced for CH5 (which is present in INV-1, Fig. 2.1). The top trace of Fig. 2.11 shows the DC-link current of INV-1. When an OC fault is induced for the switching device CH5, it drops down to zero. The second and third traces of Fig. 2.11 respectively show the setting of the fault-diagnosis flags (FDF1 & FDF2), which are set to '1' in response to the detection of OC fault. The fourth trace shows the flag 'OCFSW', which displays a value of '5' indicating that the OC fault is detected in CH5.

The process of reconfiguration is shown experimentally in Fig. 2.12. It may be noted that after the identification of the OC fault in CH5, a switched neutral is created on INV-1 and INV-2 is operated normally. Thus, one may notice a momentary interruption for both of the DC-link currents (I_S & I_{SD}) of the respective inverters (at the instant 'ta'). During the period (tb-ta), the process of identification and reconfiguration of the power circuit is carried out (as shown in Figs. 2.11 & 2.12). As the drive is operated in an open-loop, owing to the reduced

voltage applied to the phase windings of the motor, the motor speed is reduced, as is evident from the third trace of Fig. 2.12.

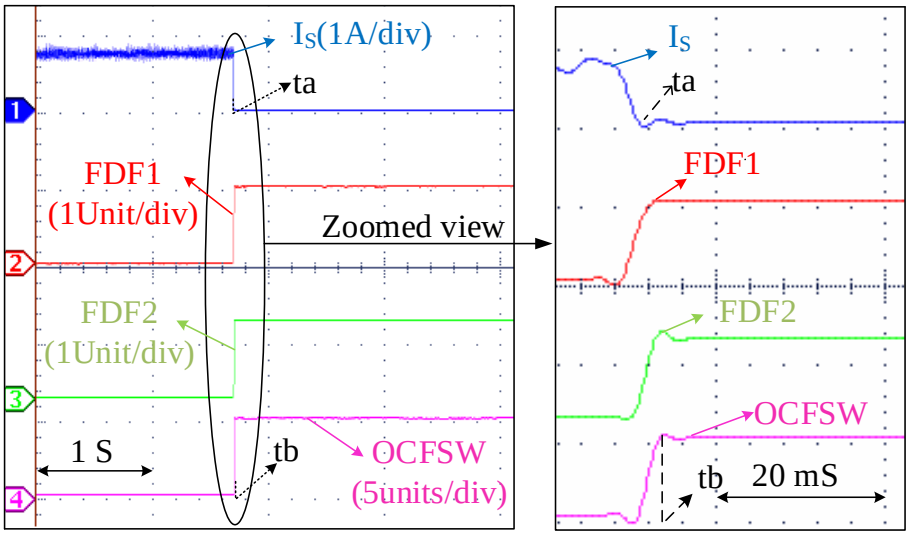


Fig. 2.11: Experimental results representing statuses of flags during OC fault in INV-1 (i.e., switch CH5) (Left: Normal view, Right: Zoomed view of encircled portion)

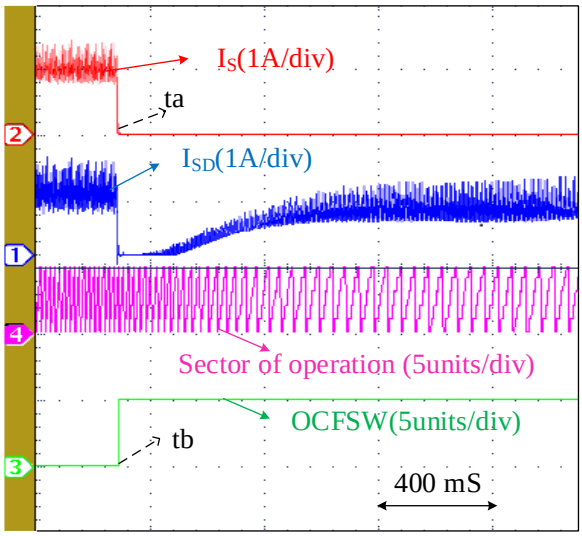


Fig. 2.12: Experimental Results for OC fault in INV-1 (i.e., switch CH5)

Fig. 2.13 shows the experimental results when the OC fault occurs in CL2' belonging to INV-2. In this case also, following the OC fault, both DC-link currents (I_S & I_{SD}) drop to zero momentarily. As explained earlier it is assumed that the OC fault takes place in INV-1 and INV-2 is operated normally, to ascertain whether or not this assumption is true. The presence of the current-zero instants in I_{SD} clearly reveals that this assumption is false (as only four out of the six sectors of conduction are possible in INV-2). Owing to the realization that the fault occurs in INV-1, it is reconfigured to a switched neutral and INV-2 is operated

normally. The third trace of Fig. 2.13 shows the status of the flag 'FINV', which is set to '1' when the assumption of INV-1 being faulty is wrong. Consequent to this, the flag 'OCFSW', which identifies the faulty switch in INV-1 is reset to the actual switch number (i.e. 2).

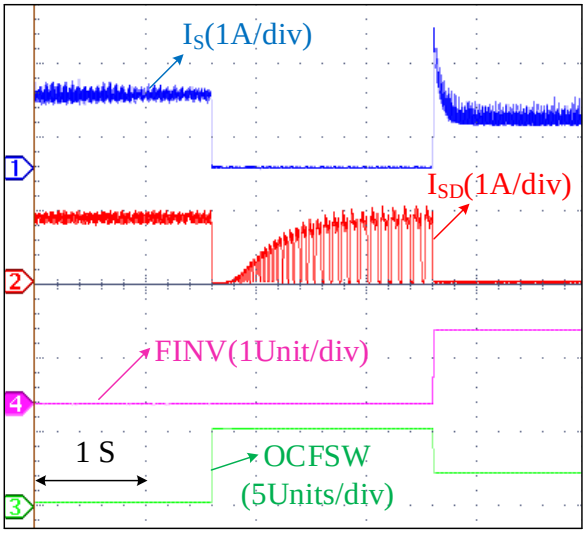


Fig. 2.13: Experimental Results for OC fault in INV-2 (i.e., switch CL2')

The experimental results, which demonstrate the performance of the drive under faulted conditions are shown in Figs. 2.14 & 2.15 (open-loop) and Figs. 2.16 & 2.17 (closed-loop). From Figs. 2.14 & 2.15 it may be observed that the speed (shown in the third trace) is reduced when only one inverter is in operation instead of two. In contrast, when the drive is operated in a closed-loop (Figs. 2.16 & 2.17), the speed is restored to the reference value, despite one inverter being out of action. However, it should be realized that the restoration of speed is possible only up to half of the rated speed of the motor.

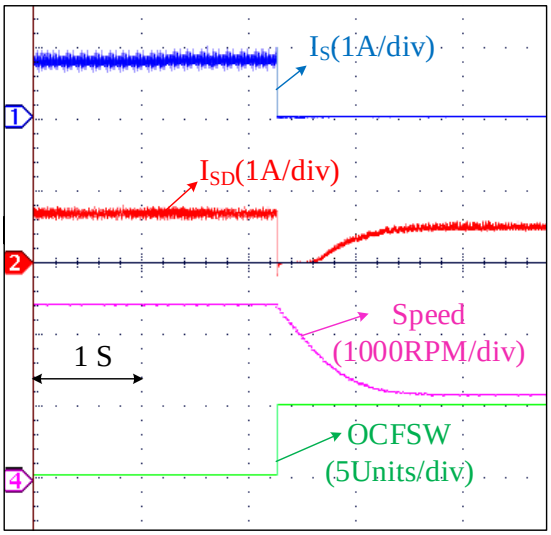


Fig. 2.14: Experimental Results for the OC fault in INV-1 under the open-loop operation of the Drive

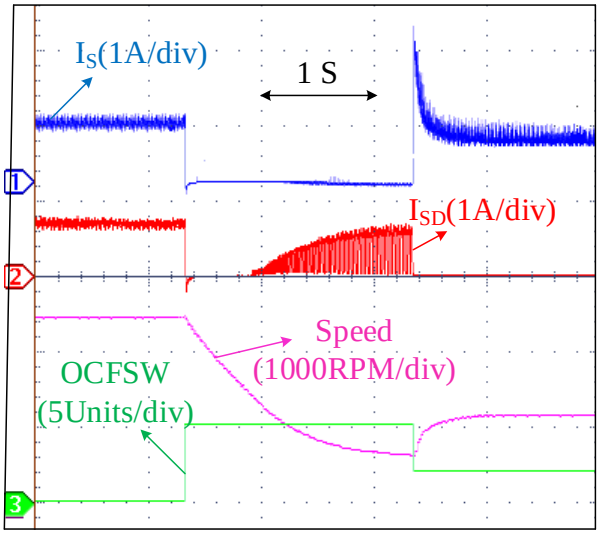


Fig. 2.15: Experimental Results for the OC fault in INV-2 under the open-loop operation of the Drive

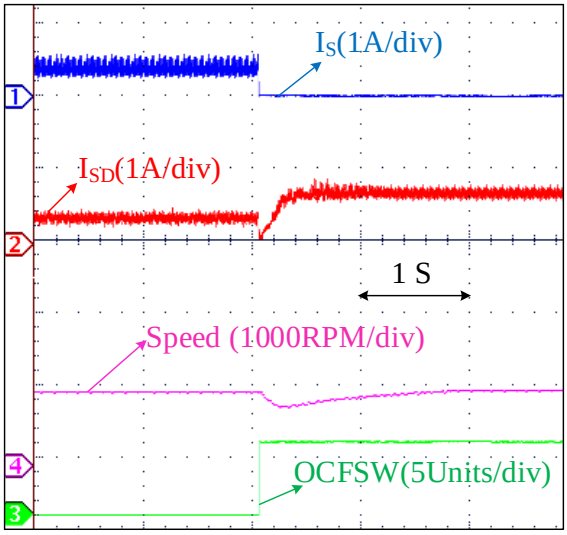


Fig. 2.16: Experimental Results for the OC fault in INV-1 under the closed-loop operation of the Drive

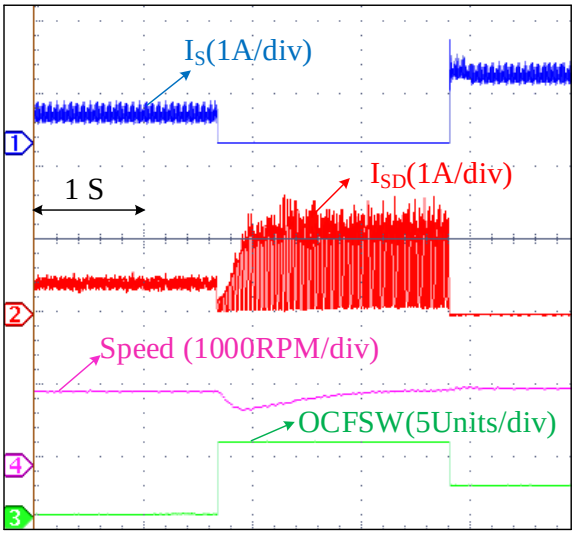


Fig. 2.17: Experimental Results for the OC fault in INV-2 under the closed-loop operation of the Drive

The experimental results, which demonstrate the diagnosis of the short-circuit fault are shown in Figs. 2.18, 2.19, 2.20 & 2.22. The six line-line voltages are monitored corresponding to the sampling frequency of the digital control platform (70 μS). To verify the effectiveness of the proposed fault-diagnosis algorithm, the gating signal to the switching device AL4 is continuously turned on from the instant 'tx' (see Figs. 2.18, 2.19 & 2.20). Under normal operating conditions, it is apparent from Fig. 2.18 that the line voltage 'v_{ab}' is not equal to zero. However, when an SC fault occurs in INV-1 at the instant 'tx' (see Figs. 2.18, 2.19 & 2.20), the line voltage (v_{ab}) drops to zero in Sector-6 (which was not supposed to be during normal conditions), triggering an accumulator. When the output of this accumulator (which is denoted as T_e, eqn. 2.12) is greater than a pre-specified count 'T_{fault}' (at the instant 'ty' in Fig. 2.19), the flag 'SCFSW' is loaded with the number corresponding to the faulty switch ('4', for the switch AL4, see Fig. 2.20) by using Table-2.2. It may be noted that after the identification of the fault and the reconfiguration of the power circuit, the entire drive current is sourced by INV-2 alone (see Figs. 2.18 & 2.20). Fig. 2.20 clearly shows the time elapsed between the initiation of the fault (at 'tx') and the identification of the fault (at 'ty'). A similar experimental result for the SC fault developed in INV-2, for the device AL4', is shown in Fig. 2.21. Figs. 2.22 & 2.23 show the speed transient when the drive is operated in open-loop and closed-loop conditions respectively when the SC fault occurs in INV-1.

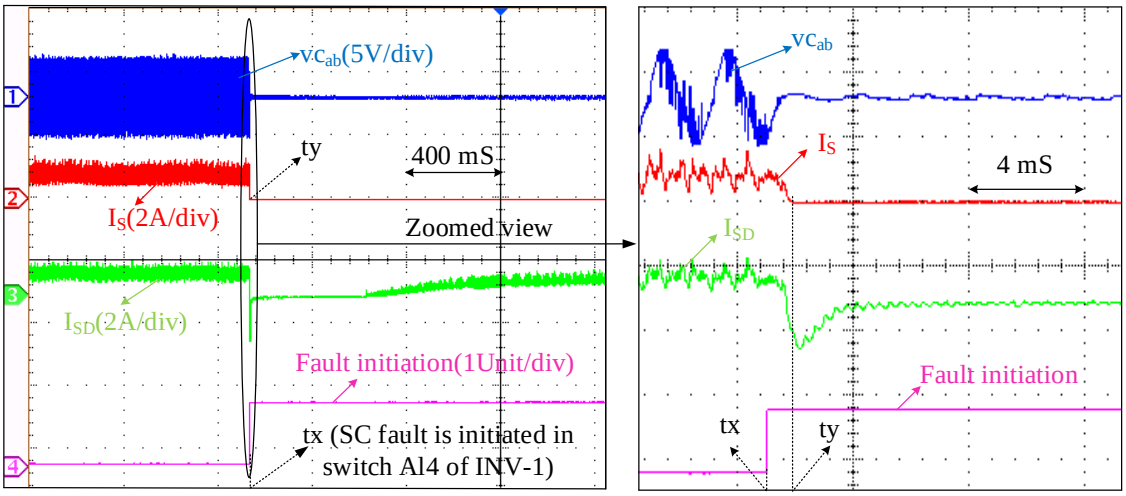


Fig. 2.18: Experimental Results for the detection of SC fault in INV-1 (i.e., switch AL4)
(Left: Normal view, Right: Zoomed view of encircled portion)

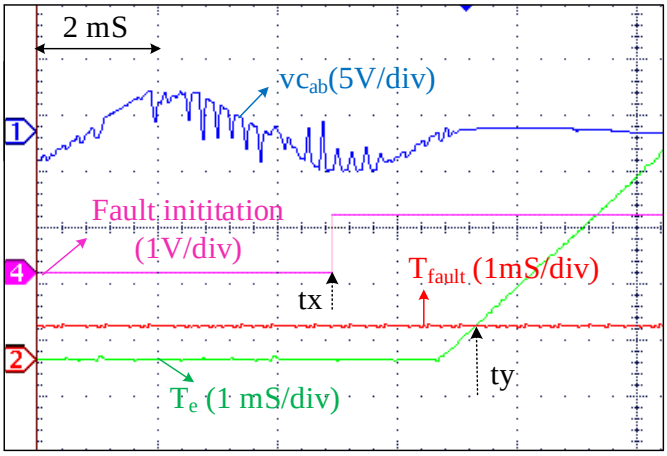


Fig. 2.19: Experimental Results for the detection of SC fault in INV-1 (i.e., switch AL4)

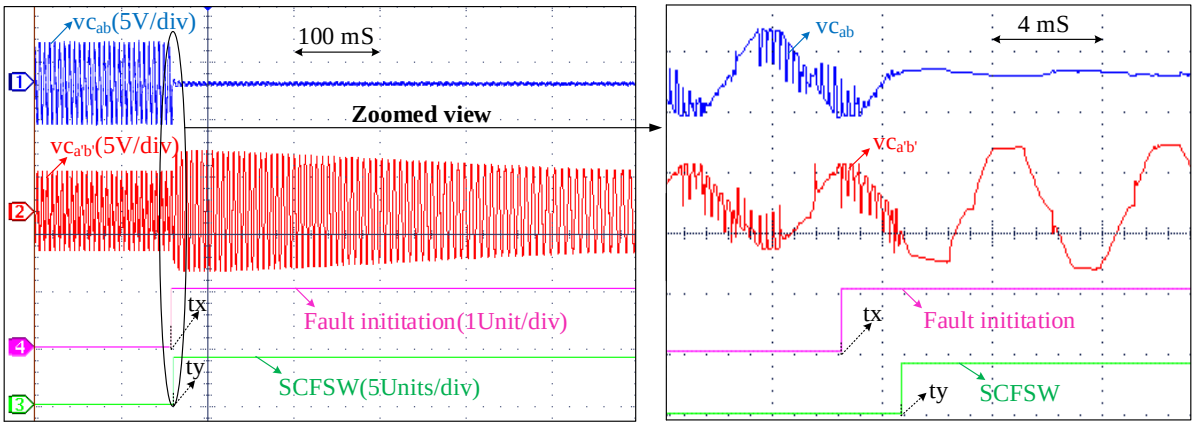


Fig. 2.20: Experimental Results for the detection of SC fault in INV-1 (i.e., switch AL4) (Left: Normal view, Right: Zoomed view of encircled portion)

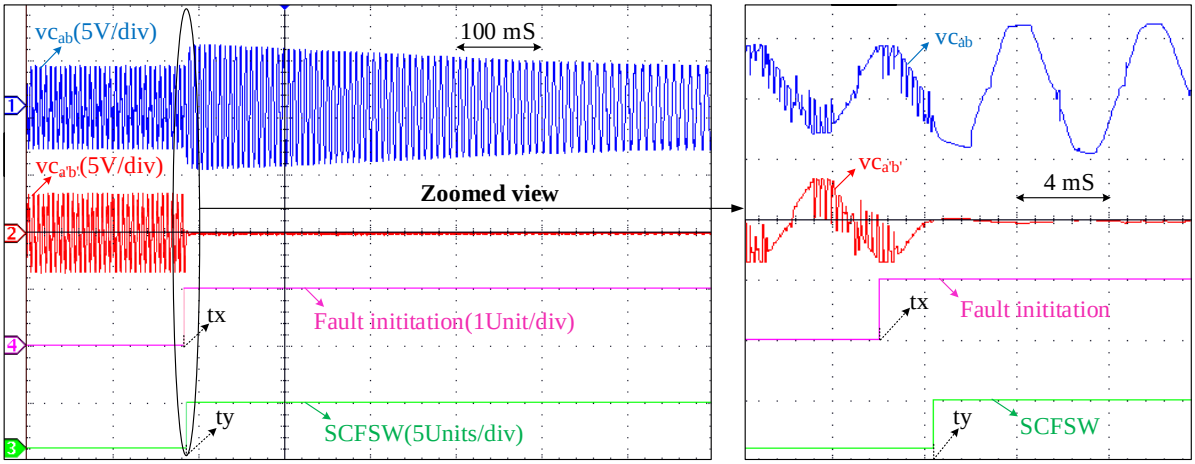


Fig. 2.21: Experimental Results for the detection of SC fault in INV-2 (i.e., switch AL4') (Left: Normal view, Right: Zoomed view of encircled portion)

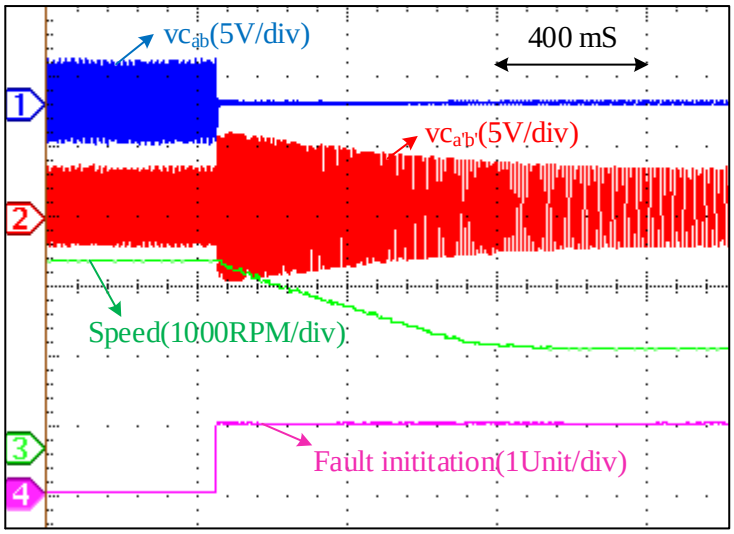


Fig. 2.22: Experimental Results for SC fault in INV-1 under open-loop operation

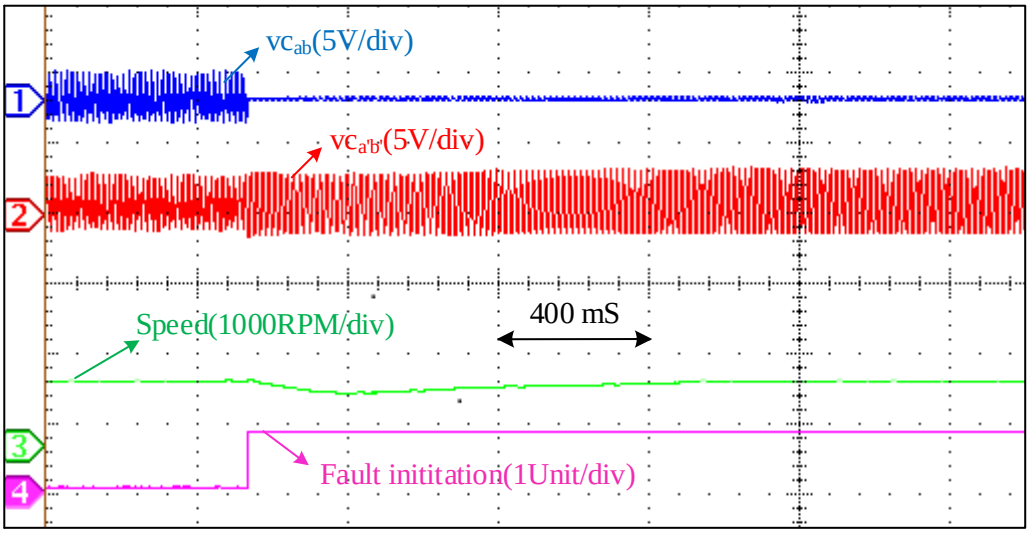


Fig. 2.23: Experimental Results for SC fault in INV-1 under closed-loop operation

The experimental result, which demonstrates the combination of OC fault-diagnosis and fault control is presented in Fig. 2.24. As mentioned earlier, whenever a fault is detected (OC fault or SC fault) and the faulty inverter is reconfigured to a switched neutral, the healthy battery bank feeding it is reconnected to its counterpart feeding the healthy inverter (in parallel). It may be noted that both I_S & I_{SD} are non-zero before the fault (see Part-I, Fig. 2.24). When an OC fault is induced in INV-1 (i.e., switch CH5) at instant 't1' (see Fig. 2.24), both 'I_S' & 'I_{SD}' fall to zero. After the successful diagnosis of the OC fault and the reconfiguration of the faulty inverter, INV-2 alone supplies power to the BLDC motor (see Part-II, Fig. 2.24). Under these conditions, it is desirable to connect the battery ('B_1') of INV-1 in parallel to its counterpart ('B_2'). This task is accomplished by turning on the transistor 'Q_1' (see Fig. 2.6) connected to the relay coil of DPDT-1 (at instant 't2', see Fig. 2.24). It may be observed from

Fig. 2.24 that the load current is then shared by the battery 'B_1' and 'B_2' following the reconnection (see Part-III, Fig. 2.24).

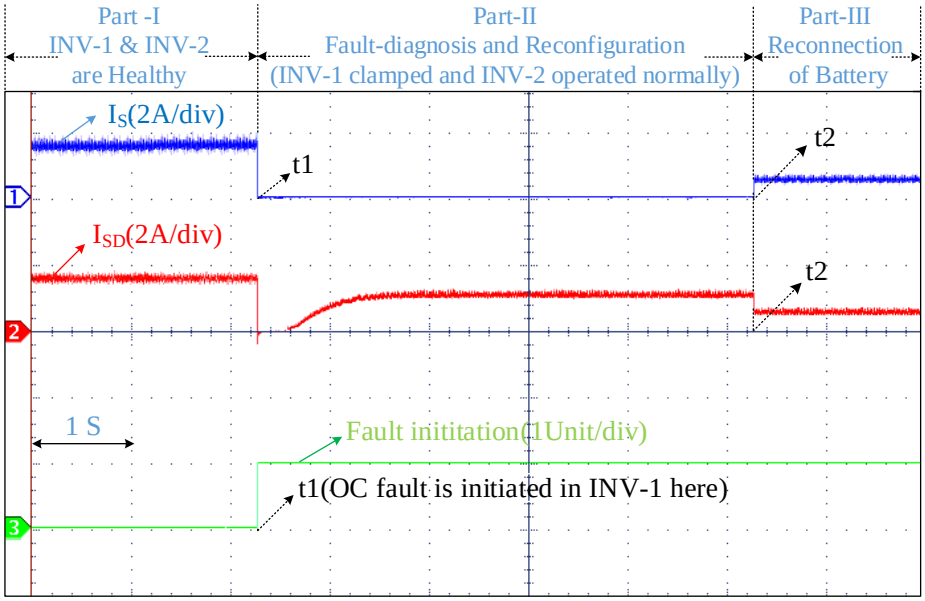


Fig. 2.24: Experimental Results showing fault-diagnosis and fault control for OC fault in INV-1

Fig. 2.25 shows the experimental results pertaining to the combination of the SC fault-diagnosis and fault control. It may be noted that the line voltage (v_{ab}) and the DC-link currents of the respective inverters (I_S and I_{SD}) are non-zero before the fault (see Part-I, Fig. 2.25). From Fig. 2.10 (a) and 2.10 (b), it is evident that line voltage 'v_{ab}' is not equal to zero in Sector-6 under healthy conditions. However, when an SC fault occurs in INV-1 (induced forcefully during the experimentation by triggering AL4 permanently) at instant 't1' (see Fig. 2.25), the line voltage (v_{ab}) drops to zero in Sector-6 (Fig. 2.10 (a) and 2.10 (b)). After the diagnosis of the SC fault based on the analog signals corresponding to the line voltage and the subsequent reconfiguration of the faulty inverter, the motor is constrained to be fed exclusively by INV-2 (see Part-II, Fig. 2.25). As in the case of the OC fault, to utilize the battery connected to the faulty inverter, the DPDT-1 relay is energized (at instant 't2', see Fig. 2.25) by turning on the transistor 'Q1' (see Fig. 2.6). Thus, the battery bank 'B_1' of INV-1 is connected in parallel to its counterpart. It may be observed from Fig. 2.25 that, following the reconnection, the load current is shared by both of the batteries 'B_1' and 'B_2' (see Part-III, Fig. 2.25).

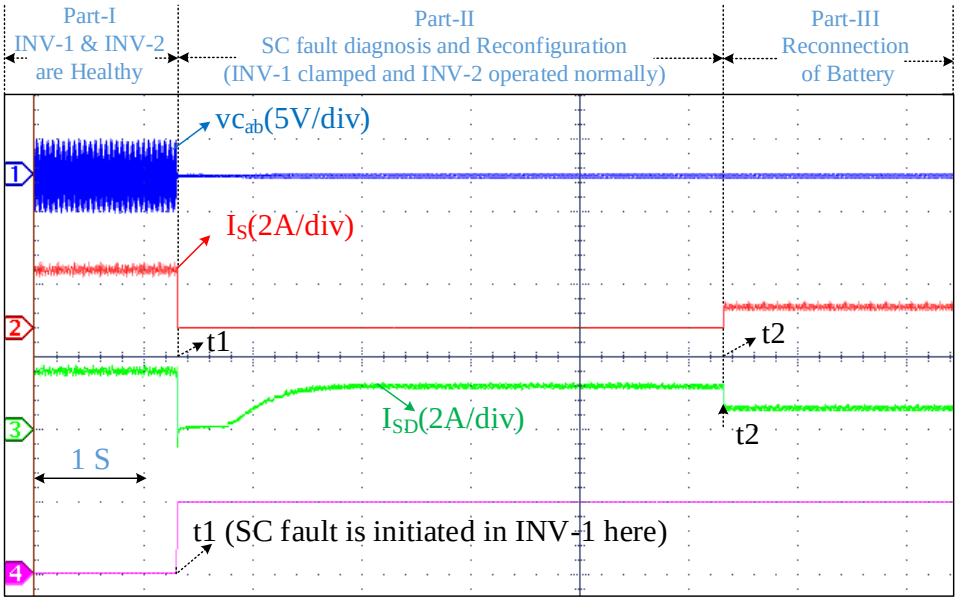


Fig. 2.25: Experimental Results showing fault-diagnosis and fault control for SC fault in INV-1

2.8 Feasibility Analysis of the proposed Power circuit configuration

A comparative study is carried out to assess the feasibility of the proposed power circuit configuration vis-à-vis the other fault-tolerant topologies reported in earlier literature. Table-2.3 summarizes the features of the proposed power circuit with other fault-tolerant topologies reported in earlier literature.

A cost analysis is also performed to assess the economic viability of the proposed power circuit configuration (shown in Table-2.4). In this analysis, the costs of additional components, which impart the feature of fault tolerance to the conventional drive configuration are considered. In this study, a 3KW BLDC motor drive configuration is considered for carrying out the cost analysis.

It should be noted that in the above analysis, only the raw material cost of the electrical items are considered and costs of vehicle chassis, vehicle body, control platform, and other accessories (which will be common for conventional and other topologies) are not included.

Thus, with an increment of reasonable additional raw material cost to the conventional electric drive configuration, the drive is capable of achieving fault tolerance to both OC and SC faults in the semiconductor switching devices, enhancing the reliability of the drive.

Table 2.3: Comparison of Different Topologies with the Proposed Topology

Topological features	Topology [70]	Topology [72]	Topology [73]	Proposed Topology
1. No. of switches in the inverter	6 switches (VSI) + 3 TRIACs	6 switches (VSI) + 6 TRIACs + 1 additional leg	12 switches	12 switches
2. Switch ratings	Rated motor voltage and current	Rated motor voltage and current	Rated motor voltage and twice the rated motor current	Half the rated motor voltage and rated motor current
3. Fault-diagnosis in inverter extra switches	No	No	Yes	Yes
4. Fault-diagnosis	Only OCF	OCF, SCF	OCF, SCF	OCF, SCF
5. Fault tolerance	Only OCF	OCF, SCF	OCF, SCF	OCF, SCF
6. Motor rating	Designed for rated voltage and current	Designed for rated voltage and current	Designed for double the rated current	Designed for rated voltage and current
7. Auxiliary components	No	Buck converter + 3switches + 1 fault protective leg	Buck converter + 1 SPDT switch + 1 fault protective leg	2 DPDT relays

Table 2.4: Cost Evaluation of Fault-Tolerant Drive Configuration (Indian Rs.)

Name of the equipment		Each unit cost (Rs./-)	No. of quantities	Total Cost (Rs./-)
(a) Motor (96 V, 3 KW BLDC motor)		31,780	1	31,780
(b) Cost of li-ion battery (12V, 60AH,720WH)		13,620	8	1,08,960
(c) Cost of Inverter with driver (with switch voltage and current safety factor taken as 2)	(c_1) Cost of OEWBLDC motor inverter topology with driver	(64+306)	12	4,440
	(c_2) Cost of conventional VSI topology with driver	(159+306)	6	2,790
(d) Sensors	(d_1) Current sensor	1,870	2	3,740
	(d_2) Voltage sensor components (ISO124, TL084CN)	(894 + 13)	ISO124→6 TL084CN→2	5,390
(e) Auxiliary components (DPDT Relays)		806	2	1,612
Percentage of additional cost incurred with respect to the conventional BLDC motor drive : $=\left(\frac{d_2+e+(c_1-c_2)+d1}{a+b+c_2}\right)$ *100% = $=\left[\frac{5390+1612+1650+3740}{31781+108960+2790}\right]$ * 100% = 8.63% ≈ 9%				

2.9 Summary

Exploiting the structural symmetry of the power circuit configuration, this chapter shows that fault-tolerant capabilities can be imparted to the OEWBLDC motor drive against both open-circuited as well as the short-circuited faults. This chapter proposes simple algorithms to diagnose these two faults for the OEWBLDC motor drives. The scheme to diagnose the SC fault is based on the fact that there exists a natural gap of sixty electrical degrees in a BLDC motor drive between the turn-off and turn-on times of the switching devices of any given phase leg. This observation paves the way to devise a diagnostic scheme, which is based on the sensing of the line voltages of the open-end winding BLDC motor. This scheme ensures that the fault is diagnosed before it can cause over currents through the switching devices. The SC fault is sensed with simple and easily available components, without compromising on the issues of electrical isolation and bandwidth. The OEWBLDC motor drive can be operated at reduced power following either of these two faults. This feature enhances the reliability of the drive. It is shown that the speed of the drive is controlled at a constant value following either OC fault or SC fault if it is intended to run the drive below half of its rated speed. A simple method of reconfiguring the power circuit is described in this chapter, wherein the faulted inverter is reconnected to provide a switched neutral point. The charge available in the healthy battery bank connected to the faulted inverter is also utilized in the proposed drive. The cost analyses reveal that, compared to the conventional BLDC motor drives, the proposed fault-tolerant systems incur a low additional raw material cost for imparting the feature of fault tolerance. The performance of the proposed fault-tolerant drive topology is verified using both simulation and experimental studies.

Chapter 3

An Open-End Winding BLDC Motor Drive for Low-Power EV Applications with Rated Post-Fault Output Power

Chapter 3

An Open-End Winding BLDC Motor Drive for Low-Power EV Applications with Rated Post-Fault Output Power

3.1 Introduction

The advantages offered by the OEWBLDC motor from the standpoint of fault tolerance have been reported for multi-phase operated drive configurations [61-67], multi-phase single-sided matrix converters [68], and MSCMG gyro drives [73].

The topology proposed in Chapter-2 exploits the advantage of the OEWBLDC motor drive configuration for the fault tolerance operation in EV applications. In the work presented in Chapter-2, a dynamically reconfigurable dual-inverter fed OEWBLDC motor drive is proposed. The proposed drive configuration is capable of handling a single OC/SC fault in any of the switching devices. Chapter-2 also proposes a post-fault circuit reconfiguration strategy, wherein the healthy battery, which is connected to the faulty inverter, is reconnected in *parallel* to the battery feeding the healthy inverter with the aid of two DPDT relays. Also, a switched neutral point is created with the remaining healthy switching devices present in the faulty inverter. While such a reconnection succeeds in utilizing the charge available in the healthy battery connected to the faulty inverter, the maximum deliverable power (and consequently the maximum deliverable speed) is reduced by 50% compared to its pre-fault value.

This Chapter proposes a dual-inverter fed OEWBLDC motor drive for low power EVs, which displays an improvised fault tolerance with reasonable switch utilization and a marginal hike in the raw material cost. In this drive, open-ended stator windings of a BLDC motor are fed with two two-level VSIs from either side. These two VSIs are powered by two individual isolated battery banks of equal voltages. It is shown that, with the aid of appropriate switchgear and the higher voltage ratings of the switching devices, it is possible to retain the full power (at rated voltage) delivering capability of the drive even under the faulty condition. This means that neither torque nor speed is compromised even in the faulted condition. Furthermore, this drive topology can handle the OCF as well as the SCF in any switching device belonging to

the dual-inverter system. This Chapter also presents a strategy to prevent a false positive assertion of OCF during dynamic operations of the drive. When the dual-inverter system is healthy, each power device blocks only half of its rated voltage. This would improve the reliability of the drive, as the switching devices display a lesser propensity to fail.

The behaviour of the OEWBLDC drive is first assessed with the aid of simulation studies. Experimental results, obtained with a laboratory prototype, validate the simulation results and prove the effectiveness of the proposed post-fault reconfiguration technique.

3.2 Proposed Fault-Tolerant Drive Configuration

Fig. 3.1 shows the proposed dual-inverter fed OEWBLDC motor drive configuration, which can tolerate the OC/SC fault in any one of the switches in the dual-inverters. The two VSIs are fed with two respective isolated DC supplies (batteries 'B_1' and 'B_2'). Each battery is of voltage ('$V_{DC}/2$'), where 'V_{DC}' denotes the rated voltage needed to power the conventional BLDC drive (wherein the motor windings are star-connected). Each side of the open-ended motor is connected to its respective battery bank through DPDT relays (DPDT-1, 2, 3 & 4) and actuators as shown in Fig. 3.1. From Fig. 3.1, it may be noted that the two DC supplies (each voltage '$V_{DC}/2$') are connected to the dual-inverter configuration using 4 DPDT relays. Under normal conditions, the controlling coils of these DPDT relays are not energized; they are energized only under emergency (i.e. fault) situations. Hence their poles are connected to the 'Normally Closed' (NC) terminals. These relays may also be replaced with 'routing' triacs as in the work reported in [72]. However, in such a scenario, these triacs would be prone to the OC/SC faults for which there is no fall-back.

The gating signals for the inverters are determined by the position of the rotor, which is sensed by the Hall-Effect sensors. The Back-EMFs developed in the motor phases and the corresponding gating signals of dual-inverter configuration are shown in Fig. 2.2. Similar to the conventional Brushless DC Motor drive, there exist six sectors of operation (represented as Sector-1 to Sector-6).

Fig. 3.2 shows the basic operating principle of the proposed drive configuration. Under healthy conditions, both inverters are active and feed the OEWBLDC motor from either side. Whenever a fault occurs (either an OCF or an SCF), the faulty inverter, through an appropriate switching action, provides a switched neutral point at the faulty end. The healthy inverter,

which is now solely operative, is constrained to power the motor. Thus, to be able to supply the rated power to the motor during the post-fault operation, the following conditions must be satisfied: (i) the battery banks supplying the respective VSIs must be connected in series, so that the rated voltage can be applied to the motor, and (ii) the power semiconductor switching devices of both VSIs should be capable of blocking the total voltage ('V_{DC}'), which is the sum of the voltages of the battery banks 'B_1' and 'B_2' (i.e. twice the voltage of 'B_1' or 'B_2').

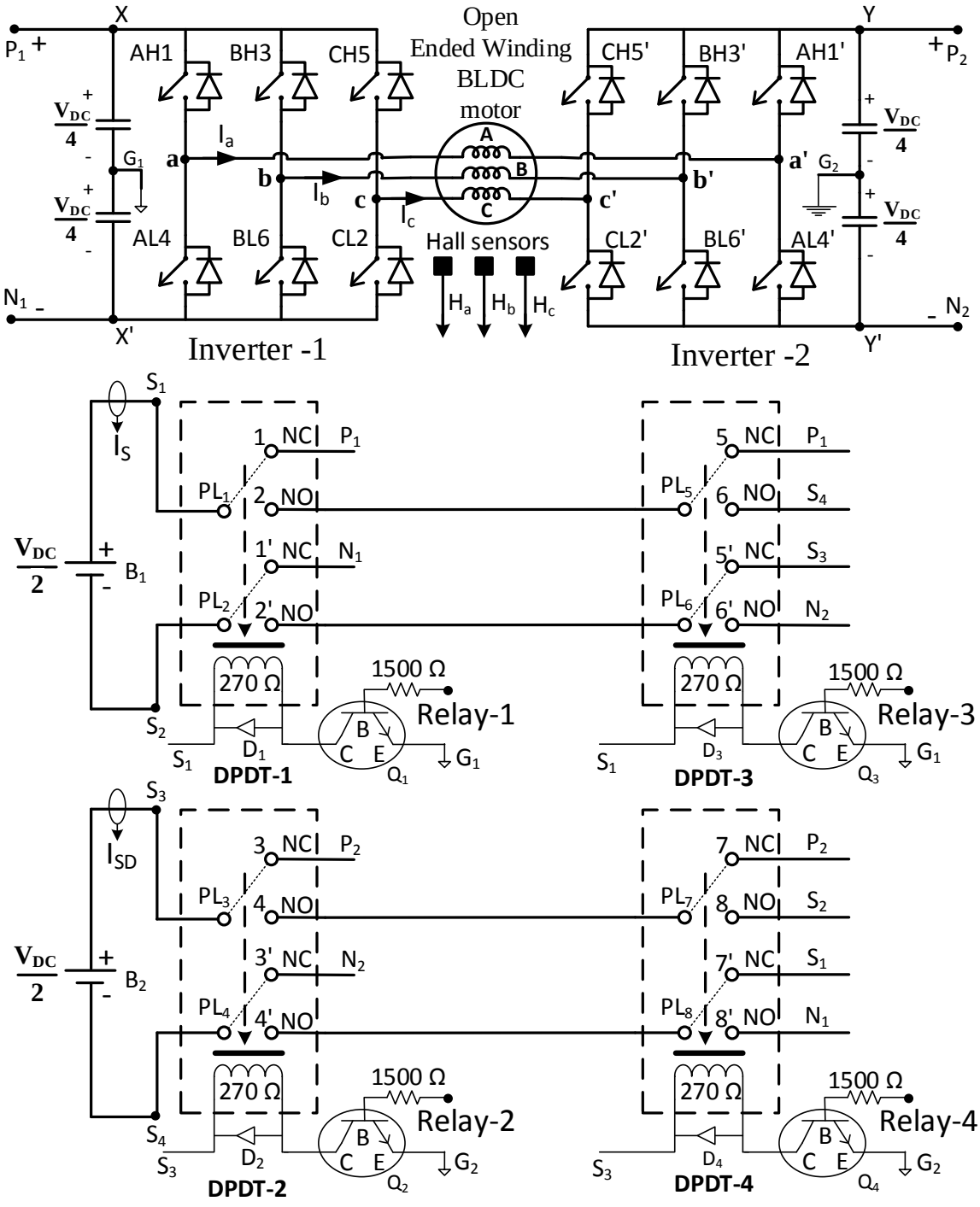


Fig. 3.1: Circuit topology of fault-tolerant OEWBLDC Motor Drive

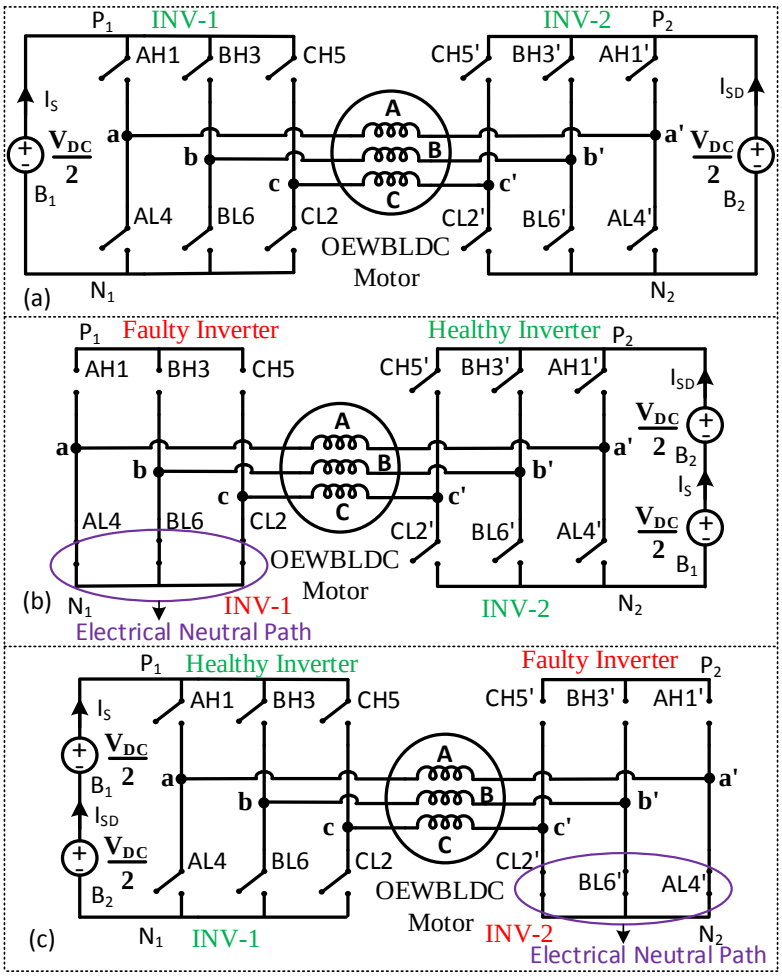


Fig. 3.2: Equivalent topological configuration for (a) steady-state operation (b) OC fault in any one of the upper switches of INV-1/ SC fault in any one of the bottom switches of INV-1 (c) OC fault in any one of the upper switches of INV-2/ SC fault in any one of the bottom switches of INV-2

Figures 3.3a and 3.3b represent the equivalent circuit diagram of the OEWBLDC drive during Sector-1 and Sector-2 operation when the drive is healthy. From Fig. 3.3a and Fig. 3.3b, it is evident that the two DC supplies are connected in series and aid each other, even though they are electrically isolated and feed individual VSIs. Figures (3.3c & 3.3d) and (3.3e & 3.3f) present the post-fault equivalent circuit of the drive when INV-1 and INV-2 develops fault (OCF/SCF) respectively. Figs. 3.3a-3.3f also provides the details regarding the actual electrical connections after the process of reconfiguration. As an example, the contents within the closing parenthesis in Fig. 3.3e, (S_1, PL_1, 2, PL_5, 5, P_1) indicate the connection sequence from the positive terminal of the battery bank 'B_1' (i.e. 'S_1') to the positive terminal of DC-link of INV-1 (i.e. 'P_1').

After diagnosing the OCF/SCF in either INV-1/ INV-2, the following reconfiguration procedure is initiated: (i) if an OCF occurs in any one of the INV-1 (INV-2) upper-bank

switching devices, the three lower-bank switches of INV-1 (INV-2) are turned on continuously to create a switched-neutral through 'N_1' ('N_2') (Figs. (3.2 & 3.3)). This switching action would reconfigure the OEWBLDC drive into the conventional drive, wherein the windings are connected in star and the motor is powered through INV-2 (INV-1). (ii) if an SCF occurs in one of the lower-bank devices of INV-1 (INV-2), the remaining two lower-bank switches of it are also turned on continuously to create a switched neutral point through 'N_1' ('N_2') (Fig. 3.2). The motor is now driven exclusively through INV-2 (INV-1) to achieve the required fault-tolerant operation.

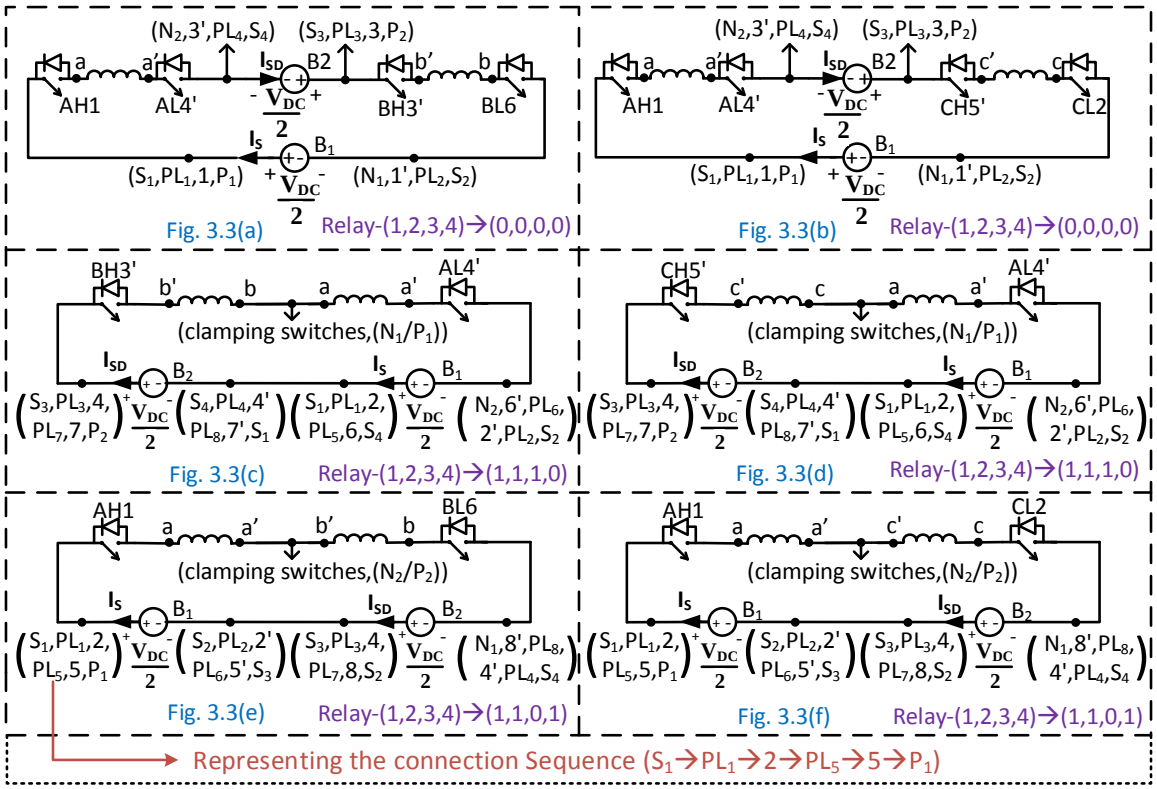


Fig. 3.3: Equivalent circuit diagram of the OEWBLDC motor drive during: (a) Sector-1, steady state operation; (b) Sector-2, steady operation; (c) Sector-1, INV-1 faulty condition (OCF/SCF); (d) Sector-2, INV-1 faulty condition (OCF/SCF); (e) Sector-1, INV-2 faulty condition (OCF/SCF); (f) Sector-2, INV-2 faulty condition (OCF/SCF)

However, this partial reconfiguration isolates the healthy battery bank, which is located on the side of the faulty inverter, from the rest of the system and renders it unusable. To make better use of the healthy battery bank, an improvised reconnection procedure is employed in this chapter, wherein the healthy battery bank of the faulty inverter is connected *in series* to its counterpart by turning on the appropriate DPDT relays.

Figs. 3.3c & 3.3d (Figs. 3.3e & 3.3f) respectively represent the equivalent circuits and connection sequence of the drive when OCF/SCF are diagnosed in INV-1 (INV-2) and the subsequent reconfiguration when the drive goes through the regions of Sector-1 and Sector-2. From these diagrams, it can be noticed that the two battery banks are connected in series and aid each other while driving the motor. Thus, the drive may be operated with full rated power and torque even under the faulty condition, as rated motor voltage can be applied to the motor.

Table-3.1 presents the strategy of energizing the DPDT relays (Relay-1 to Relay-4, Fig. 3.1) during the 'normal' as well as the 'faulty' modes of operation. As an example, after the fault (OCF/SCF) diagnosis and corresponding reconfiguration procedure for the fault in INV-1, to utilize the healthy battery connected to the faulty inverter, the control windings of the DPDT relays Relay-1, Relay-2 and Relay-3 are energized, so that their poles are connected to the Normally Open (NO) terminals. (Refer Table-3.1 & Fig. 3.1). It may be noted that, with this manoeuvre, the batteries are connected in series (aiding each other), powering the drive solely with INV-2 (Figs. 3.2, 3.3c & 3.3d). Thus, the proposed OEWBLDC drive achieves the fault-tolerant operation with the ability to deliver the rated power and the rated torque.

Table 3.1: Relay Energizing Signals and Diagnostic Information during Steady and Faulty Operations

Drive operation	DPDT relay signals Relay-(1, 2, 3, 4)	Electrical neutral path, Flags 'FINV' & ROCFD	Battery terminals connection (S_1, S_2, S_3, S_4)	Effective DC-Link voltage
Steady operation	(0, 0, 0, 0)	OEWBLDC; FINV=0;ROCFD=0	(P_1, N_1, P_2,N_2)	V_{DC}
INV-1 (OCF/SCF)	(1, 1, 1, 0)	(P1 or N1); FINV=0;ROCFD=1	(S_4, N_2, P_2, S_1)	V_{DC}
INV-2 (OCF/SCF)	(1, 1, 0, 1)	(P2 or N2); FINV=1;ROCFD=1	(P_1, S_3, S_2, N_1)	V_{DC}

3.3 Fault-Diagnosis and Control

3.3.1 Open Circuit Fault-Diagnosis algorithm and Control

Chapter-2 proposes an algorithm that is suitable to diagnose the OCF for an OEWBLDC drive. However, this algorithm shows a tendency for false-positive detection during dynamic operations of the drive. This shortcoming is addressed in this chapter and an improvised algorithm to diagnose the OCF is presented in this chapter.

The OCF proposed in Chapter-2 is briefly outlined as follows:

i) The OCF diagnosis algorithm is based on the observation that if any single device develops a fault, it would miss conduction during those sectors of operation, which need the conduction of the faulty device. The DC-link current would therefore be discontinuous, which constitutes the main symptom of OCF.

ii) Since two VSIs are in action, it won't be possible to ascertain as to which is the source of OCF in an Open-winding configuration (as two devices from individual inverters are in series in any conducting phase). Thus, it is always assumed that the OCF occurs in INV-1 by default.

iii) With that assumption, a switched neutral point is formed with the supposed healthy bank of INV-1.

iv) If the discontinuity in the DC-link current of the supposedly healthy inverter (i.e.INV-2) vanishes, then it means that the default assumption regarding the location of the fault in INV-1 is correct and the post-fault circuit reconfiguration is retained.

v) On the other hand, if the discontinuity in the DC-link current of INV-2 persists, then it is obvious that the assumption regarding the location of the OCF (that it exists in INV-1) is wrong and it is asserted that it has indeed occurred in INV-2.

vi) This leads to the step of undoing the reconfiguration affected earlier. The dual-inverter system is again reconfigured, this time correctly, wherein the switched neutral point is formed with the devices situated on the healthy bank of INV-2.

vii) The limitation of this algorithm is that the OCF diagnosis is reliable during steady operating conditions.

In the process of diagnosing the OCF, some flags are employed to store essential information. These flags are examined by the fault-diagnosing algorithms from time to time to assert the occurrence of the fault. Also, these flags play a crucial role in determining inverter reconfiguration and battery re-connection. These flags are listed as follows: (a) the flag 'OCFSEC' (with initial zero value) stores the sector number at which the OCF is first affirmed; (b) the flags 'FDF1'& 'FDF2' (with initial zero value) are set to unity when the OC fault is affirmed during the current sector of operation and the subsequent sector of operation

respectively; (c) the flag 'OCFSW' (with zero initialization) is loaded with the switch number of the diagnosed OCF switch (which is taken as pilot fault affirmation in this algorithm); (d) the flag 'FINV' set to unity (after a safe time of 'T_{invchk}' after the reliable OCF diagnosis) for the faulty actuator of 'INV-2', otherwise it remains to its initial zero when the initial assumption of fault in 'INV-1' is true.

The simulation results carried out using MATLAB/SIMULINK platform with machine parameters given in Table-A.1 are used in the following sections to facilitate a clear visualization of fault-diagnosis and circuit reconfiguration. Fig. 3.4 presents the simulation results for the OCF in switch AH1 (i.e. INV-1). Figs. 3.5-3.7, which are the zoomed versions of Fig. 3.4, at instants 'ta' & 'tc', provide the finer details of the diagnostic process for the OCF. Fig. 3.8 represents the fault-diagnosis for the OC fault in switch AL4' (i.e., INV-2).

The aforementioned diagnostic process is limited to steady operating conditions and displays a propensity to raise a false positive fault affirmation, particularly during dynamic operations of the drive. This could lead to an unnecessary post-fault circuit reconfiguration, defeating the very purpose of providing fault tolerance to the drive. To avoid this false fault-diagnosis, an improvised algorithm is presented in this chapter. This improvisation is described in detail in the following paragraphs.

Following a disturbance, the DC-link current could show a temporary drop. Thereafter, it would quickly regain the steady-state condition and shows the normal behavior, wherein all the six sectors of conduction are present. However, this is not the case with OCF, wherein a failure of one switching device would lead to the presence of only four sectors of conduction (out of 6 sectors). This would lead to a periodic disruption of the DC-link current (periodic oscillations during the time 'tc-ta', Fig. 3.4). The improvisation proposed in this chapter is based on this subtle observation. The following procedure is adopted to circumvent this problem:

With the OC fault initiated in the switch 'AH1' (i.e. at instant 'ta', see in Figs. 3.4a, 3.5b & 3.6a), the corresponding flags 'OCFSEC' (i.e. at instant 'ta1', see in Fig. 3.6d), 'FDF1' (i.e. at instant 'ta1', see in Fig. 3.6c), 'FDF2' (i.e. at instant 'ta2', see in Fig. 3.6f) are loaded with the diagnostic information. Based on these flags information, the flag 'OCFSW' (from Table-3.2) is loaded with the faulty switch number during pilot-fault affirmation stage (i.e. with '1' at instant 'tb', see in Figs. 3.4b & 3.5c).

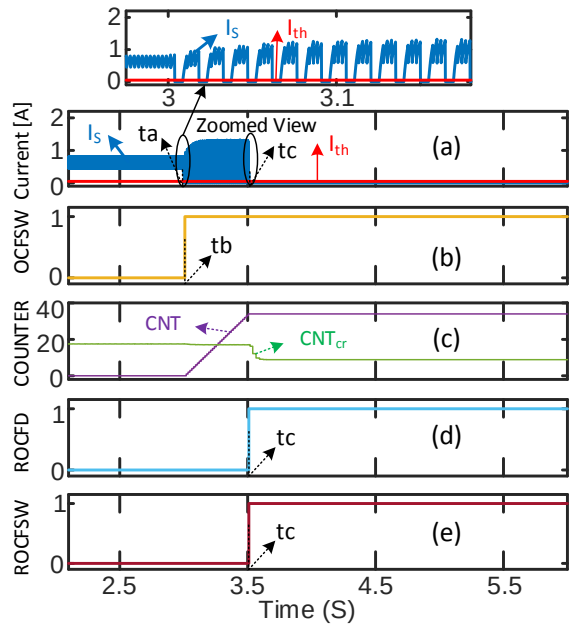


Fig. 3.4: Simulation results showing OC fault in switch AH1 of INV-1: (a) I_S, I_{th} (b) OCFSW (c) Counter (d) ROCFD (e) ROCFSW

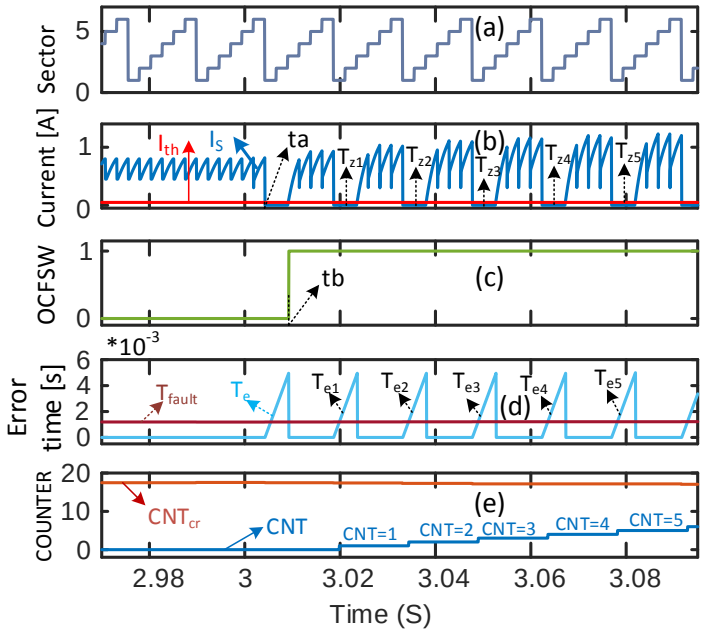


Fig. 3.5: Simulation results showing OC fault in switch AH1 of INV-1 (detailed fault-diagnosis at instant 'ta' of Fig. 3.4): (a) Operating Sector (b) I_S, I_{th} (c) OCFSW (d) T_e, T_{fault} (e) Counter

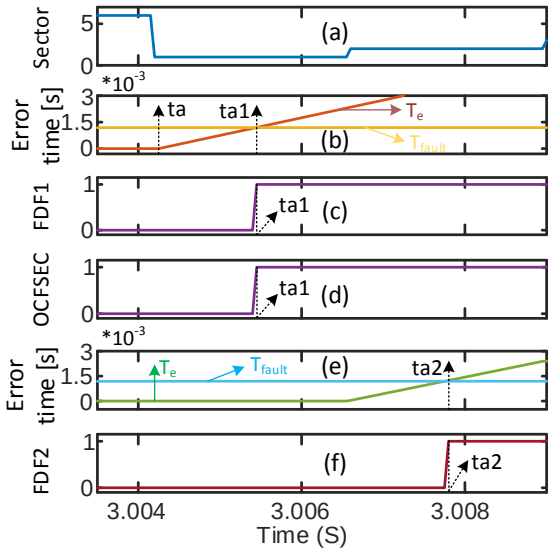


Fig. 3.6: Simulation Results showing flags statuses for OCF in switch AH1 of INV-1 (detailed fault-diagnosis at instant 'ta' of Fig. 3.4): (a) Operating Sector (b) T_e, T_{fault} (Sector-1) (c) FDF1 (d) OCFSEC (e) T_e, T_{fault} (Sector-2) (f) FDF2

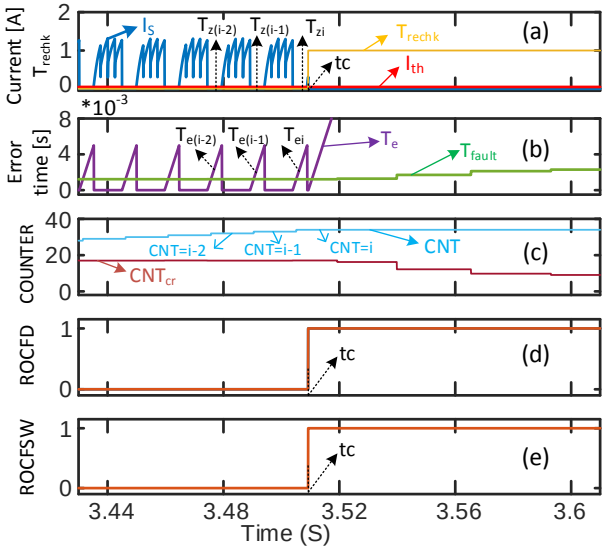


Fig. 3.7: Simulation results showing OC fault in switch AH1 of INV-1 (detailed fault-diagnosis at instant 'tc' of Fig. 3.4): (a) I_S, I_{th}, T_{rechk} (b) T_e, T_{fault} (c) Counter (d) ROCFD (e) ROCFSW

After the pilot-fault affirmation stage, to assert the occurrence of the OCF conclusively, the probation period of the fault is extended by a period of 'T_{rechk}'. If the occurrence of OCF is real, the DC link current drops below a threshold value 'I_{th}' in '2' sectors out of total '6' sectors (see Fig. 2.2) in every electrical cycle of operation (see Figs. 3.4a, 3.5b & 3.7a) during this 'T_{rechk}' time ('T_{rechk}=tc-tb'). These zero transitions of DC link current in every electrical cycle are denoted as 'T_{z1}', 'T_{z2}', …, '$T_{z(i-1)}$', 'T_{zi}' (see Figs. 3.5b & 3.7a). The corresponding error-time-periods 'T_{e1}', 'T_{e2}', …, '$T_{e(i-1)}$', 'T_{ei}' (see Figs. 3.5d & 3.7b) for which

these zero transitions (T_{z1}, T_{z2}, …,$T_{z(i-1)}$, T_{zi}) existed are calculated. The error-time-period '$T_{ex}(n)$' is an integrator that is accumulated (see eq. (3.1)) with the same rate at which the current is sampled. In the present work, a sampling time (T_s) of 70μS is employed to sense the DC-link currents.

$$\begin{cases} I_S < I_{th} & (T_{ex}(n) = T_{ex}(n-1) + T_s) \text{ for } T_{zx}(n), \\ I_S \geq I_{th} & \text{steady condition and } T_{ex}(n) = 0 \end{cases} \tag{3.1}$$

$$I_{th} = R_f * I_{ref} \tag{3.2}$$

Where x=1, 2… i; 'I_{ref}' is the reference current which is the output of the current controller (Fig. 3.10); 'R_f' is the safety factor (0.5 considered); $T_{ex}(-1)=0$.

An error-up-counter 'CNT' (with an initial value of zero) is triggered at 'tb', which starts counting (within the probation time period) whenever the zero transitions of DC link current 'I_S' ('T_{z1}', 'T_{z2}', …, '$T_{z(i-1)}$', 'T_{zi}'; see Figs. 3.5b & 3.7) are identified and existed more than the critical-time-period 'T_{fault}'. When the number of these zero-transitions (stored in 'CNT') is above a critical value, denoted by 'CNT_{cr}' (which is determined by the speed of the motor), the OCF is conclusively affirmed.

The critical period (denoted as 'T_{fault}') is determined by the dwell-time period corresponding to two sectors (i.e.120 electrical degrees, see Fig. 2.2). It depends on the speed of the motor and is calculated based on the set of relationships presented below:

The critical-time-period 'T_{fault}' is given as:

$$T_{fault} = S_f * 2 * T_{sector} \tag{3.3}$$

From eqs. (2.7) & (3.3)

$$T_{fault} = \frac{S_f * 8 * \pi}{P * \omega_{me} * 6} \tag{3.4}$$

Where, 'S_f' denotes the factor of sensitivity ($0<S_f<1$), which is a design parameter. In the present work, a value of 0.6 is chosen for 'S_f'.

The critical-count value 'CNT_{cr}' depends on the electrical time cycle 't_{el}' of the drive and the probation time employed for re-check (i.e. 'T_{rechk}'). The electrical time cycle 't_{el}' in turn depends on the running speed of the drive 'ω_{me}'.

The number of electrical time cycles 'CNT_{rechk}' within the time 'T_{rechk}' is given as:

$$CNT_{rechk} = \frac{T_{rechk}}{t_{el}} = \frac{T_{rechk} * p * \omega_{me}}{4 * \pi} \tag{3.5}$$

The critical count value 'CNT_{cr}' is given by:

$$CNT_{cr} = D_{sf} * CNT_{rechk} \tag{3.6}$$

$$CNT_{cr} = D_{sf} * \frac{T_{rechk}}{t_{el}} = D_{sf} * \frac{T_{rechk} * p * \omega_{me}}{4\pi} \tag{3.7}$$

Where 'D_{sf}' denotes the factor of safety ($0<D_{sf}<1$), which is a design parameter. In this present work, a value of 0.5 is chosen for 'D_{sf}'.

If the value accumulated in the error-up-counter 'CNT' is greater than the critical count value 'CNT_{cr}' at the end of the time period 'T_{rechk}' (at instant 'tc', see Figs. 3.4a, 3.4c & 3.7c), the flag 'ROCFD' (Re-affirmed OC fault detection) is set to a value of '1' (at instant 'tc', see Fig. 3.4d & Fig. 3.7d). If the flag 'ROCFD' is set to '1', it is finally admitted as a genuine fault.

$$\begin{cases} ROCFD = 1; & \text{if } (CNT > CNT_{cr}) \\ ROCFD = 0; & \text{Otherwise} \end{cases} \tag{3.8}$$

At this point, another flag, named Re-affirmed OCF Switch number Flag 'ROCFSW' (at instant 'tc', see Fig. 3.4e & Fig. 3.7e) is made to store the product of the contents of the flags 'OCFSW' and 'ROCFD'.

$$ROCFSW=OCFSW*ROCFD \tag{3.9}$$

The information contained in 'ROCFSW', would subsequently determine the process of post-fault circuit reconfiguration.

If the value accumulated in the error counter 'CNT' is less than the critical count value 'CNT_{cr}' at the end of the period 'T_{rechk}', then it is concluded that the OC fault is falsely diagnosed. The content of the flag 'ROCFD' is verified to arrive at this conclusion. 'ROCFD' would contain '0' after the backup test for the false diagnosis of the OC fault. Hence, all of the flags associated with the OCF (namely, 'FDF1', 'FDF2', 'OCFSEC', 'OCFSW' &'CNT') are reset to '0' again. This manoeuvre would reset the fault detecting system, which is now ready to probe a new OCF. The decision regarding the reconfiguration of the power circuit is also

based on the status of this flag ('ROCFD'). Circuit reconfiguration is affected only when this flag is set to '1'.

Fig. 3.8 represents the diagnosis procedure for the OCF in switch AL4' of INV-2 (i.e. at instant 'ta', see Fig. 3.8a). With the initial assumption of OC fault in INV-1, the switch number of AH1 (which is in series with AL4', see Figs. 3.3a & 3.3b) is stored in the flag 'ROCFSW' (at instant 'tc', see Fig. 3.8d). As the initial assumption of fault in INV-1 is false, the periodic transitions in the current are now correctly attributed to the development of OCF in INV-2. Subsequently, the flags 'FINV' is set to '1', and 'ROCFSW' is loaded with the number corresponding to the actual switch (AL4' in this case) in which the OCF has occurred (at the instant 'td', see Fig. 3.8d) after a safe period of 'T_{invchk}'.

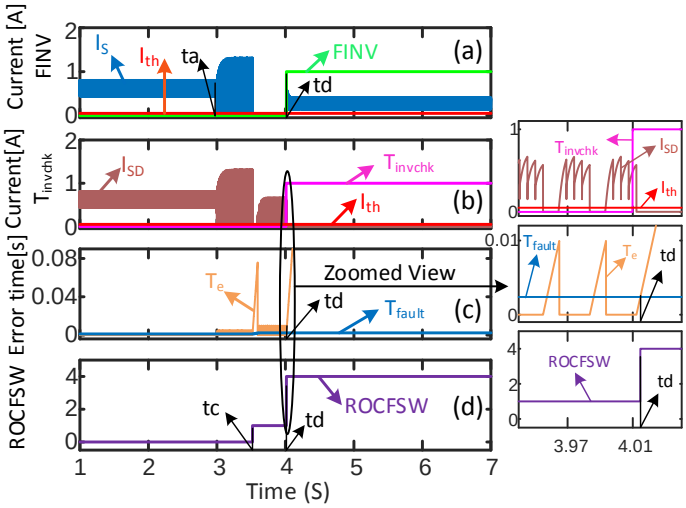


Fig. 3.8: Simulation results showing OC fault in switch AL4' of INV-2: (a) I_S, I_{th}, FINV (b) I_{SD}, I_{th}, T_{invchk} (c) T_e, T_{fault} (d) ROCFSW ((Left side: Normal view, Right side- Zoomed-view of the portion encircled)

Table-3.2 summarizes the possible OC failure in all the switches of the dual inverter configuration and also the corresponding clamping switches information required for the reconfiguration procedure based on the flags 'FDF1', 'FDF2', 'OCFSEC', 'FINV', and 'ROCFD'.

As mentioned in section-3.2, after creating a switched neutral point with the remaining healthy devices belonging to the faulty inverter, the two battery banks 'B_1' and 'B_2' are connected in series. As one may expect, the flags 'FINV' & 'ROCFD' plays a pivotal role in energizing the required set of relays. The safe battery reconnection flag 'T_{drelay}' is set to '1' by noticing the active high changeover of 'ROCFD' flag. Table-3.1 presents the relationship

between the flags ('FINV' & 'ROCFD') and the relays that are energized (using 'Relay-1/2/3/4' signals, see Fig. 3.1).

Table 3.2: OC Fault-Diagnosis Information

(FDF1,FDF2,OCFSEC)	FINV	OCFSW	Clamping switches (ROCFD=1)
(1,1,1) or (1,0,2)	0	AH1	AL4,BL6,CL2
	1	AL4'	AH1',BH3',CH5'
(1,1,3) or (1,0,4)	0	BH3	AL4,BL6,CL2
	1	BL6'	AH1',BH3',CH5'
(1,1,5) or (1,0,6)	0	CH5	AL4,BL6,CL2
	1	CL2'	AH1',BH3',CH5'
(1,1,4) or (1,0,5)	0	AL4	AH1,BH3,CH5
	1	AH1'	AL4',BL6',CL2'
(1,1,6) or (1,0,1)	0	BL6	AH1,BH3,CH5
	1	BH3'	AL4',BL6',CL2'
(1,1,2) or (1,0,3)	0	CL2	AH1,BH3,CH5
	1	CH5'	AL4',BL6',CL2'

The performance of the proposed diagnosis algorithms is experimentally verified with both open-loop and closed-loop operation of the drive. The closed-loop operation of the drive is based on the classical structure, wherein the outer speed loop specifies the reference for the inner current loop. Fig. 3.9 presents the overall control scheme, including the generation of the gating signals needed for the switching devices of the dual-inverter scheme for both healthy and faulty conditions. Fig. 3.10 represents the overall flowchart representation of diagnosis, reconfiguration and reconnection strategies required for the fault-tolerant operation.

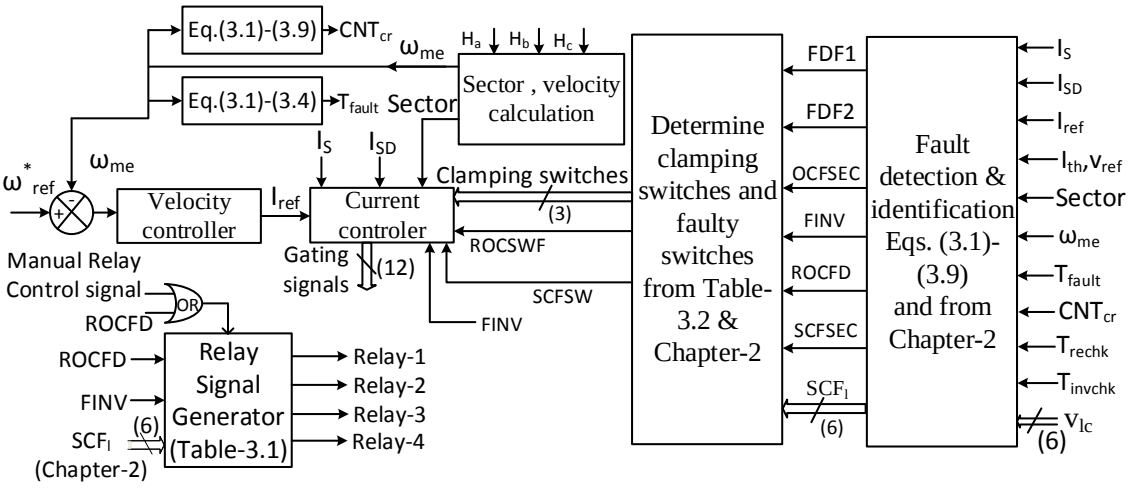


Fig. 3.9: Overall control scheme under healthy and faulty operations

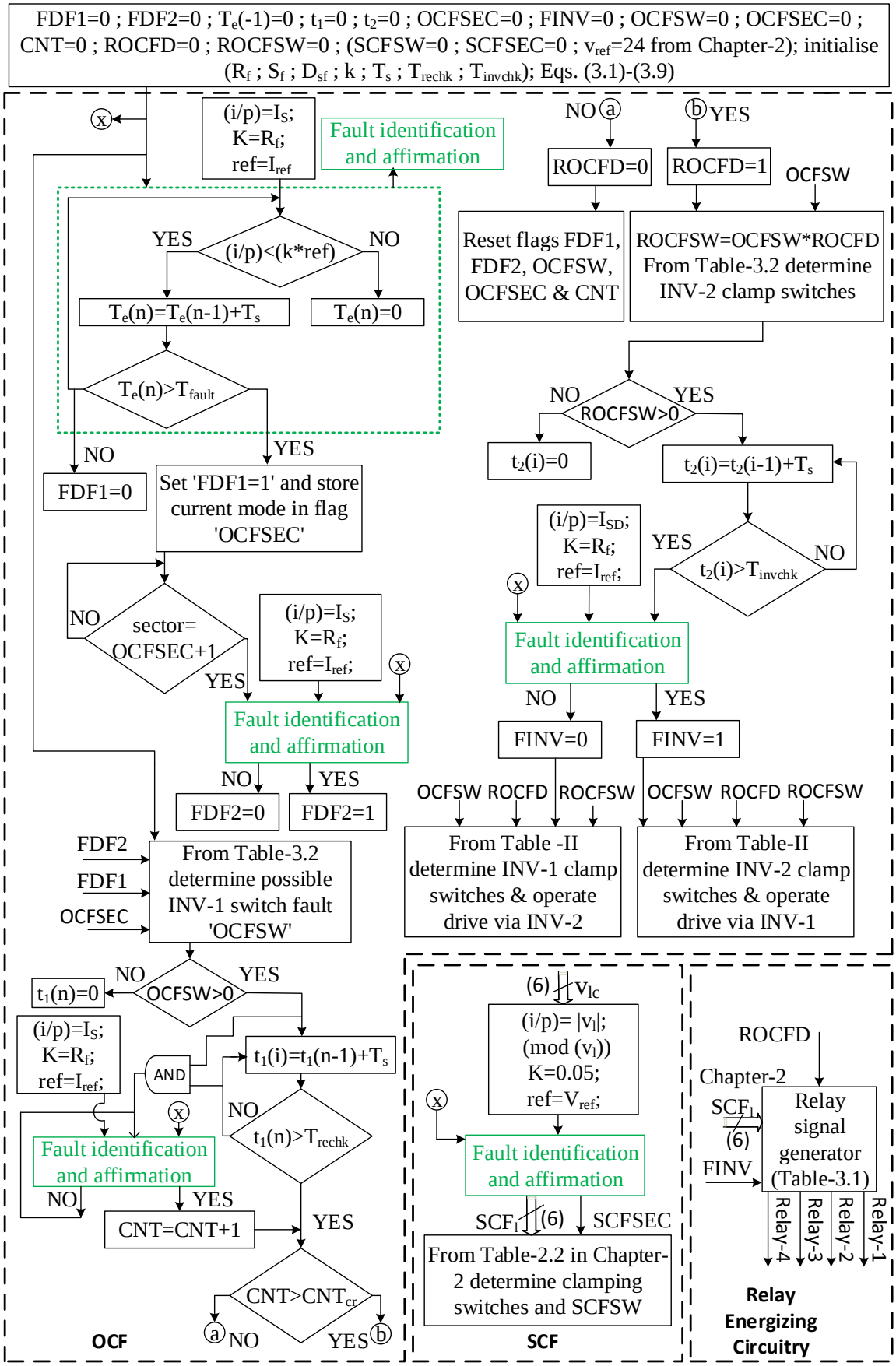


Fig. 3.10: Flowchart presenting the overall fault-tolerant operation during fault conditions

3.3.2 Short Circuit Fault-Diagnosis algorithm and Control

For the diagnosis of the SCF, the OEWBLDC motor drive proposed in this chapter also employs the same algorithm, which is developed in Chapter-2. To facilitate a ready reference, it is briefly redescribed in the following paragraph.

To make the design cost-effective, low-cost analog voltage sensors (based on the ISO-124 device) have been employed without losing bandwidth and isolation. The technique of diagnosing the SCF is based on the periodic sensing of all of the six line-line voltages, which appear across the six terminals of an open-stator winding motor. This technique is based on the observation that, for any given phase leg of a BLDC motor, there exists an interval of 60 degrees (electrical) between turning off the top switch of a given phase leg and turning on the bottom one. This technique, which is essentially anticipatory, manages to prevent the over-currents associated with the shoot-through of the two devices (one of which develops the SCF) belonging to a given phase-leg, before its occurrence (Chapter-2). With the proposed topology and the reconfiguration procedure (inverter reconfiguration & battery reconnection) mentioned in section-3.2, the drive is capable of delivering full rated power (speed) and torque for the SCF occurrence in either of the dual-inverter configuration.

3.4 Results and Discussion

Fig. A.1 shows the prototype developed for the experimental studies for the proposed fault-tolerant OEWBLDC motor drive configuration. The dSPACE-1104 control platform is used for the experimental validation. The machine parameters used for simulation as well as hardware prototype are presented in Table-A.1.

The diagnosis of OCF in INV-1 & INV-2 is validated by considering the switches CH5 and CL2' respectively. The capability of the proposed fault-diagnosis algorithms as well as the post-fault circuit reconfiguration strategy is demonstrated experimentally in terms of achieving the rated post-fault power and speed in both open-loop as well as closed-loop drive operations.

Figs. 3.11 & 3.12 show the process of diagnosing the OC fault occurring in a switching device belonging to INV-1 under open-loop drive operation. Whenever an OCF occurs in the switch CH5 of INV-1 (at instant 'tf', Fig. 3.11), the DC-link currents of both of the VSIs drop below the threshold value (at the instant 'ta', Figs. 3.11 & 3.13). Subsequently, the internal

flags 'FDF1', 'OCFSEC' & 'FDF2' (at the instants 'ta1', 'ta1' & 'ta2', see Fig. 3.11) are loaded with values (1, 5 & 1). Depending on the values of these flags, the switch, in which the OCF has occurred, is identified and the corresponding number is loaded into the flag 'OCFSW' (i.e. 'OCFSW=5' at instant 'tb', shown in Figs. 3.11, 3.12 & 3.13). Completion of these activities marks the end of the 'pilot-sensing' of the fault.

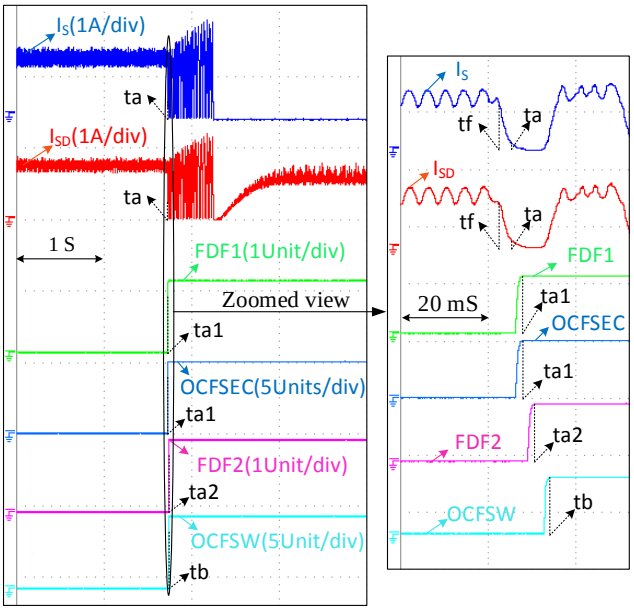


Fig. 3.11: Experimental results showing the flag statuses for the OCF in INV-1 (i.e. switch CH5) (Left side: Normal view, Right side: Zoomed-view of the portion encircled)

The confirmation of OCF is based on the multiple zero-transitions (Figs. 3.11, 3.12 & 3.13) counted during the probationary period 'T_{rechk}'. It may be noted from Fig. 3.13 that, when the probing counter 'CNT' accumulates a higher value than the critical count 'CNT_{cr}' (see CNT, CNT_{cr} of Fig. 3.12), the flags 'ROCFD' and 'ROCFSW' (eq. (3.9)) are respectively set to '1' and '5' (at the instant 'tc', Fig. 3.13). This action confirms the occurrence of the OCF, which triggers the reconfiguration of the faulted inverter as explained in Section-3.2. Consequently, the current of the battery 'B_1' (i.e. 'I_S') drops down to zero, and the motor is now exclusively powered by the battery 'B_2' through INV-2, causing a decrease in the speed of the motor (Fig. 3.13).

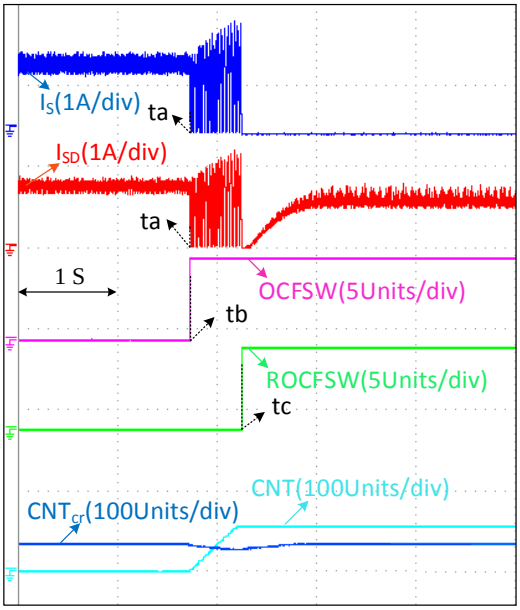


Fig. 3.12: Experimental results showing the counter and flag statuses for the OCF in INV-1 (i.e. switch CH5)

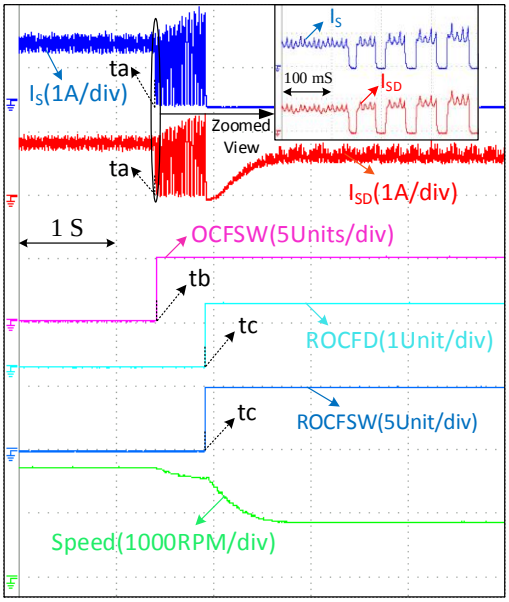


Fig. 3.13: Experimental results showing the fault-diagnosis and reconfiguration for the OCF in INV-1 (i.e. switch CH5) under open-loop operation without battery reconnection

Fig. 3.14 shows the fault-diagnosis and the dynamic behavior of the drive (operated in open-loop) when the OCF occurs in INV-2 (i.e. switch CL2'). As the algorithm for the diagnosis of OCF initially assumes that the fault occurs in INV-1, the diagnosis procedure determines the faulty switch as 'CH5', belonging to INV-1. This is indicated by the fact that the flag 'ROCFSW' showing a value of '5' at the instant 'tc' in Fig. 3.14. Consequently, the reconfiguration process is initiated and the motor is powered exclusively through INV-2. The fault-diagnosis algorithm now notices that, despite this reconfiguration, the periodic

discontinuity in the current 'I_{SD}' doesn't vanish. It obviously means that, contrary to the initial assumption, INV-2 has developed the fault. Hence, the flag 'ROCFSW' is overwritten with a value of '2' (at the instant 'td', Fig. 3.14), indicating that the switch CL2' (belonging to INV-2) has indeed developed the OCF. Thereafter, the switched neutral point is created with the switches AH1', BH3' and CH5' belonging to INV-2 and the motor is powered exclusively through INV-1, employing the battery 'B_1' (Figs. 3.3e & 3.3f).

From Fig. 3.13 & Fig. 3.14, it may be noted that the speed of the motor is reduced after the post-fault reconfiguration. This is due to the fact that, only one battery is now operative, with a voltage of '$V_{DC}/2$', and the drive is running in open loop.

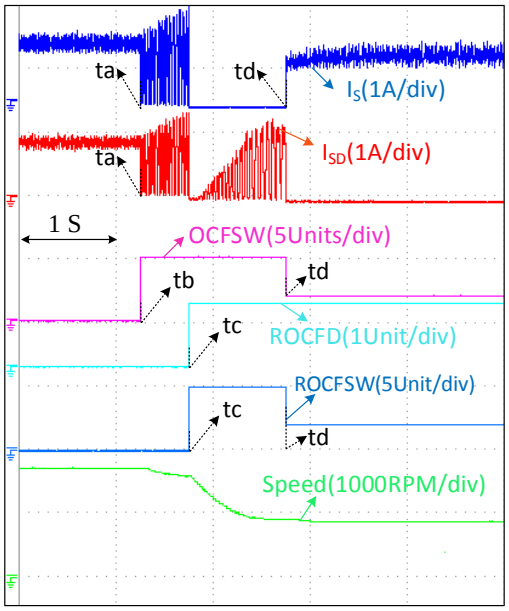


Fig. 3.14: Experimental results showing the fault-diagnosis and reconfiguration for the OCF in INV-2 (i.e. switch CL2') under open-loop operation without battery reconnection

The experimental results pertaining to the closed-loop operation are shown in Fig. 3.15 and Fig. 3.16. In the first experiment (see Fig. 3.15), the reference speed is set at 1500 rpm, which is less than half of the rated speed of the BLDC motor. When an OCF occurs in INV-1, the motor is fed exclusively through INV-2. It should be noted that, the speed is restored back to the reference value (see Fig. 3.15), even without the battery ('B_1') reconnection (i.e. T_{drelay}=0 in Fig. 3.15), This is due to the fact that, the regulated speed is below half of the rated value of the motor and it can be regulated even without the aid of the battery 'B_1'. In contrast, when the reference speed is higher than half of the rated value (i.e. 2800RPM, Fig. 3.16), to regulate the speed, it would be mandatory to reconnect the healthy battery ('B_1' in the present

case) to aid the battery, which is already present in the post-fault circuit ('B_2' in the present case). Hence, from the experimental result (Fig. 3.16), it can be noted that with the inverter reconfiguration alone (without battery reconnection (i.e. 'T_{drelay}=0' in Fig. 3.16)), the speed of the motor cannot reach its reference value which is above half of the rated speed.

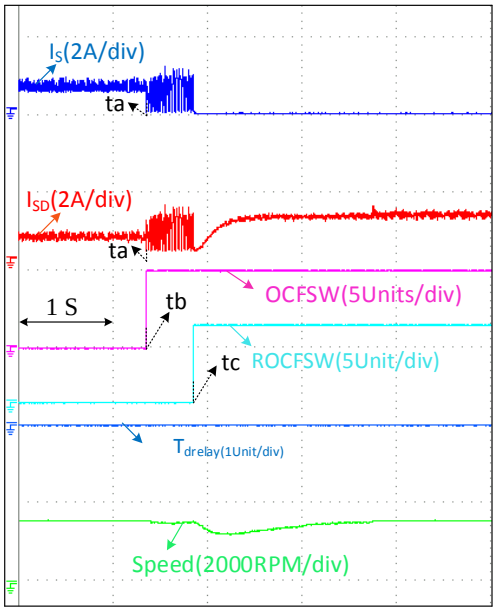


Fig. 3.15: Experimental results showing the fault-diagnosis and reconfiguration for the OCF in INV-1 (i.e. switch CH5) under closed-loop drive operation (below half the rated speed) without battery reconnection

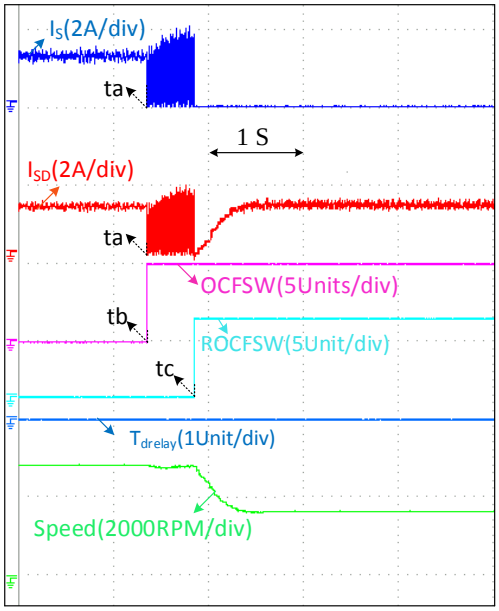


Fig. 3.16: Experimental results showing the fault-diagnosis and reconfiguration for the OCF in INV-1 (i.e. switch CH5) under closed-loop drive operation (above half the rated speed) without battery reconnection

Fig. 3.17 presents the effectiveness of the post-fault reconnection of the batteries (T_{drelay}=1 at instant 'tr', Fig. 3.17) in series for the open-loop drive operation. In contrast to the

results presented in Fig. 3.13 and Fig. 3.14 (wherein the healthy battery corresponding to the faulty inverter is not connected), it may be noted that the speed of the motor is restored back, even after the occurrence of the OCF in INV-1 under open-loop drive operation. But if the source disturbance is applied at instance 'tsd', the speed falls to a new operating value due to the open-loop operation of the motor.

The performance of the drive system with closed-loop control with the battery reconnection (T_{drelay}=1 at instant 'tr', Fig. 3.18) is demonstrated in Fig. 3.18. In this experiment, the drive is operated with a speed, which is more than half of the rated speed of the motor (2800 RPM). It is important to note that, in contrast to the magnitude of the motor speed shown in Fig. 3.16 (i.e. with inverter reconfiguration alone), the pre-fault speed and power are achieved with the aid of the proposed method of reconnecting the batteries in series. Compared to the open-loop experimental result presented in Fig.3.17, the drive is capable of regulating the speed against the supply disturbance applied at instant 'tsd'. This demonstrates the general capability of the drive for fault tolerance operation, even though the speed control (with speed loop) is not generally required in EV applications.

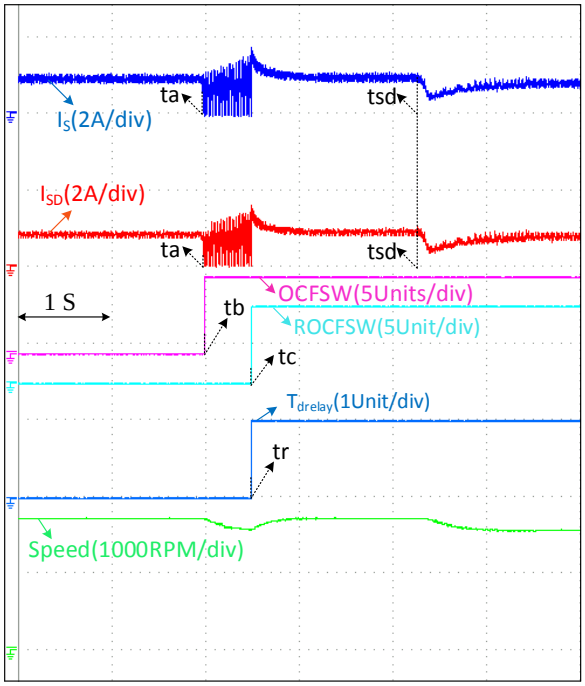


Fig. 3.17: Fault tolerance (diagnosis and control) of the drive configuration for the OCF in INV-1 (i.e. switch CH5) under open-loop drive operation with battery reconnection

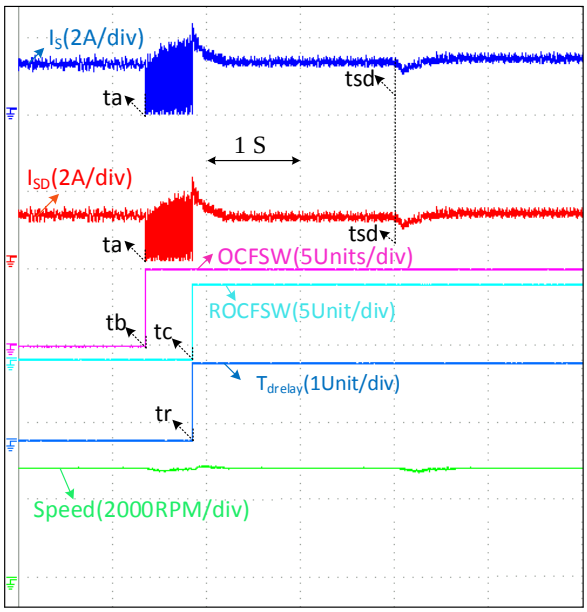


Fig. 3.18: Fault tolerance (diagnosis and control) of the drive configuration for the OCF in INV-1 (i.e. switch CH5) under closed-loop drive operation (above half the rated speed) with battery reconnection

The fault-tolerant performance of the proposed OEWBLDC drive is also assessed against the SCF when it is operated in an open loop (shown in Fig. 3.19). For this purpose, an SCF is created by continuously gating the device 'AL4', belonging to INV-1. With the proposed post-fault reconfiguration strategy, it is possible to retain the full power delivering capability, which is not the case for the post-fault reconfiguration mentioned in Chapter-2.

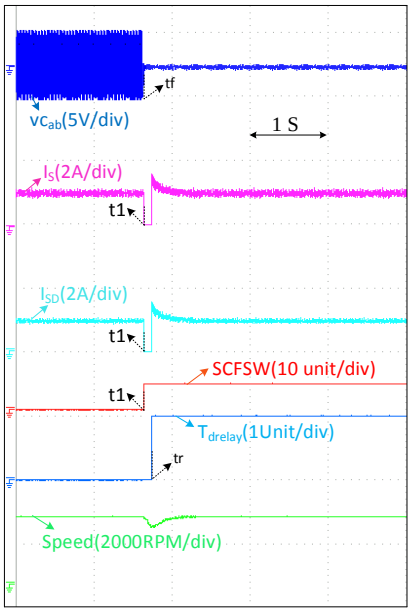


Fig. 3.19: Fault tolerance of the drive configuration for the SCF in INV-1 (i.e. switch AL4) under the open-loop drive operation

Thus, the proposed post-fault reconfiguration achieves 100% fault tolerance, for both OCF and SCF (i.e. without compromising on the power rating). Admittedly, this feature could be realized because of the selection of the voltage ratings of the switching devices, which are rated for a voltage of 'V_{DC}', compared to the rating of '$V_{DC}/2$', employed in the work proposed in Chapter-2. It would be an interesting proposition to assess as to what would be the increase in the raw material cost (RMC) to implement this feature compared to the work presented in Chapter-2 (given in section-3.5).

3.5 Feasibility Analysis of the Proposed Electric Drive Topology

Table-3.3 presents the comparison of the proposed fault-tolerant topology and the corresponding fault-diagnosis algorithm vis-à-vis the fault-tolerant topologies and fault-diagnosis algorithms, which have been reported in earlier literature.

Table 3.3: Comparison of Different Topologies with the Proposed Topology

Topological features	Topology [70]	Topology [72]	Topology [73]	Proposed Topology
1. No. of switches in the inverter	6 switches (VSI) + 3 TRIACs	6 switches (VSI) + 6 TRIACs + 1 additional leg	12 switches	12 switches
2. Switch ratings	Rated motor voltage and current	Rated motor voltage and current	Rated motor voltage and twice the rated motor current	Rated motor voltage and current
3. Fault-diagnosis in inverter extra switches	No	No	Yes	Yes
4. Fault-diagnosis	Only OCF	OCF, SCF	OCF, SCF	OCF, SCF
5. Fault tolerance	Only OCF	OCF, SCF	OCF, SCF	OCF, SCF
6. Post-fault power/torque delivered	Rated power/torque	Rated power/torque	Rated power/torque	Rated power/torque
7. Motor rating	Designed for rated voltage and current	Designed for rated voltage and current	Designed for double the rated current	Designed for rated voltage and current
8. Auxiliary components	No	Buck converter + 3 switches + 1 fault protective leg	Buck converter + 1 SPDT switch + 1 fault protective leg	4 DPDT relays

It is shown in Chapter-2 that, the fault-tolerant OEWBLDC drive proposed in Chapter-2 requires about 9% more RMC compared to the conventional BLDC drive, considering only the propulsion system of the EV. A similar assessment is undertaken in this section while evaluating the economic viability of the proposed OEWBLDC drive vis-à-vis the one proposed in Chapter-2. In this evaluation, summarized in Table-3.4, the cost of the automobile body, chassis, supervisory controllers, and additional accessories which are common to the traditional and the fault-tolerant drive topologies are not included.

It may be noted from Table-3.4 that, the hike in the RMC to achieve 100% post-fault output power (against OCF as well as SCF) is 2% only, compared to the drive proposed in Chapter-2. Considering that the fault-tolerant drive proposed in Chapter-2 delivers only 50% of the rated power in the post-fault conditions, it appears that the OEWBLDC motor drive proposed in this work appears to be financially viable. Furthermore, the percentage increase in the RMC would be further swamped when the additional costs due to the chassis, body, accessories, and aesthetics are considered.

Table 3.4: Cost Evaluation of Fault-Tolerant Drive Configuration (Indian Rs.)

<table>
<tr><th colspan="2">Name of the equipment</th><th>Each unit cost (Rs./-)</th><th>No. of quantities</th><th>Total Cost (Rs./-)</th></tr>
<tr><td colspan="2">(a) Motor
(96 V, 3 KW BLDC motor)</td><td>31,780</td><td>1</td><td>31,780</td></tr>
<tr><td colspan="2">(b) Cost of li-ion battery (12V, 60AH,720WH)</td><td>13,620</td><td>8</td><td>1,08,960</td></tr>
<tr><td rowspan="2">(c) Cost of Inverter with driver (with switch voltage and current safety factor taken as 2)</td><td>(c_1) Cost of OEWBLDC motor Inverter topology with driver</td><td>(159+306)</td><td>12</td><td>5,580</td></tr>
<tr><td>(c_2) Cost of conventional VSI topology with driver</td><td>(159+306)</td><td>6</td><td>2,790</td></tr>
<tr><td rowspan="2">(d) Sensors</td><td>(d_1) Current sensor</td><td>1,870</td><td>2</td><td>3,740</td></tr>
<tr><td>(d_2) Voltage sensor components (ISO124, TL084CN)</td><td>(894 + 13)</td><td>ISO124→6
TL084CN→2</td><td>5,390</td></tr>
<tr><td colspan="2">(e) Auxiliary components (DPDT Relays)</td><td>806</td><td>4</td><td>3,224</td></tr>
<tr><td colspan="5">Percentage of additional cost incurred for the conventional BLDC motor drive :
$=\left(\frac{d_2+e+(c_1-c_2)+d1}{a+b+c_2}\right)$ *100% = $=\left[\frac{5390+3224+2790+3740}{31781+108960+2790}\right]$ * 100% = 10.55% ≈ 11%</td></tr>
</table>

3.6 Summary

This chapter proposes a dual-inverter fed dynamically reconfigurable fault-tolerant OEWBLDC motor drive configuration. The post-fault reconfiguration depends on the type of fault developed in any given semi-conductor switching device present in the dual-inverter system. The post-fault reconfiguration of the power circuit and the reconnection of the batteries in series ensure that the BLDC motor is supplied with its rated power even after the development of either an OCF or an SCF in the dual-inverter system. Even though such an agreeable situation arises due to the doubling of the voltage rating of the switching devices by a factor of '2', it would still be an affordable proposition for low power EVs, as the total increase in the RMC (of only the propulsion system) is only about 11% compared to the conventional BLDC drive, which does not offer the feature of fault tolerance. Compared to the OEWBLDC drive configuration proposed in Chapter-2, which achieves only 50% post-fault power delivery to the motor, the hike in the RMC is only 2% with the proposed power circuit configuration, considering the costs of individual components.

Chapter 4

A Single-Switch Fault-Tolerant BLDC Motor Drive with Rated Post-Fault Power Output and a Reduced Requirement of Steering Switchgear

Chapter 4

A Single-Switch Fault-Tolerant BLDC Motor Drive with Rated Post-Fault Power Output and a Reduced Requirement of Steering Switchgear

4.1 Introduction

In The fault-tolerant topologies for the conventional star connected IM & BLDC motor drive configurations are presented in [33-35] & [60, 70 & 72]. In the research work [59], fault-tolerant VSI topology is presented which utilizes redundant semiconductor inverter branches and rugged mechanical commutators. This combination helps in providing the advantages of low losses, stress elimination, and electrical isolation for the parallel redundant branches. In the research work presented in [60], a single-switch OC (or) SC fault-tolerant drive topology for EV applications is described, which uses six TRIACs and one actuator leg additionally. However, fault-diagnosis algorithms were not described in this literature [59-60].

The drive topology proposed in [70] achieves fault-tolerant operation by adding three TRIACs to the conventional BLDC motor drive. An algorithm to detect the OC switch fault-diagnosis is also presented in this manuscript. The fault-tolerant BLDC drive topology presented in [70] requires six additional fuses for achieving SC fault tolerance.

A fault-tolerant BLDC motor drive for a Magnetically-Suspended Control moment gyro (MSCMG) for aerospace applications is presented in [72]. This drive configuration requires 6-additional TRIACs and an additional phase leg to achieve fault-tolerant operation against a single-switch OC/SC fault. However, the additional TRIACs, employed to achieve fault-tolerant operation, are kept in the normal (i.e. pre-fault) circuit configuration making them susceptible to failures. Furthermore, the fault-diagnosis algorithm presented in this work cannot identify the fault conditions in the additional TRIACs.

This chapter proposes a fault-tolerant drive configuration for low-power EV applications, which can deliver rated post-fault power to the motor. In this configuration, the additional switching resources employed to implement fault tolerance are dormant in the pre-fault condition and are therefore not susceptible to the development of faults. Furthermore, this configuration requires only one current sensor and three voltage sensors to diagnose OC and SC faults, resulting in a significant reduction in the additional raw material cost to realize

fault tolerance. The fault-tolerant operation of the proposed power converter is experimentally verified with a laboratory prototype. This chapter also presents a cost analysis to prove the economic feasibility of the proposed fault-tolerant drive configuration.

4.2 Fault-Tolerant Operation of the Proposed Drive Configuration

4.2.1 Circuit Description and Fault-Tolerant Operation of the Drive

Fig. 4.1 presents the proposed fault-tolerant BLDC motor drive configuration. This topology consists of a conventional Voltage Source Inverter (VSI) with three legs denoted as 'Leg-A', 'Leg-B' & 'Leg-C'. Under normal conditions, the VSI is fed with the DC power supply 'V_{DC}'. Hall position sensors 'H_a', 'H_b' & 'H_c' are used to sense the rotor position to generate the gating signals for the VSI. Fig. 4.2 presents the back emf, current waveforms, and inverter switching signals for all the sector positions under steady and faulty operating conditions. To achieve fault tolerance, the proposed topology employs three bidirectional switches 'B_A', 'B_B' & 'B_C' and two SPDT relays 'SPDT-1' & 'SPDT-2'. Each of these bidirectional switches is realized by the anti-series connection of two IGBTs with a common emitter connection.

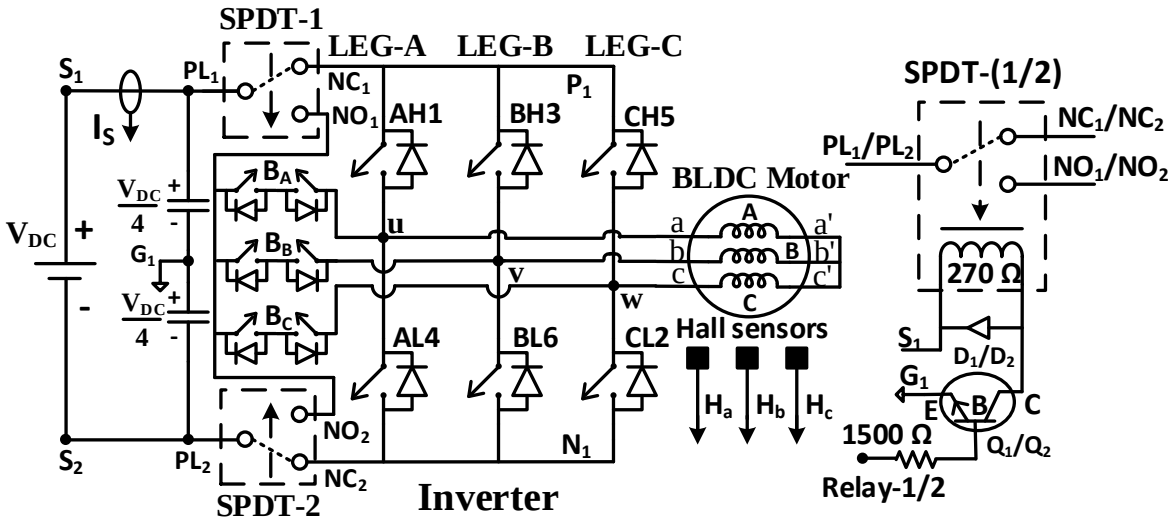


Fig. 4.1: Proposed OC/SC fault-tolerant BLDC motor drive configuration

Before the occurrence of any fault (i.e. in the default condition), the pole terminals of the SPDT relays ('PL_1' & 'PL_2') respectively connect the positive and the negative terminals of the input DC power supply (the battery in the case of an EV) to the corresponding terminals of the VSI through the Normally Closed positions 'NC_1' & 'NC_2' as shown in Figs. 4.1 & 4.3a.

Whenever a fault (it can be either an OC fault or an SC fault) is detected in the three top switches (AH1, BH3, or CH5), the relay SPDT-1 is operated. This makes the pole PL_1 to changeover from the default position NC_1 to the Normally Open (NO) contact, NO_1. This changeover connects the common-end of the bidirectional switches 'B_A', 'B_B' & 'B_C' to the positive terminal of the battery through the pole PL_1 of SPDT-1. At the same time, all the three bidirectional switches 'B_A', 'B_B' & 'B_C' are gated and the gating signals for all the three top switches (AH1, BH3, and CH5) are withdrawn. With this manoeuvre, the bidirectional switches 'B_A', 'B_B' & 'B_C' replace the three top switches and the drive continues to operate normally despite the development of the fault, delivering full power to the motor (Fig. 4.3b). It is obvious that a similar operation is achievable when a fault occurs in one of the three bottom switches. In this case, the relay SPDT-2 is operated, making the pole PL_2 to changeover from the default position NC_2 to NO_2, connecting the common-end of the bidirectional switches 'B_A', 'B_B' & 'B_C' to the negative terminal of the battery (Fig. 4.3c). Thus, it is not necessary to energize the relays in the default condition, which is an advantageous proposition.

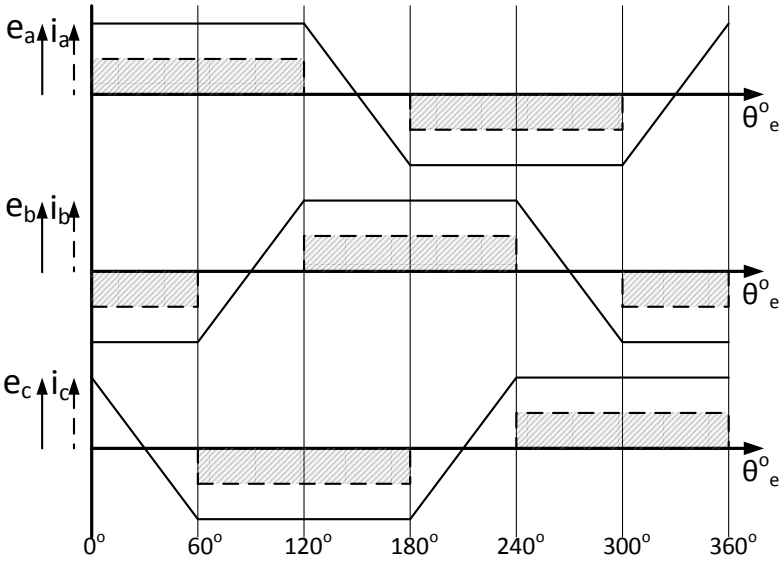


Fig. 4.2: Switching logic for each sector during steady and post fault conditions

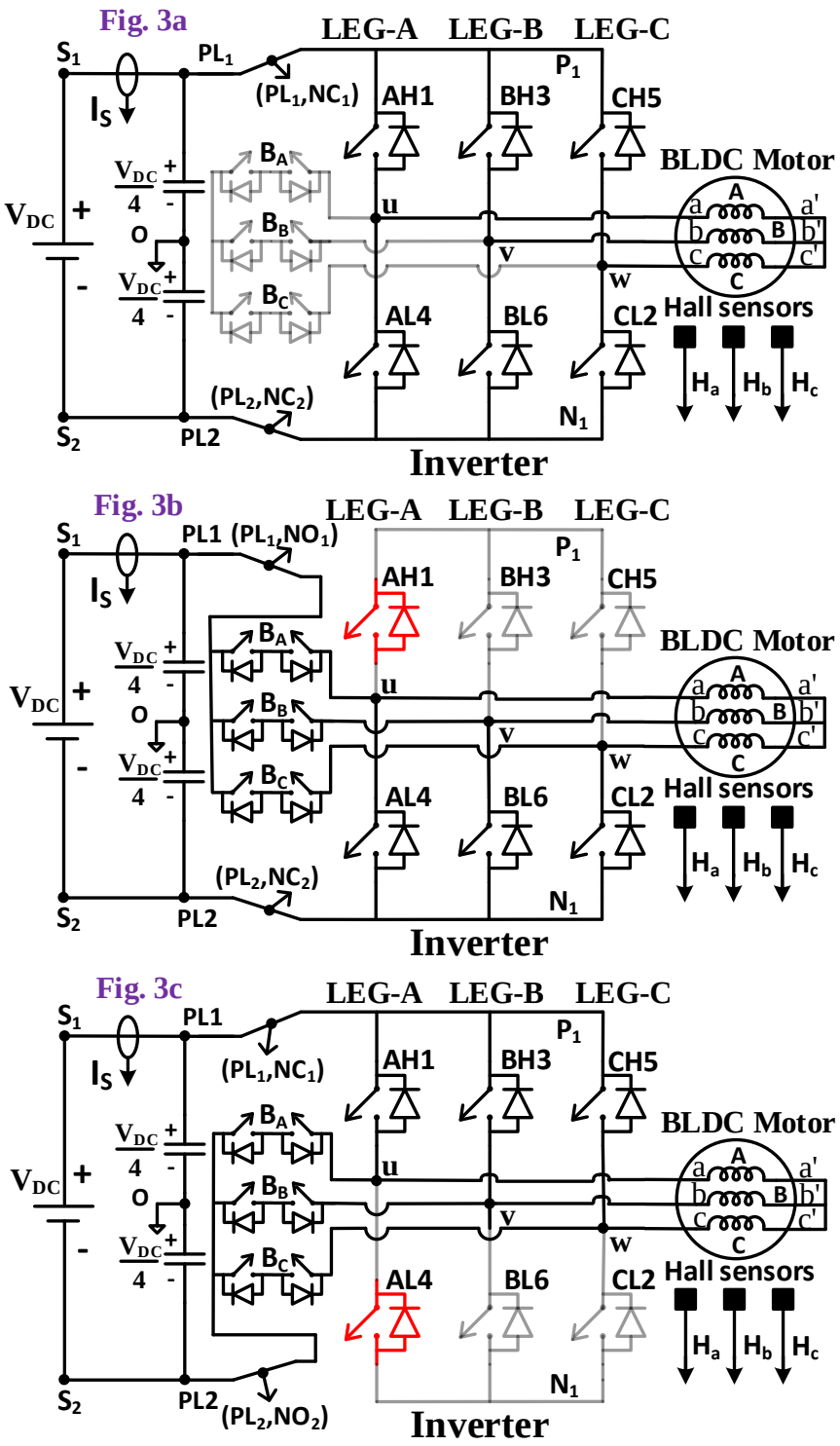


Fig. 4.3: Equivalent circuit diagram of the proposed fault-tolerant drive configuration during (a) steady operation conditions (b) OC/SC faulty conditions in switch 'AH1' (upper bank switch) (c) OC/SC faulty conditions in switch 'AL4' (lower bank switch)

It may also be noted that, while OEWBLDCM drive configurations, described in Chapters-2 & 3 require 6 voltage sensors and 2 current sensors to implement fault tolerance, the proposed topology needs only 3 voltage sensors and 1 current sensor with the same number of power semiconductor switching devices. In a scenario, wherein the cost of sensors dominates the cost of semiconductors, this topology brings in considerable savings in the raw material cost (RMC) to implement the feature of fault tolerance. Also, the proposed topology needs lesser supporting switchgear to implement 100% fault tolerance. Only 2 SPDT relays are needed in this topology as compared to 4 DPDT relays in Chapter-3, which is another contributing factor to the reduction in the RMC. Furthermore, all the 3 additional bi-directional switches are dormant in the pre-fault condition. Hence, they are not susceptible to the development of faults (Fig 4.3a).

The fault tolerance of the proposed BLDC motor drive configuration is verified for both open-loop as well as closed-loop drive operations. The closed-loop operation is performed by the traditional outer speed controller and inner current controller. Fig. 4.4 represents the schematic overview of the proposed closed-loop drive control with the fault tolerance feature.

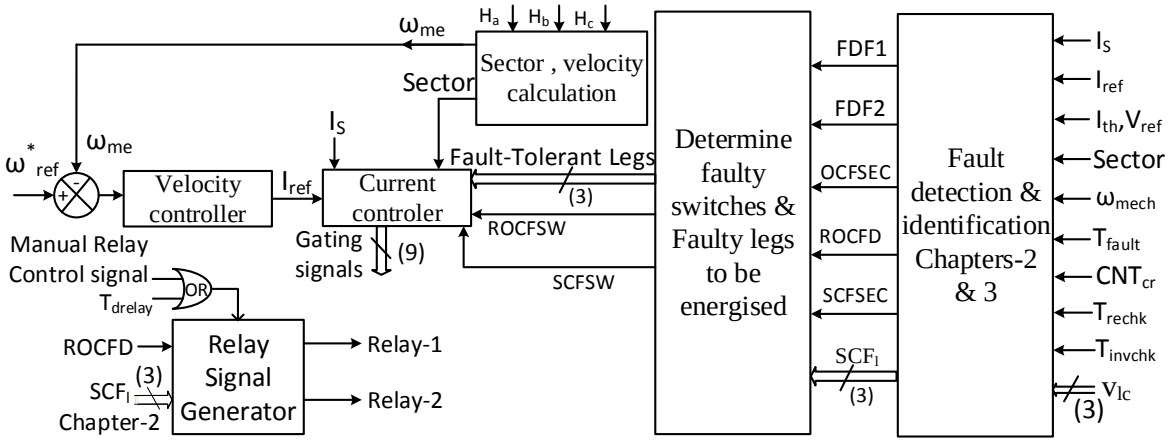


Fig. 4.4: Schematic presentation of fault-tolerant control mechanism

4.2.2 Fault-Diagnosis for the Proposed Drive Configuration

The OC & SC switch fault-diagnosis algorithms, which are proposed in Chapters-2 & 3, have been adopted in the proposed topology, which is briefly recapitulated below:

i) The diagnosis of the OC fault is accomplished by the identification of interruption in the input DC. If this current is interrupted for a pre-specified error period, the OC

fault is asserted and the corresponding sector is identified and its number is stored in a flag named 'OCFSEC'. Two more flags 'FDF1' and 'FDF2' are set to '1' if the interruption of the DC-current is affirmed in the present sector and the immediately succeeding sector. Based on the status of these flags, the faulty switch is identified and its number is stored in a flag named 'OCFSW'.

ii) The diagnosis of the SC fault is accomplished by the identification of the zero-voltage periods in line voltages, which are sensed during the non-conducting 60^o period between the top and the bottom devices in any given phase leg. The sector in which the zero-voltage period in a given line- voltage is observed is stored in the flag 'SCFSEC'. Based on this information, the SC fault is identified and the corresponding switch number is stored in the flag named 'SCFSW'.

4.3 Results and Discussion

Fig. A.1 presents the experimental prototype, which is used to validate the fault-tolerant capability of the proposed drive configuration using the dSPACE-1104 platform. Table-A.1 presents the parameters of the BLDC machine used in the experimental prototype. To emulate the occurrence of OC and SC switch faults experimentally, the gating signal for one of the switches is either withdrawn fully or maintained continuously.

The experimental validation for the fault-tolerant operation of the proposed topology for the OC fault is presented in Figs. 4.5-4.8. With the enforcement of OC fault in switch 'CH5' (at instant 'tf', Fig. 4.5), the diagnosis is carried out through the flags 'OCFSEC', 'FDF1' & 'FDF2' (at instants 'ta1', & 'ta2', Fig. 4.5). Based on this information, the switch number corresponding to the OC fault is stored in the flag 'OCFSW' (at the instant 'tb', Figs. 4.5-4.7). To conclusively assert the occurrence of the OC fault, a counter 'CNT' is triggered at this point of time, which counts the number of zero-current periods in the probation period (tc – tb). Only when this count exceeds a critical count, the fault is finally asserted and the value stored in the flag OCFSW is transferred to the final flag ROCFSW, which initiates the process of post-fault circuit reconfiguration. Fig. 4.8 validates the fault tolerance against the OC failure in switch 'CH5' for the closed-loop drive operation.

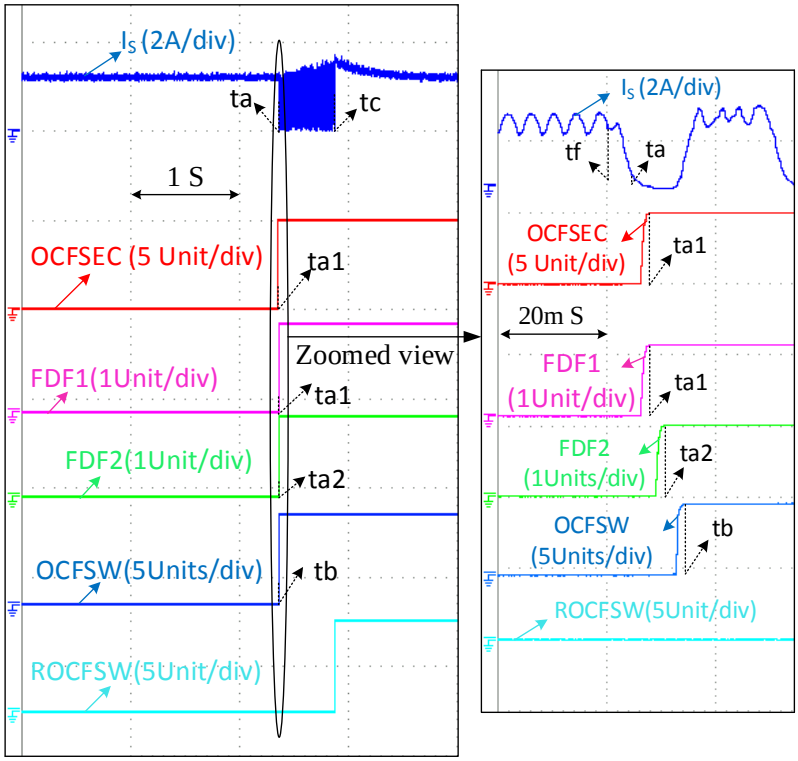


Fig. 4.5: Experimental results showing the flag statuses during OC fault-diagnosis (for OC fault in 'CH5')

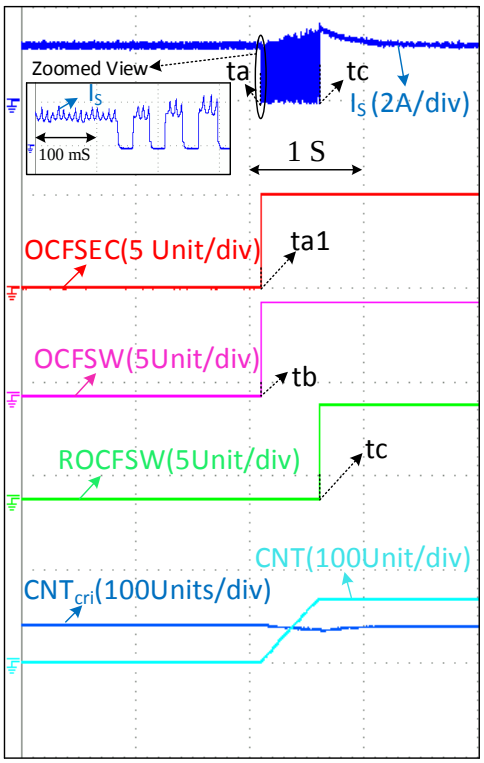


Fig. 4.6: Experimental results showing flag & counter values for OC fault in 'CH5'

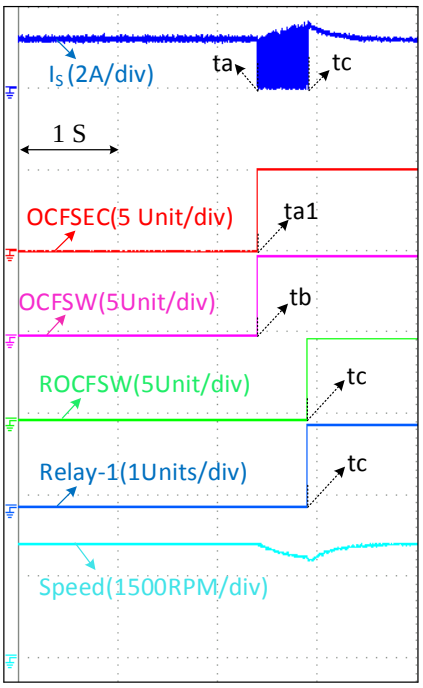


Fig. 4.7: Experimental results showing open-loop fault-tolerant drive operation for OC fault in 'CH5'

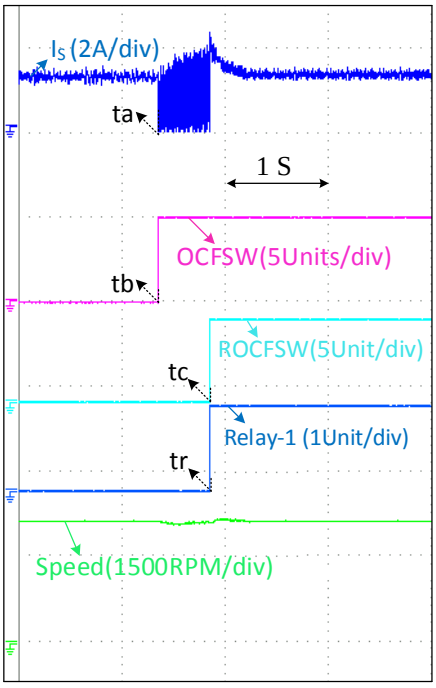


Fig. 4.8: Experimental results showing closed-loop fault-tolerant drive operation for OC fault in 'CH5'

Fig. 4.9 illustrates the experimental verification against the SC fault for the proposed drive configuration. In this experiment, the gating signal for the switch AL4 is held continuously high. With the diagnosis algorithm described in Chapter-2, the SC fault is diagnosed and the corresponding switch number is stored in the flag 'SCFSW' (at the instant 'ty', Fig. 4.9). As the number of the faulty switch belongs to the lower bank of the VSI, SPDT-2 is energized using Relay-2 (Fig. 4.1) at the instant 'ty' as shown in Fig. 4.9. With the

reconfiguration procedure explained in Section II, the drive can perform normally and eventually attains its rated speed even after the occurrence of the SC fault in the switch AL4.

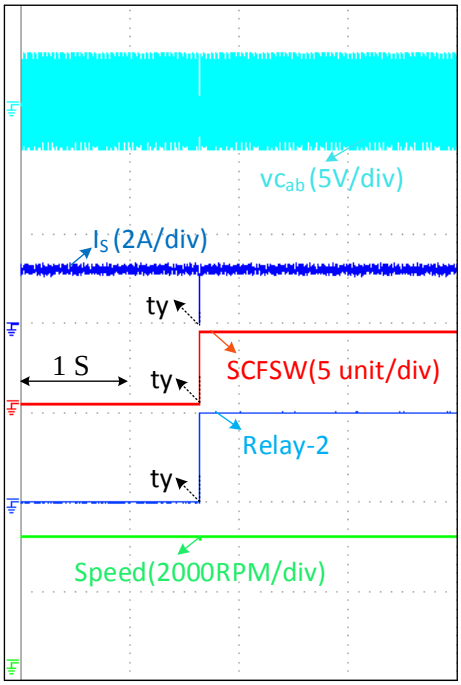


Fig. 4.9: Experimental results showing the fault-tolerant operation for SC fault in 'AL4'

4.4 Feasibility Analysis of the Proposed Electric Drive Topology

Table-4.1 summarizes the comparison of the proposed fault-tolerant BLDC motor drive topology vis-à-vis the topologies reported in the earlier literature. Table-4.2 shows the additional raw material cost incurred for the fault-tolerant topologies w.r.t the traditional drive configuration. The cost evaluation presented in Table-4.2 shows that the proposed drive configuration incurs only 5% additional RMC, while the OEWBLDC motor drives reported in Chapter-2 and Chapter-3 respectively incur 9% & 11%. The information contained in Tables-4.1 & 4.2 confirms the economic feasibility of the drive configuration for EV applications, with a post-fault delivery of 100% rated power.

Table 4.1: Comparison of Different Topologies with the Proposed Topology

Topological features	Topology [70]	Topology [72]	Topology [73]	Proposed Topology
1. No. of switches in the inverter	6 switches (VSI) + 3 TRIACs	6 switches (VSI) + 6 TRIACs + 1 additional leg	12 switches	12 switches
2. Switch ratings	Rated motor voltage and current	Rated motor voltage and current	Rated motor voltage and twice the rated motor current	Rated motor voltage and current
3. Fault-diagnosis in additional switches	No	No	Yes	Not susceptible for faults
4. Fault-diagnosis & tolerance	Only OCF	OCF, SCF	OCF, SCF	OCF, SCF
5. Post-fault power/torque delivered	Rated power/torque	Rated power/torque	Rated power/torque	Rated power/torque
6. Motor rating	Designed for rated voltage and current	Designed for rated voltage and current	Designed for double the rated current	Designed for rated voltage and current
7. Auxiliary components	No	Buck converter + 3switches +1 fault protective leg	Buck converter + 1 SPDT switch + 1 fault protective leg	2 SPDT relays

Table 4.2: Cost Evaluation of Fault-Tolerant Drive Configuration (Indian Rs.)

Name of the equipment		Each unit cost (Rs./-)	No. of quantities	Total Cost (Rs./-)
(a) Motor (96 V, 3 KW BLDC motor)		31,780	1	31,780
(b) Cost of li-ion battery (12V, 60AH,720WH)		13,620	8	1,08,960
(c) Cost of Inverter with driver (with switch voltage and current safety factor taken as 2)	(c_1) Cost of proposed Inverter topology with driver	(159+306)	(12, 9*)	4,662
	(c_2) Cost of conventional VSI topology with driver	159+306	6	2,790
(d) Sensors	(d_1) Current sensor	1,870	1	1,870
	(d_2) Voltage sensor components (ISO124, TL084CN)	(894 + 13)	ISO124→3 TL084CN→1	2,695
(e) Auxiliary components (SPDT Relays)		341	2	682
Percentage of additional cost incurred w.r.t the conventional BLDC motor drive: $=\left(\frac{d_2+e+(c_1-c_2)+d1}{a+b+c_2}\right)$ *100% = $=\left[\frac{2695+682+1872+1870}{31781+108960+2790}\right]$ * 100% = 4.96 % ≈ 5%				

*With the common-emitter connection of IGBTs to realize three bidirectional switches, one needs only 3 driver circuits.

4.5 Summary

This chapter proposes a fault-tolerant BLDC motor drive topology for low-power EV applications. This power converter uses 3 bi-directional power devices, which are inactive in the normal mode of operation, enhancing its reliability. The proposed power converter, upon diagnosing either an OC or SC fault in any one of the switching devices of the VSI, automatically reconfigures itself by inserting these bidirectional switching devices to achieve the feature of fault tolerance. Cost analysis reveals that the proposed topology, owing to its employment of fewer voltage sensors and current sensors, adds only 5% additional RMC to add the feature of fault tolerance to the conventional BLDC motor drive topology and offers a price-competent solution.

Chapter 5

An Auto-Reconfigurable BLDC Motor Drive for Electric Vehicle Applications with Multiple-Switch Fault-Tolerant Capability

Chapter 5

An Auto-Reconfigurable BLDC Motor Drive for Electric Vehicle Applications with Multiple-Switch Fault-Tolerant Capability

5.1 Introduction

In the previous chapters, fault-diagnosis methods for single switch OC and SC faults and the corresponding auto-reconfiguration strategies have been described for the Open-end winding as well as standard BLDC motor drives. However, these fault-diagnosis algorithms and circuit reconfiguration techniques cannot provide fault tolerance in the scenario of multiple-switch failures.

With this motivation, this chapter proposes a fault-tolerant BLDC motor drive topology that can achieve full (i.e.100%) fault tolerance against multiple-switch OC/SC faults. The proposed multiple-switch fault-tolerant topology requires three additional phase-legs to the VSI and 3 SPDT relays to achieve full fault tolerance. The proposed fault-tolerant BLDC motor drive topology is capable of developing the rated torque (and hence rated power) even after the occurrence of multiple-switch OC or SC faults, whereas, the works reported in the earlier Chapters-2, 3 & 4 are capable of handling only single-switch OC/SC fault conditions. This Chapter also presents the algorithm for diagnosing the multiple-switch (2-switch & 3-switch) OC fault conditions in the power semiconductor devices.

The additional switching resources of the proposed topology are pressed into service only after the occurrence of a fault. Hence, they are not vulnerable to the development of faults in the normal (i.e. pre-fault) mode of operation. The proposed fault-tolerant drive configuration needs only one Hall-current sensor and three voltage sensors are needed to implement the fault-diagnosis algorithm.

Thus, the proposed topology brings in a considerable improvement compared to the aforementioned fault-tolerant BLDC motor drives in terms of sensor requirement and the additional switchgear. As in the case of earlier chapters, this chapter also presents a feasibility analysis, which reveals that the proposed topology is quite affordable despite the requirement of additional switching devices and switchgear. Owing to these advantages, it is envisaged that the proposed power converter configurations are suitable for low-power electric vehicles.

The working principle of the proposed BLDC motor drive configuration is first verified with simulation studies. The simulation results are then experimentally validated on a laboratory prototype to demonstrate the effectiveness of the fault-diagnosis algorithm and the circuit reconfiguration strategy following the detection of a fault.

5.2 Proposed Multiple-Switch Fault-Tolerant BLDC Motor Drive Configuration

Fig. 5.1 represents the proposed multiple-switch OC/SC fault-tolerant BLDC motor drive configuration. In the proposed topology, the conventional VSI (with power poles *A*, *B*, and *C*) is augmented with three additional power poles, namely, *A'*, *B'*, and *C'* to obtain fault tolerance against multiple OC/SC faults.

The additional power poles in the topology are connected in parallel across the same DC input power supply 'V_{DC}' (a battery bank in the case of electric vehicles), avoiding the requirement of isolated DC power supplies. The terminals of a conventional star-connected BLDC motor are connected to the VSI through three SPDT relays ('*SPDT-A*', '*SPDT-B*' & '*SPDT-C*'). It may be noted that, in the normal (i.e. fault-free) mode of operation, the motor terminals (*a*, *b*, *c)* are connected to the output terminals of the VSI (*u* ,*v* ,*w*) through the poles of the SPDT relays ('PL_A', 'PL_B', & 'PL_C') and the Normally Closed contacts ('NC_A', 'NC_B', & 'NC_C').

Based on the Hall-sensor signals ('H_a', 'H_b', & 'H_c'), the position of the rotor is categorized into six symmetrical sectors, each spanning 60^o (electrical), denoted as 'Sector-1' to 'Sector-6' as shown in Fig. 5.2. Fig. 5.2 also shows the waveforms of the Back-EMFs generated in the motor phases and the switching signals required in the steady-state conditions in the healthy as well as the post-fault conditions. This figure also presents the details of the gating signals for the VSI as well as the additional legs after the processes of fault-diagnosis and circuit reconfiguration under switch fault conditions.

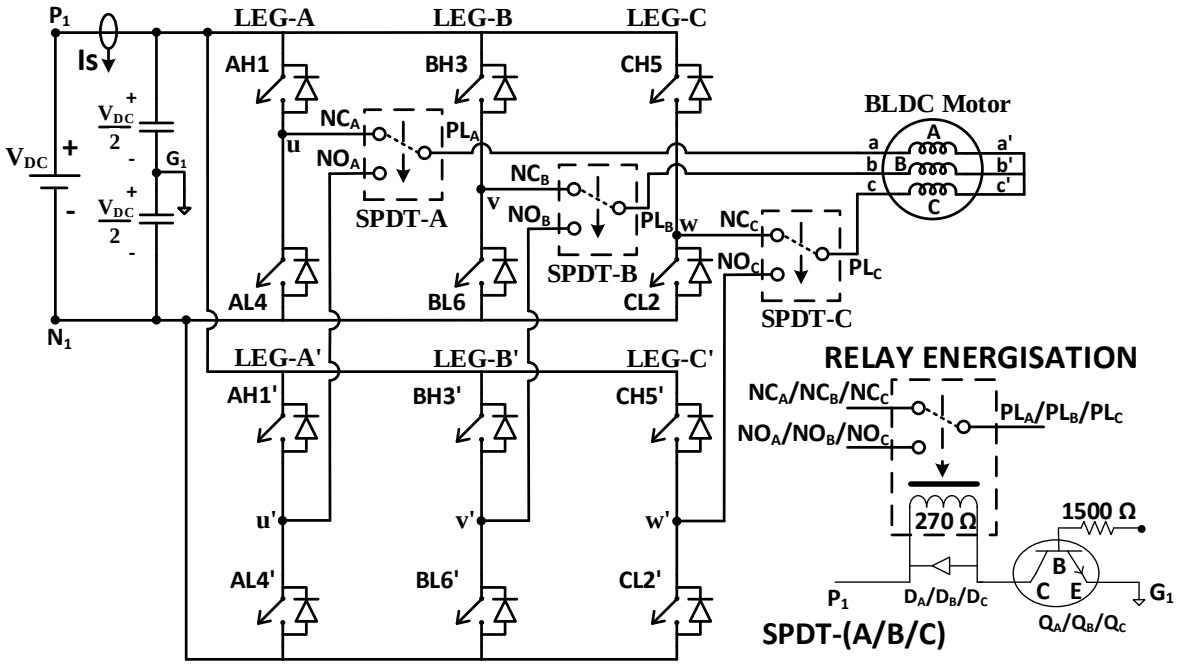


Fig. 5.1: Proposed multiple-switch OC/SC fault-tolerant drive configuration

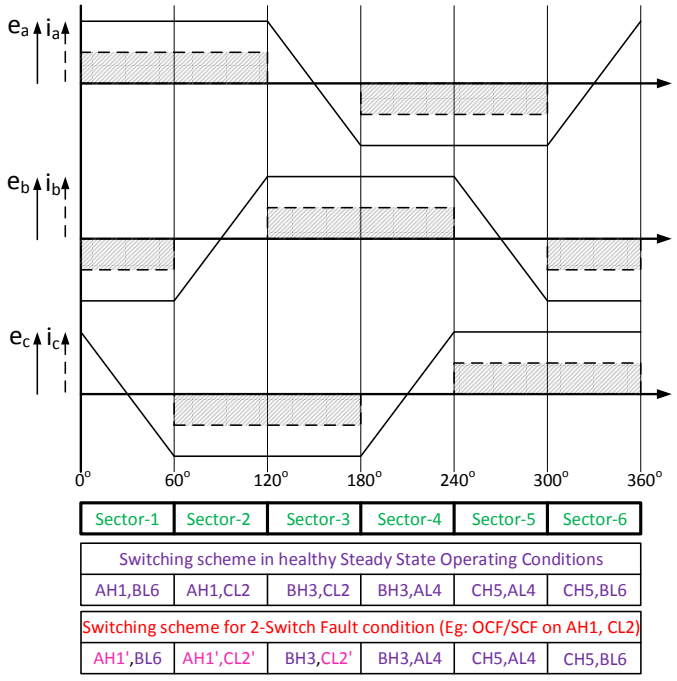


Fig. 5.2: Motor Back-EMF, phase currents & switching's during steady and faulty conditions

One may obtain fault tolerance against multiple-switch OC/SC faults, occurring in any of the phase-legs (*A*, *B*, & *C*), using the proposed fault-tolerant topology (Fig. 5.1). The only exception to the fault-tolerant operation of multiple-switch faults is the *simultaneous* occurrence of SC faults in the top and the bottom devices on a given phase-leg of the VSI,

leading to the shoot-through fault. However, this exception can be handled by providing fast-acting semiconductor fuses in each leg of the VSI.

The grey-shaded portions of Fig. 5.3a indicate the inactive portions of the proposed multiple-switch fault-tolerant topology in the healthy operating conditions. As these portions are dormant during the healthy condition of the proposed drive configuration, they are not susceptible to the occurrence of faults. The SPDT relays (*SPDT-A, SPDT-B, and SPDT-C*) steer power to the BLDC motor either through the healthy legs (Legs-A, *B*, & *C*) of the VSI through their Normally Closed (NC) contacts ('NC_A', 'NC_B', & 'NC_C'), or from the additional phase legs (Legs-A′, B′, & C′) through their Normally Open (NO) contacts ('NO_A', 'NO_B', & 'NO_C'). This arrangement avoids the necessity of energizing the SPDT-relays in the healthy condition of the drive.

Under faulty conditions, the relay coils of the pertinent SPDTs are energized through a transistor ($Q_A/Q_B/Q_C$ of Fig. 5.1) based circuitry, which is actuated based on the output of the fault-diagnosis algorithm. Fig. 5.3b shows the post-fault equivalent circuit of the drive, wherein the additional Legs-A' & C' substitutes the Legs-A & C of the VSI following the occurrence of multiple faults occurring in the Legs-A & C of the VSI.

For the conditions where the design requirement needs only single-switch OC/SC fault-tolerant operation, a circuit topology can be derived from the proposed multiple-switch fault-tolerant topology (shown in Fig. 5.3c). Where one out of the three additional legs (say Leg-A') is sufficient and all the Normally Open (NO) terminals ('NO_A', 'NO_B', & 'NO_C') of three SPDT relays ('*SPDT-A*', '*SPDT-B*' & '*SPDT-C*') are shorted and connected to the output terminal of the additional leg (as shown in Fig. 5.3c). Figs. 5.3c & 5.3d present the steady-state equivalent circuits of the derived single-switch fault-tolerant topology during healthy and faulty operating conditions (fault in Leg-A).

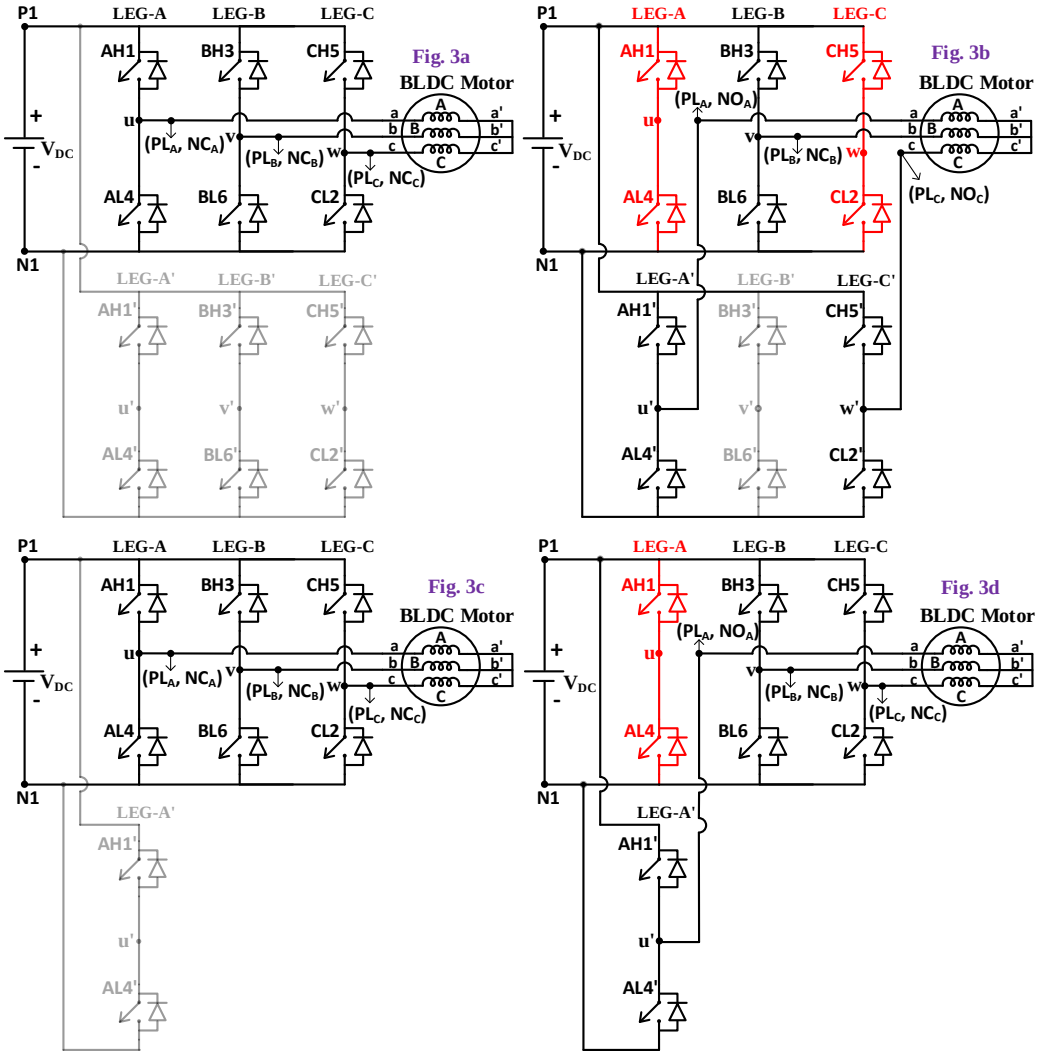


Fig. 5.3: Equivalent topology configuration of (a) multiple-switch fault-tolerant topology during steady drive operation; (b) multiple-switch fault-tolerant topology during multiple-switch OC/SC fault condition (in Leg-A & Z); (c) derived single-switch fault-tolerant topology during steady drive operation; (d) derived single-switch fault-tolerant topology during single-switch OC/SC fault condition (in Leg-A)

5.3 Fault-Diagnosis Algorithm and Fault-Tolerant Control

5.3.1 Multiple-switch Open-Circuit Fault-Diagnosis Algorithm

This chapter presents a multiple-switch OC fault-diagnosis, which is based on the measurement of the DC-source current with conventional Hall position sensors. The fault-diagnosis algorithm utilizes these Hall sensor signals to determine the sectors in which the DC-source current is absent. This information is pivotal to the identification of faulty switching devices (Chapter-2).

To simulate an OC fault in a semiconductor device, its gating signal is withdrawn. Similarly, the occurrence of SC fault is simulated by gating the pertinent device with a continuous gating signal. As a case study for the detection of multiple-switch OC fault, failure of the switching devices AH1 & CL2 is considered. Detection of all other cases pertaining to the two-switch failure is carried out using the same procedure as described in the following paragraphs.

A column matrix '**S**', with six elements, is used in the detection of the multiple-OC fault. Each element in this matrix is a *flag*, which denotes the current sector of operation. Each Flag is denoted with the symbol S_n, where the number '*n*' (n = 1, 2 ….6) denotes the current sector of operation. It should be noted that this matrix is continuously updated based on the Hall-sensor signals.

$$\begin{cases} S_n = 1, & \text{When sector} = \text{n} \\ S_n = 0, & \text{else condition} \end{cases} \text{(where } (1 \leq \text{n} \leq 6) \tag{5.1}$$

$$[\boldsymbol{S}] = [S_1, S_2, S_3, S_4, S_5, S_6]^T \tag{5.2}$$

The OC fault is identified whenever the DC-source current 'I_s' falls below a critical value 'I_{th}'. This critical current is a pre-determined fraction 'R_f' of the reference value 'I_{ref}'. Generally, the reference DC-source current 'I_{ref}' is determined by the output of the speed controller. However, for EV applications, wherein speed is controlled in an open loop, a suitable low value may be employed as the threshold current. Whenever an interruption is detected in the DC-source current, a flag named 'f_i' is set to '1'.

$$I_{th} = R_f * I_{ref} \tag{5.3}$$

$$\begin{cases} I_S < I_{th}, & f_i = 1 \ (OC\ fault\ identified) \\ I_S \geq I_{th}, & f_i = 0 \ (steady\ condition) \end{cases} \tag{5.4}$$

A single switch failure can occur in 6 different ways, while two-switch OC faults can occur in 15 (i.e. ${}^6C_2$) ways. From Fig. 5.2, it is evident that whenever a single-switch fault occurs, the DC-source current drops down to zero in two sectors. As far as the two-switch OC faults are concerned, of the 15 combinations, 6 combinations would lose the DC-source current in 3 sectors and the remaining 9 lose the DC-source current in 4 sectors (Fig. 5.2).

To assert the loss of DC-source current in any given sector, the interruption in the DC-source current must persist for a time interval, which is higher than a critical period denoted as 'T_{fault}'. Dedicated accumulators are employed to determine the time for which the DC-source current falls below the threshold value. This time period of interruption is named the 'error-time-period' and is denoted as '$T_{e,n}$ *(n=1,2…6)*'.

Whenever the current interruption flag 'f_i' is set to '1' in any given sector (where the sector number is positionally indicated in the ***S***-matrix), an accumulator corresponding to that particular sector is triggered. Based on a predetermined sampling time-period 'T_s' (70μS) and the initial condition $T_{e,n}(-1) = 0$, it accumulates a count, which is a measure of the time of interruption of the DC-source current.

All these accumulators are represented by the matrix '[$\boldsymbol{T_e}$]', which is given by:

$$[\boldsymbol{T_e}(\boldsymbol{i})]^T = (f_i) * \left[S_n * \left(T_{e,n}(i-1) + T_S\right)\right]^T \quad (5.5)$$

(Where n=1 to 6)

$$[\boldsymbol{T_e}(\boldsymbol{i})]^T = \begin{bmatrix} T_{e,1}(i) \\ T_{e,2}(i) \\ \vdots \\ T_{e,6}(i) \end{bmatrix} = (f_i) * \begin{bmatrix} S_1 * (T_{e,1}(i-1) + T_S) \\ S_2 * T_{e,2}(i-1) + T_S) \\ \vdots \\ S_6 * T_{e,3}(i-1) + T_S) \end{bmatrix} \quad (5.6)$$

Whenever *'$T_{e,n}(i)$'* is greater than the critical time-period 'T_{fault}' in any given sector (see the following paragraphs for details), the OC fault is asserted. The affected sectors owing to these OC faults are set to '1' and are captured in the corresponding *fault sector flags* denoted as '$F_{s,n}$' (where, n=1,2…6). Otherwise, the flag '$F_{s,n}$' remains at its initial value of '0'. All these flags are collectively represented by the matrix '$\boldsymbol{F_s}$' as shown in Table-5.1.

$$\begin{cases} F_{s,n} = 1, & T_{e,n}(i) \geq Tcri \\ F_{s,n} = 0, & T_{e,n}(i) < Tcri \end{cases} \quad (where\ (1 \leq n \leq 6) \quad (5.7)$$

When an OC fault is diagnosed for the first time, the corresponding sector number is stored in another flag named *first-fault-sector* (F_{fs}). In the scenario of multiple-fault detection, the remaining sectors also need to be probed for a possible fault. This process of probing is carried out until the current sector of operation again equals the value of the flag 'F_{fs}'. Upon the completion of probing all remaining sectors, another flag named *electric-fault-cycle* flag *('T_{fc}')* is set to '1'. After this event, based on the information available in the matrix *'$\boldsymbol{F_s}$'*, the

switch numbers corresponding to the faults are stored in two new flags called *'OCFSW1'* and *'OCFSW2'*. (See Table-5.1). This procedure marks the completion of the stage called *'pilot-fault-affirmation'*.

The critical-time-period 'T_{fault}' is given as:

$$T_{fault} = S_f * T_{sector} \tag{5.8}$$

From eqs. (2.7) & (5.8)

$$T_{fault} = \frac{S_f * 4 * \pi}{P * \omega_{me} * 6} \tag{5.9}$$

Where the parameter 'S_f' denotes the sensitivity factor, which is a measure of the period allocated to probe the zero-time periods of the DC-source current in a sector. Obviously, a higher value of 'S_f' results in higher accuracy.

Figs. 5.4-5.7 show the simulation results used for explaining the diagnosis procedure of multiple-switch OC fault. As explained earlier, multiple-switch OC faults are enforced artificially on switches AH1 & CL2. With the occurrence of multiple-switch OC fault (i.e. switches AH1 & ZL4) at instant '*tf2*' (see Fig. 5.6), the fall in the DC-source current is first identified at instant '*tx*' (Figs. 5.4, 5.5 & 5.6). Consequently, the accumulators *'$T_{e,1}$', '$T_{e,2}$' & '$T_{e,3}$'* of sectors numbered 1, 2 & 3 are triggered, while the others remain inactive as shown in Fig. 5.5. When the values stored in the accumulators *'$T_{e,1}$', '$T_{e,2}$' & '$T_{e,3}$'* are greater than the critical value 'T_{fault}', the fault-sector-flags '$F_{s,1}$', '$F_{s,2}$' & '$F_{s,3}$' are stored with corresponding sector information (at instant '*tx1*', '*tx2*' & '*tx3*', see Fig. 5.5), while the counts in the remaining flags (*'Fs,4', 'Fs,5' & 'Fs,6'*) remains at '0'. It may be recalled that these flags constitute the matrix *'$\boldsymbol{F_s}$'*. Based on the information available in the *'$\boldsymbol{F_s}$'* matrix, the faulty switch numbers are stored in flags *'OCFSW1'* & *'OCFSW2'* (at instant '*ty*', see Figs. 5.4, 5.5 & 5.6; see Table-5.1).

During dynamic conditions, the reference value of speed can cause a momentary dip in the DC-source current (which would eventually be restored to its previous value). This momentary dip could drop down to a value, which is below the threshold value *'I_{th}'* for a duration that is greater than the critical-time-period *'T_{fault}'* and be misinterpreted as an interruption in the DC-source current leading to the false assertion of OC faults. Whereas, under genuine OC fault conditions, the DC-source current is absent in one or more operating

sectors where the faulty switches are expected to conduct. These zero-periods appear as periodic oscillations in the DC-source current. This fact is exploited to distinguish genuine OC faults from spuriously detected OC faults and the algorithm corresponding to it is presented in the following paragraphs.

As described earlier, at the end of the pilot-fault-affirmation stage, the faulty switch numbers are stored in the flags *'OCFSW1' & 'OCFSW2'*. To confirm the fault conclusively, the probation period of fault-diagnosis is stretched to a period of *'T_{rechk}'* (i.e *'T_{rechk}=tz-ty'* in Fig. 5.4). During this period of probation, the number of zero-current periods is counted, which are shown as *'Z_1', 'Z_2'... 'Z_{n-1}', 'Z_n'* (Fig. 5.6 and Fig. 5.7). Each zero-current period is validated only when its duration, denoted as *'$T_{e,x}$'* (eq. 5.10) is higher than the *recheck-critical-time-period* given by *'TR_{fault}'* (eq. 5.11). This *'TR_{fault}'* is an integer multiple (*'N_{zts}'*) of the critical time *'T_{fault}'* (eq. 5.11), which is determined by the number of sectors over which the OC fault is detected continuously (Table-5.1). The number of such validated zero-transition periods is stored in a register, named *'CNT'*, which is inspected at the end of the probation period (*'T_{rechk}'*).

$$T_{e,x}(i) = (f_i) * \left(T_{fc}\right) * (T_{e,x}(i-1) + T_S) \tag{5.10}$$

$$TR_{fault} = N_{zts} * T_{fault} \tag{5.11}$$

The suspected OC fault is confirmed, when the count value stored in *'CNT'* is more than the critical-count value *'CNT_{cr}'* at the end of the *'T_{rechk}'* period (eq. 5.12 and eq. 5.13). This confirmation sets a new flag, named *'ROCFD'* (Reliable OC fault-diagnosis), to '1'. The corresponding reliable OC fault switch numbers are stored in the flags *'ROCFSW1'* & *'ROCFSW2'* (eq. 5.14 and eq. 5.15). Table-5.1 presents the values of these flags for all possible 2-switch OC faults.

$$CNT_{cr} = N_{zel} * D_{sf} * \frac{T_{rechk}}{t_{el}} \tag{5.12}$$

From eq. 5.12, eq. 2.4 & eq. 2.5,

$$CNT_{cr} = N_{zel} * D_{sf} * \frac{T_{rechk} * p * \omega_{me}}{4\pi} \tag{5.13}$$

$$\begin{cases} ROCFD = 1; & if\ CNT > CNT_{cr} \\ ROCFD = 0; & otherwise \end{cases} \tag{5.14}$$

$$ROCFSWx = OCFSWx * ROCFD; (x \in 1, 2) \tag{5.15}$$

The value of critical-count *'CNT_{cr}'* depends on the probation period *'T_{rechk}'* & the period of the electric cycle *'t_{ele}'* (which depends on the speed of the motor, *'ω_{me}'*). In equations 5.12 and 5.13, the symbols *'D_{sf}'* and *'N_{zel}'* respectively denote the factor of safety ($0< D_{sf} < 1$, which is the designer's choice) and the number of zero transitions appearing in an electric cycle due to faulty switches. In this work, D_{sf} is chosen to be 0.5. The values of *'N_{zts}'* and *'N_{zel}'* for all possible 2-switch combinations are presented in Table-5.1.

For the example considered (OC faults in AH1 and CL2), when the value of count stored in the register *'CNT'* is greater than the critical value *'CNT_{cr}'* at the end of *'T_{rechk}'* (i.e. *'tz - ty'* in Figs. 5.4, 5.6 & 5.7), the flags *'ROCFSW1'* & *'ROCFSW2'* (see Figs. 5.4 & 5.7) are loaded with the faulty switch numbers (eq. 5.15).

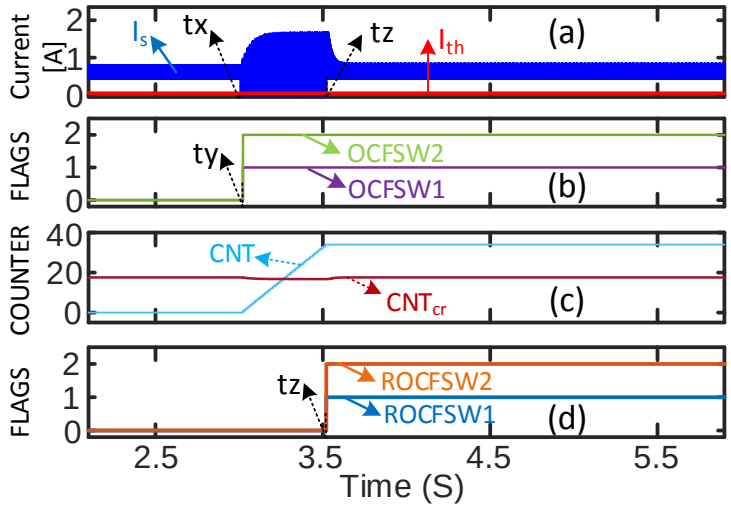


Fig. 5.4: Simulation results of multiple-switch OCF in switches AH1 & CL2: (a) I_s, I_{th} (b) OCFSW1, OCFSW2 (c) CNT, CNT_{cr} (d) ROCFSW1, ROCFSW2

Based on the information stored in the flags *'ROCFSW1'* and *'ROCFSW2'*, which conclusively identify the faulty switches, the process of circuit reconfiguration is initiated. This process consists of energizing the pertinent SPDT relays corresponding to the faulty legs using the actuating signals *Relay-[A, B, C]* (presented in Table-5.1). With this action, the motor phase windings which are connected to the faulty legs of the VSI are reconnected to the corresponding output terminals of the additional phase legs (*A', B', and C'*) resulting in the fault-tolerant operation of the drive. Table-5.1 presents the information regarding the backup phase legs, which are substituted for the corresponding phase legs of the VSI (*A, B, and C*).

If the value stored in the counter *'CNT'* is less than the *'CNT_{cr}'*, the flag *'ROCFD'* remains at the default value of '0' even after the probation period *'T_{rechk}'*. This indicates that the pilot diagnosis of the OC fault is spurious and hence the process of subsequent circuit reconfiguration is not initiated. Consequently, the pilot-diagnostic system is reset by resetting all flags associated with it (*'$F_{s,n}$'*, *'T_{fc}'*, *'OCFSW1'*, *'OCFSW2'*, *'CNT'*, *'ROCFSW1'* & *'ROCFSW2'*) and is ready to detect future faults.

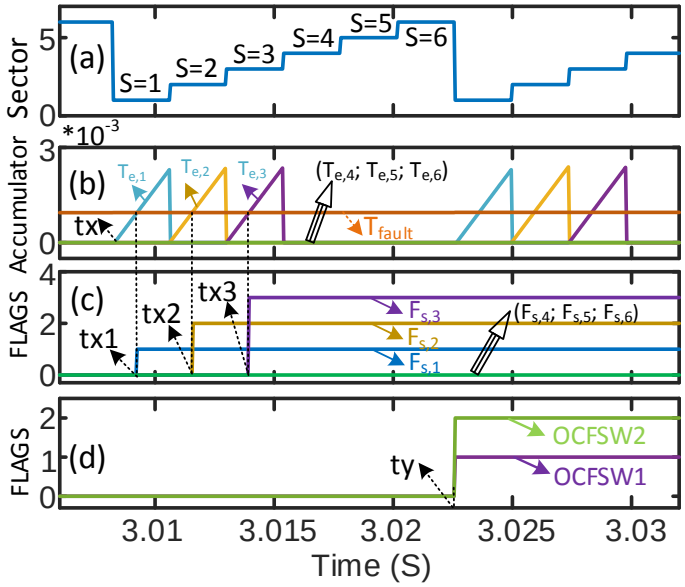


Fig. 5.5: Simulation results presenting the status of the flags for multiple-switch OC fault in switches AH1 & CL2: (a) sector of operation (b) $T_{e,n}$, T_{fault} (c) $F_{s,n}$ (d) OCFSW1, OCFSW2

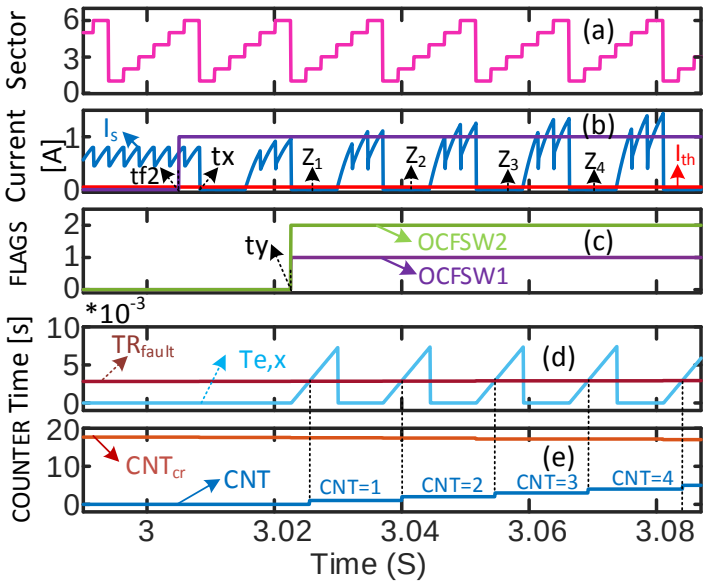


Fig. 5.6: Simulation results of multiple-switch OCF in switches AH1 & CL2 (detailed diagnosis at instant 'tx' of Fig. 5.4a): (a) sector of operation (b) I_s, I_{th}, Fault-initiation (c) OCFSW1, OCFSW2 (d) $T_{e,x}$, TR_{fault} (e) CNT, CNT_{cr}

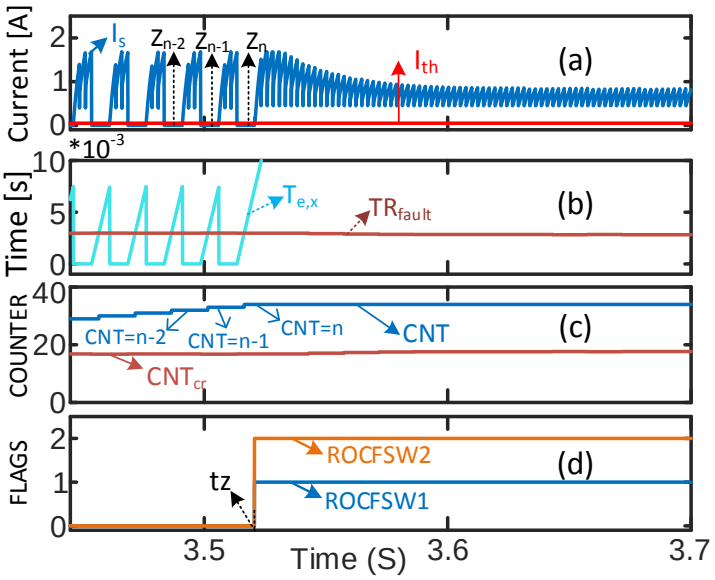


Fig. 5.7: Simulation results of multiple-switch OCF in switches AH1 & CL2 (detailed diagnosis at instant 'tz' of Fig. 5.4a): (a) I_s, I_{th} (b) $T_{e,x}$, TR_{fault} (c) CNT, CNT_{cr} (d) ROCFSW1, ROCFSW2

This procedure of fault-diagnosis can also be extended for three-switch OC fault conditions. The three-switch faults can be subdivided into two categories; in the first case, the three faulty switches belong to three different inverter legs. In the second case, two out of the three faulty switches are from one phase-leg, while the other one is present in any one of the remaining two legs.

As an example, for the OC fault in switches AH1, BH3 & CL2 (first case), the DC-source current shows a discontinuity in Sectors-(1 to 4). Correspondingly, the flags *'$F_{s,1}$'* to *'$F_{s,4}$'* are set to '1'. It may be verified that this situation is indistinguishable from the two-switch OC fault condition, wherein switches AH1 & BH3 develop OC faults. To resolve this issue, it is initially assumed that the developed fault is a two-switch fault (OC faults in AH1 & BH3) and the circuit is reconfigured accordingly (Table-5.1). This action is termed *pilot-reconfiguration*. Obviously, this pilot reconfiguration is inadequate as the OC fault in the switch CL2 is not covered, as it is not discovered yet. To discover the three-switch OC fault, the DC-source current is further probed. If the DC-source current reveals further oscillations (in Sectors-2 & 3), it is a clear indication that the fault is indeed a three-switch OC fault and a new flag *'ROCFSW3'* is set to the number corresponding to the faulty switch (2 in this example). Accordingly, *Relay-C* is actuated to bring in the backup *Leg-C'* (Fig. 5.1), completing the process of post-fault circuit reconfiguration.

In the second case, wherein switches AH1, AL4 & CL2 develop the OC fault, the DC-source current would be absent in as many as 5 of the 6 sectors (Sectors 1-5). It may be verified that this situation is indistinguishable from the one, wherein the switches AH1, AL4 & BH3 develop the OC fault. In this condition, firstly switch numbers corresponding to AH1 & AL4 are stored in flags *'ROCFSW1' & 'ROCFSW2'*, based on which the pilot-circuit reconfiguration is carried out. After this act, the DC-source current is further probed. Based on the sectors in which it is absent, the faulty switch is identified and the corresponding number is stored in the flag '*ROCFSW3*'.

5.3.2 Single-switch Short-Circuit Fault-Diagnosis Algorithm

For the diagnosis of the SCF, the fault-tolerant BLDC motor drive proposed in this chapter also employs the same algorithm, which is developed in Chapter-2. In the single switch detection algorithm described in Chapter-2, six line-line voltages need to be sensed, which need to be electrically isolated from the power circuit. As Hall-voltage sensors are expensive, low-cost analog isolation amplifiers (based on ISO-124) are employed, which are capable of achieving the same bandwidth as that of a Hall sensor. The fault sensing algorithm exploits the non-conducting interval of 60^{o} (electrical) between the top and bottom devices in any phase-leg of the VSI. As the proposed fault-tolerant topology in this chapter employs conventional star-connected BLDC motor drive, the SCF diagnosis algorithm requires only the measurement of three line-voltage signals. This reduces the cost of sensors and increases reliability.

Fig. 5.8 illustrates the flowchart presentation of the fault-diagnosis & the post-fault circuit reconfiguration strategy for the proposed fault-tolerant drive. The overall performance of the proposed fault-tolerant BLDC motor drive system is assessed with experimental studies in open-loop as well as closed-loop operation. The closed-loop drive operation uses the traditional outer speed control loop and the inner current control loop. The schematic overview of the closed-loop control system for the proposed fault-tolerant drive is shown in Fig. 5.9.

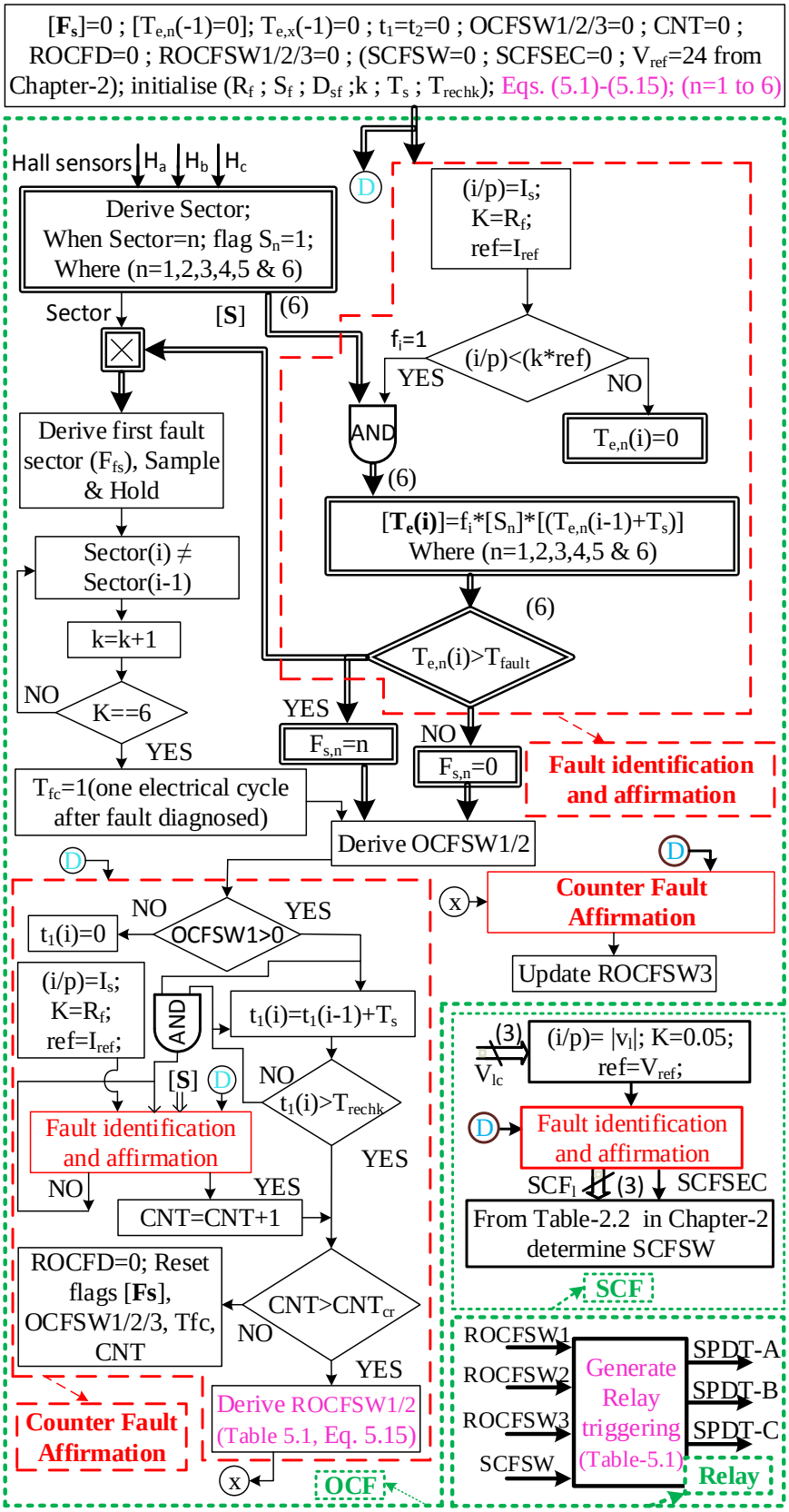


Fig. 5.8: Flowchart representation of overall fault-diagnosis & reconfiguration procedure employed for the fault-tolerant operation

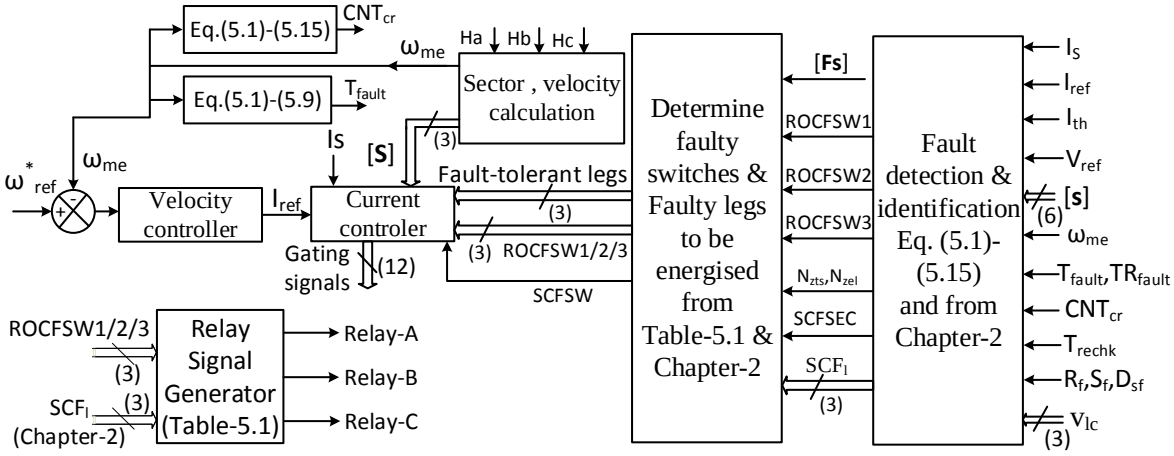


Fig. 5.9: Schematic overview of control scheme employed for fault-tolerant drive operation

Table 5.1: OC Fault-Diagnosis Information

Faulty switches	**Fs**	[ROCFSW1, ROCFSW2]	Nzts, Nzel	Relay-[A,B,C]	Backup legs
AH1	[1 1 0 0 0 0]	[1,0]	2,1	[1,0,0]	Leg-A'
CL2	[0 1 1 0 0 0]	[2,0]	2,1	[0,0,1]	Leg-A'
BH3	[0 0 1 1 0 0]	[3,0]	2,1	[0,1,0]	Leg-A'
AL4	[0 0 0 1 1 0]	[4,0]	2,1	[1,0,0]	Leg-A'
CH5	[0 0 0 0 1 1]	[5,0]	2,1	[0,0,1]	Leg-A'
BL6	[1 0 0 0 0 1]	[6,0]	2,1	[0,1,0]	Leg-A'
AH1, BH3	[1 1 1 1 0 0]	[1,3]	4,1	[1,1,0]	Legs-A' & B'
AH1, CH5	[1 1 0 0 1 1]	[1,5]	4,1	[1,0,1]	Legs-A' & C'
AH1, AL4	[1 1 0 1 1 0]	[1,4]	2,2	[1,0,0]	Leg-A'
AH1, BL6	[1 1 0 0 0 1]	[1,6]	3,1	[1,1,0]	Legs-A' & B'
AH1, CL2	[1 1 1 0 0 0]	[1,2]	3,1	[1,0,1]	Legs-A' & C'
BH3, CH5	[0 0 1 1 1 1]	[3,5]	4,1	[0,1,1]	Legs-B' & C'
BH3, AL4	[0 0 1 1 1 0]	[3,4]	3,1	[1,1,0]	Legs-A' & B'
BH3, BL6	[1 0 1 1 0 1]	[3,6]	2,2	[0,1,0]	Leg-B'
BH3, CL2	[0 1 1 1 0 0]	[3,2]	3,1	[0,1,1]	Legs-B' & C'
CH5, AL4	[0 0 0 1 1 1]	[5,4]	3,1	[1,0,1]	Legs-A' & C'
CH5, BL6	[1 0 0 0 1 1]	[5,6]	3,1	[0,1,1]	Legs-B' & C'
CH5, CL2	[0 1 1 0 1 1]	[5,2]	2,2	[0,0,1]	Leg-C'
AL4, BL6	[1 0 0 1 1 1]	[4,6]	4,1	[1,1,0]	Legs-A' & B'
BL6, CL2	[1 1 1 0 0 1]	[6,2]	4,1	[0,1,1]	Legs-B' & C'
CL2, AL4	[0 1 1 1 1 0]	[2,4]	4,1	[1,0,1]	Legs-A' & C'

5.4 Results and Discussion

An experimental prototype is built to verify the working principle of the proposed fault-tolerant BLDC motor drive, which is shown in Fig. A.1. In this system, dSPACE-1104 is employed as the control platform. Ratings and parameters of the BLDC motor used for simulation as well as experimentation are presented in Table-A.1.

Experimental results pertaining to the performance of the proposed fault-tolerant drive topology against single as well as multiple-switch OC faults are presented in Figs. 5.10-5.16.

The procedure for diagnosing a two-switch OC fault and the subsequent fault-tolerant operation of the proposed multiple-switch fault-tolerant drive topology (Fig. 5.1) are shown in Figs. 5.10-5.12. When the drive is operated in an open-loop and OC faults are wilfully induced in switches AH1 & CL2 (at instant '*tf2*', Fig. 5.10), the DC-source current falls below its threshold value in sectors 1, 2, and 3 (from instant '*ta*'), which pertain to the faulty devices as indicated in Fig. 5.2. Correspondingly, the fault-sector-flags *'$F_{s,1}$', '$F_{s,2}$' & '$F_{s,3}$'*, described in section-5.3, are set at the instants '*ta1*', '*ta2*' & '*ta3*' as shown in Fig. 5.10. Furthermore, the *electric-fault-cycle flag 'T_{fc}'* is set to '1' at the instant '*tb*'. With the available *fault-sector-flag* matrix information '***Fs***' at the instant '*tb*', the faulty switches are identified (from Table-5.1) and the corresponding faulty switch numbers are stored in flags *'ÓCF1' & 'OCFSW2'* at instant '*tb*' as shown in Fig. 5.11. The periodic absence in the DC-source current 'I_s' is further examined till the end of the probation period as described earlier in section-5.3. When the number of oscillations in the DC-source current counted in the pertinent accumulators (denoted as 'CNT') exceeds a critical value (*'CNT_{cr}'*) as shown in Fig. 5.11 (at instant *'tc'*), the multiple-switch fault is conclusively asserted and the numbers corresponding to the faulty switches are loaded in flags *'ROCFSW1' & 'ROCFSW2'* (at instant *'tc'*, Fig. 5.12). With the information available in flags *'ROCFSW1'* and/or *'ROCFSW2'*, the process of post-fault circuit reconfiguration is triggered by energizing pertinent SPDTs (*SPDT-A & SPDT-C*) in the present case (see Fig. 5.3 and Table-5.1). From the bottom trace, which shows the speed of the BLDC motor, it is evident that the post-fault speed (after the post-fault circuit reconfiguration) is the same as the pre-fault speed. This conclusively proves that the proposed fault-tolerant BLDC motor drive is capable of delivering rated power at the rated speed (developing the rated torque), thus achieving the objective of obtaining 100% fault tolerance against two-switch faults.

Figs. 5.13 and 5.14 demonstrate the processes of fault-diagnosis as well as fault-tolerant operation for a single-switch OC fault using the derived single-switch fault-tolerant topology (Fig. 5.3c). In this experiment, an OC fault is enforced on the switch AH1 under open-loop drive operation. As one might expect, the drive retains its capability of delivering the rated power after the detection of the OC fault and the subsequent process of circuit reconfiguration (Fig. 5.14).

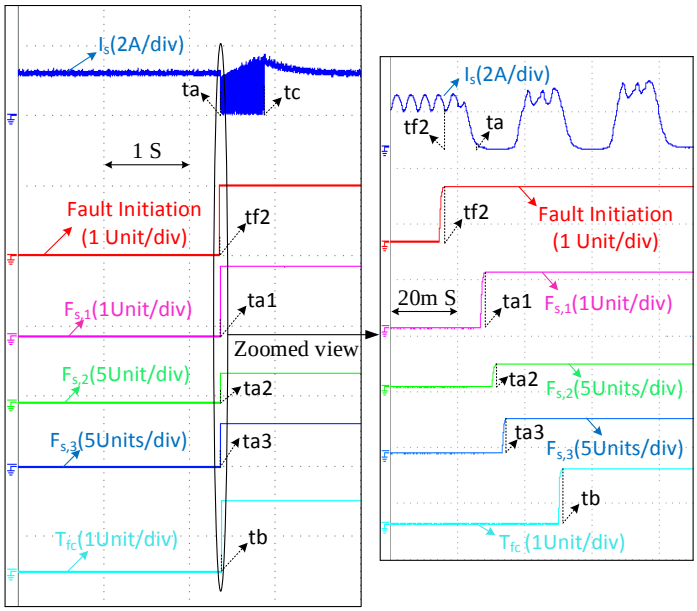


Fig. 5.10: Experimental results presenting the status of the flags during OC fault in switches AH1 & CL2 (Left-side: Normal-view, Right-side: zoomed view of the encircled figure portion)

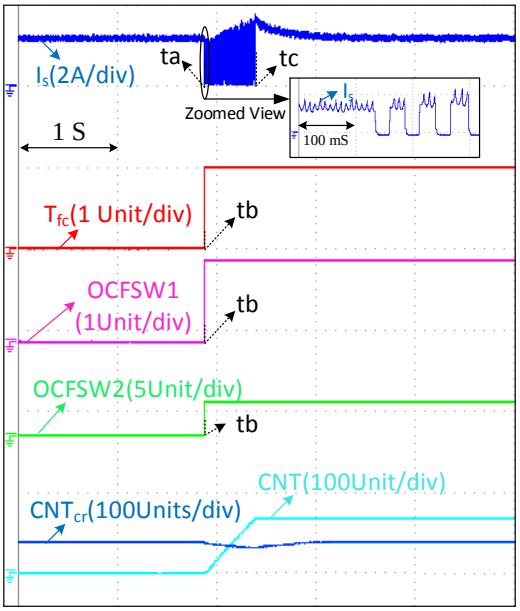


Fig. 5.11: Experimental results presenting the status of the counter and flags during OC fault in switches AH1 & CL2

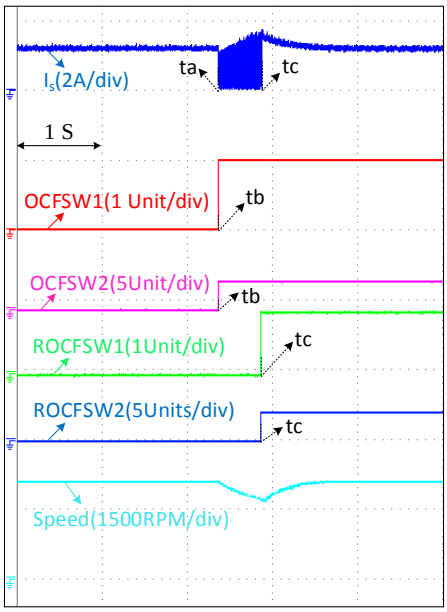


Fig. 5.12: Experimental results presenting the fault-tolerant drive operation during OC fault in switches AH1 & CL2

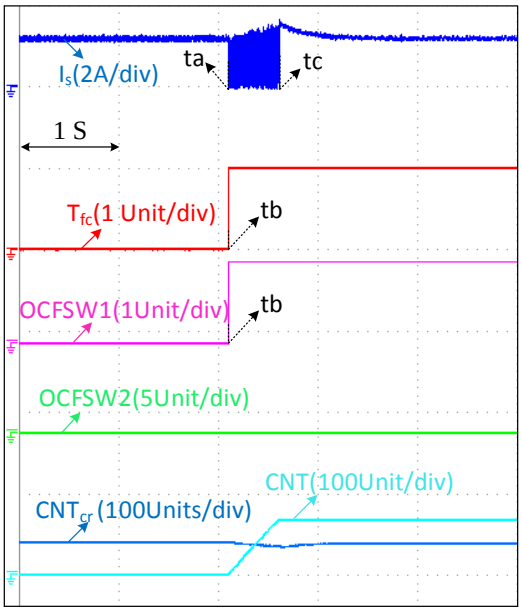


Fig. 5.13: Experimental results presenting the status of the counter and flags during OC fault in switch AH1

The suitability of the proposed multiple-switch fault-tolerant BLDC motor drive for closed-loop speed control applications is demonstrated in the experimental results presented in Fig. 5.15. To demonstrate this capability, OC faults are created in the switching devices AH1 & CL2 (Fig. 5.3). The closed-loop drive control system is implemented as shown in Fig. 5.9. With closed-loop speed control, it may be observed that the speed is restored to the reference value following the source disturbance created at the instant *'tsd'* (Fig. 5.15).

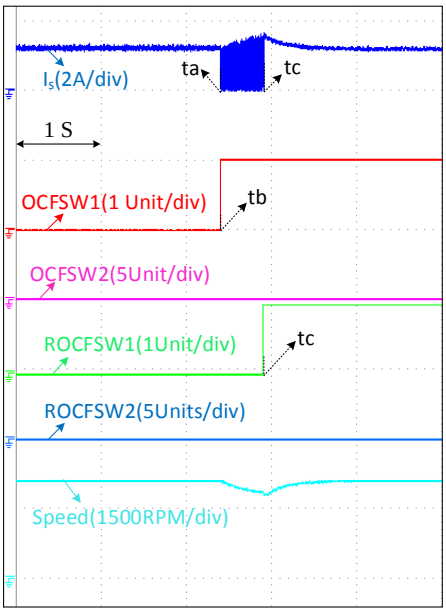


Fig. 5.14: Experimental results presenting the open-loop fault-tolerant drive operation during OC fault in switch AH1

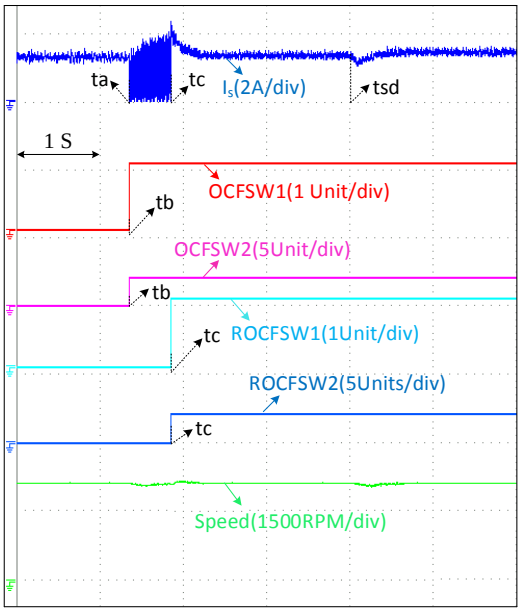


Fig. 5.15: Experimental results presenting the closed-loop fault-tolerant drive operation during OC fault in switches AH1 & CL2

Fault-tolerant operation of the proposed drive against a 3-switch OC fault is shown in Fig. 5.16. In this experiment, the switches AH1, BH3 & CL2 are intentionally turned off. For this fault, the DC-source current drops to zero in sectors 1, 2, 3, & 4. The complication is that this fault is indistinguishable from the 2-switch OC fault, wherein the switches AH1 & BH3 develop OC faults. Hence, this fault is initially treated as the 2-switch fault (as if only AH1& BH3 are faulty) and the flags *'ROCFSW1' & 'ROCFSW2'* are set to the corresponding switch

numbers at the instant '*tc*' (Fig. 5.16) to indicate the same. The DC-source current is probed after the circuit reconfiguration corresponding to the 2-switch fault. If the DC-source current shows oscillations even after this maneuver, it is realized that it is indeed a 3-switch fault. Consequently, the flag '*ROCFSW3*' is set to '2', and the corresponding circuit reconfiguration is initiated. When this process is completed, the drive regains the original speed (Fig. 5.16). Thus, the full fault tolerance is obtained by the proposed BLDC motor drive.

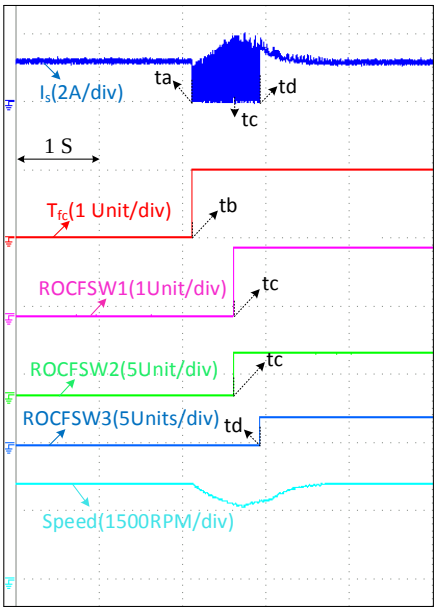


Fig. 5.16: Experimental results presenting the fault-tolerant drive operation during OC fault in switches AH1, BH3 & CL2

The experimental result shown in Fig. 5.17 shows the capability of the proposed drive configuration to handle sequential faults occurring in three different legs. In this experiment, firstly the SC fault is inflicted on the switch AL4 by continuously gating it. The SC fault-diagnosis algorithm proposed in Chapter-2 is used in this work, which loads the number corresponding to the faulty switch into the flag *'SCFSW'* at the instant '*ty*' (Fig. 5.17). This event triggers the process of circuit reconfiguration by energizing the *'SPDT-A'*, which connects the affected motor phase to the mid-point of the additional Leg-A', achieving the required fault tolerance. Once the drive attains its pre-fault speed, an OC fault is initiated in switch 'BH3'. The proposed diagnosis algorithm identifies the number corresponding to the faulty switch and stores it in flag '*ROCFSW1*' at instant *'tc1'* (Fig. 5.17). This action triggers the *SPDT-B* (Fig. 5.1) and the process of reconfiguration is initiated. At the end of the process, the *Leg-B* of the VSI is substituted by the additional *Leg-B'*, as explained in Section-5.2. Finally, another OC fault is inflicted on the switch CH5. In this case, the faulty *Leg-C* of the

VSI is substituted by the additional *Leg-C'*. Thus, this experiment clearly demonstrates that the proposed drive configuration is capable of achieving multiple-switch fault tolerance against both OC and SC faults.

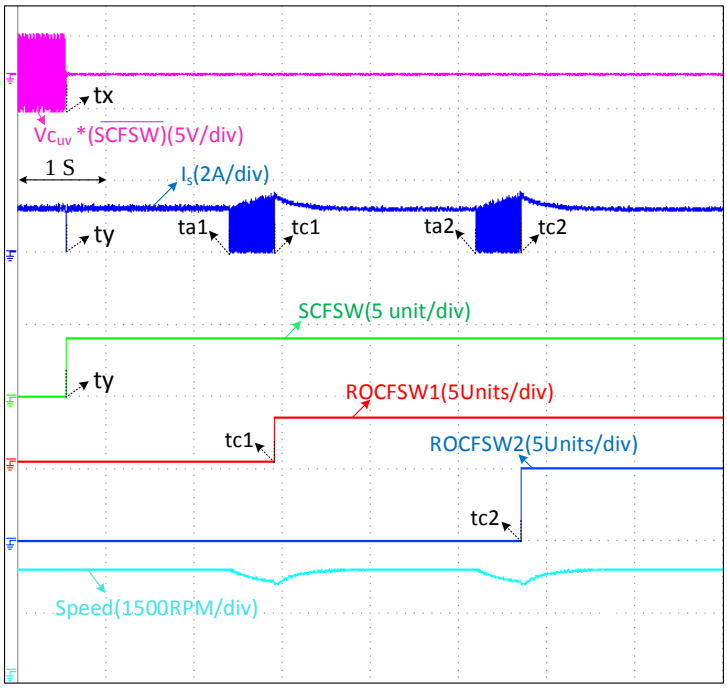


Fig. 5.17: Experimental results presenting the fault-tolerant drive operation for sequential SC fault in switch AL4, OC faults in switches BH3 & CH5

5.5 Feasibility Studies of the Proposed Power Circuit Configuration

Table-5.2 presents the comparative analysis of the proposed multiple-switch fault-tolerant BLDC motor drive topology vis-à-vis the other topologies reported in the earlier literature.

Cost analysis is carried out for the proposed multiple-switch fault-tolerant topology, which estimates the increased cost of the power circuit due to the additional components, which are needed to incorporate the feature of fault tolerance into the conventional BLDC motor drive. Though the proposed power converter needs three additional legs to achieve full-fault tolerance, it is an affordable proposition, as its raw material cost (RMC) is principally determined by the cost of sensors. It may be noted that the proposed power converter brings in a significant reduction in the number of sensors and auxiliary component requirements when compared to the fault-tolerant converter topologies presented in Chapters-2 & 3.

Table 5.2: Comparison of Different Topologies with the Proposed Topology

Topological features	Topology [70]	Topology [72]	Topology [73]	Proposed Topology
1. No. of switches in the inverter	6 switches (VSI) + 3 TRIACs	6 switches (VSI) + 6 TRIACs + 1 additional leg	12 switches	12 switches
2. Switch ratings	Rated motor voltage and current	Rated motor voltage and current	Rated motor voltage and twice the rated motor current	Rated motor voltage and current
3. Fault-diagnosis in additional switches	No	No	Yes	Not susceptible for faults
4. Fault tolerance	Only OCF	OCF, SCF	OCF, SCF	Multiple-switch OC/SC faults
5. Post-fault power/torque delivered	Rated power/torque	Rated power/torque	Rated power/torque	Rated power/torque
6. Motor rating	Designed for rated voltage and current	Designed for rated voltage and current	Designed for double the rated current	Designed for rated voltage and current
7. Auxiliary components	No	Buck converter + 3switches +1 fault protective leg	Buck converter + 1 SPDT switch + 1 fault protective leg	3 SPDT relays

Table 5.3: Cost Evaluation of Fault-Tolerant Drive Configuration (Indian Rs.)

Name of the equipment		Each unit cost (Rs./-)	No. of quantities	Total Cost (Rs./-)
(a) Motor (96 V, 3 KW BLDC motor)		31,780	1	31,780
(b) Cost of li-ion battery (12V, 60AH,720WH)		13,620	8	1,08,960
(c) Cost of Inverter with driver (with switch voltage and current safety factor taken as 2)	(c_1) Cost of proposed Inverter topology with driver	(159+306)	12	5,580
	(c_2) Cost of conventional VSI topology with driver	159+306	6	2,790
(d) Sensors	(d_1) Current sensor	1,870	1	1,870
	(d_2) Voltage sensor components (ISO124, TL084CN)	(894 + 13)	ISO124→3 TL084CN→1	2,695
(e) Auxiliary components (SPDT Relays)		341	3	1,023
Percentage of additional cost incurred w.r.t the conventional BLDC motor drive: $=\left(\frac{d_2+e+(c_1-c_2)+d1}{a+b+c_2}\right)*100\% = =\left[\frac{2695+1023+2790+1870}{31781+108960+2790}\right] * 100\% = 5.83\ \% \approx 6\%$				

From the cost analysis carried out in Table-5.3, it can be observed that the proposed multiple-switch fault-tolerant requires 6% additional cost compared to its conventional counterpart. In contrast, the single-switch fault-tolerant topologies reported in Chapters-2, 3 & 4 require additional costs of 9%, 11% & 5% respectively. Thus, with an increment of reasonable additional raw material cost to the conventional electric drive configuration, the drive is capable of achieving multiple-switch fault tolerance of the semiconductor switching devices, enhancing the reliability of the drive. This feasibility analysis shows that the proposed fault-tolerant topologies could find potential applications in the electric vehicle industry.

5.6 Summary

This Chapter proposes a multiple-switch fault-tolerant BLDC motor drive system, which could find applications where reliability is of paramount interest. The proposed topology is auto-reconfigurable and needs fewer additional components and sensors, causing a reduction in the raw material cost and an enhancement of reliability. The proposed power circuit configuration is capable of handling multiple OC and SC switch faults occurring in the VSI. The proposed multiple-switch fault-tolerant topology is capable of delivering rated power to the BLDC motor even after the occurrence of faults. This Chapter also presents algorithms, which diagnose multiple OC faults while avoiding spurious fault detection. The effectiveness of the presented multiple-switch OC fault-diagnosis and the associated post-fault circuit reconfiguration are experimentally verified. The cost analyses reveal that, compared to the conventional BLDC motor drives, the proposed fault-tolerant systems incur an affordable additional raw material cost of not more than 6%. Enhanced reliability with a low-cost overhead could make the proposed fault-tolerant BLDC motor drive system find applications for electric vehicles.

Chapter 6

Conclusion and Future Scope

Chapter 6

Conclusion and Future Scope

6.1 Conclusion

The principal focus of this thesis is to further the knowledge available on the design and development of the fault-tolerant BLDC motor drive configurations for EV applications. The thesis consists of five chapters of which, the first is introductory and the rest are contributory in nature.

Chapter-1, having reviewed the earlier literature available in this area, lays down the framework of the thesis. The motivation to embark on this research problem and the organization of the thesis are described.

The key contributions of this thesis are summarized as follows:

Exploiting the structural symmetry of the power circuit configuration, Chapter 2 shows that fault-tolerant capabilities can be imparted to the OEWBLDCM drive against both open circuited as well as the short-circuited faults. Chapter 2 proposes simple algorithms to diagnose these two faults for the OEWBLDCM drives. The scheme to diagnose the SCF is based on the fact that there exists a natural gap of 60 electrical degrees in a BLDC motor drive between the turn-off and turn-on times of the switching devices of any given phase leg. This observation paves the way to devise a diagnostic scheme, which is based on the sensing of the line voltages of the open-end winding BLDC motor. This scheme ensures that the fault is diagnosed before it can cause over currents through the switching devices. The SCF is sensed with simple and easily available components, without compromising on the issues of electrical isolation and bandwidth. The OEWBLDCM drive can be operated at reduced power following either of these two faults. This feature enhances the reliability of the drive. It is shown that the speed of the drive is controlled at a constant value following either OCF or SCF if it is intended to run the drive below half of its rated speed. A simple method of reconfiguring the power circuit is described, wherein the faulted inverter is reconnected to provide a switched neutral point. The charge available in the healthy battery bank connected to the faulted inverter is also utilized in the proposed drive. The cost analyses reveal that, compared to the conventional BLDC motor drives, the proposed fault-tolerant systems incur an affordable additional raw

material cost. The performance of the proposed fault-tolerant drive topology is verified using both simulation and experimental studies.

Chapter 3 proposes a dynamically reconfigurable OEWBLDCM drive configuration, wherein the post-fault reconfiguration of the power circuit and the reconnection of the batteries in series ensure that the BLDC motor is supplied with its rated power even after the development of either an OCF or an SCF in the dual inverter system. Even though such an agreeable situation arises due to the doubling of the voltage rating of the switching devices by a factor of '2', it would still be an affordable proposition for low-power EVs, as the total increase in the RMC (of only the propulsion system) is about 11% compared to the conventional BLDC drive, which does not offer the feature of fault tolerance. Compared to the OEWBLDC drive configuration proposed in Chapter 2, which achieves only 50% post-fault power delivery to the motor, the hike in the RMC is only 2% with the power circuit configuration proposed in Chapter 3, considering the costs of individual components based on bulk purchase.

Chapter 4 proposes a fault-tolerant BLDC motor drive topology for low-power EV applications. This power converter uses 3 bi-directional power devices, which are inactive in the normal mode of operation, enhancing its reliability. The proposed power converter, upon diagnosing either an OC or SC fault in any one of the switching devices of the VSI, automatically reconfigures itself by inserting these bidirectional switching devices to achieve the feature of fault tolerance. Cost analysis reveals that the drive configuration proposed in Chapter 4, owing to its employment of fewer sensors (compared to the drive configurations proposed in chapters 2 and 3), adds only 5% additional RMC to add the feature of fault tolerance to the conventional BLDC motor drive topology and offers a price-competent solution.

Chapter 5 proposes multiple-switch fault-tolerant BLDC motor drive systems, which could find applications where reliability is of paramount interest. The proposed topology of Chapter 5 is auto-reconfigurable and needs fewer additional components and sensors, causing a reduction in the raw material cost and an enhancement of reliability. The power circuit configurations proposed in Chapter 5 is capable of handling multiple OC and SC switch faults occurring in the VSI. The multiple-switch fault-tolerant topology proposed in Chapter 5 is capable of delivering rated power to the BLDC motor even after the occurrence of faults. Chapter 5 also presents algorithms, which diagnose multiple OC faults while avoiding

spurious fault detection. The effectiveness of the presented multiple-switch OC fault-diagnosis and the associated post-fault circuit reconfiguration are experimentally verified. The cost analyses reveal that, compared to the conventional BLDC motor drives, the proposed fault-tolerant systems incur an additional raw material cost of not more than 6%. Enhanced reliability with a low-cost overhead could make the proposed fault-tolerant BLDC motor drive system find applications for electric vehicles.

6.2 Future Scope

Based on the research done in this thesis, the recommendations for the future work are as follows:

i) The proposed fault-tolerant topologies and corresponding reconfiguration procedures can be further investigated for IM & PMSM drives.

ii) These fault-tolerant configurations can be extended for multi-phase BLDC motors drive which could ensure increased reliability of drive operation.

iii) The ideas from the presented fault-tolerant drive configurations can be integrated with the fault-tolerant strategies against the motor faults and power source failures which will enhance the drive's overall reliability and robustness.

iv) It’s an interesting proposition to apply modern control schemes such as predictive control for the fault-tolerant power circuit topologies employed in the present work.

v) The proposed fault-tolerant algorithm can be extended to sensorless drive operation, wherein the sector information required for the fault-diagnosis algorithm can be obtained from the back-EMF information.

Appendix-I

Description of the Experimental Prototype

Figure A.1 presents the photograph of the experimental prototype, which was developed to validate the algorithms of fault-diagnosis and the procedures of post-fault circuit reconfigurations for the fault-tolerant BLDC motor drive configurations proposed in this thesis.

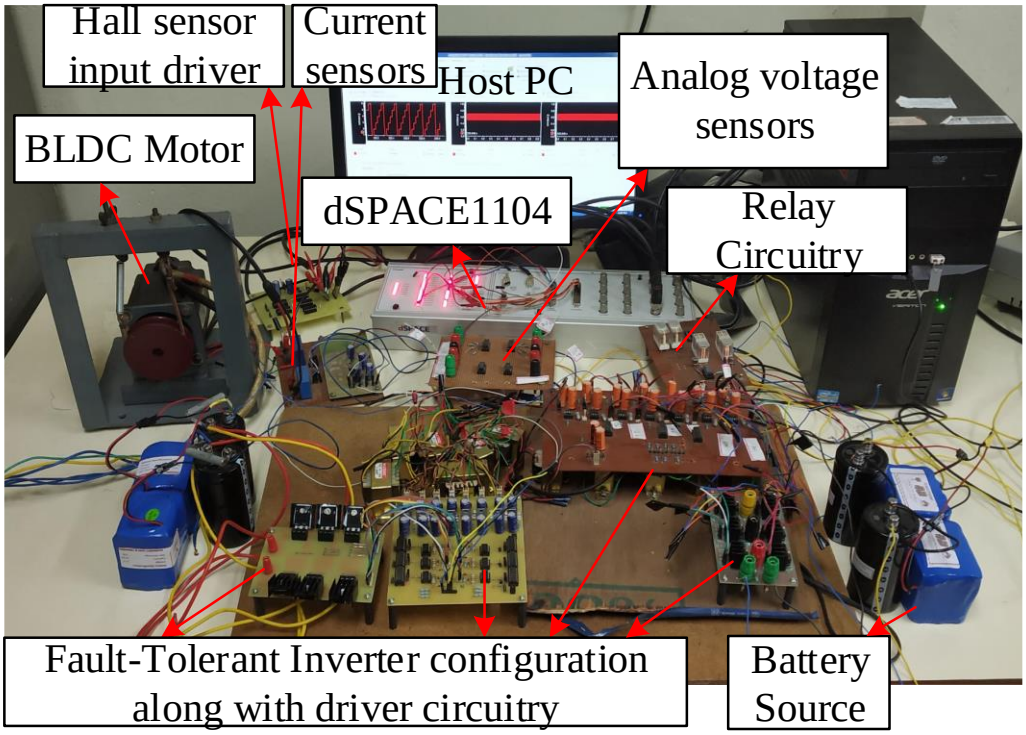


Fig. A.1: A view of the experimental set-up of fault-tolerant BLDC motor drive configuration

The line voltages required for diagnosing SC faults are obtained with analog voltage sensors, which consist of TL084CN-based differential amplifiers and a precision isolation amplifier, which are designed using ISO124. The DC-link currents required for diagnosing OC faults are sensed by using LA-55 current sensors. An existing star-connected BLDC motor was converted into an open-winding BLDC motor by opening the star-point. Table A.1 presents the comprehensive information regarding all components, which are used for experimentation.

Table A.1: Hardware Specifications of the Fault-Tolerant Drive Configuration

Motor Rated voltage	48 V
Motor Rated Torque	0.6 N-m
Motor Rated Speed	3200 Rpm
Motor Resistance per Phase	0.295 Ω
Motor Back-EMF constant	11.8 V/Krpm
Motor Rated Power	250 W
Motor Pair of Poles	4
Switch	ISL9V2040D3S
Driver (optocoupler)	A3120
Current Sensor	LA-55
Isolation Amplifier	ISO124
Differential Amplifier	TL084CN

The effectiveness of the proposed fault-diagnosing algorithms and the procedures of the post-fault circuit-reconnection are first assessed with simulation studies using the MATLAB/SIMULINK platform. Upon obtaining satisfactory results, the control scheme, realized in SIMULINK, was deployed onto the *dSPACE-DS1104* platform. The *dSPACE-DS1104* control platform produces the gating signals for the semiconductors and control signals for the steering switchgear. The *dSPACE-DS1104* control platform, which is interfaced with a host computer, is equipped with accessories such as the ADC and DAC channels that are needed to implement digital control systems. While ADCs convert analog current and voltage signals into their digital counterparts, DACs reconstruct the output of the *dSPACE-DS1104* control platform. The outputs of the DACs are connected to the digital oscilloscope to record the waveforms required for documentation.

The model is built after testing the control algorithm with Simulink that is interfaced with the *dSPACE-DS1104* control platform. After code generation and compilation for the model, the "*System Description File*" (with the .sdf extension) is loaded into the *dSPACE-DS1104* control platform, completing the process of "*building*". To facilitate the tasks of measurement and adjustment of variables in real-time, the system description file (.sdf) generated in the earlier step is exported to another software known as the "*Control Desk*". Thus, the entire operation of the proposed fault-tolerant drive configuration is monitored and controlled. Additionally, the gating signals applied to the switches can be controlled in real-time, facilitating the artificial creation of OC/SC switch fault conditions to validate the fault-tolerant drive operation. Table A.2 shows the specifications of the *dSPACE-DS1104* control platform.

Table A.2: dSPACE 1104 Specifications

Primary Processor	MPC8240, PowerPC 603e core, 250 MHz
Slave Processor	Texas Instruments' DSP TMS320F240
Muxed ADCs	4-Multiplexed ADCs, 16-Bit
ADCs	4-ADCs, 12-Bit
DACs	8-DACs, 16-Bit
Digital I/O	20-bit digital I/O
Incremental Encoder	2, 24-bit digital incremental encoders
Serial Interface	Serial UART (RS232, RS485 and RS422)
PCI Slot	32-bit PCI slot
PWM	one 3-phase PWM; four 1-phase PWM

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Publications

Journals (Accepted):

1. **P. H. Kumar**, S. Lakhimsetty and V. T. Somasekhar, "An Open-End Winding BLDC Motor Drive With Fault Diagnosis and Autoreconfiguration," in ***IEEE Journal of Emerging and Selected Topics in Power Electronics***, vol. 8, no. 4, pp. 3723-3735, Dec. 2020, doi: 10.1109/JESTPE.2019.2948968.

2. **Patnana, HK**, Veeramraju Tirumala, S, "A cost-effective and fault-tolerant brushless direct current drive with open-stator windings for low power electric vehicles," in ***International Journal of Circuit Theory and Applications,*** vol. 49, no. 9, pp. 2885– 2908, May 2021, https://doi.org/10.1002/cta.3048.

3. **P. H. Kumar** and V. T. Somasekhar, "An Enhanced Fault-Tolerant and Auto-Reconfigurable BLDC Motor Drive for Electric Vehicle Applications," in ***IEEE Journal of Emerging and Selected Topics in Industrial Electronics***, 2022, doi: 10.1109/JESTIE.2022.3196818 **(Early Access)**.

Journals (Under Review):

1. **P. H. Kumar**, V. T. Somasekhar, "A Low-Cost Fault-Tolerant BLDC Motor Drive for Low-Power EV Applications," in ***IEEE Journal of Emerging and Selected Topics in Industrial Electronics - Briefs*** *(under review).*