Investigation on Single-Phase Step-Up Multilevel Inverters for Photovoltaic Standalone Applications

Thesis
Submitted in partial fulfillment of the requirements
for the award of the degree of

Doctor of Philosophy
in
Electrical Engineering

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Dedicated to

My beloved Mother

APPROVAL SHEET

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DECLARATION

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ACKNOWLEDGMENTS

It gives me immense pleasure to express my deep sense of gratitude and thanks to my supervisor **Dr. B.L. Narasimharaju**, Associate Professor, Department of Electrical Engineering, National Institute of Technology Warangal, for his invaluable guidance, support, and suggestions. His knowledge, suggestions, and discussions helped me become a capable researcher. He has shown me the imaginative side of this wonderful and potential research area. His encouragement helped me to overcome the difficulties encountered in research as well in my life. I am extremely thankful to him to make me part of SPARC project, SERB-IMPRINT project and other collaborative research activities.

I am grateful to the **institute and other government agencies (SERB-DST, IMPRINT, SPARC and MoE, GoI)** for providing a great research facility, which immensely helped me to carry out the experimentation for my research work.

I wish to express my sincere thanks to **Prof. N. V. Ramana Rao,** Director, NIT Warangal for his official support and encouragement.

I am very much thankful to **Prof. M. Sailaja Kumari**, Head, Department of Electrical Engineering for her constant encouragement, support and cooperation.

I also express my sincere thanks to **Prof. V.T. Somasekhar** and **Prof. S. Srinivasa Rao**, former heads, Department of Electrical Engineering for their valuable suggestions, support and cooperation.

I take this opportunity to thank all my Doctoral Scrutiny Committee members, **Prof. D. M. Vinod Kumar**, Department of Electrical Engineering, **Prof. S. Srinivasa Rao**, Department of Electrical Engineering, **Dr. P. Selvi**, Assistant Professor, Department of Electrical Engineering and **Dr. P. Muthu,** Associate Professor and Head, Department of Mathematics for their detailed review, constructive suggestions and excellent advice during the progress of this research work.

I am grateful to **Prof. V.T. Somasekhar**, **Prof. S. Srinivasa Rao**, **Dr. A. Kirubakaran**, Assistant Professor, **Dr. A.V. Giridhar**, Assistant Professor, **Dr. Ch. Ramulu**, Assistant Professor, **Dr. G. Siva Kumar**, Assistant Professor, **Dr. Vinay Kumar T.**, Assistant Professor, for sharing the hardware equipment for my research work.

I also appreciate the encouragement from teaching and non-teaching members of Department of Electrical Engineering. They have always been encouraging and supportive.

I am indebted to Dr. Ratna Rahul Tupakula, Dr. Venu Sonti, Dr. V.V.K. Satyakar, Mr. Dharmesh Y., Mr. K. Hemasundar Rao, Dr. P Srinivas, Dr. K. Narendar Reddy, Mr. P Hemakumar, Mr. K. Ashok Kumar, Mr. M.F. Baba and Mr. Sumon Dhara for their brotherly care and unconditional support throughout my PhD journey.

I convey my special thanks to contemporary research scholars Dr.Vijaybabu K, Dr. U. Ramanjaneyulu, Dr. Ch. Kasi Ramakrishna Reddy, Dr. Hareesh M., Dr. Suresh L., Dr. K. V. Praveen Kumar, Dr. M. Santosh, Dr. A Pranay Kumar Mr. S. Ramkumar, Dr. K. Sateesh Kumar, Dr. Bhaskar Gupta, Dr. Dileep Krishna, Dr. B Laxman, Dr. K. Eswar, Mr. P Manoj, Mr. M. Kalyan Chakravarthi, Mr. Ch. Madhu Kishore, Dr. P Mounica, Dr. Rambabu M, Mr. K Srinivas, Mr. G. Ramesh, Mr. D. Ramesh, Mr. D. Satish Reddy, Mr. Chinmay Kumar Das, Dr. Vijay Vardhan Reddy and Mr. Sagar Petkar for being with me during my research journey.

I heartily thankful to institute health center staff and especially to **Dr. Srivastava** and **Dr. Anchoori Karthik** for being compassionate during my health emergencies.

I acknowledge my gratitude to all my teachers and colleagues at various places for supporting and co-operating with me to complete the work. I gratefully acknowledge my friends and extended family members **Jafar Sadik, K. Sriram, B. Swamy, D. Siva Kumar, K. Venkata Reddy, Y.V. Prashant** for continuous support and encouragement throughout my life.

I express my deep sense of gratitude and reverence to my beloved mother **Smt. S. Gangamma**, my grandmother **Smt. B. Dalamma**, my younger brother **S. Venu Babu** and other family members for their blessings, constant encouragement, shouldering the responsibilities and moral support rendered to me throughout my life, without which my research work would not have been possible.

ABSTRACT

In recent times, every nation is determined towards the increased use of renewable energy sources like solar, wind etc., to combat with the adverse environmental changes caused by the burning of conventional fossil fuels. Out of these, Photovoltaic (PV) technology is extremely evolved and accessible to all starting from house roof-top generation to large power plants in rural, urban and remote locations. The AC module configuration is a viable solution for low power PV application and helps to harvest maximum energy from PV either with or without grid facility. The desired features of inverter are voltage gain, compactness, low output voltage THD (Total Harmonic Distortion), efficient conversion and low cost. The conventional step-up inverters either with low frequency or high frequency transformer provide the required voltage gain. However, at low power operation the percentage of core losses are relatively high and results in reduced overall efficiency. Moreover, the presence of transformer leads to increased size and cost of the inverter. The conventional transformerless step-up inverters with front-end boost converter provide reduced size and cost, however the voltage gain is limited to 3. Moreover, the front-end boost converter process the rated power and a bulky DC-link capacitor is required to maintain the DC-link voltage. The step-up inverters with front-end DC-DC converter with floating DC-link is presented to reduce the capacitor size, however the voltage gain is limited to 3. Recent times, switched capacitor (SC) based step-up inverters are popular due to their improved voltage gain, multilevel output with lesser THD and better efficiency at low output power. However, the parallel charging and series discharging technique in SC based inverters demand a bulky capacitors for low frequency and high power applications to avoid voltage drooping issues. Further, these inverters with higher voltage levels require more number of capacitors and switching components, which results in increased system size. Additionally, the SC based inverters draw impulse current during capacitor charging intervals, which demands high current rated devices. To address the impulse charging current issue, a bulky inductor is used in the charging path of the quasi resonant switched capacitor (QRSC) based inverters. The impedance offered by the resonant inductor will reduce the peak of the charging current. However, the other merits and demerits of SC based inverters and the QRSC based inverters are similar. Hence, there is a requirement of step-up inverter, which provides reduced

capacitor charging current, improved voltage gain and higher voltage levels while utilizing less components and small size capacitors.

To meet the above objectives, a new boost DC-link integrated multilevel inverter (MLI) is realized by the integration of two two-level boost DC-link converters with a hybrid H-bridge inverter using two symmetrical voltage sources. The proposed topology with proper selection of capacitor voltage levels can produce 9-, 11- and 13-level outputs and provides a maximum voltage gain of 3.

To further improve the voltage gain and number of voltage levels, a MLI with four level boost DC-link basic unit is proposed. With two basic units and two symmetrical voltage sources it can produce 17-level output voltage and provide a voltage gain of 4. In asymmetrical mode of operation, the same configuration is able to produce 31-level output.

The proposed 13-level and 17-level MLIs are required to power from two sources. However, for PV AC module applications the step-up inverter configurations that utilize single source and provide higher voltage gain are essential. Hence, an improved buck-boost integrated MLIs with single-source is proposed. By choosing the appropriate voltage ratios of capacitor voltages with respect to the source voltage, one of the proposed converter can produce an 11-level output voltage with a voltage gain of 5 and other converter produce a 13-level output voltage with a voltage gain of 2 respectively.

The buck-boost converters presented in the proposed inverters are only process fractional part of total energy. All of the proposed MLIs utilize nearest level stair case modulation, thus produce a low frequency common mode voltage, which results in reduced leakage currents. The capacitors presented in the proposed step-up inverters are being charged at high switching frequency to the desired voltage values. Thus, provide reduced component count, capacitor size, charging current and eliminate voltage drooping issue. Therefore, the developed step-up inverters are suitable for standalone PV applications.

Contents

ACKNOWLEDGMENTS **i**

ABSTRACT **iii**

List of Figures **viii**

List of Tables **xiv**

Abbreviations & Symbols **xvi**

1 Introduction **2**

1.1 General introduction 2

1.2 PV systems 2

1.2.1 Grid connected PV systems 4

1.2.2 Off-grid PV systems 4

1.3 Single phase step-up inverters 5

1.3.1 Step-up inverters with transformer 6

1.3.2 Step-up inverters without transformer 7

2 Literature Review on Single-phase Transformerless Inverters **9**

2.1 Introduction 9

2.2 Two-level inverter with front-end boost converter 9

2.3 Step-up inverter with improved front-end boost converter 10

2.4 Multilevel inverter with front-end boost converter 11

2.5 Single-stage differential boost inverters 12

2.5.1 Conventional DBIs 12

2.5.2 Clamped DBIs: 13

2.5.3 Cascaded DBIs: . . . 17
2.6 Switched capacitor multilevel inverters . . . 19
2.7 Quasi-resonant switched capacitor multilevel inverters . . . 21
2.8 Research gaps & Motivation . . . 23
2.9 Thesis objectives . . . 25
2.10 Thesis contributions . . . 25
2.11 Thesis organization . . . 26
2.12 Summary . . . 27

3 Boost DC-link Integrated Cascaded Multilevel Inverter 29
3.1 Introduction . . . 29
3.2 Working and operating principle of the proposed BDIMLI . . . 31
3.3 Comparative analysis . . . 42
3.4 Experimental Results . . . 46
3.5 Summary . . . 50

4 Improved Boost DC-link Integrated Cascaded Multilevel Inverter 52
4.1 Introduction . . . 52
4.2 Working and operating principle of the proposed IBDIMLI . . . 52
4.3 Comparative Analysis . . . 59
4.4 Experimental Results . . . 63
4.5 Summary . . . 70

5 Single-source Buck-boost Integrated 13-level Inverter 72
5.1 Introduction . . . 72
5.2 Working and operating principle of the proposed SBMLI . . . 72
5.3 Comparative analysis . . . 80
5.4 Experimental Results . . . 82
5.5 Summary . . . 84

6 Improved Single-source Buck-boost Integrated High gain 11-level Inverter 86
6.1 Introduction . . . 86

6.2 Working and operating principle of the proposed ISBMLI 86
6.3 Comparative analysis 93
6.4 Experimental Results 94
6.5 Summary 100

7 Conclusions and future Scope of research **102**
7.1 Conclusions 102
7.2 Future scope of research work 104

Bibliography **106**

List of publications **116**

List of Figures

1.1 Block diagram of grid connected PV system during (a) the presence of sunlight (b) the absence of sunlight; and off-grid PV system during (c) the presence of sunlight (d) the absence of sunlight 3
1.2 Different grid connected PV configurations. 3
1.3 Block diagram of inverter for renewable applications. 5
1.4 Block diagram of single phase step-up inverters: (a) with low-frequency transformer (b) with high-frequency transformer (c) two-stage transformerless (d) single-stage transformerless 6

2.1 Circuit diagram of two stage two-level step-up inverter with front-end boost converter 10
2.2 Circuit diagram of improved time sharing two stage two-level step-up inverter with front-end boost converter 11
2.3 Circuit diagram of two stage multilevel step-up inverter with front-end boost converter 12
2.4 Block diagram of conventional DBIs 13
2.5 Circuit diagrams of simple DBI topologies developed using a) boost b) buck-boost c) couple boost d) SC converters as basic units 14
2.6 Model waveforms of type DBIs with decoupled full cycle modulation 15
2.7 Circuit diagrams of DBIs with by-pass switches: a) Improved boost DBI b) split inductor DBI-I c) split inductor DBI-II d) Improved buck-boost 16
2.8 Model waveforms of type: DBIs with (a) decoupled half cycle modulation [**?**] (b) decoupled dual mode half cycle modulation [**?**] 17
2.9 Circuit diagram of type: C DBIs formed by cascade connection of (a) boost & quasi Z source (b) boost & buck-boost 18

2.10 Model waveforms of type C DBIs with integrated full cycle modulation 18
2.11 Circuit diagram of SC (a) basic unit (b) basic unit when capacitor is getting charged (c) basic unit when capacitor is getting discharged 19
2.12 Model waveforms of basic unit of switched capacitor based inverters: (a) when R_o is high and duration of level-2 is short, (b) when R_o is low and duration of level-2 is short, (c) when R_o is high and duration of level-2 is long 20
2.13 Extended high step-up switched capacitor multilevel inverter 21
2.14 Circuit diagram of quasi resonant SC (a) basic unit (b) basic unit when capacitor is getting charged (c) basic unit when capacitor is getting discharged 22
2.15 Model waveforms of basic unit of quasi resonant SC based inverters 22

3.1 Two-level Boost DC-link Converter Unit. 30
3.2 Equivalent circuit of TBDC during (a) level-1 (b) level-2 while inductor charging (c) level-2 while inductor discharging 30
3.3 TBDC model waveforms: output voltage, switch gate pulses, capacitor voltage and inductor current during level-1 and level-2 operations. 30
3.4 Typical output voltage waveform of (a) SCMLI basic cell (b) TBDC 31
3.5 Schematic diagram of the proposed Boost DC-link Integrated Cascaded MLI. . 33
3.6 Model waveform of the 13-level output voltage. 34
3.7 S_{b1} & S_{b2} gate pulses:(a) logic diagram, (b) model waveforms. 34
3.8 Equivalent circuit of BDIMLI for peak output voltage. 35
3.9 Different modes of operation of the proposed BDIMLI for 13-level operation from +0V_{dc} to +6V_{dc}. 36
3.10 Different modes of operation of the proposed BDIMLI for 13-level operation from -0V_{dc} to -6V_{dc}. 37
3.11 Design characteristics for 9-level operation: (a) L_{B1} & L_{B2} versus R_o at f_s = 10kHz, 30kHz & 50kHz (b) $C_{1,min}$ & $C_{2,min}$ versus R_o at f_s = 10kHz for different ripple voltages and (c) $C_{1,min}$ & $C_{2,min}$ versus P_{max} with f_s = 10kHz and V_1=50V. 41
3.12 Design characteristics for 13-level operation: (a) L_{B1} & L_{B2} versus R_o at f_s = 10kHz, 30kHz & 50kHz (b) $C_{1,min}$ & $C_{2,min}$ versus R_o at f_s = 10kHz for different ripple voltages and (c) $C_{1,min}$ & $C_{2,min}$ versus P_{max} with f_s = 10kHz and V_1=50V. 42

3.13 Efficiency curves of proposed BDIMLI. 45
3.14 Experimental prototype of proposed BDIMLI. 46
3.15 Experimental waveforms of load voltage v_o, load current i_o, inductors L_1, L_2 currents (i_{L1}, i_{L2}), capacitors C_1, C_2 voltages (v_{c1} and v_{c2}) and dc voltage source currents (i_1 and i_2) for (a) 9-level operation and (b) 13-level operation. 47
3.16 Experimental waveforms of 13-level operation: (a) PIV of S_2, S_6, S_{L1}, S_{b1} (b) PIV of S_4, S_5, S_{L2}, S_{b2} 48
3.17 Experimental waveforms of 13-level operation: (a) CMV (b) DC source leakage currents i_{lg1} and i_{lg2}. 48
3.18 Dynamic behavior of the proposed BDIMLI with step change in load conditions: no-load to rated R load, R load to R-L load, and R-L load to R load for (a) 9-level operation and (b) 13-level operation. 49
3.19 Harmonic spectrum of load voltage v_o for (a) 9-level operation and (b) 13-level operation. 49

4.1 Proposed basic four-level unit: (a) circuit diagram (b) equivalent block diagram 53
4.2 Equivalent circuit of FLU: (a) 0 level (b) V_x (c) v_{cx} (d) $V_x + v_{cx}$. (Blue and green lines represents the inductor charging and discharging paths) 54
4.3 Generalized structure of the IBDIMLI: (a) block diagram (b) equivalent circuit for peak voltage level 57
4.4 Proposed IBDIMLI circuit for x=2 57
4.5 Variation of critical inductance and capacitance with respect to load resistance for symmetrical operation of the IBDIMLI at different switching frequencies . . 58
4.6 Comparison of (a) power loss of switches of IBDIMLI (b) total power loss distribution and (c) efficiency characteristics of proposed MLI with recent boost MLIs at different output powers. 62
4.7 Block diagram of control logic: (a) SPWM control (b) NLC (c) closed-loop PI controller for capacitor voltage V_{Cx}. 63
4.8 Modulation scheme of the proposed MLI for (a) SPWM control (b) NLC control 64
4.9 Experimental prototype of the proposed IBDIMLI. 65

4.10 Experimental waveforms of 17-level operation with SPWM: (a) v_o, i_o, v_{c1} & v_{c2} for a step change in R load (b) v_o, i_o, v_{c1} & v_{c2} for a step change in load i.e., R-load to R-L load (c) i_1, i_2, i_{L1} & i_{L2} (d) voltage of switches S_1, S_{C1}, S_{V1} & S_{B1} (e) voltage of switches S_2, S_{C2}, S_{V2} & S_{B2} (f) v_{ar}, v_{br} & v_{CMV} 66

4.11 Experimental waveforms of 17-level operation with NLC: (a) v_o, i_o, v_{c1} & v_{c2} for a step change in R load (b) v_o, i_o, v_{c1} & v_{c2} for a step change in load i.e., R-load to R-L load (c) i_1, i_2, i_{L1} & i_{L2} (d) voltage of switches S_1, S_{C1}, S_{V1} & S_{B1} (e) voltage of switches S_2, S_{C2}, S_{V2} & S_{B2} (f) v_{ar}, v_{br} & v_{CMV} 67

4.12 Experimental waveforms of 31-level operation with NLC: (a) v_o, i_o, v_{c1} & v_{c2} for a step change in R load (b) v_o, i_o, v_{c1} & v_{c2} for a step change in load i.e., R-load to R-L load (c) i_1, i_2, i_{L1} & i_{L2} (d) voltage of switches S_1, S_{C1}, S_{V1} & S_{B1} (e) voltage of switches S_2, S_{C2}, S_{V2} & S_{B2} (f) v_{ar}, v_{br} & v_{CMV} 68

4.13 Experimental waveforms of harmonic spectrum of load voltage and load current with R load and R-L load for (a) 17-level operation with SPWM (b) 17-level operation with NLC (c) 31-level operation with NLC 69

5.1 Proposed 13-level MLI 73

5.2 Equivalent circuits of SBMLI from +0 V_{dc} to +6 V_{dc} 74

5.3 Equivalent circuits of SBMLI from -0 V_{dc} to -6 V_{dc} 75

5.4 Proposed MLI model waveform 76

5.5 Equivalent circuit of the proposed MLI at +6 V_{dc}/-6 V_{dc} 77

5.6 Block diagram of closed loop control and pulse generation of BBCs 78

5.7 Comparison of source and BBCs: (a) power share at each level (b) power share at peak level (c) total energy share. 80

5.8 Experimental setup of the SBMLI 82

5.9 SBMLI's experimental results: (a) v_o, i_o, v_{C1} and v_{C2} for sudden variation in R load (i.e., 314 W to 212 W) (b) v_o, i_o, v_{C1} and v_{C2} for sudden variation in load type (i.e., 314 W to 255 VA, 0.79 power) (c) capacitors C_1 & C_2 currents and ripple voltages (d) i_1, i_{L1} and i_{L2}. 82

5.10 SBMLI's voltage waveforms of: (a) S_1, S_2, S_3 and S_8 (b) S_5, S_6, S_7 and S_{10} (c) v_{ar}, v_{br} and CMV. 83

5.11 THD of v_o and i_o for (a) & (b) 314 W R load (c) & (d) 255 VA, 0.79 power factor R-L load 83

6.1 Equivalent circuit of the ISBMLI for the peak output voltage level 87
6.2 Model waveform of ISBMLIs with nearest level control 88
6.3 Equivalent circuits of ISBMLI basic unit from 0 V_{dc} to 5V_{dc} levels. 89
6.4 Equivalent circuit of the ISBMLI for the peak output voltage level 90
6.5 Design characteristics of (a) critical inductances L_{B1} and L_{B2} (b) minimum capacitances $C_{1,min}$ and $C_{2,min}$ for 5% ripple voltage with respect load current at different switching frequencies 90
6.6 Block diagram of closed loop control and pulse generation of BBCs 91
6.7 Power processed by DC source and BBCs at different operating voltage levels . 92
6.8 Experimental setup of the ISBMLI 95
6.9 Experimental waveforms of the ISBMLI: (a) load voltage (v_o), load current (i_o) and capacitor voltages (v_{C1} and v_{C2}) during step change in R load for (i.e., 510 W R load to 260 W R load) (b) v_o, i_o, v_{C1} and v_{C2} during step change in load type (i.e., 510 W R load to 339 VA, 0.8 power factor R-L load) (c) capacitors C_1 & C_2 currents and ripple voltages (d) source current i_1, inductor currents i_{L1} and i_{L2} (e) zoomed version of source current i_1, inductor currents i_{L1} and i_{L2}. . . 96
6.10 Experimental waveforms of the ISBMLI: (a) v_o, i_o, v_{C1} and i_{C1} during step change in RL load (i.e., 228 VA, 0.94 power factor RL load to 339 VA, 0.8 power factor R-L load) (b) v_o, i_o, v_{C2} and i_{C2} during step change in RL load (i.e., 228 VA, 0.94 power factor RL load to 339 VA, 0.8 power factor R-L load) (c) v_o, i_o, rectifier output voltage and output currents v_R and i_R during step change in non-linear load (i.e., 213 W to 405 W) 97
6.11 Experimental waveforms of the ISBMLI: (a) voltages of switches S_1, S_2, S_{C1} and S_{C2} (b) voltages of switches S_{V1}, S_{V2}, S_{V3} and S_{H1} (c) pole voltages v_{ar}, v_{br}, CMV and leakage current i_{lg}. 98
6.12 ISBMLI: (a) Power loss distribution and (b) efficiency characteristics for 11-level operation at different output power conditions. 98

6.13 Experimental waveforms of the ISBMLI: (a) & (b) harmonic spectrum of v_o and i_o for 339 VA, 0.8 power factor R-L load respectively (c) & (d) harmonic spectrum of v_o and i_o for 510W R load respectively (e) & (f) harmonic spectrum of v_o and i_o for 405 W non-linear load respectively 99

List of Tables

2.1 Summary of single-phase transformerless step-up inverters 24

3.1 Capacitor voltages, and step-up ratios for 9, 11 & 13-level operation of BDIMLI with $V_1 = V_2 = V_{dc}$ 34
3.2 Switching States of the proposed BDIMLI for 9-evel operation 38
3.3 Switching States of the proposed BDIMLI for 11-level Output 39
3.4 Switching States of the proposed BDIMLI for 13-level operation 40
3.5 Comparison of Proposed BDIMLI with Existing MLI Topologies with symmetrical DC sources for 9-level output ($P_o = 1000$W, $V_{o,max} = 200$V and $f_o = 50$Hz) 43
3.6 Comparison of Proposed BDIMLI with Existing MLI Topologies with symmetrical DC sources for 13-level output ($P_o = 1000$W, $V_{o,max} = 300$V and $f_o = 50$Hz) 43
3.7 Cost comparison of the proposed BDIMLI with other step-up MLI topologies for 13-level operation at P_o = 1000W 44
3.8 Loss analysis of the Proposed BDIMLI for 9 and 13-level operation using PSIM 45
3.9 Specification & Design Parameters of BDIMLI 46
3.10 Comparison of experimental THD of the proposed BDIMLI with the MLI presented in [1] 50

4.1 Switching States of Basic FLU 54
4.2 Switching States of proposed IBDIMLI for 17 Level operation 56
4.3 Comparison of IBDIMLI with existing MLI topologies 59
4.4 Cost comparison of IBDIMLI with existing 7-level boost inverter topologies . . 61
4.5 Specification & Design Parameters of the IBDIMLI for experimental study . . . 65

5.1 Look-up table of SBMLI for 13-level operation with V_1 = 3 V_{dc}, $V_{c1} = V_{dc}$ and V_{c2} = 2 V_{dc} 76

5.2 Comparison of the SBMLI and recent 13-level MLIs 81
5.3 Specifications of the proposed 13-level MLI 81

6.1 Switching States of basic unit of ISBMLI 88
6.2 Comparative study of the ISBMLI with the recent 11-level SCMLIs 93
6.3 Comparative study of the ISBMLI and the recent SCMLIs in generalized operation 94
6.4 Specifications and Design Parameters of ISBMLI for 11-level operation 95
6.5 Power loss distribution of ISBMLI at different power ratings 97

Abbreviations & Symbols

$\%P_{c1}$	Percentage of peak power processed by each BBC-1
$\%P_{c1}$	Percentage of peak power processed by each BBC-2
$\%P_{S,max}$	Percentage of peak power processed by source
Δv_C	Ripple voltage of capacitor C
ΔV_{c1}	Ripple voltage of capacitor C_1
ΔV_{c2}	Ripple voltage of capacitor C_2
ΔV_{cx}	Ripple voltage of capacitor C_x
δ	Duty cycle of BBC
δ_x	Duty cycle of BBC x
δ_1	Duty cycle of BBC-1
δ_2	Duty cycle of BBC-2
ω_{ch}	Natural frequency of the charging circuit
C_p	Parasitic capacitance of PV panel
$C_{1,min}$	Minimum capacitance of capacitor C_1
$C_{2,min}$	Minimum capacitance of capacitor C_2
$C_{min,SC}$	Minimum capacitance of capacitor C in SC unit
C_{min}	Minimum capacitance of capacitor C
C_{xmin}	Minimum capacitance of capacitor C_x

$car1$	Carrier voltage 1
$car2$	Carrier voltage 2
E_C	Energy transfered to the capacitor C
E_L	Energy stored in the inductor L
E_S	Energy processed by the source
E_{c1}	Energy processed by BBC-1
E_{c2}	Energy processed by BBC-2
E_{Total}	Total energy delivered to load in quarter cycle
f_o	Frequency of the output voltage
f_s	Switching frequency of BBCs
f_{tri}	Frequency of carrier voltage
i_C	Instantaneous current through capacitor C
i_L	Instantaneous current through inductor L
I_o	Average output current
$I_{C,peak}$	Peak current the capacitor C
$I_{CP,QRSC}$	Peak current the capacitor C in QRSC cell
$I_{CP,SC}$	Peak current the capacitor C in SC cell
i_D	Instantaneous current through swich D
$I_{LB.peak}$	Peak current of inductor L in BCM
i_{lg1}	Leakage current 1
i_{lg2}	Leakage current 2

I_{Lpeak}	Peak current of the inductor L
$I_{o,max}$	Peak Value of output current
i_o	Instantaneous output current
i_{Sb}	Instantaneous current through swich S_b
k	Voltage level
L_B	Critical inductance of inductor L
L_{B1}	Critical inductance of inductor L_1
L_{B2}	Critical inductance of inductor L_2
L_{ch}	Inductor in QRSC cell
L_{xB}	Critical inductance of inductor L_x
m_{a1}	Amplitude modulation index 1
m_{a2}	Amplitude modulation index 2
n	Step-up ratio BBC
n_x	Step-up ratio of BBC-x
n_1	Step-up ratio of BBC-1
n_2	Step-up ratio of BBC-2
N_{cap}	Number of capacitors
N_{dc}	Number of DC sources
N_{dio}	Number of diodes
N_{dri}	Number of drivers
N_{ind}	Number of inductors

N_{lev}	Number of levels
$N_{max,asymm}$	Number of voltage levels in asymmetric mode of operation
$N_{max,symm}$	Number of voltage levels in symmetric mode of operation
N_{swi}	Number of switches
P_o	Average output power
$P_{1,avg}$	Average voltage of source 1
$P_{2,avg}$	Average voltage of source 2
P_{c1}	Maximum power delivered by capacitor C_1
P_{c2}	Maximum power delivered by capacitor C_2
P_{cond}	Total conduction losses
P_{cx}	Maximum power shared by capacitor C_x
P_{lc}	Total passive component power losses
$P_{o,max}$	Maximum value of output power
$P_{S,max}$	Peak power of source
P_{swi}	Total switching Losses
R_o	Output resistance
R_p	Parasitic resistance of PV panel
R_{c1}	Effective resistance of BBC-1
R_{c2}	Effective resistance of BBC-2
R_{cx}	Effective resistance of BBC-x
R_C	ESR of the capacitor C

R_D	ON state resistance of diode D
$R_{S,ON}$	ON state resistance of switch S
$R_{SP,ON}$	ON state resistance of switch S_P
T	Timepriod of the output voltage
T_S	Time period of the inductor L current
Tk	Duration of k^{th} level
V_1	Source 1 voltage
V_2	Source 2 voltage
v_d	DC-link voltage
V_o	RMS value of output voltage
V_x	Voltage magnitude of source x
v_{ar}	Pole a voltage
v_{br}	Pole a voltage
V_{c1}	Average voltage of capacitor C_1
v_{c1}	Instantaneous voltage of capacitor C_1
V_{c2}	Average voltage of capacitor C_2
v_{c2}	Instantaneous voltage of capacitor C_2
v_{CMV}	CMV of the MLI
v_{cx}	Instantaneous voltage of capacitor C_x
V_c	Average voltage of capacitor C
V_D	Forward voltage drop of diode D

V_{IN}	Source voltage
v_L	Instantaneous voltage across the inductor L
v_{mod}	Modulation voltage
$V_{o,peak}$	Peak value of output voltage
v_{o1}	Basic unit-1 output voltage
v_{o2}	Basic unit-2 output voltage
v_{ox}	Instantaneous output voltage of basic unit x
v_o	Instantaneous output voltage
v_{ref}	Reference voltage
v_{tri}	Carrier voltage
x	Number of basic units cascaded
AC	Alternating current
asym	symmetrical voltage sources
BBC	Buck-boost converter
BCM	Boundary conduction mode
BDIMLI	boost DC-link integrated multilevel inverter
CCM	Continuous conduction mode
CMV	Common mode voltage
Conv-1	Basic unit-1
Conv-2	Basic unit-2
CSDC	Current Spikes During Charging

CVD	Capacitor voltage drooping
DBI	Differential boost inverter
DC	Direct current
DCM	Discrete conduction mode
ESR	Equivalent series resistance
FLU	Four level unit
IBDIMLI	improved boost DC-link integrated cascaded multilevel inverter
ISBMLI	Improved single-source buck-boost integrated multilevel inverter
LGC	Level generation circuit
MLI	Multilevel inverter
NLC	Nearest level control
PV	Photovoltaic
QRSC	Quasi-resonant switched capacitor
RMS	Root mean square
SBMLI	ingle-source buck-boost integrated multilevel inverter
SC	Switched capacitor
SCMLI	Switched capacitor multilevel inverter
SPWM	Sinusoidal pulse width modulation
sym	symmetrical voltage sources
TBDC	Two-level boost DC-link converters
TBDC-1	Two-level boost DC-link converter-1

TBDC-2	Two-level boost DC-link converter-2
THD	Total harmonic distortion
TSV	Total switch voltage

Chapter 1

Introduction

Chapter 1

Introduction

1.1 General introduction

The global trend of urbanization and population growth compelling every country towards more energy generation and handling of the consequences. Majority of the world's energy is generated from burning fossil fuels like coal, diesel and petrol [2]. Power generation from conventional sources is polluting air, water bodies and causing serious global warming issues. The prices of these sources are dependent on atmosphere and political factors hence, highly unpredictable. In recent times the awareness on environmental problems forcing every nation towards the increased use of renewable energy sources like solar, wind, geothermal and tidal etc. Out of these, wind and solar energy sources are available everywhere and occupied the majority of renewable energy generation [3, 4]. The overall installation and maintenance cost of the wind energy system is high compared to solar energy systems [3]. The Photovoltaic (PV) technology is extremely evolved and accessible to all starting from house roof-top generation to large power plants in rural, urban and remote locations. Hence, the PV based power generation is an attractive solution to electrify the remote locations, where the installation of transmission lines or transport of conventional fuels are expensive.

1.2 PV systems

The PV power generation is highly variable and intermittent [5, 6] due to the dependence upon the climate conditions such as, irradiance of the sunlight, temperature and season etc., which results in unreliable power supply to the connected electrical loads. To harvest the maximum available energy from PV panels and also, to provide reliable power supply to the connected loads, there are two types [7, 8] of PV systems are in practice, namely

1. Grid connected PV systems
2. Off-grid PV systems

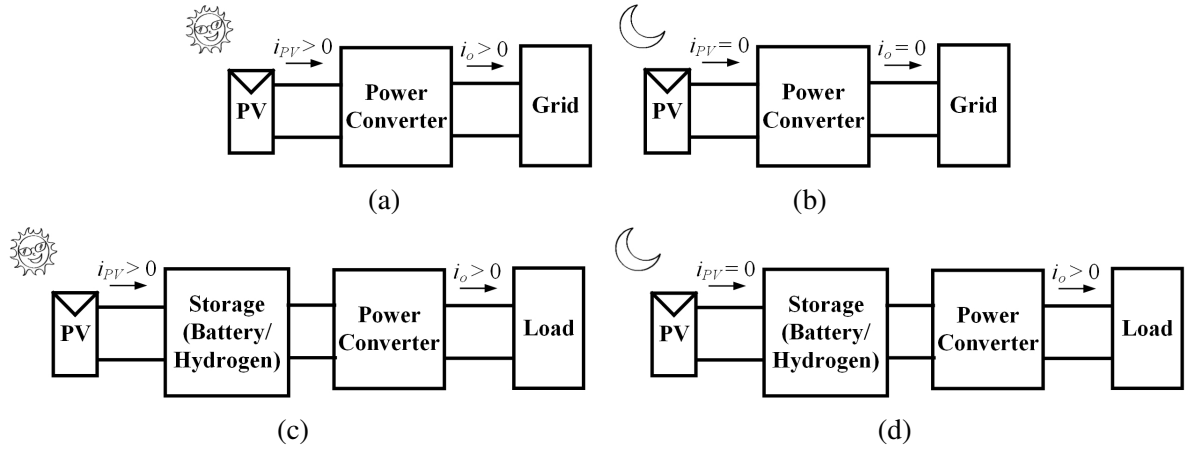


Figure 1.1: Block diagram of grid connected PV system during (a) the presence of sunlight (b) the absence of sunlight; and off-grid PV system during (c) the presence of sunlight (d) the absence of sunlight

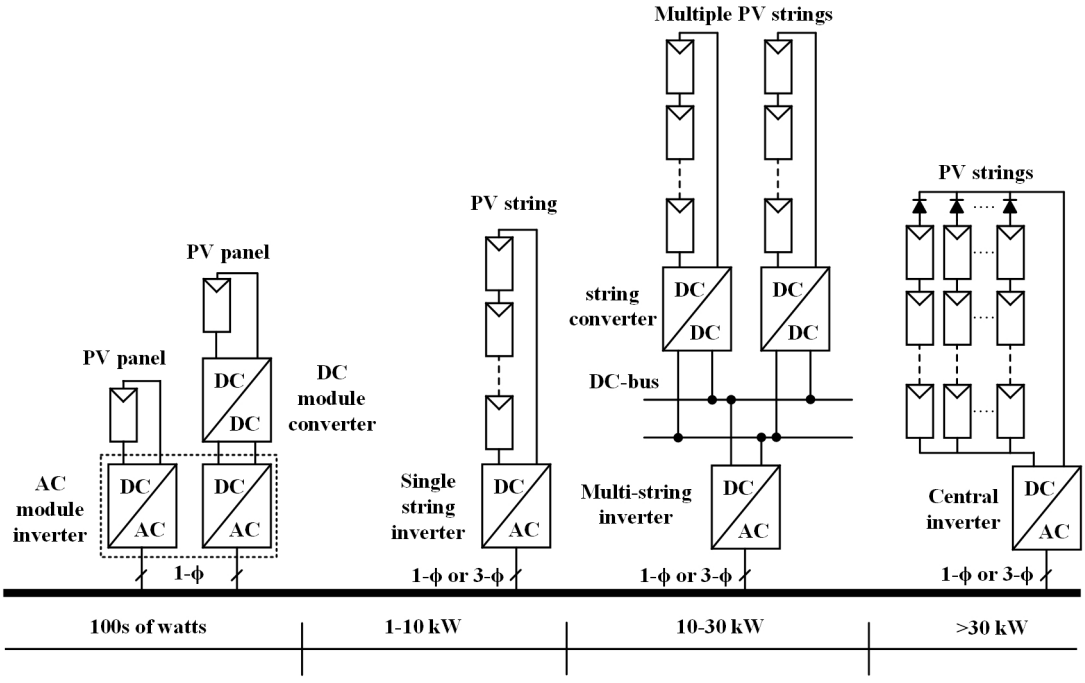


Figure 1.2: Different grid connected PV configurations.

The block diagrams of grid connected and off-grid PV systems are depicted in Figure 1.1. during the presence and absence of sunlight.

1.2.1 Grid connected PV systems

The grid connected operation of the PV shown in Figures 1.1a and 1.1b will improve the reliability and harvest the maximum energy from the PV panels to the grid. The operating power range of grid connected PV systems can be varied from hundreds of watts to tens of kilo-watts and the different grid connected PV configurations [9] are shown in Figure 1.2. They are broadly classified as central inverters, multi-string inverters [10, 11], single string inverters [12, 13] and module inverters [14–17]. The central and multi-string PV systems are used to process the PV energy at a large scale in industrial and PV power-plant applications. The single string and module structures are widely used for commercial and residential roof top applications. The partial shading conditions of PV array will affect the maximum power to be extracted in central and string based inverters. In contrast to the string inverters, the module inverters are immune to partial shading issues and provide high modularity, thus provides scope for further research.

1.2.2 Off-grid PV systems

The power generation from conventional energy sources is difficult and non-economical in remote locations such as rural, forest and islands with no grid facility [3,4]. Hence, the power generation from PV is a cost effective alternative and also, helps to preserve the sensitive eco system of the remote places. However, the absence of the grid and intermittent nature of the PV source affects the reliability of the power supply to the connected electrical appliances. To address this issue, PV with storage elements such as battery and hydrogen gas can be used to improve the reliability as shown in Figures 1.1c and 1.1d. The stored hydrogen gas can be converted to electrical energy by using fuel cell and power electronic converter. The surplus power from PV source will be stored in the storage devices and the stored energy will be delivered to the loads when power from PV is either absent or insufficient. Usually, the terminal voltage of PV, batteries and fuel cells are at low magnitude and the majority of the loads operates at high magnitude AC (alternate current) voltages. As the power rating of the off-grid PV systems are less than 1 kW, the module converters are the key structure to provide modularity and efficient conversion [18–20]. Hence, a high gain inverter is essential to convert low voltage DC (either from PV or from battery or fuel cell) to high voltage AC and the block diagram of inverters for

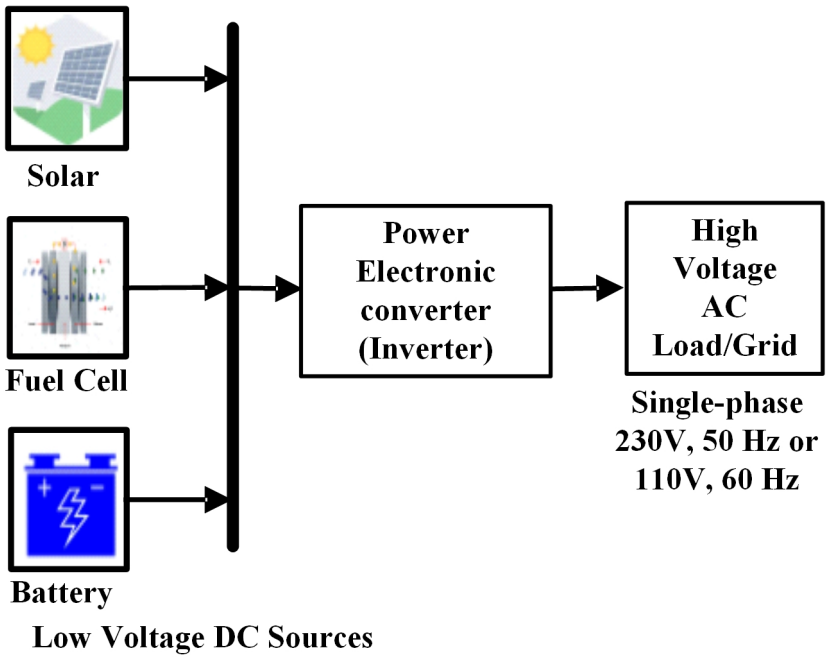


Figure 1.3: Block diagram of inverter for renewable applications.

renewable PV applications is depicted in Figure 1.3.

1.3 Single phase step-up inverters

The voltage step-up can be achieved by using various techniques such as, step-up transformer and front DC-DC converters etc. Based on the usage of transformer, the step-up inverters used for PV applications can be categorized as follows [20–25] and the respective block diagrams are depicted in Figure 1.4.

1. Step-up inverters with transformer
   (a) Step-up inverter with low or power frequency transformer
   (b) Step-up inverter with high frequency transformer
2. Step-up inverters without transformer
   (a) Two-stage transformerless step-up inverters
   (b) Single-stage transformerless step-up inverters

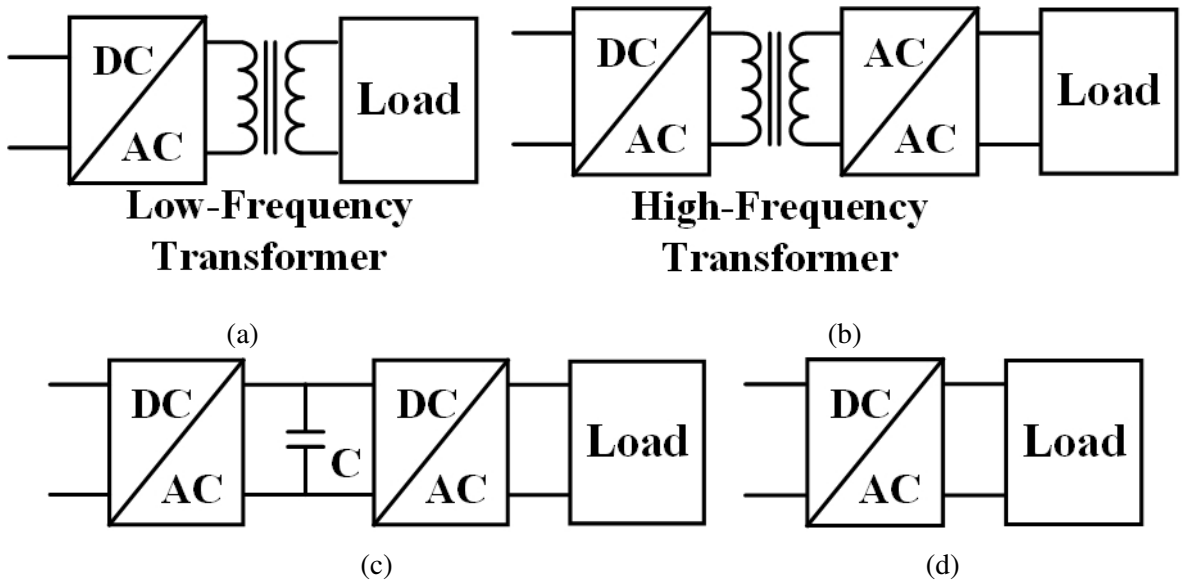


Figure 1.4: Block diagram of single phase step-up inverters: (a) with low-frequency transformer (b) with high-frequency transformer (c) two-stage transformerless (d) single-stage transformerless

1.3.1 Step-up inverters with transformer

The step-up inverters with transformer utilize a step-up transformer to step up the voltage and the transformer can be either low-frequency or high-frequency.

1.3.1.1 Step-up inverters with line-frequency transformer

The block diagram of the step-up inverter with line-frequency transformer is depicted in Figure 1.4a. Here, the inverter converts the low-magnitude DC voltage into low-magnitude low-frequency AC and then the step-up transformer will converts the low-magnitude low-frequency AC into high-magnitude low-frequency AC. With simple operation, it provides required voltage gain and galvanic isolation, however it requires a bulky line frequency transformer which results in increased cost and volume of the inverter.

1.3.1.2 Step-up inverters with high-frequency transformer

The block diagram of the step-up inverter with high-frequency transformer [26–35] is depicted in Figure 1.4b. Here, the inverter in the first stage converts the low-magnitude DC voltage into low-magnitude high-frequency AC and then the high frequency step-up transformer will

converts the low-magnitude high-frequency AC into high-magnitude high-frequency AC. The second stage converter converts high-magnitude high-frequency AC in to high-magnitude low-frequency AC. Though, the inverter process the energy in multiple stages, the utilization of high frequency transformer relatively reduces the cost and volume of the inverter compared to the inverter with low frequency transformer.

For low power applications, the percentage core losses of transformers presented in step-up inverters with transformer are relatively high, which results in reduced overall efficiency.

1.3.2 Step-up inverters without transformer

The step-up inverters without transformer, use a non isolated boost network to achieve required voltage gain. Based on the number of power conversion stages, which are further classified as two stage and single-stage transformerless inverters.

1.3.2.1 Two stage transformer less inverter

The block diagram of the two stage transformerless inverter [36–39] is depicted in Figure 1.4c. The first stage of this inverter coverts the low-magnitude DC voltage into high-magnitude DC and second stage converts the high-magnitude DC into high-magnitude low-frequency AC. The operation of this inverter is simple, however the front end DC-DC converter has to process the rated power. Hence, the cascade operation of two converters decreases the overall efficiency.

1.3.2.2 Single stage transformer less inverter

The block diagram of the single stage transformerless inverter [21, 40–45] is depicted in Figure 1.4d. The inverter directly converts the low-magnitude DC voltage into high-magnitude low-frequency AC in single stage. Thus, results in improved efficiency compared to the two stage transformerless inverters.

In summary, the transformerless step-up inverters do not provide galvanic isolation, however they provide better efficiency, reduced cost and size compared to the step-up inverters with transformer [20]. Thus, the research is mainly focused on transformerless step-up inverters for PV stand alone applications.

Chapter 2

Literature Review on Single-phase Transformerless Inverters

Chapter 2

Literature Review on Single-phase Transformerless Inverters

2.1 Introduction

This chapter presents a comprehensive review of various single-phase transformerless step-up inverters suitable for PV standalone applications. The output voltage of PV panel, fuel-cell and battery are of low magnitude DC voltage (less than 60 V). Usually, the majority loads work with high magnitude AC voltage (110 V/60 Hz or 230 V/50 Hz). To transfer the energy from the low voltage DC sources to the loads operating at high voltage AC, the inverter should posses the following features

- High Voltage gain
- Compactness
- Low output voltage THD (Total harmonic distortion)
- Efficient conversion
- Low cost

2.2 Two-level inverter with front-end boost converter

The circuit diagram of the two stage two-level step-up inverter with front-end boost converter [46–49] is depicted in Figure 2.1. The front-end boost converter increases the DC voltage magnitude and the second stage H-bridge network converts the high-magnitude DC into high-magnitude low-frequency AC. The front-end boost converter needs to process the rated power and a bulk capacitor is required to maintain a stiff DC-link voltage. The H-bridge inverter presented in the second stage produce two-level output, which result in high output voltage THD. Hence, requires a large filter to suppress the harmonic content of the inverter

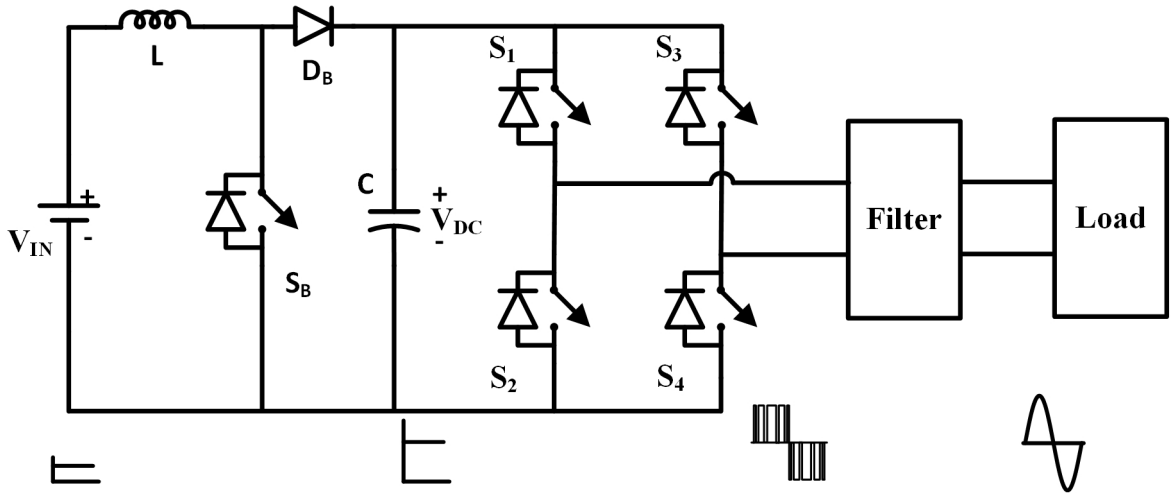


Figure 2.1: Circuit diagram of two stage two-level step-up inverter with front-end boost converter

output voltage. The efficiency of boost converter is less at higher duty cycles operation, which results in limited voltage gain.

2.3 Step-up inverter with improved front-end boost converter

The circuit diagram of the improved time sharing two stage two-level step-up inverter [36] with front-end boost converter is depicted in Figure 2.2. The front-end boost converter only operates whenever the required output voltage absolute value is greater than the input voltage and remains idle for the rest of time. Thus, the boost converter process only the fractional part of rated power and reduces the switching and conduction losses of the DC-DC converter. As shown in the figure 2.2, the inverter requires a pulsating DC-link, therefore relatively a small DC-link capacitor is sufficient. The switches in H-bridge operates with SPWM, whenever the required output voltage absolute value is lesser than the input voltage and operates with square wave modulation for the rest of time. The output voltage THD is relatively minimized, thus, the filter size is moderately reduced. The overall efficiency of the inverter is improved with time sharing operation.

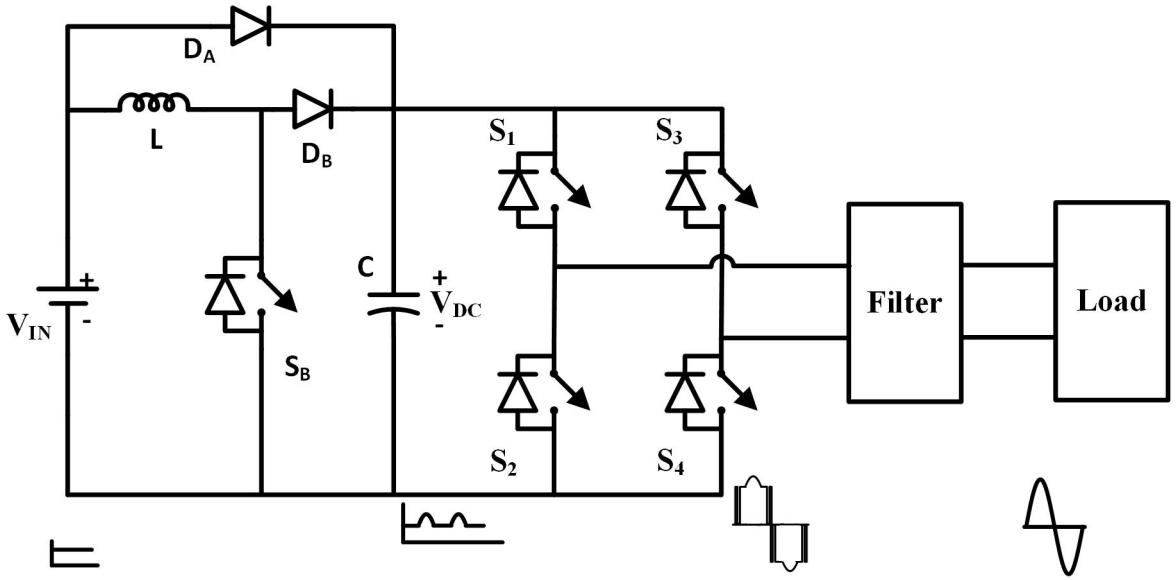


Figure 2.2: Circuit diagram of improved time sharing two stage two-level step-up inverter with front-end boost converter

2.4 Multilevel inverter with front-end boost converter

The circuit diagram of the two stage step-up multilevel inverter (MLI) with front-end boost converter [39] is depicted in Figure 2.3. Here, the conventional two-stage two-level inverters are cascaded to get multilevel output voltage. By increasing the number of cascaded units, the number of voltage levels can be increased to produce low output THD and reduce or eliminate the filter requirement. However, it requires increased number of components and bulky capacitors to main stiff DC-link voltages.

In summary, the inverters with front-end boost converter [36,39], the first stage increases the DC voltage magnitude and the second stage converts the high-magnitude DC into high-magnitude low-frequency AC. The front-end boost converter has to process the rated power and a bulky capacitor is required to maintain a stiff DC-link voltage. The H-bridge inverter presented in the second stage produce two-level output [36], which result in high output voltage THD. Hence, requires a large filter to suppress the harmonic content of the inverter output voltage. The efficiency of boost converter is less at higher duty cycles operation, hence this topology provides limited voltage gain.

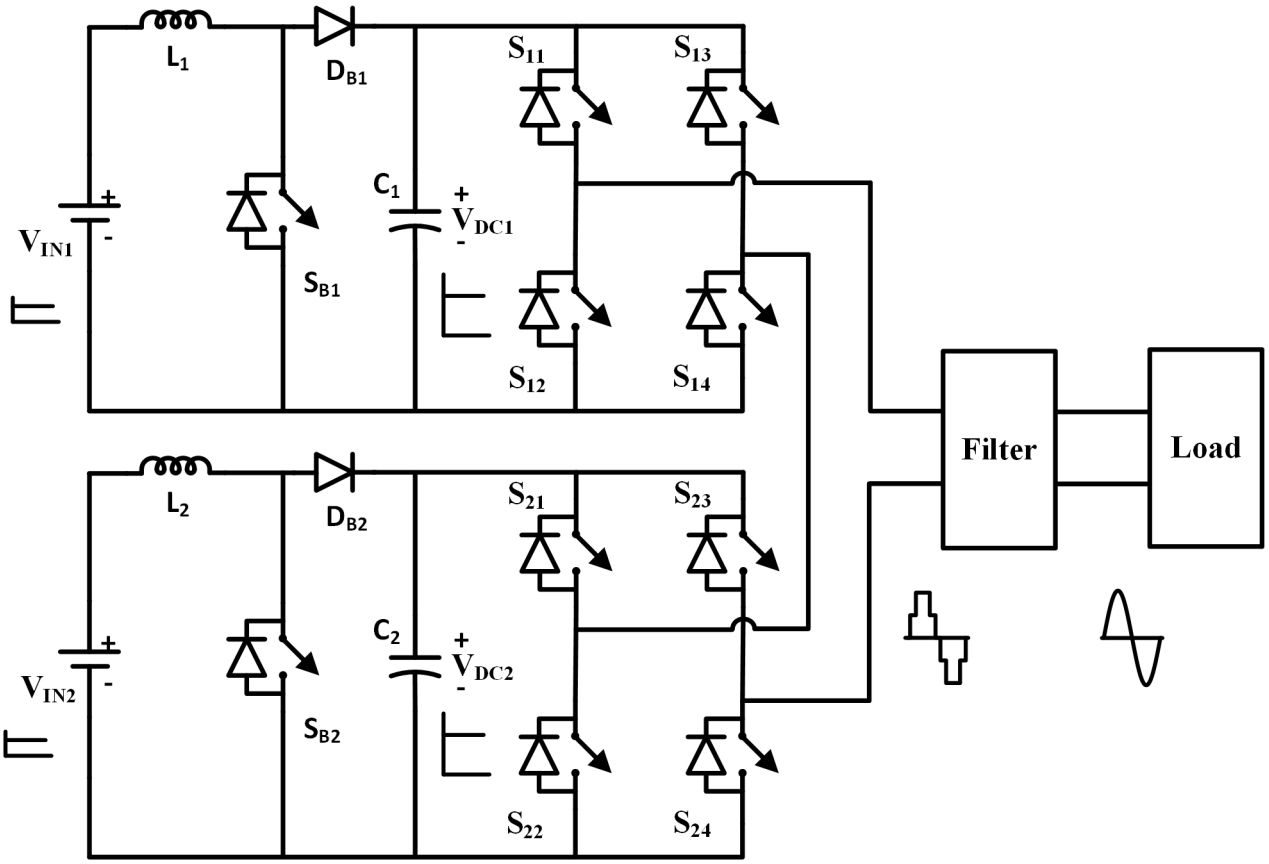


Figure 2.3: Circuit diagram of two stage multilevel step-up inverter with front-end boost converter

2.5 Single-stage differential boost inverters

The block diagram of the differential boost inverter (DBI) is as shown in Figure 2.4, in which the converter-1 and converter-2 are two identical boost/buck-boost DC-DC converters and are energized from a DC source V_{IN}. v_{o1} & v_{o2} are the respective output voltages of DC-DC converters, which are 180 degree out of phase to each other and differentially connected to produce DBI's output voltage v_o. Different DBI topologies reported in literature [50–61], which are discussed as follows:

2.5.1 Conventional DBIs

The block diagram of conventional DBIs [50–56] are illustrated in Figure 2.4. The DBI [50] shown in Figure 2.5a is formed by the differential connection of two conventional non isolated boost DC-DC converters. Similarly, the DBI [53] shown in Figure. 2.5b is formed

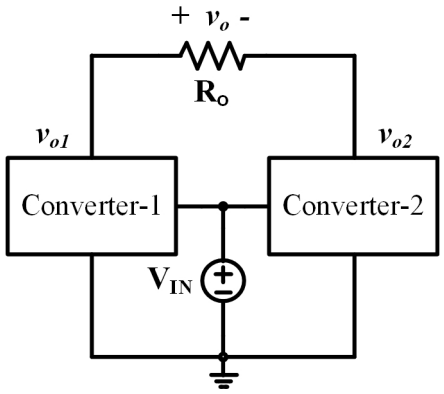


Figure 2.4: Block diagram of conventional DBIs

by using two simple non isolated buck-boost converter (BBC) topologies. DBIs [50, 53] are prone to shoot through problems in real time operation and needs dead time, which results in reduced voltage gain. In addition, the DBIs produce significant power loss, voltage and currents stresses at higher duty cycles to achieve higher step-up ratios. Hence, efficiency is less and not suitable for high step-up PV inverters. DBI with coupled inductors [54] as shown in Figure 2.5c is presented to provide higher gain with lower duty ratios. The turns ratio can be increased to achieve higher gain, but leads to increased device voltage stress due to leakage inductance of the coupled inductor. Generalized DBI with SC network [56] as shown in Figure 2.5d, in which the voltage gain can be improved with increased number of SC cells. SC DBI provides reduced voltage stress in contrast to the other DBIs [50,53,54], however requires more component count, which increases the size and cost .

Even though the construction and operation of these topologies are simple, all the switches operate at higher switching frequency and the inductors carry the current all the time. Thus, the overall switching and conduction losses are high and results in poor efficiency. The model waveforms of conventional DBIs with decoupled full cycle modulation (DFCM) are shown in Figure 2.6. The DFCM offers decoupled as well as full cycle operation ability to the DC-DC converters of the DBI.

2.5.2 Clamped DBIs:

In clamped DBIs [57–59], one of the DC-DC converter is clamped to a certain voltage (usually either V_{IN} or 0 volts), while the other converter generates AC voltage in a half cycle and

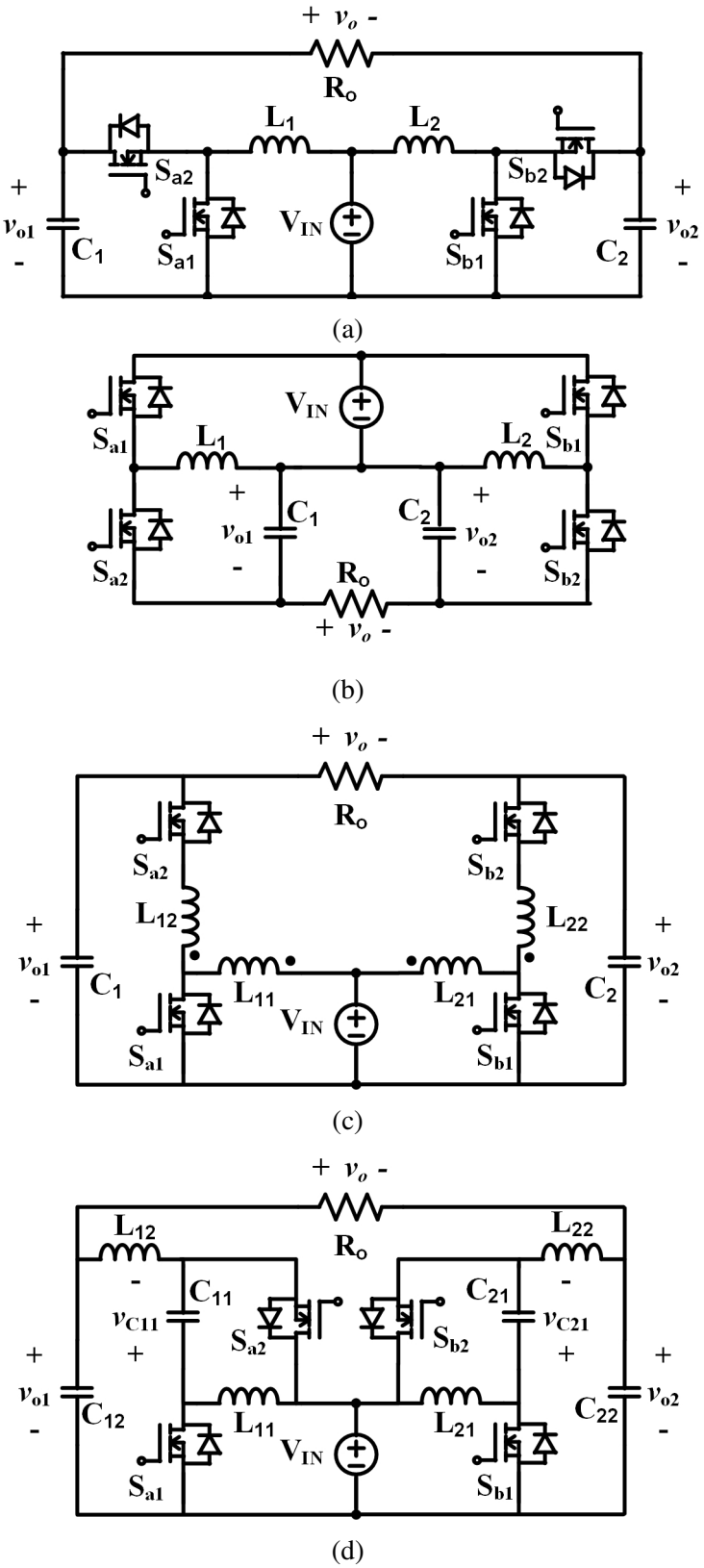


Figure 2.5: Circuit diagrams of simple DBI topologies developed using a) boost b) buck-boost c) couple boost d) SC converters as basic units

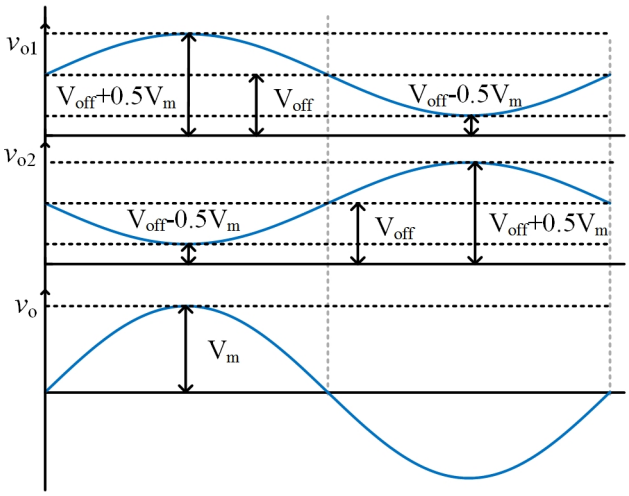
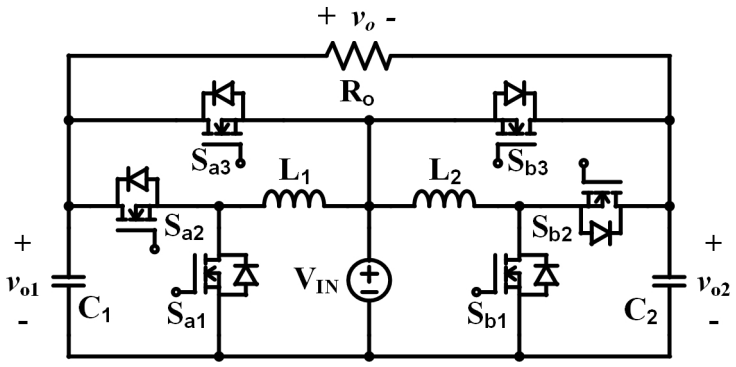


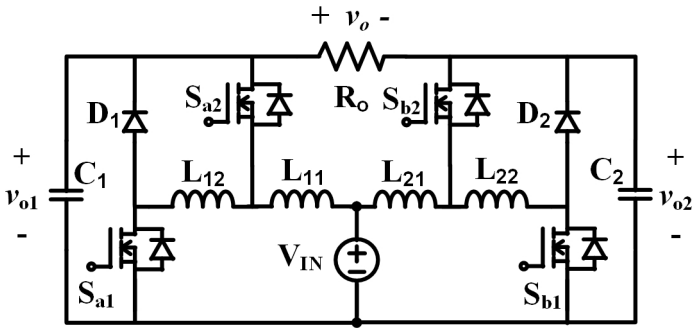
Figure 2.6: Model waveforms of type DBIs with decoupled full cycle modulation

vice-versa. For the clamping of voltage, additional switches are utilized. Improved DBI [57], which is presented with addition of by-pass switches to conventional boost DBI as depicted in Figure 2.7a. When the by-pass switch is ON, the respective converter stops DC-DC conversion and clamps to input voltage. Thus, reduces the switching losses and inductor winding losses, which results in improved efficiency. Two DBI topologies with split inductor technique [58] are presented as shown in Figure 2.7b & 2.7c. The topology shown in Figure 2.7b is capable to serve unity power factor loads only, while the second topology can handle reactive power control. Though, the number of utilized inductors count is higher than the other DBI topologies, the total magnetic volume is less (i.e., low value inductor utilized), which reduces overall size of the DBI. In these topologies, two switches operate at low switching frequency and other operate at high switching frequency. Also, these are free from shoot through issues and provide reduced voltage and current stresses.

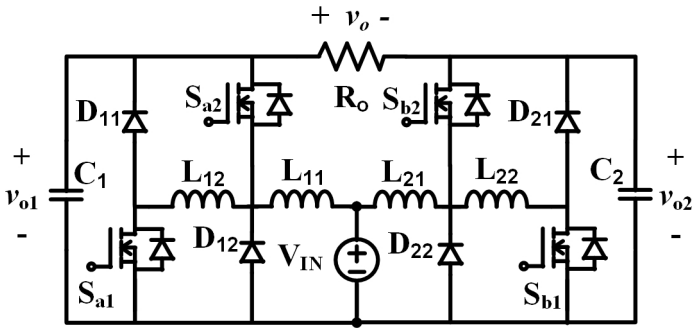
Modified buck-boost based DBI [59] as shown in Figure 2.7d is presented with addition of two more switches to the DBI. Unlike the other DBI topologies, the DC-DC converters of this DBI clamp to zero volts. Thus, well utilizes the buck capability of the buck boost converter. Also, it implements two mode modulation i.e., to generate output voltage magnitude less than the input voltage it operates in buck mode otherwise in boost mode, which results in reduced switching stresses. Here also some switches operates at lower frequency while other at higher frequency, hence reduces switching losses and improves the overall efficiency. Though, the two mode modulation helped to reduce the device ratings, the buck mode needs filter at the output



(a)



(b)



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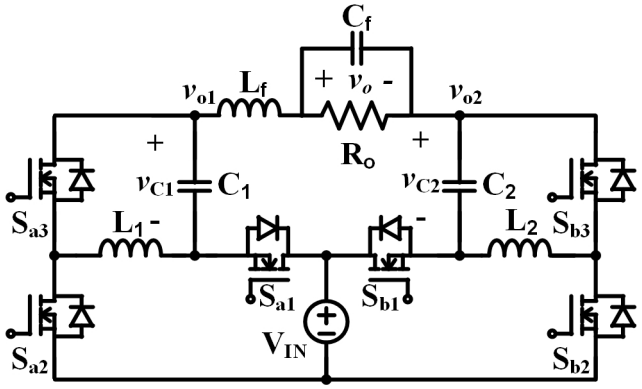


(d)

Figure 2.7: Circuit diagrams of DBIs with by-pass switches: a) Improved boost DBI b) split inductor DBI-I c) split inductor DBI-II d) Improved buck-boost

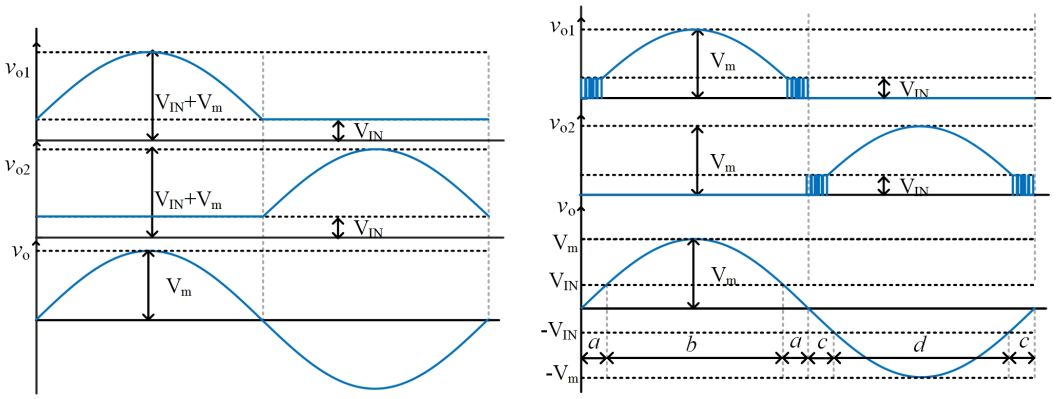


Figure 2.8: Model waveforms of type: DBIs with (a) decoupled half cycle modulation [**?**] (b) decoupled dual mode half cycle modulation [**?**]

to attenuate the higher order harmonics.

The model waveforms of DBIs [57, 58] with decoupled half cycle modulation are depicted in Figure 2.8a and for DBI [59] with decoupled dual mode half cycle modulation are depicted in Figure 2.8b.

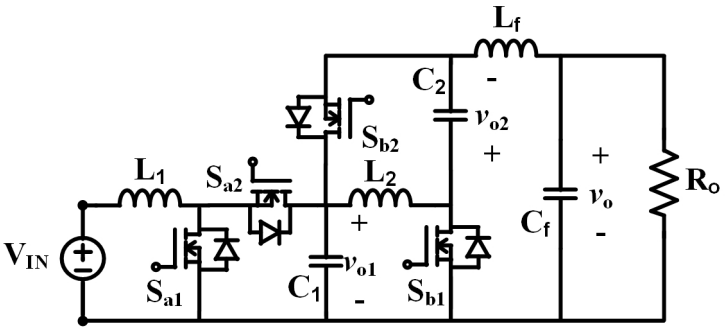
2.5.3 Cascaded DBIs:

In cascaded DBIs [60–62], one of the DC-DC converter's output fed to another DC-DC converter as input, whose outputs are differentially connected to produce output AC voltage.

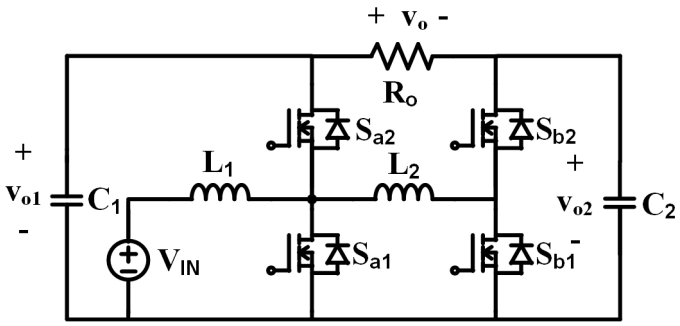
The cascaded DBI [60] as shown in Figure 2.9a is presented by the cascade connection of boost converter and quasi Z-source converter. In average sense, the output voltage is difference of the converters output voltages at any instant.

Similarly, another cascaded DBI [61] as shown in Figure 2.9b is presented, which is the cascaded connection of boost and BBCs. Unlike DBI [60], it does not need any output filter.

The model waveforms of DBIs [60,61] with integrated full cycle modulation are depicted in Figure 2.10. The common connection of both the output ground and source negative terminal helps to eliminate the leakage current problems in PV grid tie applications. However, due to the cascade operation of these DBIs, the voltage drop in the first stage causes further drop in next stage output. Thus, the positive and negative peaks of output voltage are not same and creates DC offset. Additionally, the inductor L_1 carries larger current compared to the inductor L_2.



(a)



(b)

Figure 2.9: Circuit diagram of type: C DBIs formed by cascade connection of (a) boost & quasi Z source (b) boost & buck-boost

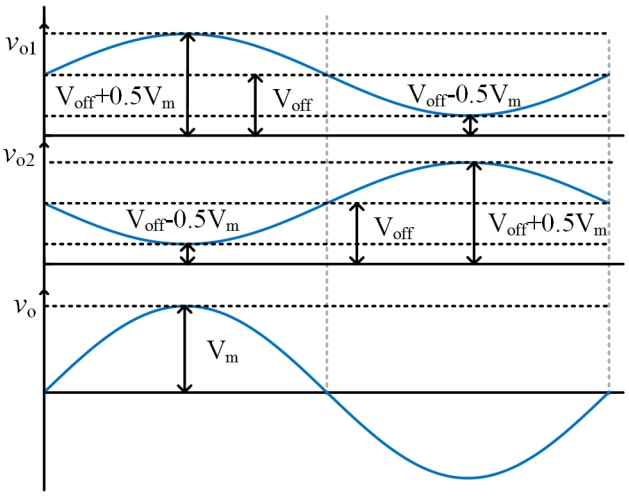


Figure 2.10: Model waveforms of type C DBIs with integrated full cycle modulation

2.6 Switched capacitor multilevel inverters

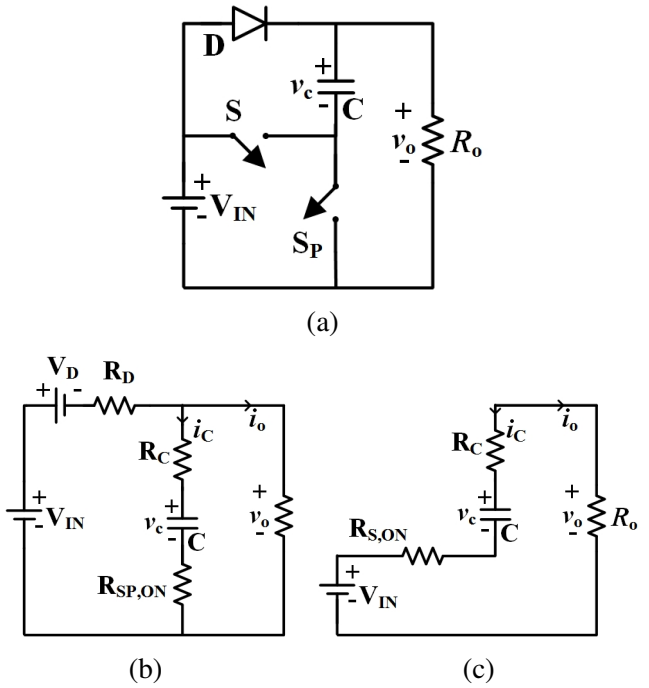


Figure 2.11: Circuit diagram of SC (a) basic unit (b) basic unit when capacitor is getting charged (c) basic unit when capacitor is getting discharged

The circuit diagram of basic unit presented in switched capacitor (SC) based transformerless inverters [63–68] is shown in Figure 2.11a. When switch S_P is ON, capacitor C gets charged to input voltage, which provides output voltage equals to input voltage and the equivalent circuit is shown in Figure 2.11b. R_C is the equivalent series resistance (ESR) of the capacitor C; $R_{SP,ON}$ & R_D are the equivalent on state resistances of the switch S_P & diode D; and V_D diode D forward voltage drop. When switch S with its on state resistance $R_{S,ON}$ is turned ON, the capacitor C gets discharged. Hence, output voltage equal to sum of input and capacitor voltages as indicated in equivalent circuit shown in Figure 2.11c. The basic unit can produce two-level output if the capacitor voltage is maintained close to the input voltage. But, the ripple voltage of capacitor C (Δv_C) depends upon the value of capacitance, load resistance (R_o) and duration of the level-2 in which capacitor is being discharged. The minimum capacitance ($C_{min,SC}$) required to maintain the ripple voltage is expressed as follows

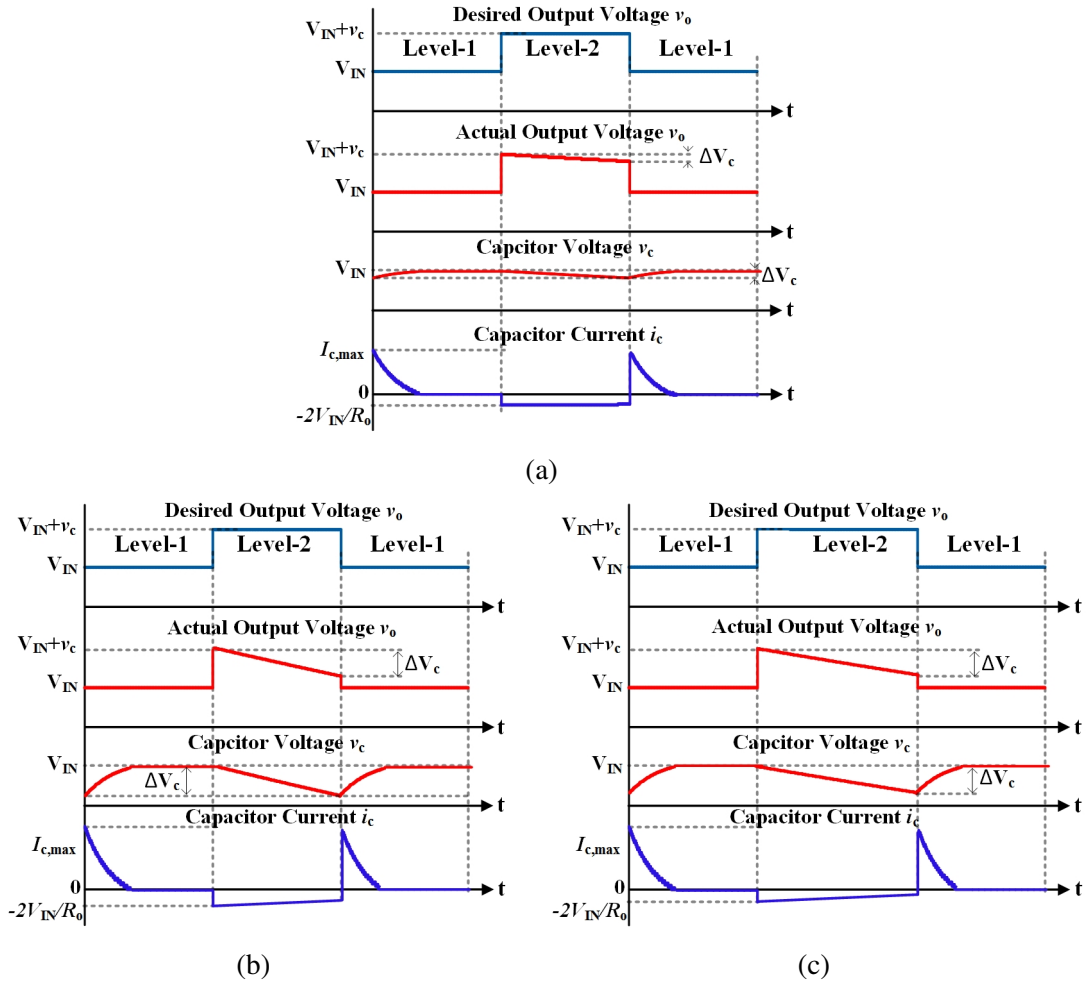


Figure 2.12: Model waveforms of basic unit of switched capacitor based inverters: (a) when R_o is high and duration of level-2 is short, (b) when R_o is low and duration of level-2 is short, (c) when R_o is high and duration of level-2 is long

$$C_{min,SC} \propto \frac{1}{\Delta v_C f_o R_o} \tag{2.1}$$

where f_o is the frequency of the output voltage.

At the beginning of level-1, the capacitor C is charged as resistance offered by the charging path i.e., $R_C + R_{SP,ON}$ is very less, hence an impulse charging current is drawn from the source. The peak of charging current ($I_{CP,SC}$) depends upon the ripple voltage and the resistance

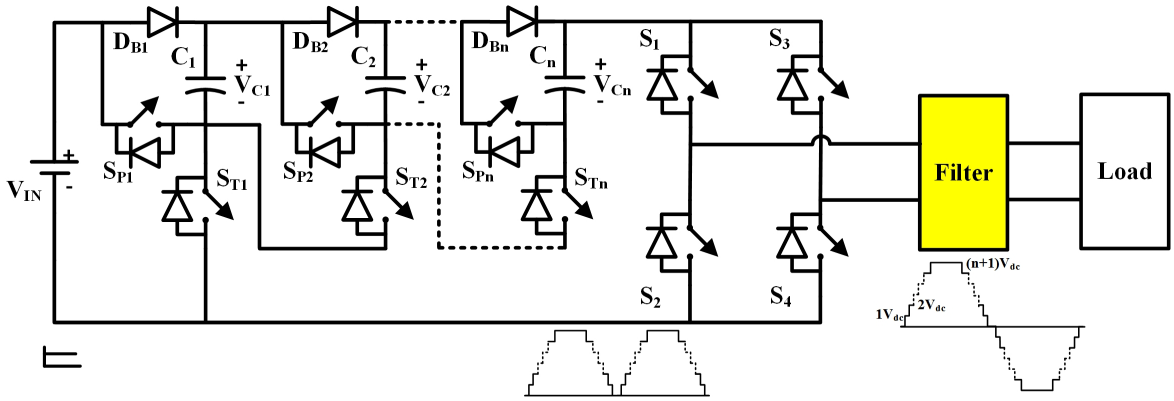


Figure 2.13: Extended high step-up switched capacitor multilevel inverter

offered by the charging path, which is expressed as follows.

$$I_{CP,SC} = \frac{V_{IN} - v_C}{R_C + R_{SP,ON}} \tag{2.2}$$

The model waveforms of the switched capacitor basic unit for different values of load resistance and duration of level-2 are depicted in Figure 2.12. The model waveforms shown in Figure 2.12a for high value of load resistance and short duration of level-2. As indicated in Figure 2.12b, the capacitor will discharge faster with lower load resistance while other parameters remains unchanged. Hence, increased capacitor ripple voltage and peak charging current. Similar phenomenon holds true for long duration of level-2 as shown in Figure 2.12c.

The switched capacitor basic unit are simple to operation and provides voltage and high efficiency at low output powers. However, the capacitor ripple voltage inversely proportional to load resistance and frequency of the output voltage, thus requires a large capacitance to limit ripple voltage. Also, it draws impulsive charging current, which needs high current rated devices.

2.7 Quasi-resonant switched capacitor multilevel inverters

Quasi-resonant switched capacitor (QRSC) based step-up inverters [69–71] are evolved to address the impulse charging current issue in the SC based step-up inverters. The basic unit of QRSC and its equivalent circuits while capacitor charging and discharging are depicted in Figure 2.14. The QRSC based inverters require a bulk inductor in charging path of the capacitor as shown in Figure 2.14b. The impedance offered by the quasi-resonant inductor reduces the

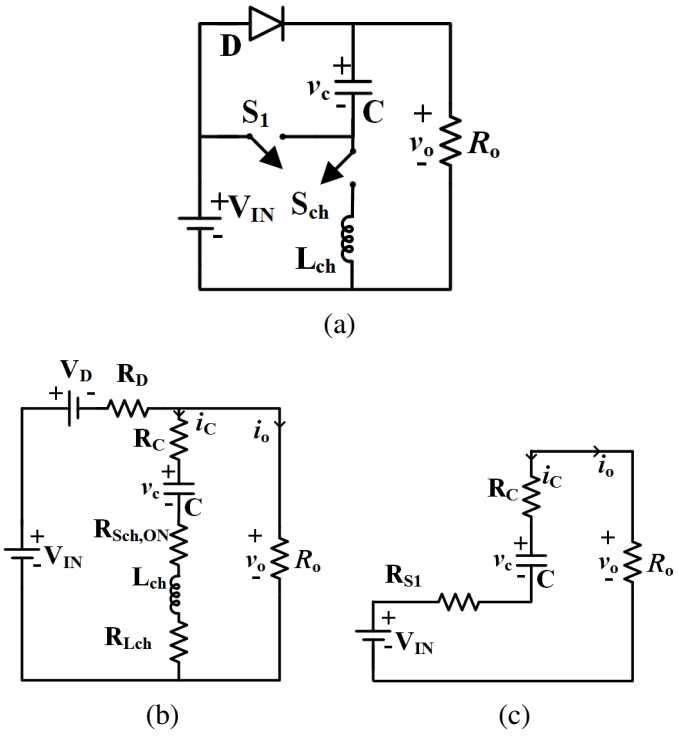


Figure 2.14: Circuit diagram of quasi resonant SC (a) basic unit (b) basic unit when capacitor is getting charged (c) basic unit when capacitor is getting discharged

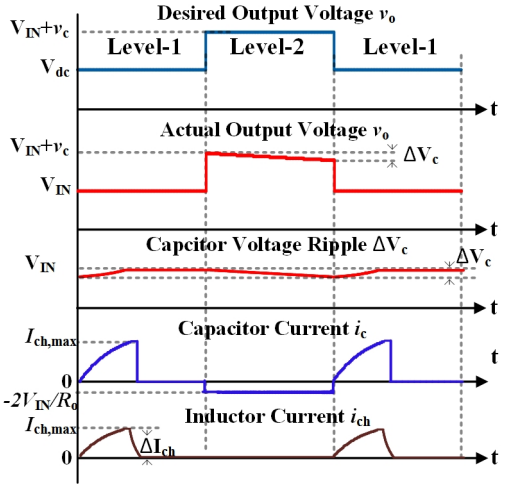


Figure 2.15: Model waveforms of basic unit of quasi resonant SC based inverters

peak charging current $I_{CP,QRSC}$, which is expressed as follows

$$I_{CP,QRSC} = \frac{V_{IN} - v_C}{\omega_{ch} L_{Ch}} \tag{2.3}$$

where ω_{ch}=$\frac{1}{\sqrt{L_{Ch}C}}$ is the natural frequency of the charging circuit.

From (2.3), it can be observed that the peak value of the capacitor charging current in QRSC based inverters can be reduced either with high value of inductor L_{Ch} or with high ω_{Ch}. The model waveforms of the QRSC based inverters are presented in Figure 2.15. Except the charging current reduction in QRSC based step-up inverters, the other merits and demerits are similar to that of SC based inverters, because both employ the parallel charge and series discharge technique for the step-up operation.

2.8 Research gaps & Motivation

The Literature review on the single-phase transformerless step-up inverters for standalone PV applications prompts the following motivations:

- Two-level step-up inverter with front-end boost converter provides improved efficiency and compactness compared to the inverters with transformer. However, the boost converter needs to process the rated output power, and also, requires bulk capacitor to maintain constant DC-link voltage.

- Improved front-end boost converter based step-up inverter with time sharing modulation technique helps to reduce the DC-link capacitor size and also, the boost converter power processing requirement.

- Both front-end and improved front-end based inverters are limited to provide voltage gain of 3. Also, these inverters provide only two-level output voltage with higher THD, which demand bulk filter.

- Cascade connection of front-end converters provides multilevel output voltage with less THD. However, this converter has similar disadvantages of front-end converter based inverters. In addition, requires high number of components and multiple isolated voltage sources.

- The differentially connected boost converters provide sinusoidal output voltage with less THD in single-stage conversion. However, the device voltage and current stresses are high at higher duty ratio operation, which affects voltage gain and efficiency.

Table 2.1: Summary of single-phase transformerless step-up inverters

Technique used for voltage step-up	Advantages	Disadvantages
Front-end boost converter	1. Simple operation Less 2. Number of components	1. Limited voltage gain (< 3) 2. Bulky DC-link capacitor 3. Higher THD 4. DC-DC converter process rated power 5. EMI Issues
Improved front-end boost converter	1. Simple operation 2. Less number of components 3. Relatively small DC-link capacitor. 4. Improved Efficiency 5. DC-DC converter process fraction of rated power	1. Limited voltage gain (< 3) 2. Higher THD 3. EMI Issues
Cascaded front-end boost converters	1. Multilevel output voltage 2. Reduced THD 3. Reduced filter or no filter 4. Fault tolerant capability	1. Increased number of components 2. Require multiple isolated voltage sources 3. Limited voltage gain 4. Bulky DC-link capacitors
Differential boost converters	1. Single stage operation 2. Sinusoidal output voltage with less THD 3. Less number of components	1. Limited voltage gain (< 3) 2. Voltage and current stresses on switches are high 3. Low efficiency
SC	1. Higher efficiency at low power applications 2. Modular operation 3. Multrilevel output with low THD 4. Self voltage balance of capacitors	1. Impulse capacitor charging current 2. Bulky capacitors 3. Capacitor voltage and overall efficiency droops with output power 4. Increased number of components to obtain more voltage levels
QRSC	1. Higher efficiency at low power applications 2. Modular operation 3. Multrilevel output with low THD 4. Self voltage balance of capacitors 5.Reduced capacitor charging current	1. Bulky capacitors 2. Capacitor voltage and overall efficiency droops with output power 3. Increased number of components to obtain more voltage levels

- SC based step-up MLIs provide modular operation, higher voltage gain with multiple SC cells and multilevel output voltage. However, the parallel charging and series discharging technique leads to the capacitor voltage drooping and efficiency drooping for high power low frequency applications. Also, require more number of components to provide improved voltage gain and higher voltage levels. In addition, these inverters draws impulse current during capacitor charging, thus require overrated components.

- To address the impulse capacitor charging current issue, QRSC based inverter with a bulk resonant inductor are presented in the literature. Apart from this, these inverters have similar advantages and disadvantages at par with the SC based inverters.

The merits and demerits of each type of step-up transformerless inverters are presented in Table 2.1.

2.9 Thesis objectives

With the above motivations, the following research objectives are formulated for the thesis work:

- To reduce impulse charging currents during capacitor charging.
- To reduce component count with increased output voltage levels.
- To eliminate capacitor voltage and inverter efficiency drooping with increase in output power.
- To reduce the number of capacitors.
- To reduce the capacitor size.
- To achieve improved voltage gain

2.10 Thesis contributions

The main aim of this thesis is to develop new step-up MLI configurations with reduced component count, capacitor size, improved voltage gain and better efficiency. The research contributions that have been made to meet the objectives are presented as follows.

I. A new boost DC-link integrated MLI is realized by the integration of two two-level boost DC-link converters with a hybrid H-bridge inverter using two symmetrical voltage sources. The proposed topology with proper selection of capacitor voltage levels can produce 9-, 11- and 13-level outputs and provides a maximum voltage gain of 3.

II. To further improve the voltage gain and number of voltage levels, a MLI with four level boost DC-link basic unit is proposed. With two basic units and two symmetrical voltage sources, it can produce 17-level output voltage and provide a voltage gain of 4. In asymmetrical mode of operation, the same configuration is able to produce 31-level output.

III. The proposed 13-level and 17-level MLIs are required to power from two sources. However, for PV AC module applications the step-up inverter configurations that utilize single source and provide higher voltage gain are essential. Hence, in contrast, an improved buck-boost integrated MLI with single-source is proposed. By choosing the appropriate voltage ratios of capacitor voltages with respect to the source voltage, on of the proposed converter can produce an 11-level output voltage with a voltage gain of 5 and another proposed converter provide a 13-level output voltage with a voltage gain of 2 respectively.

In summary, all of the proposed MLIs utilizes nearest level stair case modulation, thus produce a low frequency common mode voltage (CMV), which results in reduced leakage currents. The capacitors presented in the proposed step-up inverters are being charged from BBCs at high switching frequency to the desired voltage values. Thus, provides various benefits such as, reduced switch count, capacitor count, capacitor size and capacitor charging currents. In addition, avoids capacitor voltage drooping issues with increase in load power at low frequency operation. Further, the BBCs presented in the proposed inverters can only process fractional part of total energy.

2.11 Thesis organization

The thesis has been structured into seven chapters, which organized and described in brief as follows:

Chapter 1 briefly explains the importance of standalone PV systems. Also, it introduces the various inverter configurations that are suitable for the standalone PV operation.

Chapter 2 explores the relevant literature on single-phase transformerless step-up inverters for stand alone applications to formulate the research objectives.

Chapter 3 presents the MLI with two-level boost DC-link basic unit for 9-, 11- and 13-level operation under various loading conditions.

Chapter 4 presents the cascaded symmetrical and asymmetrical MLI with increased voltage gain and output voltage levels.

Chapter 5 presents a 13-level MLI with a single source and a voltage gain of 2.

Chapter 6 presents a 11-level MLI with a single source and high voltage gain of 5.

Finally, **Chapter 7** summarizes the main findings of the research work reported in this thesis and suggests the scope for further research in the area.

2.12 Summary

In this chapter, a comprehensive bibliographical review on single-phase transformerless step-up inverters for stand alone applications has been presented. The advantages and drawbacks of all existing topologies have been discussed. Finally, the motivation and contribution to research have been presented. The main contributions and thesis organization is presented.

Chapter 3

Boost DC-link Integrated Cascaded Multilevel Inverter

Chapter 3

Boost DC-link Integrated Cascaded Multilevel Inverter

3.1 Introduction

In recent times, switched capacitor multilevel inverter (SCMLI) topologies [63–68] are popular, which provide sufficient voltage gain, increased number of voltage levels with a simple and modular operation. However, the parallel charge and series discharge of the capacitor technique employed by the SCMLIs demands bulky capacitors for low-frequency AC applications and also, causes voltage and efficiency drooping with respect to increase in output power. Further, SCMLI capacitors are restricted to charge at a fixed voltage, thus require more components to produce higher voltage levels. In addition, the SCMLIs draw impulse current during capacitor charging, which demands high current rated components. The impulse current problem in SCMLIs is addressed with a quasi-resonant inductor [69–71], however the other issues of SCMLIs could be the scope for the further research.

This chapter presents a new boost DC-link integrated multilevel inverter (BDIMLI) topology for single-phase stand-alone PV applications. The BDIMLI is realized by the integration of 2 two-level boost DC-link converter (TBDC) units with a hybrid H-bridge inverter using symmetrical voltage sources. The proposed TBDC units charge the capacitors to the desired voltage at the high switching frequency, hence require less capacitance and component count. The proposed topology with proper selection of capacitor voltage levels can produce 9, 11, 13 - level output without altering any circuit components. Besides, the proposed topology produces low-frequency CMV.

The comprehensive analysis of BDIMLI in comparison with recent MLI topologies is presented. An experimental prototype of BDIMLI is built and its dynamic behavior with different load conditions is presented for both 9 and 13-level operations.

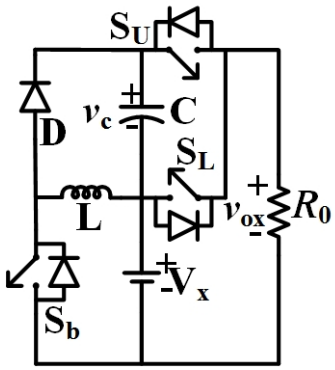


Figure 3.1: Two-level Boost DC-link Converter Unit.

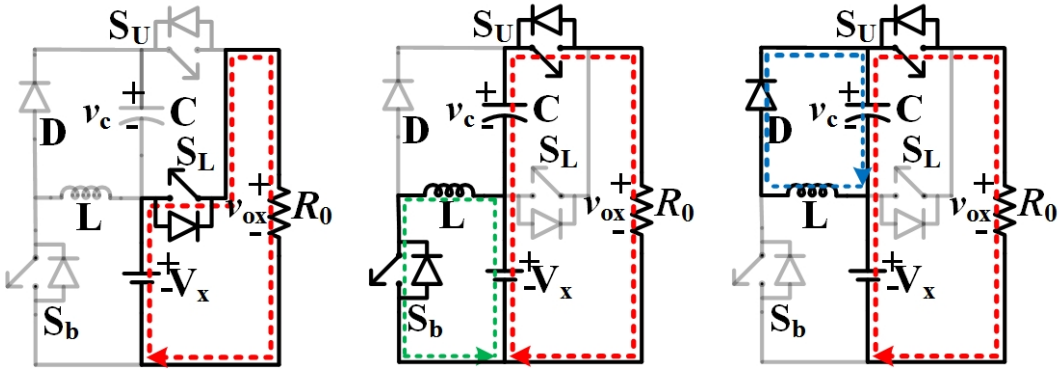


Figure 3.2: Equivalent circuit of TBDC during (a) level-1 (b) level-2 while inductor charging (c) level-2 while inductor discharging

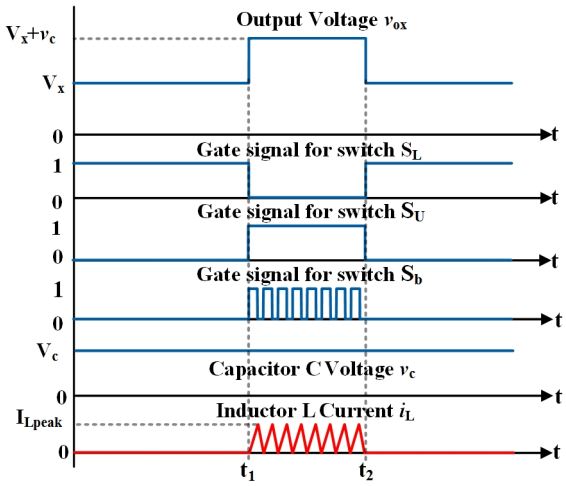
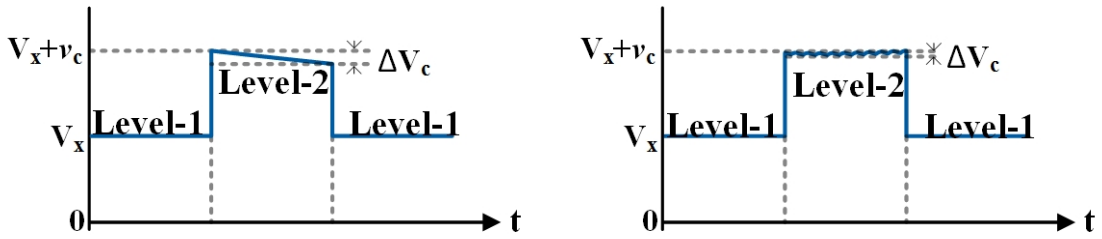


Figure 3.3: TBDC model waveforms: output voltage, switch gate pulses, capacitor voltage and inductor current during level-1 and level-2 operations.



(a) (b)

Figure 3.4: Typical output voltage waveform of (a) SCMLI basic cell (b) TBDC

3.2 Working and operating principle of the proposed BDIMLI

In this chapter, a new boost DC-link integrated cascaded MLI is proposed in which a basic block of two-level boost DC-link converter (TBDC) is utilized. Figure. 3.1 depicts the TBDC schematic, which comprises of two converters namely conv-1 and conv-2. Conv-1 is a modified BBC consisting of voltage source V_x, inductor L, boost switch S_b, diode D, capacitor C load resistance R_o. Conv-2 is a level selector circuit comprising of two switches S_L and S_U that produce an output voltage v_o equal to either V_x (Level-1) or $V_x + v_c$ (Level-2) where v_c is the voltage across the capacitor C. Corresponding equivalent circuits of TBDC for level-1 and level-2 are shown in Figure 3.2 respectively. Figure 3.3 illustrates the waveforms of TBDC explaining its operation and control. Figure 3.4 depicts the typical output voltage waveform of existing SCMLI basic cell and the TBDC respectively, which evident the voltage drooping during level-2 in the existing SCMLI basic cell. The duration of level-2 decides the capacitor ripple voltage and its capacitance. Longer the duration, the larger will be the capacitor ripple or capacitance required. Operating modes of TBDC for level-1 and level-2 are explained as follows:

Level-1 $(0 \rightarrow t_1 \,\&\, t > t_2)$**:** Figure 3.2a depicts the equivalent circuit of level-1. During this interval, switch S_L is turned ON while switches S_U & S_b are OFF. Thus, the load current conducts through the path $V_x - S_L - R_o - V_x$ and the voltage $v_{ox} = V_x$.

Level-2 $(t_1 \rightarrow t_2)$**:** During this interval, switch S_U is ON and S_L is OFF continuously, while switch S_b operates with switching frequency f_s and duty cycle δ to maintain desired capacitor voltage v_c. As shown in Figures 3.2b and 3.2c, S_U is continuously ON and the load

current conducts through the path $V_x - v_c - S_U - R_o - V_x$. Hence, the input source and capacitor voltages are in series additive resulting in an output voltage $v_{ox} = V_x + v_c$.

When S_b is ON: The equivalent circuit is shown in Figure 3.2b, where the inductor gets magnetized and the diode D is reverse biased. The inductor current increases linearly from 0 to its peak value I_{Lpeak} and conducts through the path $V_x - L - S_b - V_x$, which is indicated by green line. The currents $i_{Sb} = i_L$, $i_D = 0$ $i_c = -i_o$, and inductor peak current I_{Lpeak} is expressed as

$$v_L = L\frac{di_L}{dt} = V_x \tag{3.1}$$

$$I_{Lpeak} = \frac{V_x \delta}{L f_s} \tag{3.2}$$

where i_L, i_C, i_D, i_{Sb} & i_o are instantaneous currents through L, C, D, S_b & R_o respectively and v_L is voltage across the inductor L.

When S_b is OFF: The equivalent circuit is shown in Figure 3.2c, where Diode D conducts and the stored inductor energy will charge the capacitor as well as supply the load. Assume the capacitor voltage is constant (i.e, $v_c = V_c$). Here, the current $i_o = i_L - i_c$, $i_L = i_D$ and I_{Lpeak} is obtained as follows:

$$v_L = L\frac{di_L}{dt} = -V_c \tag{3.3}$$

$$I_{L,peak} = \frac{V_c(1-\delta)}{L f_s} \tag{3.4}$$

From (3.2) & (3.4)

$$V_c = \frac{\delta}{(1-\delta)} V_x = n V_x \tag{3.5}$$

where step-up ratio n of the BBC of TBDC is expressed as

$$n = \frac{v_o}{V_x} = \frac{\delta}{(1-\delta)} \tag{3.6}$$

At boundary conduction mode (BCM), the stored inductor energy completely transferred

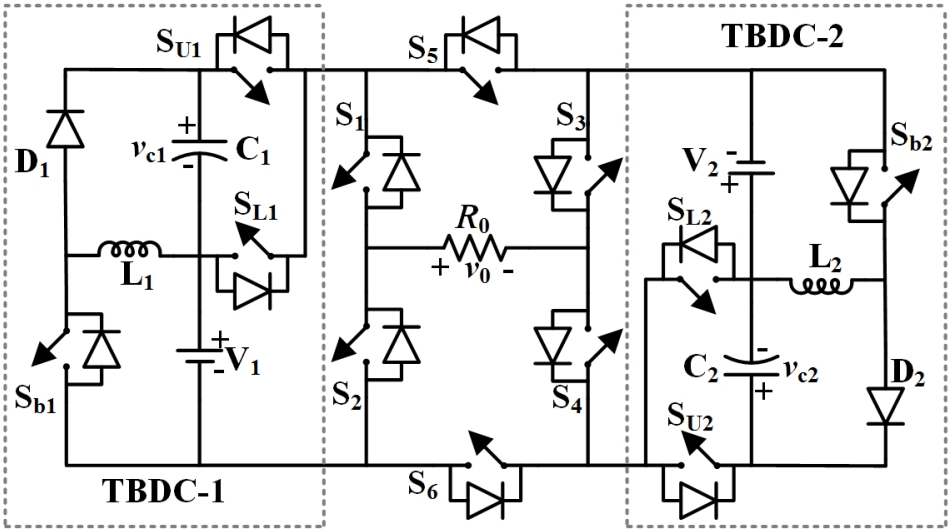


Figure 3.5: Schematic diagram of the proposed Boost DC-link Integrated Cascaded MLI.

to the capacitor. The stored inductor energy in BCM is

$$E_L = \frac{1}{2} L_B I_{LBpeak}^2 \tag{3.7}$$

where L_B is critical inductance value and I_{LBpeak} is respective inductor peak current. The energy transferred to the capacitor is

$$E_C = V_c I_0 T_s \tag{3.8}$$

From (3.2), (3.7) & (3.8)

$$\frac{1}{2} L_B I_{Lpeak}^2 = V_c I_0 T_s \tag{3.9}$$

$$L_B = \frac{R_0 \delta^2}{2n(1+n) f_s} \tag{3.10}$$

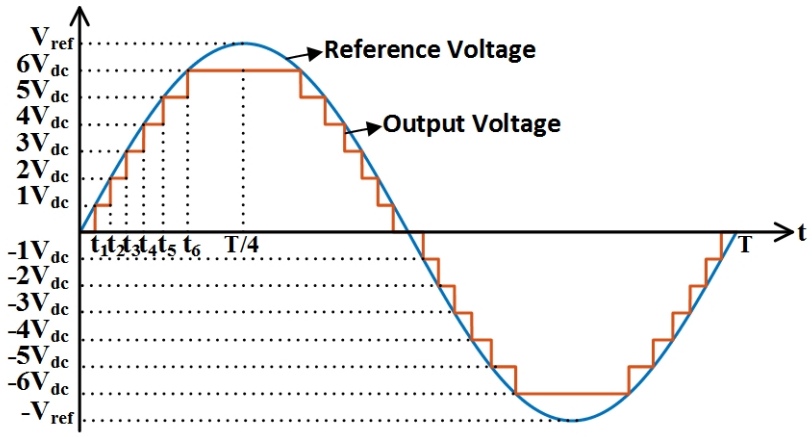


Figure 3.6: Model waveform of the 13-level output voltage.

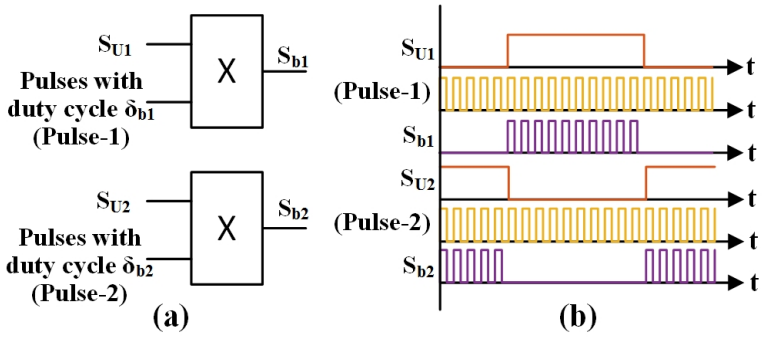


Figure 3.7: S_{b1} & S_{b2} gate pulses:(a) logic diagram, (b) model waveforms.

The critical value of the capacitor can be determined as follows:

$$C_{min} = \frac{(V_x + V_c)\delta}{R_0 \Delta V_c f_s} = \frac{V_c}{\Delta V_c} \frac{(1+n)}{n} \frac{\delta}{R_0 f_s} \tag{3.11}$$

where ΔV_c is the capacitor voltage ripple and usually the capacitor value $C \geq C_{min}$.

The schematic diagram of the proposed BDIMLI is depicted in Figure 3.5. It consists of two TBDC units and one hybrid H-bridge formed by six switches $(S_1 - S_6)$. The capacitors

Table 3.1: Capacitor voltages, and step-up ratios for 9, 11 & 13-level operation of BDIMLI with $V_1 = V_2 = V_{dc}$

Level of Operation	**Voltage** V_{c1}	**Voltage** V_{c2}	**Step-up Ratio** n_1	**Step-up Ratio** n_2
9-levels	$1V_{dc}$	$1V_{dc}$	1	1
11-levels	$1V_{dc}$	$2V_{dc}$	1	2
	$2V_{dc}$	$1V_{dc}$	2	1
13-levels	$1V_{dc}$	$3V_{dc}$	1	3
	$3V_{dc}$	$1V_{dc}$	3	1

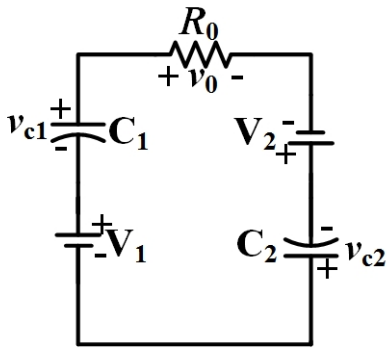


Figure 3.8: Equivalent circuit of BDIMLI for peak output voltage.

C_1 and C_2 are charged to the voltages V_{c1} and V_{c2} respectively, where V_{c1} is n_1 times of V_1 and V_{c2} is n_2 times of V_2. The TBDC-1 output voltages are V_1 and $V_1 + V_{c1}$ for the respective conduction of S_{L1} and S_{U1}. Similarly, TBDC-2 output voltages are V_2 and $V_2 + V_{c2}$ for the respective conduction of S_{L2} and S_{U2}. Figure 3.7 depicts the logical realization of gate pulses for switches S_{b1} and S_{b2}, which are synchronized with gate pulses of S_{U1} and S_{U2} respectively. δ_1 and δ_2 are the duty cycles of BBC-1 and BBC-2 respectively. The BDIMLI achieves 9 or 11 or 13-level output voltage waveform by proper selection of V_{c1} and V_{c2}. Table 3.1 provides respective capacitor voltages and step-up ratios (n_1 & n_2) for 9, 11 & 13-level operation of BDIMLI. The switching states for 9, 11 and 13-level operations are furnished in Tables 3.2, 3.3 and 3.4 respectively. The timing sequence and corresponding switching states for each level of the 13-level output voltage are realized from Figure 3.6 and Table 3.4. Similarly, the timing sequence of 9 and 11-level output voltages can be realized.

The equivalent circuit of BDIMLI depicted in Figure 3.8 represents for peak voltage level. Figure. 3.9 and 3.10 illustrate the equivalent circuits for each level of 13-level BDIMLI operation. The generalized output voltage of BDIMLI is expressed as

$$v_o = v_{o1}[(S_3 + S_4)(S_1S_6 - S_2S_5)] + v_{o2}[(S_1 + S_2)(S_3S_6 - S_4S_5)] \tag{3.12}$$

where,

$$v_{o1} = [S_{L1} + (1 + n_1)S_{U1}]V_1$$

$$v_{o2} = [S_{L2} + (1 + n_2)S_{U2}]V_2$$

The TBDC-1 and TBDC-2 topologies are designed to operate in BCM mode. The re-

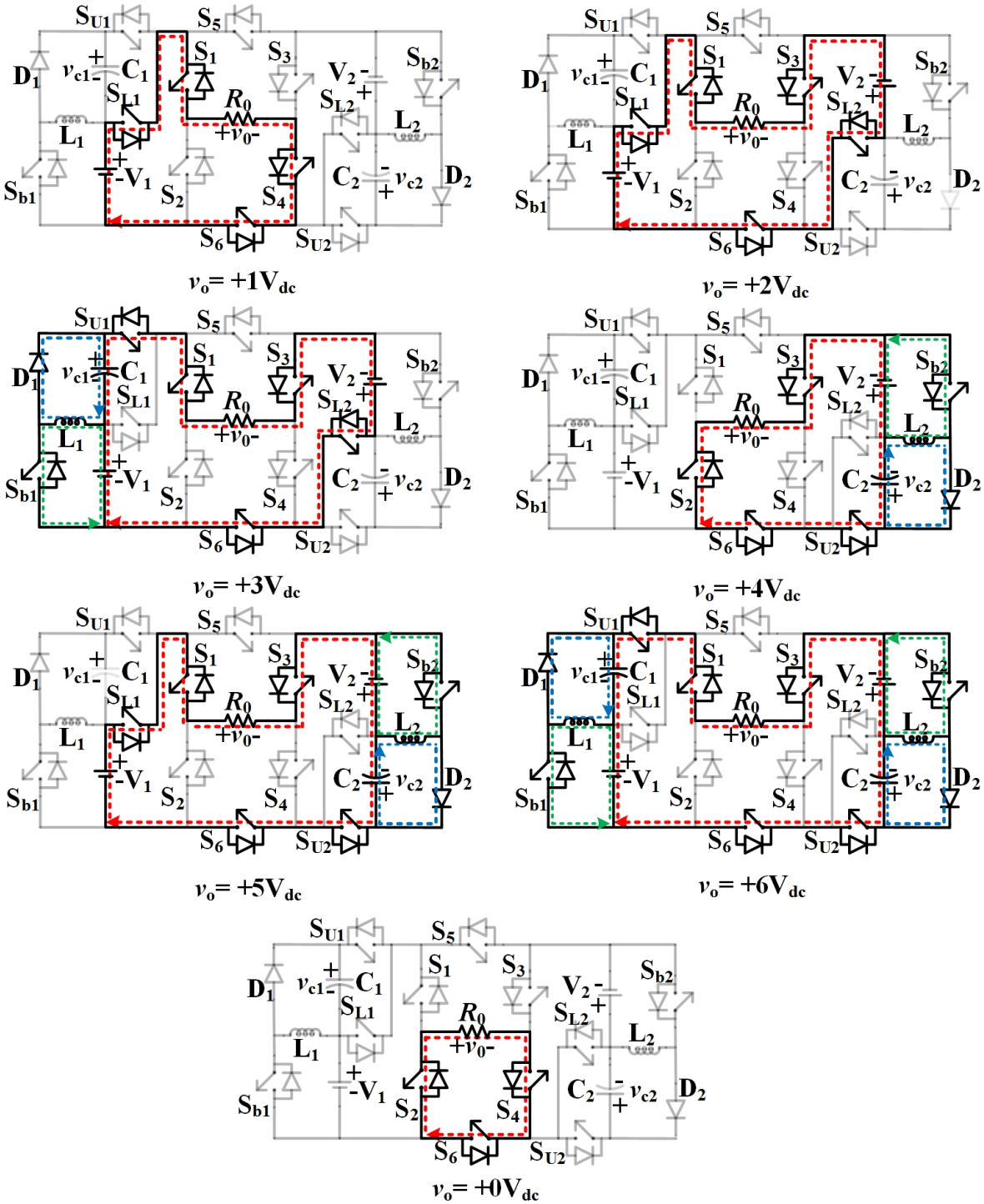


Figure 3.9: Different modes of operation of the proposed BDIMLI for 13-level operation from $+0V_{dc}$ to $+6V_{dc}$.

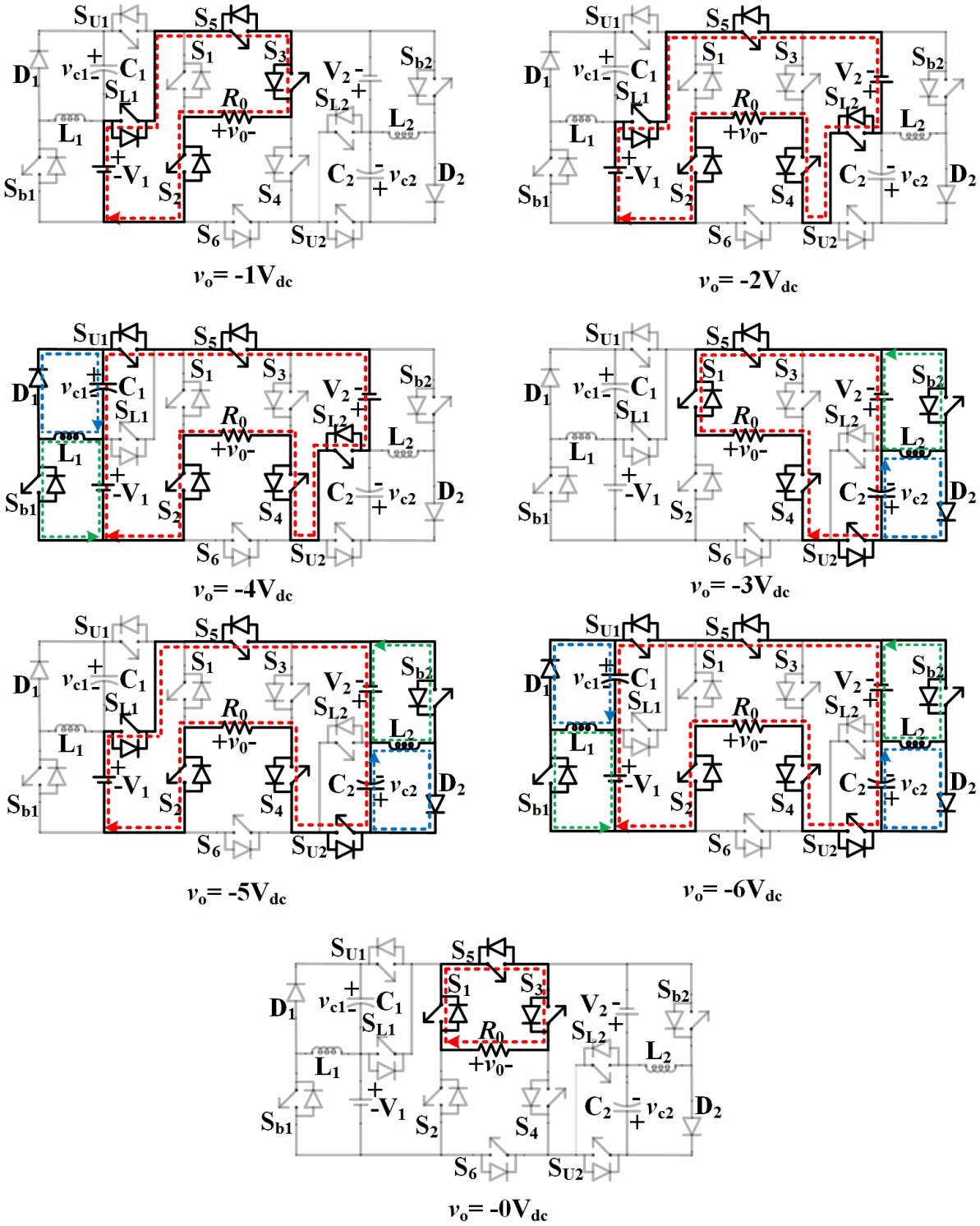


Figure 3.10: Different modes of operation of the proposed BDIMLI for 13-level operation from -0V_{dc} to -6V_{dc}.

Table 3.2: Switching States of the proposed BDIMLI for 9-evel operation

On State Switches	**Buck-boost Converter**		V_o	
	BBC-1	**BBC-2**		
S_2, S_4, S_6	OFF	OFF	**0**	
S_1, S_3, S_5				
S_{L1}, S_1, S_4, S_6	OFF	OFF	V_1	$\mathbf{1}V_{dc}$
S_{L2}, S_2, S_3, S_6			V_2	
S_{U1}, S_1, S_4, S_6	ON	OFF	$V_1 + V_{c1}$	$\mathbf{2}V_{dc}$
$S_{L1}, S_{L2}, S_1, S_3, S_6$	OFF	OFF	$V_1 + V_2$	
S_{U2}, S_2, S_3, S_6	OFF	ON	$V_2 + V_{c2}$	
$S_{U1}, S_{L2}, S_1, S_3, S_6$	ON	OFF	$V_1 + V_2 + V_{c1}$	$\mathbf{3}V_{dc}$
$S_{L1}, S_{U2}, S_1, S_3, S_6$	OFF	ON	$V_1 + V_2 + V_{c2}$	
$S_{U1}, S_{U2}, S_1, S_3, S_6$	ON	ON	$V_1 + V_2 + V_{c1} + V_{c2}$	$\mathbf{4}V_{dc}$
$S_{U1}, S_{U2}, S_2, S_4, S_5$	ON	ON	$-(V_1 + V_2 + V_{c1} + V_{c2})$	$\mathbf{-4}V_{dc}$
$S_{L1}, S_{U2}, S_2, S_4, S_5$	OFF	ON	$-(V_1 + V_2 + +V_{c2})$	$\mathbf{-3}V_{dc}$
$S_{U1}, S_{L2}, S_2, S_4, S_5$	ON	OFF	$-(V_1 + V_2 + V_{c1})$	
S_{U1}, S_2, S_3, S_5	ON	OFF	$-(V_1 + V_{c1})$	$\mathbf{-2}V_{dc}$
S_{U2}, S_1, S_4, S_5	OFF	ON	$-(V_2 + V_{c2})$	
$S_{L1}, S_{L2}, S_2, S_4, S_5$	OFF	OFF	$-(V_1 + V_2)$	
S_{L1}, S_2, S_3, S_5	OFF	OFF	$-(V_1)$	$\mathbf{-1}V_{dc}$
S_{L2}, S_1, S_4, S_5			$-(V_2)$	

spective critical inductance values L_{B1} and L_{B2} of inductors L_1 and L_2 are obtained by considering the highest output voltage level. From Figure 3.8, the peak value of output current is given by

$$I_{o,max} = \frac{V_1 + V_2 + V_{c1} + V_{c2}}{R_o} = \frac{(2 + n_1 + n_2)V_{dc}}{R_o} \tag{3.13}$$

Maximum powers P_{c1} and P_{c2} delivered by capacitors C_1 and C_2 are given by

$$P_{c1} = V_{c1}\, i_{o,max} = \frac{n_1(2 + n_1 + n_2)V_{dc}^2}{R_0} \tag{3.14}$$

$$P_{c2} = V_{c2}\, i_{o,max} = \frac{n_2(2 + n_1 + n_2)V_{dc}^2}{R_0} \tag{3.15}$$

Table 3.3: Switching States of the proposed BDIMLI for 11-level Output

On State Switches	**Buck-boost Converter**		V_o	
	BBC-1	**BBC-2**		
S_2,S_4,S_6	OFF	OFF	**0**	
S_1,S_3,S_5				
S_{L1},S_1,S_4,S_6	OFF	OFF	V_1	**1**V_{dc}
S_{L2},S_2,S_3,S_6			V_2	
S_{U1},S_1,S_4,S_6	ON	OFF	V_1+V_{c1}	**2**V_{dc}
S_{L1},S_{L2},S_1,S_3,S_6	OFF	OFF	V_1+V_2	
S_{U1},S_{L2},S_1,S_3,S_6	ON	OFF	V_1+V_2+V_{c1}	**3**V_{dc}
S_{U2},S_2,S_3,S_6	OFF	ON	V_2+V_{c2}	
S_{L1},S_{U2},S_1,S_3,S_6	OFF	ON	V_1+V_2+V_{c2}	**4**V_{dc}
S_{U1},S_{U2},S_1,S_3,S_6	ON	ON	V_1+V_2+V_{c1}+V_{c2}	**5**V_{dc}
S_{U1},S_{U2},S_2,S_4,S_5	ON	ON	$-(V_1$+V_2+V_{c1}+$V_{c2})$	**-5**V_{dc}
S_{L1},S_{U2},S_2,S_4,S_5	OFF	ON	$-(V_1$+V_2+$V_{c2})$	**-4**V_{dc}
S_{U2},S_1,S_4,S_5	OFF	ON	$-(V_2$+$V_{c2})$	**-3**V_{dc}
S_{U1},S_{L2},S_2,S_4,S_5	ON	OFF	$-(V_2$+$V_{c2})$	
S_{U1},S_2,S_3,S_5	ON	OFF	$-(V_1$+$V_{c1})$	**-2**V_{dc}
S_{L1},S_{L2},S_2,S_4,S_5	OFF	OFF	$-(V_1$+$V_2)$	
S_{L1},S_2,S_3,S_5	OFF	OFF	$-(V_1)$	**-1**V_{dc}
S_{L2},S_1,S_4,S_5			$-(V_2)$	

From (3.9), (3.10), (3.14) & (3.15) the critical values of L_{B1} and L_{B2} are expressed as follows:

$$L_{B1} = \frac{R_o \delta_1^2}{2n_1(2+n_1+n_2)f_s} \tag{3.16}$$

$$L_{B2} = \frac{R_o \delta_2^2}{2n_2(2+n_1+n_2)f_s} \tag{3.17}$$

From (3.16) & (3.17) , the characteristics of L_{B1} & L_{B2} as a function of load for 9-level and 13-level operations with f_s of 10kHz, 30kHz and 50kHz are illustrated in Figures 3.11a & 3.12a respectively. For DCM operation, inductors L_1 & L_2 are less than the L_{B1} & L_{B2} respectively and higher for CCM operation. It can be noticed from the Figures 3.11a & 3.12a that for a particular power rating, the inductor size decreases with an increase in switching frequency. From (3.11), (3.16) & (3.17), the minimum capacitances $C_{1,min}$ & $C_{2,min}$ of C_1 & C_2 required to

Table 3.4: Switching States of the proposed BDIMLI for 13-level operation

On State Switches	**Buck-boost Converter**		V_o	
	BBC-1	**BBC-2**		
S_2,S_4,S_6	OFF	OFF	**0**	
S_1,S_3,S_5				
S_{L1},S_1,S_4,S_6	OFF	OFF	V_1	V_{dc}
S_{L2},S_2,S_3,S_6			V_2	
S_{U1},S_1,S_4,S_6	ON	OFF	V_1+V_{c1}	**2**V_{dc}
S_{L1},S_{L2},S_1,S_3,S_6	OFF	OFF	V_1+V_2	
S_{U1},S_{L2},S_1,S_3,S_6	ON	OFF	V_1+V_2+V_{c1}	**3**V_{dc}
S_{U2},S_2,S_3,S_6	OFF	ON	V_2+V_{c2}	**4**V_{dc}
S_{L1},S_{U2},S_1,S_3,S_6	OFF	ON	V_1+V_2+V_{c2}	**5**V_{dc}
S_{U1},S_{U2},S_1,S_3,S_6	ON	ON	V_1+V_2+V_{c1}+V_{c2}	**6**V_{dc}
S_{U1},S_{U2},S_2,S_4,S_5	ON	ON	$-(V_1$+V_2+V_{c1}+$V_{c2})$	**-6**V_{dc}
S_{L1},S_{U2},S_2,S_4,S_5	OFF	ON	$-(V_1$+V_2+$V_{c2})$	**-5**V_{dc}
S_{U2},S_1,S_4,S_5	OFF	ON	$-(V_2$+$V_{c2})$	**-4**V_{dc}
S_{U1},S_{L2},S_2,S_4,S_5	ON	OFF	$-(V_1$+V_2+$V_{c1})$	**-3**V_{dc}
S_{U1},S_2,S_3,S_5	ON	OFF	$-(V_1$+$V_{c1})$	**-2**V_{dc}
S_{L1},S_{L2},S_2,S_4,S_5	OFF	OFF	$-(V_1$+$V_2)$	
S_{L1},S_2,S_3,S_5	OFF	OFF	$-(V_1)$	**-1**V_{dc}
S_{L2},S_1,S_4,S_5			$-(V_2)$	

limit ripple voltage to ΔV_{c1} & ΔV_{c2} respectively are given as follows:

$$C_{1,min} = \frac{V_{c1}(2+n_1+n_2)\delta_1}{\Delta V_{c1} n_1 R_0 f_s} = \frac{(2+n_1+n_2)\delta_1}{x_1 n_1 R_0 f_s} \tag{3.18}$$

$$C_{2,min} = \frac{V_{c2}(2+n_1+n_2)\delta_2}{\Delta V_{c2} n_2 R_0 f_s} = \frac{(2+n_1+n_2)\delta_2}{x_2 n_2 R_0 f_s} \tag{3.19}$$

where x_1 & x_2 are the ratios of corresponding capacitor ripple voltage to average capacitor voltage of C_1 & C_2 respectively. The $C_{1,min}$ and $C_{2,min}$ interms of maximum output power P_{max} are expressed as follows

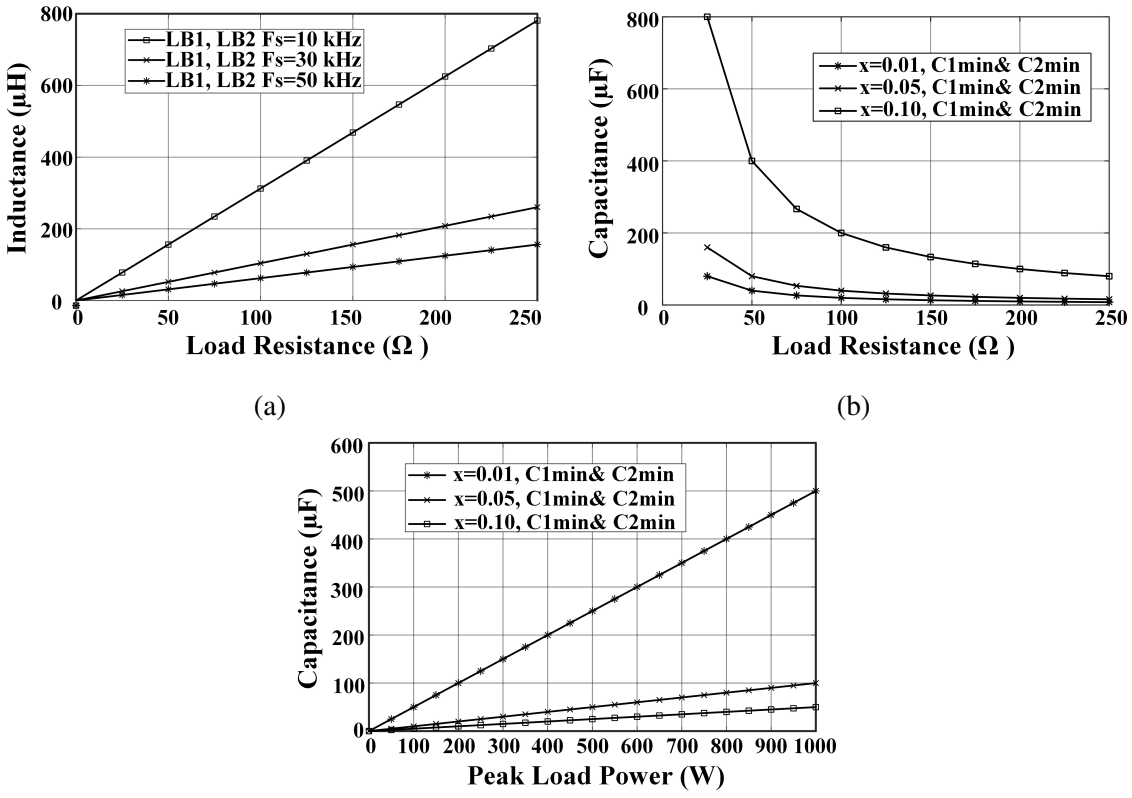


Figure 3.11: Design characteristics for 9-level operation: (a) L_{B1} & L_{B2} versus R_o at f_s = 10kHz, 30kHz & 50kHz (b) $C_{1,min}$ & $C_{2,min}$ versus R_o at f_s = 10kHz for different ripple voltages and (c) $C_{1,min}$ & $C_{2,min}$ versus P_{max} with f_s = 10kHz and V_1=50V.

$$C_{1,min} = \frac{P_{max}\delta_1}{x_1 n_1 (2+n_1+n_2) f_s {V_1}^2} \tag{3.20}$$

$$C_{2,min} = \frac{P_{max}\delta_2}{x_2 n_2 (2+n_1+n_2) f_s {V_1}^2} \tag{3.21}$$

where

$$P_{o,max} = \frac{(2+n_1+n_2){V_1}^2}{R_o}$$

Both capacitors C_1 & C_2 are charged at a high switching frequency while feeding the load. Hence, small size capacitors are adequate even at high power ratings. From (3.18), (3.19), (3.20) & (3.21) the characteristics of $C_{1,min}$ & $C_{2,min}$ as a function of R_o and P_o with f_s=10

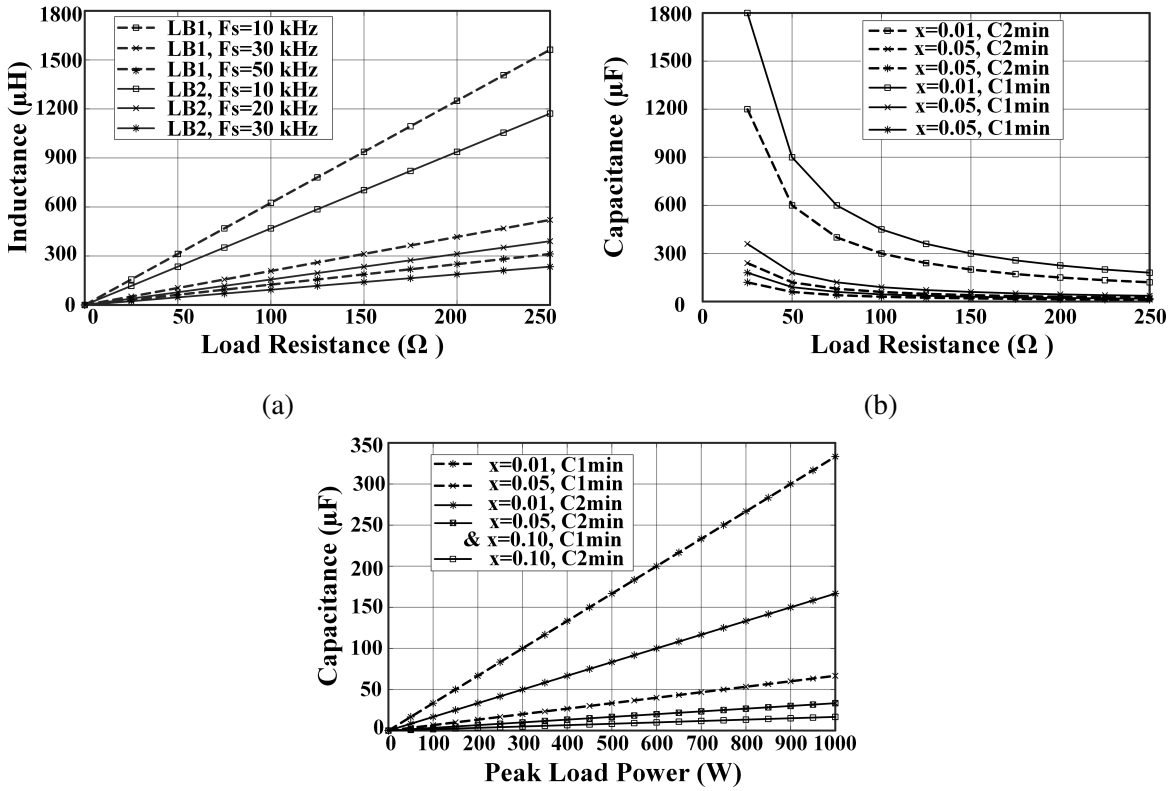


Figure 3.12: Design characteristics for 13-level operation: (a) L_{B1} & L_{B2} versus R_o at f_s = 10kHz, 30kHz & 50kHz (b) $C_{1,min}$ & $C_{2,min}$ versus R_o at f_s = 10kHz for different ripple voltages and (c) $C_{1,min}$ & $C_{2,min}$ versus P_{max} with f_s = 10kHz and V_1=50V.

kHz for 9-level and l3-level operations are illustrated in Figures 3.11b, 3.11c, 3.12b & 3.12c, respectively. From the characteristics of $C_{1,min}$ & $C_{2,min}$, the minimum capacitor value for a specific power rating can be identified.

3.3 Comparative analysis

The comparative analysis of proposed BDIMLI with existing MLI topologies utilize symmetrical voltage sources in terms of component count, capacitor size, total switch voltage (TSV), cost and boost factor is presented as follows:

Proposed BDIMLI and MLIs [1] & [65] are analyzed for an output power (P_o) of 1000W at $f_o = 50$Hz. The switching frequency of boost converters used in the proposed BDIMLI is 10kHz. The capacitor values in each topology are calculated by assuming 5% capacitor voltage ripple and are presented in Tables 3.5 and 3.6 for 9 and 13-level outputs respectively. The boost

Table 3.5: Comparison of Proposed BDIMLI with Existing MLI Topologies with symmetrical DC sources for 9-level output ($P_o = 1000$W, $V_{o,max} = 200$V and $f_o = 50$Hz)

Topology	N_{dc}	N_{swi}	N_{dio}	N_{cap}	Capacitors Values	N_{ind}	TSV	$\frac{TSV}{V_{o,max}}$	Boost Factor
[72]	4	10	—	—		—	1000	5	1
[1]-(1)	2	12	2	2	C1=21.5mF C2=21.5mF	—	1000	5	2
[65]-(1)	2	12	0	1	C1=13.6mF	—	1100	5.5	2
Proposed	2	12	2	2	C1=0.2mF C2=0.2mF	2	1400	7	2

For the proposed BDIMLI f_s =10kHz, L_1 =L_2 =62.5μH

Note: N_{dc} = No. of DC sources, N_{swi} = No. of switches, N_{dio} = No. of diodes,

N_{cap} = No. of capacitors, N_{ind} = No. of inductors, N_{dri} = No. of drivers and N_{lev} = No. of levels

Table 3.6: Comparison of Proposed BDIMLI with Existing MLI Topologies with symmetrical DC sources for 13-level output ($P_o = 1000$W, $V_{o,max} = 300$V and $f_o = 50$Hz)

Topology	N_{dc}	N_{swi}	N_{dio}	N_{cap}	Capacitors Values	N_{ind}	TSV	$\frac{TSV}{V_{o,max}}$	Boost Factor
[1]-(1)	3	18	3	3	C1=C3=15mF C2=13mF	—	1500	5	2
[1]-(2)	2	14	4	4	C1=C2=17.5mF C1P=C2P=13.5mF	—	1600	5.33	3
[65]-(2)	2	18	—	2	C1=C2=15mF	—	1650	5.5	3
Proposed	2	12	2	2	C1=0.12mF C2=0.06mF	2	1900	6.33	3

For the proposed BDIMLI f_s =10kHz L_1 =104μH, L_2 =78μH

factor used for the comparison is expressed as

$$Boost\ Factor = \frac{Peak\ Output\ Voltage(V_{o,max})}{Sum\ of\ Source\ Voltages(V_1 + V_2 ... + V_n)} \tag{3.22}$$

For 9-Level: From Table 3.5, it can be observed that the boost factor of BDIMLI is same as existing 9-level SCMLI topologies [1] & [65]. However, the capacitor size of the proposed BDIMLI is reduced approximately 60-100 times compared with the SCMLIs [1] & [65]. Also, MLI reported [72] requires less number of switches, but requires more number of sources and provides no voltage gain.

For 13-Level: From Table 3.6, it can be noticed that the proposed BDIMLI with high boost factor provides reduced component count and capacitors size compared to the MLIs [1] & [65]. Moreover, the capacitor size is reduced by nearly 100 times in contrast to the other MLIs.

Further, the voltage and current stresses of the various switches presented in the BDIMLI

Table 3.7: Cost comparison of the proposed BDIMLI with other step-up MLI topologies for 13-level operation at P_o = 1000W

Topology	Component	Required Rating	Component No	Quantity	Unit Price ($)	Amount ($)
[1]-(1)	S1a-S1d, S2a-S2d	150V/7A	IRLS640A	8	1.49	11.92
	S1,S2	100V/35A	IRFB41N15DPBF	2	2.21	4.42
	S11,S111,S22,S222	50V/17A	FDPF3860T	4	1.07	4.28
	D1,D2	100V/35A	VF40150C-M3/4W	2	1.64	3.28
	D11,D111,D22,D222	50V/7A	RB088T100HZC9	4	0.84	3.36
	C11,C22	17.5mF/50V	36DY183F075BC2A	2	59.71	119.42
	C1,C2	13.5mF/50V	DCM143U075BE2B	2	35.34	70.68
	Drivers		A3120 with aux	14	10	140
					Total cost	**357.36**
[1]-(2)	S1a-S1d,S2a-S2d,S3a-S3d	100V/7A	FDPF770N15A	12	1.37	16.44
	S1,S2,S3	50V/27A	STF45N10F7	3	2.16	6.48
	S11,S22,S33	50V/7A	FQU13N10LTU	3	0.75	2.25
	D1,D2,D3	50V/27A	DST30100C	3	1.41	4.23
	C1,C2,C3	15mF,50V	CGS153U075V5L	3	41.77	125.31
	Drivers		A3120 with aux	18	10	180
					Total cost	334.71
[65]	S1, S3a, S3b, S5, S7, S8a, S8b	100V,/26A	FDP2572	7	1.82	12.74
	S2, S4, S6, S9-14	100V/7A	FDPF770N15A	9	1.37	12.33
	ST1a, ST1b	50V/7A	FQU13N10LTU	2	0.75	1.5
	C1,C2	11mF/100V	DCMX113U150CC2B	2	61.82	123.64
	Drivers		A3120 with aux	18	10	180
					Total cost	**330.21**
Proposed	S1,S2	100V/7A	FDPF770N15A	2	1.37	2.74
	S3,S4	200V/7A	RCX100N25	2	1.86	3.72
	S5,S6	300V/7A	IRF740PBF	2	1.53	3.06
	SL1,SU1	50V/6A	FQU13N10LTU	2	0.75	1.5
	SL2,SU2	150V/6A	IRLS640A	2	1.49	2.98
	SB1	100V/22A	SQP25N15-52GE3	1	1.95	1.95
	SB2	200V/44A	IRF300P227	1	5.94	5.94
	DB1	100V/22A	TST30H150CW C0G	1	1.58	1.58
	DB2	200V/44A	SBR60A300CT	1	3.92	3.92
	C1	120uF/50V	672D127H075ET5C	1	5.06	5.06
	C2	60uF/150V	WBR60-250A	1	10.73	10.73
	L1	104uH/38A	B66387G1000X187	1	10	10
	L2	78uH/38A	B66387G1000X188	1	10	10
	Drivers		A3120 with aux	12	10	120
	Voltage Sensors		LEMLV25P	2	65	130
					Total cost	**313.18**

Table 3.8: Loss analysis of the Proposed BDIMLI for 9 and 13-level operation using PSIM

Power (W)	Level of operation					
	9-level			11-level		
	$P_{swi}(W)$	$P_{cond}(W)$	P_{lc}^{*} (W)	P_{swi} (W)	P_{cond} (W)	P_{lc}^{*} (W)
200	0.3006	20.4	2.0908	0.5206	14.71	2.6012
400	0.548	30.35	4.0914	1.02	24.21	5.194
600	0.7801	38.98	6.2149	1.527	32.7	9.282
800	1.037	46.67	8.2922	1.937	39.16	10.237
1000	1.317	53.85	10.6323	2.478	46.87	12.851

Where P_{swi}=Total switching Losses, P_{cond}=Total conduction losses and P_{lc}^{*}=Total passive component power losses

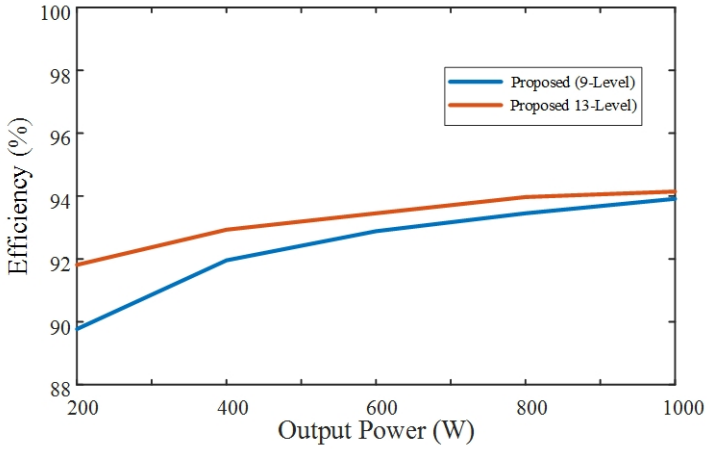


Figure 3.13: Efficiency curves of proposed BDIMLI.

and the other step-up MLIs are provided in Table 3.7. The nearest rated components are considered for the cost comparison, which are also presented in Table 3.7. From this table, it can be observed that the cost of the capacitors used in the proposed topology is very less. Even though the BDIMLI utilizes additional components such as, voltage sensors and inductors, the overall cost is relatively lesser than the other step-up MLIs presented in Table 3.7. To examine the efficient operation of BDIMLI, various power losses and overall efficiency for different output power ratings are evaluated. The thermal model of the BDIMLI is simulated for 9- and 13-level operations using PSIM [73] to evaluate various power losses and the results are presented in Table 3.8 and the corresponding efficiency curves are shown in Figure 3.13. From the Figure 3.13, it can be noticed that the efficiency curves of the proposed BDIMLI are unchanged with change in output power. Whereas the existing MLI [1] topologies provide peak efficiency at

Table 3.9: Specification & Design Parameters of BDIMLI

Parameter	**Value / Part Number**
$V_1 = V_2$	50V
f_o	50Hz
f_s	10kHz
V_o(RMS)	220V (13-Level), 150V (9-Level)
P_o	580W (13-Level), 540W (9-Level)
R_o	80Ω (13-Level), 40Ω (9-Level)
L_1, L_2	500μH, 500μH
C_1, C_2	200μF/400V, 200μF/400V
Switches	IKW40T120
Diodes	STPSC2006CW

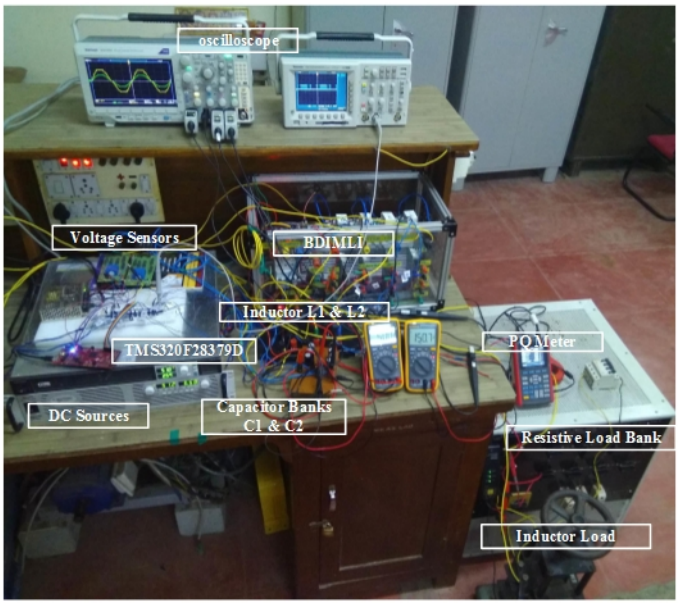
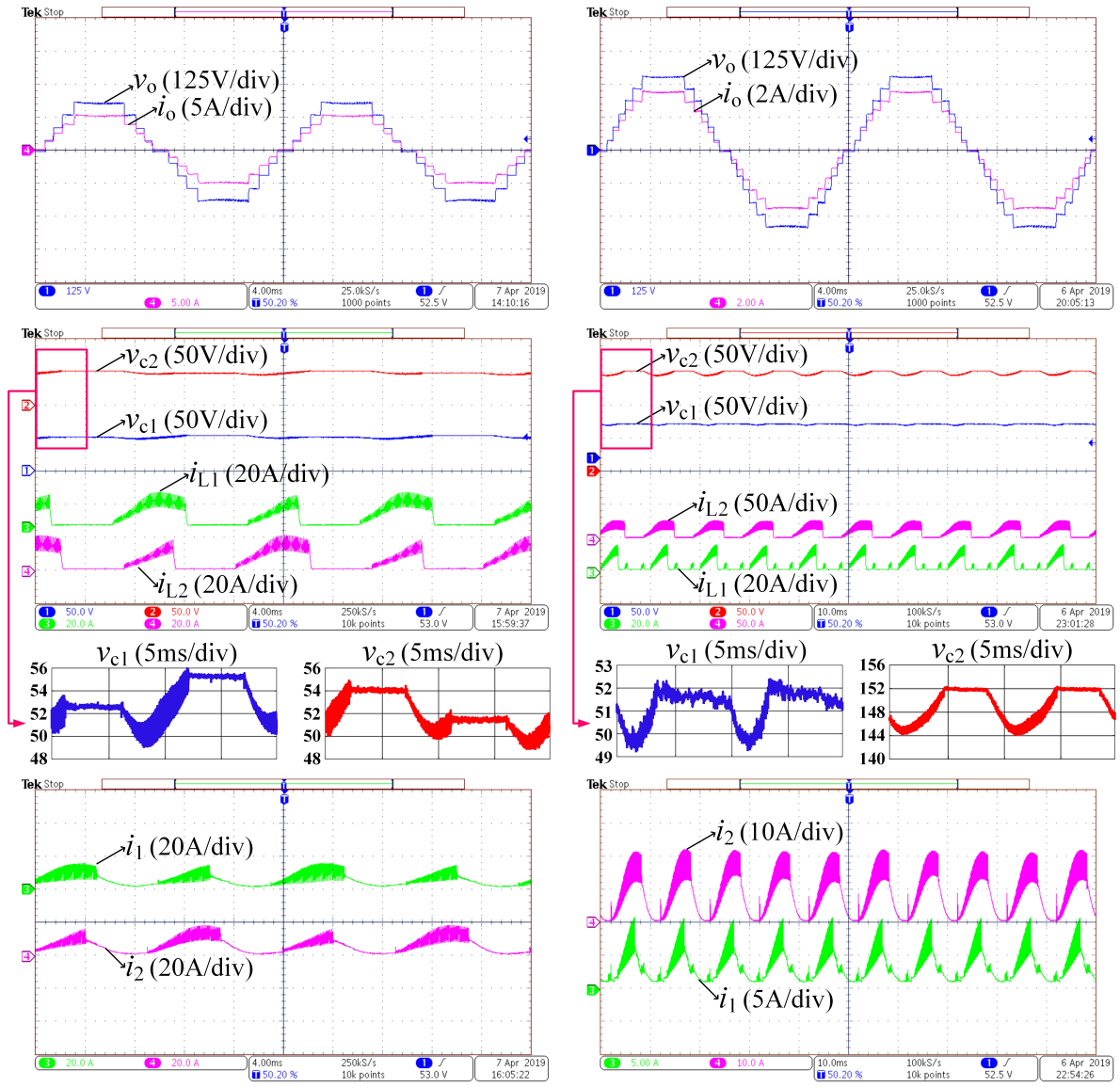


Figure 3.14: Experimental prototype of proposed BDIMLI.

low power, but droops with the increase in power rating.

3.4 Experimental Results

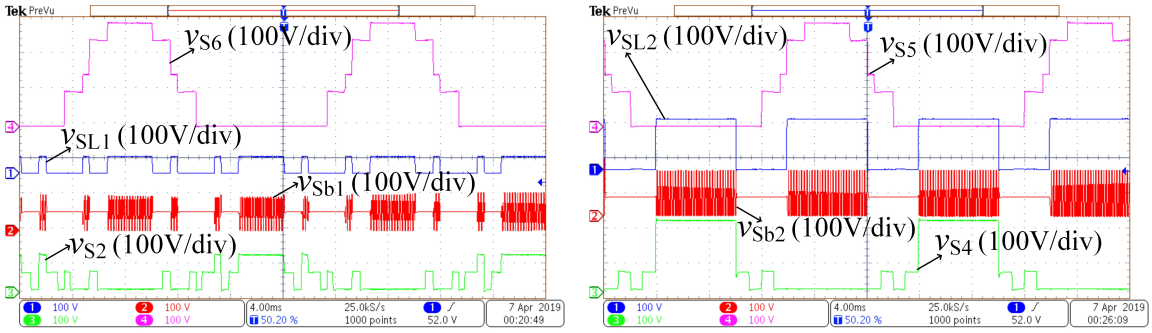
An experimental prototype of the proposed BDIMLI is developed as illustrated in Figure 3.14. Gating pulses for all the switching devices of BDIMLI are realized with the TMS320F28379d processor. S_{b1} & S_{b2} are operated with 10kHz switching frequency and S_5 & S_6 are operated with the fundamental frequency of 50Hz. While the rest of the switches are operated with



(a) (b)

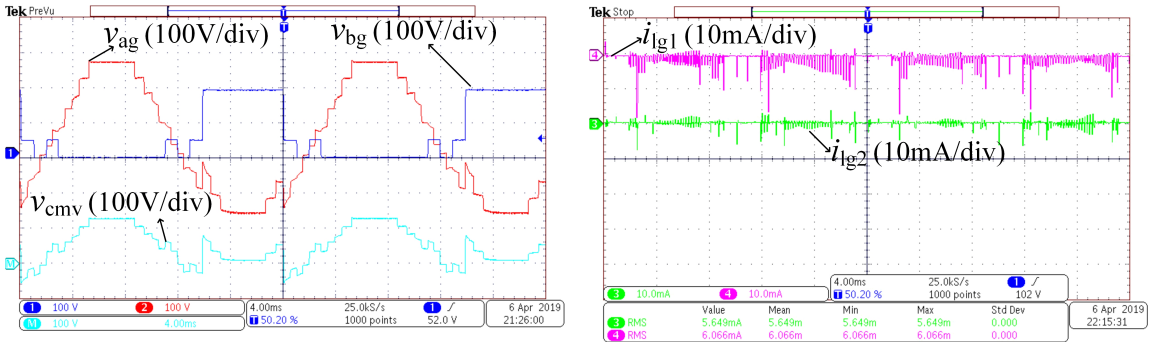
Figure 3.15: Experimental waveforms of load voltage v_o, load current i_o, inductors L_1, L_2 currents (i_{L1}, i_{L2}), capacitors C_1, C_2 voltages (v_{c1} and v_{c2}) and dc voltage source currents (i_1 and i_2) for (a) 9-level operation and (b) 13-level operation.

low frequencies (i.e approximately 5 to 6 times of fundamental frequency) depend upon the switching states of the BDIMLI. In order to achieve desired voltage V_{c1} and V_{c2} across the capacitors, PI controllers are realized through the TMS320F28379d. Figures 3.15a & 3.15b illustrate the experimental waveforms of load, inductors, capacitors and input voltage sources for 9-level (540W) and 13-level (580W) operations respectively. The tested experimental prototype provides 85.7% and 83.2% for 13- and 9-level operations at 580W and 540W output



(a) (b)

Figure 3.16: Experimental waveforms of 13-level operation: (a) PIV of S_2, S_6, S_{L1}, S_{b1} (b) PIV of S_4, S_5, S_{L2}, S_{b2}

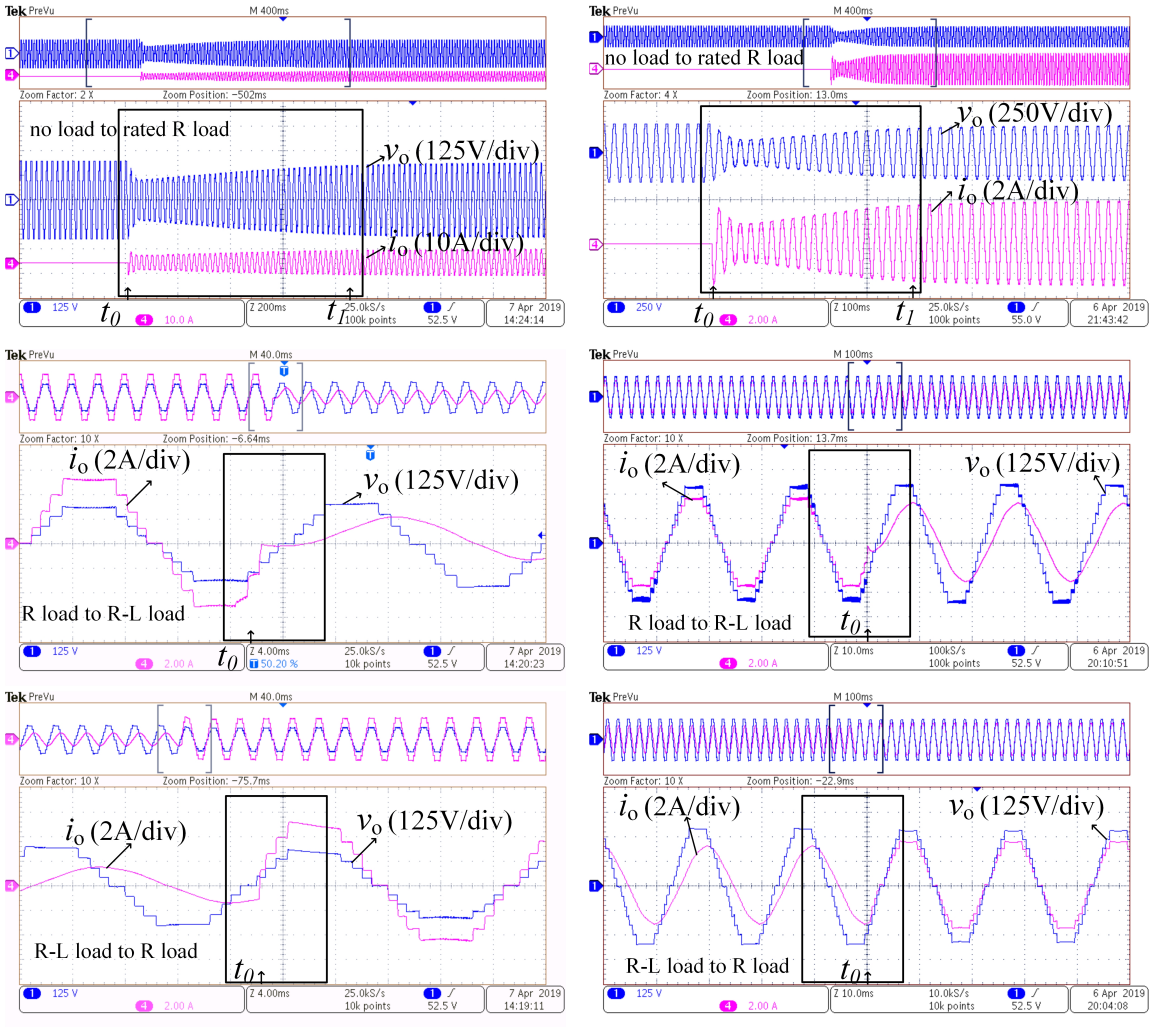


(a) (b)

Figure 3.17: Experimental waveforms of 13-level operation: (a) CMV (b) DC source leakage currents i_{lg1} and i_{lg2}.

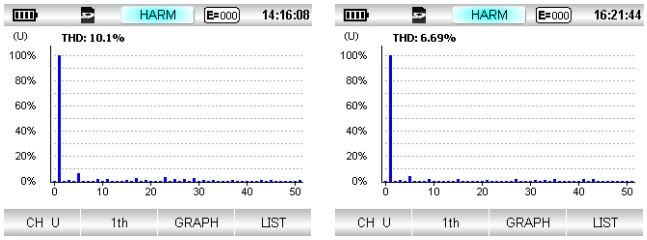
power respectively. Figures 3.16a & 3.16b present the blocking voltage of switches (S_2, S_4, S_5, S_6, S_{L1}, S_{L2}, S_{b1} and S_{b2}) for 13-level operation.

The negative terminal of voltage source V_2 is taken as a reference to measure the CMV of BDIMLI and the experimental CMV waveform is shown in Figure 3.17a. To measure the source leakage currents (i_{lg1} & i_{lg2}), a series combination of parasitic capacitance (C_p =100nF) and parasitic resistance (R_p=10Ω) is connected from each source positive terminal to load negative terminal. From Figure 3.17b, it can be observed that the measured i_{lg1} & i_{lg2} RMS values are 5.649mA & 6.066mA, which are complied with the VDE0126-1-1 standard. The dynamic behavior of the proposed BDIMLI is depicted in Figures 3.18a and 3.18b for different load changing conditions, which confirm the smooth and stable operation of the controller. During the transition from no-load to full-load, it can be observed that there is a dip in load voltage. However, the PI controllers set back the load voltage to its nominal value, which confirms the



(a) (b)

Figure 3.18: Dynamic behavior of the proposed BDIMLI with step change in load conditions: no-load to rated R load, R load to R-L load, and R-L load to R load for (a) 9-level operation and (b) 13-level operation.



(a) (b)

Figure 3.19: Harmonic spectrum of load voltage v_o for (a) 9-level operation and (b) 13-level operation.

Table 3.10: Comparison of experimental THD of the proposed BDIMLI with the MLI presented in [1]

Parameter	**Proposed BDIMLI**	**Cascaded MLI [1]**
Modulation	Nearest Level Control	Phase Shift Modulation
THD (9-level)	10.1%	19.1%
THD (13-level)	6.69%	14.1%

effective closed loop operation. From this figure, it is also evident that there is no deviation in load voltage during the step change in load i.e., resistive to inductive load and vice-versa. Single-phase power quality analyzer (PQA) UT-283A is used to measure the THD. Figures 3.19a & 3.19b presents the harmonic spectrum of load voltage for 9- and 13-level operations. The measured THD of the load voltage without any filter is obtained as 10.1% and 6.69% for 9-level and 13-level operations respectively. From the THD results, it can be noticed that the 5^{th} order harmonic is dominant in the output voltage than the 3^{rd} order, thus requires a small filter. Table 3.10 demonstrates the experimental % THD comparison of the BDIMLI and the MLI [1], which shows the significant reduction in %THD of the proposed BDIMLI.

3.5 Summary

In this chapter, a novel boost DC-link integrated MLI is proposed. The proposed BDIMLI provides various advantages such as, high boost-factor, reduced component count, capacitor size, relatively low cost and less THD. The design characteristics of inductors and capacitors are analyzed, which shows the significant reduction in capacitor size. In addition, the capacitor voltages are unchanged irrespective of load changing conditions for 9-level and 13-level operation. The benefits of proposed BDIMLI are evident with the comparative study in contrast to recent MLI topologies. Moreover, the dynamic behavior of BDIMLI under various load conditions is tested with no-load, resistive and inductive loads providing a smooth and stable operation.

Chapter 4

Improved Boost DC-link Integrated Cascaded Multilevel Inverter

Chapter 4

Improved Boost DC-link Integrated Cascaded Multilevel Inverter

4.1 Introduction

The basic unit of proposed BDIMLI presented in Chapter 3 provides only two-level output i.e., either input voltage or the sum of input and capacitor voltage, but unable to provide the capacitor voltage alone. This limitation adversely impacts the total number of switches, capacitors and levels in cascaded SCMLI operation. Thus, this chapter proposes an improved boost DC-link integrated cascaded MLI by using a four-level basic unit, which helps in generation of more levels with an improved voltage gain, reduced switch as well as capacitor count and capacitor size.

This chapter proposes an improved boost DC-link integrated cascaded multilevel inverter (IBDIMLI) with symmetrical and asymmetrical operation. The operation of the proposed MLI for symmetrical 17-level operation with sinusoidal pulse width modulation (SPWM) & nearest level control (NLC) and asymmetrical 31-level operation with NLC is explained and validated experimentally. The experimental results of static and dynamic load conditions are analyzed and discussed in detail. In addition, the proposed topology is compared with recent boost MLI topologies in terms of component count, device stress, efficiency, capacitor size and cost. From the comparative study, it is evident that the IBDIMLI provides features such as, reduced component count, capacitors size, overall cost and improved voltage gain.

4.2 Working and operating principle of the proposed IBDIMLI

Figure 4.1a shows the basic four-level unit (FLU) of the proposed MLI, which comprises of DC source, BBC and level generation circuit (LGC). BBC consists of boost switch S_{Bx}, diode D_{Bx}, inductor L_x and capacitor C_x. BBC charges the capacitor to a desired voltage v_{cx}, which equals to step-up ratio (n_x) times of the source voltage V_x, where $n_x \geq 2$.The LGC

constructed by complementary conducting switch pairs (S_{Vx}, S_{VxP}) and (S_{Cx}, S_{CxP}), which helps to generate different output voltage levels. The voltage source V_x contributes to output voltage level when switch S_{Vx} is ON and will be bypassed when S_{VXP} ON. Similarly, capacitor voltage v_{cx} will be switched by S_{Cx} and S_{CxP}. Equivalent circuits of FLU for different voltage levels of operation are presented in Figure 4.2 and the respective switching states are provided in Table 4.1. BBC operates with duty cycle δ_x and switching frequency f_s to charge the capacitor to the desired value whenever v_{cx} is required for output voltage, otherwise the BBC remains idle. The charging and discharging current paths of boost inductor L_x is illustrated in Figures 4.2c & 4.2d respectively. The output voltage v_{oX} and capacitor voltage v_{cx} of the FLU are expressed as

$$v_{ox} = (V_x)(S_{Vx}) + (v_{cx})(S_{Cx}) \tag{4.1}$$

$$v_{cx} = \frac{\delta_x}{1-\delta_x} V_x = n_x V_x \tag{4.2}$$

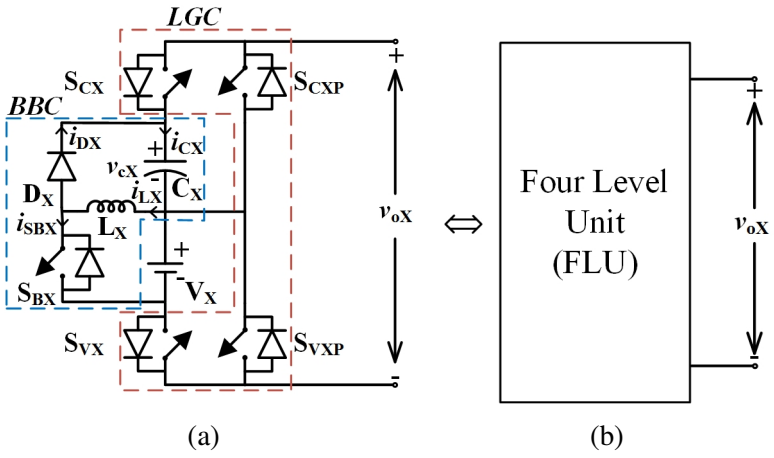


Figure 4.1: Proposed basic four-level unit: (a) circuit diagram (b) equivalent block diagram

The generalized circuit of the proposed MLI is depicted in Figure 4.3a, which is constructed by the cascade connection of x number of basic FLUs and H-bridge inverter. At any instant, the DC-link voltage v_d is the sum of all FLUs output (i.e., $v_{o1} + v_{o2} + ... + v_{oX}$), which is converted to AC output voltage v_o using H bridge inverter. The required number of switches (N_{swi}), diodes (N_{dio}), capacitors (N_{cap}), sources (N_{dc}) and inductors (N_{ind}) of the generalized

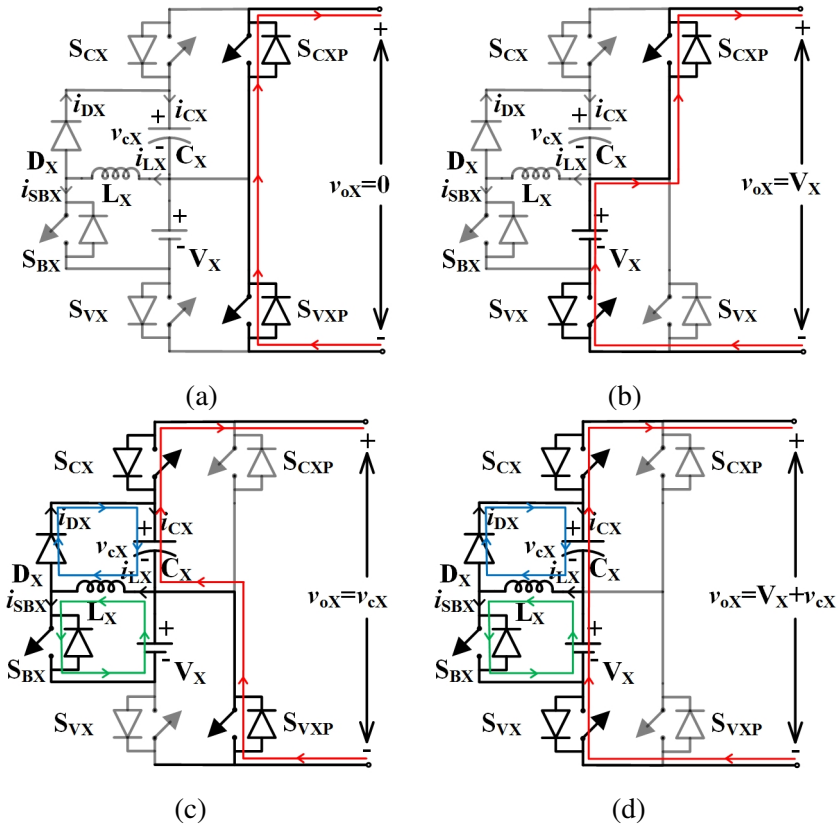


Figure 4.2: Equivalent circuit of FLU: (a) 0 level (b) V_x (c) v_{cx} (d) $V_x + v_{cx}$. (Blue and green lines represents the inductor charging and discharging paths)

Table 4.1: Switching States of Basic FLU

Voltage Level (v_{ox})	S_{Vx}	S_{VxP}	S_{Cx}	S_{CxP}	S_{Bx}
0	OFF	ON	OFF	ON	OFF
V_x	ON	OFF	OFF	ON	
v_{cx}	OFF	ON	ON	OFF	with duty cycle δ_x
$V_x + v_{cx}$	ON	OFF	ON	OFF	

Note: OFF-state represents '0' & ON-state represents '1'

MLI are given by (4.3) & (4.4).

$$N_{swi} = 5x + 4 \tag{4.3}$$

$$N_{dc} = N_{cap} = N_{ind} = N_{dio} = x \tag{4.4}$$

The MLI operates either in a symmetric or asymmetric mode based on the source voltage magnitudes. The detailed analysis and the maximum number of output levels are explained as

follows.

Symmetric Operation

In this operation, the magnitude of all DC sources remains same. i.e,

$$V_1 = V_2 = ... = V_x = V_{dc} \tag{4.5}$$

In this mode, the step-up ratio n_x of each FLU and maximum output levels ($N_{max,sym}$) of MLI are expressed as

$$n_x = x + 1 \tag{4.6}$$

$$N_{max,sym} = 2x^2 + 4x + 1 \tag{4.7}$$

Asymmetric Operation

In this operation, the magnitude of each source voltage and the capacitor voltage is given by

$$V_x = 2^{(2x-2)} V_{dc} \tag{4.8}$$

$$v_{cx} = 2^{(2x-1)} V_{dc} \tag{4.9}$$

In this mode, the $n_x = 2$ for each FLU and the maximum output levels ($N_{max,asym}$) of MLI are expressed as

$$N_{max,asym} = 2^{(2x+1)} - 1 \tag{4.10}$$

The proposed MLI with two FLUs (x=2) is shown in Figure 4.4. In the symmetric mode of operation, the source voltages $V_1 = V_2 = V_{dc}$. From (4.6) & (4.7), the n_x & $N_{max,asym}$ are calculated as 3 and 17 respectively. During asymmetric mode of operation, the source and capacitor voltages are calculated from (4.8) & (4.9) i.e., $V_1 = V_{dc}$, $V_2 = 4V_{dc}$, $V_{c1} = 2V_{dc}$ and $V_{c2} = 8V_{dc}$ respectively. In this case, the maximum levels $N_{max,asym}$ can be generated are 31, which is calculated by using (4.10). The dc-link voltage for different switching states with x=2 in symmetric mode of operation are given in Table 4.2.

The critical inductance and capacitance values are calculated for the peak load conditions with load resistance R_o. Hence, the peak load current is expressed as

Table 4.2: Switching States of proposed IBDIMLI for 17 Level operation

ON State Devices	Boost Converter		V0	
	BBC-1	BBC-2		
$S_1, S_3, S_{V1P}, S_{V2P}, S_{C1P}, S_{C2P}$ $S_2, S_4, S_{V1P}, S_{V2P}, S_{C1P}, S_{C2P}$	OFF	OFF		0
$S_1, S_4, S_{V1}, S_{V2P}, S_{C1P}, S_{C2P}$ $S_1, S_4, S_{V1P}, S_{V2}, S_{C1P}, S_{C2P}$	OFF OFF	OFF OFF	V_1 V_2	V_{dc}
$S_1, S_4, S_{V1}, S_{V2}, S_{C1P}, S_{C2P}$	OFF	OFF	$V_1 + V_2$	$2V_{dc}$
$S_1, S_4, S_{V1P}, S_{V2P}, S_{C1}, S_{C2P}$ $S_1, S_4, S_{V1P}, S_{V2P}, S_{C1P}, S_{C2A}$	ON OFF	OFF ON	v_{c1} v_{c2}	$3V_{dc}$
$S_1, S_4, S_{V1}, S_{V2P}, S_{C1}, S_{C2P}$ $S_1, S_4, S_{V1P}, S_{V2}, S_{C1}, S_{C2P}$ $S_1, S_4, S_{V1}, S_{V2P}, S_{C1P}, S_{C2A}$ $S_1, S_4, S_{V1P}, S_{V2}, S_{C1P}, S_{C2A}$	ON OFF 	OFF ON 	$V_1 + v_{c1}$ $V_2 + v_{c1}$ $V_1 + v_{c2}$ $V_2 + v_{c2}$	$4V_{dc}$
$S_1, S_4, S_{V1}, S_{V2}, S_{C1}, S_{C2P}$ $S_1, S_4, S_{V1}, S_{V2}, S_{C1P}, S_{C2A}$	ON OFF	OFF ON	$V_1 + V_2 + v_{c1}$ $V_1 + V_2 + v_{c2}$	$5V_{dc}$
$S_1, S_4, S_{V1P}, S_{V2P}, S_{C1}, S_{C2A}$	ON	ON	$v_{c1} + v_{c2}$	$6V_{dc}$
$S_1, S_4, S_{V1}, S_{V2P}, S_{C1}, S_{C2A}$ $S_1, S_4, S_{V1P}, S_{V2}, S_{C1}, S_{C2A}$	ON ON	ON ON	$V_1 + v_{c1} + v_{c2}$ $V_2 + v_{c1} + v_{c2}$	$7V_{dc}$
$S_1, S_4, S_{V1}, S_{V2}, S_{C1}, S_{C2A}$	ON	ON	$V_1 + V_2 + v_{c1} + v_{c2}$	$8V_{dc}$
$S_2, S_3, S_{V1}, S_{V2P}, S_{C1P}, S_{C2P}$ $S_2, S_3, S_{V1P}, S_{V2}, S_{C1P}, S_{C2P}$	OFF OFF	OFF OFF	$-(V_1)$ $-(V_2)$	-V_{dc}
$S_2, S_3, S_{V1}, S_{V2}, S_{C1P}, S_{C2P}$	OFF	OFF	$-(V_1 + V_2)$	-$2V_{dc}$
$S_2, S_3, S_{V1P}, S_{V2P}, S_{C1}, S_{C2P}$ $S_2, S_3, S_{V1P}, S_{V2P}, S_{C1P}, S_{C2A}$	ON OFF	OFF ON	$-(v_{c1})$ $-(v_{c2})$	-$3V_{dc}$
$S_2, S_3, S_{V1}, S_{V2P}, S_{C1}, S_{C2P}$ $S_2, S_3, S_{V1P}, S_{V2}, S_{C1}, S_{C2P}$ $S_2, S_3, S_{V1}, S_{V2P}, S_{C1P}, S_{C2A}$ $S_2, S_3, S_{V1P}, S_{V2}, S_{C1P}, S_{C2A}$	ON OFF 	OFF ON 	$-(V_1 + v_{c1})$ $-(V_2 + v_{c1})$ $-(V_1 + v_{c2})$ $-(V_2 + v_{c2})$	-$4V_{dc}$
$S_2, S_3, S_{V1}, S_{V2}, S_{C1}, S_{C2P}$ $S_2, S_3, S_{V1}, S_{V2}, S_{C1P}, S_{C2A}$	ON OFF	OFF ON	$-(V_1 + V_2 + v_{c1})$ $-(V_1 + V_2 + v_{c2})$	-$5V_{dc}$
$S_2, S_3, S_{V1P}, S_{V2P}, S_{C1}, S_{C2A}$	ON	ON	$-(v_{c1} + v_{c2})$	-$6V_{dc}$
$S_2, S_3, S_{V1}, S_{V2P}, S_{C1}, S_{C2A}$ $S_2, S_3, S_{V1P}, S_{V2}, S_{C1}, S_{C2A}$	ON ON	ON ON	$-(V_1 + v_{c1} + v_{c2})$ $-(V_2 + v_{c1} + v_{c2})$	-$7V_{dc}$
$S_2, S_3, S_{V1}, S_{V2}, S_{C1}, S_{C2A}$	ON	ON	$-(V_1 + V_2 + v_{c1} + v_{c2})$	-$8V_{dc}$

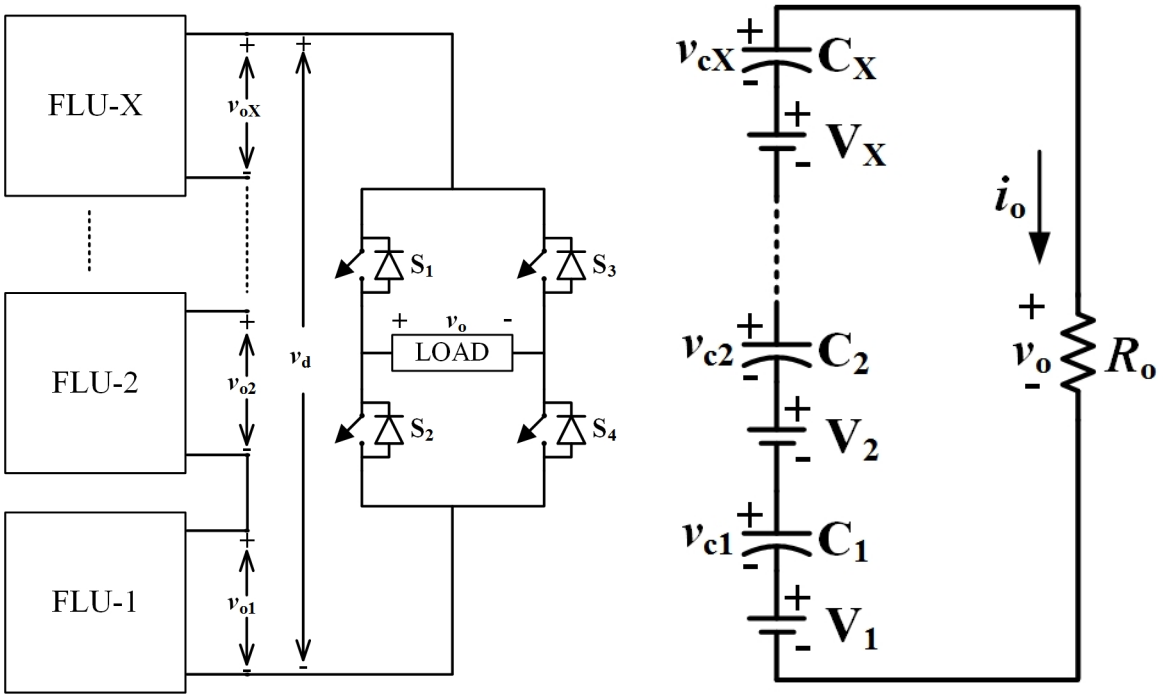


Figure 4.3: Generalized structure of the IBDIMLI: (a) block diagram (b) equivalent circuit for peak voltage level

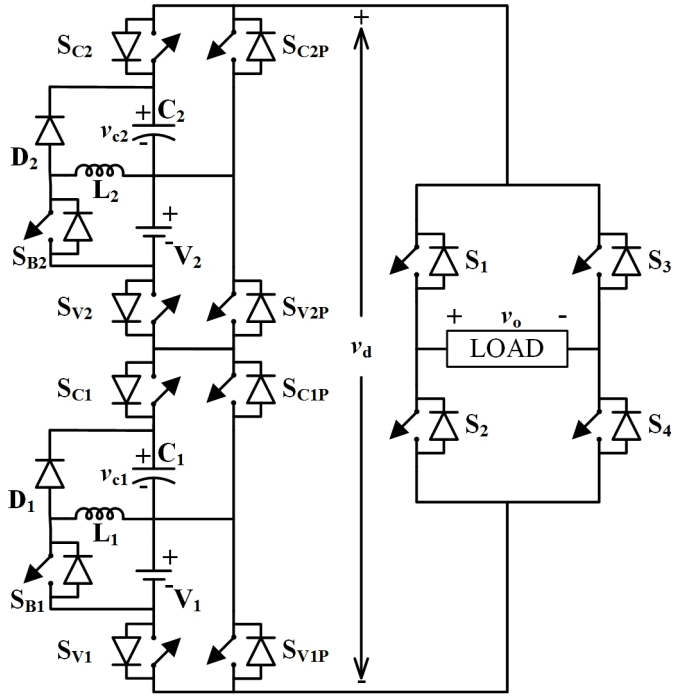
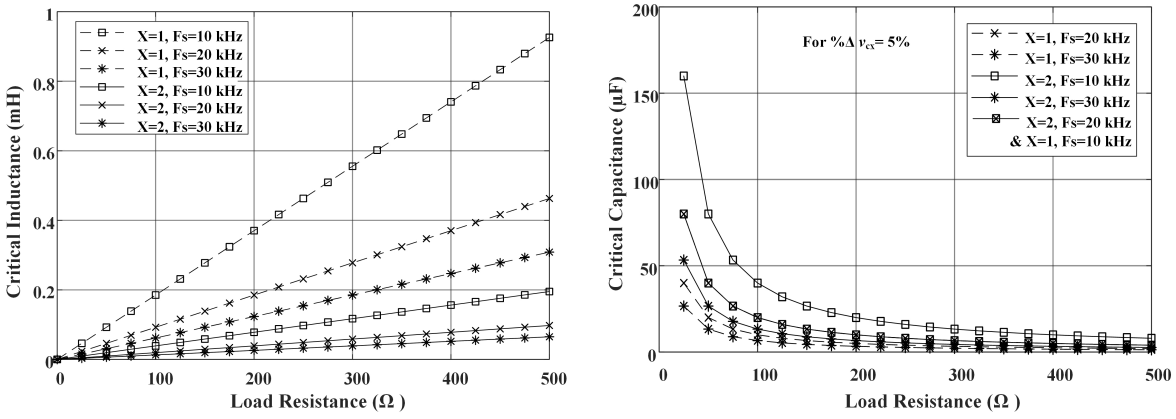


Figure 4.4: Proposed IBDIMLI circuit for x=2



(a) (b)

Figure 4.5: Variation of critical inductance and capacitance with respect to load resistance for symmetrical operation of the IBDIMLI at different switching frequencies

$$I_{o,max} = \frac{V_{o,max}}{R_o} \tag{4.11}$$

From the equivalent circuit shown in Figure 4.3b, the maximum output voltage $V_{o,max}$ can be expressed as

$$V_{o,max} = V_1 + V_{c1} + V_2 + V_{c2} + \ldots + V_x + V_{cx} \tag{4.12}$$

The peak power rating and effective resistance of each boost capacitor are given as

$$P_{cx} = V_{cx} I_{o,max} \tag{4.13}$$

$$R_{cx} = \frac{V_{cx}^2}{P_{cx}} = \frac{V_{cx} R_o}{V_{o,max}} \tag{4.14}$$

The critical inductance of the x^{th} converter is expressed as

$$L_{xB} = \frac{(1-\delta_x)^2 R_{cx}}{2 f_s} = \frac{(1-\delta_x)^2 R_o V_{cx}}{2 V_{o,max} f_s} \tag{4.15}$$

Thus, the ripple current of inductor L_x is

$$\Delta I_{Lx} = \frac{V_x \delta_x}{L_x f_s} \tag{4.16}$$

The critical capacitance of the x^{th} converter is

$$C_{xmin} = \frac{I_{o,max} \delta_x T_s}{\Delta V_{cx}} = \frac{V_{o,max} \delta_x}{\Delta V_{cX} R_o f_s} \tag{4.17}$$

where ΔV_{cx} is the ripple voltage of capacitor C_x. By using (4.16) & (4.17), the critical values of inductance and capacitance of the proposed MLI for symmetrical operation with x = 1 & 2 are analyzed and corresponding characteristic curves are demonstrated in Figure 4.5. Figure 4.5a indicates that the critical inductance decreases with increase in frequency, but increases with increase in load resistance and vice-versa. For a ripple voltage of 5%, the variation of critical capacitance as a function of R_o under different switching frequencies is illustrated in Fig 4.5b.

Table 4.3: Comparison of IBDIMLI with existing MLI topologies

Parameter	**[69]**	**[74]**	**[70]**	**[66]**	**[75]**	**Proposed**	**[64]**	**Proposed**	**Proposed**
N_{lev}	7	7	7	7	7	**7**	**17**	**17**	**31**
N_{swi}	10	14	13	10	8	**9**	18	**14**	**14**
N_{dri}	10	14	13	10	8	**9**	18	**14**	**14**
N_{dio}	4	2	3	0	4	**1**	2	**2**	**2**
N_{dc}	1	1	1	1	1	**1**	2 (sym)	**2 (sym)**	**2 (asym)**
N_{cap}	4	2	3	2	2	**1**	4	**2**	**2**
N_{ind}	1	0	1	0	1	**1**	0	**2**	**2**
Cap. Size	Bulky	Bulky	Bulky	Bulky	Small	**Small**	Bulky	**Small**	**Small**
Gain	1	3	3	3	3	**3**	2	**4**	**4**
CSDC	No	Yes	No	Yes	No	**No**	Yes	**No**	**No**
TSV	5.33	4.67	5.33	5.33	7	**7**	6	**7**	**7**
CVD	Yes	Yes	Yes	Yes	No	**No**	Yes	**No**	**No**
DAC	5	6	7	6	3	**4**	6	**6**	**6**

Note: Cap. Size= Capacitor size; CSDC=Current Spikes During Charging; CVD= capacitor voltage drooping; sym= symmetrical voltage sources; asym= asymmetrical voltage sources

4.3 Comparative Analysis

In this section, a comparative study between proposed and recent MLI topologies interms of the total number of semiconductor devices, sources, passive components, capacitors size,

efficiency and cost is presented. The quantitative values are provided in Table 4.3 and 4.4.

Generally, the total number of active and passive components utilized in the topology will decide its cost and size. The proposed topology with x=1 produces a maximum 7-level output by utilizing single source, nine switches, one diode, one capacitor and one inductor only. From Table 4.3, it can be noticed that the proposed topology for 7 level operation utilizes lesser number of devices and capacitors than the other MLI topologies [66, 69, 70, 74]. Except MLI [69], remaining 7-level MLI topologies including the proposed topology can provide a voltage gain of 3.

The IBDIMLI provides higher output voltage levels with cascaded FLUs operation. For example, the proposed topology with two basic FLUs and symmetric sources can generate 17-level output and the same circuit with two asymmetrical sources can produce 31-levels in the output waveform. The details of components for 17 and 31-level operation of the proposed topology are displayed in Table 4.3. From the table, it can be observed that the IBDIMLI in symmetrical 17-level operation requires lesser components and provides higher gain than the MLI [64].

Generally, the size, cost and reliability of any power converter depends upon rating and the number of capacitors utilized in the circuit. The low-frequency parallel charge and series discharge of capacitors in [64, 66, 69, 70, 74] require a large number of bulky capacitors, which are costly and less durable. Whereas the IBDIMLI, charges the capacitors at high frequency, hence requires less number of small size capacitors.

For an output power of 500 W with V_{dc}=100 V and $V_{o,max}$=300 V, the required component ratings of boost MLIs [66, 70, 74] and the IBDIMLI for 7-level operation are obtained through the simulation studies in PSIM software. Additionally, voltage ripple of 5% is considered for each capacitor voltage. The suitable part numbers and the cost of each component are provided in Table 4.4. From the table, it can be observed that the majority cost of existing 7-level boost MLIs [66, 70, 74] is mainly due to the bulky capacitors and the driver circuits. Even though the IBDIMLI requires higher voltage rated switches and additional components such as, voltage sensor and boost inductor, its overall cost is lower than the other MLIs [66, 70, 74].

In conventional SCMLI topologies, impulse current flows during the charging of a capacitor as shown in Figure 2.12, which demands high current rated switches and results in increased cost of the MLI.

Table 4.4: Cost comparison of IBDIMLI with existing 7-level boost inverter topologies

Components	Required Rating	Nearest Part Number (Rating)	Unit Price ($)	[74] [2018]	[70] [2019]	[66] [2020]	Proposed
MOSFETS	100V/2.8A	IRFI640GPBF (200V/10A)	1.92	$S_{11}-S_{13}, S_{21}$ $S_{23}, S_{31}, -S_{34}$	S_{11}, S_{13}, S_{21}, S_{23}, S_{31}, S_{33}	S_{10}, S_{11}	S_{V1}, S_{V1P}
	100V/6.1A			S_{14}, S_{15}, S_{22}, S_{24}, S_{25}	S_{12}, S_{14}, S_{22}, S_{24}, S_{32}, S_{34}	S_1, S_2, S_3, S_4, S_{6A}, S_{6B}	
	200V/2.8A	FQP17N40 (400V/16A)	2.63			S_8, S_9	S_{C1}, S_{C1P}
	200V/6.1A					S_5, S_7	
	300V/2.8A	IPA60R125C (600V/11A)	3.64				$S_{H1}-S_{H4}$
	300V/5A				S_{Ch}		
	300V/20A	FCP104N60 (600V/37A)	3.74				S_{B1}
DIODES	100V/2A	DPG20C200PB (200V/10A)	1.59		D_2		
	100V/5A			D_{25}			
	100V/10A	D20LC20U-7000 (200V/15A)	3.2	D_{15}			
	200V/3A	DPG10P400P (400V/10A)	2.62		D_1, D_3		
	300V/5A	STPSC2006CW (600V/20A)	6.36		D		
	300V/10A						D_{B1}
INDUCTORS	6mH/10A	B66387G1000X187 & AUXILARIES	4.44		L		
	125UF/20A						L_1
CAPACITORS	560UF/200V	B43548A9127M060 (560UF/400V)	3.5				C_1
	3300UF/100V	ALS31A332KF200 (3300UF/200V)	25.13		C_1, C_2, C_3	C_1, C_2	
	4700UF/100V	ALS30A472MF200 (4700UF/200V)	33.28	C_1, C_2			
NO.OF DRIVERS	A3120 & auxilaries		10	14	13	12	**9**
SENSOR	0-500V	LV-20NP (0-1000V)	50				**1**
TOTAL COST ($)				239.84	255.26	197.58	**184.58**

Note: Components values are taken from www.mouser.com and www.digikey.com

To avoid the capacitor impulse current, a quasi-resonant inductor [69] & [70] is employed in the charging path, which provides adequate impedance during charging and thereby limiting the peak current amplitude. The capacitor current with quasi-resonant SC cell is shown

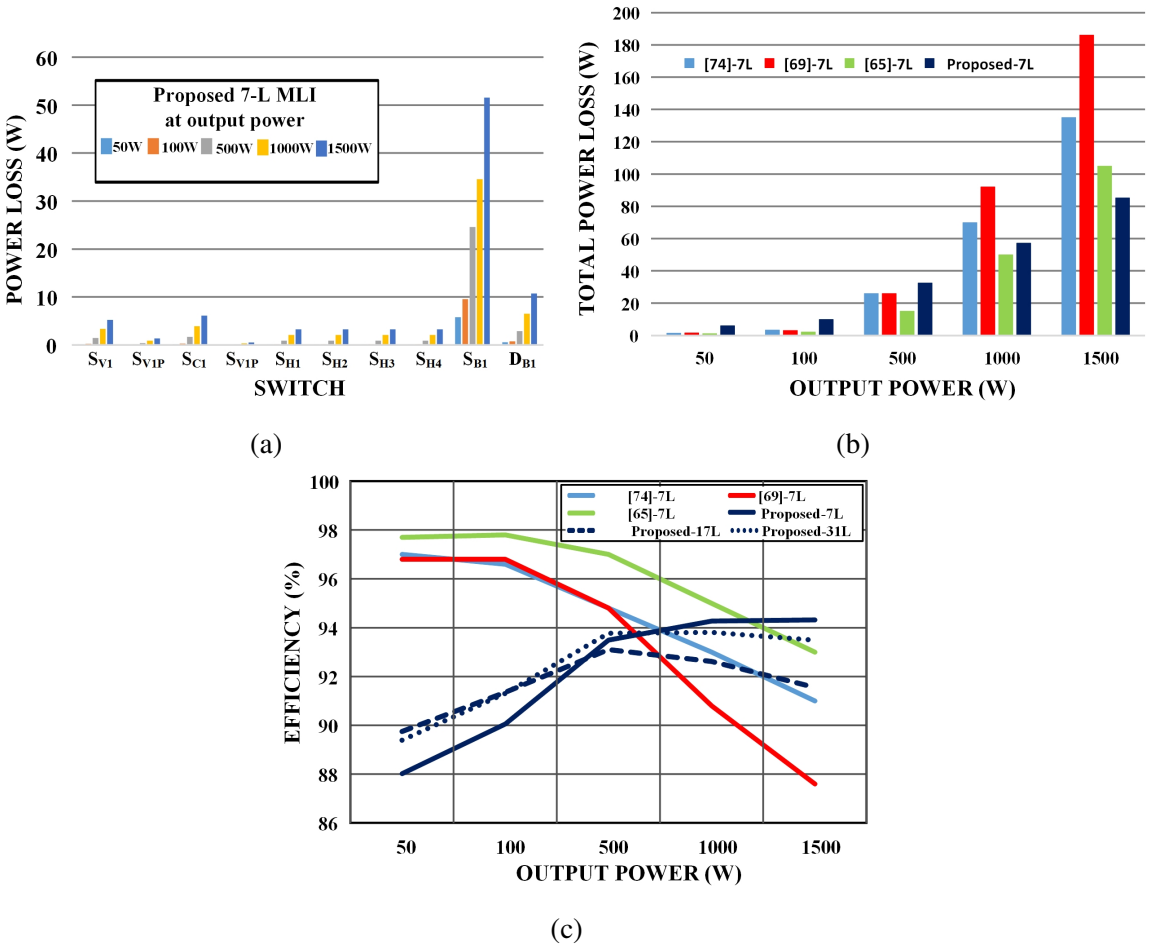


Figure 4.6: Comparison of (a) power loss of switches of IBDIMLI (b) total power loss distribution and (c) efficiency characteristics of proposed MLI with recent boost MLIs at different output powers.

in Figure 2.15.

The quasi-resonant SC cell needs a high value of inductance to reduce the charging current amplitude, which results in increased size and cost of the MLI. Whereas, in the proposed topology the capacitors charge through BBC. The inductor L_B presented in BBC limits the peaky charging current and is expressed in (4.16). As the BBC operates at the higher switching frequency, L_B is lesser compared to quasi-resonant cell [69] & [70].

As shown in Figures 2.12 and 2.15, the capacitor voltages of conventional or quasi-resonant SC cell are drooping in level-2 (i.e.,$V_{dc} + v_c$). The duration of level-2 is directly proportional to the capacitor ripple voltage. Hence, bulk capacitors are required to limit the ripple voltage for long discharging intervals. As shown in Figure 3.3, FLU cell charges the capacitor at high switching frequency, while delivering the load. Hence, prevents the drooping nature

with a small size capacitor.

The IBDIMLI's thermal model is developed in PSIM software [1, 73] to determine the power losses and efficiency at different output powers for 7-, 17- and 31-levels of operation. The parameters of IGBT and diode from the datasheets are loaded into the thermal switch and diode module in PSIM. The power loss and efficiency of the IBDIMLI and other 7-level boost MLI topologies are illustrated in Figures 4.6b and 4.6c respectively. From Figure 4.6c, it can be observed that the efficiency characteristics of 7-level boost MLIs [66, 70, 74] are drooping with respect to output power. The IBDIMLI provides significantly improved efficiency at high power conditions in contrast to the other MLIs [66, 70, 74].

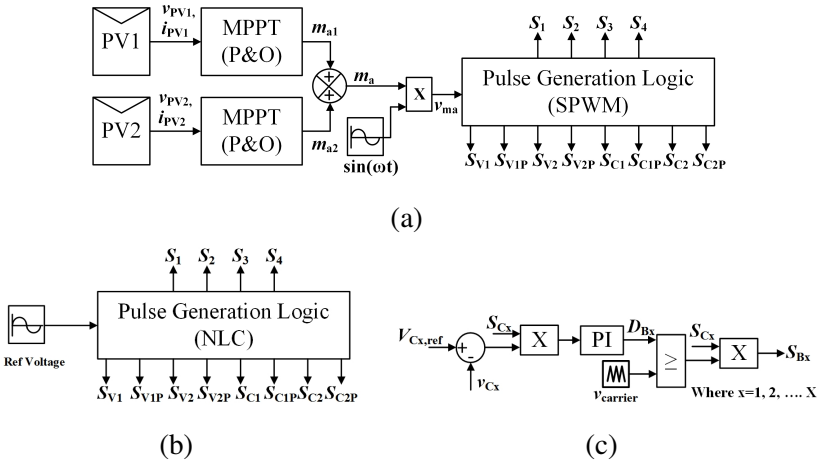
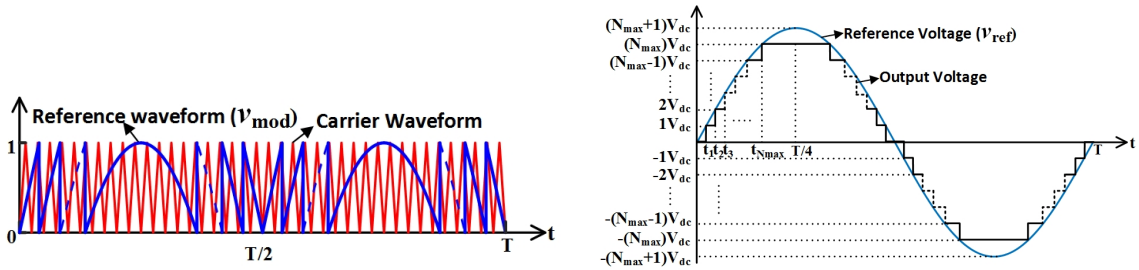


Figure 4.7: Block diagram of control logic: (a) SPWM control (b) NLC (c) closed-loop PI controller for capacitor voltage V_{Cx}.

4.4 Experimental Results

SPWM and NLC schemes are employed for the IBDIMLI operation. The control block diagrams and reference waveforms are depicted in Figures 4.7 & 4.8 respectively. The BBC capacitor voltages of the inverter are regulated at the desired values by closed-loop PI controller as shown in Figure 4.7c either in SPWM or NLC modulation.

The IBDIMLI with SPWM is useful in applications such as, variable AC voltage converters for drives, and also for PV inverters to track maximum power point. In PV applications, each source utilizes a separate MPPT controller and generates the control signals m_{a1} and m_{a2} respectively. The sum of m_{a1} and m_{a2} is multiplied by a unit amplitude sine wave of the fundamental frequency to produce v_{ref}. Further, v_{ref} is used to generate v_{mod} waveform as shown in



(a) (b)

Figure 4.8: Modulation scheme of the proposed MLI for (a) SPWM control (b) NLC control

Figure 4.8a, which is expressed as

$$v_{mod} = |v_{ref}| - i \quad if \quad i < |v_{ref}| \leq i+1 \tag{4.18}$$

Where, 'i' is a positive integer varying from 0 to (peak level-1) and represents the present lowest level of the MLI operation. For example, the $|v_{ref}|$ is 2.2 then 'i' will be 2 and v_{mod} will be 0.2. The respective v_{mod} is compared with the triangular waveform v_{tri} of frequency f_{tri} and the inverter switches between level 2 and 3.

The IBDIMLI with NLC produce less voltage THD, hence suitable for UPS and variable speed drive applications. The model waveform of NLC is presented in Figure 4.8b. In NLC, the nearest integer of the v_{ref} is considered as the level of the MLI.

To ensure the equal power-sharing among the isolated DC sources in symmetrical operation with x=2, the redundant switching states of $\pm V_{dc}$, $\pm 3V_{dc}$, $\pm 4V_{dc}$, $\pm 5V_{dc}$ & $\pm 7V_{dc}$ levels as shown in Table 4.2 are used. During the positive period of the reference sinusoidal waveform, the switching states that connect V_1 or/and v_{c1} is given high priority. Similarly, the switching states that connect the V_2 or/and v_{c2} is given high priority during the negative period. Hence, in a reference cycle, the average power drawn from each source is equal and the average powers $P_{1,avg}$ & $P_{2,avg}$ of sources V_1 & V_2 are expressed in (4.19) and (4.20) respectively.

$$P_{1,avg} = \frac{1}{T}\frac{2V_{dc}^2}{R_o}\left[\sum_{k=1,2,4,5,7,8}(T_k) + \sum_{k=-(2,5,8)}(T_k) + 3\sum_{k=3,4,5,6,7,8}(T_k) + 3\sum_{k=-(6,7,8)}(T_k)\right] \tag{4.19}$$

Table 4.5: Specification & Design Parameters of the IBDIMLI for experimental study

Parameter	**Symmetrical 17-level**	**Asymmetrical 31-level**
V_1, V_2	40 V, 40 V	22 V, 88 V
V_o(RMS)	220 V	230 V
P_o	500 W	
f_o	50 Hz	
f_s, f_{tri}	10 kHz, 10 kHz	
L_1, L_2	500 μH, 500 μH	
C_1, C_2	200 μF / 400 V, 200 μF / 400 V	
Switches	IKW40T120	
Diodes	STPSC2006CW	

$$P_{2,avg} = \frac{1}{T}\frac{2V_{dc}^2}{R_o}\left[\sum_{k=2,5,8}(T_k) + \sum_{k=-(1,2,4,5,7,8)}(T_k) + 3\sum_{k=6,7,8}(T_k) + 3\sum_{k=-(3,4,5,6,7,8)}(T_k)\right] \quad (4.20)$$

Where, k is the voltage level, T is the time period of the reference wave and T_k (time duration of k^{th} level) = $sin^{-1}((|\,k\,|+1)/9) - sin^{-1}(|\,k\,|/9)$.

Figure 4.9: Experimental prototype of the proposed IBDIMLI.

To verify the symmetrical and asymmetrical operation of the IBDIMLI, an experimental prototype is developed and is depicted in Figure 4.9. A TMS320F28379D launchpad is used to realize the control pulses to the switches present in the MLI. The specifications of the hardware

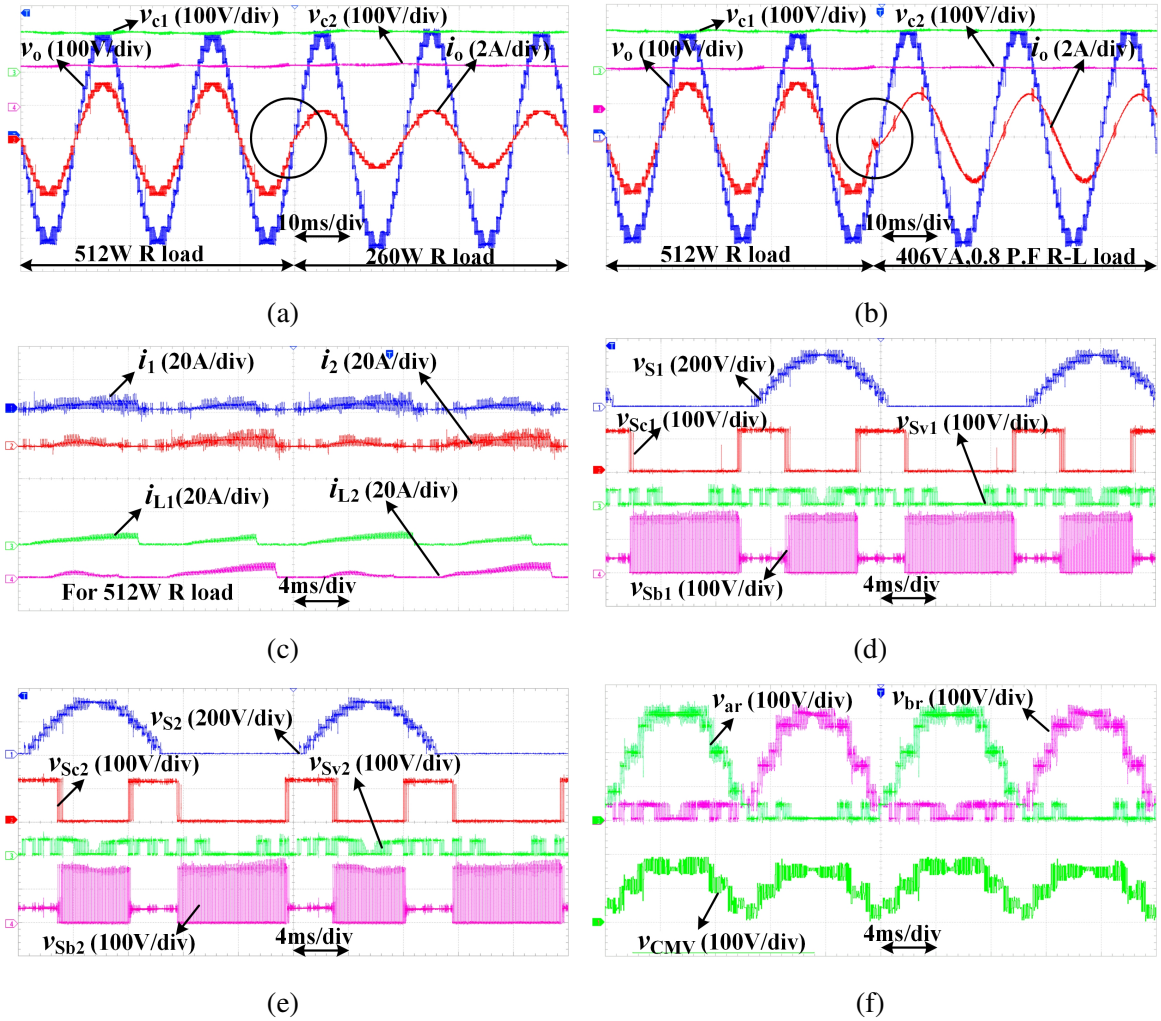


Figure 4.10: Experimental waveforms of 17-level operation with SPWM: (a) v_o, i_o, v_{c1} & v_{c2} for a step change in R load (b) v_o, i_o, v_{c1} & v_{c2} for a step change in load i.e., R-load to R-L load (c) i_1, i_2, i_{L1} & i_{L2} (d) voltage of switches S_1, S_{C1}, S_{V1} & S_{B1} (e) voltage of switches S_2, S_{C2}, S_{V2} & S_{B2} (f) v_{ar}, v_{br} & v_{CMV}

for both symmetrical (17-level) and asymmetrical (31-level) operation with two FLUs are specified in Table 4.5.

A. Symmetrical 17-level Operation

For the 17-level operation, the inverter is powered from two isolated symmetrical voltage sources of 40 V magnitude and provides 220 V (RMS) output voltage. From (4.2) & (4.6), the boost factor of FLU is determined as 3 and each capacitor reference voltage is 120 V. The IBDIMLI's symmetrical 17-level operation is tested for R & R-L loads with SPWM and NLC and all the corresponding experimental waveforms are presented in Figures 4.10 and 4.11 respectively. Figures 4.10a, 4.10b, 4.11a & 4.11b the smooth transient operation IBDIMLI with

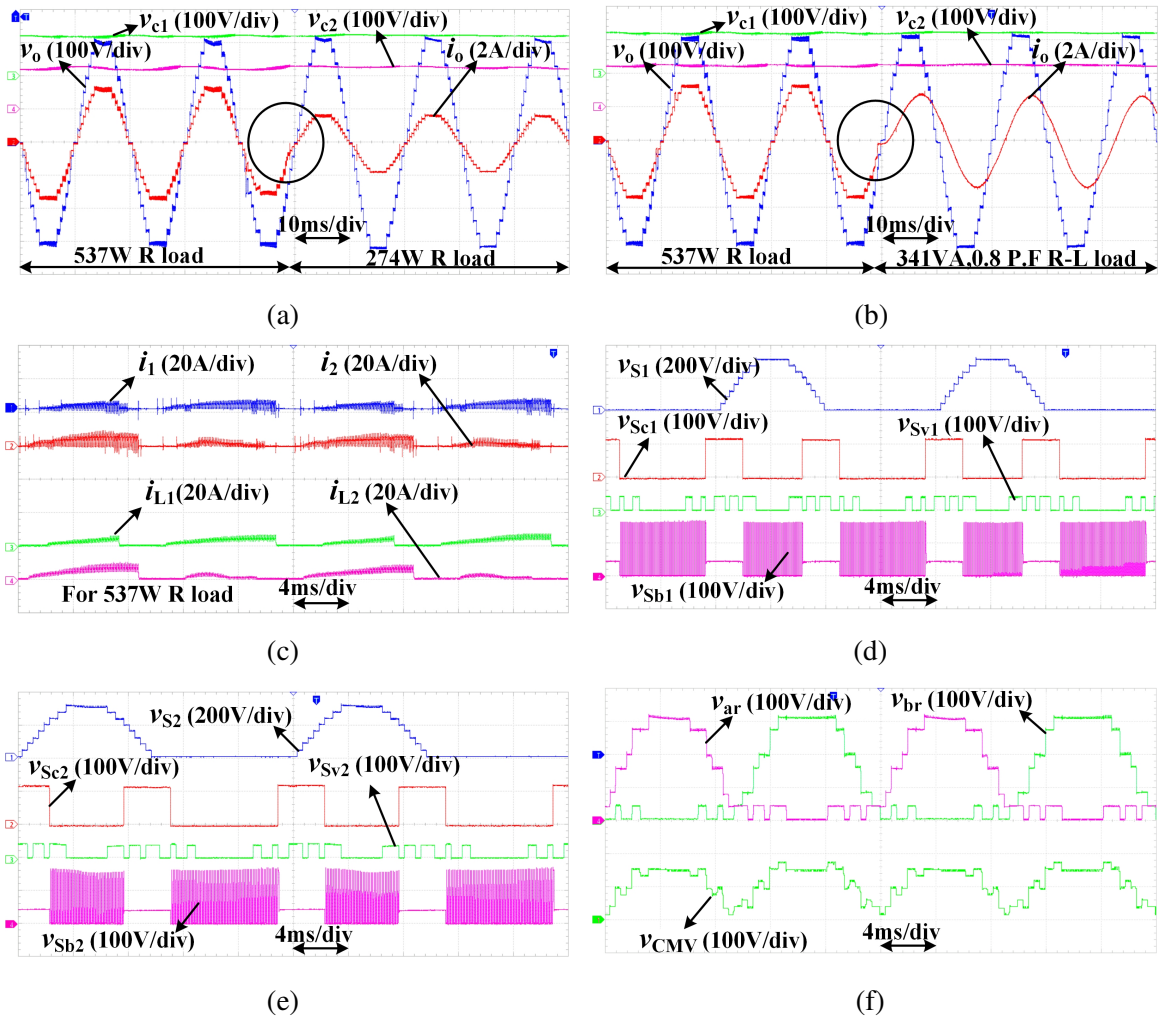


Figure 4.11: Experimental waveforms of 17-level operation with NLC: (a) v_o, i_o, v_{c1} & v_{c2} for a step change in R load (b) v_o, i_o, v_{c1} & v_{c2} for a step change in load i.e., R-load to R-L load (c) i_1, i_2, i_{L1} & i_{L2} (d) voltage of switches S_1, S_{C1}, S_{V1} & S_{B1} (e) voltage of switches S_2, S_{C2}, S_{V2} & S_{B2} (f) v_{ar}, v_{br} & v_{CMV}

step change in load, while maintaining the stable output voltage and capacitor voltages. The source and inductor current waveforms, which are shown in Figures 4.10c, 4.11c prove that the boost converter of respective FLUs operate for a short duration and hence, provides reduced power loss. The switch voltage waveforms of IBDIMLI are depicted in Figures 4.10d, 4.10e, for SPWM and Figures 4.11d & 4.11e for NLC respectively. Figures. 4.10f & 4.11f illustrates the pole voltage v_{ar}, v_{br} and CMV v_{CMV} waveform for SPWM and NLC operation respectively. The harmonic spectrum of the load voltage and load currents for R & R-L loads with SPWM and NLC are presented in Figures 4.13a and 4.13b respectively. Without a filter, the measured THD of v_o for R as well as R-L load is 7.606%, and THD of i_o for R load & R-L load are

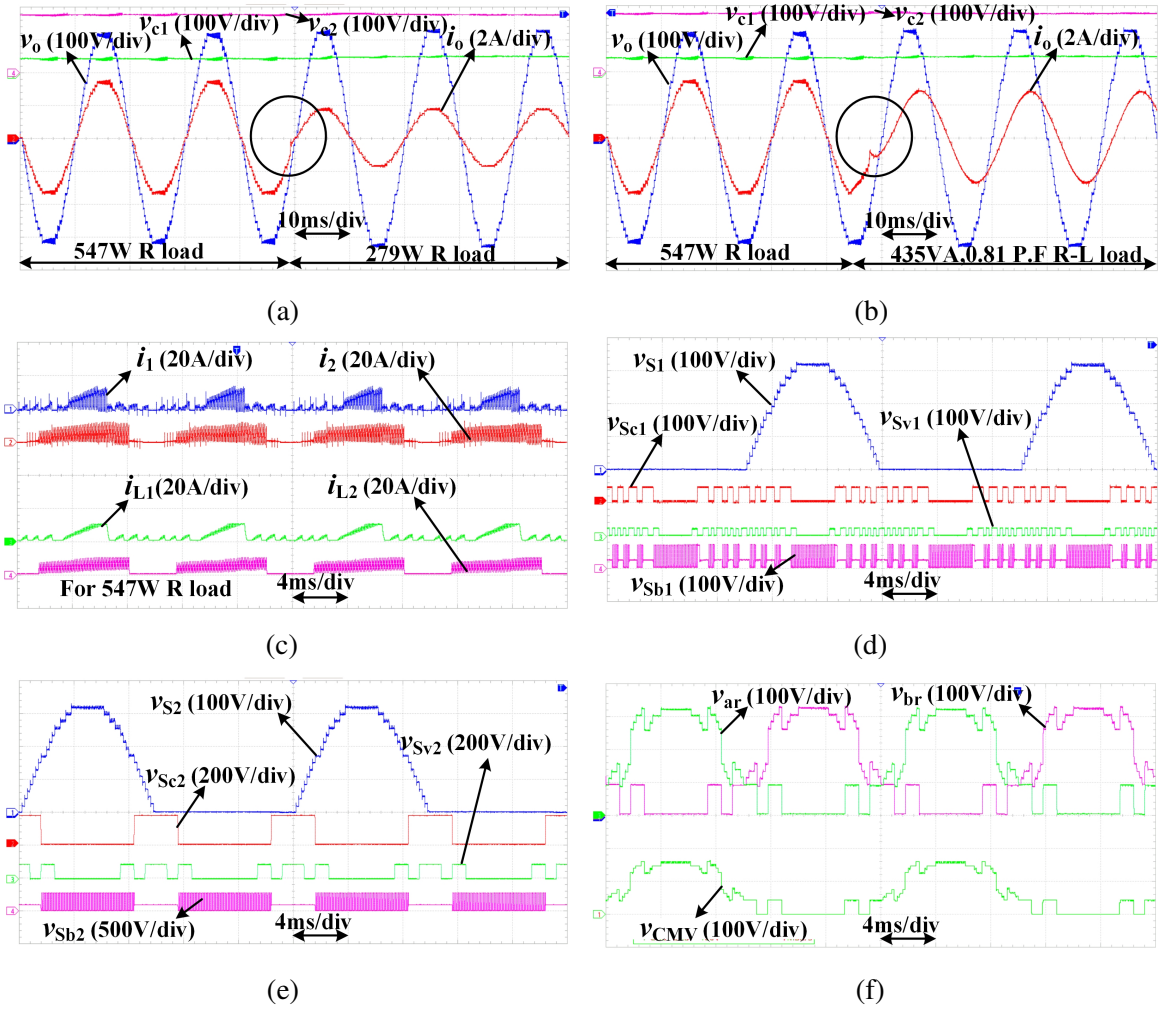
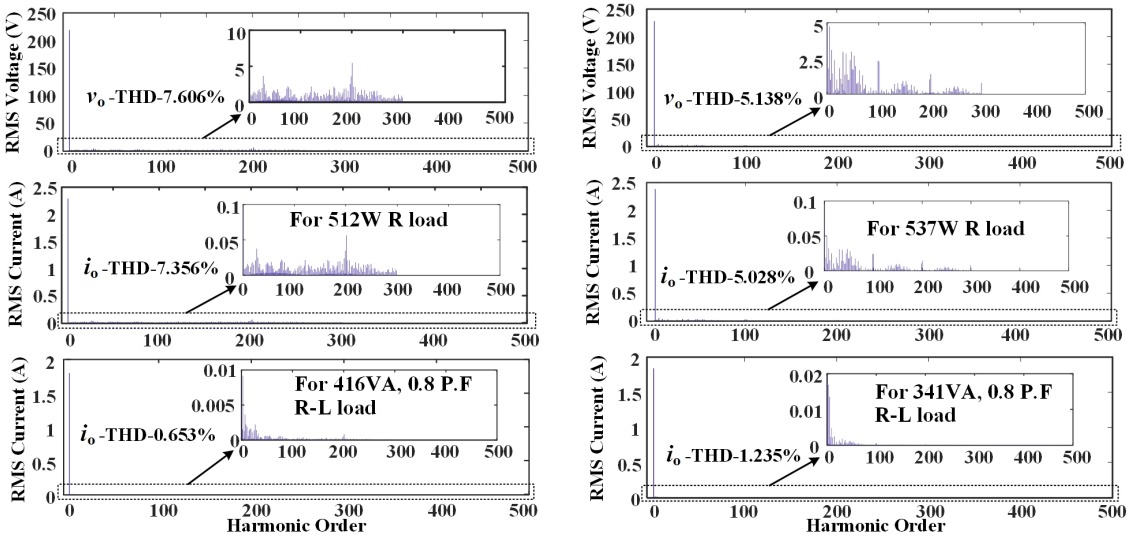


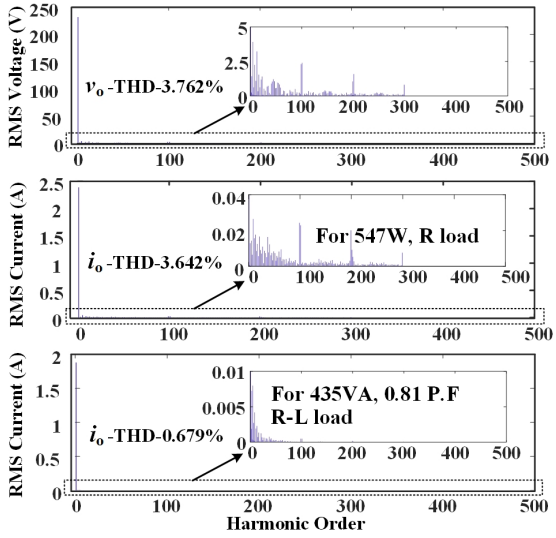
Figure 4.12: Experimental waveforms of 31-level operation with NLC: (a) v_o, i_o, v_{c1} & v_{c2} for a step change in R load (b) v_o, i_o, v_{c1} & v_{c2} for a step change in load i.e., R-load to R-L load (c) i_1, i_2, i_{L1} & i_{L2} (d) voltage of switches S_1, S_{C1}, S_{V1} & S_{B1} (e) voltage of switches S_2, S_{C2}, S_{V2} & S_{B2} (f) v_{ar}, v_{br} & v_{CMV}

7.356% & 0.653% with SPWM, which are shown in Figure 4.13a. As shown in Figure 4.13b, for NLC modulation, those are measured as 5.138%, 5.028% & 1.235% respectively. Though the THD of load voltage is higher with SPWM than the NLC, the dominant harmonic component is at high frequency. Thus, the THD of the load current for R-L load is better with SPWM than the NLC.

B. Asymmetrical 31-level Operation

The asymmetrical 31-level operation is realized by two isolated unequal voltage sources of V_1=22 V and V_2=88 V and provides 230 V (RMS) output voltage. The step-up ratio of 2 is





(c)

Figure 4.13: Experimental waveforms of harmonic spectrum of load voltage and load current with R load and R-L load for (a) 17-level operation with SPWM (b) 17-level operation with NLC (c) 31-level operation with NLC

considered for each FLU operation. The IBDIMLI's asymmetrical 31-level operation with NLC is tested for R & R-L loads and the corresponding experimental waveforms are presented in Figure 4.12. In addition, the dynamic behaviour of the MLI for 31-level asymmetric operation is tested by applying step change in load conditions (i.e., R to R load and R to R-L load) as depicted in Figures 4.12a and 4.12b respectively. From these figure, the smooth transient operation of the IBDIMLI is confirmed, while maintaining the stable output voltage for 31-level

operation. The source and inductor current waveforms are shown in Figure 4.12c and the switch voltage waveforms of IBDIMLI are depicted in Figures 4.12d & 4.12e. Figure 4.12f illustrates the pole voltage v_{ar}, v_{br} and CMV v_{CMV} waveform for NLC operation, which confirms the low frequency nature of the CMV. The harmonic spectrum of the load voltage and load currents for R & R-L loads with NLC are presented in Figure 4.13c. Without a filter, the measured THD of v_o for R & R-L load is 3.702% and THD of i_o for R load & i_o for R-L load are 3.642% & 0.679% with NLC, which are less than the 5%.

4.5 Summary

In this chapter, an improved new generalized boost integrated MLI with reduced components is proposed. The generalized operation of the IBDIMLI for symmetrical and asymmetrical operation with detailed design analysis is explained. Also, the IBDIMLI is compared with the other existing MLIs in terms of the number of active, passive components utilized and the output voltage levels. From this comparative study, it is observed that the IBDIMLI requires less component count as compared to other MLIs with reduced charging current and eliminated capacitor voltage drooping with increased load conditions. Also, provides improved efficiency at high power ratings than the other MLIs. In addition, the capacitor size and overall cost are less than the recent boost MLI counterparts. A 500 W proof-of-concept of proposed MLI is developed and tested for symmetrical 17-level operation with SPWM & NLC and also, an asymmetrical 31-level operation with NLC for R and R-L load under dynamic load conditions. Stable and smooth operation is achieved for dynamic load conditions, while maintaining the output voltage and capacitor voltages. With NLC modulation, without filter, the IBDIMLI achieved output voltage THD as 5.138% and 3.702% for 17-level and 31-level operations respectively. Using SPWM, the IBDIMLI achieved an output voltage THD of 7.606% for the 17-level operation without filter. Also, the THD of load current with R-L load is well below the 5% according to IEEE-1547 standards in both SPWM and NLC. The low-frequency operation of NLC provided a low frequency CMV, hence results in less leakage current. The proposed IBDIMLI with NLC can produce low THD output voltage, which is suitable for UPS or EV applications with constant DC sources. Otherwise, it can also be employed for drives and PV applications with SPWM.

Chapter 5

Single-source Buck-boost Integrated 13-level Inverter

Chapter 5

Single-source Buck-boost Integrated 13-level Inverter

5.1 Introduction

The proposed BDIMLI and IBDIMLI topologies presented in Chapter 3 and Chapter 4 respectively are developed for multiple PV panel configurations. However, for PV AC module applications the step-up inverter configurations that utilize single source are essential.

Hence, this chapter proposes a new single-source buck-boost integrated MLI (SBMLI) for 13-level operation with reduced components and compact capacitors, hence results in low cost. Its fundamental cell is constructed by the cascading connection of two BBCs with the source to generate a 6-level output with a gain of two. In comparison to existing SCMLI topologies, the BBCs of the proposed inverter operate at a high switching frequency to minimize capacitor size. Further, existing SCMLI capacitors are restricted to charge at a fixed voltage, while the capacitor voltages of IBDIMLI are adjustable. Thus, require less number of compact capacitors to generate a higher of voltage levels. In this chapter, the design and analysis of IBDIMLI are explained and its operation is validated by using a laboratory 300 W proof-of-concept for different loading conditions. In addition, a detailed comparison of the proposed inverter with recent SCMLIs is offered.

5.2 Working and operating principle of the proposed SBMLI

The proposed SBMLI is depicted in the Figure 5.1. The primary stage of the SBMLI is a level generator circuit (LGC), which generates folded multilevel output v_{o1}. The LGC consists of a input voltage source V_1 and two BBCs namely BBC-1 and BBC-2. BBC-1 consists of switch S_1, diode D_1, inductor L_1 and capacitor C_1. Similarly, BBC-2 consists of switch S_2, diode D_2, inductor L_2 and capacitor C_2. Both the converters BBC-1 and BBC-2 energize from the source V_1 and operates with duty cycles δ_1 and δ_2 at switching frequency f_s to produce capacitor voltages v_{C1} and v_{C2} respectively. The voltage step-up ratios n_1 and n_2 of BBC-1 and

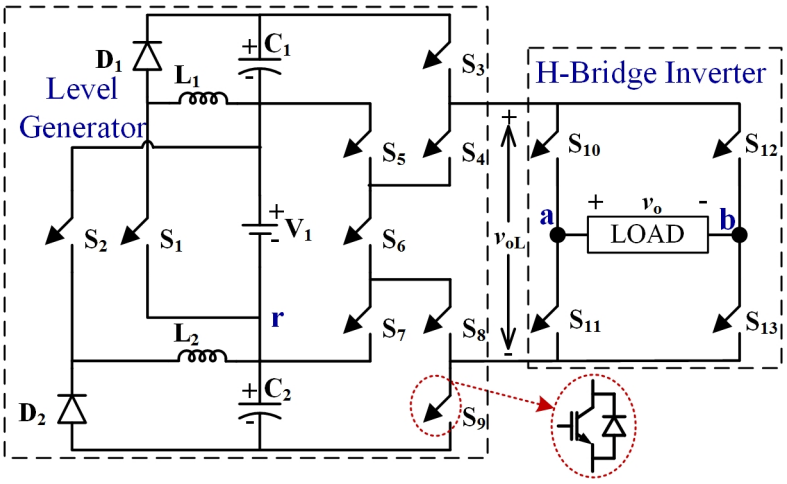


Figure 5.1: Proposed 13-level MLI

BBC-2 are expressed in (5.1) and (5.2) respectively. The switches S_3 - S_9 of the LGC are used to select a combination of voltages from V_1, v_{c1} and v_{c2} to attain a desired voltage level. The secondary stage of the SBMLI is a H-bridge inverter, which is formed by switches S_{10} - S_{13} and operates at output frequency f_o to unfold the v_{o1} and produces output voltage v_o. The duty cycles δ_1 and δ_2 of both BBCs are expressed as follows (5.3) and (5.4).

$$n_1 = \frac{V_{C1}}{V_1} \tag{5.1}$$

$$n_2 = \frac{V_{C2}}{V_1} \tag{5.2}$$

$$\delta_1 = \frac{G_1}{1+G_1} \tag{5.3}$$

$$\delta_2 = \frac{G_2}{1+G_2} \tag{5.4}$$

For 13-level operation, consider n_1 as 1/3, n_2 as 2/3 and V_{c1} as V_{dc} then V_{c2} and V_1 will be $2V_{dc}$ and $3V_{dc}$ respectively. The switching states of the SBMLI for 13-level operation are presented in Table 5.1. The operating condition (ON/OFF) of converters BBC-1 and BBC-2 at different switching states are also presented in Table 5.1, which confirms the integrated operation of the BBCs in the SBMLI. The model waveforms of the SBMLI with NLC modulation are presented in Figure 5.4. By replacing the BBCs with their equivalent output voltages, the equivalent circuits of SBMLI for 13-levels are shown in Figuers 5.2 and 5.3.

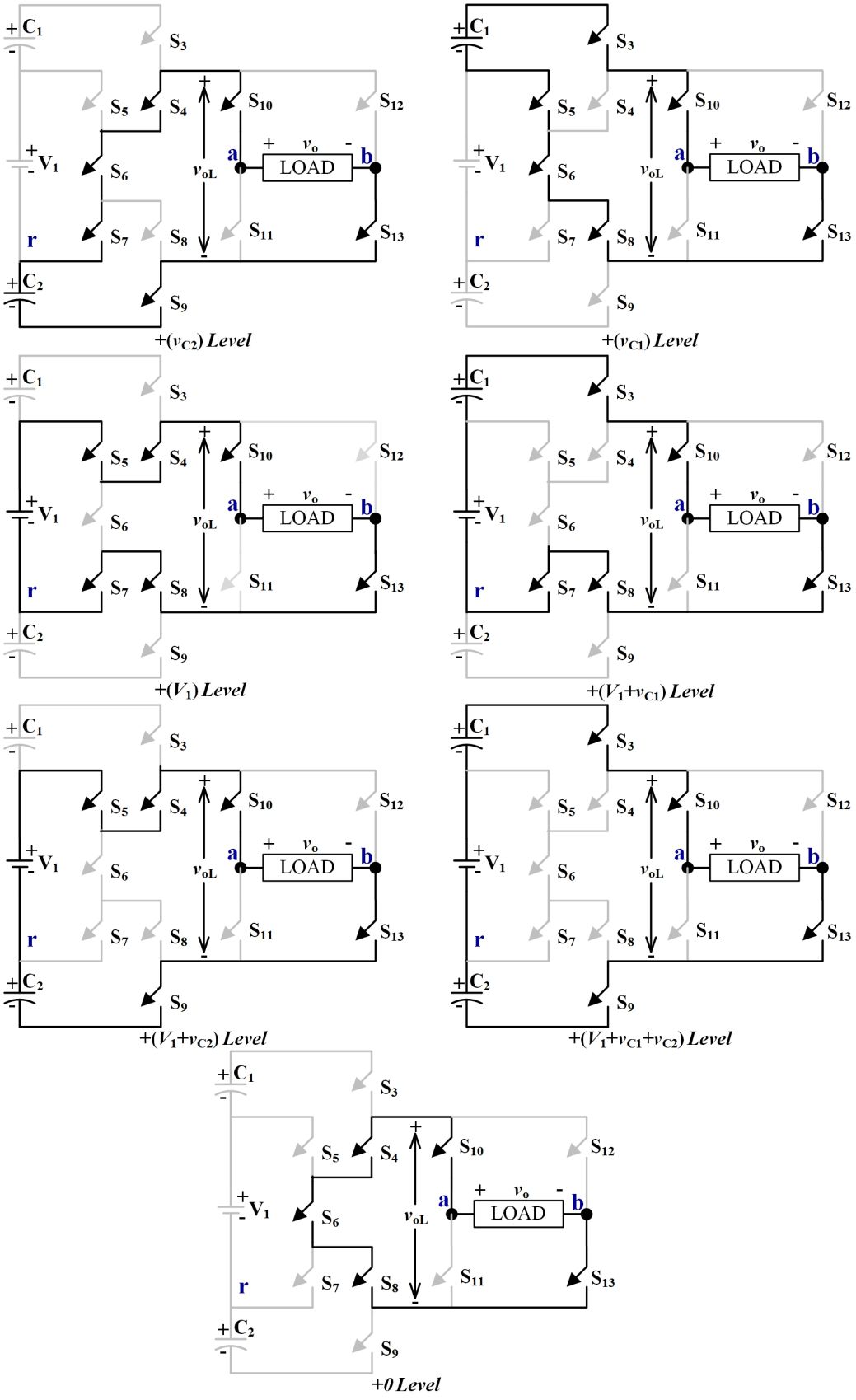


Figure 5.2: Equivalent circuits of SBMLI from +0 V_{dc} to +6 V_{dc}

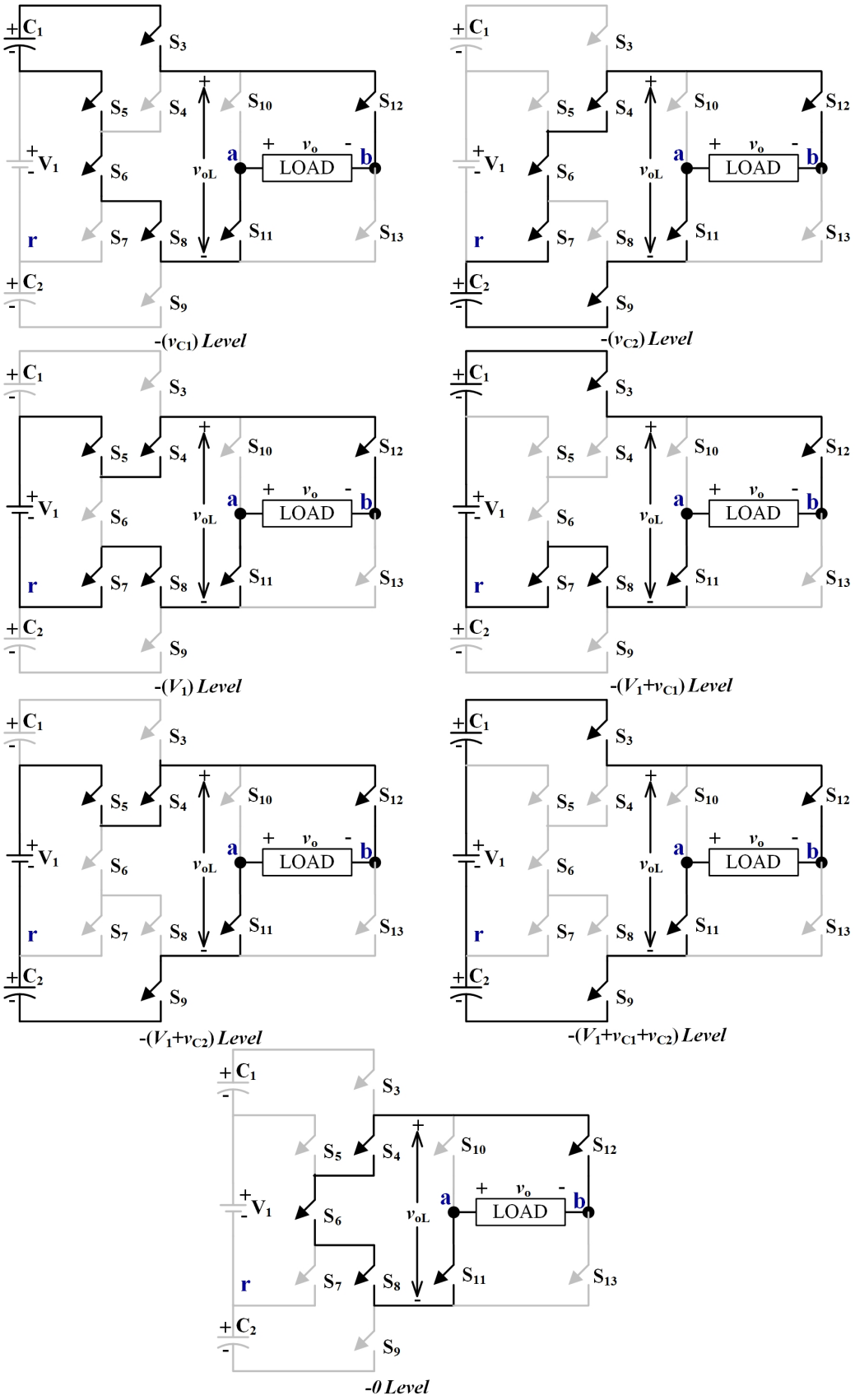


Figure 5.3: Equivalent circuits of SBMLI from -0 V_{dc} to -6 V_{dc}

Table 5.1: Look-up table of SBMLI for 13-level operation with $V_1 = 3\ V_{dc}$, $V_{c1} = V_{dc}$ and $V_{c2} = 2\ V_{dc}$

On State Switches	Buck Boost Converter		Level Generator Output (v_{o1})	H-Bridge Inverter Output (v_o)
	BBC-1	BBC-2		
$S_3, S_5, S_6, S_9, S_{10}, S_{13}$	ON	OFF	$v_{c1} = V_{dc}$	V_{dc}
$S_4, S_6, S_7, S_8, S_{10}, S_{13}$	OFF	ON	$v_{c2} = 2\ V_{dc}$	$2\ V_{dc}$
$S_4, S_5, S_7, S_9, S_{10}, S_{13}$	OFF	OFF	$V_1 = 3\ V_{dc}$	$3\ V_{dc}$
$S_3, S_7, S_9, S_{10}, S_{13}$	ON	OFF	$V_1 + v_{c1} = 4\ V_{dc}$	$4\ V_{dc}$
$S_4, S_5, S_8, S_{10}, S_{13}$	OFF	ON	$V_1 + v_{c2} = 5\ V_{dc}$	$5\ V_{dc}$
S_3, S_8, S_{10}, S_{13}	ON	ON	$V_1 + v_{c1} + v_{c2} = 6\ V_{dc}$	$6\ V_{dc}$
$S_4, S_6, S_9, S_{11}, S_{13}$	OFF	OFF	0	0
$S_4, S_6, S_9, S_{10}, S_{12}$	OFF	OFF	0	0
$S_3, S_5, S_6, S_9, S_{11}, S_{12}$	ON	OFF	$v_{c1} = V_{dc}$	$-V_{dc}$
$S_4, S_6, S_7, S_8, S_{11}, S_{12}$	OFF	ON	$v_{c2} = 2\ V_{dc}$	$-2\ V_{dc}$
$S_4, S_5, S_7, S_9, S_{11}, S_{12}$	OFF	OFF	$V_1 = 3\ V_{dc}$	$-3\ V_{dc}$
$S_3, S_7, S_9, S_{11}, S_{12}$	ON	OFF	$V_1 + v_{c1} = 4\ V_{dc}$	$-4\ V_{dc}$
$S_4, S_5, S_8, S_{11}, S_{12}$	OFF	ON	$V_1 + v_{c2} = 5\ V_{dc}$	$-5\ V_{dc}$
S_3, S_8, S_{11}, S_{12}	ON	ON	$V_1 + v_{c1} + v_{c2} = 6\ V_{dc}$	$-6\ V_{dc}$

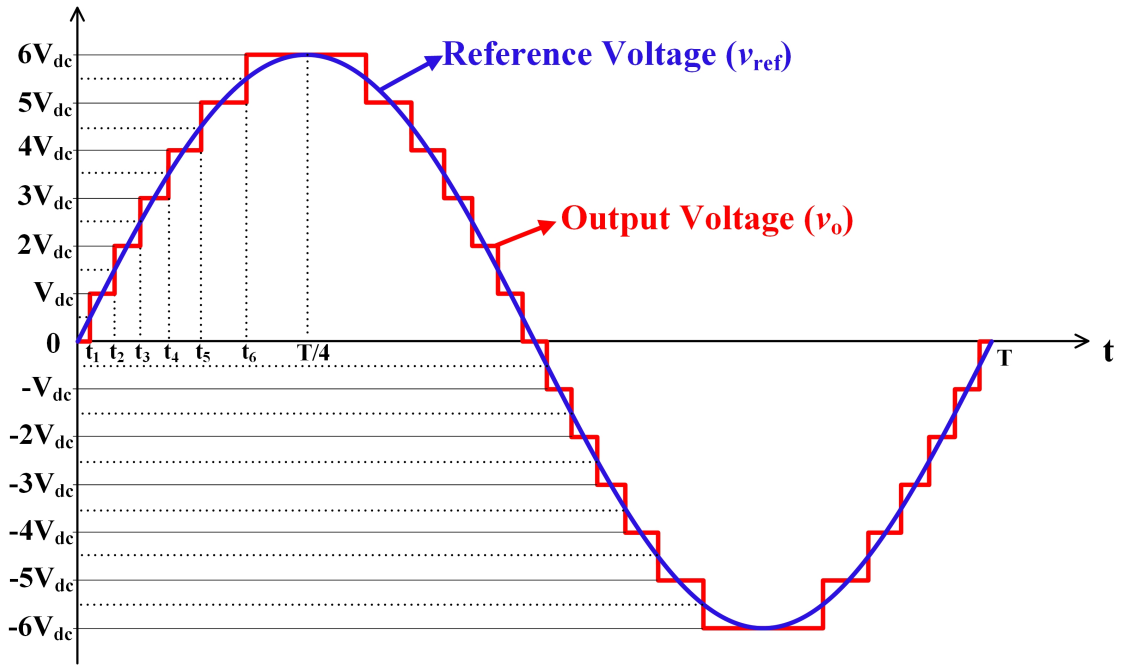


Figure 5.4: Proposed MLI model waveform

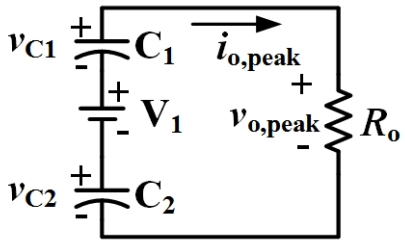


Figure 5.5: Equivalent circuit of the proposed MLI at +6 V_{dc}/-6 V_{dc}

The equivalent circuit of the SBMLI at peak voltage level with resistive load R_o is depicted in Figure 5.5, where the BBCs output terminals are represented by voltages V_{c1} and V_{c2} respectively. The peak output voltage $V_{o,max}$ and load current $I_{o,max}$ are expressed as follows

$$V_{o,max} = V_1 + V_{c1} + V_{c2} = 6V_{dc} \tag{5.5}$$

$$I_{o,max} = \frac{V_{o,peak}}{R_o} = \frac{6V_{dc}}{R_o} \tag{5.6}$$

The peak powers P_{c1} and P_{c2} processed by the BBC-1 & 2 are given as follows

$$P_{c1} = V_{c1} I_{o,max} \tag{5.7}$$

$$P_{c2} = V_{c2} I_{o,max} \tag{5.8}$$

Effective resistances R_{c1} and R_{c2} seen by each BBCs are expressed as follows

$$R_{c1} = \frac{V_{c1} R_o}{V_{o,peak}} \tag{5.9}$$

$$R_{c2} = \frac{V_{c2} R_o}{V_{o,peak}} \tag{5.10}$$

At boundary conduction mode, the boundary inductances L_{B1} and L_{B2} of respective L_1 and L_2 are calculated by matching inductor stored energy and total energy processed by respective

BBC, which are given as follows

$$L_{B1} = \frac{\delta_1^2 R_o}{2n_1(1+n_1+n_2)f_s} \tag{5.11}$$

$$L_{B2} = \frac{\delta_2^2 R_o}{2n_2(1+n_1+n_2)f_s} \tag{5.12}$$

where f_s=switching frequency of BBCs

The smallest capacitance $C_{1,min}$ and $C_{2,min}$ of C_1 and C_2 necessary to keep corresponding percentage voltage ripples x_1 and x_2 of BBC-1 and 2 are expressed as

$$C_{1,min} = \frac{(1+n_1+n_2)\delta_1 * 100}{x_1 n_1 R_o f_s} \tag{5.13}$$

$$C_{2,min} = \frac{(1+n_1+n_2)\delta_2 * 100}{x_2 n_2 R_o f_s} \tag{5.14}$$

The expressions provided in (6.8), (6.9), (6.10) and (6.11) can be used to obtain the minimum values of L_1, L_2, C_1 and C_2 for the operation of proposed 13-level inverter at given load conditions.

The function of BBCs in the SBMLI are discrete and dependent on the particular voltage level, as shown in Table 5.1. Thus, two PI controllers are implemented as shown in Figure 5.6 to regulate the capacitor voltages v_{c1} and v_{c2} as V_{dc} and $2V_{dc}$. The PI controllers generate the control pulses to switches S_1 and S_2 to make BBCs in interleaved operation. The closed loop control of BBCs also aids in the dynamic operation of the proposed inverter.

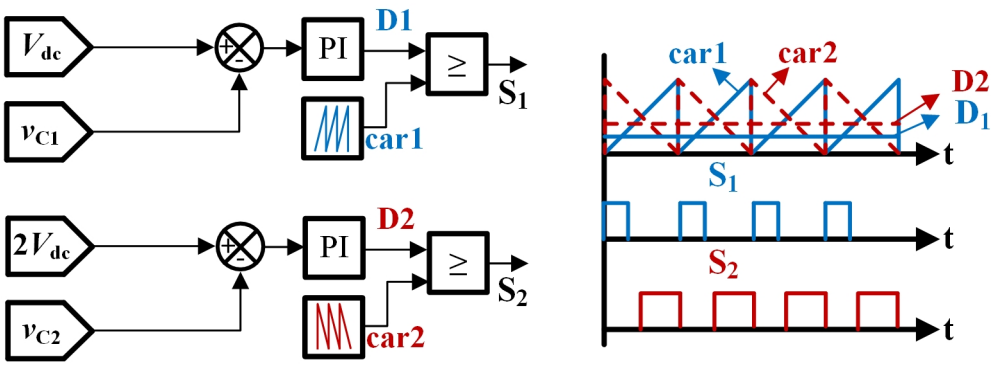


Figure 5.6: Block diagram of closed loop control and pulse generation of BBCs

At peak voltage level, the peak powers of output $P_{o,max}$ and source $P_{S,max}$ are given as

$$P_{o,max} = V_{o,max} I_{o,max} \tag{5.15}$$

$$P_{S,max} = V_{S,max} I_{o,max} \tag{5.16}$$

In SBMLI, 50% of power is handled by the BBCs and the rest is supplied by the dc source. By using (5.7), (5.8), (5.15) and (5.16) the percentage of peak power (P_{c1} & P_{c2}) processed by each BBCs and source is expressed as follows

$$\%P_{c1} = \frac{V_{c1} I_{o,max}}{V_{o,max} I_{o,max}} X100 = 16.67\% \tag{5.17}$$

$$\%P_{c2} = \frac{v_{c2} I_{o,max}}{V_{o,max} I_{o,max}} X100 = 33.33\% \tag{5.18}$$

$$\%P_{S,max} = \frac{V_1 I_{o,max}}{V_{o,max} I_{o,max}} X100 = 50\% \tag{5.19}$$

The contribution of source and BBCs depends upon the required voltage level of operation as depicted in Figure 5.7.

A quarter cycle of output voltage (i.e., from 0 to T/4) is considered to estimate total energy (E_{Total}). The energy processed by BBCs (E_{c1} & E_{c2}) and source (E_S) are expressed as follows

$$E_{Total} = \sum_{i=0}^{6} (t_{i+1} - t_i) * (i * V_{dc})^2 / R_o \tag{5.20}$$

$$E_S = \sum_{i=3,4,5,6} (t_{i+1} - t_i) * (3i * V_{dc}^2) / R_o \tag{5.21}$$

$$E_{c1} = \sum_{i=1,4,6} (t_{i+1} - t_i) * (i * V_{dc}^2) / R_o \tag{5.22}$$

$$E_{c2} = \sum_{i=2,5,6} (t_{i+1} - t_i) * (2i * V_{dc}^2) / R_o \tag{5.23}$$

where i is a positive integer from 0 to 5, t_i and t_{i+1} are the starting and ending instants of

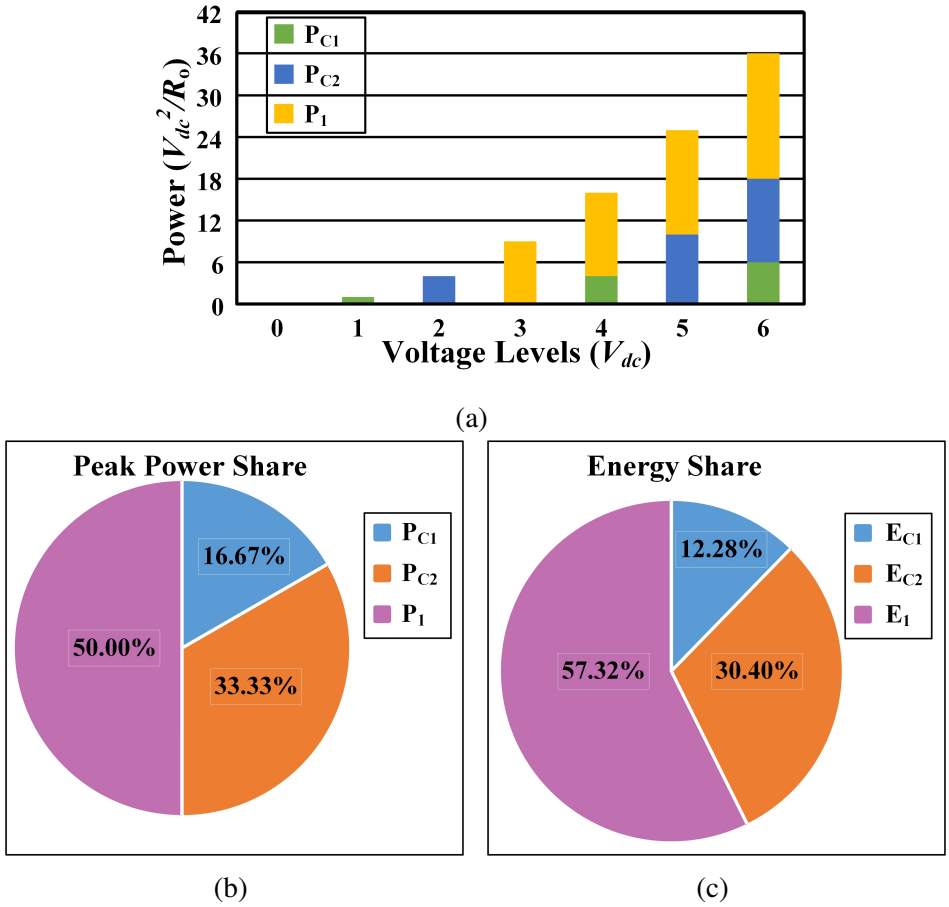


Figure 5.7: Comparison of source and BBCs: (a) power share at each level (b) power share at peak level (c) total energy share.

the i^{th} level. By using (5.20), (5.21), (5.22) and (5.23), the energy ratios of source, BBC 1 and 2 to the total energy are evaluated as 57.32%, 12.28% and 30.40% respectively.

5.3 Comparative analysis

A comparison analysis is conducted to evaluate the merits of the SBMLI over recent 13-level MLI topologies and the results are shown in Table 5.2. Numerous factors of the proposed and existing 13-level SCMLIs such as, device count, capacitor size, gain and inrush current are compared. The MLI [76] uses six isolated sources and 16 switches but provides no voltage gain. The SCMLI [1] attains a gain of 2, but requires more number of isolated sources and other passive components. The SCMLIs [65, 67, 69] and the SBMLI are developed by using single source to achieve 13-level output, which are helpful in PV based AC module applications. The proposed MLI and SCMLIs [65, 67] that are being operated with single source, which

Table 5.2: Comparison of the SBMLI and recent 13-level MLIs

Parameter	**[76]**	**[1]**	**[69]**	**[65]**	**[67]**	**Proposed**
N_{dc}	6	3	1	1	1	1
N_{swi}	16	18	14	18	14	13
N_{dio}	0	3	6	0	0	2
N_{cap}	0	3	6	2	4	2
Capacitor Size	NA	interms of mF	interms of mF	interms of mF	interms of mF	interms of uF
N_{ind}	0	0	1	0	0	2
Gain	1	2	1	3	1.5	2
Inrush current	NA	Yes	No	Yes	Yes	No

NA-Not applicable

Table 5.3: Specifications of the proposed 13-level MLI

Parameter	Value / Part Number
V_1	75 V
V_o (RMS)	110 V
v_{C1}, v_{C2}	25 V, 50 V
f_o	50 Hz
f_s	20 kHz
P_o	220 W
L_1, L_2	500 μH, 500 μH
C_1, C_2	300 μF/50 V, 200 μF/100 V

only provide voltage gain among SCMLIs [65, 67, 69]. The SCMLI [67] provides better gain, however it requires more switches compared to the proposed MLI. All the SCMLIs [1,65,67,69] charge the capacitor at low frequency, hence requires bulky capacitors compared to the SBMLI, which employs high frequency charging. Also, except SCMLI [65] all other SCMLI [1, 67, 69] use higher number of bulky capacitors compared to the SBMLI. Moreover, all the SCMLIs apart from the SCMLI [69] are experiencing inrush current, hence require high current rated devices. Though the SCMLI [69] is free from inrush current by employing a bulky quasi-resonant inductor, it provides no voltage gain. Hence, from this comparison study it is evident that the SBMLI provides better gain with reduced device count and use compact capacitors than the other 13-level SCMLIs [1, 65, 67, 69].

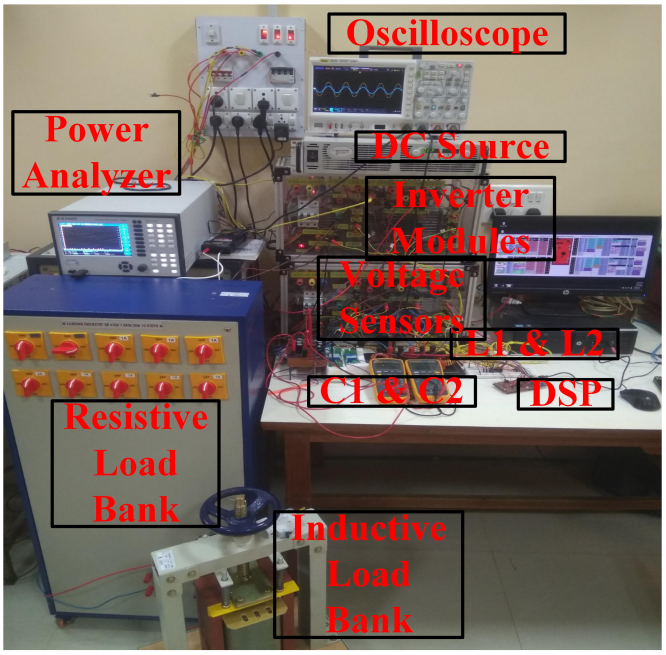


Figure 5.8: Experimental setup of the SBMLI

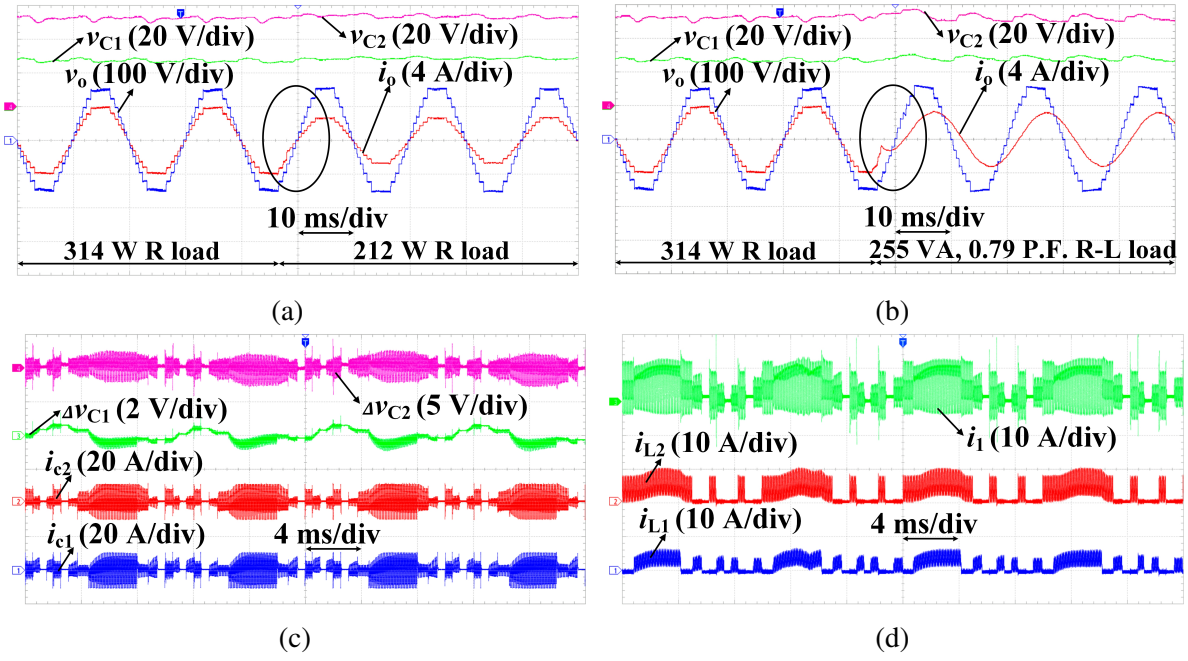


Figure 5.9: SBMLI's experimental results: (a) v_o, i_o, v_{C1} and v_{C2} for sudden variation in R load (i.e., 314 W to 212 W) (b) v_o, i_o, v_{C1} and v_{C2} for sudden variation in load type (i.e., 314 W to 255 VA, 0.79 power) (c) capacitors C_1 & C_2 currents and ripple voltages (d) i_1, i_{L1} and i_{L2}.

5.4 Experimental Results

A 300 W proof-of-concept is developed to demonstrate the desired operation of the SBMLI as shown in Figure 5.8 for the parameters listed in the Table 5.3. The TMS320F28379D

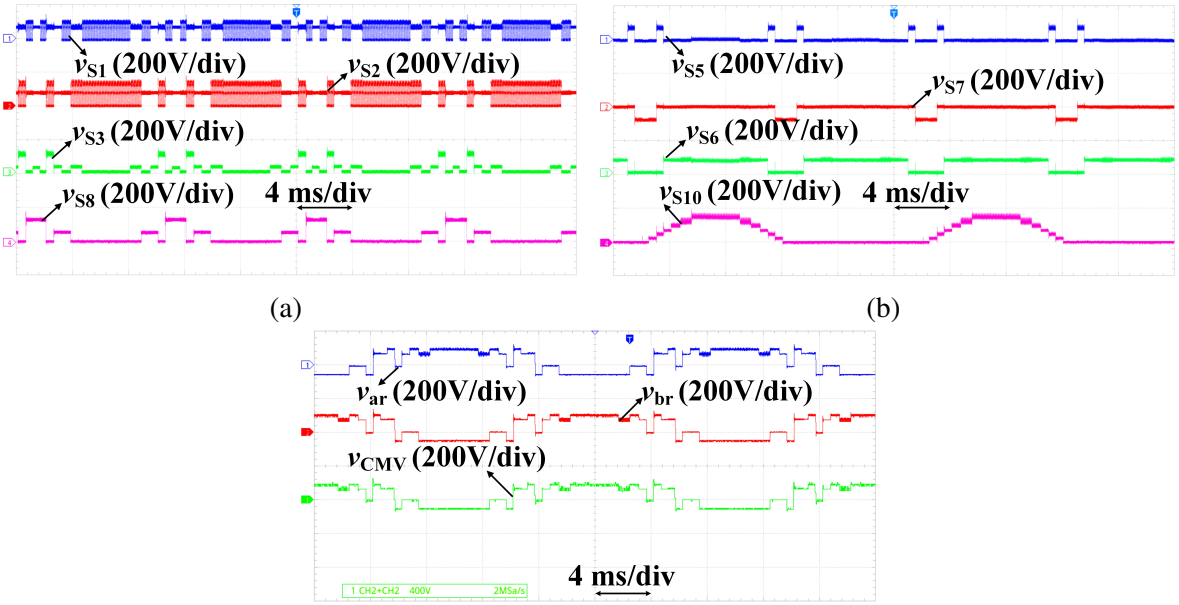


Figure 5.10: SBMLI's voltage waveforms of: (a) S_1, S_2, S_3 and S_8 (b) S_5, S_6, S_7 and S_{10} (c) v_{ar}, v_{br} and CMV.

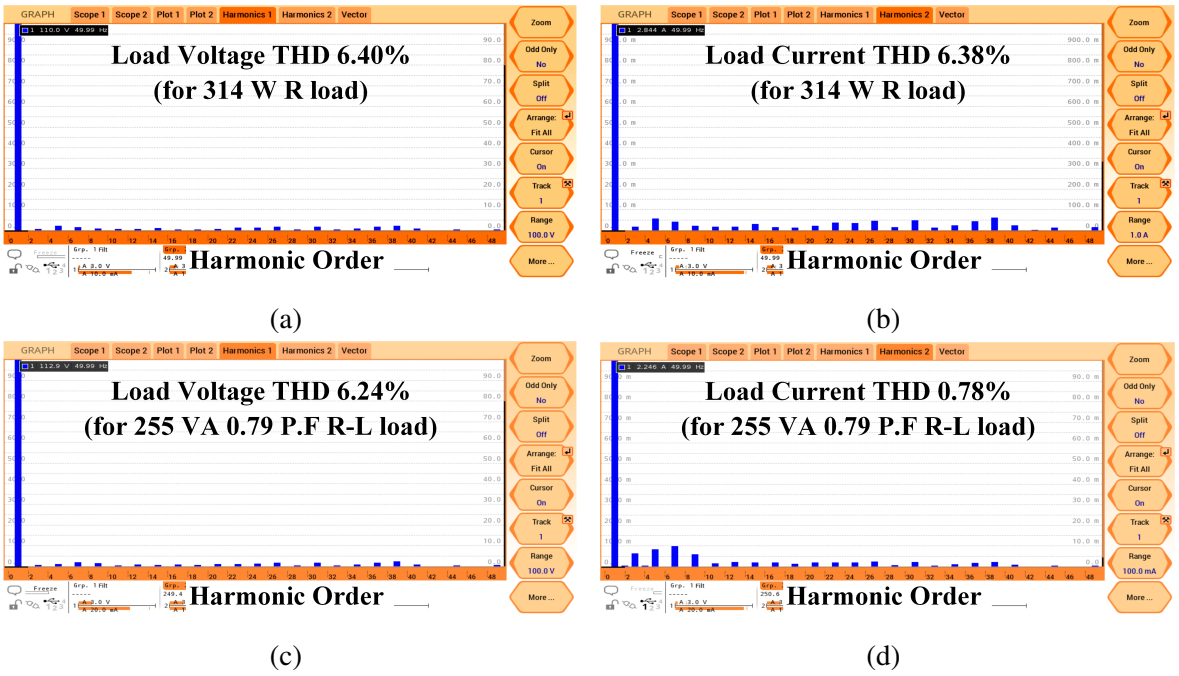


Figure 5.11: THD of v_o and i_o for (a) & (b) 314 W R load (c) & (d) 255 VA, 0.79 power factor R-L load

digital controller produces the control signals necessary for the SBMLI.

Its dynamic behaviour is tested and the corresponding experimental results of load voltage (v_o), load current (i_o) and capacitors voltages (v_{C1} and v_{C2}) are depicted in Figure 5.9.

Figure 5.9a, illustrates the sudden variation in R load (i.e., from 314 W R load to 212 W R load). Similarly, Figure 5.9b illustrates the step variation in load (i.e., from 314 W R load to 255 VA R-L load with 0.79 power factor). From the waveforms shown in Figures 5.9a and 5.9b, it can be noticed that the v_o, v_{C1} and v_{C2} are consistent for the dynamic load variation. The current and ripple voltage waveforms of capacitors C_1 and C_2 depicted in Figure 5.9c prove that the ripple voltages are less than 5%. The current waveform of source (i_1) and inductors (i_{L1} and i_{L2}) are depicted in Figure 5.9d.

The SBMLI's switch voltage waveforms are depicted in Figures 5.10a & 5.10b, which prove that except S_1 and S_2 remaining the switches operate at low frequency. The pole voltages (v_{ar} and v_{br}) and CMV illustrated in Figure 5.10c prove that the proposed inverter produce low frequency CMV.

The 13-level output voltage of SBMLI is directly fed to the load without output filter. The harmonic spectrum of load voltage and current for 314 W resistive load and 255VA, 0.79 P.F. inductive load are depicted in Figure 5.11. From the Figure, the measured voltage & current THD are 6.40% & 6.38% for the resistive load and 6.24% & 0.78% for the inductive load respectively.

5.5 Summary

A new single source 13-level step-up MLI with reduced components and compact capacitors is presented. It is constructed by the cascading connection of two BBCs (BBC) with the source to generate a 6-level output with a gain of two. An experimental 300 W proof-of-concept is developed and verified with R and R-L load under dynamic load conditions. For R and R-L load, the acquired load voltage THD are 6.40% and 6.24% respectively with no filter. A detailed comparison of the SBMLI and recent 13-level SCMLIs is offered, proving that the proposed inverter has a voltage gain of 2, while using reduced components and compact capacitors. Furthermore, it results in a low frequency CMV.

Chapter 6

Improved Single-source Buck-boost Integrated High gain 11-level Inverter

Chapter 6

Improved Single-source Buck-boost Integrated High gain 11-level Inverter

6.1 Introduction

The proposed SBMLI topology in chapter 5 produce a voltage gain of two. However, the desired voltage gain of inverter used for PV AC module applications should be more than three. Thus, in this chapter, an improved single-source buck-boost integrated multilevel inverter (ISBMLI) for 11-level operation is proposed. The ISBMLI consists of a 5-level basic unit formed by two interleaved BBCs, whose outputs are cascaded with the source to achieve a voltage gain of five. The capacitors present in the BBCs are charged at the high switching frequency, therefore the ISBMLI utilizes small capacitors compared to the existing SCMLI topologies. Moreover, capacitors presented in the conventional SCMLI are limited to fixed voltage charging, whereas the capacitors of the ISBMLI can be charged to desired voltages by adjusting respective BBC duty cycles. Hence, the ISBMLI requires a relatively less number of compact capacitors to produce the higher number of voltage levels. In this chapter, the design and operation of the ISBMLI for 11-level operation is presented. A 500W proof-of-concept is developed and the experimental results are presented for linear and non-linear loads under static and dynamic load conditions. Additionally, a comprehensive comparative study of the ISBMLI and the recent SCMLI is presented.

6.2 Working and operating principle of the proposed ISBMLI

The ISBMLI is depicted in the Figure 6.1. It consists of a basic unit and H-bridge inverter. Further, the basic unit contains a buck-boost network and a level selector network. The buck-boost network employs two BBCs which are energized from the input voltage source. The output voltages of BBCs (i.e capacitor C_1 and C_2 voltages) are connected in series with the source to provide voltage gain and two more voltage levels. Each BBC comprises of a

switch, diode, inductor and capacitor. The capacitor C_1 and C_2 voltages v_{C1} and v_{C2} are n_1 and n_2 times of the source voltage V_{dc} respectively. Voltage step-up ratios n_1 and n_2 of the BBCs either 1 and 3 or 3 and 1 to produce maximum number of five levels using a basic unit. The level selector network is formed by the switches S_{C1}, S_{C1P}, S_{C2}, S_{C2P}, S_{V1}, S_{V2}, S_{V3} to select the required combination of voltages of buck-boost network. Table 6.1 describes the corresponding switching states of level selector network and BBCs state of operation for different output voltage levels of basic unit.

The proposed basic units can be cascaded to generate more number of levels and the H-bridge inverter unfolds the waveform. With one basic unit, the ISBMLI produces a 11-level output voltage waveform. The voltage step-up ratios of BBC-1 and BBC-2 are considered as $n_1 = 1$ and $n_2 = 3$, that means $V_{c1} = V_{dc}$ and $V_{c2} = 3V_{dc}$. The duty cycles δ_1 and δ_2 of BBCs are expressed as

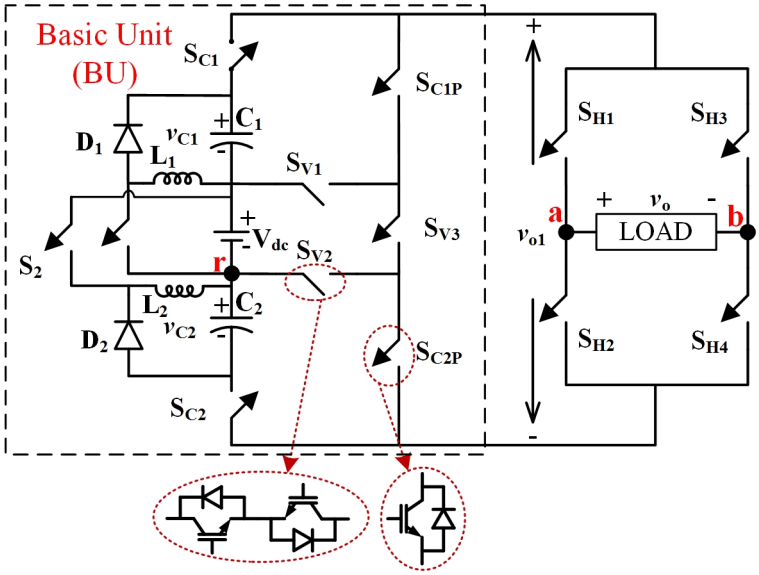


Figure 6.1: Equivalent circuit of the ISBMLI for the peak output voltage level

$$\delta_1 = \frac{n_1}{1+n_1} \tag{6.1}$$

$$\delta_2 = \frac{n_2}{1+n_2} \tag{6.2}$$

Operation of a BBC depends upon the output level as specified in the Table 6.1. The nearest level controller as shown in Figure 6.2 is utilized to realize switching levels of the

Table 6.1: Switching States of basic unit of ISBMLI

On State Devices	**Boost Converter**		v_{0X}
	BBC-1	**BBC-2**	
S_{C1P}, S_{V3}, S_{C2P}	OFF	OFF	0
$S_{C1P}, S_{V1}, S_{V2}, S_{C2P}$			V_1
$S_{C1}, S_{V1}, S_{V3}, S_{C2P}$	ON	OFF	$v_{C1} = V_1$
S_{C1}, S_{V2}, S_{C2P}	ON	OFF	$V_1 + v_{C1} = 2V_1$
$S_{C1P}, S_{V3}, S_{V2}, S_{C2}$	OFF	ON	$v_{C2} = 3V_1$
S_{C1P}, S_{V1}, S_{C2}	OFF	ON	$V_1 + v_{C2} = 4V_1$
S_{C1}, S_{C2}	ON	ON	$V_1 + v_{C1} + v_{C2} = 5V_1$

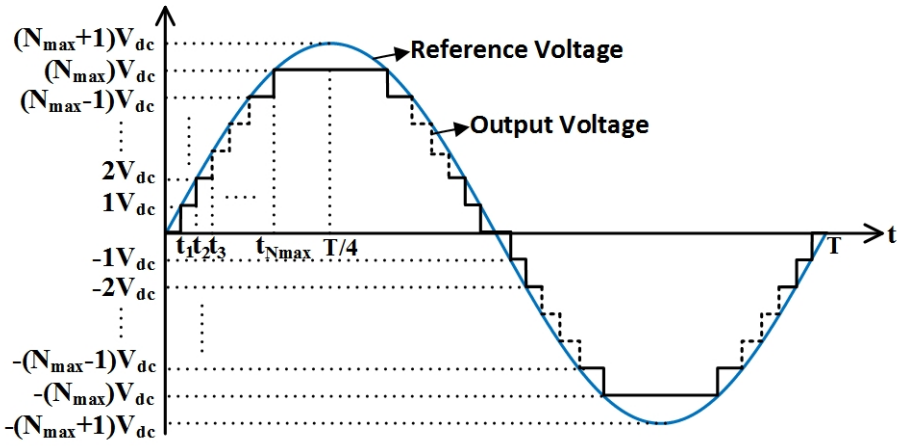


Figure 6.2: Model waveform of ISBMLIs with nearest level control

ISBMLI. Equivalent circuits of the basic unit for different levels of operation are presented in FIGURE. 6.3, whereas the BBCs are represented by their output voltages.

The highest level of the ISBMLI is considered for the design of inductor and capacitors of the BBCs. The equivalent circuit is illustrated in Figure 6.4 with a resistive load R_o. The respective peak load current $I_{o,max}$ can be expressed as

$$I_{o,max} = \frac{V_{dc} + V_{c1} + V_{c2}}{R_o} = \frac{V_{o,max}}{R_o} \tag{6.3}$$

where $V_{o,max}$ is peak of the load voltage, which is the sum of the voltages V_{dc}, V_{C1} and V_{C2} .

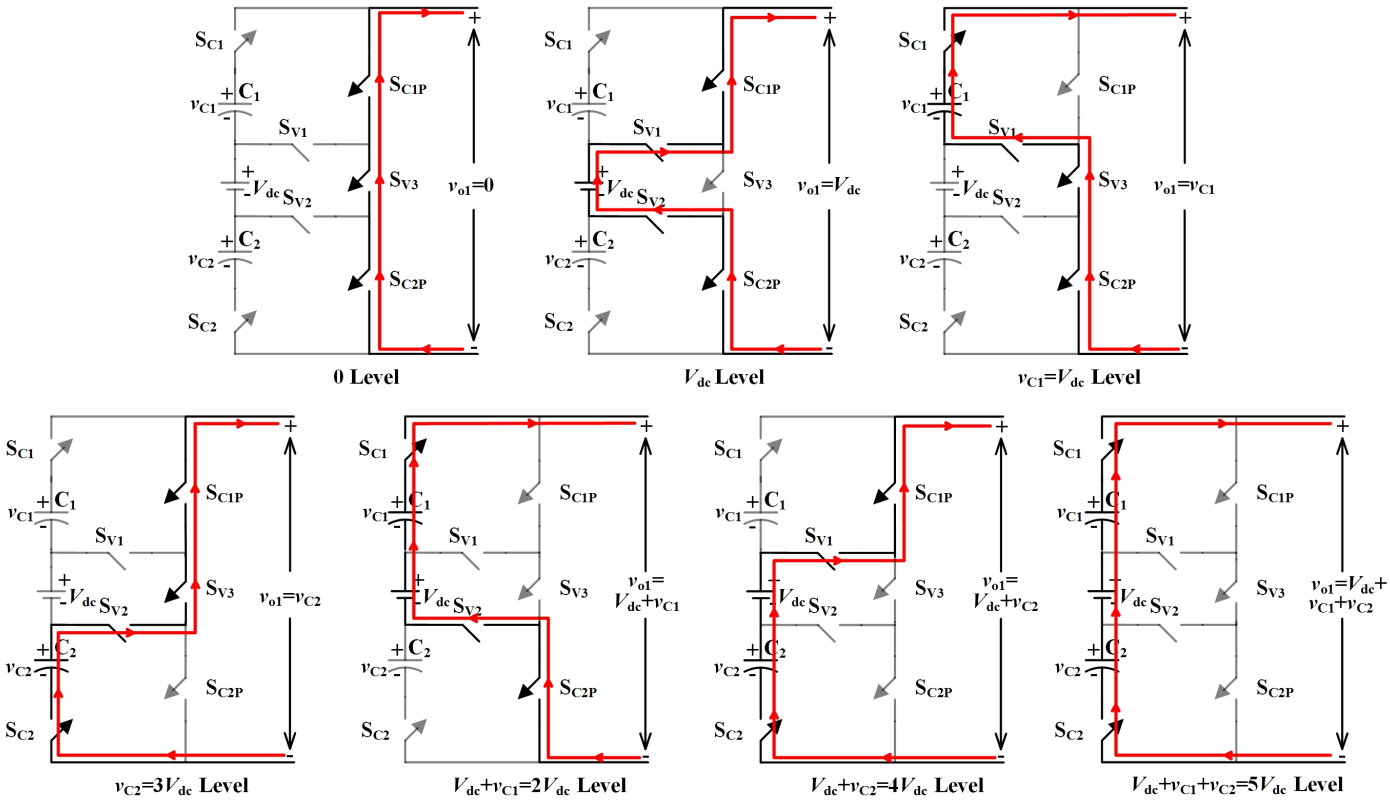


Figure 6.3: Equivalent circuits of ISBMLI basic unit from 0 V_{dc} to 5V_{dc} levels.

The powers P_{c1} and P_{c2} handled by the capacitors of the BBCs are given as follows

$$P_{c1} = V_{c1} I_{o,max} \tag{6.4}$$

$$P_{c2} = V_{c2} I_{o,max} \tag{6.5}$$

Equivalent resistance seen by each BBC is

$$R_{c1} = \frac{V_{c1}^2}{P_{c1}} = \frac{V_{c1} R_o}{V_{o,max}} \tag{6.6}$$

$$R_{c2} = \frac{V_{c2}^2}{P_{c2}} = \frac{V_{c2} R_o}{V_{o,max}} \tag{6.7}$$

By assuming the boundary conduction mode, the critical inductances L_{B1} and L_{B2} of respective L_1 and L_2 are obtained by equating the energy stored in the respective inductor during ON

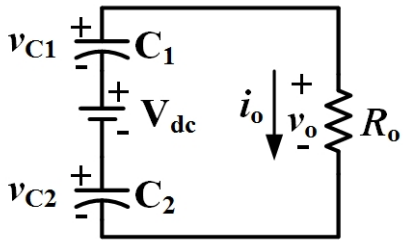
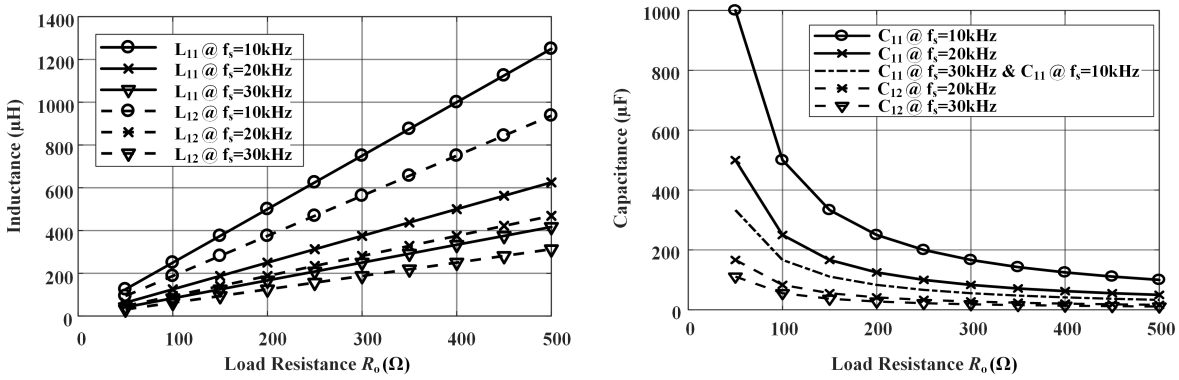


Figure 6.4: Equivalent circuit of the ISBMLI for the peak output voltage level



(a) (b)

Figure 6.5: Design characteristics of (a) critical inductances L_{B1} and L_{B2} (b) minimum capacitances $C_{1,min}$ and $C_{2,min}$ for 5% ripple voltage with respect load current at different switching frequencies

period and equivalent energy transferred by the BBC, which are expressed as

$$L_{B1} = \frac{\delta_1^2 R_o}{2n_1(1+n_1+n_2)f_s} \tag{6.8}$$

$$L_{B2} = \frac{\delta_2^2 R_o}{2n_2(1+n_1+n_2)f_s} \tag{6.9}$$

where f_s=switching frequency of buck boost converters

The minimum capacitance values $C_{1,min}$ and $C_{2,min}$ of C_1 and C_2 required to maintain respective percentage capacitor voltage ripples x_1 and x_2 of BBC-1 and 2 are given by

$$C_{1,min} = \frac{(1+n_1+n_2)\delta_1 * 100}{x_1 n_1 R_o f_s} \tag{6.10}$$

$$C_{2,min} = \frac{(1+n_1+n_2)\delta_2 * 100}{x_2 n_2 R_o f_s} \tag{6.11}$$

With the help of (6.8) and (6.9), the critical inductances L_{B1} and L_{B2} required for different load resistance at different switching frequencies can be obtained as illustrated in Figure 6.5a. Similarly, (6.10) and (6.11) are utilized for calculation of minimum capacitances $C_{1,min}$ and $C_{2,min}$ required to maintain capacitor voltage ripples less than 5% as depicted in Figure 6.5b.

To maintain desired capacitor voltages of BBCs with dynamic load conditions, two voltage control loops with PI controller are employed for each converter as shown in the Figure 6.6. In the figure, *car*1 and *car*2 are the carrier signals with frequency of f_s, which are used for the PWM generation of BBC-1 and BBC-2 respectively. The generated pulses from the two control loops are fed to BBC switches S_1 and S_2 respectively. These pulses are realized by the interleaved pulse width modulation to reduce input ripple current.

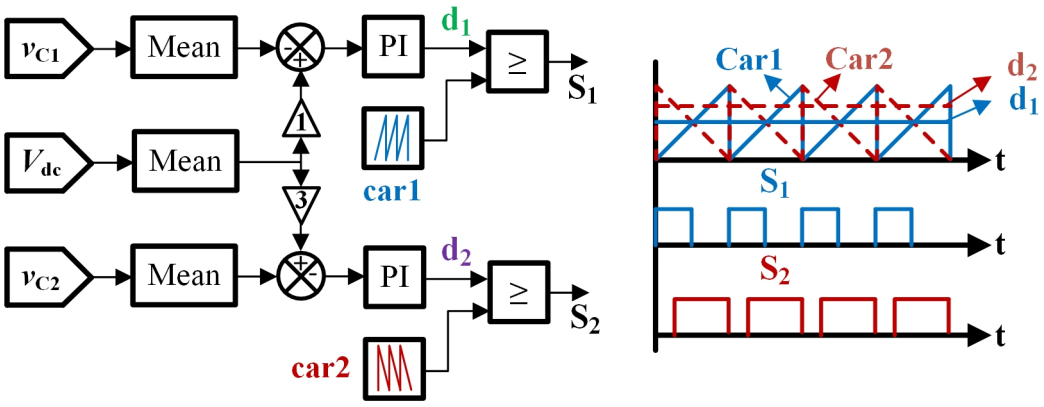


Figure 6.6: Block diagram of closed loop control and pulse generation of BBCs

In the ISBMLI, considerable amount of power is processed by the BBCs and the remaining is delivered from the voltage source. The maximum power handling ratio of each BBC is obtained from the peak power instant of the inverter. The peak output power $P_{o,max}$ and

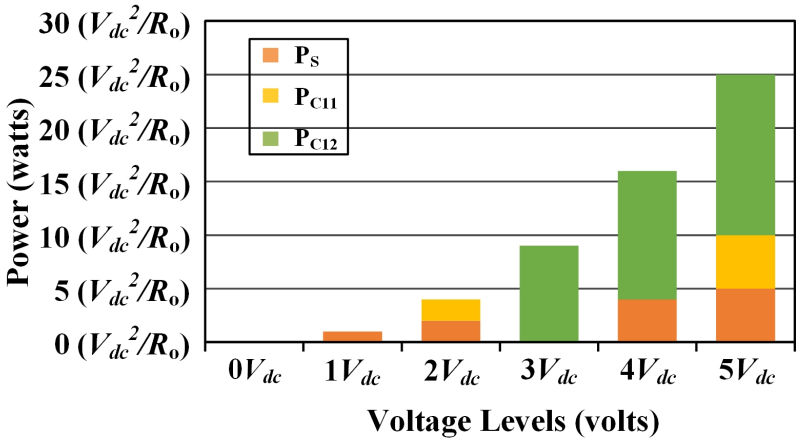


Figure 6.7: Power processed by DC source and BBCs at different operating voltage levels

respective source power $P_{S,max}$ can be expressed as

$$P_{o,max} = V_{o,max} I_{o,max} \tag{6.12}$$

$$P_{S,max} = V_{dc} I_{o,max} \tag{6.13}$$

By using (6.4), (6.5), (6.12) and (6.13) the percentage of peak power processed by each BBC ($\%P_{c1}$ & $\%P_{c2}$) and source ($\%P_{S,max}$) are calculated as follows

$$\%P_{c1} = \frac{V_{c1} I_{o,max}}{V_{o,max} I_{o,max}} X100 = 20\% \tag{6.14}$$

$$\%P_{c2} = \frac{V_{c2} I_{o,max}}{V_{o,max} I_{o,max}} X100 = 60\% \tag{6.15}$$

$$\%P_{S,max} = \frac{V_{dc} I_{o,max}}{V_{o,max} I_{o,max}} X100 = 20\% \tag{6.16}$$

From the above equations, it is confirmed that the both BBCs together are rated for 80% out of total rated power. The instantaneous powers of source (P_S) and BBCs (P_{c1} & P_{c2}) processed at different voltage levels are shown in Figure 6.7.

Assume T is the total time period of voltage waveform; E_{Total} is the total energy delivered to the load during the $T/4$ period; E_S, E_{C1} and E_{C2} are the energies processed by source and BBCs respectively in $T/4$ duration. The energies E_{Total}, E_S, E_{c1} and E_{c2} can be obtained as

follows

$$E_{Total} = \sum_{i=0}^{5} (t_{i+1} - t_i) * (i * V_{dc})^2 / R_o \tag{6.17}$$

$$E_S = \sum_{i=1,2,4,5} (t_{i+1} - t_i) * (i * V_{dc}^2) / R_o \tag{6.18}$$

$$E_{c1} = \sum_{i=2,5} (t_{i+1} - t_i) * (i * V_{dc}^2) / R_o \tag{6.19}$$

$$E_{c2} = \sum_{i=3}^{5} (t_{i+1} - t_i) * (3i * V_{dc}^2) / R_o \tag{6.20}$$

where 'i' is a positive integer from 0 to 5, t_i and t_{i+1} are the is starting and ending instants of the i^{th} level. By using (6.17), (6.18), (6.19) and (6.20), the utilization ratios of source, BBCs 1 and 2 are calculated as 20.873%, 15.3215% and 63.8055% respectively.

6.3 Comparative analysis

To verify the advantages of the ISBMLI in contrast with the recent 11-level SCMLI topologies, a comparative study is carried out and the data is presented in Tables 6.2 and 6.3. Various parameters like number of switches, diodes, sources, inductors, capacitors, capacitors' size, voltage gain, inrush current during capacitor charging and efficiency of the ISBMLI and

Table 6.2: Comparative study of the ISBMLI with the recent 11-level SCMLIs

Parameter	**[69]**	**[74]**	**[77]**	**[78]**	**[79]**	**[68]**	**[71]**	**Proposed**
N_{dc}	1	1	1	1	1	1	1	**1**
N_{swi}	12	24	13	13	12	12	20	**15**
N_{dio}	5	4	4	0	0	2	8	**2**
N_{cap}	5	4	4	4	4	4	8	**2**
Capacitor Size	Bulky	Bulky	Bulky	Bulky	Bulky	Bulky	Bulky	**Small**
N_{ind}	1	0	0	0	0	0	1	**2**
N_{dri}	12	24	13	13	12	12	20	**15**
Gain	1	5	5	5	2.5	5	5	**5**
Inrush Current	No	Yes	Yes	Yes	Yes	Yes	No	**No**
Efficiency (%)	93.5	88.9	—	—	93.0	92.1	96.0	**93.0**

Table 6.3: Comparative study of the ISBMLI and the recent SCMLIs in generalized operation

Parameter	**[74]**	**[77]**	**[68]**	**[69]**	**[71]**	**Proposed**
N_{lev}	2x+1	2x+3	10x+1	2x+1	2x+3	10x+1
N_{dc}	1	1	n	1	1	x
N_{swi}	5x-1	2x+5	12x	2x+2	4x+4	15n
N_{dio}	0	x	2x	x	2x	2x
N_{cap}	x-1	x	4x	x	2x	2x
Capacitor Size	Bulky	Bulky	Bulky	Bulky	Bulky	Small
N_{ind}	0	0	0	1	1	2n
N_{dri}	5x-1	2x+5	12x	2x+2	4x+4	13n
Inrush Current	Yes	Yes	Yes	No	No	No
Gain	x+1	x+1	5	1	x+1	5

Note: x= No. of cascaded units

the SCMLIs for 11-level operation are compared. The ISBMLI requires less number of small capacitors vis-á-vis MLIs [68, 69, 71, 74, 77–79], hence improves the reliability of the inverter. Although the SCMLIs [69, 79] require less number of switches, they provide the voltage gains of 2.5 and 1 respectively, whereas the ISBMLI provides a voltage gain of 5. However, SCMLI [77] utilize less number of switches and provides voltage gain of 5, it requires higher number of diodes and bulk capacitors. The SCMLIs [69, 74] require higher number of devices and bulk capacitors as compared to the ISBMLI. During the charging period of the capacitors, the SCMLIs [68, 74, 77–79] draw impulsive current, hence require high current rated switches. Whereas, ISBMLI the inductors L_1 and L_2 limit the capacitor charging current. Except the ISBMLI, all other SCMLIs presented in Table 6.2 use parallel charge and series discharge of capacitors, thus suffer from capacitor voltage droop problem at high power ratings. Whereas, the capacitor voltages of the ISBMLI are controlled by the closed-loop controllers, hence free from voltage drooping issues.

6.4 Experimental Results

To verify the desired function of the ISBMLI, a 500 W proof-of-concept is developed as shown in Figure 6.8 for the specifications mentioned in the Table 3.9. TMS320F28379D digital signal processor is used to generate the gate pulses required for the ISBMLI.

Table 6.4: Specifications and Design Parameters of ISBMLI for 11-level operation

Parameter	Value / Part Number
Input voltage (V_1)	60 V
Output voltage (V_o, RMS)	220 V
BBC's capacitors voltages (v_{C1}, v_{C2})	60 V, 180 V
Output frequency (f_o)	50 Hz
Switching frequency (f_s)	20 kHz
Peak output Power (P_o)	500 W
BBC's inductors (L_1,L_2)	156 μH, 117 μH
BBC's capacitors (C_1, C_2)	300 μF/400 V, 200 μF/400 V
Switches	IKW40T120
Diodes	STPSC2006CW
R load	95 Ω for 510 W load
	180 Ω for 260 W load
R-L load	95 Ω & 200 mH for 339 VA, 0.8 P.F load
	180 Ω & 200 mH for 228 VA, 0.94 P.F load
Non-linear load (with rectifier and R-L load)	95 Ω & 400 mH for 405 W load
	180 Ω & 400 mH for 213 W load

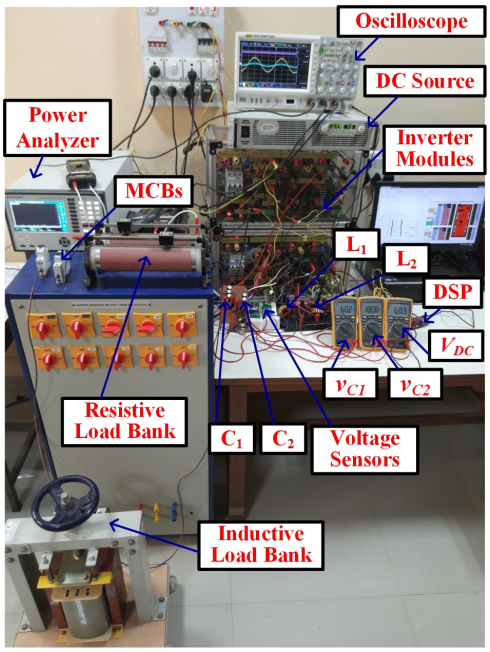


Figure 6.8: Experimental setup of the ISBMLI

The ISBMLI dynamic performance is examined with linear loads and the respective experimental waveforms of load voltage (v_o), load current (i_o) and capacitors voltages (v_{C1} and

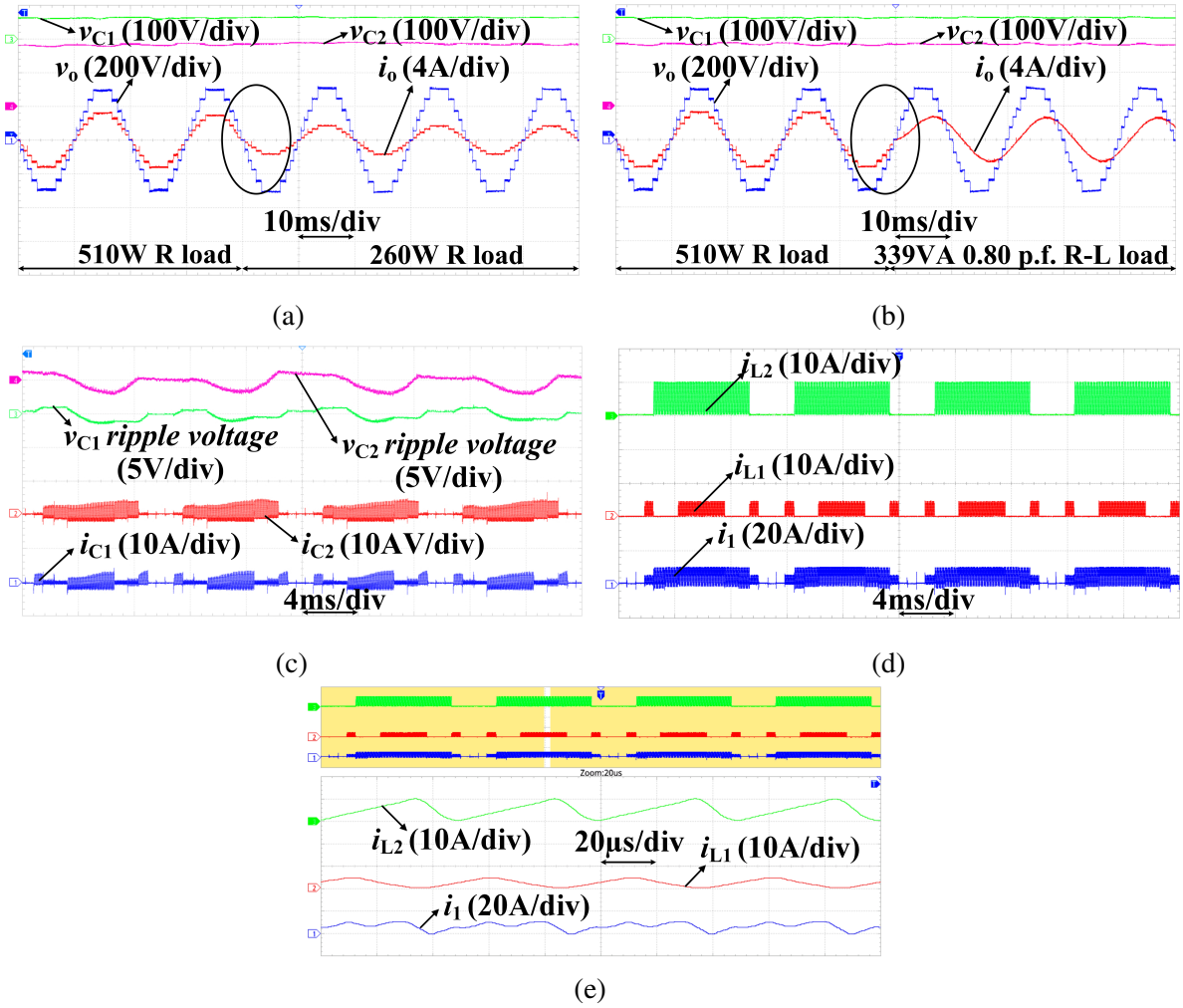


Figure 6.9: Experimental waveforms of the ISBMLI: (a) load voltage (v_o), load current (i_o) and capacitor voltages (v_{C1} and v_{C2}) during step change in R load for (i.e., 510 W R load to 260 W R load) (b) v_o, i_o, v_{C1} and v_{C2} during step change in load type (i.e., 510 W R load to 339 VA, 0.8 power factor R-L load) (c) capacitors C_1 & C_2 currents and ripple voltages (d) source current i_1, inductor currents i_{L1} and i_{L2} (e) zoomed version of source current i_1, inductor currents i_{L1} and i_{L2}.

v_{C2}) are presented in Figure 6.9. The corresponding waveforms for the step change in R load (i.e., from 510 W R load to 260 W R load) and load type (i.e., from 510 W R load to 339 VA R-L load with 0.8 power factor) are shown in Figures 6.9a and 6.9b respectively. In both cases, it can be observed that the capacitor voltages (v_{C1} and v_{C2}) and load voltage (v_o) are unaltered and ensures the firm dynamic operation of the ISBMLI. The current and ripple voltage waveforms of capacitors C_1 and C_2 depicted in Figure 6.9c confirms that the ripple voltages are below 5%. Input current (i_1) and inductor currents (i_{L1} and i_{L2}) are depicted in Figure 6.9d. Also, the ISBMLI dynamic response during step change in R-L load is verified and the respective

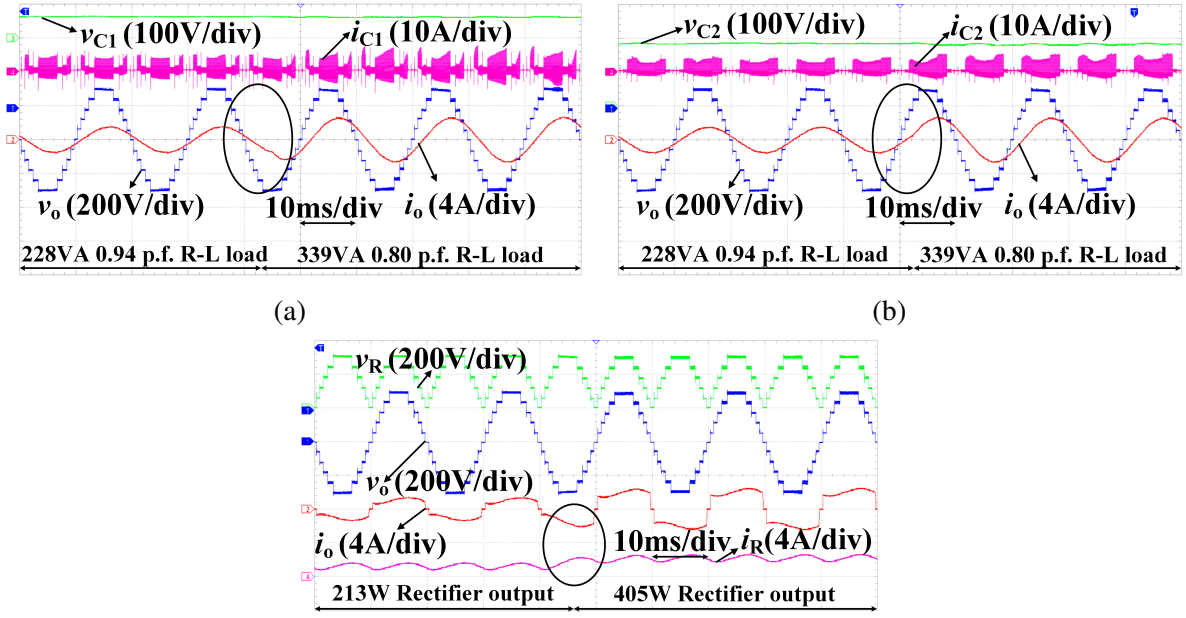


Figure 6.10: Experimental waveforms of the ISBMLI: (a) v_o, i_o, v_{C1} and i_{C1} during step change in RL load (i.e., 228 VA, 0.94 power factor RL load to 339 VA, 0.8 power factor R-L load) (b) v_o, i_o, v_{C2} and i_{C2} during step change in RL load (i.e., 228 VA, 0.94 power factor RL load to 339 VA, 0.8 power factor R-L load) (c) v_o, i_o, rectifier output voltage and output currents v_R and i_R during step change in non-linear load (i.e., 213 W to 405 W)

Table 6.5: Power loss distribution of ISBMLI at different power ratings

Cond_INV (W)	0.90	1.81	2.82	3.77	4.58	5.72	6.70	7.68	11.77	12.81
Swi_INV (W)	0.08	0.08	0.08	0.09	0.09	0.10	0.10	0.10	0.13	0.13
Cond_BBC (W)	1.04	2.18	3.37	4.63	5.58	7.04	8.35	9.74	13.11	16.79
Swi_BBC (W)	3.12	3.97	4.68	5.34	5.81	6.48	7.04	7.61	9.77	10.28
Cond_L&C (W)	0.27	0.74	1.35	2.08	2.69	3.41	4.62	8.96	9.11	11.51
Toatl losses (W)	**5.41**	**8.77**	**12.30**	**15.90**	**18.76**	**22.75**	**26.81**	**34.10**	**43.88**	**51.53**
Output Power (W)	**50**	**100**	**150**	**200**	**250**	**300**	**350**	**400**	**450**	**500**
Efficiency (%)	**90.23**	**91.93**	**92.42**	**92.63**	**93.02**	**92.95**	**92.89**	**92.15**	**91.11**	**90.66**

experimental waveforms of load voltage (v_o), load current (i_o), capacitors voltages (v_{C1} and v_{C2}) and capacitors currents (i_{C1} and i_{C2}) are presented in Figures 6.10a and 6.10b respectively.

To verify the operation of the ISBMLI with non-linear load, a rectifier with R-L load is considered and the load parameters are specified in Table 6.4. The corresponding load voltage (v_o), load current (i_o), rectifier output voltage (v_R), rectifier output current (i_R) waveforms for

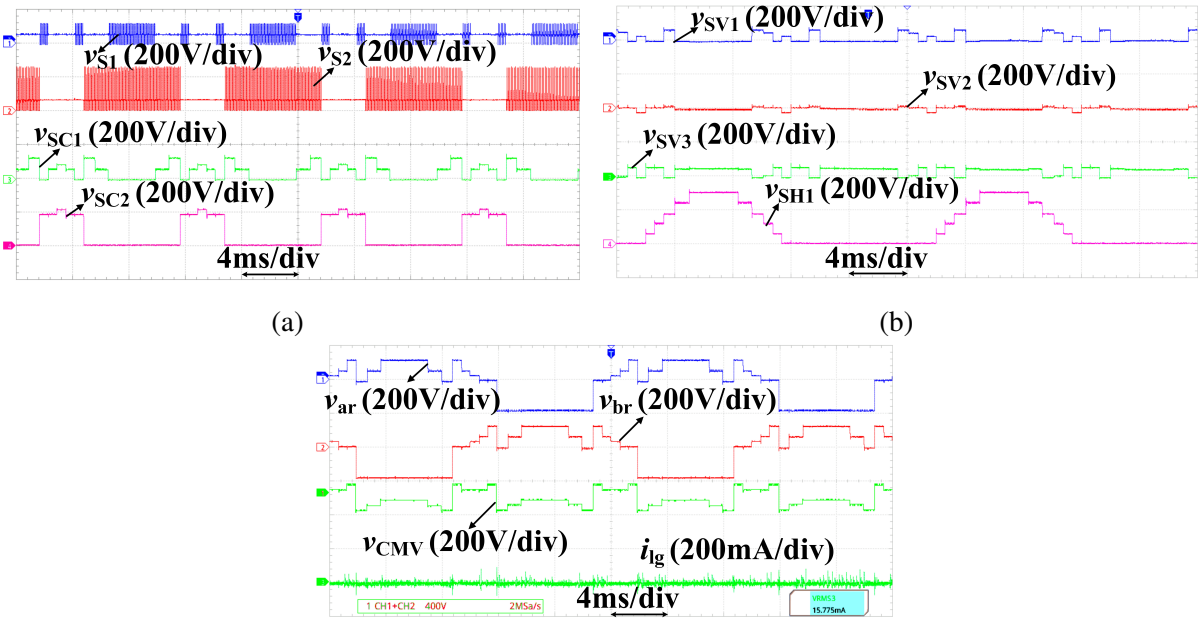


Figure 6.11: Experimental waveforms of the ISBMLI: (a) voltages of switches S_1, S_2, S_{C1} and S_{C2} (b) voltages of switches S_{V1}, S_{V2}, S_{V3} and S_{H1} (c) pole voltages v_{ar}, v_{br}, CMV and leakage current i_{lg}.

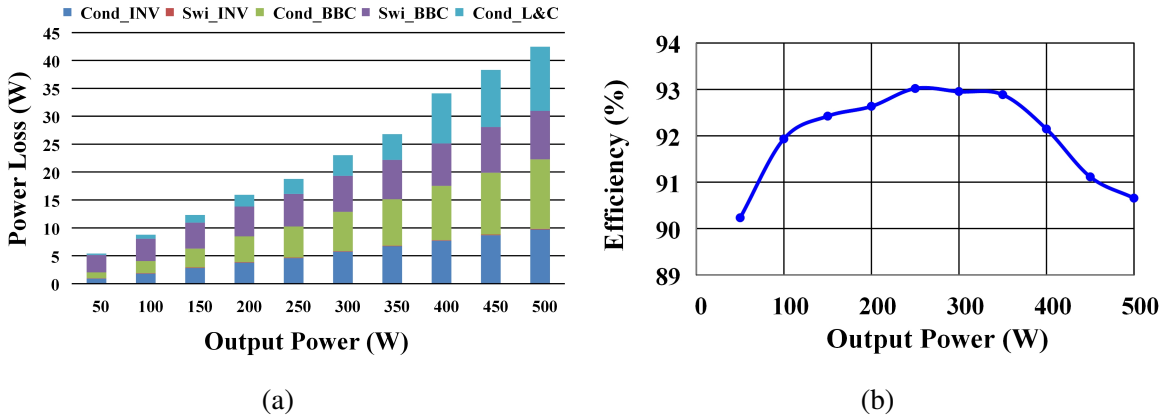


Figure 6.12: ISBMLI: (a) Power loss distribution and (b) efficiency characteristics for 11-level operation at different output power conditions.

the step change in non-linear load (i.e., from 230 W to 405 W) are shown in Figures 6.10c.

The blocking voltage waveforms of the ISBMLI switches are depicted in Figures 6.11a & 6.11b. From these waveforms, it can be noticed that all the waveforms are of low frequency except for switches S_1 and S_2. Further, the pole voltages (v_{ar} and v_{br}), CMV and leakage current (i_{lg}) are presented in Figure 6.11c. As the switching frequency of the H-bridge and DC-link voltage are low, thus produces low frequency CMV, which results in low leakage current.

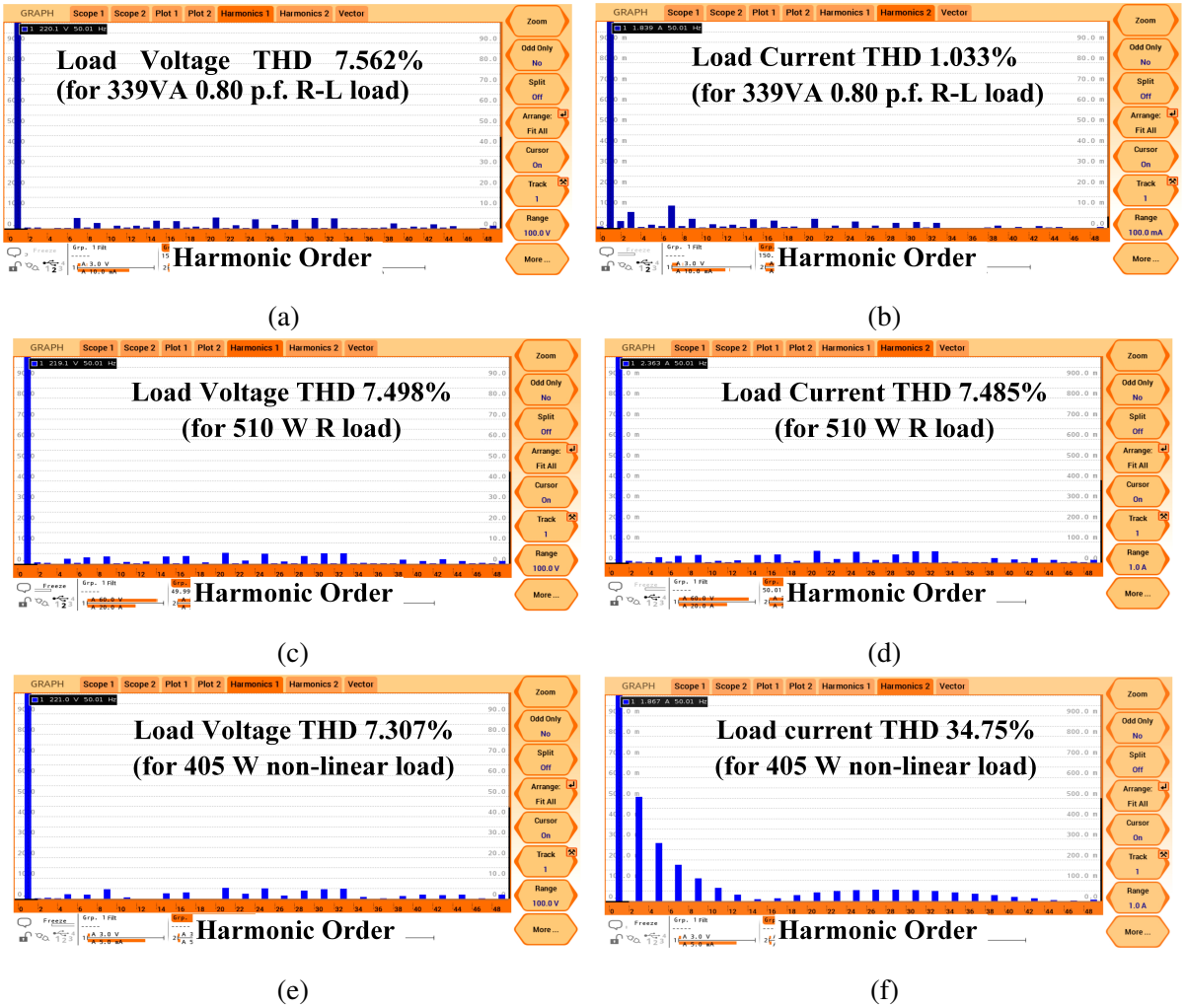


Figure 6.13: Experimental waveforms of the ISBMLI: (a) & (b) harmonic spectrum of v_o and i_o for 339 VA, 0.8 power factor R-L load respectively (c) & (d) harmonic spectrum of v_o and i_o for 510W R load respectively (e) & (f) harmonic spectrum of v_o and i_o for 405 W non-linear load respectively

From Figure 6.11c, the measured RMS value of the leakage current is 15.775 mA, which is significantly less than the VDE 0126-1-1 standard limit of 30 mA.

Without filter, the measured THD of load voltage and load current for 510 W R load are 7.498% and 7.485%, for 339 VA, 0.8 p.f R-L load are 7.562% and 1.033% and for 405 W, non-linear load are 7.307% and 34.75% respectively. The voltage and current harmonics for 339 VA, 0.8 p.f R-L load are presented in Figures 6.13a & 6.13b. Thermal model of the ISBMLI is developed by using PLECS software to evaluate the power losses of the various sections presented in the ISBMLI. The calculated switching losses (Swi_Inv and Swi_BBC) and conduction losses (Con_Inv and Con_BBC) of inverter and buck-boost network of the ISBMLI

are presented in Table 6.5 and Figure 6.12a for different output power conditions. It can be observed that the buck-boost network constitutes majority losses than the other network of the ISBMLI. Further, the efficiency curves of the ISBMLI for the input voltage of 60V at different output powers are presented in Figure 6.12b.

6.5 Summary

An improved buck-boost integrated MLI with reduced components and capacitor size is presented. The design procedure and generalized operation of the ISBMLI is presented. A 500 W proof-of-concept of the ISBMLI for 11-level operation is developed. The detailed experimental results for dynamic R load, R-L load and non-linear load are demonstrated. The THD of output voltage without filter is obtained as 7.498% and 7.562% for R load and R-L load, respectively. A comprehensive comparative study of the ISBMLI and recent SCMLIs for 11-level operation is presented, which shows that the ISBMLI offers a voltage gain of 5 with reduced components and compact capacitors. Also, it provides low frequency CMV and low leakage current of 15.775 mA (RMS) which is significantly complied the VDE 0126-1-1 standard limit of 30 mA. Hence, it is a potential candidate for PV and EV applications with low input voltage.

Chapter 7

Conclusions and future scope of research

Chapter 7

Conclusions and future scope of research

7.1 Conclusions

In recent times, PV systems are being highly utilized to electrify remote areas such as, villages, forests and islands. The energy from the PV is highly intermittent, which will affect the reliability of the power supply. To address this issue, PV along with energy storage systems such as, batteries and fuel cells with hydrogen gas storage is being used. The PV, battery, and fuel cell operate at a low voltage DC, but the load requires a high voltage AC. To process the energy from the sources to the load, an inverter with step-up capability is essential. In the literature, there are various step-up inverter topologies with and without transformers. However, for low power applications, the percentage of transformer losses in transformer-based inverters is relatively high, which reduces the overall efficiency. Hence, the recent research is focused on transformerless step-up inverters. Nowadays, SC based step-up inverters are prevalent for low power applications due to their high voltage gain, high efficiency, low voltage THD and simple modular operation without using a transformer. SC step-up MLIs employ parallel charge and series discharge techniques, which make the capacitors charge to fixed voltages and result in increased component count to achieve a higher number of levels. For low frequency applications, they require bulky capacitors in order to limit the ripple voltage within the limit. Furthermore, the SCMLIs' draw impulsive currents during capacitor charging which demands high current rated devices. To limit the impulse charging current issue, quasi-resonant SCMLIs are presented, however other issues are scope for the further research. Hence, this thesis presents the buck-boost integrated step-up MLIs to for the stand alone applications which address the issues presented in existing SCMLI topologies. The thesis work is summarized as follows.

The importance of PV energy systems and the various step-up inverter topologies that are suitable for PV standalone applications are discussed in Chapter 1 .

A comprehensive literature review on transformerless inverters suitable for PV standalone applications is presented in Chapter2 to formulate the research objectives. An overview of the proposed step-up inverters towards thesis contributions is discussed as follows:

In chapter 3, a novel boost DC-link integrated MLI is proposed. BDIMLI provides various advantages such as, high boost-factor, reduced component count, capacitor size, relatively low cost and less THD. The design characteristics of inductors and capacitors are analyzed, which shows the significant reduction in capacitor size. In addition, the capacitor voltages are unchanged irrespective of load changing conditions for 9-level and 13-level operation. The benefits of proposed BDIMLI are evident with the comparative study in contrast to recent MLI topologies. Moreover, the dynamic behavior of BDIMLI under various load conditions is tested with no-load, resistive and inductive loads providing a smooth and stable operation.

Chapter 4 presents an improved boost integrated cascaded MLI with reduced components and improved voltage gain. A 500 W proof-of-concept of IBDIMLI is developed and tested for symmetrical 17-level operation with SPWM & NLC, and also an asymmetrical 31-level operation with NLC for R and R-L load under dynamic load conditions. Stable and smooth operation is achieved for dynamic load conditions, while maintaining the output voltage and capacitor voltages. With NLC modulation, without filter, the IBDIMLI achieved output voltage THD as 5.138% and 3.702% for 17-level and 31-level operations respectively. Using SPWM, the IBDIMLI achieved an output voltage THD of 7.606% for the 17-level operation without filter. Also, the THD of load current with R-L load is well below the 5% according to IEEE-1547 standards in both SPWM and NLC.

In Chapter 5, a new single source buck-boost integrated MLI with fewer components and compact capacitors is presented. SBMLI is constructed by the cascading connection of two BBCs with the source to generate a 6-level output with a gain of two. An experimental proof-of-concept is developed and verified with R and R-L load under dynamic load conditions. For R and R-L load, the acquired load voltage THD are 6.40% and 6.24% respectively with no filter. A detailed comparison of SBMLI and recent 13-level SCMLIs is offered, proving that the SBMLI has a voltage gain of 2 while using fewer components and compact capacitors. Furthermore, it generated a low frequency CMV resulting in less leakage current.

Chapter 6 presents an improved single-source buck-boost integrated MLI with high voltage gain, reduced components and capacitor size. The design procedure and generalized operation of ISBMLI is presented. A 500 W proof-of-concept of ISBMLI for 11-level operation is developed. The detailed experimental results for dynamic R load, R-L load and non-linear load are demonstrated. The THD of output voltage without filter is obtained as 7.498% and 7.562% for R load and R-L load, respectively. A comprehensive comparative study of ISBMLI and recent SCMLIs for 11-level operation is presented, which shows that the ISBMLI offers a voltage gain of 5 with reduced components and compact capacitors. Also, it provides low frequency CMV and low leakage current of 15.775 mA (RMS) which is significantly less than the VDE 0126-1-1 standard limit of 30 mA. Hence, it is a potential candidate for PV applications

7.2 Future scope of research work

The research work presented in this thesis can be further investigated on following issues:

- Selective harmonic elimination technique can be applied to the proposed MLIs to eliminate the lower order harmonic and to improve the output voltage THD.
- An improved MLI topology can be proposed with reduced switches, if the main inverter switches are used to control the BBCs.
- The total switch voltage of the proposed MLIs can be reduced by eliminating the output H bridge network.
- With the sensor-less operation, the overall cost of the proposed inverter can be further minimized.

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List of publications

International journal publications:

[1] Sambhani Madhu Babu, B.L. Narasimharaju, Akshay Kumar Rathore, "**A New Buck-boost Integrated Multilevel Inverter with Reduced Capacitors and Capacitor Size for Low-frequency AC Applications**," *Wiley, International Transactions on Electrical Energy Systems*, vol. 13, no. 12, e13176, 2020 https://doi.org/10.1002/2050-7038.13176.

[2] Sambhani Madhu Babu, and B. L. Narasimharaju, "**Single-phase boost DC-link integrated cascaded multilevel inverter for PV applications**," *IET Power Electronics* vol. 13, no. 10, pp. 2086-2095, 2020, https://doi.org 10.1049/iet-pel.2019.1460.

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[1] Sambhani Madhu Babu and B. L. Narasimharaju, " **A New Generalized Symmetrical/Asymmetrical Boost Integrated Multilevel Inverter with Reduced Components**," in *International Journal of Electronics*.

[2] Sambhani Madhu Babu and B. L. Narasimharaju, " **Design and Analysis of Single-source 13-level Step-up Inverter with Reduced Components and Capacitor Size**," in *IETE Journal of Research*.