Novel Transformerless Multilevel Inverter Topologies for Photovoltaic System with Voltage Boosting and Leakage Current Compliance

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by

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CERTIFICATE

This is to certify that the thesis entitled **"Novel Transformerless Multilevel Inverter Topologies for Photovoltaic System with Voltage Boosting and Leakage Current Compliance"**, which is being submitted by **Mr. Sumon Dhara** (Roll No. 717012), is a bonafide work submitted to National Institute of Technology, Warangal in partial fulfilment of the requirement for the award of the degree of **Doctor of Philosophy** in **Department of Electrical Engineering**. To the best of my knowledge, the work incorporated in this thesis has not been submitted elsewhere for the award of any degree.

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APPROVAL SHEET

This thesis entitled "**Novel Transformerless Multilevel Inverter Topologies for Photovoltaic Systems with Voltage Boosting and Leakage Current Compliance**" by **Sumon Dhara** is approved for the degree of Doctor of Philosophy

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DECLARATION

This is to certify that the work presented in the thesis entitled "**Novel Transformerless Multilevel Inverter Topologies for Photovoltaic Systems with Voltage Boosting and Leakage Current Compliance"** is a bonafide work done by me under the supervision of **Dr. V. T. Somasekhar**, Department of Electrical Engineering, National Institute of Technology Warangal, India and was not submitted elsewhere for the award of any degree.

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ABSTRACT

The present scenario of dwindling resources of fossil fuels and the pollution of the environment demands the harvesting of clean and green energy. To this end, governments, industries, policymakers, and research communities steadfastly endeavour to promote the use of renewable energy sources (RES), which encompass solar, wind, tidal energies, etc. Of these RES', solar energy reaps benefits such as abundance (practically infinite), low maintenance requirement, silent operation, etc. The PV source outputs electrical energy in the form of DC, which is of limited use unless it is converted into the AC form. In a solar PV-based power generating system, this task is accomplished by an inverter. In this context, transformerless PV inverter topologies are poised to become popular owing to their high-power density and high efficiency. Recent developments in inverter technology resulted in the Multilevel Inverters (MLI), which strive to produce an output that is closer to a sinusoid, compared to the conventional two-level voltage source inverters (VSI). The present trend in the design of MLIs is to employ as few power semiconductor switching devices as possible. This thesis presents transformerless PV inverter configurations for both string and microinverter applications. The thesis tries to address some major challenges, which include the reduction of leakage current, integrated voltage boosting, reactive power capability, multilevel operation with reduced switching devices, etc. This thesis addresses some of these challenges, integrated voltage boosting network-based multilevel inverters are introduced, which are capable of reducing the leakage current and injecting both active and reactive powers into the grid.

Firstly, a single-phase, seven-level, transformerless inverter is proposed, which employs a semi-double stage-based power conversion technique. The proposed configuration achieves voltage boosting using a non-isolated interleaved buck-boost converter, which is fused with the inverter configuration through two switched capacitors (SCs). The interleaved front-end boost stage is capable of achieving a voltage gain of three while resulting in a reduced peak current stress on the switching devices. With this topology, a considerable part (about 37%) of the load power is transferred directly from the PV source, while the other part is transferred through the SCs. The proposed topology, with the aid of a bidirectional switch at the output and its pulse-width modulation (PWM) technique, reduces the leakage current by eliminating high-frequency transitions in the voltage across the parasitic capacitance of

the PV panel. This advantage outweighs the disadvantage of high *dv/dt* impressed across the semiconductor switches due to its modulation technique.

The second contribution of this thesis is to conceptualize and design a single-phase, nine-level T-type hybrid boost inverter, which successfully overcomes the limitations of the modulation scheme that is employed in the previous work. Unlike the previously proposed topology, this converter doesn't require an additional decoupling network. As in the case of the previous work, the efficiency in the boosting stage of the proposed converter system is improved by transferring a significant portion of the PV energy directly from the PV source to the load (about 42%). Furthermore, this work introduces a modified zone-based PWM technique, which eliminates the requirement of an additional decoupling network to minimize the leakage current. Thus, the modulation technique eliminates the leakage current without compromising on the advantages of conventional multilevel inverters such as low *dv/dt*, and inductive power capability.

In the third contributory chapter of this thesis, a thirteen-level inverter configuration is proposed with the *same* number of power switching devices. A generalized mathematical analysis for this MLI is carried out to evaluate the effects of various switching states on the parasitic voltage and the common-mode voltage (CMV). This analysis paves the way for the formulation of two PWM schemes to meet the safety standards. The first PWM scheme, which applies to inverters with asymmetrical filters, eliminates switching transitions from the PV parasitic voltage only. The second PWM scheme, which applies to inverters with symmetrical filters, achieves this objective along with the reduction of the common-mode voltage. Unlike the existing decoupling topologies, the proposed inverter configuration, along with its modulation strategies, does not require any additional switching resources to reduce the leakage current.

Finally, an integrated three-phase transformerless inverter configuration is proposed to extend the dual-mode power transfer technique for three-phase systems. The proposed 3-Ph topology is capable of synthesizing a three-level (3L) voltage waveform at its output. With the aid of an interleaved dual-output buck-boost converter, the proposed configuration is capable of achieving a voltage boosting factor of 2. Besides that, the modulation technique eliminates all high-frequency transitions in the voltage across the parasitic capacitive branch for the effective suppression of the leakage current, which is of paramount interest in transformerless PV systems.

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Abbreviations

AC	Alternating Current
ANPC	Active Neutral Point Clamped
CCM	Continuous-current Conduction Mode
CF	Cost Function
CG	Common Ground
CHB	Cascaded H-Bridge
CMLC	Common-mode Leakage Current
CMV	Common-mode voltage
DSP	Digital Signal Processor
DC	Direct Current
DCM	Discontinuous-current Conduction Mode
EMI	Electromagnetic interference
ESR	Equivalent Series Resistance
FC	Flying Capacitor
FFT	Fast Fourier transform
FPGA	Field Programmable Gate Arrays
HB	Half Bridge
HERIC	Highly Efficient and Reliable Inverter Concept

IGBT	Insulated Gate Bipolar Transistor
IPUR	Instantaneous Power Utilization Ratio
LSPWM	Level Shifted Pulse Wish Modulation
LSU	Level Selection Unit
MATLAB	Matrix Laboratory
MLI	Multilevel Inverter
MOSFET	Metal–oxide semiconductor with field-effect transistor
MPPT	Maximum Power Point Tracking
MPP	Maximum Power Point
NPC	Neutral Point Clamped
PCC	Point of Common Coupling
PCU	Power Conditioning Unit
P&O	Perturb and Observe
PF	Power Factor
PGU	Phase Generation Unit
PI	Proportional Integral
PLECS	Piecewise Linear Electrical Circuit Simulation
PLL	Phase Locked Loop
PR	Proportional Resonant
PSPWM	Phase Shifted Pulse Width Modulation

PV	Photovoltaic
PWM	Pulse Width Modulation
RMS	Root Means Squares
SISO	Single Input, Single-Output
SOGI	Second Order Generalized Integrator
SPWM	Sinusoidal Pulse Width Modulation
SVPWM	Space Vector Pulse Width Modulation
SC	Switched Capacitor
SCMLI	Switched Capacitor based Multilevel inverter
TCMV	Total Common-mode Voltage
TSV	Total Standing Voltage
THD	Total Harmonic Distortion
UPF	Unity Power Factor
VBU	Voltage Boosting Unit
VSI	Voltage Source Inverter

List of Symbols

i_{leak}	Leakage current
v_{Pg}	Total Common-mode voltage
v_{CMV}	Common-mode voltage
v_g	Grid voltage
i_g	Grid current
v_{xy}	Inverter output voltage
i_{xy}	Inverter output current
L_f	Inverter side Inductor of LCL filter configuration
C_f	Capacitor of LCL filter configuration
L_g	Grid-side Inductor of LCL filter configuration
Z_{CM}	Common-mode Impedance
L_{b1}, L_{b2}	Energy Storage Inductors front-end voltage boosting stage.
S_1, S_2 …. S_n	Switching devices of the inverter.
g	Ground Node
R_P	Equivalent parasitic resistance of the parasitic path between PV panel and ground.
C_P	Equivalent parasitic capacitance of the parasitic path between PV panel and ground.
R_g	Ground impedance.

V_{PV}	PV source voltage
I_{PV}	PV source current
I_m	Peak value of load current.
f_{swi}	Switching frequency of inverter switches.
f_{swb}	Switching frequency of the front-end stage.
$V_{DC\text{-}link}$	DC-link voltage of the inverter
f_m	Modulation frequency.
m_a	Modulation Index
f_{ZCM}	Resonance frequency of common mode impedance.
ω_{grid}	Angular frequency of the grid
D_{max}	Maximum duty cycle of front-end boosting stage.
P_o	Total output power
Δi_{PP}	Current ripple in filter inductor
ΔV_{CX}	Voltage ripple across the capacitor
f_{LCL}	Resonant frequency of the LCL filter
k_{pc}	Proportional gain of PR current controller
k_{rc}	Resonant gain of PR current controller
ω_n	Bandwidth of PR controller
ω_b	Resonant frequency of PR controller
k_{pv}	Proportional gain of PI controller in front-end stage

k_{iv}	Integral gain of PI controller in front-end stage
E_S	Energy transferred from PV source to the load in a fundamental cycle
E_{CX}	Energy transferred from switched capacitors to the load in a fundamental cycle
E_T	Total energy transferred to the load in a fundamental cycle
E_{Sf}	Energy utilization factor for single-stage operation
D_{max}	Maximum duty cycle of front-end boosting stag.e.
P_o	Total output power.
P_{rated}	Rated power of the inverter.
Δi_{PP}	Current ripple in filter inductor.
ΔV_{CX}	Voltage ripple across the capacitor.
f_{LCL}	Resonant frequency of the LCL filter.
k_{pc}	Proportional gain of PR current controller.
k_{rc}	Resonant gain of PR current controller .
ω_n	Bandwidth of PR controller.
ω_b	Resonant frequency of PR controller.
k_{pv}	Proportional gain of PI controller in front-end stage.
k_{iv}	Integral gain of PI controller in front-end stage.
E_S	Energy transferred from the PV source to the load in a fundamental cycle.

E_{CX}	Energy transferred from the corresponding switched capacitor to the load in a fundamental cycle.
E_T	Total energy transferred to the load in a fundamental cycle.
E_{Sf}	Energy utilization factor for single-stage operation.
E_{CXf}	Energy utilization factor for the corresponding switched capacitor.

Chapter 1

Introduction

Chapter 1

Introduction

1.1 General Overview

The ever-increasing world population and increased standards of living have resulted in heavy stress on energy resources, especially electrical energy. Electrical energy, generated with coal and other fossil fuels has taken a heavy toll on the environment and ecosystems. This crisis motivates the promotion of renewable energy resources on a large scale and has resulted in the paradigm shift in the generation of electrical energy.

Of several sources of renewable energy, solar and wind energies have emerged as the frontrunners in the past couple of decades. In particular, power generation with solar photovoltaic (PV) panels offers several advantages such as reliability of source and abundance of sunlight. Further, solar PV generation does not create any pollution in terms of air, water, and sound.

Another, attractive feature related to the solar power generation system is that it requires nearly zero maintenance due to the absence of moving parts. Also, PV panels have a long life of nearly 20-25 years. Due to these obvious advantages, PV-based power generation gained tremendous popularity across the globe, resulting in several largescale installations with huge investments. Most developed and developing countries have steadfastly promoted solar PV energy systems through governmental support such as low taxation and extending subsidies. Figure 1.1 shows the year-wise annual statistics of the total installed capacity of the PV power generated in GW in various countries in recent years [1, 2].

The renewable energy market of India stands in the fourth position in the global scenario and is still expanding. As of 2020, India ranks fourth in wind energy, fifth in solar energy, and fourth in terms of installed capacity. Power generation with renewable sources

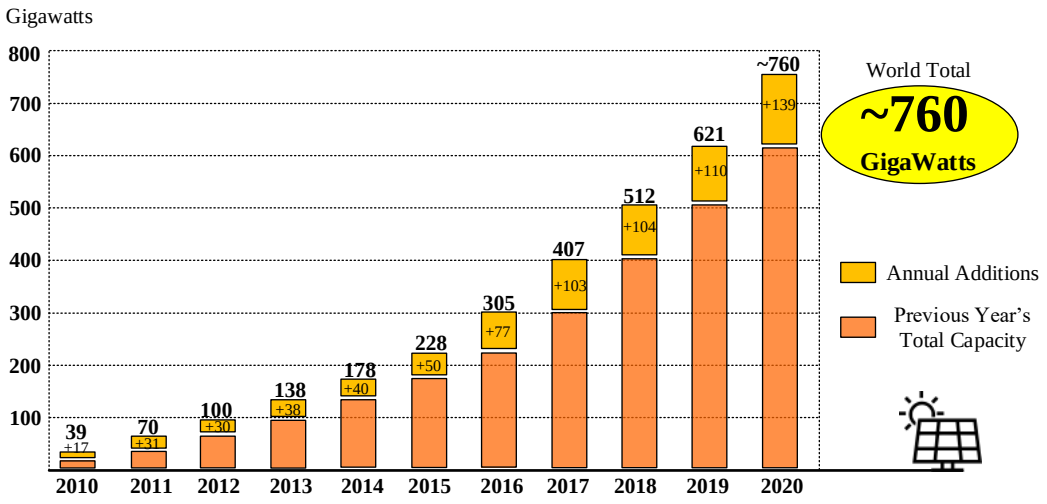


Figure 1.1: Solar PV Global capacity with yearly additions [1].

has shown a meteoric growth in recent years, with a compound annual growth rate (CAGR) of 17.33% from FY16 to FY20 [3].

Notwithstanding these positives, the growth of PV power generation is hindered due to the requirement of heavy capital investment. A significant portion of the initial investment is spent on PV panels and their erection. Further, the low conversion efficiency of the PV cells (sunlight to electricity) is a contributing factor to the high capital investment. This demands high efficiencies for the power conditioning units (PCU) in PV systems. Therefore, the design and selection of PV power conditioning units [4] are gaining the attention of researchers. To achieve high-efficiency PV inverters, several PV inverter configurations have been proposed by researchers in the recent past. The classification of these power converters has been carried out in the next section.

1.2 PV Panel Integration Schemes

Based on their power ratings [5], popular integrated grid-interactive PV systems are classified into three categories: (a) the centralized inverter system, (b) the string inverter system, and (c) the microinverter system.

1.2.1 Central Inverter

Centralized PV inverter schemes are used when the installed power capacity is in the range of 100–1000 kW. The PV modules are connected in series and parallel and are

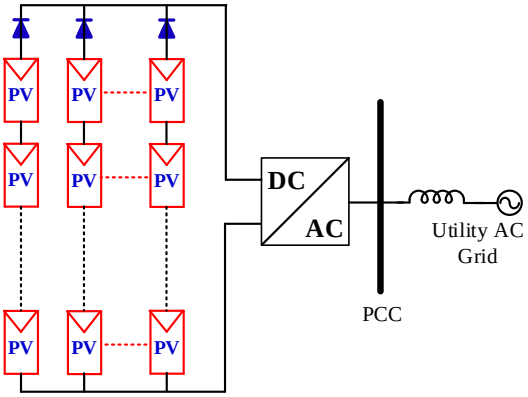


Figure 1.2: Configuration of Central Solar

connected to a single inverter as shown in Figure 1.2. The merits and demerits of the central inverter system are enumerated below:

- Structural simplicity, which is amenable for integration for high-power applications.
- High efficiency (> 98.5%) of power conversion due to single-stage operation.
- Cost-effective as fewer semiconductors are required to extract power from PV panels.
- Maximum power point tracking (MPPT) control is unreliable as many PV modules are connected in series and parallel.
- This scheme is not reliable as faults in the inverter may lead to the loss of power generation.
- Requirement of an additional blocking diode in each string, which reduces the overall efficiency.

1.2.2 String Inverter

In this configuration, the input of each modular structured string inverter is connected to each PV string, which consists of series-connected solar panels. The output of each string is connected to the grid through a common parallel path as shown in Figure 1.3. In case of the requirement of high DC-link voltage to inject power into the grid, a voltage boosting stage may be included between the PV panels and the inverter. The string inverter achieves the following advantages in comparison to a centralized integration system.

- Better PV power extraction w.r.t the MPPT performance.
- No additional power loss in the blocking diodes.

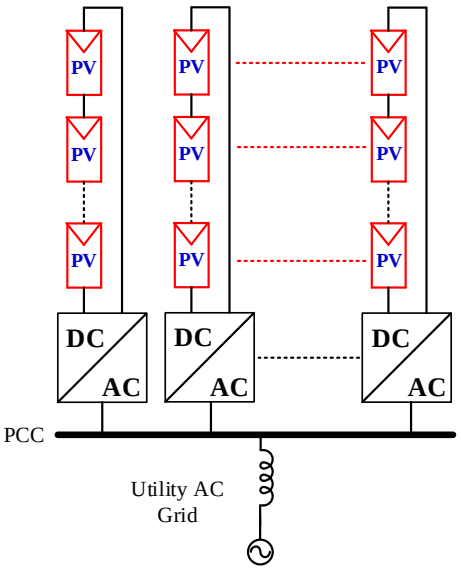


Figure 1.3: Configuration of String Solar Inverter.

- The current from the PV string is limited at lower irradiance levels.
- Requirement of an inverter for each string.
- Efficiency ranges from 97.8% to 98%. [6]

1.2.3 Micro-Inverter

Microinverter topologies are chosen for the power level ranging from 100W to 500W. In this scheme, the power processing unit (PPU) is connected to an individual PV module to achieve independent MPPT for each PV module. This is capable of maximizing power output from the PV system as each module is integrated into the grid via one or two power conversion stages. In the case of the partial-shading condition, these systems outperform both central and string inverter schemes. The merits of this scheme are enumerated below:

- The 'plug-and-play' feature of this scheme facilitates easier implementation and maintenance.
- Microinverters are flexible and modular in structure.
- As these configurations are an integrated part of each PV module, it minimizes the power loss due to irradiance mismatch among the PV panels.
- The installation cost per kW is comparatively higher.
- Higher boosting is required to match the PV panel voltage with the grid voltage.
- The typical efficiency of this type of system is 96.5%.[6]

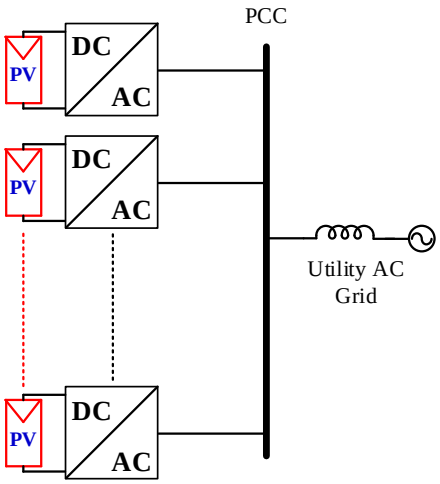


Figure 1.4: Configuration of Module-based Solar Inverter.

Table 1.1: Comparison of PV Module Integration schemes

PV Integration Scheme	**Module Based**	**String**	**Central**
Power Range	200-500W	5-10kW	>100kW
Converter Efficiency	up to 96.5%	up to 97.8%	up to 96.8%
MPPT control	1.Simple to implement. Easy to track MPP. 2.Highest MPPT efficiency.	1.Improved MPPT performance in comparison to the centralized inverter.	1.Maximum power point tracking (MPPT) control is disproportionate as it is common for the combined PV array.
Advantages	1. Flexible and modular. 2. Easy implementation 3. Its 'plug and play' feature simply system installation and maintenance. 4. Panel level hot-spot risk is removed and panel lifetime can be improved.	1.No string diodes. 2.Reduced DC wiring. 3.Flexible and modular structure.	1.Cost-effective for utility-scale applications.
Limitation	1.High cost per watt. 2.A two-stage system with voltage boosting is necessary. 3.High power losses.	1.High component count. 2.An inverter is required for each string. 3.Power from the PV string is limited by the shaded PV panel.	1.Needs blocking diode. Reduction in energy yield in case of partial shading, and may lead to hot spot failure under significant unequal shading. 2.Need for high-voltage DC cables between PV panels and inverter.
Commercial Products	Enphase IQ8 Microinverter,	Danfoss ULX4000	Sunny Central inverter, with 1,850 kVA/2,200 kVA for 1,000 V_{DC}

1.3 Classification of PV Inverter Topologies

Another classification of the PV inverters is based on the number of power conversion stages and the type of transformers employed in the system [7]. These transformers can be either low-frequency transformers (LFT) or high-frequency transformers (HFT). The non-isolated inverter topologies, which do not possess transformers, are also known as transformerless topologies. These topologies are classified into the following groups:

1.3.1 Low-Frequency Transformer Based Single-stage Inverter

These configurations possess a line-frequency transformer at the output terminal of the inverter configuration. These configurations are capable of boosting the output voltage as well as providing galvanic isolation. Further, the galvanic isolation eliminates the leakage current. However, these configurations suffer from reduced energy density, increased weight and volume, and low efficiency on account of power losses in the transformer.

1.3.2 Transformerless Single-stage Inverter

These configurations do not possess any transformer in their structure. As these configurations have a single power conversion stage to convert PV power, they display higher efficiencies. However, these configurations lack the capability of voltage boosting and do not provide galvanic isolation. The lack of galvanic isolation causes significant leakage current, which is a definitive drawback in these systems. Besides this shortcoming, these configurations require a higher number of PV panels to be connected in series.

1.3.3 Low-Frequency Transformer Based Two-stage Inverter

In this category, similar to an LFT-based single-stage inverter, a ~~low~~ line-frequency isolation transformer is inserted between the output of the inverter and the load, which provides galvanic isolation. In these converter configurations, the PV power is processed through an additional front-end non-isolated dc-dc converter. This dc-dc converter boosts the PV voltage and regulates the DC-link voltage. The demerit of these types of topologies is the increased cost, weight, and power loss, making these configurations less attractive and uneconomical.

1.3.4 High-Frequency Transformer Based Two-stage Inverter

High frequency-transformer-based inverter configurations are elegant in the aspect of the size and weight of PV systems. In this category, a high-frequency transformer is inserted in the front-end dc-dc conversion stage. The high-frequency transformer adds the benefit of reduced size and weight of the overall system. Also, the galvanic isolation between the PV panel and the load has the benefit of eliminating the leakage current. However, the inclusion of the high-frequency DC-DC isolation stage increases the number of power processing stages in the system, which results in reduced efficiency.

1.3.5 Transformerless Two-stage Inverter

In this category, a non-isolated dc-dc power conversion stage is inserted in between the PV source and a single-stage transformerless PV inverter. The dc-dc boost conversion stage lowers the number of PV panels at the input, reducing the volume, weight, and losses in the system. However, the non-existence of galvanic isolation between the PV source and the load results in a significant leakage current.

1.4 Leakage Current in Transformerless PV systems

PV panels have a metallic frame, which needs to be grounded to comply with various safety regulations and standards [8]. Since PV panels accumulate a considerable charge on their surfaces, a parasitic capacitance is formed with the metallic frame as shown in Figure 1.5. This parasitic capacitance is a distributed parameter, which depends on the following parameters:

- The surface area of the PV panel and metallic frame.
- Dust and humidity are generally responsible for the electrical conductivity of the surface.
- Environmental Conditions

The value of parasitic capacitance of various PV panels from different manufacturers (e.g. Soleil FVG 36-125, Kyocera KS10, and BP Solar MSX120) is extensively measured at various conditions of humidity. It is observed that the value of the parasitic capacitance varies between 50nF to 150nF per kW of installed PV panels. Though this parasitic capacitance is

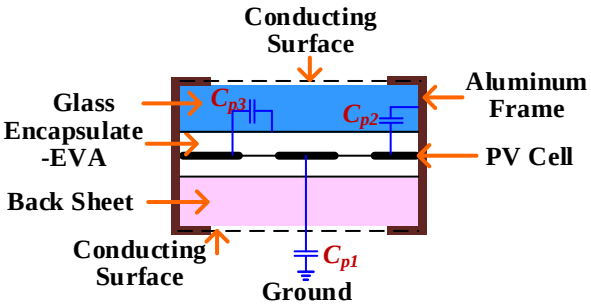


Figure 1.5: Parasitic capacitances in a typical PV Panel.

present in every PV installation, the production of the leakage current depends on the return path provided by the power converter circuit.

The equivalent value of the parasitic capacitance is the summation of all partial capacitances (C_{p1}, C_{p2}, C_{p3}..) as shown in Figure 1.5. Since the value of the parasitic capacitance varies in a wide range due to the atmospheric condition and construction, a lumped equivalent value of 100nF/kW has been chosen for the simulation and experimental study of the proposed system w.r.t the ground leakage current.

A transformerless inverter configuration lacks galvanic isolation between the PV array and the grid. As the terminals of the PV panel are directly connected to the grid through power electronic switching devices, voltage fluctuations between PV panels and the grid see a capacitive return path. These voltage fluctuations charge and discharge the parasitic capacitance formed between the charged surface of the PV cells and the metallic structure of the panel, which leads to the flow of the leakage current. According to various studies, it can pose an electrical hazard when a person touches the exposed parts of the PV panels as the ground leakage current can flow through the human body, leading to an electrical shock and possibly, a serious injury [9]. In addition, this ground leakage current causes an increase in current harmonics, higher power losses, and electromagnetic interference (EMI) issues [10]. This current also deteriorates the lifespan of the PV panel.

1.5 Requirement of Voltage Boosting

For grid-connected applications, the dc-input voltage of inverters should be higher than the peak voltage of the grid. As an example, if the grid voltage is 110V, the minimum

DC-link voltage of the inverter is 200V. Similarly, for a 230V grid, the minimum DC-link voltage should be 400V. On the other hand, in standalone applications, the DC-link voltage is decided by the load. However, popular PV panels have a low voltage range. Thus, to achieve a higher voltage at the dc-input terminals, multiple PV panels are connected in series. During partial-shading conditions, a shaded cell is reverse biased by the voltage from series-connected and unshaded cells. In the reverse biased condition, a cell dissipates much of the power injected from unshaded cells and converts it into heat. With the bias and elevated temperature, localized heating on the cell (i.e., hot spot) due to the high-density current going through localized defects of low shunt resistance may cause permanent damage to the cell's P-N junction, and cause delamination, back sheet burning, and even fire [11]. Besides that, the power loss incurred due to the reverse current in the blocking diodes degrade the overall efficiency of the power conservation stage. Potential induced degradation (PID) is often caused in crystalline silicon PV modules. High rates of PID are observed when the outer surface of the module becomes electrically conductive forming the ground electrode against the negative cell bias [12-13]. This effect is caused by surface humidity in real operation and can be simulated in climatic cabinets by applying wet cloth or highly conducting layers on the glass panes (e.g. aluminium foils or carbon) paper [14]. The high potential causes a circulating current, which is a measure of the degradation rate [15-16] of the panels. The magnitude of the circulating current varies proportionately with the maximum voltage in a series branch based on temperature and humidity conditions. Thus, it is obvious that one should use a voltage-boosting stage rather than an increased number of panels in series. Varying environmental conditions may also affect the voltage across the series string of the PV array, which further emphasizes the necessity of voltage boosting in PV systems [17].

1.6 Outline and Parameters of Grid-connected PV System

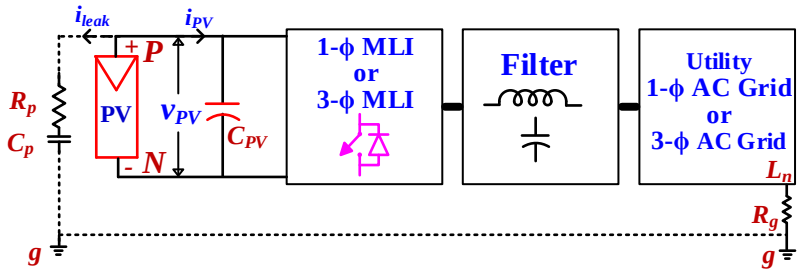


Figure 1.6: Outline of a grid-connected PV-based system.

Grid-connected PV systems are composed of the PV source and the inverter that is connected to the utility grid. Based on the voltage level of the PV array, a PV inverter may be designed either as a single-stage system or as a two-stage system as per the variants illustrated in section 1.3. In single-stage systems, the voltage of the PV array should be adequately high, to be able to inject power into the utility grid. Besides the implementation of the maximum power point tracking (MPPT), power injection into the grid is also controlled in a single-stage system. In a double-stage system, a front-end dc-dc stage is inserted between the PV source and inverter. The dc-dc stage boosts the PV array voltage while achieving maximum power point tracking. This stage can be implemented by any one of the several boost topologies suggested in [18].

Figure 1.6 illustrates the general layout for a transformerless inverter for PV systems. A front-end dc-dc stage is often inserted between the PV source and the inverter. A passive filter is connected to the output of the inverter, based on the harmonic requirement of the load. The output terminals of the inverter can either be connected to a standalone load or a grid. The neutral point of the single-phase or three-phase load is denoted as L_n in Figure 1.6. Due to the lack of galvanic isolation, a parasitic closed path is formed from the PV terminal to load neutral (which is also grounded). The grounding impedance of the proposed system is indicated as R_g. This path consists of a large stray capacitance, which is formed between the PV panel and its structure. The lumped model of this distributed stray capacitance is represented as a series branch, which consists of a resistor (R_P) and a capacitor (C_P) in Figure 1.6. It can be observed that this parasitic branch is energized by the voltage, which appears across the positive terminal of the PV panels (*i.e.* **P**) and the load ground terminal (*i.e.* **g**).

This voltage is termed the *PV parasitic voltage* [19-20] or total common-mode voltage [21-22] in various works of literature. The current (i_{leak}) flowing through this parasitic path is termed as *leakage current* [8,23] or *common-mode leakage current* [18]. Due to the capacitive nature of the parasitic path, the high-frequency voltage transitions in v_{Pg} produce the leakage current. This leakage current contains components corresponding to the switching frequency, which inject harmonics into the grid current. Some of the well-known ill-effects of the leakage current are: increased power loss, poor electromagnetic compatibility, and decreased operational safety (possible electric shock) [9], [24].

1.7 Important Standards Dealing with PV Systems

While injecting the generated power into the grid, PV systems should comply with different standards as stipulated by various international agencies [25-29]. When a PV system operates in the grid-connected mode, some important parameters need to be taken care of to achieve an acceptable performance level. These include total harmonic distortion (THD), injected direct current, range of grid frequency, power factor, and leakage current. In most PV standards (IEEE 1547, AS4777, EN 61000-3-2), the maximum allowable THD of the grid-current is limited to 5%, which is the reason for an improved power quality at the distribution feeders.

Considering the lack of galvanic isolation between the PV panels and the grid in the transformerless grid-tied systems, the leakage current generated by the PV parasitic capacitor should be handled carefully to avoid disconnection from the grid. The peak value of leakage current over 300 mA must trigger a break in the circuit within 0.3 sec as per the German standard VDE 0126-1-1. Irrespective of the power level, if the amplitude of leakage current increases beyond an acceptable value, a break in the circuit should be triggered within a certain time as listed in Table 1.2. To improve the grid stability and reliability, the standard VDE-AR-N-4105 specifies that the inverter should be capable of delivering reactive power within the power factor range of 0.9 to 0.95.

Table 1.2:Various Standards and Codes for PV Systems

Standard	Parameter	Range
IEEE 1547 **IEC 61727** **IEC 613000-3-2**	THD	<5%
VDE 01260-1-1	Leakage Current	< 300 mA (peak)
VDE-AR-N-4015	Reactive Power	0.95 lagging and 0.95 leading

1.8 Motivation

Based on the above literature review, the following observations were made w.r.t the existing transformerless PV inverter topologies:

1. The PV inverter topologies available in the existing literature are confined only to three-level systems. These power converters require either a higher number of switching devices or multiple PV sources. This increases the cost and complexity of the power converter and poses difficulties while implementing the maximum power point tracking algorithm.
2. Most of the existing transformerless topologies are not capable of boosting the input PV voltage. Thus, an additional dc-dc boost stage is employed to obtain the required dc input voltage for the inverter. This calls for additional high-power switching devices in the dc-dc boosting stage, reducing the overall efficiency and reliability of the system.
3. The conventional switched-capacitor-based multilevel inverter (SC-MLIs) configurations are capable of boosting the input PV voltage while providing multilevel output. However, most of these configurations operate with the hard-charging of the switched capacitors, causing pulsed currents of large magnitude. This stresses the semiconductor devices associated with the switched capacitor network.
4. Apart from the additional semiconductor devices, some of the inverter topologies require complex clamping-circuitry and common mode filters to eliminate high-frequency transitions in the PV parasitic voltage to reduce the leakage current. This further increases the size, volume, and cost of the system.

This thesis describes the research endeavor directed to address the aforementioned shortcomings and further the existing knowledge pool in this area.

1.9 Objectives

The research work presented in this thesis puts an effort to address the following issues:

1. Propose new power converter configurations to simultaneously realize the objectives of voltage-boosting, multilevel inversion while achieving compliance with the specified standards for the leakage current
2. Investigate the possibility of enhancing the overall efficiency of the power converter by transferring a considerable portion of the generated PV power directly to the load with the aid of the switched-capacitor networks
3. Conceive strategies to avoid the hard-switching of the switched capacitor networks to alleviate current stresses on the semiconductor switching devices and the passive components.
4. Develop new PWM schemes / adopt the existing PWM schemes for the proposed power converters to minimize or reduce high-frequency transitions in the PV parasitic voltage, which paves the way to the suppression of common-mode voltages and consequently the leakage current.

1.10 Organization of the Thesis

This thesis is structured into six chapters, which are summarized below:

Chapter 2, addresses the comprehensive review of several transformerless PV inverter configurations for single-phase and three-phase applications. The PV inverter topologies are classified into three basic categories i.e. half-bridge, common-ground, and full-bridge type based on various methods of leakage current reduction techniques. Further, the existing literature on multilevel converters (which are realized by extending these basic configurations) is reviewed.

Chapter 3, presents a single-phase seven-level transformerless PV inverter configuration. Further, this chapter presents a modulation technique for the proposed inverter configuration to eliminate the high-frequency switching transitions from the PV parasitic

voltage / total common-mode voltage. The principle of the PWM technique is then validated with mathematical analysis based on the switching functions. It is shown that this power converter is capable of transferring 37% of PV power directly to the load, which enhances its efficiency. Also, the control scheme of the proposed inverter configuration is presented in the grid-connected mode. The concept and performance of the proposed inverter are then validated through simulation and experimental studies. Finally, the proposed configuration is compared with the existing multilevel inverter configurations to emphasize its features and advantages.

Chapter 4, presents a nine-level hybrid T-type transformerless PV inverter configuration along with its PWM technique. The working principle and various modes of operation of the proposed nine-level inverter are presented. The comparative analysis of the proposed PWM scheme is also presented to highlight its advantages vis-à-vis the other schemes reported in the literature. It is shown that this power converter transfers 42% of the generated PV power directly to the load, which plays a pivotal role in the enhancement of its efficiency. The simulation and experimental results are presented to validate the operation of the proposed configuration. Finally, the comparison of the proposed nine-level hybrid boost inverter with the other existing transformerless inverter is presented to highlight its benefits.

Chapter 5, presents a thirteen-level transformerless PV inverter configuration and two modulation techniques. The operation of the proposed inverter configuration is presented with both of these PWM schemes. Analysis of leakage current is also presented for the proposed inverter. Further, a comparative study of the proposed PWM scheme with the existing leakage current reduction techniques is presented. Simulation and experimental results are presented to validate the operation of the proposed power converter. Finally, the benefits obtained by the proposed power converter, compared to the other converters available in the existing literature, are presented.

Chapter 6, presents a T-type hybrid transformerless three-phase inverter with voltage boosting capability. Various modes of operation of the proposed configuration are presented along with its PWM scheme for the reduction of the leakage current. Employing switching functions, the common-mode voltage is analysed. Also, the powers processed in single-stage

operation and the double-stage operation are assessed. Simulation and experimental results are presented to validate the proposed configuration. Further, a comparison with existing three-phase configurations is presented to highlight the features of the proposed configuration.

Chapter 7, summarizes the important findings of the research work reported in this thesis and suggests possible extensions for future work.

Chapter 2

Literature Survey

Chapter 2

Introduction to Transformerless PV inverter topologies

This chapter presents a comprehensive review of various single-phase and three-phase transformerless inverter configurations for PV systems. The reviewed transformerless PV power circuit configurations are categorized based on their basic structures and multilevel extensions of these structures. A detailed discussion about these transformerless PV inverters on the voltage boosting technique, the number of levels in the output voltage, and reactive power sourcing capability are presented in this chapter.

2.1 Single Stage PV Inverters

The classification of single-phase transformerless PV inverter topologies is presented in Figure 2.1. The inverter topologies are also broadly classified based on the type of filter connected to the output. An asymmetrical output filter is used in half-bridge, common-ground, and unfolding-type configurations whereas a symmetrical type filter is employed in full-bridge-based configurations.

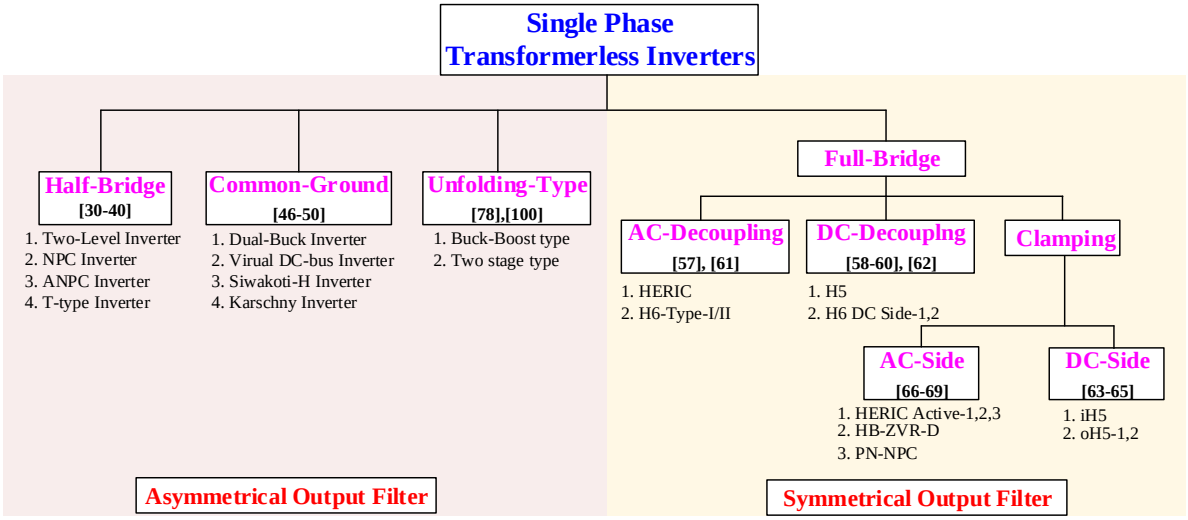


Figure 2.1: Classification of single-phase transformerless PV inverter topologies.

2.1.1 Half-bridge Type Transformerless Inverter Topologies

In this family of inverter configurations, the load neutral is connected to the mid-point of the DC-link capacitors. The half-bridge (HB) inverter based on two switches [30] utilizes the DC-link capacitors to generate the output voltage (Figure 2.2 (a)). In this scheme, the cyclic utilization of the DC-link capacitors results in an increased current ripple at the output. Implementation of MPPT at unequal irradiance conditions is also complicated in this scheme. To improve the efficiency and reduce the current ripple, a neutral point clamped (NPC) topology is introduced in [31] (Figure 2.2 (b)). In contrast to the half-bridge structure, a zero-voltage state is imposed through the clamping diodes of the inverter. Though the NPC configuration is capable of reducing the cost and size of the filter, it results in an unbalanced conduction loss among the semiconductor switches. In this context, an active NPC (ANPC) is introduced in [32] (Figure 2.2 (c)), which mitigates the limitation of the NPC-based configuration. The diodes in the NPC structure are replaced with switches to improve the efficiency of the overall system. To reduce the conduction loss further, a bidirectional switch is connected as a T-leg, (Figure 2.2 (d)) [33] which is inserted between the mid-points of the DC-link. The T-leg is constituted by an anti-series connection of two semiconductor devices with l7ow voltage drops. To improve power quality and reduce the complexity of control, the

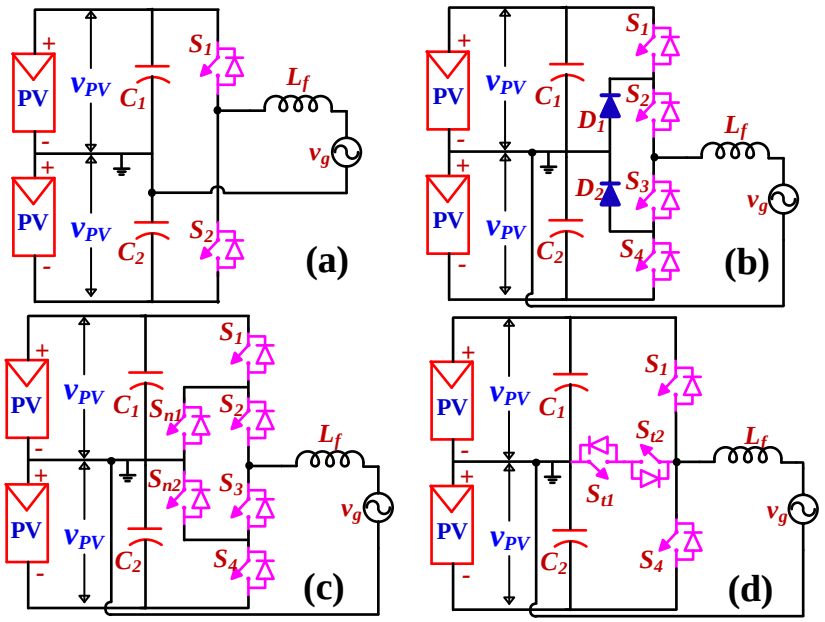


Figure 2.2: Half-bridge based 2L inverter configuration (a) Half-bridge, (b) NPC type, (c) ANPC type, (d) T-type.

the half-bridge-based configurations (T-type, NPC, and ANPC) are extended to their multilevel versions for high power applications [34-35]. These configurations also achieve high conversion efficiency with low switching losses [36] and elimination of the leakage current [37].

The aforementioned inverter configurations are capable of providing only three levels in the output voltage. A higher number of levels in output voltage is possible with the topologies introduced in [38-45]. Diode-clamped and flying-capacitor (FC) based neutral-point-clamped (NPC) MLI configurations are described in [38] and [39]. The diode-clamped NPC configuration synthesizes five distinct voltage levels using eight switches, six diodes, four DC-link capacitors, and two isolated PV sources. In contrast, the FC-based NPC MLI requires five capacitors and eight switching devices to generate a five-level voltage waveform at the output. These configurations suffer from the disadvantage of an increased number of switching devices and capacitor voltage balancing issues. These issues are addressed in the configuration given in [40]. In this paper, a five-level ANPC type clamped inverter is presented. The inverter configuration utilizes six switches and one PV source to generate a five-level voltage waveform at the output. The topology is also capable of sourcing reactive power to the load while reducing voltage ripple across the DC-link capacitors. Due to the neutral point connection, the topology is capable of eliminating leakage current effectively. However, the half-bridge-based configuration suffers from voltage oscillation in the DC-link capacitors. In addition, the required DC-link voltage for these configurations is twice that of the grid-peak voltage. This increases the required number of PV panels to be connected in series.

2.1.2 Common Ground Type Transformerless Inverter Topologies

In these configurations, the negative terminal of the PV panel is directly connected to the neutral terminal of the load. This type of connection is capable of maintaining the PV parasitic voltage to be a constant value irrespective of the switching frequency of the inverter and the type of the load connected at the output. This connection is also capable of minimizing the common-mode leakage current. The inverter topology (Figure 2.3(a)) proposed in [46] utilizes the virtual DC bus technique to generate three-level voltage output. The virtual-dc

capacitor is utilized to generate a negative voltage at the output. Furthermore, the common-ground structure restricts all transitions in the voltage across the parasitic path, keeping its magnitude constant. However, the design of the virtual dc capacitor is crucial as it is required to regulate the voltage in each switching period. A common-ground inverter configuration, which is based on the concept of a charge pump, is discussed in [47]. This topology utilizes the same number of switching devices as the full-bridge inverter. A two-stage charge transfer process is utilized in this configuration to reduce the current stress on the switching devices. However, the inverter configuration has two diodes in its charging path, which reduces its efficiency and the operation of the inverter is limited to three-level output. Likewise, a flying-inductor-based common-ground inverter configuration is given in [48]. Due to the discontinuous conduction mode (DCM) of operation, semiconductor devices suffer from high peak current stresses and high conduction loss, which reduces the efficiency of the inverter configuration. Another type of common-ground inverter structure is based on the integration of two buck converter modules [49, 50] (Figure 2.3 (b), (c)). One of these buck-converters is utilized to generate the positive half-cycle of the output while the other produces the negative half-cycle. These two buck-converter modules can be connected either in series or parallel. The series connection [49] based approach is implemented with NPC structure and two inductors as shown in Figure 2.3(b). In this configuration, the DC-link voltage requirement is twice that of the peak voltage of the grid. The variant based on the parallel connection requires a lower DC-link voltage [50] (Figure 2.3(c)). This reduces the requirement for the PV panels to be connected in series. Though these configurations are capable of avoiding the shoot-through problem of the half-bridge topology, the filter inductors of this inverter configuration increase the cost and power density.

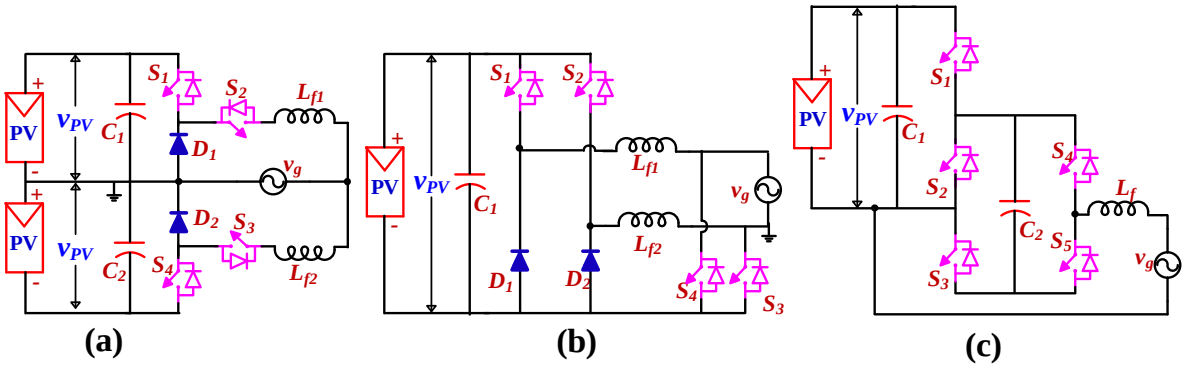


Figure 2.3: Common ground-based 2L inverter (a) Virtual DC-bus, (b) Series connected buck inverter, (c) Parallel connected buck inverter.

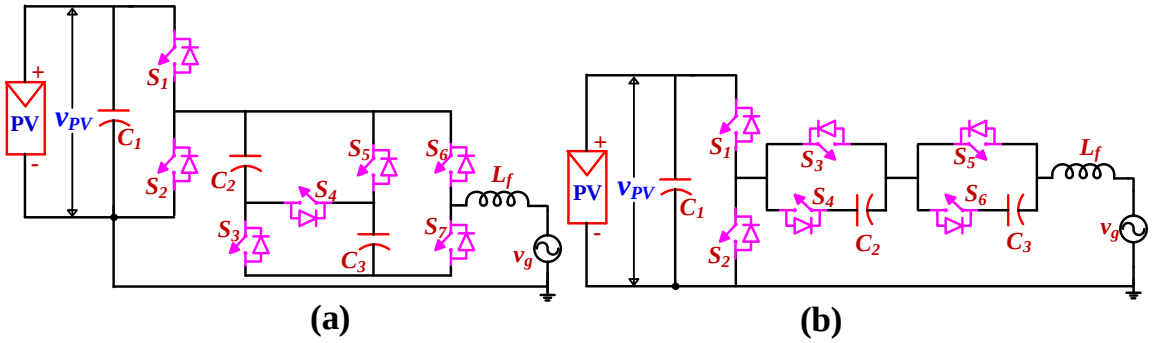


Figure 2.4: Common ground-based 5L inverter (a) Virtual DC-bus, (b) Series connected FC unit.

Multilevel inverter configurations based on the common ground are introduced in [51-74]. In [51], a five-level common ground transformerless inverter is developed, which utilizes switched-capacitor cells to synthesize multi-level voltage output. But the additional capacitors are charged only during the positive half-cycle period of the grid voltage, which requires a capacitor of high value to maintain the regulated dc-voltage during the period of negative half-cycle of the grid voltage. In addition, the maximum modulation index for this configuration is also limited by the power factor (PF) of the load, which leads to the underutilization of the DC-link. Considering the concept of a virtual dc bus with switched capacitors, a five-level common-ground-based inverter configuration is introduced in [52] as shown in figures 2.4 (a) & (b). The configuration utilizes two switched capacitors for the synthesis of five levels at the output voltage. However, the switching devices associated with the charging path for both of the capacitors withstand high current stress which reduces the overall efficiency of the inverter. However, these topologies also suffer from the asymmetric positive and negative half cycle of the fundamental grid voltage cycle.

2.1.3 Full-bridge Transformerless Inverter

Single-phase full-bridge inverter configurations can be operated either with a unipolar PWM scheme or a bipolar PWM scheme. The unipolar PWM scheme [55] improves the harmonic performance of the inverter. The unipolar PWM strategy results in a reduced current ripple which further reduces the requirement of the size of the filter at the output. However, in a unipolar PWM scheme, the occurrence of an active zero state in each switching cycle causes the common-mode voltage to oscillate at the switching frequency. These voltage transitions result in a high leakage current for PV inverter applications which violates safety

standards and affects the lifetime of the PV panels. In contrast, the bipolar PWM scheme [56] eliminates all the high-frequency transitions from the common-mode voltage. This reduces the leakage current in the parasitic elements of the PV panel which allows its applicability for PV-based applications. However, the bipolar modulation scheme results in higher losses in the filter as the output voltage switches between the positive DC-link voltage to the negative DC-link voltage in each switching cycle. It also increases the filter requirement of the inverter. In this context, the conventional full-bridge inverters are modified with additional semiconductor devices with various decoupling and clamping techniques to obtain improved harmonic performance and reduced leakage current. These power converter configurations are described in the following section.

2.1.3.1 AC Decoupling Based Full-bridge Inverter

An AC decoupling network in a full-bridge inverter configuration is formed by inserting a bi-directional switch across the inverter output terminals. Different types of ac-decoupling networks are presented in Figure 2.5. Two anti-parallel IGBTs, each connected to a series diode accomplish the bi-directional capability [57] as shown in Figure 2.5(a). The other variant implements the bidirectional functionality with two IGBTS connected in anti-series (Figure 2.5 (b)) or a full-bridge diode module with an IGBT. At the zero-voltage level, the bi-directional switch is turned on, which decouples the PV panel and the load. This eliminates high-frequency voltage transitions from the PV parasitic voltage without sacrificing the harmonic performance of the inverter at the output. It also achieves an improved efficiency, as only one of the two switches conducts in each turn-off state.

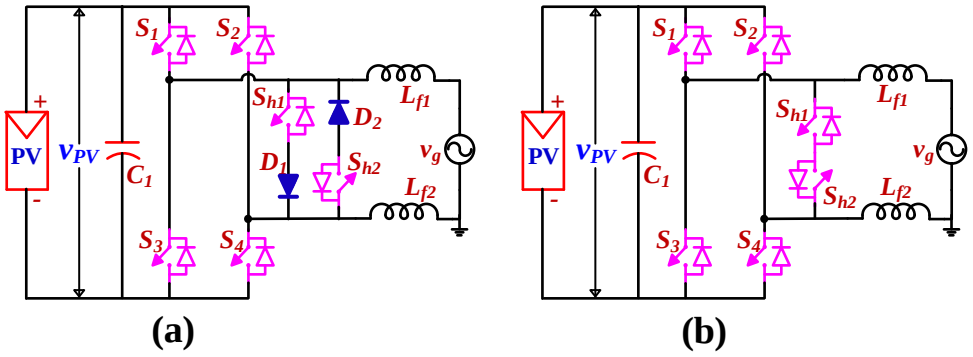


Figure 2.5: HERIC inverter with variants (a) HERIC inverter variant-1 (b) HERIC inverter variant-2.

2.1.3.2 DC Decoupling Based Full-bridge Inverter

In this class of power converters, an active switch that acts as a dc decoupling network [58] is inserted between the positive terminal of the PV source and the full-bridge inverter module as shown in Figure 2.6. The zero-voltage level is implemented using inverter high-side switches (S_1 and S_2) while the decoupling switch S_5 is turned off to disconnect the PV panel from the grid at those instants. This eliminates all of the high-frequency transitions from the PV parasitic voltage which reduces the leakage current. However, the switching frequency of the decoupling switch is twice compared of the other inverter switches, which results in an unbalanced switching and conduction loss which further burdens thermal management. Another variant of the dc-decoupling network is introduced in [59] wherein, a switch is inserted in both positive and negative rails as shown in Figure 2.6(b). This configuration allows the employment of the unipolar SPWM with a balanced loss distribution among the high-frequency switches. Also, this converter reduces the filter requirements and improves the harmonic performance of the inverter while minimizing the leakage current. However, inverter configurations based on the dc decoupling suffer from an overall increment of the conduction loss due to the additional power devices in the series of the load current path.

Multilevel inverter configurations with dc-decoupling are introduced in [60-62]. A 5L inverter topology is presented in [60], which employs a cascaded half-bridge (HB). The basic configuration has been modified with dc-decoupling [60] and ac-decoupling [61]. The alleviation of the leakage current is achieved by the employment of the modified modulation techniques in these papers. However, the output voltage of both of these inverter

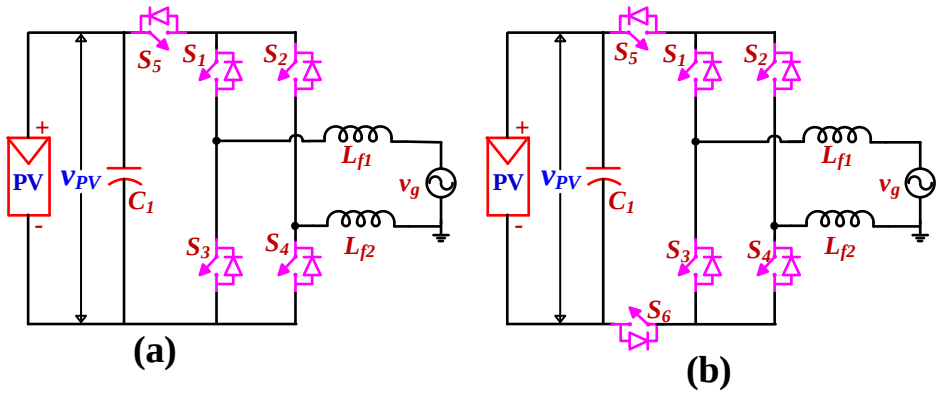


Figure 2.6: (a) H5 inverter (b) H6 inverter.

configurations suffers from two major disadvantages: (a) high total harmonic distortion (THD) and (b) high *dv/dt* across the switches w.r.t the conventional staircase type multilevel output voltage. In addition, these configurations require two PV sources which further increases the complexity to implement the MPPT. Besides that, as the presented configuration is a cascaded structure, the power ratings of the PV panels are unequal, which restricts the applicability of this type of power converter configuration.

2.1.3.3 Mid-Point Clamping Based Full-bridge Inverter

In full-bridge inverters, a resonant path is constituted by the filter inductor, the switch parasitic capacitance, and the PV parasitic capacitance during the freewheeling mode of operation. It is also observed that high-frequency voltage transitions in the PV parasitic voltage may cause resonance, which may lead to the generation of leakage current. To clamp the PV Parasitic voltage to half of the DC-link voltage during the freewheeling period, the DC-link capacitors are divided into two capacitors of the same value. A clamping cell is inserted between the mid-point and full-bridge inverter module. This can provide a well-defined and constant PV parasitic voltage during each switching transition, which eliminates the effect of the junction capacitors of the switches. The active and passive clamping schemes can be employed to eliminate the parasitic resonance and additional leakage current. The active clamped dc-based iH5 inverter is derived [63] when an active switch is inserted between the midpoint and the upper terminal of the full-bridge module as shown in Figure 2.7 (a). Based on the position of the clamping network, these configurations are further classified as DC-side or AC-side clamped inverters. The other topologies based on the DC-side clamping are as follows: oH5-1 [64], oH5-2 [64], H5-D [65], etc. Besides that, clamping networks situated on the AC side are also used to clamp the common-mode voltage effectively at a constant value and avoid the floating operation. The highly efficient HERIC topology is an example of this class of converters, which leads to the genesis of a family of advanced transformerless inverters with leakage current elimination.

If the bidirectional switch is realized by two IGBTs, connected in an anti-parallel fashion along with their diodes, a clamping switch can be inserted between the midpoint of the series bus capacitors and the anode of the bidirectional switch. Similarly, if the

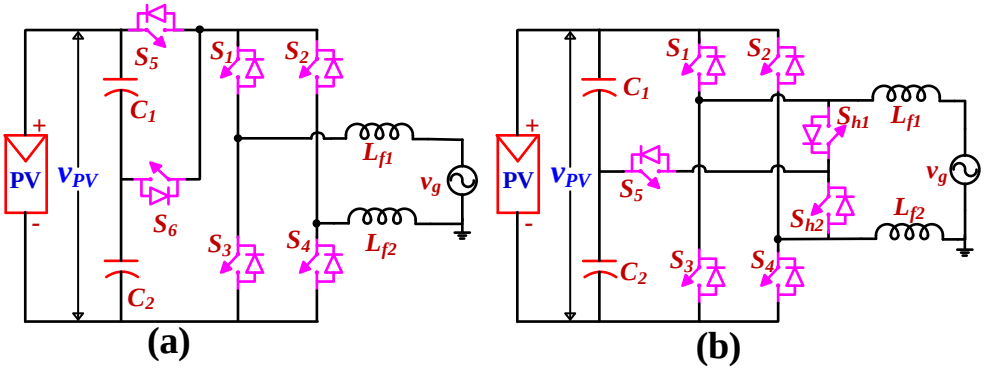


Figure 2.7: Full bridge transformerless inverter based on neutral point clamping at (a) DC side, (b) AC side.

bidirectional switch is obtained with the anti-series connection of two IGBTs, another active switch is required to perform the function of active clamping as shown in Figure 2.7 (b). As mentioned before, the resonance between the parasitic capacitors of the power switches and the output filters during the zero voltage generation stage causes high-frequency pulsed components. These are effectively eliminated in the HERIC-based active clamping inverter, as the terminal voltages are completely clamped to half of the bus voltage by turning on the active-clamp switch. A set of active and passive clamping techniques on HERIC configuration and their operations has been presented in [66]. Some more topologies based on the AC-side clamping are as follows: PN-NPC [67], HB-ZVR [68], HB-ZVR-D[69], etc.

From the comprehensive review and detailed comparison of state-of-the-art transformerless inverters, it can be concluded that the ac-based decoupling topologies are highly efficient and cost-effective. Inverter configurations, which do not possess the ability of clamping, produce additional leakage current because of the occurrence of high-frequency resonance. These topologies are capable of eliminating high-frequency voltage transitions from both CMV and PV parasitic voltages. This results in an effective reduction of the leakage current. However, the topologies based on clamping require more semiconductor devices in comparison to the inverter configurations, which are based on decoupling. This compromises the efficiency of the overall system.

Table 2.1: Comparison of Different Transformerless Inverter Configurations

Inverter Configuration Type	**Advantages**	**Disadvantages**	**Similar structured with different voltage levels**
Half-bridge Based: NPC, ANPC, T-type	• Leakage current effect eliminated. • Required smaller filter at the output. • Possibility to extend for three phases • Reactive power capability.	• Input voltage is twice that of the grid peak voltage. • Higher voltage ripple in dc-link capacitors.	3L: [30-33] 5L: [40],[41] 7L: [42],[43] 9L: [44], [45]
Common ground Inverter	• No CM effect. • Requires lesser semiconductor devices • Small filter required.	• Requirement extra switched capacitor or flying inductor or flying capacitor. • Increased power loss due to peak current capacitor charging current	3L:[46-50] 5L: [51],[52] 7L:[53],[54]
AC Decoupling	• Minimal leakage current. • Low conduction loss. • Lower THD. • Output current doesn't flow through the anti-parallel diodes of full-bridge.	• Requires additional switches. • Residual line frequency leakage current.	3L: [57] 5L:[61]
DC Decoupling	• Minimal leakage current. • Lower component count.	• High conduction losses. • Requires additional devices • Unbalanced switching. •	3L: [58], [59] 5L: [60], [62]
Mid-point Clamping	• Minimal leakage current.	• Increased component count. • Complexity in control implementation.	[64],[65],[66],[67]
HB-ZVR	• Reactive power exchange is possible. Minimal leakage current.	• Less efficiency compared to HERIC configuration and the requirement of a higher number of passive devices	[68]

2.2 Conventional Two-Stage PV Inverters

These power converters consist of a dc/dc power processing stage and an inversion stage. The input PV voltage is boosted to obtain the required DC-link voltage and is regulated with a dc/dc stage. To reduce the filter size and improve the spectral performance, a multilevel inverter is employed at the output stage of the power converter. These PV systems simplify the implementation of the control scheme. Such transformerless two-stage PV systems are reported in [70-73]. In [70], a two-stage, seven-level inverter configuration is derived. It utilizes a conventional boost converter as the front-end converter, which boosts the voltage of the input PV source. This configuration utilizes a spilt-capacitor network to synthesize

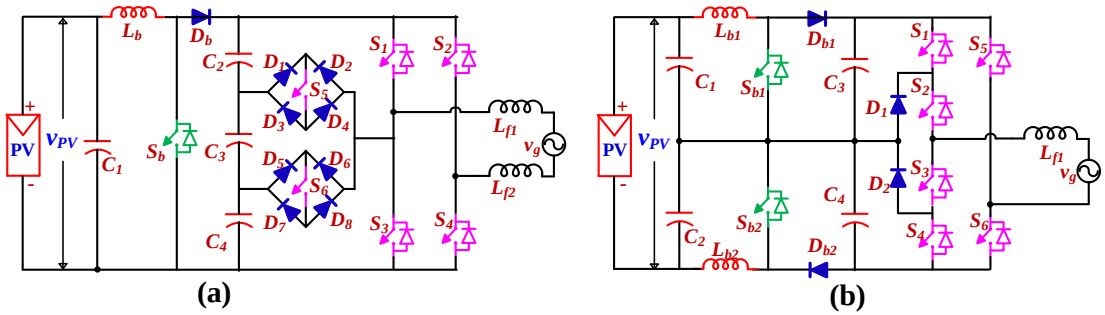


Figure 2.8: Conventional Two-stage based PV inverter: (a) [70] (b) [72].

multiple voltage levels. The unequal power utilization from the split-capacitors leads to the unbalancing of their voltages. Furthermore, this inverter configuration causes high-frequency voltage transitions in PV parasitic voltage, which induces leakage current. A common-mode filter is employed at the output of this configuration to limit the leakage current. Another two-stage PV system with a reduced number of switches is presented in [71], which consists of a front-end dc-dc converter with an asymmetrical seven-level inverter. The dc-dc converter based on the high-frequency transformer generates two isolated voltage sources, which feed the packed U-cell-based inverter. The inverter configuration is capable of generating a seven-level staircase voltage waveform at the output. However, a common-mode filter at the output is mandatory to limit the leakage current in this system. A high-efficiency, two-stage inverter configuration is introduced in [72]. This converter employs a three-level step-up converter at the dc-dc conversion stage. The inversion stage of this converter is capable of synthesizing a five-level voltage waveform. The control scheme for this converter is capable of achieving MPPT control along with the voltage balancing of the DC-link capacitors. The PV parasitic voltage for this configuration [72] is also capable of restricting the leakage current within the limit stipulated by the standard VDE-0126-1-1.

2.3 Integrated Voltage Boosting Based PV Inverters

To reduce the number of passive components and semiconductor devices in PV-based power converters, inverter configurations based on the integrated voltage boosting are introduced [74-79]. In these inverter configurations, some of the switching devices of the inverter stage are shared with the boosting stage. A review of such integrated voltage boosting topologies is presented in [74]. The authors of [75] propose a transformerless PV inverter

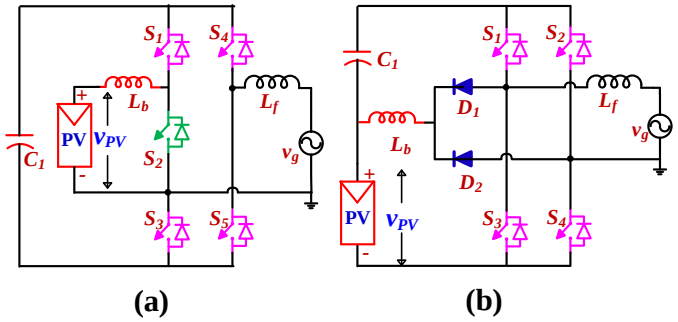
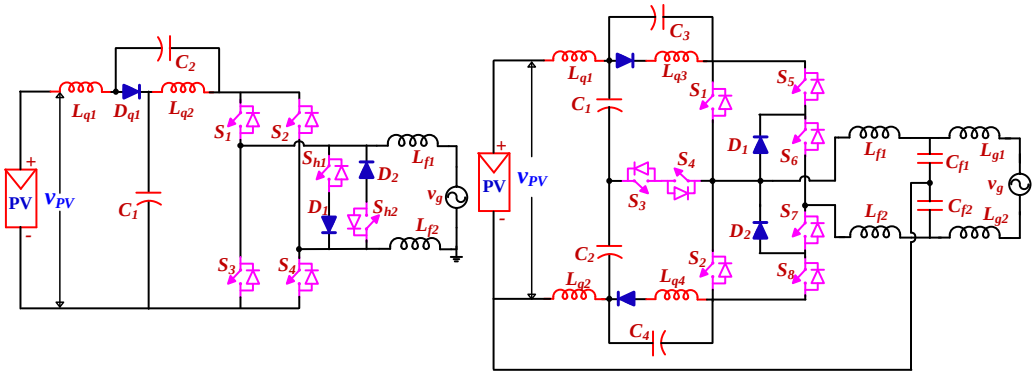


Figure 2.9: Integrated voltage boosting based PV inverter configurations: (a) [77] (b) [78].

with voltage boosting. In this configuration, the boost converter is connected in series with a switched-capacitor (SC) cell to generate the required magnitude of voltage. Since the ground terminal of the load is directly connected to the negative rail of the PV source, the common-mode leakage current is very low as the PV parasitic voltage doesn't contain high-frequency voltage transitions. However, the harmonic performance of the inverter deteriorates due to the DCM operation of the converter. Another integrated power converter with single-stage voltage boosting and inversion is discussed in [76]. This converter also aims to reduce the leakage current by suppressing high-frequency voltage transitions from the PV parasitic voltage. The drawback of this converter is that the number of output voltage levels is limited to three, increasing the filtering requirement. An improved integrated power converter is given in [77], wherein the boost converter is fused with a two-level inverter. Though the input voltage is boosted with the dc-dc conversion stage, the current stresses on the semiconductor switches are high as DCM is chosen to operate the dc-dc converter. Besides that, the number of voltage levels at the output is limited to two, requiring a higher filtering effort.

2.4 Quasi-Z-Source Based PV Inverters

A quasi-z-source (qZS) network [80] is capable of boosting the input DC voltage, based on the duty-ratio of the shoot-through mode, which is employed by the modulation scheme. Some qZS-based integrated PV inverter configurations, which provide the required voltage boosting are discussed in [81-83]. A transformerless quasi-Z-source-based two-level inverter configuration is given in [81]. In this work, the leakage current is reduced by employing the ac-decoupling method. However, these topologies require a higher number of passive devices which penalize the overall efficiency of the system. In addition, this system



(a) **(b)**

Figure 2.10: Quasi-Z-source based PV inverter configurations: (a) [81] (b) [82].

requires that the switches of the inverter configuration be switched with a higher switching frequency, which leads to increased switching power losses. A five-level qZS network-based inverter configuration has been presented in [82]. The presented inverter configuration is capable of boosting the input voltage without any front-end dc-dc conversion stage. It is also capable of eliminating high-frequency transitions from the PV parasitic voltage, which reduces the leakage current in the given configuration. However, the modulation scheme causes more dv/dt across the switches. The efficiency of the overall system is lowered due to a higher number of passive components and the presence of diodes in the path of the load current.

2.5 Switched Capacitor Based PV Inverter

A group of single-stage inverter configurations is reported in [84-98] to address the issue of the requirement of semiconductor devices with higher power ratings in the front-end voltage boosting stage. This class of converters avoids the requirement of high step-up converters at the front-end dc-dc stage. To achieve multilevel operation along with the voltage boosting capability, the concept of switched capacitors (SCs) has been introduced in [84] and [85]. A seven-level boost inverter is presented in [86], which uses this concept. This configuration utilizes a T-leg and two floating capacitors to synthesize a seven-level voltage waveform at the output. The configuration achieves self-balancing of floating capacitor voltages, enabling this configuration to achieve a voltage boost factor of 1.5. Further, this configuration eliminates all high-frequency transitions from the PV parasitic voltage, which reduces the leakage current. A similar implementation is adopted in the works described in

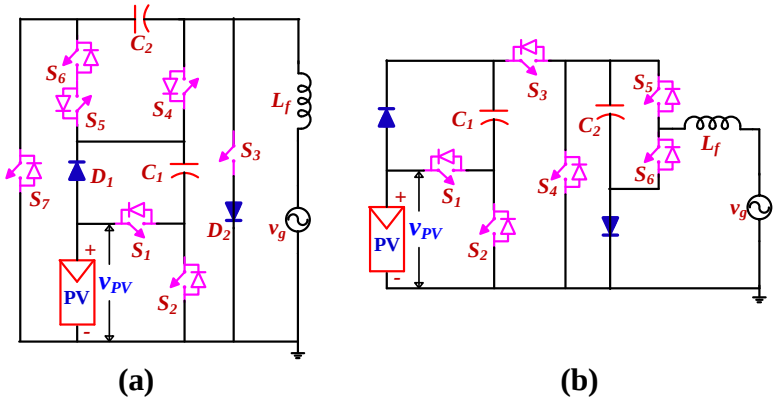


Figure 2.11: Switched capacitor-based PV inverter configurations: (a) [95] (b) [96].

[87-88], wherein a nine-level voltage is achieved at the output with a boosting factor of four. However, a higher number of bulky SCs increases the size and volume of the power converter, reducing the overall power density of the inverter. Furthermore, SCs (which are generally bulky at higher ratings) increase the peak current stresses on the associated semiconductor devices (up to six to ten times that of the load current) [89]. Thus, these topologies suffer from high-pulsed curents associated with hard-charging [90-91] of the SCs causing leading to high current stresses on the components. This further degrades the reliability, and efficiency of the inverter configuration at higher power ratings. It also reduces the durability of semiconductor devices [92]. To address these issues, another class of converters namely, the modified quasi-resonant SCMLI topologies are discussed in [91, 93-94]. These converters are capable of reducing current stresses on the inverter switches. A resonant inductor is incorporated in these power circuit configurations to provide a soft-charging current path for the switched capacitors. However, these configurations suffer from high-frequency voltage transition in the PV parasitic voltage, which causes a higher leakage current.

2.6 Semi Double-stage Based PV Inverter

The voltage-boosting based inverter configurations, which are introduced in [99] and [100] are capable of transferring the PV power in both single-stage as well as double-stage modes of operations. Both of these configurations suffer from some major drawbacks. The front-end dc-dc boosting stage in both of these configurations operates in the continuous conduction mode (CCM) to limit the peak current through the semiconductor devices and the

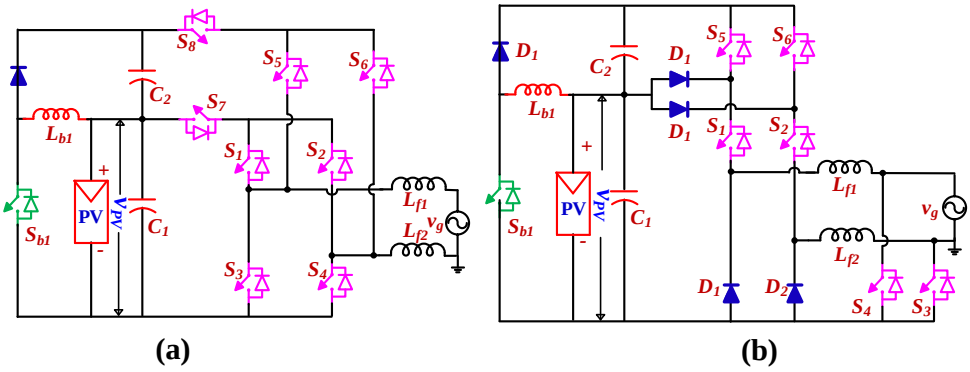


Figure 2.12: Semi-double stage-based PV inverter configurations: (a) [99] (b) [100].

step-up inductor. Similar to that of a conventional step-up chopper, the high reverse recovery current of the step-up diode causes higher power losses and momentary short-circuiting of DC-link capacitors. Furthermore, despite operating in the continuous conduction mode (CCM), high-peak currents through the semiconductor devices and inductors limit the power level of this converter topology. In addition to that, the front-end step-up converter of [100] contains a high-frequency switch which reduces the overall efficiency. Both of these configurations provide galvanic isolation neither in the voltage boosting stage nor in the inverting stage. Consequently, the issue of the leakage current is a major concern for them. The power circuit configuration presented in [99] results in transitions at the switching frequency in the common-mode voltage. Consequently, it requires additional common-mode filters to meet the required standard, which is stipulated for the leakage current. This leads to increased size, volume, and cost of the system. Also, both of these inverter configurations require a higher number of semiconductor devices, increasing the complexity of the implementation of the control scheme.

2.7 Three-Phase PV Inverter

Three-phase Multilevel Inverters (MLI) have become very popular in recent times due to several of their advantages such as improved harmonic performance, reduced power losses, etc. [101-105]. However, the conventional three-phase power inverters display the drawback of voltage oscillations in the common-mode voltage (CMV) [104]. The high-frequency transitions in the CMV cause leakage current through the parasitic capacitors, which exist between solar cells and the metallic structure of the panel. Apart from deteriorating the system

performance, the presence of leakage current causes unwanted effects such as electromagnetic interference (EMI) [106], lowered lifespan of PV panels [107], distortion of current, and safety issues [108] - [109]. Therefore, it is highly desirable to eliminate or reduce the CMV while designing the inverter. Such a design would reduce the size of the EMI filters and common mode chokes, which are generally required to meet the required safety standards. To this end, the focus of researchers is directed to minimize the ill effects of the CMV either by eliminating or reducing high-frequency transitions in the CMV. Mitigation of voltage transitions in the CMV with the aid of modulation strategies is more popular, as it does not require any additional switching devices or modification of grounding practices.

Complete elimination of the CMV is reported by Zhang *et. al.* [110]. This is achieved with the employment of a modulation strategy that utilizes only those voltage space vectors (SV), which result in the CMV with a value of zero (ZCMV). However, with this PWM scheme, the number of the voltage levels in the output is reduced due to the availability of a limited number of space vectors with ZCMV to implement the space vector modulation (SVM) technique [110]. Similar ZCMV-based SVM modulation schemes discussed in [111-113], underutilize the space vector locations making a three-level inverter appear as a two-level inverter. A similar ZCMV-SVM strategy given in [114] renders a 5-level inverter to operate as a 3-level inverter. Another major drawback with the ZCMV-SVM scheme is the reduction of the DC-link utilization, which increases the dc-input voltage requirement [110], [114] - [116]. This situation can be remedied by stepping up the PV input voltage using a conventional dc-dc boost conversion stage. However, the use of an extra power converter increases the number of components and reduces the overall efficiency and reliability of the power converter.

The single dc-source power circuit configuration introduced by Dagan *et al* [117] addresses the problem of underutilizing the dc-bus while resorting to the ZCMV technique. However, the number of semiconductors used in this power converter doesn't commensurate with the number of switching vectors. Thus, there arises a necessity to optimize the component count w.r.t the number of voltage levels obtained at the output with the power converter topology presented in [117]. In this context, Hota *et. al.* have derived a new MLI topology [108], wherein the component count is minimized by reducing the number of unused

SVs. However, this converter uses more dc-sources and the dc-bus utilization has further deteriorated. For PV applications, multiple isolated PV strings pose difficulties to implement the MPPT control.

The inverter configurations discussed in [118-119] employ additional semiconductor switches to decouple the PV source from the grid to restrict the voltage transitions in CMV. This technique is capable of reducing the leakage current by restricting the *dv/dt* in the CMV, which is achieved by reducing the amplitude of transitions in the PV parasitic voltage. However, the transitions in the common-mode voltage in these configurations are dependent on the input PV voltage and the switching frequency of the inverter. Thus, the leakage current increases further in high voltage or high-frequency applications.

A voltage-boosted three-phase inverter configuration [120] and its associated modulation strategy are derived in [121], which is capable of minimizing the transitions in the CMV. In this power converter, the compromised DC-link utilization is compensated by boosting the input voltage. However, the maximum limit of the boost factor in this converter is constrained by the value of the modulation index. Furthermore, this topology outputs only a two-level voltage waveform. The work presented in [122] extends this theme to derive a three-level output. However, the issues of the CMV and the leakage current are not addressed in this paper.

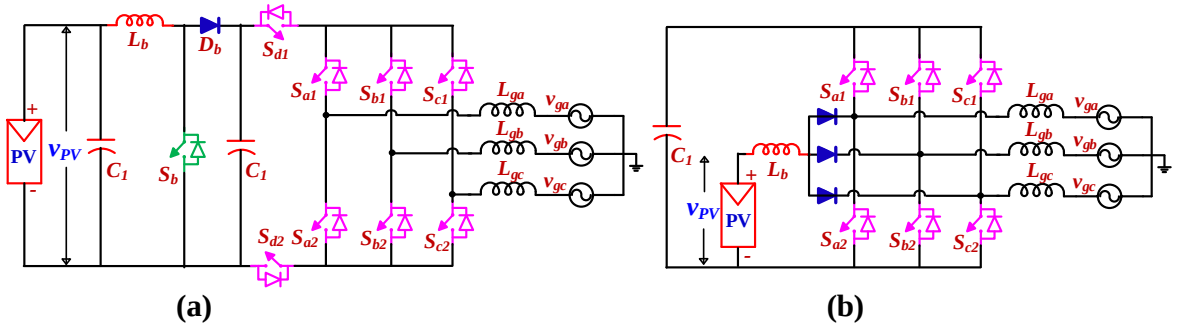


Figure 2.13: Three phase PV inverter configurations: (a) [119] (b) [120].

Chapter 3

Semi-Double Stage Integrated Seven-Level Boost Inverter

Chapter 3

Semi-Double Stage Integrated Seven-Level Boost Inverter

3.1 Introduction

The boost-converter-based photovoltaic systems (double-staged systems) have extensively been studied in the past for both grid-connected and standalone inverter applications, and have become quite popular. Apart from addressing the issue of incompatibility of PV voltage with the load-end voltage, this solution caters to the low-voltage problems caused by varying environmental conditions (such as partial shading) [126]. However, these circuit configurations reduce the overall efficiency and increase the ratings of the switching device for the boosting stage [127,75]. A partial charging technique of the DC-bus capacitor has been proposed in [128,129] to improve the efficiency of the boosting stage and alleviate the current stress. In this work, a seven-level (7L) inverter topology is proposed, which is configured with an asymmetrical charged DC bus capacitor and a polarity generator configuration. A high-frequency transformer is also used in this work to charge the DC bus capacitors with parallel processing of input PV power. Though this power converter is operable with a single PV source, it requires a boost converter at the input side of the converter. An improvised SC technique with a bi-directional buck-boost converter is proposed in [130]. In this work, a common ground transformerless inverter has been proposed to reduce the size of the capacitor and current stress in the switches. However, this topology achieves single-stage power conversion at the expense of multilevel operation. A novel configuration for voltage boosting in a single-stage power converter configuration is proposed in [50], which employs a buck-boost converter. A novel methodology for generating more voltage levels by charging the SC is introduced in this work. The leakage current is minimized by the employment of a modified DC-decoupling technique. However, the analysis of common-mode voltage (CMV) *dv/dt* transitions and leakage current are not reported in this work. Furthermore, the design and rating of the converter are also not analyzed.

This chapter presents a new integrated PV system, wherein a semi-double-staged voltage boosting network is fused into a seven-level MLI. The proposed MLI configuration employs two half-bridges (HBs) and one full H-bridge in its structure. Also, it contains a HERIC leg to mitigate the issue of the leakage current due to the parasitic elements of the PV panel. The advantage of the proposed integrated PV system is that it needs only one PV source and two symmetrical SCs to synthesize a seven-level output voltage waveform with unipolar PWM switching. Some unique features of the proposed inverter are mentioned below:

- This configuration contains an interlinking high DC voltage, which is about three times that of the input PV voltage.
- As the proposed PV system contains a single PV source, the implementation of MPPT algorithms is simplified.
- The proposed configuration exhibits a structural symmetry, which increases the redundancy in the switching state. This feature facilitates devising PWM schemes to achieve an inherent capability of balancing the voltage across the DC-link capacitors.
- Owing to the structural symmetry of the proposed power circuit configuration, it is possible to devise symmetrical PWM schemes. Hence, the power losses are evenly distributed amongst the power semiconductor switching devices.
- The proposed topology is capable of transferring nearly 36% of the total energy processed in single-stage conversion. The rest of the energy is equally shared between the two SCs, which is fed by an interleaved buck-boost converter.
- The single carrier-based implementation of the PWM scheme on a digital control platform is very much simplified for the proposed power converter. Furthermore, the PWM scheme described in this chapter achieves a seamless transition amongst various voltage levels present in the VSI. This PWM scheme can easily be extended for a higher number of voltage levels.
- The proposed inverter needs twelve switching devices to generate a 7L waveform. Of these twelve devices, six devices are switched at the fundamental frequency (50Hz), while other switches are switched at a high frequency in a given half-cycle. This ensures an overall reduction of switching power loss in the system.

Apart from achieving the aforementioned features of the proposed topology and the associated PWM technique, this chapter presents a detailed analysis of stray capacitor voltage, CMV, and leakage currents with the aid of switching theory. It is also shown that the PWM scheme employed in this work is capable of complying with the *VDE-0126-1-1[26]* standards. The simulation results and experimental results obtained from the laboratory prototype validate the mathematical analysis of the proposed topology and the associated PWM scheme.

3.2 Operation Principle of the Proposed Seven-level MLI

3.2.1 General Description

The schematic circuit of the proposed single PV source fed seven-level multilevel inverter is shown in Figure 3.1. The proposed configuration employs two SCs (C_1, C_3), one DC-link capacitor (C_2), twelve semiconductor switches, two high-frequency inductors (L_1, L_2), two filter inductors (L_{g1}, L_{g2}), and one filter capacitor (C_f). The resistance in the ground path is indicated by R_g. The variable v_g refers to the instantaneous grid voltage. The parasitic resistance and capacitance of the PV panels are denoted by R_p and C_p respectively in Figure 3.1. The currents through the high-frequency energy storage inductors are denoted by i_{L1} and i_{L2} respectively. The variables i_{xy}, i_f, i_g, *and* i_{leak} respectively represent the output current of the 7L MLI, the current flowing through the filter capacitor, the current injected into the grid (load current), and the induced leakage current flowing between the PV array and ground through the parasitic elements of PV panel.

Each SC (C_1, C_3) of the proposed configuration is energized through an interleaved buck-boost converter, which is constituted by two MOSFETs, two inductors, and two diodes. The SC C_1 is being charged through S_U, L_1, and D_1, whereas the capacitor C_3 is charged through S_L, L_2, and D_2. Both the SC C_1 and C_3 are being charged up to the same voltage level as that of the input PV voltage (V_{PV}). The proposed inverter configuration also contains four pairs of half-bridge legs (S_1, S_2), (S_3, S_4), (S_5, S_6), (S_7, S_8), and one bi-directional switch (S_9, S_{10}) which generates seven distinct levels in output voltage waveform. The devices in the pair S_1 and S_2 are switched complimentarily. Similarly, the devices in the pair S_3 and S_4 are also switched complementarily. In order to avoid the high switching frequency operation of these switches (S_1, S_2, S_3, S_4), the switching states of these switches are not altered during the

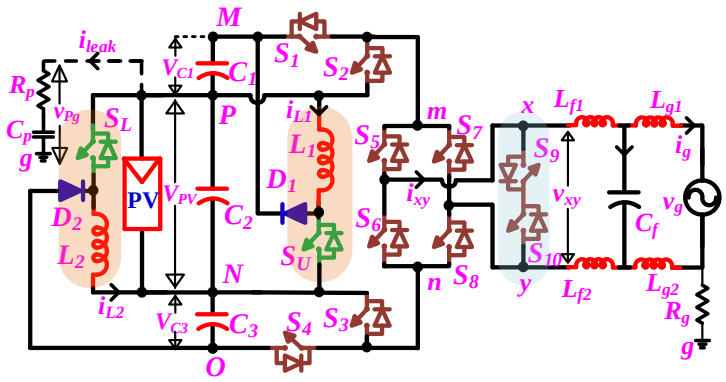


Figure 3.1: Circuit schematic for seven-level MLI with PV source and parasitic elements.

freewheeling state from the previous active switching state. These switch-pairs determine the voltage across the points 'm' and 'n' (i.e. v_{mn}). The H-bridge, which is constituted by switches (S_5, S_6, S_7, S_8), operates as a polarity generator for the output voltage. In addition, these switches are not switched in a complementary fashion to isolate the PV and grid in the freewheeling state.

3.2.2 Switching State for Different Modes of Operation

Switching states of individual devices to obtain various voltage levels in the proposed circuit configuration are enumerated in Table 3.1. The equivalent circuit of the proposed inverter for each level of operation is shown in Figures 3.2, 3.3, 3.4, 3.5. Corresponding to the output voltage levels $\pm 3V_{PV}$, $\pm 2V_{PV}$, $\pm V_{PV}$, and 0, four distinct modes of operation exist in the proposed power circuit. The operation of the power circuit in these four modes is described in the following paragraph.

Table 3.1: Switching states for Respective Output Voltage Levels.

Output Voltage v_{xy}	**S_1**	**S_2**	**S_3**	**S_4**	**S_5**	**S_6**	**S_7**	**S_8**	**S_9**	**S_{10}**
$+3V_{PV}$	1	0	0	1	1	0	0	1	1	0
$+2V_{PV}$	1	0	1	0	1	0	0	1	1	0
$+2V_{PV}$	**0**	**1**	**0**	**1**	**1**	**0**	**0**	**1**	**1**	**0**
$+V_{PV}$	0	1	1	0	1	0	0	1	1	0
0	0	1	1	0	0	0	0	0	1	0
0	0	1	1	0	0	0	0	0	0	1
$-V_{PV}$	0	1	1	0	0	1	1	0	0	1
$-2V_{PV}$	**1**	**0**	**1**	**0**	**0**	**1**	**1**	**0**	**0**	**1**
$-2V_{PV}$	0	1	0	1	0	1	1	0	0	1
$-3V_{PV}$	1	0	0	1	0	1	1	0	0	1

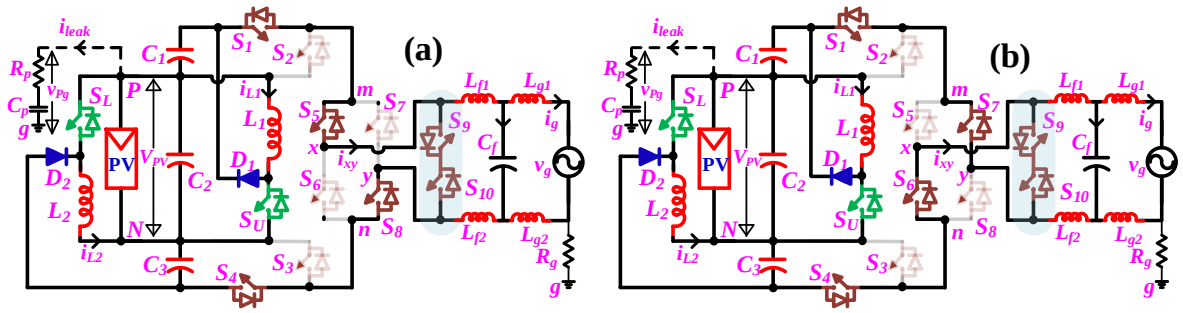


Figure 3.2: In Mode I operation, the proposed configuration produces: (a) v_{xy} = +3V_{PV} in positive half-cycle (b) v_{xy} = -3V_{PV} in negative half-cycle.

Mode I: The proposed power circuit exhibit this mode of operation, when both the SC (C_1 and C_3) is charged up to V_{PV} and switches S_1 and S_4 are turned ON. Due to this switching operation 3V_{PV} appears across the terminals 'm' and 'n' (i.e. v_{mn} =3V_{PV}). Then by turning on either the pair (S_5, S_8) or the pair (S_6, S_7) from the polarity generator circuit, it is possible to impress +3V_{PV} or -3V_{PV} across the load respectively as shown in Figure 3.2 (a), (b).

Mode II: In this mode of operation, the voltage across the terminal 'm' and 'n' is 2V_{PV} (i.e. v_{mn} =2V_{PV}). This can be achieved by energizing any one of the SCs between C_1 and C_3 and turning ON the associated switch (S_1 or S_4). So, out of these redundancies, SC C_3 is energized during the positive half-cycle whereas C_1 is energized during the negative half-cycle, in order to equalize the utilization over a fundamental period. Then by turning on either the pair (S_5, S_8) or the pair (S_6, S_7) from the polarity generator circuit, it is possible to generate +2V_{PV} or -2V_{PV} across the load respectively as shown in Figure 3.3 (a), (b).

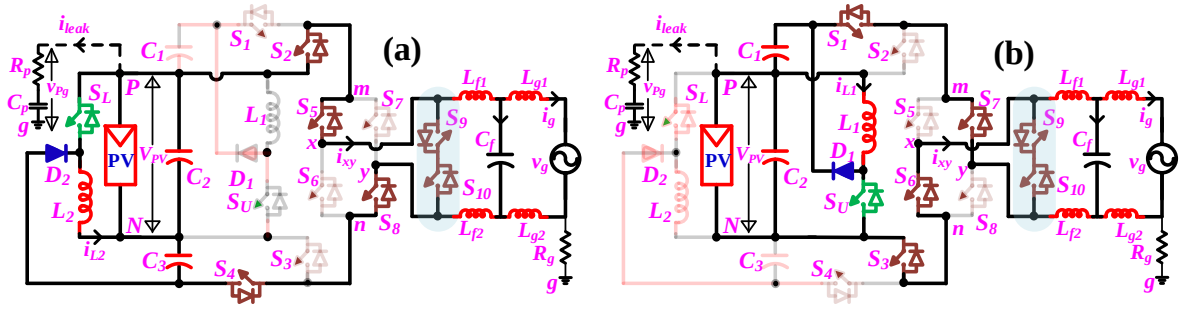


Figure 3.3: In Mode II operation, the proposed configuration produces: (a) v_{xy} = +2V_{PV} in positive half-cycle (b) v_{xy} = -2V_{PV} in negative half-cycle.

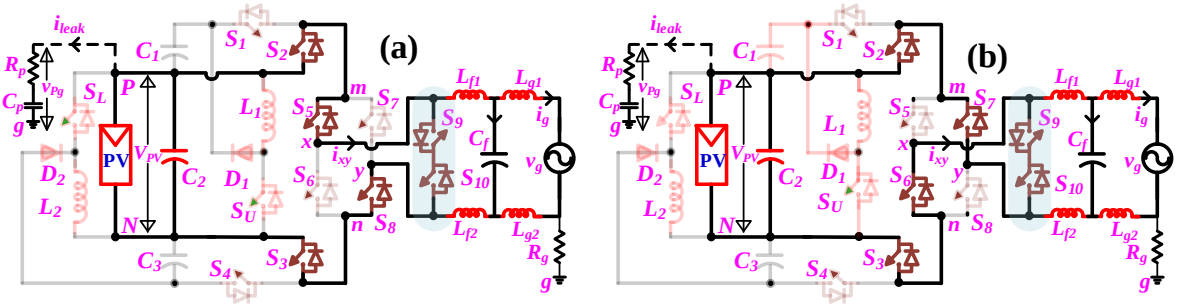


Figure 3.4: In Mode III operation, the proposed configuration produces: (a) v_{xy} = +V_{PV} in positive half-cycle (b) v_{xy} = -V_{PV} in negative half-cycle.

Mode III: In this mode of operation, both of the switches S_1 and S_4 are turned OFF as neither of the SCs are utilized. Hence, V_{PV} appears across the terminals 'm' and 'n' (i.e. v_{mn} =V_{PV}). Thereafter, either the pair (S_5, S_8) or the pair (S_6, S_7) from the polarity generator circuit is turned ON to generate +V_{PV} or -V_{PV} across the load as shown in Figure 3.4 (a), (b).

Mode IV: The most important feature in this mode of operation is the isolation or disconnection between the PV source and the grid. If the freewheeling state is obtained by turning on the devices S_5 and S_7, there exists a path of conduction between the positive terminal of PV and the freewheeling point through the body diode of S_2. A similar conduction path exists from the PV negative terminal due to the body diode of S_3 (when freewheeling is affected by turning on the devices S_6 and S_8). Lack of isolation between the PV source terminals and the grid leads to high-frequency voltage transitions in the total common-mode voltage (i.e. across PV positive terminal and load ground terminal) [50]. Therefore, the isolation is achieved by turning off all of the switches in the polarity generator circuit as shown in Figure 3.5. In order to provide the freewheeling path for the inductive current component during each ZERO state transition, either S_9 or S_{10} switch is turned ON during the positive half-cycle and negative half-cycle respectively. Due to this switching action, the terminals of the PV panel are isolated from the grid terminals, which employs a high impedance path for leakage current.

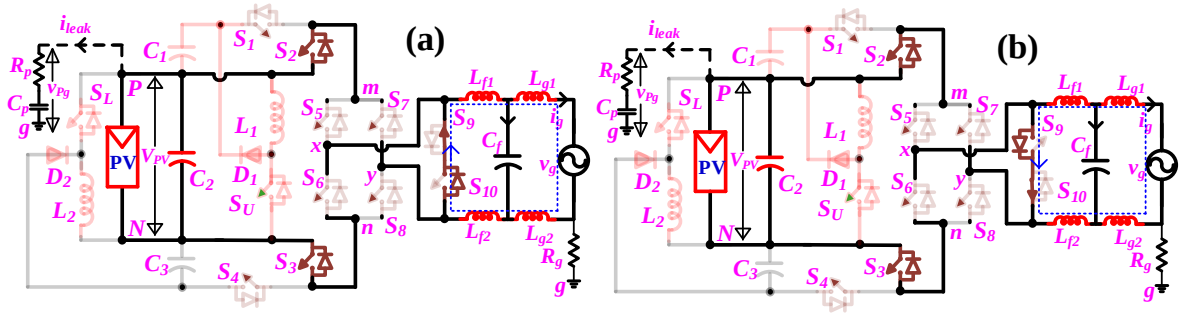


Figure 3.5: In Mode IV (Freewheeling State) operation, the proposed configuration produces: v_{xy} = 0 in (a) positive half-cycle, (b) negative half-cycle.

3.3 Modulation Strategy and Control Scheme

As mentioned in the section 3.2.1, the proposed system requires a single PV source and two SCs (C_1, C_3) to synthesize the 7L output voltage waveform. The SCs are energized/charged through the front-end interleaved buck-boost converter, which consisted of two switches (S_U, S_L), two inductors (L_1, L_2), and two diodes (D_1, D_2), with the same voltage magnitude as that of the input PV voltage. The transitions in the output voltage always occur between zero voltage level and a specific voltage level depending on modes of operation as discussed earlier. This switching action allows the configuration to eliminate the switching-frequency transitions in the total common-mode voltage v_{Pg}. This section describes the control scheme for charging the SCs, the logical implementation of the modulation strategy, and the analysis of the total common-mode voltage v_{pg}.

3.3.1 The Control Scheme for The Charging of SCs

An interleaved-based PWM technique is employed for the front-end buck-boost converter to extract power symmetrically from the PV source. The implementation of the control scheme and the PWM generation is shown in Figure 3.6 (a). It can be observed that the carrier signals (v_{carr1}, v_{carr2}) are phase-shifted by π radians to obtain interleaved PWM pulses. The capacitors (C_1 and C_3) are charged in alternative switching half cycles, which reduce the peak current stress on the PV source irrespective of the loading conditions. The duty factors for the lower and upper sections of boosting stages are respectively denoted as d_{LP} and d_{UP}. To implement effective voltage control over the SCs, the boundary condition of CCM-DCM has been chosen to design the inductors and capacitors for the converter [132].

Assuming, the converter is operating in critical conduction mode (DCM-CCM), the voltage across the capacitor can be expressed as follows:

$$V_{C1} = \frac{d_{UP}}{1-d_{UP}} V_{PV} \tag{3.1}$$

$$V_{C3} = \frac{d_{LP}}{1-d_{LP}} V_{PV} \tag{3.2}$$

A simple voltage mode-based closed-loop control scheme is implemented with a linear PI regulator to maintain the same voltage at the SCs C_1 and C_3. The output of the PI regulator is limited to such a value that, the maximum value for both of the duty ratios (i.e. d_{LP} and d_{UP}) is 0.5. (Figure 3.6 (b)). This scheme improves the dynamic response of the capacitor voltages at various loading conditions of the inverter.

3.3.2 Generation of Voltage Levels

To generate the switching pulses for the inverter, a fundamental modulation wave with a modulating factor of m_a is considered as per the following eqn:

$$v_m = m_a \sin \omega t \tag{3.3}$$

As a single carrier-based PWM scheme is adopted, it is required to modify the modulation signal to synthesize a 7L output. Depending on the modulating factor (m_a), the modulating signal is modified in order to achieve the generation of a 7-level output voltage. The modified

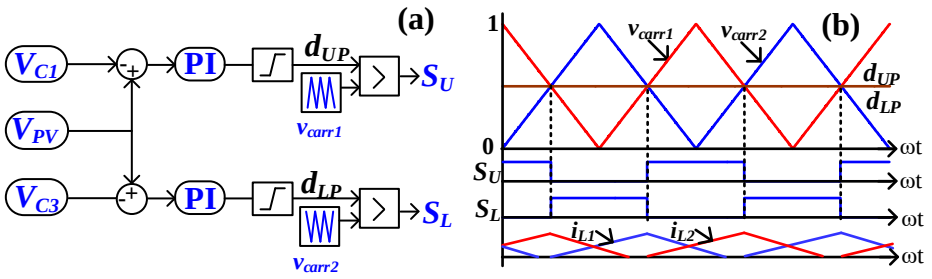


Figure 3.6: (a) Closed-loop voltage control scheme, (b) Phase–shifted carrier employed for front-end buck-boost converter.

reference signals are chosen, based on the mode of operation described in the previous section, as follows:

Mode III: Switching actions between V_{PV} to 0.

$$v_{ref1} = v_m \quad \text{when} \quad 0 \le v_m < \frac{1}{3} \tag{3.4}$$

Mode II: Switching actions between $2V_{PV}$ to 0.

$$v_{ref2} = \frac{v_m}{2} \quad \text{when} \quad \frac{1}{3} \le v_m < \frac{2}{3} \tag{3.5}$$

Mode I: switching actions between $3V_{PV}$ to 0.

$$v_{ref3} = \frac{v_m}{3} \quad \text{when} \quad \frac{2}{3} \le v_m < 1 \tag{b(3.6)}$$

The modified reference signal (v_{ref_mod}) is obtained by concatenating individual reference signals as given in eqns (3.4), (3.5), (3.6) and shown in Figure 3.7.

$$v_{ref\_mod} = v_{ref1} + v_{ref2} + v_{ref3} \tag{3.7}$$

The modified reference signal is compared with the symmetrical triangular carrier wave (v_{tri}) to achieve the 7L output of the proposed inverter. In order to generate the switching pulses for switches S_9 and S_{10}, the fundamental modulation wave (v_m) is compared with zero to identify the duration of the positive and negative half cycle. In other words, S_9 is turned on throughout the positive half-cycle, while S_{10} is turned on throughout the negative half-cycle. Table 3.2 shows the relationship between the modulation index (m_a) and the voltage levels in the output of the proposed inverter. The implementation of the modulation technique for the proposed inverter is shown in Figure 3.8. The reference variables rv_1, rv_2, and the gains g_1, g_2, which are used for the implementation of the control scheme, are also defined in Table 3.2. Whenever the magnitude of the modified reference signal is greater than that of the carrier

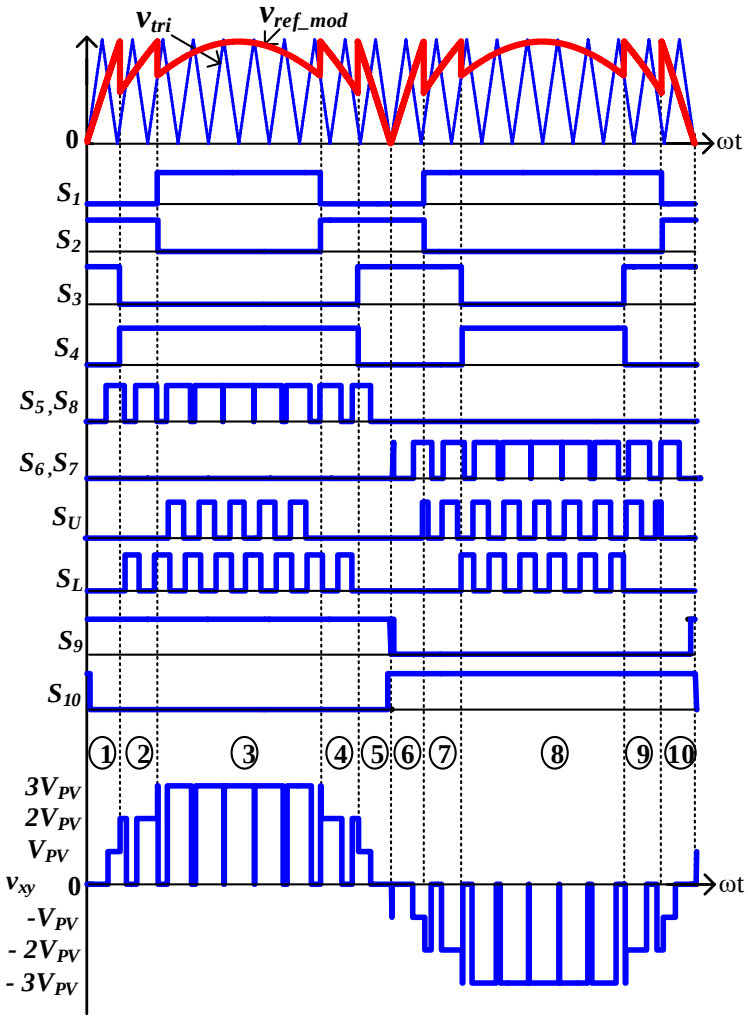


Figure 3.7: Synthesis of the modified reference signal (v_{ref_mod}) and PWM generation for the inverter switches.

the switching pattern corresponding to the voltage level, determined by the mode of operation (eqns (3.4), (3.5), (3.6)), is generated (Table 3.1). It can be observed that the switching pattern is chosen in such a way that, only two devices toggle their switching state in any given half-cycle, leading to the reduction of switching power losses in semiconductor devices.

Table 3.2: Factors at Different Modulation Index

Operation	Modulation limits	rv_1	rv_2	g_1	g_2
Seven-level	$1 < m_a \leq 0.67$	0.33	0.67	0.33	0.5
Five-level	$0.67 < m_a \leq 0.33$	0.5	1	0.5	0
Three-level	$0.33 < m_a \leq 0$	1	1	0	0

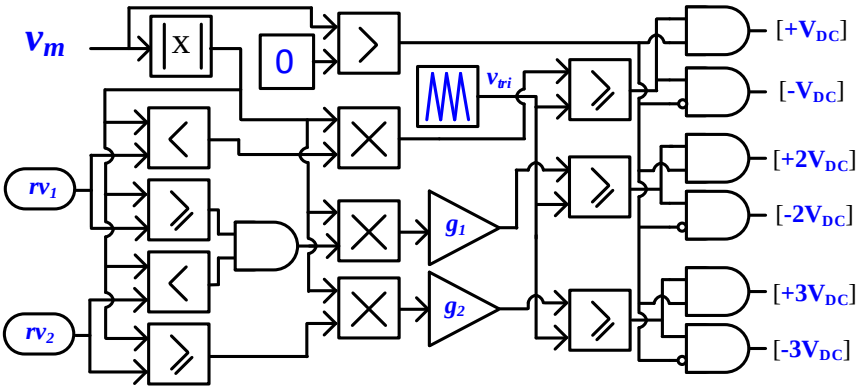


Figure 3.8: Logical implementation of the modified-modulation signal from fundamental modulation signal (v_m).

The block diagram of the control scheme for the grid-tie operation of the proposed inverter configuration is shown in Figure 3.9. In this scheme, P&O based conventional MPPT algorithm [60, 133] is considered. The reference voltage (V_{PV}^*) and the available PV power (P_{PV}) are further processed by the power regulator block, which outputs the reference power, which can be delivered to the grid. An instantaneous power calculator, based on the PQ-control [134], is employed to determine the power being injected into the grid. These two parameters are further processed by the grid-current reference generator, which provides the magnitude of the reference grid-current. To obtain the grid-synchronization a single-phase SOGI phase-locked loop (PLL) [135] is employed. Further, a proportional resonant (PR) control is used to control the grid current [136,51-77] w.r.t the reference grid-current. The PR current controller outputs the modulation signal (v_m), which is given to the logical implementation of the proposed PWM technique as given in Figure 3.8.

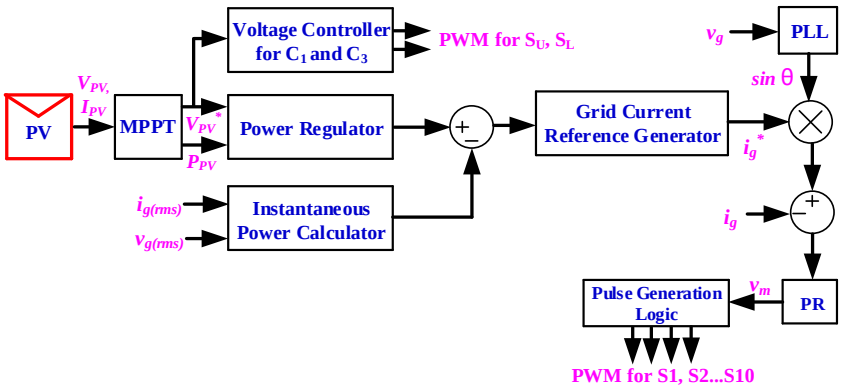


Figure 3.9: Block diagram of the control scheme for the proposed seven-level inverter configuration in grid-tie mode.

3.3.3 Analysis of Power Utilization Ratios

The proposed configuration processes the PV power either with only single-stage or with double-stage conversion. In the double-stage conversion mode, a second converter is augmented to the PV source. The second converter is an interleaved buck-boost converter. In order to design the second converter instantaneous power utilization ratios (IPUR) are derived for the PV source and each SC. The extracted power from the PV source and the SCs are derived by the following equations:

$$P_{C1} = S_1 v_{ref\_mod} V_{C1} i_g \tag{3.8}$$

$$P_{C3} = S_4 v_{ref\_mod} V_{C3} i_g \tag{3.9}$$

$$P_S = v_{ref\_mod} V_{PV} i_g \tag{3.10}$$

Now, the IPUR is the ratio of power extracted from a given particular SC or the PV source to the total power processed through the inverter. The IPUR for the PV source and the SCs (C_1 and C_3) is represented by P_{S_ratio} , P_{C1_ratio} and P_{C2_ratio} respectively. The relation between these variables is as follows,

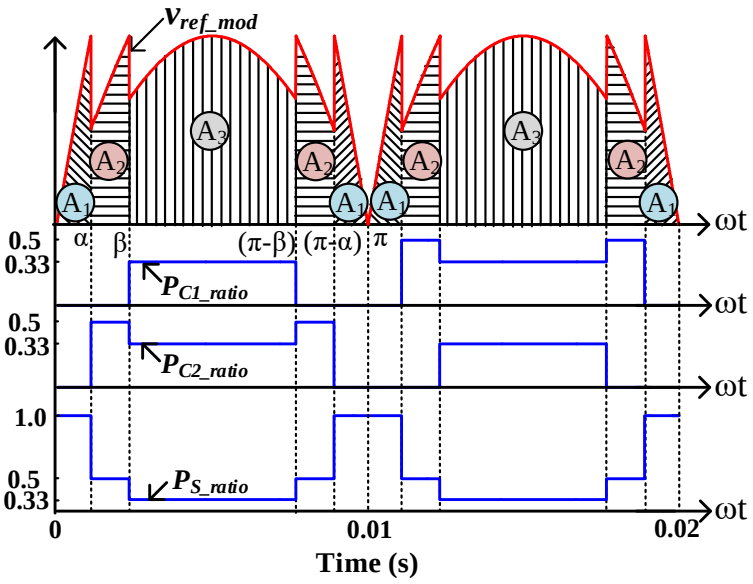


Figure 3.10: Instantaneous power utilization ratios for PV source and SCs (C_1 & C_3).

$$P_{C1\_ratio} = \frac{P_{C1}}{P_{C1} + P_{C3} + P_s} \tag{3.11}$$

$$P_{C3\_ratio} = \frac{P_{C3}}{P_{C1} + P_{C3} + P_s} \tag{3.12}$$

$$P_{S\_ratio} = \frac{P_S}{P_{C1} + P_{C3} + P_s} \tag{3.13}$$

The IPUR for PV source (P_{S_ratio}) and the SCs C_1 and C_3 (P_{C1_ratio}, P_{C3_ratio}) are plotted with respect to time in Figure 3.10. It can be observed that the peak power utilization ratio of the SCs are only 50% of the total power demand. Thus, it is evident that the upper and lower section of the interleaved buck-boost converter is required to be designed for only 50% of the full load rating of the inverter.

In order to establish the energy utilization factor mathematically among the PV source and the SC, the total energy for a given fundamental cycle is calculated as follows (eqn. 3.14):

$$E_T = 2 \times \int_0^{\pi} (V_{C1} + V_{C2} + V_{C3}) \times i_g \times d(\omega t) \tag{3.14}$$

$$i_g = I_m \sin(\omega t - \phi) \tag{3.15}$$

where, $V_{C1,}$ and V_{C3} are voltages across the SCs (C_1 and C_3), V_{C2} is the voltage across the PV source and i_g is the load current.

As mentioned, earlier the extracted PV energy is either directly delivered to the load (single-stage operation) or via the energized SCs C_1 and C_3 (double-stage operation). The symbol E_S demotes the energy delivered to the load in the single-stage operation. Similarly, E_{C1} and E_{C3} respectively denote the energies transferred to the load from the SCs C_1 and C_3. The total energy extracted from the PV source is transferred to load either through single-stage operation (E_s) or through SCs (E_{C1} & E_{C3}). The expression for total energy can be as follows,

$$E_T = \int (V_{C1}) \times i_g \times d(\omega t) + \int (V_{C2}) \times i_g \times d(\omega t) + \int (V_{C3}) \times i_g \times d(\omega t) \quad (3.16)$$

$$E_T = E_{C1} + E_{C3} + E_s \quad (3.17)$$

It is assumed that the SCs (C_1, C_2) are charged to the same voltage as that of the input PV voltage. i.e.

$$V_{C1} = V_{C2} = V_{C3} = V_{PV} \quad (3.18)$$

From Figure 3.10 it can be observed that to determine E_{C1}, E_{C3}, E_S, the area under the modified modulation curve is to be determined. The relation between the area (E_{A1}, E_{A2}, E_{A3}) and the (E_{C1}, E_{C3}, E_S) are as follows,

$$E_S = 2 \times (2E_{A1} + 2E_{A2} + E_{A3}) \quad (3.19)$$

$$E_{C1} = (E_{A3}) + (2E_{A2} + E_{A3}) \quad (3.20)$$

$$E_{C3} = (2E_{A2} + E_{A3}) + (E_{A3}) \quad (3.21)$$

The energy under the sections A_1, A_2, and A_3 can be calculated as per the following equation:

$$E_{A1} = \int_0^{\alpha} V_{PV} \times (m_a \sin(\omega t)) \times (I_m \sin(\omega t)) d(\omega t) \quad (3.22)$$

$$E_{A2} = \int_{\alpha}^{\beta} V_{PV} \times (\frac{m_a}{2} \sin(\omega t)) \times (I_m \sin(\omega t)) d(\omega t) \quad (3.23)$$

$$E_{A3} = \int_{\beta}^{(\pi-\beta)} V_{PV} \times (\frac{m_a}{3} \sin(\omega t)) \times (I_m \sin(\omega t)) d(\omega t) \quad (3.24)$$

The average energy utilization factor for the PV source (E_{Sf}) and each SCs (E_{C1f} & E_{C3f}) can be derived using eqns.(3.14)-(3.24), as follows:

$$E_{C1f} = \frac{E_{C1}}{E_T} \times 100\% = 31.5\% \tag{3.25}$$

$$E_{C3f} = \frac{E_{C3}}{E_T} \times 100\% = 31.5\% \tag{3.26}$$

$$E_{Sf} = \frac{E_S}{E_T} \times 100\% = 37\% \tag{3.27}$$

From these numerical values, it is evident that 37% of energy is transferred directly to the load through single-stage conversion. The rest of 63% is transferred through the double stage conversion. The 63% double stage power transfer is shared equally between the two SCs. Though the peak power handled by *each* of the SC is 50% (see Figure 3.10), the average energy transferred to the load is 31.50 % of the total energy. In contrast, in the case of the conventional DC-DC converter-based boosting method, the total PV power has to be processed through the DC-DC conversion stage. This shows that the structure of the proposed power circuit configuration inherently displays the capability to process energy efficiently while boosting the input PV voltage. Moreover, it can be observed that the values of both E_{C1f} and E_{C3f} are the same. It implies that the average energy transferred in a given fundamental period through the SCs (C_1 and C_3) is the same. This helps in the self-balancing of the SCs and it enables the structure to be operated in an open-loop condition in fixed load condition. This feature achieves the voltage balancing of the SCs, alleviating the burden on the closed-loop system, which is described earlier.

3.3.4 Analytical derivation of total common-mode voltage

Now, the generation of leakage current in parasitic elements of PV panel, due to the high-frequency transitions in the total common-mode voltage (v_{Pg}), is one of the significant issues in PV inverter configurations. To address the issue of leakage current in the proposed inverter, a modified modulation technique, described in the previous section, is employed. The nature of the leakage current can be analysed mathematically by deriving an expression for the total common-mode voltage with respect to the terminal points M, P, N, and O as

shown in Figure 3.1. It may be noted that the PV source is connected across points P and N (Figure 3.1). Therefore, to analyse the leakage current through the PV panel, the total common-mode voltage v_{Pg} is derived mathematically. The SS_x represents the switching function for the switch S_x with (S_1, S_2, S_3 .....S_{10}). The value of SS_X is "1" or "0" with respect to the switching state of S_X (turned ON or OFF), respectively. Applying the superposition theorem and using switching functions the voltage, v_{Pg} (Figure 3.1) can be expressed as follows:

$$v_{Pg} = SS_1 v_{Pg1} + SS_2 v_{Pg2} \tag{3.28}$$

where v_{Pg1} and v_{Pg2} are the voltages at the P terminal of the PV source with respect to the ground 'g' when S_1 and S_2 are turned on respectively. The following paragraph presents the analysis pertaining to the switching modes of switch S_1.

Case (i): When S_1 is turned ON:

In this case, from the following eqn. it is noted that it is required to evaluate v_{Mg1} to derive an expression for v_{Pg1},

$$v_{Pg1} = v_{Mg1} - V_{PV} \tag{3.29}$$

Similarly, other terminal points equations (v_{Og1}, v_{Ng1}) can also be expressed in terms of v_{Mg1} as follows,

$$v_{Og} = v_{Mg1} - 3V_{PV} \tag{3.30}$$

$$v_{Ng} = v_{Mg1} - 2V_{PV} \tag{3.31}$$

The inverter output terminal voltage v_{xg} and v_{yg} are also derived using the switching function analysis. From Figure 1, v_{xg} and v_{yg} are expressed in terms of v_{Mg1}, v_{Ng1}, v_{Og1} as follows,

$$v_{xg} = SS_1 SS_5 v_{Mg1} + (1 - SS_3) SS_6 v_{Og} + SS_3 SS_6 v_{Ng} \tag{3.32}$$

$$v_{yg} = SS_1 SS_7 v_{Mg1} + (1 - SS_3) SS_8 v_{Og} + SS_3 SS_8 v_{Ng} \tag{3.33}$$

Using KCL in the circuit shown in Figure 3.11 (a), the relation between v_{xg}, v_{yg} and grid voltage v_g can be expressed as follows,

$$v_{xg} + v_{yg} = v_g \tag{3.34}$$

Now, substituting the v_{xg}, v_{yg} expression (eqn. (3.32) and (3.33)) into the above expression(eqn. 3.34), and simplifying,

$$v_{Mg1} = \frac{v_g + 3V_{PV}(SS_6 + SS_8) - V_{PV}SS_3(SS_6 + SS_8)}{SS_1SS_5 + SS_1SS_7 + (SS_6 + SS_8)} \tag{3.35}$$

The voltage v_{Pg1} is obtained by substituting v_{Mg1} (eqn. (3.35)) into eqn. (3.29):

$$v_{Pg1} = \frac{v_g + 3V_{PV}(SS_6 + SS_8) - V_{PV}SS_3(SS_6 + SS_8)}{SS_1SS_5 + SS_1SS_7 + (SS_6 + SS_8)} - V_{PV} \tag{3.36}$$

Case (ii): When S_1 is turned OFF:

In this case, the expressions for the voltages in terminal points (N, O) v_{Ng1} and v_{Og1} are expressed as follows,

$$v_{Og} = v_{Pg2} - 2V_{PV} \tag{3.37}$$

$$v_{Ng} = v_{Pg2} - V_{PV} \tag{3.38}$$

Similarly, the inverter output terminal voltages can be expressed as,

$$v_{xg} = (1-SS_1)SS_5v_{Pg2} + (1-SS_3)SS_6v_{Og} + (1-SS_3)SS_6v_{Ng} \tag{3.39}$$

$$v_{yg} = (1-SS_1)SS_7v_{Pg2} + (1-SS_3)SS_8v_{Og} + (1-SS_3)SS_8v_{Ng} \tag{3.40}$$

Similarly, from eqns. (3.34), (3.37), (3.38), (3.39), (3.40), and (3.41) one obtains,

$$v_{Pg2} = \frac{v_g + 2V_{PV}(SS_6 + SS_8) - V_{PV}SS_3(SS_6 + SS_8)}{(1 - SS_1)(SS_5 + SS_7) + (SS_6 + SS_8)} \qquad (3.41)$$

Substituting v_{Pg1}, v_{Pg2} (eqn. (3.36) and (3.41)) in the eqn. (3.28), the total common-mode voltage can be obtained. Besides that, the CMV can be calculated from the following eqn.,

$$v_{CMV} = (v_{xg} + v_{yg})/2 \qquad (3.42)$$

CMV and the total common-mode voltage are simulated using MATLAB. The following parameters are used for simulating the equations: (a) frequency of carrier = 1 kHz, (b) grid frequency = 50 Hz. In simulation studies, the frequency of the carrier wave was restricted to 1 kHz, to facilitate easy visualization of the discontinuities associated with the undefined states in total common-mode voltage (v_{Pg}) *and* common-mode voltage (v_{CMV}). The total common-mode voltage (v_{Pg}) and the CMV (v_{CMV}) are respectively shown in Figure 3.11 (c) and (d) for two grid cycles and the undefined states are encircled with red color. The voltage transitions in the total common-mode voltage and the CMV for different switching combinations are also tabulated in Table 3.3. It can be observed from Figure 3.11 (c), (d) that the isolation between the grid and the PV module during the freewheeling state results in a discontinuity in the total common-mode voltage and CMV waveform. The discontinuities observed in the total common-mode voltage and CMV are due to the undefined values, arising out of the division by zero, within the simulation process. However, in practical circuits, the total common-mode voltage and CMV are continuous and these undefined values would be the same as obtained in the previous active state. Since there is no direct connection between the PV source terminals and the grid terminals, the PV terminal points (nodes P, N) float.

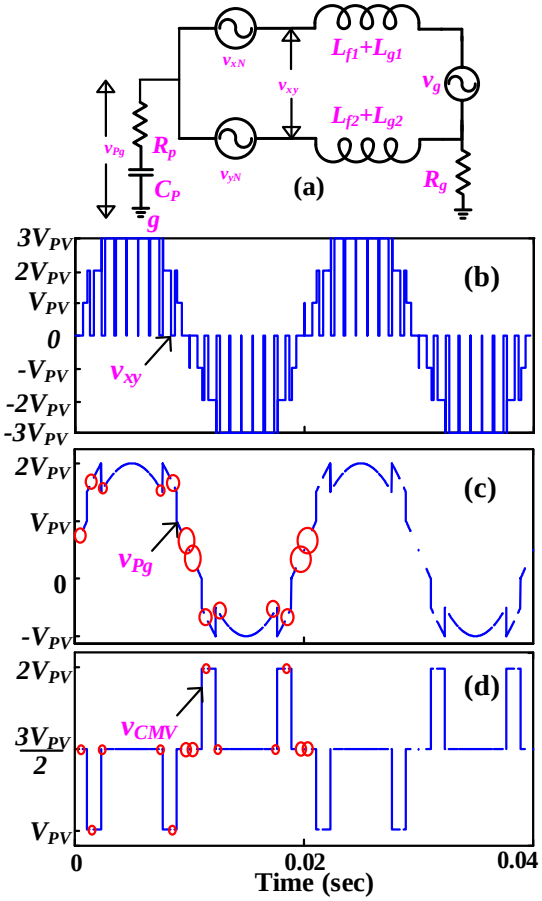


Figure 3.11: (a) Equivalent common-mode circuit of the inverter, Analytical waveforms (b) output voltage, (c) total common-mode voltage (TCMV), and (d) common-mode voltage (CMV).

Hence, they are not affected by any high-frequency voltage transitions. From Figure 3.11 (c), it is evident that the sinusoidal total common-mode voltage is over-ridden by four spikes (two spikes during each half-cycle). As the spikes display identical geometrical properties and symmetry, the moving average of the total common-mode voltage remains sinusoidal. This leads to the effective reduction of leakage current, as the PV-array capacitance offers a high impedance to low-frequency transitions. It can also be observed from Table 3.3 that, the low-frequency transitions among any two different voltage levels (in both terminal and CMV) is $V_{PV}/2$. However, the total DC-link voltage is $3V_{PV}$. Therefore, it can be inferred that the voltage transitions in both CMV and total common-mode voltage are *1/6*th of the total DC-link voltage. This leads to the complete elimination of switching frequency transitions as well as the reduction in the low-frequency transitions (compared to most the conventional

Table 3.3: Total Common-mode Voltage and CMV obtained for all Switching States

Region	v_{xy}	S_1	S_3	S_5, S_8	S_6, S_7	S_9	v_{Pg}	v_{CMV}
1	*0*	0	0	0	0	1	undefined	undefined
	V_{PV}	1	1	0	1	1	$\frac{V_{PV}}{2}+\frac{e_g}{2}$	$\frac{3V_{PV}}{2}$
2	*0*	0	0	0	0	1	undefined	undefined
	$2V_{PV}$	1	1	0	0	1	$V_{PV}+\frac{e_g}{2}$	V_{PV}
3	*0*	0	0	1	0	1	undefined	undefined
	$3V_{PV}$	1	1	1	0	1	$\frac{V_{PV}}{2}+\frac{e_g}{2}$	$\frac{3V_{PV}}{2}$
4	*0*	1	1	1	0	0	undefined	undefined
	$-V_{PV}$	1	0	1	0	0	$\frac{V_{PV}}{2}+\frac{e_g}{2}$	$\frac{3V_{PV}}{2}$
5	*0*	1	1	0	1	0	undefined	undefined
	$-2V_{PV}$	1	0	0	1	0	$\frac{e_g}{2}$	$2V_{PV}$
6	*0*	1	1	1	1	0	undefined	undefined
	$-3V_{PV}$	1	0	1	1	0	$\frac{V_{PV}}{2}+\frac{e_g}{2}$	$\frac{3V_{PV}}{2}$

modulation technique). As a consequence, effective suppression of leakage current occurs, which is well below the standard mentioned by VDE-0126-1-1, due to the high impedance offered by the capacitive parasitic elements to the low-frequency stray capacitor voltage. Moreover, as the proposed system does not require any extra components such as a common mode filter, choke, etc., the size and efficiency of the proposed inverter are also optimized.

Now, the equivalent impedance for the common-mode circuit of the proposed inverter configuration can be written [132] as follows,

$$Z_{CM} = 0.5s(L_{g1} + L_{g2}) + R_g + R_P + \frac{1}{sC_P} \tag{3.43}$$

In the present design, For, the reference design the following parameters are considered: (a) power rating (P_{rated}) = 1 kW, (b) switching frequency (f_{sw}) = 20 kHz, (c) modulation frequency (f_m) = 50 Hz, (c) input PV voltage (V_{PV}) = 133 V, (d) total boosted DC-link voltage ($V_{DC\text{-}link}$) =400 V and (d) ground resistance R_g = 10 ohm. For the effective elimination of the switching harmonics, the LC filter is designed based on the procedure described in [136], which deduces C_f = 1.15 µF and (L_{g1}= L_{g2}=) 2.5 mH. The following transfer function expresses the relationship between the excitation voltage (stray capacitor voltage) and the leakage current:

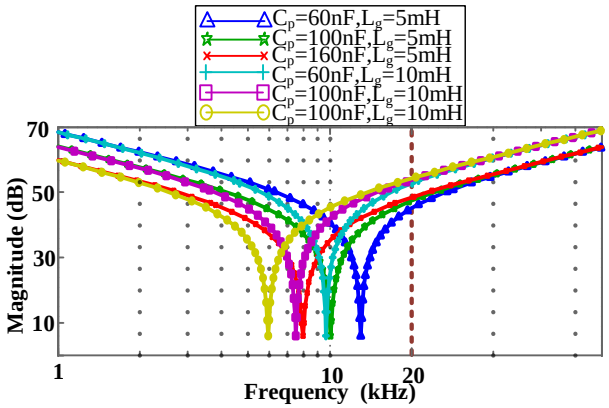


Figure 3.12: : Magnitude bode plot of the common-mode impedance with various combinations of parasitic elements of the PV panel.

$$i_{leak}(s) = \frac{v_{Pg}(s)}{Z_{CM}(s)} \tag{3.44}$$

where Z_{CM} is the equivalent impedance for the common-mode circuit of the proposed inverter configuration [132],

In order to minimize the effect of resonance on the leakage current, the first measure is to decrease the high-frequency transitions in the excitation voltage (i.e. v_{Pg}) of the resonant circuit. In this chapter, the high-frequency component across the parasitic capacitor is reduced by employing the proposed modulation strategy as shown in Figure 3.11. The magnitude bode plot of Z_{CM} is shown in Figure 3.12 for different combinations of parasitic capacitance and grid filter inductor L_g ($=L_{g1}+ L_{g2}$). It is observed that the magnitude of Z_{CM} increases consistently at higher frequency points beyond the resonance frequency of the common mode network (f_{ZCM}). This indicates that when the proposed 7-level inverter is switched at a frequency more than f_{ZCM} , the leakage current is well suppressed. Hence, the optimal switching frequency for the inverter can be chosen from the following inequality,

$$f_m << f_{ZCM} << f_{sw} \tag{3.45}$$

Thus, in order to avoid the resonance phenomenon, the resonant frequency (f_{ZCM}) must be much higher than the fundamental frequency (f_m) and the same time much lower than the first switching sideband to avoid excessive i_{leak} [132, 137].

3.4 Design Equations

3.4.1 Interleaved Buck-Boost Converter Design

The front-end buck-boost stage inductor L_i (i for 1, 2) is designed to operate at the boundary of the conduction mode at rated power output. As per the analysis given in section 3.3.1, the interleaving parts of the front-end converter process a fraction of the total power. The inductors for each interleaving section of the front-end boost converter can be selected as,

$$L_{1,2} = \frac{(1-D_{\max})^2}{2 f_{swb}} \frac{V_{PV}^2}{k_f P_o} \tag{3.46}$$

where D_{max} represents the maximum duty cycle of switches corresponding to each interleaving part of the converter, k_f represents the proportion of the output power processed through the corresponding interleaving part, P_o represents the total output power of the proposed inverter configuration. Besides that, the instantaneous power difference between the front-end side and the inverter side is supplied by the DC-link capacitors (C_1-C_3). Thus, to meet the requirements of various standards, the ripple of the DC-link voltage is required to be maintained below a specific value. The value of the DC-link capacitors [138] can be obtained as,

$$C_{1,2,3} = \frac{k_f P_o}{2\omega_{grid} V_{CX} \Delta V_{CX}} \tag{3.47}$$

where ω_{grid} is the angular frequency of the grid, V_{CX} is the mean voltage across the respective capacitors, and ΔV_{CX} is the amplitude of the voltage ripple.

3.4.2 Design of LCL Filter

Among various filter structures, the LCL filter displays an excellent harmonic suppression capability [139-140]. The LCL filter is used as an interfacing element between the grid and the proposed power converter. L_f refers to the converter-side inductor, L_g is the grid-side inductor and, C_f refers to the capacitor in the LCL filter structure. To suppress the inherent resonant peak of the LCL filter, a passive damping resistance is connected in series

with the capacitor. The value of the resistance is equal to the capacitive reactance at the resonant frequency. Besides that, the sum of the inductor should be small to keep the voltage drops in the filter negligible. The total sum of the inverter side inductor (L_f) and the grid side inductor (L_g) should be within 10% of the base impedance [139].

$$L_f = \frac{V_{dc-link}}{4k_V f_{sw} \Delta i_{pp}} \tag{3.48}$$

where $V_{DC\text{-}link}$ represents the maximum DC-link voltage for the inverter, k_v represents the ratio of the maximum voltage difference between two consecutive voltage levels to the total DC-link voltage, f_{sw} represents switching frequency and Δi_{PP} represents the maximum allowed current ripple in the injected current. Further, based on the harmonic suppression criteria and the limit for reactive power consumption by the filter, the grid-side inductor and capacitors are designed [141]. In addition, the resonant frequency of the LCL filter (f_{LCL}) must follow the given inequality to avoid control complexity and resonance condition,

$$10 f_g < f_{LCL} = \frac{1}{2\pi} \sqrt{\frac{L_f + L_g}{C_f L_f L_g}} < \frac{f_{sw}}{2} \tag{3.49}$$

3.4.3 Design of PR Current Control Scheme

The proposed inverter configuration is operated with the current-control mode to inject power into the grid. The MPPT algorithm [133] along with the power injection algorithm [134] outputs the magnitude of the current, which can be delivered to the grid. The reference current magnitude is then multiplied with the phase-locked loop (PLL) output, which is synchronized with the grid, to obtain the reference current signal (i_g^*) as shown in Figure 3.9. The error between the reference current and the actual grid-current (i_g) is processed by the PR-based current controller. The output of the PR controller is further utilized to synthesize the modulating signal for the proposed inverter configuration. The gate pulses for each switching device are generated from the controller, where the PWM logic is programmed. The PR controller is designed to achieve 0.4% maximum steady-state error at a 50-Hz frequency. The modelling based on the small-signals approach is utilized to derive the transfer function of the system, which includes the proposed inverter configuration and the

LCL filter. The proportional gain of the PR controller mainly determines the dynamics of the controller, while the resonant gain determines the amplitude gain at the resonant frequency, and controls the bandwidth around it. The proportional gain (k_{pc}) and resonant gain (k_{rc}) of the PR current controller is obtained using the SISO toolbox in MATLAB [140] by tuning with the required gain margin and phase margin. The transfer function of the PR controller is considered as follows,

$$G_{PR}(s) = k_{pc} + k_{rc}\frac{2\omega_b}{s^2 + 2\omega_b s + \omega_n^2} \tag{3.50}$$

where ω_n is the resonant frequency and ω_b is the bandwidth around the resonant frequency.

3.5 Simulation Results

In order to validate the working principle of the proposed inverter, it is simulated in the MATLAB-SIMULINK environment. The parameters for the numerical simulation of the inverter are presented in Table 3.4. An LCL filter is employed on the load side based on the above-mentioned design values for filtering out the hi-frequency components in output voltage (v_{xy}). In order to analyse the effect of the parasitic capacitance of the PV source in the proposed system, a parasitic path consisting of a resistance (R_p) series with a capacitance (C_p) is connected across the PV positive terminal and the load neutral. The parasitic capacitance varies between 60–160 nF/kW for different standards of PV panels and atmospheric conditions [142]. To evaluate the effectiveness of the proposed configuration in the worst conditions, a higher value of capacitance (about 150 nF/kW) and a lower value of ground resistance (about 10 Ω) are taken. The selection of the DC-link capacitor for the proposed system is based on the procedure described in [51]. A resistive load (R_L) of 100 Ω is considered to emulate the behaviour of the proposed inverter, which injects only active power into the grid. This simplification allows to emphasize the structural benefits obtained with the proposed inverter and facilitates the analysis of the modulation strategy.

To obtain 230V (RMS) at the inverter output, the required voltage at the DC-link is 400V. As the input voltage is boosted using an interleaved front-end buck-boost converter

Table 3.4: Specifications Considered for Simulation of Proposed Inverter.

Parameter	Values	Parameter	Values
V_{PV}	133 V	L_1 , L_2	0.5 mH
$V_{DC\text{-}link}$	400 V	L_{f1} , L_{f2}	1 mH
P_{rated}	1 kW	L_{g1} , L_{g2}	2.5 mH
f_m	50 Hz	C_f	3.28 uF
f_{swi}	20 kHz	R_p , C_p	10ohm,100nF
f_{swb}	20 kHz	C_1, C_2 ,C_3	1 mF
R_g	0.1ohm		

with a gain factor of three, around 130-140V is required at the input voltage. Thus, a PV array with a maximum power point (MPP) voltage of 133V is considered to be the input voltage for the inverter. The simulated waveforms of output voltage, current, and SC voltage for the proposed seven-level inverter configuration are shown in Figure 3.13. It can be observed that the inverter output voltage has seven distinct voltage levels at +/- 400V, +/- 266V, +/- 133V, and 0V, which is in the agreement with the 7-level unipolar operation of the inverter as shown in Figure 3.13 (a). The total harmonic distortion (THD) of the load current shown in Figure 3.13 (b) is around 1.26%, which meets the IEEE-1547-2018 standard [25]. The input voltage (V_{PV}) and two SC voltages (V_{C1}, V_{C3}) maintain a voltage level of 133V each as shown in Figure 3.13 (c), whereas the total DC-link voltage goes up to 400V as presented in Figure 3.13 (a). The elements of the front-end buck-boost stage are designed based on the equations

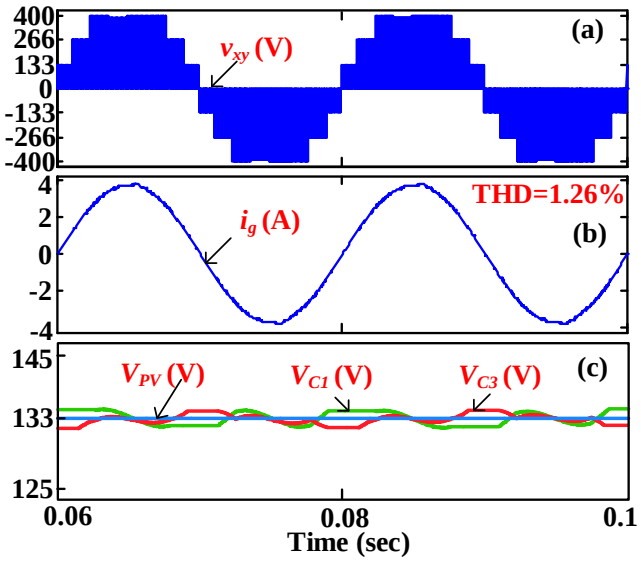


Figure 3.13: Simulation results of (a) inverter output voltage, (b) load current, (c) input PV voltage (V_{PV}), and voltages of the switched capacitors (V_{C1} and V_{C2}).

given in section 3.4.1. The PI controllers for the closed-loop operation of the voltages of the C_1 and C_3 capacitors are designed using the *SISO toolbox* in MATLAB [143]. The control parameters for the voltage control loop are tuned to achieve a gain margin of 11.2 dB and a phase margin of 55^0 to ensure the stability of the closed-loop voltage control loop. The proportional gain (k_{pv}) and integral gain (k_{iv}) for each of the PI controllers in the front-end converter are obtained as 0.0006674 and 0.298 respectively. The performance of the front-end buck-boost converter in the closed-loop condition is analysed and the voltage ripples in the SC (C_1 and C_3) are presented in Figure 3.13 (c). The simulation results demonstrate the effectiveness of the closed-loop operation, as the voltage ripple with a closed-loop is lesser compared to the open-loop condition.

Figure 3.14 presents the simulation results for the performance of the front-end interleaved buck-boost converter for two different loading conditions. At light-lading conditions (Figure 3.14 (a)-(d)), the front-end interleaved converter operates in DCM mode as can be observed from Figure 3.14 (c)-(d). However, when the load is increased the converter operates in DCM with an increased peak inductor current as shown in Figure 3.14

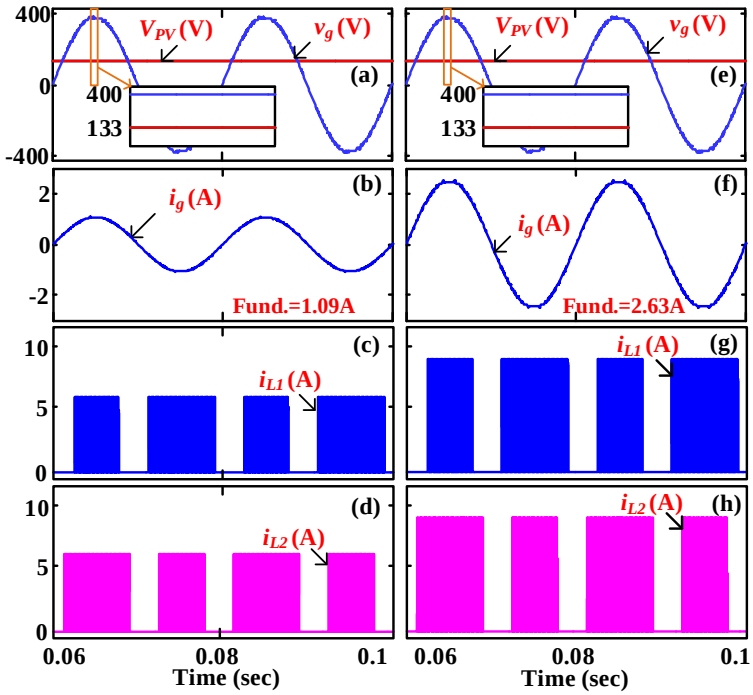


Figure 3.14: Simulation waveforms of input PV voltage (V_{PV}) and load voltage (v_g), load current (i_g) , inductor current (i_{L1}), inductor current (i_{L2}) : (a-d) at light loading (R_L=200Ω), (e-h) at full loading (R_L=100Ω) conditions.

(g)-(h). Therefore, it can be concluded that the performance of the proposed inverter is unaltered in different loading conditions.

Further, to analyse the performance of the proposed inverter configuration, simulation results are presented in the left and right columns (i.e. columns I and II) of Figure 3.15 for two different modulation indices of 0.9 and 0.6 respectively. The reduction in voltage levels can be observed by comparing Figure 3.15 subplots I (a) and II (a). The fundamental peak of the load current is also reduced linearly with the modulation index. However, there is no significant variation in the harmonic spectrum as well as THD with respect to the variation in the modulation index variation as shown in Figure 3.15 (subplot (I) and (II) (b)). Subplots I (c) and II (c) respectively show the nature of the voltage across the positive terminal of the PV source and the load neutral. It can be observed that the total common-mode voltage displays only eight voltage transitions, each with a magnitude of $1/6^{th}$ of the total DC-link voltage (i.e. 400V), in any given fundamental cycle. These transitions limit the maximum peak value of the leakage current is limited to 150mA and the maximum RMS value of 15mA, which are well below the standard DIN VDE 0126-1-1 as shown in subplots I (d) and II (d). In contrast, any conventional PWM technique would result in a much higher number of transitions causing higher leakage current [144]. Thus, the proposed PWM scheme would lower the leakage current significantly enhancing the level of safety for the operating personnel. Further, the proposed modulation strategy also reduces the switching-frequency voltage transition in the CMV (v_{CMV}), which can be observed from subplots I and II (e). This reduces the requirement of the size, weight, and cost of the common mode EMI filter/choke to be employed with the proposed PV inverter system.

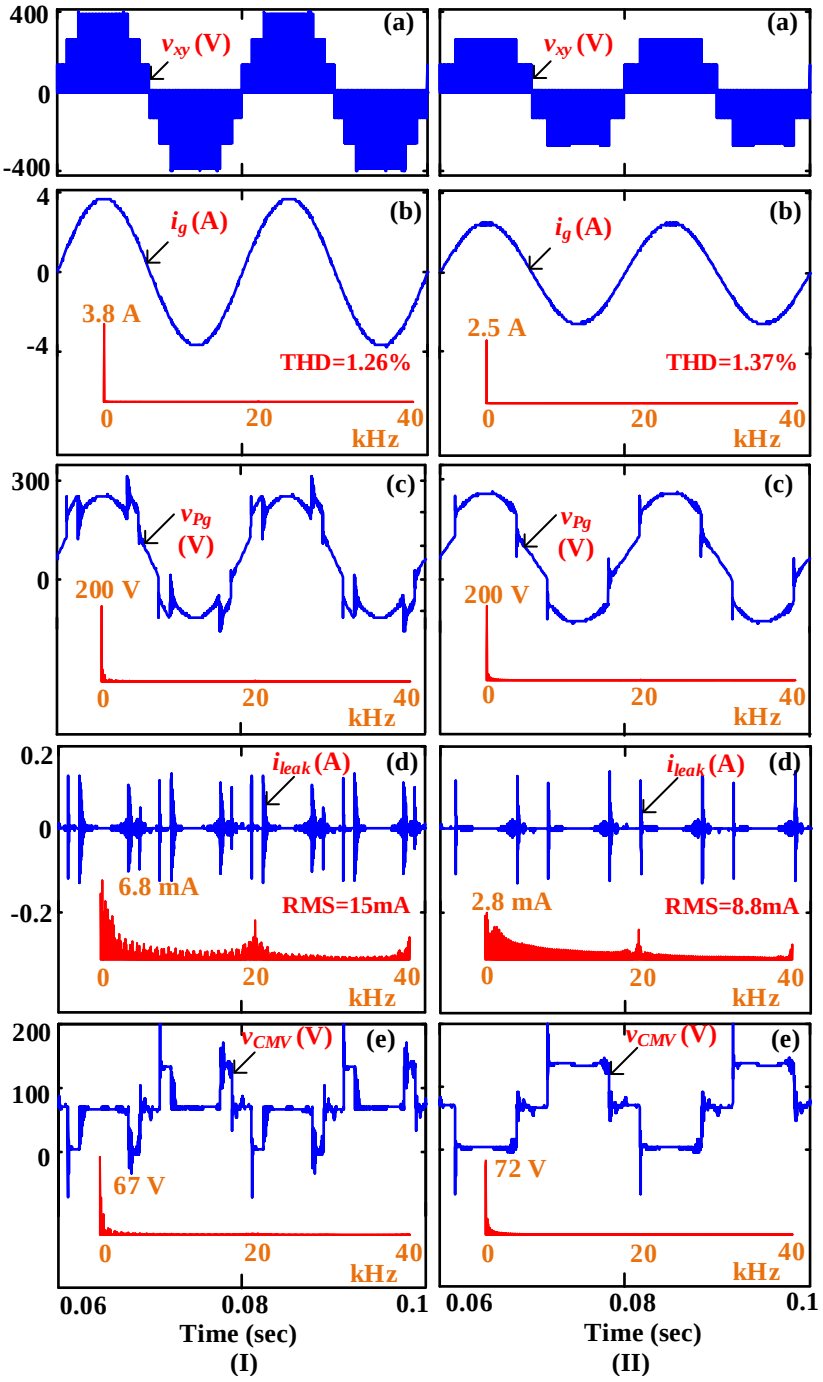


Figure 3.15: Simulation waveform of (a) inverter output voltage (v_{xy}), (b) load current (i_g), (c) total common-mode voltage (v_{Pg}), (d) leakage current (i_{leak}), (e) CMV(v_{CMV}) for the modulation indices: (I) m_a = 0.9 and (II) m_a = 0.6 .

3.6 Experimental Results

In order to assess the performance of the proposed power circuit configuration, an experimental prototype of 200VA has been fabricated. Table 3.5 summarizes the operation

Table 3.5: Specifications Considered for Experimental Prototype

Parameter	Values
Input Voltage (V_{PV})	50 V
Total Boosted Voltage ($V_{DC\text{-}link}$)	150 V
Rated Power, *S*	200 VA
Modulation frequency (f_m)	50 Hz
Switching frequency (f_{sw})	20 kHz
Switched Capacitor(C_1,C_3) (metalized polyester)	24×(6.8) uF,300V
DC-link Capacitor C_2 (Electrolytic)	1 mF, 400V
DC inductors (L_1 , L_2)	0.5 mH
Filter inductors (L_{f1},L_{f2})	1 mH
Grid inductors (L_{g1},L_{g2})	2.5 mH
Filter Capacitor (C_f)	3.26 uF
Parasitic elements (R_p,C_p)	10 ohm,100nF

and circuit parameters of the system. MOSFETs (IRF 840) are used as semiconductor switches of the inverter configuration and HCPL 3120 ICs are used as gate drivers for these MOSFETs. A programmable DC source is used in order to emulate a PV source for the inverter configuration. The crystalline silicon-based PV modules, which are widely used for PV applications, provide a maximum power point (MPP) voltage from 30V-60V and provides power in a range of 100-500W [74]. In this context, the input voltage of the inverter is maintained at 50V. For the generation of PWM pulses for the inverter switches, the modulation technique is implemented using the Xilinx Blockset and deployed into the FPGA SPARTAN 6. The Tektronix MDO 3024 is used for the acquisition of experimental results. A picture showing the fabricated inverter configuration with an experimental testing bench is depicted in Figure 3.16. Twenty-four (24) metalized-polyester type capacitors (each 6.8uF,

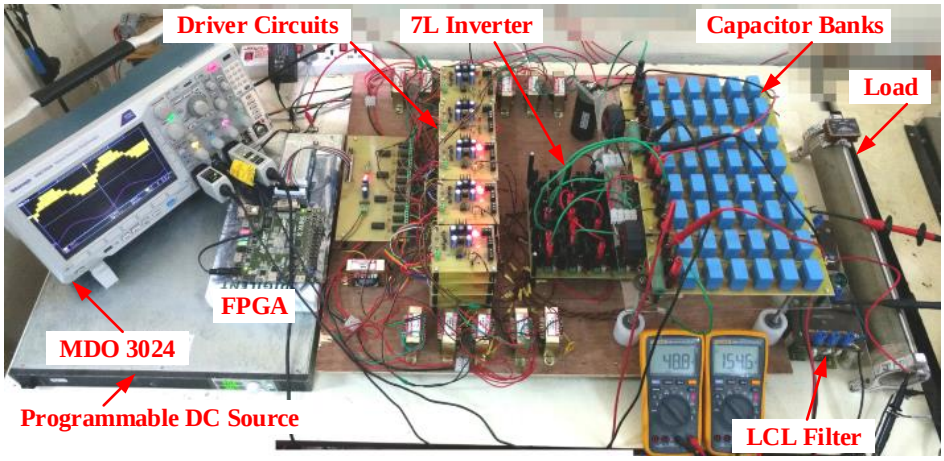


Figure 3.16: Experimental prototype for the proposed 7L inverter configuration.

300V) are connected in parallel to realize each switched capacitor. The parasitic element of the PV source is added by connecting a resistance and a capacitance in series between the source positive terminal and the load neutral.

From Figure 3.17 (a) it can be observed that both of the SCs are charged to the same voltage as the input PV voltage i.e. 50 V. It can also be observed that, the charging duration of both of the SCs is cyclic to equalize the utilization of the SCs. From the inductor current shown in Figure 3.17 (b), it can be observed that the switching logic employed creates a phase difference of π radians between them. This is in clear agreement with the phase-shifted modulation technique presented in section 3.3.1 (Figure 3.6).

To emphasize the advantages obtained with the proposed PWM technique in comparison to the conventional SPWM technique, both of these PWMs are applied to the proposed power circuit with unaltered circuit parameters. Figure 3.18 (a) and (c) present the output voltage waveform and load current obtained with conventional SPWM and proposed PWM technique respectively. It can be observed that the conventional SPWM technique results in a conventional staircase-based output voltage waveform whereas, the proposed PWM technique incorporates freewheeling states in each of the switching cycles. The parasitic voltage waveform, obtained with the conventional SPWM technique, contains high-frequency voltage transitions (corresponding to switching frequency). However, the proposed PWM technique eliminates all the high-switching frequency transitions from the parasitic voltage waveform. As the parasitic branch of the PV panel is capacitive, it offers low impedance to the high-frequency voltage transitions, which further induces leakage current transitions against each voltage transition. With identical circuit parameters, the proposed

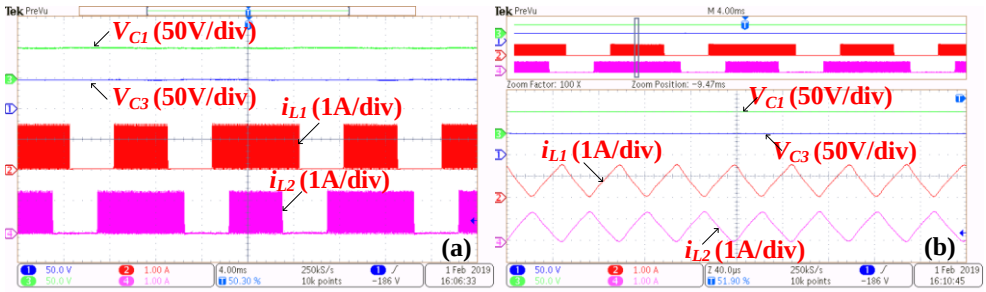


Figure 3.17: Experimental results (a) switched capacitor voltage (v_{C1}, v_{C2}) and inductor current (i_{L1}, i_{L2}), (b) zoomed waveform of (a).

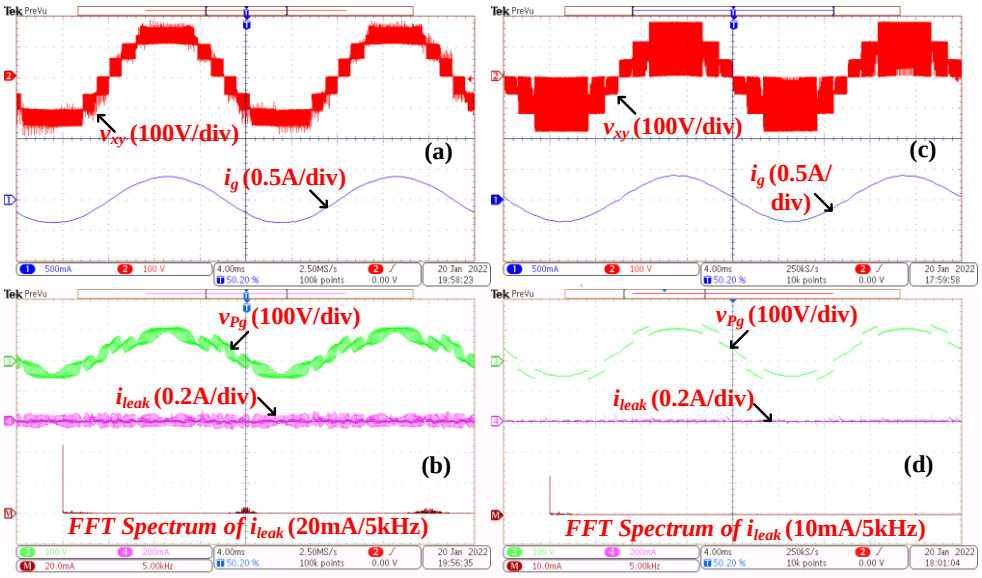


Figure 3.18: Experimental results inverter output-voltage (v_{xy}), load-current (i_g), voltage across parasitic elements (v_{Pg}), leakage current (i_{leak}) (a)-(b) obtained with conventional LSPWM, (c)-(d) obtained with proposed PWM technique.

PWM results in a much lower RMS value of the leakage current (3.61mA, RMS) compared to the one obtained with the conventional SPWM (48.1 mA, RMS). In addition, as the magnitude and the number of each voltage transition depends on the input voltage and the switching frequency, the leakage current increases further with the increase of these parameters. These experimental results are in agreement with the simulation results, validating the operation and the working principle of the proposed power circuit configuration with the proposed modulation scheme.

The left and right columns (i.e. column I and column II) of Figure 3.19 respectively present the experimental results for the modulation indices of 0.9 and 0.6. The voltages of SCs (v_{c1}, v_{c3}) and the respective charging currents (i_{L1} and i_{L2}) for the modulation index are shown in subplots I (a) and II (a). Subplots I (b) and II (b) shows the output voltage and load current. It can be observed that output voltage contains seven distinct levels at +/-150V, +/-100V, +/- 50V, and 0V demonstrating the seven-level operation. As the modulation index reduces the voltage level containing +/-150V is eliminated and it continues to work as a five-level inverter (Figure 3.19 (II) (b)). This fact is in good match with the simulation results presented in Figure 3.15 (II). To analyse the performance of the inverter in terms of the leakage current, the total common-mode voltage (v_{Pg}) across PV positive terminal and load

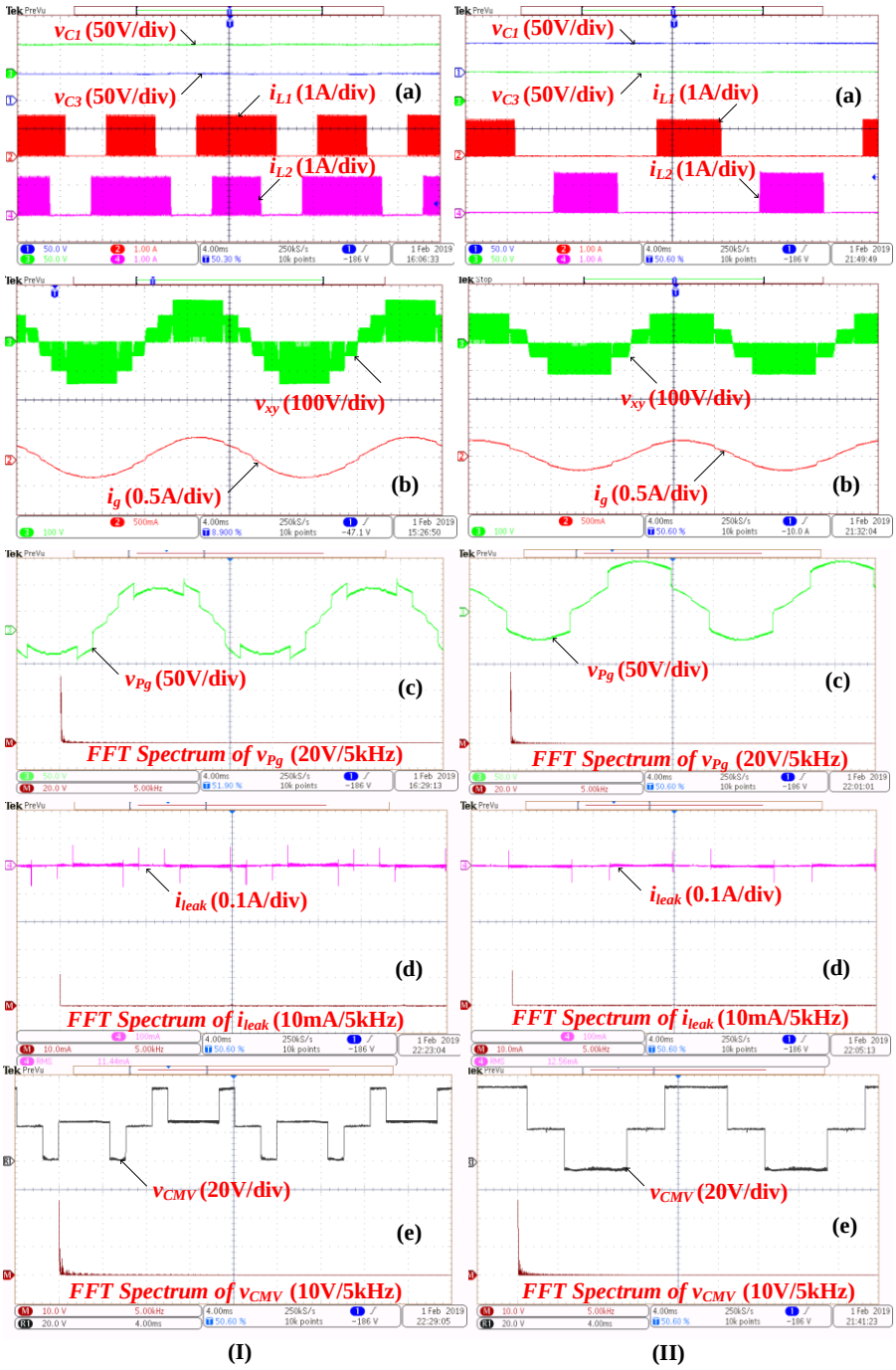


Figure 3.19: Experimental results of (a) SCs voltages (V_{C1}, V_{C3}), charging current(i_{L1}, i_{L2}), (b)inverter output voltage(v_{xy}) and load current (i_g), (c) total common-mode voltage (v_{Pg}), (d)leakage current (ileak), (e) common mode voltage (v_{CMV}) for the modulation indices: (I) m_a=0.9 and (II) m_a=0.6.

neutral is recorded. This voltage appears across the parasitic path of the PV source. Therefore, the presence of switching voltage transitions in the total common-mode voltage contributes to the transitions in the leakage current since $i_{leak} = C_{PV}(dv_{Pg}/dt)$. From the subplots I(c) and II(c), it can be observed that the total common-mode voltage (v_{Pg}) oscillates at the

fundamental frequency, which effectively reduces the leakage current. The experimentally obtained leakage currents for both the modulation indices are shown in Figure 3.19 (d). The maximum RMS value of i_{leak} reaches only 13 mA, which is significantly lesser than the maximum limit of 300 mA as stipulated by VDE 0126-1-1. Moreover, the common-mode voltage, shown in Figure 3.19 (e), is recorded using the following mathematical operation on 0.5 (v_{xN} + v_{yN}). It can also be implied that the common-mode voltage also oscillates at the fundamental frequency. The FFT spectrum, confirms the absence of high-frequency components in the CMV waveform. This further reduces the size and order of the common mode choke and EMI filter of the proposed configuration. Thus, the experimental results (presented in Figure 3.19) are in good agreement with the simulation results (presented In Figure 3.15), validating the operating principle of the proposed power circuit topology and the associated PWM technique.

Further, the performance of the inverter is validated in the grid-tie condition. The block diagram of the control scheme for the proposed configuration is shown in Figure. 3.20. The PQ-based approach is adapted to the conventional MPPT algorithm to attain the reference of the grid current [134]. The PR current controller is designed based on system parameters as given in Table 3.5. The value of the proportional gain (k_{pc}) and resonant gain (k_{rc}) for the current controller are obtained as per the procedure given in section 3.4.3. The value of k_{pc} and k_{rc} are obtained as 0.132 and 8.68 respectively for the proposed power converter. The gain margin and phase margin of the overall closed-loop system are obtained as 11 dB and 66.3^0 as shown in Figure 3.20. This further confirms the stability of the current control scheme

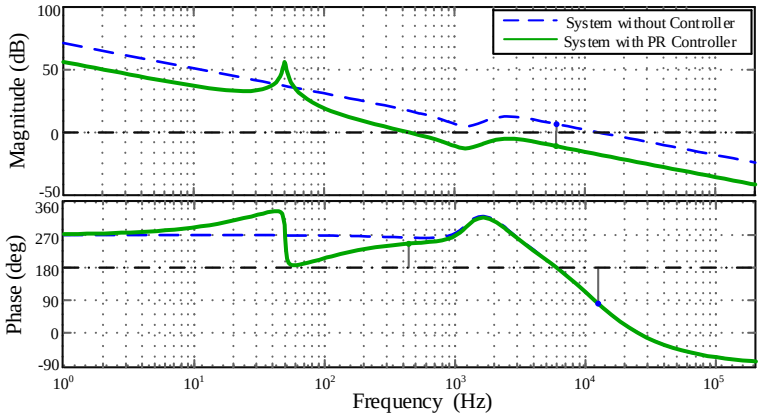


Figure 3.20: Bode plot for PR controller and the proposed integrated seven level inverter.

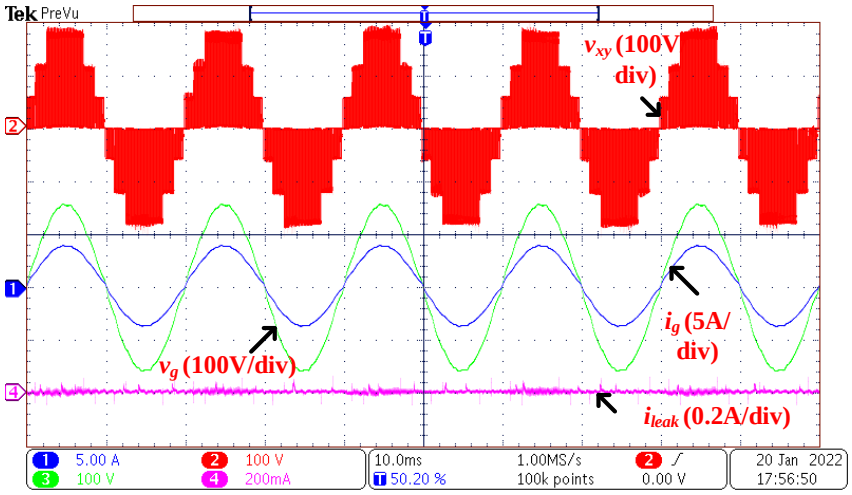


Figure 3.21: Experimental results: inverter output voltage (v_{xy}), grid-voltage (v_g), grid-current ($_{ig}$) and total common-mode voltage (v_{Pg}).

for the proposed power converter. The effectiveness of the current controller is also evident in Figure 3.21, which demonstrates the operation of the proposed configuration to inject power into the grid. The proposed configuration injects a current of 1.6A (peak) at UPF to the grid. It is observed that the operation of the inverter is unaltered in comparison to the standalone operation of the inverter.

3.7 Comparison with Existing Transformerless Configurations

3.7.1 Semiconductor Voltage and Current Stress Comparison

To demonstrate the merits of the proposed topology, a comparative evaluation is presented in Table 3.6 with the prevailing switched capacitor-based MLI (SCMLI) configurations. For a fair comparison, only those configurations, which are equipped with a single PV source, are taken into consideration. As the literature available on 7-level inverters with the features of voltage boosting and mitigation of leakage current is limited, the comparison with 5-level and 3-level topologies is also carried out.

In order to comprehensively present the features of the proposed topology, it has been compared with various classical configurations as well as recently proposed topologies available in the literature. The comparison is performed in terms of the number of components and the performance indices enumerated in Table 3.6. Though the topologies proposed in

Table 3.6: Comparison Table with Existing Configurations

Parameter	[145]-3L	[46]-3L	[146]-5L	[99]-5L	[85]-7L	[147]-7L	Proposed-7L
N_{Sw}	6	5	6	9	16	14	12
N_{diode}	0	0	2	1	0	2	2
N_{Cap}	1 bulky	2 bulky	2 bulky	2 small	2 bulky	2 bulky	2 small, 1 bulky
N_{Ind}	0	0	0	1	0	0	2
TSV_{pu}	6	5	6	8.5	5.33	4.67	8.67
Gain	Unity	Unity	Unity	2	3	3	3
i_{leak}	Min.	NIL	Min.	NIL	High	High	Min.
Peak i_{sw}	I_L	$6I_L$	I_L	$2\text{-}3I_L$	$6I_L$	$5\text{-}6I_L$	$2.5I_L$
ESR loss	Low	High	High	Low	High	High	Low
THD_V	52.7	52.9	27.5	27.1	20.4	21.1	37.2
THD_I	4.2	4.3	2.9	2.9	2.1	2.2	2.8

[145] and [46] display higher efficiencies and better reduction of leakage current, they lack the inherent voltage gain and result in only 3L output voltage. A modified T-type topology is proposed in [146], which results in a 5L output voltage waveform as well as a low leakage current. However, significant common-mode voltage still exists and higher-order EMI filters are required to be employed in this topology for its suppression. A novel integrated dc-dc converter-based topology is proposed in [99], which results in multilevel operation with a single dc source as well as a significant reduction in the leakage current. Compared to the topology proposed in [99], the proposed configuration achieves about three times at 7L operation with a single dc source. The topologies proposed in [85] and [147] employ bulky switched capacitors to achieve a gain of three and operate with a single DC source, reducing the energy density of the inverter. Furthermore, due to the SC technique, these configurations are prone to high switch current stress and high ESR loss in the capacitor. Thus, the principal advantage of the proposed power circuit configuration and the associated PWM scheme is that, together, they render the dual advantage of seven-level operation and a good voltage boosting (of about three times) with lower switch count and lower SC size (Table 3.6).

3.7.2 Semiconductor Power-loss Calculation and Comparison

In order to assess the performance of the proposed topologies, a thermal model has been employed and simulations are carried out in the PLECS environment for a power rating of 1.5 kW with an input voltage of 133 V. All the specifications of the semiconductor devices are obtained from the datasheet of the IGBT device (with body diode) IKW30N60T. In the comparative analysis, the following parameters have been considered: (i) semiconductor

losses (both switching loss (P_{sw}) and conduction loss (P_{cond})), (ii) inductor conduction loss (P_{ind}), and (iii) capacitor ESR loss (P_{cap}). The losses in the passive devices are theoretically calculated from the equations given in [148]. The proposed configuration is compared with the four existing configurations proposed in [46], [60], [70], [72], [85], [99], [145] and [146] for the same power output. In order to facilitate a fair comparison of the proposed boosting technique, a boost converter is employed with the existing power circuit configurations reported in [46], [60], [70], [72], [145] and [146] to maintain a total DC-link voltage of 400V from the 133V input voltage. Figure 3.22 (a) illustrates various power losses incurred in power circuit configuration as well as those incurred in the proposed 7L MLI along with the respective front-end boosting circuits. The configuration proposed in [99] is more efficient. However, it results in a lower number of voltage levels (five levels) and lower voltage boosting (by a factor of two) compared to the work presented in this chapter. The conduction losses in the switches for configuration [85], [147] are more as switched capacitor-based boosting technique is incorporated for the boosting of voltage. Moreover, from Figure 3.22 (a), it is evident that the power loss in the parasitic elements of the passive devices is higher with most of the existing configurations compared to the proposed configuration. The principal reason for this phenomenon is that all these topologies employ the conventional boost converter as a boosting stage between the PV source and respective inverter configuration. This means that all of the power obtained by the PV source must necessarily be processed through the conventional boost converter. In contrast, in the proposed power circuit topology, only 63% is processed through the boosting stage. Thus, it may be expected that the power loss in the boosting stage is significantly lower, which is supported by Figure 3.22 (a). Furthermore, it may be observed that the power loss incurred in the capacitor in the proposed circuit is much lesser as the ESR associated with the metalized polyester capacitor is significantly lower than the bulky electrolytic capacitor.

Furthermore, a theoretical analysis is carried out to assess the efficiency of the proposed power circuit at different power levels considering the above-mentioned factors. The efficiency plot, presented in Figure 3.22 (b), is determined by considering power loss in the inverter as well as in the boosting stage while varying the power output from 500W to 2.5kW at two different input voltage levels (133V, 270V). It can be observed that, as the input voltage increases, the requirement of voltage boosting reduces, thereby reducing the power

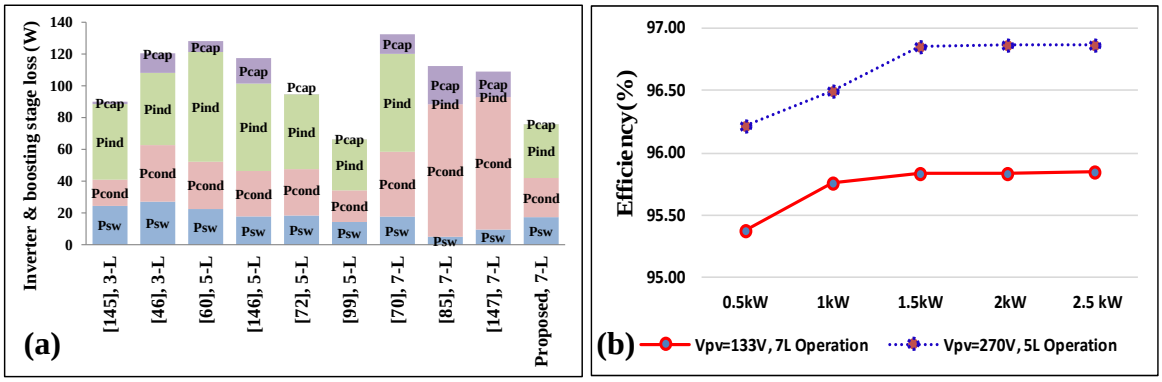


Figure 3.22: (a) Comparison of total loss incurred in existing and proposed configuration at a power rating of 1.5kW, (b) Efficiency of the proposed configuration at two different voltage levels (i.e. 133V, 270V).

loss in the boosting section. Thus, higher input voltage with 5L operation displays a higher efficiency compared to the 7L operation of the proposed configuration.

The total harmonic distortion (THD) and power factor are measured using UNI-T UT283A single-phase power analyzer. Figure 3.23 (I) (b) and Figure 3.23 (II) (b) give the THD plot for the load current for 7L operation and 5L operation at unity power factor conditions respectively. The THD of the load current is found to be 1.56% for the 7L operation and 2.22% for the 5L operation, which are within the limits specified in the IEEE-1547-2018 standards. Moreover, according to EN 50438, a PV inverter should be able to operate at least up to PF=0.95[149]. Therefore, the active and reactive power capability of the proposed inverter is examined experimentally by connecting a resistive load (R_L= 60 ohm) and a reactive load (R = 100 ohm, L=200 mH (cos ϕ = 0.83)) at the output terminals of the inverter. For, both of these cases 110V_{rms} is maintained with 7L operation. It can be observed that for both of these cases the nature of total common-mode voltage is unaltered. Thus, the same leakage current results in both of these cases. The efficiency of the proposed converter at PV voltage of 50V and total DC-link voltage of 150V is found to be 90.10% (for P_{out} = 150 W) and 91.04% (for P_{out} = 200 W) at 7L operation. In case of 5L operation, the efficiency is observed to be 91.43% (for P_{out} = 100 W) and 93.50% (for P_{out} = 150 W). These results are similar to the ones reported in [99].

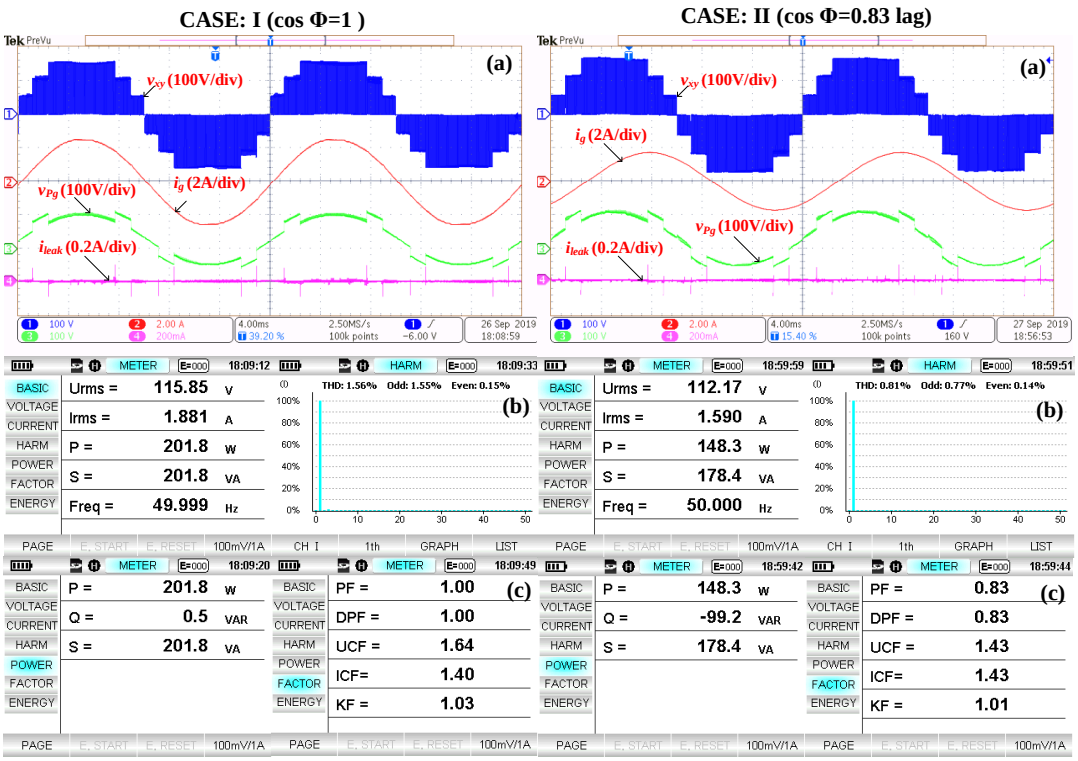


Figure 3.23: (a)Inverter output voltage(v_{xy}), current(i_{xy}), total common-mode voltage (v_{Pg}), leakage current (i_{Leak});(b) RMS output voltage(v_{rms}), Harmonic spectrum of the load current, (c) active power (P), reactive power (Q),apparent power (S), power factor (PF)) for (I) 7L operation at P_{out}=200W, UPF (II) 7L operation at P_{out}=180VA, with 0.83 lagging.

3.8 Conclusion

In this chapter, a transformerless 7-level inverter configuration and its modulation technique are proposed. This semi-double-stage topology, wherein the boosting stage is integrated with 7-level VSI, achieves an overall boost factor of three. The proposed topology eliminates the problems associated with conventional SCMLI configurations such as the requirement of bulky capacitors and the peak current stresses on the switches. The most important advantage of the proposed boost stage (integrated with the inverter) is that only 63% of the power from the PV source is processed through it, while the rest 37% of power is transferred directly from the PV source to the load. It is shown from the power loss analysis that the proposed boosting scheme reduces the losses in the passive devices compared to the conventional boosting schemes. Through detailed mathematical analysis, numerical simulation, and experimental validation, it is shown that both the RMS value and the peak values of the leakage current are well below the German standard DIN VDE 0126-1-1. Thus,

it is envisaged that the proposed topology, along with the PWM scheme, is suitable for both standalone as well as grid-connected applications.

Chapter 4

Nine-Level Transformerless Boost Inverter with Improved Modulation Technique

Chapter 4

Nine-Level Transformerless Boost Inverter with Improved Modulation Technique

4.1 Introduction

The proposed power converter in Chapter 3 achieves voltage boosting and a reduction in the leakage current. Also, it transfers a considerable portion of the PV power directly to the load. However, the output voltage waveform of the inverter (Figure 4.1(b)) suffers from two major disadvantages (a) high total harmonic distortion (THD) and (b) high *dv/dt* across the switches, when compared to the conventional multilevel output voltage (Figure 4.1(a)). Also, this topology needs a decoupling network to reduce the leakage current in the common mode network.

From the comprehensive study of the available literature, it is clear that there is a need for a multilevel single-phase transformerless inverter topology with the following features:

i) Complete dc-bus utilization as opposed to HB-based configurations
ii) Voltage boosting capability with reduced current stress on the semiconductor devices as opposed to conventional SC-based topology.
iii) Elimination of switching frequency transitions from the total common-mode voltage (TCMV) waveform *exclusively* with modulation technique (i.e. without any additional circuitry).
iv) A simplified generation of MLI output voltage from a single PV source (This avoids the complexity of multi-loop MPPT algorithms for multiple PV sources).
v) Ability to handle inductive loads (similar to the conventional MLIs), without any additional clamping diodes or capacitors.

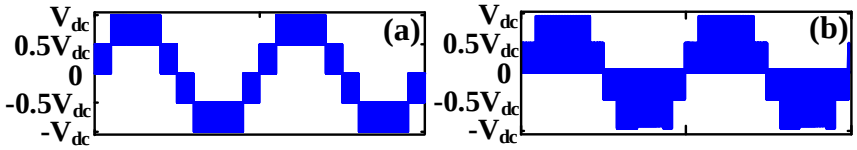


Figure 4.1: (a) Conventional multilevel output, (b) Modified PWM techniques.

This chapter presents a new integrated transformerless, single-phase 9L-MLI, wherein an interleaved buck-boost converter is fused with a level generation unit to realize the above-mentioned features. The main contribution of this chapter is to introduce a new power circuit configuration with semi-double staged multilevel inversion along with a modified modulation strategy. In addition to that, the proposed configuration exhibits a symmetrical structure, which increases the redundancy among the switching combinations. This feature facilitates devising a PWM scheme, which employs a cyclic utilization of the DC-link capacitors and consequently an even distribution of power losses among the interleaving sections of the boosting stage. It is also shown that the leakage current resulting from this system is capable of complying with the *VDE-0126-1-1* standards for the PV inverter [156]. A common-mode model of the proposed topology along with the mathematical derivation of the TCMV is also presented in the chapter.

4.2 Operation of the Proposed Nine-level Hybrid Boost Inverter

The power circuit configuration of the proposed nine-level T-type hybrid boost inverter (9L-T-HBI) is shown in Figure 4.2. This MLI configuration employs two HB (half-bridge), one bi-directional T-branch, and one polarity generator H-bridge in its structure. This power circuit configuration comprises nine power switches (S_1, S_2, … S_9) for the generation of distinct nine voltage levels at the output. An interleaved buck-boost converter, which is constituted by two switches (S_{b1}, S_{b2}), two inductors (L_1, L_2), and two diodes (D_1, D_2) energizes the SCs (C_1, C_4). However, the DC-link capacitors (C_2, C_3) are directly connected

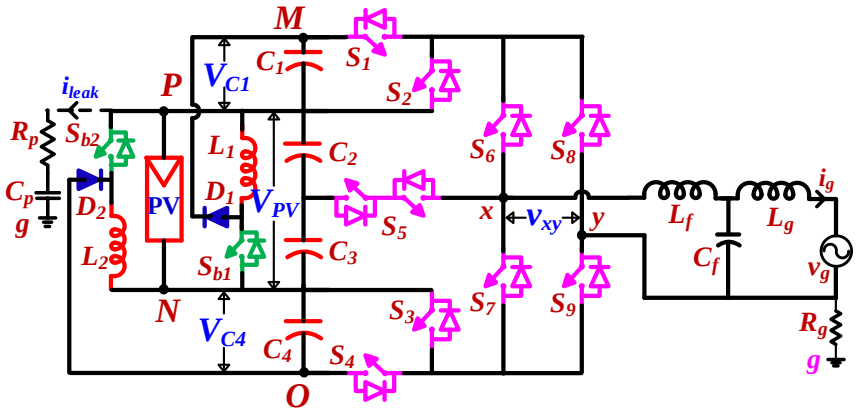


Figure 4.2: Circuit schematic of proposed 9L-T-HBI topology.

across the PV source. This configuration decouples the dependency of the charging durations of the SCs from the inverter modulation scheme. This further helps in the independent design of SCs, compared to the requirement of bulky SCs in recent SC-based boosting topologies [151-153].

The switching states of the individual switching devices to obtain individual voltage levels are listed in Table 4.1, wherein their turn-on and turn-off states of them are indicated as '1' and '0' respectively. The modes of operation to synthesize nine distinct voltage levels are presented in Figure 4.3. The switching sequences of Mode I ($\pm 3V_{PV}$) are indicated as S^{+3} and S^{-3} in Table 4.1 respectively for positive and negative half-cycles. It is observed that, in this mode, the total DC-link voltage is realized by the PV source and the two SCs (C_1 and C_4). It may be observed that Mode II ($\pm 2V_{PV}$) exhibits redundant switching states; these are represented as S^{+2A}, S^{+2B} for the positive half cycle, and S^{-2A}, S^{-2B} for the negative half cycle respectively. In Mode III ($\pm V_{PV}$) and Mode IV ($\pm 0.5V_{PV}$), both of the boosting circuits are disabled, as the power directly flows from the PV source to the load. The switching sequence for Mode III and IV are represented as (S^{+1}, S^{-1}) and ($S^{+0.5}$ and $S^{-0.5}$) respectively for the positive and negative half-cycles. From Figure 4.3, it is evident that the proposed 9L-T-HBI configuration allows a path for the load current in both directions (i.e. positive and negative) in all modes. Thus, it may be noted that the proposed configuration can also handle reactive loads [127], [157].

Table 4.1: Switching States of Voltage Levels

Switching Sequence	**S_1**	**S_2**	**S_3**	**S_4**	**S_5**	**S_6**	**S_7**	**S_8**	**S_9**	**Output Voltage Level**
S^{+3}	1	0	0	1	0	1	0	0	1	$+3V_{PV}$
S^{+2A}	0	1	0	1	0	1	0	0	1	$+2V_{PV}$
S^{+2B}	1	0	1	0	0	1	0	0	1	$+2V_{PV}$
S^{+1A}	0	1	1	0	0	1	0	0	1	$+V_{PV}$
$S^{+0.5A}$	0	1	1	0	1	0	0	0	1	$+0.5V_{PV}$
S^{+0}	0	1	1	0	0	0	1	0	1	0
S^{-0}	0	1	1	0	0	1	0	1	0	0
$S^{-0.5A}$	0	1	1	0	1	0	0	1	0	$-0.5V_{PV}$
S^{-1A}	0	1	1	0	0	0	1	1	0	$-V_{PV}$
S^{-2A}	0	1	0	1	0	0	1	1	0	$-2V_{PV}$
S^{-2B}	1	0	1	0	0	0	1	1	0	$-2V_{PV}$
S^{-3}	1	0	0	1	0	0	1	1	0	$-3V_{PV}$

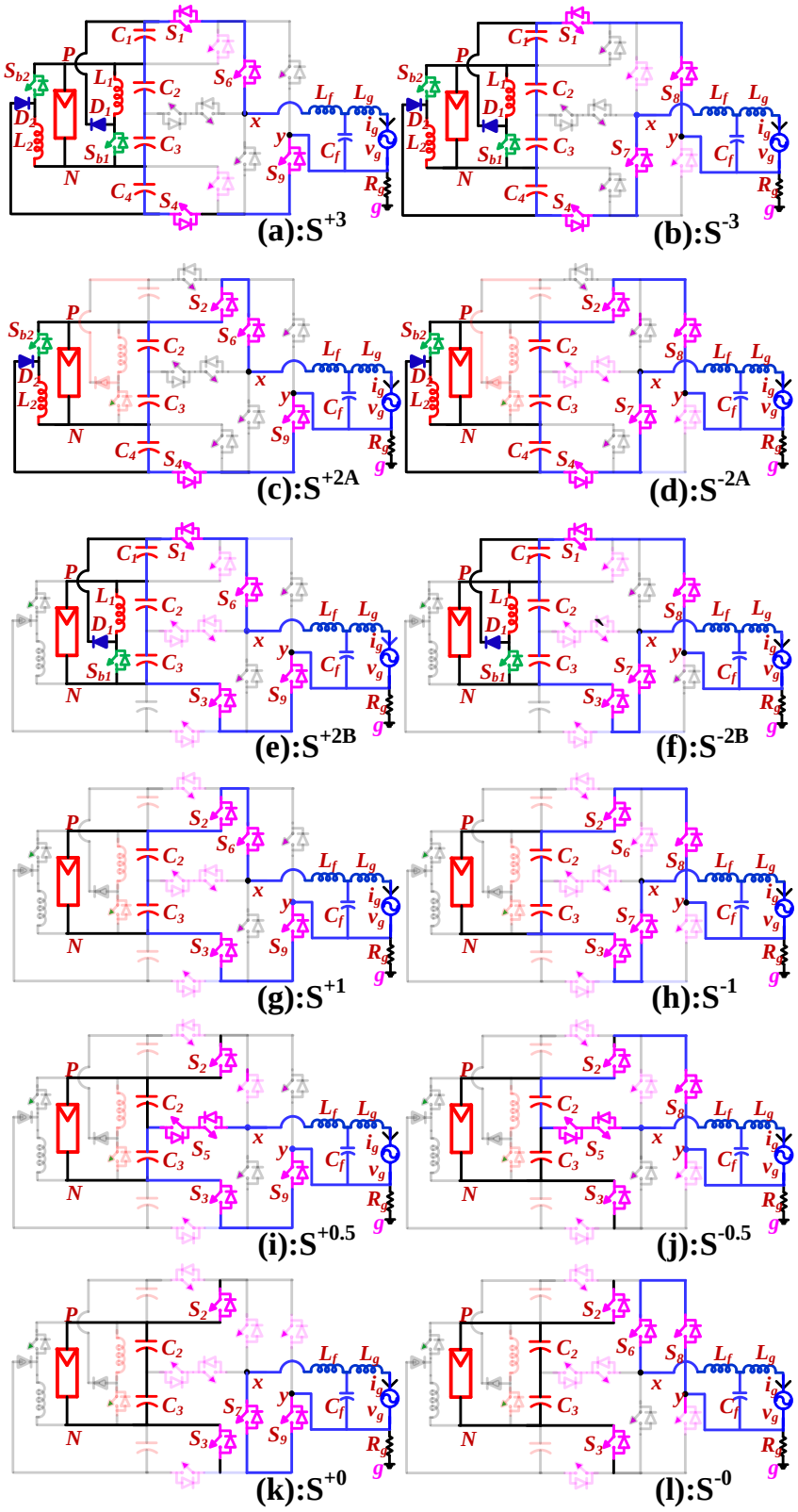


Figure 4.3: Mode I: (a)+3V_{PV},(b)-3V_{PV}; Mode IIA:(c)+2V_{PV} (d)-2V_{PV}; Mode IIB: (e) +2V_{PV} (f) +2V_{PV} ; Mode III: (g)+V_{PV},(h) -V_{PV}; Mode IV: (i)+0.5V_{PV} (j)-0.5V_{PV}; Mode V: (k)freewheeling ,(l) freewheeling.

4.3 Common-Mode Voltage Analysis

The common-mode equivalent circuit for the proposed inverter configuration is presented in Figure 4.4 (a)-(c), wherein the PV parasitic element is modeled as a series connection of an equivalent resistor R_P and capacitor C_P. R_g specifies the ground impedance with respect to load neutral. According to the common-mode model presented in Figure 4.4 (c), the total common- mode voltage (TCMV) (v_{Pg}) feeds the parasitic path, which eventually induces the leakage current. As the PV parasitic elements are capacitive, it offers a low impedance path to high-frequency voltage components present in the TCMV.

A thorough TCMV analysis is carried out with the aid of the switching function analysis for the proposed configuration. The switching variables used in the study are indicated as S_{SX}, wherein '*SX*' denotes the corresponding switch (S_1, S_2, … S_9). The values of the switching function S_{SX} is either '1' or '0' depending on the switching states of that switch. Furthermore, the common-mode equivalent circuits of the proposed 9L-T-HBI topology are derived as per the procedures derived in [157-158]. To obtain the mathematical expression of the TCMV (v_{Pg}), it is convenient to express the pole voltages (v_{xo}, v_{yo}) of each

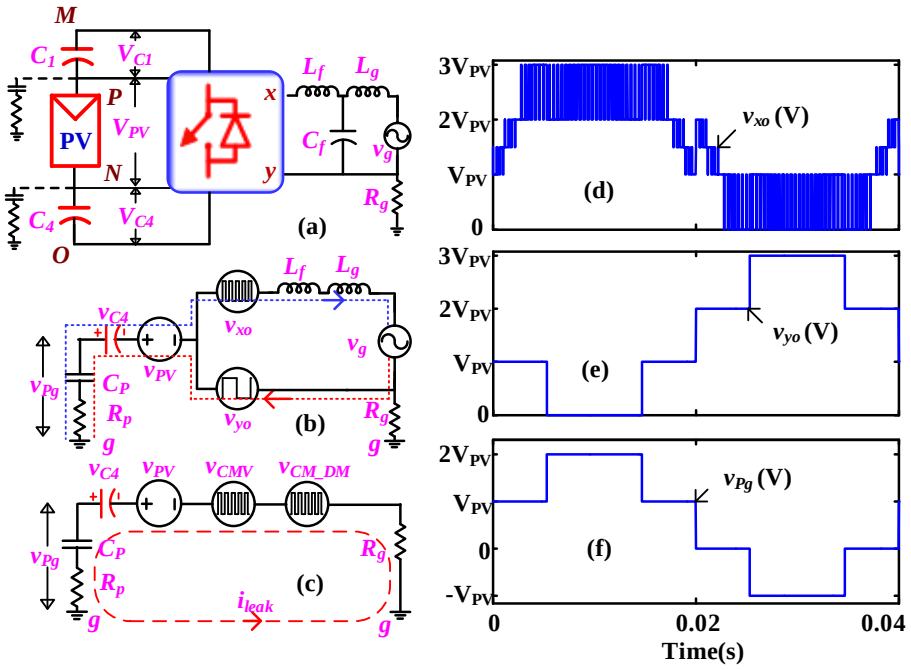


Figure 4.4: (a), (b), (c) common-mode equivalent circuit; pole voltage: (d) v_{xo}, (e) v_{yo}, (f) total common mode voltage (v_{Pg}).

output terminal (*x*,*y*) with respect to the reference node 'O' of the proposed configuration as shown in Figure 4.4 (c). The pole voltages can be expressed as per the following eqns. (4.2, 4.3):

$$v_{xO} = [(1 - S_{S8})(S_{S1}(2 - S_{S6}) + S_{S6} + S_{S5} + 1) + S_{S8}(S_{S3}(2 - S_{S7}))] \times V_{PV} \quad (4.2)$$

$$v_{yO} = ((2 - S_{S3} + S_{S1})S_{S8} + S_{S3}) \times V_{PV} \quad (4.3)$$

The voltage waveforms of v_{xo} and v_{yo} are shown in Figure 4.4 (d) and (e) respectively. Similarly, the common-mode voltage (v_{CMV}), and the differential mode voltage (v_{xy}) can be derived from the following eqns.,

$$v_{CMV} = \frac{v_{xO} + v_{yO}}{2} \quad (4.4)$$

$$v_{xy} = v_{xo} - v_{yo} \quad (4.5)$$

Moreover, the TCMV equation can also be realized with the aid of Millman's theorem as follows [158]:

$$v_{Pg} = V_{PV} + V_{C4} - V_{eqv} \quad (4.6)$$

where,

$$v_{eqv} = v_{CMV} + \frac{(L_2 - L_1)}{2(L_1 + L_2)} v_{xy} = v_{CMV} - \frac{v_{xy}}{2} \quad (4.7)$$

where, $L_2 = 0$ and $L_1 = L_f$, as the configuration is a single inductor-based topology. Now, simplifying the eqn. (4.6) and eqn. (4.7), the TCMV can be written as follows:

$$v_{Pg} = V_{PV} + V_{C4} - v_{yO} \quad (4.8)$$

The waveform of the TCMV (v_{Pg}) is shown in Figure 4.4 (f). Further, from Figure 4.4(c), the TCMV equation can be expressed in terms of i_{leak} as:

$$v_{Pg} = (R_G + R_P + \frac{1}{sC_P})i_{leak} = z_{leak} i_{leak} \quad (4.9)$$

where z_{leak} is the parasitic impedance of the PV panel. Therefore, the leakage current can also be estimated for the proposed configuration as per the following eqn.:

$$i_{leak} = \frac{v_{Pg}}{z_{leak}} = \frac{V_{PV} + V_{C4} - v_{yO}}{z_{leak}} \quad (4.10)$$

Thus, the TCMV for each switching state can be determined from eqns. (3) and (8) using the switching states listed in Table 4.1. The leakage current can also be estimated mathematically using eqn. (4.10). The critical observation from Table 4.2 is that the switching sequence S^{+2A} and S^{+2B} result in the same output voltage i.e. $2V_{PV}$ whereas the TCMV of the switching sequences are $2V_{PV}$ and V_{PV} respectively. Similarly, both of the switching sequences (S^{-2A}, S^{-2B}) output the same voltage level (i.e. $-2V_{PV}$) despite their difference in the corresponding TCMV magnitude.

It is evident that the proposed MLI configuration results in four different magnitudes in TCMV, namely $2V_{PV}$, V_{PV}, 0, $-V_{PV}$. When the inverter switches between two consecutive voltage levels, which possess two different TCMV magnitudes, switching transitions appear in the TCMV. These transitions cause leakage current. It is also observed that the maximum difference between any two magnitudes of the TCMV in consecutive levels is V_{PV}, which*1/3rd of the total DC-link voltage*, as given in the following eqn. (4.11):

$$\max(|\, v_{Pg}{}^{i} - v_{Pg}{}^{i+1} \,|) = V_{PV} \quad (4.11)$$

Table 4.2: Pole Voltages and TCMV corresponding to each Switching States

i	Sw. Seq.	v_{xo}	v_{yo}	v_{xy}	TCMV(v_{Pg})
1	S^{+3}	$3V_{PV}$	0	$3V_{PV}$	$2V_{PV}$
2	S^{+2A}	$2V_{PV}$	0	$2V_{PV}$	$2V_{PV}$
3	S^{+2B}	$3V_{PV}$	V_{PV}	$2V_{PV}$	V_{PV}
4	S^{+1}	$2V_{PV}$	V_{PV}	V_{PV}	V_{PV}
5	$S^{+0.5}$	$1.5V_{PV}$	V_{PV}	$0.5V_{PV}$	V_{PV}
6	S^{+0}	V_{PV}	V_{PV}	0	V_{PV}
7	S^{-0}	$2V_{PV}$	$2V_{PV}$	0	0
8	$S^{-0.5}$	$1.5V_{PV}$	$2V_{PV}$	$-0.5\ V_{PV}$	0
9	S^{-1}	V_{PV}	$2V_{PV}$	$-V_{PV}$	0
10	S^{-2A}	0	$2V_{PV}$	$-2V_{PV}$	0
11	S^{-2B}	V_{PV}	$3V_{PV}$	$-2V_{PV}$	$-V_{PV}$
12	S^{-3}	0	$3V_{PV}$	$-3V_{PV}$	$-V_{PV}$

4.4 Voltage Boosting Scheme

In this chapter, a time-sharing-based PWM is employed for the front-end symmetrical interleaved buck-boost converter to charge the SCs from the PV source with reduced peak current stress on the semiconductor devices. The implementation of the control logic for the upper and lower section of the boosting circuit is given in Figure 4.5 (a). Further, the converter is always made to operate in the discontinuous mode of conduction (DCM) by an appropriate choice of the energy storage inductors (L_1 and L_2) pertaining to the boosting stage [132]. In DCM, whenever the inductor current fallbacks to zero (Figure 4.5 (d)), the trapped energy in the inductors is dissipated in each switching cycle. It may be noted that, when operated in DCM, the switch and diode are both operated in ZCS during the turn-on and turn-off times respectively. This eventually leads to the reduction of the switching power loss incurred in semiconductor devices. Furthermore, the operation in DCM results in smaller values of the inductors. Consequently, the RHP-zero associated with the system transfer function is placed far to the right compared to the switching frequency [78]. Hence a simple PI regulator-based voltage mode control can be implemented to regulate the voltages at the SCs (C_1, C_4). The PWM pulses for the switches S_U and S_L are finally generated after the 'AND' operation of pulses obtained after the comparison with respective carrier signals (v_{carr1} and v_{carr2}) and the corresponding utilization signals of SC's (i.e. s_{C1} and s_{C4}), which are based on the modes of operation as explained in section 4.2. It is also evident from Figure 4.5 (a) and (b) that, L_1

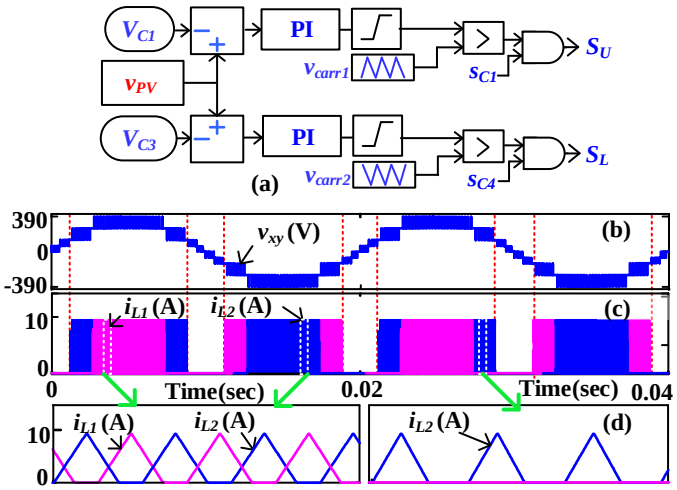


Figure 4.5: (a) Closed-loop control strategy for voltage boosting, (b) inverter output voltage (v_{xy}), (c) inductor currents (i_{L1}, i_{L2}), (d) zoomed view of (i_{L1}, i_{L2}).

supplies boosted energy in $+3V_{PV}$, $+2V_{PV,}$ and $-3V_{PV}$ states, whereas L_2 supplies it in $+2V_{PV}$, $-2V_{PV,}$ and $-3V_{PV}$ states. The closed-loop control also regulates the voltage across the SCs during the dynamic operation of the inverter.

4.5 Analysis of Proposed Modulation Strategy

4.5.1 Implementation of Proposed Modulation Strategy

The phase-disposition sinusoidal pulse width modulation (PDSPWM) method is widely used for MLIs due to their superior harmonic performance and ease of implementation with commercial digital controllers [159]. A modified PDSPWM is employed for the proposed inverter configuration as shown in Figure 4.6 (b). It can be observed that a modified sinusoidal modulation wave is compared with a triangular carrier to generate all nine voltage levels. The modified signal (v_{mod}) is synthesized from the fundamental modulation signal (r) with a modulation index m_a,

$$r = m_a \sin \omega t \tag{4.12}$$

The modified modulation (v_{mod}) waveform can be written as per the following equation,

$$v_{\text{mod}} = 6|r|z_1 + (6|r|-1)z_2 + (3|r|-1)z_3 + (3|r|-2)z_4 \tag{4.13}$$

where, z_1 =1 when ($0 \le 6|r|<1$); z_2 =1 when ($0 \le 6|r|-1<1$); z_3 =1 when ($0 \le 3|r|-1<1$); z_4 =1 when ($0 \le 3|r|-2<1$); z_s =1 when ($r>0$). Further, all nine voltage levels are grouped into eight zones (R_1, R_2, …R_8) based on the values of the z_1, z_2, z_3, z_4, and z_s as given in the Table 4.3.

Table 4.3: Logic Truth Table for Identification of Zone Of Operation

Zones	z_s	z_1	z_2	z_3	z_4
Region - 1 (R_1)	**1**	0	0	0	**1**
Region - 2 (R_2)	**1**	0	0	**1**	0
Region - 3 (R_3)	**1**	0	**1**	0	0
Region - 4 (R_4)	**1**	**1**	0	0	0
Region - 5 (R_5)	0	**1**	0	0	0
Region - 6 (R_6)	0	0	**1**	0	0
Region - 7 (R_7)	0	0	0	**1**	0
Region - 8 (R_8)	0	0	0	0	**1**

A typical switching sequence showing the voltage levels corresponding to the aforementioned 8 zones is shown in Figure 4.6 (a). The modified reference signal and the generation of PWM signals for each switch are shown in Figure 4.6 (b). The PWM modulator is programmed to output the switching sequence corresponding to each zone. These sequences can be selected independently from the available switching combinations (as given in Table 4.1). It may be noted from Figure 4.6 (b) that, each zone comprises two consecutive voltage levels. To avoid the voltage transitions across the parasitic capacitor (C_P), the adjacent voltage levels in any given zone should have an identical magnitude of TCMV. The proposed PWM strategy realizes this objective by an appropriate selection of switching sequences, as suggested in Table 4.2. Thus, the proposed PWM is capable of eliminating all switching frequency transitions in each operating zone, which reduces the RMS value of the leakage current. In general, in a closed-loop PV system, the output of the MPPT controller determines the modulation index (m_a) for the inverter. Figure 4.7, which shows the block diagram for the implementation of the proposed modulation technique, indicates that the modulation index is input to this block diagram to generate the switching pulses for the inverter.

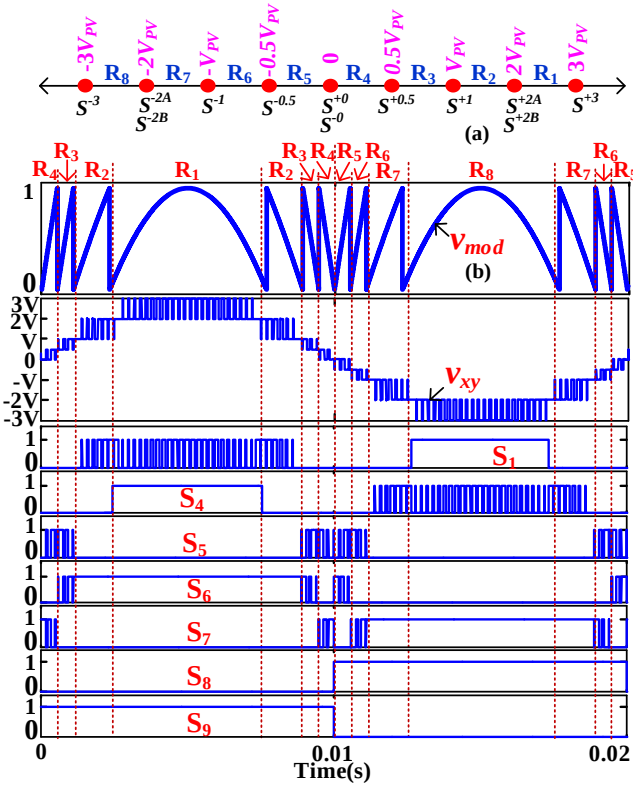


Figure 4.6: (a) Eight regions in output voltage vector, (b) generation of the modified modulation signal and the PWM signals for the switches.

Further, to operate the proposed inverter configuration in the grid-tie mode, a similar control scheme is implemented as described in Figure 3.9. The P&O-based MPPT algorithm along with the PR current controller is also implemented as described in sub-section 3.3.2. The output of the PR current controller is employed as the fundamental modulation signal (v_m), which is further processed to synthesize the modified modulation waveform (v_{mod}) as shown in Figure 4.7.

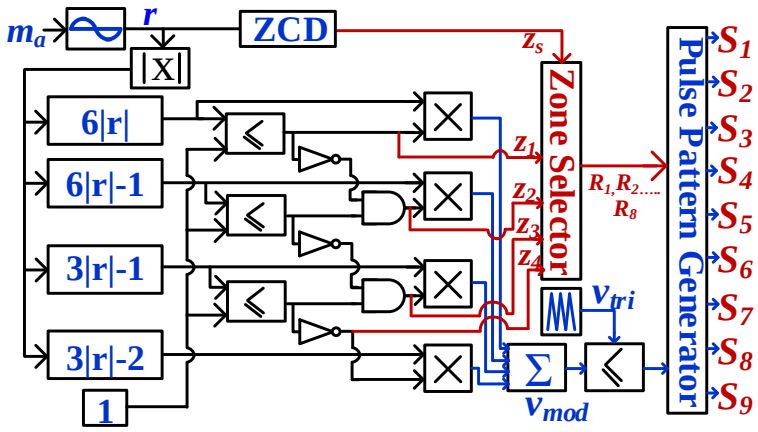


Figure 4.7: The block diagram of the proposed modulation technique.

4.5.2 Comparison with Conventional SPWM Strategy

The number of transitions in TCMV is determined for both conventional SPWM [86, 159] and the proposed PWM technique. When the conventional SPWM technique is used, the switching sequence for a particular voltage level is chosen irrespective of the zone of operation. This leads to affect the zones R_1, R_5, and R_8 with high-frequency (switching frequency) voltage transitions in TCMV. The voltage transitions in each switching period in zones R_1, R_5, and R_8 for the proposed PWM technique and conventional SPWM technique are shown in Figure 4.8. With the conventional PWM, in zone R_1, the output voltage switches between $3V_{PV}$ and $2V_{PV}$, and simultaneously, the TCMV switches between $2V_{PV}$ and V_{PV}. Hence, with the conventional SPWM technique, during zone R_1, TCMV displays *two transitions in each switching period*. Further, to find out the total number of voltage transitions in a fundamental cycle, the period of each zone and its relationship with the switching frequency of the inverter (f_{swi}) are determined. The number of transitions in zone R_1 would then corresponds to 11 times that of the value of switching frequency ($11f_{swi}$, where f_{swi} inverter switching frequency in kHz). In contrast, no transitions are encountered when the

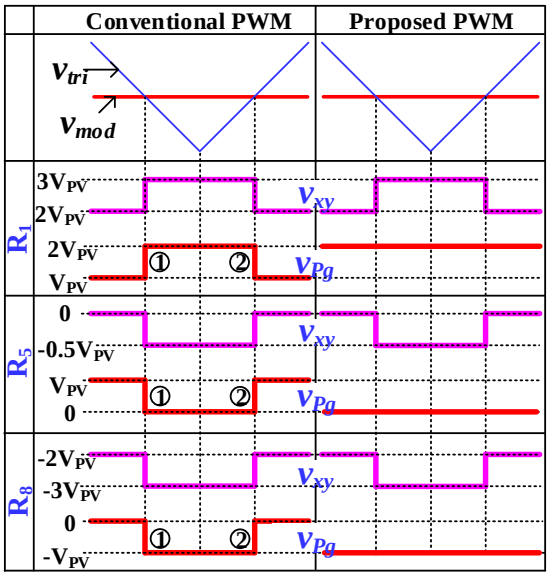


Figure 4.8: Number of voltage transitions during each switching cycle in the output voltage (v_{xy}) and the TCMV (v_{Pg}) for the zones R_1, R_5, and R_8.

proposed PWM technique is employed, as shown in Table 4.4. A similar number of transitions are also encountered in zone R_5 and R_8, where the TCMV switches between V_{PV} to 0 and 0 to $-V_{PV}$ respectively. Table 4.4 presents the total number of transitions in the TCMV over a fundamental cycle by summing up all the transitions in each zone In Table 4.4), the symbols **Z, N_C, N_P**, and **T** respectively denote the zone, the number of voltage transitions in TCMV with the conventional SPWM, the number of voltage transitions in TCMV with the proposed PWM, and the total number of voltage transitions in TCMV during a fundamental cycle.

It is evident from Table 4.4, that the proposed PWM technique induces only *six transitions in each fundamental cycle* in the TCMV, whereas the conventional SPWM induces

Table 4.4: Number of Voltage Transitions in a fundamental cycle

Zone of Operation	Number of Voltage Transitions with Conventional SPWM	Number of Voltage Transitions with Proposed PWM
Region - 1 (R_1)	$11f_{swi}$	0
Region - 2 (R_2)	2	2
Region - 3 (R_3)	0	0
Region - 4 (R_4)	0	0
Region - 5 (R_5)	$3f_{swi}$	2
Region - 6 (R_6)	0	0
Region - 7 (R_7)	0	0
Region - 8 (R_8)	$11f_{swi}$	2
Total	**$25f_{swi}$**	**6**

*f_{swi} (in **kHz**)

a total of $25f_{swi}$ *transitions in each fundamental cycle*. Thus, for conventional SPWM the leakage current increases with the value of the switching frequency (f_{swi}) of the inverter. In contrast, with the proposed PWM technique, the number of transitions per cycle is reduced. Also, it becomes independent of the switching frequency of the inverter.

4.5.3 Evaluation of Power Utilization Factors

From the section 4.4, it is obvious that the proposed configuration extracts the PV power in both single-stage (direct mode) and double-stage (boost modes 1 and 2) operating modes. The durations of these modes are presented in Figure 4.9 (a). In Figure 4.9 (a), the variables α, β are defined as $\alpha = \sin^{-1}(1/3)$ and $\beta = \sin^{-1}(2/3)$. The rest of the duration can be determined from the waveform symmetry. In the direct mode, the PV power is directly routed to the load through the inverter. In contrast, in boost modes 1 and 2, the power is processed through the combination of the interleaved buck-boost converters before multilevel inversion. In order to determine the ratings of the components and assess the power loss associated with the power conversion stage, the power utilization factors need to be determined. In this context, the power transferred in the direct mode (P_d) and boost modes (P_{C1}, P_{C4}) are derived using the following eqns:

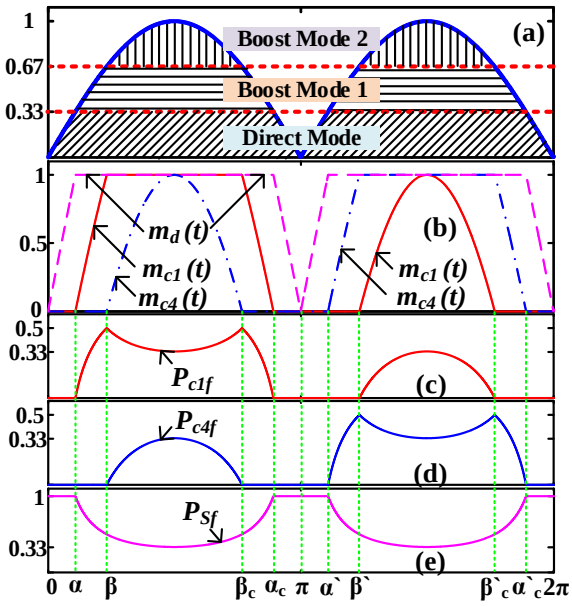


Figure 4.9: (a) Direct and boost modes of operation, (b) Modulating function for direct mode and boost modes, Power utilization factors: (c) P_{C1f} ,(d)P_{C2f} ,(e) P_{Sf}.

$$P_{C1} = m_{C1} V_{C1} i_g \tag{4.14}$$

$$P_{C4} = m_{C4} V_{C4} i_g \tag{4.15}$$

$$P_d = m_S V_{PV} i_g \tag{4.16}$$

$$i_g = I_m \sin(\omega t - \phi) \tag{4.17}$$

where V_{C1} and V_{C4} are the voltages across the SCs C_1 and C_4. The amplitude of the load current is denoted by the symbol I_m. The functions $m_d(t)$, $m_{C1}(t)$ and $m_{C4}(t)$ respectively represent the modulating function referred to the PV source in the direct mode and the two boost modes (Figure 4.9 (b)). These modulating functions can also be defined from the following equations:

$$m_S(t) = 6|r|z_1 + (z_2 + z_3 + z_4) \tag{4.18}$$

$$m_{C1}(t) = ((6|r|-1)z_2 + z_3 + z_4)z_s + (6|r|-2)(z_3 + z_4)(1 - z_s) \tag{4.19}$$

$$m_{C4}(t) = (6|r|-2)(z_3 + z_4)z_s + ((6|r|-1)z_2 + z_3 + z_4)z_s \tag{4.20}$$

The total power processed by the inverter can now be written as follows,

$$P_T = P_{C1} + P_{C4} + P_S \tag{4.21}$$

The utilization factor for the direct mode (P_{Sf}), as well as each of the boost modes (P_{C1f}, P_{C4f}), can be determined by the ratio of each power component to the total power (P_T). The waveforms of the power utilization factors corresponding to the boost modes (P_{C1f} and P_{C4f}) and direct mode (P_{Sf}) are shown in Figure 4.9 (c), (d), and (e) respectively. It can be observed that both of the SCs attain a maximum power utilization factor of 0.5. Thus, it is evident that each section of the interleaved buck-boost converter processes a maximum of 50% of the load requirement. This key observation paves the way for the selection of the components pertaining to the boosting stage of the proposed converter. Further, to determine the amount of energy processed in each mode, namely (i) direct-mode, (ii) boost modes in a given power cycle, the eqns. (4.14)-(4.16) are integrated over time. The total energy processed by the inverter can be written as follows (eqn. 4.17):

$$E_T = \int_0^{2\pi} (P_{C1} + P_{C4} + P_S) d(\omega t) \tag{4.22}$$

The energy processed in the direct mode (E_S) and boost modes (E_{C1} and E_{C4}) can also be derived from the following eqns.:

$$E_S = V_{PV} \left[4\int_0^{\alpha} m_S i_g d(\omega t) + 2\int_{\alpha}^{\pi-\alpha} i_g d(\omega t) \right] \tag{4.23}$$

$$E_{C1} = V_{PV} \left[2\int_{\alpha}^{\beta} m_{C1} i_g d(\omega t) + \int_{\beta}^{\pi-\beta} i_g d(\omega t) + \int_{\beta`}^{\pi-\beta`} m_{C1} i_g d(\omega t) \right] \tag{4.24}$$

$$E_{C4} = V_{PV} \left[\int_{\beta}^{\pi-\beta} m_{C4} i_g d(\omega t) + 2\int_{\alpha'}^{\beta`} m_{C4} i_g d(\omega t) + \int_{\beta'}^{\pi-\beta'} i_g d(\omega t) \right] \tag{4.25}$$

The average energy utilization factors over a fundamental cycle are obtained by evaluating the integrals, which appear in eqns. (4.22-4.25):

$$E_{Sf} = \frac{E_S}{E_T} \times 100\% = 41.6\% \tag{4.26}$$

$$E_{C1f} = \frac{E_{C1}}{E_T} \times 100\% = 29.2\% \tag{4.27}$$

$$E_{C4f} = \frac{E_{C4}}{E_T} \times 100\% = 29.2\% \tag{4.28}$$

It is evident from the above derived numerical values that the proposed modulation technique enables the proposed configuration to transfer an amount of 42% of the total energy in the direct mode. The rest of the 58% of the total energy is transferred through the interleaved converter. Further, the foregoing analysis reveals that each interleaving section of the converter needs to handle only 29% of the total load requirement. In contrast, the conventional boosting methods demand that the total (i.e. 100%) load power be processed through the DC-DC conversion stage. Thus, the proposed power circuit configuration reduces the effective power loss incurred in the interleaved converter, while boosting the input PV voltage. Moreover, as per the obtained numerical values in eqns. (4.26, 4.27, 4.28), it implies

that the average energies transferred in each fundamental cycle for both the SCs (C_1 and C_4) are the same. Further, the design of these SCs can be carried out using the charge balance equation and the constraint of the allowed voltage ripple as described in [160-161]. The charge balance equation for these SCs is derived using the boosted energy from the interleaved buck-boost converter and the required energy by the load.

4.6 Simulation Validation

The working principle and the performance of the proposed inverter configuration have been validated by simulation studies using the MATLAB-SIMULINK platform. The parameters used in the simulation of the proposed inverter and the associated modulation strategy are presented in Table 4.5. The passive elements in the front-end interleaved buck-boost converter and the output LCL filter are designed based on the procedure presented in section 3.4. The TCMV and the leakage current are assessed with the aid of a circuit branch consisting of parasitic elements, namely a resistance (R_p) and a capacitance (C_p). This branch is placed across the positive terminal of the PV source and the load neutral as shown in Figure 4.2. According to [142] and [162], the value of parasitic capacitance ranges between 60nF-160nF depending on the type of the PV panel and atmosphere conditions.

In order to emphasize the benefits of the proposed PWM technique, these simulation results are compared with those obtained with conventional SPWM for the proposed 9L-T-HBI with identical parameters. Besides that, to acquire a 230V (RMS) at the inverter output, the required voltage at the DC-link is 400V. The required input voltage is estimated to be around 130-140V, as the input voltage is boosted using the interleaved front-end buck-boost converter with a gain factor of three. Thus, a PV array with a maximum power point (MPP) voltage of 130V is considered to be the input voltage for the inverter. The output voltage

Table 4.5: Circuit Parameters for Simulation Validation

Parameter	Values	Parameter	Values
V_{PV}	130 V	C_1, C_4	470 uF
$V_{DC\text{-}link}$	400 V	C_2 , C_3	1 mF
P_{rated}	1.5 kW	L_1 ,L_2	0.5 mH
f_m	50 Hz	L_f, L_g	2.5 mH
f_{swi}	5kHz	C_f	0.1 uF
f_{swb}	10kHz	R_p,C_p	10 Ω,100nF

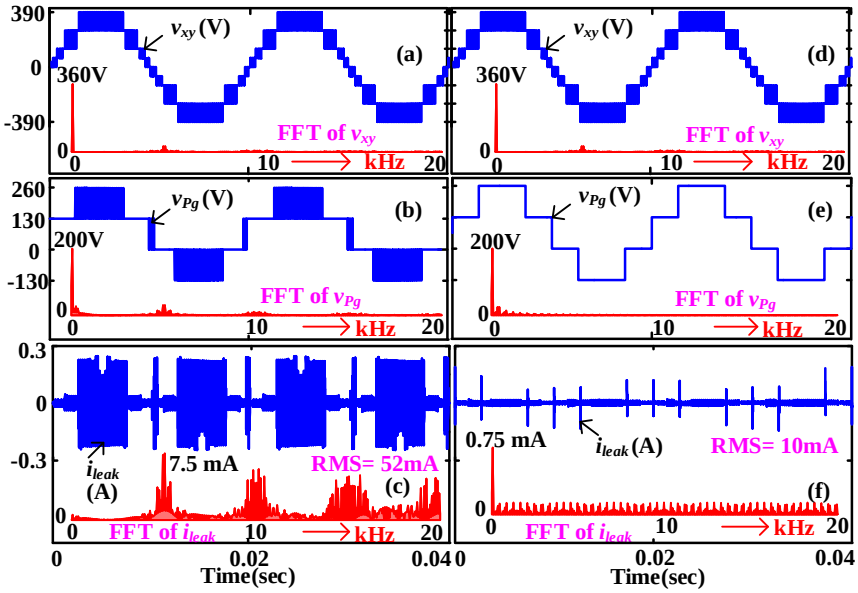


Figure 4.10: Simulated results: (a) v_{xy} (b) v_{Pg} (c)i_{leak} for conventional SPWM, (d) v_{xy} (e)v_{Pg} (f)i_{leak} for proposed PWM technique at m_a = 0.9.

waveforms display nine distinct voltage levels, namely: ±390V, ±260V, ±130V, ±65V, and 0. The output voltage (v_{xy}) spectra obtained with these two modulation techniques (Figure 10 (a) and (d)) are identical. Significant harmonic components occur at frequencies corresponding to the integral multiples of the inverter switching frequency (f_{swi}), facilitating the criterion to design the filter inductor [160]. It is important to note that, when the conventional SPWM is employed, high-frequency voltage transitions appear in TCMV. In comparison, the proposed PWM strategy succeeds in eliminating the high-frequency transitions, as is evident from Figure 4.10 (b), (e). TCMV obtained with the proposed PWM strategy contains only *six transitions*, wherein the magnitude of each transition is *1/3rd of the total DC-link voltage* (i.e., 130V). Consequently, the leakage current would also display only six spikes in its waveform (Figure 4.10 (f)). The obtained RMS value of the leakage current is only 10mA, which is well below the limit of 30mA, stipulated by *VDE0126-1-1* [142], [156]. In contrast, the RMS value of the leakage current caused by the application of the SPWM scheme is 52mA, which is so large as to violate the *VDE-0126-1-1* standard.

4.7 Experimental Validation

To provide experimental validation for the proposed 9L-T-HBI configuration and the associated control algorithm, a scaled-down hardware prototype has been developed (Figure

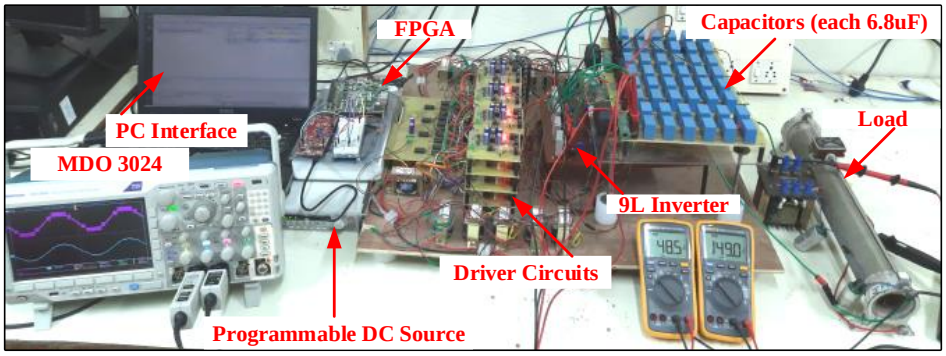


Figure 4.11: Laboratory prototype for the proposed 9L-T-HBI configuration.

Table 4.6: Circuit Parameters for Experimental Prototype

Parameter	Values	Parameter	Values
V_{PV}	60 V	C_1, C_4	24 × 6.8 uF =160uF
$V_{DC\text{-}link}$	180 V	C_2 , C_3	1 mF
VA_{rated}	500VA	L_1 ,L_2	0.5 mH
f_m	50 Hz	L_f	2 mH
f_{swi}	5kHz	C_f	0.1 uF
f_{swb}	10kHz	R_p,C_p	10 Ω,100nF

4.11). The circuit parameters and operating conditions are presented in Table 4.6. The following power semiconductor switching devices are used for the fabrication of the proposed power circuit configuration: IRF 840 (S_1, S_2…S_9), IRF 460 (S_{UP}, S_{LP}), and MBR1520 (D_1, D_2). The prototype is fed by a programmable DC source, which emulates the characteristic of a PV source [60, 94]. Each SC consists of a bank of 24 capacitors (Metalized polyester type, each 6.8uF). The proposed modulation strategy is implemented with a Spartan 6 FPGA platform. The equivalent parasitic impedance of the PV panel is connected across the load neutral terminal and the source positive terminal, which consists of resistance (R_p) with a series capacitor (C_p). The dynamic performance of the prototype at unity power factor (UPF) is assessed by connecting a resistive load, which is switched between required values of resistance [131]. Similarly, the reactive power capability is demonstrated with an equivalent RL-load corresponding to a PF of 0.8 (lag) as suggested in [89]. Further, the ratings of the passive components such as the DC-link capacitors, and filter inductors are calculated using the procedures laid out in [163].

To demonstrate the advantage obtained with the proposed PWM strategy compared to the conventional SPWM technique, both of these PWMs are applied to the proposed power

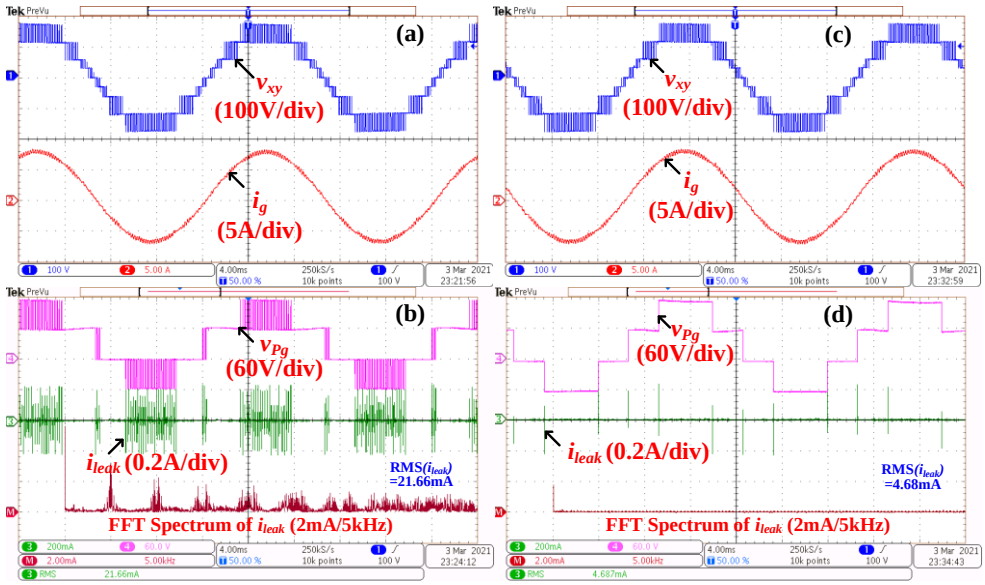


Figure 4.12: Experimental results: (a)v_{xy}, i_g (b)v_{Pg}, i_{leak} for conventional SPWM, (c)v_{xy}, i_g (d) v_{Pg}, i_{leak} for proposed PWM technique.

converter. Figure 4.12 (a) and (c) show that the output voltage waveforms with either of these modulation techniques are identical. Thus, the proposed converter and the proposed modulation technique retain all of the advantages obtained with the conventional MLIs such as reduced *dv/dt* stresses across the switches and reduction in the size of filters. Also, the THDs of the load current for both of the modulation techniques are the same (1.05%). However, the TCMV waveform shows high-frequency voltage transitions (corresponding to the switching frequency) when the conventional SPWM is used. In contrast, with the proposed modulation strategy, the TCMV oscillates at the fundamental frequency. It is well known that the presence of the voltage transitions in the TCMV waveform causes the leakage current as $i_{leak} = C_{pv} (dv_{Pg}/dt)$. It can be observed that the TCMV waveforms have *six transitions* in a given fundamental cycle. With identical values of the switching frequency (5 kHz), input voltage (60V), and other circuit parameters, the proposed PWM results in a much lower RMS value of the leakage current (4.68mA, RMS) compared to the one obtained with the conventional SPWM (21.66 mA, RMS). Thus, the RMS value of the leakage current obtained with the proposed PWM is about 4.5 times lesser than the one obtained with the conventional SPWM technique. It is also observed from Figure 4.12 (b) that the harmonic spectrum of leakage current obtained with the conventional SPWM contains significant peaks at f_{swi} and its higher-order multiples. Thus, it is evident that the size and order of the common-mode choke and EMI filters are reduced with the proposed configuration. These experimental

results are in agreement with the simulation results, validating the operation and the working principle of the proposed power circuit configuration and the associated control algorithm.

Another set of experimental results has also been presented, corresponding to the modulation index (m_a) of 0.9, to validate the voltage boosting capability for the proposed power converter. The nine distinct voltage levels output by the proposed 9L-T-HBI, namely, ±180V, ±120V, ±60V, ±30V, and 0 can easily be distinguished in Figure 4.13 (a). The employed PI controllers regulate the voltages of the SCs (V_{C1} and V_{C4}). The proportional gain (k_{pv}) and integral gain (k_{iv}) for each of the PI controllers are designed with the help of the SISO toolbox in MATLAB. The overall voltage-mode control scheme for the front-end converter is designed to achieve a gain margin of 10.8 db and a phase margin of 58^0 to ensure the stability of the system. It is observed from Figure 4.13 (b) that, the voltage of the SCs (C_1 and C_4) are regulated at 60V. It is observed that the boosting circuit delivers power only when the inverter outputs more than ±60V. This helps in balancing the voltages and reducing the power loss. Further, as an interleaved PWM is used for the buck-boost stage, the inductor currents (i_{L1}, i_{L2}) appear to be anti-phased with reference to each other as shown in the zoomed

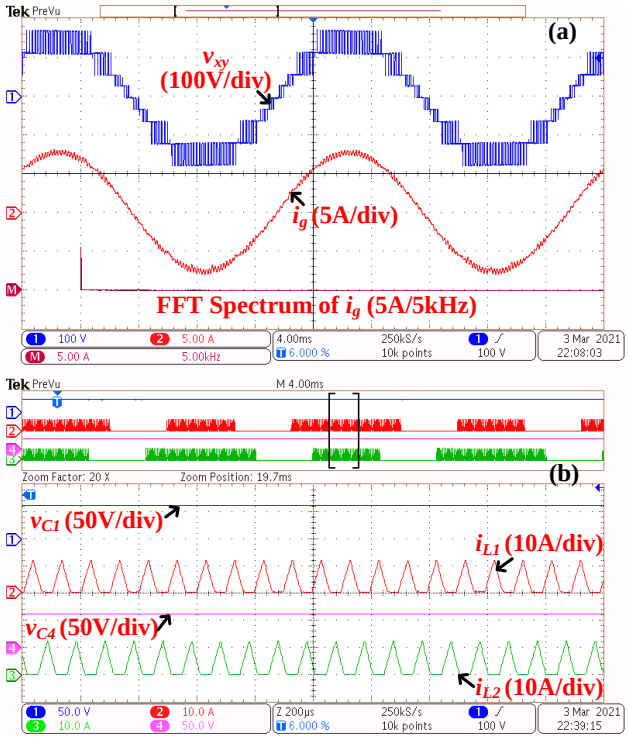


Figure 4.13: Experimental results: (a) v_{xy}, i_g (b) v_{C1}, v_{C4}, i_{L1} ,i_{L2} for proposed PWM technique at m_a=0.9.

view of Figure 4.13 (b).

Further, the voltage regulation of the SCs with load variation is demonstrated. Figure 4.14(a) presents the transient response of the load current when the peak load current reference is suddenly varied from 4A to 7A. This results in shifting the operating point on the PV characteristic and eventually, the PV voltage (v_{PV}) undergoes a small change (~2V). It is observed that, following the load disturbance, each of these two SC voltages is individually regulated to the PV voltage (v_{PV}) (i.e. around 60V) and the voltage controller restores the voltage across the two SCs (i.e. v_{C1} and $v_{C4,}$) in less than 20ms. Also, the inverter output voltage (v_{xy}) does not suffer any distortion during this transient condition as demonstrated in the experimental result shown in Figure 4.14 (b). To further test the dynamic response of the proposed power converter, , the load on the converter is suddenly changed from UPF to a lagging load with a PF of 0.8. The experimental result, presented in Figure 4.14 (c) reveals that the controller handles even this condition well, as no apparent distortion in the output waveform is observed. Further, this experiment shows that the voltages across the SCs are

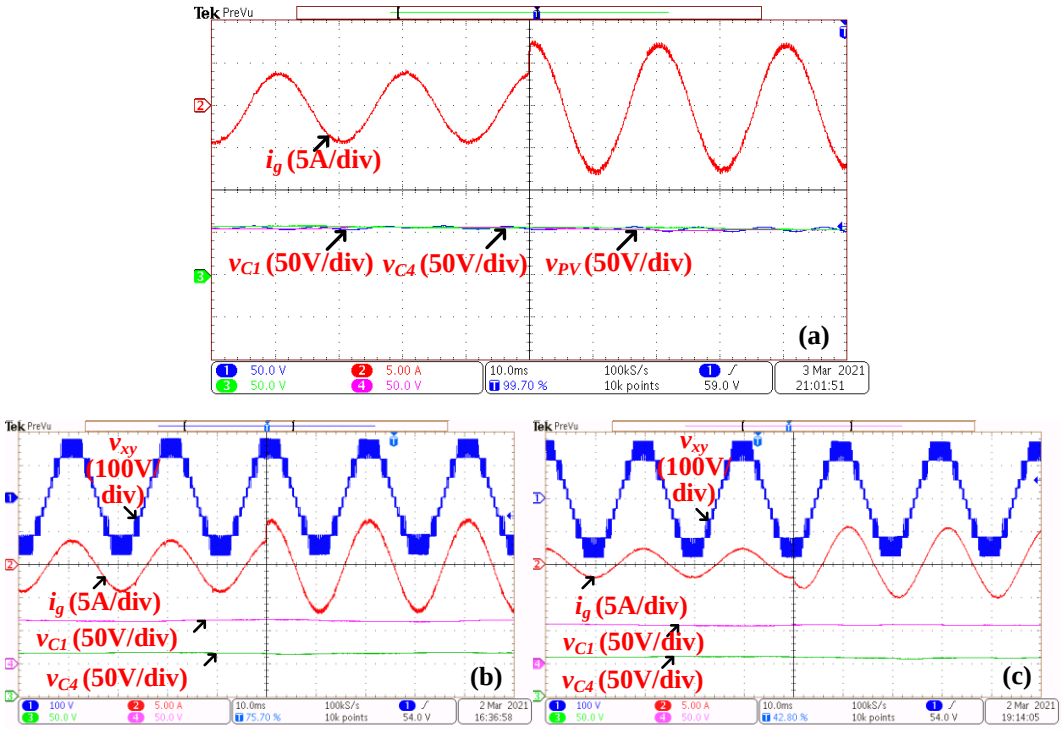


Figure 4.14: Experimental results for the dynamic response of the (a) voltages across the SCs (V_{C1}, V_{C4}) at step change of load current (ig), (b) v_{xy}, i_g, V_{C1}, V_{C4} captured for load dynamics with UPF, (c) v_{xy}, i_g, V_{C1}, V_{C4} captured for load dynamics with PF=0.8.

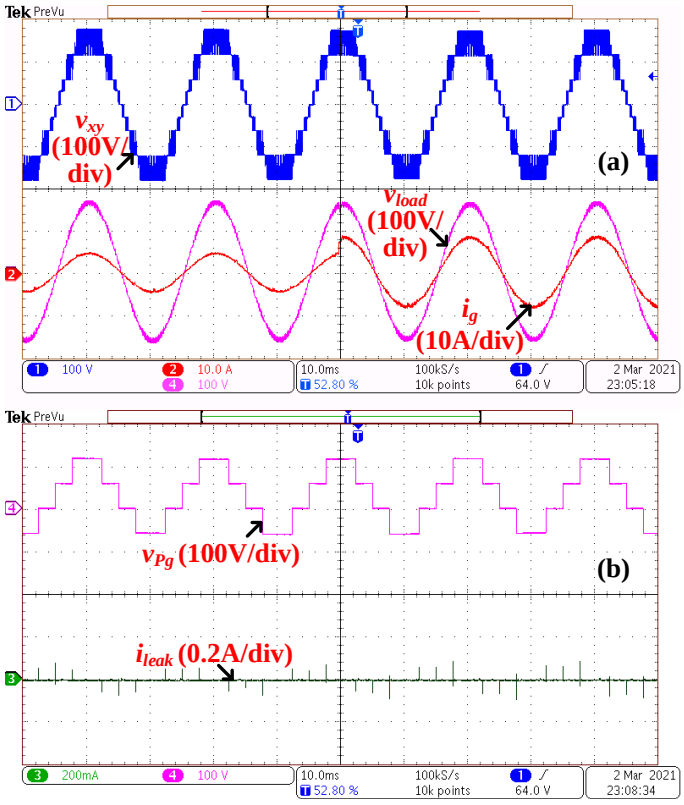


Figure 4.15: Experimental results for the dynamic load change of the proposed configuration with the proposed modulation technique: (a) v_{xy}, v_{load}, i_g, (b) v_{Pg}, i_{leak} at UPF.

regulated for this condition as well.

Figure 4.15 shows the dynamic performance of the proposed 9L-T-HBI when the reference of the peak load current is altered from 4A to 8A. The waveforms of the inverter output voltage (v_{xy}), the load current (i_g), the voltage across the load (v_{load}), total common-mode voltage (v_{Pg}), and leakage current (i_{leak}) are shown (Figure 4.15). It is seen from Figure 4.15 (a) that, despite the load disturbance, the waveform of the inverter output voltage remains identical. This demonstrates the regulating capability of the controller against disturbances. From Figure 4.15 (b), it is evident that both the TCMV and the leakage current remain unaltered. Thus, it is demonstrated that the proposed configuration is capable of reducing the leakage current, independent of the magnitude and the nature of the load current.

Further, in order to verify the reactive power sourcing capability of the proposed 9L-T-HBI converter, an impedance corresponding to PF = 0.8 is connected across the output terminals of the inverter. The effect of the lagging load manifests as a significant phase

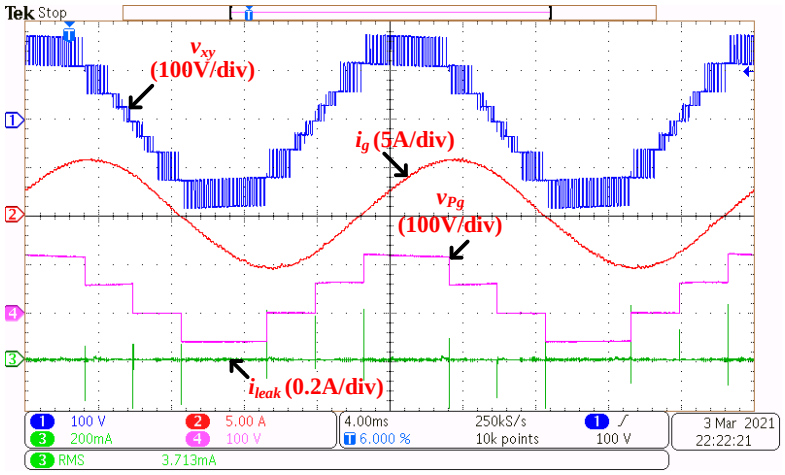


Figure 4.16: Experimental results: v_{xy}, i_g, v_{Pg}, i_{leak} with lagging load (PF=0.8).

difference between the inverter output voltage and load current (Figure 4.16). It can be observed that the performance of the total common-mode voltage and the leakage current are unaltered compared to the results obtained for unity PF load. Therefore, it is evident that the proposed inverter configuration is capable of delivering active as well as reactive power without sacrificing either the quality of the output waveform or the reduction in the leakage current.

The experimental efficiency of the proposed configuration is measured with a precision digital power meter (*Yokogawa WT332E*). The measurement of power is carried out using two isolated channels of this meter. These two channels respectively provide data regarding the voltage and power at the input and the output of the proposed power converter (Figure 4.17 (b)). Figure 4.17 (a) shows the voltage (v_{xy}), current (i_g), TCMV (v_{Pg}), and leakage current (i_{leak}) at the output of the inverter. In order to measure the power, THD, and the PF at the output of the inverter, a single-phase power analyzer (*UNI-T UT283A*) is also connected at the output of the inverter. Figure 4.17 (b) shows the measurements of the PV voltage (v_{PV}), the RMS value of inverter output voltage (v_{xy}), the input power to the inverter (P_{in}), and the output ac power (P_{out}). From these measured values, the efficiency of the inverter is obtained as 94.90% at the given operating condition (the output power, P_{out} = 508 W). It may also be noted that the obtained THD of the load current is also well within the limit of the

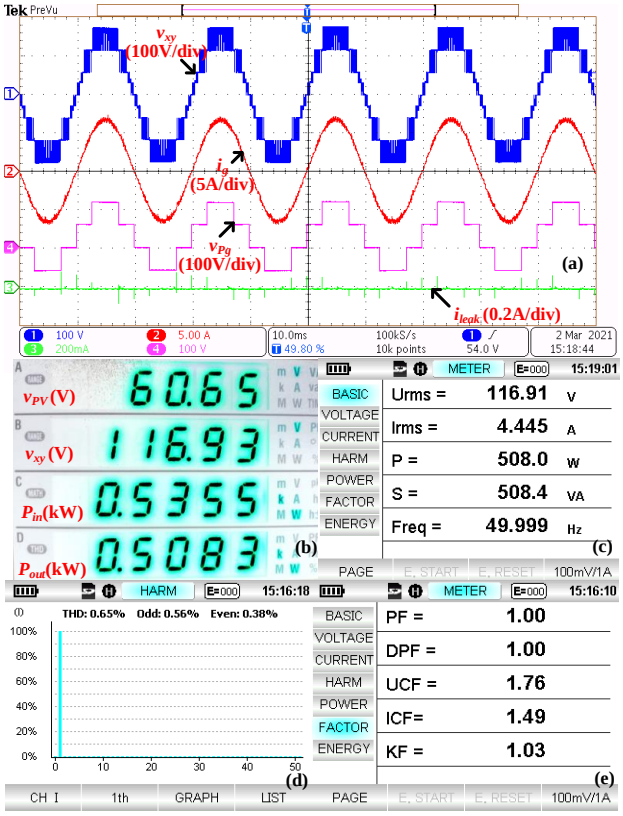


Figure 4.17: Experimental results: (a) v_{xy}, i_g, v_{Pg}, $i_{leak,}$ (b) measurements of input PV voltage (v_{PV}), RMS of inverter output voltage (v_{xy}), input power to the inverter (P_{in}), output ac power (P_{out}) from the digital power meter (c) RMS of the inverter voltage, Active power (P), apparent power (S), (d) THD and harmonic spectrum of the load current at P_{out} =508W, (e) PF of the load.

IEEE-1547-2018 standards (Figure 4.17 (d)). It is envisaged that the efficiency can be further improved at higher power ratings by improving the design of the magnetic components and the use of advanced power semiconductor switching devices.

Further, the performance of the inverter is validated in the grid-tie condition. The current loop is designed based on the inverter parameters listed in Table 4.6. The values for proportional gain (*kpc*) and resonant gain (*krc*) for the current control loop are obtained using the SISO Toolbox of MATLAB. The value of *kpc* and *krc* are obtained as 0.081 and 4.231 respectively for the proposed power converter. To ensure stability and a good dynamic response, the controller gains are selected to achieve gain margin and phase margin of the overall system as 11.6 dB and 60.9^0 respectively as shown in Figure 4.18. The effectiveness of the current controller is also evident in Figure 4.19, which demonstrates the operation of the proposed configuration to inject power into the grid. The proposed configuration injects a current of 6A(peak) at UPF.

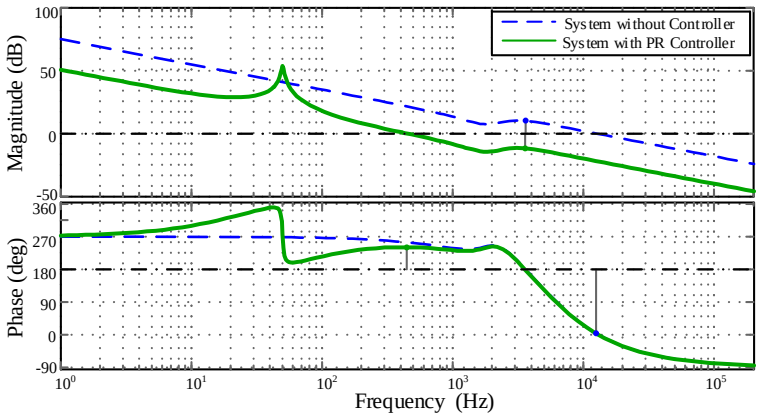


Figure 4.18: Bode plot for PR controller and the proposed nine level boost inverter.

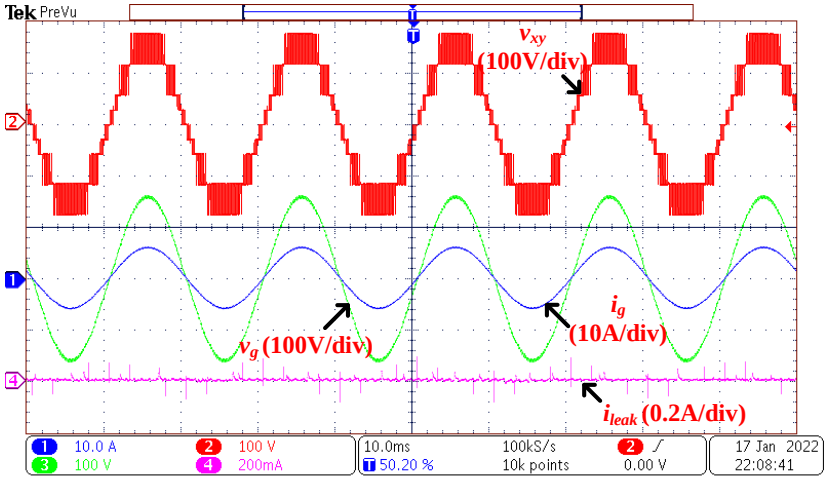


Figure 4.19: Experimental results: inverter output voltage (v_{xy}), grid-voltage (v_g), grid-current (i_g) and leakage current (i_{leak}).

4.8 Comparison with Existing Transformerless Inverter Topologies

The performance of the proposed 9L-T-HBI configuration vis-à-vis the recently reported topologies is compared to demonstrate its benefits and features. Table 4.7 presents various parameters for which the performances are compared. The literature available on 9L transformerless inverter topologies, which require one PV source and simultaneously achieve reactive power sourcing capability and mitigation of leakage current, is scanty. In view of this, *single PV source*-based 7L and 5L inverter topologies are also considered for comparison. The topologies presented in [60] and [72] employ an additional voltage boosting stage to achieve the required voltage boosting capability. Hence, these topologies incur higher power losses (Figure 4.20) in the boosting inductors, as the boosting stage is constrained to

transfer the entire power from the PV source to the load. The topology presented in [99], addresses this problem with the introduction of a novel boosting technique, which partially reduces the power losses in the boosting inductors. However, the PWM technique used in this work [99] causes a high (*dv/dt*) across the inverter switches. Though the topology described in [164] synthesizes 9 levels and displays a better leakage current reduction, it lacks boosting capability and requires a higher input voltage. Further, 9-level topologies are proposed in [147] and [165], which achieve voltage boosting as well as a multilevel operation by the employment of SCs. However, in these converters, the switching devices are subject to higher current stress due to the hard-charging of the SCs, calling for a conservative selection of the switching devices. This would further affect the energy density of the converter. In contrast, the proposed topology alleviates the current stress on the switching devices, as the SCs are

Table 4.7: Comparison of the Proposed 9L-T-HBI with Existing Topologies

	[60] -5L	**[72] -5L**	**[99] -5L**	**[86] -7L**	**[164] -9L**	**[147] -9L**	**[165] -9L**	**9L-T- -HBI**
A	7	8+4	9+1	10	10	19+3	8+3	12+2
B	2	4	2	4	3	3	3	4
C	0	2	1	0	1CI$^{\#}$	0	0	2
D	400	200	200	267	800	133	100	133
E	5.5	5	7.5	7.3	8	4.75	5.75	8
F	-	-	Soft	Hard	Soft	Hard	Hard	Soft
G	1-2I_m	1-2I_m	2-3I_m	5-6I_m	1-2I_m	5-6I_m	5-6I_m	2-3I_m
H	f_o	f_o	f_o	0	0	f_{sw}	f_{sw}	f_o
I	2.8	410	110	2.2	3.5	73	820	10
J	small	high	high	small	small	high	high	small
K	No	No	Yes	Yes	Yes	Yes	Yes	Yes
L	43.5	27.4	27.1	19.4	15.1	14.8	13.7	18.5
M	3.2	2.9	2.9	2.0	1.7	1.6	1.5	2.1

A: (Number of switches + Number of diodes);
B: Number of capacitors;
C: Number of inductors;
D (in volt): Required input voltage for 230V$_{rms}$ application;
E: Total standing voltage in per unit. (with respect to the peak value of the output voltage);
F: hard-charging or soft-charging of the SCs;
G: Peak current stress of the semiconductor devices in voltage boosting path,
H: TCMV frequency,
I (in mA): RMS of leakage current,
J: Requirement of additional common mode filter,
K: Capability of reactive power exchange.
where f_o is grid-frequency, f_{sw} is switching-frequency, I_m peak value of the grid-current, CI$^{\#}$ is coupled inductor.
L: THD (in %) of the output voltage.
M: THD (in %) of the load current.

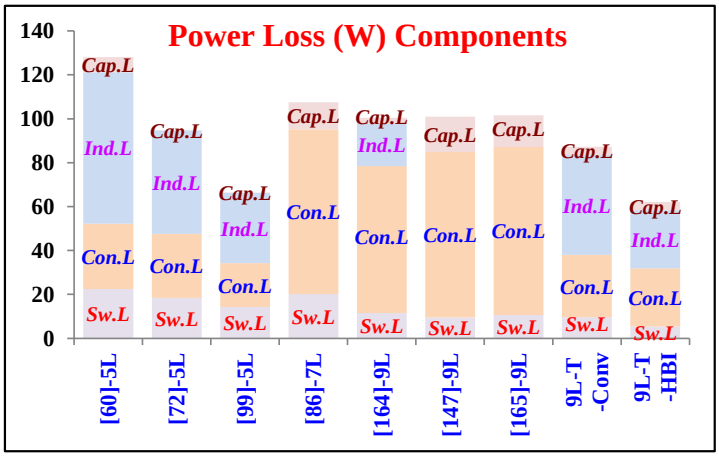


Figure 4.20: Comparison of power losses ((i) switching power loss (*Sw.L*), (ii) conduction loss (*Con.L*) of all semiconductor devices, (iii) inductor ohmic loss (*Ind.L*) and (iv) capacitor ESR loss (*Cap.L*)) of the inverter configurations.

charged softly through the inductor while achieving a boost factor of three.

Using the theoretical power loss equations [77], the efficiency of the proposed power converter can be assessed. The recent trend in this direction is to employ a PLECS simulation to evaluate various components of the power losses [163-165]. Thus, a comparative simulation study of the proposed power converter is implemented in PLECS simulation software using the thermal model of the semiconductor devices IKW30N60T (Figure 4.20). In order to facilitate a fair comparison, all configurations are analyzed with an input voltage of 130V and an output power of 1.5kW. However, for those topologies, which do not possess the voltage-boosting capability, a conventional voltage boosting stage is incorporated as suggested in [119], [89]. Further, the power losses incurred with the conventional voltage boosting technique (i.e., conventional boost converter) with the nine-level T-type inverter are also evaluated (9L-T-Conv) and presented in Figure 4.20. The power loss incurred for the proposed configuration is indicated as 9L-T-HBI in Figure 4.20.

Figure 4.21 presents the simulated and experimentally obtained efficiencies of the proposed 9L-T-HBI configuration. The efficiency is measured at power output ranging from 100W to 500 W in steps of 100W. It may be noted that the experimentally obtained efficiencies are in close agreement with their simulated counterparts. Further, at the rated condition, the scaled-down laboratory prototype results in an efficiency of 95% (approx.), which is close to the efficiency obtained through the simulation study.

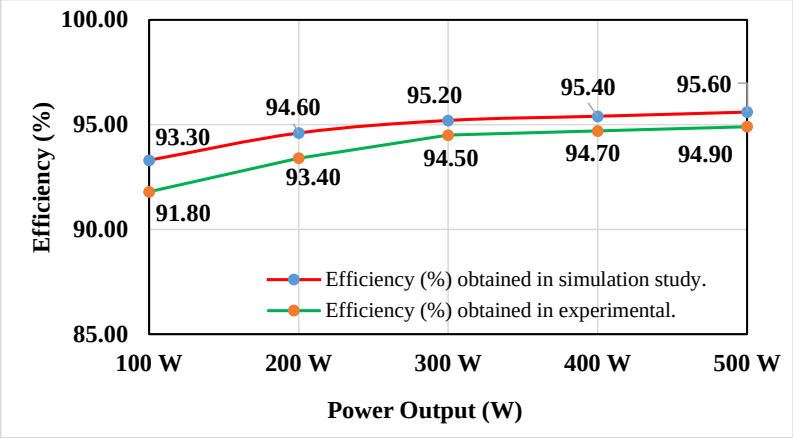


Figure 4.21: Comparative efficiency plot of the proposed 9L-T-HBI configuration ranging from 100W to 500W obtained in the simulation study and measured in the experiment.

4.9 Conclusion

In this chapter, a single PV source-based 9L-T-HBI along with its PWM strategy is proposed. The proposed power converter and its associated PWM scheme achieve the dual objectives of voltage boosting and leakage current reduction. Compared to the conventional voltage boosting methodologies, the integrated boosting technique of the proposed system achieves a boosting factor of three and a reduced power loss. With the proposed power converter, a smooth transition between the single-stage and the double-stage operation is achieved while maintaining symmetric utilization of the SCs with reduced voltage ripple. The principal advantage of the proposed inverter configuration is that it achieves the direct transfer of about 42% of energy from the PV source to the load in a given fundamental cycle. Simulation and experimental results reveal that the THD of the load current is less than 2%, which is well within the IEEE-1547-2018. Besides that, as the proposed PWM technique eliminates all high-frequency voltage transitions from the TCMV, the RMS value of the leakage current is also reduced compared to the conventional SPWM modulation technique. The RMS value of the leakage current for the proposed PWM scheme is found to be well within the stipulated safety limit of the VDE-0126-1-1 standard. Owing to these features, it is envisaged that the proposed 9L-T-HBI configuration could be employed for both residential and grid-connected PV applications.

Chapter 5

Generalized PWM Schemes for MLI with Symmetrical and Asymmetrical Filters

Chapter 5

Generalized PWM Schemes for MLI with Symmetrical and Asymmetrical Filters

5.1 Introduction

The proposed configuration in Chapter 3 utilizes a symmetrical inductor filter, whereas the proposed configuration in Chapter 4 utilizes an asymmetrical inductor filter. From these investigations, it is observed that the structure of the output inductor filter affects the common-mode equivalent circuit of the inverter configuration. A similar approach was made in [144], where two different modulation schemes are presented to reduce the transitions in TCMV and common mode voltage. However, when compared to a conventional MLI, these modulation schemes result in (a) higher total harmonic distortion (THD) and, (b) higher *dv/dt* across the switches. However, the simultaneous elimination of high-frequency transitions from the TCMV as well as the CMV has not been attempted in previous research. From the comprehensive study of the existing literature, it is clear that there is a requirement to develop a multilevel single-phase transformerless inverter topology (along with an associated PWM scheme), which is capable of fulfilling the following objectives:

i) Voltage boosting capability with reduced current stress on the semiconductor devices
ii) Elimination of high-frequency switching transitions from the total common-mode voltage (TCMV) waveform exclusively with modulation technique (i.e. without any additional circuitry).
iii) Operability with a single PV source (to avoid complex multi-loop MPPT algorithms associated with multiple PV sources).
iv) Capability of handling inductive loads (similar to the conventional MLIs), without any additional clamping diodes or capacitors.

With these objectives in mind, this chapter proposes two PWM strategies for the inverter configuration introduced in [171]. While one of the proposed PWM strategies applies to the inverter with an asymmetrical filter, the other applies to its symmetrical counterpart.

The proposed single-phase inverter configuration is capable of synthesizing thirteen distinct voltage levels with a reduced number of switching devices. In addition, the proposed inverter configuration is fused with an interleaved buck-boost converter at its front-end. Thus, this power converter is capable of achieving a voltage boost factor of three with reduced current stress on semiconductor devices. In this chapter, mathematical analyses have also been carried out for the TCMV with the aid of switching functions, for both asymmetrical and symmetrical inductor-based structures. Both simulation and experimental studies confirm that the proposed PWM strategies for the proposed power converter are capable of suppressing high-frequency transitions in the total common-mode voltage.

5.2 Operation of the Proposed Circuit Configuration

The circuit diagram of the proposed multi-level inverter (MLI) configuration is presented in Figure 5.1, which is capable of realizing a thirteen-levels in its output. The inverting stage of the proposed configuration needs ten semiconductor switches to realize: (i) two half-bridge cells (with switches S_{U1}, S_{U2}, $S_{L1,}$ and S_{L2}), (ii) one polarity generator H-bridge (with switches S_{P1}, S_{P2}, $S_{P3,}$ and S_{P4}) and (iii) one switched capacitor cell (with switches S_{P5}, S_{P6}) in its structure. Besides that, the proposed power circuit configuration employs an interleaved buck-boost converter as a voltage boosting unit, which comprises two power switches (S_{b1}, S_{b2}), two inductors (L_1, L_2), two diodes (D_1, D_2), and three capacitors (C_1 – C_3). The proposed power converter is capable of synthesizing thirteen distinct voltage levels from a single PV source while achieving a voltage-boosting factor of three. In addition, the propos-

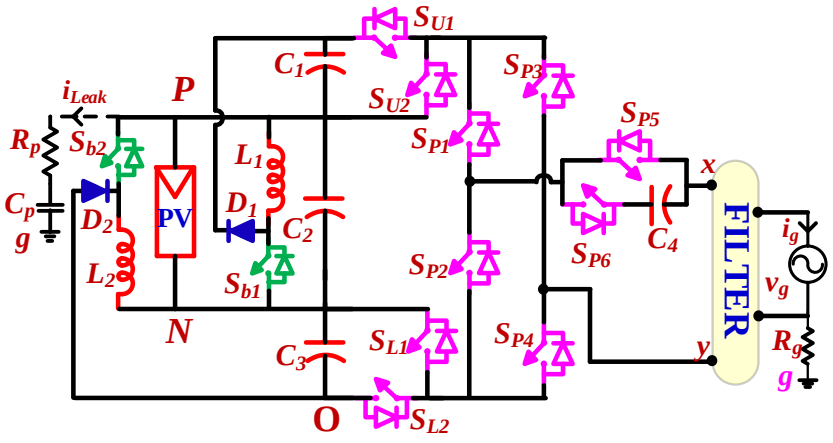


Figure 5.1: Circuit schematic of proposed 13L-HBI configuration.

-ed topology is capable of delivering a fraction of the PV power directly to the inverting stage through the capacitor C_2. A filter is connected between the output terminals of the inverter (*x* and *y*, Figure 5.1) and the grid. The parasitic elements of the PV panel, which determine the leakage current, are modeled with equivalent values of resistance (R_p) and capacitance (C_p). The parasitic branch is connected across the PV positive terminal and the ground terminal of the load (Figure 5.1). Table 5.1 summarizes the voltage levels output by the proposed configuration and the corresponding switching combinations. The turn-on and turn-off states of a switching device are represented by '1' and '0' respectively. Based on the power transferring capabilities of the proposed configuration, the modes of the operation are categorized into three modes, namely the direct-mode, the single-boosting mode, and the double-boosting mode. In the direct mode, the PV power is directly processed through the inverting stage as shown in Figure 5.2(a). The possible voltage levels in this mode are $\pm V_{PV}$ and $\pm 0.5V_{PV}$. In the double-boosting mode, both of the interleaving parts in the boosting stage are activated as shown in Fig. 5.2(b). The voltages levels obtained in this mode are $\pm 3V_{PV}$. The single-boosting mode utilizes only one of the interleaving sections in the boosting stage

Table 5.1: Switching States for Proposed Configuration

Sw. Seq.	S_{U1}	S_{L2}	S_{P1}	S_{P3}	S_{P5}	Output Voltage Level	Common-mode Voltage Level
Sq_{+3}	1	1	1	0	1	$+3V_{PV}$	$1.5V_{PV}$
$Sq_{+2.5}$	1	1	1	0	0	$+2.5V_{PV}$	$1.25V_{PV}$
Sq_{+2A}	0	1	1	0	1	$+2V_{PV}$	V_{PV}
Sq_{+2B}	1	0	1	0	1	$+2V_{PV}$	$2V_{PV}$
$Sq_{+1.5A}$	0	1	1	0	0	$+1.5V_{PV}$	$0.75V_{PV}$
$Sq_{+1.5B}$	1	0	1	0	0	$+1.5V_{PV}$	$1.75V_{PV}$
Sq_{+1}	0	0	1	0	1	$+V_{PV}$	$1.5V_{PV}$
$Sq_{+0.5}$	0	0	1	0	0	$+0.5V_{PV}$	$1.25V_{PV}$
Sq_{0}	0	0	0	0	1	0	V_{PV}
$Sq_{-0.5A}$	0	0	0	0	0	$-0.5V_{PV}$	$0.75V_{PV}$
$Sq_{-0.5B}$	0	0	1	1	0	$-0.5V_{PV}$	$1.75V_{PV}$
Sq_{-1}	0	0	0	1	1	$-V_{PV}$	$1.5V_{PV}$
$Sq_{-1.5}$	0	0	0	1	0	$-1.5V_{PV}$	$1.25V_{PV}$
Sq_{-2A}	0	1	0	1	1	$-2V_{PV}$	V_{PV}
Sq_{-2B}	1	0	0	1	1	$-2V_{PV}$	$2V_{PV}$
$Sq_{-2.5A}$	0	1	0	1	0	$-2.5V_{PV}$	$0.75V_{PV}$
$Sq_{-2.5B}$	1	0	0	1	0	$-2.5V_{PV}$	$1.75V_{PV}$
Sq_{-3}	1	1	0	1	1	$-3V_{PV}$	$1.5V_{PV}$

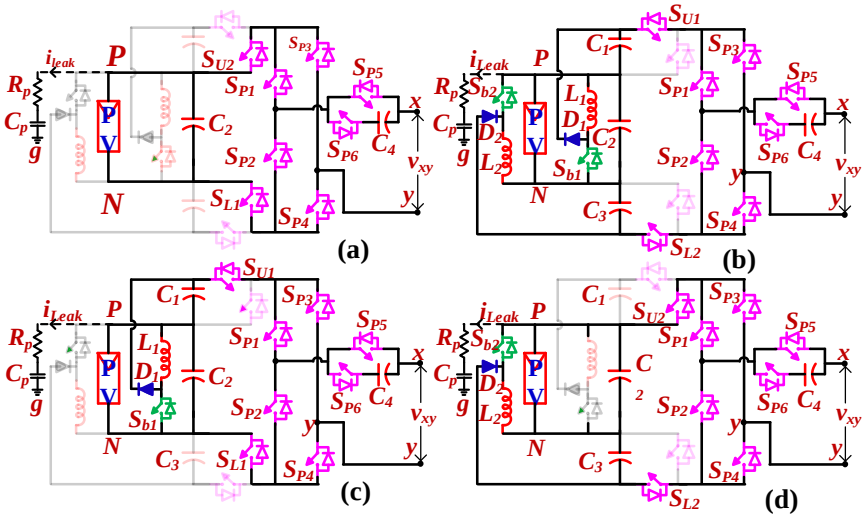


Figure 5.2: Modes of operation for the proposed 13L-HBI configuration (a) Single-stage operation, (b) double stage operation with two interleaved buck-boost converter, (c) double stage operation with upper buck-boost converter, (d) double stage operation with lower buck-boost converter.

as shown in Fig. 5.2(c) and Fig. 5.2(d). In this mode, the possible voltage levels are $\pm 2.5V_{PV,}$ $\pm 2V_{PV,}$ and $\pm 1.5V_{PV}$. Either the set of switches corresponding to the upper or lower HB cells (S_{U1}, $S_{U2,}$ or S_{L1}, S_{L2}) is operated while synthesizing a given voltage level.

5.3 Modelling of Common-mode Equivalent Circuit

Figure 5.3 (a-c) presents the common-mode equivalent circuits of the proposed power converter with an asymmetrical filter. The same is presented for a symmetrical filter in Fig. 5.3 (d-f). Switching states, as well as the filter structure (i.e. symmetrical or asymmetrical), affect the magnitude of the total common-mode voltage (v_{Pg}) and consequently the leakage current. The common-mode equivalent circuit is analyzed for both asymmetrical and symmetrical filter structures to assess their influence on the total common-mode voltage (v_{Pg}). This model is simplified using lumped circuit parameters (the resistor and capacitor) between the positive terminal of the PV panel and the ground terminal to estimate the leakage current. All of these models represent the impedance that is present between the ground and the load neutral point with the symbol R_g. The concept of *switching function* [144] is used for the proposed power converter to analyse the effect of each switching state on the leakage current, the pole voltages (v_{xo}, v_{yo}), the differential voltage (v_{xy}), and the common-mode voltage (v_{CMV}).

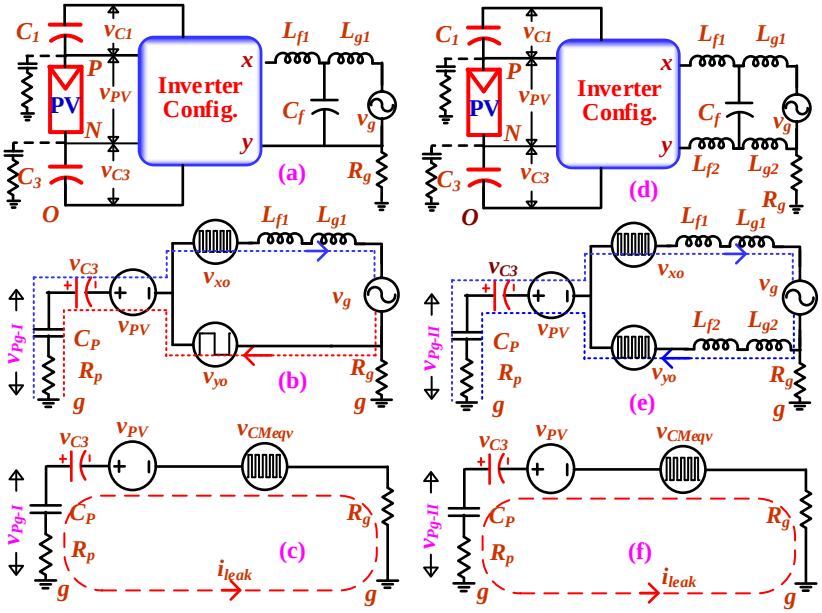


Figure 5.3: (a-c) common-mode equivalent circuit for PWM strategy - I; (d-f) common-mode equivalent circuit for PWM strategy - II.

The state of each switch of the proposed configuration is represented with a switching variable bearing the symbol *'SV_k'*, wherein the subscript *'k'* corresponds to the switches (S_{U1}, S_{L2}, S_{P1}, S_{P3}, S_{P5}). For any given switch, the switching variable SV_k assumes a value of either '1' or '0' for the turn-on and turn-off states respectively. For the proposed configuration, pole voltages, the total common-mode voltage (abbreviated as TCMV and is denoted as v_{Pg}), and the common-mode voltage (v_{CMV}) are derived by adopting the procedure described in [144]. With reference to the point 'O', the pole voltages (v_{xo}, v_{yo}) of the inverter are expressed as:

$$v_{xo} = \left[3SV_{SU1}SV_{SP1} + 2(1-SV_{SU1})SV_{SP1} + (1-SV_{SL2})(1-SV_{SP1}) - 0.5(1-SV_{SP5})\right]V_{PV} \quad (5.1)$$

$$v_{yo} = \left[3SV_{SU1}SV_{SP3} + 2(1-SV_{SU1})SV_{SP3} + (1-SV_{SL2})SV_{SP5}\right]V_{PV} \quad (5.2)$$

The output voltage (v_{xy}), which is the differential of the pole voltages and the common-mode voltage (v_{CMV}) of the proposed configuration is given by:

$$v_{xy} = v_{xo} - v_{yo} \quad (5.3)$$

$$v_{cmv} = 0.5(v_{xo} + v_{yo}) \quad (5.4)$$

As the pole voltages are measured from the reference point 'O', the equation for the TCMV (v_{Pg}) is derived in terms of the voltage across the capacitor C_3 (Fig. 5.3) and the PV source as follows,

$$v_{Pg} = v_{Po} - v_{CMeqv} \tag{5.5}$$

$$v_{Pg} = v_{PV} + v_{C3} - v_{CMeqv} \tag{5.6}$$

In eqn. (5.6), the magnitude of v_{CMeqv} depends on the common-mode voltage (v_{CMV}), output voltage, and the structure of the filter (asymmetrical/symmetrical) connected at the inverter output terminals. The expression for v_{CMeqv} is given by:

$$v_{CMeqv} = v_{CMV} + v_{xy}\left(\frac{L_{f2} - L_{f1}}{L_{f2} + L_{f1}}\right) - \frac{\beta v_g}{2} \tag{5.7}$$

In eqn. (5.7), L_{f1} and L_{f2} represent the equivalent values of the inductors connected between the inverter and load terminals. The value of β is equal to '0' for asymmetrical filters (Fig. 5.3 (b)), it is '1' for symmetrical filters (Fig. 5.3 (e)). The symbol v_g represents either the grid voltage or the load voltage for a standalone load. Simplifying eqn. (5.6) and eqn. (5.7), the TCMV for the asymmetrical filter ($v_{Pg\text{-}I}$) (Fig. 5.3 (c)) and the symmetrical filter ($v_{Pg\text{-}II}$) (Fig. 5.3 (f)) are obtained as:

$$v_{Pg-I} = v_{PV} + v_{C3} - v_{yo} \tag{5.8}$$

$$v_{Pg-II} = v_{PV} + v_{C3} - v_{CMV} + \frac{v_g}{2} \tag{5.9}$$

Based on the eqn. (5.3) and (5.4), the magnitude of the output voltage (v_{xy}) and the common-mode voltage (v_{CMV}) are determined for all switching combinations, which are summarized in Table 5.1. The parasitic voltages for the proposed configuration with asymmetrical and symmetrical filters are analyzed using the expressions presented in eqn. (5.8) and (5.9). From Table 5.1, it may be noted that the proposed configuration shows redundant switching states *i.e.* some of the voltage levels are synthesized with more than one switching combination. Though the redundant states realize the same output voltage, they result in different magnitudes of TCMV. Thus, these redundant states are exclusively used to design modulation strategies to eliminate the high-frequency transitions, corresponding to the switching frequency, from the TCMV.

5.4 PWM Strategies to Minimize the Leakage Current

The conventional level-shifted pulse width modulation (LSPWM) technique [147-165] is popular due to its improved harmonic performance and easier implementation. However, the conventional LSPWM technique induces a time-varying common-mode voltage (CMV), which results in the generation of leakage current in PV source-based applications. The CMV elimination schemes reported so far, require larger switching resources to achieve a constant CMV, compromising on the number of voltage levels. As the parasitic elements are capacitive, a path of low impedance is offered to the high-frequency transitions present in the total common-mode voltage (v_{Pg}) increasing the RMS value of the leakage current. To address this issue, the proposed power converter and its associated PWM strategies are designed to utilize the redundant states to eliminate high-frequency transitions from the TCMV (v_{Pg}) and the CMV (v_{CMV}). The PWM strategies proposed in this chapter termed PWM strategy - I and PWM strategy - II, are respectively designed for asymmetrical and symmetrical filters. Both of these PWM strategies are based on a zone-based approach for the selection of appropriate switching states to realize any given voltage level while mitigating high-frequency transitions in the TCMV.

It should be noted that the amplitudes of the modulation signals for both of the proposed modulation strategies are determined by the maximum power point tracking algorithm (ex: Perturb and Observe), which is employed for the proposed power converter. The modulating signals are represented with the symbols $v_{mod\text{-}I}$ and $v_{mod\text{-}II}$ respectively for PWM strategies – I and II.

5.4.1 Implementation of PWM Strategy - I

PWM strategy - I is designed for the proposed power converter with an asymmetrical filter (Fig. 5.3(a)). In this case, the required values of filter inductors (L_f and L_g) are kept only in the path of the line, i.e. $L_{f1} = L_f$, $L_{g1} = L_g$. In contrast, in a symmetrical filter, these inductors are equally distributed on the line side as well as the neutral side; i.e. $L_{f1}=L_f/2$, $L_{g1}=L_g/2$, and, $L_{f2}= L_f/2$, $L_{g2}= L_g/2$ (Fig. 5.3(d)). In general, the generation of gating signals for any inverter with *(2n+1)* number of levels involves a comparison of *2n* level-shifted carrier waves with a sinusoidal modulating wave. Thus, in the present situation, 12 carrier waveforms are needed

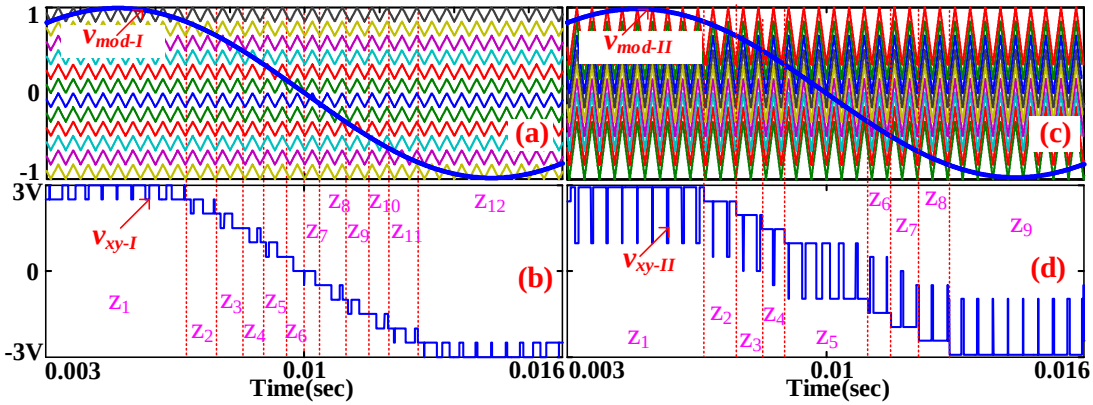


Figure 5.4: (a-b) Modulation signal (v_{mod-I}) and twelve regions in output voltage (v_{xy-I}) for the PWM strategy - I, (c-d) Modulation signal (v_{mod-II}), and nine regions in output voltage (v_{xy-II}) for the PWM strategy - II.

to generate a 13-level output voltage. Each carrier waveform defines a unique time zone, wherein each zone is defined as the period between the crossings of the modulating signal (v_{mod-I}) with the upper and the lower peak values of the corresponding carrier waveform as shown in Fig. 5.4(a). To minimize the leakage current, the proposed PWM strategy - I selects the switching states in such a manner that the magnitude of the TCMV (v_{Pg-I}) remains unaltered while switching any two consecutive voltage levels (Table 5.2).

This effectively eliminates the high-frequency transitions in the TCMV in each time zone. Further, it can also be observed that the output voltage waveform is identical to the one obtained with a conventional MLI, with low *dv/dt*. The operating principle of PWM strategy-I is verified with the help of numerical simulation of the mathematical model defined by

Table 5.2: Selection of Switching Patterns for PWM Strategy-I and II

PWM Strategy-I				**PWM Strategy-II**			
Zone	**Switching Patters**		v_{Pg-I}	**Zone**	**Switching Patters**		v_{CMV-II}
1	Sq_{+3}	$Sq_{+2.5}$	$+V_{PV}$	**1**	Sq_{+3}	Sq_{+1}	$1.5V_{PV}$
2	$Sq_{+2.5}$	Sq_{+2A}	$+V_{PV}$	**2**	$Sq_{+2.5}$	$Sq_{+0.5}$	$1.25V_{PV}$
3	Sq_{+2A}	$Sq_{+1.5A}$	$+V_{PV}$	**3**	Sq_{+2A}	Sq_{0}	V_{PV}
4	$Sq_{+1.5B}$	Sq_{+1}	0	**4**	$Sq_{+1.5A}$	$Sq_{-0.5A}$	$0.75V_{PV}$
5	Sq_{+1}	$Sq_{+0.5}$	0	**5**	Sq_{+1}	Sq_{-1}	$1.5V_{PV}$
6	$Sq_{+0.5}$	Sq_{0}	0	**6**	$Sq_{+0.5}$	$Sq_{-1.5}$	$1.25V_{PV}$
7	Sq_{0}	$Sq_{-0.5A}$	0	**7**	Sq_{0}	Sq_{-2A}	V_{PV}
8	$Sq_{-0.5B}$	Sq_{-1}	$-V_{PV}$	**8**	$Sq_{-0.5A}$	$Sq_{-2.5A}$	$0.75V_{PV}$
9	Sq_{-1}	$Sq_{-1.5}$	$-V_{PV}$	**9**	Sq_{-1}	Sq_{-3}	$1.5V_{PV}$
10	$Sq_{-1.5}$	Sq_{-2A}	$-V_{PV}$				
11	Sq_{-2A}	$Sq_{-2.5A}$	$-V_{PV}$				
12	$Sq_{-2.5B}$	Sq_{-3}	$-2V_{PV}$				

equations 1-9 (section 5.3) for a PV source voltage (v_{PV}) of 130V and a carrier frequency of 5 kHz. The pole voltages ($v_{xo\text{-}I}$, $v_{yo\text{-}I}$), the output voltage ($v_{xy\text{-}I}$), the common-mode ($v_{CMV\text{-}I}$), and the total common-mode voltage ($v_{Pg\text{-}I}$) obtained with PWM strategy – I, are presented in Fig. 5.5 (a-e). The output voltage ($v_{xy\text{-}I}$) waveform displays 13 distinct levels, while the total common-mode voltage results only in six transitions in a given fundamental cycle irrespective of switching frequency. Further, the magnitude of each of these transitions is limited to V_{PV}, which is 1/3rd of the total DC-link voltage (i.e. $3V_{PV}$). This further reduces the peak value of the leakage current corresponding to each of these transitions.

5.4.2 Implementation of PWM Strategy - II

PWM strategy - II is intended to eliminate the high-frequency transitions from both the common-mode voltage and the PV parasitic voltage ($v_{Pg\text{-}II}$). This PWM strategy is an improvement to the one presented in [144]. As mentioned earlier, this PWM strategy is employed when the proposed power converter employs a symmetrical filter (Figure 5.3(d)). From the expression of the TCMV ($v_{Pg\text{-}II}$) with the symmetrical filter (Eqn. 5.9), it is observed that the switching states of the voltage levels, which are apart by a voltage difference of $2V_{PV}$

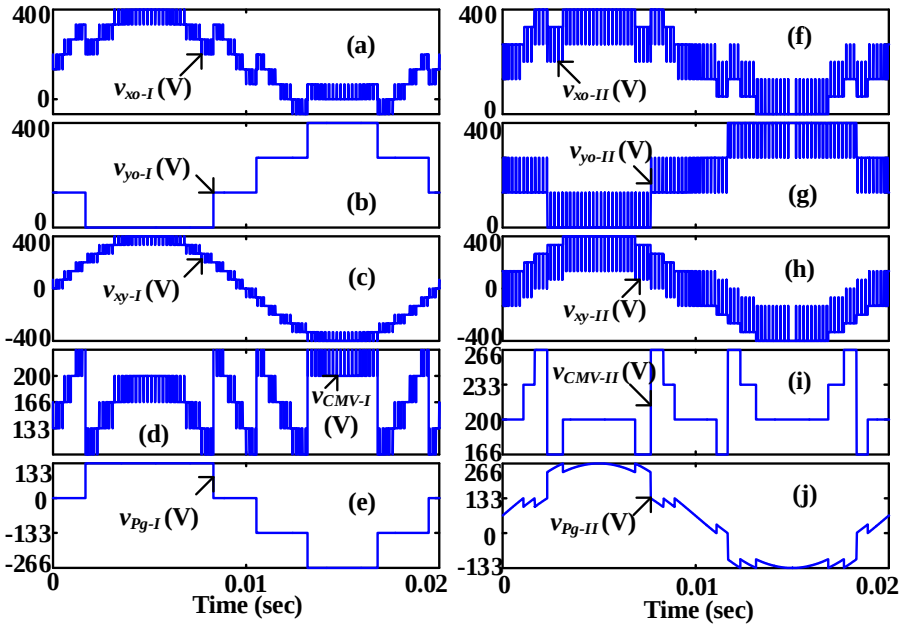


Figure 5.5: The plot of pole voltages, output voltage, common-mode voltage, and total common-mode voltage for (a-e) PWM strategy - I, (f-j) PWM strategy - II.

result in the same magnitude of CMV. Exploiting this fact to its advantage, the PWM strategy - II is designed in such a way that the voltage difference between two adjacent voltage levels is $2V_{PV}$. In general, an inverter producing *(2n+1)* voltage levels needs *(2n-3)* carrier waves to implement this strategy. Hence in the present case (where n = 6), the PWM strategy needs 9 *interleaved* carrier waves, which are compared with the modulating wave ($v_{mod\text{-}II}$) to obtain a 13-level output voltage waveform. Consequently, this PWM strategy displays nine time zones, in which all the 13 distinct voltage levels are accommodated as listed in Table 5.2. With an appropriate selection of switching states in each time zone, it is possible to eliminate the high-frequency transitions from the CMV as well as the total common-mode voltage.

As in the previous case, numerical simulations are used to assess the performance of the PWM strategy - II. These simulations are also carried out for a PV source voltage (v_{PV}) of 130V and a carrier frequency of 5 kHz. The pole voltages ($v_{xo\text{-}II}$, $v_{yo\text{-}II}$), the output voltage ($v_{xy\text{-}II}$), the common-mode ($v_{CMV\text{-}II}$), and the total common-mode voltage ($v_{Pg\text{-}II}$) corresponding to PWM strategy - II are presented in Figure 5.5 (f-i). From these simulation studies, it is evident that PWM strategy - II is capable of switching 13 voltage levels even though the voltage difference between two consecutive voltage levels is $2V_{PV}$. Furthermore, PWM strategy - II results in only four significant transitions with a magnitude of $0.75V_{PV}$ in a given power cycle irrespective of the switching frequency. This further reduces the peak and the RMS values of the leakage current.

5.5 Voltage Control and Power Distribution Analysis

5.5.1 Implementation of Voltage Controller Scheme:

The proposed power converter employs an interleaved buck-boost DC-DC conversion stage to charge the switched capacitors (SCs: C_1, and C_3). The voltages across these two capacitors are regulated through a couple of linear PI voltage controllers. These two voltage controllers individually regulate the SC voltages. Two carrier signals (v_{carr1} and v_{carr2}, Figure 5.6), which are phase-shifted by 180^0, are employed to compare the outputs of the voltage controllers to generate the required gating signals for each of the two devices of the interleaved buck-boost stage. The reference voltage for each of these two SCs is determined by the PV source voltage. Though the individual voltage across each SCs is equal to V_{PV},

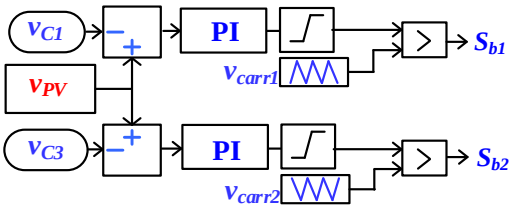


Figure 5.6: The control scheme for the interleaved buck-boost converter.

owing to the structure of the proposed power converter (Figure 5.1), the total DC-link voltage is equal to $3V_{PV}$. The energy stored in each of the inductors (L_1 or L_2) is transferred to the corresponding SC in each switching cycle (Figure 5.1).

From the foregoing discussion, it is evident that the proposed configuration is capable of transferring the PV source power to the load in both single-stage and double-stage modes. The individual periods of single and double stage modes determine the *peak power utilization* of the interleaved buck-boost converter.

5.5.2 Power Distribution Analysis:

The switching variables, defined earlier in section 5.3, are used to derive the period of each mode of operation.

$$A_s = Sv_{SP1}Sv_{SP4} + Sv_{SP2}Sv_{SP3} \tag{5.10}$$

$$A_{C1} = Sv_{SU1}A_S\,,\ A_{C3} = Sv_{SL2}A_S \tag{5.11}$$

In equations (10) and (11), the symbol A_S represents the period of the single-stage mode. The duration corresponding to the double-stage operation is divided into two sub-periods A_{C1}, and A_{C2} corresponding to the SCs C_1 and C_2 respectively. The energy transferred to the load in the single-stage operation is given as follows,

$$E_S = 2\int_0^{\pi} A_S v_{PV} i_L d(\omega t) \tag{5.12}$$

where $v_{PV,}$ and i_L respectively represent the PV source voltage and the load current.

The energy processed in the double-stage operation is derived as the sum of the powers processed through the SCs (C_1 and C_3):

$$E_{BB}=E_{C1}+E_{C3}=2\left[\int_0^{\pi} A_{C1}v_{C1}i_L d(\omega t)+\int_0^{\pi} A_{C3}v_{C3}i_L d(\omega t)\right] \quad (5.13)$$

where v_{C1} and v_{C3} are the voltages across the SCs C_1 and C_3. The voltage of each of these capacitors are regulated at v_{PV} due to the voltage mode control for each of the interleaving part. Now, to quantify the amount of energy processed through the boosting stage, an energy fraction index (E_{Sf}) is defined as:

$$E_{Sf}=\frac{E_S}{E_S+E_{BB}}=\frac{v_{pv}i_L\times 1.56\times 10^{-3}}{(1.56+2.14)\times v_{pv}i_L\times 10^{-3}}\times 100=42.1\% \quad (5.14)$$

Eqn. (5.14) reveals that, in any given power cycle, the proposed hybrid-inverter structure is capable of processing 42% of the total energy through the single-stage mode, while the rest of the 58% of the energy is processed through the double-stage mode. This reduces the overall power loss in the boosting stage, as the conventional voltage boosting schemes are constrained to process the entire (i.e. 100%) load energy through the double-stage operation only [73]. The design of the SCs is carried out as per the procedure outlined in [172], which aims to limit the voltage ripple.

5.6 Simulation Results

The operation of the proposed inverter configuration along with the proposed PWM strategies is validated through simulation studies in the MATLAB-SIMULINK environment. The parameters (*i.e.* input voltage (V_{PV}), modulation frequency (f_m), inverting stage switching frequency (f_{swi}), voltage boosting stage switching frequency (f_{swb})) used to simulate the proposed power converter are summarized in Table 5.3. In reality, the leakage current in a PV system depends on the distributed resistance and the distributed capacitance, which are present between the PV source and the ground (*i.e.* neutral terminal of the load). However, in the simulation studies, these distributed parameters are replaced by their lumped equivalent values (R_p, C_p, Figure 5.1). The behavior of the proposed power converter with an asymmetric filter structure (Figure 5.3(a)) and the PWM strategy – I, is assessed with simulation studies

Table 5.3: Circuit Parameters for Simulation

Parameter	Values	Parameter	Values
V_{PV}	130 V	C_2 , C_3	1 mF
f_m	50 Hz	L_1 ,L_2	0.5 mH
f_{swi}	5kHz	L_f	2 mH
f_{swb}	10kHz	C_f	0.1 uF
C_1, C_4	470 uF	R_p,C_p	10 Ω,100nF

and the corresponding results are presented in Fig. 5.7(a) – 5.7(e). Also, the corresponding results with symmetric filter structure and PWM strategy - II are presented in Figure 5.7(f) – 5.7(j). Figures 5.7(a) and 5.7(f) respectively present the simulated output voltages with PWM strategies – I & II. Comparing these simulated results (Figure 5.7) with the analytical results, which are obtained with switching function analysis (Figure 5.5) reveals the concurrence of these two approaches in analyzing the power converter and the associated PWM strategies. The phase difference between the peak values of the output voltages and the load currents reveals that the proposed converter is capable of handling reactive power also. It is evident from Figure 5.7 (d) and Figure 5.7 (i) that, both of the PWM strategies are capable of eliminating high-frequency transitions from the TCMV, which induces the leakage current in PV panels. These simulation results suggest that both of the proposed PWM strategies succeed to restrict high-frequency transitions in the TCMV, paving the way to effective management

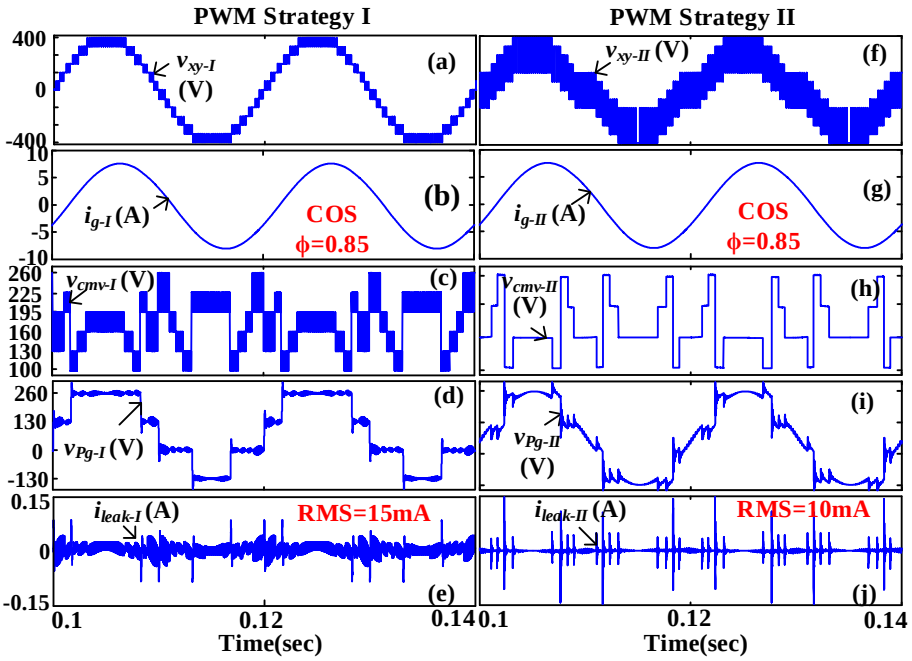


Figure 5.7: Simulation results with PWM strategy-I (a) v_{xy-I}, (b) i_{g-I}, (c) v_{CMV-I} , (d) v_{Pg-I}, (e) i_{leak-I} ; with PWM strategy-II (f) v_{xy-II}, (g) i_{g-II}, (h) v_{CMV-II} , (i) v_{Pg-II}, (j) $i_{leak-II}$.

of the leakage current. It may be noted that the respective RMS values of the leakage current are 15mA and 10mA with PWM strategy - I and PWM strategy - II. These values are well within the limit of 30mA, stipulated by the VDE0126-1-1 standard [156].

In addition, the performance of the proposed modulation technique is compared with the leakage current elimination techniques, which are reported earlier. Figures 5.8 (a-c) present the output voltage, the TCMV, and the leakage current for the proposed configuration with the conventional LSPWM technique. Figure 5.8(c) reveals that the leakage current, in this case, violates both the peak and the RMS limits specified by the VDE0126-1-1 standard[3]. The CMV elimination [173, 174] technique shows a better performance in the elimination of the leakage current (Figures 8 (d-f)). However, for the same switching resources, the conventional CMV elimination calls for a compromise in the number of voltage levels (to 4) to eliminate the CMV. The dc- and the ac-decoupling techniques are widely used

Table 5.4: Comparison of Existing Leakage current minimization techniques.

Schemes for Proposed Inverter	**A**	**B**	**C**	**D**	**E**	**F**	**G**
Conv. LSPWM [147,165] [Figure 5.8(a-c)]	-	2%	one inductor	High-freq.	350mA	Yes	96.76%
Conv. CMV Elimination based approach [173,174] [Figure 5.8(d-f)]	-	4.8%	two inductors	Low-freq.	2mA	Yes	96.80%
DC-decoupling H5 based approach [60,173] [Figure 5.8(g-i)]	1	4.5%	two inductors	Low-freq.	20mA	No	95.40%
AC-decoupling HERIC based approach [61,175] [Figure 5.8(j-l)]	2	4.5%	two inductors	Low-freq.	25mA	No	95.90%
Proposed Method-I [Figure 5.7(a-e)]	-	1.5%	one inductor	High-freq.	15mA	Yes	95.76%
Proposed Method-II [Figure 5.7(f-j)]	-	1.8%	two inductors	Low-freq.	10mA	Yes	95.02%

A: Number of additional switching devices.
B: THD of the load current.
C: Type of required filter at the output.
D: Nature of total common-mode voltage.
E: RMS value of the leakage current.
F: Reactive power sourcing capability.
G: Calculated efficiency.

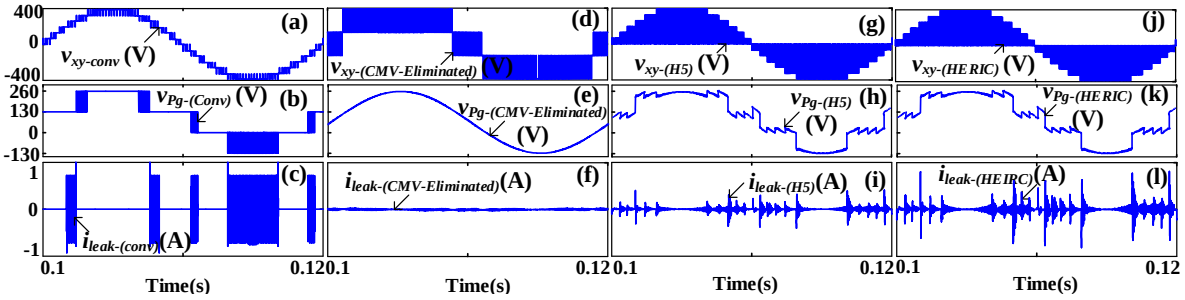


Figure 5.8: Proposed configuration with (a-c) conventional LSPWM, (d-f) CMV elimination, (g-i) H5 based dc-decoupling, (j-l) HERIC based ac-decoupling.

for multilevel inverter applications [61-62, 175], which demand additional semiconductor devices as well as refined modulation strategies to minimize the transitions in the TCMV as shown in Figure 5.8 (g-l). However, the modulation strategies associated with decoupling impose a high *dv/dt* across the switches and increase the size, cost, and power loss in filters. Further, the thermal efficiency of the proposed power converter was assessed with the PLECS software for all of the above-mentioned strategies, while maintaining identical input and output parameters. Table 5.4 summarizes the effectiveness of these strategies to limit the leakage current.

5.7 Experimental Results

A scaled-down hardware prototype (Figure 5.9) has been developed for the proposed power converter to validate its operating principle along with the PWM strategies – I and II. The operating parameters for the experimental prototype are summarized in Table 5.5. The power semiconductor switching devices employed to fabricate the laboratory prototype are IRF 460 (MOSFET) and MUR1560 (diode). The SPARTAN-6 FPGA control platform is used to implement the proposed modulation strategies. Galvanic isolation between the power circuit and the control platform is provided with an optocoupler-based (HCPL-3120) driver

Table 5.5: Circuit Components & Operating Parameters used in the Prototype.

Parameter	Values	Parameter	Values
V_{PV}	60 V	C_1, C_4	24×6.8 uF =160uF
$V_{DC\text{-}link}$	180 V	C_2 , C_3	1 mF
VA_{rated}	500VA	L_1 ,L_2	0.5 mH
f_m	50 Hz	L_f	2 mH
f_{swi}	5kHz	C_f	0.1 uF
f_{swb}	10kHz	R_p,C_p	10 Ω,100nF

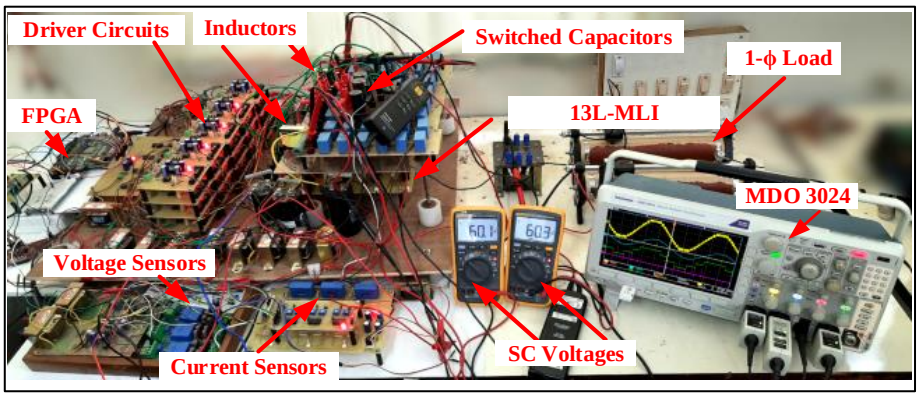


Figure 5.9: Laboratory prototype for the proposed inverter configuration.

circuit. The input PV source is emulated with a programmable dc-source. The path for the leakage current is emulated with a branch consisting of the equivalent lumped circuit parameters R_p and C_p (Figure 5.1, Table 5.5).

Figures 5.10 (a-c) demonstrate the operation of the proposed configuration with the conventional LSPWM technique, where it is observed that the configuration is capable of synthesizing thirteen distinct voltage levels (Figure 5.10 (a)). These voltage levels correspond to $\pm 3V_{PV}$, $\pm 2.5V_{PV}$, $\pm 2V_{PV}$, $\pm 1.5V_{PV}$, $\pm V_{PV}$, $\pm 0.5V_{PV}$, and 0. It may be noted that the amplitude of the output voltage corresponds to 180 V. Thus, it is evident that a voltage boosting factor of three is achieved, as the input PV voltage is equal to 60 V (Table 5.5). It may further be observed that the unconstrained selection of switching states results in a large number of high-frequency voltage transitions in both the common-mode (v_{CMV}), and the total common-mode voltage (v_{Pg}). In addition, the number of voltage transitions increases linearly with the increase of the switching frequency of the inverter, suggesting that the number of high-frequency switching transitions is not independent of the switching frequency of the inverter (Figure 5.10(c)). Thus, the conventional LSPWM may not be suitable for PV inverter applications as it violates the limits of the VDE0126-1-1 standard. Experiments are performed to validate the operation of the proposed configuration using PWM strategies - I and II. The differential characteristics (output-voltage, load-current) and the common mode characteristics (CMV, TCMV, leakage current) of the proposed configuration with PWM strategy - I and II are presented in Figure 5.10 (d-f) and Figure 5.10 (g-i) respectively. It may be observed that the experimental results are in agreement with the results obtained with the numerical simulation. It is evident that both of the PWM strategies are capable of switching all of the thirteen voltage

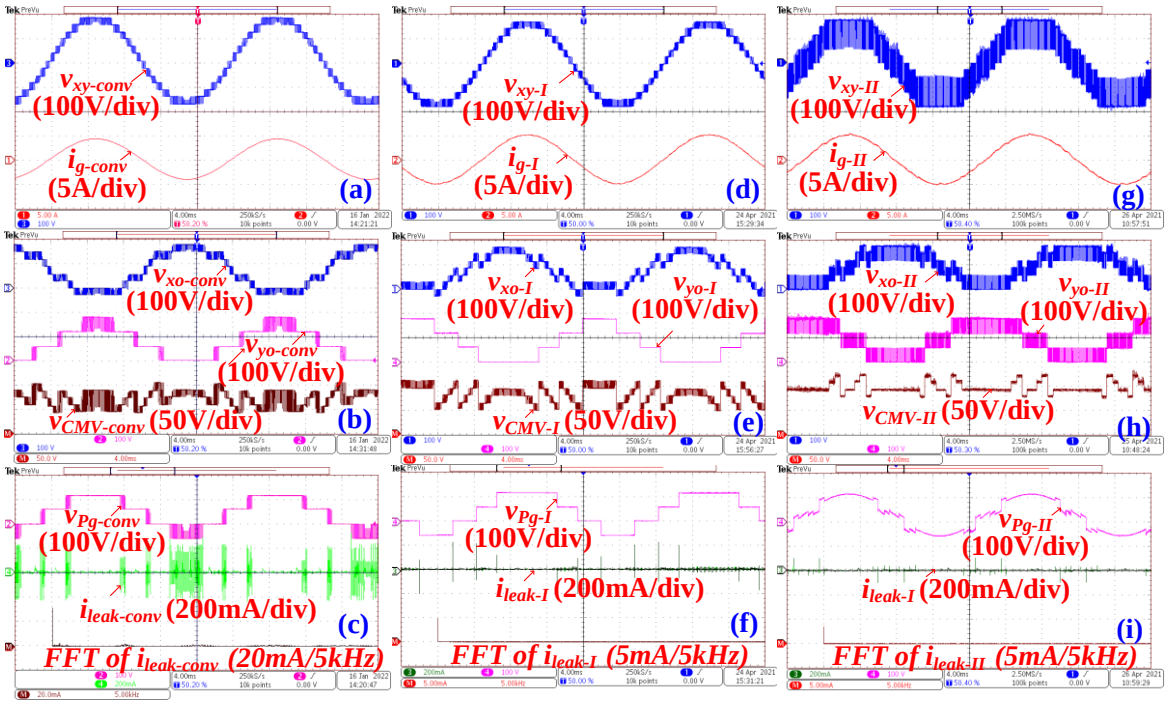


Figure 5.10: Experimental results for conventional PWM strategy: : (a)output voltage ($v_{xy\text{-}conv}$), load current($i_{g\text{-}conv}$), (b) pole voltages ($v_{xo\text{-}conv}$, $v_{yo\text{-}conv}$), common mode voltage ($v_{CMV\text{-}conv}$) (c) TCMV and leakge current($i_{leak\text{-}conv}$) , PWM strategy - I: (a)output voltage ($v_{xy\text{-}I}$), load current($i_{g\text{-}I}$), (b) pole voltages ($v_{xo\text{-}I}$, $v_{yo\text{-}I}$), common mode voltage ($v_{CMV\text{-}I}$) (c) TCMV and leakge current($i_{leak\text{-}I}$) , for PWM strategy - II: (a)output voltage ($v_{xy\text{-}II}$), load current($i_{g\text{-}II}$), (b) pole voltages ($v_{xo\text{-}II}$, $v_{yo\text{-}II}$), common mode voltage ($v_{CMV\text{-}II}$) (c) TCMV and leakge current($i_{leak\text{-}II}$).

levels mentioned: ±180V, ±150V, ±120V, ±90V, ±60V, ±30V, and 0. Further, PWM strategy - I retains all of the good features of a conventional MLI such as reduced *dv/dt* stress and improved harmonic performance. It is evident from Figure 5.10 (f) that, in each fundamental cycle, the resultant total common-mode voltage (TCMV) displays only six transitions in its magnitude, *irrespective of the switching frequency of the inverter*. The magnitude of each voltage transition is only 60 V, which is 1/3rd of the total DC-link voltage, which reduces the amplitude of the leakage current.

In contrast, with the PWM strategy - II, the voltage difference between two consecutive voltage levels is $2V_{PV}$ (i.e. 120V). This PWM strategy is capable of eliminating *all* high-frequency transitions from both CMV and the TCMV. PWM strategy - II results in four significant transitions of a magnitude of 45V ($0.75V_{PV}$) in $v_{Pg\text{-}II}$ (Figure 5.10 (i)) in a fundamental cycle *irrespective of the switching frequency of the inverter.* This advantage outweighs the slight disadvantage associated with a marginal increase in the value of THD of the load current w. r. t the conventional output (Figure 5.10 (a) and 5.10 (d)). With identical

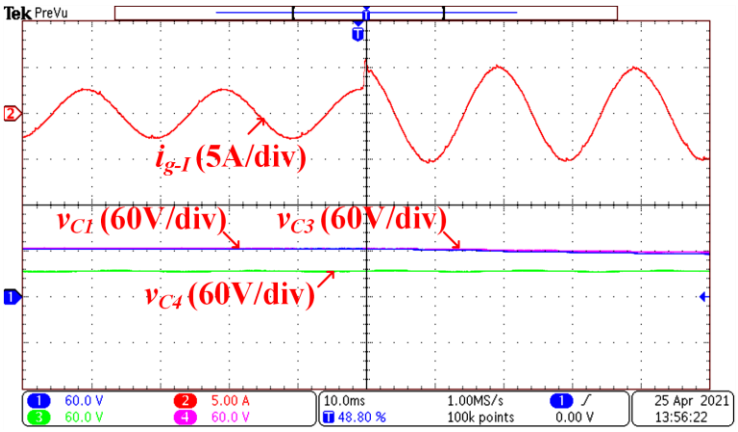


Figure 5.11: Experimental validation for dynamic current reference variation from 2.5A to 5A.

switching frequencies (5 kHz), input voltages (60V), and other circuit parameters, PWM strategies - I and II respectively result in leakage currents having RMS values of 8.20mA and 5.70mA. It may be noted that in both of these cases, the RMS values of the leakage current are much lower than the limit stipulated by the VDE-0126-1-1 standard.

The dynamic response of the voltage across the SCs is presented in Figure 5.11, wherein the peak current reference is varied from 2.5A to 5A. This operation results in the shifting of the operating point on the PV characteristics as the output power is increased, which manifests as a small decrease (~1.5V) in the PV voltage. The decreased PV voltage would redefine the reference voltages for the SCs (Figure 5.6) and accordingly the closed-loop controller re-adjusts the voltages on the SCs (C_1 and C_3). This readjustment is affected within 20ms without causing any distortion in the output and eventually, the voltage across the capacitor C_4 settles down at half of the input PV voltage.

Further, separate experiments have been performed, with a lagging load impedance (PF=0.8), to establish the reactive capability of the proposed configuration with the proposed PWM strategies. The experimental results presented in Figure 5.12 (a-b) reveal a significant phase shift between the output voltage and current, proving this point. Experimental results presented in Figure 5.11 (UPF) and Figure 5.12 (PF = 0.8 lag) reveal that neither the total common-mode voltage nor the leakage current is affected by the type of the load (UPF or lagging PF). Thus, the proposed configuration, along with the proposed PWM strategies, is capable of delivering active as well as reactive power to the load without compromising either the differential mode or the common-mode performances.

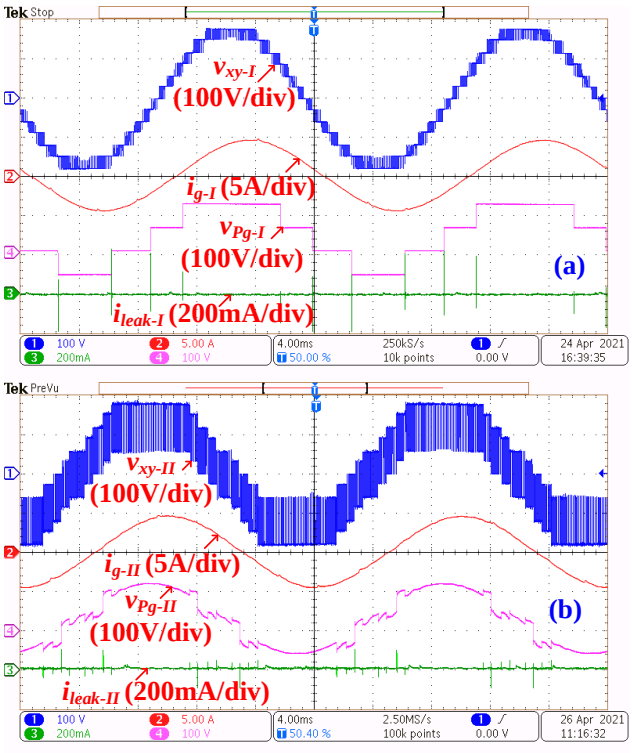


Figure 5.12: Experimental results for PWM strategy - I (a) v_{xy-I}, i_{g-I}, v_{Pg-I}, i_{leak-I} and for for PWM strategy - II (a) v_{xy-II}, i_{g-II}, v_{Pg-II}, $i_{leak-II}$ with lagging load (PF=0.8).

Furthermore, the performance of the laboratory prototype is evaluated at the power output of 500W for both of the PWM strategies. The experimental results obtained with PWM strategies I and II are presented in Figure 5.13 and Figure 5.14 respectively. To measure the power and THD of the load current, a single-phase power-analyzer (UNI-T UT283A) is also connected across the output terminals of the experimental prototype. Besides that, a precision digital power meter (Yokogawa WT332E) is also employed to determine the efficiency of the inverter. To obtain both the input and the output powers simultaneously, one of the isolated channels of the power meter is connected across the input terminals of the prototype, while the other is connected at the output terminals. From these measured values, the efficiency of the proposed configuration with PWM strategy - I is obtained as 94.60% at an output voltage of $110V_{rms}$ and the output power (P_{out}) of 500 W. The THD of the load current with the PWM strategy – I, is obtained as 1.29% as shown in Figure 5.13 (c). Similar experimentation is performed with PWM strategy - II and these experimental results are presented in Figure 5.14 (a). From the measured values of the input and the output powers, the efficiency of the proposed power converter is obtained as 93.80% with PWM strategy - II at the same operating

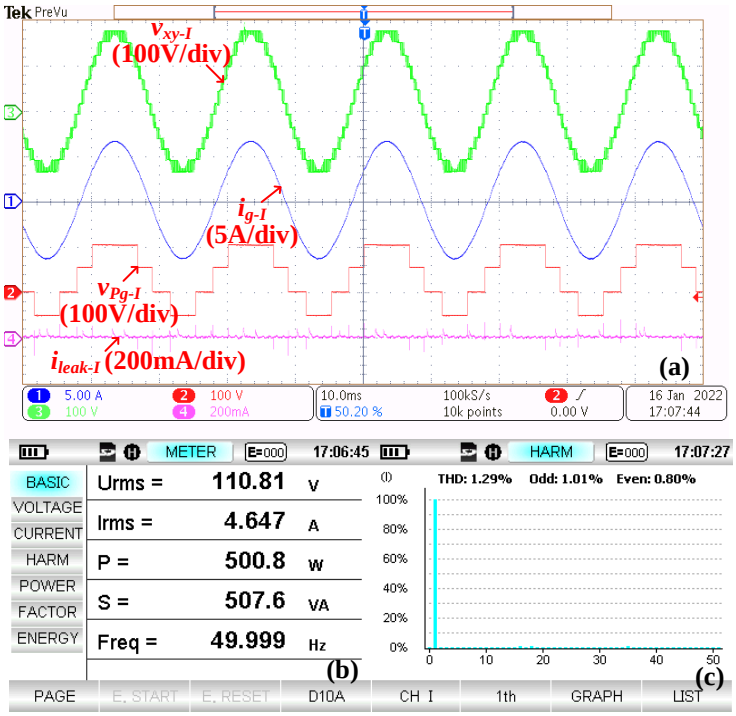


Figure 5.13: Experimental results of the proposed inverter configuration with PWM strategy - I: (a) output voltage (v_{xy-I}), grid current (i_{g-I}), total common-mode voltage (v_{Pg-I}), leakage current (i_{leak-I}), (b) RMS of the inverter voltage, Active power (P), apparent power (S), (d) THD and harmonic spectrum of the load current at P_{out} =500W.

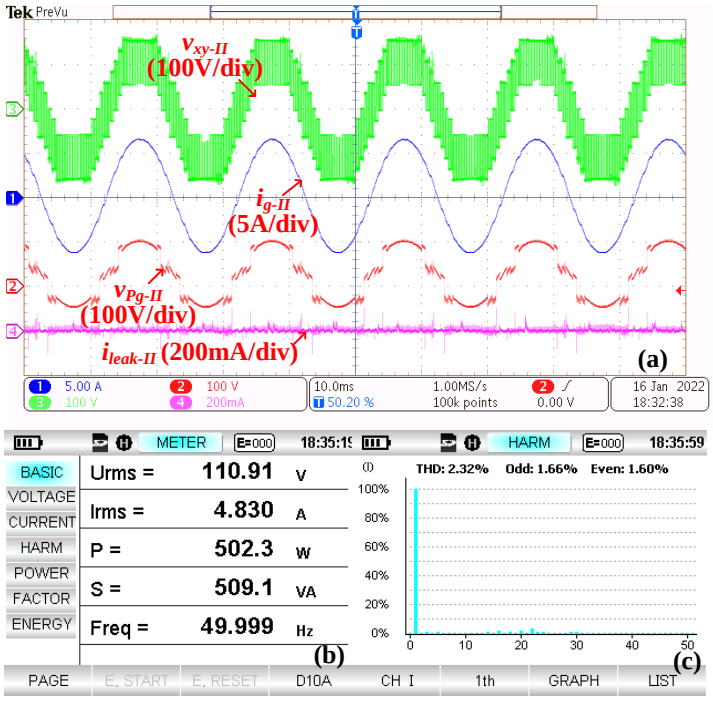


Figure 5.14: Experimental results of the proposed inverter configuration with PWM strategy - II: (a) output voltage (v_{xy-II}), grid current (i_{g-II}), total common-mode voltage (v_{Pg-II}), leakage current ($i_{leak-II}$), (b) RMS of the inverter voltage, Active power (P), apparent power (S), (d) THD and harmonic spectrum of the load current at P_{out} =500W.

conditions (110 V_{rms}, 500W). The THD of the load current with PWM strategy - II is obtained as 2.32% as shown in Figure 5.14 (c).

Further, the performance of the inverter configuration is validated in the grid-tie conditions with both of the PWM strategies. The overall control scheme for grid-tie operation is as per the procedure mentioned in chapter 3 section 3.4.3. The values for proportional gain (k_{pc}) and resonant gain (k_{rc}) for the current control loop are determined using the SISO Toolbox of MATLAB. The value of k_{pc} and k_{rc} are obtained as 0.0483 and 2.212 respectively for the proposed power converter. The stability and fast dynamic response of the system are ensured by keeping the gain margin and phase margin of the overall system at 11.4 dB and 61.9° respectively as shown in Figure 5.15. The effectiveness of the current controller is demonstrated for both PWM strategy - I and PWM strategy - II and the corresponding experimental results are shown in Figure 5.16 (a) and (b) respectively. For both of these case studies, a peak current reference of 4A is considered to inject power at the UPF condition.

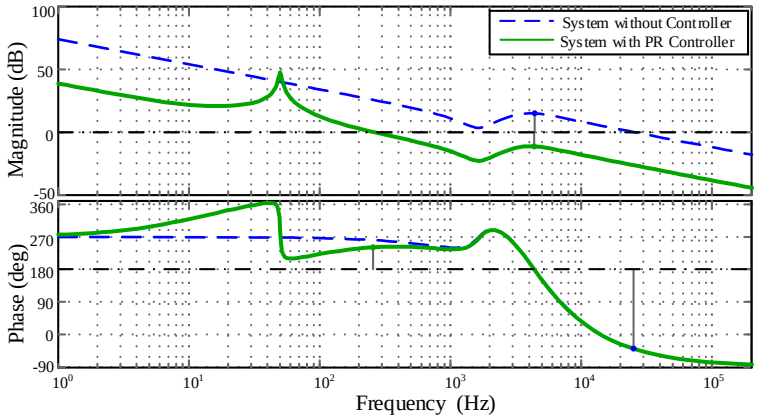


Figure 5.15: Bode plot for PR controller and the proposed thirteen level boost inverter.

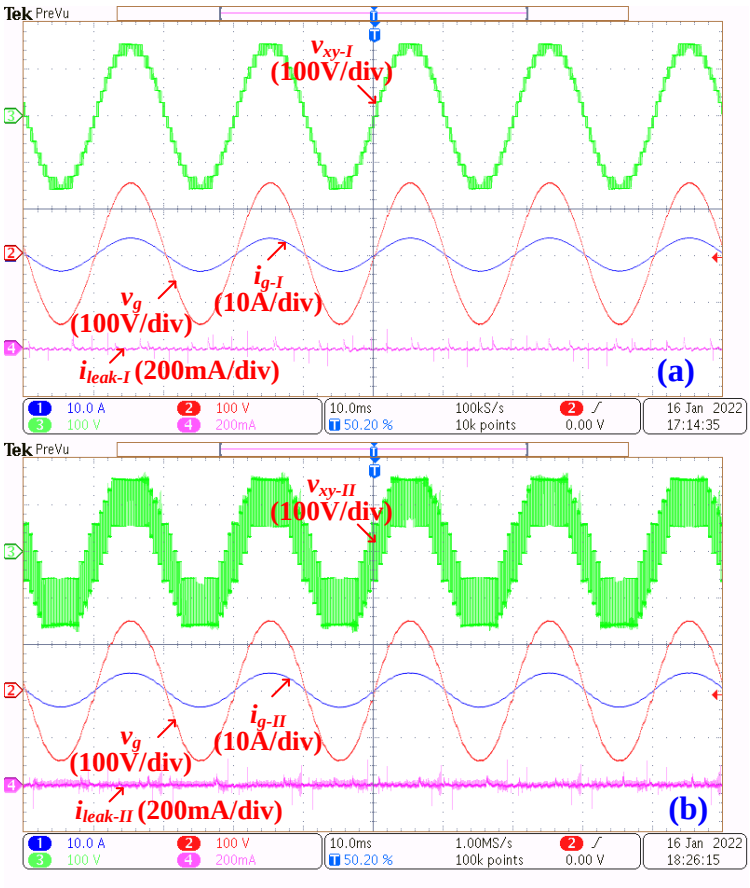


Figure 5.16: Experimental results: inverter output voltage, grid-voltage, grid-current, and leakage current for (a) PWM strategy - I and (b) PWM strategy - II.

5.8 Comparison with Existing Transformerless Inverter Topologies

Table 5.6 demonstrates the effectiveness of the proposed power circuit configuration vis-à-vis similar transformerless inverter topologies reported in the earlier literature. As the literature available on 13L transformerless inverter configuration is scanty, similar transformerless power converters, which output 5-level and 9-level voltage waveforms, are also considered for comparison. The comparison is based on the *per-unit* basis to justify topologies with an unequal number of voltage levels. The cost function (CF, Table 5.6) for each of the considered configurations is determined [98]. In this context, it should be noted that the power converter introduced in [99] shows improved performance when compared with systems with a conventional voltage boosting scheme. However, the number of output voltage levels for this inverter configuration [99] is limited to five. Furthermore, the modulation technique described in [99] causes a high (*dv/dt*) stress across the inverter

Table 5.6: Comparison of Existing Topologies.

	[99] -5L	**[144] -9L**	**[147] -9L**	**[165] -9L**	**[97] -13L**	**[98] -13L**	**Proposed -13L**	
A	9+1	10+0	19+3	8+3	16+0	15+0	12+2	
B	1	0	3	3	4	3	3	
C	1	0	0	0	0	0	2	
D	1	4	1	1	2	1	1	
E	2	1	4	4	3	6	3	
F	7.5	5	4.75	5.75	5.6	5	8	
G	Soft	-	Hard	Hard	Hard	Hard	Soft	
H	2-3I_m	-	5-6I_m	5-6I_m	5-6I_m	5-6I_m	2-3I_m	
I	f_o	f_o	f_{sw}	f_{sw}	f_{sw}	f_{sw}	f_o	
J (mA)	110	100	73	820	820	820	10	
K	Yes	Yes	Yes	Yes	Yes	Yes	Yes	
L	27.1	19.7	14.8	13.7	10.6	11.1	10.7	27.6
M	2.9	2.2	1.6	1.5	1.41	1.47	1.44	1.83
CF	5.90	3.22	5.53	3.19	3.35	3.00	3.00	

A: (Number of switches + Number of diodes);
B: Number of capacitors;
C: Number of inductors;
D: Number of required DC sources,
E: Voltage gain factor (total DC-link/input voltage),
F: Total standing voltage in per unit (TSV_{pu}). (with respect to the max. the peak value of the output voltage);
G: hard-charging or soft-charging of the SCs;
H: Peak current stress of the semiconductor devices in voltage boosting path,
I: Nature of TCMV waveform,
J (in mA): RMS of leakage current,
K: Capability of reactive power exchange,
L: THD (in %) of the output voltage. (* For the proposed topology two values indicate PWM strategy - I and II respectively.)
M: THD (in %) of the load current. (* For the proposed topology two values indicate PWM strategy - I and II respectively.)
CF: Cost function. CF= (Number of switches + Number of drivers for switches + Number of diodes + Number of capacitors + Number of inductors + Number of sources + TSV_{pu}) / Number of voltage levels.
where f_o is modulation frequency, f_{sw} is switching frequency, I_m peak value of the grid-current.

switches. The inverter configuration proposed in [144] requires a reduced number of switches (based on the per-unit consideration) to synthesize a nine-level output voltage while reducing the leakage current. However, it requires four isolated PV sources. This increases the complexity to implement the MPPT algorithm, as it is to be implemented separately for each PV source. The requirement of multiple PV sources is avoided with the conventional SC-based configurations proposed in [147] and [165], which obtain multi-level inversion along with the voltage boosting capability. Though these topologies achieve self-balancing of the SC voltages, the hard-charging of the SCs causes increased current stress in the switching

devices. The extension of this technique paved the way for the enhancement of the number of voltage levels and the voltage boosting capability. The power converters proposed in [97] and [98] are capable of synthesizing a 13-level voltage waveform with a voltage-boosting factor of 6. These topologies are having a similar per-unit cost function value as the proposed configuration. However, these configurations suffer from high-leakage current, which restricts their applicability to transformerless PV systems. Compared to the aforementioned systems, the proposed power converter limits the peak values of currents in those switches, which are responsible for the charging of the switched capacitors. This is simply achieved by the placement of the boosting inductors in their charging paths. The proposed configuration also achieves a voltage boost factor of three. In addition, both of the proposed PWM strategies – I and II manage to restrict the leakage current to be well within the limit specified by the VDE-0126-1-1 standard.

Further, the proposed configuration (along with the two proposed PWM strategies) is simulated in the PLECS environment to assess its performance. These simulations are performed for a total DC-link voltage of 400V and an active power output of 1kW at 230V (RMS). The equivalent thermal models of *IKW30N60T* (IGBTs along with their internal

Table 5.7: Loss Distribution of Semiconductor Devices For PWM Strategies - I and II[#]

Power Loss Analysis								
PWM Strategy - I								
Inverting Stage	S_{U1}	S_{U2}	S_{L1}	S_{L2}	S_{P1}	S_{P2}	S_{P3}	S_{P4}
	1.75	1.72	1.14	2.31	1.61	1.57	1.52	1.73
Boosting Stage	S_{b1}	S_{b2}	D_1	D_2	**Total Semiconductor Power Loss**			
	5.92	5.90	2.15	2.35	**33.45W**			
PWM Strategy - II								
Inverting Stage	S_{U1}	S_{U2}	S_{L1}	S_{L2}	S_{P1}	S_{P2}	S_{P3}	S_{P4}
	3.01	0.67	1.23	2.24	1.58	1.63	1.54	1.60
Boosting Stage	S_{b1}	S_{b2}	D_1	D_2	**Total Semiconductor Power Loss**			
	6.14	6.44	2.51	2.51	**34.35W**			

[#]All power loss values are given in watts.

diodes) are considered for these simulations. The PLECS software estimates both switching and conduction power losses incurred in each power semiconductor switching device. The computation of the power losses incurred in each device paves the way to the assessment of the power loss occurring in the inverting stage as well as the boosting stage, which are presented in Table 5.7. It is observed that the proposed configuration achieves an overall efficiency of about 96% with both of the proposed PWM strategies.

Figure 5.17 presents the simulated and the experimentally obtained efficiencies of the proposed thirteen-level inverter configuration with PWM scheme - I. The efficiency is measured at output power ranging from 100W to 500 W in steps of 100W. It may be noted that the experimentally obtained efficiencies are in close agreement with their simulated counterparts. Further, at the rated condition, the scaled-down laboratory prototype results in an efficiency of 95% (approx.), which is close to the efficiency obtained through the simulation study.

5.9 Conclusion

This chapter proposes a thirteen-level transformerless inverter configuration along with two PWM strategies. With the aid of an interleaved semi-double staged structure, the proposed power converter achieves a voltage boost factor of three with reduced power stress. This converter employs a control scheme, which is capable of regulating the voltage of the switched capacitors (SCs) while obtaining a smooth transition between single- and double-stage operations. Furthermore, this chapter presents a detailed step-by-step procedure to deri-

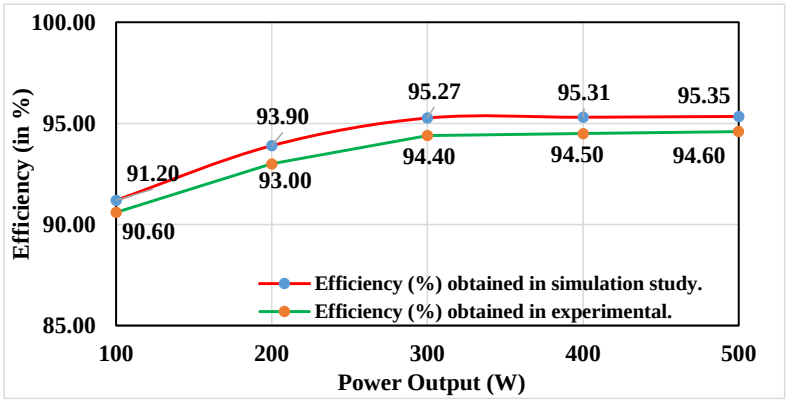


Figure 5.17: Comparative efficiency plot of the proposed configuration ranging from 100W to 500W obtained in the simulation study and measured in the experiment.

-ve the parasitic PV voltage for a generic multilevel inverter with symmetrical or asymmetrical filter structures. This analysis establishes a relationship between the common-mode voltage and the total common-mode voltage for each switching state. It also paves the way for the design of two PWM strategies, namely *PWM strategy -I* and *PWM strategy - II*, which are respectively applicable to inverters with unsymmetrical and symmetrical filter structures. These two PWM strategies succeed to reduce high-frequency transitions in the CMV and the parasitic PV voltage when compared to the conventional LS-PWM strategy. Despite the presence of high-frequency components in the CMV, PWM strategy - I retains some of the good features of conventional MLIs such as low harmonic contamination and low *dv/dt* stress across the switches. In contrast, the PWM strategy - II eliminates high-frequency transitions from both the common-mode voltage and the parasitic PV voltage at the expense of higher *dv/dt*. Both of the proposed PWM strategies result in a low RMS value of the leakage current, which is well within the stipulated safety limit of the VDE-0126-1-1 standard. Thus, the proposed power converter, modulated with the PWM strategies (both I and II), achieves low values of leakage and common mode currents without any additional circuit components. Also, the requirements of the EMI filter or the common mode filter at the output of the inverter are low for this power converter configuration. Owing to these features, it is envisaged that the proposed configuration could be employed for both standalone and grid-connected PV applications.

Chapter 6

Three-Phase Semi-Single Stage Boost PV Inverter

Chapter 6

Three-Phase Semi-Single Stage Boost PV Inverter

6.1 Introduction

As discussed in Section 1.5, voltage boosting schemes are necessary for varying environmental conditions. Some interesting circuit topologies are proposed in [119,182], wherein the voltage boosting stage is merged with the inverter configuration. These configurations are capable of mitigating the leakage current, while the loss of the DC-link utilization is compensated by the voltage boosting unit. However, these topologies transfer the total PV power through the boosting stage, which results in a significant power loss in the voltage boosting unit. With the motivation of improving efficiency, a voltage-boosting network, which is similar to that of the one proposed in Chapter-3, Chapter-4, and Chapter-5 is employed for a three-phase system.

This chapter proposes a single source-based PV configuration, which is obtained by the fusion of a 3-phase 3-level inverter and a voltage boosting unit. Another advantage of the proposed system is that any existing three-phase, 3-level VSI is compatible with the proposed boosting stage. Thus, it serves as a retrofit solution for any existing 3-phase, 3-level inverter topologies such as the cascaded H-bridge, the NPC, and the ANPC-based inverter configurations [33]. The proposed power converter topology, along with its modulation technique, is capable of reducing the leakage current without sacrificing the multilevel voltage at the output. The mathematical analysis of the partial power transfer capability is also carried out with the help of the switching function.

6.2 Operation of the Proposed Three-Phase TBMLI

The circuit diagram of the proposed three-phase T-type transformerless boost inverter (3-ϕ TBMLI) for the PV applications is shown in Figure 6.1. The presented inverter configuration requires a single string of solar panels, two DC-link capacitors (C_2, C_3), and

two switched capacitors (SCs: C_1 and C_4). The proposed power circuit configuration consists of three sections: (i) the voltage boosting unit (VBU), (ii) the level selector unit (LSU), and (iii) the phase generation unit (PGU). The VBU is realized with a back-to-back connection of an inverting and a non-inverting buck-boost converter as shown in Figure 6.1. The LSU consists of two half-bridge legs, which are connected across the SCs. Thus, the T-legs of each output phase can be connected to the appropriate junction points (J_0, J_1…J_4) through the LSU (Figure 6.1). The output terminals of the 3-level VSI are connected to a star-connected load.

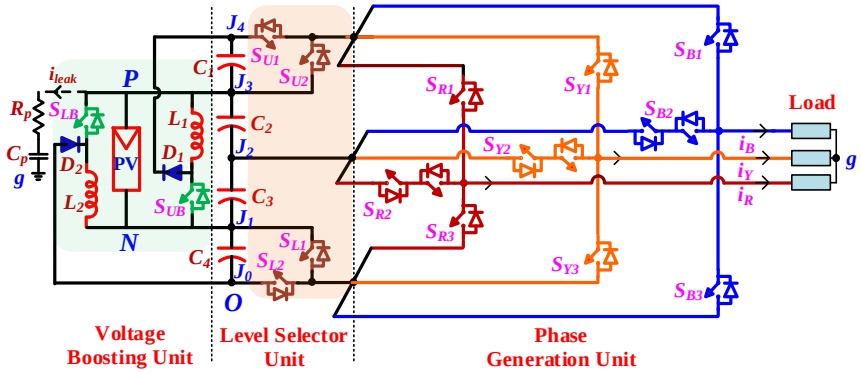


Figure 6.1: The proposed three-phase T-type multilevel boost inverter configuration.

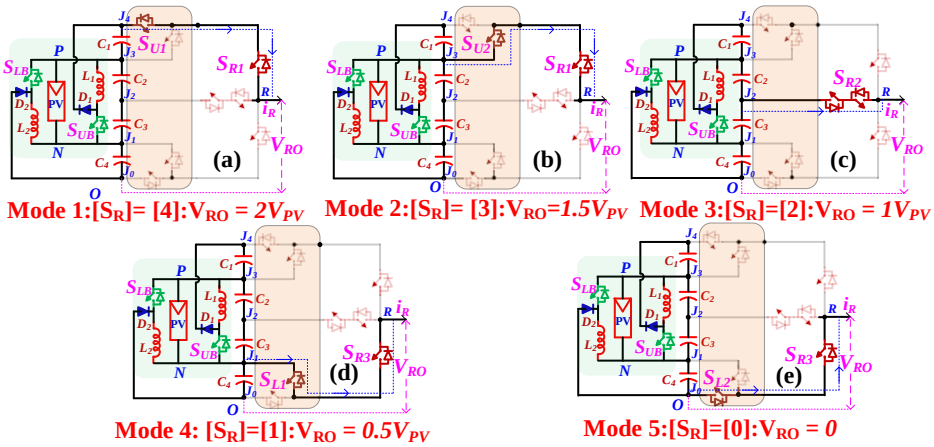


Figure 6.2: All modes of operation for R-phsae: (a) Mode 1 ,(b) Mode 2 ,(c) Mode 3 ,(d) Mode 4 ,(e) Mode 5 .

Table 6.1: Different Modes of Operation of Phase-R

Mode	S_R	V_{RO}	S_{U1}	S_{U12}	S_{L1}	S_{L2}	S_{R1}	S_{R2}	S_{R3}
1	4	$2V_{PV}$	1	0	X	X	1	0	0
2	3	$1.5V_{PV}$	0	1	X	X	1	0	0
3	2	$1V_{PV}$	X	X	X	X	0	1	0
4	1	$0.5V_{PV}$	X	X	1	0	0	0	1
5	0	0	X	X	0	1	0	0	1

The three-phase load currents are indicated as i_R, i_Y, and i_B for the corresponding three phases R, Y, and B. An equivalent branch for the parasitic elements of the PV panel is represented by a series connection of a resistor (R_p) and a capacitor (C_p) as shown in Figure 6.1. The parasitic voltage (v_{Pg}) and the leakage current (i_{leak}) can also be measured across this branch. The proposed inverter configuration is capable of switching 49 space vector locations with the available switching resources in LSU and PGU. The switching operations corresponding to the five modes of operation, which cause five distinct voltage levels of the R-phase are shown in Figure 6.2 (a-e). Table 6.1 further summarizes the voltage levels for the pole voltage 'v_{RO}' (*i.e.* voltage difference across 'R' phase output and the reference point 'O') and the corresponding states of the switching devices pertaining to that phase. In Table 6.1, the symbols 'S_R' and 'V_{PV}' respectively represent the space vector index corresponding to the 'R-phase' and the input voltage for the inverter. The symbol 'X' in Table 6.1 indicates that the given pole voltage does not depend on those particular switching states. This results in the redundancy of switching states, which further allows the utilization of the LSU for other phases. Similarly, the pole voltages for the other two phases can be defined with the help of the space vector indices 'S_Y' and 'S_B' corresponding to their pole voltages i.e. 'v_{YO}' and 'v_{BO}'.

6.3 Modulation Technique

An emphasis is laid on the integration of the voltage boosting unit and inverting unit in the proposed system. As the switching devices corresponding to the LSU (Figure 6.1) are kept common for all the three phases, the total number of switching devices for the inverter configuration is reduced. This is possible because, the adopted modulation technique explored and utilizes the benefits of redundant switching vectors, which would not result in any transition of voltage across the parasitic branch of the PV panel (consisting of R_P and C_P, Figure 6.1). To analyze the effects of each switching vector, the pole voltages (*i.e.* v_{RO}, v_{YO}, v_{BO}) of each phase are modeled with the corresponding space vector index (*i.e.* S_R, S_Y, S_B) as,

$$v_{RO} = S_R \times 0.5V_{PV} \tag{6.1}$$

$$v_{YO} = S_Y \times 0.5V_{PV} \tag{6.2}$$

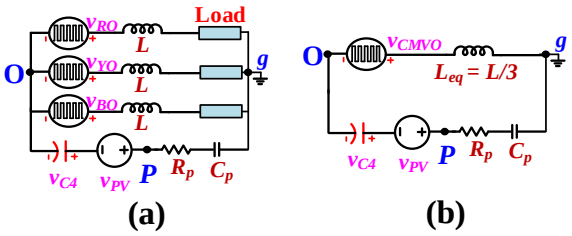


Figure 6.3: Equivalent circuit of the proposed configuration (a) with pole voltages of each phase, (b) equivalent value of common-mode voltage.

$$v_{BO} = S_B \times 0.5V_{PV} \tag{6.3}$$

In order to derive the mathematical relation of total common-mode voltage, which is the main cause of leakage current, the common-mode equivalent circuit is analyzed in Figure 6.3.

From Figure 6.3, it is clear that the total common-mode voltage (i.e. v_{Pg}), which appears across the parasitic elements can be given as follows,

$$i_{leak} = \frac{v_{Pg}}{Z_{CM}} \tag{6.4}$$

where Z_{CM} is the impedance in the parasitic path.

The simplified mathematical relation for total-common mode voltage is derived as follows,

$$v_{Pg} = v_{PV} + v_{C4} - v_{CMVO} \tag{6.5}$$

where common-mode voltage (i.e. v_{CMVO}) of the inverter w. r. t to the point 'O'. It can be derived as follows,

$$v_{CMVO} = (S_R + S_Y + S_B)\frac{V_{PV}}{6} \tag{6.6}$$

Thus, the mathematical relation for total-common mode voltage can be further simplified as,

$$v_{Pg} = V_{PV} + \frac{V_{PV}}{2} - (S_R + S_Y + S_B)\frac{V_{PV}}{6} \tag{6.7}$$

$$v_{Pg} = \left[9 - (S_R + S_Y + S_B)\right]\frac{V_{PV}}{6} \tag{6.8}$$

Now, in order to minimize the leakage current, the *switching vectors of the inverter configuration* are required to be *selected* in such a way that v_{Pg} becomes a constant over the complete period of the fundamental component. To apply this technique, the value of v_{Pg} for all possible switching combinations is required to be evaluated for the proposed converter. The parasitic voltage (v_{Pg}) corresponding to each space vector location is determined from eqn. (6.8) and summarized in Table 6.2.

It can be observed that, out of the total number of 49 space vectors, the maximum number of space vectors (i.e., 19) possessing the same value of v_{Pg} belong to Type-III, with a magnitude of $V_{PV}/2$. Hence it is evident that exclusive employment of these 19 space vectors would not cause any transition in the value of v_{Pg}, forcing dv_{Pg}/dt to become equal to zero (always). Consequently, the space vectors employed in this modulation technique (shown

Table 6.2: List of the available space vector combinations

Type	Space Vectors [S_R S_Y S_B]	Total common-mode voltage (v_{Pg})
I	[400], [040], [004],[211],[121], [112],	$v_{Pg}=5V_{PV}/6$
II	[311],[331],[131],[133],[113],[313],[221], [122], [212]	$v_{Pg}=4V_{PV}/6$
III	[222], [321], [231], [132], [123], [213], [312], [420], [441], [240], [141], [042], [144], [024], [114], [204], [414], [402], [411]	$v_{Pg}=3V_{PV}/6$
IV	[421], [241], [142], [124], [214], [412]	$v_{Pg}=2V_{PV}/6$
V	[440], [044], [404], [431],[341], [143],[134], [314],[413]	$v_{Pg}=V_{PV}/6$

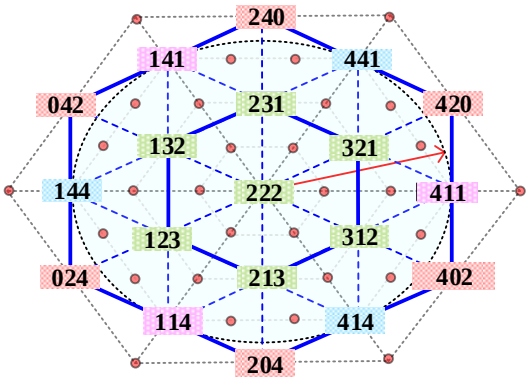


Figure 6.4: Formation of the space vector diagram from the selected switching vector location.

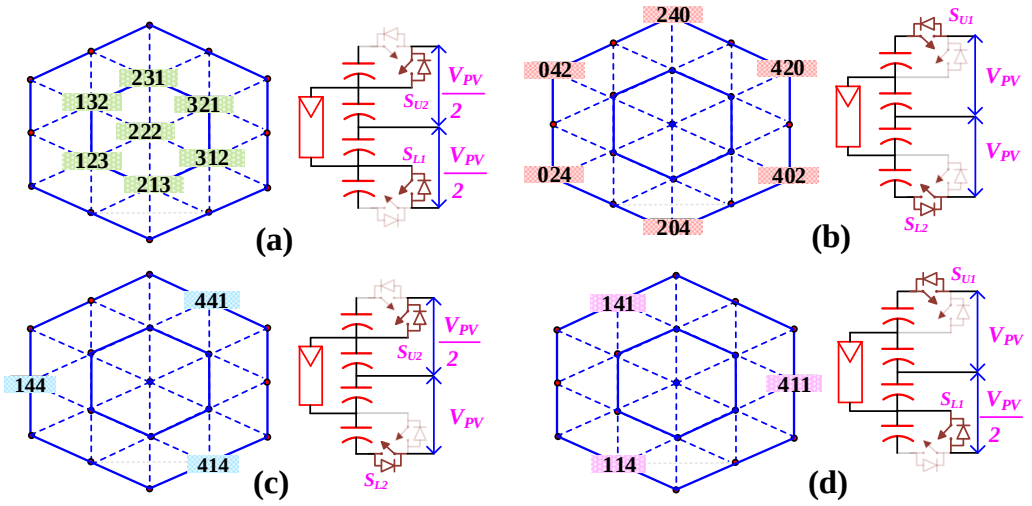


Figure 6.5: Space vector locations when following switch-pairs of the LSU are turned on (a) S_{U2}, S_{L1}; (b) S_{U1}, S_{L2}; (c) S_{U2}, S_{L2}; (d) S_{U1}, S_{L1}.

numbered) are indicated in Figure 6.4. It may be noted that these 19 vectors constitute a two-layered hexagonal structure with 24sectors as shown in Figure 6.4, facilitating three-level operation while maintaining a constant magnitude of v_{Pg}. This also eliminates all the corresponding transitions in the leakage current, which flows through the parasitic elements of the PV panel. Further, from the eqn. (6.5), it is evident that the difference between v_{Pg} and v_{CMVO} is distinguished by the voltage across the capacitor C_2 and PV voltage. Thus, the exclusively selected 19 space vector locations also result in the consonant common-mode voltage. It may further be appreciated that the proposed power converter overcomes the drawback associated with topologies such as the one proposed in [116], wherein the switching resources are underutilized to achieve a constant common-mode voltage. Besides that, all space vector locations are categorized as per the corresponding switching action in the LSU in Figure 6.5.

A linear PI controller is employed to regulate the voltage of SCs (V_{C1}, V_{C4}) to half of the input voltage (V_{PV}/2) as shown in Figure 6.6. The design and implementation of the the controller has followed the procedures given in chapter 3 section 3.3.1. In this control scheme also, two carrier signals (v_{carr1} and v_{carr2}, Figure 6.6), which are phase-shifted by 180^o, are employed to compare the outputs of the voltage controllers to generate the required gating

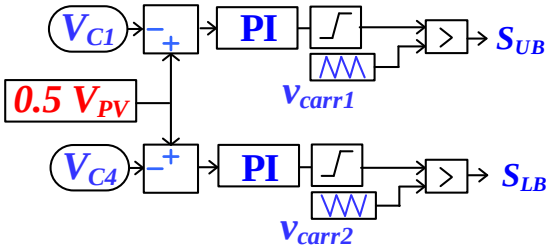


Figure 6.6: Implementation of the closed-loop voltage control scheme.

signals for each of the two devices of the interleaved buck-boost stage. The reference voltage for each of these two SCs (C_1 and C_4) is considered half of the input voltage (*i.e.* PV source voltage V_{PV}). Further, for both standalone, the modulation index is considered to regulate the output voltage. The overall block diagram for the proposed modulation strategy is shown in Figure 6.7. As the proposed configuration has a single input PV source, it requires only a single loop-based maximum power point tracking.

However, in a grid-connected system, an inner current controller can be suitably inserted to determine the required modulation index. The modulation index (m_a) determines the amplitudes of the modulation signals (v_{modR}, v_{modY}, v_{modB}) for the three phases. These modulation signals are then compared with two level-shifted, in-phase carrier waveforms and are further processed as shown in Figure 6.7 to generate the SV locations [S_R S_Y S_B] for the corresponding phases. Each space-vector index assumes one of the five values amongst [0, 1, 2, 3, 4]. Table 6.3 presents the conditions to be fulfilled to generate the PWM signals for the switching devices present in the LSU. Similarly, the devices of each output T-legs are switched based on the value of the corresponding space vector as given in Table 6.4.

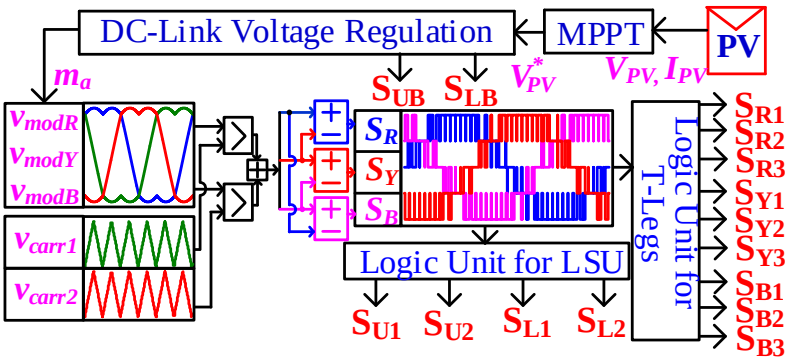


Figure 6.7: The control scheme for the proposed configuration with MPPT control.

Table 6.3: Logical Conditions for the Switches of the LSU

Device	**S_{U1}**	**S_{U2}**	**S_{L1}**	**S_{L2}**
Logical Condition to 'Turn-ON'	(S_R ==4) OR (S_Y ==4) OR (S_B ==4)	(S_R ==3) OR (S_Y ==3) OR (S_B ==3)	(S_R ==1) OR (S_Y ==1) OR (S_B ==1)	(S_R ==0) OR (S_Y ==0) OR (S_B ==0)

Table 6.4: Logical Conditions for the Switches of PGU (T-LEGs)

T-leg (Phase-R)		**T-leg (Phase-Y)**		**T-leg (Phase-B)**	
Device	**Cond.**	**Device**	**Cond.**	**Device**	**Cond.**
S_{R1}	S_R >2	**S_{Y1}**	S_Y >2	**S_{B1}**	S_B >2
S_{R2}	S_R ==2	**S_{Y2}**	S_Y ==2	**S_{B2}**	S_B ==2
S_{R3}	S_R <2	**S_{Y3}**	S_Y <2	**S_{B3}**	S_B<2

6.4 Analysis of Semi-Single Stage Operation

One of the important features of the proposed power circuit is that it can transfer a significant portion of the PV power directly to the load (referred to as 'single-stage operation'). The remaining portion of the generated PV power is processed through the VBU, shown in Figure 6.1 (referred to as 'double-stage operation'). To establish the relationship between the total load power and the power processed through each power stage (single-stage and double-stage), instantaneous power equations are derived with the help of switching functions and three-phase load currents (i_R, i_Y, and i_B). The switching variable for any particular switch S_k (k ∈ S_{R1}, S_{Y1}, S_{B1} …. etc.) is represented as S_{Sk} (i.e. S_{SR1}, S_{SY1} ...etc). The variable S_{Sk} assumes a value of '1' when the corresponding switch is turned on, and a value of '0' while it is turned off. The instantaneous power utilization (p_{C1} and p_{C4}) of the SCs are derived by summing up the power utilization corresponding to each phase as,

$$p_{C1} = p_{C1R} + p_{C1Y} + p_{C1B} = v_{C1}S_{SU1}(|i_R|S_{SR1} + |i_Y|S_{SY1} + |i_B|S_{SB1}) \quad (6.9)$$

$$p_{C4} = p_{C4R} + p_{C4Y} + p_{C4B} = v_{C4}S_{SL2}(|i_R|S_{SR3} + |i_Y|S_{SY3} + |i_B|S_{SB3}) \quad (6.10)$$

The symbols v_{C1} and v_{C4} respectively represent the voltages across the capacitors C_1 and C_4. The eqns. (6.3)-(6.4) are simulated assuming that the proposed power converter delivers a load of 1kW and the input voltage V_{PV} is 100V. Thus, the voltage across each capacitor is 50V i.e. ($V_{C1} = V_{C2} = V_{C3} = V_{C4} = 50$V).

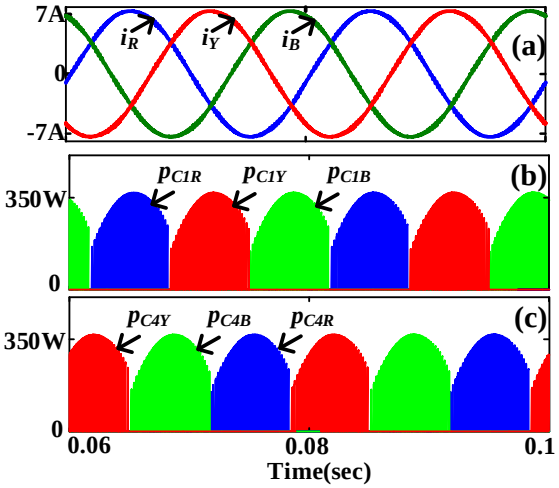


Figure 6.8: (a) Power utilization of C_1 for each phases (i.e. p_{C1R}, p_{C1Y}, p_{C1B}), (b) Power utilization of C_4 for each phases (i.e. p_{C4R}, p_{C4Y}, p_{C4B}).

The simulation results corresponding to the load currents and the power processed through the switched capacitor (p_{C1}, p_{C4}) are shown in figures 6.8(a), (b), and (c) respectively. Similarly, the instantaneous powers (p_{C2} and p_{C3}) of the DC-link capacitors are derived as:

$$p_{C2} = v_{C2}(|i_R|S_{R1} + |i_Y|S_{Y1} + |i_B|S_{B1}) \tag{6.11}$$

$$p_{C3} = v_{C3}(|i_R|S_{R3} + |i_Y|S_{Y3} + |i_B|S_{B3}) \tag{6.12}$$

Now, the total power (p_{Total}) can also be derived as,

$$p_{Total} = p_{C1} + p_{C2} + p_{C3} + p_{C4} \tag{6.13}$$

In order to determine the average energy utilization of each capacitor, in each power cycle, the energy utilization factors (E_i, where $i \in C_1, C_2, C_3,$ and C_4) are determined as,

$$E_{C1} = \frac{\int_0^{\pi} p_{C1} d(\omega t)}{\int_0^{\pi} p_{Total} d(\omega t)} = 20\%; \quad E_{C4} = \frac{\int_0^{\pi} p_{C4} d(\omega t)}{\int_0^{\pi} p_{Total} d(\omega t)} = 20\% \tag{6.14}$$

$$E_{C2} = \frac{\int_0^{\pi} p_{C2} d(\omega t)}{\int_0^{\pi} p_{Total} d(\omega t)} = 30\%; \quad E_{C3} = \frac{\int_0^{\pi} p_{C3} d(\omega t)}{\int_0^{\pi} p_{Total} d(\omega t)} = 30\% \tag{6.15}$$

It is evident from the above analysis that, the proposed configuration is capable of delivering 60% of the total PV energy through the single-stage operation (i.e. ($E_{C2} + E_{C3}$)). Also, the two DC-link capacitors are self-balanced as the single-stage energy is equally divided between them. The rest of the 40% of the PV energy is transferred through the double-stage operation (i.e. ($E_{C1} + E_{C4}$)). Since this energy is also distributed equally among the upper and lower SCs, the power loss and the size of the passive elements are reduced. In contrast, with the conventional front-end boost stage, the total energy is processed through two stages, incurring higher power losses in the dc-dc stage. In addition, the design of the passive elements (C_i, L_i) in the VBU can be derived using the following expressions:

$$C_i = \frac{4P_T f_m}{\omega v_{ph} f_{sw} \Delta V}; L_i = \frac{\sqrt{2} P_T V_{PV}}{3 v_{Ph} f_{sw} I_{Li}^2} \tag{6.16}$$

where P_T represents the total load power, ω is the electrical angular frequency, v_{Ph} is the RMS values of the output phase voltage, f_{sw} is the switching frequency of VBU, f_m represents the modulation frequency, ΔV indicates voltage ripple in the SC and I_{Li} is the peak value of the inductor current.

6.5 Simulation Results

The working principle and the performance of the proposed inverter configuration are validated through simulation studies using MATLAB-SIMULINK platform. The parameters related to inverter configuration and the modulation strategy are presented in Table 6.5. The leakage current for the inverter configuration is assessed by inserting an equivalent value of the parasitic capacitor (C_P) and resistor (R_P) across the PV positive terminal and the ground terminal. The value of the parasitic capacitance varies between 60nF-160nF [142] depending on the type of the PV panel and atmosphere conditions. To estimate the maximum value of the leakage current, a higher value of parasitic capacitance (100nF) is considered.

Table 6.5: Parameters for Simulation Study

V_{PV}	f_m	f_{swb}	f_{swb}	Load	C_2,C_3	C_1,C_4	L_1, L_2	R_P	C_P
100V	50Hz	10kHz	5kHz	45Ω, 2mH	1mF	1mF	3mH	5Ω	100nF

The performance and operation of the proposed three-phase inverter configuration are validated in both conventional phase-shifted pulse-width modulation (PSPWM) [113] and the proposed PWM strategy. The inverter output voltage, current, total common-mode voltage, and the leakage current are analyzed for both the PWM strategies and presented in Figure 6.9. It can be observed from figures 6.9 (a) and (e), that both the PWM strategies are capable of generating three-level waveforms at the output voltage. In addition, both of the PWM strategy effects in similar THD (*i.e.* 1.50%) at the load current with identical filter and load conditions. The total common-mode voltage (v_{Pg}), obtained with the conventional PSPWM contains voltage transitions of switching frequency. In contrast, the common-mode voltage obtained with the proposed PWM does not have any voltage transition, and a constant voltage magnitude is maintained at the parasitic elements. The capacitive parasitic path does not induce any leakage current with the application of the proposed PWM strategy. However, a significant amount of leakage current is induced for the case of conventional PWM strategy as the capacitive impedance of the parasitic path affects low-impedance to the high-frequency voltage transitions. Thus, the amount of leakage current induced by the conventional PWM

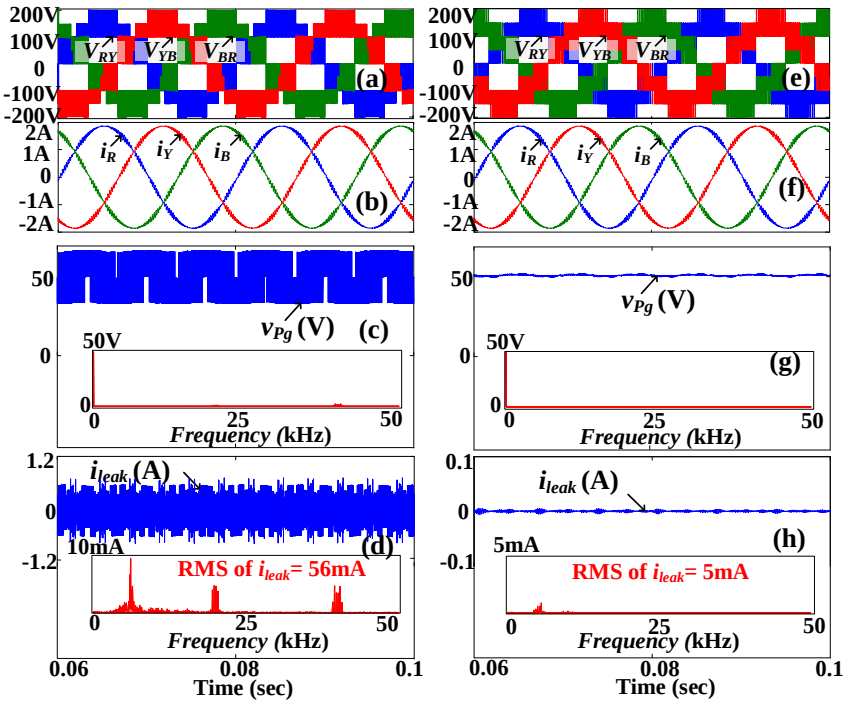


Figure 6.9: line-to-line voltage, three phase current (i_R, i_Y, i_B), common-mode voltage (v_{Pg}), leakage current (i_{leak}) with (a-d) PSPWM, (e-h) proposed modulation technique for 3-ϕ TBMLI configuration.

strategy is dependent on the input voltage of the inverter and the switching frequency of the inverter. The RMS value of the leakage current further violates the limit of 30mA, as stipulated by VDE0126-1-1 [26].

6.6 Experimental Results

The performance of the proposed power converter, along with the associated PWM technique, is assessed with experimental studies with the aid of a scaled-down prototype (Fig. 6.10). The circuit parameters, which are used for experimental validation, are listed in Table 6.6. The MOSFET IRF 460 along with the HCPL-3120 gate-driver are used in the hardware prototype. The gating signals for the switching devices, with the adopted modulation strategy, are obtained with the aid of a SPARTAN-6 FPGA platform. The experimental hardware prototype of the inverter configuration is shown in Figure 6.10.

A programmable dc-source with a voltage connected across the P and N terminals (Figure 6.1). The voltage waveforms of the SCs (v_{C1}, v_{C4}) and the corresponding currents (i_{L1}, i_{L2}) in the energy storage inductors are shown in Figure 6.11 (a). From Figure 6.11 (a), it is evident that the voltages across both of the SCs are regulated at 50V, while the total DC-link voltage ($V_{DC\text{-}link}$) is regulated at 200V. The three-phase line-to-line voltages (v_{RY}, v_{YB}, v_{BR}), along with input current (i_{PV}), are shown in Figure 6.11 (b). Furthermore, the blocking voltage

Table 6.6: Parameters for Experimental Prototype

V_{PV}	f_m	f_{swb}	f_{swi}	Load	C_2,C_3	C_1,C_4	L_1, L_2	R_P	C_P
100V	50Hz	10kHz	5kHz	45Ω, 2mH	1mF	1mF	3mH	5Ω	100nF

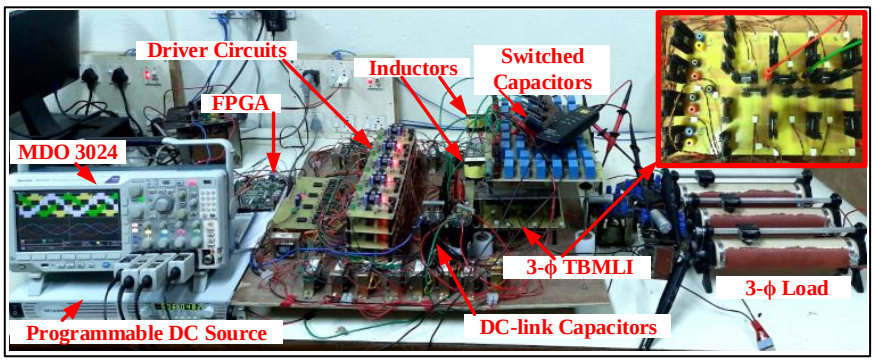


Figure 6.10: Experimental prototype for the proposed 3-ϕ TBMLI.

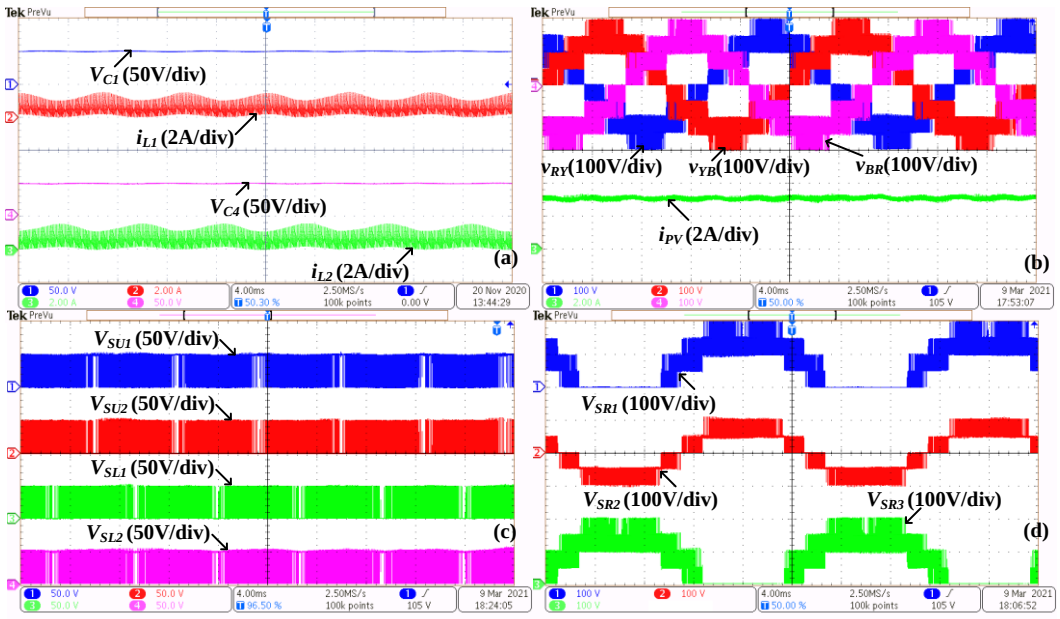


Figure 6.11: (a) SC voltages (V_{C1}, V_{C4}), and inductor currents (i_{L1}, i_{L2}), (b) three-phase voltage, input PV current, (c) and (d) blocking voltages of the switches in the LSU and R-phase respectively.

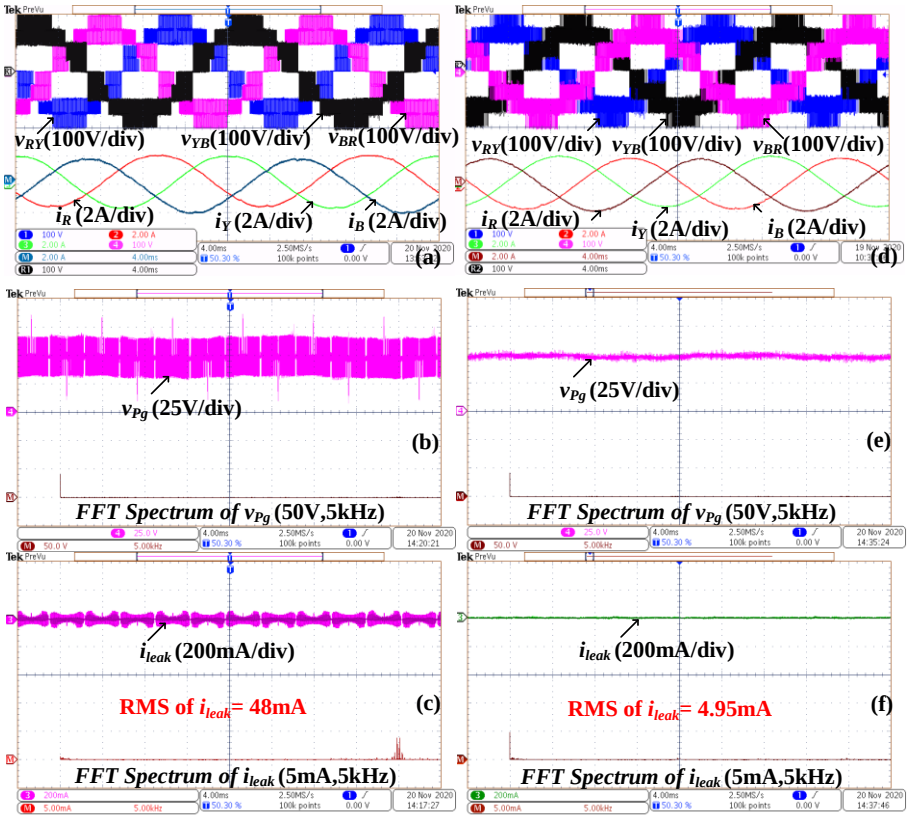


Figure 6.12: Experimental results for three-phase line-voltages (v_{RY}, v_{YB}, v_{BR}) and currents (i_R, i_Y, i_B) for conventional SPWM (a-c) and proposed PWM (d-f).

of the switches in the LSU and one of the phases (R-phase) are shown in Figure 6.11 (c) and (d) respectively. From these experimental results, it is evident that the switches in LSU should be rated to withstand 1/4th of the total DC-link voltage (i.e., $V_{DC\text{-}link}$ = 200V). Similarly, the top and bottom switches (e.g., S_{R1}, S_{R3}) of the phases and the bi-directional switch (e.g., S_{R2}) should be rated to withstand the voltages $V_{dc\text{-}link}$ and $V_{dc\text{-}link}/2$ respectively. Figure 6.12 presents the comparison of the inverter operation between the conventional phase-shifted SPWM strategy and the proposed PWM scheme at the limit of linear modulation. From these waveforms, it is apparent that the proposed PWM scheme doesn't compromise on the harmonic performance compared to the conventional SPWM scheme. In addition, to analyze the influence of this modulation strategy on the leakage current, the parasitic voltage (v_{Pg}) and the leakage current (i_{leak}) are measured and presented in Figure 6.12 ((a-c),(d-f)). Though the conventional phase-shifted SPWM technique with the proposed configuration has the capability of reducing the magnitude of high-frequency transitions to 50% [183], the leakage current is still strongly influenced by the switching frequency and the input voltage of the inverter. However, the proposed modulation strategy is capable of eliminating all high-frequency transitions from the total common-mode voltage (v_{Pg}) (Figure 6.12 (e)). Consequently, the leakage current through the parasitic capacitive elements of the PV panel is reduced (Figure 6.12 (f)). The RMS values of the respective leakage currents with the conventional phase-shifted and the proposed PWM (48mA and 4.95mA) support this fact. Thus, it is evident that the proposed configuration along with its modulation technique is capable of reducing the leakage current irrespective of the switching frequency and the input voltage of the inverter without sacrificing the harmonic performance and the DC-link utilization. Total elimination of transitions in parasitic voltage (v_{Pg}) reduces the requirement of additional common-mode chokes and EMI filters, which further improves the overall efficiency of the system.

Further, the performance of the inverter is validated in the grid-tie condition. The current loop is designed based on the control scheme given in [184-186] and the inverter parameters listed in Table 6.6. The values for proportional gain (k_{pc}) and resonant gain (k_{rc}) for the current control loop are obtained using the SISO Toolbox of MATLAB. The value of

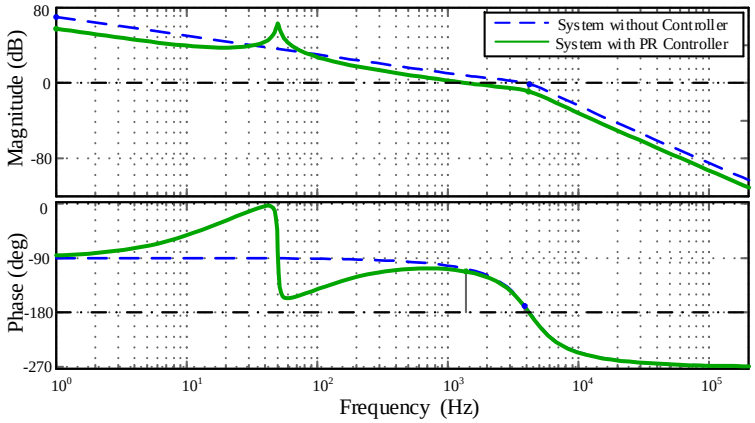


Figure 6.13: Bode plot for PR controller and the proposed integrated three-phase inverter.

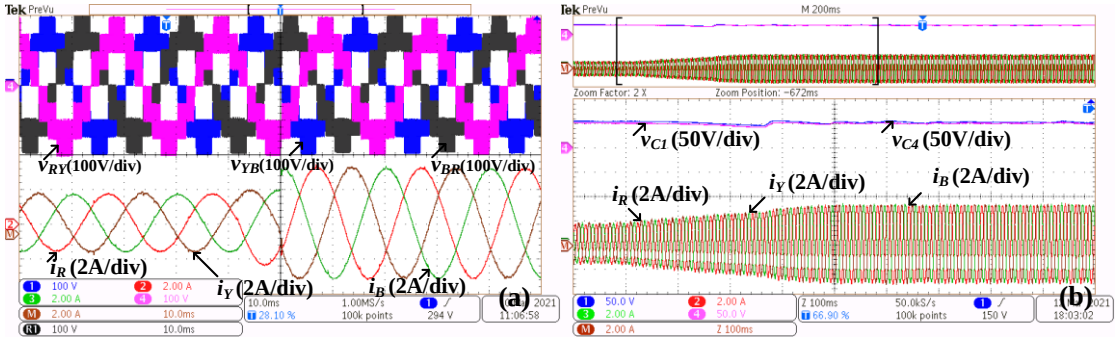


Figure 6.14: Three-phase line-voltages (v_{RY}, v_{YB}, v_{BR}) and currents (i_R, i_Y, i_B) at (a) step-change in load current, (b) dynamic variation in atmosphere condition.

k_{pc} and k_{rc} are obtained as 0.4 and 21.36 respectively for the three-phase inverter configuration. To ensure stability and a good dynamic response, the controller gains are selected to achieve gain margin and phase margin of the overall system as 9.02 dB and 67.6^0 respectively as shown in Figure 6.13. The dynamic behaviour of the proposed configuration for the variation of the load current and irradiance are shown in Figure 6.14 (a) and (b) respectively. It is observed that the control scheme is capable of regulating the SC voltages for both of these dynamic conditions.

6.7 Performance Analysis

A power-loss analysis has been carried out (Figure 6.15) using the PLECS software to compare the performance of the proposed voltage boosting strategy with the conventional boost strategy. The efficiency of the proposed system for both of the voltage boosting

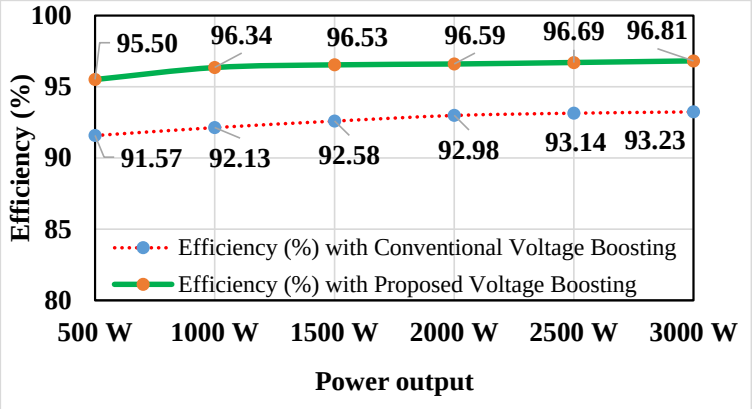


Figure 6.15: The plot of efficiency vs. power output for the proposed configuration and conventional voltage boosting strategy.

strategies is obtained at power output ranging from 500W to 3kW in steps of 500W as presented in Figure 6.15. The detailed thermal model of the switching device (IKW30N60T) and its body diode are extracted from the manufacturer's datasheet. The power losses incurred in the passive elements of these converters are also considered for comparison. It is observed that the power loss incurred in the inverting stage is the same for both conventional and the proposed voltage boosting techniques. However, the power loss incurred in the voltage boosting stage is significantly higher for conventional boosting methods. Thus, the improved efficiency of the proposed converter can be attributed to its partial direct power transfer capability.

A comparison of the proposed power converter with those reported earlier is summarized in Table 6.7. Though the configurations introduced in [116], [180], and [104] are capable of reducing the leakage current, they require a higher number of switching devices and isolated PV sources. Though the topology presented in [5] requires a reduced number of devices, the CMV and the leakage current are strongly influenced by the inverter switching frequency and the input voltage. In contrast, the proposed topology is capable of eliminating all hi-frequency transitions in the CMV, leading to the reduction of the leakage current while achieving a voltage boosting factor of '2'.

Table 6.7: Comparative analysis with the existing inverter configurations

Topology	A	B	C	D	E	F	G
[104]	24+0	6+0	4	3 p.u.	1	Constant	10mA
[116]	24+0	8+0	1	2 p.u.	1	Constant	10mA
[179]	16+2	6+0	2	2 p.u.	1	Oscillating	120mA
[180]	16+0	4+0	4	2 p.u.	1	Constant	10mA
Proposed	18+2	4+2	1	1 p.u.	2	Constant	12mA

A: Number of switches + diodes,
B: Number of capacitors + inductors,
C: Number of required isolated source,
D: Total DC-link voltage requirement,
E: Boost factor = (total DC-link voltage)/ (input PV voltage),
F: Nature of CMV,
G: Peak magnitude of the leakage current.

6.8 Conclusion

This chapter proposes an integrated three-phase inverter configuration, which is capable of: (i) synthesizing a three-level voltage waveform from a single PV source (ii) obtaining a boosting factor of two while limiting the inrush currents in comparison to the existing switched-capacitor (SC) based networks (iii) eliminating all of the voltage transitions across the parasitic capacitance of the PV panels, paving the way to the reduction of the leakage current irrespective of the PV panel voltage and the switching frequency of the inverter. The most important feature of this configuration is its capability of transferring a larger portion (60%) of the PV energy directly to the load; only 40% of it is processed through the boosting stage. This feature improves the overall efficiency of the system in comparison with the conventional boosting scheme. The proposed boosting stage results in an improved power density and equalization of power loss amongst the two interleaved sections. Owing to these features, it is envisaged that the proposed 3-ϕ TBMLI configuration is suitable for PV systems with three-phase output.

Chapter 7

Conclusions and Future Work

Chapter 7

Conclusions

7.1 General

This thesis proposes a few transformerless multilevel inverter configurations for PV systems. These configurations are structured to achieve integrated voltage boosting with reduced current stress on the power semiconductor switching devices. The modulation strategies, which are either originally proposed, or adopted from earlier works, reduce the leakage current to comply with the safety standard stipulated by the *VDE 0126-1-1*. The principles of operation of the proposed power converters are validated in both the standalone and the grid-tie modes.

The thesis consists of six chapters of which, the first is introductory, the second is an introduction to the existing transformerless PV inverter topologies and the rest are contributory investigations.

The major contributions of this thesis are as follows:

1. A single-phase, seven-level, transformerless inverter employing a semi-double stage-based conversion technique is presented. The proposed configuration achieves the required voltage boosting with a non-isolated interleaved buck-boost converter, which is fused into the inverter configuration through two switched capacitors (SCs). The interleaved front-end boost stage is capable of achieving a voltage gain of 3 while resulting in a reduced peak current stress on the switching devices. In this topology, 37% of the power supplied to the load is transferred directly from the PV source, while the rest of 63% is transferred through the SCs. The proposed topology and the associated pulse width modulation (PWM) technique are capable of reducing the leakage current by isolating the terminals of the PV source in the freewheeling state. Through a detailed mathematical analysis, numerical simulation, and experimental validation, it is shown that

both RMS and peak values of the leakage current are well below the German standard DIN VDE 0126-1-1.

2. A transformerless nine-level T-type hybrid boost inverter is proposed to achieve the twin objectives of voltage-boosting and multilevel inversion. The efficiency of the boosting stage of the proposed system is improved as 42% of the PV energy is directly transferred from the PV source to the load, while the rest is processed through an interleaved converter, which is fused with the inverter. This ensures a higher power density and reduces the power ratings of semiconductor devices. The proposed zone-based PWM technique achieves the complete elimination of voltage transitions corresponding to the switching frequency across the parasitic elements of the PV panel. This technique mitigates the leakage current while preserving the principal advantages of conventional multilevel inverters such as low *dv/dt*, and inductive power capability.
3. A single-phase transformerless 13-level inverter configuration is proposed, which requires a reduced number of switching devices. In this power converter, the back-end inverter is fused with the front-end interleaved voltage boosting network. The structural symmetry is capable of reducing the peak values of switch currents and thermal stresses on the semiconductor devices. A mathematical analysis is carried out to evaluate the effect of various switching states on the parasitic voltage and the common-mode voltage (CMV) in PV inverters with symmetrical as well as asymmetrical inductor filters. This analysis paves the way for the formulation of two PWM schemes. The first PWM scheme, which applies to inverters with asymmetrical filters, eliminates switching transitions from the PV parasitic voltage only. The second PWM scheme, which applies to inverters with symmetrical filters, achieves this objective along with the reduction of the common-mode voltage. Unlike the existing decoupling topologies, the proposed inverter configuration, along with its modulation strategies, does not require any additional switching resources to reduce the leakage current. While meeting the safety standards, it doesn't forego the advantages associated with the conventional multilevel inverters such as low dv/dt, and reactive power sourcing capability.
4. An integrated three-phase transformerless inverter configuration, which is capable of synthesizing a three-level (3L) voltage waveform at its output from a single PV source. Furthermore, high-frequency transitions in the voltage across the parasitic capacitive branch are altogether eliminated to facilitate an effective suppression of the leakage

current. It is shown that, with the aid of an interleaved dual-output buck-boost converter, the proposed configuration is capable of achieving a voltage boosting factor of two. The efficiency of the proposed power converter is considerably improved, as a significant amount of the PV power is transferred directly to the load. Further, mathematical equations are derived using the theory of switching functions to assess the amount of power that can be transferred directly to the load through the inverting stage.

It is therefore concluded that the common features across all of the proposed transformerless power converter configurations and proposed PWM schemes are that, all of them try to transfer a fraction of the total PV power directly, all of them try to achieve compliance with the VDE 0126-1-1 regarding the leakage current.

7.2 Scope for Future Work

Based on the research work presented in this thesis, further research may focus on the following aspects of transformerless PV inverters.

1. It would be interesting to explore the possibility of improving the efficiency of the interleaved buck-boost converter by employing soft-switching techniques, which reduce the switching losses.
2. The design of the proposed configurations can be further improved with the employment of active power decoupling techniques, which reduce the requirement of the DC-link capacitance. It would be interesting to explore the possibility of employing film capacitors for the SC, which improve the power density and the reliability of the inverter.
3. Throughout this thesis, a PR-based current controller is employed to synthesize the reference voltage vector for the proposed power circuit configurations. It makes an interesting study to investigate the applicability of advanced control schemes, such as model predictive control, deadbeat control, sliding-mode control, etc. to improve the dynamic performance of the inverter.

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