Design and Analysis of Modified GAA Nanosheet FET Based Circuits for High Frequency Applications

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by

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To the best of our knowledge, the work incorporated in this thesis has not been submitted elsewhere for the award of any degree.

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Dedicated to My

Parents, Gurus, & Friends

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ABSTRACT

Semiconductor devices transformed the human lives from the past few decades. The major technological breakthrough in semiconductor devices is the invention of Complementary Metal Oxide Semiconductor (CMOS) technology. Also, the heart of CMOS technology is Metal Oxide Semiconductor Field Effect Transistor (MOSFET). CMOS scaling is the driving mechanism for technological applications. However, in addition to the advantages, disadvantageous short channel effects (SCEs) also came into the picture with scaling. Thus, to get around the CMOS scaling limitations, some possible alternatives, such as multigate semiconductor devices are proposed. The multi-gate (MuG) based MOSFETs play a significant role in downscaling the MOSFET dimension, allowing for better control over the device carriers. Moreover, to enhance gate's electrostatic integrity and to achieve the SS close to the Boltzmann tyranny of 60 mV/decade, multi-gate (MuG) architectures such as double gate, trigate, Fin-shaped FET (FinFET), gate-all-around (GAA) nanowires (NW), and nanosheets (NS) can be used. The GAA nanosheet FET (NSFET) is proven to be a potential candidate to continue the scaling for sub-5-nm nodes.

In GAA NSFETs, the gate surrounds the channel in all directions. Wrapping the channel on all sides by the gate leads to greater gate control, lower power, minimized drain effect on channel electrostatics and reduced leakage in GAA NS transistors. For the same physical channel area as a FinFET, the GAA channel reduces SCEs and improves the effective area of the channel and hence boosting the drive current. Thus reduced SCEs with GAA FETs drive towards optimal performance and ensures continued scaling for future technology nodes. Increasing the number of stacked nanosheets is a viable option to increase the drive current. However, as the number of nanosheets increases, the parasitic capacitances also increase, which increases the delay of the device.

Therefore, in this thesis, the NSFET with two vertically stacked nanosheets is designed. Moreover, the geometry of the nanosheet plays a crucial role in the device's performance. Thus, it is highly essential to analyse the performance at different geometry of the nanosheet. Though some works addressed the geometrical impact at the device level, the geometry impact at high frequency circuit applications needs to be explored. The influence of geometry on DC metrics, Analog/RF metrics and circuit applications is analysed in detail by varying the geometry of the nanosheet.

Further, semiconductor devices are very much sensitive to variations in temperature. The impact of temperature on the multigate FETs is addressed by some researchers. However, none has addressed the impact of temperature on NSFET in high frequency circuit applications. Thus, in this work, the impact of temperature at both device and circuit levels is analysed for NSFET based high frequency circuit applications.

To continue the scaling, the effective area (W_{eff}) per footprint (FP) (W_{eff}/FP), needs to be reduced, which affects the performance of the device with scaling. Thus, it is essential to improve the on current without increasing the FP by using device engineering such as structural engineering and high-k gate stack engineering. Thus, to increase the W_{eff} under the same FP, the Fin-like interbridge is combined with nanosheets to form Comb-like-channel structure along with high-*k* gate stack is proposed. The proposed structure enhances the on current and switching ratios of the device significantly. Moreover, the device's behaviour in circuit applications such as ring oscillators is addressed and compared with traditional NSFET under the same FP. The analysis reveals that by using the proposed device, the performance of the device can be increased and is capable of scaling for sub-5-nm nodes.

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NOMENCLATURE

IC	Integrated chip
IoT	Internet of things
BTBT	Band to band to tunneling
DIBL	Drain induced barrier lowering
I_{OFF}	OFF-state leakage current
I_{ON}	ON current
V_{DD}	Supply Voltage
k	Dielectric constant
EOT	Equivalent oxide thickness
JL FET	Junctionless field effect transistor
f_T	Cut-off frequency
SOI	Silicon on insulator
MOSFET	Metal oxide semiconductor field effect transistor
CMOS	Complementary metal oxide semiconductor
SCEs	Short channel effects
V_{th}	Threshold voltage
RDF	Random dopant fluctuations
GAA	Gate all around
HP	High performance
AC	Accumulation
DG	Double gate
t_{ox}	Gate oxide thickness
TG	Trigate
BOX	Buried oxide
SS	Subthreshold swing
TGF	Transaction generation factor
C_{gd}	Miller Capacitance
C_{gg}	Gate capacitance
C_{ox}	Gate oxide capacitance
GBW	Gain band width product

L_G	Gate length
N_W	Nanosheet width
N_T	Nanosheet thickness
τ	Intrinsic delay
ITRS	International technology roadmap for semiconductors
IRDS	International roadmap for devices and systems
Q	ON-OFF performance metric
L_{eff}	Effective channel length
INV	Inversion mode
TFP	Transconductance frequency product
GFP	Gain frequency product
GTFP	Gain transconductance frequency product
EDP	Energy delay product
PDP	Power delay product
V_{EA}	Early voltage
WF	Work function
G_m	Transconductance
L_S	Source side spacer length
L_D	Drain side spacer length
I_{ON}/I_{OFF}	ON-OFF current ratio
V_{GS}	Gate voltage
V_{DS}	Drain voltage
I_D	Drain current
f_{OSC}	Frequency of oscillations
T	Temperature
I_{SC}	Switching current
NM	Noise margin
NML	Noise margin low
NMH	Noise margin high
V_M	Switching threshold

Chapter-1
Introduction

1.1 Introduction

Due to the ever-increasing demand for low-power, high-speed, and smaller-size electronic equipment, electronic gadgets have gotten a lot of attention in recent decades [1]. The device technology boosted the performance of various fields. From hand-held calculators, radios, walkmans, and CD/DVD players in the past to today's smart devices such as electronic wrist watches, smartphones, displays, cameras, sensors, smart driver-less cars, bipedal robots, and medical devices such as heart-beat measurement devices, pacemakers, and oximeters, as well as the internet of things (IoTs) are advanced by the continuous growth of semiconductor industry. Nanoelectronic devices with ultra-low power consumption are being explored extensively around the world in order to enable the aforementioned technological applications. The tremendous increment in functionality and substantial downsizing of integrated circuits is achieved by Complementary Metal Oxide Semiconductor (CMOS) scaling and which enabled the growth of IoT and the big data era [2], [3]. Mobile phones, which are equal to early supercomputers, are now a part of every household because of superb CMOS technology. MOSFETs (Metal Oxide Semiconductor Field-Effect Transistors) are the building blocks of CMOS circuitry, and they can be used as switches in integrated circuits. Usually, in the OFF-state, the switch should not consume any power, and the switching from the OFF-condition to the ON-condition should be seamless. However, MOSFET's subthreshold swing (SS) is restricted to the Boltzmann tyranny of 60 mV/decade due to the intrinsic thermionic injection method of conduction [4]. As a result, the supply voltage required to produce a reasonable switching ratio (I_{ON}/I_{OFF}) is strictly limited [5].

To enable applications that go beyond technological constraints, active research is being conducted all around the world on ultra-low power nano electronic devices. Since the first transistor invention in 1948 by Bardeen, Brattain, and Shockley at Bell Labs [6], [7] and the evolution of the Integrated Circuit (IC) in 1958 by Jack Kilby at IBM, the packing density of transistors in IC has been steadily improving over the time, following the well-known Moore's law trend [8], [9]. Then comes the development of the MOSFET, the most widely manufactured electronic device, sometimes known as the "workhorse" of the electronics industry. The

following Fig. 1.1 shows the number of transistors per integrated circuit with respect to process technology node from the year of the invention of the transistor by intel microprocessor.

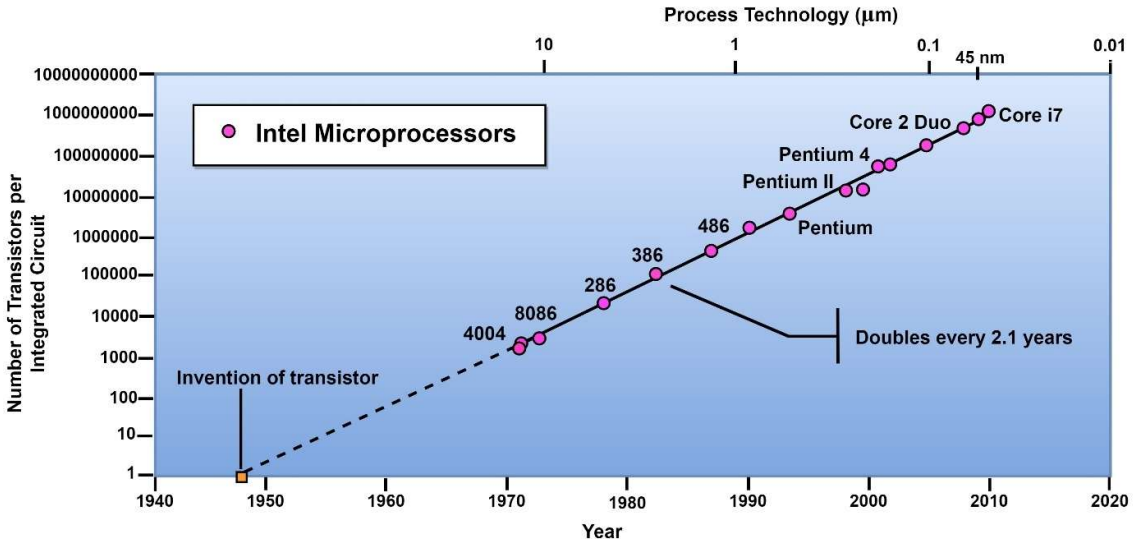


Fig. 1.1: Number of transistors per integrated circuit for various process technology nodes from the year of the invention of transistor by intel microprocessor [10].

The CMOS scaling created revolutions in human life. Microelectronics, a branch of electronics studies about miniature electronic components and designs, has grown substantially from MOSFET scaling over the past three decades. In addition to the enhancement in performance, the CMOS technology offered more benefits in terms of smaller physical device manufacturing with scaling. The higher package density and enhanced efficiency demonstrated the superiority of reduced physical size. Due to the decreased parasitic capacitances and supply voltages, this continual growth resulted in significant power savings per node, which increased Integrated Circuit performance [10].

Table 1.1 demonstrates various crucial parameters like processor name, number of transistors, area, process node, and fabrication techniques used for various CPUs built since the year 2000, explaining the trend of scaling. SCEs and greater gate leakage currents, which become much more prevalent at smaller dimensions, limit device performance in terms of microprocessor speed, and power consumption with MOSFET scaling [11]. With scaling, the disadvantages like poor gate electrostatic integrity, increased leakage currents, performance/power ratio and reliability of the device. Gate induced drain leakage (GIDL), DIBL, SS, gate oxide tunnelling of carriers, and source/drain direct tunnelling are examples of SCEs that degrade device

performance and consequently alter subthreshold characteristics. In section 1.4, these adverse effects are discussed in detail.

Processor	Process	Year	Area	Transistors	Designer	Fabrication technology
Pentium 4 Willamette	180 nm	2000	217	4.20×10^7	Intel	-
Pentium III Tualatin	130 nm	2001	81	4.50×10^7	Intel	-
Itanium 2 McKinley	180 nm	2002	421	2.20×10^8	Intel	Bulk CMOS process
Itanium 2 Madison 6M	130 nm	2003	374	4.10×10^8	Intel	-
Pentium 4 Prescott	90 nm	2004	110	1.12×10^8	Intel	-
Pentium D Smithfield	90 nm	2005	206	2.28×10^8	Intel	-
Core 2 Duo Conroe	65 nm	2006	143	2.91×10^8	Intel	-
Pentium 4 Cedar Mill	65 nm	2006	90	1.84×10^8	Intel	-
POWER6	65 nm	2007	341	7.89×10^8	IBM	Partially depleted SOI
Core 2 Duo Wolfdale	45 nm	2007	107	4.11×10^8	Intel	-
AMD K10 quad-core 6M L3	45 nm	2008	258	7.58×10^8	AMD	SOI Technology
Six-core Xeon 7400	45 nm	2008	503	1.90×10^9	Intel	High-*k* process
Six-core Opteron 2400	45 nm	2009	346	9.04×10^9	AMD	SOI technology
8-core POWER7 32M L3	45 nm	2010	567	1.20×10^9	IBM	-
16-core SPARC T3	40 nm	2010	377	1.00×10^9	Sun/Oracle	-
Six-core Core i7 (Gulftown)	32 nm	2010	240	1.17×10^9	Intel	-
10-core Xeon Westmere-EX	32 nm	2011	512	2.60×10^9	Intel	High-*k*/Metal Gate
Atom "Medfield"	32 nm	2012	64	4.32×10^9	Intel	High-*k*/Metal Gate
61-core Xeon Phi	22 nm	2012	720	5.00×10^9	Intel	Trigate

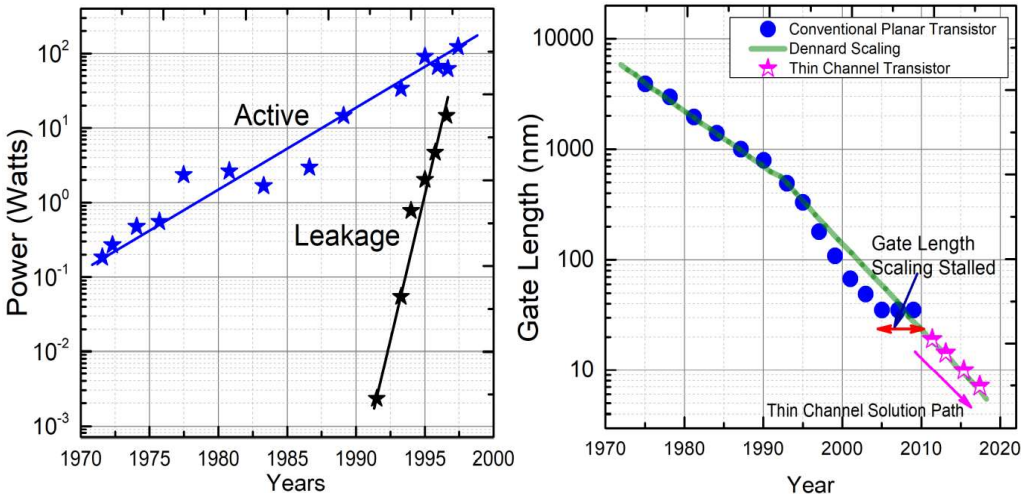
Quad+GPU Core i7 Ivy Bridge	22 nm	2012	160	1.40 x 109	Intel	FinFET Tri Gate transistors
Six-core Core i7 Ivy Bridge E	22 nm	2013	256	1.86 x 10^9	Intel	FinFET Tri gate transistors
A7 (dual-core ARM64)	28 nm	2013	102	1.00 x 10^9	Apple	High-*k* metal gate process
18-c Xeon Haswell-E5	22 nm	2014	661	5.56 x 10^9	Intel	-
A8	20 nm	2014	89	2.00 x 10^9	Apple	-
A8X	20 nm	2014	128	3.00 x 10^9	Apple	-
A9	14 nm	2015	96	2.00 x 10^9	Apple	FinFET process
A9X (dual-core ARM64)	16 nm	2015	143.9	3.00 x 10^9	Apple	FinFET+ Process
Xeon Broadwell-E5	14 nm	2016	456	7.20 x 10^9	Intel	Trigate FinFET
Snapdragon 835	10 nm	2016	72.3	3.00 x 10^9	Qualcomm	FinFET Process
A11 Bionic	10 nm	2017	89.23	4.30 x 10^9	Apple	FinFET process
Snapdragon 850	10 nm	2017	94	5.30 x 10^9	Qualcomm	FinFET Process
Tegra Xavier SoC	12 nm	2018	350	9.00 x 10^9	Nvidia	FinFET process
GC2 IPU	16 nm	2018	825	2.36 x 10^{10}	Graphcore	FinFET process
Snapdragon 8cx	7 nm	2018	112	8.50 x 10^9	Qualcomm	FinFET Process
A12X Bionic	7 nm	2018	122	1.00 x 10^{10}	Apple	FinFET Process
A12 Bionic	7 nm	2018	83.27	6.90 x 10^9	Apple	FinFET process

Table 1.1: Area, designer, production year (2000 onwards), process node count of transistors, and fabrication technology for various processors [12].

1.2 CMOS Technology Scaling

Power consumption is an important consideration in the design of modern integrated circuits. Users want a portable hand-held device with a longer battery life in general. CMOS circuits should therefore be designed in such a way that they dissipate less power. In CMOS circuits, power consumption is majorly classified into two categories. Those are (a) dynamic power

consumption, which is due to the charging and discharging of the load capacitor while switching, and (b) static power consumption, which is the leakage power consumed by the device in idle condition.



(a) **(b)**

Fig. 1.2: (a) Various power consumptions [4], (b) gate length scaling with respect to time [8].

When the size of MOSFETs is scaled down, the dynamic power dissipation decreases due to a decrease in gate capacitance. However, at the beginning of the 1990's, dynamic power started dominating overall consumption [4], [13]. Furthermore, as demonstrated in Fig. 1.2(a), the active and leakage power increases dramatically every year [8]. In order to increase the packing density of transistors in ICs, the transistor size is reduced by scaling down the channel length and other device parameters. The electrostatic integrity of silicon CMOS devices began to deteriorate due to leakage through scaled ultra-thin gate oxide and different device characteristics, resulting in the introduction of unfavourable SCEs such as DIBL, gate leakage, and threshold voltage roll-off [14]. The high-*k* metal gate (HKMG) is suggested as a way to avoid leakage through ultra-thin oxide [15], [16]. Despite HKMG solutions, rising leakage power reached active power levels around the year 2000, arresting scaling patterns Fig. 1.2 (b).

However, further downscaling the conventional MOSFET is cumbersome due to various adverse SCEs which limit the processor efficiency and power dissipation aspects. To prevent leakage power dissipation and improve gate controllability, Multiple gate FETs like FinFET (Fin Field Effect Transistor), ultra-thin body and box (UTBB) fully depleted silicon-on-insulator (SOI) are proposed [17]. These options laid the groundwork for keeping Moore's law alive for future scaling.

1.3 Conventional MOSFET

Usually, the conventional MOSFET contains four terminals called source, drain, gate, and body. The schematic of conventional n-type MOSFET is shown in Fig. 1.3. As it is well known, the n-type MOSFET's channel and body are doped with p-type impurities, whereas, the source/drain are doped with n-type impurities.

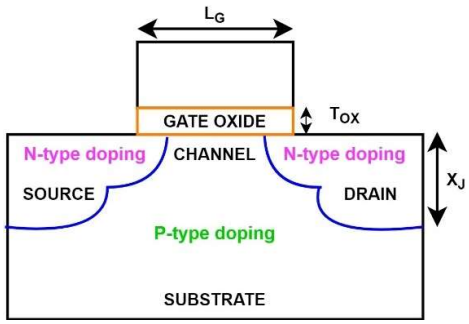


Fig. 1.3: Schematic view of conventional MOSFET [18].

However, for p-type MOSFET, the source/drain terminals are doped with p-type doping, and the channel is doped with n-type impurities.

The body of a MOSFET is often connected to the source, resulting in a three-terminal device known as a field-effect transistor (FET). The voltage applied at the gate terminal controls the channel that exists beneath the gate region. Insulating oxide (SiO_2) separates the gate terminal from the silicon material, resulting in a strong interface between the gate and channel. In n-channel operation, the drain is biased at a higher potential than the source. When the applied voltage is zero at the gate terminal, the current between the source and drain is comparatively low due to the large potential barrier for electrons between the source and channel; this is referred to as the transistor's OFF state. The minority carriers in the substrate are drawn to the channel surface when a positive bias is applied to the gate terminal owing to the electric field created across the gate dielectric (hence, the field effect). Inversion mode refers to the accumulation of minority carriers in the channel, which inverts the type of free carriers present at the channel's surface. The inverted channel acts as a conducting layer between the source and drain terminals. As a result, a substantial current flow exists in the device, indicating that the device is in the ON state. By utilizing these ON and OFF mechanisms, the MOSFET can be used as a switch. The switch should be turned OFF when the voltage provided to the control gate is less than a predetermined threshold voltage (V_{th}). The device should be ON with a limited

amount of current (indicated as I_{ON}) between the source and drain once the control gate voltage is above V_{th}. The MOSFET, on the other hand, is unable to attain optimal switching behaviour. The gate is normally operated in the positive voltage regime for n-channel operation. The subthreshold region is defined as the range of gate to source voltages (V_{GS}) between 0 V and V_{th}, where the current grows exponentially with gate voltage. Depending on the bias applied for above V_{th} the MOSFET can be operated in either linear or saturation regions [18].

1.4 Short Channel Effects

Short channel length devices are more prone to SCEs due to the merging of depletion zones below the gate between the source and drain junctions. As a result, the electrostatics of the channel area of short channel MOSFETs are influenced by the gate voltage, as well as the source and drain voltages. The threshold voltage is reduced as a result of the significant sharing of channel depletion charges by the depletion zones of the source/channel and drain/channel junctions. Reduced gate length in nanoscale MOSFETs has a number of negative consequences, including reduced V_T, increased I_{OFF}, higher SS, increased power dissipation, deteriorated DIBL, hot carrier effects, minimised effective channel length (channel length modulation), increased GIDL, increased gate-oxide tunnelling leakage current, direct source to drain quantum tunnelling (ballistic transport), surface scattering, and impact ionisation. In MOSFET scaling theory, these effects are referred to as short-channel effects (SCEs). Some important SCEs are discussed as follows:

1.4.1 Drain Induced Barrier Lowering (DIBL):

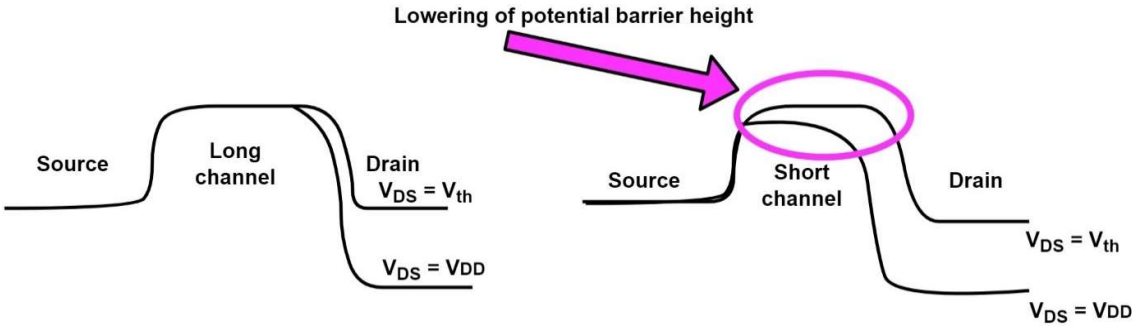


Fig. 1.4: The effect of DIBL on (a) Long channel (b) Short channel MOSFET [18], [19].

In conventional MOSFETs, the gate alone controls the flow of current through the channel. However, when channel length decreases, the drain begins to act as a second gate, i.e., the drain current, I_D is controlled by both gate and drain voltages. Usually, for long channel devices, with

the rise in $V_{DS,}$ the drain side bands only affect. However, as the gate length shortens, rise in the V_{DS} leads to the lowering of the source to channel barrier (which the gate should be able to regulate) also. This phenomenon is often referred to as drain induced barrier lowering [18], [19] which is shown in Fig. 1.4.

1.4.2 Subthreshold Swing (SS):

Sub-threshold swing (SS) is an important metric for device application in logic circuits. The SS is defined as the change in the gate voltage needed to get a decade change in current. For a MOSFET SS can be given by the equation shown [20]:

$$SS = \left(\frac{KT}{q}\right) * \ln(10) * (1 + (C_D/C_{Ox})) \quad (1.1)$$

Here, T is the temperature in kelvin, q is the electron charge, C_D is the depletion capacitance, and C_{ox} is the gate oxide capacitance. The term $(1+C_D/C_{ox}) \geq 1$ denotes the coupling efficiency of the gate voltage to the channel potential. Even the second term is ignored since it is less than 1. The first term limits SS to 60 mV/Decade. Thus, for MOSFET, the SS is limited to 60 mV/dec, which is the thermodynamic limit, also called as Boltzmann limit. The SS value tends to rise with short channel lengths.

1.4.3 Channel Length Modulation:

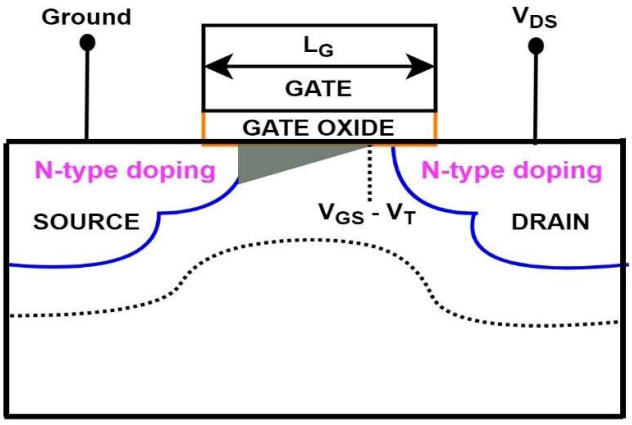


Fig. 1.5: Channel length modulation illustration in MOSFET [18].

When the drain voltage, V_{DS} exceeds the gate overdrive voltage, pinch off occurs at the drain end by a length of ΔL_G [21], [22] as shown in Fig. 1.5.

The relation between I_D and ΔL_G can be expressed as [22]:

$$I_D = I_{Dsat}/(1 - \Delta L_G/L_G) \quad (1.2)$$

Here, ΔL_G is more critical parameter and is a function of V_{DS} in the short channel device. The device exhibits non-saturation behaviour and lowering V_{th} due to the channel length modulation. For shorter channel lengths, the V_{th} is a strong function of L_G, and it falls drastically for shorter channel lengths [23]. It is also known as V_{th} - roll off with L_G scaling.

The drain current (I_D) becomes relatively constant with respect to the drain voltage when $V_{DS} \geq V_{GS}$-V_{th}, and the device is considered to be in the saturation regime. The inversion charge $Q_{I(x)}$ approaches zero when V(x) approaches V_{GS}-V_{th}. Where V(x) is the channel potential, the inversion charge density $Q_{I(x)}$ is proportional to V_{GS}-V(x)-V_{th} [24]. As a result, the creation of the channel inversion area is limited to the region $0 \leq x \leq$ L' channel length (L) below the gate for $V_{DS} > V_{GS}$-V_{th} and the MOSFET is said to be in the pinch-off situation. Further, increase in V_{DS}, the effective channel length (L') reduces. Thus, the channel length modulation refers to L's dependence on the drain voltage [18], [25]. In the saturation region, this effect lowers channel resistance and raises drain current (I_D). In other words, while the device is in its saturation mode of operation, the slope of the I_D-V_{DS} curve becomes slightly positive and alters from the ideal zero value.

1.4.4 Gate Oxide Leakage:

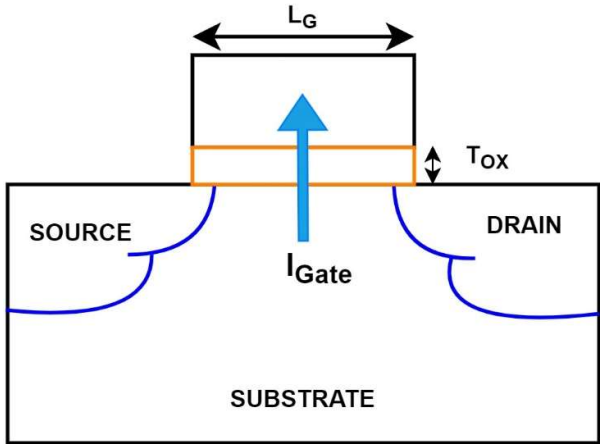


Fig. 1.6: Leakage current through gate oxide in MOSFET [18].

In the MOSFET structures, the SiO_2 is a suitable contender and an excellent insulator. With scaling, it is inevitable to scale gate oxide thickness. However, when the oxide thickness reaches scaling of less than 3 nm, the carriers tunneling probability rises, resulting in gate oxide leakage

current [18], [26]. As a solution for this, a high-*k* dielectric material is utilised to avoid gate oxide tunneling. The direct tunneling of carriers is reduced with high-*k* dielectric oxide.

1.4.5 Velocity Saturation:

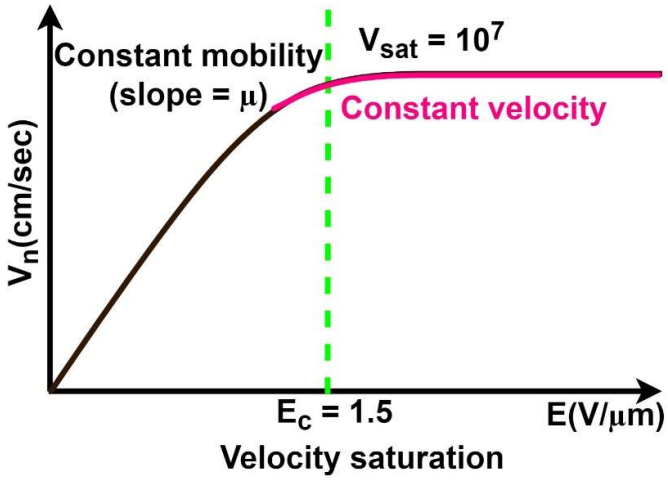


Fig. 1.7: Velocity saturation in MOSFET [18].

The carriers' velocity tends to saturate at higher electric fields due to mobility saturation. Constant field scaling helps to sustain the equal electric fields and can be advantageous. However, constant field scaling is not always preferred by the semiconductor industry [27]. For example, compared to supply voltage scaling, oxide thickness scaling is more at particular technology node. As a result, in nano-scale MOSFETs, higher electric fields are present and tend to be the saturation of carriers. There will be no adverse effect if saturation is attained at drain voltages larger than the overdrive voltage. However, at the nanoscale regime, this phenomenon can be observed at lower drain voltages and offers less ON current. From Fig. 1.7, it is noticed that for lower electric fields the velocity increases linearly, whereas, for higher electric fields, it tends to saturate at 10^7 cm/s around $E_c=10^5$ V/cm at room temperature [19].

1.4.6 Surface Scattering:

As the depletion layer extends laterally into the channel area with scaling, the lateral electric field tends to rise, due to which the surface mobility is affected by electricfield. The surface scattering mechanism in the thin inversion layer of MOSFET tends to reduce the mobility under the influence of vertical electric field. Thus, travelling parallel to the surface is difficult for the carriers [28], as shown in Fig 1.8.

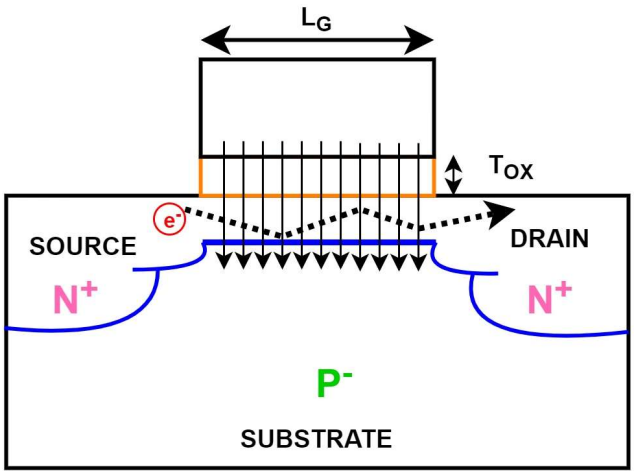


Fig. 1.8: Surface scattering effect in MOSFET [28].

1.4.7 Gate Induced Drain Leakage (GIDL):

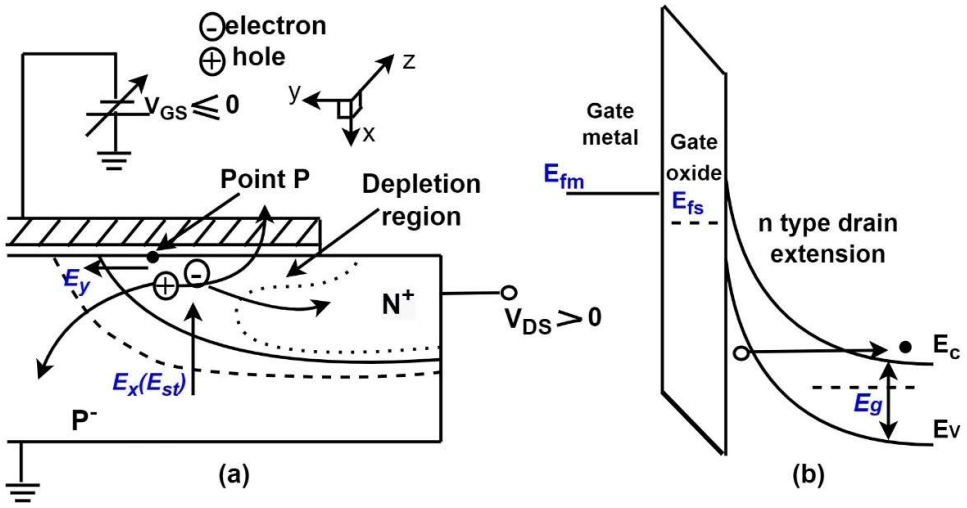


Fig. 1.9: (a) The GIDL effect in the MOSFET (b) Electron tunneling phenomena by GIDL effect [31].

Usually, the electric field between the gate-end of the channel and the drain/channel junction is quite strong when a high drain bias voltage with low or negative gate bias voltage is applied to MOSFETs. Tunneling of electrons from the channel valence band to empty states in the drain region is likely to happen [29], which is shown in Fig 1.9(a) and (b). In OFF-state, this band-to-band tunnelling (BTBT) exacerbates the drain leakage current in MOSFETs and leads to more static power dissipation.

1.4.8 Random Dopant Fluctuations (RDFs):

In nanoelectronics devices, random doping fluctuations (RDFs) are a severe concern, resulting in the loss of different performance metrics like effective carrier mobility and threshold voltage (V_{th}). As the doping in nano electronic devices cannot be accurately controlled, minimising these effects becomes more difficult. Initially, this problem is addressed by Meng-Hsueh Chiang [30]. He stated that extremely scaled nano electronic devices are more prone to RDFs. Ultra-short nano scale devices having gate length around 12 nm have the highest RDF impact. This may be attributed to the fact that maintaining ultra-sharp doping gradients near S/D junctions is highly difficult at this level. A few orders of change in doping concentration at both channel and source/drain is required while moving from source to channel and then channel to drain within a few nanometres, which further raises the thermal budget requirements substantially. The researchers explored many methods to overcome this issue. According to Tetsu Ohtou et al., SOI-based nano electronic devices are more resistant to RDF and process variations when the substrate impurity concentration is higher than that of the channel [31]. Electrostatic doping (ED) has lately emerged as a potential technique for doping nanoscale electronics, in contrast to the regularly used ion-implantation strategy. In summary, we may conclude that addressing the issue of uniform doping at the nanoscale is fundamental.

1.4.9 Direct Source to Drain Quantum Tunneling:

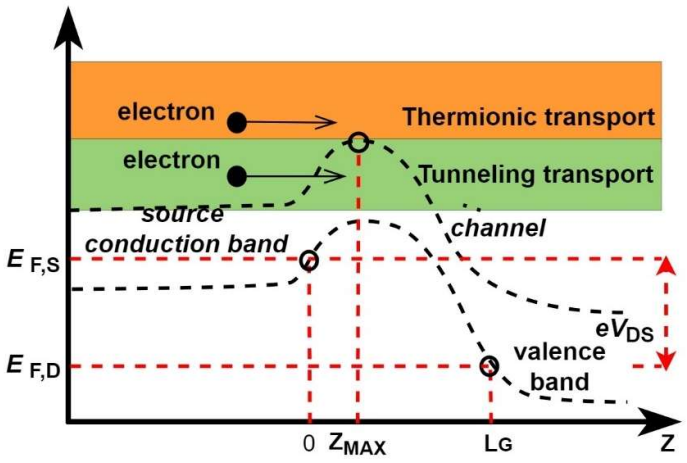


Fig. 1.10: Ballistic transport mechanism in the MOSFET [18].

As the channel length shrinks, the lateral electric field in the channel grows. The likelihood of carriers tunneling directly from the source to the drain through the incredibly narrow channel between them increases in the presence of a strong electric field in the channel. This ballistic

transport phenomenon must be considered for calculating the device parameters of MOS transistors with channel lengths below 30–40 nm. The ballistic transport for nearly less than 10 nm channel length contributes to a leakage current in addition to the thermionic current [32] and is shown in Fig. 1.10.

1.4.10 Impact Ionization

Due to the high electron velocity in the channel of a short-channel MOSFET in the presence of a strong electric field, the impact ionisation process can produce electron-hole pairs in the depletion zone of the channel/drain junction. Gate leakage current, GIDL, and substrate leakage current are all unwanted for the device if the generated carriers travel toward the gate, drain, and substrate [33]. Any remaining holes collect in the bulk substrate as the electrons travel in the direction of the drain. Fig. 1.11 depicts the various contributions to the unwanted substrate leakage current in MOSFETs by forming the p-type base of an n-p-n parasitic BJT [34].

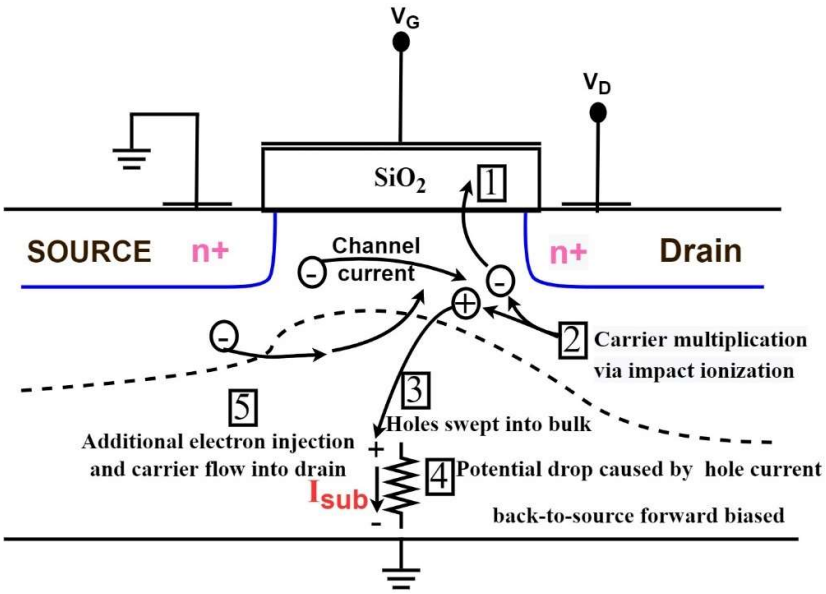


Fig. 1.11: Various leakage current mechanisms in the MOSFET [18].

1.4.11 Hot Carrier Effects

There is a strong electric field at the drain side of the MOSFET with high V_{DS} and low V_{GS}. The increasing lateral field may induce the carriers to accelerate at the channel-drain junction. Certain carriers may thereby accumulate sufficient kinetic energy to pass through the gate oxide dielectric region, damaging the channel/oxide contact as shown in Fig. 1.12.

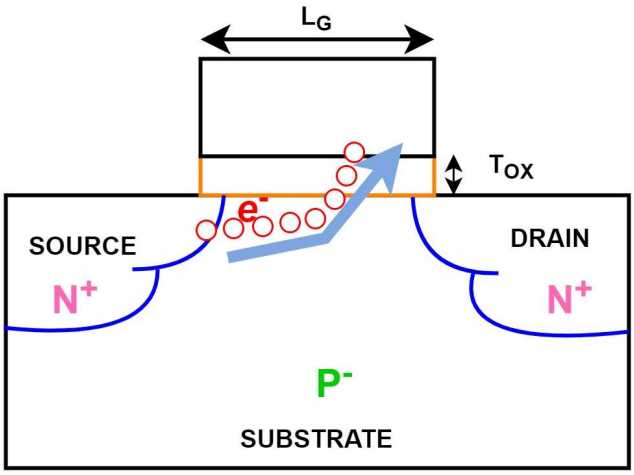


Fig. 1.12: Schematic of hot carrier effect of MOSFET [18].

This might change the oxide interface charges, which would disrupt the device's usual electrical behaviour. At higher fields, hot carriers could harm the oxide interface and affect the device's operation [30].

1.4.12 Punch Through Effect

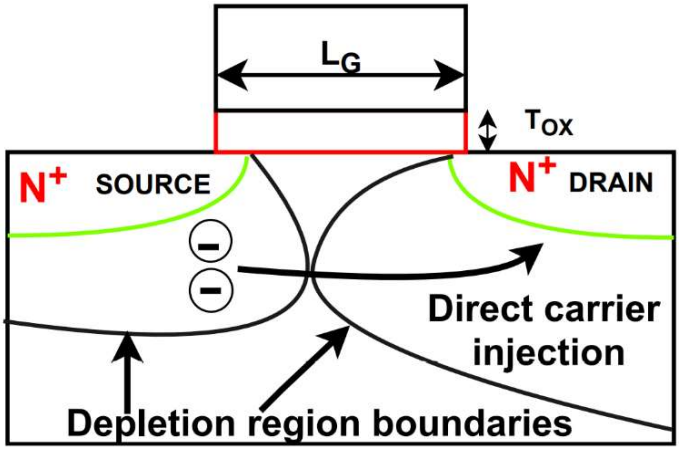


Fig. 1.13: Effect of the punch through in the MOSFET [18].

The punch through effect happens in a MOSFET when the depletion areas between the source/channel and the channel/drain unite to form a single depletion zone, as shown in Fig. 1.13. In this situation, the drain current is not controlled by the gate voltage, and it rapidly rises with the drain voltage. Punch through effect can be lessened by increasing substrate doping, using thinner oxides, and using junctions with shallower depths [35].

1.5 Multigate Architectures

In order to further reduce the MOSFET size and improve control over the channel, multi-gate (MuG) based MOSFETs are crucial. Moreover, to obtain the SS close to the Boltzmann tyranny of 60 mV/decade, multi-gate (MuG) architectures are proposed. Double gate [36], [37], trigate [38], and gate-all-around FETs [39]–[42] are some examples of MuG FETs and are shown in Fig 1.14. In double gate, the gate covers the channel in top and bottom directions. The gate covers both sides and the top of the channel in trigate structures. In gate all around (GAA) structures, the gate wraps around the channel on all sides. For scaling feasibility, the GAA topologies are the most promising for ultimate MOSFET scalability. The GAA structures offer the best controllability over the gate as the gate wraps around the channel in all directions. SCEs such as SS, DIBL, V_{th} roll-off, etc., are thereby greatly diminished in GAA nanowire (NW)/nanosheet (NS) MOSFETs, bringing SS closer to the desired 60 mV/decade limit.

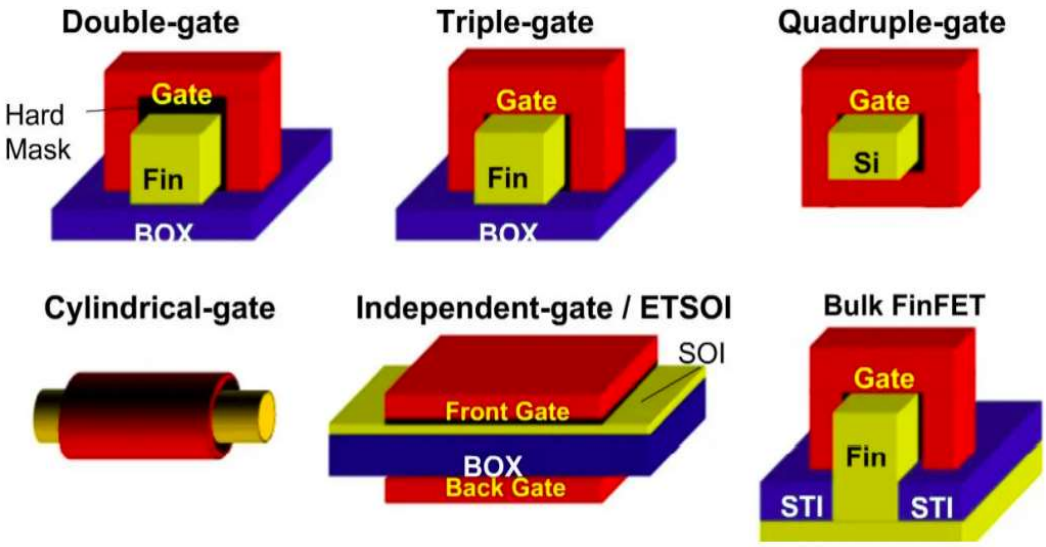


Fig. 1.14: Various Multigate FET architectures [36].

1.5.1 Fin Field Effect Transistor (FinFET):

Intel was the first significant semiconductor company to commercialise 14 nm FinFET technology in 2014. On a silicon-on-insulator (SOI) or bulk silicon wafer, a Fin shape channel is etched and patterned to create a FinFET. Unlike MOSFETs, where the channel is solely controlled by one gate, FinFETs use gate structures which regulate the channel in three directions. As a result, thin fin can be regulated by the gate more effectively than planar MOSFETs. FinFETs have far better gate control than planar MOSFETs, which significantly

reduces leakage current. In FinFETs, the effective area of the channel is increased, resulting in greater drive current compared to the planar MOSFET [37], [43]. As a result, FinFET enables a large packing density of ICs [44]. Moreover, technology giants like TSMC announced the manufacturing of FinFET at advanced (7 nm) technology nodes [45]. However, at these lower nodes, disadvantageous SCEs like threshold voltage roll-off, SS degradation, DIBL, increased power consumption, and higher parasitic capacitances are raised. Moreover, scaling of FinFET became difficult for sub-5-nm nodes as it possesses fabrication difficulties and reliability issues.

1.5.2 GAA Nanosheet FETs

Advanced multi-gate architectures such as GAA nanosheet FET (NSFET) transistors are proposed (Fig. 1.15) to continue the scaling for sub-5-nm nodes [39]. The GAA FETs received a lot of attention in recent years owing to their superior electrical performance. Interest in NS architectures has increased as a result of Intel, IBM, Global Foundry, and IMEC's announcement that they are going to adapt the GAA FETs into their IC fabrication [46]. As the gate covers the channel in all directions, superior gate control, lower power, minimizing the effect of drain effect on channel electrostatics and reduced leakage in GAA NS transistors can be achieved by using GAA FETs [47], [48]. Under the same footprint (FP), compared to FinFET, the GAA NSFET can reduce SCEs and improve device performance [49].

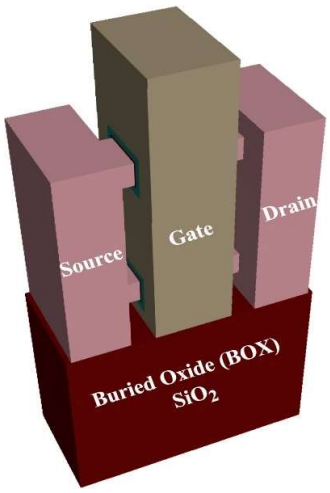


Fig. 1.15: GAA Nanosheet FET.

As a result, the GAA FETs promote optimal performance and ensure the scaling of the transistor for future technology nodes to manifest Moore’s law.

1.6 Motivation

Multi-gate structures are proposed in the literature to improve device performance. Fin-shaped Field Effect Transistor (FinFET) was ideal for sub-22-nm technology nodes. However, it is shown that for sub-7-nm node technologies, the scaling feasibility of FinFET is questionable and more prone to SCEs. As a result, researchers came up with a solution for the gate all around (GAA) structures such as Nanosheet FETs. Major industry giants announced that Nanosheet FETs are going to be adopted by their fabrication units.

The GAA Nanosheet FET is proven to be capable of continuing Moore's law for sub-5-nm technology nodes. Though various literature is available on Nanosheet FET [49]–[53], the impact of device geometry on Nanosheet FET and its circuit applications needs to be addressed in detail. Further, semiconductor devices are meant to be used at various temperatures [54]. As the nanoscale devices are very much sensitive to temperature, the effect of temperature at both device and circuit levels needs to be addressed to estimate the robustness of Nanosheet FET towards thermal variations.

Furthermore, while adding more sheets in NSFET might enhance drive current in GAA devices, but taller fin devices complicate the manufacturing process and add parasitic capacitances. Also, despite having greater gate electrostatic control, GAA FETs must minimize the channel width per layout footprint (W_{eff}/FP) while scaling. So, to obtain enhanced performance under the same FP, the different device engineering techniques, like structural engineering along with high-k gate stack, need to be explored on Nanosheet FET to further optimize the performance. Also, it is highly essential to study circuit behaviour in high-frequency applications with optimized Nanosheet FET by incorporating various device engineering at the device level.

1.7 Novelty of Overall Proposed Work

1. The geometry of the nanosheet plays a crucial role on the performance of the device. It is highly essential to address the impact of geometry and process parameters on Nanosheet FET (NSFET). Thus, GAA Nanosheet FET, according to the N5 [65] criteria, is designed and analysed its performance variations towards varied geometrical and process parameters.

2. Further, Analysis of analog/RF performance of the device is essential to estimate the device's suitability for analog/RF circuit applications. Also, the impact of geometry in high frequency circuit applications needs to be explored. To address the gap in the existing literature, which

mainly focuses on device level analysis, the circuit-level performance analysis of GAA nanosheet FET is carried out with varied geometrical parameters.

3. Moreover, semiconductor devices are sensitive to variations in temperature. The impact of temperature on the multigate FETs is addressed by some researchers. However, none has addressed the impact of temperature on NSFET in high frequency circuit applications. Thus, the impact of temperature on nanosheet FET for CMOS circuit applications is demonstrated at elevated temperatures.

4. To continue the scaling of NSFETs, the effective area (W_{eff}) per footprint (FP) (W_{eff}/FP), needs to be reduced, which affects the performance of the device with scaling. Thus, there is a need to improve the device's on current without increasing the FP by using device engineering such as structural engineering and high-k gate stack engineering. To increase the W_{eff} under the same FP, the CombFET is designed by combining Fin-like interbridge with nanosheets. Moreover, the performance is compared for both CombFET and NSFET devices for CMOS Circuit Applications.

1.8 Device Simulation

The 3-D Cogenda Visual Technology Computer Aided Design (TCAD) device simulator [55] is utilised in this thesis study to generate and simulate various device architectures. The TCAD are used in VLSI technology to model the electrical, thermal, optical, and electronic aspects of semiconductor devices.

These simulations are quite useful for figuring out how the device functions by solving physics-based equations. Particularly, simulators are a group of TCAD tools. It helps process and device engineers to comprehend semiconductor devices' manufacturing and reliability. It supports 2-D and 3-D simulation flows, as well as a variety of materials, including silicon and III-V compound semiconductor devices. Industries are constrained by time and financial constraints. Therefore, producers must create new process nodes quickly. Because of this, simulation tools make it easier to design process flows and optimise devices before wafer processing and manufacture. Without having to construct the devices, the physics, operation, and performance of the device may be immediately investigated using TCAD tools, thus saving time and money during the research and development process.

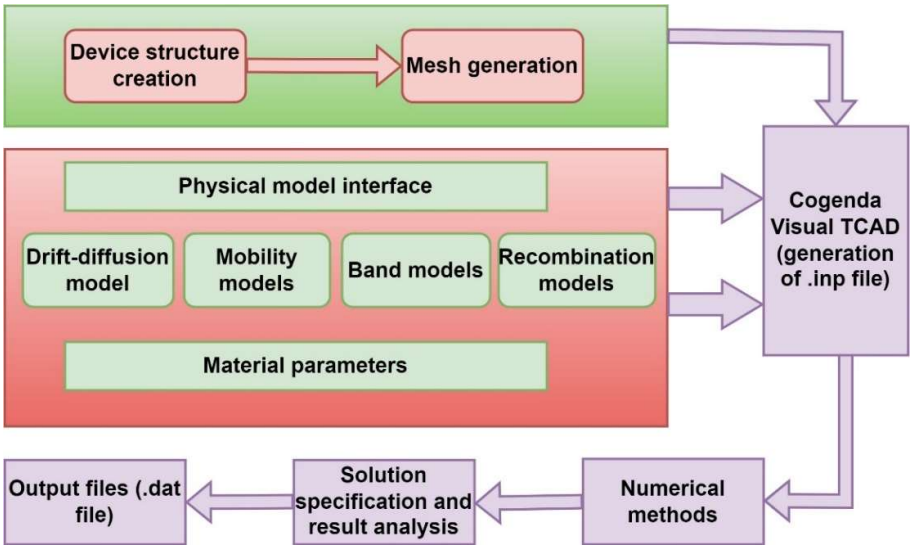


Fig. 1.16: Simulation process from device generation to outputs extraction.

The fully coupled Poisson and continuity equations are systematically solved by the Cogenda Visual TCAD device simulator to determine the various physical quantities required to undertake DC, AC, and transient analysis on the semiconductor device under consideration. The scheme command file is used to send all structural parameters, including dimensions, doping, and others, into the simulator, as illustrated in Fig.1.16. Without needing to manufacture the device, these simulation techniques can be used to estimate the device's realistic performance and the impact of process variation. These simulation tools significantly reduced the cost of designing, increasing the efficiency and speed of the production process. In order to effectively estimate the performance of the device, appropriate physical models must be included.

1.9 Workflow

The workflow of overall research is depicted in Fig. 1.17. Initially, the GAA nanosheet FET is designed in Visual TCAD and calibrated the device physics with experimental data. The calibrated physics is incorporated into the device physics to carryout the subsequent device simulations. For all the analysis, the Silicon (Si) material is considered. For circuit level analysis, lookup table based Verilog-A model is used to generate the symbols of the device and circuit simulations are performed in the Cadence tool. The contributions (C1-C4) are given in Fig. 1.17.

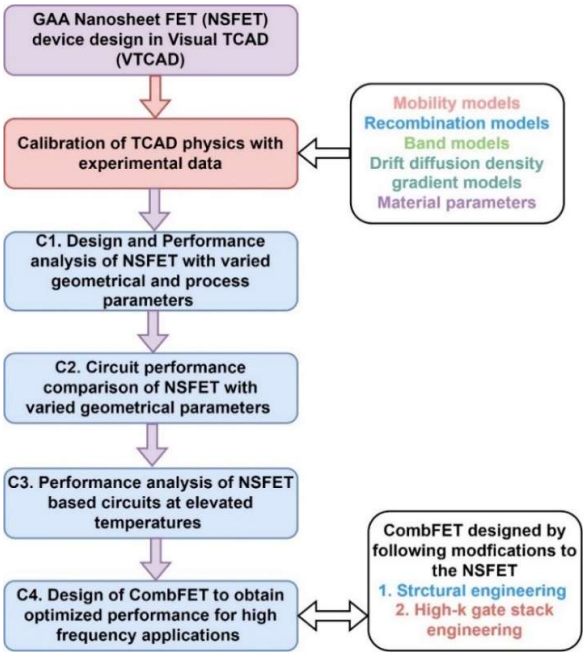


Fig. 1.17: Workflow along with contributions (C1-C4).

1.10 Research Specifications

The specifications of the research are as follows:

a. All the device design and simulations are carried out using 3-D Cogenda Visual Technology Computer Aided Design (TCAD) device simulator [55].

b. The device is designed according to IRDS standards [65], [134]. The parameters are listed below.

   1. Length of the gate - 16 nm
   2. Source/Drain doping (cm^{-3}) - 10^{20} (cm^{-3})
   3. Doping of the channel (cm^{-3}) - 10^{15} (cm^{-3})
   4. EOT (T_{SiO2} +($\varepsilon_{SiO2}/\varepsilon_{HfO2}$) ×$T_{HfO2}$) - 0.78 nm
   5. Length of Drain/Source (nm) - 12 nm
   6. Height of the gate - 60 nm

c. For all the circuit simulations are carried out in Cadence tool [120] through lookup table based Verilog - A models.

1.11 Research Objectives

The objectives of the research are as follows:

1. To design and analyze the performance variations of GAA Nanosheet FET with Varied Geometrical and Process Parameters at 5-nm technology node.

2. To analyze the circuit-level performance of GAA Nanosheet FET with varied geometrical parameters.

3. To evaluate the robustness of Nanosheet FET based circuits at elevated temperatures as the nanoscale devices' behaviour is very sensitive to temperature fluctuations.

4. To optimize the Nanosheet FET using both structural engineering with high-k gate stack to obtain better performance parameters like on current (I_{ON}), ON/OFF current ratio (I_{ON}/I_{OFF}) and performance assessment of optimized Nanosheet FET in high frequency integrated circuit applications like ring oscillator to get high frequency of oscillations (f_{OSC}).

1.12 Thesis Organization

The thesis presents the Design and Analysis of Modified GAA Nanosheet FET Based Circuits for High Frequency Applications. The thesis is organized into seven chapters. The following section gives a summary of the chapters.

Chapter 1: Presents an introduction to the work, motivation, and problem statement.

Chapter 2: Explores a literature overview of the present state-of-the-art on device engineering such as structural engineering, high-k gate stack, and performance analysis of NSFET and circuit applications. This chapter concludes with a brief outline of the thesis.

Chapter 3: Design and performance evaluation of NSFET with varied geometrical and process parameters.

Chapter 4: Device and circuit-level performance comparison of GAA nanosheet FET with varied geometrical parameters.

Chapter 5: Temperature assessment of nanosheet FET for CMOS circuit applications.

Chapter 6: A comprehensive analysis and performance comparison of CombFET and NSFET for CMOS Circuit Applications

Chapter 7: Conclusion and future scope.

Chapter 2

Literature Review

2.1 Literature Survey

As the MOSFET's size shrinks, SCEs have become more prominent in CMOS circuits. Many researchers have explored new technologies to circumvent the SCEs and fabrication related issues. Various approaches, such as multigate architectures [56], gate stack engineering [57], bottom spacer [58], strain engineering [59], dielectric pockets [60], and gate engineering [61], have been employed to address these SCEs. In this chapter, various multigate devices and different device engineering techniques are studied as part of the literature survey. Moreover, a comparison table is included, which provides various details of emerging multigate devices.

Kaushik Roy et al. [62] give various transistor intrinsic leakage mechanisms, including weak inversion, drain-induced barrier lowering, gate-induced drain leakage, and gate oxide tunneling. Channel engineering techniques, including retrograde well and halo doping, to manage SCEs for continuous scaling of CMOS devices. As changing the doping profile in the channel region, the distribution of the electric field and potential contours can be altered, and this results in the decrease of off-state leakage while an increase of linear and saturated drive currents. For digital applications, the most undesirable SCE is the reduced gate threshold voltage at which the device turns on, especially at high drain voltages. Circuit design techniques, namely transistor stacking, multiple and dynamic V_{DD} and, supply voltage scaling, threshold voltage scaling, can be done for leakage reduction in digital circuits.

S. K. Mohapatra *et al.* [63] have proposed the process parameters like H_{fin}, W_{fin}, and aspect ratio (AR = W_{Fin}/H_{fin}) are designed towards various architectures like FinFET, trigate, and planar MOSFET that meets the needs of high performance (HP) or low standby power (LSTP) applications. From the results analysis, taller fins are capable of higher current drivability, and thinner fins are capable of reducing SCEs. Moreover, the comparison of planar MOSFETs, trigate and FinFET has been made. The comparison shows trigate gives better performance in terms of delays due to higher I_{eff}. However, power dissipation and cut-off frequency are better for planar MOSFETs and FinFETs. According to the result analysis, larger fins are necessary for higher current drivability, whereas narrower fins are required for higher SCE immunization.

FinFETs can be freed from substrate-related effects by thinning the W_{Fin}, which increases the device A_V, V_{EA}, and R_o.

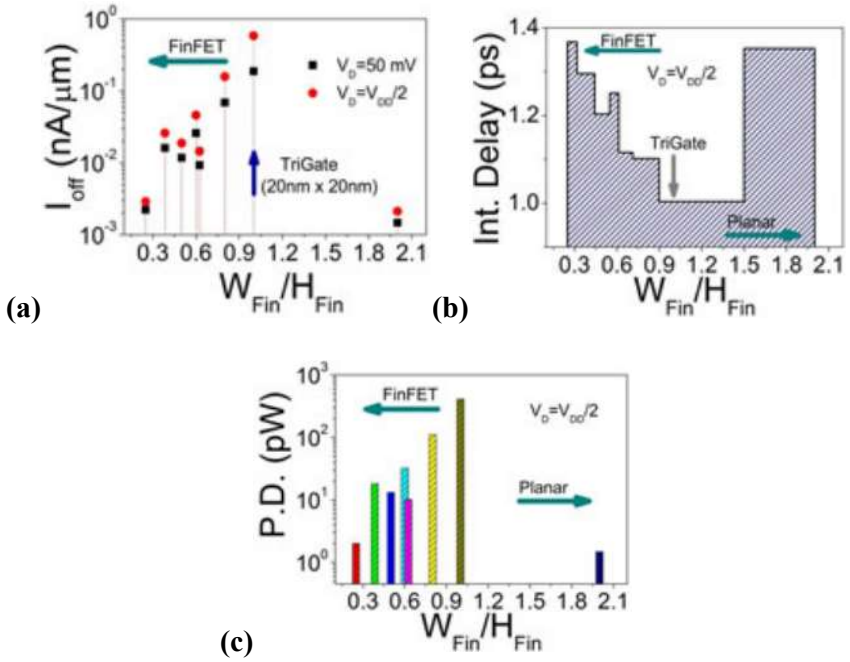


Fig. 2.1: (a) OFF state leakage current (b) Intrinsic delay and (c) Power dissipation.

D. Nagy et al. [51] stated that for gate lengths (L_G) of below 16 nm, the NS FET is a potential candidate to replace the existing FinFET technology as it provides a higher ON current compared to the FinFET. The comparison reveals that nanosheet FET is a feasible alternative for the FinFET in high performance (HP) applications, giving a larger on-current (I_{ON}) and somewhat superior sub-threshold property. Moreover, it is found that the GAA NW and NSFETs offer slightly better subthreshold performance compared to the FinFET devices. For L_G less than 16 nm, NW FET offers near ideal subthreshold swing, lowest off current and higher switching ratio (I_{ON}/I_{OFF}), thereby enhancing the performance. However, the NW FET suffers from early saturation of drain current owing to the surface roughness factor. As a result, the NS FET has proven to be capable of scaling for sub-5-nm nodes.

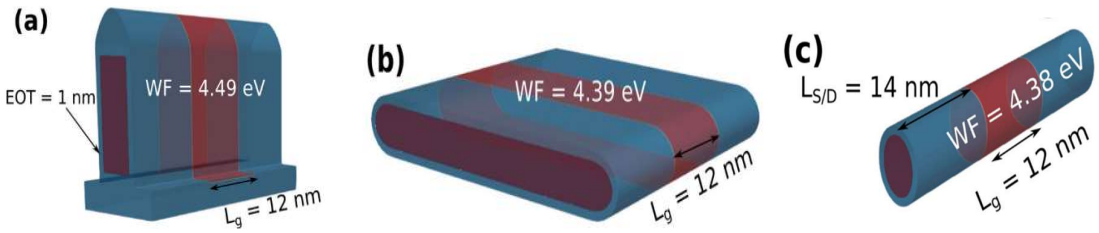


Fig. 2.2: Device structures of (a) FinFET, (b) GAA NSFET and (c) GAA NWFET.

For the first time, Loubet et al. [64] demonstrated that horizontally stacked gate-all-around (GAA) Nanosheet structure is a good candidate for the replacement of FinFET at the 5nm technology node and beyond. Horizontally stacked gate-all-around (GAA) Nanosheet offers increased effective width (W_{eff}) per active footprint and better performance compared to FinFET. Moreover, the frequency analysis of the device is presented at different widths of NS. According to the analysis, good electrostatics are reported at L_G of 12 nm for GAA Nanosheet FETs.

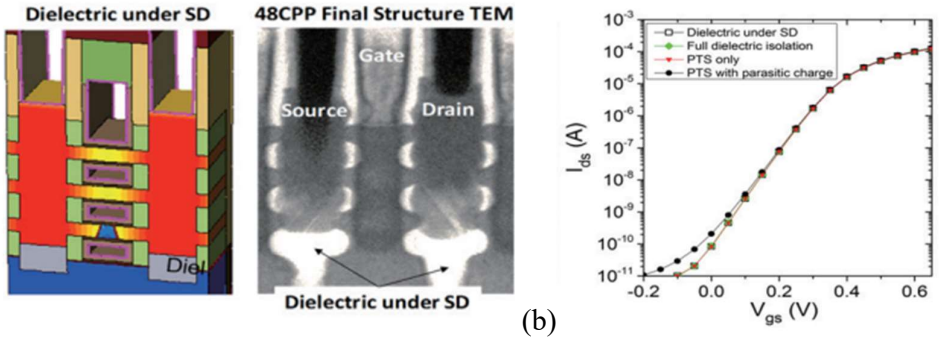


Fig. 2.3: Device structures of (a) NSFET and its TEM image (b) transfer characteristics of NSFET.

Vinay et al. [65] presented the performance comparison of bulk CMOS FinFET, GAA Nanowire and Nanosheet structures at 5-nm technology node. The analysis of subthreshold characteristics and various SCEs is carried out at different gate lengths. From the simulated results, it is proven that the GAA structures offer superior performance. Moreover, the SRAM analysis presented and concluded that the GAA FETs offer 40% improvement compared to FinFETs.

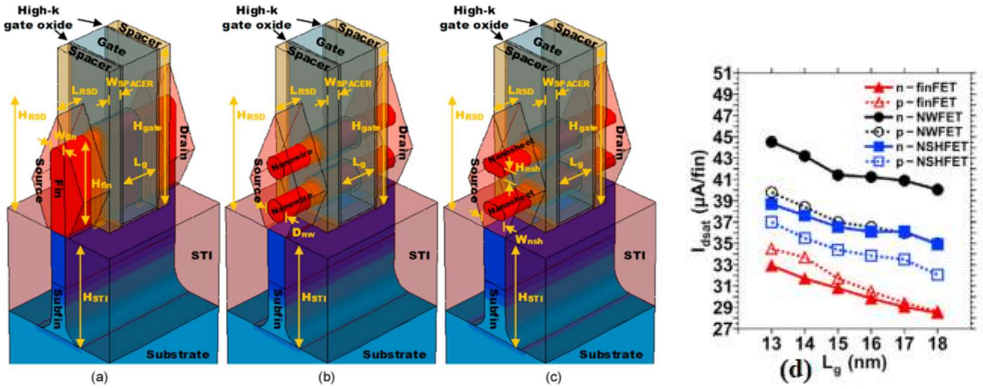


Fig. 2.4: Simulated structures of (a) FinFET (b) GAA NSFET (c) GAA NWFET (d) drain current (I_{dsat}).

Hsin-Cheng Lin et al. [66] reported the analog performance of stacked Nanosheets by using 3-D TCAD simulations. By considering the same array layout, it is shown that the Nanosheet FET can offer higher transconductance and lower capacitance than FinFET. Also, by using the optimized Nanosheet FET with an EOT of 0.8 nm, the authors were able to obtain the cut-off frequency and maximum oscillation frequencies of 340 GHz and 370 GHz, respectively. Also, it is demonstrated that compared to FinFETs, Nanosheet FETs can offer superior RF performance. Thus, the Nanosheet FETs are appropriate for 6G wireless communications.

Chi-Woo Lee et al. [54] investigated the junctionless (JL) Nanowire FET performance at elevated temperatures. Also, the comparison was made with accumulation and conventional doping to analyse the performance. It is noted that the JL NW FET exhibits the highest threshold voltage variations with temperature. Moreover, the mobility deteriorated with conventional NW FET owing to the various scattering mechanisms. However, the JL NW FET offers an increment in current with the rise in temperature owing to the less mobility degradation with temperature.

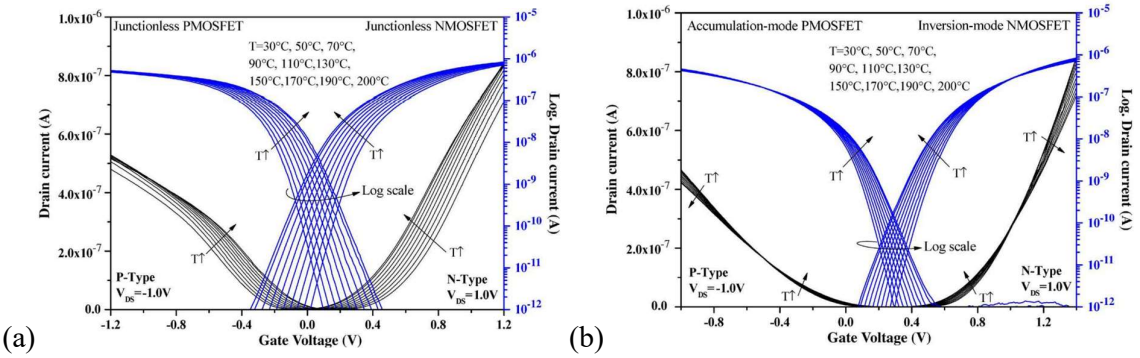


Fig. 2.5: Simulated I_D-V_{GS} characteristics of NW FET with (a) JL mode (b) accumulation and inversion mode at elevated temperatures.

Rajesh Saha et al. [67] investigated the performance of dual material gate (DMG) FinFET at various temperatures. The DC, analog/RF performance is discussed in detail with temperature. The DC metrics such as on current, off current, SS and DIBL are investigated. Moreover, the analog/RF figures of merit (FOMs), such as cut-off frequency (f_T), gain frequency product (GFP), intrinsic gain and so on, are analysed with variations in temperature. Further, the impact of temperature on the linearity of the device is discussed. It is noted that at high temperatures, the f_T tends to degrade, which hinders the device's speed. However, a remarkable performance enhancement is obtained with an increment in temperature. Thus, the device's electrical performance tends to degrade with the rise in temperature.

Anil Kumar Gundu et al. [68] discussed the computational analysis of GAA stacked nanosheet devices. In this paper, the device design guidelines are given for low-power applications at 5-nm node and beyond. The 3-D stacked nanosheet devices offer lower values of SS, DIBL, and subthreshold leakage current. It is shown that 3-D stacked nanosheets can reduce the SS, DIBL and leakage currents. Also, it is proved that in comparison to SOI FinFET technology, the GAA nanosheet can offer higher inverter gain along with better noise margins. Moreover, by increasing the supply voltage, compared to FinFET, the nanosheet FET can reduce energy consumption.

Vishal et al. [69] demonstrated the performance of a common source amplifier circuit which is implemented using rectangular core-shell double gate junctionless transistor (RCS-DGJLT). Further, the author presented the process from device to circuit level simulations in detail in this paper. The analysis of RCS-DGJLT is carried out and the same compared with DGJLT. The simulation results show that the RCS-DGJLT structure is capable of high frequency circuits on of CMOS inverter.

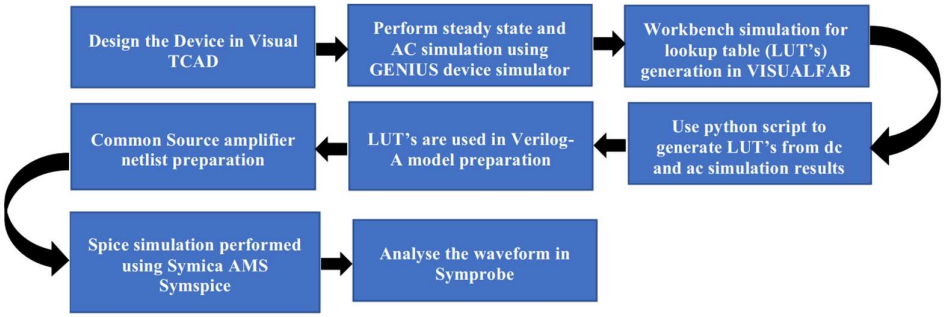


Fig. 2.6: Flowchart of the process followed to design the circuit using look up table-based Verilog-A model.

Baral et al. [70] analysed the effect of ion implantation on the performance of cylindrical gate (CG) junctionless accumulation mode (JAM) MOSFET. Further, an inverter is designed using lookup table-based Verilog-A model using Cadence simulator. Also, the calibration of the Verilog-A model with TCAD is performed and presented. Further, the 6 T SRAM is implemented, and its performance is demonstrated with the proposed CG-JAM MOSFET.

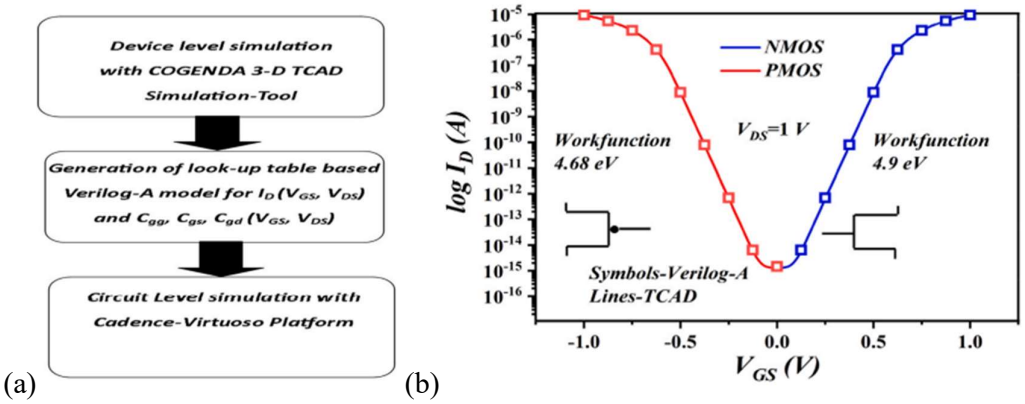


Fig. 2.7: (a) Process flow from TCAD to circuit simulations and (b) Verilog-A model calibration with TCAD.

Genaro Mariniello *et al.* [71] have discussed the fundamental analog figures of merit of n-type vertically stacked nanowires with variable fin width, and channel length, including transconductance, output conductance, transconductance over drain current ratio, intrinsic voltage gain, and harmonic distortion (or non-linearity). The basic electrical properties of the investigated transistors, such as threshold voltage, subthreshold slope, and low field electron mobility, were also studied to provide a physical understanding of the results. According to the findings, short-channel effects had a minor impact on all 2-channel stacked nanowires. The maximum voltage gain was achieved for the smaller channel width and longer channel length dimensions. The results reveal that narrower and longer stacked nanowire devices have better distortion qualities, with a prevalence of second harmonic distortion.

Biswajit Jena et al. [72] investigated the performance of emerging CMOS nanowire FET for low power applications. Also, the paper presents the numerical analysis of cylindrical NW FET with work function modulation. Further, the circuit level simulations were carried out for CMOS inverter using the proposed device. Various inverter performance metrics, such as switching current, noise margins (NM), DC response, average propagation delay and transient response, are discussed in detail. It is shown that the proposed device can offer sharp transitions, high speed along with superior NM. Thus, it is shown that cylindrical gate FET is capable of driving high speed logic applications.

Wen-Li Sung et al. [73] reported the performance of stacked Nanosheets with and without using the metal side wall (MSW) contacts for source and drain. Also, the comparison is presented at both device and circuit levels. It is shown that as the channel number increases, the Nanosheet FET without MSW performance degrades. However, in the same case, the performance can be

enhanced by incorporating the MSW contacts as it provides uniform distribution of electric potential. Moreover, the digital CMOS inverter and ring oscillator (RO) performance is analysed and compared with and without using the MSW contacts. For the six-channel Nanosheet FET, the oscillation frequency of 3-stage RO was enhanced by 57% by utilizing the MSW contacts.

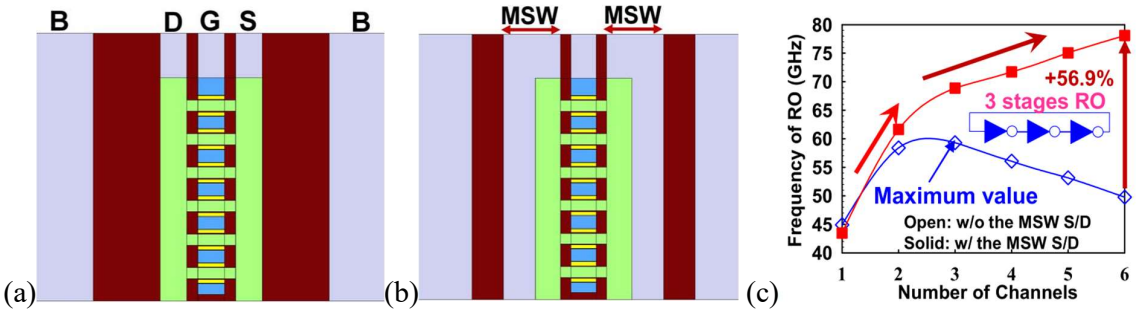


Fig. 2.8: Nanosheet FET (a) without MSW contact (b) with MSW contact and (c) variations in the frequency of oscillations as a function of the number of channels.

K. P. Pradhan et al. [74] studied the impact of high-*k* gate stack on the performance of DG MOSFET by considering various high-*k* gate dielectric materials along with SiO_2 in the gate stack. The analog/RF performance is compared and presented at various effective oxide thickness (EOT) values. It is shown that by incorporating high-*k* gate stack, the crucial DC metrics like SS and DIBL are improved owing to the enhanced gate electrostatic integrity. Morevoer, the analog/RF analysis tell that high-*k* gate stack is a better option to use the device in analog/RF circuit applications.

For the first time, Xinhao Li et al. [75] proposed and numerically assessed a novel comb-like-channel field-effect transistor (CombFET). The device can be realized by combining the fin like interbridge with the nanosheet structure in the channel area. The fabrication process of CombFET is compatible with that of the FinFET process and offers process flexibility. By using the side wall selective epitaxy of the channel, the CombFETs are realized. The simulation outcomes demonstrate that using CombFET on current improved by 53% compared to gate-all-around FET (GAAFET) under the same footprint. This enhancement is achieved owing to the large effective area offered by CombFET.

Refer-ence	Device	L_G (nm)	I_{ON}	I_{OFF}	I_{ON}/I_{OFF}	SS (mV /dec)	DIBL (mV/V)
[53]	NS FET	10	85 µA	7.08 nA	1.2×10^4	80	100
[68]	FinFET	5	392.57 µA/µm	20.48 nA/µm	$1.9x10^4$	112	73
	1 sheet Nanosheet FET	5	421.13 µA/µm	8.72 nA/µm	$4.8x10^4$	98	64
	2 sheet Nanosheet FET	5	324.98 µA/µm	6.41 nA/µm	$5.1x10^4$	97	57
	3 sheet Nanosheet FET	5	299.41 µA/µm	4.26 nA/µm	$7.0x10^4$	94	50
[72]	Cylindrical NW	35	7.6×10^{-5} A	2.37×10^{-12} A	3.2×10^7	62	37
[73]	NS FET	12	200 µA	150×10^{-12} A		68.5	61
[76]	GAA NW FET	35	3.8×10^{-5} A	15×10^{-12} A	2.5×10^6	65	85
[77]	NW FET	35	3.6×10^{-5} A	20×10^{-12} A	1.3×10^6	67.5	50
[78]	Trigate	1000	0.9×10^{-5} A	1.2×10^{-12} A	7.5×10^6	187	27
	NS FET	1000	1×10^{-5} A	5×10^{-14} A	2×10^8	100	0.13
[79]	NW FET	350	1×10^{-5} A	$\sim 1 \times 10^{-12}$ A	$> 10^7$	99	15.22
[80]	NS FET	12	144 µA/µm	-	-	64.6	20.6
	NS FET	12	147 µA/µm	-	-	64.6	20.7
	NS FET	12	179 µA/µm	-	-	64.4	31.4
[81]	NS FET	80	1×10^{-7} A	1×10^{-14} A	10^7	68	-
[82]	NW FET	10	105 µA	10nA	1.05×10^4	74	80
[83]	Rectangular NW FET	100	840 µA/µm	4 nA/µm	2.1×10^5	64	32
[84]	Trigate JL ACC FET	26	$\sim 10^{-3}$A/µm	$\sim 10^{-9}$A/µm	$\sim 10^6$	-	~90
[85]	JL GAA MOSFET	50	$\sim 10^{-6}$A	$\sim 10^{-15}$A	$\sim 10^9$	-	~46
[86]	JL NW FET	40	$\sim 10^{-6}$A	$\sim 10^{-15}$A	$\sim 10^9$	~70	~48
[87]	Core-shell NW	20	$\sim 10^{-5}$A	$\sim 10^{-10}$A	$\sim 10^5$	-	-
[88]	JL MOSFET	20	$\sim 10^{-4}$ A/µm	$\sim 10^{-10}$ A/µm	$\sim 10^5$	~70	
[89]	Nanotube JL FET	7	$\sim 10^{-6}$ A/µm	$\sim 10^{-13}$ A/µm	$\sim 10^7$	-	-

Table. 2.1 Comparison of performance of Multigate FETs reported in the literature.

2.3 Research Gaps Identified

1. When the channel length is very less (L_G<20 nm), the short channel effects (SCEs) hinder the transistor's performance. However, to manifest Moore's law, the downscaling of the transistor is inevitable. Thus, there is a need to look for solutions in such a way that the device's performance should not deteriorate by scaling. Though the FinFET technology replaced the conventional MOSFET for sub-22-nm technology nodes, the fabrication issues raised to scale the FinFETs for sub-7-nm nodes. As a result, to enhance the device's performance, the GAA technology is suggested.

2. In GAA FETs, the gate covers the channel in all directions so that the electrostatic integrity of the gate increases. More number of nanosheets can be stacked vertically to enhance the drive current. However, as the number of nanosheets increases, the parasitic capacitances also increase, which increases the delay of the device. Thus, it is highly essential to analyse the performance at different geometry of the nanosheet. Though some works addressed the geometrical impact at the device level, none has addressed the geometry impact at high frequency circuit applications.

3. The semiconductor devices are very much sensitive to variations in temperature. The impact of temperature on the multigate FETs is addressed by some researchers. However, none has addressed the impact of temperature on NSFET in high frequency circuit applications.

4. To continue the scaling, the effective area (W_{eff}) per footprint (FP) (W_{eff}/FP), needs to be reduced, which affects the performance of the device with scaling. Thus, there is a need to improve the device's on current without increasing the FP by using device engineering such as structural engineering and high-k gate stack engineering.

2.3 Conclusion

It is clear from the literature survey that multigate FETs are predominant in reducing SCEs effectively and ensuring fundamental scaling. Moreover, the GAA Nanosheet FETs offer enhanced performance and are suitable for low power and high performance applications. The studied literature shows the path for finding research problems for continued scaling with minimized SCEs.

Chapter 3

Performance Evaluation of GAA Nanosheet FET with Varied Geometrical and Process Parameters

3.1 Introduction

Multiple gate devices, including as double gate (DG), trigate (TG), and quadruple gate (GAA) architectures, have evolved to continue scaling for sub-10-nm domains, as was described in section 1.5. Compared to conventional MOSFETs, the DG MOSFET's performance is enhanced owing to the increment in the gate's electrostatic integrity. DG MOSFETs contain two gates, in which gates are present at the bottom and top of the device. By maintaining the two gates, the channel's electrostatic integrity increases and offers better short channel performance. However, in double gate MOSFETs, the misalignment problem of the top gate and bottom gate is present, which causes degradation in on current [90]. To combat these problems associated with conventional MOSFET and DG MOSFET with scaling, alternative structures such as trigate FET and FinFETs are explored. In trigate and FinFET devices, the gates surround the channel in the left, top and right directions and are possible candidates to replace the orthodox MOSFETs in the semiconductor industry. Moreover, FinFET structures are more immune to SCEs and offer fewer DIBL and SS values for sub-22-nm technology nodes. The semiconductor companies like TSMC and INTEL have adopted FinFETs into their significant portion of IC fabrication since 2011.

However, for further scaling of FinFETs, taller and thinner fins are required to get more drive current, which increases the process complication of the device. Moreover, maintaining the taller fins on a narrow base may lead to fracture and malfunction of the circuit [64], [91], [92]. To circumvent these problems, researchers came up with the solution of GAA configurations. Since the channel in the GAA structure is controlled in all directions by the gate and hence improves the subthreshold performance. Nanosheet (NS) and nanowire (NW) are examples of GAA structures. On the other hand, it is reported that, due to the surface roughness factor, the nanowire performance deteriorated [93]. The GAA nanosheet structures are FinFET successors for sub-7-nm technology and beyond, and have emerged as viable challengers for traditional FinFETs since they offer greater control over the channel region. Robust leakage control and

strong current driving capacity are two advantages of nanosheet architectures. Due to the tight electrostatic control over the channel region, NSFETs are resistant to short channel effects. S. D Kim reported that NSFETs exhibited greater electrostatic performance on the channel compared to GAA nanowire and FinFET architectures [94], [95]. By making minimal changes to the fabrication flow of FinFET, NSFET can be fabricated. Also, it is shown that by using NSFETs instead of FinFETs, a 30% higher effective width (W_{eff}) can be produced on the same footprint. Another remarkable observation is that single stack nanosheets have been shown to have superior intrinsic performance than FinFETs or stacked nanowires for a given active width due to lower parasitic capacitance. In a given footprint, nanosheets offer a higher effective width making them good at driving capacitive loads [64], [96]. Moreover, nanosheet width doesn't affect by fin pitch which provides greater flexibility in maintaining appropriate W_{eff}. The usage of more stacked nanosheets to maximize the drive current is a better option, but the larger height of the device exacerbates parasitic capacitances [53].

So, in this chapter, the performance of two stack GAA NSFET at 5-nm technology node is analysed towards electrical performance. As the geometry of the device plays a crucial role in determining the device's performance, the nanosheet width and thickness are varied in addition to the gate length to observe the performance variations. On top of that, the temperature analyses in done to identify the temperature compensation point, which helps to get optimum performance of the device irrespective of temperature variations of the device. Moreover, the performance of the NSFET is assessed with variations in workfunction values.

3.2 Device Structure and Simulation Framework

The device structure of the NSFET is generated by using the Cogenda Genius 3D TCAD simulator [55]. The 3D NSFET with gate length (L_G) of 16 nm, each sheet thickness (N_T) of 5 nm, and sheet width (N_W) of 10 nm is generated and simulated. The n-type source/drain and p-type channel regions are doped with a doping concentration of 10^{20} cm^{-3} and 10^{15} $cm^{-3,}$ respectively. For a high-*k* gate stack, to get an effective oxide thickness (EOT) of 0.78 nm, thickness values of 0.5 nm and 1.5 nm are considered for SiO_2 and $HfO_{2,}$ respectively. To ensure better electrostatic integrity, the EOT of 0.78 nm and gate work function of 4.6 eV are taken for all simulations. As the continuous scaling of the device leads to abnormal SCEs, spacers are incorporated to improve the short channel performance of the device. However, the drive current is degraded due to an increase in series resistance in the underlap sections. By using high-*k* spacers in the underlap area, series resistance can be lowered and the drive current can

be increased. Various high-*k* materials like Si_3N_4 and HfO_2 are explored in the literature, and is reported that by using Si_3N_4 spacer, the static power consumption is reduced compared to other spacer materials [97]. Moreover, the idealized geometries such as sharp interfaces, perfect crystal structures, perfect planar layers are assumed. To improve the sub threshold behaviour, a nitride spacer with a length of 5 nm is maintained throughout the simulations [98].

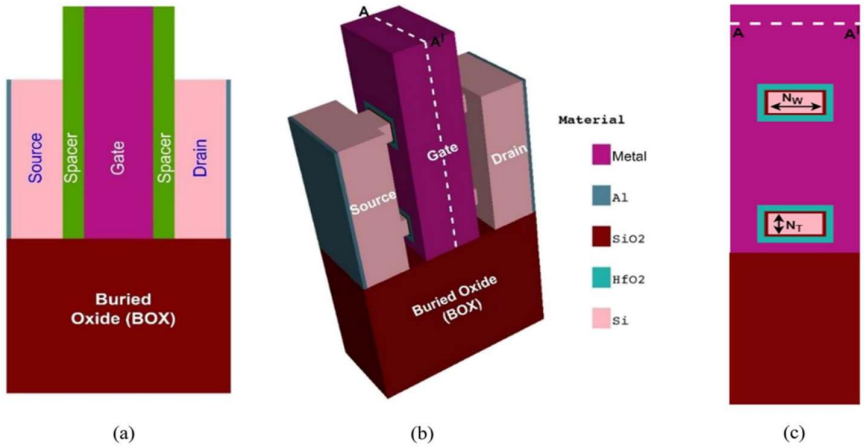


Fig. 3.1: (a) 2-D view of NSFET with nitride spacer, (b) 3-D schematic view of NSFET and (c) 2-D cross sectional view of NSFET.

Figure 3.1(a) depicts the 2-D NSFET with Nitride spacer. The 3-D view of NSFET with stacked nanosheets is shown in Fig. 3.1(b). 2-D view of NSFET with N_T and N_W is depicted in Fig. 3.1(c). The device is well calibrated using [27, 33], and the I_D-V_{GS} characteristics are depicted in Fig. 2. The physical models incorporated for simulation are considered from [50] and are as follows. Schenk's bandgap narrowing model is used to account for narrow bandgap effects caused by larger doping levels. The Shockley-Read-Hall (SRH) recombination method is used to assess the consequences of carrier generation and recombination.

The Lombardi mobility model is used to account for scattering phenomena such as surface roughness. The thin layer mobility model, which deals with mobility degradation at the semiconductor-insulator interface, is also used. For high field mobility effects, the Lucent model is considered. Since the device considered has low effective channel length, carriers are supposed to be vertically limited because of thin channel thickness. Therefore, in simulations, quantum effects are considered by the density gradient into account. Quantum confinement effects are included in the density gradient method by incorporating the quantum mechanical behavior of electrons in nanoscale materials. This is done by solving the Schrödinger equation

self-consistently with the Poisson equation. The Selberherr impact ionization model is used to calculate the electron-hole pair's generation rate. Also, field dependence mobility model parameter, i.e., saturation velocity (V_{sat}) is adjusted to 1.5×10^7 cm/s for achieving a better matching [50]. The models used for simulations are calibrated with experimental results, and the transfer characteristics are presented in Fig. 3.2. Table. 3.1 provides the values of device parameters included in the simulation.

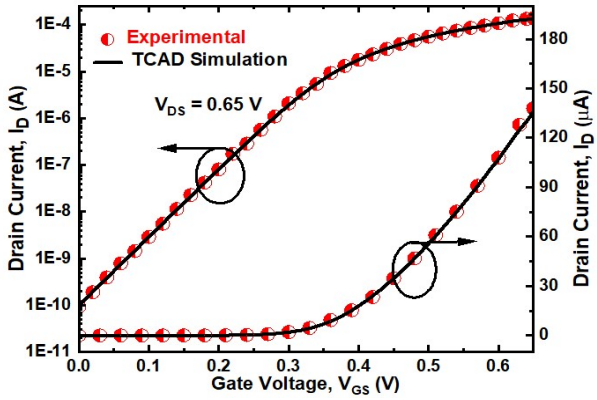


Fig. 3.2: Calibration of simulation models with that of experimental results [64].

Device Parameter	Value
Nanosheet thickness (nm)	5-9
Nanosheet width (nm)	10-50
Gate length (nm)	5 - 20
Source/Drain doping (cm^{-3})	10^{20}
Channel doping (cm^{-3})	10^{15}
EOT (nm)	0.78
Spacer dielectric	Nitride
Source/Drain length (nm)	12
Underlap spacer length (nm)	5
Workfunction of the gate (eV)	4.3 - 4.7
Height of the gate (nm)	60

Table 3.1: Device parameters used in the simulation.

3.3 Results and Conclusions

3.3.1 Impact on DC Performance of NSFET with Geometric Variations

The DC performance of NSFET is analysed by changing the NS physical dimensions like width (N_W) and thickness (N_T). The N_W varied from 10 nm to 50 nm, and N_T varied from 5 nm to 9 nm. In this section, the key performance parameters like on current, off current, switching ratio, threshold voltage (V_{th}), DIBL, and SS are discussed.

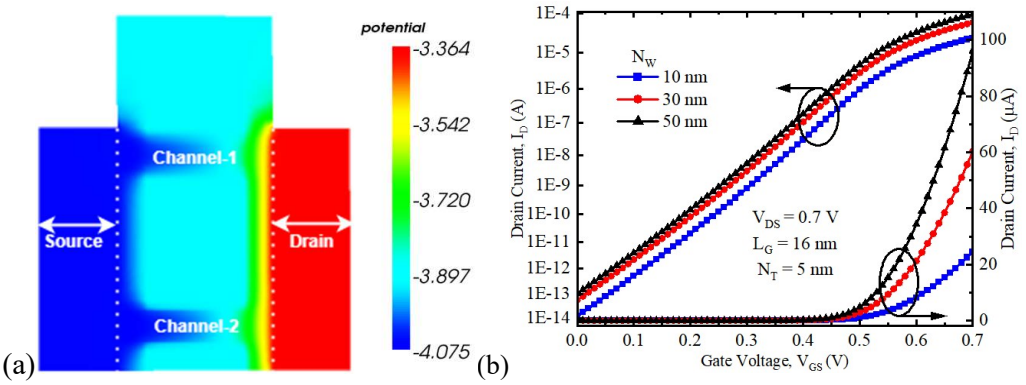


Fig. 3.3: (a) Contour plot of the potential distribution of NSFET in ON state (b) Transfer characteristics of NSFET in linear and log scale for V_{DS} = 0.7 V.

The Contour plot of the potential distribution of NSFET is shown in Fig. 3.3(a). It can be observed that the potential distribution at the drain side is high compared to the source side. Also, it can be clearly seen that the drain potential impact on the channel is reduced because of the spacer. Fig. 3.3(b) depicts transfer characteristics in both linear and log scales for various widths of nanosheet at V_{DS} = 0.7 V for a constant N_T of 5 nm.

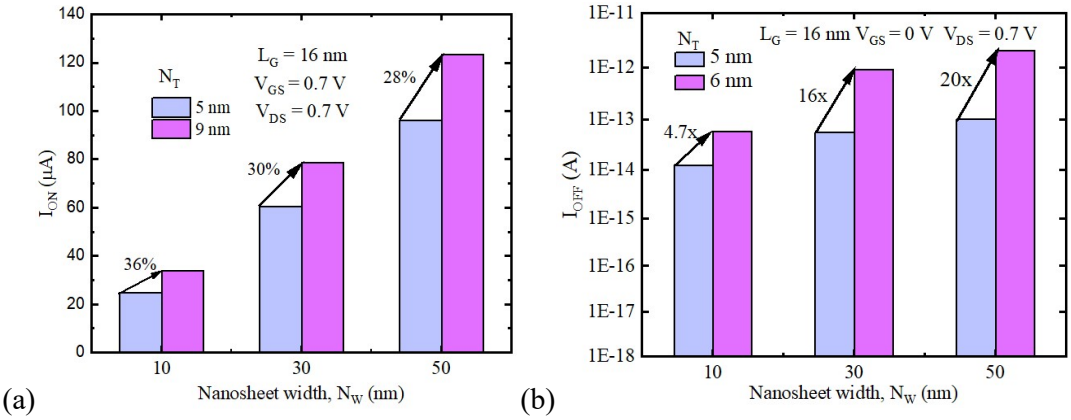
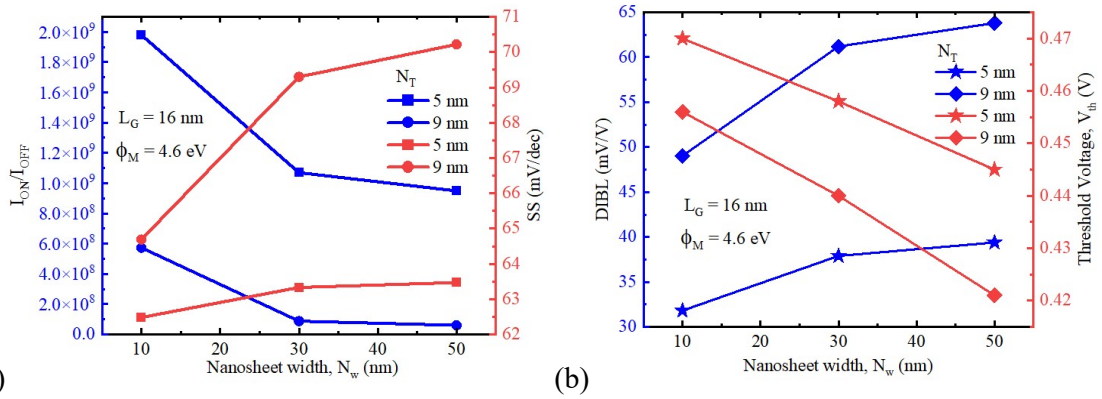


Fig. 3.4: (a) I_{ON} and (b) I_{OFF} as a function of N_W for various N_T values.

Channel width controls the amount of flow of current through the NSFET. The I_{ON} is directly proportional to the effective width of the channel, which leads to an increment in the I_{ON} as the width of the sheet increases. From Fig. 3.4(a), it can be seen that the maximum increment of 36% in I_{ON} is observed when the thickness is increased from 5 nm to 9 nm at nanosheet width of 10 nm. It is observed that for larger widths of nanosheet, higher I_{ON} is obtained due to the increment of effective width of the nanosheet. On the other hand, in addition to the increment in I_{ON}, the increment in the I_{OFF} also observed. As the width of the channel increases, the gate loses its control on the channel and leads to more leakages in the device. These leakages will increase the I_{OFF} of the device. Moreover, the increment in I_{OFF} is observed for higher thickness values of nanosheet because of the reduction in potential barrier height, and conduction band energy in the channel for off state condition [50]. For thinner nanosheets off state current can be reduced, however, a slight reduction in the I_{ON} is observed because of the mobility degradation due to enhancement in the perpendicular electric field [50]. These results are shown in Fig 3.4(b). The maximum increment of 20× in off current is observed for thickness from 5 nm to 9 nm at a nanosheet width of 50 nm.



(a) (b)

Fig. 3.5:(a) I_{ON}/I_{OFF} and SS (b) DIBL and V_{th} as a function of N_W for various N_T values.

Fig. 3.5(a) shows I_{ON}/ I_{OFF} and SS values for different widths of nanosheet. As the N_W increases, the switching ratio followed decreasing manner because of the raise in off current. Moreover, as the width increases, there is a decrement of 71% and 94% in switching ratio is observed for thickness values of 5 nm and 9 nm, respectively. It can be observed that the switching performance of the device gets deteriorates with the increment in geometrical values.

Sub-threshold swing (SS) is an important metric for device application in logic circuits. The SS is defined as the change in the gate voltage needed to get a decade change in drain current. The Sub-threshold swing (SS) can be calculated by using equation 3.1 [99].

$$SS = \left(\frac{\partial log_{10} I_D}{\partial V_{GS}}\right)^{-1} \qquad (3.1)$$

From Fig. 3.5(a), it can be seen that for more width, SS followed an increasing manner since the gate loses its control over the channel. Furthermore, as the width varies from 10 nm to 50 nm, there is an increment of 1.6% and 8.5% in SS is observed for thickness values of 5 nm and 9 nm, respectively. Since a lower value of SS is preferred for good sub threshold performance, nanosheet having width and height of 10 nm and 5 nm respectively outperforms with SS of 62.5 mV/dec, which is near to ideal SS.

Fig. 3.5(b) depicts DIBL and V_{th} for different widths of nanosheet. The threshold voltage is extracted by using the constant current method at 100× W_{eff}/L_G. Where W_{eff} is given by n × (2× (N_T + N_W)), where N_T and N_W are the thickness and the width of the nanosheet respectively. The term n indicates the number of vertically stacked nanosheets [100]. As the thickness and width of the nanosheet are increasing, from Fig. 3.5(b), it can be seen that the threshold voltage is reducing because of SCEs. Furthermore, there is a threshold voltage roll-off of 5.3%, and 8% is observed for thickness values of 5 nm and 9 nm, respectively when the nanosheet width is varied from 10 nm to 50 nm. It can be seen that the V_{th} roll-off is more for higher thickness values of nanosheet.

Drain induced barrier lowering (DIBL) is also one of the crucial sub-threshold performance metrics, and it should be as low as possible for good performance of the device. The DIBL is computed by using equation 3.2 [101].

$$DIBL = \frac{V_{tlin} - V_{tsat}}{V_{Dsat} - V_{Dlin}} \qquad (3.2)$$

Here, V_{tlin} is the threshold voltage extracted at linear supply voltage, V_{Dlin} = 0.04 V and V_{tsat} is the threshold voltage extracted at saturation supply voltage, V_{Dsat} = 0.7 V. It can be observed that, as the nanosheet dimensions are increasing, the DIBL gets increasing. Moreover, as the N_W increased from 10 nm to 50 nm, there is an increment of 24% and 30% in DIBL observed for nanosheet thickness values of 5 nm and 9 nm, respectively. The DIBL can be lowered by incorporating the nanosheets which are having smaller widths and thickness values. The results show that DIBL is sensitive towards width and thickness variations.

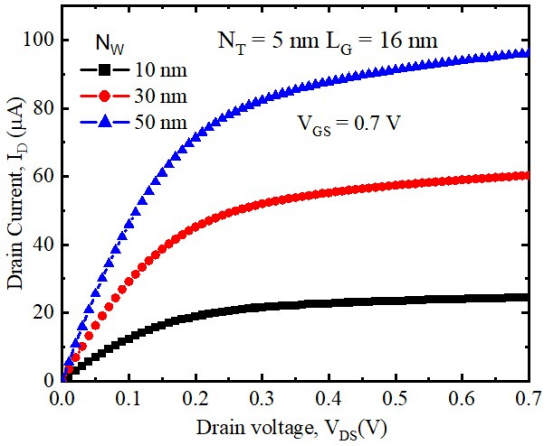


Fig. 3.6: Output characteristics for various N_W values as a function of drain voltage.

Fig. 3.6 shows the output characteristics for various Nanosheet width values with respect to drain voltage at a fixed gate voltage of 0.7 V. It is observed that as the N_W increases, the drain current increases due to the increment in effective width.

3.3.2 Impact on DC Performance of NSFET with Scaling

In this section, the impact of scaling on the DC performance of NSFET is analysed for sub -7-nm technology nodes. The gate length is downscaled from 20 nm to 5 nm, and the results are depicted in Fig. 3.7(a). The transfer characteristics are obtained by fixing the thickness to 5 nm and width to 10 nm for the nanosheet.

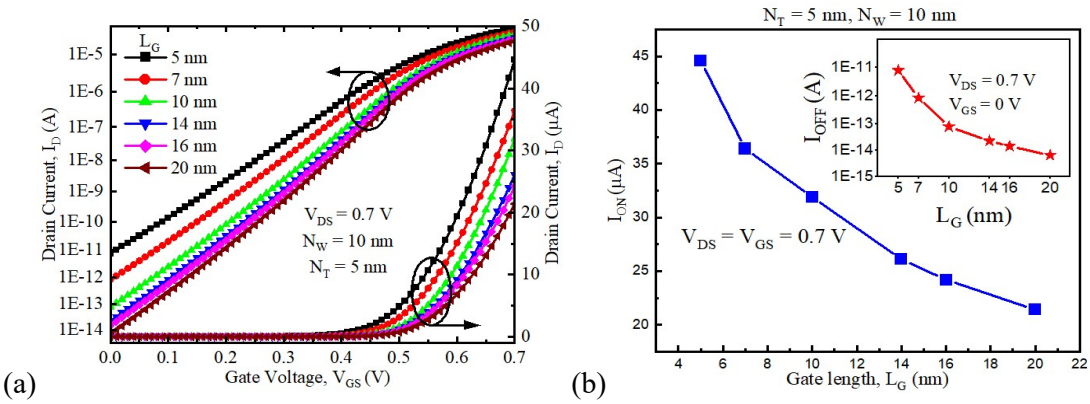


Fig. 3.7: (a) Transfer characteristics for various L_G values and (b) I_{ON} and I_{OFF} (inset) as a function of L_G.

From Fig. 3.7(b), it is observed that as the channel length decreases, the on current is increased since the distance between the source and drain is decreased. However, the off current also increased due to the SCEs.

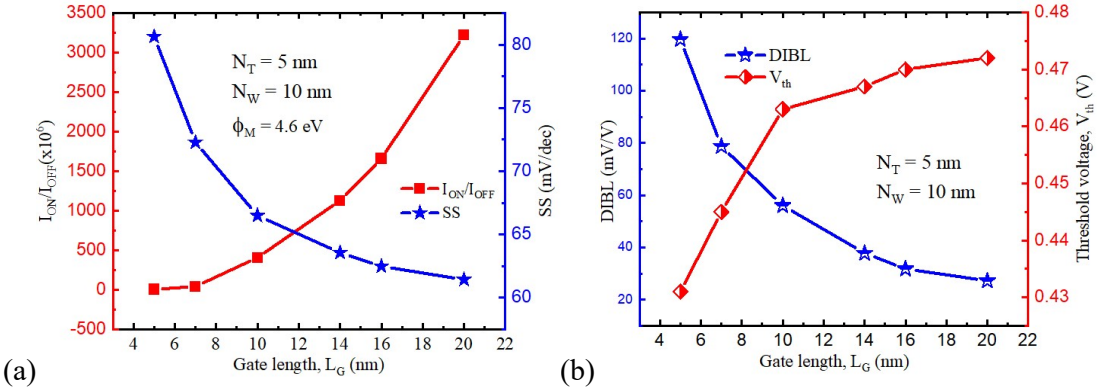


Fig. 3.8: (a) I_{ON}/I_{OFF} and SS (b) DIBL and V_{th} as a function of L_G.

Fig. 3.8(a) depicts the I_{ON}/I_{OFF} and SS as a function of the gate length. It can be seen that as the channel length is decreasing, the switching ratio has deteriorated. However, even at L_G of 5 nm, the switching ratio of 10^6 is maintained, which ensures that NSFET is a suitable candidate for good logic applications and continued scaling [53], [102]. Moreover, as the gate length decreases, the SS is increased, and there is an increment of 31% is observed as the gate length is scaled from 20 nm to 5 nm. The increment in SS is due to an increment in leakage currents. Other important short channel metrics such as DIBL and V_{th} are shown in Fig. 3.8(b). DIBL is another parameter that severely affects with scaling. As the gate length decreases, the impact of drain potential is more on the channel and leads to the increment of DIBL. From Fig. 3.8(b),

it can be seen that the DIBL is increased and a growth rate of 339% is observed as the gate length ranging from 20 nm to 5 nm.

The threshold voltage variations as a function of gate length are depicted in Fig. 3.8(b). The deterioration in threshold voltage is observed as the gate length is increasing due to the threshold voltage roll-off. As the gate length decreased from 20 nm to 10 nm, a reduction of 1.9% in threshold voltage is observed, whereas from 10 nm to 5 nm, a reduction of 7% is observed. It is obvious that for sub -10 nm, the threshold voltage roll-off is more due to increased SCEs.

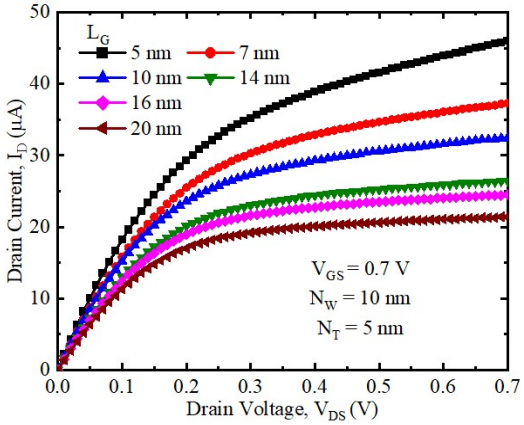


Fig. 3.9: Output characteristics for various L_G values as a function of drain voltage.

The drain current variations with respect to drain voltage are depicted in Fig. 3.9. It can be seen that as the gate length decreases, the drain current is improved. However, the slope in the saturation region is increases with scaling, which lowers the driving capacity of the device.

3.3.3 Impact of Temperature and work function variations on NSFET

Nanoscale transistors are used in a wide variety of fields including communication, automobiles, medical equipment, analog and digital integrated circuits, sensing applications and power electronics. As per the requirement, the nano transistors are used at different temperatures and are crucial to analyze the performance of transistors at various ranges of temperatures [103].

Temperature dependency on drain current as a function of gate voltage is plotted in Fig. 3.10(a). The temperature is varied in the range of -43°C to 127°C. It is very much required to bias these circuits so that the performance or *V-I* characteristics are insensitive or independent towards temperature variations.

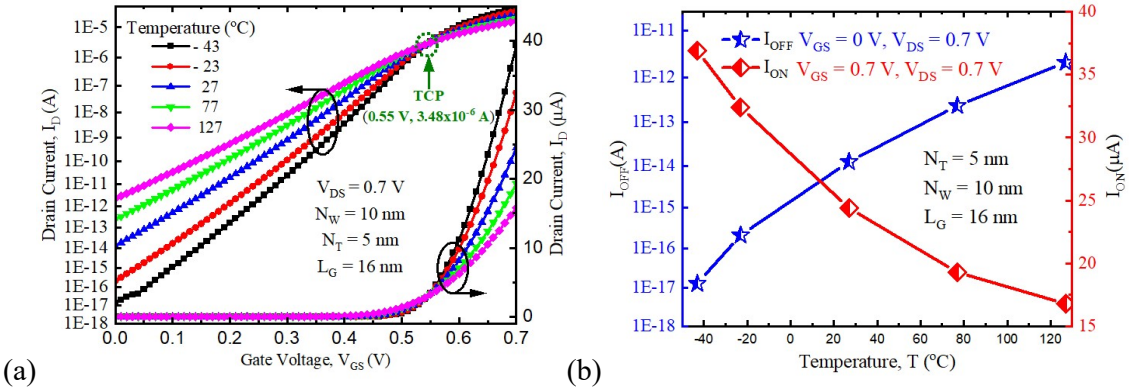


Fig. 3.10: (a) I_D-V_{GS} and (b) I_{ON} and I_{OFF} variations with temperature.

IC designers are very much interested to know this inflection point of temperature. This biasing point is called the temperature compensation point (TCP) [104]. From Fig. 3.10 (a), the TCP is observed at V_{GS} = 0.55 V and I_D = 3.48×10^{-6} A. From Fig. 3.10(b), it is clear that as the temperature increases, an increment in off currents is observed because of the dominance of impurity scattering. Moreover, a slight decrement in on current is observed with rise in temperature due to the mobility reduction.

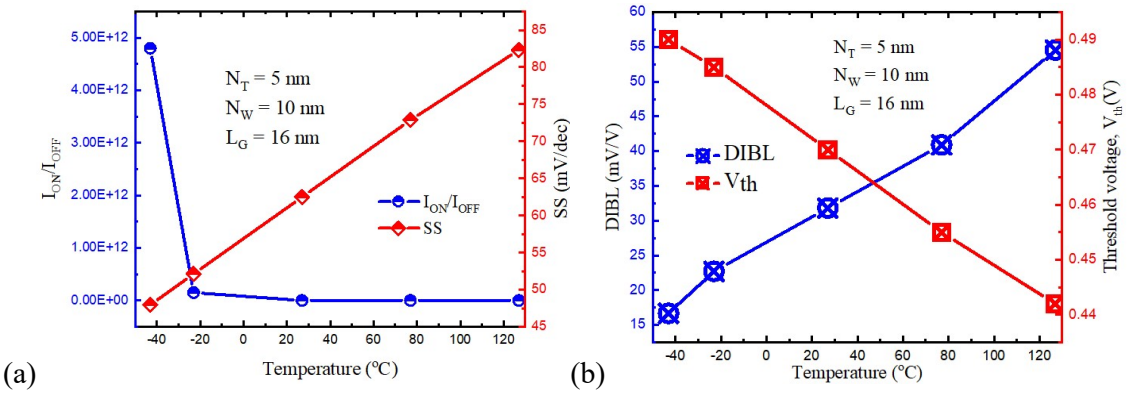


Fig. 3.11: (a) I_{ON}/I_{OFF} and SS (b) DIBL and V_{th} variations as a function of temperature.

I_{ON}/I_{OFF} and SS variations as a function of temperature are presented in Fig. 3.11(a). It is observed that there is deterioration in the switching ratio as the temperature increases because of the significant improvement in the off current. Furthermore, the value of SS is less at low temperatures and ensures faster operation of the device [105]. Fig. 3.11(b) depicts DIBL and V_{th} variations with respect to temperature and is observed that as temperature increases, the rise in DIBL is observed because of the decrement in threshold voltage. Furthermore, threshold voltage deteriorated with the rise in temperature due to scattering phenomena [106]. A Threshold voltage roll-off of 9.7% is observed as temperature increases from -43°C to 127°C.

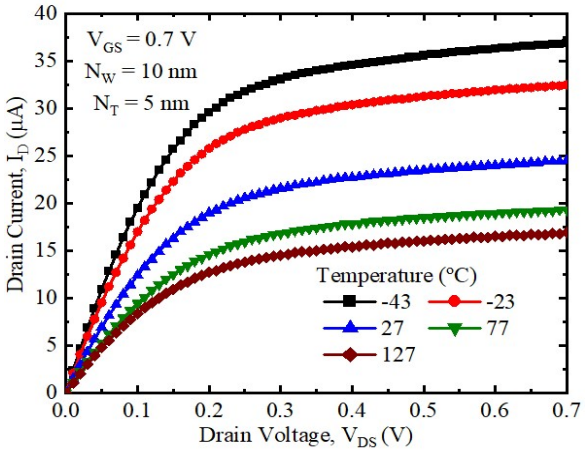
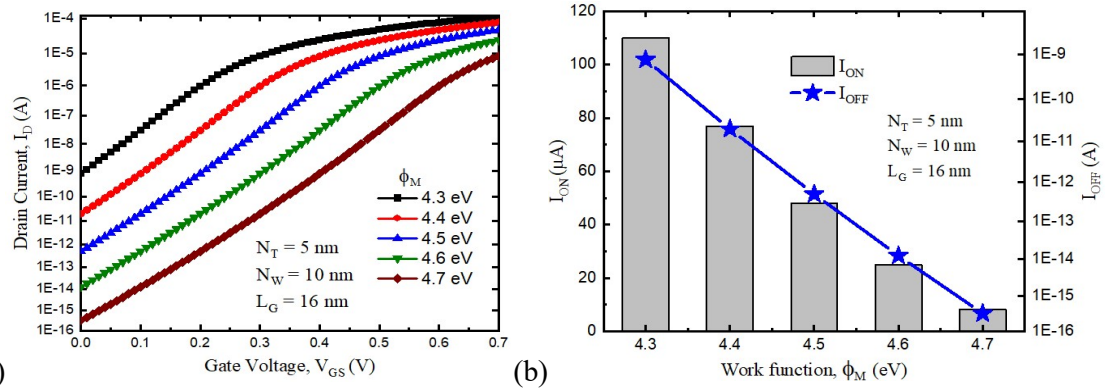


Fig. 3.12: Output characteristics for various temperature values as a function of drain voltage.

The I_D-V_{DS} characteristics for various temperatures are shown in Fig. 3.12. The characteristics are obtained at constant N_W and N_T of 10 nm and 5 nm, respectively. It can be noticed that as the temperature increases, deterioration in drain current is observed due the reduction in mobility.

Work function is one of the important process parameter, which plays a detrimental role in turning on and off of a device. Higher gate work function ensures that the device is fully depleted rapidly and that the device performs better in the off state [107].



(a) (b)

Fig. 3.13: (a) Drain current variations with work function (b) I_{ON} and I_{OFF} variations as a function of work function.

Work function impact on drain current as a function of gate voltage is shown in Fig. 3.13(a). The work function of the device is varied from 4.3 eV to 4.7 eV. From Fig. 3.13(b), it can be inferred that for higher work function of the device, along with the deterioration in on current, a significant reduction in off current is observed. An Increment in work function lowers the

tunneling between gate and channel and also between gate and drain/source [108], which helps to reduce the leakage current.

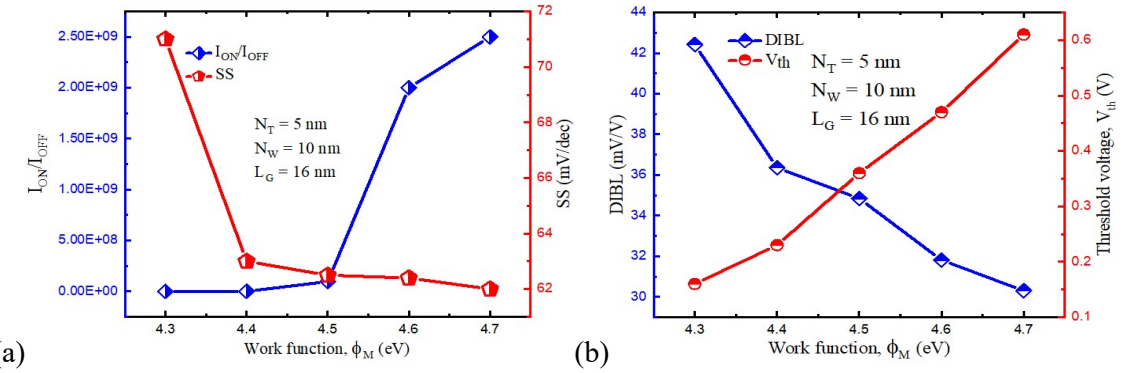


Fig. 3.14: (a) I_{ON}/I_{OFF} and SS (b) DIBL and V_{th} variations as a function of work function.

Switching ratio variations with respect to work function are shown in Fig. 14(a). The switching ratio improved significantly with the rise in work function due to a huge reduction in off current. With the increment of work function, the SS gets decremented and ensures good subthreshold performance. Fig. 14(b) depicts the DIBL and threshold voltage variations as a function of the work function. DIBL decreases with the rise in work function, and lesser DIBL indicates that the electrostatic integrity of the gate is more on the device and less sensitive to drain voltage variations. A minimum DIBL of 30.30 mV/V is obtained for work function of 4.7 eV, and there is a decrement of 28.6% in DIBL is observed when the work function varied from 4.3 eV to 4.7 eV. However, there is a huge decrement in threshold voltage with the fall in the work function of the device. There is a decrement of 3.9x in threshold voltage as the work function is decreased from 4.7 eV to 4.3 eV, and this leads to more SCEs. Moreover, the study tells that the devices with more work function will have high threshold voltages and makes the device sluggish.

From Fig. 3.15, it can be seen that for higher work function values, the slope of I_D -V_{DS} characteristics is less and ensures lower output conductance value. Furthermore, it is noticed that the slope for $\Phi_M = 4.7$eV is less compared to $\Phi_M = 4.3$eV.

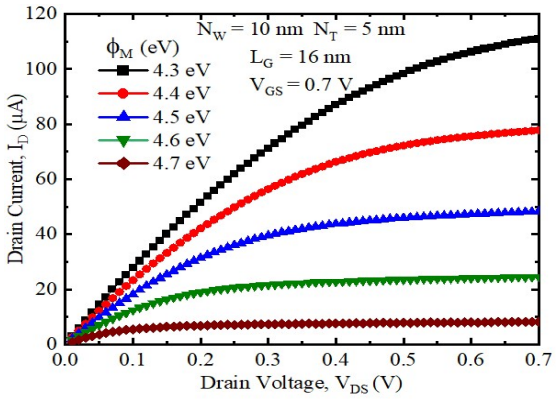


Fig. 3.15: Output characteristics for various work function values as a function of drain voltage.

In this chapter, the detailed DC performance of 3D vertically stacked NSFET is analyzed by varying the thickness and width of the nanosheet. It is observed that there is an increment in both on current and off current as the width and thickness values are increased. However, the switching ratio, DIBL, and SS are degraded as the dimensions of NSFET increase. Moreover, the performance of NSFET is analysed with scaling of gate length to ensure the device feasibility for lower technology nodes. Also, the temperature analysis is performed for a wide range of temperatures to identify the TCP point, which is more essential for biasing the device in various real-time applications. Finally, the impact of work function on device transfer characteristics is analysed. These results will give deep insights into the performance of NSFET with different device parametric variations.

3.4 Conclusion

1. It is observed that there is an increment in both on current and off current as the width and thickness values are increased. However, the switching ratio, DIBL, and SS are degraded as the dimensions of NSFET are increasing.

2. The impact of temperature on DC performance is addressed. The result analysis reveals that as the temperature increases, DC performance is degraded. The important process parameter, workfunction analysis is performed and analysed its impact on DC performance of the device. As workfunction increases, both on current and off current decrease and threshold voltage increases.

3. The scaling of NSFET explored for sub-5-nm nodes. The results analysis indicates that the NSFET is capable to continue Moore's law.

Chapter-4

Device and Circuit-Level Performance Comparison of GAA Nanosheet FET With Varied Geometrical Parameters

4.1 Introduction

The impact of geometry, temperature and work function variations on DC performance of NSFET is discussed in chapter 3. As the N_W and N_T values increases, the device current increases owing to the increased effective area of the channel. However, the subthreshold performance metrics such as SS and DIBL are degraded with the rise in dimensions owing to the depreciation of gate control over the channel with the rise in dimension of the channel.

For a device to be used in analog/RF applications, it is highly essential to examine the analog/RF figures of merit (FOM). Thus, in this chapter, DC and analog/RF figures of merit (FOMs) for different geometrical variations of the Gate all around (GAA) Nanosheet FET (NSFET) are computationally examined. For each nanosheet, the thickness (N_T) varied from 5 nm to 9 nm and the width (N_W) varied from 10 nm to 50 nm to analyze the performance variations with the device's geometry. Various analog/RF FOMs like transconductance (g_m), output conductance (g_{ds}), intrinsic gain (g_m/g_{ds}), cut-off frequency (f_T), transconductance frequency product (TFP), and gain bandwidth product (GBW), gain frequency product (GFP), and gain transconductance frequency product (GTFP) are analysed by altering the geometry of NS.

Moreover, the device is the building block of any circuit. The circuit's performance is affected by the behaviour of the device. Thus, in this chapter, the impact of device geometry on circuit performance is discussed in detail. In order to evaluate the NSFET performance towards circuit applications, digital circuits like inverter and ring oscillator (RO) are designed and demonstrated their performance. According to the various results analyses, NSFET is a promising device for high performance and high frequency analog/RF applications for sub-7-nm.

4.2. Device Structure and Simulation Methodology

The three-dimensional diagram of GAA NSFET is depicted in Fig. 4.1(a). 2-D cross sectional view in the XZ plane is shown in Fig. 4.1(b), where N_T and N_W are the thickness and width of each nanosheet, respectively. Further, the NSFET with stacked nanosheets is shown in Fig. 4.1(c).

A gate length (L_G) of 16 nm is considered for NSFET. A p-type doping concentration of 10^{15} cm^{-3} and an n-type doping concentration of 10^{20} cm^{-3} for channel and source/drain, respectively used for simulation. To overcome the gate oxide tunneling a high-k gate stack with HfO_2 of 1.5 nm and interfacial oxide of 0.5 nm, which forms an effective oxide thickness (EOT) of 0.78 nm, is considered. The metal gate with the work function of 4.6 eV is maintained throughout the simulations. To overcome the direct tunneling a spacer distance of 5 nm is incorporated, which improves the subthreshold performance [109]. Table. 4.1 provides the values of device parameters included in the simulation.

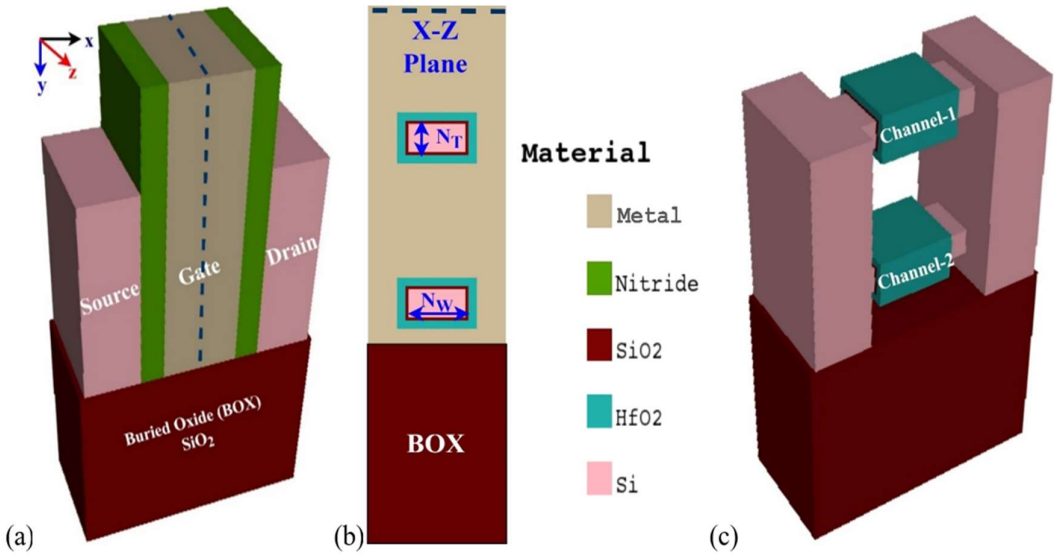


Fig. 4.1: (a) Three-dimensional view of NSFET with nitride spacer, (b) cross sectional view of NSFET with N_T and N_W and (c) three-dimensional view of NSFET with nanosheet channels.

Parameter	Value
Thickness of nanosheet (nm)	5-9
Width of nanosheet (nm)	10-50
Length of the gate (nm)	16
Source/Drain doping (cm^{-3})	10^{20}
Doping of the channel (cm^{-3})	10^{15}
EOT (T_{SiO2} +($\varepsilon_{SiO2}/\varepsilon_{HfO2}$) ×$T_{HfO2}$) (nm)	0.78
Dielectric of Underlap	Nitride
Pad length of Drain/Source (nm)	12
Source/Drain underlap length (nm)	5
Gate work function (eV)	4.6
Height of the gate (nm)	60

Table 4.1: Simulation parameters

All the simulations have been performed using the Genius 3D simulator by Cogenda [55] at a fixed temperature of 300 K. The calibration of the proposed device is performed and discussed in chapter 3.

4.3. Results and Conclusions

4.3.1. Geometry Dependence on DC Metrics of NSFET

In this section, the NSFET's DC metrics are evaluated with various thickness and width values and are discussed in detail. The major performance characteristics mentioned in this section include I_{ON}, I_{OFF}, switching ratio (I_{ON}/I_{OFF}), threshold voltage (V_{th}), DIBL, and SS.

The dependence of electron mobility on the channel in the ON state is depicted in Fig.4.2(a). The device exhibits higher mobility in the channel area due to better gate electrostatics. Fig.

4.2(b) depicts the electric field distribution of NSFET. The device exhibits a higher electric field in the spacer region. However, the impact is lower on the channel. Fig. 4.2(c) depicts the potential distribution of NSFET at $V_{DS} = V_{GS} = 0.7$ V.

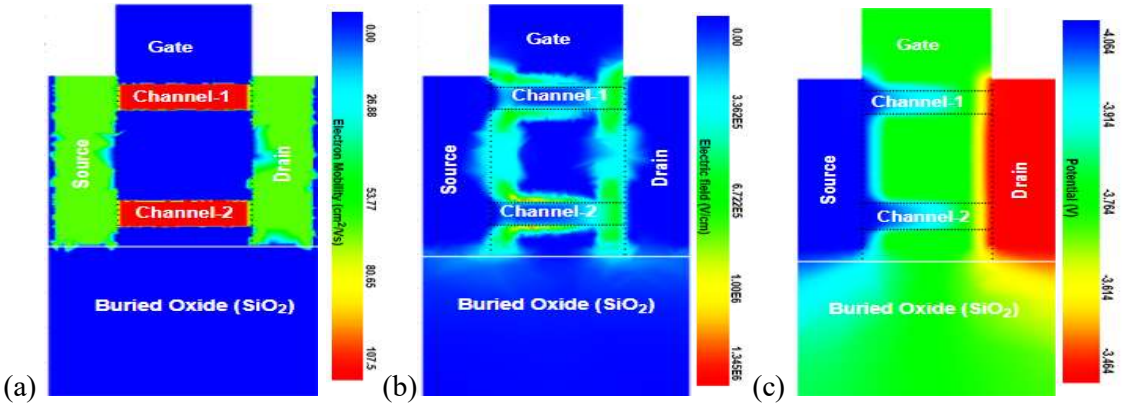


Fig. 4.2: (a) Electron mobility (b) Electric field distribution (c) Potential of NSFET.

The rise in drain current and parasitic capacitance is a trade-off when using high-k spacers to reduce circuit delay. Enhanced spacer designs will be required to improve circuit and device performance even more by lowering parasitic capacitances while maintaining a high drive current [110]. In our work, the nitride spacer with an optimized thickness of 5 nm is considered, which offers lower degradation of the I_{eff}/C_{eff} electrical performance [64]. The introduction of high-*k* spacers induces field coupling through the fringing effect and enhances switching ratios [111]. By using nitride spacer due to the more distance between the channel and drain ensures reduced drain potential over the channel and minimizes SCEs as shown in Fig. 4.2(c).

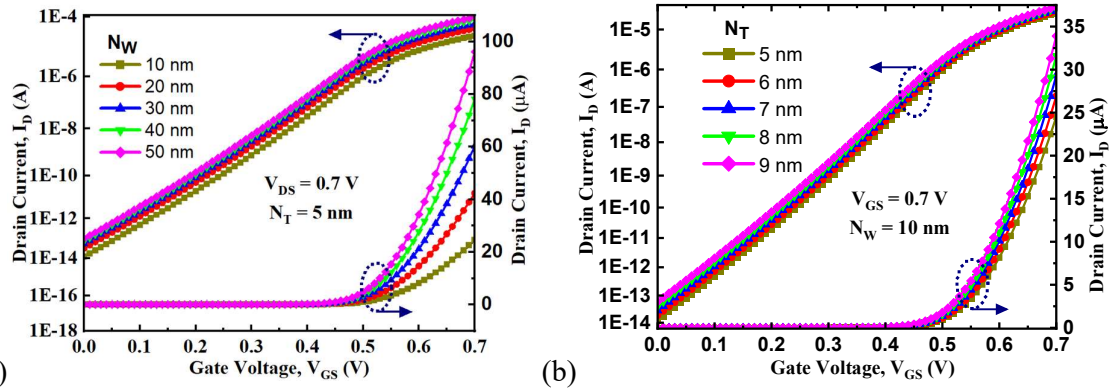


Fig. 4.3: Transfer characteristics of NSFET in linear and log scale for various (a) N_W values and (a) N_T values.

Figure 4.3(a) and (b) show the transfer characteristics NSFET with various widths and thicknesses, respectively at a constant L_G of 16 nm. The flow of current in the nanosheet is dependent on the width and thickness of the nanosheet. In order to evaluate the impact of I_D on N_W, the device width is varied from a minimum of 10 nm to 50 nm. Moreover, the N_T is also varied from 5 nm to 9 nm to see the impact of N_T on I_D. As the N_W and N_T values increase, the I_D increases owing to the raised area of the channel.

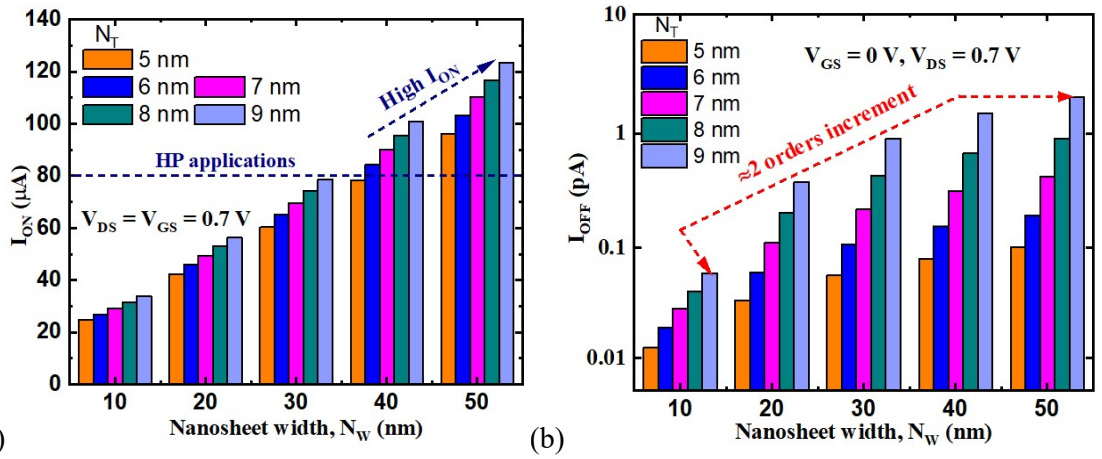


Fig. 4.4: (a) I_{ON} and (b) I_{OFF} as a function of N_W for various N_T values.

Figure 4.4(a) depicts the ON current (I_{ON}) of the device at $V_{GS} = V_{DS} = 0.7$ V, which is a crucial measure for high performance applications. Also, the proportionality increment in I_{ON} with respect to effective width gives rise to higher currents when the nanosheet's geometry increases. The highest increment of 286% in I_{ON} is observed for N_T of 5 nm for the N_W ranging from 10 nm to 50 nm. The OFF current (I_{OFF}) variations are shown in Fig. 4.4(b) with respect to various width and thickness values of the nanosheet. In addition to the increment in I_{ON}, I_{OFF} also gets incremented with the increment in the geometry of NS and is shown in Fig. 4.4(b). This phenomenon is observed since an increment in N_W leads to more leakages in the device because of the degraded control of the gate over the channel. It is evident that by using thinner nanosheets, the I_{OFF} is mitigated. In the OFF state, as the N_T increases, the potential barrier height and conduction band energy in the channel gets reduced and lead to an increment in leakage currents. However, as the thickness decreases, the I_{ON} decreases marginally due to mobility degradation caused by an increase in the perpendicular electric field [50]. An increment of 2 orders in I_{OFF} is observed with the increment in N_W from 10 nm to 50 nm at N_T of 9 nm. As N_T is increasing, there is a large increment in the I_{OFF} is observed due to the degradation of electrostatic integrity over the channel.

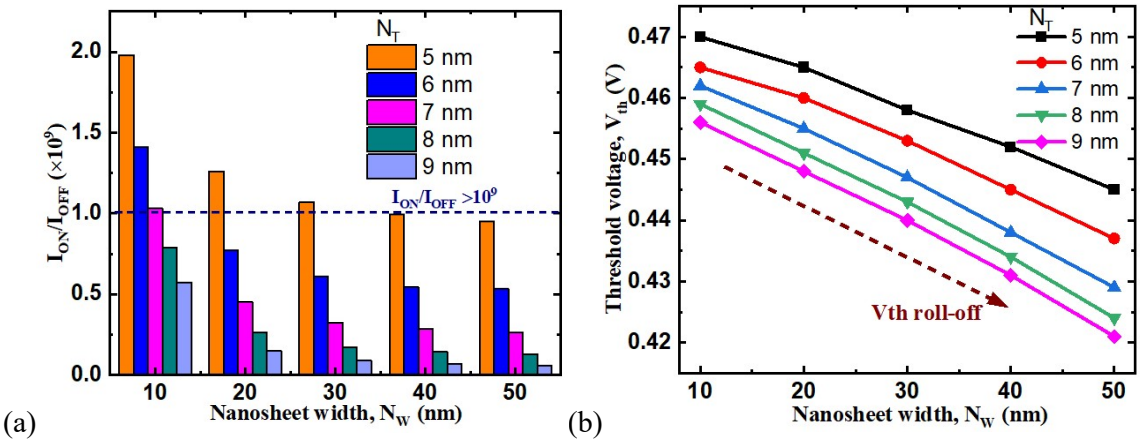


Fig. 4.5: (a) Switching ratio and (b) Threshold voltage (V_{th}) variations as a function of N_W for various N_T values.

Fig. 4.5(a) depicts I_{ON}/I_{OFF} variations with respect to N_W for various values of N_T. For better logic applications, the switching ratio of 10^6 is feasible. It is observed from Fig. 4.5(a) that the switching ratio performance deteriorates as the N_W increases due to large increment in I_{OFF}. A large increment in the I_{OFF} with a marginal increment in I_{ON} tends to cause a downfall in the I_{ON}/I_{OFF} as N_W increases. Moreover, the switching ratio decreases as the N_T increase, which is because of a huge increment in I_{OFF} due to the reduced electrostatic integrity of the gate over the channel. The highest decrement 89% in switching ratio is noticed for N_T of 9 nm as the N_W is increased towards 50 nm. Degradation of the switching ratio is more as the N_T increases due to weak electrostatic control of the gate over the channel. Threshold voltage (V_{th}) variations are shown in Fig. 4.5(b). The V_{th} gets decrement as the N_W is increases due to an increment in leakage currents. The same trend is observed as the N_T is increased. It is seen that a downfall of 2.9% and 5.4% in V_{th} for N_W of 10 nm and 50 nm, as the N_T is ranges from 5 to 9 nm. Similarly, a fall of 5.3% and 7.6% in V_{th} are observed for the N_T of 5 and 9 nm, as the N_W is increased. As the N_T and N_W values are increasing, the V_{th} roll-off is more since the deterioration of gate electrostatics on the channel region.

SS is an essential parameter for the evaluation of subthreshold performance towards low power applications. SS gives the value of V_{GS} required to get a decade change in I_D. Lower SS values are preferred for the good subthreshold operation of the device. SS values as a function N_W for various N_T values are given in Fig. 4.6(a). The NSFET with geometrical values of N_W and N_T of 10 nm and 5 nm performs best with an SS of 62.5 mV/dec, which is close to the optimum value.

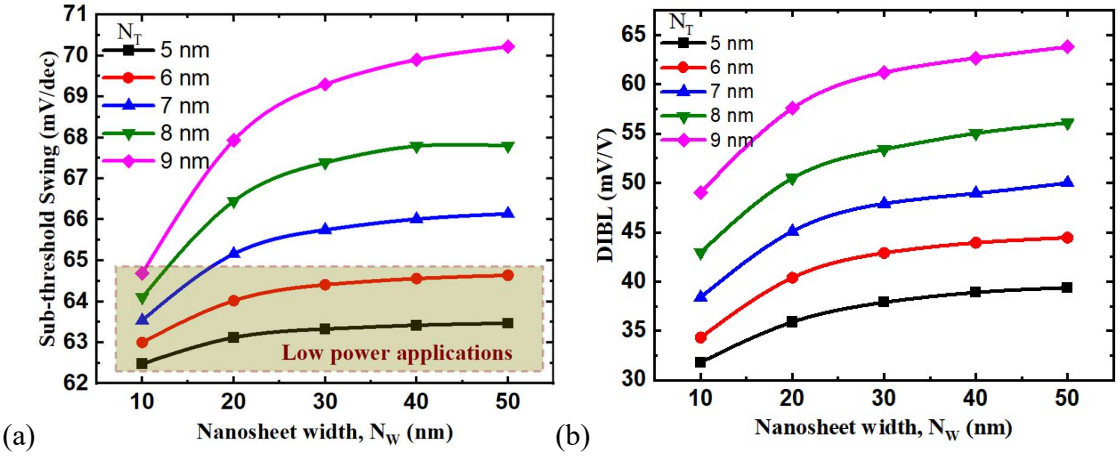


Fig .4.6: (a) SS and (b) DIBL as a function of N_W for various N_T values.

As the N_W is increasing, a maximum increment of 8.6% in SS is found for N_T of 9 nm. As the N_T is raised, a maximum growth of 10.6% in SS is noticed for N_W of 50 nm. The sub-threshold performance degrades for higher N_W and N_T values because of higher SS. DIBL is another important sub-threshold performance measure, and a low value of DIBL is preferred for optimal device performance. Fig. 4.6(b) depicts DIBL values as a function of N_W for various N_T values. It can be seen that when the dimensions of the nanosheets grow, the DIBL grows as well. By integrating nanosheets with lesser width and thickness, the DIBL can be reduced due to low V_{th} roll-off. For N_W 50 nm, the highest increment of 30.6% in DIBL is observed. Also, for N_T of 9 nm, the highest increment of 62% in DIBL is noticed. From this, it can be inferred that DIBL is sensitive towards higher width and thickness variations.

4.3.2. Geometry Influence on Analog/RF Response of GAA NSFET.

The aggressive scaling of devices made it possible to build system-on-chip (SOC) devices. Analog and RF circuits are embedded in SOC for various applications. Thus, the study of analog and RF metrics of a device is very crucial to estimate the potential of the device towards analog and RF applications. In this section, various analog/RF metrics like g_m, TGF, g_{ds}, intrinsic gain, cut-off frequency, intrinsic delay, TFP, GFP, GTFP, and GBW are studied for different geometries of NSFET.

Transconductance (g_m) is one of the important analog metrics which evaluates the change in I_D obtained to the corresponding change in V_{GS}. Inherently g_m gives the speed of a device and better g_m indicates that the device can operate at high speed for logic operations. Moreover, the

gate transport efficiency is high for devices which are having high g_m. Transconductance decides the amplifying capability of the device. A higher amount of gain or amplification can be obtained by having more g_m values for analog applications. g_m can be calculated by using equation 4.1.

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \qquad (4.1)$$

Fig. 4.6(a) depicts the g_m variations for various N_W and N_T values. It is noticed that for the lesser nanosheet widths, the value of g_m is less. Higher g_m values can be obtained by increasing the nanosheet thickness and width. Due to the peak electron velocity at the source region and less channel doping in the channel region, higher g_m is obtained. As the N_W increasing, the highest increment of 273% in g_m is observed for N_T of 5 nm. Also, the highest increment of 32% in g_m is observed for N_W of 10 nm as the N_T increases towards the upper bound. It is noticed that the improvement in g_m is due to the raise in drain current for larger N_T and N_W values.

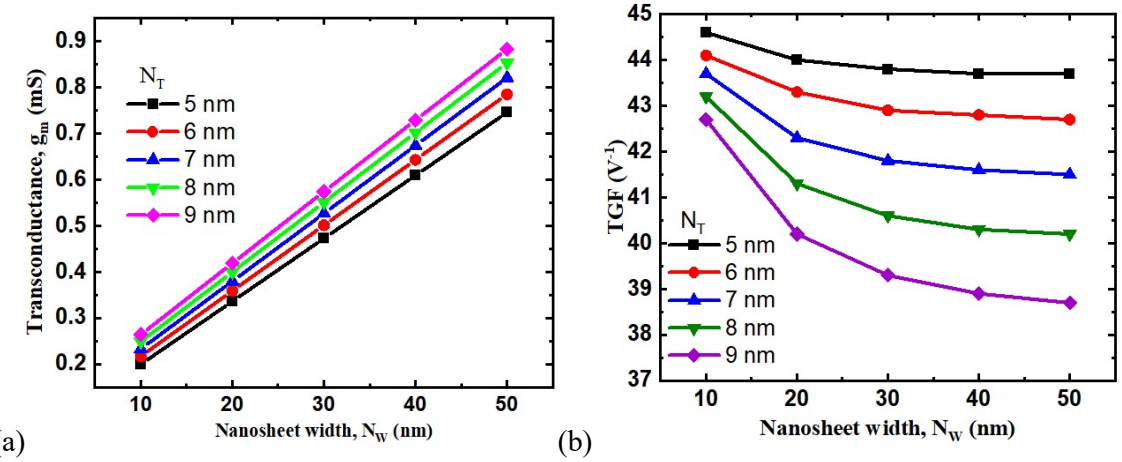


Fig .4.7: (a) Transconductance (g_m) and (b) Transconductance generation factor (TGF) values as a function of N_W for various N_T values.

Transconductance generation factor (TGF = g_m/I_D), is another crucial analog FOM and it estimates the efficient use of drain current to obtain the agreeable value of g_m. It is also taken as accessible gain per unit power dissipation. The device with more TGF values can be operated at lower voltages without deteriorating the performance [112]. Also, TGF is used to estimate

the power required to achieve high speed [52]. The variations in TGF as a function N_W for various N_T values are depicted in Fig. 4.7(b). As the N_T and N_W values increase, a reduction in TGF is noticed. In the weak inversion region, higher TGF values are obtained and tend to decrease in the super threshold region due to velocity saturation.

In addition to the increase in g_m, an increase in I_D is noticed when the N_W and N_T increase due to the rise in effective width. There is a growth rate of 273% in g_m observed when the N_W is increased from 10 nm to 50 nm. However, the growth rate of 286 % in I_D is observed when the width is increased from 10 nm to 50 nm, which is more than the growth rate of g_m. This makes the TGF downfall in spite of the increment in g_m. The highest 8.8% in TGF is observed for N_T of 9 nm as the N_W is increased from 10 nm to 50 nm. Also, the highest decrement 8.3% in TGF is observed for N_W of 50 nm as the N_T is raised from 5 to 9 nm. It can be seen that the deterioration in TGF is observed for increment in N_W and N_T values of NSFET.

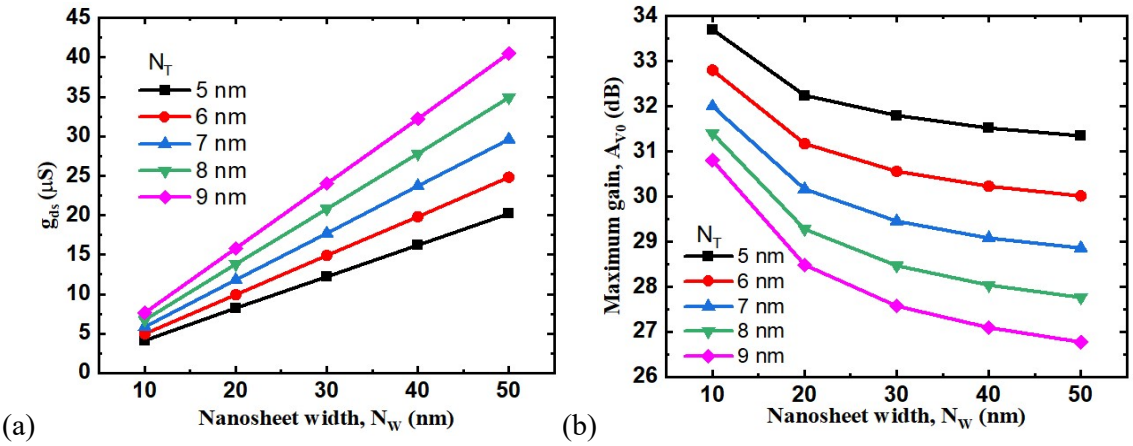


Fig. 4.8: (a) g_{ds} and (b) Maximum gain, A_{V0} values as a function of N_W for various N_T values.

Another essential analog/RF figure of merit is output conductance (g_{ds}), and it should be minimum for good performance of the device. Mostly, the devices incorporated in analog circuit design are operated at the saturation region. Ideally, in the saturation region, the drain current is independent of drain voltage. However, because of short channel effects like DIBL, the variation in drain voltage leads to variations in drain current also. To measure the dependency of drain current on drain voltage in the saturation region, the parameter gds is evaluated and for better performance, the g_{ds} values should be as minimum as possible. The g_{ds} is given by equation (4.2).

$$g_{ds} = \frac{\partial I_D}{\partial V_{DS}} \qquad (4.2)$$

Fig. 4.8(a) depicts g_{ds} variations for various nanosheet width and thickness values. It is clearly seen that for nanosheet width of 10 nm and thickness of 5 nm outperforms remaining all variations and can be concluded that for higher values of nanosheet's width and thickness, the amplification capacity of the device degrades since g_{ds} is increasing. Moreover, for thicker nanosheets, g_{ds} is increasing drastically. The highest increment of 431% in g_{ds} is noticed for N_T 9 nm, respectively as the N_W is increased from 10 nm to 50 nm. Also, an increment 101% in g_{ds} is observed for N_W of 50 nm as the N_T is increased from 5 to 9 nm.

Intrinsic gain for various N_W and N_T variations is shown in Fig. 4.8(b). It is noticed that with the increment in N_W, the gain is deteriorating because of the increased dependency of drain current on drain voltage. Similarly, the higher gain is obtained for thinner nanosheets because of the decrement in output conductance and enhanced gate electrostatics over the channel. The highest decrement of 13.1% in gain is observed for N_T of 9 nm as the N_W is increased from 10 nm to 50 nm. Also, the highest deterioration of 14.6% in gain is observed for N_W of 50 nm as the N_T is increased from 5 to 9 nm. For higher values of N_W and N_T the gain is deteriorating because of the increment in output conductance.

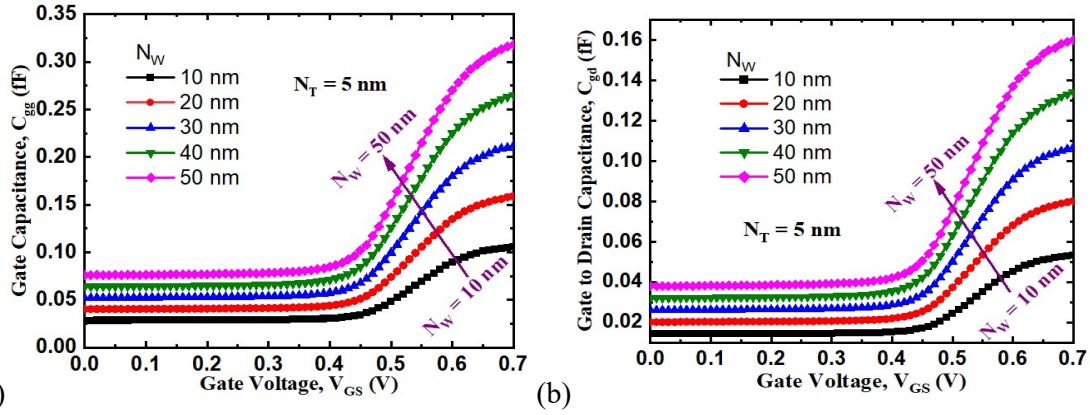


Fig. 4.9: (a) C_{gg} and (b) C_{gd} versus V_{GS} for various N_W values for constant N_T of 5 nm.

Fig. 4.9(a) and (b) show the C_{gg} and C_{gd} variations as a function of V_{GS} for various N_W values at a constant N_T of 5 nm. Also, Fig. 4.10(a) and (b) depict the C_{gg} and C_{gd} variations with V_{GS} for various N_T values of the nanosheet at a constant N_W of 10 nm. The gate capacitance is the summation of both C_{gs} and C_{gd}, i.e., $C_{gg} = C_{gd} + C_{gs}$. It can be deduced from Figs. 4.9 and 4.10

that as the nanosheet dimensions grow, the C_{gg} and C_{gd} increase due to the increase in effective area.

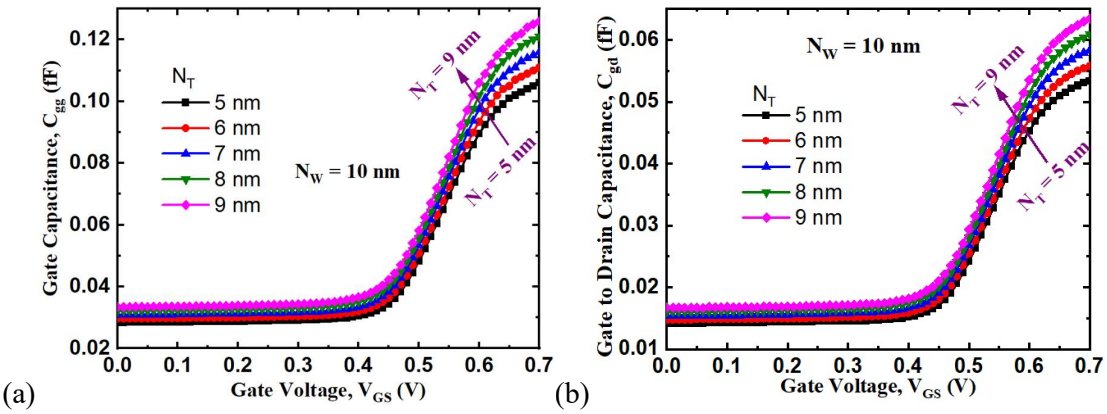


Fig. 4.10: (a) C_{gg} and (b) C_{gd} values as a function of V_{GS} for various N_T values for constant N_W of 10 nm.

To analyze a device for its suitability for high frequency applications, it is crucial to consider the Miller capacitance (C_{gd}) [39]. Miller capacitances are capacitances between the output and input that mitigate the device's gain performance at high frequencies. The crucial FOMs, which are dependent on Miller capacitances, are discussed further in this chapter.

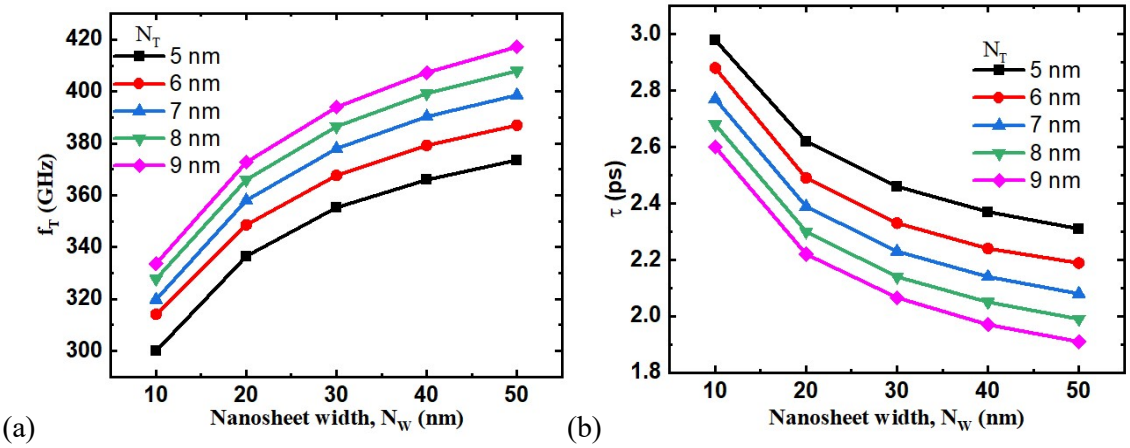


Fig. 4.11: (a) f_T (b) Intrinsic delay, τ values with respect to N_W for different N_T values.

Cut-off frequency (f_T) is another important characteristic to consider when evaluating the device's analog/RF performance. Usually, the f_T is derived by taking into account of the frequency at which the magnitude of current gain is equal to one. The cut-off frequency is defined as [113], given in equation 4.3.

$$f_T = \frac{g_m}{2\pi(C_{gs}+C_{gd})} \qquad (4.3)$$

From Fig. 4.11(a), the variations in f_T are observed from different geometrical variations of NSFET. It can be seen that with the rise in N_W, the f_T followed an increasing manner. As the N_W and N_T increase, the transconductance, effective width, and capacitance values increase and cause an increase in cut-off frequency. The maximum increment of 24.6%, in cut-off frequency, is obtained for N_T of 7 nm N_W increases from lower to upper bound. Also, the highest increment of 10.8% in f_T is observed for N_W of 20 nm as N_T is increased from the lower to upper bound.

The intrinsic delay, τ is shown in Fig. 4.11(b). Basically, τ can be obtained by taking the product of total resistance and total capacitances [114]. τ is very important FOM to evaluate the device's practicality in SOC applications [115]. The intrinsic delay is given by the equation (4.4).

$$\tau = \frac{C_{gg}V_{DD}}{I_{ON}} \qquad (4.4)$$

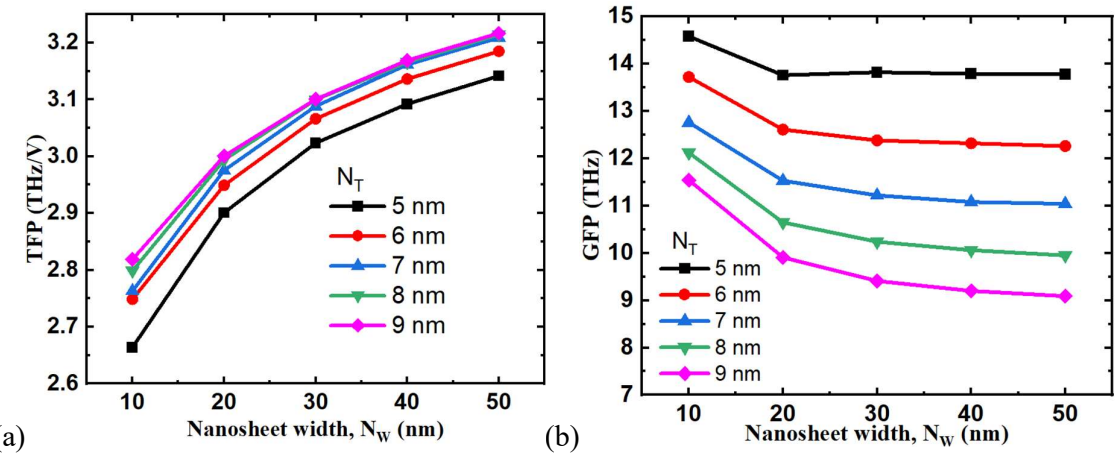
From equation (4.4), it can be seen that τ is proportional to the total capacitance C_{gg} and power supply and is inversely proportional to the I_{ON} of the device. It is obvious that as the effective width of the nanosheet increases, both on current and gate capacitance of the device are boosted up. As the N_W is increased from 10 nm to 50 nm, there is an enhancement of 4x in I_{ON} and 2x in C_{gg} for a fixed N_T of 5 nm. So compared to the improvement in on current, the increment in the gate capacitance is less. Thus, there is a downfall in τ as the N_W ranges from 10 nm to 50 nm. It is noticed that the lowest delay characteristics are obtained for an N_W of 50 nm. The decrement of 22.5% and 26.5% in τ is observed for N_T values of 5 nm and 9 nm, respectively as the N_W raised from 10 nm to 50 nm. Also, the decrement of 12.7% and 17.3% in the τ is observed for N_W of 10 nm, and 50 nm, respectively, as the N_T is increased from 5 to 9 nm.

The TFP is shown in Fig. 4.12(a). TFP is another important analog/RF figure of merit and is obtained by taking the product of transconductance and cut-off frequency, given by equation (4.5) [101].

$$TFP = \frac{g_m}{I_D} \times f_T \qquad (4.5)$$

TFP gives the trade-off between bandwidth and power and is used in medium and high-speed circuit applications [116]. From Fig. 4.12(a), it can be observed that TFP is more for higher N_T and N_W values because of the increment in cut-off frequency. The highest increment of 17.9%

and the lowest increment of 14.11% are observed as the N_W is varied from 10 nm to 50 nm for N_T of 5 nm and 9 nm, respectively. Also, the maximum increment of 5.8% and minimum increment of 2.4% in TFP are noticed for N_W of 10 nm and 50 nm, respectively as the N_T is increased from 5 nm to 9 nm.



(a) (b)

Fig. 4.12: (a) TFP and (b) GFP values as a function of N_W for various N_T values.

Gain frequency product (GFP) is another crucial analog/RF figure of merit [117], given by

$$GFP = \frac{g_m}{g_{ds}} \times f_T \qquad (4.6)$$

As the intrinsic gain is the most important parameter for operational amplifiers, GFP is depicted in Fig. 4.12(b) is used to estimate the performance of operational amplifiers in high frequency circuit implementations. There is a decrement in GFP observed for increment in N_W and N_T values. The decrement of 5.5% and of 21% in GFP was observed as the N_W varies from 10 nm to 50 nm for N_T of 5 nm and 9 nm, respectively. Also, the decrement of 21% and 34% in GFP are observed for N_W of 10 nm and 50 nm, respectively as the N_T is increased from 5 nm to 9 nm. More deterioration in GFP is observed for higher N_T and N_W values since there is an increment in the g_{ds}.

The gain transconductance frequency product (GTFP) is very much useful for circuit designers. GTFP allows the designers to identify the optimum region achieving a good trade-off among parameters like transconductance, speed, and gain of the device [116]. GTFP is given by equation 4.7.

$$GTFP = A_{V0} \times TFP = \frac{g_m}{g_{ds}} \times \frac{g_m}{I_D} \times f_T \quad (4.7)$$

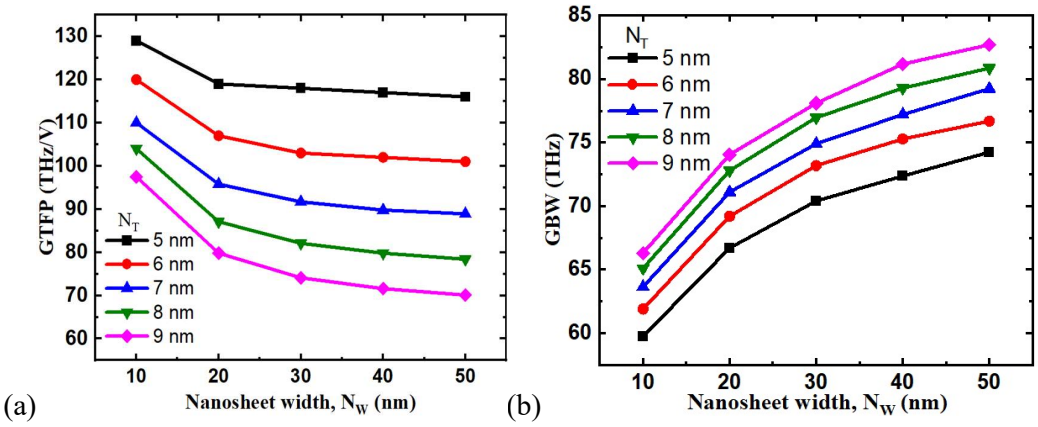


Fig. 4.13:(a) GTFP and (b) GBW values as a function of N_W for various N_T values.

The GTFP as a function of nanosheet width for various nanosheet thickness values is depicted in Fig. 4.13(a). It can be seen that by using less N_W and N_T for nanosheet, higher GTFP can be achieved. For N_T of 5 nm and 9 nm, respectively, the decrement of 10% and 28% in GTFP were found when the N_W varied from 10 nm to 50 nm. Also, the decrement of 24% and of 40% in GTFP is observed for N_W of 10 nm, and 50 nm, respectively, as the N_T is increased from 5 nm to 9 nm.

Another crucial analog/RF FOM is the gain bandwidth product (GBW) which is used to evaluate device efficiency in high frequency applications. GBW can be calculated by the following equation 4.8 [117].

$$GBW = \frac{g_m}{20\pi C_{gd}} \qquad (4.8)$$

From Fig. 4.13(b), it can be seen that as the width and thickness increase, the increment in GBW is observed since it is proportional to transconductance (g_m). Miller capacitance or gate to drain capacitance (C_{gd}) increases with increment in width and thickness values. However, the improvement in GBW is observed because of a large improvement in g_m compared to C_{gd}. An increment of 23.8% and 24.7%, in GBW is observed for thickness values of 6 nm and 9 nm respectively as the N_W is increased from 10 to 50 nm. Moreover, an increment of 10.93% and 12.2% in GBW is observed for N_W of 30 nm and 40 nm respectively as the N_T is increased from 5 to 9 nm. The comparison of DC and analog/RF metrics with existing literature is given Table. 4.2.

Reference	I_{ON}	I_{OFF}	I_{ON}/I_{OFF}	SS (mV/dec)	DIBL (mV/V)	g_m (S)	f_T (GHz)
[50]	6.8×10^{-5} A	6.7×10^{-12} A	2.3×10^{7}	71	22.8	-	404
[118]	16.6×10^{-5} A	-	-	-	32	78×10^{-5}	607
[119]	2.37×10^{-5} A/µm	1.15×10^{-10} A/µm	2×10^{5}	70.89	-	5.4×10^{-5}	3790
[51]	832 µA/µm	13.3 nA/µm	6.3×10^{4}	74	-	-	-
This work	2.45×10^{-5} A	1.24×10^{-14} A	1.98×10^{9}	62.48	31.81	2E-4	300

Table 4.2: Comparison of DC and analog/RF metrics with existing literature.

4.3.3. Geometry Influence on Circuit Applications of GAA NSFET.

In this section, the impact of nanosheet width on the inverter and ring oscillator's performance is analysed by performing the SPICE simulation using look up table-based Verilog-A model [39]. The flow of the SPICE simulation is shown in Fig. 4.14. Also, the matching of TCAD with Cadence data is shown in Fig. 4.15.

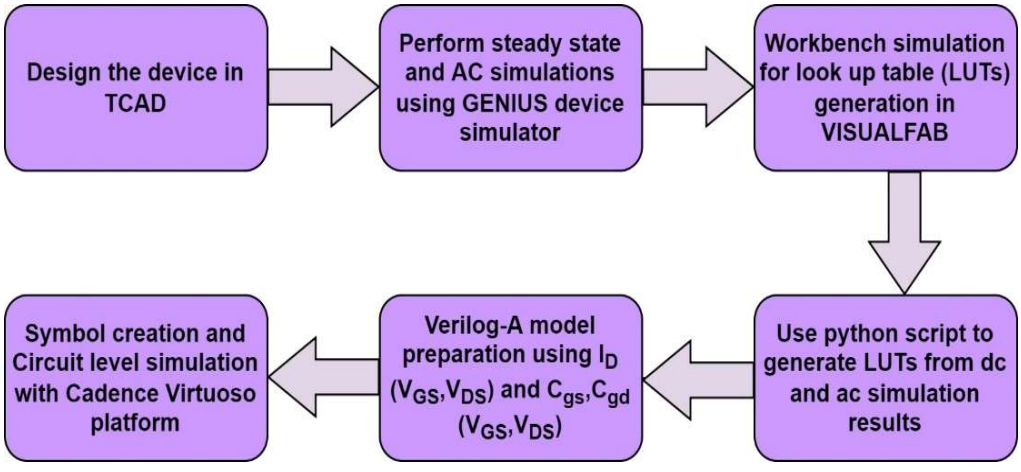


Fig. 4.14: Flow chart of Verilog-A model creation and SPICE simulation.

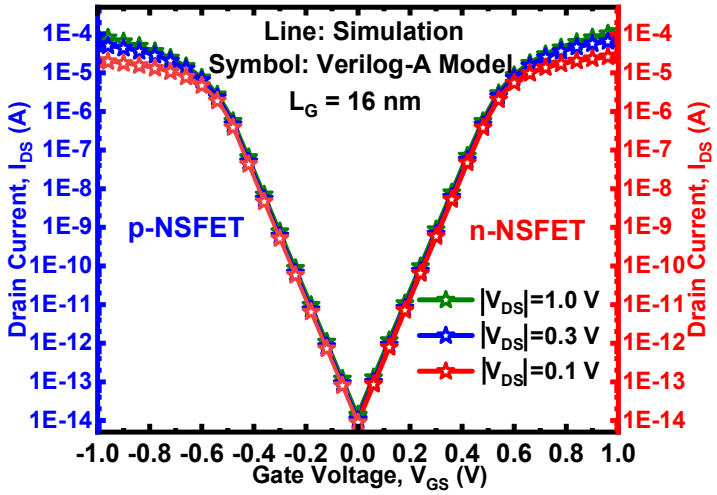


Fig. 4.15: Calibration of TCAD data with Verilog-A model.

Initially, the device is designed using the Visual TCAD tool [55]. On top of that, the DC and AC characteristics are obtained using the Visual Fab parallel simulation platform. From the obtained characteristics, the look up tables are prepared using the format shown in Fig. 4.16. By using the look up tables and Verilog - A model, the symbol is created in the Cadence Virtuoso tool [120] and is further used in schematic diagrams.

I_DV_{GS}-NSFET.tbl

V_{DS}	V_{GS}	I_D
---	---	---
⋮	⋮	⋮
---	---	---

Cgd-NSFET.tbl

V_{ds}	V_{gs}	C_{gd}
---	---	---
⋮	⋮	⋮
---	---	---

Cgs-NSFET.tbl

V_{ds}	V_{gs}	C_{gs}
---	---	---
⋮	⋮	⋮
---	---	---

Verilog - A code

```
`include "constants.vams"
`include "disciplines.vams"

module NSFET(d,g,s);
inout d,g,s;
electrical g,d,s;
real Ids, Cgs, Cgd, Qgs, Qgd, Qg;
real VgsEff;
integer out_file;
parameter real W=1;

analog begin

Ids=$table_model(V(d,s), (V(g,s)), "IDVGS-NSFET.tbl","1LL,1LL");
Cgd=$table_model(V(d,s), (V(g,s)), "Cgd-NSFET.tbl","1LL,1LL");
Cgs=$table_model(V(d,s), (V(g,s)), "Cgs-NSFET.tbl","1LL,1LL");

if(analysis("dc")) begin
   I(d,s) <+ 1*Ids*W;
end
else begin
 if(analysis("tran")) begin
    Qgd = (W*1*Cgd)*(V(g,d));
    Qgs = (W*1*Cgs)*(V(g,s));
    Qg=Qgs+Qgd;
    I(d,s) <+ 1*Ids*W ;
    I(d) <+ ddt(-1*Qgd);
    I(s) <+ ddt(-1*Qgs);
    I(g) <+ ddt(Qg);
 end
end

end
endmodule
```

Fig. 4.16: Look up table format (left) and Verilog-A code for symbol creation (right).

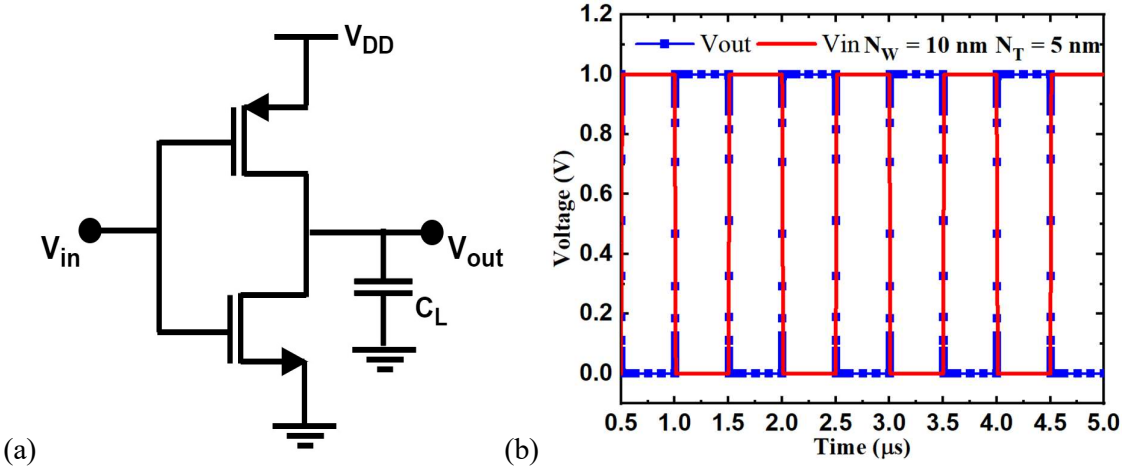


Fig. 4.17: (a) Inverter schematic diagram (b) transient response of inverter for N_W = 10 nm and N_T = 5 nm.

Fig. 4.17(a) depicts the schematic of the inverter diagram. In the inverter diagram, V_{DD} is the supply voltage, V_{in} and V_{out} are the input and output voltages, respectively. The transient response for N_W of 10 nm is shown in Fig. 4.17(b). For digital applications, it is important to evaluate the parameters like propagation delay (τ_P), energy delay product (EDP), switching current and noise margins to estimate the digital performance of the device. For the designed inverter, these parameters are calculated and compared the performance variations for N_W of 10 nm and 50 nm at a constant N_T of 5 nm.

Various transient and dc responses of the inverter are simulated using Cadence Virtuoso platform. The load capacitance C_L is taken as the sum of C_{gg} of both N-NSFET and P-NSFET [73]. The transient response of the inverter is shown in Fig. 4.17(b) for the time of 5 μs.

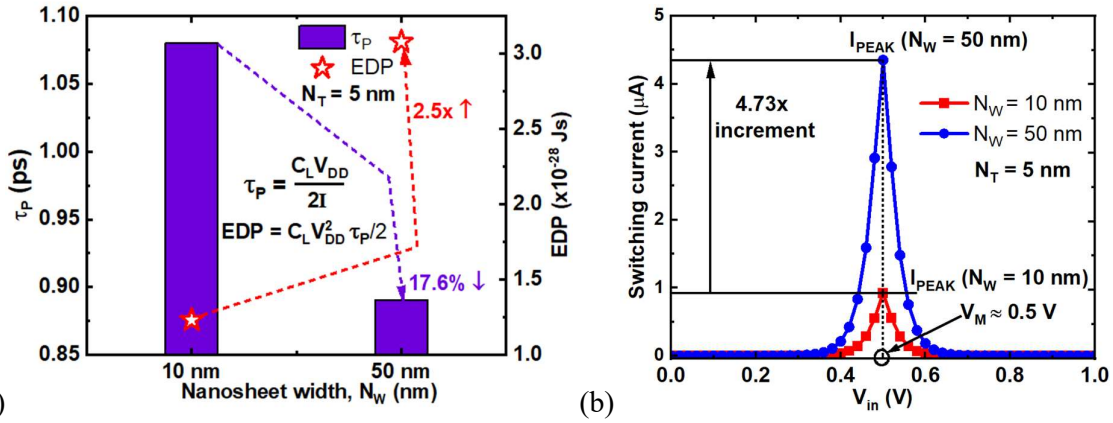


Fig. 4.18: (a) Propagation delay (τ_P), EDP and (b) Switching current of inverter for different N_W at constant N_T of 5 nm.

Fig. 4.18(a) shows the propagation delay of the inverter for N_W of 10 nm and 50 nm. The overall propagation delay (τ_P) obtained by considering the formula shown in Fig. 4.18(a) [72]. Where C_L is the load capacitance, I is the average current in the circuit. As τ_P α C_L × (1/I_{ON} (N-NSFET) + 1/I_{ON} (P-NSFET)), with the increment in N_W, both I and C_L will increase. However, the relative increment in I is higher compared to that of C_L and causes decrement in τ_P. From the result analysis, it is noticed that as the N_W increases from lower to upper bound, the τ_p decreased by 37%. Fig. 4.18(a) also shows EDP of the inverter for different N_W values. An increment of 2.5x is noticed in EDP as the N_W increases towards its upper bound.

Fig. 4.18(b) depicts the switching current (I_{SC}) of inverters for N_W values 10 nm and 50 nm. The inverter with higher N_W is delivering more switching current and an increment of 4.73× is observed in peak switching current with N_W of 50 nm. Also, the static current (at V_{in} = 0 V, V_{in} = V_{DD}) is less than 10 pA and offers much lower static power dissipation and energy efficient. Moreover, the switching threshold (V_M), which is the point where V_{in} = V_{out} is much closer to ideal value which is 0.5 V.

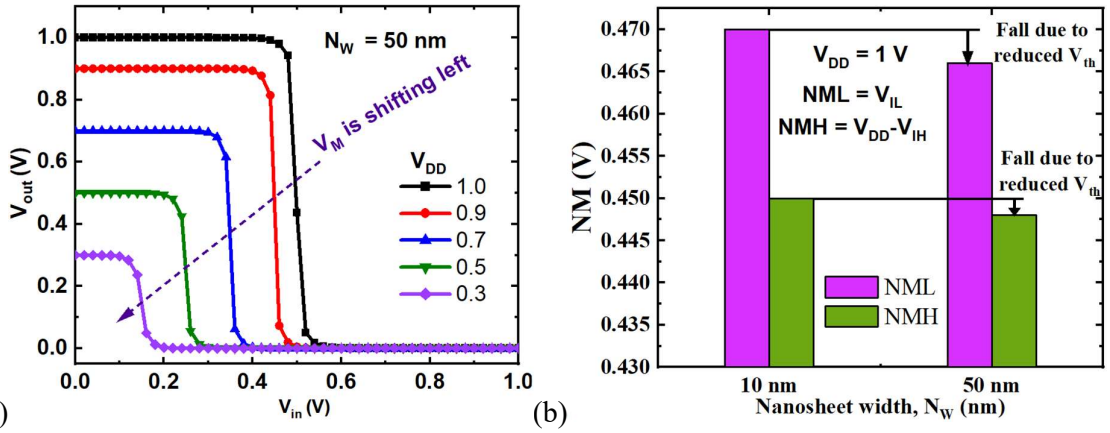


Fig. 4.19: (a) Transfer characteristics of inverter for various V_{DD} values (b) NM as a function of N_W at V_{DD} = 1 V.

Fig. 4.19(a) shows the DC response for various supply voltages (V_{DD}) for N_W of 50 nm. It is noticed that as the V_{DD} is decreasing, the V_M is shifting towards the left and affecting the switching characteristics. Fig. 4.19(b) shows the noise margins (NM) for different nanosheet widths. The noise margin low (NML) and noise margin high (NMH) are calculated using the formulas shown in Fig. 4.19(b). V_{IL} and V_{OH} are the input voltages where the gain of inverter (dV_{out}/dV_{in}) = -1 [121]. It is found that the NM followed the threshold voltage and gets

decrement with raise in N_W. Also, the noise margin is higher than its ideal value ($V_{DD}/2$) by 83% for N_W of 50 nm which is good for static logic applications [122].

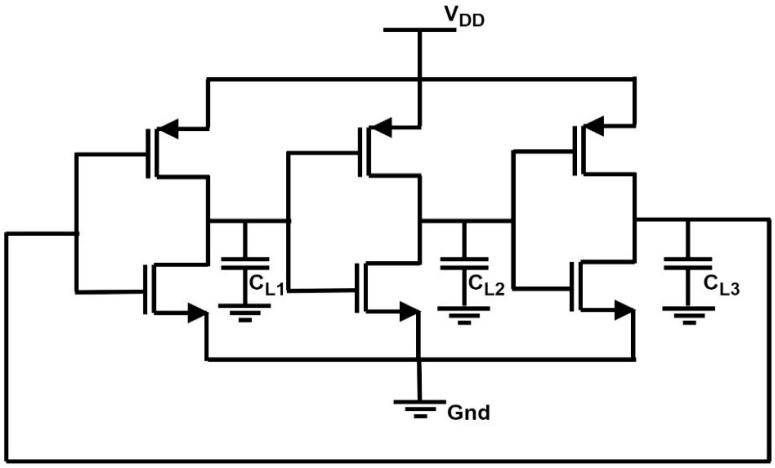


Fig. 4.20: 3- stage ring oscillator (RO).

Fig. 4.20 shows the 3-stage Ring oscillator (RO) in which all the load capacitances are assumed as same. Initially, an input of '0' V was forced to initiate the oscillations.

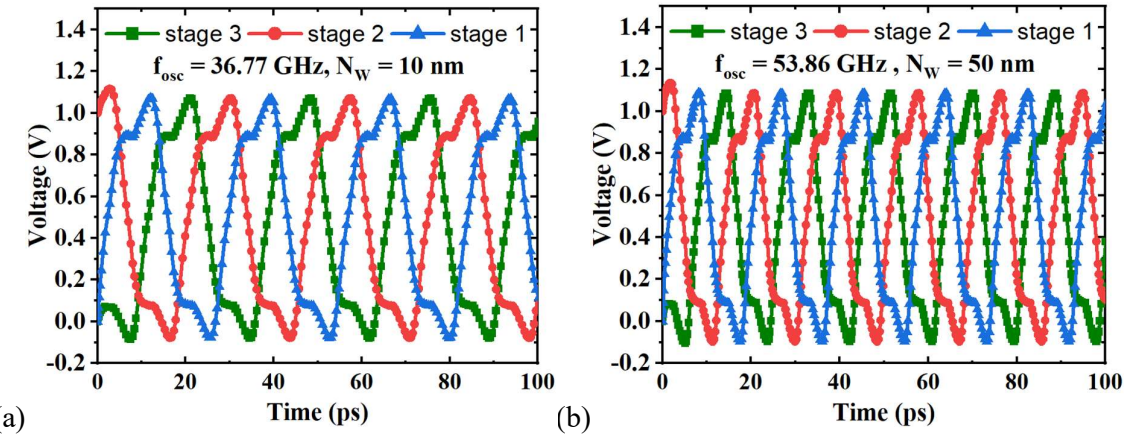


Fig. 4.21: 3- stage ring oscillator transient response for (a) N_W of 10 nm and (b) N_W of 50 nm.

From Fig. 4.21(a) and (b), it is observed that the frequency of oscillations (f_{osc}) is increasing with the width of nanosheet. As the τ_p decreases with the increment in N_W, the f_{osc} increases with width. There is an increment of 46.5% is observed for N_W increment from 10 nm to 50 nm due to higher I_{ON}. As a result of the foregoing research, greater widths assure device flexibility for high-speed applications. The comparison of f_{osc} with existing literature is shown in Table. 4.3.

Reference	Number of stages	f_{osc} (GHz)	Technology node
[123]	3	52.44	22
[124]	3	6.02	90
[125]	3	41.10	30
[126]	3	2.45	180
[127]	9	9	50
This work (N_W = 10 nm)	3	36.77	5
This work (N_W = 50 nm)	3	53.86	5

Table. 4.3: Comparison of f_{osc} with existing literature

In this chapter, the DC and analog/RF performance of NSFETs is investigated in this research by altering the geometry of each nanosheet at 5 nm technology node. As the N_T and N_W are raised, there is an increase in both I_{ON} and I_{OFF}. The optimum values for switching ratio, DIBL, and SS are obtained for lower values of N_W and N_T. However, analog/RF FOMs like g_m, g_{ds}, f_T, TFP, and GBW are more for higher N_W and N_T values of NS. These results will give an understanding of DC and analog/RF performance of NSFET with geometrical variations of the device. Moreover, the circuit performance assessed for circuits like inverter and 3-stage RO and found that with the increment in width, the propagation delay gets decremented and f_{osc} increases. These results will give performance insights of GAA NSFET at both device level and circuit level.

4.4. Conclusion

1. As the N_T and N_W are raised, there is an increase in both I_{ON} and I_{OFF}. The optimum values for switching ratio, DIBL, and SS are obtained for lower values of N_W and N_T.

2. Analog/RF FOMs like g_m, g_{ds}, f_T, TFP, and GBW are more for higher N_W and N_T values of NS.

3.The circuit performance assessed for circuits like inverter and 3-stage RO and found that with the increment in width, the propagation delay gets decremented and f_{osc} increases. Thus, the results will give performance insights into GAA NSFET at both device level and circuit level.

Chapter-5

Temperature Assessment of Nanosheet FET for CMOS Circuit Applications

5.1 Introduction

Temperature has a huge impact on the performance of nanoscale devices as they are very much sensitive to thermal variations. Due to a variety of electronic applications in industries such as military, automotive, nuclear, satellite communication, space, infrared detectors, and terrestrial systems that are extremely temperature dependent, it is highly essential to analyse the device's behaviour at elevated temperatures. The fundamental building elements in the majority of the aforementioned applications are logic gates and analog circuits. As the transistor is the building block of any circuit, the performance of the circuit also varies significantly owing to the variations at the device level. This contribution assesses and compares the NSFET performance at elevated temperatures ranging from 25^0C to 200^0C with high-*k* gate stack. Section 5.2 presents the device dimension details. The result analysis of section 5.3.1 presents the impact of temperature on DC and analog/RF performance with variations in temperature. Section 5.3.2 deals with the circuit performance variations at different temperatures.

5.2. Device Structure and Simulation Methodology

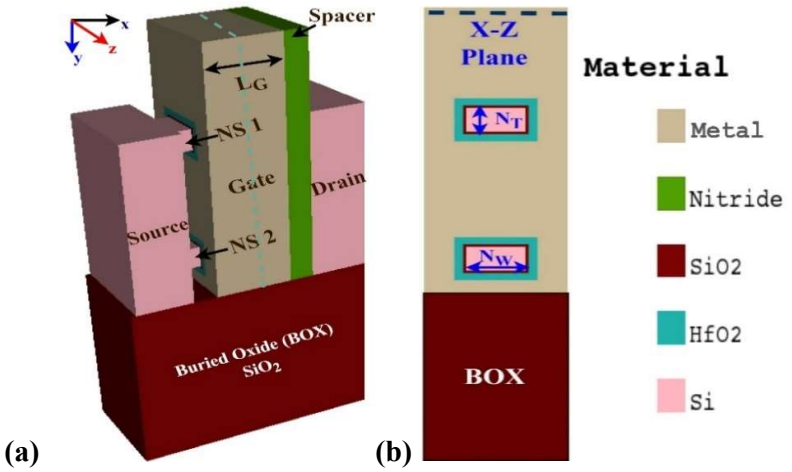


Fig 5.1: (a) 3-D view of NSFET representing stacked nanosheets, (b) 2-D cross-section view of NSFET.

Figure 5.1(a) and (b) depict the 3D and 2D schematic views of NSFET along with the materials used. Various device parameters used for NSFET are depicted in Table. 5.1. The calibration of the device is performed as given in section 3.2.

Parameter	NSFET
Gate length (nm)	16
Source/Drain length (nm)	12
Nanosheet width (nm)	10
Nanosheet thickness (nm)	5
Source/Drain doping (cm^{-3})	10^{19} (donor)
Channel doping (cm^{-3})	10^{15} (acceptor)
Work function (eV)	4.5159
EOT (nm)	0.78
Spacer length (nm)	5
Effective width (nm)	60
Temperature	25^0C -200^0C

Table. 5.1: Design parameters for NSFET.

5.3. Results and Conclusions

5.3.1 Impact of Temperature on DC and Analog/RF Metrics of NSFET

This section describes the various SCEs and transfer characteristics of the two stack nanosheet FET with temperature variations from 25^0C to 200^0C. The impact of temperature is studied on various crucial DC metrics like off current (I_{OFF}), on current (I_{ON}), switching ratio, DIBL, threshold voltage (V_{th}) and SS.

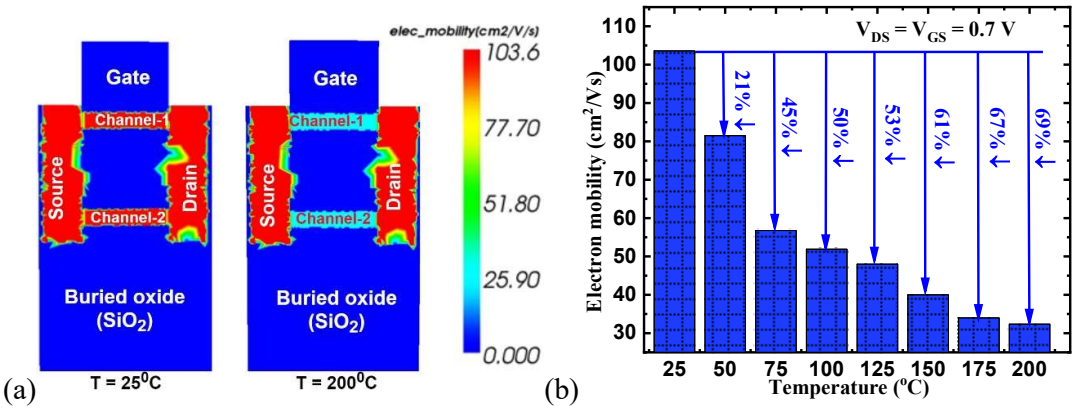


Fig. 5.2:(a) Contour plot for electron mobility of NSFET at 25^{0}C and 200^{0}C and (b) electron mobility at different temperatures.

Fig. 5.2 (a) depicts contour plots of the electron mobilities of NSFET at 25^{0}C and 200^{0}C. Also, Fig. 5.2 (b) depicts the relation between temperature and mobility for different temperatures. It can be observed that as temperature increases its highest bound, the mobility gets degraded severely due to scattering phenomena [54], [128]. The highest fall of 69% was observed for electron mobility as temperature increased from 25^{0}C and 200^{0}C.

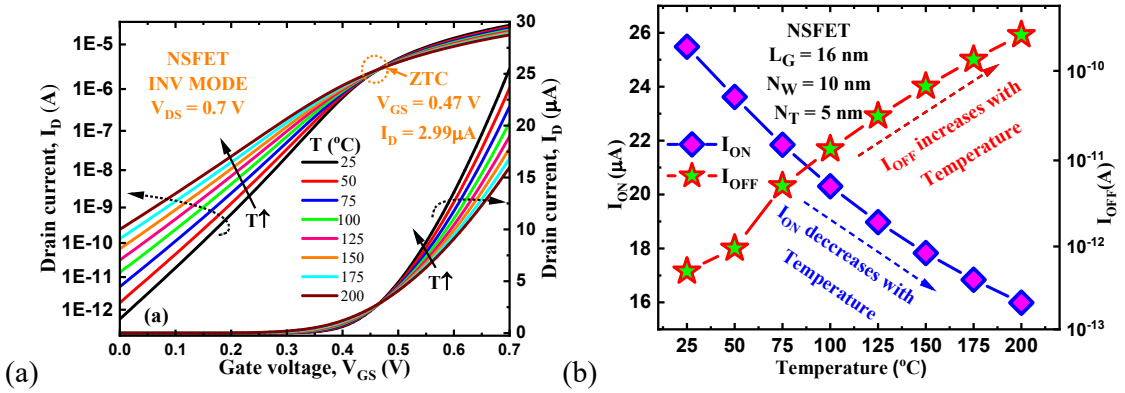


Fig. 5.3: (a) Transfer characteristics and (b) I_{ON} and I_{OFF} of NSFET at different temperatures.

Fig. 5.3(a) depicts the I_D-V_{GS} characteristics NSFET for various temperatures at V_{DS} = 0.7 V. The relation between temperature and drain current is given in [129], and is shown in equation 5.1.

$$I_D(t) \approx \mu(T)[V_{GS} - V_{th}(T)] \qquad (5.1)$$

The mobility term (μ) is deteriorated at high temperatures and causes a reduction in on current. However, the term (V_{GS}-V_{th}) improves since V_{th} decreases as temperature increases. The opposite effects of these two dependent factors are neutralized at a certain voltage, called zero

temperature coefficient (ZTC) or temperature compensation point (TCP), and is used in IC applications. At this point, the drain current is the same and is independent of variations in temperature [130]. This point is very much required to avoid the disadvantageous effects of temperature on the performance of the device. The TCP is identified at V_{GS} = 0.47 V and I_D = 2.99 µA.

Fig. 5.3(b) depicts variations in I_{ON} and I_{OFF} with respect to temperature. As temperature increases, the phonon scattering phenomena and lattice vibration play the dominant role and decreases the on current. The increment in I_{OFF} is mainly due to the increment in intrinsic carrier concentration (n_i), which causes to rise in both generation and diffusion currents [54].

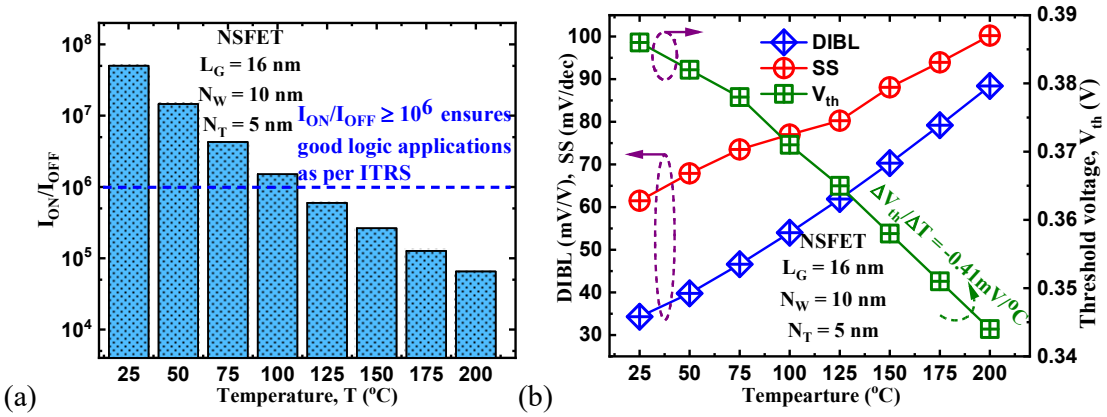


Fig. 5.4: (a) I_{ON}/I_{OFF} (b) SS, DIBL and V_{th} of NSFET at different temperatures.

Fig. 5.4(a) depicts the I_{ON}/I_{OFF} values at different temperatures. It is observed that as temperature increases, I_{ON}/I_{OFF} tends to fall due to the increment in off-state current, I_{OFF}. Fig. 5(b) depict SS, DIBL and V_{th} values at different temperatures. According to the constant current method, V_{th} extracted at W_{eff}/L_G $\times 10^{-7}$ A. Where W_{eff} is the number of stacked nanosheets multiplied by the perimeter of the nanosheet. It is noticed that as temperature rises, a fall in V_{th} is observed and found that dV_{th}/dT is -0.41mV/°C as shown in Fig. 5.4(b).

Subthreshold swing (SS), gives the value of the required change in gate voltage to get a change of one decade in drain current. To evaluate device performance towards low power applications, SS acts as one of the critical metrics [98]. For optimum subthreshold behaviour, the lowest SS values are required. Fig. 5.4(b) shows variations of SS as a function of temperature, which is varied from 25^{0}C to 200^{0}C. The SS tends to increase with the rise in temperature due to the increment in I_{OFF}. An increment of 63% in SS is noticed when the temperature increases towards its upper bound. At high temperatures, the degradation in subthreshold performance is noticed.

Drain induced barrier lowering (DIBL) is another crucial metric of short channel performance, and for the transistor to function well in the subthreshold region, minimum DIBL values are recommended. Fig. 5.4(b) depicts DIBL variations for various temperatures. It is observed that DIBL values are increasing with rise in temperature due to the degradation of leakage currents. An increment of 2.6x is noticed for DIBL when temperature increases towards 200^0C.

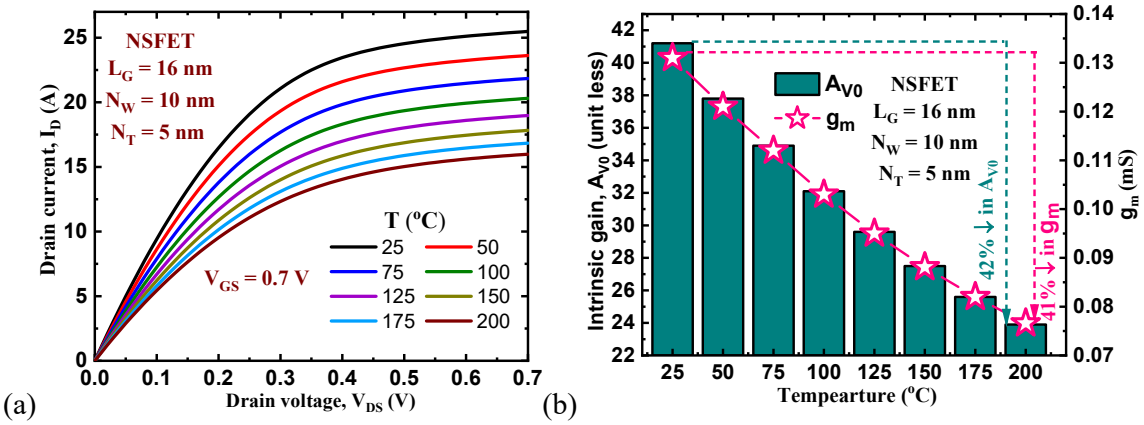


Fig. 5.5: (a) Output characteristics and (b) A_{v0} and g_m of NSFET with temperature.

Fig. 5.5(a) shows the drain characteristics at different temperatures. Further, as temperature increases, the drain current tends to degrade because of scattering phenomena. The intrinsic gain (A_{v0}) and transconductance (g_m) are depicted in Fig. 5.5(b). The g_m is calculated by taking the derivate of drain current with respect to gate voltage, i.e., $g_m = \frac{\partial I_D}{\partial V_{GS}}$ [131]. Also, the intrinsic gain is calculated using the formula $A_{V0} = \frac{g_m}{g_d}$ [132]. Both A_{v0} and g_m are degraded with respect to temperature due to the degradation of on current. Moreover, the deterioration of 42% and 41% in A_{v0} and g_m are noticed, respectively, as the temperature increases from 25^0C to 200^0C.

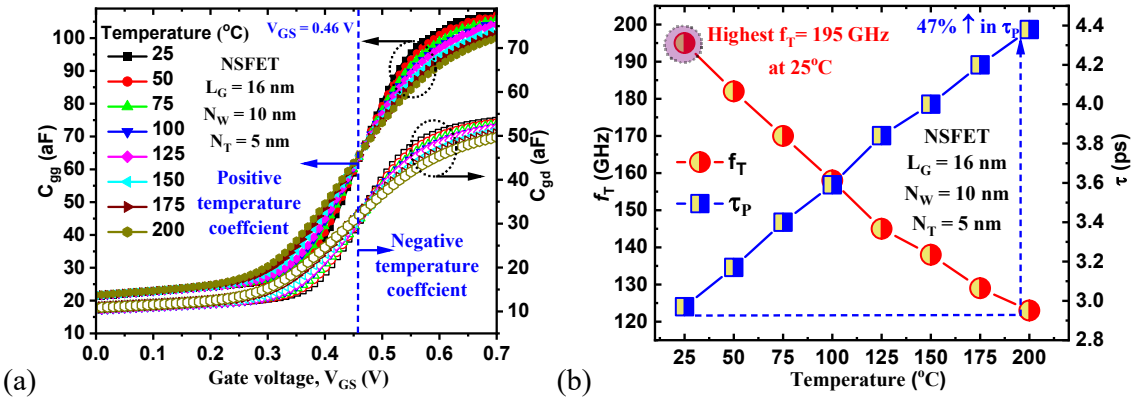


Fig. 5.6: (a) C_{gg}, C_{gd} (b) cut-off frequency (f_T), intrinsic delay (τ) of NSFET at various temperatures.

The C_{gd} and C_{gg} of NSFET are shown in Fig. 5.6(a) for different temperatures. With the rise in gate voltage, the capacitance values are increased. Moreover, it is noticed that the capacitances have positive and negative temperature coefficients for lower and higher gate voltages, respectively. This might be explained by the fact that when the temperature rises, surface potential decreases. Fig. 5.6(b) depicts cut-off frequency (f_T) with temperatures ranging from 25^0C to 200^0C. The f_T is calculated using equation 4.3. It can be seen that the f_T is dependent on both g_m and gate capacitances [133]. With the rise in temperature, f_T tends to decrease and a decrement of 37% is noticed when temperature increases to 200^0C because of severe degradation in g_m.

Intrinsic delay (τ), is another crucial analog metric and which helpful in evaluating the device feasibility in practical SOC applications [117]. The τ is a function of gate capacitance, drive voltage and the drain current. Equation 4.4 is used to calculate the τ value. It is obvious that to have lower τ, lower C_{gg} values are preferred. Fig. 7(b) depicts intrinsic delay (τ) variations with temperature. An increment of 47% was observed in τ when the temperature increased to 200^0C due to the decrement of drain current with respect to temperature.

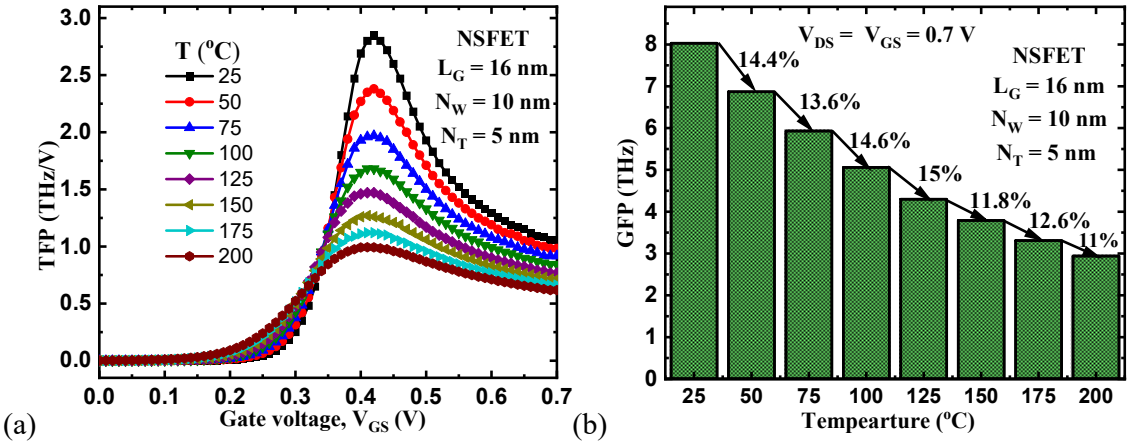


Fig. 5.7: (a) TFP and (b) GFP of NSFET at various temperatures.

Another significant analog/RF FOM is the transconductance frequency product (TFP) [97], which is derived using equation 4.5. TFP provides the trade-off between bandwidth and power and is employed in high- and medium-speed circuit applications. Fig. 5.7(a) depicts TFP as a function of temperature. As the temperature increases toward 200^0C, a decrement in TFP is observed. A decrement of 42% as temperature increases from 25^0C to 200^0C at V_{GS} = 0.7 V.

Gain frequency product (GFP), another significant analog/RF figure of merit, is calculated using equation 4.6. The performance of analog amplifier circuits in high frequency applications

is estimated using GFP [101], as shown in Fig. 5.7(b). As temperature increases, GFP tends to decrease, and a maximum decrement of 15% is observed when temperature increases from 100^0C to 125^0C. Also, a minimum change of 11% in GFP is observed when temperatures increase from 175^0C to 200^0C.

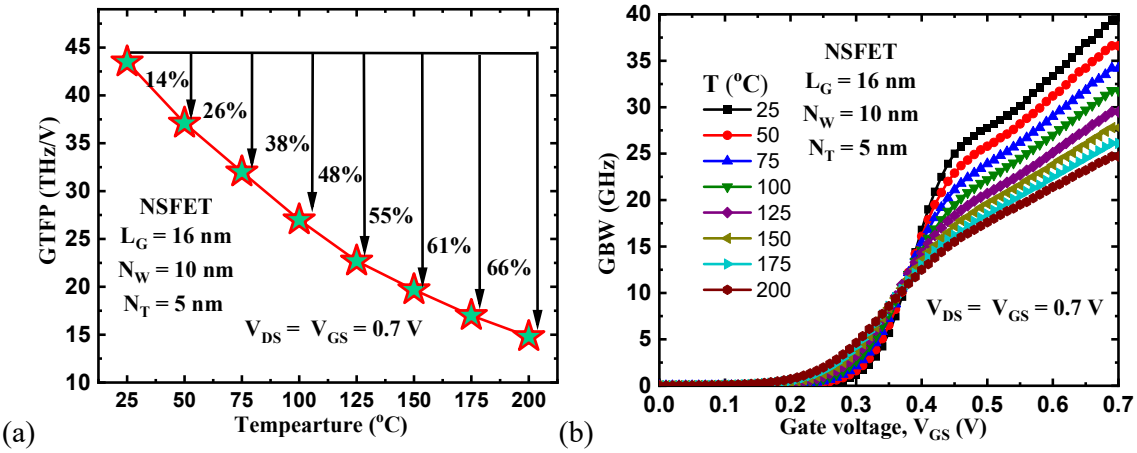


Fig. 5.8: (a) GTFP and (b) GBW of NSFET at various temperatures.

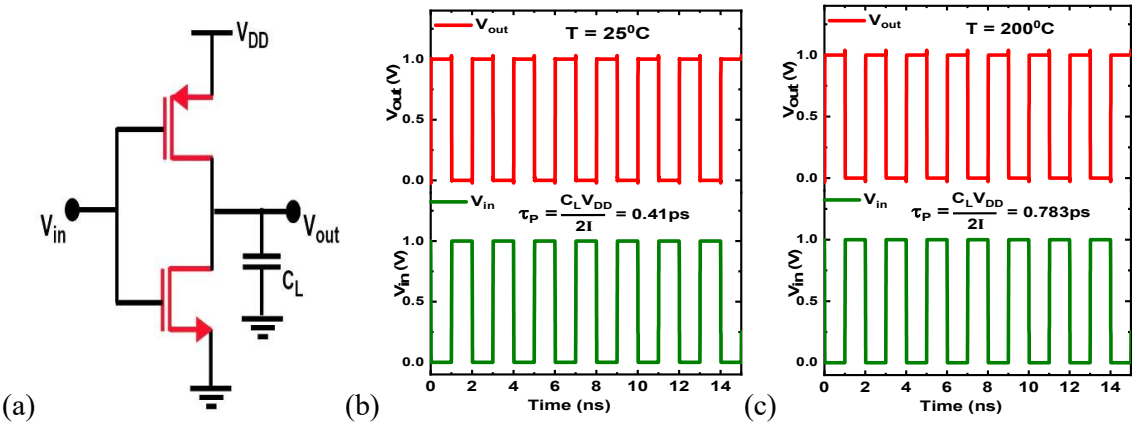
Gain transconductance frequency product (GTFP) is obtained by multiplying the TFP with gain. Moreover, GTFP enables designers the freedom to choose a zone where parameters like the device's g_m, delay, and A_{V0} can be traded off favourably [101]. GTFP is given by equation 4.7. For various temperatures, the GTFP is shown in Fig. 8(a). Due to the fall in A_{V0}, the GTFP tends to degrade with the rise in temperature. A maximum fall of 66% in GTFP is noticed as temperature increases from 25^0C to 200^0C.

Fig. 5.8(b) shows the GBW of NSFET at various temperatures and is calculated by using equation 4.8. The device's efficiency towards high-frequency circuits can be assessed using GBW. It is noticed that GBW tends to fall with a rise in temperature. Moreover, the GBW followed the g_m trend, which is obvious from equation 4.8. A decrement of 37% in GBW is observed when the temperature increases to 200^0C due to the decrement of transconductance with temperature.

5.3.2 Impact of Temperature on Circuit Applications

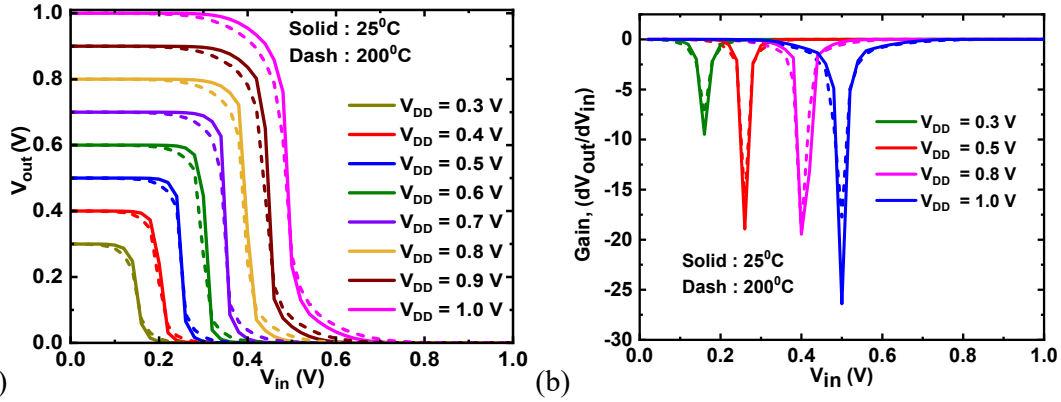
The impact of temperature on the CMOS inverter is studied in this section in detail. The circuit simulations are carried out using the Cadence platform [120] through the lookup table-based Verilog-A model, as given in section 4.3.2.

The schematic of CMOS inverter is depicted in Fig. 5.9(a). Where V_{DD} is the supply voltage, C_L is the load capacitance, V_{in} and V_{out} are the input and output voltages of the inverter, respectively. The transient responses at 25^{0}C and 200^{0}C are depicted in Fig. 5.9(b) and (c), respectively. The propagation delay (τ_P) of the inverter is calculated using the formula, $\tau_P = \frac{C_L V_{DD}}{2I}$ [72]. It is noticed that as the temperatures increase, the inverter propagation delay degrades. An increment of 91% in τ_P is noticed as the temperature increase from 25^{0}C to 200^{0}C.



(a) (b) (c)

Fig. 5.9: (a) Schematic of the inverter, transient response of inverter at (b) T = 25^{0}C and (c) T = 200^{0}C.



(a) (b)

Fig. 5.10: (a) Output characteristics of inverter at different temperatures and (b) Gain of the inverter at 25^{0}C and 200^{0}C.

The output characteristics of the inverter at various supply voltages are shown in Fig. 5.10(a). It is observed that as temperature increases, the output characteristics tend to degrade due to the degradation of on current. Further, the gain (dV_{out}/dV_{in}) of the inverter is depicted in Fig. 5.10(b) at various V_{DD}. It is noticed that the gain of the inverter deteriorates as the temperature increases

towards 200^{0}C due to the reduction in mobility at high temperatures. Furthermore, the gain degraded by 49% from 25^{0}C and 200^{0}C at V_{DD} = 1 V.

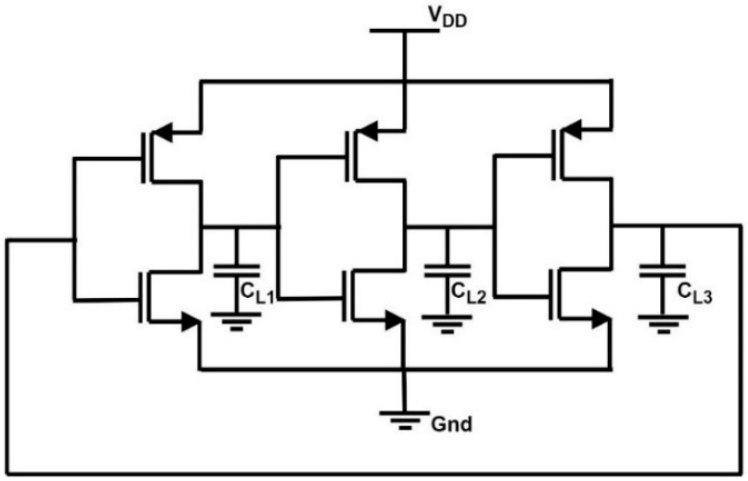


Fig. 5.11: Schematic of the 3-stage ring oscillator.

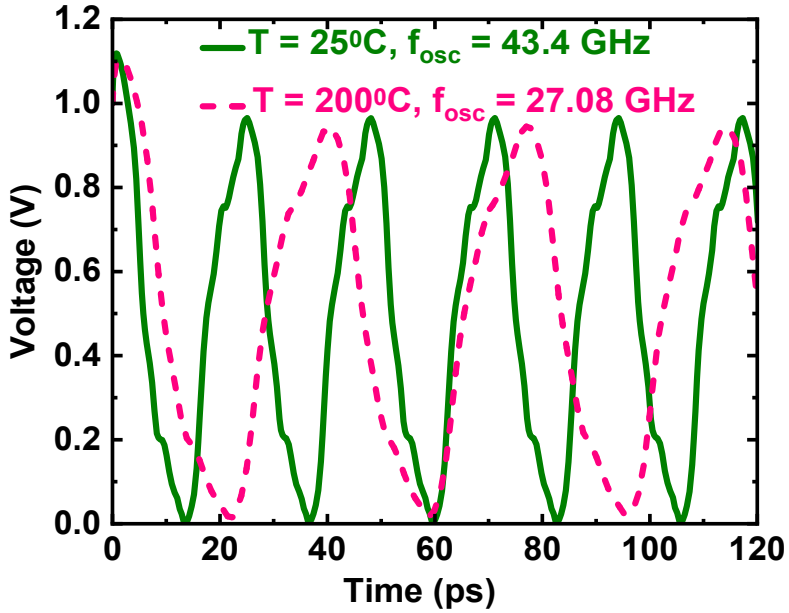


Fig. 5.12: Transient response of RO at 25^{0}C and 200^{0}C.

Three-stage ring oscillator (RO) is shown in Fig. 5.11, where it is assumed that all load capacitances are equal. In the CADENCE simulator, '0' V was initially forced to start the oscillations. The transient response of RO is depicted in Fig. 5.12 at V_{DD} = 1 V. As the temperatures increases, degradation of the oscillation frequency (f_{osc}) is noticed. At 25^{0}C, the f_{osc} is 43.4 GHz, whereas the f_{osc} deteriorated to 27.08 GHz at 200^{0}C. The results will give deep insights into the performance of NSFET at elevated temperatures.

In this chapter, the DC and analog/RF performance analysis of 3D vertically stacked NSFET is analyzed at elevated temperatures from 25ºC to 200ºC. It is observed that with the increment in temperature, deterioration in I_{ON} is observed due to the mobility reduction. Also, the I_{ON}/I_{OFF}, SS and DIBL are degraded with increment in temperature. Moreover, analog/RF FOMs comparison is presented with variations in temperature. With the rise in temperature, analog/RF FOMs like g_m, A_{V0}, f_T, GBW, GFP, GTFP and TFP have deteriorated. Further, the CMOS inverter and ring oscillator performance analysis was presented at different temperatures using the Verilog-A model. As the temperature increases, the propagation delay and gain of the inverter are degraded and offer less performance. Also, the oscillation frequency of ring oscillator degraded as temperatures increased to 200^0C. These results will give deep understanding of the performance of NSFET at both device and circuit levels at elevated temperatures.

5.4. Conclusion

1. It is observed that with the increment in temperature, deterioration in I_{ON} is observed due to the mobility reduction. Also, the I_{ON}/I_{OFF}, SS and DIBL are degraded with increment in temperature.

2. Analog/RF FOMs comparison is presented with variations in temperature. With the rise in temperature, analog/RF FOMs like g_m, A_{V0}, f_T, GBW, GFP, GTFP and TFP have deteriorated.

As the temperature increases, the propagation delay and gain of the inverter are degraded and offer less performance. Also, the oscillation frequency of the ring oscillator degraded as temperatures increased to 200^0C.

Chapter-6

A Comprehensive Analysis and Performance Comparison of CombFET and NSFET for CMOS Circuit Applications

6.1 Introduction

In previous chapters, the NSFET design and its performance at both device and circuit levels were demonstrated. As it can be seen that the NSFET offers more electrostatic integrity over the channel since the gate covers the channel in all directions. NSFETs can be fabricated by making minimal changes to the existing FinFET fabrication technology, and patterning difficulties related to lower technology nodes can be reduced. Under the same footprint (FP), a substantial boost in performance is achieved through NSFET compared to FinFET by offering a better W_{eff}/C_{eff} trade-off and good electrostatics. Moreover, it is shown that by varying the nanosheet width, the power performance trade-offs in logic can be optimized. This can be achieved by fine tuning of NS width, which is enabled by the Extreme Ultraviolet Lithography (EUV) process. Also, 30% more W_{eff} can be achieved by using stacked NSs compared to FinFET under the same FP.

However, to continue the scaling, the effective area (W_{eff}) per footprint (FP) (W_{eff}/FP), needs to be reduced, which affects the performance of the device with scaling. Thus, there is a need to improve the device's on current without increasing the FP by using device engineering such as structural engineering and high-k gate stack engineering.

This chapter proposes a modified NSFET to enhance the drive current for sub-5 nm technology nodes. The modification is done to the existing NSFET by implementing the Fin-shaped inter bridge between the NSFET channels which is also known as comb-like channel field effect transistor (CombFET). To enhance the performance further, high-*k* gate stack is implemented to CombFET, which none has explored yet. The performance of CombFET and nanosheet FET (NSFET) is addressed at both device and circuit levels at the 5-nm node with the high-k gate stack.

6.2 Device Structure and Simulation Parameters

The NSFET and CombFET devices are designed according to International Roadmap for Devices and Systems (IRDS). The gate length of 16 nm and spacer length of 8 nm were

considered according to IRDS criteria [134]. The device structures of both NSFET and CombFET are shown in Fig. 6.1. The process flow of CombFET is depicted in Fig. 6.2. Initially, the bulk silicon wafer is considered, and SiGe/Si epitaxy is formed. Further, the IB is formed by spacer defined Fin patterning through Fin side selective epitaxy [75]. After that, the second SiGe epitaxy is formed, followed by chemical mechanical polishing (CMP) and the second Si epitaxy. Hence, the IB is created between the two NSs. The Comb teeth are supported by the fin side of CombFET. After that, the dummy gate, spacer formation and source/drain deposition is done. The SiGe sacrificial layers are removed, and the process ends with the back end of line (BEOL) process. The device's geometrical parameters and their dimensions are presented in Table 6.1. The calibration of TCAD is performed as given in section 3.2.

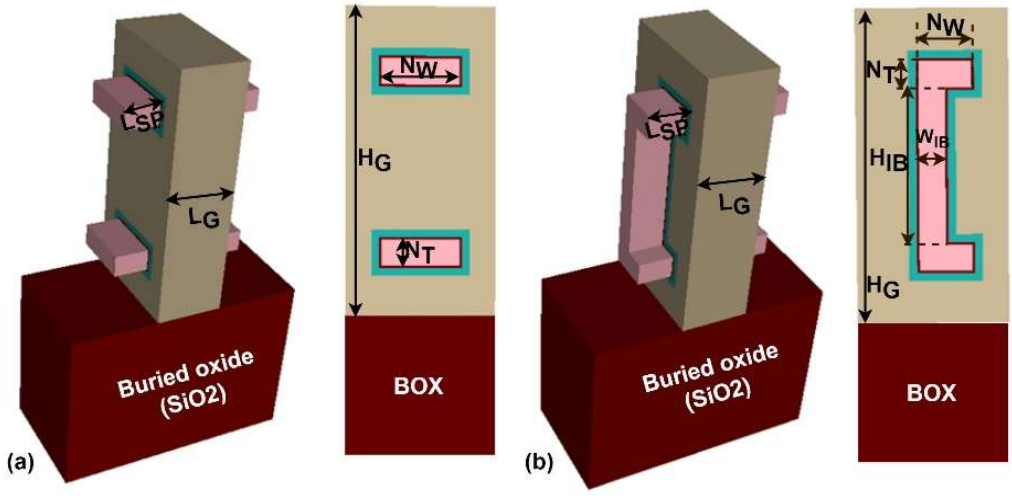


Fig. 6.1: 3-D and 2-D cross-sectional views of (a) NSFET and (b) CombFET.

Fig. 6.2: Process Flow of CombFET [75], [135].

Device parameter	NSFET	CombFET
Gate Length (L_G)	16 nm	16 nm
N_W	15 nm	10 nm
N_T	5 nm	5 nm
Width of Interbridge (W_{IB})	-	5-9 nm
Height of Interbridge (H_{IB})	-	10-30 nm
EOT	0.78 nm	0.78 nm
Spacer dielectric	Nitride	Nitride
Length of spacer	8 nm	8 nm
Source/drain doping	1×10^{20} cm^{-3}	1×10^{20} cm^{-3}
Channel doping	1×10^{15} cm^{-3}	1×10^{15} cm^{-3}
Gate work function	4.346 eV	4.367 eV

Table. 6.1 Device Parameters.

6.3 Results and Conclusions

6.3.1 DC and analog/RF FOMs Analysis of both NSFET and CombFET

In this section, the detailed DC and analog/RF performance comparison for both NSFET and CombFET has been made in this section. The DC performance metrics like ON current (I_{ON}), subthreshold swing (SS), drain induced barrier lowering (DIBL) are discussed. Further, the crucial analog metrics like transconductance (g_m), transconductance generation factor (TGF), output conductance (g_{ds}), intrinsic gain (g_m/g_{ds}), cut-off frequency (f_T), and intrinsic delay (τ_P) are discussed.

Fig. 6.3 depicts the various contour plots for both NSFET and CombFETs. The higher electron mobility is observed in the channel region for both FETs, as seen in Fig. 6.3(a). The contour plots for potential along the lateral direction are shown in Fig. 6.3(b). The higher potential is noticed at the drain end for both FETS due to the applied drain voltage [98]. For CombFET, slightly higher potential was observed in the channel region compared to the NSFET because of more charge density in the channel region [135]. The electric field variations in the vertical cross-sectional view are shown in Fig. 6.3(c). Compared to NSFET, the more electric field is

noticed in CombFET. The larger E filed resulted in CombFET because of more charges in the channel region [135].

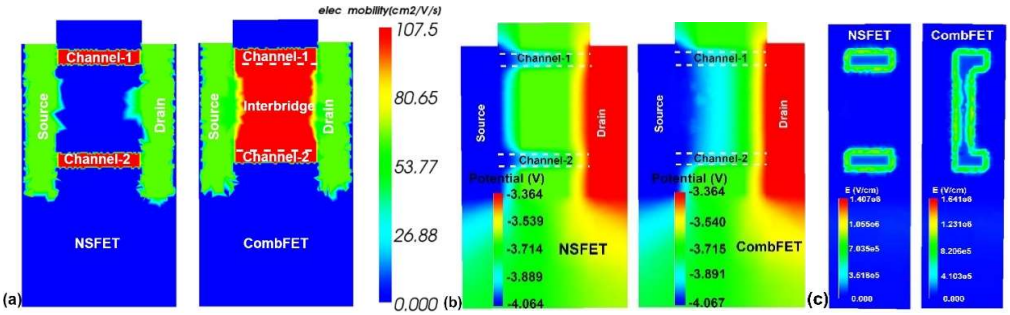


Fig. 6.3: Contour plots of both NSFET and CombFET for (a) electron mobility, (b) potential, and (c) electric field in ON state.

Fig. 6.4(a) depicts the transfer characteristics at various drain voltages for both NSFET and CombFET. For a reasonable assessment of both FETs, the I_{OFF} is matched at 250 pA [136]. It can be noticed that the ON current is significantly higher for CombFET than NSFET. As the more effective width can be achieved at the same footprint, the CombFET offers more ON current compared to NSFET. Fig. 6.4(b) depicts output characteristics at different gate voltages for both NSFET and CombFET. Evidentially, the I_D decreases as the gate voltage decreases. Moreover, CombFET offers more drain current compared to NSFET.

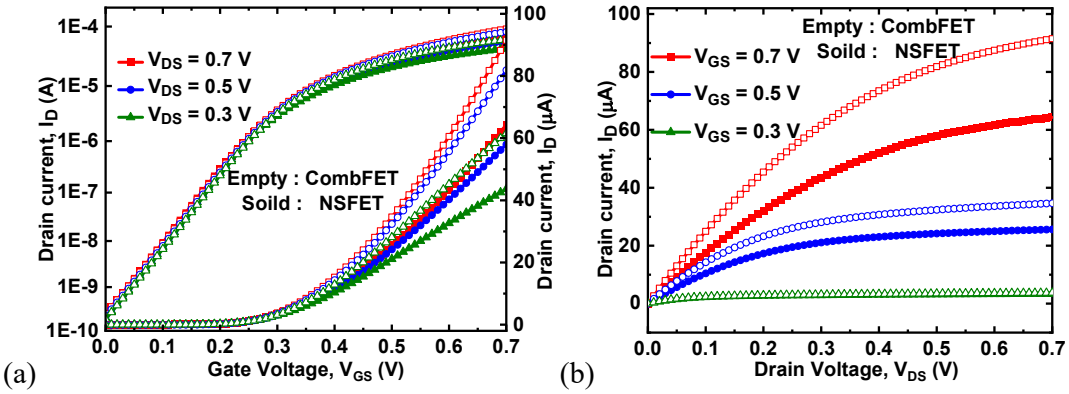


Fig. 6.4: (a) I_D-V_{GS} and (b) I_D-V_{DS} for both NSFET and CombFET at different voltages.

The SS, DIBL and I_{ON} values are depicted in Fig. 6.5(a). It is noticed that DIBL and SS values are slightly higher for CombFET than NSFET. The SS degrades slightly due to the lower area-volume ratio in the channel area, which reduces the electrostatic integrity of the gate marginally. Further, the increment in DIBL is owing to the fact that the gate control is less in the IB area because of the trade-off between gate controllability and the tunneling area [135]. There is an

increment of 1.2% and 3.7% noticed in SS and DIBL from NSFET to CombFET at the same OFF current. The I_{ON} is calculated at $V_{DS} = V_{GS} = 0.7$ V. An increment of 42% was observed in I_{ON} from NSFET to CombFET due to the presence of the IB.

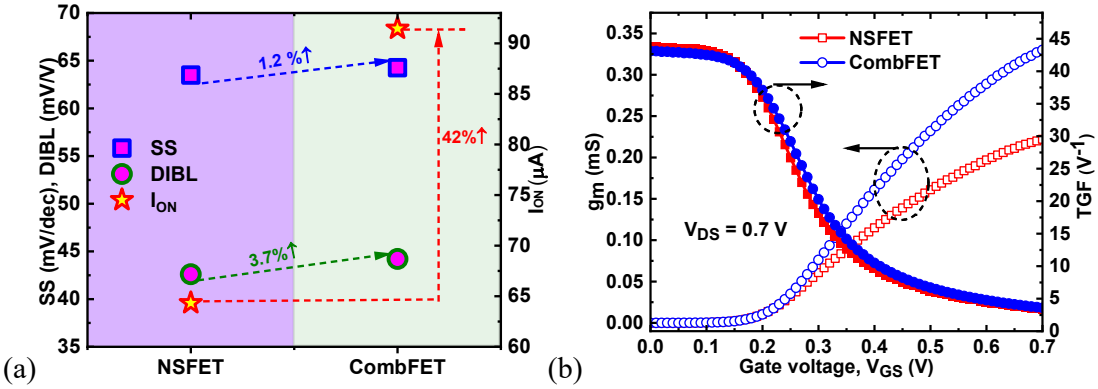


Fig. 6.5: (a) SS, DIBL and I_{ON}, (b) g_m and TGF for both NSFET and CombFET.

Transconductance ($g_m = \frac{\partial I_D}{\partial V_{GS}}$) is a crucial metric to assess the speed of the device. Higher g_m values are preferred for the device to use in high speed applications. Fig. 6.5(b) depicts the g_m for both FETs at $V_{DS} = 0.7$ V. The higher g_m is obtained for CombFET because of the high ON current. At $V_{DS} = V_{GS} = 0.7$ V, an increment of 1.5× in g_m is noticed from NSFET to CombFET. The transconductance generation factor (TGF = $\frac{g_m}{I_D}$) is another important metric, and it evaluates the optimum use of I_D to get the acceptable value of g_m. Also, to operate the device at lower voltages without compromising performance, greater TGF values are desirable [101]. The TGF is shown in Fig. 6.5(b). For both NSFET and CombFETs, almost similar TGF is observed. The TGF tends to degrade with the rise in V_{GS}, since the drain current gets saturated at higher gate voltages.

The output conductance ($g_{ds} = \frac{\partial I_D}{\partial V_{DS}}$) values of both FETs are depicted in Fig. 6.6(a). Lower g_{ds} values are favoured for better performance of the device [131]. The drain current should be invariant with the drain voltage in the saturation area. However, due to SCEs, the drain current modifies slightly with V_{DS}, and is measured using g_{ds} values. From Fig. 6.6(a), slightly lower g_{ds} values are obtained for NSFET compared to CombFET. The intrinsic gain ($A_{V0} = \frac{g_m}{g_{ds}}$) is another important analog metric and measures the device's amplification capability [133]. Fig 6.6(a) depicts the A_{V0} with V_{GS} for both NSFET and CombFET at $V_{GS} = 0.7$ V. The A_{V0} is marginally higher for NSFET due to the lower g_{ds}.

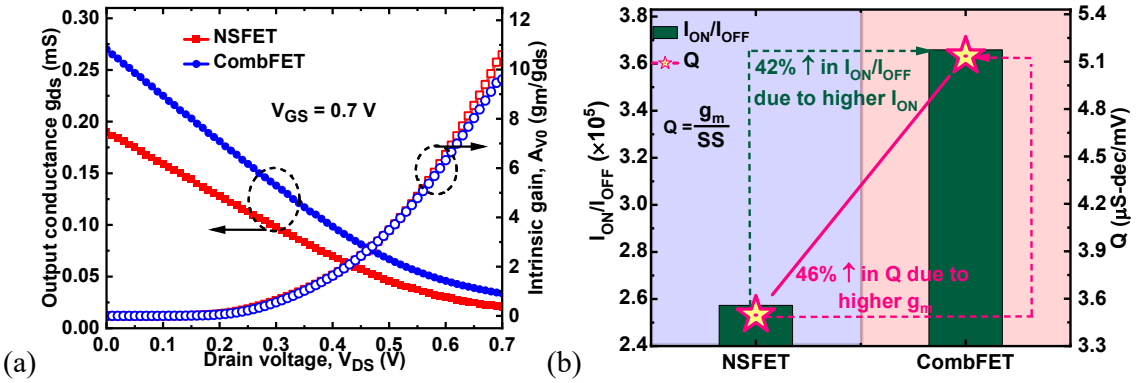


Fig. 6.6: (a) Output conductance (g_{ds}) and intrinsic gain (A_{V0}) (b) I_{ON}/I_{OFF} and Q for both NSFET and CombFET.

Fig. 6.6(b) depicts the switching ratio (I_{ON}/I_{OFF}) for both NSFET and CombFET at a fixed OFF current of 250 pA. It is observed that the switching ratio is more for CombFET compared to NSFET due to the higher I_{ON}. Also, a significant increment of 42% in I_{ON}/I_{OFF} is observed from NSFET to CombFET. Further, the ON-OFF performance metric, Q ($Q = \frac{g_m}{SS}$) is another important metric which estimates the device's performance by combining the effect of both analog and DC metrics [109]. The highest CombFET exhibits the highest Q values of 5.13 mS-dec/mV, which is 46% higher than NSFET. This superior performance in Q is obtained because of the high ON current for CombFET.

The gate to source capacitance (C_{gs}) and gate to drain capacitance (C_{gd}) are two essential parameters of the device. The C_{gd} is also known as feedback capacitance or miller capacitance. The capacitances are evaluated at the frequency of 1 MHz [97] and are shown in Fig. 6.7(a). Both C_{gs} and C_{gd} tend to increase with the rise in gate voltage. Also, compared to NSFET, CombFET exhibits higher capacitances due to the broader area of the channel. The total gate capacitance (C_{gg}), where $C_{gg} = C_{gd} + C_{gs}$, is another essential characteristic to measure analog/RF performance. The C_{gg} is also higher for CombFET than NSFET, as depicted in Fig. 6.7(b).

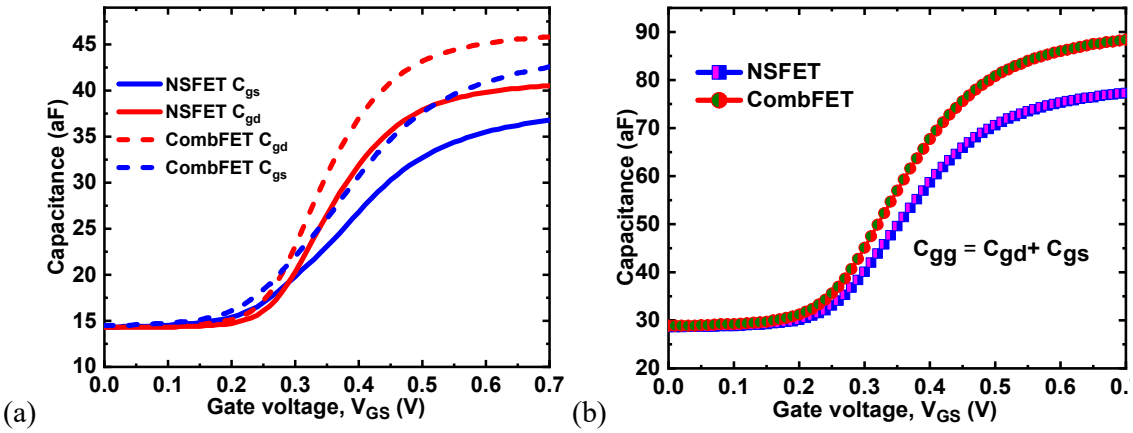


Fig. 6.7: (a) C_{gs}, C_{gd} and (b) C_{gg} for both NSFET and CombFET.

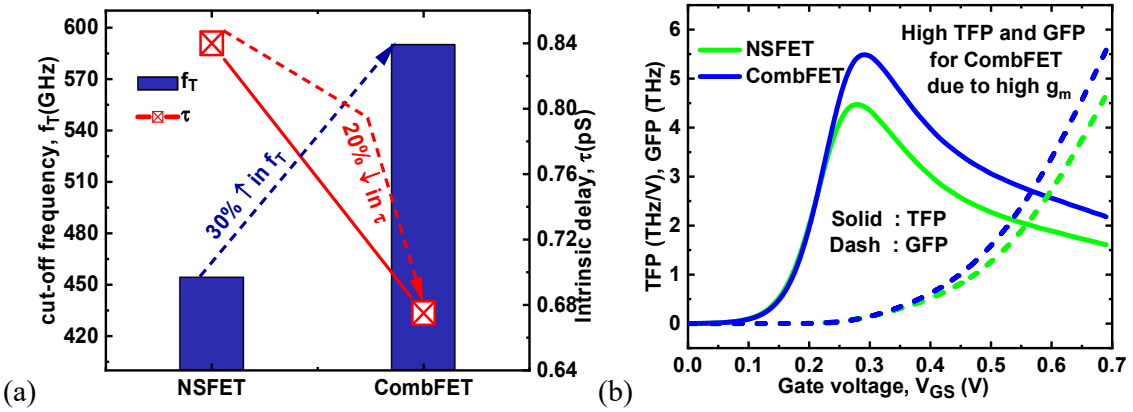


Fig. 6.8: (a) f_T and τ, and (b) TFP and GFP for both NSFET and CombFET.

The cut-off frequency ($f_T \approx \frac{g_m}{2\Pi(C_{gd}+C_{gs})}$) inherently gives the device's speed and is a significant parameter while characterizing the device in RF and microwave applications [137]. It is also termed as the frequency, where the short circuit current gain is one. Higher f_T values are preferred for high speed applications. Fig. 6.8(a) depicts the f_T values for both NSFET and CombFET at V_{GS} = 0.7 V. While moving from NSFET to CombFET, 30% more f_T is obtained due to the higher I_{ON}. Further, the intrinsic delay ($\tau = \frac{C_{gg}V_{DD}}{I_{ON}}$) is another critical metric that gives the device's delay performance [138]. The τ is dependent on total gate capacitance, supply voltage and ON current. Lower τ values are preferred for the optimum performance of the device. From Fig. 6.8(a), it can be seen that CombFET outperforms with a delay of 0.675ps and a delay decrement of 20% attained using CombFET compared to NSFET under the same FP.

Transconductance frequency product (TFP = $\frac{g_m}{I_D} \times f_T$) is another important metric and is used in high-speed applications [138]. The TFP inherently provides the relation between the

bandwidth and power of the device. TFP as a function of V_{GS} for both NSFET and CombFET is depicted in Fig. 6.8(b). The CombFET offers higher TFP than NSFET because of high f_T provided by CombFET. Further, the gain frequency product (GFP = $\frac{g_m}{g_{ds}} \times f_T$) is presented in Fig. 6.8(b). GFP [117] is widely used to measure the performance of high speed applications such as operational amplifiers. The CombFET exhibits higher GFP than NSFET due to the higher gain offered by CombFET.

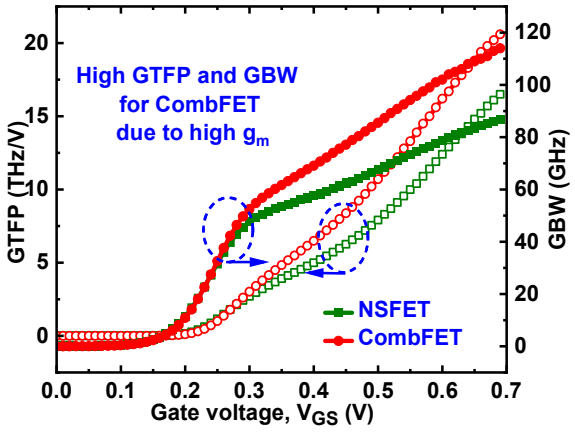


Fig. 6.9: GTFP and GBW for both NSFET and CombFET.

Fig. 6.9 depicts the gain transconductance frequency product (GTFP = $\frac{g_m}{g_{ds}} \times \frac{g_m}{I_D} \times f_T$), which is a very valuable metric for circuit designers. It offers the trade-off between gain, transconductance and speed of the device [117]. The CombFET exhibits higher GTFP than NSFET because of its high cut-off frequency and transconductance. Further, the gain bandwidth product (GBW = $\frac{g_m}{20\pi C_{gd}}$) is another crucial analog/RF metric, which is useful to assess the efficiency of the device in high speed applications [117]. The GBW for both NSFET and CombFET is shown in Fig. 6.9. The CombFET offers more GBW because of its higher g_m.

6.3.2 Impact of Interbridge Width (W_{IB}) on the Performance of CombFET

In this section, the W_{IB} is varied from 5 nm to 9 nm to evaluate the impact of W_{IB} on the performance of CombFET. The H_{IB} is considered as 30 nm and performed the simulations. Fig. 6.10 shows the I_D-V_{GS} characteristics in both linear and log scales with variations in W_{IB} at V_{DS} = 0.7 V. It is observed that with the rise in V_{GS}, the drain current tends to increase due to an increment in carrier density. Further, Fig. 6.10 (b) depicts the I_D-V_{DS} characteristics at V_{GS} = 0.7 V. The drain current tends to rise with an increment in drain voltage, as seen in Fig. 6.10 (b).

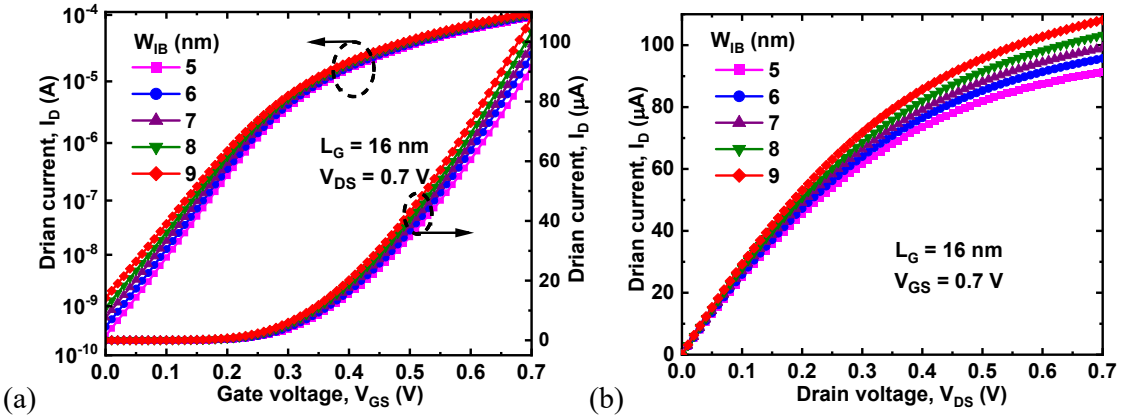


Fig. 6.10: (a) I_D-V_{GS} and (b) I_D-V_{DS} for various W_{IB} values.

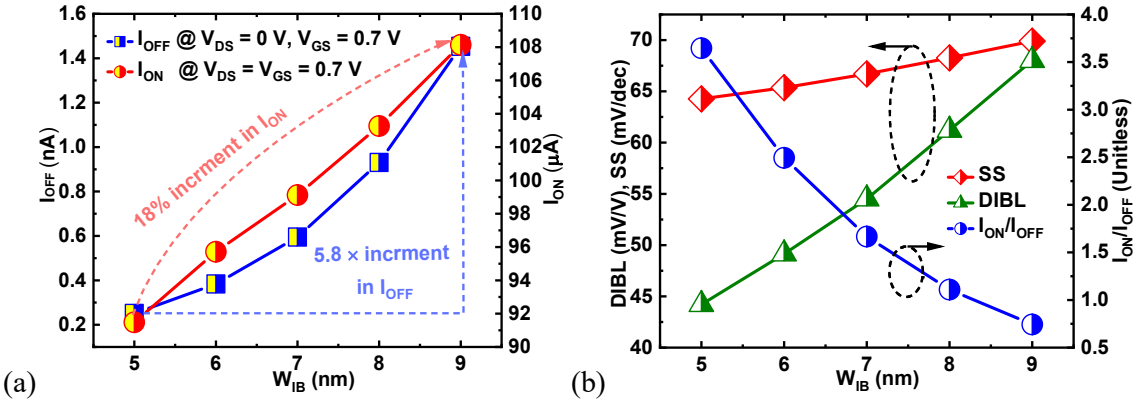


Fig. 6.11: (a) I_{ON} and I_{OFF} (b) SS, DIBL and I_{ON}/I_{OFF} for various W_{IB} values.

Fig. 6.11(a) depicts the I_{ON} and I_{OFF} for various W_{IB} values. It is noticed that as W_{IB} increases, both I_{ON} and I_{OFF} are increased. The increment in I_{ON} is due to the increment in channel area [135], and an increment of 18% is noticed in I_{ON} with the increment of W_{IB} from 5 nm to 9 nm. Further, an increment in I_{OFF} is noticed owing to the marginal degradation of gate control with an increment in W_{IB}. As a result, the I_{OFF} increased by 5.8× from 5 nm to 9 nm of W_{IB}. The DIBL and SS values are depicted in Fig. 6.11(b) for various W_{IB}. As the W_{IB} increases, both DIBL and SS are increased owing to the deterioration of gate electrostatic integrity on the channel. Further, the I_{ON}/I_{OFF} values as a function of W_{IB} are shown in Fig. 6.11(b). As the percentage increment in I_{ON} is lower than that of increment in I_{OFF}, the I_{ON}/I_{OFF} ratio tends to degrade with the rise in W_{IB} and is depicted in Fig. 6.11(b).

6.3.3 Impact of Interbridge Height (H_{IB}) on the Performance of CombFET

The height of the interbridge (H_{IB}), is another crucial dimensional metric as the device with larger H_{IB} values can generate high on current. To assess the impact of H_{IB} on the electrical

performance of CombFET, the H_{IB} is varied from 10 nm to 30 nm with a step of 5 nm. The transfer characteristics (I_D-V_{GS}) and output characteristics (I_D-V_{DS}) are depicted in Fig. 6.12 (a) and (b), respectively. It is observed that with the rise in H_{IB}, the drain current tends to increase as the effective channel area increases.

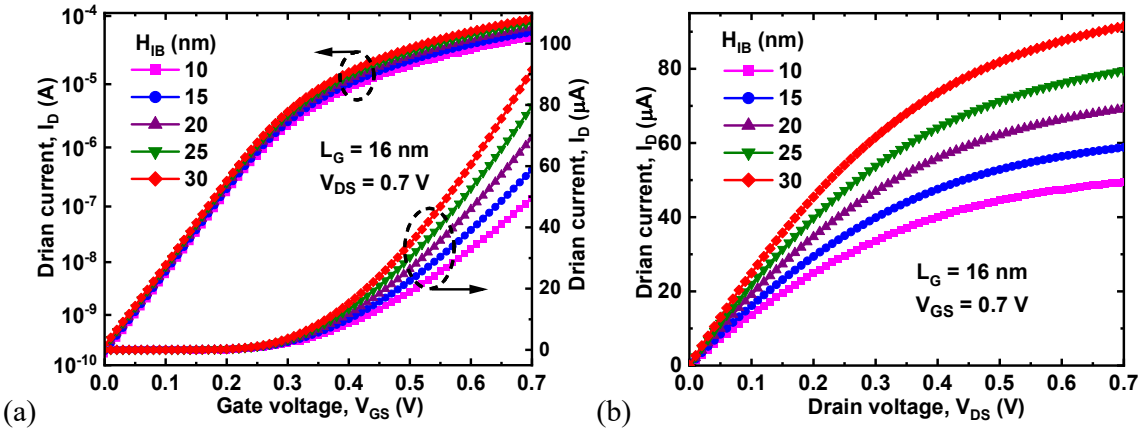


Fig. 6.12: (a) I_D-V_{GS} and (b) I_D-V_{DS} for various H_{IB} values.

The I_{ON} and I_{OFF} as a function H_{IB} are shown in Fig. 6.13(a). As the H_{IB} increases towards 30 nm, the I_{ON} also gets increases owing to the increased effective width of the channel. Moreover, an increment of 84% in I_{ON} is observed when the H_{IB} increases from 10 nm to 30 nm. Further, the I_{OFF} also rises with increment in H_{IB} due to the more electron tunnelling area in the off state. An increment of 47.5% in I_{OFF} is observed from 10 nm to 30 nm.

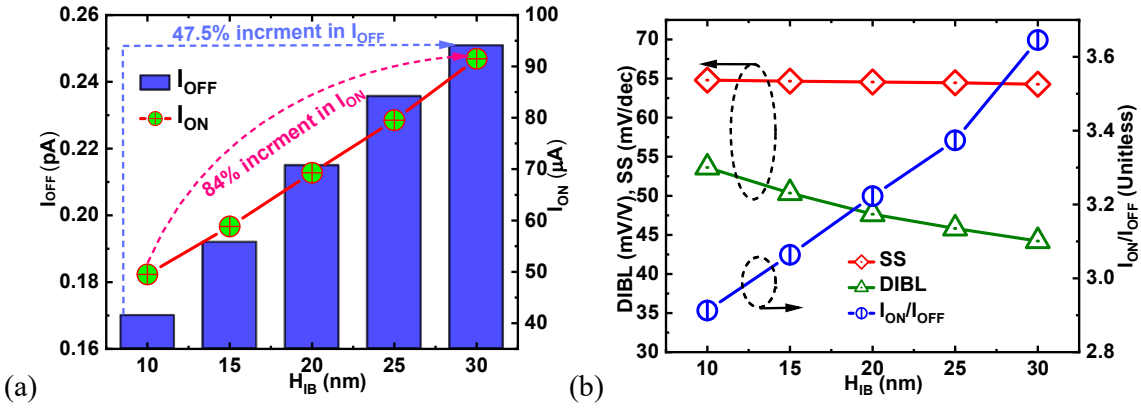


Fig. 6.13: (a) I_{ON} and I_{OFF} (b) SS, DIBL and I_{ON}/I_{OFF} for various H_{IB} values.

The switching ratio (I_{ON}/I_{OFF}) variations with H_{IB} are shown in Fig. 6.13(b). It is noticed that the I_{ON}/I_{OFF} values tend to increase with increment in H_{IB} due to the more increment in I_{ON} than in the I_{OFF}. Thus, H_{IB} with 30 nm offers good performance towards switching applications compared to 10 nm. Further SS and DIBL values are depicted in Fig. 6.13(b). With the rise in

H_{IB}, DIBL decreases as the drain field spreads over a larger area, weakening the DIBL effect. In addition, SS also tends to decrease owing to the increased metal gate area of Fin shaped IB [139].

6.3.4 Performance Comparison of NSFET and CombFET for Circuit Applications

In this section, the circuit behaviour of both NSFET and CombFET is studied for ring oscillator (RO). Initially, the device's current and capacitances with respect to gate voltage are simulated at different drain voltages using the VisualFAB parallel simulation tool by Cogenda. On top of that, the data is exported into the look up tables, which are used while creating the symbol in the Cadence simulator [120] through the Verilog-A model [120]. The process followed to do circuit-level simulation is given in section 4.3.2.

Fig. 6.14 depicts the schematic of the 3-stage Ring oscillator (RO) designed in the Cadence simulator. V_{DD} is the supply voltage. Here, all the load capacitances are considered to be equal, i.e., $C_L = C_{L1} = C_{L2} = C_{L3}$ [123], and V_{DD} is the supply voltage. The load capacitance, C_L is considered as the summation of the total capacitances of both PMOS and NMOS. The oscillations are initiated by forcing an initial voltage of "0" V. Further, the transient response for both NSFET and CombFET based ROs are presented in Fig. 6.15(a) and (b), respectively, for a time of 50 ps at V_{DD} = 1 V.

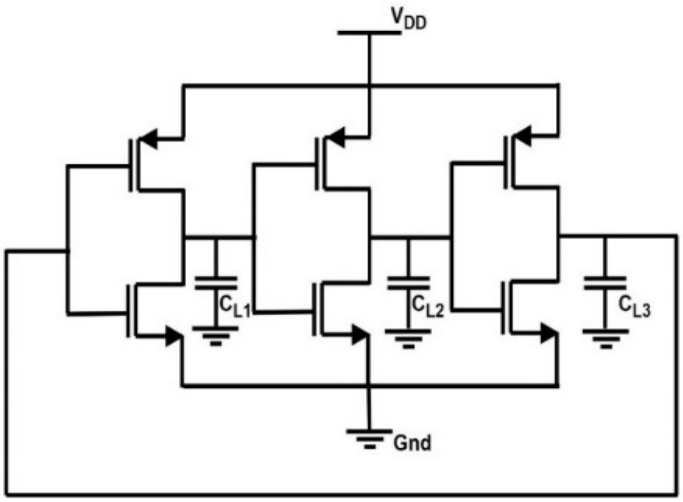


Fig. 6.14: Schematic diagram of the 3-stage ring oscillator (RO).

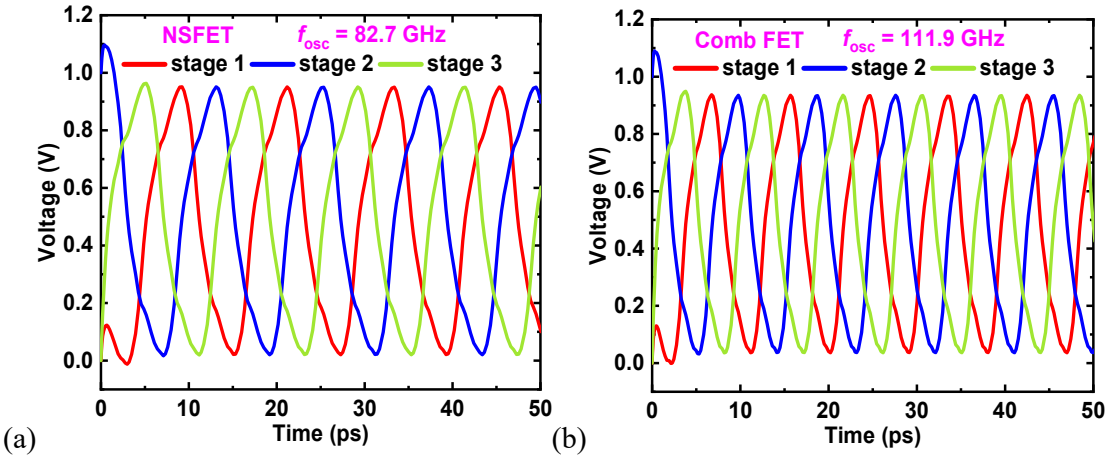


Fig. 6.15: The transient response for (a) NSFET based RO and (b) CombFET based RO.

Fig. 6.15(a) and (b) depict the transient responses of RO for NSFET and CombFET, respectively. It can be noticed that the CombFET based RO outperforms with an f_{OSC} of 111.9 GHz, which is 35% more than NSFET based RO. Though the total capacitances are more for CombFET, the increased I_{ON} helps to offer attractive performance for CombFET, as seen in Fig. 6.15(b).

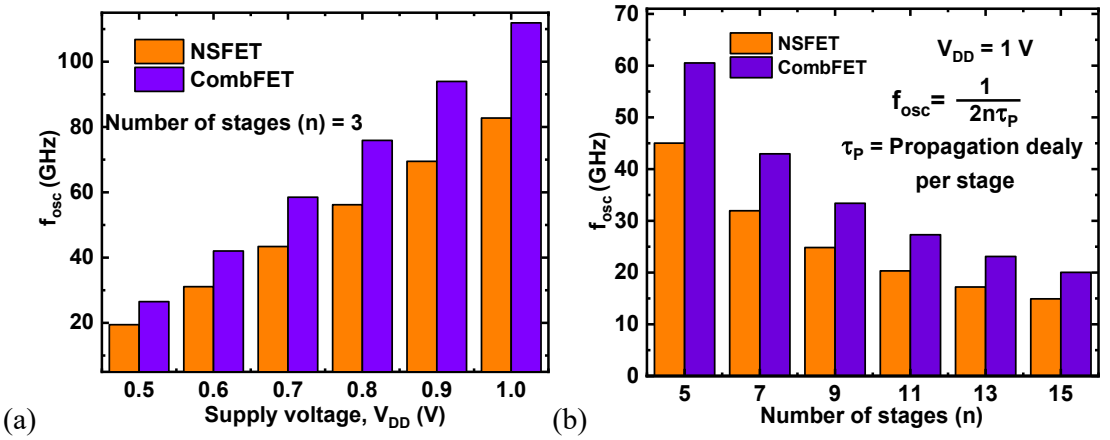


Fig. 6.16: Variations in f_{OSC} with (a) supply voltage and (b) number of stages.

Fig. 6.16(a) depicts the variation in f_{OSC} with supply voltage (V_{DD}) for 3-stage RO. It is noticed that the f_{OSC} tends to rise with the increase in V_{DD} due to the enhancement in I_{ON}. Also, for all the V_{DD}, the CombFET outperforms in terms of f_{OSC}. Further, the f_{OSC} variations with respect to the number of stages (n) of RO are shown in Fig. 6.16(b). As the f_{OSC} is inversely proportional to n, it tends to decrease with rise in the number of stages [72]. Moreover, it is also observed that irrespective of the number of stages, the CombFET outperforms for all the cases. Further, the comparison with existing literature at both device and circuit levels is given in Table. 6.2.

Reference	L_G (nm)	I_{ON} (μA)	SS (mV/dec)	f_T (GHz)	f_{OSC} (GHz) (3-stage RO)
[75]	15	150	67.1	-	-
This Work (NSFET)(Obj-2)	16	24.5	62.48	300	36.77
[73]	12	140	68.2	-	62
This work (NSFET)	16	64	63.49	454	82.7
This work (CombFET)	16	91.5	64.26	590	111.9

Table 6.2: Comparison with existing literature.

In this chapter, the emerging 3-D NSFET and CombFET performances were demonstrated and compared at both device and circuit levels at the 3-nm technology node. The comparison was made under the same footprint and off current. The CombFET, which is the combination of NSFET and fin-like interbridge offer superior ON current compared to conventional NSFET due to its wider channel region. The DC, Analog/RF performances were discussed and compared in detail for both devices by considering various FOMs. An increment of 42%, 48.6% and 46% is noticed in switching ratio, transconductance and Q, respectively, from NSFET to CombFET. Furthermore, the dimensional impact on the electrical performance of CombFET is demonstrated. It is noticed that I_{ON} and I_{OFF} are increased by 18% and 5.8× from IB width of 5 nm to 9 nm. Also, an increment of 84% and 47.5% was observed in I_{ON} and $I_{OFF,}$ respectively, when IB height varied from 10 nm to 30 nm. Further, the 3-stage RO was designed for circuitlevel demonstration and compared the oscillation frequencies. Interestingly, the CombFET based RO outperforms irrespective of its higher capacitances due to the more on current compared to that of NSFET. Moreover, the behaviour of f_{OSC} with respect to the supply voltage and the number of stages is discussed in detail. In all cases, CombFET offers better performance compared to NSFET. Thus, the CombFET device is a promising candidate to continue further scaling as it provides superior performance and is compatible with the existing FinFET fabrication process.

6.4 Conclusion

1. In this chapter, the CombFET device is proposed, which is realized by combining the Fin-like interbridge with nanosheets to obtain larger W_{eff}.

2. The performance comparison is made for both NSFET and CombFET at the matched off currents. The CombFET shows superior performance in I_{ON} of the device. As a result, CombFET is a promising candidate for HP applications.

3. The circuit level analysis is also carried out for 3-stage RO. Though the capacitances are slightly larger for CombFET device, because of the huge increment in I_{ON} tends to offer a significant increment in f_{OSC}.

Chapter-7

Results, Conclusion and Future Scope of the Work

7.1 Results and Overall Conclusions

The need for high performance devices is currently quite high in the microelectronics industry. In this device province, the NSFET transistor has shown to be a promising device in terms of higher performance and compatibility of the fabrication process with FinFET. This work presents detailed analysis of DC, analog/RF and circuit performance on NSFET and CombFET architectures. Device physics in nano regime is studied in detail. The structural dimensional impact for continuing scaling is demonstrated. Moreover, the temperature impact on both device and circuit performance is presented. Further, the structural engineering to NSFET, which is CombFET with high-*k* gate stack implemented to enhance on current, thereby achieving high frequency.

The thesis contains four contributions for designing and analysing NSFET with high performance: (i) Design and performance evaluation of NSFET with varied geometrical and process parameters, (ii) Device and circuit-level performance comparison of GAA Nanosheet FET with varied geometrical parameters, (iii) Temperature assessment of Nanosheet FET for CMOS circuit applications, and (iv) A comprehensive analysis and performance comparison of CombFET and NSFET at 5-nm node for CMOS circuit applications.

In the first contribution, the detailed DC performance of 3D vertically stacked NSFET is analyzed by varying the thickness (N_T) and width (N_W) of the nanosheet. It is observed that there is an increment in both on current and off current as the width and thickness values are increased. However, the switching ratio, DIBL, and SS are degraded as the dimensions of NSFET increase. Moreover, the performance of NSFET is analysed with scaling of gate length to ensure the device feasibility for lower technology nodes. Also, the temperature analysis is performed for a wide range of temperatures to identify the TCP point, which is more essential for biasing the device in various real-time applications. Finally, the impact of work function on device transfer characteristics is analyzed.

In the second contribution, the analog/RF performance of NSFETs is investigated by altering the geometry of each nanosheet at the 5 nm technology node. As the N_T and N_W are raised, there is an increase in both I_{ON} and I_{OFF}. The optimum values for switching ratio, DIBL, and SS are obtained for lower values of N_W and N_T. However, analog/RF FOMs like g_m, g_{ds}, f_T, TFP, and GBW are more for higher N_W and N_T values of NS. These results will give an understanding

of DC and analog/RF performance of NSFET with geometrical variations of the device. Moreover, the circuit performance was assessed for circuits like inverter and 3-stage RO and found that with the increment in width, the propagation delay gets decremented and f_{osc} increases. These results will give performance insights into GAA NSFET at both device level and the circuit level.

The third contribution presents the DC and analog/RF performance analysis of NSFET at elevated temperatures from 25^0C to 200^0C. It is observed that with the increment in temperature, deterioration in ION is observed due to the mobility reduction. Also, the I_{ON}/I_{OFF}, SS and DIBL are degraded with an increment in temperature. Moreover, analog/RF FOMs comparison is presented with variations in temperature. With the rise in temperature, analog/RF FOMs like gm, A_{V0}, f_T, GBW, GFP, GTFP and TFP have deteriorated. Further, the CMOS inverter and ring oscillator performance analysis was presented at different temperatures using the Verilog-A model. As the temperature increases, the propagation delay and gain of the inverter are degraded and offer less performance. Also, the oscillation frequency of the ring oscillator degraded as temperatures increased to 200^0C. These results will give a deep understanding of the performance of NSFET at both device and circuit levels at elevated temperatures.

In the fourth contribution, the emerging 3-D NSFET and CombFET performance were demonstrated and compared at both device and circuit levels at 5-nm technology nodes. The comparison was made under the same footprint and off current. The CombFET, which is the combination of NSFET and fin-like interbridge, offer superior on current compared to conventional NSFET due to its wider channel region. The DC, Analog/RF performances were discussed and compared in detail for both devices by considering various FOMs. Further, the 3-stage RO was designed for circuit level demonstration and compared the oscillation frequencies. Interestingly, the CombFET based RO outperforms irrespective of its higher capacitances due to the more on current compared to that of NSFET. Moreover, the behavior of f_{OSC} with respect to the supply voltage and number of stages is discussed in detail. In all cases, CombFET offers better performance compared to NSFET. Thus, the CombFET device is a promising candidate to continue further scaling as it offers superior performance and is compatible with the existing FinFET fabrication process.

Therefore, the proposed contributions offer more insights into the performance of emerging NSFET and CombFET devices. Also, the performance optimization is achieved by using the CombFET along with high-*k* gate stack in terms of high frequency and is suitable for high-frequency IC applications such as ring oscillators.

7.2 Future Scope of the Work

The majority of the conclusions presented in this work are based on simulation data obtained by using appropriate models. There is a lot of scope for an investigation into the various materials used in the devices. The implementation of the suggested device is also a significant challenge that necessitates a detailed investigation of manufacturing methods and might be the subject of a separate thesis. Moreover, in this work, the idealized geometries such as sharp interfaces, perfect crystal structures, perfect planar layers are assumed. However, realizing defect-free device structure practically may be difficult. Thus, the analysis can be carried out by considering these effects. In addition, there is a lot of room to expand on the thesis's notion by implementing it on additional device architectures. Studying reliability difficulties and designing models that account for them is, once again, an attractive research area. Moreover, the radiation impact of these emerging Nanosheet FETs and CombFETs can be explored. The proposed CombFET device can be extended to high frequency applications such as 5G communications and above.

Appendix A

Visual TCAD Input File for Nanosheet FET

```
GLOBAL    T=300  DopingScale=1e20 ResistiveMetal = False

# Create an initial simulation mesh

MESH      Type = S_Tet4  tetgen="pzAq"

X.MESH    WIDTH=0.001  N.SPACES=1   #al

X.MESH    WIDTH=0.012  N.SPACES=1       # source

X.MESH    WIDTH=0.026  N.SPACES=26      #channel+spacers

X.MESH    WIDTH=0.012  N.SPACES=1       #drain

X.MESH    WIDTH=0.001  N.SPACES=1       #al

Y.MESH    DEPTH=0.005  N.SPACES=1  #metal

Y.MESH    DEPTH=0.014 N.SPACES=21       #si

Y.MESH    DEPTH=0.005  N.SPACES=1     #metal

Z.MESH    WIDTH=0.019  N.SPACES=1

Z.MESH    WIDTH=0.0015 N.SPACES=1       #hfo2

Z.MESH    WIDTH=0.0005 N.SPACES=1       #sio2

Z.MESH    WIDTH=0.005  N.SPACES=5

Z.MESH    WIDTH=0.0005 N.SPACES=1       #sio2

Z.MESH    WIDTH=0.0015 N.SPACES=1       #hfo2

Z.MESH    WIDTH=0.020  N.SPACES=1

Z.MESH    WIDTH=0.0015 N.SPACES=1       #hfo2

Z.MESH    WIDTH=0.0005 N.SPACES=1       #sio2

Z.MESH    WIDTH=0.005  N.SPACES=5

Z.MESH    WIDTH=0.0005 N.SPACES=1       #sio2

Z.MESH    WIDTH=0.0015 N.SPACES=1       #hfo2

Z.MESH    WIDTH=0.003  N.SPACES=1

Z.MESH    WIDTH=0.040  N.SPACES=5  #box

REGION      Label=NGate        Material=NPoly  X.MIN=0.018    X.MAX=0.034  Y.MIN=0.0
Y.MAX=0.024        Z.min=0.0    Z.max=0.060
```

REGION Label=NOxHf Material=HfO2 X.MIN=0.018 X.MAX=0.034 Y.MIN=0.005 Y.MAX=0.019 Z.min=0.019 Z.max=0.028

REGION Label=NOxide Material=Ox X.MIN=0.018 X.MAX=0.034 Y.MIN=0.0065 Y.MAX=0.0175 Z.min=0.0205 Z.max=0.0265

REGION Label=channel Material=Si X.MIN=0.018 X.MAX=0.034 Y.MIN=0.007 Y.MAX=0.017 Z.min=0.021 Z.max=0.026

REGION Label=NOxHf1 Material=HfO2 X.MIN=0.018 X.MAX=0.034 Y.MIN=0.005 Y.MAX=0.019 Z.min=0.048 Z.max=0.057

REGION Label=NOxide1 Material=Ox X.MIN=0.018 X.MAX=0.034 Y.MIN=0.0065 Y.MAX=0.0175 Z.min=0.0495 Z.max=0.0555

REGION Label=channel1 Material=Si X.MIN=0.018 X.MAX=0.034 Y.MIN=0.007 Y.MAX=0.017 Z.min=0.050 Z.max=0.055

REGION Label=NOxideL Material=Nitride X.MIN=0.013 X.MAX=0.018 Y.MIN=0.000 Y.MAX=0.024 Z.min=0.0 Z.max=0.060

REGION Label=NOxideR Material=Nitride X.MIN=0.034 X.MAX=0.039 Y.MIN=0.000 Y.MAX=0.024 Z.min=0.0 Z.max=0.060

REGION Label=LDD_S Material=Si X.MIN=0.013 X.MAX=0.018 Y.MIN=0.007 Y.MAX=0.017 Z.min=0.021 Z.max=0.026

REGION Label=LDD_D Material=Si X.MIN=0.034 X.MAX=0.039 Y.MIN=0.007 Y.MAX=0.017 Z.min=0.021 Z.max=0.026

REGION Label=LDD_S1 Material=Si X.MIN=0.013 X.MAX=0.018 Y.MIN=0.007 Y.MAX=0.017 Z.min=0.050 Z.max=0.055

REGION Label=LDD_D1 Material=Si X.MIN=0.034 X.MAX=0.039 Y.MIN=0.007 Y.MAX=0.017 Z.min=0.050 Z.max=0.055

REGION Label=NSiliconL Material=Si X.MIN=0.001 X.MAX=0.013 Y.MIN=0.000 Y.MAX=0.024 Z.min=0.016 Z.max=0.060

REGION Label=NSiliconR Material=Si X.MIN=0.039 X.MAX=0.051 Y.MIN=0.000 Y.MAX=0.024 Z.min=0.016 Z.max=0.060

REGION Label=NSource Material=Al X.MIN=0.0 X.MAX=0.001 Y.MIN=0.000 Y.MAX=0.024 Z.min=0.016 Z.max=0.060

REGION Label=NDrain Material=Al X.MIN=0.051 X.MAX=0.052 Y.MIN=0.000 Y.MAX=0.024 Z.min=0.016 Z.max=0.060

REGION Label=box Material=Ox X.MIN=0.0 X.MAX=0.052 Y.MIN=0.0 Y.MAX=0.024 Z.min=0.060 Z.max=0.100

DOPING Type=analytic

PROFILE Type=Uniform Ion=Donor N.PEAK=1E19 X.MIN=0.013 X.MAX=0.039 Y.MIN=0.007 Y.MAX=0.017 Z.min=0.021 Z.max=0.026

PROFILE Type=Uniform Ion=Donor N.PEAK=1E19 X.MIN=0.013 X.MAX=0.039 Y.MIN=0.007 Y.MAX=0.017 Z.min=0.050 Z.max=0.055

PROFILE Type=Uniform Ion=Donor N.PEAK=1E19 X.MIN=0.001 X.MAX=0.013 Y.MIN=0.000 Y.MAX=0.024 Z.min=0.016 Z.max=0.060

PROFILE Type=Uniform Ion=Donor N.PEAK=1E19 X.MIN=0.039 X.MAX=0.051 Y.MIN=0.000 Y.MAX=0.024 Z.min=0.016 Z.max=0.060

model region=NSiliconL Esurface=true H.Mob=false #fermi=true #

model region=LDD_S Esurface=true H.Mob=false #fermi=true #

model region=channel Esurface=true H.Mob=false #fermi=true

model region=LDD_D Esurface=true H.Mob=false #fermi=true

model region=NSiliconR Esurface=true H.Mob=false #fermi=true #

model region=LDD_S1 Esurface=true H.Mob=false #fermi=true

#dg.elec=true dg.hole=true qnfactor=1e-1 qminconcentration=1e-2

model region=channel1 Esurface=true H.Mob=false #fermi=true

model region=LDD_D1 Esurface=true H.Mob=false #fermi=true

PMI region=NSiliconL type=basic Model=Sdevice print=1

PMI region=LDD_S type=basic Model=Sdevice print=1

PMI region=channel type=basic Model=Sdevice print=1

PMI region=LDD_D type=basic Model=Sdevice print=1

PMI region=NSiliconR type=basic Model=Sdevice print=1

PMI region=LDD_S1 type=basic Model=Sdevice print=1

PMI region=channel1 type=basic Model=Sdevice print=1

PMI region=LDD_D1 type=basic Model=Sdevice print=1

PMI region=LDD_S type=mob Model=Lombardi print=1 real<MUP2.LSM>=80.5 real<MUN2.LSM>=110

PMI region=channel type=mob Model=Lombardi print=1 real<MUP2.LSM>=80.5 real<MUN2.LSM>=110

PMI region=LDD_D type=mob Model=Lombardi print=1 real<MUP2.LSM>=80.5 real<MUN2.LSM>=110

PMI region=LDD_S1 type=mob Model=Lombardi print=1 real<MUP2.LSM>=80.5 real<MUN2.LSM>=110

PMI region=channel1 type=mob Model=Lombardi print=1 real<MUP2.LSM>=80.5 real<MUN2.LSM>=110

PMI region=LDD_D1 type=mob Model=Lombardi print=1 real<MUP2.LSM>=80.5 real<MUN2.LSM>=110

#PMI region=NSiliconL type=Band Model=Schenk print=1

PMI region=LDD_S type=Band Model=Schenk print=1

PMI region=channel type=Band Model=Schenk print=1

PMI region=LDD_D type=Band Model=Schenk print=1

#PMI region=NSiliconR type=Band Model=Schenk print=1

#PMI region=NSiliconL1 type=Band Model=Schenk prin .t=1

PMI region=LDD_S1 type=Band Model=Schenk print=1

PMI region=channel1 type=Band Model=Schenk print=1

PMI region=LDD_D1 type=Band Model=Schenk print=1

PMI Region=NOxide Type=basic real<PERMITTI>=35 Print=1

PMI Region=NGate Type=basic real<AFFINITY>=4.17 Print=1

model region=LDD_D Esurface=true H.Mob=false #fermi=true

#dg.elec=true dg.hole=true qnfactor=1e-1 qminconcentration=1e-2

model region=LDD_D1 Esurface=true H.Mob=false

#model region=LDD_D2 Esurface=true H.Mob=false

PMI region= LDD_D type=basic Model=Sdevice print=1

PMI region= LDD_D1 type=basic Model=Sdevice print=1

#PMI region= LDD_D2 type=basic Model=Sdevice print=1

PMI region=LDD_D type=mob Model=Lombardi print=1 real<MUP2.LSM>=80.5 real<MUN2.LSM>=110

PMI region=LDD_D1 type=mob Model=Lombardi print=1 real<MUP2.LSM>=80.5 real<MUN2.LSM>=110

model region=LDD_S Esurface=true H.Mob=false #fermi=true

model region=LDD_S1 Esurface=true H.Mob=false

PMI region= LDD_S type=basic Model=Sdevice print=1

PMI region= LDD_S1 type=basic Model=Sdevice print=1

PMI region=LDD_S type=mob Model=Lombardi print=1 real<MUP2.LSM>=80.5 real<MUN2.LSM>=110

PMI region=LDD_S1 type=mob Model=Lombardi print=1 real<MUP2.LSM>=80.5 real<MUN2.LSM>=110

Contact ID=NGate Type=gatecontact workfunction=4.6

VSource Type=VDC ID=DrainConst VConst=0.0

VSource Type=VDC ID=SourceConst VConst=0

METHOD Type=DDML1 LS=MUMPS PC=ASM MaxIt=50 toler.relax=1e8 Relative.Tol=1e-1

SOLVE Type=equ

Attach Electrode="NDrain" Vapp="DrainConst"

Attach Electrode="NSource" Vapp="SourceConst"

METHOD Type=DDML1 LS=MUMPS PC=ASM MaxIt=50 #toler.relax=1e7 Relative.Tol=1e-4

Solve Type=OP Label="ramp1" VstepMax=0.2 out.prefix="ramp1"

Solve Type=DC Label=result VScan=NGate VStart=0 VStop=1 VStep=0.01 out.prefix="m_0.0"

EXPORT VTKFILE=nsfet.vtu CGNSFILE="w10h5.cgns"

Visual TCAD Input File for CombFET

GLOBAL T=300 DopingScale=1e20 ResistiveMetal = False

#---- Create an initial simulation mesh ----

MESH Type = S_Tet4 tetgen="pzAq"

X.MESH WIDTH=0.001 N.SPACES=1 #al

X.MESH WIDTH=0.012 N.SPACES=1 # source

X.MESH WIDTH=0.032 N.SPACES=32 #channel+spacers

X.MESH WIDTH=0.012 N.SPACES=1 #drain

X.MESH WIDTH=0.001 N.SPACES=1 #al

Y.MESH DEPTH=0.005 N.SPACES=1 #metal

Y.MESH DEPTH=0.019 N.SPACES=19 #si(15)+(sio2(1nm)+highk(1nm))*2

Y.MESH DEPTH=0.005 N.SPACES=1 #metal

Z.MESH WIDTH=0.008 N.SPACES=1 #16+3

Z.MESH WIDTH=0.001 N.SPACES=1 #hfo2

Z.MESH WIDTH=0.001 N.SPACES=1 #sio2

Z.MESH WIDTH=0.005 N.SPACES=5

Z.MESH WIDTH=0.001 N.SPACES=1 #sio2

Z.MESH WIDTH=0.001 N.SPACES=1 #hfo2

Z.MESH WIDTH=0.026 N.SPACES=1

Z.MESH WIDTH=0.001 N.SPACES=1 #hfo2

Z.MESH WIDTH=0.001 N.SPACES=1 #sio2

Z.MESH WIDTH=0.005 N.SPACES=5

Z.MESH WIDTH=0.001 N.SPACES=1 #sio2

Z.MESH WIDTH=0.001 N.SPACES=1 #hfo2

Z.MESH WIDTH=0.008 N.SPACES=1

Z.MESH WIDTH=0.040 N.SPACES=1 #box

REGION Label=NGate Material=NPoly X.MIN=0.021 X.MAX=0.037 Y.MIN=0.0 Y.MAX=0.029 Z.min=0.0 Z.max=0.060

REGION Label=NOxideL Material=Nitride X.MIN=0.013 X.MAX=0.021 Y.MIN=0.000 Y.MAX=0.029 Z.min=0.0 Z.max=0.060

REGION Label=NOxideR Material=Nitride X.MIN=0.037 X.MAX=0.045 Y.MIN=0.000 Y.MAX=0.029 Z.min=0.0 Z.max=0.060

REGION Label=NOxHf Material=HfO2 X.MIN=0.021 X.MAX=0.037 Y.MIN=0.005 Y.MAX=0.019 Z.min=0.008 Z.max=0.009

REGION Label=NOxide Material=Ox X.MIN=0.021 X.MAX=0.037 Y.MIN=0.006 Y.MAX=0.017 Z.min=0.009 Z.max=0.010

REGION Label=NOxHf1 Material=HfO2 X.MIN=0.021 X.MAX=0.037 Y.MIN=0.005 Y.MAX=0.006 Z.min=0.009 Z.max=0.017

REGION Label=NOxide1 Material=Ox X.MIN=0.021 X.MAX=0.037 Y.MIN=0.006 Y.MAX=0.007 Z.min=0.010 Z.max=0.016

REGION Label=NOxHf2 Material=HfO2 X.MIN=0.021 X.MAX=0.037 Y.MIN=0.006 Y.MAX=0.011 Z.min=0.016 Z.max=0.017

REGION Label=NOxide2 Material=Ox X.MIN=0.021 X.MAX=0.037 Y.MIN=0.007 Y.MAX=0.012 Z.min=0.015 Z.max=0.016

REGION Label=NOxHf3 Material=HfO2 X.MIN=0.021 X.MAX=0.037 Y.MIN=0.010 Y.MAX=0.011 Z.min=0.017 Z.max=0.044

REGION Label=NOxide3 Material=Ox X.MIN=0.021 X.MAX=0.037 Y.MIN=0.011 Y.MAX=0.012 Z.min=0.016 Z.max=0.045

REGION Label=NOxHf4 Material=HfO2 X.MIN=0.021 X.MAX=0.037 Y.MIN=0.005 Y.MAX=0.010 Z.min=0.043 Z.max=0.044

REGION Label=NOxide4 Material=Ox X.MIN=0.021 X.MAX=0.037 Y.MIN=0.006 Y.MAX=0.011 Z.min=0.044 Z.max=0.045

REGION Label=NOxHf5 Material=HfO2 X.MIN=0.021 X.MAX=0.037 Y.MIN=0.005 Y.MAX=0.006 Z.min=0.044 Z.max=0.052

REGION Label=NOxide5 Material=Ox X.MIN=0.021 X.MAX=0.037 Y.MIN=0.006 Y.MAX=0.007 Z.min=0.045 Z.max=0.051

REGION Label=NOxHf6 Material=HfO2 X.MIN=0.021 X.MAX=0.037 Y.MIN=0.006 Y.MAX=0.018 Z.min=0.051 Z.max=0.052

REGION Label=NOxide6 Material=Ox X.MIN=0.021 X.MAX=0.037 Y.MIN=0.007 Y.MAX=0.017 Z.min=0.050 Z.max=0.051

REGION Label=NOxHf9 Material=HfO2 X.MIN=0.021 X.MAX=0.037 Y.MIN=0.018 Y.MAX=0.019 Z.min=0.009 Z.max=0.052

REGION Label=NOxide9 Material=Ox X.MIN=0.021 X.MAX=0.037 Y.MIN=0.017 Y.MAX=0.018 Z.min=0.009 Z.max=0.051

REGION Label=channel Material=Si X.MIN=0.021 X.MAX=0.037 Y.MIN=0.007 Y.MAX=0.017 Z.min=0.010 Z.max=0.015

REGION Label=channel1 Material=Si X.MIN=0.021 X.MAX=0.037 Y.MIN=0.007 Y.MAX=0.017 Z.min=0.045 Z.max=0.050

REGION Label=tree Material=Si X.MIN=0.021 X.MAX=0.037 Y.MIN=0.012 Y.MAX=0.017 Z.min=0.015 Z.max=0.045

REGION Label=tree_LDD_S Material=Si X.MIN=0.013 X.MAX=0.021 Y.MIN=0.012 Y.MAX=0.017 Z.min=0.015 Z.max=0.045

REGION Label=tree_LDD_D Material=Si X.MIN=0.037 X.MAX=0.045 Y.MIN=0.012 Y.MAX=0.017 Z.min=0.015 Z.max=0.045

REGION Label=LDD_S Material=Si X.MIN=0.013 X.MAX=0.021 Y.MIN=0.007 Y.MAX=0.017 Z.min=0.010 Z.max=0.015

REGION Label=LDD_D Material=Si X.MIN=0.037 X.MAX=0.045 Y.MIN=0.007 Y.MAX=0.017 Z.min=0.010 Z.max=0.015

REGION Label=LDD_S1 Material=Si X.MIN=0.013 X.MAX=0.021 Y.MIN=0.007 Y.MAX=0.017 Z.min=0.045 Z.max=0.050

REGION Label=LDD_D1 Material=Si X.MIN=0.037 X.MAX=0.045 Y.MIN=0.007 Y.MAX=0.017 Z.min=0.045 Z.max=0.050

REGION Label=NSiliconL Material=Si X.MIN=0.001 X.MAX=0.013 Y.MIN=0.000 Y.MAX=0.029 Z.min=0.005 Z.max=0.060

REGION Label=NSiliconR Material=Si X.MIN=0.045 X.MAX=0.057 Y.MIN=0.000 Y.MAX=0.029 Z.min=0.005 Z.max=0.060

REGION Label=NSource Material=Al X.MIN=0.0 X.MAX=0.001 Y.MIN=0.000 Y.MAX=0.029 Z.min=0.005 Z.max=0.060

REGION Label=NDrain Material=Al X.MIN=0.057 X.MAX=0.058 Y.MIN=0.000 Y.MAX=0.029 Z.min=0.005 Z.max=0.060

REGION Label=box Material=Ox X.MIN=0.0 X.MAX=0.058 Y.MIN=0.0 Y.MAX=0.029 Z.min=0.060 Z.max=0.100

DOPING Type=analytic

PROFILE Type=Uniform Ion=Donor N.PEAK=1E15 X.MIN=0.013 X.MAX=0.045 Y.MIN=0.007 Y.MAX=0.022 Z.min=0.010 Z.max=0.015

PROFILE Type=Uniform Ion=Donor N.PEAK=1E15 X.MIN=0.013 X.MAX=0.045 Y.MIN=0.007 Y.MAX=0.022 Z.min=0.045 Z.max=0.050

PROFILE Type=Uniform Ion=Donor N.PEAK=1E15 X.MIN=0.013 X.MAX=0.045 Y.MIN=0.012 Y.MAX=0.017 Z.min=0.015 Z.max=0.045

PROFILE Type=Uniform Ion=Acceptor N.PEAK=1E20 X.MIN=0.001 X.MAX=0.013 Y.MIN=0.000 Y.MAX=0.029 Z.min=0.005 Z.max=0.060

PROFILE Type=Uniform Ion=Acceptor N.PEAK=1E20 X.MIN=0.045 X.MAX=0.057 Y.MIN=0.000 Y.MAX=0.029 Z.min=0.005 Z.max=0.060

model region=NSiliconL Esurface=true H.Mob=false #fermi=true #

model region=LDD_S Esurface=true H.Mob=false #fermi=true #

model region=channel Esurface=true H.Mob=false #fermi=true

model region=LDD_D Esurface=true H.Mob=false #fermi=true

model region=NSiliconR Esurface=true H.Mob=false #fermi=true #

model region=LDD_S1 Esurface=true H.Mob=false #fermi=true #dg.elec=true dg.hole=true qnfactor=1e-1 qminconcentration=1e-2

model region=channel1 Esurface=true H.Mob=false #fermi=true

model region=LDD_D1 Esurface=true H.Mob=false #fermi=true

model region=tree Esurface=true H.Mob=false #fermi=true

model region=tree_LDD_D Esurface=true H.Mob=false #fermi=true

model region=tree_LDD_S Esurface=true H.Mob=false #fermi=true

PMI region=NSiliconL type=basic Model=Sdevice print=1

PMI region=LDD_S type=basic Model=Sdevice print=1

PMI region=channel type=basic Model=Sdevice print=1

PMI region=LDD_D type=basic Model=Sdevice print=1

PMI region=NSiliconR type=basic Model=Sdevice print=1

PMI region=LDD_S1 type=basic Model=Sdevice print=1

PMI region=channel1 type=basic Model=Sdevice print=1

PMI region=LDD_D1 type=basic Model=Sdevice print=1

PMI region=tree type=basic Model=Sdevice print=1

PMI region=tree_LDD_D type=basic Model=Sdevice print=1

PMI region=tree_LDD_S type=basic Model=Sdevice print=1

PMI region=LDD_S type=mob Model=Lombardi print=1 real<MUP2.LSM>=80.5 real<MUN2.LSM>=110

PMI region=channel type=mob Model=Lombardi print=1 real<MUP2.LSM>=80.5 real<MUN2.LSM>=110

PMI region=LDD_D type=mob Model=Lombardi print=1 real<MUP2.LSM>=80.5 real<MUN2.LSM>=110

PMI region=LDD_S1 type=mob Model=Lombardi print=1 real<MUP2.LSM>=80.5 real<MUN2.LSM>=110

PMI region=channel1 type=mob Model=Lombardi print=1 real<MUP2.LSM>=80.5 real<MUN2.LSM>=110

PMI region=LDD_D1 type=mob Model=Lombardi print=1 real<MUP2.LSM>=80.5 real<MUN2.LSM>=110

PMI region=tree type=mob Model=Lombardi print=1 real<MUP2.LSM>=80.5 real<MUN2.LSM>=110

PMI region=tree_LDD_D type=mob Model=Lombardi print=1 real<MUP2.LSM>=80.5 real<MUN2.LSM>=110

PMI region=tree_LDD_S type=mob Model=Lombardi print=1 real<MUP2.LSM>=80.5 real<MUN2.LSM>=110

PMI region=LDD_S type=Band Model=Schenk print=1

PMI region=channel type=Band Model=Schenk print=1

PMI region=LDD_D type=Band Model=Schenk print=1

PMI region=LDD_S1 type=Band Model=Schenk print=1

PMI region=channel1 type=Band Model=Schenk print=1

PMI region=LDD_D1 type=Band Model=Schenk print=1

PMI region=tree type=Band Model=Schenk print=1

PMI region=tree_LDD_D type=Band Model=Schenk print=1

PMI region=tree_LDD_S type=Band Model=Schenk print=1

PMI Region=NGate Type=basic real<AFFINITY>=4.17 Print=1

model region=LDD_D Esurface=true H.Mob=false #fermi=true

model region=LDD_D1 Esurface=true H.Mob=false

PMI region= LDD_D type=basic Model=Sdevice print=1

PMI region= LDD_D1 type=basic Model=Sdevice print=1

PMI region= tree type=basic Model=Sdevice print=1

PMI region= tree_LDD_D type=basic Model=Sdevice print=1

PMI region= tree_LDD_S type=basic Model=Sdevice print=1

PMI region=LDD_D type=mob Model=Lombardi print=1 real<MUP2.LSM>=80.5 real<MUN2.LSM>=110

PMI region=LDD_D1 type=mob Model=Lombardi print=1 real<MUP2.LSM>=80.5 real<MUN2.LSM>=110

PMI region=tree type=mob Model=Lombardi print=1 real<MUP2.LSM>=80.5 real<MUN2.LSM>=110

PMI region=tree_LDD_D type=mob Model=Lombardi print=1 real<MUP2.LSM>=80.5 real<MUN2.LSM>=110

PMI region=tree_LDD_S type=mob Model=Lombardi print=1 real<MUP2.LSM>=80.5 real<MUN2.LSM>=110

model region=LDD_S Esurface=true H.Mob=false #fermi=true

model region=tree Esurface=true H.Mob=false

model region=tree_LDD_D Esurface=true H.Mob=false

model region=tree_LDD_S Esurface=true H.Mob=false

model region=LDD_S1 Esurface=true H.Mob=false

PMI region= LDD_S type=basic Model=Sdevice print=1

PMI region= LDD_S1 type=basic Model=Sdevice print=1

PMI region=LDD_S type=mob Model=Lombardi print=1 real<MUP2.LSM>=80.5 real<MUN2.LSM>=110

PMI region=LDD_S1 type=mob Model=Lombardi print=1 real<MUP2.LSM>=80.5 real<MUN2.LSM>=110

Contact ID=NGate Type=gatecontact workfunction=4.6

VSource Type=VDC ID=DrainConst VConst=0.7

VSource Type=VDC ID=SourceConst VConst=0.7

METHOD Type=DDML1 LS=BCGS PC=ASM MaxIt=50 toler.relax=1e8 Relative.Tol=1e-1

SOLVE Type=equ

Attach Electrode="NDrain" Vapp="DrainConst"

Attach Electrode="NSource" Vapp="SourceConst"

METHOD Type=DDML1 LS=MUMPS PC=ASM MaxIt=50 #toler.relax=1e7 Relative.Tol=1e-4

Solve Type=OP Label="ramp1" VstepMax=0.2 out.prefix="ramp1"

Solve Type=DC Label=result VScan=NGate VStart=0 VStop=0.7 VStep=0.01 out.prefix="comb_ioff"

EXPORT VTKFILE=combns2.vtu

Look-up Table Based Verilog-A code

`include "constants.vams"

`include "disciplines.vams"

module NSFET(d,g,s);

inout d,g,s;

electrical g,d,s;

real Ids, Cgs, Cgd, Qgs, Qgd, Qg;

real VgsEff;

integer out_file;

parameter real W=1;

analog begin

Ids=$table_model(V(d,s), (V(g,s)), "IDVGS-NSFET.tbl","1LL,1LL");

Cgd=$table_model(V(d,s), (V(g,s)), "Cgd-NSFET.tbl","1LL,1LL");

Cgs=$table_model(V(d,s), (V(g,s)), "Cgs-NSFET.tbl","1LL,1LL");

```
if(analysis("dc")) begin
   I(d,s) <+ 1*Ids*W;
end
else begin
  if(analysis("tran")) begin
     Qgd = (W*1*Cgd)*(V(g,d));
     Qgs = (W*1*Cgs)*(V(g,s));
     Qg=Qgs+Qgd;
     I(d,s) <+ 1*Ids*W ;
     I(d) <+ ddt(-1*Qgd);
     I(s) <+ ddt(-1*Qgs);
     I(g) <+ ddt(Qg);
  end
end
end
endmodule
```

List of Publications

A. Published Journals

1. N. Aruna Kumari, Prithvi, P. Performance Evaluation of GAA Nanosheet FET with Varied Geometrical and Process Parameters. Silicon 14, 9821–9831 (2022). https://doi.org/10.1007/s12633-022-01695-7 (**SCI**)
2. N. Aruna Kumari, P. Prithvi, "Device and circuit-level performance comparison of GAA nanosheet FET with varied geometrical parameters", Microelectronics Journal,2022,105432, ISSN0026-2692, https://doi.org/10.1016/j.mejo.2022.105432. (**SCI**)
3. N. Aruna Kumari, P. Prithvi, "A comprehensive analysis and performance comparison of CombFET and NSFET for CMOS circuit applications", AEU - International Journal of Electronics and Communications, Volume 158, 2023, 154447, ISSN 1434-8411, https://doi.org/10.1016/j.aeue.2022.154447 (**SCI**)

B. Under Review Journals

1. Aruna Kumari N., Prithvi, P. "Temperature Assessment of Nanosheet FET for CMOS Circuit Applications," – **Submitted to Silicon, Springer, SCI Indexed (Under review)**
2. Aruna Kumari N., Prithvi, P. "Impact of Scaling on Performance of NSFET for CMOS Analog/RF Circuit Applications" – **Submitted to ECS Journal of Solid State Science and Technology, IOPscience, SCI Indexed, (Under review)**

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