Improvised Space-Vector Pulse Width Modulation Schemes for Four-Level Open-End Winding Induction Motor Drives

Submitted in partial fulfillment of the requirements

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Doctor of Philosophy

by

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CERTIFICATE

This is to certify that the thesis entitled **"Improvised Space-Vector Pulse Width Modulation Schemes for Four-Level Open-End Winding Induction Motor Drives"**, which is being submitted by **Mr. Suresh Lakhimsetty** (Roll No. 715015), is a bonafide work submitted to National Institute of Technology, Warangal in partial fulfilment of the requirement for the award of the degree of *Doctor of Philosophy* in *Department of Electrical Engineering*. To the best of my knowledge, the work incorporated in this thesis has not been submitted elsewhere for the award of any degree.

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DECLARATION

This is to certify that the work presented in the thesis entitled **"Improvised Space-Vector Pulse Width Modulation Schemes for Four-Level Open-End Winding Induction Motor Drives"** is a bonafide work done by me under the supervision of **Prof. V. T. Somasekhar, Department of Electrical Engineering, National Institute of Technology Warangal** and was not submitted elsewhere for the award of any degree.

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ABSTRACT

In this thesis, the Open-End Winding Induction Motor (OEWIM) drive is considered for achieving the multilevel operation. The OEWIM drive is realized by removing the star or delta connections of the stator winding of an induction motor and feeding it with two two-level Voltage Source Inverters (VSIs) from either side. In the present thesis, the VSIs are operated with two different DC input voltages, which are in the ratio of 2:1, to achieve four-levels across each motor phase winding. Thus, this drive configuration is named as the four-level Open-End Winding Induction Motor Drive.

The four-level OEWIM drive circuit configuration mainly suffers from two problems. They are: (i) the lower dc-link voltage capacitor is overcharged by its counter-part, i.e. the higher dc-link voltage capacitor (ii) the presence of zero-sequence current (ZSC) in the motor phase windings. However, the ZSC can be avoided by denying a path for the circulation of zero-sequence current by using isolated dc-power supplies.

This thesis investigates about the applicability of various Space-Vector Pulse Width Modulation (SVPWM) schemes for two circuit topologies of the four-level OEWIM drive (of which, one circuit is a slightly improvised version of an existing topology). The proposed SVPWM techniques avoid the overcharging of the lower-voltage dc-link capacitor and improve the drive performance. A closed-loop control strategy, based on Model Predictive Control (MPC), is also proposed to improve the performance of the OEWIM drive.

To improve the performance of the four-level OEWIM drive, four variants of *Discontinuous-Decoupled SVPWM (DDSVPWM)* techniques are proposed. It is known that, the Discontinuous-SVPWM techniques reduce the switching power loss in inverters. However, lack of structural symmetry of the power circuit renders it unwieldy to devise these SVPWM schemes. Chapter-2 explores the applicability of the Discontinuous-Decoupled SVPWM techniques for the four-level OEWIMD, without compromising on the waveform symmetries. It is shown that the proposed SVPWM techniques, while avoiding the overcharging

phenomenon of the low-voltage dc-link capacitor, also lower the *dv/dt* across the motor phase windings.

Three variants of SVPWM strategies are proposed in Chapter-3 for the four-level OEWIM drive with two isolated dc-power supplies to reduce the switching power loss and to improve the drive performance. In the proposed SVPWM schemes, the inverter, which is operated with the lower dc-link voltage is clamped to the nearest sub-hexagonal centre (NSHC), while the other inverter is switched around it. The proposed SVPWM schemes, apart from avoiding the overcharging phenomenon and achieving all waveform symmetries, reduce power loss in the dual-inverter system (compared to the Discontinuous Decoupled SVPWM schemes available in chapter-2).

A nested rectifier-inverter topology with two dc-power supplies (as against three reported in the earlier literature) is proposed in Chapter-4 to improve the reliability of the four-level OEWIM drive. The unwanted phenomenon of overcharging the low-voltage capacitor is avoided with this power circuit also. To suppress the zero-sequence currents, an SVPWM scheme is proposed and is named as *Nested Inverter Clamped Sample-Averaged Zero-Sequence Elimination (NICSAZE)*. The proposed *NICSAZE-PWM* scheme eliminates the zero-sequence currents in the average sense and reduces the power loss in the dual-inverter system.

An improvised Predictive Current Control (PCC) algorithm, which belongs to the genre of MPC, is proposed to control the load currents of the four-level OEWIM drive in Chapter-5. The conventional PCC uses all of the available 37 candidate voltage vectors of the dual-inverter system to select the optimal voltage vector. In contrast, the proposed PCC (which utilises the concept of NSHC described in Chapter-3) requires the testing of only 5 candidate voltage vectors for the selection. Thus, the proposed PCC results in a considerable alleviation of the computational burden on the control platform. It is also shown that, compared to the conventional PCC, the proposed PCC technique results in the reduction of power loss incurred in the dual-inverter system for a considerable portion of the operating range of the drive.

All the PWM schemes, circuit topologies and the closed-loop control strategies proposed in this thesis are first simulated using *MATLAB/SIMULINK* software and the results are then validated by implementing these schemes on a 5-HP, 400 V, 50 Hz, 1445 RPM, three-phase open-end winding induction motor. The experimental work presented in this thesis is carried out using the *dSPACE1104* control platform.

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List of Symbols

V_{DC}	:	Input dc-link voltage
q	:	Number of levels (i.e. q = 2, 3, 4,....)
v_{ao}, v_{bo}, and v_{co}	:	Pole voltages of inverter-1
$v_{a'o'}$, $v_{b'o'}$ $v_{c'o'}$	:	Pole voltages of inverter-2
$v_{aa'}$, $v_{bb'}$, $v_{cc'}$	:	Stator phase voltages of open-end winding induction motor
θ	:	angle subtended by the 'q-axis' of the 'dq0' reference frame with respect to the axis of the A-phase winding of the stator
$v_{aa'r'}$, $v_{bb'r'}$ & $v_{cc'r'}$	:	Rotor phase voltages of open-end winding induction motor
v_z	:	Zero-sequence voltage
v_{ref}	:	Reference voltage space vector
m_a	:	Modulation index
f	:	Rated supply frequency
f_l	:	Fundamental frequency of the drive
T_s	:	Sampling time period
T_{s1}	:	Sampling time period of inverter-1
T_{s2}	:	Sampling time period of inverter-2
T_o	:	Time period of fundamental frequency ($1/f_l$)
α	:	Angle subtended by the reference vector with respect to a-phase axis
v_x^*	:	Instantaneous phase reference voltage (where $x \in a, b, c$)
$2v_a^*/3$, $2v_b^*/3$, $2v_c^*/3$	:	Instantaneous phase reference voltages of inverter-1
$v_a^*/3$, $v_b^*/3$, $v_c^*/3$		Instantaneous phase reference voltages inverter-2
T_{xs1}	:	Imaginary switching time period of inverter-1 (where $x \in a, b, c$)
T_{xs2}	:	Imaginary switching time period of inverter-2 (where $x \in a, b, c$)
T_{eff}	:	Effective time period of dual-inverter
T_{eff1}	:	Effective time-period of inverter-1
T_{eff2}	:	Effective time-period of inverter-2

T_{max1}	:	Maximum amongst the three imaginary switching times of inverter-1
T_{min1}	:	Minimum amongst the three imaginary switching times of inverter-1
T_{max2}	:	Maximum amongst the three imaginary switching times of inverter-2
T_{min2}	:	Minimum amongst the three imaginary switching times of inverter-2
T_z	:	Zero-vector or null-vector time period
T_{z1}	:	Null-vector time period of inverter-1
T_{z2}	:	Null-vector time period of inverter-2
$T_{offset1}$	:	Offset time period of inverter-1
$T_{offset2}$	:	Offset time period of inverter-2
T_{ga1}, T_{gb1}, T_{gc1}	:	Phase switching time periods of inverter-1
T_{ga2}, T_{gb2}, T_{gc2}	:	Phase switching time periods of inverter-2
T_1, T_2	:	Dwell time periods
T_A^+	:	Top switching device of phase-A leg
T_A^-	:	Bottom switching device of phase-A leg
D_A^+	:	Anti-parallel diode of top switching device of phase-A leg
D_A^-	:	Anti-parallel diode of bottom switching device of phase-A leg
P_{SW}	:	Switching power loss
P_{con}	:	Conduction power loss
v_{SW}	:	Voltage blocked by the switch in its OFF-state (i.e. V_{DC})
$i_{SW} = I_{ON}$	:	Current flowing through the switch in its on-state
f_s	:	Switching frequency
v_{ON}	:	on-state voltage drop
t_{ri}, t_{rv}	:	Rise times of current and voltage respectively
t_{fv}, t_{fi}	:	Fall times of voltage and current respectively
t_{ON}	:	Switch turn-on time
V_t	:	IGBT fixed voltage drop under zero-current condition
R_{CE}	:	IGBT on-drop resistance

V_f	:	Diode fixed voltage drop under zero-current condition
R_{AK}	:	Diode on-drop resistance
R_s	:	Stator resistance of the OEWIMD
R_{rp}	:	Rotor resistance of the OEWIMD referred to stator
x_{ls}	:	Stator leakage reactance of the OEWIMD
$x_{lr'}$	:	Rotor leakage reactance of the OEWIMD referred to stator
X_m	:	Magnetizing reactance of the OEWIMD
J	:	Moment of inertia of the OEWIMD
B	:	Friction coefficient of the OEWIMD
P	:	Number of poles of the OEWIMD
V_1	:	Fundamental voltage component of phase voltage
V_n	:	n^{th} harmonic voltage component of the phase voltage
n	:	Harmonic order (i.e. n = 2, 3, 4, ...)
i_1	:	Fundamental current component of phase current
i_n	:	n^{th} harmonic current component of the phase current
Ns	:	Number of samples
ω_a	:	Arbitrary angular frequency
v_s	:	Stator voltage space vector of the OEWIM
v_r	:	Rotor voltage space vector of the OEWIM
i_s	:	Stator current space vector of the OEWIM
i_r	:	Rotor current space vector of the OEWIM
ψ_s	:	Stator flux space vector of the OEWIM
ψ_r	:	Rotor flux space vector of the OEWIM
R_r	:	Rotor resistance of the OEWIM
L_s	:	Stator inductance of the OEWIM
L_r	:	Rotor inductance of the OEWIM
L_m	:	Mutual inductance of the OEWIM
ω	:	Electrical rotor angular speed
$\nu_{\alpha s}$	:	Real component of the OEWIM voltage space vector
$\nu_{\beta s}$	:	Imaginary component of the OEWIM voltage space vector
$i_{\alpha s}$	:	Real component of the OEWIM current space vector

$i_{\beta s}$	:	Imaginary component of the OEWIM current space vector
T_e^*	:	Reference torque component from output of speed PI-controller
ψ_r^*	:	Reference rotor flux equal to the rated rotor flux of the machine
g_i	:	Cost function based on OEWIM reference and predicted currents
g_v	:	Cost function based on OEWIM reference and predicted voltages

List of Abbreviations

VSI	:	Voltage Source Inverter
PWM	:	Pulse Width Modulation
MV	:	Medium Voltage
ASD	:	Adjustable-Speed Drives
SVPWM	:	Space Vector PWM
NPC	:	Neutral Point Clamped
FC	:	Flying Capacitor
ANPC	:	Active NPC
CHB	:	Cascaded H-Bridge
HNPC	:	Hybrid NPC
IGBT	:	Insulated-Gate Bipolar Transistor
IEGT	:	Injection-Enhanced Gate Transistor
GCT	:	Integrated Gate-Commutated Thyristor
MMC	:	Modular Multilevel Converter
HVDC	:	High-Voltage Direct Current
THD	:	Total Harmonic Distortion
WTHD	:	Weighted THD
OEWIM	:	Open-End Winding Induction Motor
ZSV	:	Zero-Sequence Voltage
ZSC	:	Zero-Sequence Current
SAZE	:	Sample Averaged Zero-Sequence Elimination
DSAZE	:	Decoupled SAZE
SPWM	:	Sine PWM

NSPWM	:	Near state PWM
EDPWM	:	Equal switching Duty PWM
PDPWM	:	Proportional switching Duty PWM
OEWIMD	:	Open-End Winding Induction Motor Drive
NICSAZE	:	Nested Inverter Clamped SAZE
FOC	:	Field-Oriented Control
DTC	:	Direct-Torque Control
FS-MPC	:	Finite Set – Model Predictive Control
PTC	:	Predictive Torque Control
PCC	:	Predictive Current Control
EV	:	Electric Vehicle
HEV	:	Hybrid EV
DDPWM	:	Discontinuous Decoupled PWM
CSPWM	:	Center-Spaced PWM
PCPWM	:	Phase Clamped PWM
NSHC	:	Nearest Sub-Hexagonal Center

Chapter 1

Introduction

Contents

Chapter 1
Introduction

This chapter presents a brief description about the background and the motivation of this thesis. The emergence of multilevel inverter technology, and recent developments with reference to the dual-inverter driven open-ended motors are described. Finally, the objective of this research work is presented along with the organization of the thesis.

1.1 Background

Rapid growth of industrialization and depleting fossil fuel resources are the principal causes for the ever-rising demand of electrical energy, which compel efficient and optimal employment of the resources of electrical energy. Also, industrial applications often call for conversion of electrical energy from one form to another, to suit a given application. In the contemporary industrial scenario, digital signal processing and power electronic converters play crucial roles to realize these objectives, while improving the quality of output power.

The present-day industry extensively employs power electronic converters such as Voltage-Source Inverters (VSI) in a wide range of applications due to their higher efficiency and performance [1-2]. VSI-driven variable speed induction motor drives are increasingly being employed in applications such as fans, compressors and pumps in industries. For most of these drives, which don't demand high dynamic performance, a simple scalar control is adequate. However, for applications, which demand a high dynamic performance (such as rolling-mill applications), vector-control is being used. A basic three-phase two-level VSI fed induction motor drive is shown in Fig. 1.1. In general, Pulse Width Modulation (PWM) strategies are used to generate the gating pulses to the VSI. The PWM of VSI serves two principal purposes. Firstly, it controls the magnitude and frequency of the fundamental component of the output voltage. Secondly, it improves the harmonic performance of the VSI by reducing the magnitude of the components of higher order harmonics, without the aid of external filters. In general, in VSI-driven induction motor drives, it is desirable to switch power semiconductor devices at high switching frequencies to improve the harmonic

performance. However, increase in the switching frequency increases the switching power loss, which could be significant at high power levels.

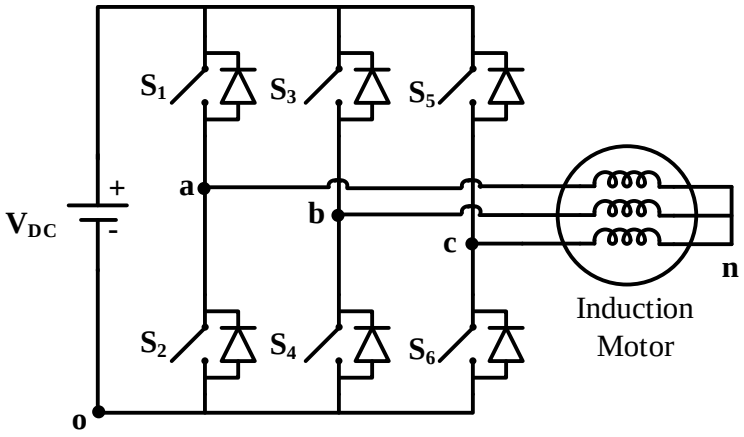


Fig. 1.1: Conventional two-level voltage source inverter

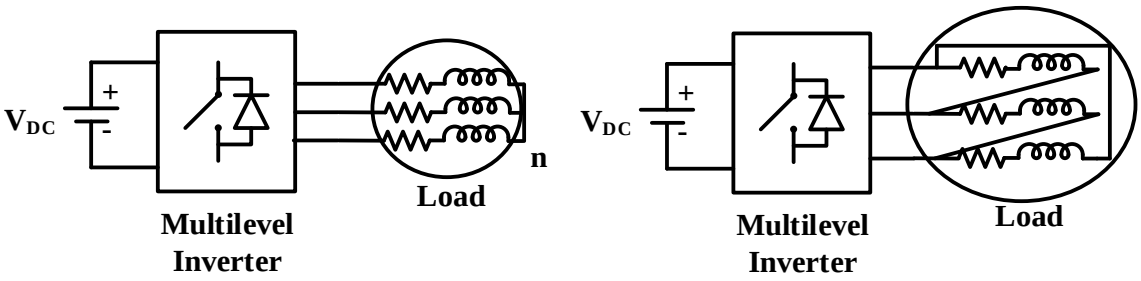
The maximum output voltage of the VSI, shown in Fig. 1.1, depends on the maximum modulation index and the dc input voltage [3]. In practice, the dc-input voltage is limited by the blocking voltage of the semiconductor devices.

To avoid high switching power loss and the blocking voltage limitation of the semiconductor devices, multilevel voltage source inverters are being developed for the past few decades [4-8].

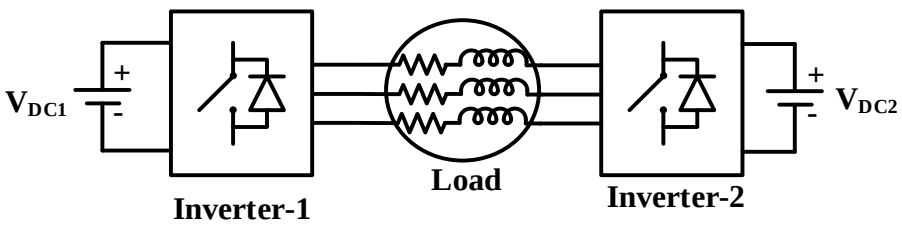
In multilevel inverters, fractional voltages of the input dc power supply are obtained with the aid of capacitors. These fractional voltages are then applied to the end connections of the series connected power semiconductor devices. These devices are switched with appropriate PWM schemes to achieve multilevel output voltages. In the last two decades, multilevel inverters have emerged in high power, medium voltage (MV) applications. High power converters and MV drives were first developed in the mid-1980s [5]. The voltage of MV drive-converters range from 3.3 kV to 6.6 kV and the output power ranges from 1 to 50 MW [8].

Applications of multilevel inverters are now widely spread across industry. They include pipeline pumps, gas compressors in the petrochemical industry [9], raw sewage pumps, treatment pumps, freshwater pumps in water pumping stations [10], renewable energy sources [11], reactive power compensators [12], crushers, rolling mills, hoists in mining and metal industry [13], traction drives for locomotives [13], Kiln-induced draft fans, forced draft fans in cement industry [14], naval vessels, shuttle tankers in transportation industry, power distribution, laminators, conveyors, blowers, compressors, adjustable-speed drives (ASDs) for medium-voltage induction motors [15-18] and others [19].

Multilevel converter systems can be divided into two groups, based on the supply techniques. Conventional multilevel inverter topologies use single-ended converter and the load is either star connected (left) or delta connected (right), as shown in Fig. 1.2 (a). The other system uses two power supplies across each phase of the load as shown in Fig. 1.2 (b), known as the dual-inverter system [20]. Two conventional VSIs are sufficient to realize the dual-inverter system to achieve multilevel operation. However, two isolated DC power supplies are needed as compared to the single-ended multilevel converter system.



(a)



(b)

Fig. 1.2: Inverter topologies based on supply techniques (a) Multilevel inverter with single-ended load (b) Dual-inverter with open-ended load

The dual-inverter system, while retaining all of the advantages of the single-ended multilevel converters, displays the additional advantage of offering more redundancy in terms of switching vector selection. A proper selection of the input dc-link voltages for the dual inverter system facilitates multilevel inversion. When the supplies are symmetrical (i.e. 1:1), three-level inversion is obtained. With asymmetric dc-link voltages, four (i.e. 2:1) or more levels can be achieved. Abundant amount of research work was reported on the topic of *three-level open-end winding induction motor drives*. However, the dual-inverter system with asymmetric input supplies (i.e. four-level operation) has not adequately been explored. This is the motivating factor to undertake the study of the dual-inverter system with asymmetric supplies, which provides four-level inversion.

1.2 Literature Review

As stated earlier, multilevel inverter technology is still emerging, showing promise for many industrial applications. Many topologies and new control strategies have been proposed for high power applications [4-8]. These works mainly explain the traditional and well-established inverter topologies, such as, the Neutral Point Clamped (NPC), Flying Capacitor (FC) and the Cascaded H-Bridge (CHB), as well as specific modulation strategies to control their operation.

The main advantages of the multilevel inverters (MLIs), as compared to the two-level inverter are as follows:

- Achievement of higher AC voltages with semiconductor switching devices of lower voltage ratings.
- Enhanced spectral performance i.e. reduced Total Harmonic Distortion (THD), as output voltages are nearly sinusoidal.
- Low dv/dt on the semi-conductor devices.
- Low Electro Magnetic Interference (EMI).
- Smaller or no requirement of filters.
- Reduction in the stress on winding insulation.
- Operability with lower switching frequencies.

- Reduced common-mode voltages (CMVs), which reduces unwanted bearing currents. Additional modulation methods can be adopted in order to eliminate the CMVs.

In many industrial applications, induction motors are used as variable speed drives, which requires variable voltage and variable frequency. However, the grid provides a fixed voltage and a fixed frequency. Hence, to achieve variable-speed operation, power electronic converters are to be used between the grid and the induction motor. A typical industrial medium voltage motor drive is shown in Fig. 1.3 [19].

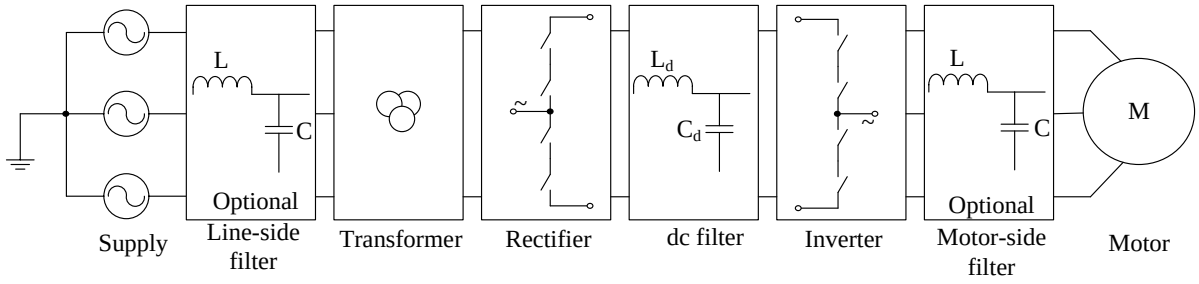


Fig. 1.3: General block diagram of industrial MV drive [19]

The general practice prevailing in power electronic converters is to switch power semiconductor devices at high switching frequencies in order to minimize the harmonic content and the filter size [21]. However, the increased switching frequency increases the switching power loss and reduces the overall drive efficiency.

One method to reduce the switching power loss is to construct a resonant circuit by adding an LC network to the hard switched inverter topology. One such resonant converter topology was proposed by R.W. DeDoncker *et. al.* [22]. In this work, the authors proposed an auxiliary resonant commutated pole converter to reduce the switching loss by operating the inverter switches when the voltage is zero.

Another topology was proposed by J. He *et. al.* [23], wherein the converter includes the resonant dc-link. In this proposal, the dc-link circuit is used as an interface between the dc voltage and the PWM inverter to provide a short zero voltage period in the dc-link voltage to allow the zero voltage switchings.

The principal drawbacks with the power circuit configurations proposed in [22] and [23] is that, the inverter peak-currents or the voltages are considerably higher than those encountered in the hard switched converters, which increases the device rating. Also, an added auxiliary triggered resonant commutation circuit increases the system complexity and cost.

In early 1980s, A. Nabae, I. Takahashi, and H. Akagi presented the first multi-level converter [24]. This converter is a three-level voltage source inverter, shown in Fig. 1.4. This inverter is named as the *Neutral Point Clamped* (NPC) inverter, which is also known as the *diode-clamped* inverter [24]. This inverter is a simple modification to a two-level voltage source inverter in that, two more semiconductor switches and clamping diodes are added in series with each leg of Fig. 1.1. For the same dc-link voltage, the voltage ratings of the semiconductors is half as compared to the conventional 2-level VSI. Conversely, if these semiconductors are of the same voltage rating as that of the two-level case, the dc-link voltage can be doubled, enhancing the power handling capability of the inverter. In literature, the proposed topology is extended to more levels [25-27] to increase the power rating of the converter and to enhance the spectral performance. Also, the extension of the NPC configuration for higher number of levels allows its operability with lower switching frequencies, which reduces the switching power loss (compared to the 3-level NPC).

Despite these advantages, the NPC topology has the following drawbacks: i) requirement of high voltage rating for the clamping diodes, ii) unequal device ratings, iii) requirement of higher number of clamping diodes as the levels increases, iv) unbalanced dc-link capacitor voltages, v) complexity of control for higher number of levels, vi) increased switching losses due to the reverse recovery current of clamping diodes, vii) unsymmetrical distribution of power losses in semiconductor switching devices causing unsymmetrical distribution of the semiconductor junction temperature, which demand better strategies for the thermal management [7] and viii) difficulty to extend the converter range by series connection of semiconductors [2, 4, 7, 28].

At present, research is focused to balance the dc-link capacitor voltages using the conventional and advanced strategies such as SVPWM and model predictive control (MPC) [29-30]. Recently, C. Xia *et. al.* proposed a new discontinuous PWM technique for the reduction of the switching loss [31]. T. Bruckner *et. al.* proposed active NPC (ANPC) converter to overcome the unequal loss distribution [32]. Another type of diode clamped converter, called the hybrid neutral point clamped converter [33], proposed by T. B. Soeiro *et. al.*, utilizes extra two semiconductor devices than the traditional NPC converter. The proposed topology is also overcome the unequal loss distribution. However, even this topology suffers from some of the drawbacks which are mentioned above.

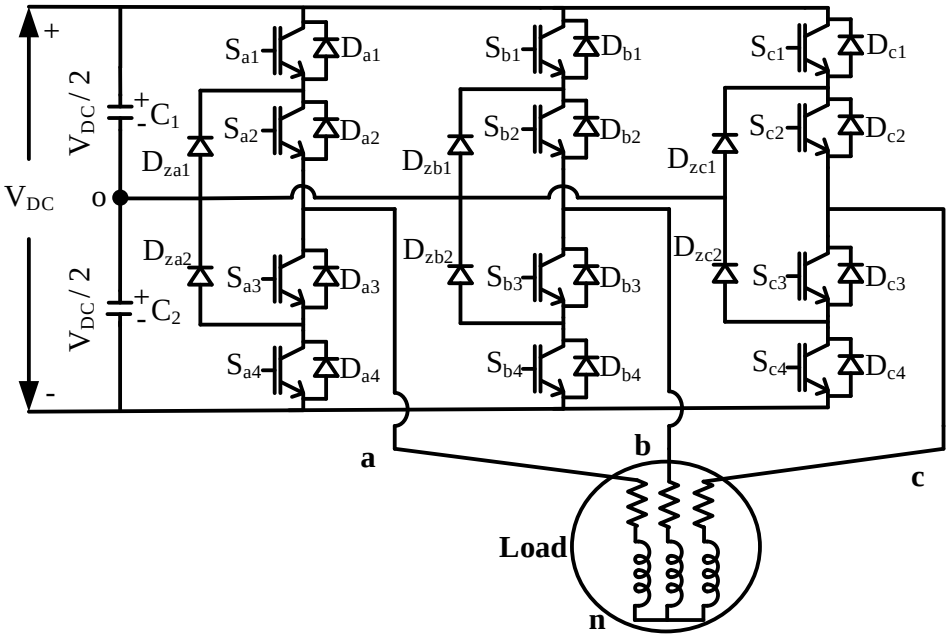


Fig. 1.4: Three-level NPC MLI

Another popular three-level inverter topology, named as the *Flying Capacitor* Multi-Level Inverter (FCMLI) was proposed in the year 1992 by T. Maynard *et. al* [34]. This power circuit configuration is shown in Fig. 1.5. This topology is also realized by the series connection of two more semiconductor devices in series with each leg of Fig. 1.1. Unlike the NPC MLI, which uses the clamping diodes to realize the multilevel inversion, the FCMLI uses clamping capacitors. Compared to the NPC based MLI, the FC topology possesses more number of redundant switching states to control the capacitor charge balance [35]. Currently, four-level FCMLIs are being manufactured by an organization, which produces MV industrial

drives [36]. Similar to the NPC MLI, the FCMLI is also extended for more number of levels [34-36].

However, the FCMLI has the following disadvantages [1-2, 4]: i) requirement of excessive number of floating capacitors leading to higher cost, ii) occupation of larger space due to the bulkiness of capacitors, iii) requirement of higher switching frequency, leading to higher switching losses, and iv) requirement of more complex control strategies to balance the floating capacitor voltages.

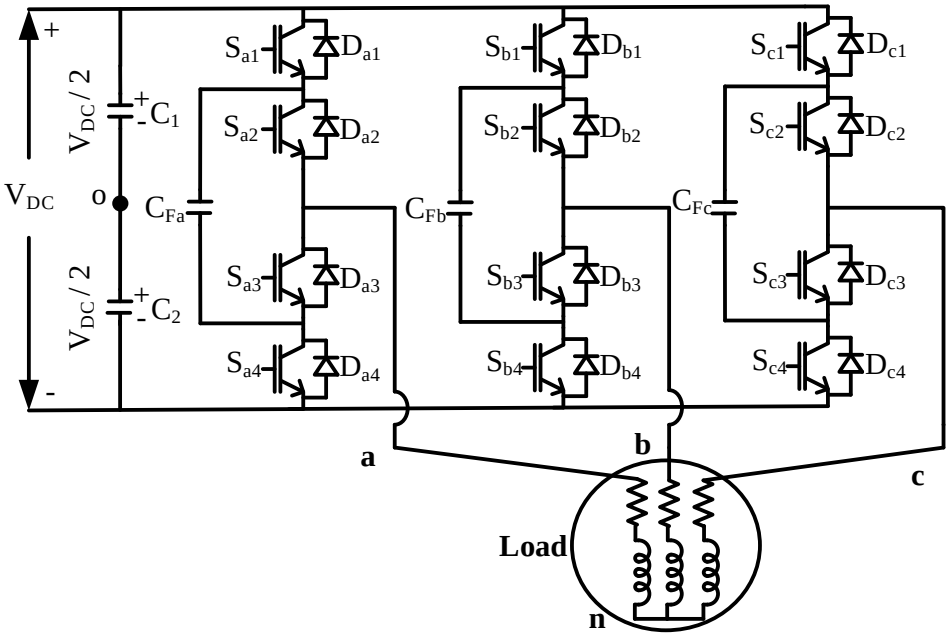


Fig. 1.5: Three-level FC MLI

P. W. Hammond proposed a cascaded H-bridge converter (CHB) for MV drives in 1990s, wherein single-phase inverters are connected in series with separate dc sources [37] as shown in Fig. 1.6. This is one of the simplest converter structures with reduced cost of commissioning and maintenance. Also, this converter avoids clamping diodes, voltage balancing of flying capacitors, while introducing some fault tolerant capability [38]. The advantage of the CHB converter appears profoundly in such applications, where isolated voltage sources are inherent (example fuel cells, photovoltaic power applications and grid connected battery storage systems) [39-40].

However, as several single-phase inverters are connected in series in the CHB converter, the input dc sources must be isolated from each other. In general, phase shifting transformers are used to obtain isolated power supplies, which are bulky and expensive. As the levels are increased, there is a need for more isolated dc sources.

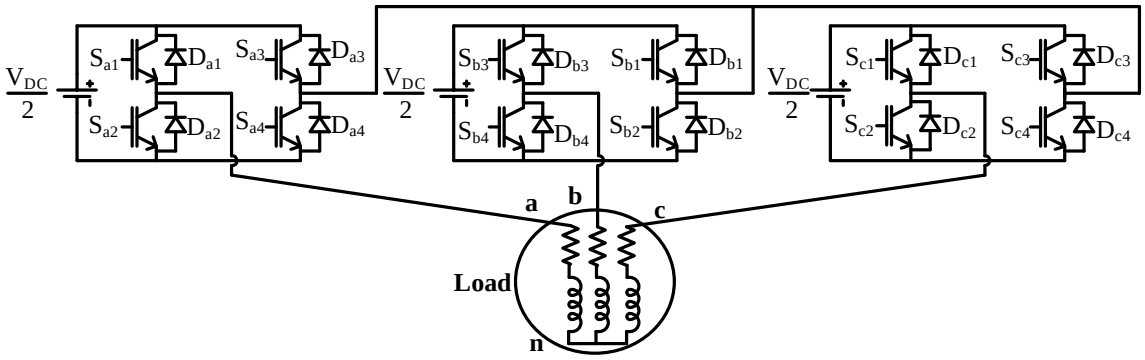


Fig. 1.6: Three-level CHB MLI

In addition to the 3-level MLIs presented above, the per-phase diagrams of four-level MLIs of the types NPC and FC are presented in the Figs. 1.7 and 1.8 respectively, to show the complexity of the MLI structures as the number of levels increased.

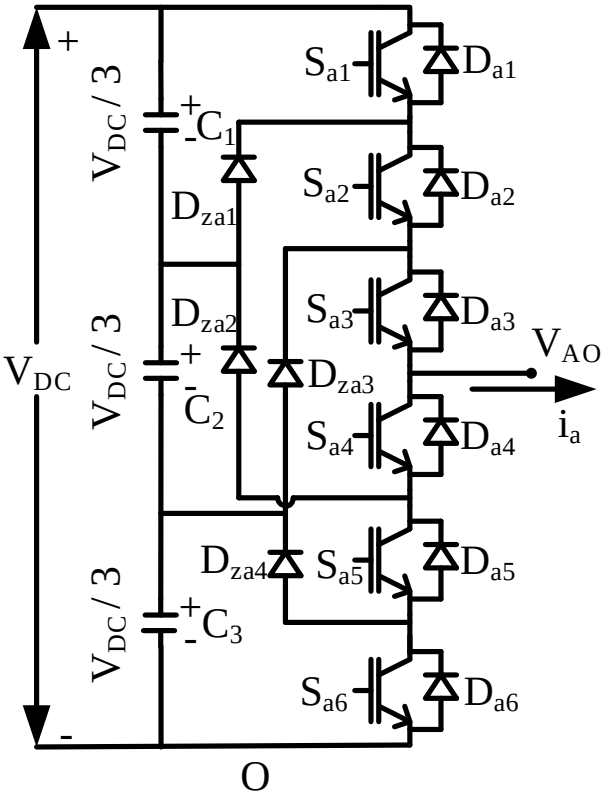


Fig. 1.7: Per-phase diagram of a four-level NPC MLI

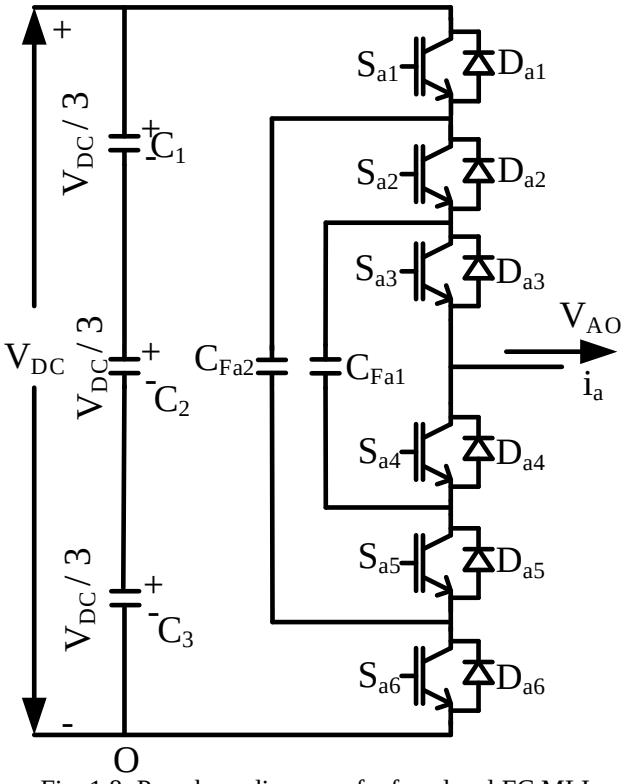


Fig. 1.8: Per-phase diagram of a four-level FC MLI

The device count details per leg of NPC, FC and CHB converters are presented in Table 1.1 [4].

Table 1.1: Comparison between NPC, FC and CHB converters

Topology	**NPC**	**FC**	**CHB**
Main switching devices	2(q-1)	2(q-1)	2(q-1)
Main diodes	2(q-1)	2(q-1)	2(q-1)
Clamping diodes per phase	(q-1)(q-2)	0	0
Flying capacitors per phase	0	(q-1)(q-2)/2	0
DC bus capacitors	(q-1)	(q-1)	Depends on type of supply
Voltage unbalancing	average	High	Very small

1.2.1 Recent advances in MLIs

Since the introduction of MLIs, different new topologies have been proposed. Often, the proposed inverters are the hybrid forms of the conventional MLIs. Some advanced multilevel converters have also been proposed in literature [8].

One such hybrid topology, named as the *H-bridge NPC (HNPC)* was proposed by C.M. Wu *et. al.* in the year 1999 [41]. The HNPC topology uses the H-bridge connection of the two classical 3-level NPC per leg, forming a 5-level HNPC converter. Several 5L-HNPC configurations have been reported in literature, where 24- or 36-pulse diode bridge rectifiers are used with MV-IGBTs, IEGTs, or GCTs, up to 7.8-kV output voltage, 120-Hz output frequency and 120 MVA output power [42-43]. As with the traditional H-bridge, the converter needs isolated power supplies. The disadvantage of having bulky phase-shifting transformer is partially compensated with the attractive feature of enhanced input side power quality.

Recently, J. Meili *et. al.* introduced another variant of the ANPC concept, which was realized by connecting the 3L-ANPC leg with a three-level FC power cell [44], which forms a five-level converter. The added FC cell increases the voltage levels and introduces more redundant states to balance the FC voltages. However, these advantages are partially marred by circuit complexity, issues related to the initialization and balancing of FC voltages along with the NPC neutral point voltage balancing. A commercial version of this topology has been introduced, aimed at medium voltage (6–6.9 kV) but not high power (0.4 to 1 MVA), with a maximum output frequency of 75 Hz [42].

Another multilevel converter configuration, which has recently found industrial applications, particularly in the HVDC transmission system is named as *Modular Multilevel Converter (MMC)* [45]. This topology was proposed by R. Marquardt in the early 2000s [46]. The MMC topology is composed by series connected half-bridge inverters. The attractive feature of this topology is its modularity and scalability to implement medium and high-voltage levels. It also improves the supply side power quality, compared to the two-level converter configuration used in HVDC. However, the capacitors used in this topology are floating, calling for an appropriate voltage balancing technique [47].

A three-level inverter, which is realized by cascading two two-level conventional VSIs is also reported [48]. This topology doesn’t require clamping diodes, neutral point fluctuations are absent and needs only two isolated power supplies as compared to three in the case of

CHB converter. The proposed circuit can be operated as a conventional two-level inverter in the lower modulation region, by clamping one of the inverters. However, three switches of this topology are to be rated to block the entire dc-link voltage. When this power circuit is operated with a single dc power supply, the issue of capacitor voltage balancing arises as in the case of the NPC 3-level inverter. However, it can be avoided by using the redundancy in the switching states.

1.2.2 Open-End Winding Induction Motor drives

Two-level VSI driven induction motor drives are being employed in a wide variety of industrial and transportation applications as they offer advantages such as low-cost and robustness. Also, it is easier to manufacture and maintain two-level inverters.

On the other hand, the general requirement of lowering harmonic distortion, reduction of switching stress on power semiconductor devices (by lowering dv/dt), enhancing the efficiency by lowering switching frequency, avoidance of insulation stress to enhance reliability of the motor are better served by MLIs compared to the conventional two-level VSI. Therefore, it is an advantageous proposition to obtain multilevel inversion using two-level VSIs as the basic building blocks. Such a power circuit configuration would inherit ruggedness (i.e. reliability) from the 2-level VSI and all of the above mentioned advantages pertinent to the multilevel inverters.

The Open-End Winding Induction Motor Drives (OEWIMDs) are conceived to achieve this objective [49].

The open-end winding configuration is obtained by opening the star-point for star-connected stator windings, or the end-connections of a delta-connected stator winding of an electric machine as shown in Fig. 1.2 (a). Thus, six ends of the open-stator windings are brought out and are fed with two two-level conventional VSIs from either end. Such a power circuit-configuration is termed as the “Dual-Inverter fed Open-End Winding Induction Motor Drive”. As mentioned earlier, the main feature of the open-end winding topology is that, it uses the conventional two level VSIs to achieve multilevel inversion. It may be noted that,

overall dc-link voltage is shared between the two constituent inverters, the voltage blocking capability of the switching devices remains the same.

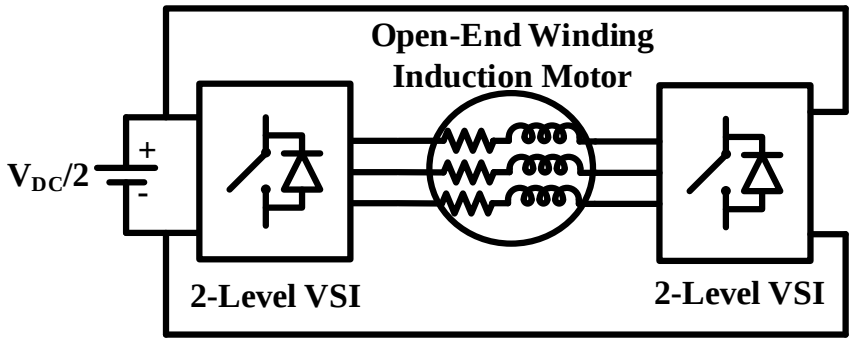
It is interesting to note that, the OEWIMD is very flexible and offers several possibilities in terms of the selection of VSI topologies, the distribution of input dc voltage levels and the switching strategies adopted for the control of VSIs.

The first three-level OEWIM, which is similar to the NPC converter was proposed by H. Stemmler *et. al.* [49]. The authors suggested two topologies in this paper are shown in Fig. 1.9 to realize three-level inversion. The main features of these topologies are absence of clamping diodes, flying capacitors and a lower number of isolated power supplies as compared to the NPC, FC and CHB MLIs respectively. Another advantage with this topology is that the dual-inverter system is capable of providing a total of 64 space vector combinations, as each two-level VSI is capable of assuming 8 states independently of the other. These 64 switching states are distributed over 19 space vector locations (or vectors). In contrast, the conventional 3-level VSIs provide only '27' switching states and 19 vectors. It may therefore the intuitively reasoned out that the dual-inverter fed OEWIMD, on account of its redundancy, offers more flexibility to devise PWM algorithms to control it.

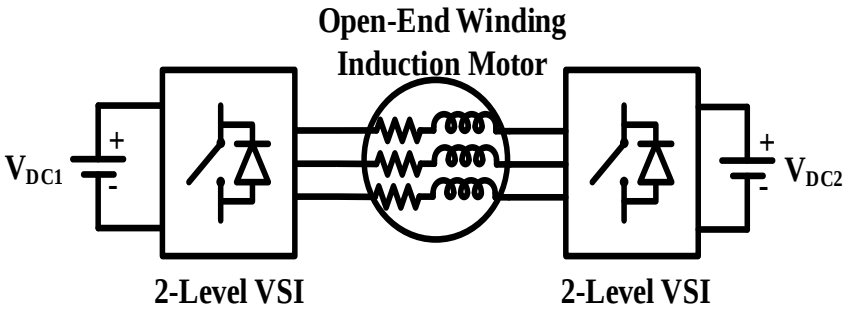
The topology proposed in Fig. 1.9 (a) uses the common dc-link voltage for both of the inverters (i.e. same voltage rating), which are identical. However, common dc rails provide path for the circulation of zero-sequence currents (ZSCs). The ZSC doesn't participate in the process of electromechanical energy conversion. It is deleterious to both motor as well as the semiconductor devices on account of the presence of harmonic components of triplen order. Thus, the presence of ZSC causes the derating of the motor and demands higher current rating of semiconductor devices, increasing the cost and reducing the reliability. In [49], the ZSCs are suppressed by using zero-sequence chokes. Thus, the overall system is bulky and expensive.

T. Boller *et. al.* proposed a five-level inverter system using two 3-level NPC MLIs with a single dc-link and used a new synchronous optimal PWM to operate the entire drive at

low switching frequency [50]. The proposed PWM is capable of reducing the harmonic distortion, the common mode voltage and the size of common mode inductors.



(a)



(b)

Fig. 1.9: Open-End Winding topologies for realization of three-level operation with symmetric power supplies. (a) Single dc-link (b) Isolated dc-links

The dead-time and the voltage drop across the switching devices have been identified as the sources for circulating currents by A. Somani *et. al.* [51]. The issue of dead-time compensation for the OEWIMD was addressed by using a pulse based dead-time PWM strategy [52]. However, the common mode voltage due to the device voltage drops is eliminated by using the common mode-choke.

Another three-level inverter topology with reduced switch count was proposed by S. Figarado *et. al.* [53] for the dual-inverter fed OEWIM drive with a common dc-link. However, in this work, only those switching vectors, which give zero value of common-mode voltage are selected by the PWM strategy to eliminate the common mode voltages leading to the underutilization of switching resources.

A PWM switching strategy was proposed to suppress the zero sequence currents of 3-level OEWIM for all of the switching space vector combinations by V.T. Somasekhar *et. al.* [54]. The proposed PWM strategy improves the dc-link utilization. However, the proposed PWM strategy uses four additional bidirectional switching devices to eliminate the triplen harmonic currents.

V. T. Somasekhar *et. al.* proposed two more PWM strategies to eliminate the zero-sequence voltages in the average sense, which are named as Sample-Averaged Zero-Sequence Elimination (SAZE) and Decoupled SAZE (DSAZE) PWM techniques [55, 56]. With these two PWM techniques, it is possible to operate the OEWIMD with a single dc power supply. However, with these PWM strategies the overall dc-link utilization is reduced by 15% compared to the case of the OEWIMD, which is operated with two isolated dc power supplies.

The topology illustrated in Fig 1.9 (b) uses two isolated dc power supplies isolated by two transformers instead of Fig. 1.9 (a) [49]. The employment of two isolated dc-sources prevents the circulation of the zero-sequence (constituted by the harmonic components of triplen order), resulting in the employability of all space vectors. Furthermore, the OEWIMD with two isolated dc power supplies exhibits a fault tolerant capability (i.e. if one inverter fails the system can still be operated with the healthy inverter at a reduced power level). If the input dc-power supplies of the dual-inverter systems have their voltages in the ratio of 1:1, then 3-level operation is achieved. The sine-triangle PWM (SPWM) technique was used to obtain multilevel inversion in the work reported in [49]. However, the employment of SPWM technique leads to the under-utilization of the overall dc-link voltage by a factor of 15% compared to the employment of the Space Vector PWM (SVPWM) scheme.

A space vector based PWM technique was proposed to the 3-level OEWIM by E.G. Shivakumar *et. al.* [57]. This technique improves the dc-link utilization by 15%. However, the PWM technique proposed in this work is very complex to implement and uses the hysteresis comparators to identify the sectors. Another SVPWM strategy proposed by M. R. Baiju *et. al.* to the 3-level OEWIM with symmetrical power supplies in Fig. 1.9 (b) [58]. The proposed

PWM technique was implemented by using instantaneous phase voltage references and doesn't require any look-up tables and sector identification. J. Kalaiselvi *et. al.* suggested several conventional and hybrid PWM techniques to eliminate or reduce the common-mode voltages and bearing currents for the 3-level OEWIM drive [59].

Recently, A. D. Kiadehi *et. al* proposed a near-state based decoupled PWM (NSPWM) technique [60]. In this PWM technique, the reference vector is built by switching the three nearest active space vectors, while clamping one phase to positive dc-rail or negative dc-rail. The NSPWM is able to minimize the voltage THD. However, the null vector states are underutilized and to avoid the limitation on the range of modulation index, adjustable phase angle displacement was implemented to extend the range of voltage.

K. A. Corzine *et. al.* suggested different methods to obtain multilevel inversion for the circuit topology shown in Fig. 1.9(b) [61]. It is shown that, if the two power supplies of the dual-inverter system are asymmetric, then there is a possibility to obtain more than three-levels. If the $V_{DC_2} = \frac{1}{2}V_{DC_1}$, in the circuit topology shown in Fig. 1.9 (b), some of the voltage space vectors overlap and voltage pattern is identical to that of a four-level inverter. The circuit diagram for the four-level OEWIMD with unequal dc-link voltages is shown in Fig. 1.10. The corresponding space vector diagram of Fig. 1.10 is shown in Fig. 1.11, which exhibits 64 space vector combinations and are spread over 37 locations. The authors made a detailed comparison between the conventional three-level, four-level inverters and the three-level, four-level inversion obtained by the open-end winding configuration.

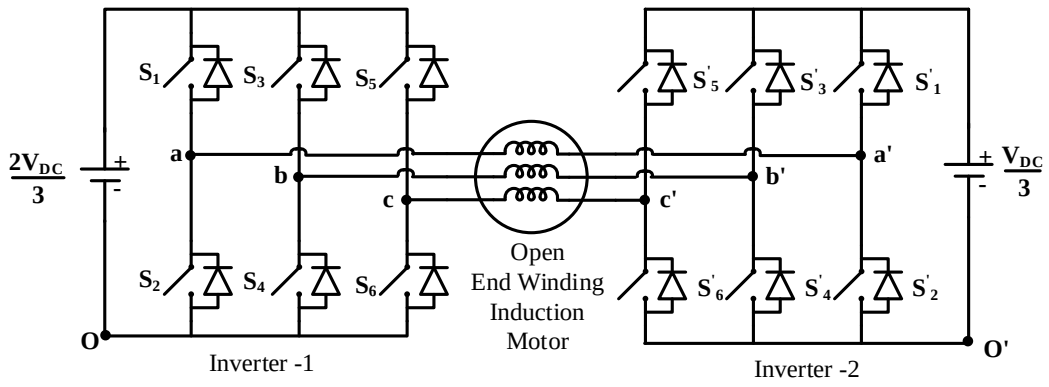


Fig. 1.10: Four-level OEWIMD with unequal dc-link voltages

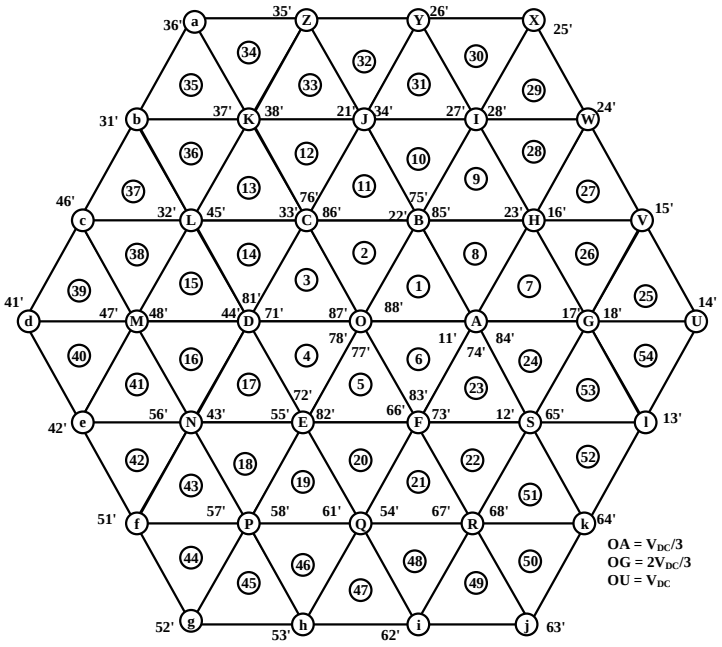


Fig. 1.11: Space vector diagram of four-level OEWIMD

An elegant and simple SVPWM strategy was proposed for the circuit topology in Fig. 1.10 with asymmetric voltage sources by V T Somasekhar *et. al.* [62]. The proposed SVPWM technique requires only the instantaneous phase references in all of the sectors and the modulation waveform was controlled based on the speed of the OEWIM drive. However, it uses the hysteresis comparators to identify the sector information. A controlled dc-link voltage is required, otherwise the inverter with higher dc-link voltage capacitor can overcharge the inverter with lower dc-link voltage capacitor for some of the space vector combinations [62]. In the proposed SVPWM, exploiting the redundancy of vector combinations, those problematic space vectors are avoided to get four-level inversion.

V. Oleschuk *et. al.* suggested a novel space-vector based continuous and discontinuous PWM strategies, named as synchronized PWMs, for the control of dual-inverter fed OEWIM drive [63]. The proposed PWM technique provides a continuous controlled power sharing between the two VSIs, based on their individual voltage magnitudes and also avoids even harmonics and sub-harmonics in the output voltage of the OEWIM drive. However, in the proposed method with continuous PWM, both of the inverters are switched, resulting in an increased switching power loss. On the other hand, the discontinuous PWM technique results in a reduced switching loss and better THD compared to the continuous PWM.

A simple SVPWM based algorithm was proposed to the four-level OEWIM by G. Shiny *et. al.* [64]. This PWM scheme doesn't use the sector information to realize the space vector reference. However, to realize the four-level operation by using OEWIM, one 3-level inverter (formed by cascading of two 2-level inverters with symmetric dc power supplies) as well as one 2-level inverter are used, which increases the switch count. Also, in the cascaded inverter structure, some of the switches are constrained to block the total input dc-link voltage.

As the four-level OEWIM drive is plagued with the problem of overcharging (i.e. the lower dc-link voltage capacitor is charged by the higher dc-link voltage capacitor). B. Venugopal Reddy *et. al.* suggested two decoupled SVPWM techniques to avoid the overcharging phenomenon of the lower dc-link voltage capacitor [65]. The two PWM techniques are named as the Equal Switching Duty PWM (EDPWM) and the Proportional Switching Duty PWM (PDPWM). It is shown that the later PWM scheme reduces the switching losses by 10% compared to the former. Though the proposed techniques are able to avoid the overcharging phenomenon, both inverters are switched during every sampling time period causing higher switching power losses.

To eliminate the overcharging phenomenon in the four-level OEWIMD, a new topology was suggested by B. V. Reddy *et. al.*, named as the *nested rectifier-inverter* topology [66]. In this topology, the dc rails are common to both of the inverters and hence there is a provision for the circulation of zero-sequence currents. The DSAZE and SAZE PWM techniques, which were originally proposed for the conventional OEWIMD shown in Fig. 1.9 (a) are extended to this power circuit configuration also [66-67]. The advantage of the nested rectifier-inverter topology is that, a total dc-link voltage of 0.77 PU is sufficient to apply 1.0 PU voltage to the motor phases for the four-level OEWIMD. However, the nested rectifier-inverter topology uses the 3-isolated dc power supplies, which makes the drive expensive and bulky.

A new power circuit configuration was proposed to avoid the overcharging of the lower dc-link voltage capacitor and to the achieve four-level inversion for the OEWIMD [68].

The proposed power circuit segments the motor phase winding into two groups, which are in the ratio of 2:1 and with each group forming an isolated neutral to deny a path for the circulation of ZSCs. Also, each group of motor phase windings are fed with two 2-level inverters with common dc-rails. The proposed topology enhances the dc-bus utilization by 33% and uses the decoupled SVPWM technique. However, the proposed topology is suitable only for induction motors with 6*n* (n = 1, 2, ...) number of poles and because of the employment of the decoupled strategy, both inverters are to be switched, which increases the switching power loss of the dual-inverter system.

S. Chowdhury *et. al.* proposed a new topology for the three-phase OEWIMD [69] to realize four-level inversion. The proposed topology uses a single dc voltage source for the main inverter and the second inverter is connected to a floating capacitor bank. Thus, the proposed topology avoids one bulky isolation transformer and results in the cost reduction of the drive system. To achieve multilevel operation, the redundant switching states are used to maintain the second inverter voltage at half of the main inverter dc-link voltage (i.e. 2:1). The floating capacitor inverter is operated as the conditioning inverter to improve the waveform quality. A modified decoupled SVPWM scheme was used in the proposed topology to avoid unwanted levels in the phase-voltage waveform during the dead-time intervals and to improve the waveform quality. However, when the reference space vector lies in the outer hexagon, the available switching states to charge the capacitor are limited to two in each sector. Due to the lack of capacitor charging states in the outer sectors (space vector locations U-Z and a-l, Fig. 1.11) the dc-link capacitor of the floating bridge shows a tendency to discharge. This discharge phenomenon is further aggravated as the motor draws active power. Because of these two restrictions on the floating capacitor, the modulation index is limited to 0.66 only. As a result, the usable phase-voltage levels are restricted to nine, compared to fourteen for the circuit topology shown in Fig. 1.10, where the dc sources are operated in the ratio of 2:1. Thus, in this topology, the dc-link voltage utilization is reduced by 33% compared to the one shown in Fig. 1.10. It is also worth noting that the singly supplied OEWIMD, shown in Fig. 1.9 (a), results in an under-utilization of the dc-link voltage by 15% only. As the topology suggested in [69] uses the modified decoupled PWM strategy, where both inverters are switched, the switching power loss is increased. It was proven by the authors that the overall efficiency of the topology proposed in [69] is on par to the 3-level NPC, but lesser than the OEWIMD operated with symmetric voltage supplies (which results in three-level operation).

1.2.3 Closed loop operation of OEWIMD

A lot of literature is available on the open-loop control methods, which were applied to the dual-inverter fed OEWIMD. These methods aim to reduce the losses, dv/dt, reduction/elimination of CMVs, and the avoidance of capacitor overcharging phenomenon. The reference signal generation for open-loop control doesn't require any measurement and is typically employed, where dynamic performance is not a critical issue.

The drawbacks associated with the open-loop control methods can be reduced, if closed-loop control is used [70]. In the case of close-loop control, the controller has to follow one or more references, which are either defined by the user and/or another controller. The reference signals may correspond to currents, voltages, torque, fluxes, active and reactive powers. The output of the controller is input to the modulator to generate the gating signals for the semiconductor switching devices. This approach has become very popular in MV high power industrial drives. The commercially implemented closed-loop control techniques are: i) The Field-Oriented Control (FOC) and ii) The Direct Torque Control (DTC) [70].

A limited literature is available for the closed-loop control of OEWIMD. M. N. Surya Prakash *et. al.* extended the conventional FOC technique to the 3-level OEWIMD with isolated power supplies [71]. However, the implementation of FOC is cumbersome as it needs: i) coordinate transformation, ii) field orientation, iii) tuning of inner current loops, which is often complex and iv) decoupling of $'q'$ and $'d'$ variables [72-74].

Arbind Kumar *et. al.* proposed two variants of DTC control strategies to the 3-level OEWIMD based on the SVPWM technique and imaginary switching times [75-76]. These methods avoid the hysteresis controllers and reduce the switching losses by reducing the switching frequency. K. I. Nirsha *et. al.* proposed a DTC technique for the 3-level OEWIMD with a single dc-bus [77-78]. This DTC technique avoids the CMVs, while accounting for the effect of stator resistance in the calculation of flux at low speeds, facilitating accurate selection of voltage vectors. Recently, B. R. Vinod *et. al.* proposed a 5-level DTC strategy to the OEWIMD fed with two 3-level isolated cascaded inverters [79].

These DTC techniques avoid the drawbacks of the FOC technique as well as the disadvantage associated with the variable switching frequency operation. However, the DTC strategy depends on the stator resistance of the motor and results higher ripple in the steady-state torque.

The emergence of fast and powerful digital controllers paved way to a new gamut of control techniques, which are named as *Model Predictive Control (MPC)* techniques. The MPC techniques are relatively recent and are very promising for applications pertaining to the control of power electronic converters and motor drives [80]. The advantages of the MPC technique include: i) simplicity of implementation, ii) quick response, iii) multivariable control and iv) the ability to handle more nonlinear constraints [80-82]. In spite of these positive features, the MPC suffers from the draw backs such as: i) dependence on the system model parameters, ii) increased number of prediction horizons to compensate for the delay in calculation, iii) complicated estimation of unmeasurable state components, iv) difficulty in selecting the weighting factors if the controlled variables have different units and/or magnitudes and v) variable switching frequency [80-86]. Though some of the aforementioned problems are solved [87], the tuning of the weighting factor is still a challenging task in the implementation of MPC.

The Predictive Torque Control (PTC) strategy is similar to the DTC technique in several aspects [80]. In the PTC controlled drives, the torque and the flux are controlled by choosing the optimal switching vector with the help of the measured and their predicted values of speed, flux, currents and torque. A detailed comparison and implementation between the PTC techniques and the *Predictive Current Control (PCC)* (where in the motor phase currents are taken as references to control the dynamics of the drive) techniques was explained by B. Zhu *et. al.* [88]. However, the PTC technique suggested in [88] needs a judicious selection of the flux weighting factor for both of the MPC techniques. All of the voltage space vectors (i.e. 19 in case of 3-level OEWIM) are to be evaluated in one sampling time period, which further increases the burden on the controller.

K. V. Praveen Kumar *et. al*. implemented PTC for four-level open-end winding induction motor drive [89]. The authors selected the voltage vector based on the speed of operation of the OEWIMD. However, the proposed PTC technique needs judicious selection of weighting factor.

K. M. R. Eswar *et. al.* proposed a modified PTC strategy for the four-level OEWMD [90], which eliminates the requirement of weighting factor for the torque and the stator flux control objectives. However, the proposed scheme calls for a complex ranking-based approach, which restricts its applicability when more constraints are added to the cost function [90]. Furthermore, the proposed strategy requires trigonometric functions, which cause additional computational burden to the processor.

1.3 Applications, advantages and disadvantages of dual inverter fed OEWIND

The advantages of the dual-inverter fed OEWIMD as compared to the existing MLI topologies are:(i) redundancy in the space vector locations, which offers the possibility to implement several interesting PWM schemes [63-65] (ii) capability of operating under faulted conditions (iii) absence of clamping diodes (when compared to the NPC MLI) (iv) avoidance of the problems associated with voltage imbalance of floating capacitors (when compared to the FC MLI) and (v) employment of lower number of DC sources (as compared to the CHB MLI).

The principal drawbacks are: (a) presence of Zero-Sequence Voltages in the motor phase windings (b) overcharging of the lower dc-link voltage capacitor by its counterpart, when the OEWIMD operates with asymmetric power supplies and (c) the requirement of additional cabling. The ZSVs cause zero-sequence current, which causes an additional power-loss in the motor and calls for a conservative peak current rating of the power semiconductor devices.

The application of dual-inverter is advantageous where the isolated power supplies are inherent. One of such applications is a battery powered Electric Vehicle (EV) or a hybrid EV [91-92]. Another application is a grid connected PV system, where two separate PV arrays can be used to supply individual inverters [93-94]. The dual-inverter system can be used in ship propulsion and water pumping applications also [95-96].

Furthermore, OEWIMDs can be considered for the conventional induction motor drive applications such as compressors, blowers, fans etc., if the motor is not far from the dual-inverter system.

1.4 Motivation

The following observations are made on the dual-inverter fed Open-End Winding Induction Motor Drives from the literature review:

i) The OEWIM drive can achieve either three-level or four-level operation by operating the dual-inverter system with equal or unequal dc-input-voltages respectively.

ii) The three-level OEWIMD is realized either by a single dc-power supply or two isolated dc power supplies. When two isolated power supplies are employed, the zero-sequence current can't flow because of the lack of a return path.

iii) In literature, different PWM schemes and control strategies are proposed for 3-level OEWIMD. The objective of some of these PWM schemes is to reduce the common-mode voltage or eliminate it completely in the average sense. Also, some PWM schemes improve the dynamic performance by reducing the flux and torque ripple.

iv) A limited literature is available on the four-level OEWIMD. The four-level operation can be achieved by operating two isolated dc power supplies of the dual-inverter system in the ratio of 2:1.

v) The four-level OEWIMD shown in Fig. 1.10, mainly suffers from two problems. They are: (i) the lower dc-link voltage capacitor is overcharged by the higher dc-link voltage capacitor (ii) the presence of zero-sequence current (ZSC) in the motor phase windings. However, as mentioned earlier, the ZSC can be avoided by denying a path for the zero-sequence current by using two isolated dc-power supplies.

vi) The overcharging problem can be overcome by using the nested rectifier-inverter topology and also by the employment of appropriate PWM techniques (SAZE & DSAZE). However, this topology needs three isolated dc power supplies.

vii) To avoid one isolated power supply (which generally requires a bulky isolation transformer), a dual-inverter system with one floating-bridge capacitor was also suggested, wherein, the charging and discharging switching sequences are used to control the floating bridge. However, the overall efficiency of this drive is low and the dc-link voltage is underutilized by 33%.

viii) Also, the advanced closed-loop control techniques like Model Predictive Current control were not considered for the four-level OEWIMD to enhance the drive performance.

Owing to the above observations, the performance of the four-level OEWIMD with isolated power supplies can further be improvized by reducing losses in the dual-inverter system. This objective should be achieved along with (a) avoidance of overcharging of the dc-link capacitor of lower voltage (b) suppression/elimination of zero-sequence currents and (c) avoidance of more than two isolated dc-power supplies.

1.5 Objectives

The research work presented in this thesis has the following objectives:

1. The first objective is to investigate about the applicability of discontinues PWM techniques to the four-level OEWIMD, to achieve waveform symmetries, while avoiding the overcharging phenomenon of the dc-link capacitor with lower voltage and the flow of the zero-sequence current.

2. The second objective is to formulate improvized SVPWM strategies to eliminate the overcharging phenomenon and to enhance the performance of the OEWIMD.

3. The third objective is to investigate the possibility of operating the nested rectifier-inverter topology with only two isolated dc-power supplies (as against three reported in the literature) to improve the reliability of the drive system. This objective is also coupled to the requirements of suppressing the zero-sequence current and reducing the power loss in the dual-inverter system.

4. The fourth objective is to implement Model Predictive Control (MPC) algorithm to control the load currents of the drive and to introduce the discontinuous PWM technique in the control algorithm to reduce the switching loss.

5. Simulating all of the proposed PWM schemes, circuit topologies and validating them with experimentation.

1.6 Organization of the thesis

The thesis is organized as follows:

Chapter 1 gives the background, literature survey on the existing multilevel inverters and presents their advantages and disadvantages. This chapter also presents the challenges associated with the dual-inverter fed open-end winding induction motor drive and its advantages and disadvantages as compared to the existing multilevel inverters. The motivation, objectives and the thesis structure are also presented in this chapter.

Chapter 2 presents the four-level open-end winding induction motor drive. The four-level operation is achieved by operating the dual-inverter system with dc-link voltages in the ratio of 2:1. The two sources are isolated to deny a path for the circulation of zero-sequence currents. As each inverter is capable of assuming 8 states independently of the other, the resultant space vector combinations of the dual-inverter system are $64\ (8 \times 8)$, which are spread over 37 space vector locations.

The EDPWM and PDPWM techniques are Decoupled PWM techniques. In both of these decoupled techniques, synthesis of the reference space vector is obtained by switching both of the inverters in every sampling time interval. These PWM techniques automatically deploy the space vectors, which don't overcharge the capacitor of inverter-2. However, these PWM schemes incur more switching power loss, as both of the inverters are switched.

The applicability of the discontinuous PWM techniques are investigated to achieve the four-level operation with EDPWM strategy and to reduce the switching power loss. A total of four variants of Discontinuous-Decoupled PWMs (DDPWM) are proposed and named as DDPWM-1, 2, 3 and 4. The proposed PWM techniques achieve the quarter-wave, the half-wave and the three-phase waveform symmetries. With the help of the improvised loss model, it is shown that, the proposed PWMs perform better (in terms of THD and dual-inverter loss) compared to the EDPWM and PDPWM schemes.

As shown in an earlier work [65], for some of the switching combinations, the dc-link capacitor of the inverter (say inverter-2) operating with a lower dc-link voltage of $V_{DC}/3$, is overcharged by its high-voltage counterpart (i.e. the dc-link capacitor with a voltage of $2V_{DC}/3$ belonging to inverter-1). Such an unwanted overcharging can only be avoided by avoiding those problematic switching combinations.

Chapter 3, proposes a 'Biasing Inverter PWM Strategy', where inverter-2 clamps to the nearest sub-hexagonal centers and switches inverter-1 around the clamped inverter i.e. inverter-2. By the strategic placement of the effective time period of the switching inverter, three SVPWM techniques are derived, which are and named as the Center-Spaced PWM, Phase Clamped PWM-1 & Phase Clamped PWM-2.

With the help of the improvised loss evaluation model presented in the chapter-2, it is shown that, the proposed SVPWM techniques display better performance (in terms of dual-inverter power loss) as compared to the proposed discontinuous SVPWM techniques in the chapter-2.

Chapter 4, proposes a new circuit topology, wherein, a rectifier-inverter combination is nested within a conventional 2-level inverter. The conventional inverter feeds one end of the open-end winding induction motor and the nested rectifier-inverter feeds the other end. With an appropriate choice of the dc-link voltages of the nested rectifier-inverter, four-level operation is obtained, which avoids the overcharging of the lower dc-link voltage capacitor. The proposed circuit topology also displays a certain type of fault tolerant capability in that, the motor phase voltage remains unaffected despite the unbalance in the capacitor voltages of the nested rectifier-inverter. The proposed topology is realized with only two isolated dc power supplies as compared to three in the four-level inverter topology reported earlier [66]. With the reduction of the requirement of dc-power supplies, the reliability of the drive system is increased.

The nested rectifier-inverter combination allows paths for the circulation of zero-sequence currents. To suppress the zero-sequence voltages over a sampling time period, in an average sense, the existing DSAZE PWM technique is extended to the proposed topology. However, with the DSAZE PWM scheme, both inverters are switched. To reduce the switching power loss further, a new SVPWM technique, named as the Nested Inverter Clamped SAZE (NICSAZE) PWM is proposed. The proposed NICSAZE PWM technique dynamically balances the zero sequence voltages by clamping the nested inverter having lower dc-link voltage and switching the conventional inverter around the clamped inverter states. The loss model is used to demonstrate the superior performance of the proposed NICSAZE PWM technique as compared to the DSAZE PWM strategy by quantifying the loss of the dual-inverter system.

Chapter 5 presents a Predictive Current Control (PCC) strategy to control the motor phase currents. This algorithm falls in the category of Model Predictive Control (MPC). The detailed implementation of the PCC for four-level open-end winding induction motor is presented. As compared to the PTC, the PCC avoids the tuning of the weighting factor. To reduce the compensation delay and switching frequency, a modified PCC technique is proposed by introducing a discontinuous PWM strategy to select the optimal voltage vector for the dual-inverter system. In the modified PCC, the inverter with lower dc-link capacitor voltage operates with fundamental frequency (i.e. clamped to nearest the sub-hexagon) and

the inverter with higher dc-link capacitor voltage is switched around it. The modified PCC uses only 5 candidate voltage space vectors as compared to the conventional PCC, wherein 37 candidate voltage space vectors are to be evaluated. It is also shown that the proposed algorithm reduces the computational burden on the processor.

All the PWM schemes proposed in this thesis are first simulated using *MATLAB/SIMULINK* and the results are verified by implementing these schemes on a 5-HP, 400 Volts, 50 Hz, 1445 RPM, three-phase open-end winding induction motor with v/f control for different modulation indices covering the entire range of speed. Owing to the limitation of the inverters used in the present study, dc-link voltages of 200 V and 100 V are respectively employed for the individual inverters. The gating pulses to the dual-inverter system are generated using *dSPACE1104*. The agreement between the simulation results and the experimental results demonstrate the validity of the proposed PWM strategies. The principles of all of the proposed PWM schemes are quite general in nature and it is hoped that they are amenable for high power applications also.

Chapter-6 summarizes the results of the research work and discusses the possibilities for further work in this field of research.

1.7 Summary

This chapter presents an introduction to the research work undertaken in this doctoral thesis. The motivation and objectives are clearly spelt out after the introduction of pertinent literature available on this topic, which includes various MLI topologies and the associated PWM schemes.

The Open-End Winding Induction Motor Drives are introduced in general, and four-level OEWIMD is discussed in particular. Finally, this chapter presents the organization of this thesis.

Chapter 2

Discontinuous Decoupled SVPWM Schemes for a Four-Level Open-End Winding Induction Motor Drive with Waveform Symmetries

Contents

2.1 Introduction

As discussed in Chapter-1, in an Open-End Winding Induction Motor Drive (OEWIMD), the stator windings of a 3-phase induction motor are opened and are fed with a two-level inverter from either side. While the the conventional motor is considered as a separate entity for the MLI configurations considered in Chapter-1, it is an integral part of the drive system in the case of an OEWIMD. It was shown that it is possible to derive multilevel phase voltage waveforms from this power circuit configuration [59-61]. The advantages and limitations of this configuration compared to the other MLI topologies are well documented [62].

OEWIM drives can find applications wherein employment of two individual dc power supplies is not considered to be disadvantageous. Some of the the potential applications for the OEWIM drive include: (i) electric vehicles [91-92], (ii) electric propulsion of ships [95] and (iii) aircraft motion control [100].

The work reported in [62] describes a four-level OEWIMD. This topology is realized by feeding either end of the open-stator windings of an induction motor with two 2-level VSIs with unequal dc-link voltages. These dc-link voltages are in the ratio of 2:1. This drive has a disadvantage in that, the lower voltage dc-link capacitor is overcharged by the dc-link capacitor of higher voltage [65].

The problem of overcharging of the lower dc-link capacitor is tackled with the Decoupled SVPWM techniques reported in [65]. Two variants of the Decoupled SVPWM schemes were described in [65], namely the Equal Duty PWM (EDPWM) technique and the Proportional Duty PWM (PDPWM) technique. In both of these schemes, the reference voltage space vector of the dual-inverter scheme is resolved into two anti-phased references for the individual inverters, which are in the ratio of 2:1. These individual reference voltage vectors are then synthesized with the respective inverters. It was shown that, compared to the EDPWM scheme, the PDPWM scheme results in 10% lesser switching power loss in the dual-inverter system [65]. These Decoupled SVPWM schemes make use of the concepts developed in [101] to obtain the Quarter-wave, Half-wave and the Three-phase symmetries.

This chapter presents Discontinuous Decoupled SVPWM (DDPWM for the rest of the chapter) techniques for a four-level OEWIMD shown in Fig. 2.1. Admittedly, these PWM schemes are well known for a simple two-level VSI. However, the extension of these PWM techniques for the four-level OEWIMD is not straight forward on account of the unsymmetrical nature of the power circuit. It is an interesting proposition to derive the switching patterns to implement the DDPWM scheme (to lower switching power losses) and derive all of the aforementioned waveform symmetries from an unsymmetrical network with DDPWM schemes.

In this chapter, a critical comparison of the DDPWM schemes with the EDPWM and the PDPWM schemes is also undertaken. To this end, an improvised loss model is devised to evaluate the conduction and the switching power losses in the dual-inverter scheme. Also, this model facilitates the evaluation of various indices of performance such as THD and WTHD.

Simulation and experimental results indicate that the DDPWM techniques perform better compared to the Decoupled Center spaced SVPWM techniques, while avoiding the overcharging of the capacitor of the lower voltage dc-link.

2.2 Mathematical Model of a Four-Level OEWIMD

The power circuit configuration of the OEWIMD described in [62] is reproduced in Fig. 2.1 to facilitate an easy reference. Two unequal dc sources, which are in the ratio of 2:1 feed an open-end winding induction motor from either side. Inverter-1 is fed with a dc-link voltage of $2V_{DC}/3$, while inverter-2 is fed with a dc-link voltage of $V_{DC}/3$. The states of inverter-1 and inverter-2 are numbered 1-8 and $1'$ to $8'$ respectively, as shown in Fig. 2.2. The resultant space vector diagram of the dual-inverter system with 64 (8x8) space vector combinations, spread over 37 locations with 54 sectors is shown in Fig. 2.3. Table 2.1 shows the states offered by the individual inverters. The pole voltages of inverter -1 are denoted as v_{ao}, v_{bo}, and v_{co}. The pole voltages for inverter-2 are denoted as $v_{a'o'}$, $v_{b'o'}$ and $v_{c'o'}$. The pole voltage of inverter-1 (v_{ao}) assumes one of the two possible values amongst $V_{DC}/3$ and $-V_{DC}/3$. Similarly, the pole voltage of inverter-2 ($v_{a'o'}$) toggle between $V_{DC}/6$ and $-V_{DC}/6$. As one might expect, the difference of these pole voltages take four values as shown

in Table 2.2. The sum of motor phase voltages $v_{aa'}$, $v_{bb'}$, and $v_{cc'}$ do not add to zero, indicating that there exists a zero-sequence voltage in the motor phases. This zero-sequence voltage tries to circulate a zero-sequence current in the motor phase windings. The zero-sequence components flowing through the motor phase windings are cophasal, as they are caused by the components of triplen order. Owing to the electrical isolation of the constituent inverters, there exists no return path for the zero-sequence currents to flow in the motor phases. Thus, the zero-sequence currents are prevented in the motor phases.

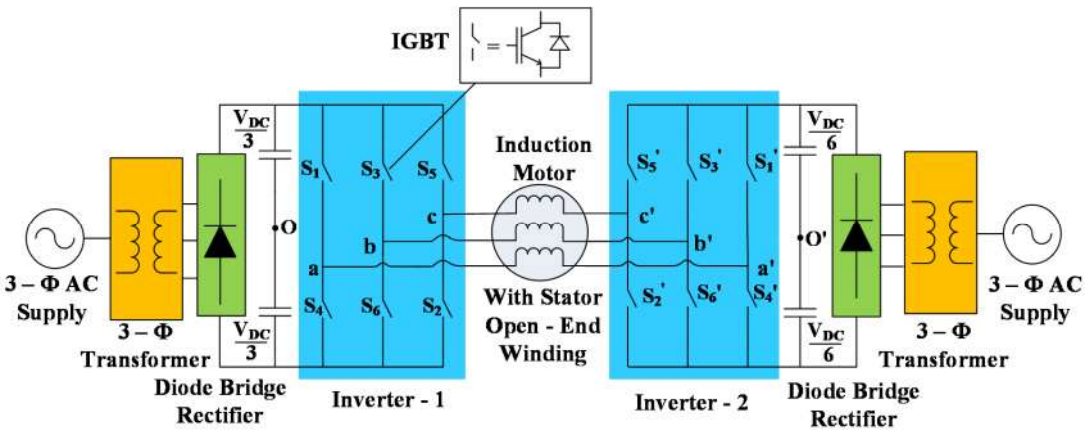


Fig. 2.1: Circuit configuration for four-level OEWIMD

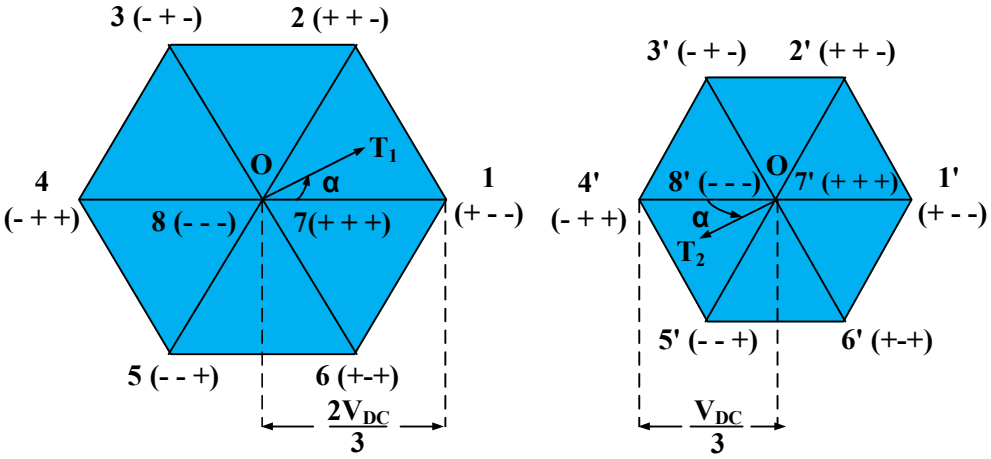


Fig. 2.2: Space vector locations of inverter-1 (left) & inverter-2 (right) (not drawn to scale)

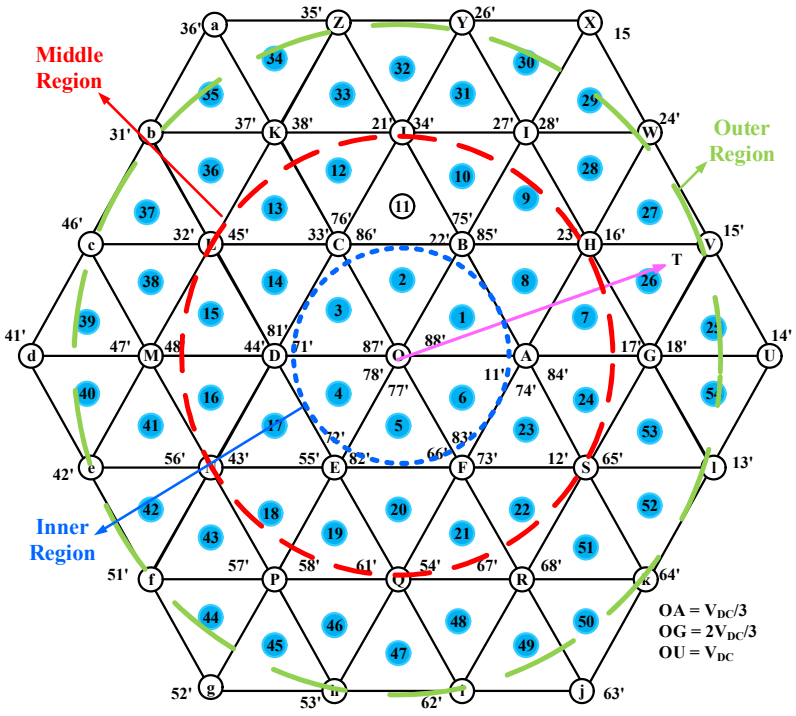


Fig. 2.3: Space vector combinations of dual-inverter system

Table 2.1: Individual switching states of inverters

State of inverter-1	Switches turned ON	State of inverter-2	Switches turned ON
1 (+ - -)	S_6, S_1, S_2	1′ (+ - -)	S_6', S_1', S_2'
2 (+ + -)	S_1, S_2, S_3	2′ (+ + -)	S_1', S_2', S_3'
3 (- + -)	S_2, S_3, S_4	3′ (- + -)	S_2', S_3', S_4'
4 (- + +)	S_3, S_4, S_5	4′ (- + +)	S_3', S_4', S_5'
5 (- - +)	S_4, S_5. S_6	5′ (- - +)	S_4', S_5'. S_6'
6 (+ - +)	S_5. S_6, S_1	6′ (+ - +)	S_5', S_6', S_1'
7 (+ + +)	S_1, S_3, S_5	7′ (+ + +)	S_1', S_3', S_5'
8 (- - -)	S_2, S_4, S_6	8′ (- - -)	S_2', S_4', S_6'

Table 2.2: Difference of pole voltages

S.No.	v_{ao}	$v_{a'o'}$	Difference of pole voltages $v_{aa'} = v_{ao} - v_{a'o'}$
1	$V_{DC}/3$	$V_{DC}/6$	$V_{DC}/6$
2	$V_{DC}/3$	$-V_{DC}/6$	$V_{DC}/2$
3	$-V_{DC}/3$	$V_{DC}/6$	$-V_{DC}/2$
4	$-V_{DC}/3$	$-V_{DC}/6$	$-V_{DC}/6$

The mathematical modeling equations of induction motor are given as:

$$I = L^{-1}\lambda \tag{2.1}$$

$$\dot{\lambda} = \Omega\,\lambda - R\bar{I} + I_4\bar{V} \tag{2.2}$$

where

$$\bar{I} = \begin{bmatrix} i_{qs} & i_{ds} & i_{qr'} & i_{dr'} \end{bmatrix}^T$$

$$\lambda = \begin{bmatrix} \lambda_{qs} & \lambda_{ds} & \lambda_{qr'} & \lambda_{dr'} \end{bmatrix}^T$$

$$\bar{V} = [v_{qs} \quad v_{ds} \quad v_{qr'} \quad v_{dr'}]^T$$

I_4= 4 × 4 unity diagonal matrix

$$R = \begin{bmatrix} r_s & 0 & 0 & 0 \\ 0 & r_s & 0 & 0 \\ 0 & 0 & r_{r'} & 0 \\ 0 & 0 & 0 & r_{r'} \end{bmatrix}$$

$$\Omega = \begin{bmatrix} 0 & -\omega & 0 & 0 \\ \omega & 0 & 0 & 0 \\ 0 & 0 & 0 & -(\omega - \omega_r) \\ 0 & 0 & (\omega - \omega_r) & 0 \end{bmatrix}$$

$$L = \begin{bmatrix} L_{ls} + L_m & 0 & L_m & 0 \\ 0 & L_{ls} + L_m & 0 & L_m \\ L_m & 0 & L_{lr'} + L_m & 0 \\ 0 & L_m & 0 & L_{lr'} + L_m \end{bmatrix}$$

The current vector, $\bar{I}$ is obtained by solving the eqs. (2.1) and (2.2) and electromagnetic torque can be obtained as,

$$m_d = \left(\frac{2}{3}\right)\left(\frac{P}{2}\right)\left(i_{qs}i_{dr'} - i_{ds}i_{qr'}\right) \tag{2.3}$$

The equation for rotor speed is obtained as,

$$m_d = J\frac{d\omega}{dt} + B\omega + m_L$$

$$\omega = \frac{1}{J}\int (m_d - m_L - B\omega)\, dt \tag{2.4}$$

The induction motor d-q axis voltages are defined from the dual-inverter open-end winding induction motor as,

$$v_{qs} = \left(v_{aa'} \cos\theta + v_{bb'} \cos\left(\theta - \frac{2\pi}{3}\right) + v_{cc'} \cos\left(\theta + \frac{2\pi}{3}\right)\right) \tag{2.5}$$

$$v_{ds} = \left(v_{aa'} \sin\theta + v_{bb'} \sin\left(\theta - \frac{2\pi}{3}\right) + v_{cc'} \sin\left(\theta + \frac{2\pi}{3}\right)\right) \tag{2.6}$$

$$v_{qr'} = \left(v_{aa'r'} \cos\theta + v_{bb'r'} \cos\left(\theta - \frac{2\pi}{3}\right) + v_{cc'r'} \cos\left(\theta + \frac{2\pi}{3}\right)\right) \tag{2.7}$$

$$v_{dr'} = \left(v_{aa'r'} \sin\theta + v_{bb'r'} \sin\left(\theta - \frac{2\pi}{3}\right) + v_{cc'r'} \sin\left(\theta + \frac{2\pi}{3}\right)\right) \tag{2.8}$$

where

$v_{aa'}$, $v_{bb'}$ & $v_{cc'}$ – Stator phase voltages of open-end winding induction motor

θ – angle subtended by the 'q-axis' of the 'dq0' reference frame with respect to the axis of the A-phase winding of the stator

$v_{aa'r'}$, $v_{bb'r'}$ & $v_{cc'r'}$ - Rotor phase voltages of open-end winding induction motor

The difference of pole voltages of open-end winding induction motor are given as,

$$v_{aa'} = v_{ao} - v_{a'o} \tag{2.9}$$

$$v_{bb'} = v_{bo} - v_{b'o} \tag{2.10}$$

$$v_{cc'} = v_{co} - v_{c'o} \tag{2.11}$$

Zero-sequence voltages are defined as,

$$v_z = \frac{1}{3}\left[v_{aa'} + v_{bb'} + v_{cc'}\right] \tag{2.12}$$

The phase voltages of the open-end winding induction motor is determined by assuming the O and O' points of dual inverter drive are at same potential and their expressions are given as,

$$v_{aa'} = v_{ao} - v_{a'o} - \frac{1}{3}v_z \tag{2.13}$$

$$v_{aa'} = \frac{2}{3}(v_{ao} - v_{a'o'}) - \frac{1}{3}[(v_{bo} - v_{b'o'}) + (v_{co} - v_{c'o'})] \tag{2.14}$$

2.3 Discontinuous Decoupled SVPWM Strategies for Four-Level OEWIMD with Equal Duty

The vector ***OT*** (i.e.$|v_{ref}|$) shown in Fig. 2.3 represents the reference voltage space vector for the overall dual-inverter fed four-level OEWIMD system. The vector ***OU*** (Fig. 2.3), which measures V_{DC}, represents the effective dc-link voltage of the dual-inverter topology (the sum of the respective dc-link voltages of individual inverters). The vector ***OT*** is to be produced in the average sense using a suitable SVPWM technique. The reference voltage space vector ***OT*** is sampled 42 times per cycle, irrespective of the fundamental frequency. For a conventional two-level inverter, such a sampling would result in 7 samples per sector. The angular interval between successive samples would then be equal to 8.57^o $(\text{i.e. } 360/42)$ and the first sample of any cycle is placed at 4.28^0, to avoid samples on the sector boundaries. It was shown in [101] that such measures achieve the attainment of the waveform symmetries.

In this work, the proposed SVPWM scheme is applied to the four-level OEWIMD, which is operated in open-loop with v/f control. The rated voltage and the rated frequency of the motor are 400 V (line-line) and 50 Hz respectively. The modulation index of dual-inverter drive is defined as,

$$m_a = \frac{|\boldsymbol{v_{ref}}|}{V_{DC}} \tag{2.15}$$

Further, the overall dc-link voltage (|***OU***|, Fig. 2.3) is scaled in such a way that the rated voltage and the rated frequency are applied at the edge of liner modulation $\left(\text{i. e. } m_a = \sqrt{3}/2\right)$. For the aforementioned motor, the overall dc-link voltage becomes equal to 564 V. Thus, the frequency of the fundamental component of the dual-inverter drive, operated with a modulation index of m_a is given by,

$$f_1 = \frac{m_a}{\sqrt{3}/2} \times 50 \tag{2.16}$$

The sampling time period (T_S) of each inverter of dual-inverter topology can be defined as,

$$T_{S1} = T_{S2} = T_S = T_o/42 \tag{2.17}$$

Where, $T_o = 1/f_1$ the time period of the fundamental component of the dual-inverter drive.

The operating principle of DDPWM techniques are explained with help of Fig. 2.2. The reference voltage vector ***OT*** (Fig. 2.3) of the dual inverter topology is realized with the help of two 2-level VSIs having reference voltage vectors of ***OT1*** (for inverter-1) and ***OT2*** (for inverter-2) as shown in Fig. 2.2. Since the dc-link voltages of respective inverters are in the ratio of 2:1, it is logical to resolve the reference vectors for the individual inverters in the same ratio. It is also obvious that the reference vectors for the individual inverters should be opposite to each other as the motor phase voltage is the *difference* of the individual pole voltages.

Thus, when the reference voltage space vector for the dual-inverter system is equal to $|\boldsymbol{v_{ref}}|\angle\alpha$ (Fig. 2.3), the reference vectors of the individual inverters are $|2\boldsymbol{v_{ref}}/3|\angle\alpha$ and $|\boldsymbol{v_{ref}}/3|\angle(180° + \alpha)$ respectively. For the situation depicted in Fig. 2.3 and Fig. 2.2 (wherein ***OT*** = ***OT1***+ ***OT2***), the vector ***OT1*** is synthesized with inverter-1, by switching

among the states $8-1-2-7$ (states corresponding to sector-1, Fig. 2.2), while the opposite vector $\boldsymbol{OT_2}$ is synthesized by the inverter-2, while switching among the states $8'-5'-4'-7'$ (states corresponding to sector-4, Fig. 2.2).

The switching algorithm presented in [98] for the conventional two-level VSI is extended to the dual-inverter system pertaining to the four-level OEWIMD, by applying it to the individual inverters. This switching algorithm needs only the instantaneous phase reference voltages unlike the conventional implementation of the SVPWM scheme (which needs lookup tables and sector identification).

The above discussion leads to the fact that, if the reference voltage space vector $\boldsymbol{OT}$ (which corresponds to the dual-inverter system) is constructed by the instantaneous phase voltage references ($v_a^*,\ v_b^*$ and v_c^*), then the reference voltage vectors for the individual inverters ($\boldsymbol{OT_1}$ and $\boldsymbol{OT_2}$) are constituted by the sets: $\{2v_a^*/3,\ 2v_b^*/3\ ,2v_c^*/3\}$ (for inverter-1) and $\{\ -v_a^*/3,\ -v_b^*/3\ ,\ -v_c^*/3\ \}$ (for inverter-2).

The algorithm presented in [98] is based on the concept of imaginary switching times. The imaginary switching times for the inverter-1 and inverter-2 are given as,

$$T_{xs1} = \ (T_s/V_{DC}) \times (2v_x^*/3),\ \ x \in a,b,c \tag{2.18}$$

$$T_{xs2} = \ (T_s/V_{DC}) \times (-v_x^*/3),\ \ x \in a,b,c \tag{2.19}$$

The time period during which active power is transferred from the input dc-bus to the output ac-lines of the inverter is called the effective time period and is denoted with the symbol $\boldsymbol{T_{eff}}$. This duration is equal to the sum of the switching periods of the two active states of the pertinent sector. Thus, for the individual inverters of the dual-inverter scheme the $\boldsymbol{T_{eff}}$ defined as [98],

$$T_{eff1} = \ T_{max1} - \ T_{min1} \tag{2.20}$$

$$T_{eff2} = T_{max2} - T_{min2} \tag{2.21}$$

where $T_{max1} = max(T_{as1}, T_{bs1}, T_{cs1})$, $T_{min1} = \min(T_{as1}, T_{bs1}, T_{cs1})$, $T_{max2} = max(T_{as2}, T_{bs2}, T_{cs2})$ and $T_{min2} = min(T_{as2}, T_{bs2}, T_{cs2})$

During the remaining time period of the sampling time interval $\boldsymbol{T_s}$, there is no power flow from the input dc rails to the output ac side of the inverter. This time interval is called as the zero-vector (or the null-vector) time period and is denoted as $\boldsymbol{T_z}$. The null-vector time periods for the individual inverters are given by,

$$T_{z1} = T_s - T_{eff1} \tag{2.22}$$

$$T_{z2} = T_s - T_{eff2} \tag{2.23}$$

The offset time needed for the center spacing of the effective time period within the sampling time interval of $\boldsymbol{T_s}$ for both inverters given as,

$$T_{offset1} = T_{z1}/2 - T_{min1} \tag{2.24}$$

$$T_{offset2} = T_{z2}/2 - T_{min2} \tag{2.25}$$

The phase switching time period of any given phase of the constituent inverters is defined as the time period for which that phase terminal is connected to the positive rail of the respective input dc-bus. It is shown in [98] that the phase switching time periods $\{T_{ga1}, T_{gb1}, T_{gc1}\}$ for inverter-1 and $\{T_{ga2}, T_{gb2}, T_{gc2}\}$ for inverter-2 are related to imaginary switching time periods T_{xs1} and T_{xs2} respectively, by a simple expression,

$$T_{gx1} = T_{xs1} + T_{offset1}, \quad x \in a, b, c \tag{2.26}$$

$$T_{gx2} = T_{xs2} + T_{offset2}, \quad x \in a, b, c \tag{2.27}$$

It could be helpful to recapitulate briefly about the implementation of SVPWM schemes for the conventional two-level inverter, which provides an impetus for the four-level dual-inverter fed OEWIMD. For the conventional 2-level VSI, the PWM strategy implemented with the offset time period given by eq. 2.24 (or 2.25) results in the center spacing of the effective time period ($\boldsymbol{T_{eff}}$) in any given sampling time period. For this reason, this Decoupled PWM scheme is called as the *Center-Spaced PWM* (CSPWM). Two more well-known variants of the PWM scheme, called *Discontinuous Decoupled PWM* (DDPWM) schemes, which are also known as the *Phase-Clamped SVPWM* schemes, are implemented by the placement of the effective time periods at either end of a sampling time period. In the first variant of these two, the *DDPWM-1*, the effective time period is kept at the extreme left corner, while in the other, the *DDPWM-2*, it is placed at the extreme right corner. These two PWM schemes are implemented with simple alterations in the offset time period. The offset time periods of $(-T_{min})$ and $(T_s - T_{max})$, respectively implement *DDPWM-1* and *DDPWM-2* [98]. The switching sequences used for the implementation of these three PWM schemes for the conventional two-level VSI in *sector-1* are depicted in Fig. 2.4. It is assumed that 42 samples are employed per cycle (i.e.7 samples/sector).

It may be noted that the CSPWM employs the conventional sequences 8-1-2-7 and 7-2-1-8 alternatively as shown in Fig. 2.4. It may also be noted that the beginning and ending sequences for *DDPWM-1 r*espectively are 1-2-7 and 8-1-2 (i.e. for samples 1 and 7). The center sample (i.e. sample no. 4) should be so implemented as to facilitate a natural transition between these two sequences. Also, in the interest of symmetry, the effective time period should be center spaced as shown in Fig. 2.4 (middle). Both of these requirements are automatically achieved by implementing the center sample with CSPWM, using the sequence 7-2-1-8 [101]. The switching sequences for the other sectors may similarly be worked out. It then follows that, the center samples of all the six sectors, which are situated at 30^0, 90^0, 150^0, 210^0, 270^0 and 330^0, should be implemented with center spacing [101]. One can devise the switching sequences for DDPWM-2 in a similar manner by choosing the initial, center and end sequences as 2-1-8, 8-1-2-7 and 7-2-1 respectively (Fig. 2.4 (right)).

As mentioned in the earlier section, the reference phase voltages corresponding to the four-level dual-inverter scheme ***OT*** (Fig. 2.3) are resolved in the ratio of 2:1 for the individual

inverters and are anti-phased with respect to each other to implement the *Decoupled SVPWM* scheme [65]. The references of the individual inverters are then synthesized in the average sense using SVPWM technique. The *effective time period*, which is the sum of the time periods during the active vectors are switched ($T_1 + T_2$), is kept exactly at the center of each sampling time interval [65]. The principal drawback of this scheme is that, it calls for the switching of all the three phases of both inverters (i.e. a total of six switching's in any given sampling time interval), causing excessive switching loss.

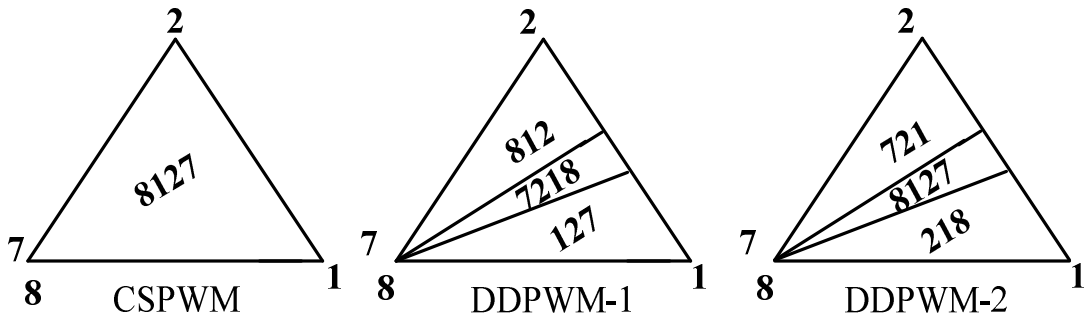


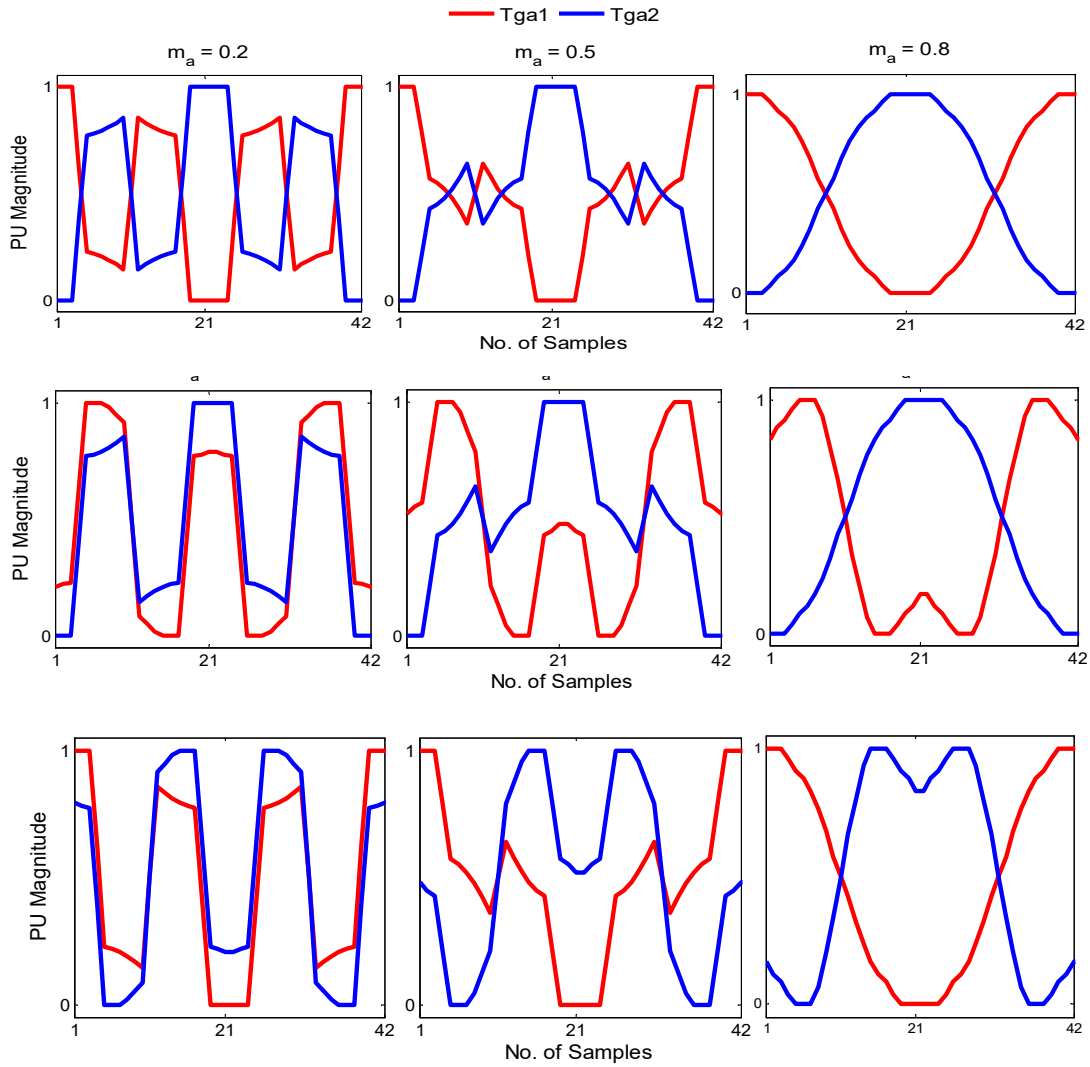
Fig. 2.4: Sequence of voltage vectors applied in sector-I for the conventional 2-level VSI for CSPWM (left), DDPWM-1 (middle), DDPWM-2 (right)

This is the motivating factor to explore the possibilities of implementing the DDPWM schemes for the dual-inverter system. However, deriving waveform symmetries with DDPWM schemes is a difficult proposition due to the lack of symmetry in the structure of the power circuit configuration (Fig. 2.1) as well as the DDPWM schemes.

Table 2.3 demonstrates the switching sequences used for both of the inverters to implement the DDPWM schemes in sector-1 (i.e. for a span of 60^0). As explained earlier, in the decoupled SVPWM scheme, the references of inverter-2 are anti-phased with respect to the references of inverter-1. Consequently, the vectors output by inverter-2 are opposite to those output by inverter-1 (Table 2.3). The modulating signals corresponding to the inner, the middle and the outer regions of the hexagon corresponding to the modulation indices of 0.2, 0.5 and 0.8 are presented in Fig. 2.5. It is easily observed that the inner region corresponds to $m_a \leq 1/2\sqrt{3}$. The middle ant the outer regions respectively correspond to $\left(1/2\sqrt{3} \leq m_a \leq 1/\sqrt{3}\right)$ and $m_a \geq 1/\sqrt{3}$ (Fig. 2.3).

Table 2.3: Switching sequences of DDPWM-1, 2, 3 & 4 in sector-1

Sample No.	DDPWM-1		DDPWM-2		DDPWM-3		DDPWM-4	
	Inverter-1	Inverter-2	Inverter-1	Inverter-2	Inverter-1	Inverter-2	Inverter-1	Inverter-2
1	1-2-7	8-5-4	2-1-8	8-5-4	1-2-7	7-4-5	2-1-8	7-4-5
2	7-2-1	4-5-8	8-1-2	4-5-8	7-2-1	5-4-7	8-1-2	5-4-7
3	1-2-7	8-5-4	2-1-8	8-5-4	1-2-7	7-4-5	2-1-8	7-4-5
4	7-2-1-8	7-4-5-8	8-1-2-7	7-4-5-8	7-2-1-8	8-5-4-7	8-1-2-7	8-5-4-7
5	8-1-2	5-4-7	7-2-1	5-4-7	8-1-2	4-5-8	7-2-1	4-5-8
6	2-1-8	7-4-5	1-2-7	7-4-5	2-1-8	8-5-4	1-2-7	8-5-4
7	8-1-2	5-4-7	7-2-1	5-4-7	8-1-2	4-5-8	7-2-1	4-5-8



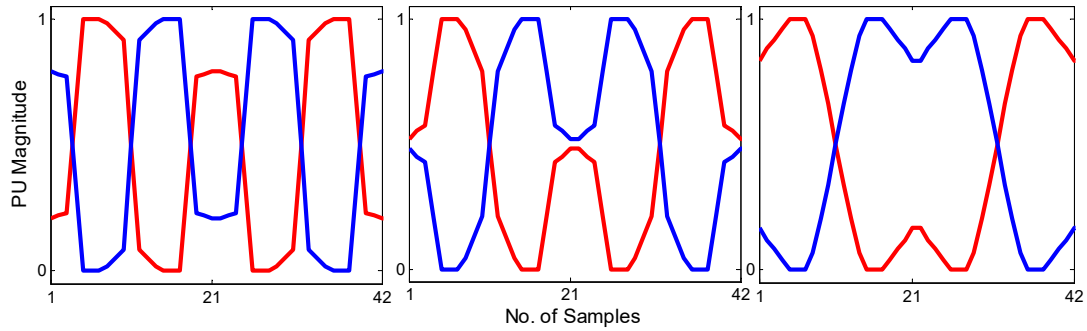
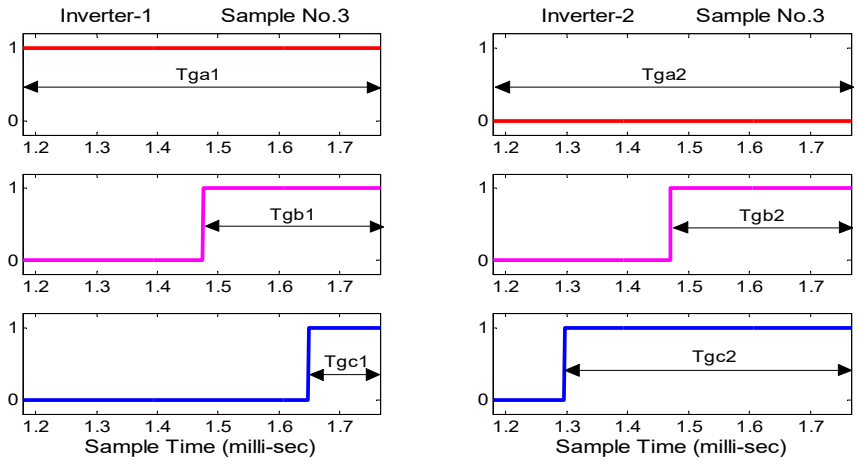
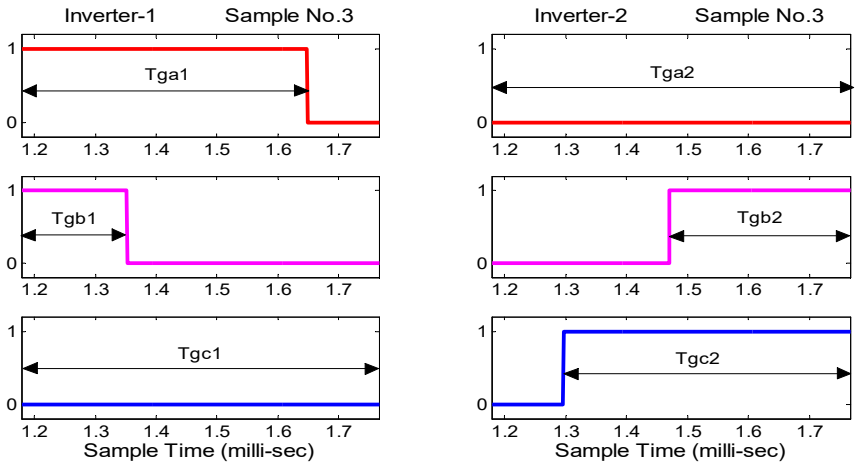


Fig. 2.5: Modulating signals for DDPWM-1 (top), DDPWM-2 (second), DDPWM-3 (third) and DDPWM-4 (bottom)

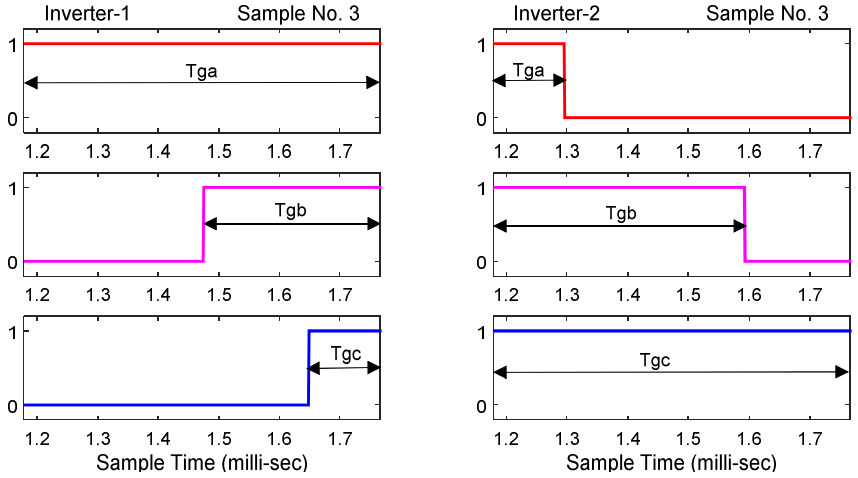
It is evident from the traces presented in Fig. 2.5, that each phase is clamped for 120^0. It may therefore be anticipated that the switching power losses would be less with DDPWM schemes as compared to the decoupled SVPWM strategies proposed in [65]. From the modulating signals it can be observed that, the modulating waves of the individual inverters are in two different shapes and are alternatively assigned to the individual inverters of the dual inverter system to form the four proposed DDPWMs. Fig. 2.6 (a) and Fig. 2.6 (b) present the typical gating signals for the proposed DDPWM-1 & 2 schemes at sample no. 3, (i.e. $\alpha = 21.42^0$). The PWM signals for the other two DDPWM schemes are also similar to the DDPWMs-1 & 2.



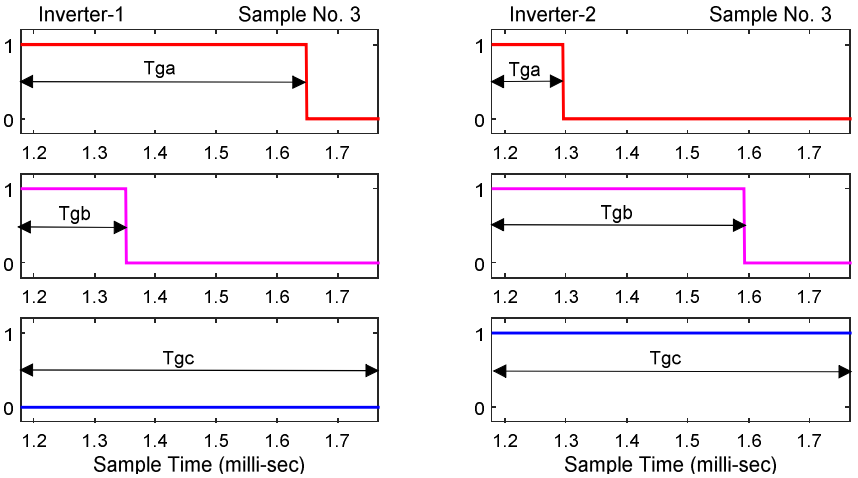
(a)



(b)



(c)



(d)

Fig. 2.6: Simulated switching time periods of inverter-1 (left) and inverter-2 (right). (a) DDPWM-1 (b) DDPWM-2 (c) DDPWM-3 (d) DDPWM-4

From these traces, it is evident that the A-phase is clamped for both of the inverters with DDPWM-1. In contrast, two different phases are clamped in the respective inverters with DDPWM-2 (Phase-A for inverter-1 and Phase-C for inverter-2). Also, the sequence of switching is the same for both of the inverters with DDPWM-1 ('low' to 'high'). However, with DDPWM-2, the sequences are different for the two inverters. It may be observed that while inverter-2 has the same switching sequence as in the case of DDPWM-1, inverter-1 has the reverse switching sequence ('high' to 'low'). This behavior is the direct consequence of the fact that while the modulating functions are identical for inverter-2, they are different for inverter-1 (Fig. 2.5). It may therefore be intuitively reasoned out that DDPWM-1 should result in a better harmonic performance compared to DDPWM-2 on account its structural symmetry. Similar observations and conclusions can be drawn for the DDPWM-3 and DDPWM-4 as well. Fig. 2.6 (c) and Fig. 2.6 (d) respectively show the corresponding switching sequences for DDPWM-3 and DDPWM-4.

2.4 Simulation and Experimental Results

The simulation and experimental results for the four-level OEWIMD, with the proposed DDPWM techniques are presented in this section. The simulation results are carried out using *Matlab/Simulink* software and the parameters used for modeling of the OEWIM are given in Table 2.4.

Table 2.4: Parameters of the OEWIM

Induction motor	**Squirrel cage type, 3-Φ, 50 Hz, 400 V**
Stator resistance (R_s)	4.215 Ω
Rotor resistance (referred to stator) (R_{rp})	4.185 Ω
Stator leakage inductance (L_{ls})	17.52 mH
Rotor leakage inductance (referred to stator) (L_{lrp})	17.52 mH
Magnetizing inductance (L_m)	516.6 mH
Moment of inertia (J)	0.0131Kg m^2
Damping coefficient (B)	0.002985 N/rad/s

The experimental validation is carried out on a 3-phase, 50 Hz OEWIM using open-loop v/f control. The name-plate details of the motor are shown in Table 2.5. For verification, an experimental setup of Fig. 2.1 has been built in the laboratory. Its physical layout and the hardware specifiations are given in Fig. A-1 and Table A1. The experimental

set up consists of an auto-transformer, two isolation transformers, two diode bridge rectifiers, two 3-ph voltage source inverters, a *dSPACE-1104* control platform with a host PC to produce the gating signals and a three-phase OEWIMD.

Table 2.5: Name plate details of the OEWIM

Induction motor	Squirrel cage type, 3-Φ, 50 Hz supply
Voltage (Line-Line)	400 V
Motor Current	7.5 A
Rotor speed	1445 RPM
Power	5 HP
No. of poles	4

Inverter-1 and inverter-2 (Fig. 2.1) are operated with the respective dc-link voltages of 200 V and 100 V, to obtain an effective dc-link voltage of 300 V for the dual-inverter system ($|\boldsymbol{OU}|$, Fig. 2.3).

The voltage to frequency ratio is maintained in such a way that the rated frequency of 50 Hz is applied at the edge of linear modulation. Above this limit, the dual inverter system operates in the region of overmodulation, wherein the relationship between the modulation index and the output voltage of the dual-inverter system is nonlinear.

The simulated waveforms are presented for the cases of linear modulation, at modulation index (eq. 2.15) of 0.2 and 0.7. The frequency of the fundamental component corresponding to m_a = 0.2 and 0.7 is 11.55 Hz and 40.4 Hz (eq. 2.16) respectively. Fig. 2.7 – Fig. 2.10 shows the simulated phase-A voltage, current and FFT analysis for the DDPWM-1, 2, 3 & 4 techniques at m_a = 0.2.

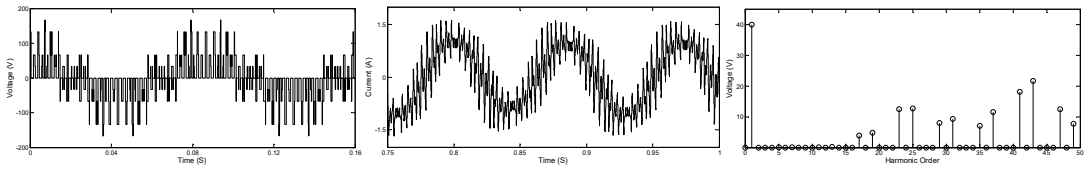


Fig. 2.7: Simulated Phase-A voltage (left), current (middle) and harmonic spectrum (right) of DDPWM-1 at m_a = 0.2

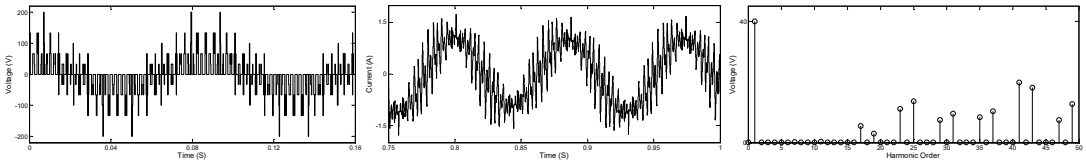


Fig. 2.8: Simulated Phase-A voltage (left), current (middle) and harmonic spectrum (right) of DDPWM-2 at m_a = 0.2

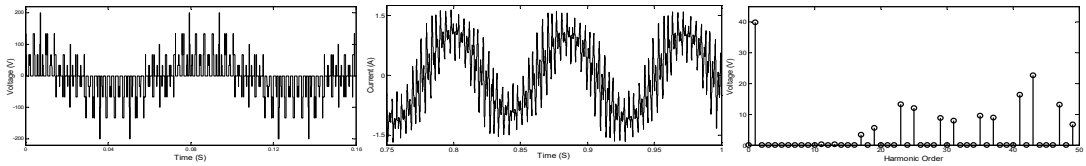


Fig. 2.9: Simulated Phase-A voltage (left), current (middle) and harmonic spectrum (right) of DDPWM-3 at m_a = 0.2

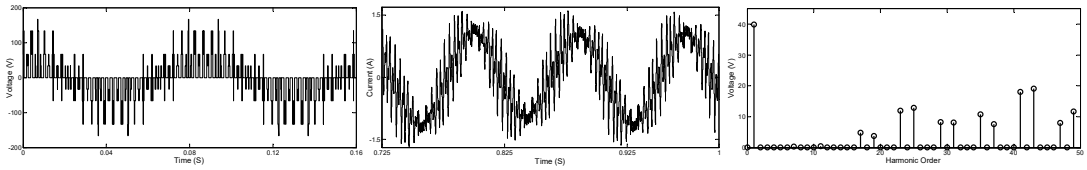
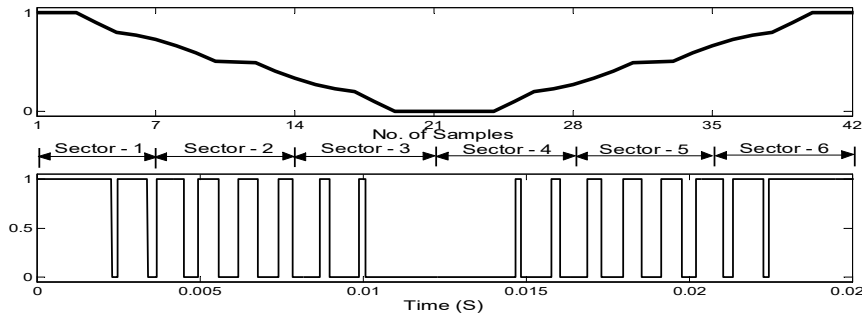
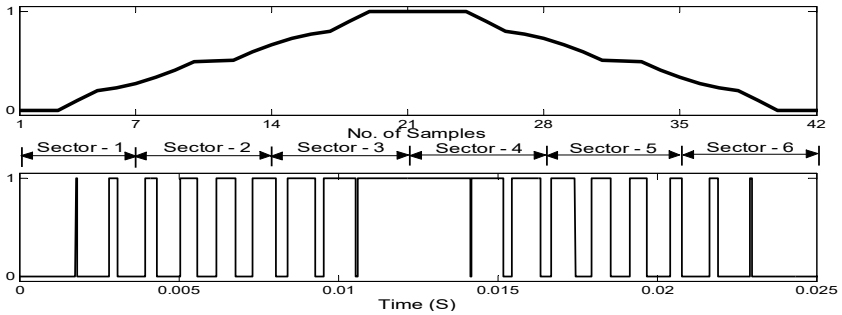


Fig. 2.10: Simulated Phase-A voltage (left), current (middle) and harmonic spectrum (right) of DDPWM-4 at m_a = 0.2

The simulated waveforms of the dual-inverter control signals at a modulation index of 0.7 are shown in Figs. 2.11 and 2.12 for DDPWMs-1 & 2. The simulated phase-A voltage, current and phase-A voltage harmonic spectrum for the DDPWM-1, 2, 3 & 4 techniques at the modulation index of 0.7 are shown in Figs. 2.13-2.16.

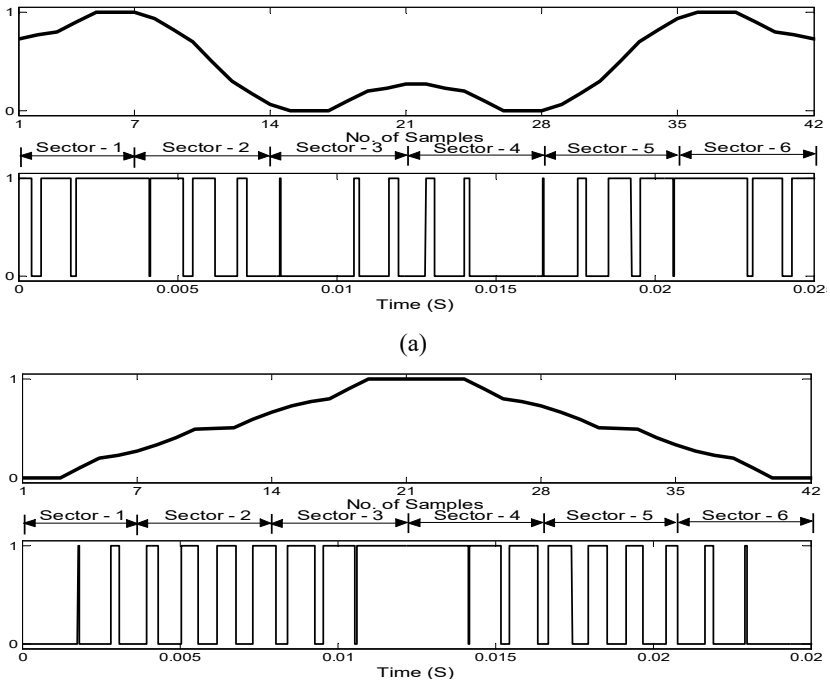


(a)



(b)

Fig. 2.11: Simulated control signals with modulating waveforms for DDPWM-1 at $m_a = 0.7$. (a) inverter-1 (b) inverter-2



(a)

(b)

Fig. 2.12: Simulated control signals with modulating waveforms for DDPWM-2 at $m_a = 0.7$. (a) inverter-1 (b) inverter-2

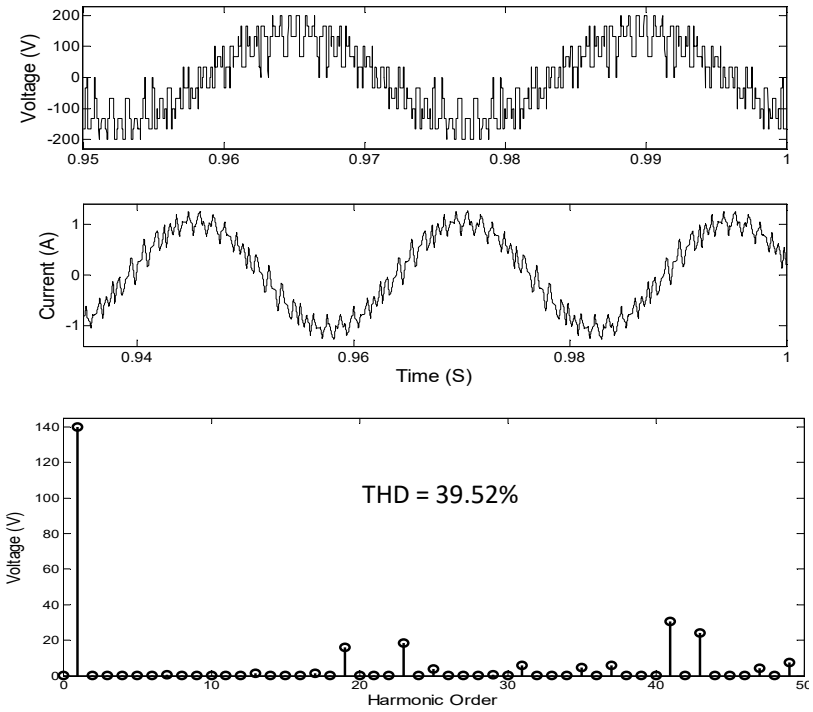


Fig. 2.13: Simulated Phase-A voltage (top), current (middle) waveforms and harmonic spectrum of phase-A voltage (bottom) of DDPWM-1 at $m_a = 0.7$

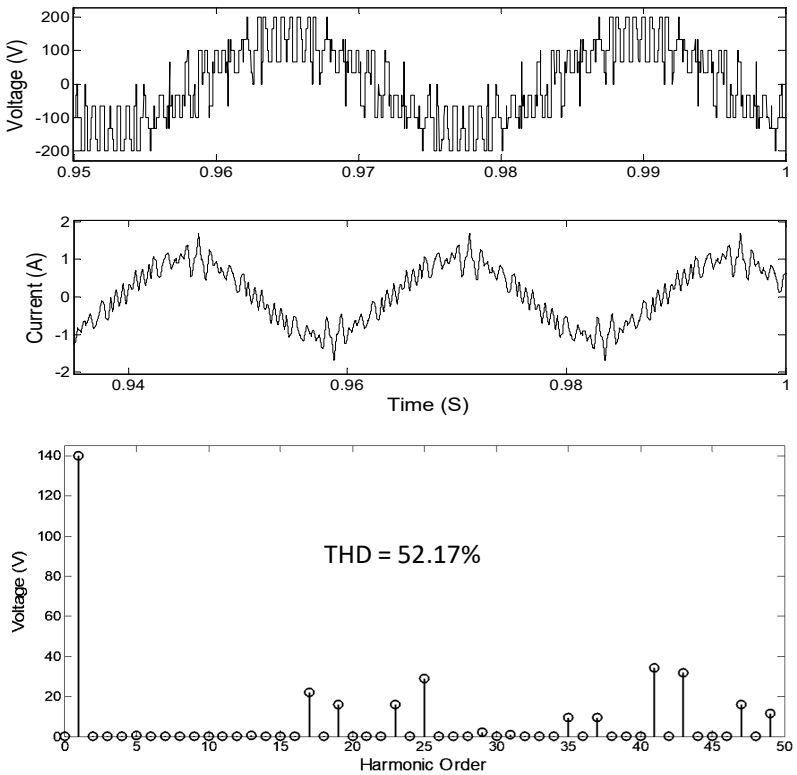


Fig. 2.14: Simulated Phase-A voltage (top), current (middle) waveforms and harmonic spectrum of phase-A voltage (bottom) of DDPWM-2 at $m_a = 0.7$

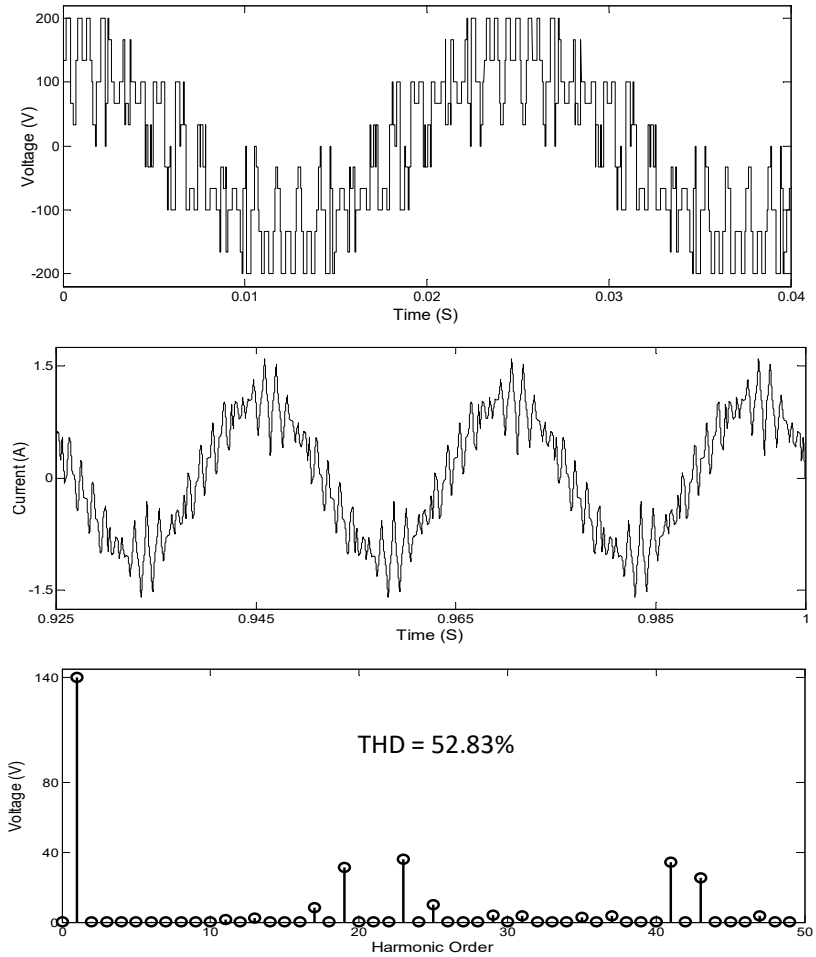
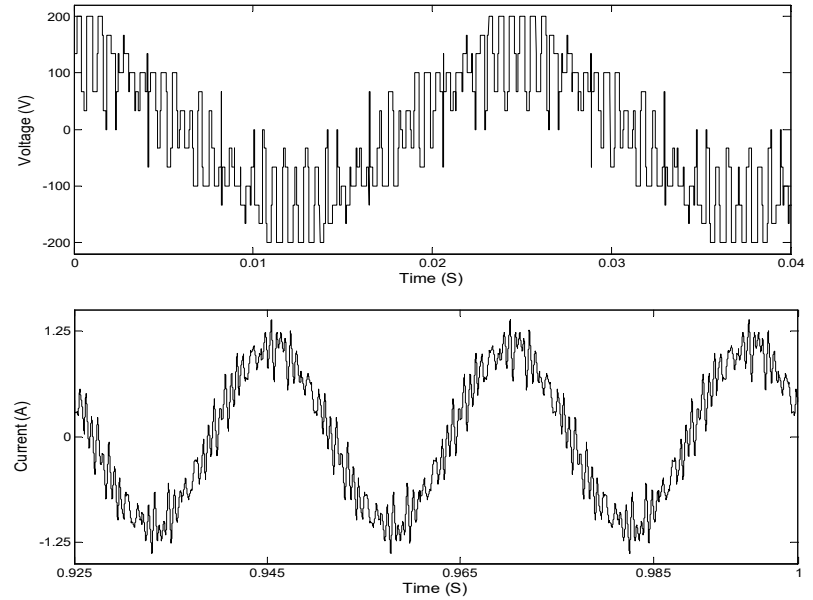


Fig. 2.15: Simulated Phase-A voltage (top), current (middle) waveforms and harmonic spectrum of phase-A voltage (bottom) of DDPWM-3 at $m_a = 0.7$



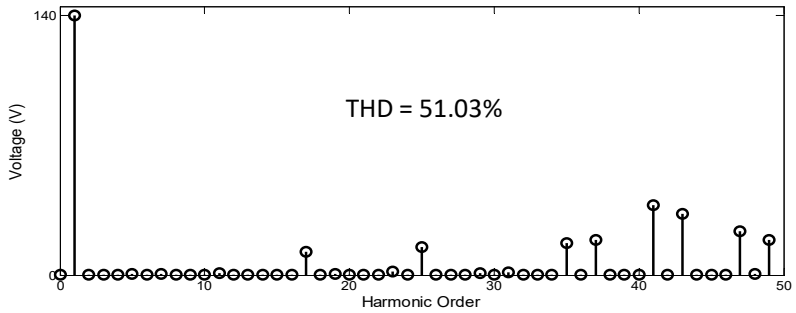


Fig. 2.16: Simulated Phase-A voltage (top), current (middle) waveforms and harmonic spectrum of phase-A voltage (bottom) of DDPWM-4 at $m_a = 0.7$

Comparing the voltage spectra (bottom trace) presented in Figs. 2.13 – 2.16, it is clear that DDPWM-1 results in a better spectral performance compared to DDPWM-2, 3 & 4 for the four-level dual-inverter system (as predicted in the previous section). This fact is also evident from the waveforms of motor phase-A voltage (top trace) and current (middle trace) (Figs. 2.13 - 2.16).

The experimental waveforms are presented for the cases of (i) linear modulation, at modulation index of 0.2, 0.7 and (ii) for the case of over modulation. The experimental common mode voltage, which is dropped across the points o and o' (Fig. 2.1), phase-A voltage and current waveforms are shown in Figs. 2.17 - 2.20, at $m_a = 0.2$, for all of the four DDPWM techniques.

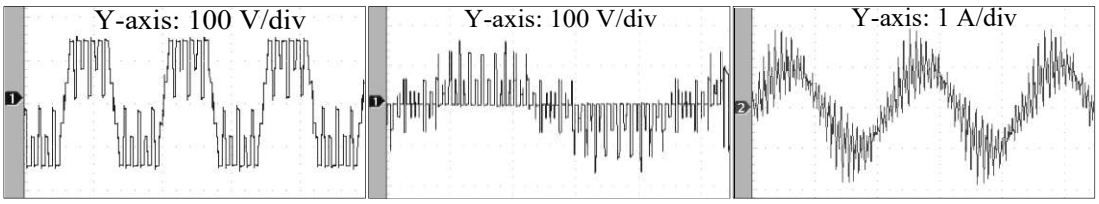


Fig. 2.17: Experimental waveforms of common mode voltage (left), Phase-A voltage (middle) and current (right) at $m_a = 0.2$ for DDPWM-1 technique (X-axis: 10 ms/div)

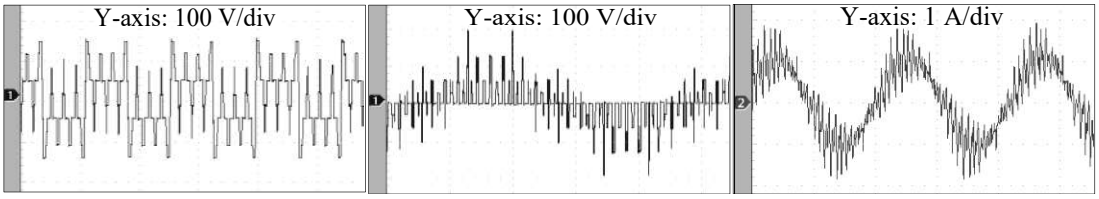


Fig. 2.18: Experimental waveforms of common mode voltage (left), Phase-A voltage (middle) and current (right) at $m_a = 0.2$ for DDPWM-2 technique (X-axis: 10 ms/div)

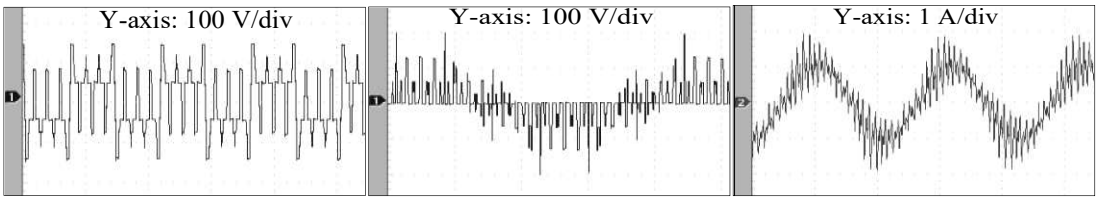


Fig. 2.19: Experimental waveforms of common mode voltage (left), Phase-A voltage (middle) and current (right) at m_a = 0.2 for DDPWM-3 technique (X-axis: 10 ms/div)

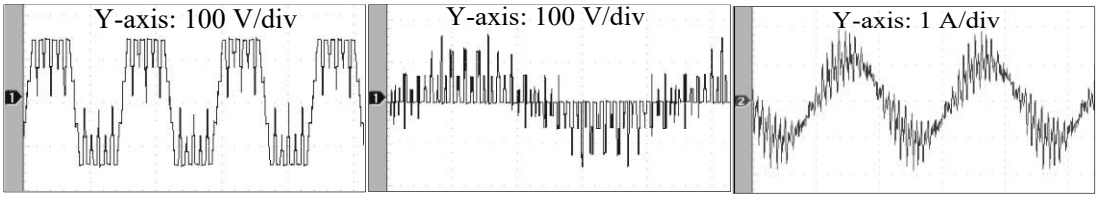
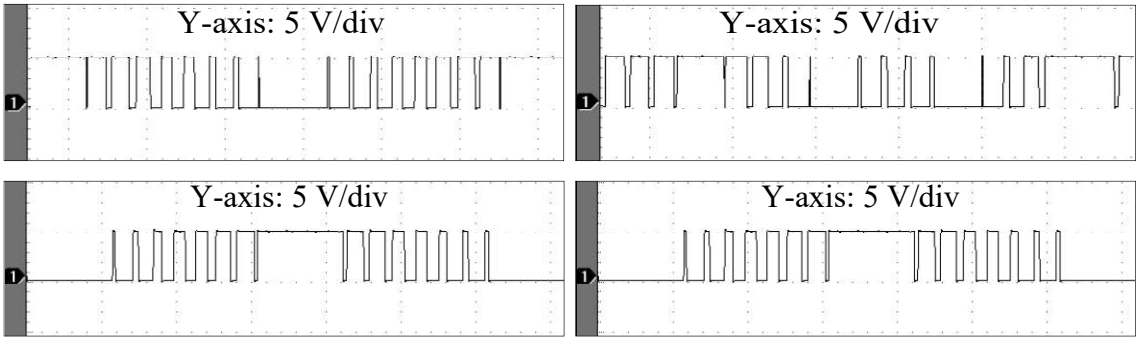


Fig. 2.20: Experimental waveforms of common mode voltage (left), Phase-A voltage (middle) and current (right) at m_a = 0.2 for DDPWM-4 technique (X-axis: 10 ms/div)

The control signals generated from the dSPACE-1104 for the DDPWM-1&2 techniques in one cycle are shown in Fig. 2.21 at at m_a = 0.7. The experimental common mode voltage, phase-A voltage and current waveforms for the DDPWM-1 technique at m_a = 0.7 and 1 are shown in Figs. 2.22 – 2.25. Fig. 2.22 shows the experimental pole voltage waveforms of inverter-1 (left) and inverter-2 (right) respectively. Fig. 2.23 shows the experimentally obtained zero-sequence voltage. The experimentally obtained phase-A voltage and current waveforms are shown in Fig. 2.24. The experimental voltage and current waveforms of phase-A in the case of over modulation (i.e.$m_a \geq 1$) are shown in Fig. 2.25.



(a) (b)

Fig. 2.21: Experimental control signals for Phase-A of dual inverters (inverter-1 (top), inverter-2 (bottom)) at m_a = 0.7 (X-axis: 4 ms/div). (a) DDPWM-1 (b) DDPWM-2

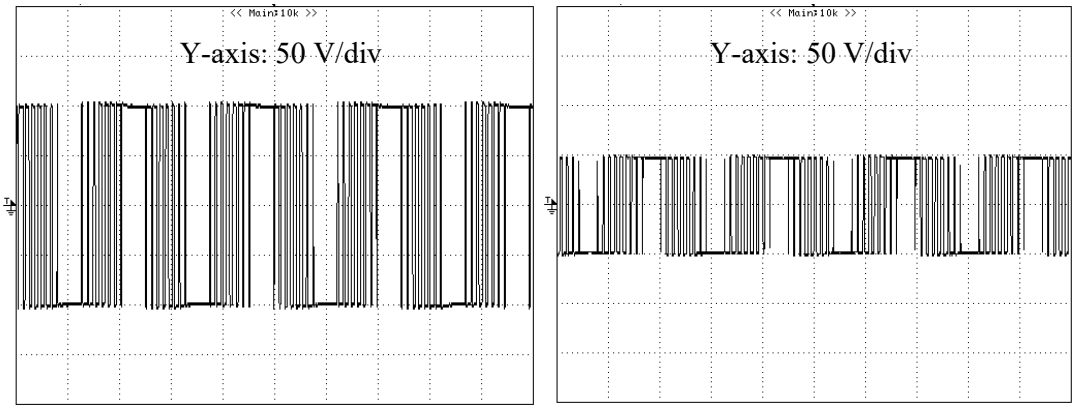


Fig. 2.22: Experimental Pole voltages of inverter-1(left), inverter-2 (right) at $m_a = 0.7$ for DDPWM-1 (X-axis: 10 ms/div)

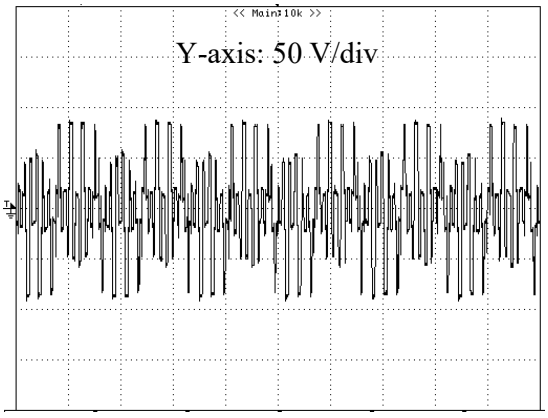


Fig. 2.23: Experimental common mode voltage waveform for DDPWM-1 at $m_a = 0.7$ (X-axis: 5 ms/div)

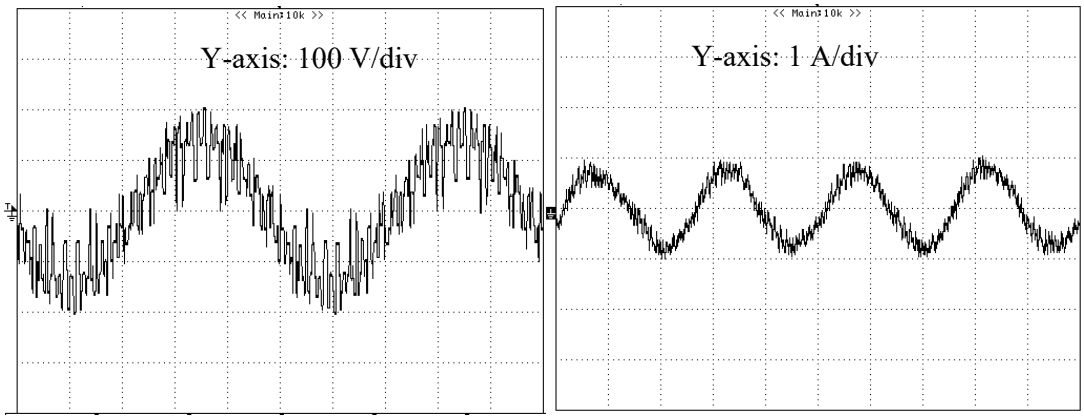


Fig. 2.24: Experimental Phase-A voltage (left) and current (right) waveforms for DDPWM-1 at $m_a = 0.7$. (X-axis: 5 ms/div(left), 10 ms/div (right))

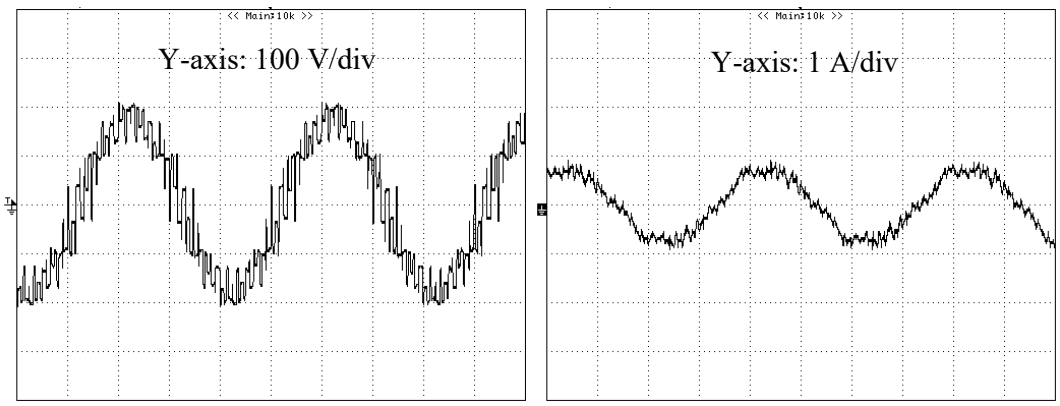


Fig. 2.25: Experimental Phase-A voltage (left) and current (right) waveforms for DDPWM-1 at $m_a = 1$ (X-axis: 5 ms/div)

The experimental results for the case of DDPWM-2 technique are shown in Figs. 2.26 – 2.29 for $m_a = 0.7$ and for over modulation. The experimental pole voltage waveforms for both of the inverters are shown in Fig. 2.26. Comparison of the pole voltages obtained for DDPWM-1 (Fig. 2.22) and DDPWM-2 (Fig. 2.26)) reveals that the pole voltages of inverter-2 appear identical, while the pole voltages are different for inverter-1. This result is anticipated as the modulating functions of inverter-2 are identical for both of the DDPWM schemes, while they are different for inverter-1 (Fig. 2.5). Fig. 2.27 shows the experimental waveform of common mode voltage for DDPWM-2. The practically obtained phase-A current and voltage waveforms are shown in Fig. 2.28. In the case of over modulation, the experimentally obtained phase-A voltage and current waveform are shown in Fig. 2.29.

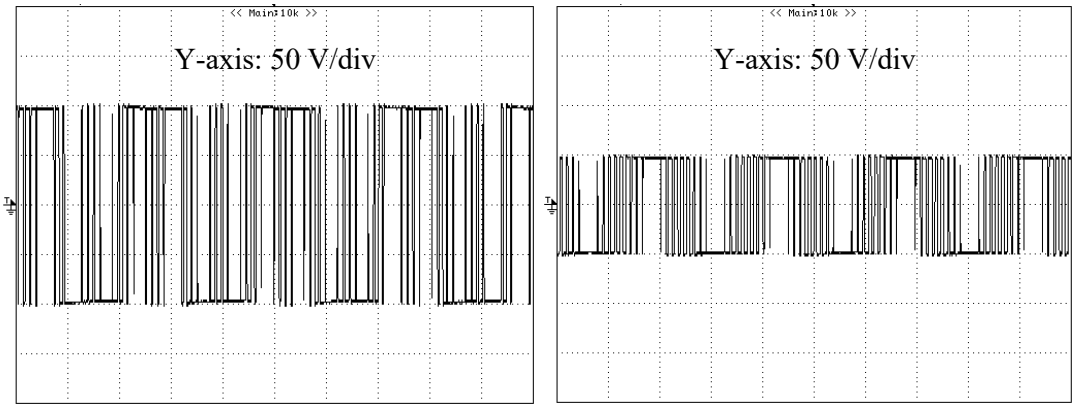


Fig. 2.26: Experimental Pole voltages of inverter-1(left), inverter-2 (right) at $m_a = 0.7$ for DDPWM-2 (X-axis: 10 ms/div)

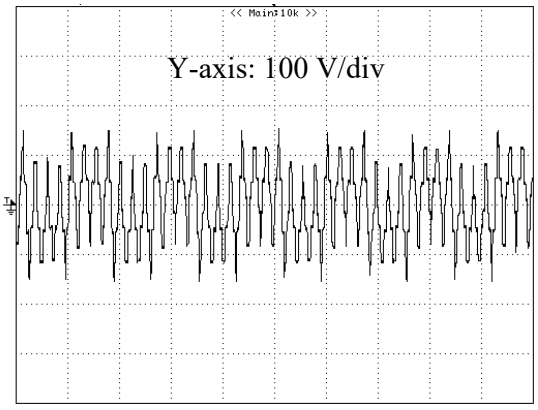


Fig. 2.27: Experimental common mode voltage waveform for DDPWM-2 at $m_a = 0.7$ (X-axis: 10 ms/div)

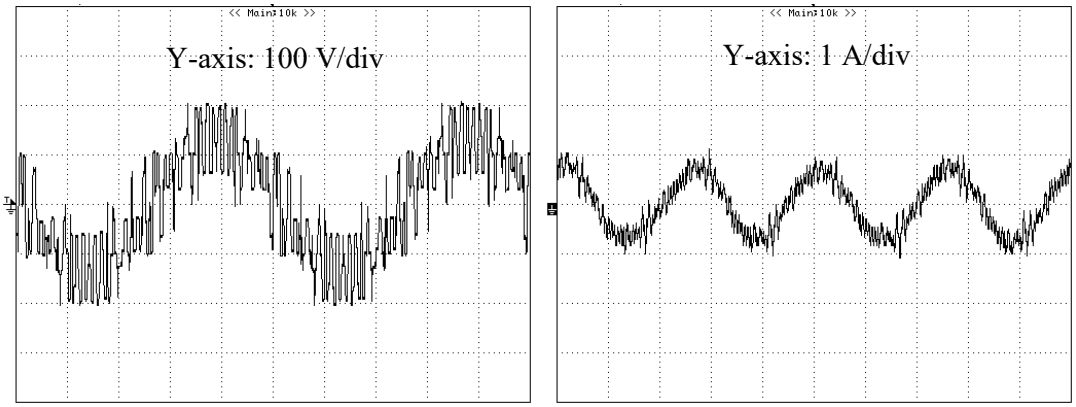


Fig. 2.28: Experimental Phase-A voltage (left) and current (right) waveforms for DDPWM-2 at $m_a = 0.7$ (X-axis: 5 ms/div (left), 10 ms/div (right))

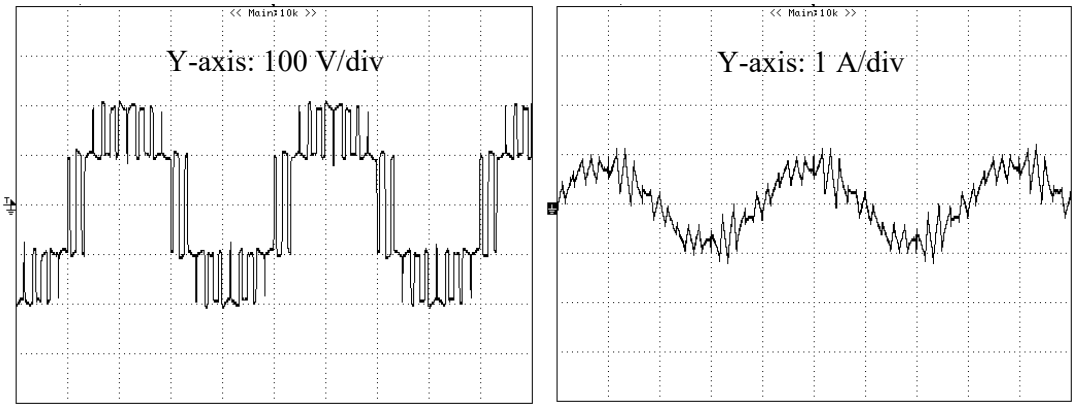


Fig. 2.29: Experimental Phase-A voltage (left) and current (right) waveforms for DDPWM-2 at $m_a = 1$ (X-axis: 5 ms/div)

Similar experimental waveforms are presented in the case of DDPWM-3 and DDPWM-4 in Figs. 2.30 – 2.35 respectively. In the case of the DDPWMs-3 & 4, the

experimental pole voltages are not presented. In DDPWM-3, the switching sequences of the respective inverters are the reversed versions of those for DDPWM-2 in any given sector. For example, the switching sequence corresponding to the first sample in DDPWM-3 (1-2-7) is obtained by reversing the switching sequence corresponding to the 7th sample (7-2-1) of DDPWM-2. In DDPWM-4, the switching sequences applied to inverter-1 and inverter-2 are identical to the switching sequence of the inverter-1 of the DDPWM-2 and inverter-2 of the DDPWM-3 respectively (see Table 2.3).

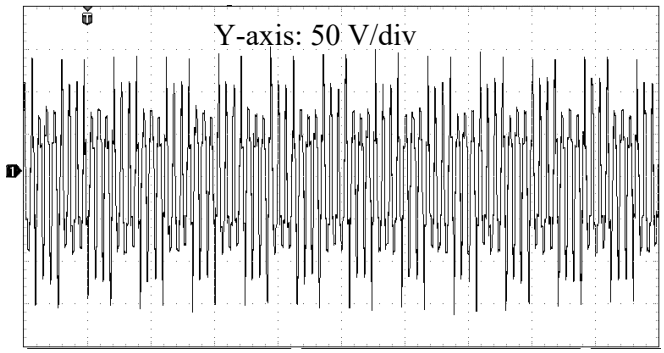


Fig. 2.30: Experimental common mode voltage waveform for DDPWM-3 at $m_a = 0.7$ (X-axis: 10 ms/div)

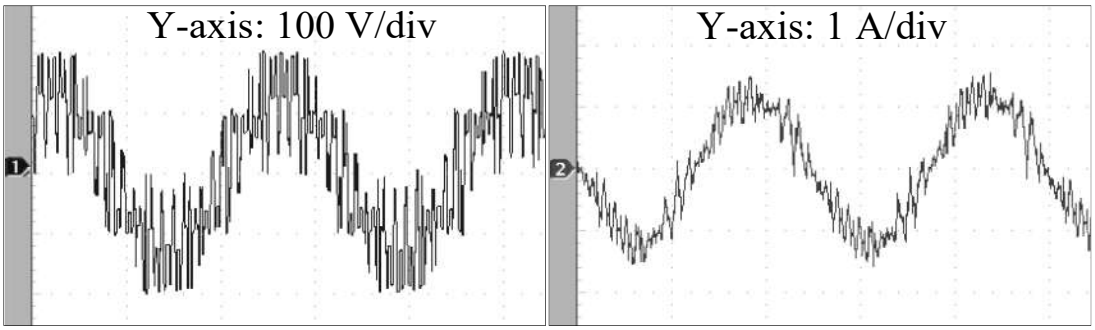


Fig. 2.31: Experimental Phase-A voltage (left) and current (right) waveforms for DDPWM-3 at $m_a = 0.7$ (X-axis: 10 ms/div)

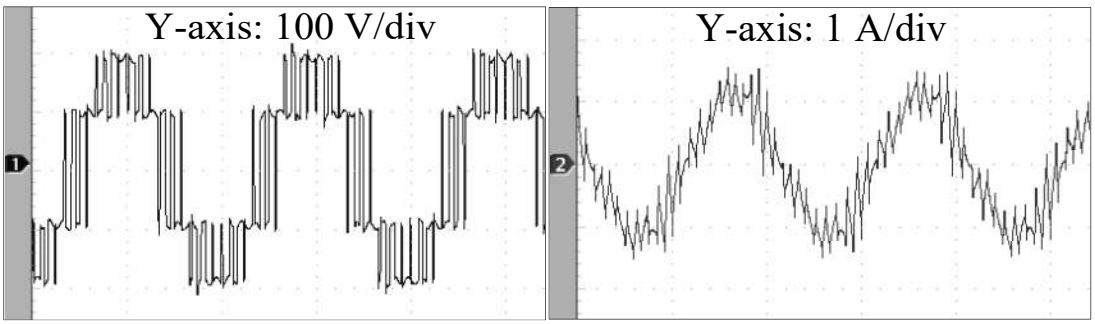


Fig. 2.32: Experimental Phase-A voltage (left) and current (right) waveforms for DDPWM-3 at $m_a = 1$ (X-axis: 10 ms/div)

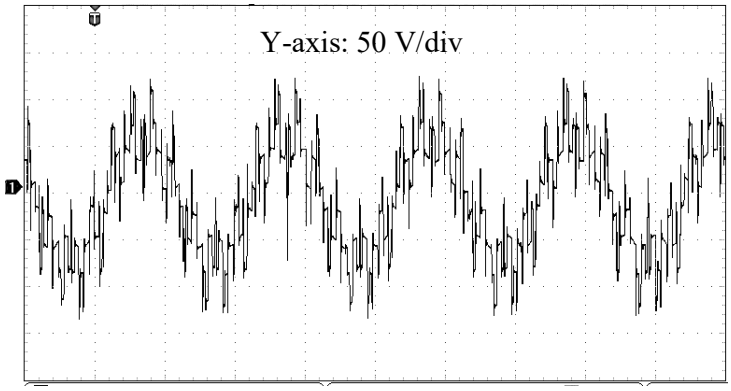


Fig. 2.33: Experimental common mode voltage waveform for DDPWM-4 at $m_a = 0.7$ (X-axis: 4 ms/div)

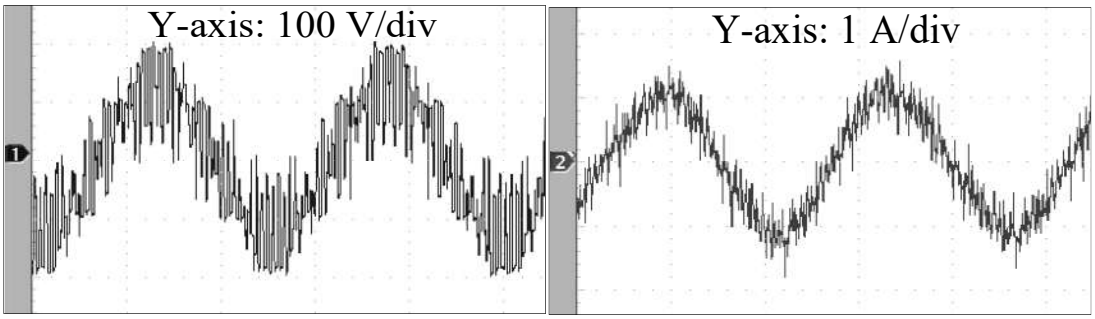


Fig. 2.34: Experimental Phase-A voltage (left) and current (right) waveforms for DDPWM-4 at $m_a = 0.7$ (X-axis: 10 ms/div)

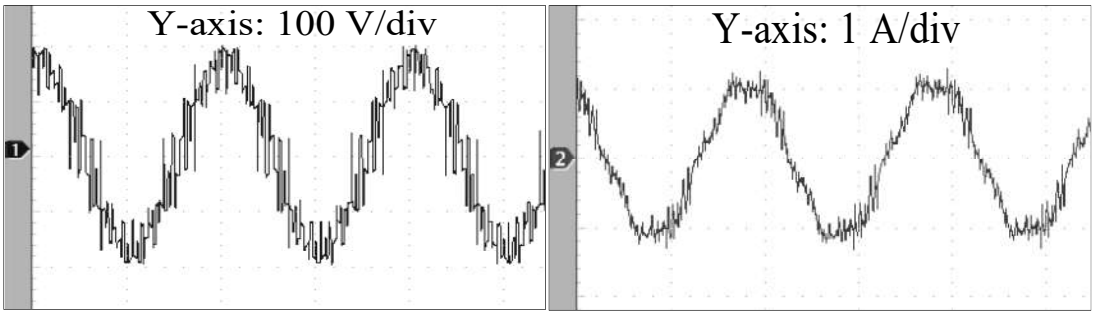


Fig. 2.35: Experimental Phase-A voltage (left) and current (right) waveforms for DDPWM-4 at $m_a = 1$ (X-axis: 10 ms/div)

2.5 Comparative Analysis of DDPWM & CSPWM Strategies

This section critically compares the proposed DDPWM techniques with the Decoupled *Center-Spaced* PWM schemes proposed in [65]. The decoupled SVPWM techniques proposed in [65] are named as *Equal-Duty PWM* (EDPWM) and *Proportional-Duty* PWM (PDPWM). To ensure fairness in comparison, both inverters are switched with 42

samples/cycle, for all the four of the PWM schemes. However, the comparable situation in the case of PDPWM technique is to switch inverter-1 and inverter-2 (Fig. 2.1) with 30 and 54 samples/cycle respectively [65]. The total dc-link voltage (564 V) is selected in such a way that the rated motor phase voltage (230 V) is applied to the motor at the limit of linear modulation (i.e. $m_a=\sqrt{3}/2$).

The loss analysis for the dual-inverter system is carried out on the basis of the losses incurred per one phase-leg (say phase-A of inverter-1), shown in Fig. 2.36. The IGBTs of the phase-A leg are represented as T_A^+, T_A^- and their anti-parallel diodes are denoted by D_A^+, D_A^-.

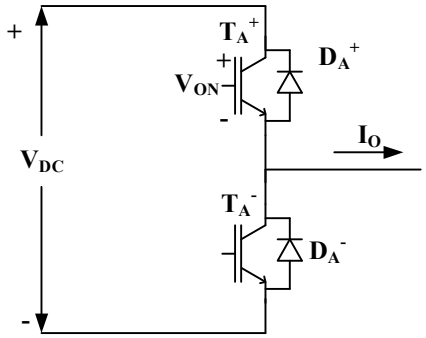


Fig. 2.36: One of the A-Phase leg of dual-inverter topology

The top trace of Fig. 2.37 (a) shows the typical gating waveform for the IGBT T_A^+. The second trace of Fig. 2.37 (b) shows the current flowing through the switching device T_A^+ and the anti-parallel diode D_A^-, while considering the diode reverse recovery current into account. The fig. 2.37 (c) shows the voltage across the switch T_A^+ and the anti-parallel diode D_A^- [3]. The last trace shows the total power loss incurred in the device, which includes the switching, and conduction power losses in T_A^+ and the conduction loss in the diode D_A^-.

The switching power loss (P_{SW}) and conduction power loss (P_{CON}) are given by [3]:

$$P_{SW} = \left[\frac{1}{2} v_{SW} i_{SW} (t_{ri} + t_{fv}) + \frac{1}{2} v_{SW} i_{SW} (t_{rv} + t_{fi})\right] \times f_s \tag{2.28}$$

$$P_{CON} = \frac{V_{ON} I_{ON} t_{ON}}{T_S} \tag{2.29}$$

where, v_{SW} = voltage blocked by the switch in its OFF-state (i.e. V_{DC}), $i_{SW} = I_{ON} =$ current flowing through the switch in its on-state, f_s = switching frequency, $T_s = 1/f_s =$ switching time period, v_{ON}= on-state voltage drop, t_{ri}, t_{rv} = rise times of current and voltage, $t_{fv}, t_{fi} =$ fall times of voltage and current, and $t_{ON} =$ switch turn-on time.

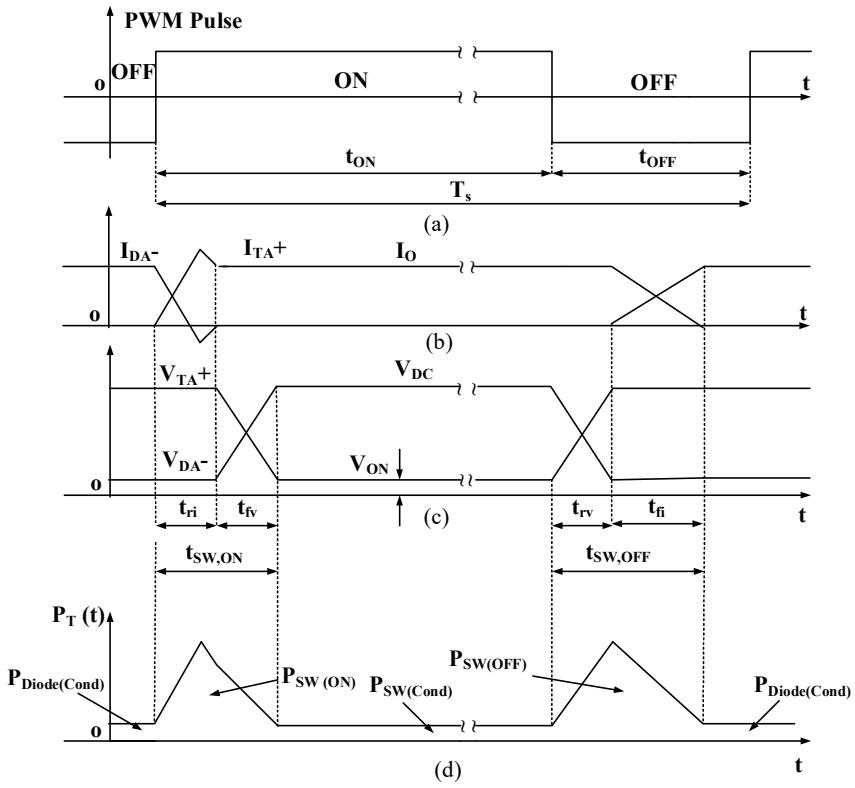


Fig. 2.37: Current through and Voltage across T_A^+, D_A^- with diode reverse recovery current

$$v_{ON} = V_t + i_{ON} R_{CE} \text{ for IGBT}$$

$$v_{ON} = V_f + i_{ON} R_{AK} \text{ for the anti-parallel diode}$$

where V_t is the IGBT fixed voltage drop under zero-current condition, R_{CE} is the IGBT on-drop resistance, V_f is the diode fixed voltage drop under zero-current condition and R_{AK} is the diode on-drop resistance. The parameters of the IGBT module-*SKM150GB12T4* are considered for the evaluation of the conduction loss.

Computation of the switching and conduction losses of the switching devices is facilitated by the loss-computation model, suggested in [99]. However, the loss model suggested in [99], neglects the diode conduction loss and the additional power loss incurred due to the reverse recovery current of the diode. Fig. 2.38 shows an improvised loss-model, which accounts for these losses.

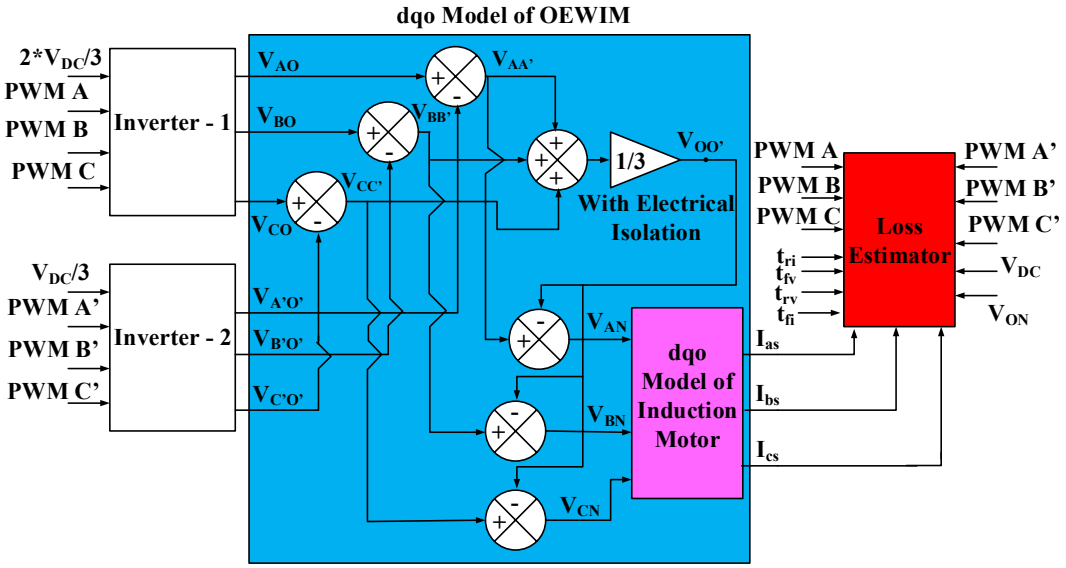


Fig. 2.38: Improvised loss model for four-level OEWIMD

The switching and conduction losses in each switching device are computed by assuming the following data: $t_{fv} = 1\ \mu S, t_{rv} = 2\ \mu S, t_{fi} = 4\ \mu S$ and $t_{ri} = 2\ \mu S$. To ensure fair comparison, this data is kept identical for all the six PWM schemes (i.e. the four proposed DDPWM techniques and the two Center Spaced Decoupled SVPWM schemes described in [65]). Keeping in view of the fact that the losses in the power semi-conductor switching devices as well as the conduction loss are both load dependent, a load torque of 20 N-m is applied to the OEWIM chosen for analysis (5 HP, i.e. 3.7 KW, 1445 RPM, 50 Hz). The parameters of the OEWIMD are given in Table 2.4.

Fig. 2.39 shows the simulation results in per-unit representation, which are obtained by using the improvised loss model (Fig. 2.38). The top trace shows the typical turn-on current through a top-device (such as T_A^+ of inverter-1, Fig. 2.36), which includes the diode

reverse recovery current. The middle trace shows the voltage across it and the bottom trace shows the voltage across the bottom-diode (such as D_A^-, Fig. 2.36).

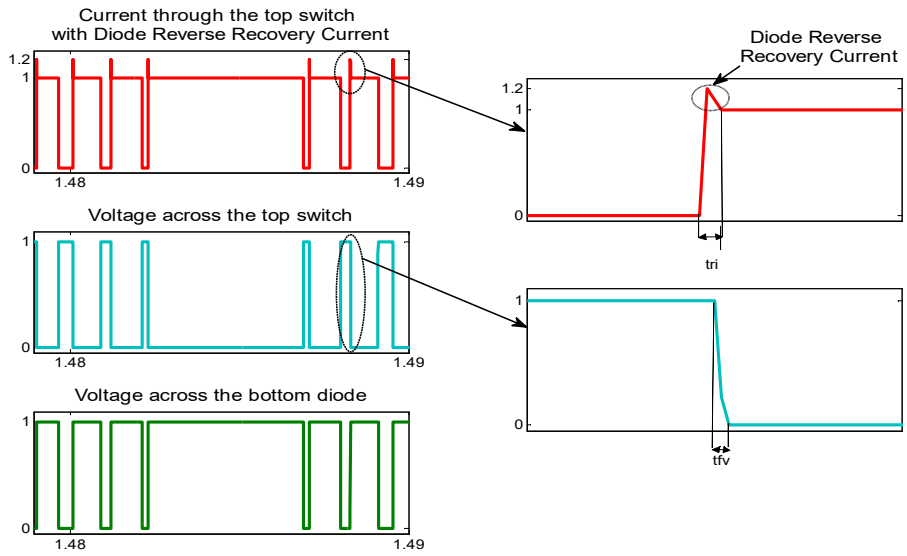


Fig. 2.39: Simulated current and voltage waveforms of the top switching device with diode reverse recovery current and the bottom diode

Fig. 2.40 shows the simulation results corresponding to (i) the switching power loss in a top-device, such as T_A^+ (top trace), (ii) the conduction power loss in it (middle trace) and (iii) the conduction power loss in the bottom-diode, such as D_A^- (bottom trace) and presents a zoomed version between the time periods 1.43 sec to 1.45 sec. From the zoomed version of Fig. 2.40, it can be observed that the switching power losses (top trace) show up as peaks, which are of the order of kilo-watts occurring for extremely small time duration corresponding to the order of switching time periods ($t_{fv} = 1\ \mu S, t_{rv} = 2\ \mu S, t_{fi} = 4\ \mu S, t_{ri} = 2\ \mu S$). It may also be observed that these peaks occur at the extreme edges of the conduction regime (middle trace) of the top switching device. It is also apparent that the ripple in the motor phase current considerably affects both the conduction losses of the semi-conductor devices as well as the ohmic loss in the motor.

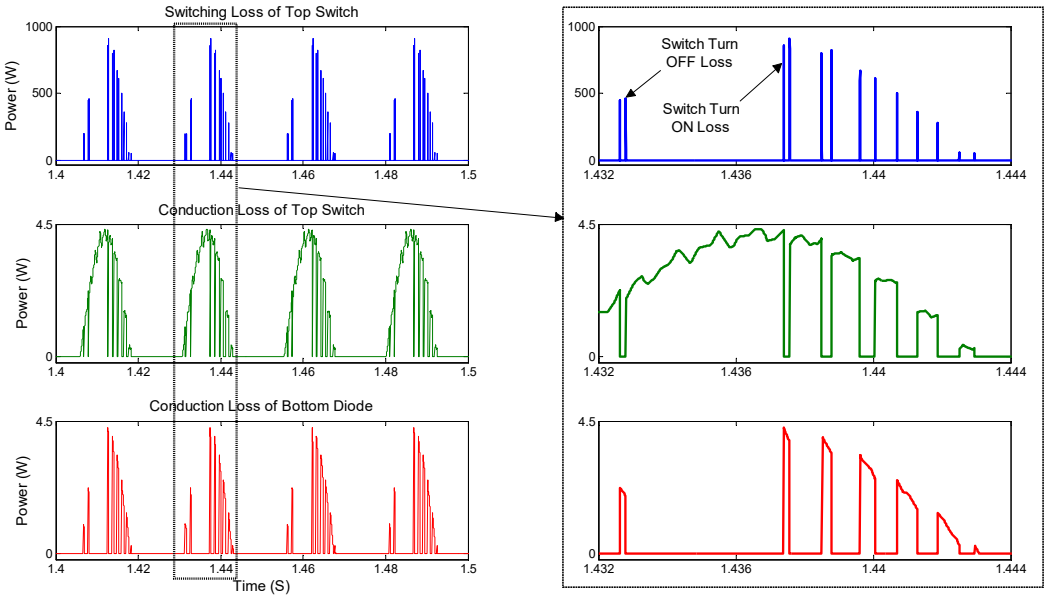
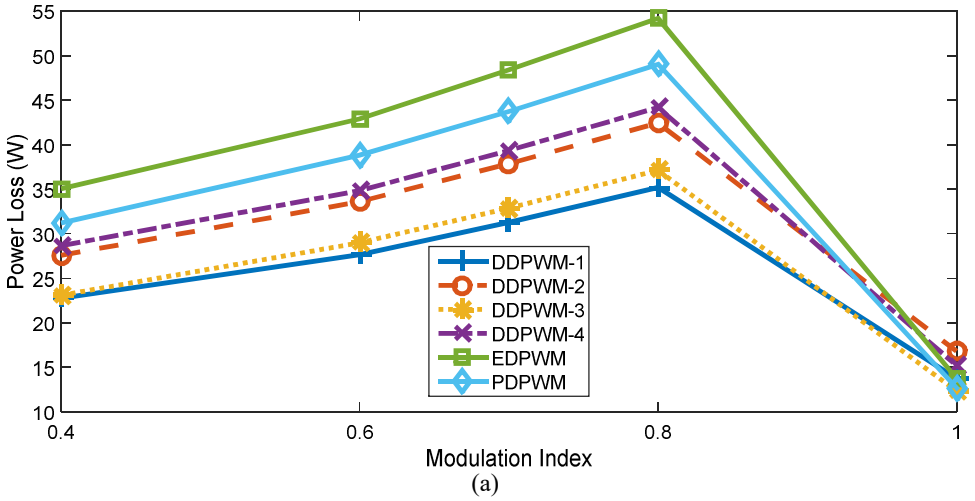
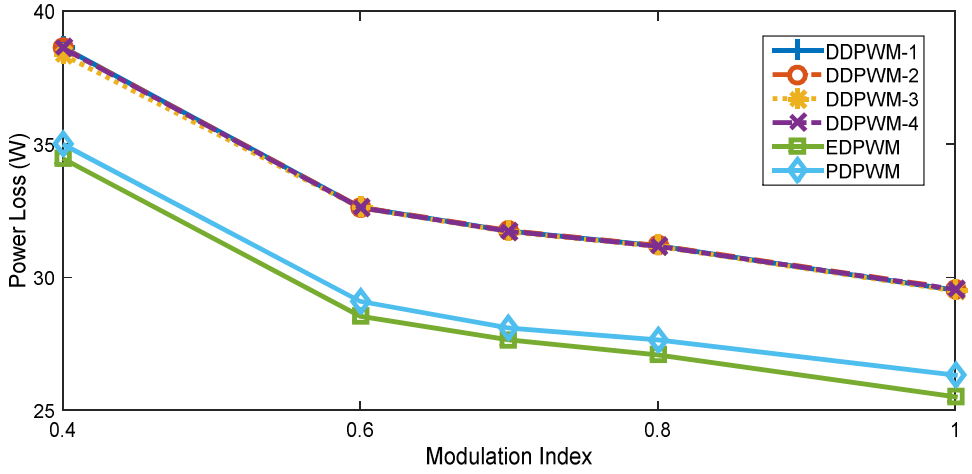


Fig. 2.40: Simulated loss waveforms of top switching device and bottom anti-parallel diode with zoomed portion

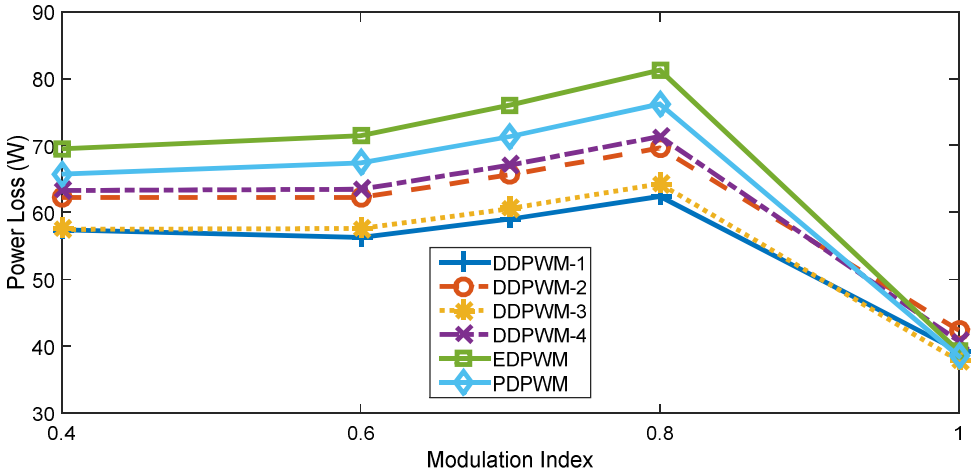
The switching and conduction power loss of the four-level OEWIMD are shown in Fig. 2.41 (a, b) respectively. The overall loss (i.e. the sum of the switching and the conduction loss) of the dual-inverter system is shown in Fig. 2.41 (c).



(a)



(b)



(c)

Fig. 2.41: Loss of dual-inverter fed four-level OEWIM (a) total switching power loss, (b) total conduction power loss, (c) Overall dual-inverter loss

The simulation results reveal that the proposed DDPWM techniques result in lesser overall loss compared to the decoupled SVPWM schemes. As reasoned out in the foregoing section, DDPWM-1 performs better amongst the four DDPWM techniques. The overall power loss increases linearly with the modulation index up to the limit of linear modulation (0.866), as the fundamental frequency depends on the modulation index (eq. 2.15). Thus, the sampling time period decreases (or in other words, the switching frequency is increased) with the increase of the modulation index as the number of samples per cycle are fixed at 42/cycle. In the case of overmodulation (i.e. $m_a \geq 0.866$), the fundamental frequency is clamped to 50 Hz, which results in the decrease of switching loss. Consequently, the total power loss also decreases.

The Total Harmonic Distortion (THD) is one of the most extensively used indices of performance, which quantifies the harmonic contamination in the output of inverter circuits. It is defined as:

$$V_{THD} = \frac{\sqrt{\sum_{n=2}^{\infty} V_n^2}}{V_1} \tag{2.30}$$

In eq. (2.30), V_1 and V_n respectively represent the fundamental component and n^{th} harmonic components of the RMS phase voltage. THD is a measure of the harmonic pollution in voltage, which is expressed in per unit or percentage, taking the fundamental quantity as the base value. The THD is evaluated for the motor phase voltage with all of the four SVPWM techniques, as a function of modulation. It is again seen that the PWM schemes proposed in this chapter perform considerably better than the Decoupled SVPWM techniques, as shown in Fig. 2.42. Again, as one might expect, the DDPWM-1 scheme gives a better harmonic performance amongst the four DDPWM schemes.

However, in motor drive applications, it is more apt to quantify the harmonic distortion in the motor phase current rather than the motor phase voltage, as the primary interest is to draw currents which are as close to a sinusoid as possible. The THD in current (iTHD) is such a measure, which is expressed as:

$$i_{THD} = \frac{\sqrt{\sum_{n=2}^{\infty} I_n^2}}{I_1} \tag{2.31}$$

When a sinusoidal voltage source feeds an induction motor, the motor draws only magnetizing current at no-load. Neglecting the leakage inductance, which is often small compared to the magnetizing inductance L_m, the no-load current is approximately equal to $(V_1/\omega L_m)$. However, when a non-sinusoidal source (such as a VSI) supplies the motor, any harmonic current component of n^{th} order is given by $(V_n/n\omega L_m)$. Thus, the RMS value of all harmonic components put together is given by $\sum_{n\neq 1}(V_n/n\omega L_m)^2$. Thus, the Weighted Total Harmonic Distortion (WTHD) is given by,

$$V_{WTHD} \triangleq \frac{\sqrt{\sum_{n=2}^{\infty}\left(\frac{V_n}{n}\right)^2}}{V_1} \tag{2.32}$$

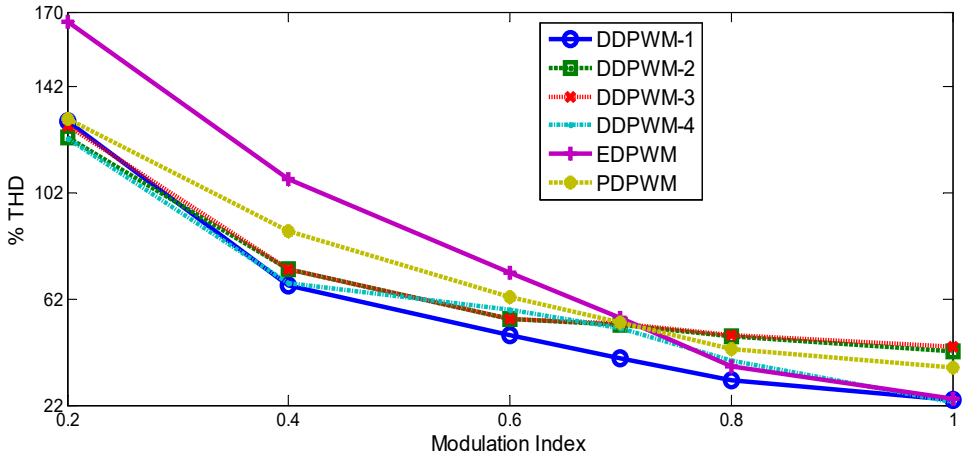


Fig. 2.42: THD for four-level OEWIMD

Fig. 2.43 shows that the WTHD with all of the six PWM schemes. From Fig. 2.43, as per the expectation, the DDPWM-1 scheme performs better than the other SVPWM schemes.

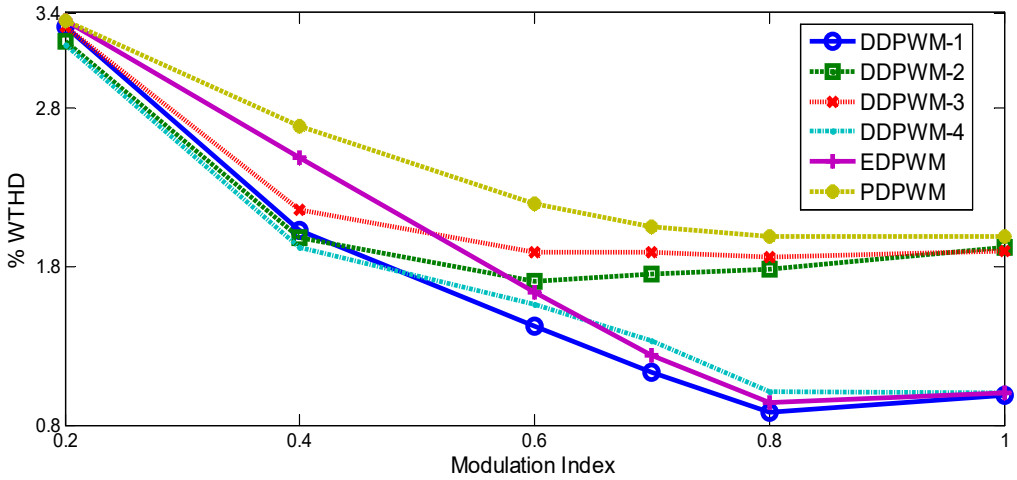


Fig. 2.43: WTHD for four-level OEWIMD

Reviewing all aspects and the graphical data presented in Figs. 2.41 (a, b and c), 2.42 and 2.43, it is apparent that the DDPWM techniques perform better than the Decoupled SVPWM techniques.

It is fairly well known that, application of PWM voltages with a large value of dv/dt is deleterious to the motor [19]. In this aspect, the DDPWM-1 scheme performs better compared to the Decoupled SVPWM schemes. The magnified versions of the simulated motor phase voltage waveforms with the proposed DDPWMs and the Decoupled SVPWM schemes are shown in Fig. 2.44. It may be noted that the voltage pulses appearing across the motor phase windings with the DDPWM-1 scheme show lower levels of transition compared to the Centre Spaced Decoupled SVPWM schemes [65]. This indicates that the motor phase windings are subject lower dv/dt with the proposed DDPWM schemes (Fig. 2.44).

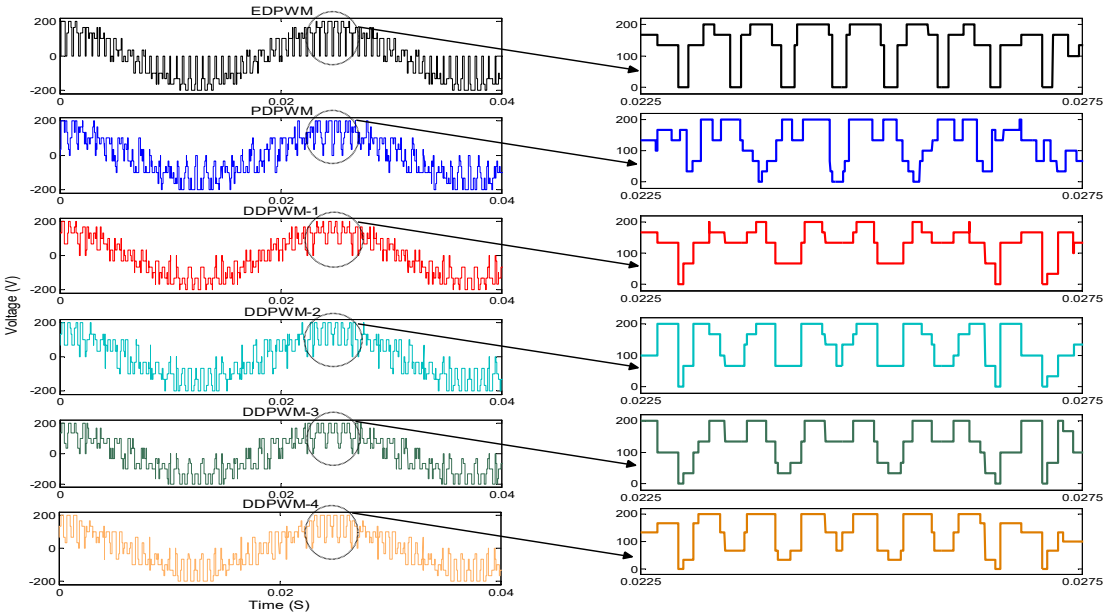


Fig. 2.44: The voltage pulses appearing across the motor winding with the EDPWM (top), PDPWM (second), DDPWM-1 (third) DDPMW-2 (fourth), DDPWM-3 (fifth) and the DDPWM-4 (bottom) techniques

2.6 Conclusion

In this chapter, the application of Discontinuous Decoupled PWM (DDPWM) schemes for a four-level OEWIMD is investigated. Though the application of DDPWM (also called Phase Clamped PWM) is very well known for the conventional two-level inverters, its application for a four-level OEWIMD is not reported in the literature (in the case of Decoupled SVPWM with equal duty). Application of DDPWM schemes poses problems owing to the fact that the power circuit configuration is not symmetrical. It is difficult to

derive waveform symmetries from an unsymmetrical power circuit using an unsymmetrical (i.e. non-center spaced) Decoupled PWM scheme.

Simulation studies reveal that, of the several possibilities of placing the effective time period at the edge of sampling time interval, only four succeed in resulting all the three symmetries namely, the quarter-wave, the half-wave and the three-phase symmetries. These four possibilities are named as DDPWM-1, DDPWM-2, DDPEM-3 and DDPWM-4. Simulations as well as experimental studies show that DDPWM-1 performs better than DDPWM-2, 3, & 4. Apart from obtaining waveform symmetries, the proposed DDPWM schemes ensure that the dc-link capacitor of the inverter operating with lower dc-link voltage is not overcharged by its high voltage counterpart, which is a nagging problem in the unsymmetrical four-level OEWIMD.

Further, the relative performances of these PWM schemes are investigated by comparing them with the decoupled centre-spaced SVPWM schemes reported in earlier literature, namely, the EDPWM and the PDPWM schemes. To this end, an improvised loss model is developed, which computes the switching power loss and conduction power loss of the dual-inverter system. This model also accounts for the conduction losses incurred in the anti-parallel diodes and the additional power loss due to the reverse recovery current of the diodes.

A comparative study is also undertaken to assess the performance of DDPWM schemes vis-à-vis the earlier decoupled schemes (i.e. EDPWM and PDPWM). The aspects considered for the sake of comparison are: switching power loss, conduction power loss and the total losses in the dual-inverter system, THD and WTHD. Simulation results reveal that, DDPWM schemes perform better than the EDPWM and the PDPWM schemes in all of the above aspects expect WTHD in the higher range of the modulation index when compared to the EDPWM.

Additionally, the DDPWM schemes result in considerably lower dv/dt across the power semiconductor devices when compared to the decoupled centre-spaced SVPWM schemes, resulting in the longevity of bearings and winding insulation.

Chapter 3

Single Inverter Switched SVPWM Schemes for a Four-Level Open-End Winding Induction Motor Drive

Contents

3.1 Introduction

The previous chapter proposes Discontiuous Decoupled SVPWM (DDPWM) schemes for the dual-inverter fed four-level OEWIMD. These PWM schemes achieve the objective of avoiding the overcharging of the capacitor connected to the dc-link of lower voltage. The previous chapter also provides an assesment of the DDPWM schemes vis-à-vis their centre-spaced counterparts.

This chapter investigates the possibility of switching only one inverter of the dual-inverter system, as switching both of them could lead to higher switching power loss.

The dual-inverter fed four-level OEWIMD with unequal dc-link voltages (which are in the ratio of 2:1) is reproduced in Fig. 3.1 to facilitate an easy reference. The resultant space vector diagram is also shown in Fig. 3.2.

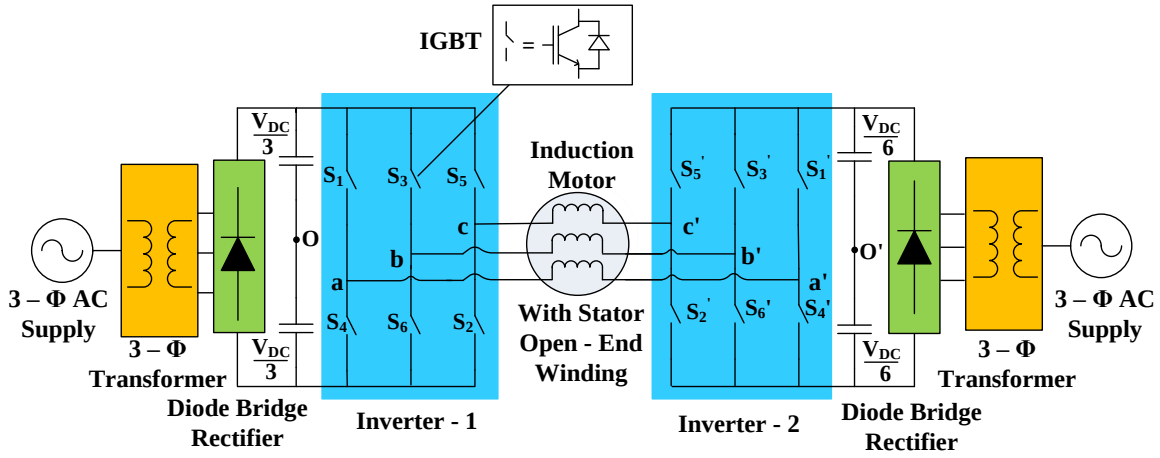


Fig. 3.1: A four-level OEWIMD with unequal dc-link voltages

As discussed in the previous chapter, the power circuit shown in Fig. 3.1 suffers from a severe shortcoming. To be able to implement the minimum-ripple SVPWM technique [62], it is imperative to have inverter-1 clamped to a fixed state in any given sampling time period, while inverter-2 is switched. However, for the switching combinations 11′, 22′, 33′, 44′, 55′, 66′, 12′, 16′, 23′, 34′, 45′ and 56′ (see Fig. 3.2), which are pivotal to implement this scheme (i.e. switching the vertices situated in the closest vicinity to the sample), cannot be employed

[62, 65]. When these troublesome combinations are used, the capacitor of the lower dc-link voltage (which feeds inverter-2) is overcharged by its counterpart feeding inverter-1 (which is of a higher voltage). Thus, the required dc-link ratio of 2:1 is disturbed, which distorts the motor phase voltages and currents rendering the circuit unusable.

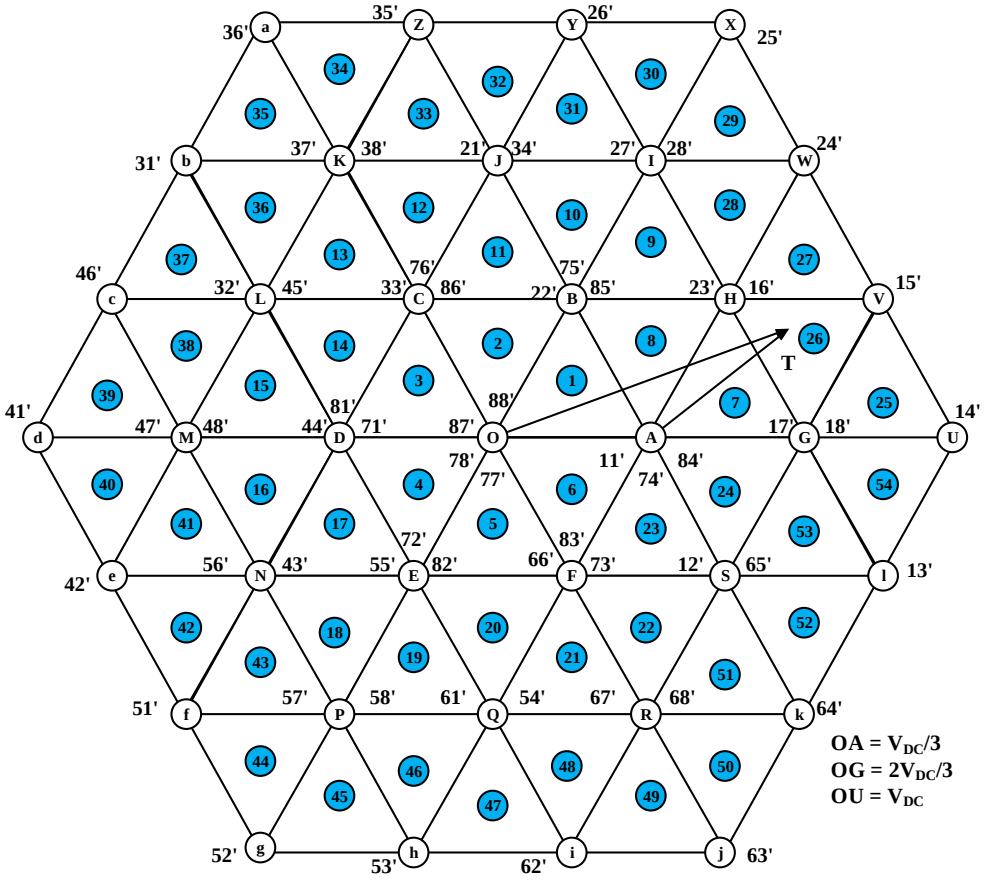


Fig. 3.2: Space vector combinations of dual-inverter system

To circumvent this problem, the work reported in [65] employs the decoupled SVPWM technique, which proposes to resolve the overall reference voltage vector of the dual-inverter system into two anti-phased components, which are in the ratio of 2:1. These components are then individually synthesized by the respective inverters. Two versions of the decoupled SVPWM technique are reported in [65], namely: (i) the equal duty scheme and (ii) the proportional duty scheme. It has been shown that both of these PWM schemes avoid the overcharging phenomenon. However, the price paid to avoid this overcharging is excessive switching, as both inverters are switched. The switching power loss is therefore higher with both of these schemes. It is shown in [65] that the latter scheme is slightly better compared to

the former in this aspect. The other disadvantages include a high dv/dt in the output voltage waveform and an inferior spectral performance.

To reduce the total switching power loss of the dual-inverter system and to improve the drive performance, chapter-2 presents four variants of DDPWM techniques for a four-level OEWIMD. It has been shown that, the proposed DDPWM techniques perform better as compared to the EDPWM and PDPWM techniques and achieve all waveform-symmetries with less dv/dt in the output voltage waveform. Among the four variants of DDPWM techniques, the DDPWM-1 technique registers better performance.

In this chapter, a simple SVPWM technique is proposed to improvise the performance of the four-level OEWIMD shown in Fig. 3.1. It is shown that clamping inverter-2 (the one operating with lower dc-link voltage) and switching inverter-1 (the one operating with higher dc-link voltage) would yield better results compared to both of the decoupled SVPWM strategies reported in [65] and the DDPWM techniques proposed in Chapter-2. Various indices of performance such as Total Harmonic Distortion (THD) in voltage, Weighted THD (WTHD), power loss in the dual inverter system (comprising of switching and conduction power loss) with the proposed SVPWM technique are simulated and compared with the DDPWM-1 technique presented in Chapter-2.

3.2 Principle of the Proposed Biasing SVPWM Scheme

The proposed PWM scheme uses inverter-2 as the clamping inverter, which produces the vectored offset around which inverter-1 is switched. This means that, inverter-2 is employed as the biasing inverter to provide the required vectored offset (or the biasing vector). It may be noted that this simple alteration avoids of the deployment of the troublesome vector combinations cited in the previous section [65] and results in a considerably better performance of the dual-inverter fed OEWIMD compared to the DDPWM techniques proposed in Chapter-2.

The Proposed PWM scheme can be explained with the help of Fig. 3.2, which shows a core hexagon ABCDEF, centered around O. Fig. 3.2 also shows six more hexagons, termed *Sub-hexagons*, which are *OBHGSF*, *OCJIHA*, *ODLKJB*, *OENMLC*, *OFQPND* and *OASRQE*, respectively centered around the so-called *Sub-hexagonal centers A, B, C, D, E* and *F*. The sub-hexagonal centers provide the vectored offset to the biasing inverter (i.e. inverter-2).

Let it be assumed that the reference voltage space vector $(\boldsymbol{v_{sr}})$ ***OT,*** located in sector 26 (Fig. 3.2), is to be synthesized by the dual-inverter system shown in Fig. 3.1. The overall dc-link voltage (V_{DC}) is given by the vector ***OU*** (Fig. 3.2). The modulation index m_a is defined as:

$$m_a = \frac{\boldsymbol{OT}}{\boldsymbol{OU}} = \frac{|\boldsymbol{v_{sr}}|}{V_{DC}} \tag{3.1}$$

The dual-inverter system is so scaled that the rated frequency (50 Hz) and rated line voltage (400 V, line-line) are delivered at the limit of liner modulation, which is $(\sqrt{3}/2)$ with SVPWM scheme. With this scaling, the frequency of the fundamental component of the dual inverter system at a modulation index of m_a would become:

$$f_1 = \frac{m_a}{\sqrt{3}/2} \times 50 \tag{3.2}$$

Further, the reference phase voltages, which constitute the reference voltage space vector of the dual-inverter system, are sampled 42 times per one cycle irrespective of the frequency. This results in 7 samples per sector. In order to obtain waveform symmetries, samples at sector boundaries are avoided [65]. The angle between successive samples is 8.57^0 $(i.e. 360°/42)$. The sampling time period is given as:

$$T_s = \frac{1}{f_1 \times 42} \tag{3.3}$$

The reference vector ***OT*** can be resolved into two components ***OA*** and ***AT*** (Fig. 3.2), which respectively constitute the biasing and switching vectors. The column vectors corresponding to the instantaneous phase reference voltages of vectors ***OT*** and ***AT*** are respectively given by $[v_a{}^* \; v_b{}^* \; v_c{}^*]^T$ and $[v_a \; v_b \; v_c]^T$. With an appropriate coordinate transformation it can be shown that:

$$[v_a \;\; v_b \;\; v_c \;]^T \;=\; I_3\,[v_a^* \;\; v_b^* \;\; v_c^*]^T + \frac{2V_{dc}}{9}\begin{bmatrix} -\cos\big((m-1)\times\pi/3\big) \\ \cos(m\pi/3) \\ \cos\big((m-2)\times\pi/3\big) \end{bmatrix} \qquad (3.4)$$

where

$I_3 \;= 3 \times 3$ Unity Diagonal Matrix

m = 1, 2… 6 corresponding to the sub hexagonal centers A, B,…F

It can be so arranged that the vector **OA** is output by inverter-2 in a given sampling time interval. The vector **AT** is synthesized, in the average sense with inverter-1 by switching amongst the vertices **A**, **U** and **W** (Fig. 3.2). This would clamp inverter-2 at the state $4'$ (- + +) during the sampling time period, while inverter-1 switches through the states 8(---), 1(+ - -), 2(++-) and 7(+++). Thus, the space vector combinations $84'$, $14'$, $24'$ and $74'$ are sequentially deployed with this switching strategy. The sum of the time periods for which states $14'$ and $24'$ are switched is called the effective time period and is denoted by $'T_{eff}'$. The sum of the time periods for which the vector combinations $84'$ and $74'$ are switched is denoted by the symbol $'T_z'$. To obtain the gating pulses for the switching inverter, the switching algorithm reported in [98] is employed, which is based on the concept of imaginary switching time periods. The flow chart of the switching algorithm is presented in Fig. 3.3.

Depending on the distribution of the time interval $'T_z'$ amongst the contending vector combinations $84'$ and $74'$, three possibilities arise (Fig. 3.3): (i) the time period $'T_z'$ is equally distributed amongst them (ii) the combination $84'$ is switched for the entire time period $'T_z'$ and (iii) the combination $74'$ is switched for the entire time period $'T_z'$ [98]. Of these three variants, the first is known as the Centre Spaced PWM (CSPWM) technique, while the latter two are known as the Phase Clamped PWM-1 (PCPWM-1) and Phase Clamped PWM-2

(PCPWM-2) strategies respectively. The generalized offset time period to realize these three variants is given by the expression:

$$T_{offset} = KT_z/2 - T_{min} \tag{3.5}$$

Where

K = 1, 0, 2 for CSPWM, PCPWM-1 and PCPWM-2 respectively.

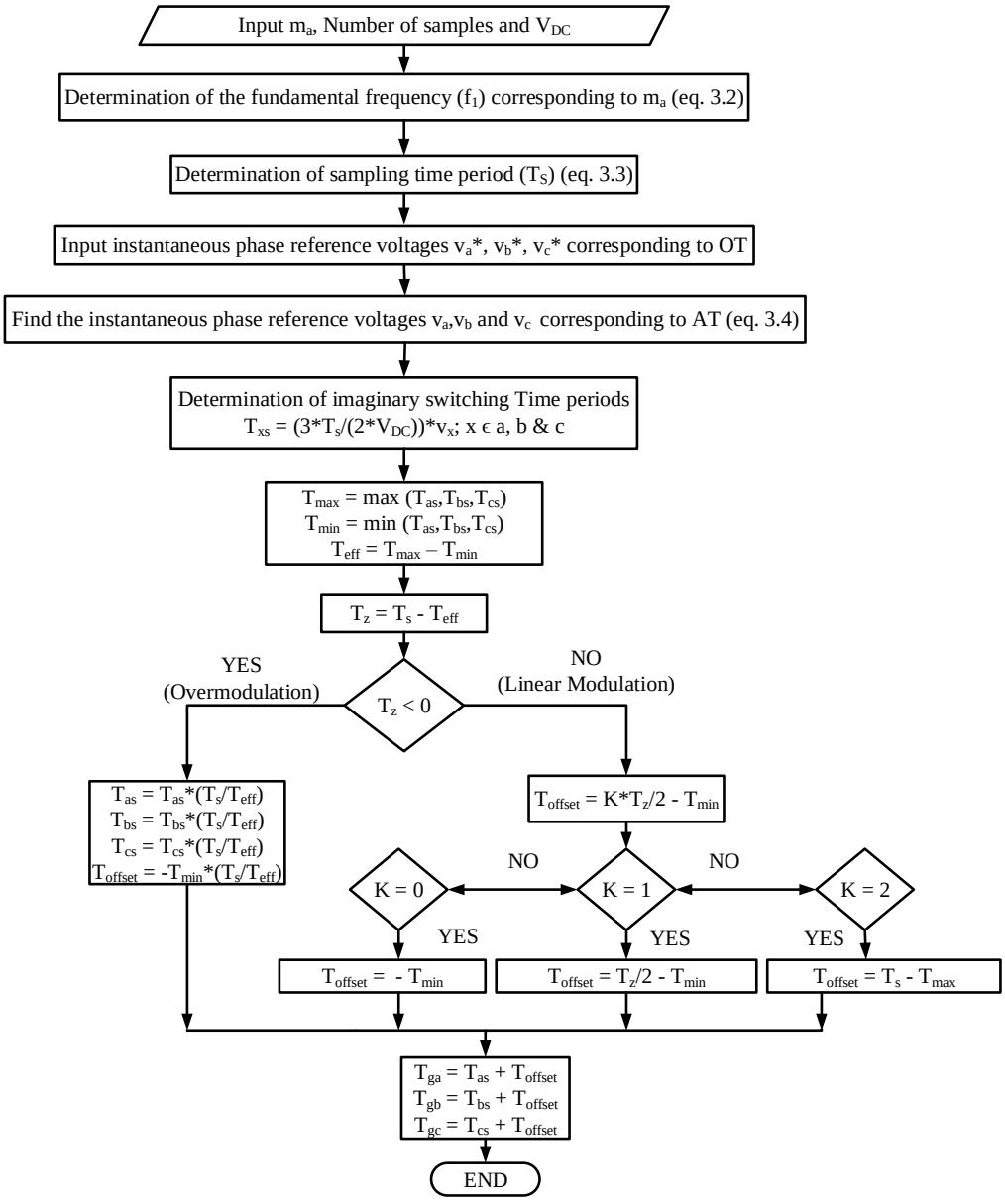


Fig. 3.3: Flow chart of proposed SVPWM Strategy

In other words, PCPWM-1 and PCPWM-2 are realized by placing the effective time period (T_{eff}) either at the left edge (i.e. K = 0) or at the right edge (K = 2). It may be noted

that K = 1 corresponding to the case of CSPWM. To achieve the waveform symmetries with the PCPWMs-1&2, the switching sequences employed in Chapter-2 for the implementation of the DDPWM techniques are extended here and shown in Table 3.1, when the tip of the reference vector $\boldsymbol{OT}$ in sector-1 (i.e. for a span of 60^0).

Table 3.1: Switching sequences of Inverter-1 with PCPWM-1 & 2 in sector-1

Sample No.	PCPWM-1	PCPWM-2	K
1	1 – 2 – 7	2 - 1 - 8	2
2	7 - 2 – 1	8 - 1 - 2	0
3	1 - 2 – 7	2 - 1 - 8	2
4	7-2-1-8	8-1-2-7	1
5	8 - 1 – 2	7 - 2 - 1	0
6	2 - 1 – 8	1 - 2 - 7	2
7	8 - 1 – 2	7 - 2 - 1	0

When $|\boldsymbol{OT}| > |\boldsymbol{OU}|$, the tip of the reference vector lies outside the hexagon (Fig. 3.2). In such a case, the time period $'T_z'$ would become negative, which calls for the necessity to implement over modulation. The negative value of $'T_z'$ is re-adjusted to a value of zero by multiplying the imaginary switching time periods and the offset time period with a factor of T_S/T_{eff}.

The modulating functions for the three variants i.e. CSPWM, PCPWM-1 and PCPWM-2 are presented in Fig. 3.4 at a modulation index of 0.7.

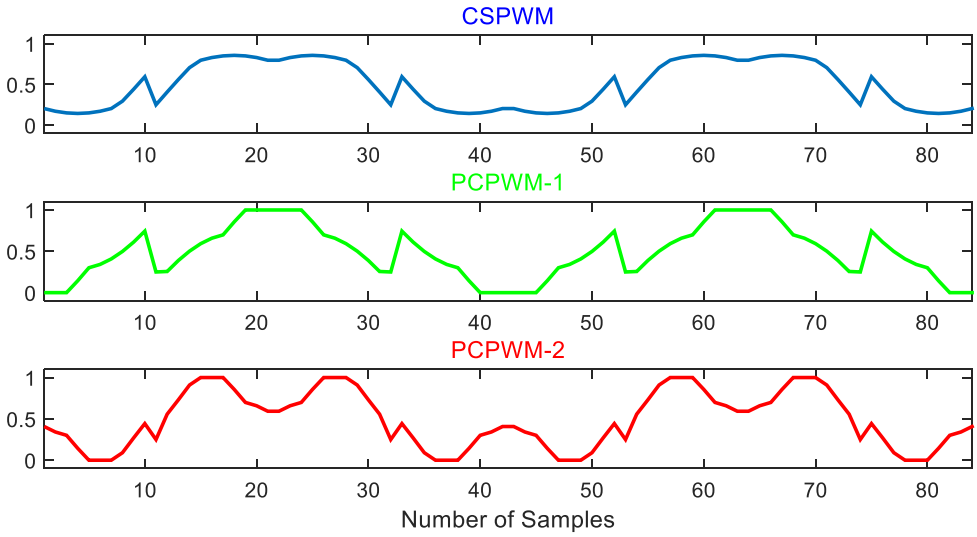


Fig. 3.4: Modulating signals for CSPWM, PCPWM -1 & PCPWM -2

From the traces presented in Fig. 3.4, it is evident that a given phase is clamped either to the positive or negative state. It may therefore be expected that the switching losses with PCPWM-1 and PCPWM-2 would be significantly lesser than the centre-spaced SVPWM case.

3.3 Simulation & Experimental Results

The four-level OEWIMD shown in Fig. 3.1 with the proposed SVPWM scheme is simulated using *MATLAB/Simulink* and is implemented experimentally with *dSPACE-1104* system. The drive is operated with *V/Hz* control in open-loop and its performance is compared with the Discontinuous Decoupled SVPWM-1 technique. The dc-link voltages used in the present work are 200 V for inverter-1 and 100 V for inverter-2 respectively. In other words, the effective dc-link voltage is equal to 300 V.

The four-level OEWIMD could be operated at various modulation indices covering the entire speed range. When, the modulation index $m_a \leq 0.33$, the sample is situated within the core hexagon ABCDEF (Fig. 3.2). It is obvious that one doesn't need both inverters to synthesize the sample in this case. Hence only inverter-2 is switched, clamping inverter-1 to a null state (Fig. 3.1).

The four-level OEWIMD is operated in the entire speed range and results are shown at three different modulation indices. The fundamental frequency varies linearly with respect to the modulation index up to 0.866. Above this limit, the dual-inverter system operates in the region of over modulation and the relation between them becomes nonlinear.

The simulated and experimental results obtained for the CSPWM is shown in Figs. 3.5-3.10 for the modulation index $m_a = 0.4$. Fig. 3.5, 3.6 shows the simulated and experimentally obtained pole voltages of inverter-1 and 2. The fundamental frequency for this modulation index is 23.1 Hz (eq. 3.2). The Simulated and experimentally obtained zero-sequence voltages, which are dropped across the points O and O', are shown in Fig. 3.7. The simulated and experimental motor phase voltage (which is obtained after the subtraction of

the common mode voltage from the difference of pole voltages) and the simulated harmonic spectrum of the motor phase voltage are shown in Figs. 3.8 and 3.9. Fig. 3.10 shows no-load phase current of dual-inverter drive system.

Similar results are shown in Figs. 3.11-3.16 for modulation index of 0.7. At this depth of modulation, the OEWIMD operates with a fundamental frequency of 40.4 Hz (eq. 3.2). Figs. 3.17-3.22 presents the simulation and experimentally obtained results for over modulation, where in the hexagon UXadgj (Fig. 3.2) is traced by the tip of the reference voltage space vector, with the fundamental frequency of 50 Hz.

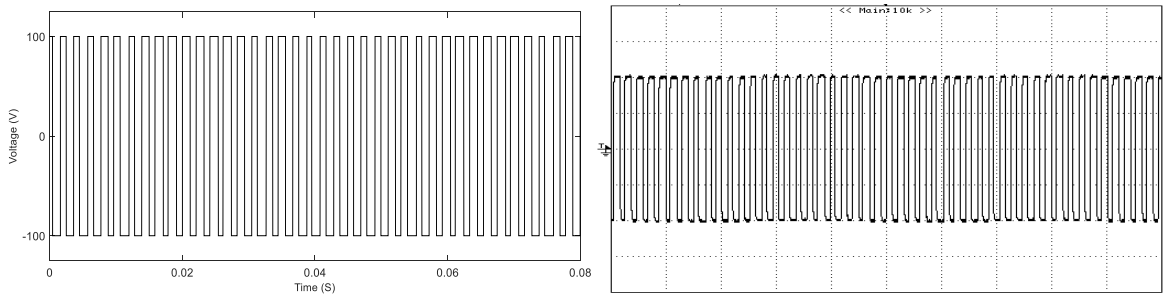


Fig. 3.5: Simulated (left) and experimentally (right) obtained inverter-1 pole voltage at m_a = 0.4 for CSPWM. Scale: X-axis: 20 ms/div, Y-axis: 50 V/div

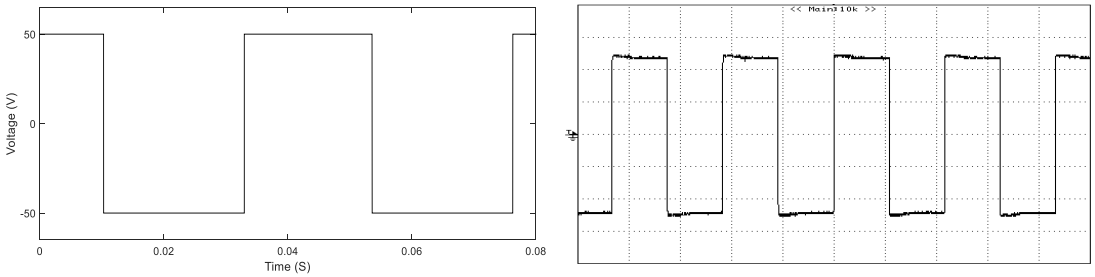


Fig. 3.6: Simulated (left) and experimentally (right) obtained inverter-2 pole voltage at m_a = 0.4 for CSPWM. Scale: X-axis: 20 ms/div, Y-axis: 20 V/div

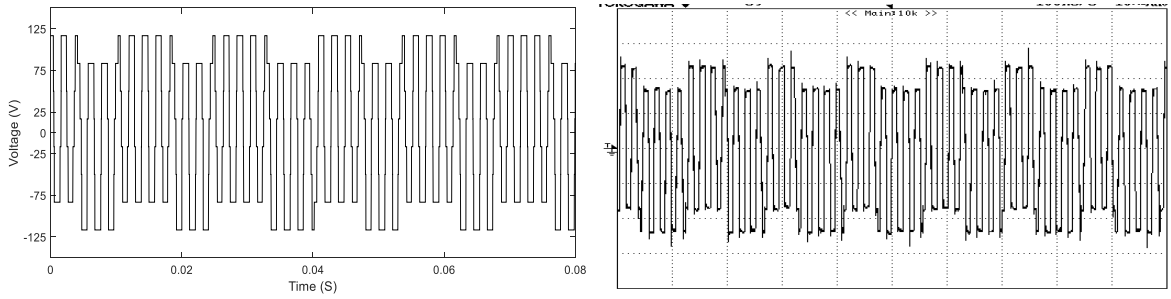


Fig. 3.7: Simulated (left) and experimentally (right) obtained common mode voltage at m_a = 0.4 for CSPWM. Scale: X-axis:10 ms/div, Y-axis: 50 V/div

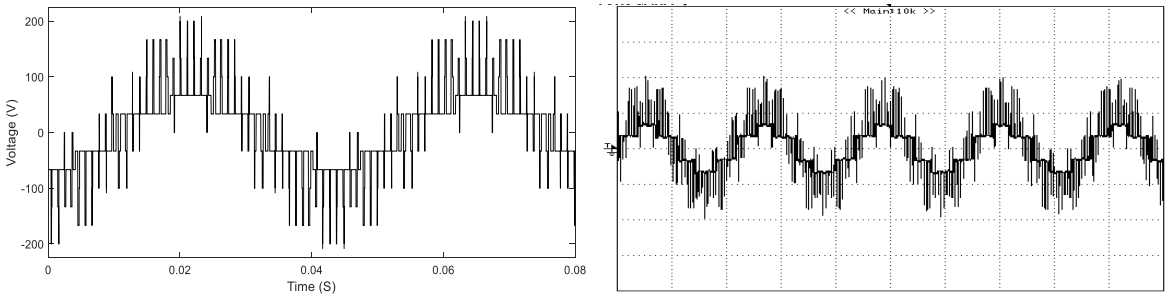


Fig. 3.8: Simulated (left) and experimentally (right) obtained Phase-A voltage at m_a = 0.4 for CSPWM. Scale: X-axis: 20 ms/div, Y-axis: 100 V/div.

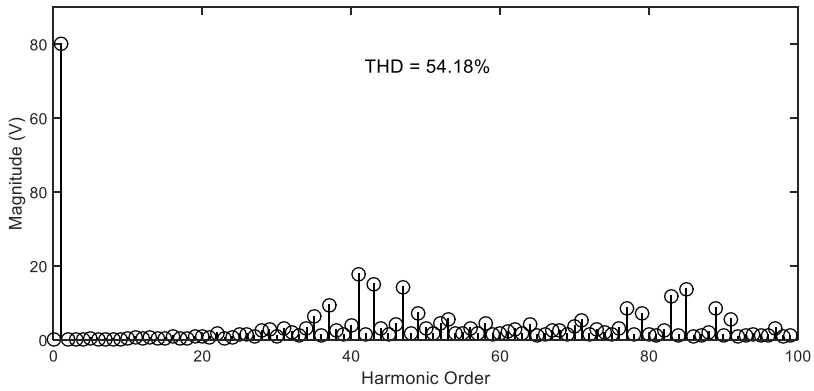


Fig. 3.9: FFT analysis of Phase-A voltage at m_a = 0.4 for CSPWM

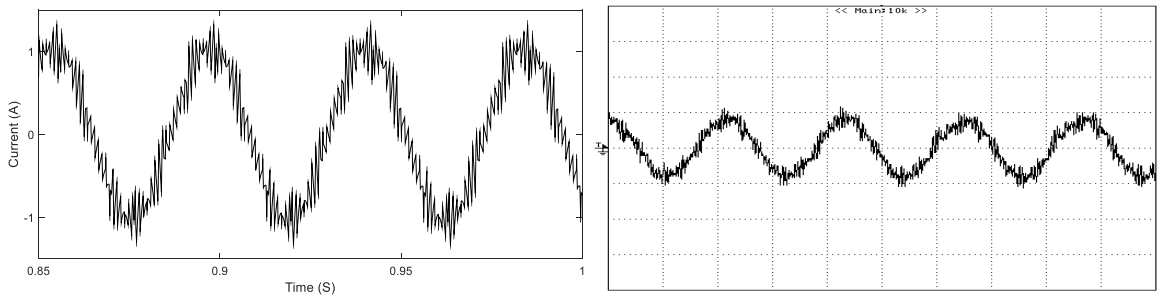


Fig. 3.10: Simulated (left) and experimentally (right) obtained Phase-A Current at m_a = 0.4 for CSPWM. Scale: X-axis: 20 ms/div, Y-axis: 1 A/div.

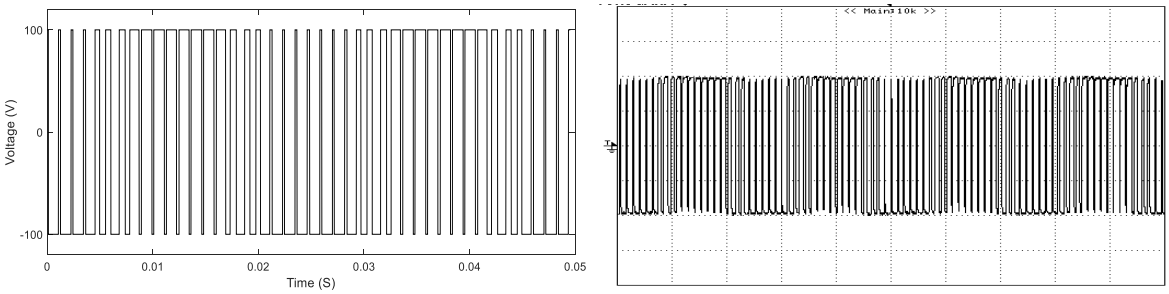


Fig. 3.11: Simulated (left) and experimentally (right) obtained inverter-1 pole voltage at m_a = 0.7 for CSPWM. Scale: X-axis: 10 ms/div, Y-axis: 50 V/div.

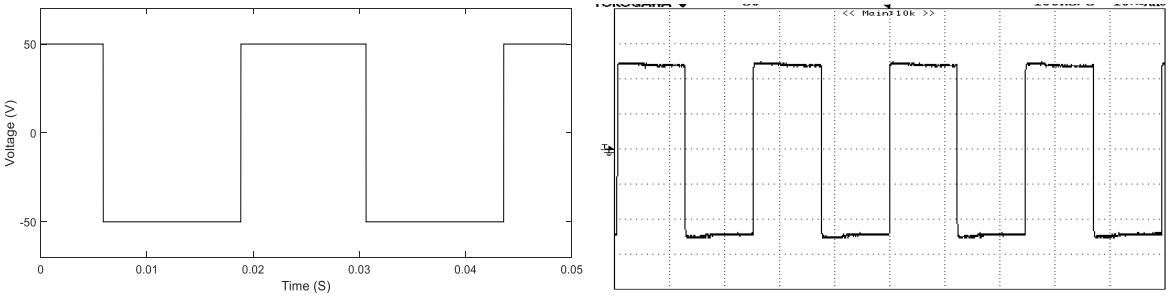


Fig. 3.12: Simulated (left) and experimentally (right) obtained inverter-2 pole voltage at $m_a = 0.7$ for CSPWM. Scale: X-axis: 10 ms/div, Y-axis: 20 V/div.

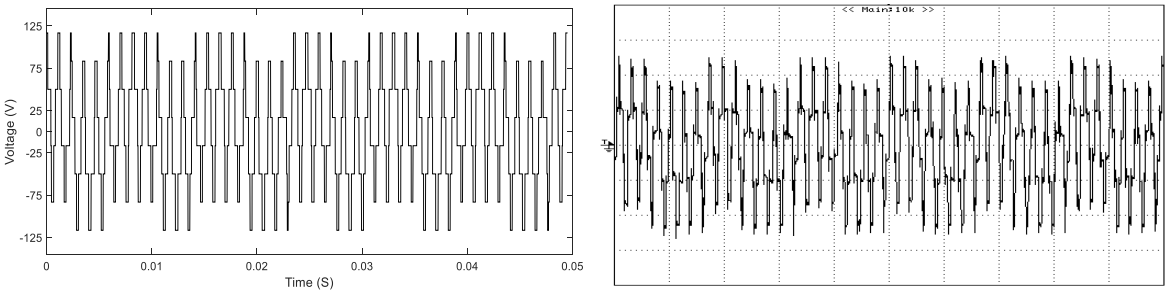


Fig. 3.13: Simulated (left) and experimentally (right) obtained common mode voltage at $m_a = 0.7$ for CSPWM. Scale: X-axis: 5 ms/div, Y-axis: 50 V/div.

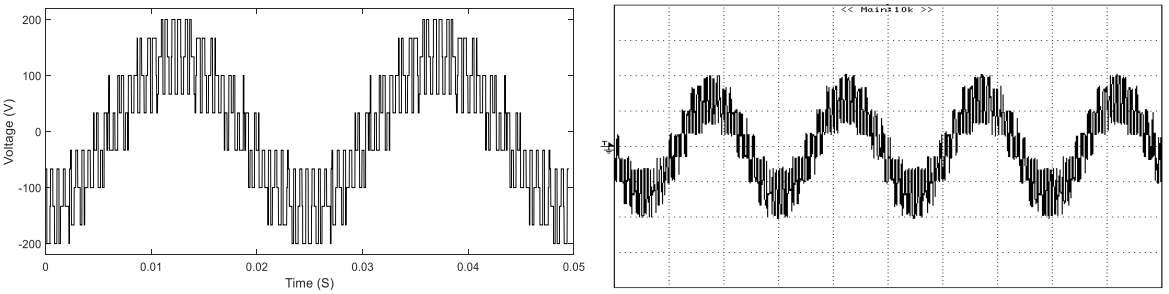


Fig. 3.14: Simulated (left) and experimentally (right) obtained Phase-A voltage at $m_a = 0.7$ for CSPWM. Scale: X-axis: 10 ms/div, Y-axis: 100 V/div.

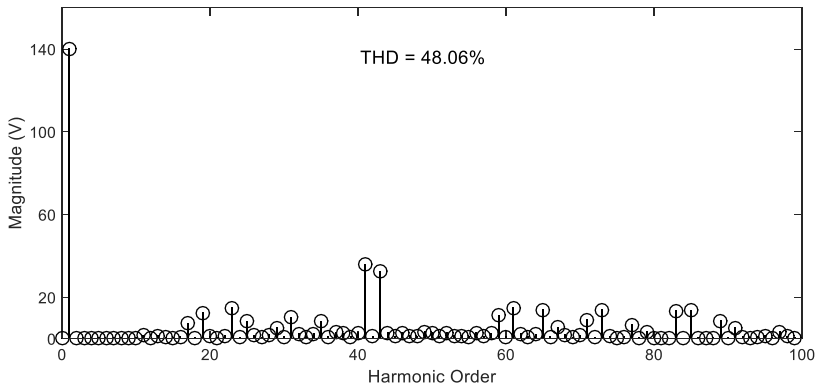


Fig. 3.15: FFT analysis of Phase-A voltage at $m_a = 0.7$ for CSPWM

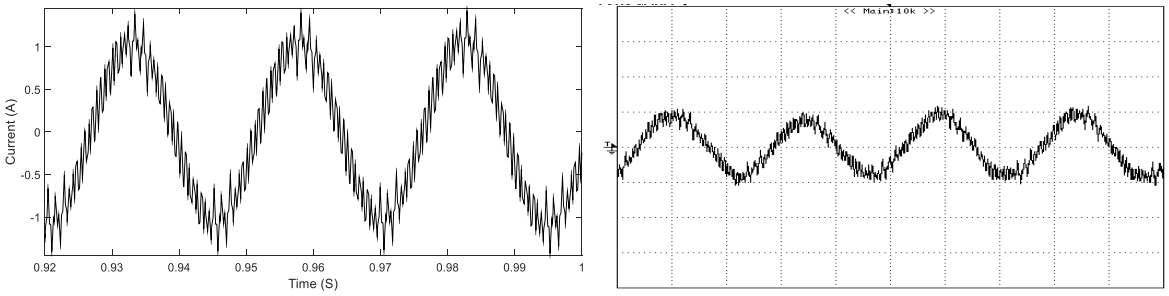


Fig. 3.16: Simulated (left) and experimentally (right) obtained Phase-A Current at $m_a = 0.7$ for CSPWM.
Scale: X-axis: 10 ms/div, Y-axis: 1 A/div.

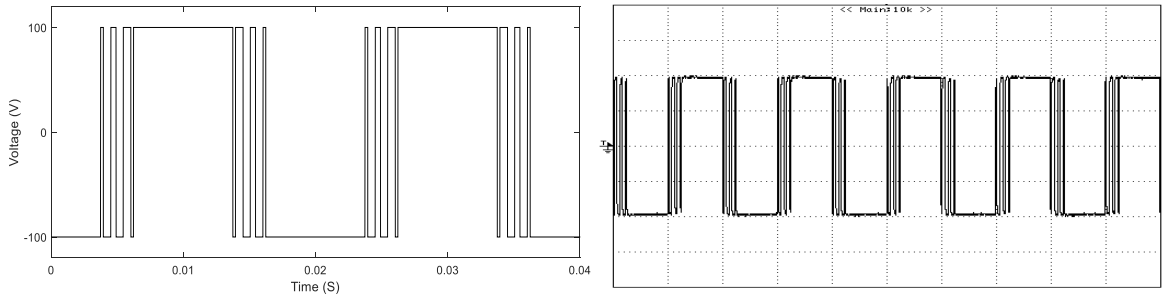


Fig. 3.17: Simulated (left) and experimentally (right) obtained inverter-1 pole voltage at $m_a = 1$ for CSPWM.
Scale: X-axis: 10 ms/div, Y-axis: 50 V/div.

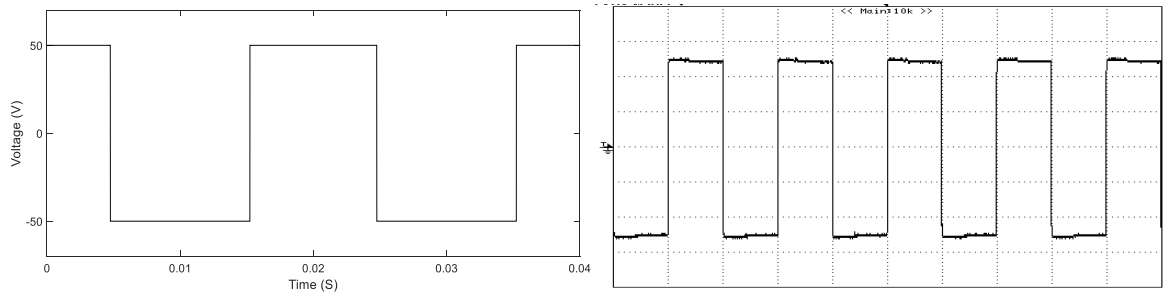


Fig. 3.18: Simulated (left) and experimentally (right) obtained inverter-2 pole voltage at $m_a = 1$ for CSPWM.
Scale: X-axis: 10 ms/div, Y-axis: 20 V/div.

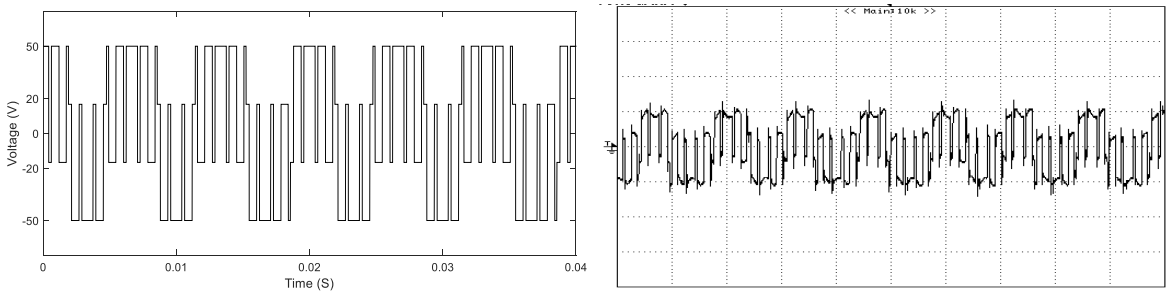


Fig. 3.19: Simulated (left) and experimentally (right) obtained common mode voltage at $m_a = 1$ for CSPWM.
Scale: X-axis: 5 ms/div, Y-axis: 50 V/div.

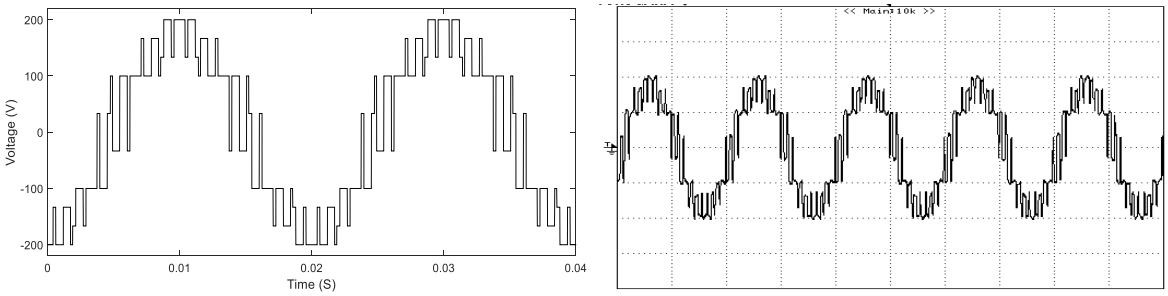


Fig. 3.20: Simulated (left) and experimentally (right) obtained Phase-A voltage at m_a = 1 for CSPWM. Scale: X-axis: 10 ms/div, Y-axis: 100 V/div.

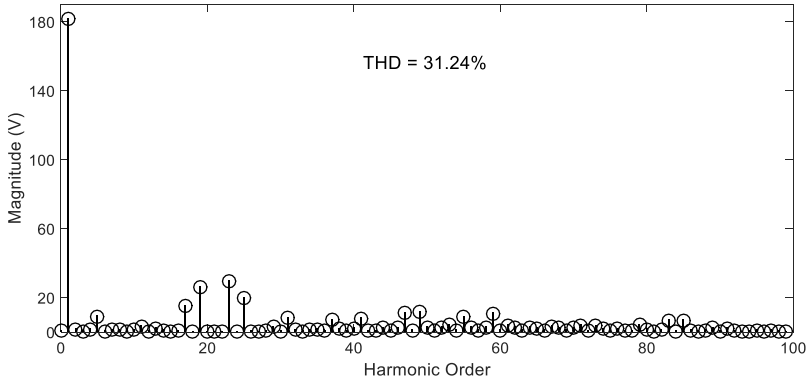


Fig. 3.21: FFT analysis of Phase-A voltage at m_a = 1 for CSPWM

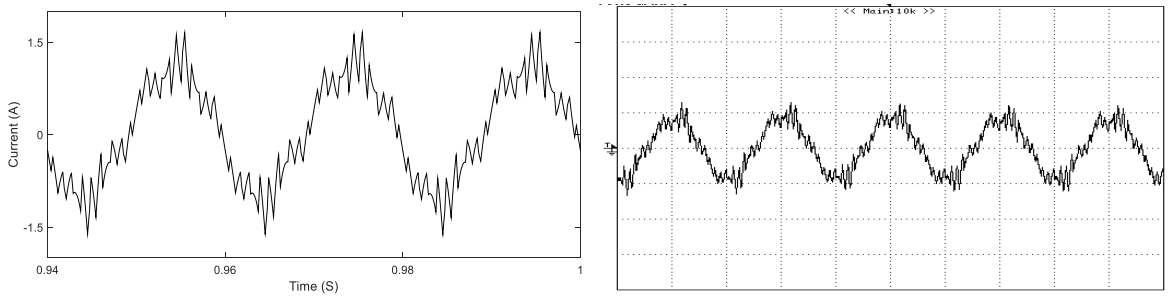


Fig. 3.22: Simulated (left) and experimentally (right) obtained Phase-A Current at m_a = 1 for CSPWM. Scale: X-axis: 10 ms/div, Y-axis: 1 A/div.

It is possible to reduce the switching power loss of the dual-inverter system by clamping one of the phases of the switching inverter (i.e. inverter-1). As mentioned in section-3.2, it is accomplished by a simple alteration of the offset time T_{offset} for both of the PCPWM-1&2. The simulated and experimental results with PCPWM-1 are presented in Figs. 3.23-3.34 for m_a = 0.4 and 0.7. Similar results for PCPWM-2 are presented in Figs. 3.35-3.46.

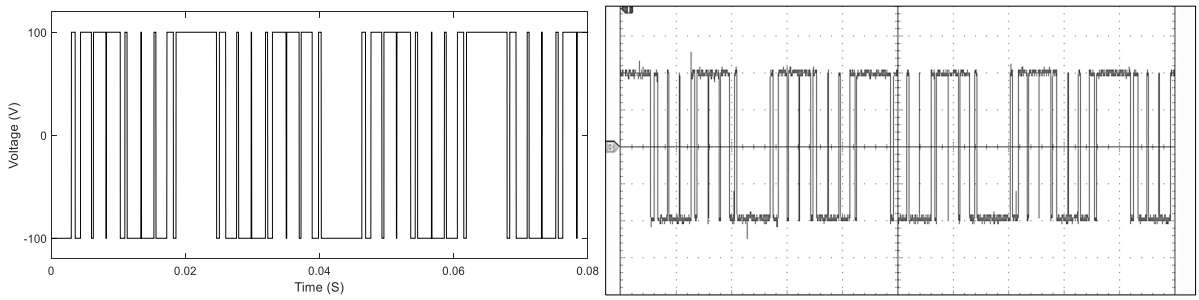


Fig. 3.23: Simulated (left) and experimentally (right) obtained inverter-1 pole voltage at m_a = 0.4 for PCPWM-1. Scale: X-axis: 10 ms/div, Y-axis:50 V/div.

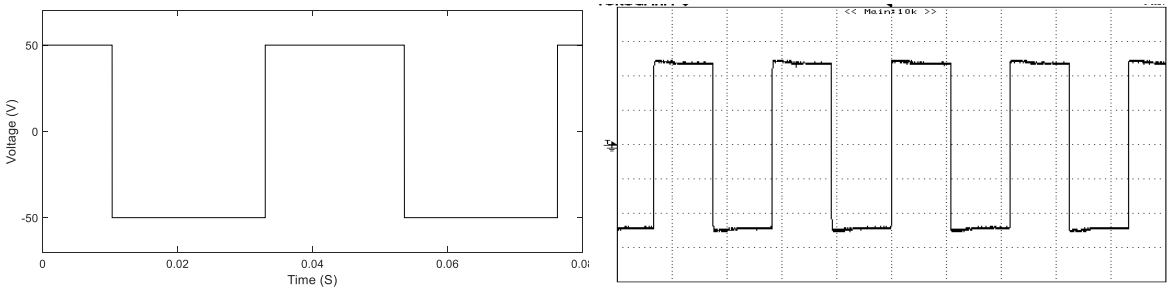


Fig. 3.24: Simulated (left) and experimentally (right) obtained inverter-2 pole voltage at m_a = 0.4 for PCPWM-1. Scale: X-axis: 20 ms/div, Y-axis: 20 V/div.

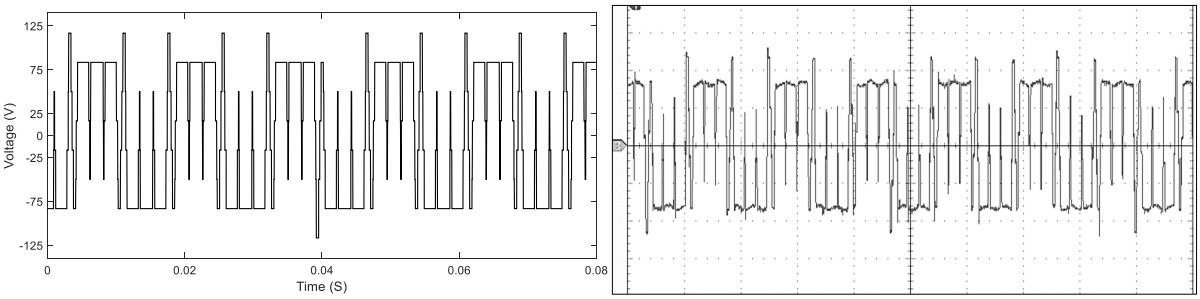


Fig. 3.25: Simulated (left) and experimentally (right) obtained common mode voltage at m_a = 0.4 for PCPWM-1. Scale: X-axis: 10 ms/div, Y-axis: 50 V/div.

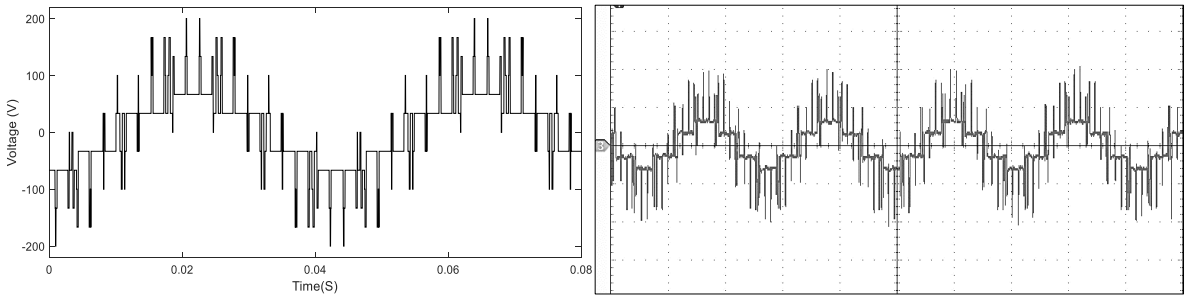


Fig. 3.26: Simulated (left) and experimentally (right) obtained Phase-A voltage at m_a = 0.4 for PCPWM-1. Scale: X-axis: 20 ms/div, Y-axis: 100V/div.

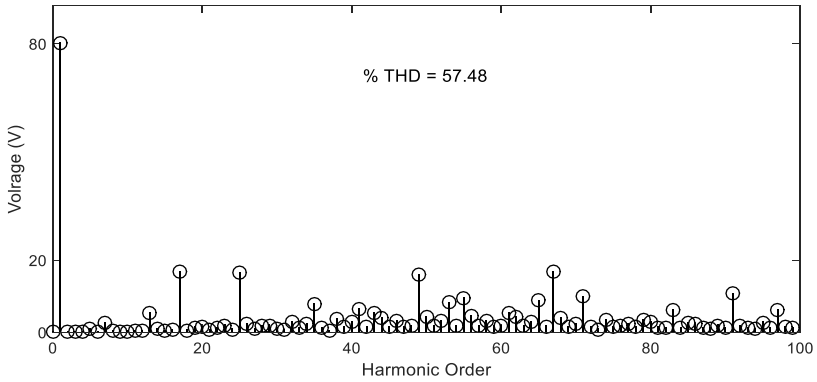


Fig. 3.27: FFT analysis of Phase-A voltage at m_a = 0.4 for PCPWM-1

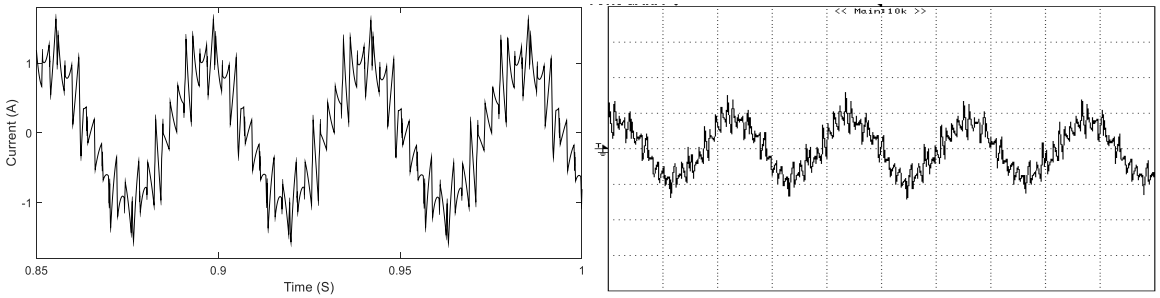


Fig. 3.28: Simulated (left) and experimentally (right) obtained Phase-A Current at m_a = 0.4 for PCPWM-1.

Scale: X-axis: 20 ms/div, Y-axis: 1 A/div.

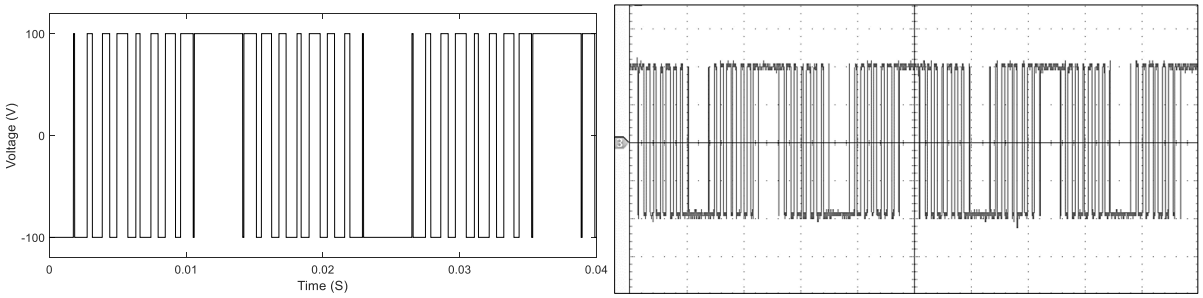


Fig. 3.29: Simulated (left) and experimentally (right) obtained inverter-1 pole voltage at m_a = 0.7 for PCPWM-1.

Scale: X-axis: 10 ms/div, Y-axis: 50 V/div.

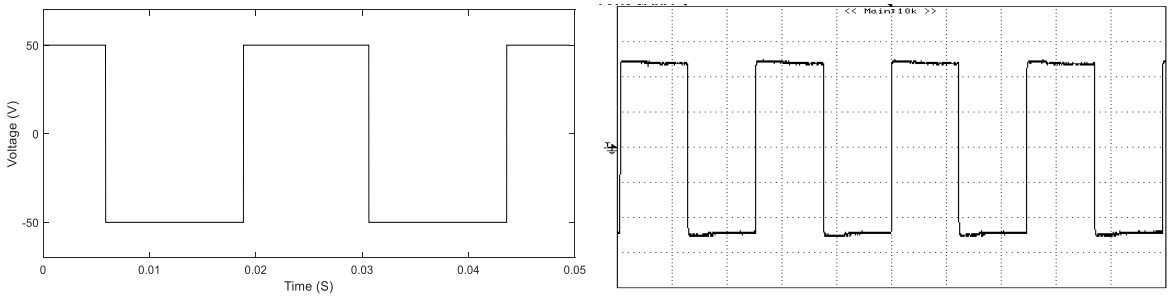


Fig. 3.30: Simulated (left) and experimentally (right) obtained inverter-2 pole voltage at m_a = 0.7 for PCPWM-1.

Scale: X-axis: 10 ms/div, Y-axis: 20 V/div.

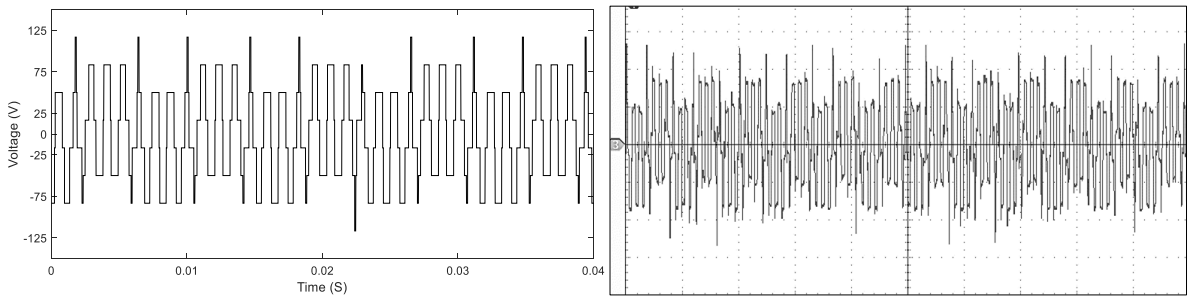


Fig. 3.31: Simulated (left) and experimentally (right) obtained common mode voltage at m_a = 0.7 for PCPWM-1. Scale: X-axis: 10 ms/div, Y-axis: 50 V/div.

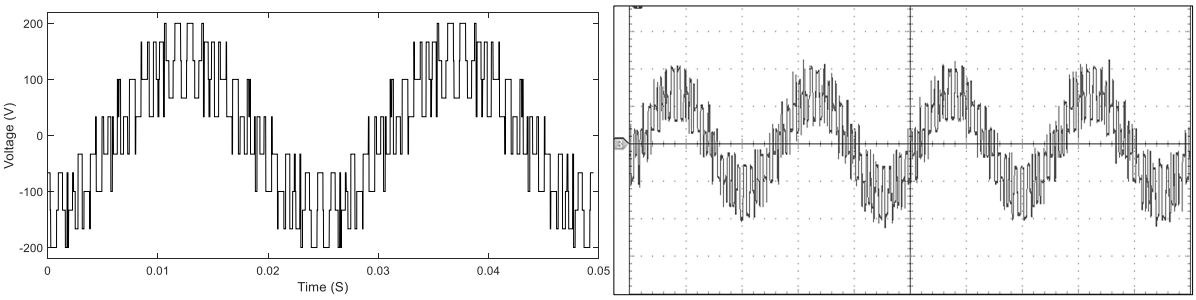


Fig. 3.32: Simulated (left) and experimentally (right) obtained Phase-A voltage at m_a = 0.7 for PCPWM-1. Scale: X-axis: 10 ms/div, Y-axis: 100 V/div.

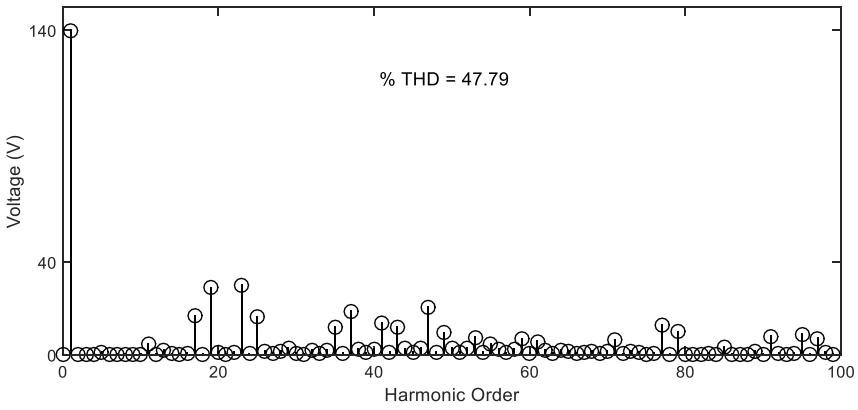


Fig. 3.33: FFT analysis of Phase-A voltage at m_a = 0.7 for PCPWM-1

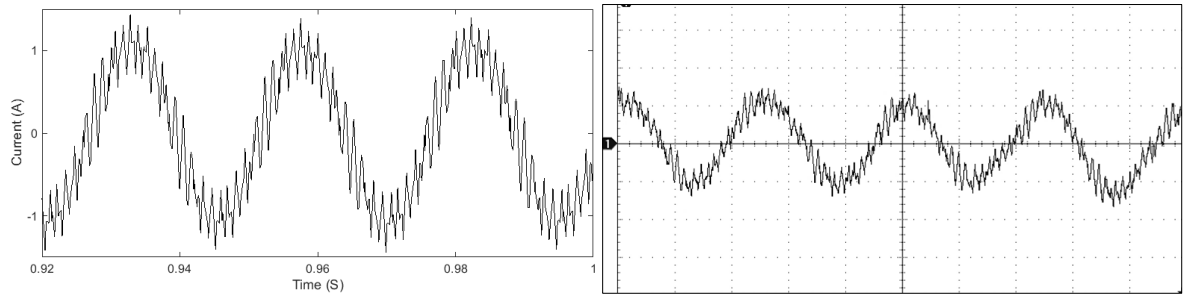


Fig. 3.34: Simulated (left) and experimentally (right) obtained Phase-A Current at m_a = 0.7 for PCPWM-1. Scale: X-axis: 10 ms/div, Y-axis: 1 A/div.

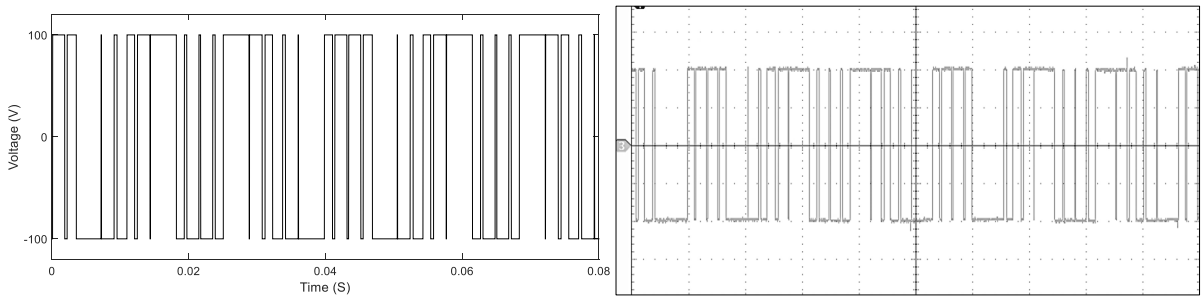


Fig. 3.35: Simulated (left) and experimentally (right) obtained inverter-1 pole voltage at m_a = 0.4 for PCPWM-2. Scale: X-axis: 10 ms/div, Y-axis: 50 V/div.

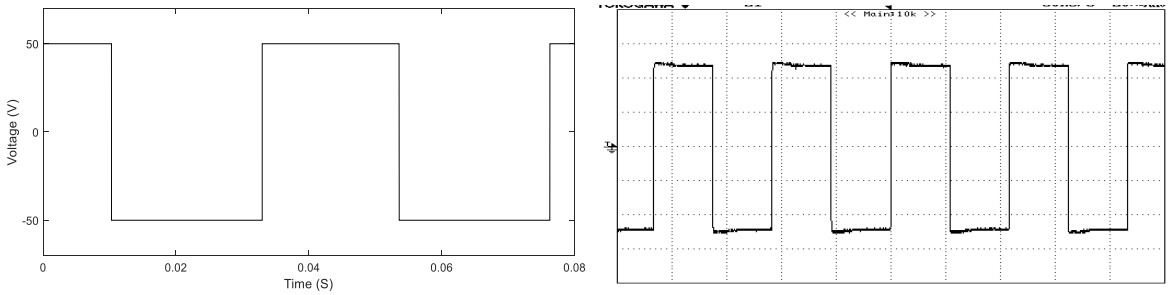


Fig. 3.36: Simulated (left) and experimentally (right) obtained inverter-2 pole voltage at m_a = 0.4 for PCPWM-2. Scale: X-axis: 20 ms/div, Y-axis: 20 V/div.

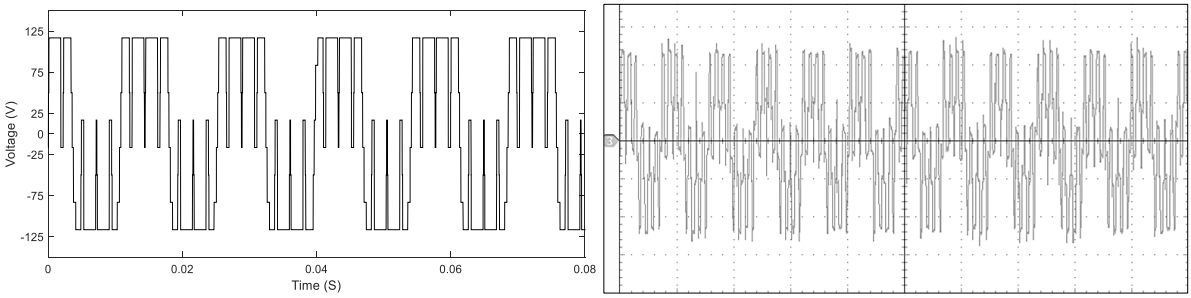


Fig. 3.37: Simulated (left) and experimentally (right) obtained common mode voltage at m_a = 0.4 for PCPWM-2. Scale: X-axis: 10 ms/div, Y-axis: 50 V/div.

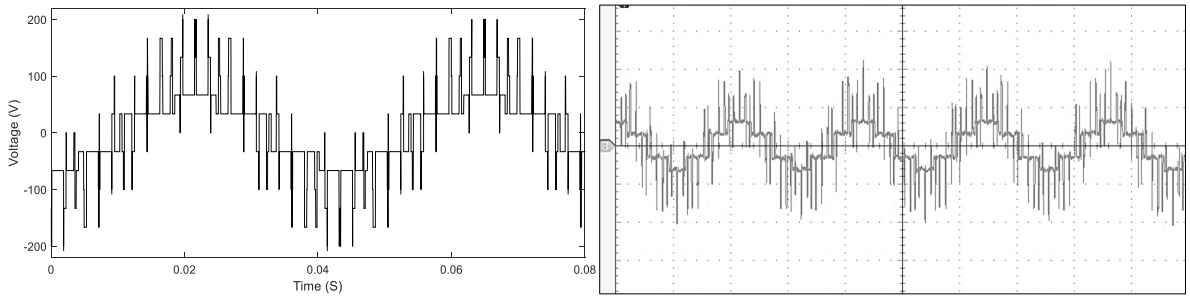


Fig. 3.38: Simulated (left) and experimentally (right) obtained Phase-A voltage at m_a = 0.4 for PCPWM-2. Scale: X-axis: 20 ms/div, Y-axis: 100 V/div.

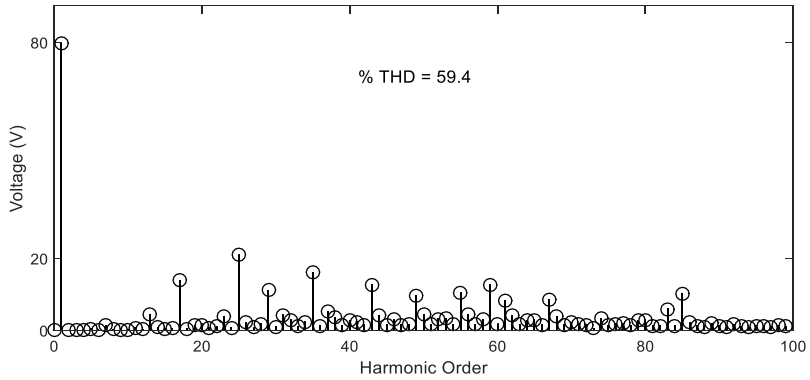


Fig. 3.39: FFT analysis of Phase-A voltage at m_a = 0.4 for PCPWM-2

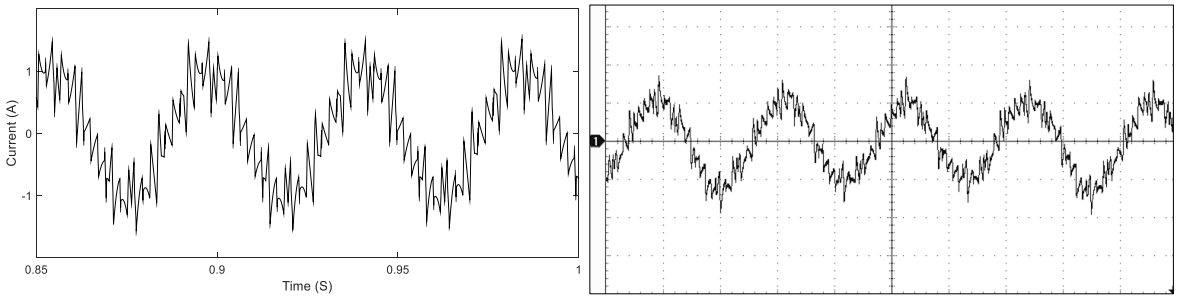


Fig. 3.40: Simulated (left) and experimentally (right) obtained Phase-A Current at m_a = 0.4 for PCPWM-2.
Scale: X-axis: 20 ms/div, Y-axis: 1 A/div.

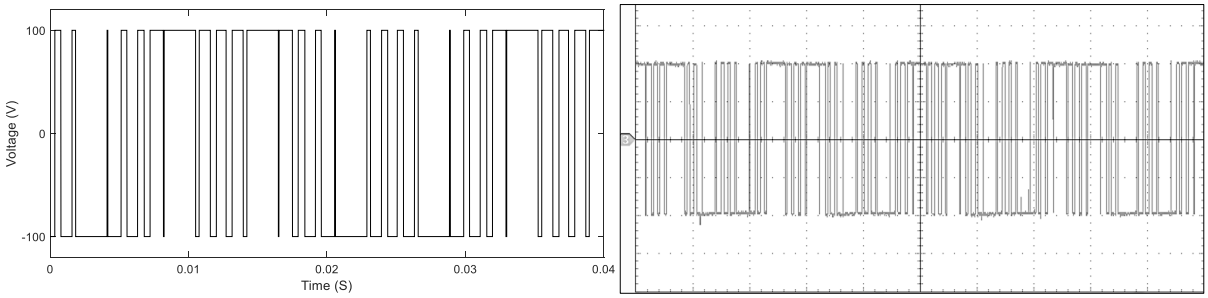


Fig. 3.41: Simulated (left) and experimentally (right) obtained inverter-1 pole voltage at m_a = 0.7 for PCPWM-2.
Scale: X-axis: 10 ms/div, Y-axis: 50 V/div.

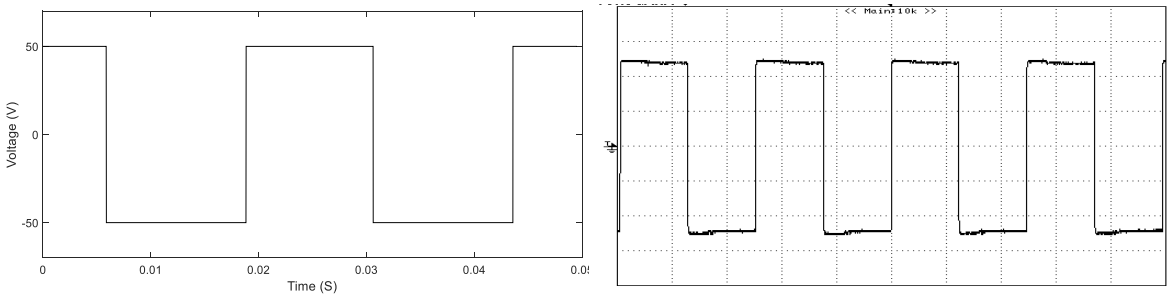


Fig. 3.42: Simulated (left) and experimentally (right) obtained inverter-2 pole voltage at m_a = 0.7 for PCPWM-2.
Scale: X-axis: 10 ms/div, Y-axis: 20 V/div.

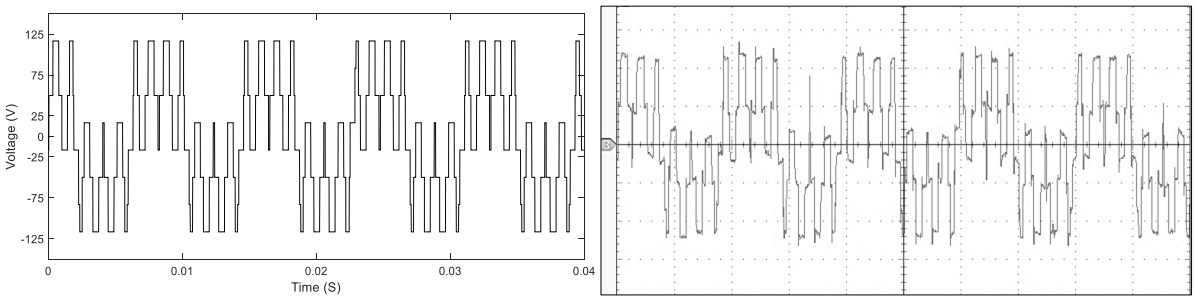


Fig. 3.43: Simulated (left) and experimentally (right) obtained common mode voltage at $m_a = 0.7$ for PCPWM-2. Scale: X-axis: 5 ms/div, Y-axis: 50 V/div.

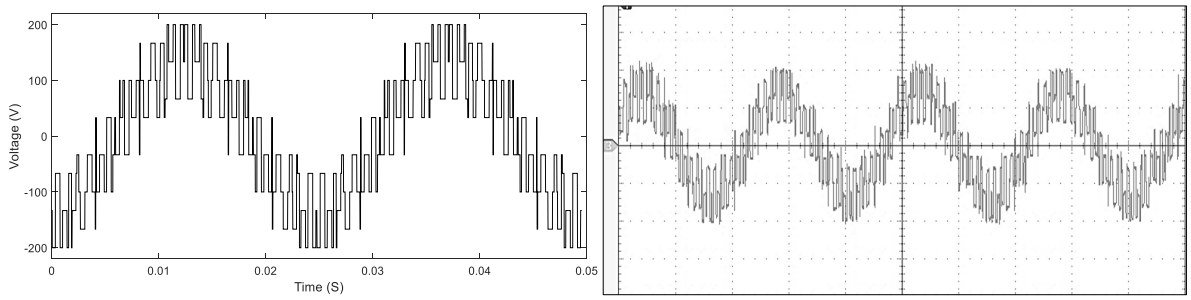


Fig. 3.44: Simulated (left) and experimentally (right) obtained Phase-A voltage at $m_a = 0.7$ for PCPWM-2. Scale: X-axis: 10 ms/div, Y-axis: 100 V/div.

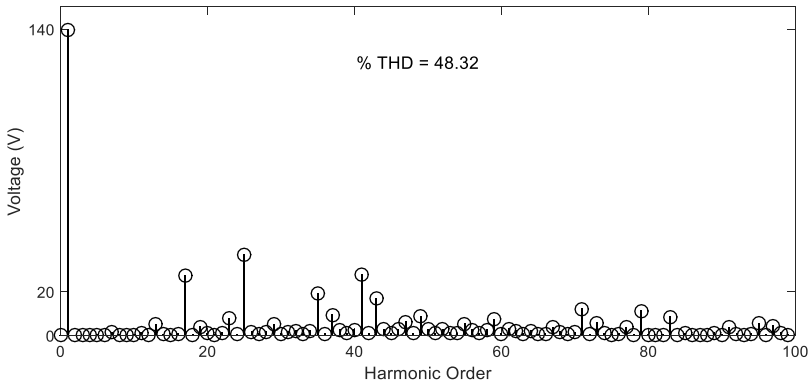


Fig. 3.45: FFT analysis of Phase-A voltage at $m_a = 0.7$ for PCPWM-2

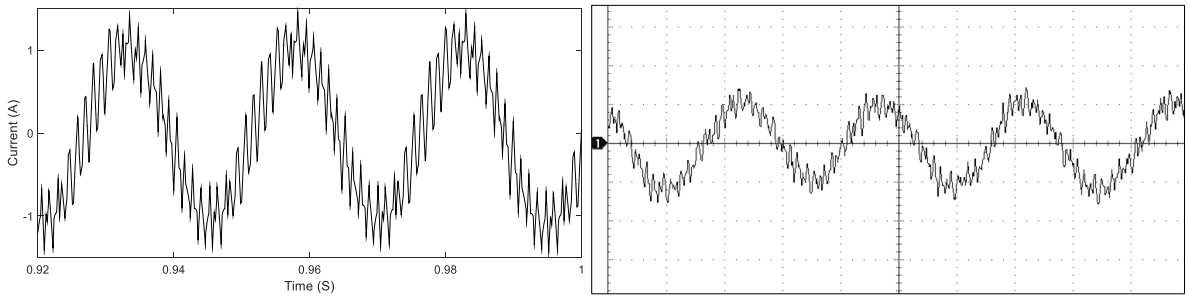


Fig. 3.46: Simulated (left) and experimentally (right) obtained Phase-A Current at $m_a = 0.7$ for PCPWM-2. Scale: X-axis: 10 ms/div, Y-axis: 1 A/div.

It may be observed that the experimental results are in agreement with the simulation results. The comparative evaluation of these three PWM schemes is presented in the next section.

3.4 Comparative Performance Analysis Of Improvised SVPWM techniques

In this section, the performance of the three variants of the SVPWM technique proposed in this chapter (namely CSPWM, PCPWM-1 and PCPWM-2) are compared with the SVPWM technique proposed in chapter-2, which is named as the Discontinuous Decoupled SVPWM (DDPWM-1) technique. The dual-inverter switching power loss, conduction power loss, total dual-inverter loss (i.e. sum of the switching power loss and conduction power loss), THD and WTHD are considered as performance indices. It should be reiterated here that all the four SVPWM techniques achieve the prevention of overcharging of the dc-link capacitor of inverter-2 (the one with lower input voltage) as well as the avoidance of the zero sequence current.

For fairness of comparison, the switching inverter in all the PWM schemes is switched with 42 samples/cycle. To evaluate the conduction loss in the dual-inverter scheme, which depends on the motor load current, a load torque of 20 N-m is applied to the shaft of the OEWIM. This torque is about 80% of the full-load torque of the 3.7 KW motor chosen for analysis (5 HP, i.e. 3.7 KW, 1445 RPM, 50 Hz). The dc-ink voltages of the dual-inverter scheme sum to a total of 564 V, which is the total dc-link voltage needed to apply rated voltage to the motor at the brink of linear modulation (i.e. m_a = 0.866). As mentioned in chapter-2, the currents obtained with the model of the OEWIMD are used to compute the switching and conduction power losses in the semiconductor devices. It should be noted that ripple in the motor current would not only influence the motor ohmic loss, but also the conduction loss in the individual power semiconductor devices, as the motor current is routed through the devices.

All of the aforementioned performance indices are computed by employing an *improvised loss model*, which was proposed in chapter-2 for the loss calculation of the 4-L

OEWIMD. The same model was extended to this work to compute the losses occurred in the 4-L OEWIMD.

The switching power loss is the sum of the turn-on switching power loss and turn-off switching power loss during the turn-on transition and the turn-off transition of the switching device respectively. The expressions for the switching power loss and conduction power loss are given as [3],

$$P_{SW} = \left[\frac{1}{2} v_{SW} i_{SW} (t_{SWON} + t_{SWOFF})\right] \times f_S$$

$$P_{SW} = \left[\frac{1}{2} v_{SW} i_{SW} (t_{ri} + t_{fv}) + \frac{1}{2} v_{SW} i_{SW} (t_{rv} + t_{fi})\right] \times f_s \quad (3.6)$$

$$P_{Con} = \frac{v_{ON}\, i_{ON} t_{ON}}{T_S} \quad (3.7)$$

where, $v_{ON} = V_t + i_{ON} R_{CE}$ for IGBT

$v_{ON} = V_f + i_{ON} R_{AK}$ for the anti-parallel diode

where V_t is the IGBT fixed voltage drop under zero-current condition, R_{CE} is the IGBT on-drop resistance, V_f is the diode fixed voltage drop under zero-current condition and R_{AK} is the diode on-drop resistance. The parameters of the IGBT module-*SKM150GB12T4* are considered for the evaluation of the conduction loss. The following data is assumed to compute the switching and conduction loss in each device: $t_{fv} = 1\ \mu s$, $t_{rv} = 2\ \mu s$, $t_{fi} = 4\ \mu s$, and $t_{ri} = 2\ \mu s$.

Fig. 3.47 presents the sum of the inverter-1 and inverter-2 switching losses incurred with these four versions of SVPWM techniques. It may be noted that, in all the four cases, these losses increase uniformly till the edge of linear modulation, wherefrom all of them decrease uniformly. As the number of samples are fixed at 42/cycle irrespective of the modulation index, the frequency of the fundamental component, which in turn determines the sampling frequency and hence the switching power loss, uniformly increases till the edge of

linear modulation (m_a= 0.866). The fundamental component is clamped to the rated frequency when $m_a \geq 0.866$, this reduces switching and hence the switching power loss.

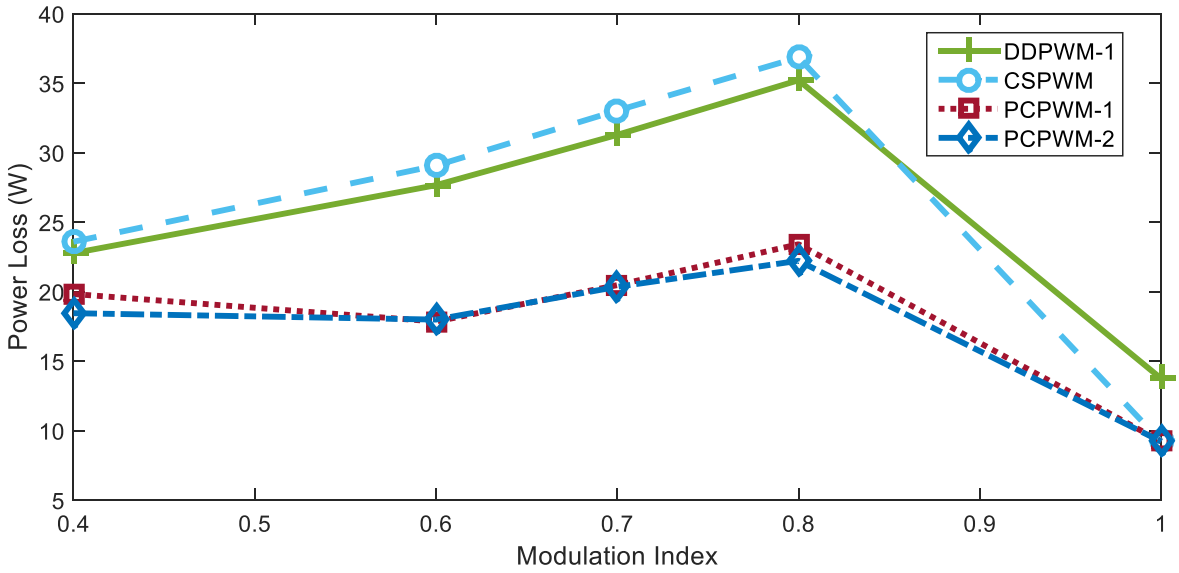


Fig. 3.47: Dual-inverter switching power loss of four-level OEWIMD

It is apparent that the PCPWMs-1 & 2 perform better than the DDPWM-1 technique proposed in chapter-2 in this aspect. This is due to the fact that in the proposed PWM schemes, one of the inverters (inverter-2) of the dual-inverter system is clamped in any given sampling time period and switching inverter (i.e. inverter-1) is also clamped for 120^0. As one may anticipate, amongst these three PWMs, the PCPWMs incur lesser switching loss compared to the CSPWM.

The total conduction loss is the sum of the individual conduction losses of the constituent inverters of the dual-inverter system. Again, the conduction loss incurred in each inverter is the sum of both the switch conduction losses and the diode conduction losses. The total conduction loss with all the four PWM schemes is shown in Fig. 3.48. It may be observed that the conduction loss in the PCPWM schemes is higher compared to the CSPWM scheme, as each phase is clamped for a duration corresponding to 120^0, even in the switching inverter.

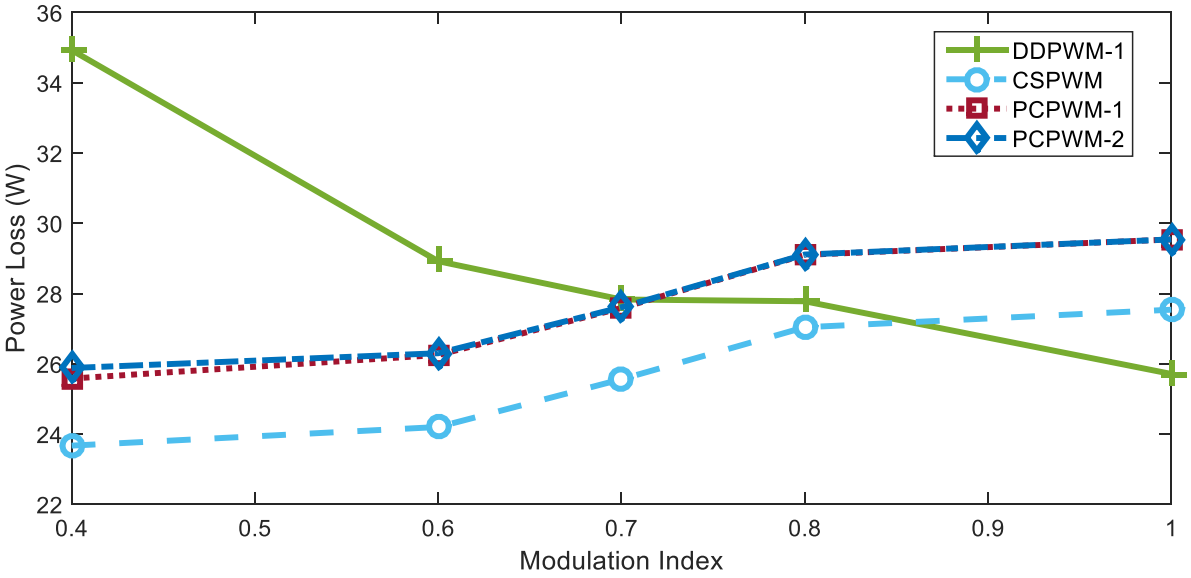


Fig. 3.48: Dual-inverter conduction power loss of four-level OEWIMD

The total inverter loss (i.e. the sum of switching and conduction power loss) for all the PWM schemes is presented in Fig. 3.49. The overall dual-inverter loss are less for PCPWMs as compared to the CSPWM and DDPWM-1.

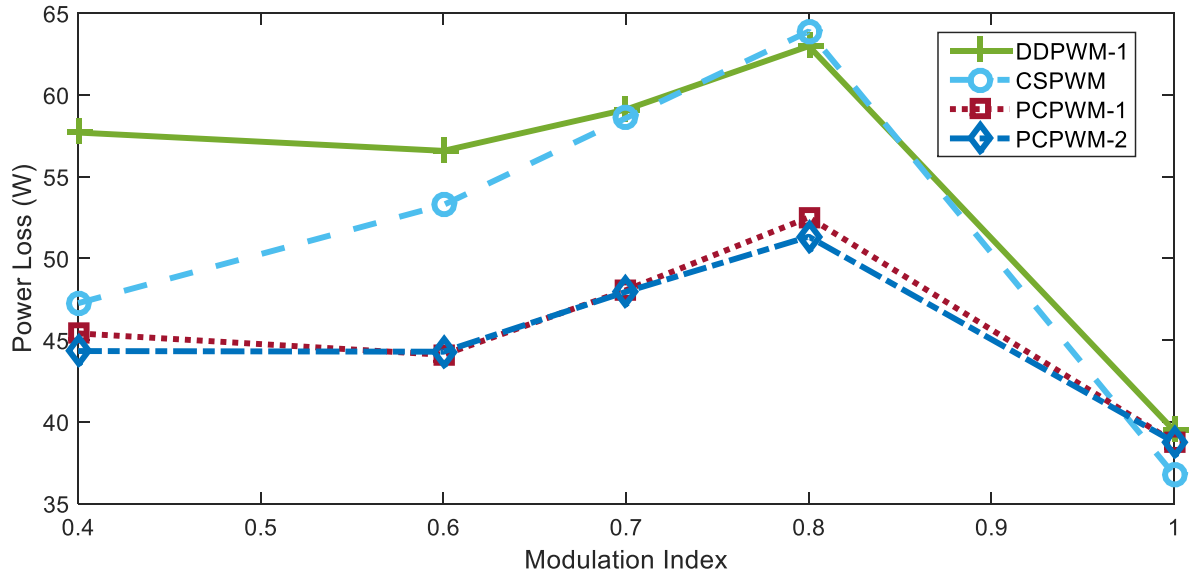


Fig. 3.49: Dual-inverter power loss of four-level OEWIMD

It is interesting to note from Figs. 3.47-3.49 that, amongst the three PWM schemes proposed (CSPWM, PCPWMs-1 & 2), the advantage of reducing the switching frequency outweighs the disadvantage associated with the increase of the conduction loss in the power

semiconductor devices. The simulation results presented in Fig. 3.49 suggest that an energy efficient OEWIMD should employ the PCPWM techniques, rather than the CSPWM scheme.

The THD is a widely used measure to quantify the spectral performance of the inverter. THD in the output of the voltage is defined as:

$$V_{THD} = \frac{\sqrt{\sum_{n=2}^{\infty} v_n^2}}{v_1} \tag{3.8}$$

Where V_1 and V_n are the RMS values of the fundamental component and n^{th} harmonic components of the phase voltage. THD in voltage is a measure of harmonic contamination, which is normalized with respect to the fundamental quantity. The THD in voltage is evaluated for all the four PWM techniques. It may be noted that the PWM techniques proposed in this chapter perform better than the Discontinuous Decoupled SVPWM scheme in the lower range of modulation, while the DDPWM-1 performs marginally better in the middle anf upper range of modulation. As one may anticipate, among the PWM schemes proposed in this chapter, the CSPWM performs slightly better than the PCPWMs as shown in Fig. 3.50.

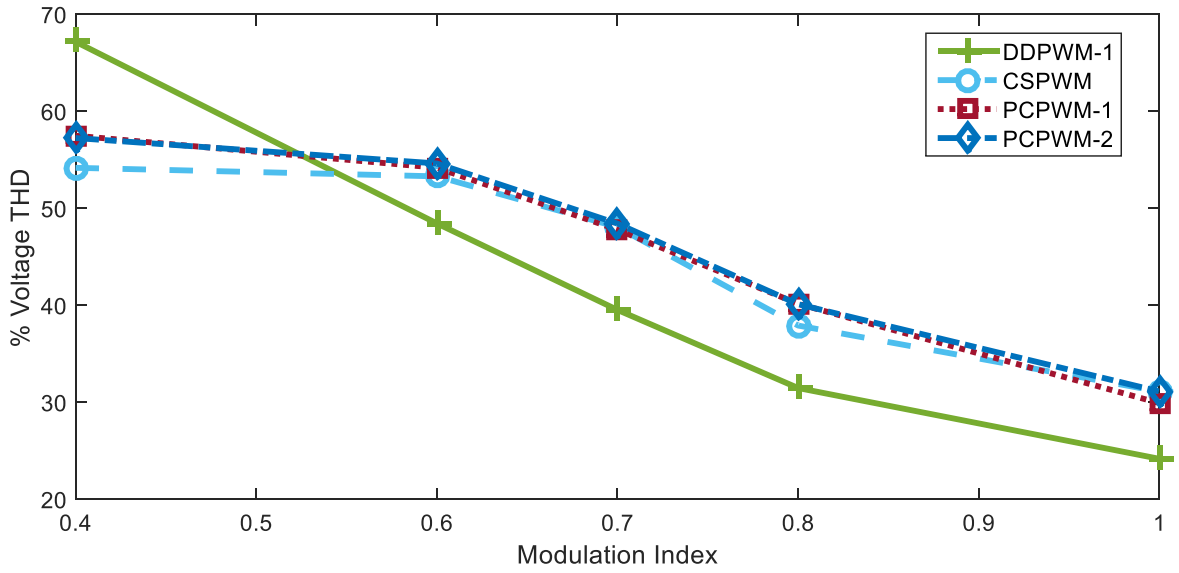


Fig. 3.50: Modulation index vs Phase Voltage THD of four PWM Techniques

The effectiveness of a modulation scheme can also be assessed by the weighted THD. It is generally reckoned that WTHD captures the performance of a PWM scheme in a better way than the THD in voltage. When an induction motor is fed by a sinusoidal voltage source, the motor draws a magnetizing current, which is given by $(V_1/\omega L_m)$. However, when the motor is supplied with a non-sinusoidal input, any harmonic current component of n^{th} order is given by $(V_n/n\omega L_m)$. Thus the quantity $\sum_{n\neq 1}(V_n/n\omega L_m)^2$ represents the RMS value of all harmonic components put together. Thus, the WTHD represents the normalized harmonic contamination in current, with the fundamental component chosen as the base value. The WTHD is defined as:

$$V_{WTHD} \triangleq \frac{\sqrt{\sum_{n=2}^{\infty}\left(\frac{v_n}{n}\right)^2}}{v_1} \tag{3.9}$$

Fig. 3.51 shows that the WTHD of all the four PWM schemes. From Fig. 3.51, the CSPWM scheme performs better in the lower and middle range of modulation, while the DDPWM-1 performs better in the upper range.

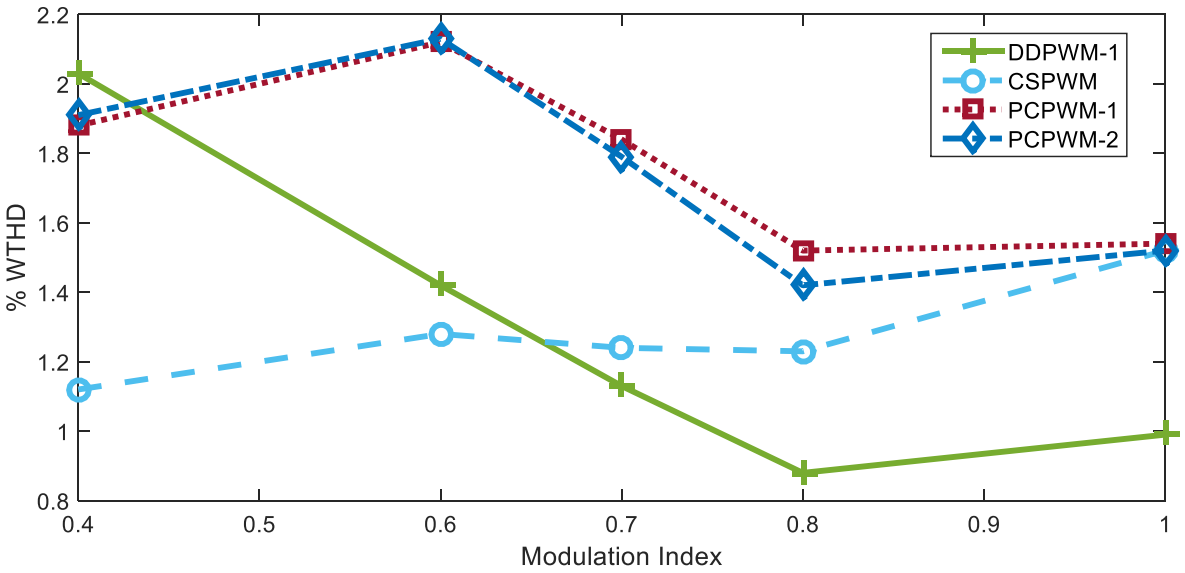


Fig. 3.51: Modulation Index vs WTHD of four PWM Techniques

From Fig. 3.47-3.51, it is apparent that SVPWM techniques proposed in this chapter perform better than the DDPWM-1 in terms of switching power loss and toal dual-inverter loss. The simulated motor phase voltage waveforms are shown in Fig. 3.52, of which the

central part is zoomed. The proposed PWM techniques in this chapter result considerably lesser dv/dt across the motor windings as is evident in Fig. 3.14 (CSPWM), Fig. 3.32 (PCPWM-1) and the Fig. 3.44 (PCPWM-2) and achievs all of the wavefrom symmetries.

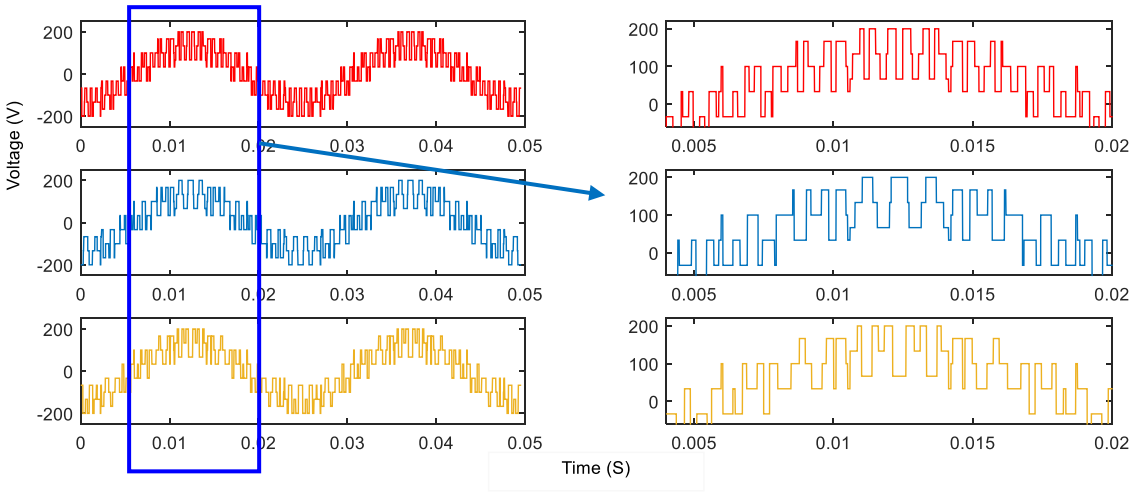


Fig. 3.52: Phase voltage waveforms with waveform symmetries CSPWM (top), PCPWM-1 (middle) and PCPWM-2 (bottom)

3.5 Conclusion

This chapter suggests three variants of a simple SVPWM scheme to improvise the performance of a four-level OEWIMD, which is obtained by feeding an open-end winding induction motor with two two-level inverters from either side. The constituent inverters are operated with unequal dc-link voltages, which are in the ratio of 2:1. The performance of the OEWIMD employing these PWM techniques is compared with the DDPWM-1 technique reported in the chapter-2. The common objective of all these four PWM strategies is to avoid the overcharging of the dc-link capacitor of the inverter operating with lower input voltage.

Using both simulation studies and experimentation, it is shown that the proposed SVPWM strategies perform better compared to the DDPWM-1 strategy to an appreciable extent in terms of power loss. The proposed PWM techniques result in lower losses in the switching devices, lower overall loss of the dual-inverter system, throughout the range of modulation. Also, with the proposed PWM techniques, the motor phase windings experience considerably lower dv⁄dt across them. This results in the longevity of the life of insulation and lower bearing currents, which increases the life of bearings.

Chapter 4

A Four-Level Open-End Winding Induction Motor Drive with a Nested Rectifier-Inverter Combination with Two DC Power Supplies

Contents

4.1 Introduction

The four-level OEWIMD, realized by feeding an OEWIM with two 2-level conventional VSIs with unequal dc-link voltages, which are in the ratio of 2:1 is reproduced in Fig. 4.1 [65]. The main difficulty associated with this power circuit is that, for some of the space vector switching combinations, the lower dc-link voltage capacitor is overcharged by its counterpart (i.e. higher dc-link voltage capacitor). The undesirable effects of such an overcharging phenomenon are well documented in [65].

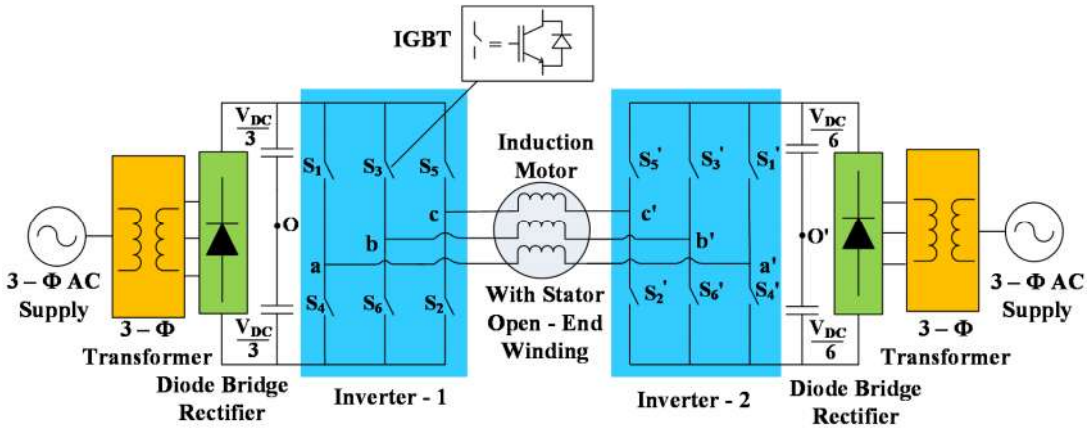


Fig. 4.1: Four-level OEWIM with isolated dc-power supplies

To avoid the overcharging of the lower voltage dc-link capacitor, a circuit topology was proposed in [66], which embeds a rectifier-inverter combination operating with a lower dc-link voltage in an outer combination of similar construction operating with a higher dc-link voltage. This topology uses the Decoupled Sample Averaged Zero-sequence Elimination (DSAZE) Space Vector Pulse Width Modulation (SVPWM) [66] and the Sample Averaged Zero-sequence Elimination (SAZE) SVPWM techniques [67], to avoid the ZSVs. However, this power circuit configuration uses three isolation transformers and three diode bridge rectifiers.

In this chapter, a modified nested rectifier-inverter topology is proposed for the four-level OEWIMD, in which one side of the OEWIM is fed with a 2-L VSI and the other end is fed with a nested rectifier-inverter combination. The proposed topology uses only two isolation transformers, to avoid the overcharging phenomenon of the lower dc-link voltage capacitor. The dc-link utilization in this power circuit is on par to the one proposed in [66], as

the sum of the individual dc-link voltages of the constituent inverters is equal to 0.77 V_{DC} (i.e. a decrease of around 23%). The zero-sequence voltages are eliminated by employing (a) the DSAZE SVPWM technique [66], and (b) a modified version of the SAZE SVPWM technique [67]. The performance indices considered for the comparative evaluation are: conduction power loss, switching power loss, and the total power loss in the dual-inverter system.

4.2 New Nested Rectifier-Inverter Configuration for four-level OEWIMD

4.2.1 Description of topology

The proposed circuit topology for the four-level (4-L) Open-End Winding Induction Motor Drive (OEWIMD) is shown in Fig. 4.2. The proposed configuration consists of two isolation transformers, which maintain the rectified dc-link voltages are in the ratio of 2:1. Two conventional 2-level VSIs (VSI-1 and VSI-2) are used in the proposed topology, wherein VSI-1 feeds one side of the OEWIMD, while VSI-2 feeds the other side and is nested within VSI-1. The individual space vectors corresponding to the VSIs-1 and 2 (Fig. 4.2) are shown in Fig. 4.3. The resultant space vector diagram of the dual-inverter configuration consists of 64 (8×8) space vector combinations, spread over 37 locations with 54 sectors as shown in Fig. 4.4.

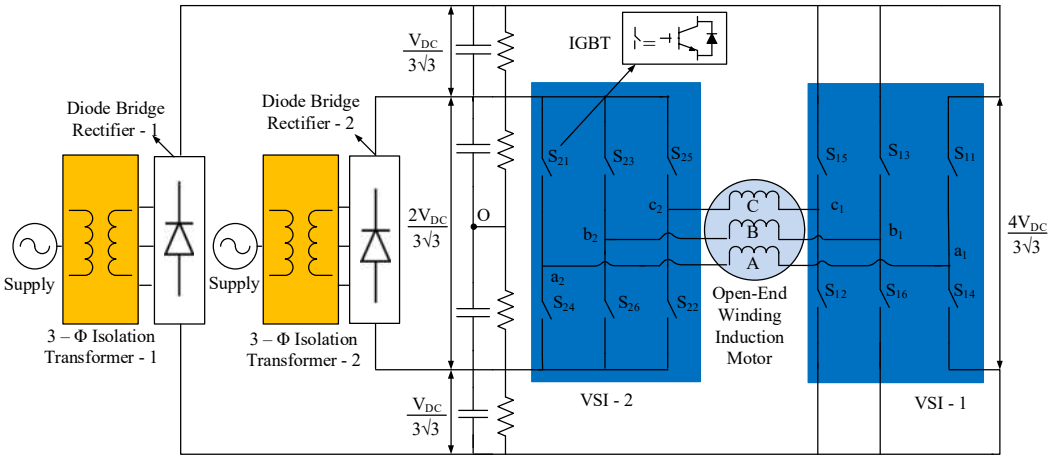


Fig. 4.2: Proposed topology for 4-L OEWIMD

The pole voltage of VSI-1 (v_{a_1o}) is switched between the $2V_{DC}/3\sqrt{3}$,

and $-2V_{DC}/3\sqrt{3}$. Similarly, the pole voltage of VSI-2 (v_{a_2o}) is switched between $V_{DC}/3\sqrt{3}$ and $-V_{DC}/3\sqrt{3}$. Thus, the resultant voltage applied across the system (Fig. 4.2) displays four-levels in the dual-inverter (motor phases). The different voltage levels of phase-A $(v_{a_1a_2})$ are listed in Table 4.1.

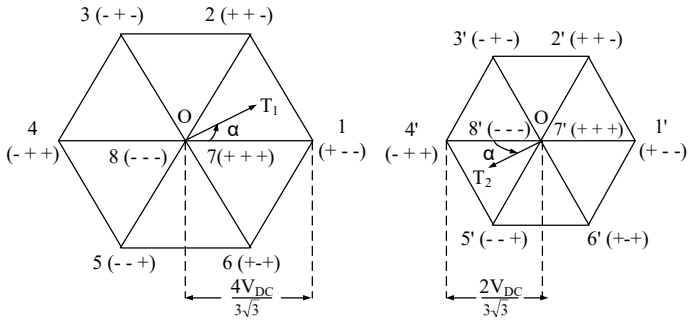


Fig. 4.3: Individual space vector locations of VSIs-1 (left) and 2 (right) (not drawn to scale)

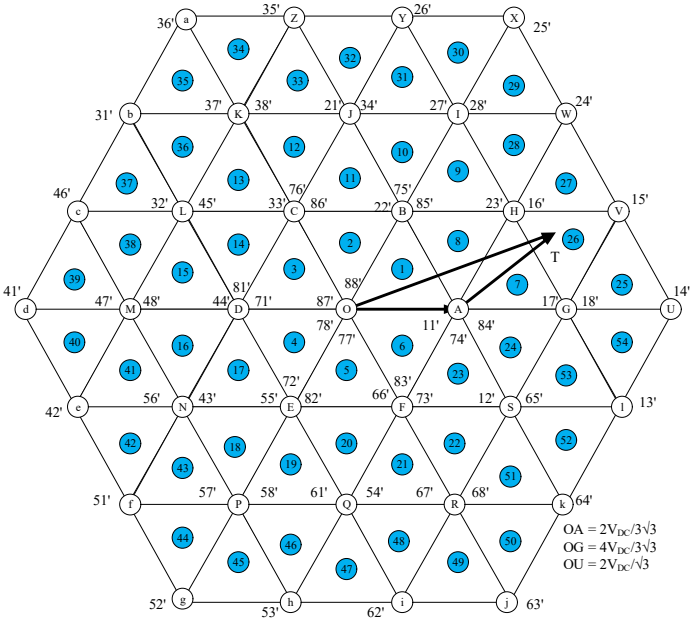


Fig. 4.4: Resultant space vector diagram of proposed 4-L OEWIMD

Table 4.1: Four Levels in the phase voltage of proposed topology

$\mathbf{v_{a_1o}}$	$\mathbf{v_{a_2o}}$	$\mathbf{v_{a_1a_2} = v_{a_1o} - v_{a_2o}}$
$\mathbf{-2V_{DC}/3\sqrt{3}}$	$V_{DC}/3\sqrt{3}$	$-V_{DC}/\sqrt{3}$
$\mathbf{-2V_{DC}/3\sqrt{3}}$	$-V_{DC}/3\sqrt{3}$	$-V_{DC}/3\sqrt{3}$
$\mathbf{2V_{DC}/3\sqrt{3}}$	$V_{DC}/3\sqrt{3}$	$V_{DC}/3\sqrt{3}$
$\mathbf{2V_{DC}/3\sqrt{3}}$	$-V_{DC}/3\sqrt{3}$	$V_{DC}/\sqrt{3}$

Table 4.1 clearly demonstrates that the *open-end winding* topology is capable of rendering four-level inversion, if the dc-link voltages of the individual inverters are maintained in the ratio of 2:1.

4.2.2 Avoidance of lower dc-link voltage capacitor overcharging

As explained in [65], for the circuit configuration shown in Fig. 4.1, for the switching combinations $11'$, $22'$, $33'$, $44'$, $55'$, $66'$, $12'$, $16'$, $23'$, $34'$, $45'$ and $56'$ (see Fig. 4.4) overcharge the lower dc-link voltage capacitor by its counterpart.

The present topology avoids such an undesirable overcharging, while preventing the flow of the zero-sequence current. For the switching combinations $11'$ and $12'$, the avoidance of such an overcharging is explained in the following paragraphs:

For the switching combination $11'$, the VSI-1 assumes the state 1 (+ - -), while the VSI-2 assumes the state $1'$ (+ - -). Consequently, the IGBTs S_{11}, S_{16} and S_{12} are turned ON for the VSI-1, while the IGBTs S_{21}, S_{26} and S_{22} are turned ON for the VSI-2. Fig. 4.5 (left) refers to the equivalent circuit of the proposed topology (see Fig. 4.2) for the switching combination $11'$. While, the phase-A winding of the OEWIM is directly connected across the positive rails of the isolated power supplies, whereas the phase-B and C windings of the OEWIM are connected across the negative rails of the isolated power supplies. A similar situation prevails for the combinations $33'$ and $55'$, wherein, one of the motor winding either B or C is directly connected across the positive rails of the isolated power supplies. For the combinations $22'$, $44'$ and $66'$, two motor windings are connected between the positive rails of the isolated power supplies. In all of these circuit situations, the capacitor dc-link voltage of VSI-1 is not connected to the counterpart capacitors of VSI-2. From this it can be concluded that the capacitor voltages are balanced and are maintained in the ratio of 2:1.

For the switching combination $12'$, the equivalent circuit of the present topology is depicted in Fig. 4.5 (right). It may be readily observed that, the dc-link capacitors of VSI-2 are not connected to its high-voltage counterpart in this circuit situation also. The vector

combination $16'$ also results in a similar circuit situation, wherein the motor windings B, C reverse their roles.

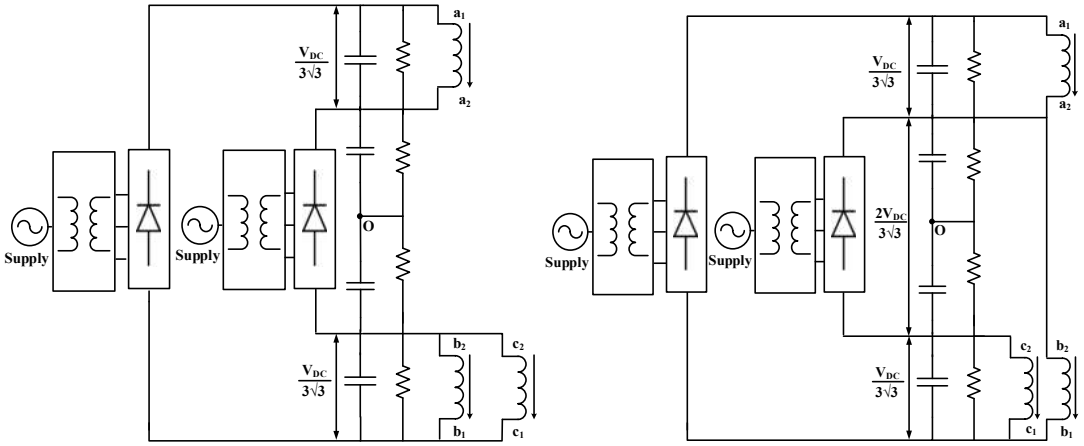


Fig. 4.5: OEWIM winding connections for the switching combination $11'$ (left), $12'$ (right)

It can be therefore be conclude that, the overcharging of the lower dc-link voltage capacitors by their higher dc-link voltage counterparts is avoided in the proposed topology, as is evident from the Fig. 4.5 and similar explanation can be applicable to the other switching combinations.

The concept of balancing the capacitor voltages in the proposed topology for two-level and four-level operation is explained in the equivalent circuits presented in Fig. 4.6. The capacitor balancing for two-level operation is depicted in Fig. 4.6 (a). The two-level operation is obtained by employing the voltage vector combinations: $88' - 11' - 22' - 77'$, i.e. sector OAB belonging to the core-hexagon ABCDEF (Fig. 4.4). Similarly, Fig. 4.6 (b) depicts the capacitor balancing for the four-level operation, wherein the voltage vector combinations $84' - 14' - 24' - 74'$ (i.e. sector AUW in Fig. 4.4) are selected.

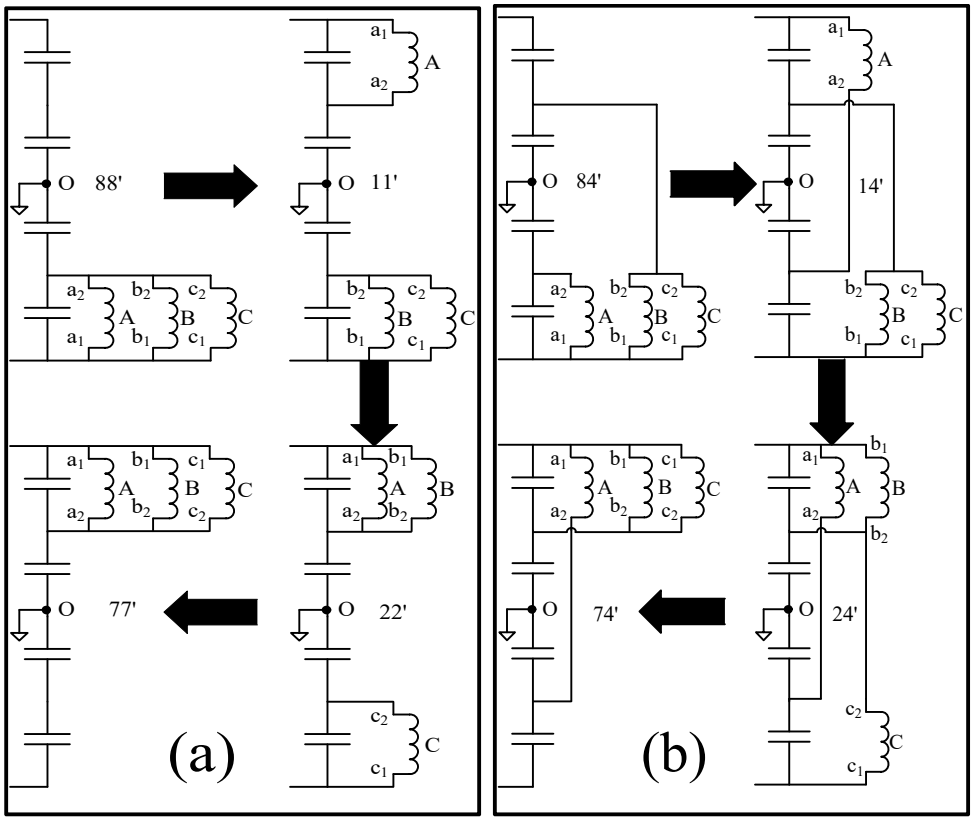


Fig. 4.6: OEWIM phase connections during mode-by-mode transition: (a) two-level operation (b) four-level operation

4.2.3 Comparison with other 4-L multilevel inverter topologies

The comparison between the proposed topology and previously reported 4-L multilevel inverter topologies for induction motor drives is shown in Table 4.2. It is generally known that any Multilevel Inverter (MLI), irrespective of its topology needs an isolation transformer for high power - high voltage applications [102-105]. Also, the power rating of the transformer corresponds to that of the MLI. Thus, the sum of individual ratings of the constituent transformers would practically remain the same across the circuit topologies. From this discussion, it is evident that even though the operation of this circuit is identical to the one proposed in [66], the number of dc-power supplies are reduced from 3 to 2 in the proposed circuit. The number of IGBTs used in the proposed topology and recently proposed topology [66] are 12, where as in the NPC, FC MLI topologies, and the count is 18. The number of isolation transformers used in the present topology are two, while the required isolation transformers are 3 in the power circuit proposed in [66]. The total device count in the proposed topology is 26, where as in the [66], NPC and FC MLIs, the count is 33, 37 and 37 respectively. As the overall device count of the proposed topology is less as compared to

other, then the reliability of the proposed topology is increased and it does not require fast recovery clamping diodes and floating capacitors of large ratings as compared to NPC, FC MLIs.

Table 4.2: Comparison between 4-L MLI topologies

Component	Voltage Rating	4-L MLIs			
		NPC	FC	*Ref [66]	*Proposed Topology
IGBT	$2V_{DC}/3$	0	0	6	6
	$V_{DC}/3$	18	18	6	6
Clamping diodes	$V_{DC}/3$	12	0	0	0
Diodes in Bridge Rectifier	V_{DC}	6	6	0	0
	$2V_{DC}/3$	0	0	6	6
	$V_{DC}/3$	0	0	0	6
	$V_{DC}/6$	0	0	12	0
Floating capacitors	$2V_{DC}/3$	0	12	0	0
Uncontrolled DC Sources	$2V_{DC}/3$	0	0	1	1
	$V_{DC}/3$	1	1	0	1
	$V_{DC}/6$	0	0	2	0
Total		37	37	33	26

* The required total dc-link voltage is $0.77*V_{DC}$

4.3 SVPWM Techniques For The Elimination Of Zero-Sequence Voltages

The Open-End Winding Induction Motor Drive (OEWIMD) configuration shown in Fig. 4.1, mainly suffers from two problems: 1) overcharging of the lower dc-link voltage capacitor by its counterpart and 2) the presence of the Zero-Sequence Voltages (ZSV) across the motor phase windings.

The present topology avoids the problem of overcharging as explained in the section 4.2. To eliminate the ZSVs, the SVPWM techniques called Sample Averaged Zero-sequence Elimination (SAZE) and Decoupled SAZE (DSAZE) proposed for the three-level OEWIMD in [106] are extended to the topology presented in [66]. The proposed SVPWM techniques do not require any look up table and sector identification, and are implemented by using the instantaneous phase reference voltages. The proposed topology uses these two SVPWM

techniques to eliminate the ZSV of the 4-L OEWIMD [66-67].

The SVPWM techniques are explained by assuming that the reference voltage vector (v_{sr}) ***OT***, is located in sector 26 (see Fig. 4.4). The vector ***OU*** represents the total dc-link voltage required by the dual-inverter system. These two vectors are related by the modulation index (m_a) and is defined as,

$$m_a = \frac{|v_{sr}|}{2V_{DC}/\sqrt{3}} \tag{4.1}$$

The motor is operated with the open-loop v/f control. At the edge of the linear modulation$(i.e. m_a = \sqrt{3}/2)$ the rated fundamental voltage and the frequency component (f) of the OEWIMD are 400 V (line-line, RMS) and 50 Hz respectively. The frequency of the fundamental component corresponding to m_a is given in eq. 4.1 as,

$$f_1 = \frac{f \times m_a}{\sqrt{3}/2} \tag{4.2}$$

The vector ***OT*** of the dual-inverter system is synthesized with N_S = 66 samples/cycle irrespective of the fundamental frequency and the sampling time of the dual-inverter system is given as,

$$T_S = 1/(f_1 \times N_S) \tag{4.3}$$

In the DSAZE PWM scheme, the reference vector ***OT*** is decomposed into two anti-phased components, which are in the ratio of the respective dc-link voltages of the individual inverters (i.e. 2:1). Both of these components are then synthesized independently using the principles of space vector modulation. While the DSAZE PWM scheme modulates each VSI individually, the SAZE PWM scheme views the entire dual-inverter scheme as a single entity. In the SAZE scheme, the reference vector ***OT*** is resolved into two components ***OA*** and ***AT*** (Fig. 4.4). The vectors ***OA*** and ***AT*** are named as clamping and switching vectors respectively.

The switching vector is switched around the Nearest Sub-Hexagonal Center (NSHC) of the clamped vector [106] and [107]. The PWM scheme presented in [107] avoids of the over-charging of the lower dc-link capacitor, while the PWM suggested in [106] manages to suppress the zero-sequence current through the motor phase windings by the dynamic balancing of the zero-sequence current. In this chapter, these two PWM strategies are combined. Since the dc-link capacitor of the nested inverter has the tendency to get overcharged, it is clamped emulating the PWM scheme proposed in [107]. Thus, this PWM technique is named as *Nested Inverter Clamped Sample Averaged Zero-Sequence Elimination (NICSAZE)*. The detailed principle operation of both of these PWM techniques is explained in the following sub-sections.

4.3.1 DSAZE PWM Technique

As said above, the reference voltage vector ***OT*** is resolved into two components ***OT₁*** and ***OT₂*** in the ratio of 2:1 is shown in Fig. 4.3, which are anti-phased (see Fig. 4.3). The switching algorithm presented in [98] for the two-level VSI is extended to the dual-inverter system of the present topology. The imaginary switching time periods [98] for VSI-1 is given as,

$$T_{xs_1} = \frac{T_s}{4V_{DC}/3\sqrt{3}} \frac{2v_{xs}}{3} \quad x \in a, b, c \tag{4.4}$$

The effective time period for VSI-1, where the power transfer from input DC side to the output AC side of the inverter is given as,

$$T_{eff_1} = T_{max_1} - T_{min_1} \tag{4.5}$$

where $T_{max_1} = max(T_{xs_1})$, $\mathrm{T_{min_1}} = \min(\mathrm{T_{xs_1}})\ \mathrm{x} \in \mathrm{a, b, c}$

The time period there is no power flow from the input DC side to the output AC side of the inverter. This time interval is called as the zero-vector (or the null-vector) time period and is denoted as T_z. The null-vector time periods for the VSI-1 is given by,

$$T_{z_1} = T_s - T_{eff_1} \tag{4.6}$$

The offset time needed for the center spacing of the effective time period within the sampling time interval of $\boldsymbol{T_s}$ for the VSI-1 given as,

$$T_{offset_1} = T_{z_1}/2 - T_{min_1} \tag{4.7}$$

It is shown in [98] that the phase switching time periods T_{gx_1} for VSI-1 are related to imaginary switching time periods T_{xs_1}, by a simple expression,

$$T_{gx_1} = T_{xs_1} + T_{offset_1}\, x \in a, b, c \tag{4.8}$$

It is shown in [65] that, the phase switching time periods of the VSI-2 is simply obtained as,

$$T_{gx_2} = T_s - T_{gx_1} \tag{4.9}$$

It is also proven in [65] that the offset time needed to eliminate the ZSVs in DSAZE PWM technique, is given as,

$$T_{offset} = Ts/2 \tag{4.10}$$

By using eqs. 4.2 and 4.3, the sampling time period T_s can be rewritten in terms of modulation index and number of samples as,

$$T_s = \frac{\sqrt{3}}{2(f \times m_a \times N_S)} \tag{4.11}$$

Now, by using eq. 4.11, the eq. 4.10 can be rewritten as,

$$T_{offset} = \frac{\sqrt{3}}{4(f \times m_a \times N_S)} \tag{4.12}$$

4.3.2 NICSAZE SVPWM Strategy

The NICSAZE SVPWM technique, proposed for the present topology is explained with help of the Fig. 4.7. The resultant space vector diagram of the dual-inverter system, shown in Fig. 4.7, is divided into six regions, which are centered around the Space Vector Locations (SVLs) A, B, C, D, E and F. A typical hexagon centered on the sub-hexagonal center 'A' (the hexagon UWJDQk) is also shown in Fig. 4.7, with a hatched boundary.

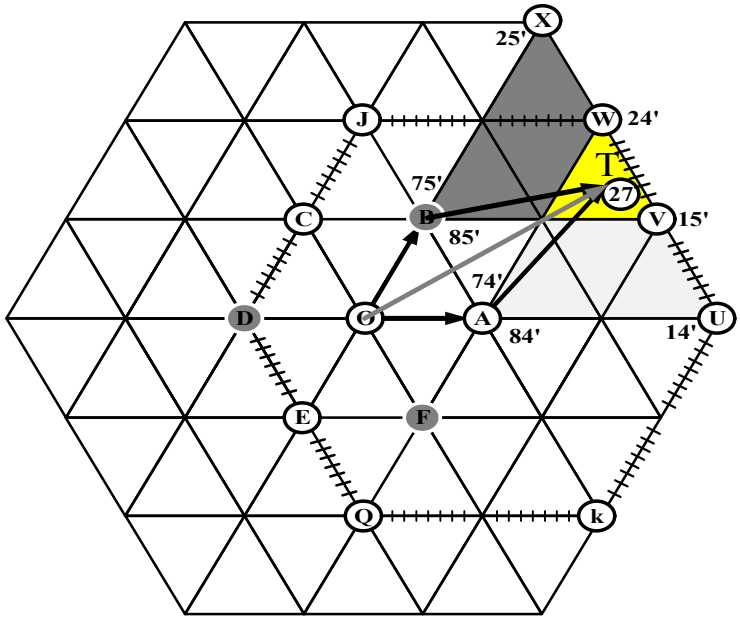


Fig. 4.7: Principle operation of NICSAZE SVPWM technique

Let it be assumed that the reference vector for the dual-inverter system is located in sector 27 (vector ***OT*** in Fig. 4.7). It is intended to realize this vector with the help of the component sets: either $\{OA, AT\}$ or $\{OB, BT\}$. The space vectors available at A, U and W are utilized to realize the vector $\overline{AT}$ in the average sense. Similarly, the vectors available at the locations B, V and X can be used to synthesize the vector $\overline{BT}$. Thus, by using the vectors $\overline{OA}$ and $\overline{OB}$ as biasing vectors and the vectors $\overline{AT}$ and $\overline{BT}$ as switching vectors, one may construct the overall reference vector $\overline{OT}$ using the method of space vector modulation.

Vectors such as $\overline{OA}, \overline{OB}, \overline{OC}$ etc. are applied to the dual-inverter system with VSI-2 and remain clamped throughout a given sample time period. On the other hand, VSI-1 act as the switching inverter and produces the switching vectors such as $\overline{AT}, \overline{BT}, \overline{CT}$ etc. (Fig. 4.4).

For the switching inverter (i.e. VSI-1), the space vector switching locations are switched respectively for the time periods T_z, T_1 and T_2, which sum up to the sampling time period T_s.

To avoid the common mode voltages on average sense, the null vector switching time period (T_z) is divided in the ratio of $(1-x)T_z$ and xT_z [98] to strategically place the effective time period (T_1+T_2) in T_s. Let it be assumed that $\overline{OA}$ and $\overline{AT}$ are the clamping and switching vectors respectively. The vector $\overline{OA}$ is applied to the dual-inverter system by clamping VSI-2 to the state of $4'(-++)$ (see Fig. 4.4). The switching vector $\overline{AT}$ is applied to the dual-inverter system with VSI-1 (i.e. the switching inverter), by switching through the state 8-1-2-7. Thus, the space vector combination deployed by the dual-inverter system to the OEWIM are $84'$- $14'$- $24'$ - $74'$ (see Fig. 4.7).

In the proposed SVPWM technique (NICSAZE) the time durations for these switching combinations are given by $(1-x)T_z, T_1, T_2$ and xT_z, respectively. From [65], the Zero-Sequence voltages for these combinations are calculated as $-14V_{DC}/18\sqrt{3}$, $-6V_{DC}/18\sqrt{3}$, $2\,V_{DC}/18\sqrt{3}$ and $10V_{DC}/18\sqrt{3}$. It stands to reason that, if one intends to suppress the Zero-Sequence Current (ZSC), the Zero-Sequence Voltage (ZSV) must be suppressed (as the ZSV causes ZSC). Generally speaking, it is the best proposition to suppress the zero-sequence voltage on an instantaneous basis. However, in the proposed topology, this won't be possible because all of the available 64 switching vector combinations possess a non-zero value of zero-sequence voltage. Thus, the only alternative is to suppress the ZSV in the average sense over a period of the time (the smaller the time period, the better). With the proposed NICSAZE PWM scheme, it is intended to suppress the ZSV to an average value of zero in *every sampling time period*.

The sampled average zero-sequence voltage is forced to zero over the time period T_s, in the region centered on the SVL 'A' and the corresponding offset time period T_{offset} can be calculated as follows:

Let the sampled average zero-sequence voltage $\left(V_{zs,Samp\ avg.}\right)$ is zero, i.e.

$$V_{zs,Samp\ avg.} = 0 \tag{4.13}$$

The value of $V_{zs,Samp\ avg}$ over a time T_s, in terms of ZSVs and their respective dwell-times is given in eq. 4.13 as,

$$V_{zs,Samp\ avg.} = \frac{1}{T_S}\left[\left(-\frac{14V_{DC}}{18\sqrt{3}}\right)(1-x)T_z + \left(-\frac{6V_{DC}}{18\sqrt{3}}\right)T_2 + \left(\frac{2V_{DC}}{18\sqrt{3}}\right)T_1 + \left(\frac{10V_{DC}}{18\sqrt{3}}\right)(xT_z)\right] = 0 \tag{4.14}$$

After simplifying the eq. 4.14 one obtains: $2T_1 - 6T_2 - 14T_z + 24xT_z = 0$

$$\text{i.e. } xT_z = \frac{T_1}{12} - \frac{T_2}{4} - \frac{7T_z}{12} \tag{4.15}$$

From eq. 4.7, the offset time period corresponding to the SVLs ‘A’, ‘C’ and ‘E’ is denoted as $T_{offset-A,C,E}$. Thus,

$$T_{offset-A,C,E} = (1-x)T_z - T_{min} = T_z - xT_z - T_{min} \tag{4.16}$$

By using eqs. 4.15 and 4.16, the simplified form of $T_{offset-A,C,E}$ is given as,

$$T_{offset-A,C,E} = T_z - \left[\frac{T_1}{12} - \frac{T_2}{4} - \frac{7Tz_z}{12}\right] - T_{min}$$

$$T_{offset-A,C,E} = \frac{T_1 - 3T_2 + 10T_z - 12T_{min}}{12} \tag{4.17}$$

From [98], the dwell time periods can be rewritten as,

$$\left.\begin{array}{c} T_1 = T_{max} - T_{mid} \\ T_2 = T_{mid} - T_{min} \\ T_{eff} = T_{max} - T_{min} \\ T_z = T_s - T_{eff} \text{ and} \\ T_{max} + T_{mid} + T_{min} = 0 \end{array}\right\} \quad (4.18)$$

By substituting the eq. 4.18 in eq. 4.17, the modified eq. for the $T_{offset-A,C,E}$ is given as,

$$T_{offset-A,C,E} = \frac{(T_{max} - T_{mid}) - 3(T_{mid} - T_{min}) + 10T_z - 12T_{min}}{12}$$

$$T_{offset-A,C,E} = \frac{5(T_{max} - T_{min} + T_z)}{12} \quad (4.19)$$

Using eq. 4.18 in eq. 4.19 can be rewritten as,

$$T_{offset-A,C,E} = \frac{5T_S}{12} \quad (4.20)$$

Now, by using eq. 4.11, the eq. 4.20 can be modified as,

$$T_{offset} = \frac{5\sqrt{3}}{24\,(f \times m_a \times N_S)} \quad (4.21)$$

Thus, by simply affecting the offset time period given by eq. 4.21 in terms of modulation index and number of samples, one would succeed in forcing the average value of the zero-sequence voltage over a sampling time period to zero in the region centered on SVL 'A'. It can be proved that for the alternating SVLs 'C', 'F' would also have the same T_{offset}.

Let it be considered that the sample to be synthesized is located in sector-27 is with space vector switching locations B, V and X, which is centered on SVL 'B'. The associated switching vector combinations (see Fig. 4.7) $85'$, $15'$, $25'$ and $75'$ are to be switched for the

time periods $(1-x)T_z, T_1, T_2$ and xT_z respectively to implement the NICSAZE PWM technique, to suppress the zero-sequence voltages. Adopting the above procedure, the T_{offset} needed for the SVLs 'B', 'D' and 'F' is given by,

$$T_{offset-B,D,F} = \frac{7T_S}{12} \tag{4.22}$$

Now, by using eq. 4.11, eq. 4.22 can be rewritten in terms of modulation index and number of samples as,

$$T_{offset-B,D,F} = \frac{7\sqrt{3}}{24\,(f \times m_a \times N_S)} \tag{4.23}$$

4.4 Simulation and Experimental Results

To test and validate the proposed topology, initially the simulation results are carried out using *Matlab/Simulink* software and the parameters used for modeling of the OEWIM are given in Table 4.3. The experimental results are carried out on a 3-phase, 50 Hz OEWIM using open-loop v/f control with 66 samples/cycle irrespective of the modulation index.. The name plate details of the motor are shown in Table 4.4. The voltage source inverters VSI-1 and VSI-2 (Fig. 4.2) are operated with dc-link voltages of 200 V and 100 V respectively (in the ratio of 2:1). Therefore, resultant dual-inverter configuration will have an equivalent dc-link voltage of 300 V (i.e. the magnitude of ***OU*** in Fig. 4.4).

Table 4.3: Motor parameters for computer simulation

Dual-inverter dc-link voltage	300 V
Induction motor	Squirrel cage type, 3-Φ, 50 Hz, 400 V
Stator resistance	4.215 Ω
Rotor resistance (referred to stator)	4.185 Ω
Stator leakage inductance	17.52 mH
Rotor leakage inductance (referred to stator)	17.52 mH
Magnetizing inductance	516.6 mH
Moment of inertia	0.0131Kg m^2
Damping coefficient	0.002985 N/rad/s

Table 4.4: Parameters of the OEWIMD

Motor rating	Voltage (Line-Line)	400 V
	Rotor speed	1445 RPM
	Power	3.7 KW
	No. of poles	4

4.4.1 Simulation Results

Simulation results are presented for the modulation indices of 0.7 (from eq. 4.1, the fundamental frequency (f_1) is 40.41 Hz) and over-modulation (f_1 = 50 Hz) to cover the entire speed range of the drive. Over-modulation corresponds to the case, wherein the magnitude of the reference vector $|\boldsymbol{OT}| \geq |\boldsymbol{OU}|$ (Fig. 4.4), where $|\boldsymbol{OU}|$ represents the effective dc-link voltage of the dual-inverter system.

Fig. 4.8 shows the simulated waveforms of the phase voltage, current and their FFT analysis, for a modulation index of 0.7, with *Center-Spaced SVPWM*. From the phase current and FFT analysis of both voltage and the current, it can be observed that the motor phase current shows the presence of zero-sequence currents (as the motor phase voltage itself contains the zero-sequence component).

Figs. 4.9 and 4.10 show the motor phase voltage $(v_{a_1a_2})$, phase current (i_a) and the spectra corresponding to them, while operating drive system using the DSAZE PWM technique. Figs. 4.11 and 4.12 show similar results with the proposed NICSAZE PWM technique. The simulation results reveal that, the currents are sinusoidal despite the presence of some of the harmonic components of the triplen family (i.e. the zero-sequence component).

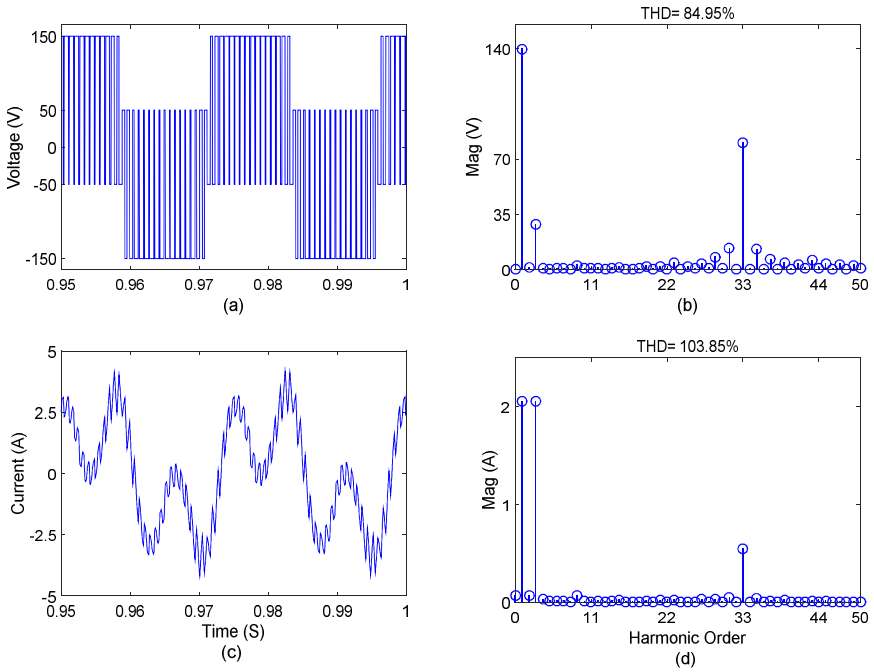


Fig. 4.8: Simulation results for center spaced SVPWM technique at $m_a = 0.7$: (a) $v_{a_1a_2}$ (b) $v_{a_1a_2}$ FFT analysis (c) i_a and (d) i_a FFT analysis

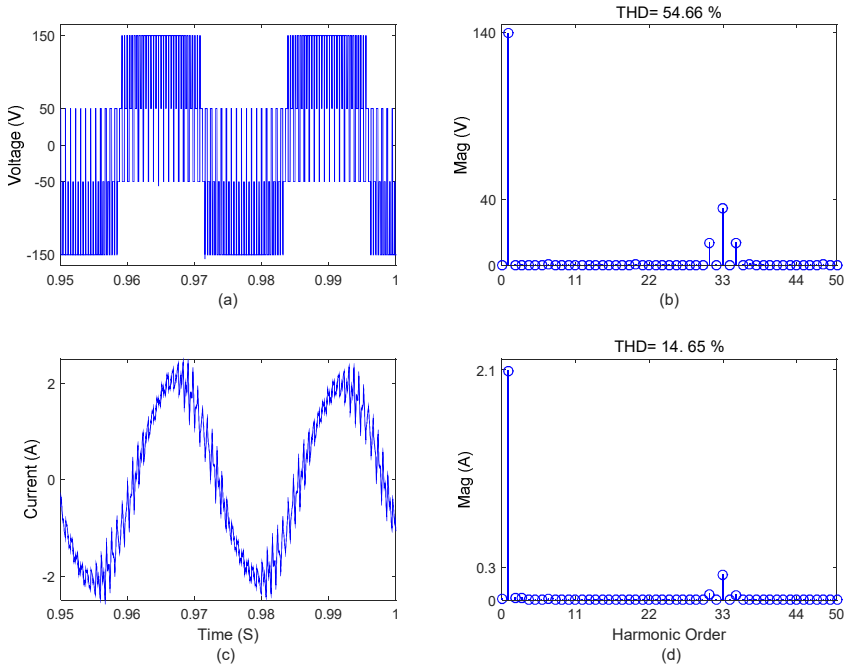


Fig. 4.9: Simulation results for DSAZE PWM technique at $m_a = 0.7$: (a) $v_{a_1a_2}$(b) $v_{a_1a_2}$ FFT analysis (c) i_a and (d) i_a FFT analysis

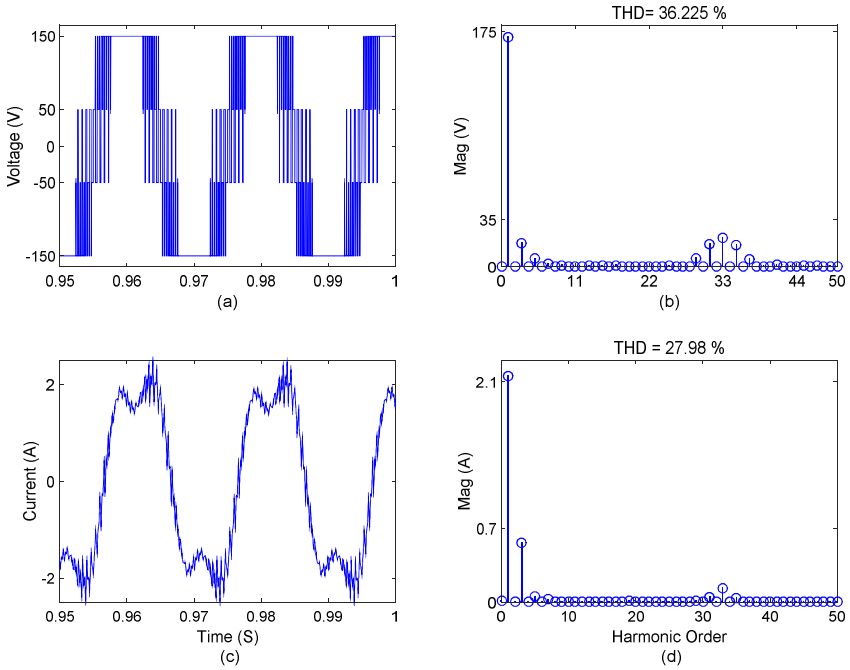


Fig. 4.10: Simulation results for DSAZE PWM technique at m_a = 1: (a) $v_{a_1a_2}$ (b) $v_{a_1a_2}$ FFT analysis (c) i_a and (d) i_a FFT analysis

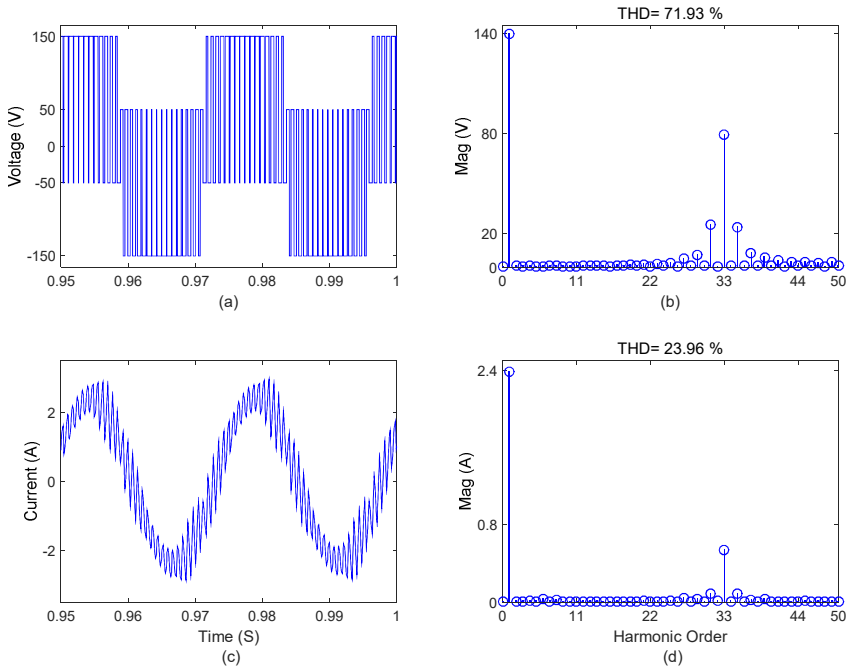


Fig. 4.11: Simulation results for NICSAZE PWM technique at m_a = 0.7: (a) $v_{a_1a_2}$ (b) $v_{a_1a_2}$ FFT analysis (c) i_a and (d) i_a FFT analysis

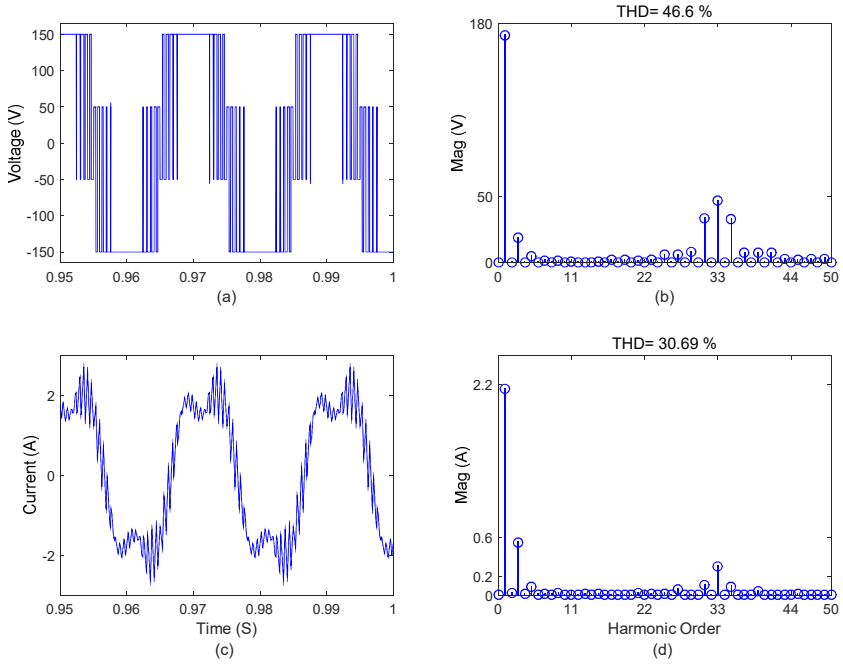


Fig. 4.12: Simulation results for NICSAZE PWM technique at m_a = 1: (a) $v_{a_1a_2}$ (b) $v_{a_1a_2}$ FFT analysis (c) i_a and (d) i_a FFT analysis

From the FFT analyses of the motor phae voltage and current, it can be concluded that, with the centre-spaced SVPWM scheme, the zero-sequence components (i.e. harmonics corresponding to the triplen order) exist in the motor phase voltage (Fig. 4.8 (a) & (b)), which cause the zero-sequence current (Fig. 4.8 (c) & (d)). The effectiveness of the DSAZE PWM and the proposed NICSAZE PWM is evident, as the zero-sequence voltage is forced to become equal to zero in every sampling time interval (Figs. 4.9 and 4.11).

4.4.2 Experimental Results

To validate the proposed power circuit configuration and the NICSAZE PWM scheme, a dual-inverter system is fabricated with dc-link voltages of 200V and 100V respectively for VSI-1 and VSI-2. To achieve waveform symmetries 66 samples are used in any given cycle [65], irrespective of the modulation index. This means that at a modulation index of unity, the sampling frequency would be equal to 3.3 KHz and the switching frequency is half of the sampling frequency [108]. The hardware control platform *dSPACE-1104* is used to generate the gating pulses for the dual-inverter configuration.

Fig. 4.13 shows the experimentally obtained waveforms for the motor phase voltage and current with the conventional (i.e. the center-spaced) SVPWM technique. It may be noted that the experimental results are in agreement with the simulation results. It is evident that the motor phase current has a significant zero-sequence component in it.

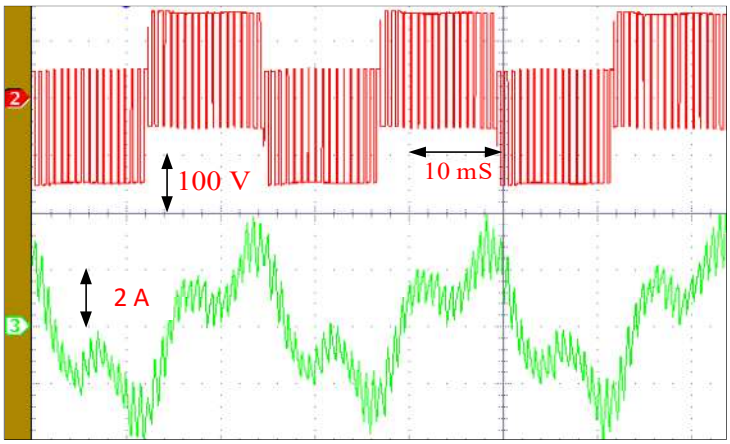
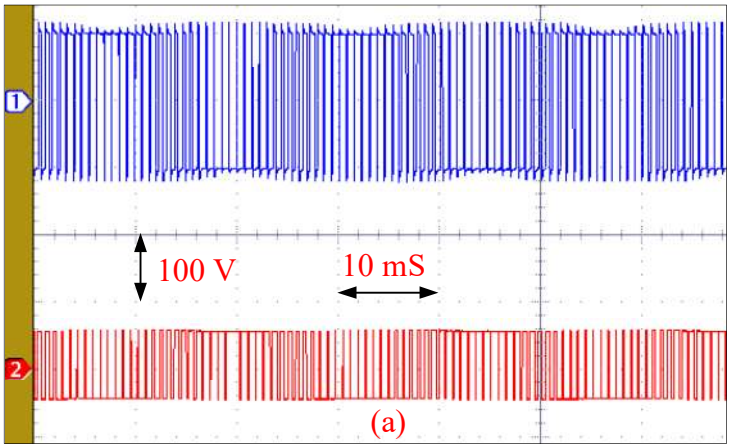


Fig. 4.13: Experimental results for Center-Spaced SVPWM technique at $m_a = 0.7$: $v_{a_1a_2}$ (top) and i_a (bottom)

Experimentation is carried out for the both of the PWM techniques to validate the simulations results are presented in Figs. 4.14-4.17. Fig. 4.14 and 4.15 shows the pole voltages of VSI- 1 and 2, motor phase voltage, current waveforms with FFT analysis when the DSAZE PWM technique is applied to the system. Figs. 4.16 and 4.17 shows the similar results, when the proposed 4-L OEWIMD is operated using the proposed NICSAZE PWM scheme.



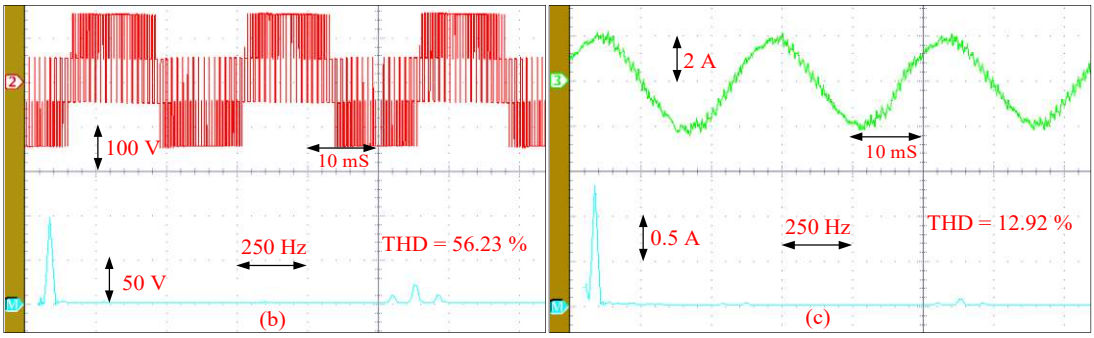


Fig. 4.14: Experimental results for DSAZE PWM technique at $m_a = 0.7$: (a) Pole voltage of VSI-1 (top) and VSI-2 (bottom), (b) $v_{a_1a_2}$ and its harmonic spectrum (c) i_a and its harmonic spectrum

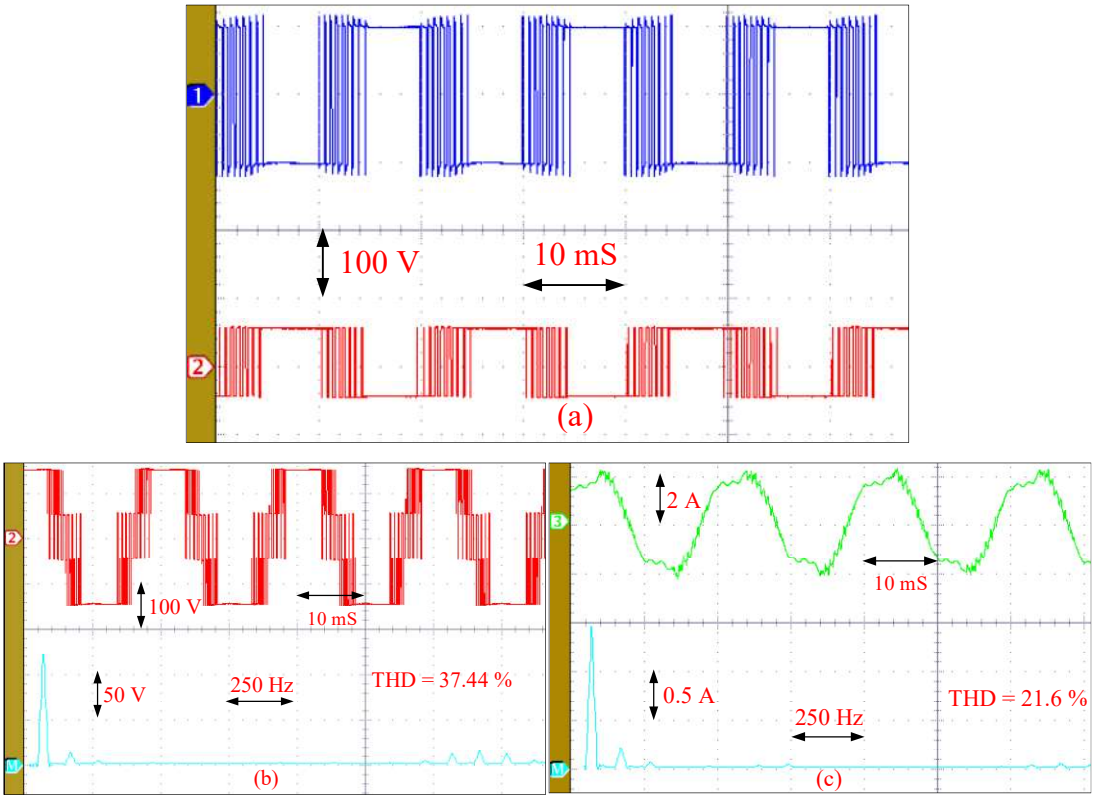


Fig. 4.15: Experimental results for DSAZE PWM technique at $m_a = 1$: (a) Pole voltage of VSI-1 (top) and VSI-2 (bottom), (b) $v_{a_1a_2}$ and its harmonic spectrum (c) i_a and its harmonic spectrum

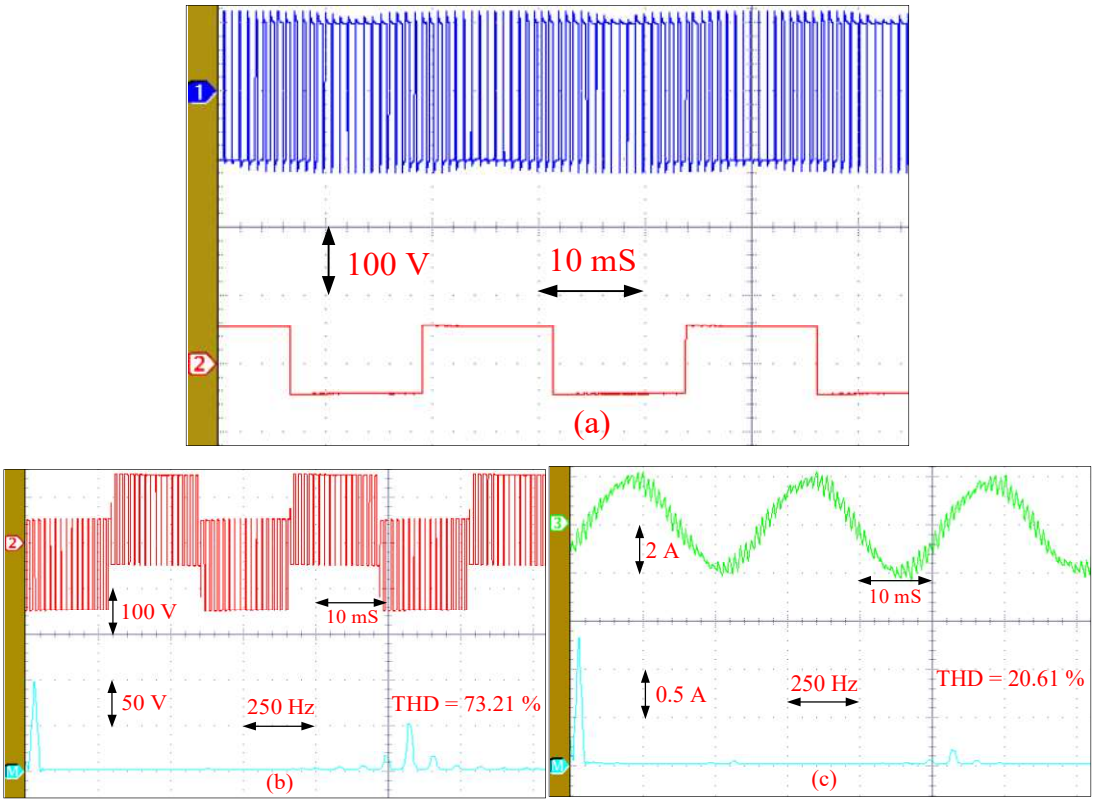
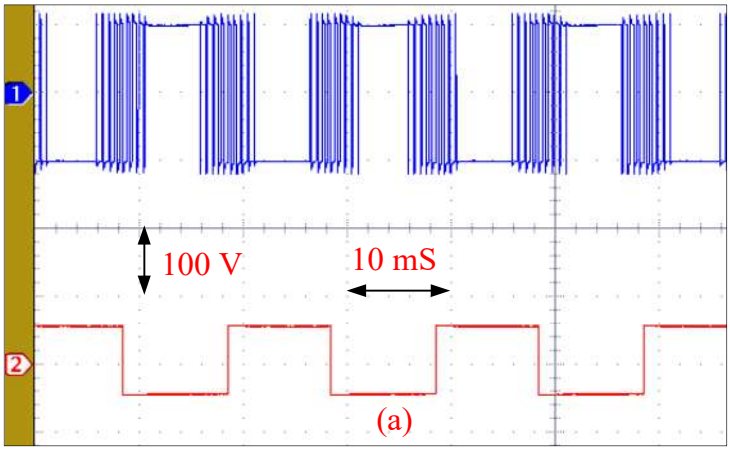


Fig. 4.16: Experimental results for NICSAZE PWM technique at m_a = 0.7: (a) Pole voltage of VSI-1 (top) and VSI-2 (bottom), (b) $v_{a_1a_2}$ and its harmonic spectrum (c) i_a and its harmonic spectrum



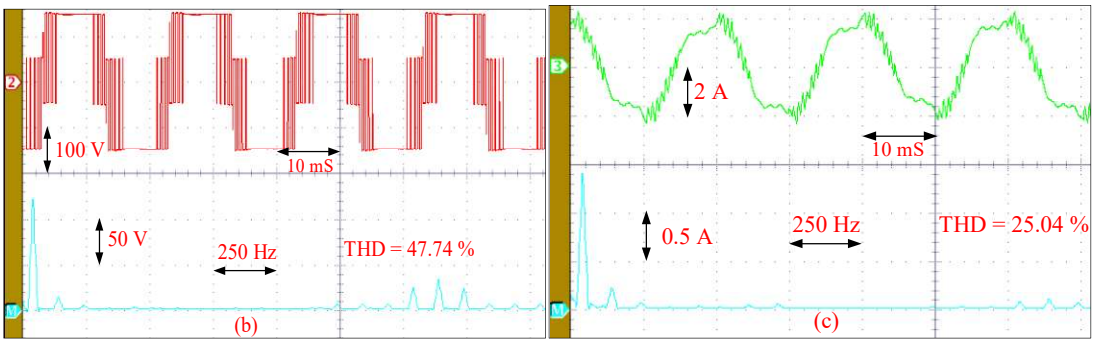


Fig. 4.17: Experimental results for NICSAZE PWM technique at m_a = 1: (a) Pole voltage of VSI-1 (top) and VSI-2 (bottom), (b) $v_{a_1a_2}$ and its harmonic spectrum (c) i_a and its harmonic spectrum

The agreement of simulation and experimental results validate the applicability of the proposed NICSAZE PWM scheme for the proposed circuit configuration for the four-level OEWIMD.

From the pole voltages presented in Figs. 4.14 (a) and 4.16 (a) it can be easily observed that both inverters are switched in the case of the DSAZE PWM technique. It may also be observed that VSI-2 is clamped, while VSI-I is switched in the case of the proposed NICSAZE PWM scheme.

It may also be readily observed that the motor phase voltage waveforms show four levels with both of the PWM schemes. However, based on the harmonic spectrum of the current waveforms, it can be observed that the current ripple is less with the DSAZE PWM compared to the NICSAZE PWM scheme.

This is not surprising considering the fact that higher switching would decrease the ripple in the current. However, the switching loss in the inverter is increased with the DSAZE PWM scheme. In contrast, the NICSAZE PWM results in a lower switching loss. Thus, it is evident that the proposed NICSAZE PWM scheme is an engineering compromise between the elimination of the zero-sequence current and the minimization of switching power loss in the dual-inverter system. It would be interesting to compare the switching and conduction power losses occurring in the dual-inverter system with these two PWM schemes.

The experimental torque and speed waveforms of the OEWIMD with the proposed topology are shown in Fig. 4.18 for NICSAZE PWM technique.

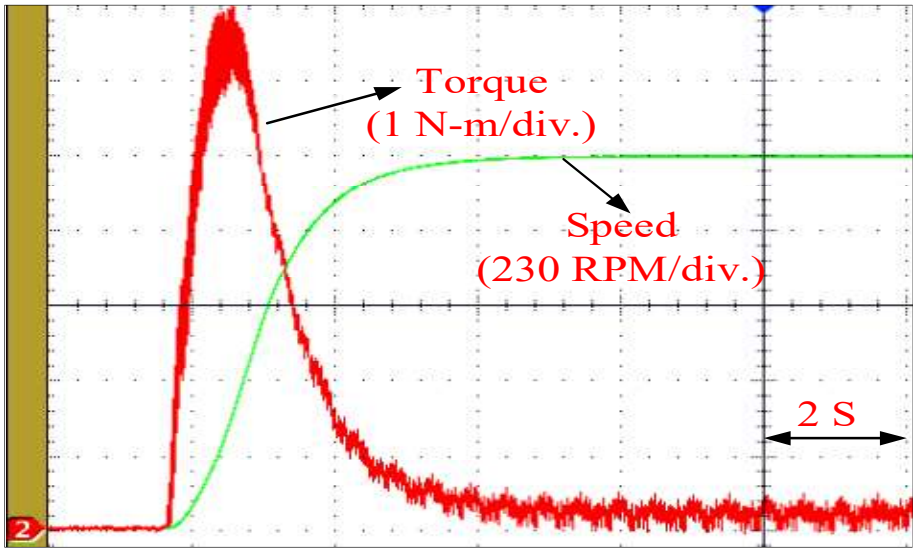


Fig. 4.18: Experimental torque and speed waveforms of OEWIMD with NICSAZE PWM technique at $m_a = 0.7$

4.4.3 Fault tolerant capability of the proposed power circuit configuration

A certain type of fault tolerance is observed with this circuit-configuration. The proposed circuit shows fault tolerance towards the imbalance of the dc-link capacitor of the nested rectifier. Fig. 4.19 shows the distribution of the dc-link capacitors of the nested rectifier. The sum of these two dc-link capacitors must remain the same, even though the voltages of individual dc-link capacitors are different. Let it be assumed that the variable 'x' denotes the degree of such an imbalance. The voltage levels impressed upon the terminals a_1 and a_2 are shown in Table 4.5.

It can easily be verified that the difference of these two pole voltages (which is equal to the motor phase voltage) would be the same for any value of $'x'$. It may be noted that $x = 1/2$ corresponds to the case of balanced operation of the dc-link capacitors of the nested rectifier.

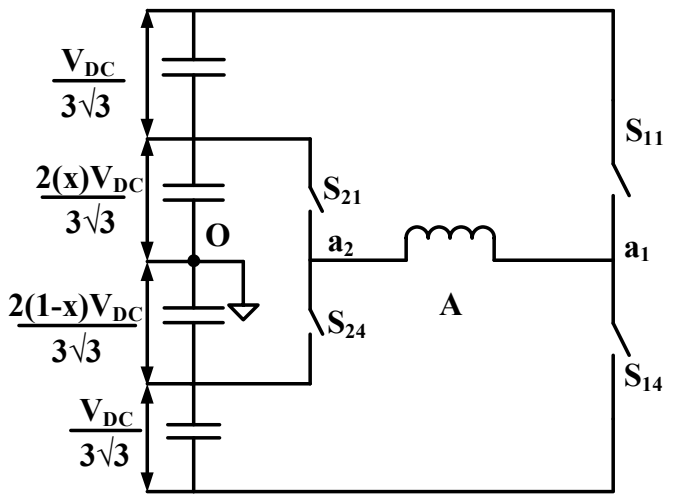


Fig. 4.19: Distribution of dc-link voltages for the proposed topology with unbalance

Table 4.5: Unbalanced voltage levels across phase-A winding of OEWIMD

Pole Voltage	Voltage Level	Switch turned on	Switch turned off
V_{a_2o}	$\frac{2x}{3\sqrt{3}}V_{DC}$	S_{21}	S_{24}
	$\frac{-2(1-x)}{3\sqrt{3}}V_{DC}$	S_{24}	S_{21}
V_{a_1o}	$\frac{2}{\sqrt{3}}\left\{\frac{xV_{DC}}{3}+\frac{V_{DC}}{6}\right\}$	S_{11}	S_{14}
	$\frac{-2}{\sqrt{3}}\left\{\frac{(1-x)V_{DC}}{3}+\frac{V_{DC}}{6}\right\}$	S_{14}	S_{11}

To practically demonstrate this assertion, an imbalance is deliberately introduced on the dc-link capacitors of the nested rectifier by removing an equalizing resistor connected across the capacitor. Fig. 4.20 (a) shows the pole voltages of individual inverters, which clearly shows the imbalance. However, the motor phase voltage (see Fig. 4.20 (b)) (i.e. the difference of the pole voltages) remains balanced, despite the imbalance of the individual pole voltages. The dual-inverter system is loaded to explain its ruggedness under this condition. Fig. 4.20 (c) shows the motor phase current and the total dc-link voltage under loaded conditions, corresponding to the case of x= 0.35. It may be noted that the sum of the voltages of the individual dc-links remains unaltered even when the dual-inverter system is loaded such an unbalanced condition. Thus, the fault tolerant capability of the dual-inverter system is demonstrated.

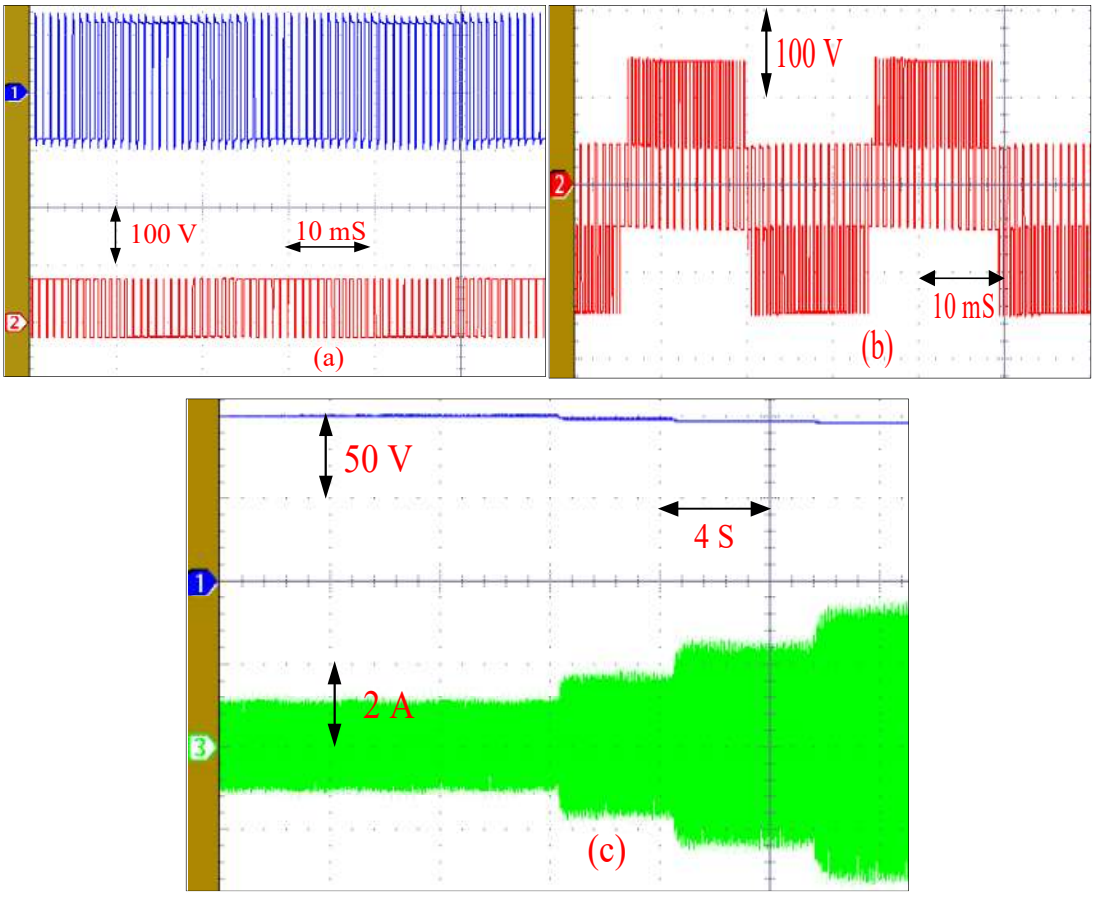


Fig. 4.20: (a) Unbalanced pole voltages of VSI-1 (top), VSI-2 (bottom), (b) balanced phase voltage and (c) OEWIMD phase current in loaded conditions at m_a = 0.6 with lower dc-link voltage

4.4.4 Performance characteristics of the proposed topology

The performance characteristics of the proposed topology mainly depends on the PWM strategy. In this section, the performance of the PWM techniques (namely DSAZE and NICSAZE) are critically compared in terms of the switching power loss, conduction power loss, total power loss in the dual inverter system.

In order to make a fair comparison an equal number of samples are used for both PWM schemes and same effective dc-link voltage is chosen: the number of samples employed are 66, as an odd number of samples/sector would ensure all types of symmetries [65]. A dc-link voltage of 564 V ensures that the rated voltage (230 V) is applied to the motor phases at the limit of linear modulation$\left(\sqrt{3}/2\right)$. A load of 20 N-m (approx. 80% of the full

load, see Table 4.3 and Table 4.4 for the motor parameters) is applied to the motor to compute the power loss incurred in the dual-inverter system.

All of the aforementioned performance indices are computed by employing an *improvised loss model*, which was proposed in chapter-2 for the loss calculation of the 4-L OEWIMD. The same model was extended to this work to compute the losses occurred in the 4-L OEWIMD.

The total power loss in the dual-inverter system comprises of switching loss (P_{SW}) in power semiconductor devices and the conduction loss (P_{Con}) in them.

The switching power loss (P_{SW}) is the sum of the $P_{SW,ON}$, and $P_{SW,OFF}$; where $P_{SW,ON}$ is the switching power loss during the turn-on transition of the switch and $P_{SW,OFF}$ is the switching power loss during the turn-off transition of the switching device. P_{SW}, P_{Con} are measured by extracting the simulation data of the voltage across the switch (v_{SW}) and the current through the switch (i_{SW}). The expressions for the P_{SW} and P_{Con} are given as [3],

$$P_{SW} = \left[\frac{1}{2} v_{SW} i_{SW} (t_{SWON} + t_{SWOFF})\right] \times f_S$$

$$P_{SW} = \left[\frac{1}{2} v_{SW} i_{SW} (t_{ri} + t_{fv}) + \frac{1}{2} v_{SW} i_{SW} (t_{rv} + t_{fi})\right] \times f_s \tag{4.24}$$

$$P_{Con} = \frac{v_{ON}\, i_{ON} t_{ON}}{T_S} \tag{4.25}$$

where, $v_{ON} = V_t + i_{ON} R_{CE}$ for IGBT

$v_{ON} = V_f + i_{ON} R_{AK}$ for the anti-parallel diode

where V_t is the IGBT fixed voltage drop under zero-current condition, R_{CE} is the IGBT on-drop resistance, V_f is the diode fixed voltage drop under zero-current condition and R_{AK} is the diode on-drop resistance. The parameters of the IGBT module-*SKM150GB12T4* are considered for the evaluation of the conduction loss. The following data is assumed to

compute the switching and conduction loss in each device: $t_{fv} = 1\ \mu s$, $t_{rv} = 2\ \mu s$, $t_{fi} = 4\ \mu s$, and $t_{ri} = 2\ \mu s$.

The plots of the P_{SW}, P_{Con} and overall loss for the dual-inverter system (P_{DI}) for the entire modulation range are shown in Fig. 4.21 (a)-(c) respectively. As explained earlier, the switching power loss is more with DSAZE, because of the switching of both of the inverters.

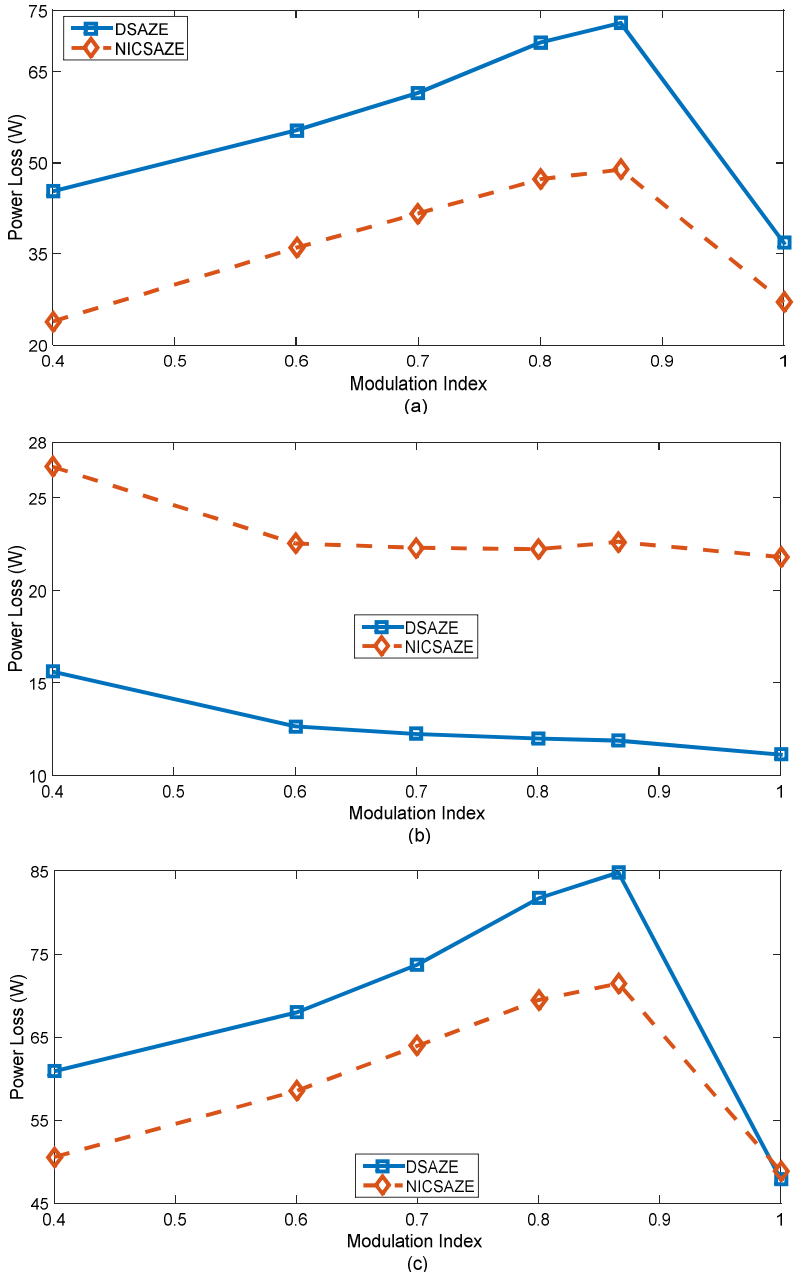


Fig. 4.21: Simulation results: (a) P_{SW} versus m_a (b) P_{Con} versus m_a (c) P_{DI} versus m_a

As one might expect, the conduction loss is more for the NICSAZE PWM technique because of the clamping of VSI-2 compared to the DSAZE PWM scheme. The overall loss for the dual-inverter system (P_{DI}) is less with the NICSAZE PWM as compared to the DSAZE, as the loss in the dual-inverter system is dominated by P_{SW}.

4.5 Conclusion

This chapter suggests a new circuit topology for the four-level Open-End Winding Induction Motor Drive, which is operated with unequal dc-link voltages, which are in the ratio of 2:1. The proposed circuit configuration avoids the overcharging of the lower dc-link voltage capacitor by its counterpart, when compared to the conventional topology and requires only two isolated dc-power supplies compared to the nested rectifier-inverter configuration proposed earlier. The proposed circuit configuration exhibits immunity to the internal imbalance of the dc-link voltages of the nested rectifier.

A new PWM strategy called the Nested Inverter Clamped Sample Average Zero-Sequence Elimination (NICSAZE) is also proposed to arrest the flow of zero-sequence current in the circuit. Simulation studies indicate the overall power loss incurred in the dual-inverter system is lower compared to the DSAZE PWM scheme proposed earlier. However, the NICSAZE PWM scheme is plagued with the limitation of an inferior spectral performance compared to the DSAZE PWM schemes.

Chapter 5

An Efficient Predictive Current Control Strategy for a Four-Level Open-End Winding Induction Drive

Contents

5.1 Introduction

The most recent tool added to the gamut of control strategies for power electronic converters and electric drives is the *Finite-Set Model Predictive Control (FS-MPC).*

Unlike the classical control strategies, FS-MPC algorithms typically employ cost functions to optimize a given control objective. FS-MPC algorithms try out all available candidate-solutions (switching vectors in the present context) by substituting them in the cost function and then decide as to which of them is the best. Often, the best solution is the one, which results in the minimum error between the reference values and the actual variables. The most important advantage of the FS-MPC strategy lies in its flexibility of formulating the cost function, which can easily accommodate several variables and constraints. The advantages and disadvantages associated with FS-MPC vis-à-vis the classical control strategies are well described in [80]. Availability of fast control platforms with tailor-made architectural features, which can cope with the extensive computational burden associated with the implementation of FS-MPC, is the principal contributing factor for the application of FS-MPC strategies to electric drive applications.

Recently, an FOC technique was implemented by using FS-MPC algorithm, named as Predictive FOC (PFOC) or Predictive Current Controller (PCC) [80]. This is an alternative to the Predictive Torque Control (PTC) to control electrical drives. Instead of minimizing the errors in torque and flux magnitudes as in PTC, PCC directly exerts control over the motor phase currents, without any weighting factor in its cost function.

This chapter proposes an improvised PCC strategy for a four-level OEWIMD to select the optimal voltage vector. The optimal voltage vector is selected based on the clamping of one of the inverter (operating with lower dc-link voltage) and is identified by using the concept of the Nearest Sub-Hexagonal Center. The other inverter is switched around the clamped inverter. The cost function of the proposed scheme takes only 5 voltage vectors to evaluate the optimal value based on the difference of two voltage vectors, without adding any additional constraints. The proposed PCC improves the performance of the drive in terms of the voltage and current THDs and ripple in the steady state torque. It is shown that, the overall

losses in the drive system are reduced with the proposed PCC in the low speed as well as the high speed range of operation. Furthermore, the proposed scheme reduces the switching frequency and the computational burden on the controller.

5.2 Modeling of Four-Level OEWIM Drive

The Power circuit for the four-level OEWIM Drive, which was described in Chapters 2 and 3, is considered for the application of the PCC algorithm and is reproduced in Fig. 5.1 to facilitate an easy reference. The dc-link voltages of Fig. 5.1 are maintained in the ratio of 2:1 to realize four-level inversion [62] and isolated power supplies are used to avoid the path for the zero-sequence current.

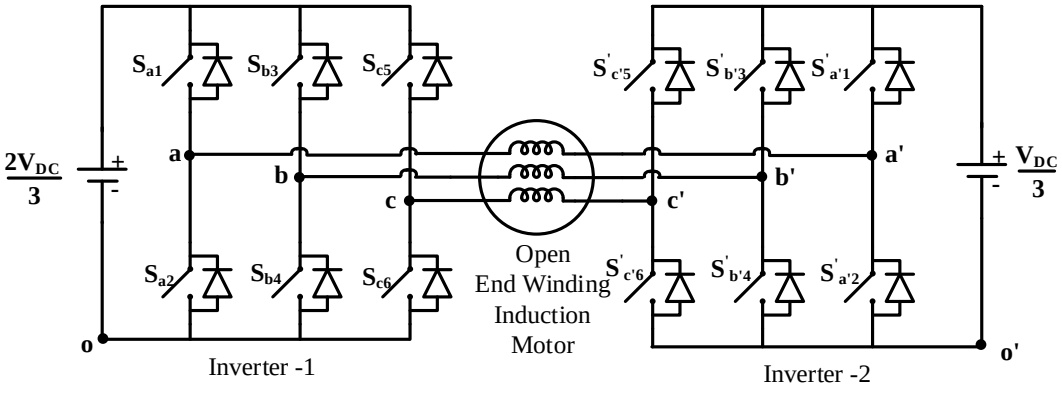


Fig. 5.1: Circuit diagram of four-level OEWIMD

The individual inverters of this OEWIM Drive have 8 individual switching states and hence the resultant space vector diagram for the dual-inverter system of the OEWIMD have 64 space vector combinations and are spread over 37 space vector locations as shown in Fig. 5.2.

The mathematical model of an induction motor can be extended to an open-end winding induction motor in any arbitrary reference frame rotating at an angular frequency of $'\omega_a'$, which is given by [80]:

$$\bar{v}_s = R_s\bar{\imath}_s + d\bar{\psi}_s/dt + j\omega_a\bar{\psi}_s \quad (5.1)$$

$$\bar{v}_r = R_r \bar{\imath}_r + d\bar{\psi}_r/dt + j(\omega_a - \omega)\bar{\psi}_r \quad (5.2)$$

$$\bar{\psi}_s = L_s \bar{\imath}_s + L_m \bar{\imath}_r \quad (5.3)$$

$$\bar{\psi}_r = L_m \bar{\imath}_s + L_r \bar{\imath}_r \quad (5.4)$$

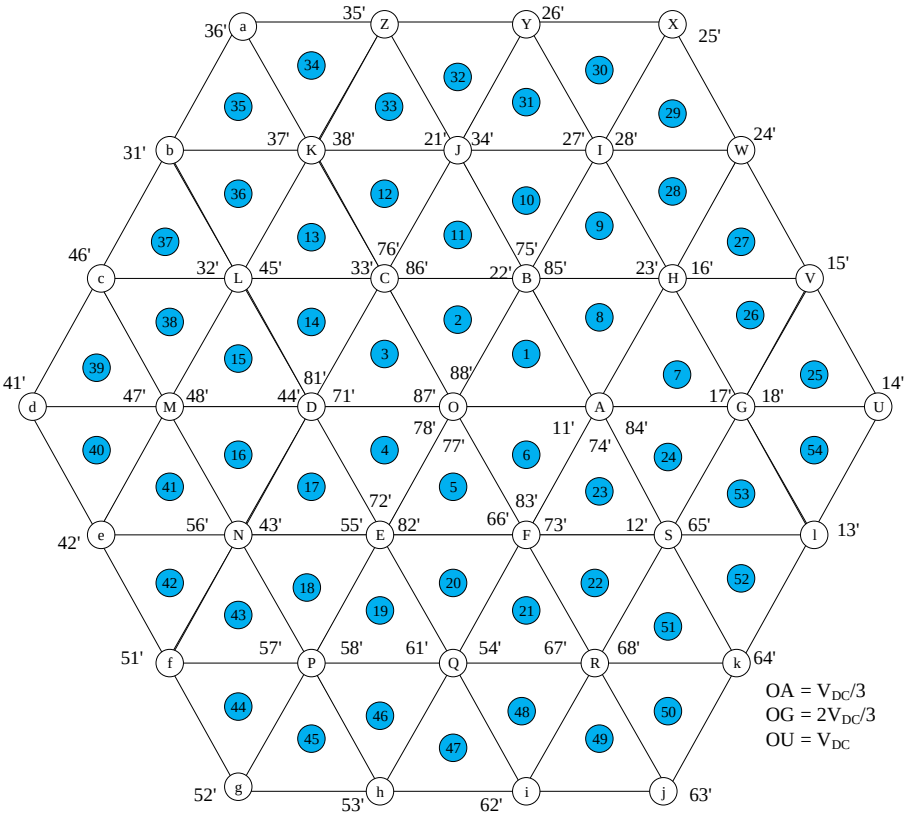


Fig. 5.2: Dual-inverter system overall space vector diagram

The subscripts s, r stands for stator and rotor variables respectively. The symbols $\bar{v_s}$ and $\bar{v}_r$ respectively denote the space vectors corresponding to the applied stator voltage and the rotor voltage (which is equal to zero, for a squirrel cage machine). Similarly, the symbols $\bar{\imath_s}$, $\bar{\imath_r}$ denote the current vectors and $\bar{\psi}_s, \bar{\psi}_r$ denote the flux-linkage vectors. R_s, R_r are the resistances, L_s, L_r are the inductances and L_m is the mutual inductance. The variable $'\omega'$ represents the electrical rotor angular speed. In general, the rotor resistance $'R_r'$ is referred to the primary side (i.e. stator), which is denoted as R_{rp}.

The pole voltages of inverter-1 (v_{ao}, v_{bo} and v_{co}) & inverter-2 ($v_{a'o'}, v_{b'o'}$ and $v_{c'o'}$) in terms of switching pulses are shown in eq. 5.5 & 5.6 [107].

$$\begin{bmatrix} v_{ao} \\ v_{bo} \\ v_{co} \end{bmatrix} = \frac{2V_{DC}}{3} \begin{bmatrix} S_{ay} \\ S_{by} \\ S_{cy} \end{bmatrix} \tag{5.5}$$

$$\begin{bmatrix} v_{a'o'} \\ v_{b'o'} \\ v_{c'o'} \end{bmatrix} = \frac{V_{DC}}{3} \begin{bmatrix} S_{a'y} \\ S_{b'y} \\ S_{c'y} \end{bmatrix} \tag{5.6}$$

where $s_{xy} = 0, 1$ ($x \in a, b, c, a', b', c'$ and $y \in 1, 2, 3, 4, 5, 6$)

The voltage across the stator phase winding of OEWIMD, is the difference between pole voltages of inverter-1 and 2 are given in eq. 5.7,

$$\begin{bmatrix} \Delta v_{aa'} \\ \Delta v_{bb'} \\ \Delta v_{cc'} \end{bmatrix} = \begin{bmatrix} v_{ao} \\ v_{bo} \\ v_{co} \end{bmatrix} - \begin{bmatrix} v_{a'o'} \\ v_{b'o'} \\ v_{c'o'} \end{bmatrix} \tag{5.7}$$

Using eq. 5.7, the zero-sequence voltages are defined as,

$$v_z = \frac{1}{3} [\Delta v_{aa'} + \Delta v_{bb'} + \Delta v_{cc'}] \tag{5.8}$$

From eqs. 5.7 and 5.8, the phase voltage expressions of the open-end winding induction motor are given as,

$$\begin{bmatrix} v_{aa'} \\ v_{bb'} \\ v_{cc'} \end{bmatrix} = \begin{bmatrix} \Delta v_{aa'} - v_z \\ \Delta v_{bb'} - v_z \\ \Delta v_{cc'} - v_z \end{bmatrix} \tag{5.9}$$

$$\begin{bmatrix} v_{aa'} \\ v_{bb'} \\ v_{cc'} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} \Delta v_{aa'} \\ \Delta v_{bb'} \\ \Delta v_{cc'} \end{bmatrix} \tag{5.10}$$

Using eq. 5.10 and Clark transformation, the quadrature components of the motor phase voltages are given as,

$$\nu_{\alpha s} = \frac{3}{2}\,\nu_{aa'} \tag{5.11}$$

$$\nu_{\beta s} = \frac{\sqrt{3}}{2}(\nu_{bb'} - \nu_{cc'}) \tag{5.12}$$

5.3 Conventional Predictive Current Controller for a Four-Level OEWIMD

The basic block diagram of the Predictive Current Controller (PCC) for the four-level OEWIMD is shown in Fig. 5.3. From the block diagram, it may be noted that the following quantities need to be measured at the $'k^{th}'$ sampling instant to implement the PCC: (i) stator currents of any two phases (say $i_{as}(k)$ and $i_{bs}(k)$) from which, the stator current space vector $\bar{\imath}_s(k)$ is obtained (ii) the dc-link voltage V_{DC} and the available dual-inverter system switching states together are used to constitute the stator voltage space vector $\bar{v}_s$(k) (iii) the motor speed w_m(k). Based on these quantities, the rotor flux vector $\psi_r(k)$ is estimated. Using the Clark's transformation the measured stator currents $i_{as}(k)$ and $i_{bs}(k)$ are converted into $i_{\alpha s}(k)$ and $i_{\beta s}(k)$ and are compared with the reference currents $i^*_{\alpha s}(k)$ and $i^*_{\beta s}(k)$ respectively. These references (i.e. $i^*_{\alpha s}(k)$ and $i^*_{\beta s}(k)$) are obtained from the speed-PI controller and the reference rotor flux.

5.3.1 Stator current prediction

The proposed conventional PCC strategy uses the stator current ($\bar{\imath}_s$) and rotor flux ($\bar{\psi}_r$) as state variables [109]. The stator currents can be directly measured, whereas the rotor flux has to be estimated, because the rotor state variables cannot be measured directly in a squirrel cage machine. From the eqs. 5.1 – 5.4, the estimated value of the rotor flux is given as [80, 109]:

$$\bar{\psi}_r + \tau_r \frac{d\bar{\psi}_r}{dt} = -j(\omega_a - \omega)\tau_r\bar{\psi}_r + L_m\bar{\imath}_s \tag{5.13}$$

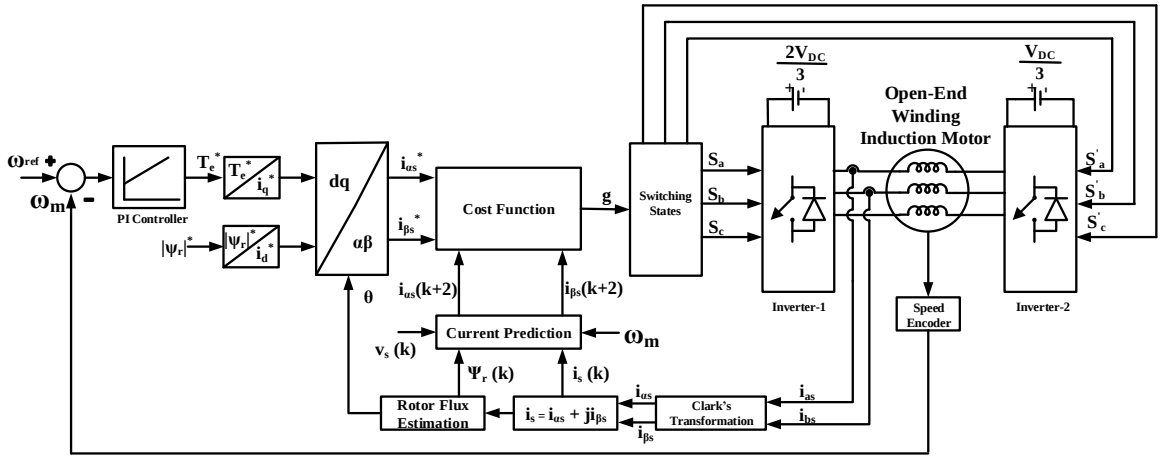


Fig. 5.3: Block diagram of PCC

From the measured currents and the estimated ψ_r, the stator current can be obtained as [80]:

$$\bar{\imath}_s + \tau_\sigma \, d\bar{\imath}_s/dt = -j\omega_a \tau_\sigma \bar{\imath}_s + k_r/R_\sigma \left(1/\tau_r - j\omega\right)\bar{\psi}_r + \bar{v}_s/R_\sigma \qquad (5.14)$$

where, $T_s = L_s/R_s$, $T_r = L_r/R_{rp}$, $\sigma = 1 - \left(\frac{((L_m)^2)}{(L_r L_s)}\right)$, $k_r = L_m/L_r$, $R_\sigma = R_s + {K_r}^2 R_{rp}$, $\tau_\sigma = \sigma L_s/R_\sigma$

Eq. 5.14 is discretized using the following relationships and considerations:

(i) $\frac{d\bar{\imath}_S}{dt} = \frac{\bar{\imath}_S(k+1) - \bar{\imath}_S(k)}{T_S}$

(ii) $\omega_a = 0$ (i.e. stationary frame is chosen for prediction and control)

(iii) The rotor flux $\bar{\psi}_r(k)$ is a constant

(iv) The voltage space vector is the optimum vector obtained by the evaluation of the cost function (shown in Fig. 5.3 and discussed in the next section) in the previous (i.e.$(k-1)^{th}$) sampling time period.

Based on the above relationships and considerations, the discretized version of eq. 5.14 is:

$$\bar{\imath}_s^p(k+1) = \left(1 + \frac{T_s}{\tau_\sigma}\right)\bar{\imath}_s(k) + \frac{T_s}{\tau_\sigma + T_s}\left\{\frac{1}{R_\sigma}\left[\left(\frac{k_r}{\tau_r} - k_r j\omega_m\right)\bar{\psi}_r(k) + \bar{v}_s(k)\right]\right\} \quad (5.15)$$

Furthermore, the following observations are made based on the implementation issues:

(i) Delay due to data acquisition, computation and output is inevitable in digital control systems, which must be compensated for [110].

(ii) In MPC systems, the optimal vector corresponding to the $(k+1)^{th}$ instant should be predicted at the k^{th} instant. This optimal vector must be applied at the k^{th} instant itself.

(iii) Since it is impossible to achieve this objective (due to the delay), the predictive horizon is extended and the optimal vector corresponding to the $(k+2)^{th}$ instant is obtained by applying all of the candidate vectors (37 or 5 in the present case for the four-level OEWIMD) to the cost function.

(iv) Since all of this activity takes place between the $(k)^{th}$ and $(k+1)^{th}$ instants, the optimal vector $(i.e.\ \bar{v}_s(k+1))$ applied at the $(k+1)^{th}$ instant to force $\bar{\imath}_s(k+2)$ to become equal to the reference current generated by speed-PI controller and reference rotor flux i.e.

$$i_\alpha^*(k+2) + j i_\beta^*(k+2) = i_\alpha(k+2) + j i_\beta(k+2)$$

Owing to the extension of the predictive horizon to the $(k+2)^{th}$ instant, eq. 5.15 becomes as:

$$\bar{\imath}_s^p(k+2) = \left(1 + \frac{T_s}{\tau_\sigma}\right)\bar{\imath}_s^p(k+1) + \frac{T_s}{\tau_\sigma + T_s}\left\{\frac{1}{R_\sigma}\left[\left(\frac{k_r}{\tau_r} - k_r j\omega_m\right)\bar{\psi}_r(k+1) + \bar{v}_s(k+1)\right]\right\} \quad (5.16)$$

From eq. 5.16, it can be observed that, the predicted current values are also dependent on the dual-inverter system voltage $(\bar{v}_s(k+1))$. As explained earlier, the four-level OEWIMD possess a total of 64 space vector combinations spread over 37 space vector locations (Fig. 5.2). Using eqs. 5.10, 5.11 and 5.12 the dual-inverter voltage space vector $\left(\bar{v}_s(k+1)\right)$ is computed in the stationary frame of reference for all of the 37 space vector combinations.

5.3.2 Generation of Reference Currents

The generation of reference currents is necessary for the predictive current controller. The reference torque component (T_e^*) is the output of the speed PI-controller, which tries to make the error between the reference speed and actual speed to zero. The rotor flux reference (ψ_r^*) is a constant, which is equal to the rated rotor-flux of the machine. The values of the reference currents (i_q^*, i_d^*) for the respective T_e^* and ψ_r^* in rotor field orientation are calculated as follows [84]:

$$\left.\begin{aligned} i_q^*(k) &= \frac{2}{3}\frac{L_r}{L_m}\frac{T_e^*}{|\psi_r^*|} \\ i_d^*(k) &= \frac{|\psi_r^*|}{L_m} \end{aligned}\right\} \tag{5.17}$$

The stator current space vector $(i_s^*(k))$ is constructed using eq. 5.17 and is transformed to the $\alpha - \beta$ frame using the inverse-park transformation before getting substituted into the cost function. As mentioned in the previous section, the stator currents are predicted two samples ahead. However, the reference currents pertain only to the present time instant (i.e. k^{th} sampling time interval). Thus, the reference current is also calculated at two samples ahead by the Lagrange extrapolation method [80] and the resultant expression is given as follows:

$$\bar{\imath}_s^*(k+2) = 6\bar{\imath}_s^*(k) - 8\bar{\imath}_s^*(k-1) + 3\bar{\imath}_s^*(k-2) \tag{5.18}$$

5.3.3 Cost-function

From the principle of the PCC, for every sample time period the predicted stator current from all of the possible voltage space vectors is to be compared by its reference value and then an optimal voltage vector is chosen based on the minimal value of the cost function and is defined as follows:

$$g_i(p) = \sqrt{\left\{real\left(\left|\bar{\imath}_s^*(k+2) - \left(\bar{\imath}_s^p\ (k+2)_p\right)\right|\right)^2 + \ imag\left(\left|\bar{\imath}_s^*(k+2) - \left(\bar{\imath}_s^p\ (k+2)_p\right)\right|\right)^2\right\}} \tag{5.19}$$

here, $p\ \in 0, 1, 2, 3, \ldots, 36$ and the cost function evaluates all of the 37 voltage space vectors to identify the optimal one, which minimizes the error.

It is important to note the following points, while implementing the conventional PCC: 1) the compensation delay should be considered, otherwise the motor-drive performance would deteriorate as documented in [80, 81]. 2) The cost function has to evaluate all of the 37 candidate voltage space-vectors. Because of this, the computational burden on the controller is increased.

5.4 Predictive Current Controller for a Four-Level OEWIMD based on Nearest Sub-Hexagonal Centers

As mentioned in the earlier section, in order to determine the optimal voltage vector, the cost function has to be evaluated for all of the 37 voltage space vectors. The main advantage of the OEWIMD is that, it is very rich in redundancy of switching states. In chapter-3, a discontinuous modulation scheme based on the space vector PWM technique is proposed, wherein one inverter is operated as a clamping inverter and other inverter acts as a switching inverter. The switching states of the clamping inverter are identified based on the principle of the Nearest Sub-Hexagonal Center (NSHC explained in the next section), which is extended here to implement the PCC for the OEWIMD. The detailed procedure is explained in the following sections.

5.4.1 Selection of optimal voltage vector

In the conventional PCC, based on the optimal voltage vector, both of the inverters of the OEWIMD are switched. However, it is possible to have one of the inverters of the dual-inverter system clamped and other one switched around it [107]. The clamped state of the inverter is identified by using the NSHC approach [107]. In order to implement this strategy, the eq. 5.15 is rewritten as follows:

$$\overline{v_s}(k) = R_\sigma \left\{ \frac{T_s+\tau_\sigma}{T_s} \left(\overline{i_s^p}(k+1) - \left(\frac{T_s+\tau_\sigma}{T_s} \right) \overline{i_s}(k) \right) \right\} - \left(\frac{k_r}{\tau_r} - j k_r \omega_m \right) \overline{\psi_r}(k) \qquad (5.20)$$

In the conventional PCC, the predicted stator current at $(k+1)^{th}$ instant has to be equal to the generated reference currents (output of speed-PI controller, reference rotor flux)

[80], i.e. $\bar{\imath}_s^p(k+1) = \bar{\imath}_s^*(k+1)$ and the eq. 5.20 is rewritten (assuming $\psi_r(k+1) = \psi_r(k)$) as,

$$\bar{v}_s^*(k+1) = R_\sigma \left\{ \frac{T_s+\tau_\sigma}{T_s} \left(\bar{\imath}_s^*(\mathrm{k}+1) - \left(\frac{T_s+\tau_\sigma}{T_s} \right) \bar{\imath}_s(k) \right) \right\} - \left(\frac{k_r}{\tau_r} - jk_r\omega_m \right) \overline{\psi_r}(k) \quad (5.21)$$

From eq. 5.21, the reference voltage vectors are obtained in the $\alpha - \beta$ frame. The following steps are used to identify the NSHC and the corresponding available voltage vectors in each sector.

Step-1: Obtaining the instantaneous reference phase voltage variables v_a^*, v_b^* and v_c^* from the $v_{\alpha s}^*, v_{\beta s}^*$ using the *inverse-Clark transformation.*

Step-2: Determination of the *maximum* and *minimum* of phase voltage values using $v_{max} = \mathrm{maximum}[(v_a^*, v_b^*, v_c^*, -v_a^*, -v_b^*, -v_c^*)]$ [107].

Step-3: Identification of the NSHC based on the step-2. For example, if $'v_a^{*\prime}$ is the maximum phase voltage, then NSHC is $'\mathrm{A}'$ and inverter-2 of the OEWIMD is clamped to the state $4'(-++)$ (see Fig. 5.4).

Step-4: Identifying the candidate voltage space vectors based on the NSHC for the switching inverter (inverter-1 in Fig. 5.1).

Step-5: Identifying the pole phase of the switching inverter, which is clamped to the positive dc-rail or the negative dc-rail based on the maximum or minimum reference voltages.

To explain the above steps, let it be assumed that $v_{max} = -v_a^*$ i.e. the NSHC is $'\mathrm{D}'$ (Fig. 5.4). Now, inverter-2 of the dual-inverter system acts as the clamped inverter with the sub-hexagonal center 'D' (i.e. state $1'(+--)$) and the corresponding vector is OD. Inveter-1 acts as the switching inverter. From Fig. 5.4, the possible space vector switching locations for the inverter-1 are at O, D, b, d and f. From this discussion, it can be concluded that, as compared to the conventional PCC, the voltage vectors are limited to 5 instead of 37. It

should be noted that the vectors at O and D are applied in the low speed range, while the vectors at D, b, d and f are employed in the medium and the high-speed range.

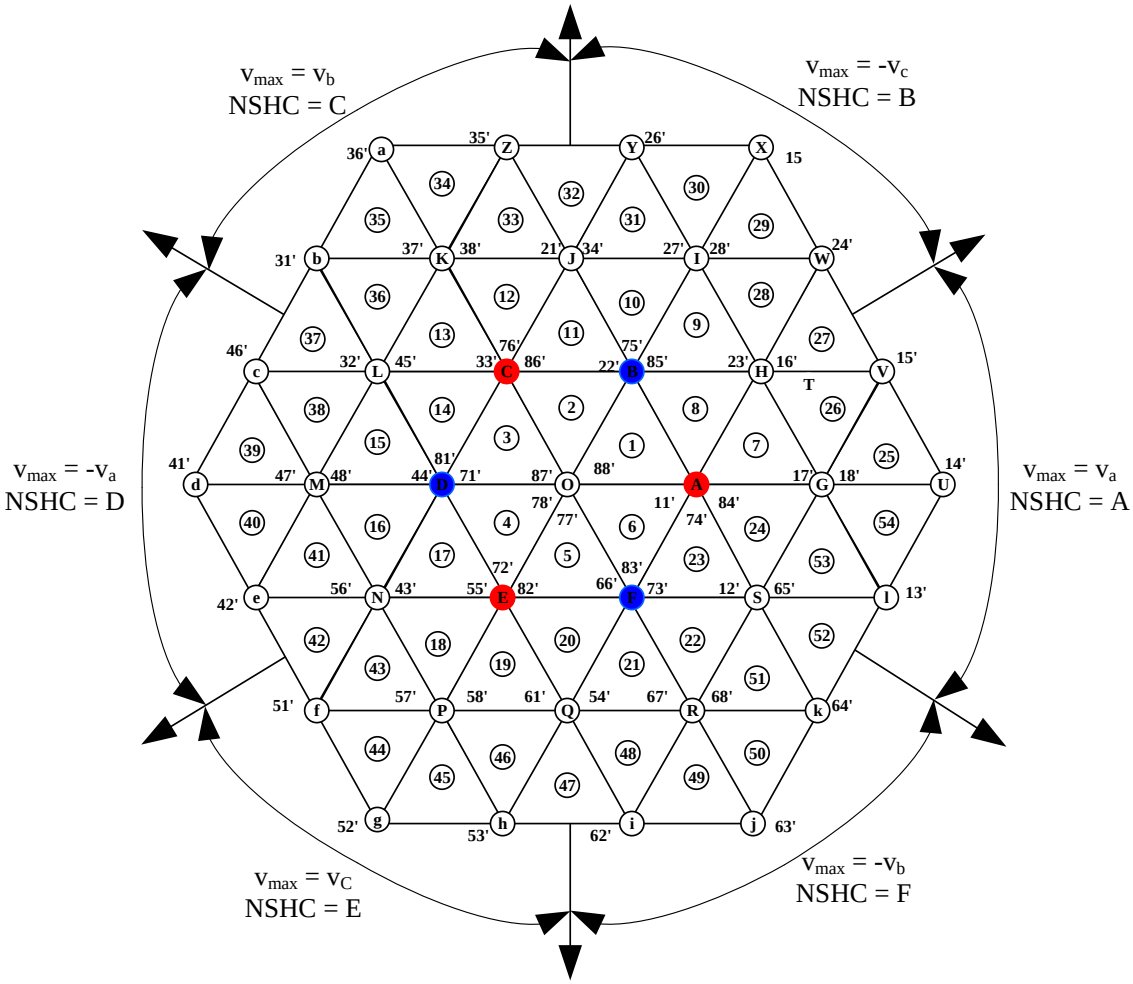


Fig. 5.4: Voltage vector selection using NSHC for OEWIMD

Thus, the salient features of the proposed PCC may be enumerated as follows: i) the identification of NSHC is very simple, and doesn't require any complicated equations and trigonometric functions. ii) Based on the NSHC, inverter-2 is clamped to one of the six switching states, while inverter-1 is switched around it. In the switching inverter (i.e. inverter-1), one phase is always clamped, depending on the sub-hexagonal center. For example, in the medium and high speed ranges, the vectors employed for the switching inverter, situated at b, d, f and D are: 3(-+-), 4(-++), 5(--+) and 8(---). It is obvious that, phase-A of inverter-1 is clamped to the negative dc-rail (Fig. 5.1) when these vector are switched.

5.4.2 Formulation of the Cost-function based on Voltage References

Sample delay is inevitable in the discrete systems. To accommodate this delay a compensation scheme is used, wherein the predictive horizon is extended to the $(k+2)^{th}$ sample and the eq. 5.21 is rewritten as,

$$\overline{v_s^*}(k+2) = R_\sigma \left\{ \frac{T_s+\tau_\sigma}{T_s} \left(\overline{i_s^*}(\mathrm{k}+2) - \left(\frac{T_s+\tau_\sigma}{T_s} \right) \overline{i_s^p}(k+1) \right) \right\} - \left(\frac{k_r}{\tau_r} - j k_r \omega_m \right) \overline{\psi_r}(k) \quad (5.22)$$

Unlike the conventional PCC, wherein the optimal vector is identified with a current-based cost function, the proposed PCC employs a voltage-based cost function which is defined as follows.

$$g_v(p) = \sqrt{\left| v_{\alpha s}^*(k+2) - v_{\alpha s}(k)_p \right|^2 + \left| v_{\beta s}^*(k+2) - v_{\beta s}(k)_p \right|^2} \quad (5.23)$$

where, $p \in 0, 1, 2, 3, \& \, 4$

From eq. 5.22, the reference voltage is generated. Similarly, based on the NSHC, the corresponding candidate voltage vectors ($\bar{v}_s(k)$) in each sector are identified. Each of these five candidate vectors are individually tried out in eq. 5.23 and the one which results in minimum error is identified as the optimal vector.

The detailed control algorithm flow chart and the block diagram to implement the proposed PCC technique for the four-level OEWIMD are shown in Figs. 5.5 and 5.6.

Based on the above discussion, the following conclusions may be drawn: i) The number of candidate vectors is reduced from 37 to 5, implying that the burden on the controller is reduced. ii) The switching frequency is also reduced as one of the inverter acts as the clamping inverter.

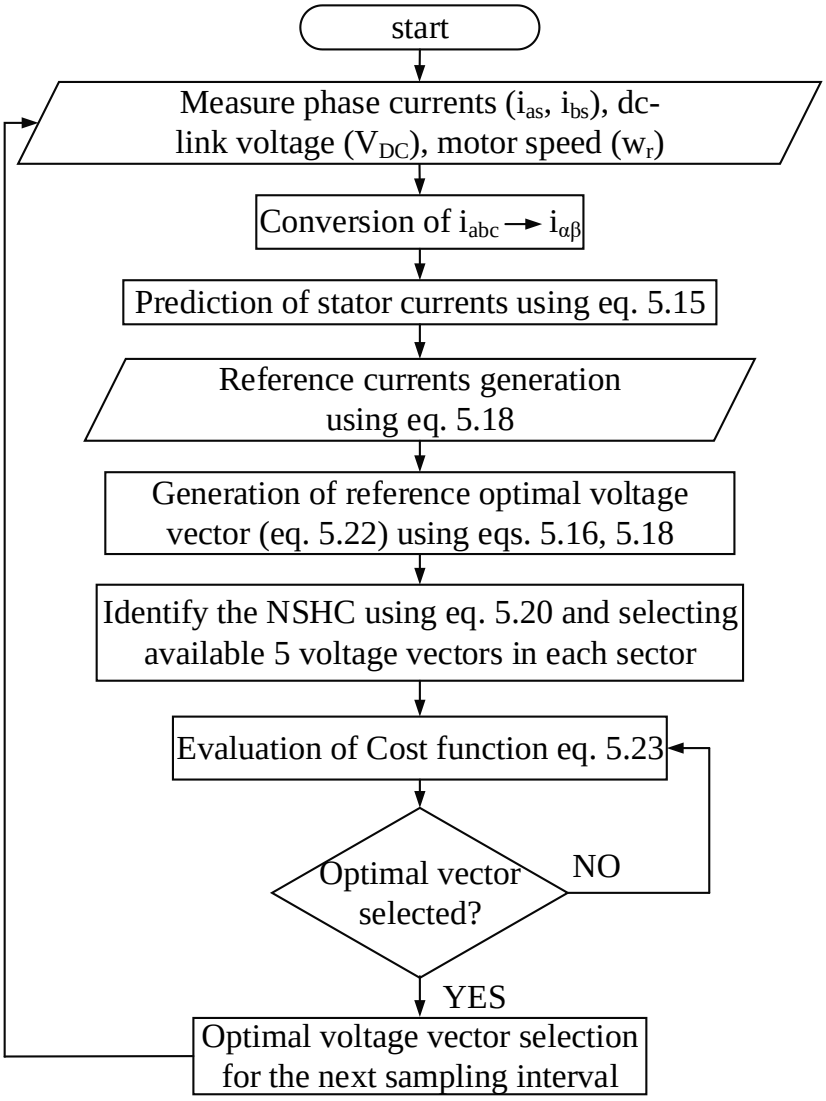


Fig. 5.5: Flow chart for the proposed PCC strategy

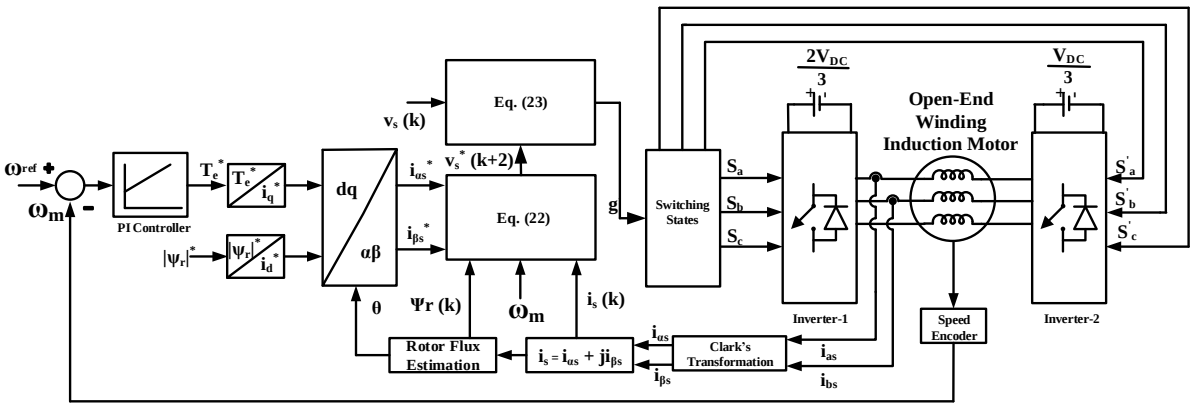


Fig. 5.6: Block diagram of proposed PCC for a four-level OEWIMD

5.5 Simulation and Experimental Results

The performances of the conventional as well as the proposed PCC techniques are obtained through simulation studies. These are compared to assess the effectiveness of the proposed PCC. To carry out these simulations, a 3.7 KW, 1445 RPM, 400 V (Line-line), 4-pole, 50 Hz OEWIMD supplied with two two-level voltage source inverters is employed.

The operating condition of the dual-inverter system is such that, a total dc-link voltage of the dual-inverter system is chosen as 564 V. The individual DC-link voltages of the individual inverters are maintained in the ratio of 2:1 to achieve four-level inversion. This means that, inverter-1 is operated with 376 V, whereas inverter-2 is operated with 188 V. While simulations are used to assess the performance of the drive with both of the PCC techniques in the steady state conditions, experimental studies capture the behavior of the drive in both dynamic as well as the steady state operating conditions.

The OEWIMD parameters are tabulated in Table 5.1. The *Matlab/Simulink* software is used to carry out the simulation.

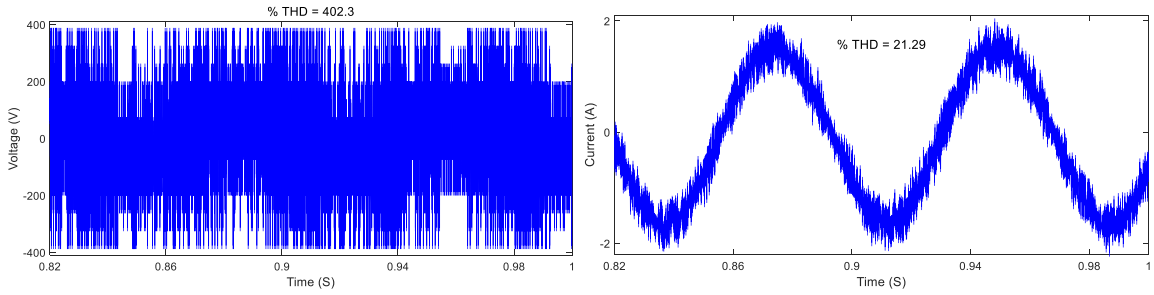
To validate the simulation results, the experimental results are performed on OEWIMD (Table 5.2 for motor parameters). The set-up used for the experimentation is shown in Fig. A1. The total dc-link voltage of the dual-inverter system is taken as 564 V to ensure rated motor phase voltage (i.e. 230 V). The Semikron IGBTs (1200 V, 30A) are used in the dual-inverter system. The rapid prototyping dSPACE-1104 controller is used to implement the proposed PCC and to generate the gating signals. Electrical isolation between the power circuit and the control platform is obtained with the opto-coupler based A3120 driver IC. One (1 number) Hall-effect based voltage sensor (LV 25-P) and two current sensors (LA 55-P) are used to sense the dc-link voltage of the dual-inverter system and the phase currents i_{as}, i_{bs} of the OEWIMD respectively. The sampling time period for the experimentation is chosen as 120 μS.

When the OEWIMD is operated lower speeds (400 RPM), the tip of the reference voltage vector is situated in the region of core-hexagon ABCDEF (Fig. 5.4). Under this condition, the conventional PCC evaluates all of the available candidate voltage vectors to

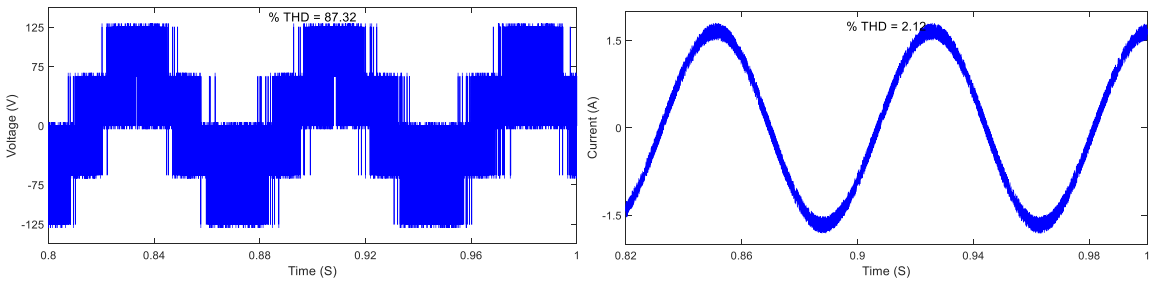
choose the optimal vector. In contrast, in the proposed PCC, inverter-1 is clamped to a null state (i.e. either 7 (+++) or 8 (---), providing a switched neutral point on one side), while inverter-2 is switched. Thus, at low speeds, with the proposed PCC, the four-level OEWIMD is operated as the conventional two-level VSI driven induction motor drive. The simulated and the experimentally obtained motor phase voltage $(v_{aa'})$ and current $(i_{aa'})$ waveforms for both of the methods are shown in Figs. 5.7 & 5.8 at a speed of 400 RPM demonstrate this feature.

Table 5.1: OEWIMD Parameters

Stator resistance (R_s)	4.5 Ω
Stator inductance (L_s)	0.5632 H
Rotor resistance (R_{rp})	6.2 Ω
Rotor inductance (L_r)	0.5632 H
Magnetizing inductance (L_m)	0.54 H
Reference rotor flux (ψ_r^*)	1.36 Wb
Line-Line Voltage	415 V
Supply frequency	50 Hz
Power	5 HP
Rotor Speed	1445 RPM
No. of Poles	4

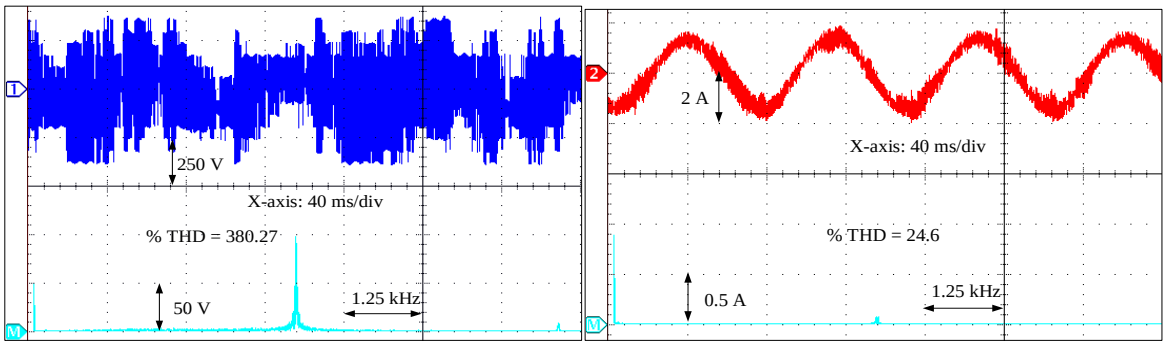


(a)

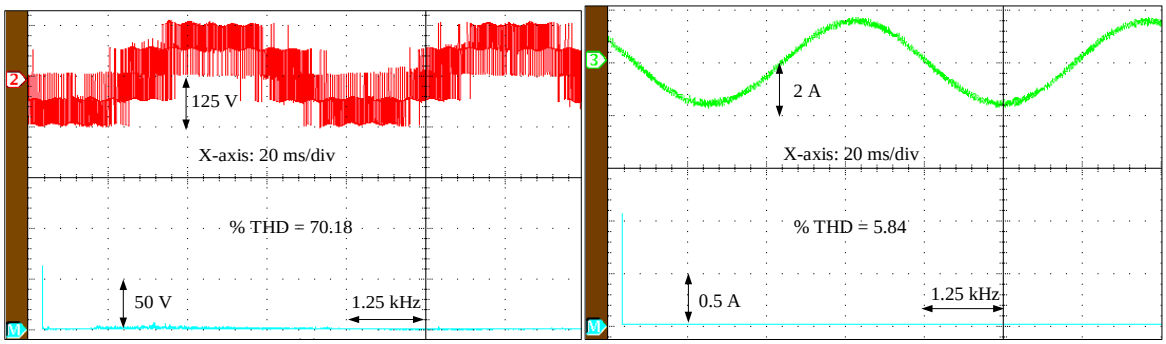


(b)

Fig. 5.7: Simulation results of phase voltage (left) and current (right) at speed of 400 RPM. (a) Conventional PCC (b) Proposed PCC



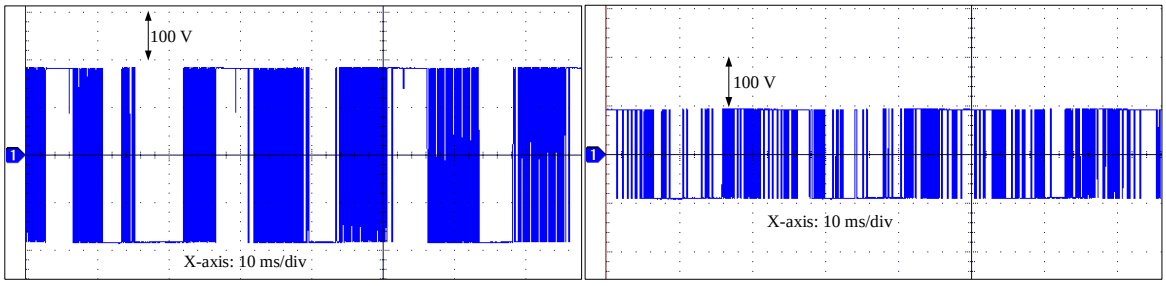
(a)



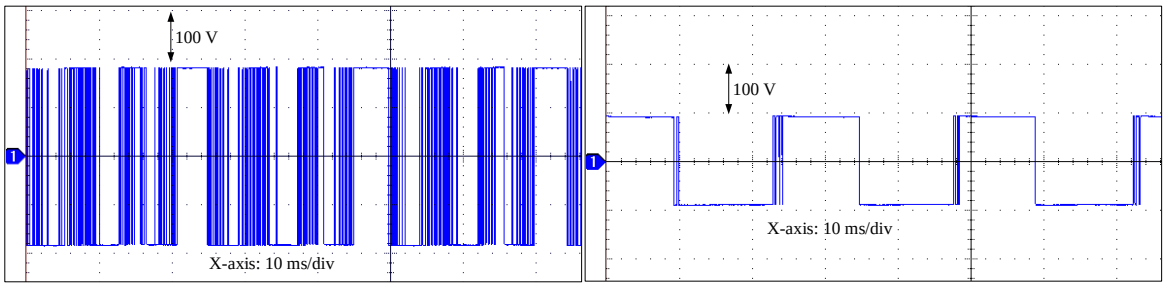
(b)

Fig. 5.8: Experimental phase voltage (left) and current (right) with FFT analysis at speed of 400 RPM. (a) Conventional PCC (b) Proposed PCC

To demonstrate the principle of the proposed PCC technique, the experimentally obtained pole voltage of the inverter-1 and inverter - 2 are shown in Fig. 5.9, at a speed of 1200 RPM. From Fig. 5.9, it can be observed that both of the inverters are switched for the conventional PCC, whereas in the proposed PCC inveter-2 is clamped to the switching state based on the NSHC (Fig. 5.4) and the inverter-1 acts as switching inverter. It can be concluded that with the proposed PCC, there is a reduction in the switching power loss at higher speeds.



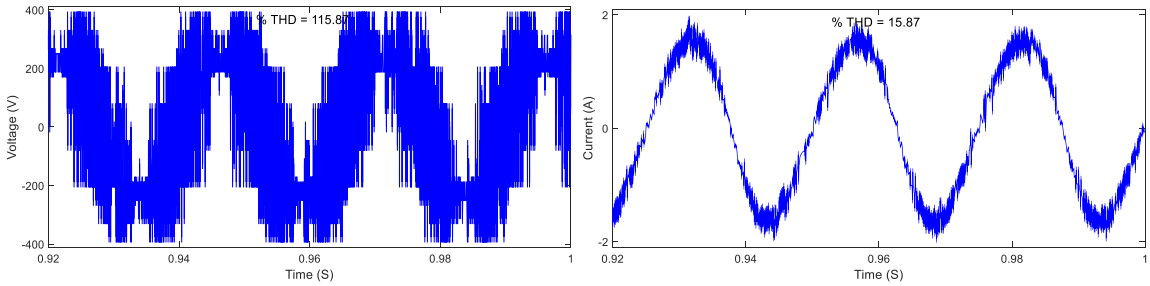
(a)



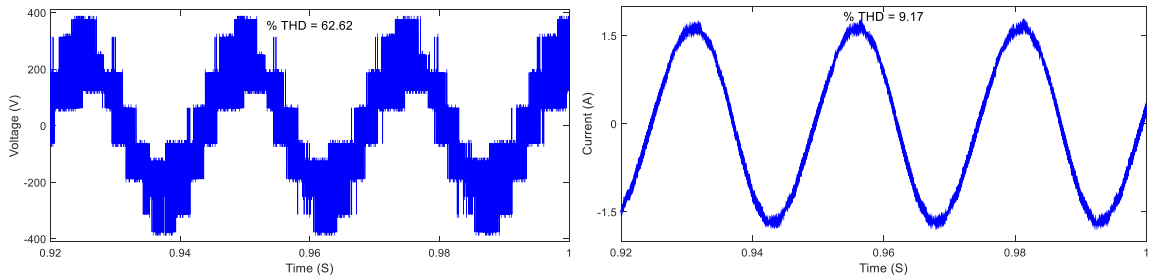
(b)

Fig. 5.9: Experimentally obtained pole voltage of inverter-1 (left) and inverter-2 (right). (a) Conventional PCC (b) Proposed PCC

The simulation and experimental results for the motor phase voltage and current are presented in Fig. 5.10 & 5.11, when the four-level OEWIMD is operated at a speed of 1200 RPM. The experimentally obtained steady state electromagnetic torque for both conventional and proposed PCC are shown in Fig. 5.12, when the four-level OEWIMD is operated at a speed of 1200 RPM.

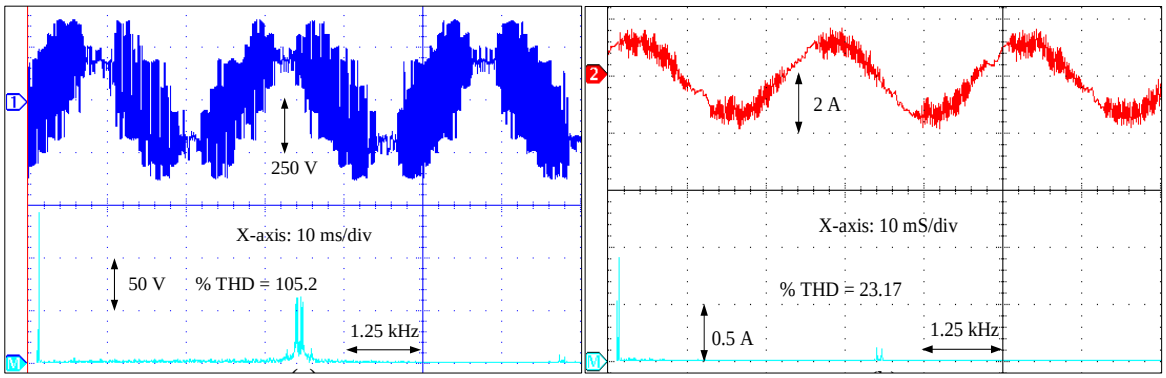


(a)

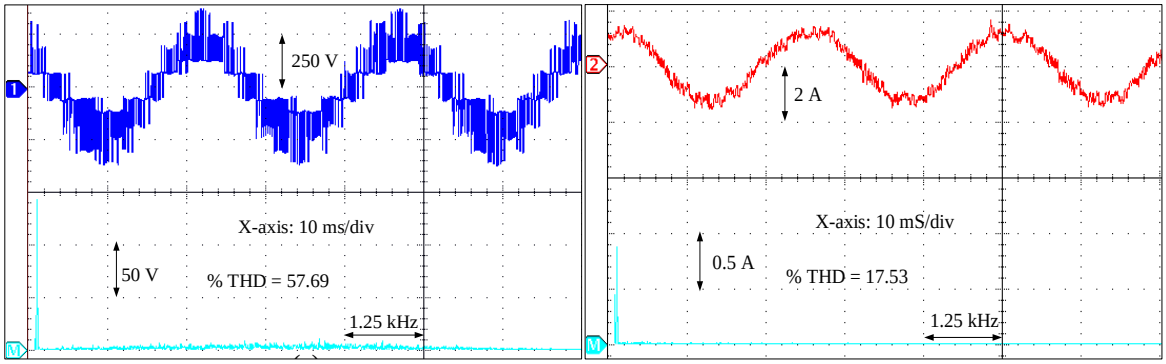


(b)

Fig. 5.10: Simulation results of $v_{aa'}$ (left) and $i_{aa'}$ (right) at a speed of 1200 RPM. (a) Conventional PCC, (b) Proposed PCC



(a)



(b)

Fig. 5.11: Experimental phase voltage (left) and current (right) waveforms with FFT analysis at a speed of 1200 RPM. (a) Conventional PCC, (b) Proposed PCC

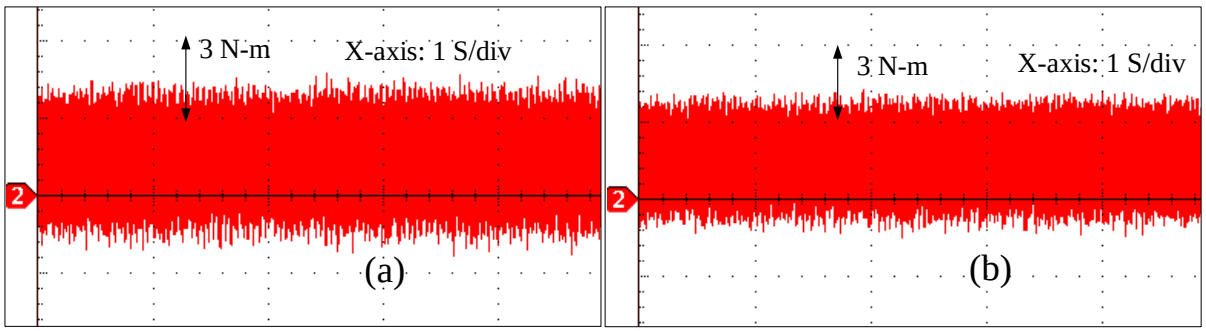


Fig. 5.12: Experimental steady state torque of OEWIMD: (a) Conventional PCC (b) Proposed PCC at a speed of 1200 RPM

From the simulation and the experimental results, it is evident that, the proposed PCC results in a better performance with reduced voltage and current THDs and the torque ripple, compared to the conventional PCC.

Fig. 5.13 presents the magnitudes of the cost function, (i.e. |g|) for the conventional and the proposed PCC, when the four-level OEWIMD is operated at a speed of 1200 RPM. It may be noted that, unlike the conventional PCC, which uses 37 voltage vectors, the proposed PCC uses only 4 vectors to obtain the optimal voltage vector, which minimizes the error between reference and the predicted values of the motor phase current. From this, it can be intuitively reasoned out that the proposed PCC, the burden on the controller is reduced as compared to the conventional PCC.

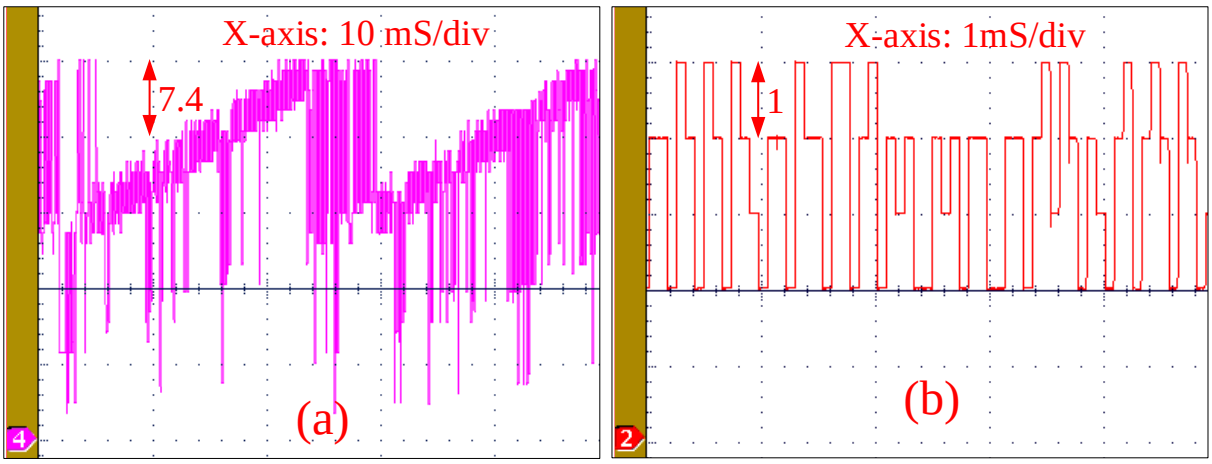


Fig. 5.13: Experimental cost function value at a speed of 1200 RPM: (a) Conventional PCC (b) Proposed PCC

The average execution time for the conventional PCC and for the proposed PCC is shown in Table 5.2. From Table 5.2, the execution time spent for the prediction and optimization of proposed PCC is 22.7 µS and 50.14 µS for the conventional PCC. The burden on the controller is reduced by around 53 % with the proposed PCC as compared to the conventional PCC.

Table 5.2: Computational burden on the controller with sampling time (Ts = 120 µs)

Name of the index	**Execution Time (µS)**	
	Conventional PCC	Proposed PCC
Measurements	11.92	
Rotor flux estimation	14.64	
PI controller & reference generation	14.56	
Prediction and optimization	50.14	22.7
Total	91.26	63.82

The dynamic performance of both of the PCC techniques is assessed during acceleration, during speed reversal and for torque transient of the four-level OEWIMD. The experimentally obtained waveforms, during the acceleration of the OEWIMD, are shown in Fig. 5.14. From results it can be observe that, the controller achieves fast dynamics within in 1 second.

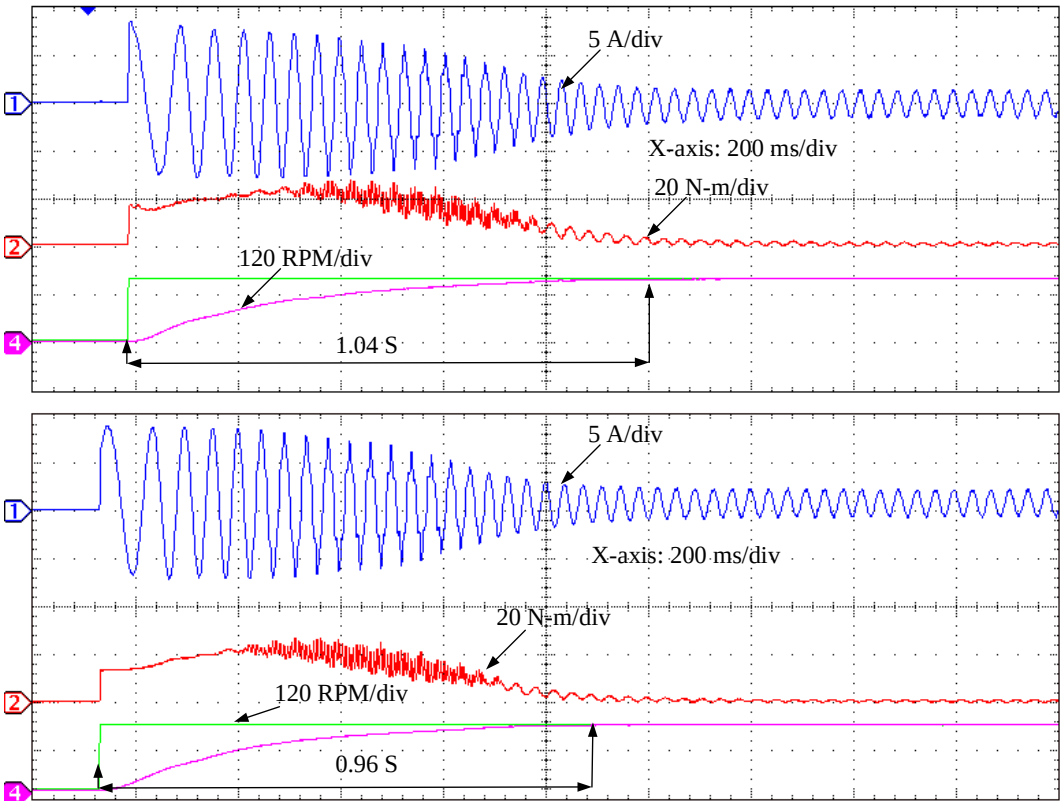


Fig. 5.14: Experimental result of stator current, torque and speed of four-level OEWIMD during acceleration: conventional PCC (top), Proposed PCC (bottom)

A speed reversal operation is performed at a speed of $\pm$1000 RPM without any load torque to investigate the speed transient response of the controller. The experimentally obtained waveforms are shown in Fig. 5.15.

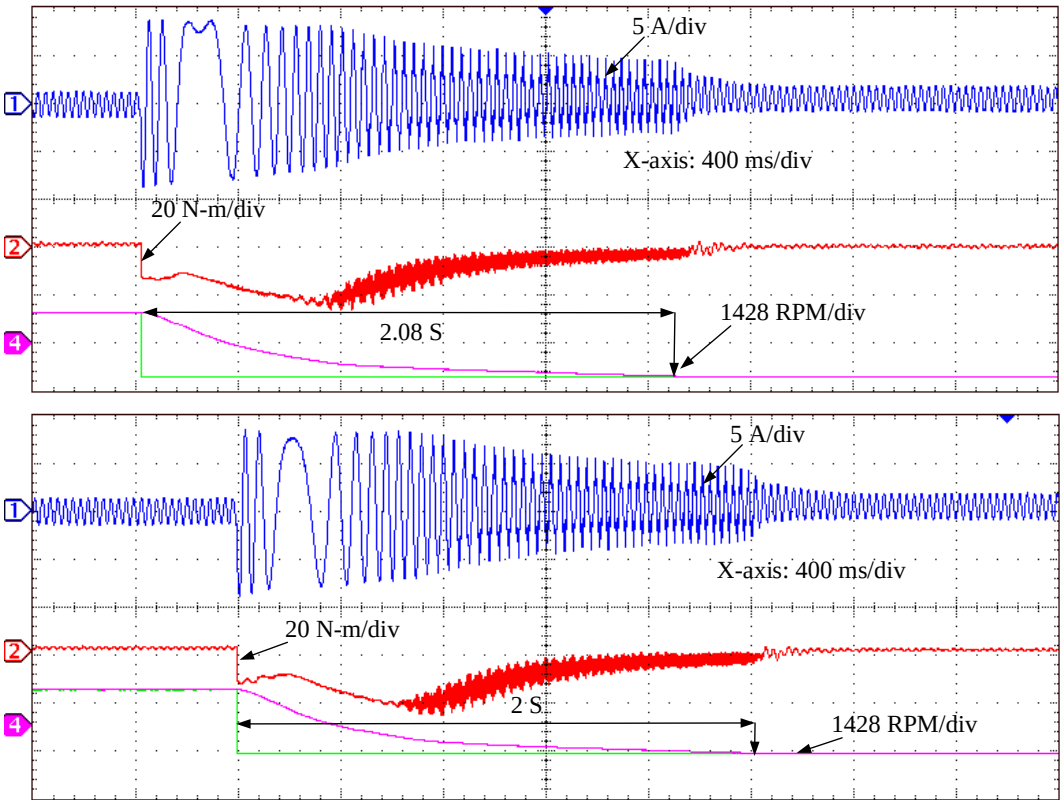


Fig. 5.15: Experimental result of stator current, torque and speed of four-level OEWIMD during speed-reversal: Conventional PCC (top), Proposed PCC (bottom)

The torque transient response is demonstrated by applying a sudden load of 5 N-m with help of dc-generator connected to the shaft of the OEWIMD. The corresponding experimental results are shown in the Fig. 5.16. From Fig. 5.16, it can be observed that, for the same values of PI-controller, the dynamic response of the proposed PCC technique is considerably quicker compared to the conventional PCC.

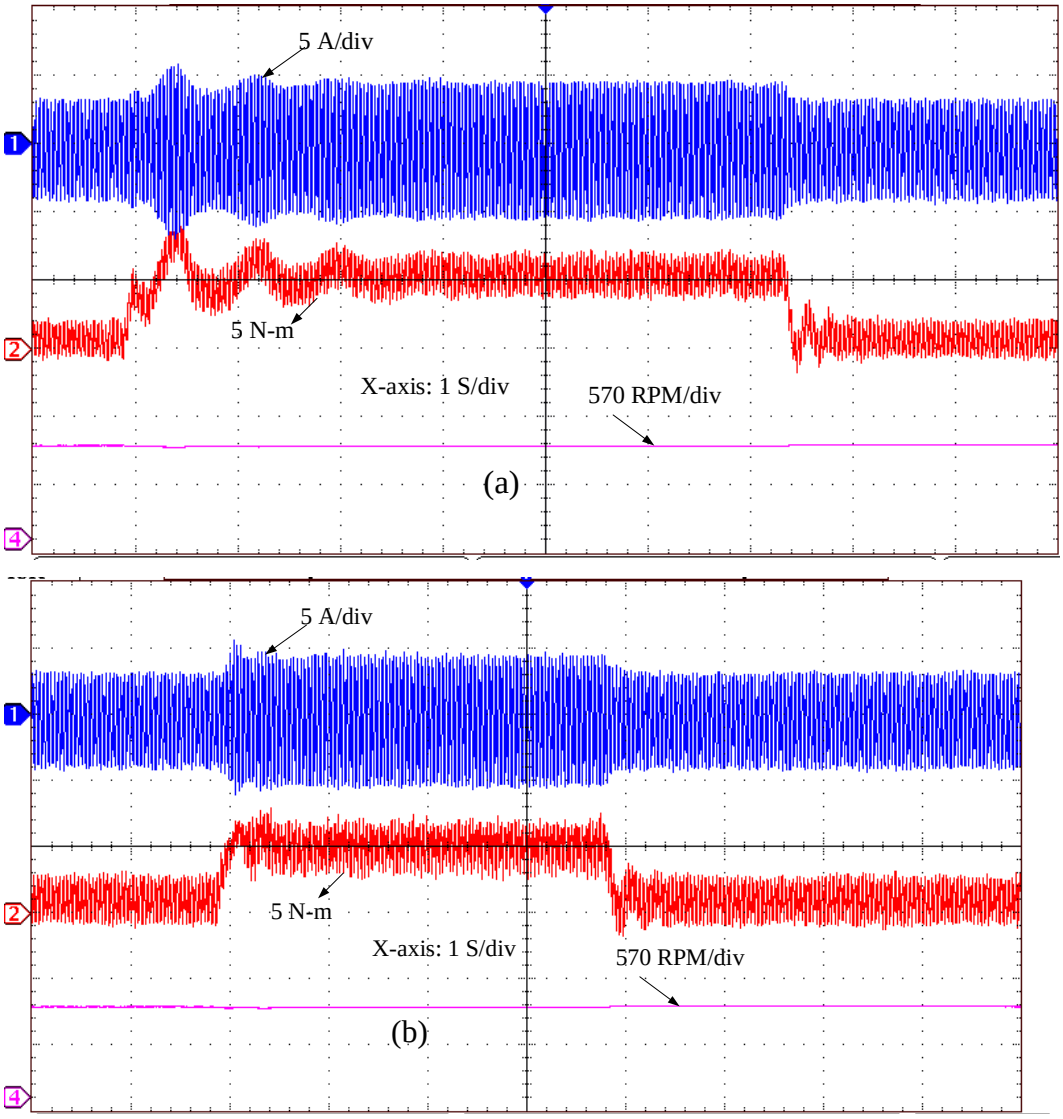
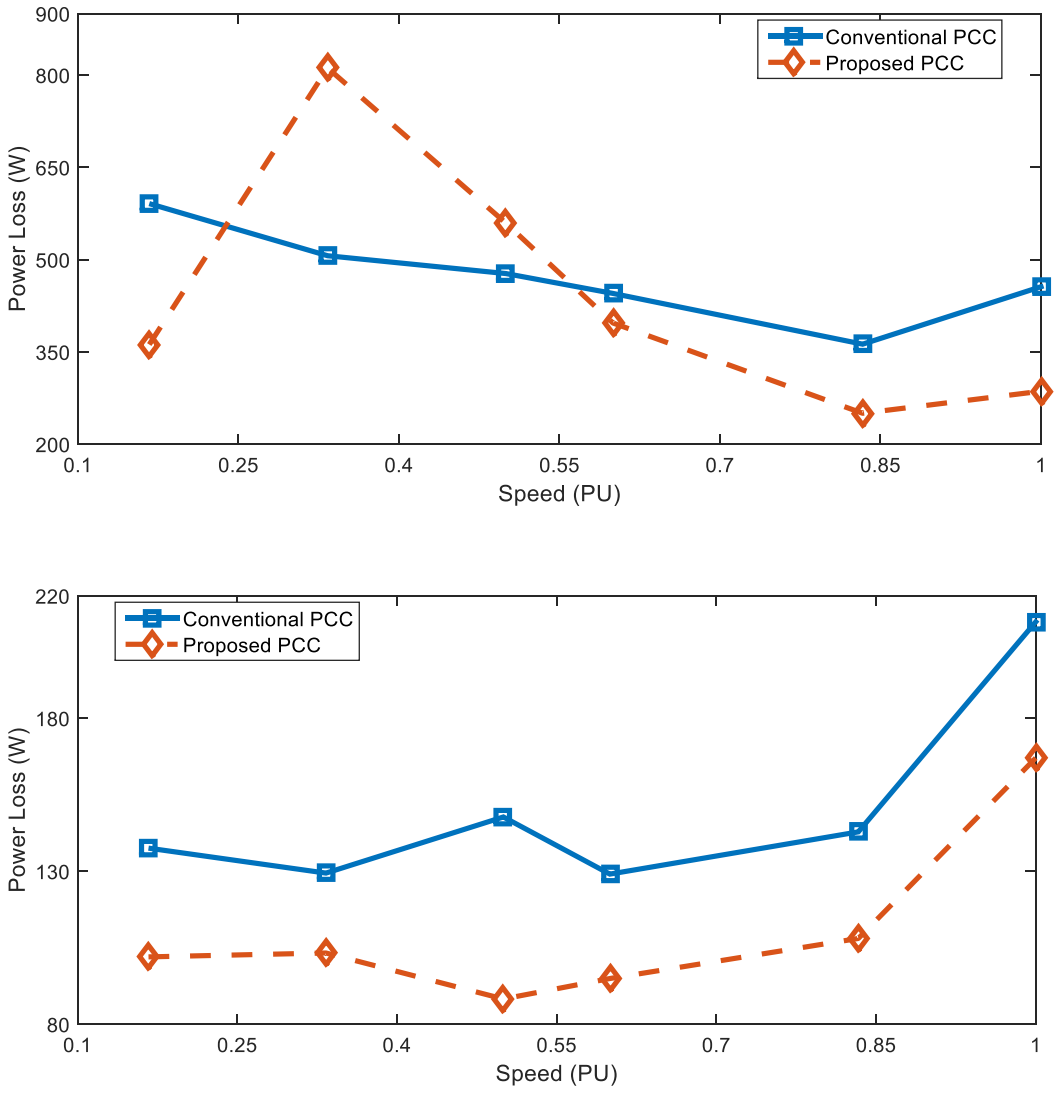


Fig. 5.16:- Experimental torque response of OEWIMD: (a) Conventional PCC (b) Proposed PCC

The total power loss of the OEWIMD system consists of the power losses in the dual-inverter system and the motor. The power loss in the dual-inverter system comprises of the sum of the switching power loss and conduction loss of the power semiconductor switching devices. Further, the ripple in the motor current contributes to the ohmic loss in the motor. All of these losses are evaluated by employing the *loss model*, which was suggested for four-level OEWIMD in the Chapter-2.

In order to make a fair comparison in computation of device losses, the total dc-link voltage is kept at 564 V and the load on the OEWIMD is considered as 80% (i.e. 20 N-m, see Table 5.1).

Fig. 5.17 presents the total power loss incurred in the dual-inverter fed four-level OEWIMD. From Fig. 5.17, it can be observed that, the proposed PCC results in a lower power loss in the lower and higher range of speed. The higher power loss in inverter-1 is attributed to the additional switching of inverter-1 (i.e. the inverter with the higher dc-link voltage) in the mid-speed range.



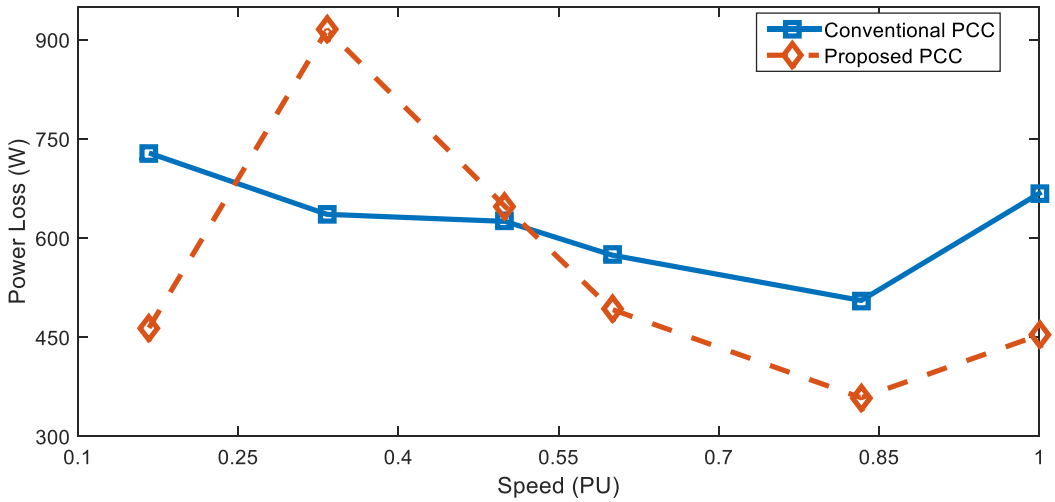


Fig. 5.17: Total power loss of four-level OEWIMD: Dual-inverter loss (top), Ohmic loss (middle), Drive loss (bottom)

5.6 Conclusion

This chapter proposes an improvised PCC for a four-level OEWIMD. The conventional PCC for this drive evaluates all of the available 37 candidate voltage vectors to select the optimal one, which increases the computational burden on the controller. In contrast, the proposed PCC tests only 5 candidate vectors to determine the optimal voltage vector. The proposed algorithm is based on the nearest sub-hexagonal center corresponding to the inverter with lower dc-link voltage and the clamping of that inverter. Thus, with the proposed PCC strategy, the burden on the controller is reduced. The simulated as well as the experimental results indicate that the proposed PCC technique results in a better performance in terms of the voltage THD, current THD and the steady state torque ripple. The switching frequency is also reduced with the proposed PCC as compared to the conventional PCC technique. This advantage manifests as the reduction of overall loss of the four-level OEWIMD system for most of the operating speed range.

Chapter 6

Conclusion and Future work of Research

Contents

6.1 Conclusion

The principal focus of this thesis is to further the knowledge available on the PWM schemes and control strategies pertaining to the four-level Open End Winding Induction Motor Drive (OEWIMD). The thesis consists of five chapters of which, the first is introductory and the rest are contributory in nature.

Chapter-1, having reviewed the earlier literature available in this area, lays down the framework of the thesis. The motivation to embark this research problem and the organization of the thesis are described.

The key contributions of this thesis are subdivided into major and minor contributions and are summarized as follows:

6.1.1 Major Contributions of the Thesis

Chapter-2 presents the modeling of the four-level OEWIM. It is identified that with the existing decoupled PWM schemes, both inverters are switched, which increases the switching power loss in the dual-inverter system. The contribution of Chapter-2 is to reduce the switching power loss by the development of Discontinuous Decoupled PWM (DDPWM) schemes. The other contribution is to suggest unsymmetrical (i.e. non-center spaced) decoupled PWM schemes to derive waveform symmetries from an unsymmetrical power circuit. There are four possibilities to achieve waveform symmetries, which are named as DDPWM-1, DDPWM-2, DDPWM-3 and DDPWM-4. Simulations as well as experimental studies indicate that DDPWM-1 performs better in terms of Voltage THD, WTHD, Switching Power loss and overall dual-inverter loss than DDPWM-2, 3, 4, EDPWM and PDPWM.

In order to reduce the current ripple and the switching power loss, a Biasing PWM scheme is suggested in Chapter-3, wherein the inverter with lower dc-link voltage is clamped and the other inverter is switched around it. The simulation and experimental results reveal

that, the proposed PWM techniques avoids the overcharging phenomenon and reduces the switching power loss compared to all of the DDPWM schemes proposed in Chapter-2.

Chapter-4 contributes a new circuit topology for the four-level OEWIMD, which is operated with unequal dc-link voltages, which are in the ratio of 2:1. The proposed circuit configuration has an inherent mechanism to avoid the overcharging of the lower dc-link voltage capacitor by its counterpart and it requires only two dc-power supplies compared to the nested rectifier-inverter configuration proposed in earlier literature. The proposed circuit configuration exhibits immunity to the internal imbalance of the dc-link voltages of the nested rectifier. A new PWM strategy called the Nested Inverter Clamped Sample Average Zero-Sequence Elimination (NICSAZE) is also proposed to avoid the flow of zero-sequence current in the circuit (in the average sense). The performance of the NICSAZE SVPWM scheme is verified using both simulation and experimental studies.

The four-level OEWIM with unequal dc-link voltages is revisited in chapter-5. The conventional approach for the implementation of PCC for this drive requires the evaluation of all of the available 37 candidate voltage vectors to select the optimal one, which increases the computational burden on the controller. To avoid this, an improvised Predictive Current Control (PCC) technique is proposed. The proposed PCC tests only 5 candidate vectors to determine the optimal voltage vector. The proposed algorithm is based on the concept of the *Nearest Sub-Hexagonal Center* (NHSC) corresponding to the inverter with lower dc-link voltage and the clamping of that inverter. It is shown that, with the proposed PCC strategy, the burden on the controller is reduced. The simulated as well as the experimental results indicate that the proposed PCC technique results in a better performance in terms of the voltage THD, current THD and the steady state torque ripple compared to the implementation with conventional approach. The switching frequency is also reduced with the proposed PCC as compared to the conventional PCC technique. This feature manifests as the reduction in the overall power loss of the four-level OEWIMD system for most of the operating speed range.

6.1.2 Minor Contributions of the Thesis

An improvised loss model was used to assess the switching power loss, conduction power loss and diode conduction power loss with reverse recovery current in the chapters-2, 3, 4 and 5. This model is capable of evaluating the additional power loss incurred in the power semiconductor switching devices due the reverse recovery current in the anti-parallel (feedback) diodes.

6.2 Future scope

Based on the research done in this thesis, the recommendations for the future work are as follows:

6.2.1 Power Circuit Configurations for Open-End Winding Induction Motor Drives:

It could be beneficial to replace the diode bridge rectifiers, which feed the individual inverters of the dual-inverter system, with active front-end converters to regulate the voltage across the dc-link capacitors of inverter-2 with closed loop control strategies. Apart from providing a stiff dc-link voltage for inverter-2 and imparting the regeneration capability, the closed loop control would also improve the input power factors of the respective active front-end converters.

6.2.2 Control strategies for Open-End Winding Induction Motor Drives:

Throughout this thesis, a fixed number of samples are used to synthesize the reference voltage vector. It makes an interesting study to investigate about the applicability of hybrid PWM methods (such as level shifted carrier based PWM techniques, which includes center spaced PWM and bus clamping PWM techniques) to improve the performance of the open-end winding induction motor drive as well as to avoid the overcharging phenomenon of the lower dc-link voltage capacitor.

It’s an interesting proposition to apply heuristic controllers such as fuzzy and neural networks for the power circuit topologies employed in the present thesis. The fuzzy based

DTC techniques, which are employed for the induction motor drive, can be extended to the open-end winding induction motor to improve the steady state performance of the drive.

Throughout this thesis, a fixed number of samples are used to synthesize the reference voltage vector. At lower modulation indices, this would lead to large sampling time periods, which would result in a poor synthesis of the reference voltage vector. To avoid this unwanted phenomenon, one may think of increasing the sampling rate as the modulation index decreases so that the reference vector is constructed with a better resolution, without unduly increasing the switching power loss. Such a loss-budgeted SVPWM technique should carefully be evaluated for its viability as there would be an inevitable tradeoff between the switching power loss and the reduced ripple in the motor current.

Applying the concept of the *Nearest Sub-Hexagonal Center* technique, to the Predictive Torque Control (PTC) could make an interesting study. It could be a rewarding investigation if such a PTC, while eliminating the cumbersome process of selecting the weighting factors (associated with the implementation of conventional PTC), also results in a reduced switching frequency.

Appendix-I

Experimental set-up

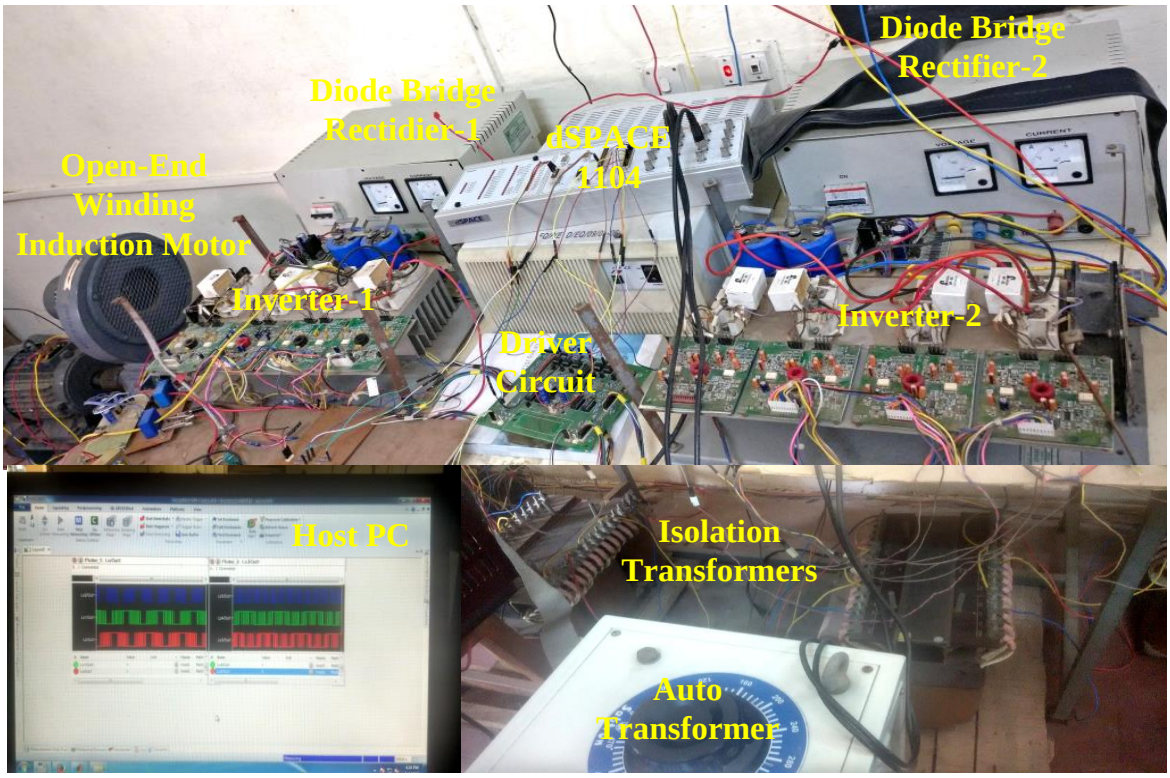


Fig. A.1: A view of experimental set-up of four-level Open-End Winding Induction Motor

Hardware Specifications of the Dual-Inverter system are given in Table A1.

Table A1: Hardware specifications of the dual-inverter system

AC input voltage	415 V
DC-link voltage	650 V
AC output Voltage	3-phase, 480 V
AC output current	30 A
Fundamental Frequency	50 Hz
IGBT module	SKM 150GB12T4
Diode Bridge module	SKD 160/18
IGBT drivers	SKHI 22BR
DC-link Capacitors (2 Numbers)	4700 µF, 450 V

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List of publications

Accepted papers in Referred Journals:

1. S. Lakhimsetty, N. Surulivel and V. T. Somasekhar, "Improvised SVPWM Strategies for an Enhanced Performance for a Four-Level Open-End Winding Induction Motor Drive," in *IEEE Transactions on Industrial Electronics*, vol. 64, no. 4, pp. 2750-2759, April 2017.

2. S. Lakhimsetty and V. T. Somasekhar, "Discontinuous decoupled SVPWM schemes for a four-level open-end winding induction motor drive with waveform symmetries," in *IET Power Electronics*, vol. 11, no. 2, pp. 280-292, 20 2 2018.

3. S. Lakhimsetty and V. T. Somasekhar, "A Four-Level Open-End Winding Induction Motor Drive With a Nested Rectifier–Inverter Combination With Two DC Power Supplies," in *IEEE Transactions on Power Electronics*, vol. 34, no. 9, pp. 8894-8904, Sept. 2019.

4. S. Lakhimsetty and V. T. Somasekhar, "An Efficient Predictive Current Control Strategy for a Four-Level Open-End Winding Induction Motor Drive," in *IEEE Transactions on Power Electronics* (Early Access). DOI: 10.1109/TPEL.2019.2954864.