POWER QUALITY ENHANCEMENT BY DSTATCOM WITH IMPROVED PERFORMANCE

A THESIS

submitted by

HAREESH MYNENI

for the award of the degree

of

DOCTOR OF PHILOSOPHY

DEPARTMENT OF ELECTRICAL ENGINEERING
NATIONAL INSTITUTE OF TECHNOLOGY WARANGAL
MARCH 2019

THESIS CERTIFICATE

This is to certify that the thesis titled **"POWER QUALITY ENHANCEMENT BY DSTATCOM WITH IMPROVED PERFORMANCE"**, submitted by **Mr. Hareesh Myneni**, to the National Institute of Technology, Warangal, for the award of the degree of **Doctor of Philosophy**, is a bonafide record of the research work done by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

Dr. G. Siva Kumar
Supervisor
Assistant Professor
Dept. of Electrical Engineering
NIT-Warangal, 506004

Place: Warangal

Date: December 16, 2019

ACKNOWLEDGEMENT

I would like to express my deep gratitude towards **Dr. G. Siva Kumar**, Assistant Professor, Electrical Engineering Department for his excellent guidance, support and constant reviewing throughout the course of research work. The interactions with him ensured right direction of this work and helped in completion of the thesis.

I am also thankful to **Prof. S Srinivasa Rao**, **Prof. N. Vishwanathan** and **Prof. V. T. Somasekhar**., Heads of the Electrical Department during the period of research. I am sincerely grateful to **Prof. M Sydulu**, **Dr. D Sreenivasarao** and **Prof. D. Dinakar** who assessed my work and encouraged me as the members of my doctoral scrutiny committee. I would also like to thank **Dr. M. Raja Vishwanathan**, Assistant Professor, Department of Humanities & Social Science for the proof reading of thesis.

I wish to express my sincere thanks to **Prof. N.V. Ramana Rao**, Director, NIT Warangal for his official support and encouragement.

My sincere thanks to my colleagues especially Mr. Pranay, Mr. Rathna Rahul, Dr. Ramanjaneya Reddy, Dr. Kiran, Dr. Kasi Rama Krishna Reddy, Mr. Praveen, Mr. Suresh, Mr. Venu Sonti, Dr. Vijay Babu K, Mr. Chinna K, Mr. M Santhose, Mr. O V S R Vara Prasad, Mr. S Viveka Naidu (M,Tech), Mr. C. Amarnath (M,Tech) for answering all the questions whenever I was in need.

I also appreciate the encouragement from teaching, non-teaching members, and fraternity of Department of Electrical Engineering of NIT Warangal.

I also acknowledge my sincere gratitude to the Ministry of Human Resources Development (MHRD), Government of India for their financial support to carry out this research.

My heartily gratitude to my parents Shri. M Venkateswararao & Smt. M Suchitra, my sister Smt. M Purnima, my brother-in-law Shri. M Srinivas, my son-in-law M Sravan my relatives and my well wishers for their support. Finally, I wish to express my utmost gratitude to my wife M Lakshmi for her support and encouragement throughout my

research work. My deep love to my son, M Sri Charan for bearing the long hours of my absence.

Above all, I thank the almighty for giving me this learning opportunity and blessing me to finish my work successfully.

Hareesh Myneni.

ABSTRACT

KEYWORDS: Distribution Static Compensator (DSTATCOM); distribution system; energy management; harmonics; *LCL*-filter; power quality; reactive power; solar photo-voltaic; switching losses; voltage source converter; voltage stress.

In present day, major power consumption loads on distribution system have been reactive in nature, such as fans, pumps, motor drives and power electronic converters. The excessive reactive power consumption results of low power factor and poor voltage regulation and which reduces the active power flow capability in the distribution system. Moreover, the proliferation of power electronic devices in the distribution system worsens the operating conditions and leads to power quality problems. The major power quality issues in the three-phase distribution system are current harmonics, voltage harmonics, reactive power consumption, load unbalancing and excessive neutral current. Harmonic regulation guidelines such as IEEE 519-1992 and IEC 61000 are applied to limit the current and voltage harmonic levels. To satisfy these guidelines, the harmonics must be mitigated by using harmonic filters. Passive and active filters are used either together to form hybrid filters or on an individual basis to mitigate harmonics. In recent years, with the advent of sophisticated electrical and electronic equipment, Power Quality (PQ) has become an issue of concern and extensive research is being done to improve power quality.

A promising group of solutions that deals with power quality problems in the distribution system are Custom Power Devices (CPDs). The family of CPDs includes Distribution Static Compensator (DSTATCOM), Dynamic Voltage Restorer (DVR) and Unified Power Quality Conditioner (UPQC) which are used for compensating power quality problems. Among these members, DSTATCOM is a shunt connected device, which mitigates current related power quality problems. In this thesis, an attempt has been made to develop a split-capacitor DSTATCOM for power quality improvement in three-phase four-wire (3P4W) distribution system.

It is well known that high performance and cost-effective converter are a prerequisite for the realization of DSTATCOM. These converters can be broadly categorized into two classes, namely, Voltage Source Converter (VSC) and Current Source Converter (CSC). The discussion about the performance of the VSC and CSC as a power circuit of DSTATCOM is beyond the scope of this thesis. In the present work, VSC has been considered as a power circuit for DSTATCOM as it has higher market penetration and more noticeable development over the last decades, in comparison to CSC topologies.

In the present work, DSTATCOM has been used to mitigate harmonics, reactive power compensation and balancing of three-phase source currents. A new methodology is proposed to improve the performance of DSTATCOM with more appropriate design of dc-link voltage. For that, a reference dc-link voltage is derived based on the load operating point. With this approach, the switch voltage stress and switching losses are reduced when compared to conventional fixed dc-link voltage method. The switching losses in the proposed method are calculated and are compared with conventional fixed dc-link voltage method. The proposed variable dc-link voltage method is validated by simulation and experimental studies.

An attempt has been made to reduce the required value of interfacing inductance in DSTATCOM applications, since it makes the system bulky and expensive. For that an *LCL*-filter based DSTATCOM is implemented based on switching dynamics, which improves DSTATCOM performance. In addition to current control, the application of *LCL*-DSTATCOM has been extended to voltage control intended for voltage regulation at PCC. The proposed method is validated by simulation and experimental studies.

The method which is available in the literature to reduce the rating of VSC is a *LC*-filter based DSTATCOM topology. In which, an ac-capacitor is connected in series with the interfacing inductor. The series ac-capacitor supports the inverter voltage such that the dc-link voltage requirement is reduced. The amount of dc-link voltage required depends on series ac-capacitor voltage, which indeed depends on the current flowing through the capacitor. In existing methods, the dc-link voltage is fixed even through ac-capacitor voltage is varied, which leads to more voltage drop across interfacing inductor, results in degrading the performance of DSTATCOM. A new methodology is proposed, in which the dc-link voltage requirement corresponding to ac-capacitor voltage support is calculated and it has been maintained, such that the performance is improved.

An attempt has been made to integrate Solar Photo-voltaic (SPV) to grid by DSTATCOM. In general, the SPV is integrated with grid through a DC-DC converter and VSC, which is named as two-stage conversion. In view of efficiency of system, the single-stage conversion becomes more popular and in which Maximum Power Point Tracking (MPPT) of SPV and real power injection are achieved with VSC alone. But, if single-stage conversion system consists of Battery Energy Storage (BES) on dc-side of VSC, then to achieve simultaneous operation of MPPT and real power injection, a co-ordination control is required. In the proposed single-stage grid connected SPV and BES system a co-ordinate control is implemented along with energy management. In this method, the algorithm coordinates VSC and BES system based on the State of Charge (SoC) of the battery and available SPV power so that MPPT and power injection are achieved simultaneously. The proposed method not only injects real power, but also compensates reactive power and mitigate harmonics. Further, an active rectification operation during non-SPV hours is achieved. The multi-functional features of the proposed method are explained using simulation studies and are also validated through experimental studies.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

ABBREVIATIONS

AC	Alternating Current
APF	Active Power Filter
CPD	Custom Power Device
DC	Direct Current
DSTATCOM	Distribution Static Compensator
DVR	Dynamic Voltage Restorer
IEEE	Institute of Electrical and Electronics Engineers
IEC	International Electrotechnical Commission
IGBT	Insulated Gate Bipolar Transistor
PCC	Point of Common Coupling
PI	Proportional Integral
PQ	Power Quality
PWM	Pulse Width Modulation
rms	root mean square
THD	Total Harmonic Distortion
TDD	Total Demand Distortion
VA	Volt-Ampere
VSC	Voltage Source Converter
CSC	Current Source Converter
CCM	Current Control Mode
VCM	Voltage Control Mode
SOGI	Second Order Generalized Integrator
HC	Hysteresis Controller
UCC	Unit Capacitor Constant
ISC	Instantaneous Symmetrical Component
IRT	Instantaneous Reactive Power
SRF	Synchronous Reference Frame
3P4W	Three-phase Four-wire

3P3W	Three-phase Three-wire
SPV	Solar Photo-voltaic
MPPT	Maximum Power Point Tracking
BES	Battery Energy Storage
SoC	Stage of Charge
P&O	Perturb and Observe
PLL	Phase Locked Loop

NOTATIONS

v_s	Instantaneous source voltage
i_s	Instantaneous source current
i_l	Instantaneous load current
i_f	Instantaneous filter or DSTATCOM current
i_{ln}	Instantaneous load neutral current
i_{sn}	Instantaneous source side neutral current
v_p	Instantaneous voltage at PCC
R_s	Equivalent resistance of feeder
L_s	Equivalent inductance of feeder
L_f	Interfacing inductance
C_{dc}	DC-link capacitance
P_s	Source real power
Q_s	Source reactive power
P_l	Load real power
Q_l	Load reactive power
P_f	DSTATCOM real power
Q_f	DSTATCOM reactive power
I_s	rms source current
I_l	rms load current
I_f	rms filter current
m_a	Amplitude modulation index
$Q_{f,max}$	Maximum DSTATCOM reactive power
$I_{f,max}$	Maximum filter current
Q_f^*	Reference DSTATCOM reactive power
V_{dc}^*, $V_{dc,ref}$	Reference dc-link voltage
I_f^*	Reference rms filter current
f_{sw}	Switching frequency
E_{sw}	Energy dissipation in switch

P_{sw}	Switching losses
T_j	Junction temperature of switch
$I_{f,n}$	Nominal rms filter current
$V_{dc,n}$	Nominal dc-link voltage
$T_{j,n}$	Nominal junction temperature of switch
k_i	Current dependency factor of IGBT
k_v	Voltage dependency factor of IGBT
TC_{sw}	Temperature co-efficient of switching losses
r_d	Damping resistance
C_r	Resonance capacitance
i_{cr}	Instantaneous current through resonance capacitor
C_f	Series ac-capacitance
L_{fi}	Converter side inductance
L_{fg}	Grid side inductance
h	Hysteresis band
P_{lavg}	Average real or active power of load
i_p	Active current component of load
i_q	Reactive current component of load
v_{inv}	Instantaneous inverter or converter ac side voltage
f	Fundamental supply frequency
ω	Fundamental frequency of the supply voltage in rad/s
θ	Angle between voltage and current

CHAPTER 1

INTRODUCTION

This chapter introduces the research work. It starts with a brief background to foremost power quality problems in distribution system. Then, the solutions to the power quality problems have been discussed, through which DSTATCOM is selected as a compensator in distribution system. Next, motivations, objectives, and organization of thesis are explained.

1.1 General Overview

In alternating current (AC) power system, the term Power Quality (PQ) is used to estimate and maintain the quality of power at the level of generation, transmission, distribution, and utilization. The quality of power is quantified in terms of voltage, current and frequency deviation of the supply system. Typically, voltage related power quality problems at the point of common coupling (PCC) consist of voltage sag, swell, harmonics, surge, fluctuations, notches, voltage unbalance, glitches, spikes, flickers, outages, and so on, while current related PQ problems are poor power factor, current unbalance, an excessive neutral current due to unbalance, and harmonic currents generated by non-linear loads. Some of the reasons for power quality problems in AC power system are summarized below.

- Operation of non-linear loads such as adjustable speed drives (ASDs), uninterrupted power supplies (UPSs), switched mode power supplies, arc furnaces, high efficiency lighting.
- Natural reasons include flashover, lightning phenomena, fault conditions, and failure of electrical equipment (e.g. electrical cables and transformers).
- Unequal distribution of all single-phase loads among the three-phases of distribution system.

- Energization of large capacitor banks and transformers.
- Frequent switching or start and stop of large loads such as electric motors and oscillating loads.

Due to power quality issues, the following problems occur in AC distribution power system:

- Increased losses in the distribution system
- Excessive current due to resonance
- Negative sequence currents in generators and motors
- Failure of capacitor banks
- Overheating of cables and transformers
- Interference with communication systems
- Relay and breaker malfunctions due to signal interference, false metering, interferences with the motor controllers and digital controllers
- Dielectric breakdown, noise and vibrations.

The severity of PQ problems is much more at the utilization level, therefore the study of PQ becomes an important area in electrical engineering, especially in distribution system. These power quality problems become more serious with the use of solid-state devices, which cannot be dispensed due to the benefits of size reduction, ease of control, and other reduced maintenance requirements in modern electric equipment. However, the adverse effects of power quality issues in terms of cost is very high in distribution system [1]–[3]. Therefore, it has created a great challenge to both manufacturers and the electric utilities. The manufacturers must develop electric equipment, which must be immune to or override the power quality disturbances and the utilities must supply good quality power to consumers for satisfactory operation of their equipment. For completeness, the current related power quality problems, such as reactive power burden, current harmonics and excessive neutral current are briefly discussed below.

1.1.1 High reactive power demand

In distribution system, some loads demand high reactive power for successful operation. When enough reactive power is not available in the system, it is not possible to transfer the real power demanded by the loads through feeder lines [4]. Some of the loads, which demand high reactive power in distribution system are:

- Phase-controlled rectifiers
- Motors
- Transformers, tap-changing transformers
- Choke inductors of loads

Due to high reactive power demand, the following problems are associated in the distribution system.

- Losses will be more in the distribution system
- Low efficiency owing to more losses
- Low power factor and poor voltage regulation

1.1.2 Effect of current harmonics

Harmonics are basically the additional frequency components present in the fundamental voltage or current and which are integral multiples of the fundamental frequency. Harmonics are produced by operating non-linear loads in the distribution system. Some sources of harmonics are rectifiers, cycloconverters, ac voltage controllers, adjustable speed drives, soft starters, electronic ballast for discharge lamps, switched-mode power supplies and HVDC transmission. The harmonic distortions change the sinusoidal nature of the ac current, and results in disruption in the ac distribution power system. It causes interference with communication system, damages capacitors, and causes malfunction of other electrical and electronic equipments connected to the same system [5], [6]. The maximum acceptable values of harmonic contamination are specified in Institute of Electrical and Electronics Engineers (IEEE) standard in terms of total harmonic distortion (THD) and Total Demand Distortion (TDD).

1.1.3 Effect of excess neutral current

In many residential and office buildings, power is supplied from a three-phase four-wire (3P4W) distribution system [7]. The unequal distribution of single-phase loads among three-phases create unbalance in the system and results of excessive neutral current flow. The equipment, which produce neutral currents are switched-mode power supplies, such as PCs, printers, photocopiers, and any triplets generator [8]. Neutral current seriously affects the neutral conductor temperature and overloading of distribution feeders and transformers. Some temporary solutions for handling excess neutral current are, 1) over sizing the neutral conductor, 2) derating of distribution feeders and transformers and 3) providing separate neutral conductor.

Due to the above discussed power quality problems, there are distortions and deviations in the various electrical quantities, such as voltage, current and power factor. To limit the level of deviation and distortion, several standards have been developed, recommended, and enforced depending upon the evolution of technology to maintain and quantify the level of power quality.

1.2 Power Quality Standards

Power quality problems affect customers in many ways, such as equipment failure, economic penalty due to power loss, interruption in the process, malfunction of equipment and loss of production. In view of these facts, various terms and definitions are used to quantify the power quality problems in terms of different performance indices. Moreover, various organizations at national and international levels have been working closely with engineers, equipment manufactures, and research organizations to come up with standards governing guide lines, recommended practices, and harmonic limits [6]. The primary objective of the standards is to provide a common ground for all the parties involved to work together to ensure compatibility between the end-user equipments and the supply system. The most commonly used harmonic standards are IEEE-519-1992 [9], International Electrotechnical Commission standard IEC-61000 [10] and European standard EN-50160. IEEE-519-1992 standard limits the amount of current harmonics injected by a user at the Point of Common Coupling (PCC) [9]. For example, the IEEE-519-1992 standard recommends a limit of 5% Total Harmonic Distortion

(THD) in the current at the PCC in a weak system.

1.3 Solution for Power Quality Problems

Electricity consumers are affected in many ways due to low quality power. This causes damage to the equipment or appliances connected to the system, loss of production and sometimes may also be detrimental to human health. Therefore, it is very important to maintain good power quality in the distribution system. Researchers all over the world have worked for decades and provided solutions for power quality problems. In earlier, passive filters are used as solution for PQ problems in distribution system. But, in general, the operating load in distribution system changes frequently, during which passive elements do not respond correctly. In recent years, due to easy control and reduced cost of semiconductor devices, power electronic converters are an affordable solution for power quality problems.

1.3.1 Passive power filters

Passive power filters consist of inductors, capacitors, and resistors, and they are classified into passive tuned filters and high pass filters. The power quality problems can be resolved to some extent by using passive power filters [11]. Depending on the type of connection with load, passive power filters are categorized as shunt and series passive filters. In case of shunt passive filter, the filter is connected in parallel with the load, which is traditionally used to bypass current harmonics in distribution systems [12]. Shunt passive filters provide low impedance path to divert current harmonics to ground such that, it is not allowed into the distribution system. The disadvantages of using passive filter are that they are tuned for a particular harmonic elimination, bulky in size and have resonance problem [12], [13]. There are different types of shunt passive filters are available [14], but the most commonly used passive tuned filters are: single-tuned and double tuned, while high pass filters are: first order, second order and third order filter. The tuned filters and high pass filters are shown in Fig. 1.1 and Fig. 1.2, respectively.

In earlier, passive filters have been used in power system, because of the following advantages [12]:

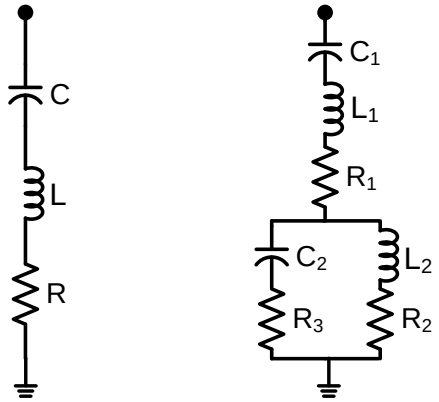


Fig. 1.1 Passive tuned filters: (a) single-tunned and (b) double tunned

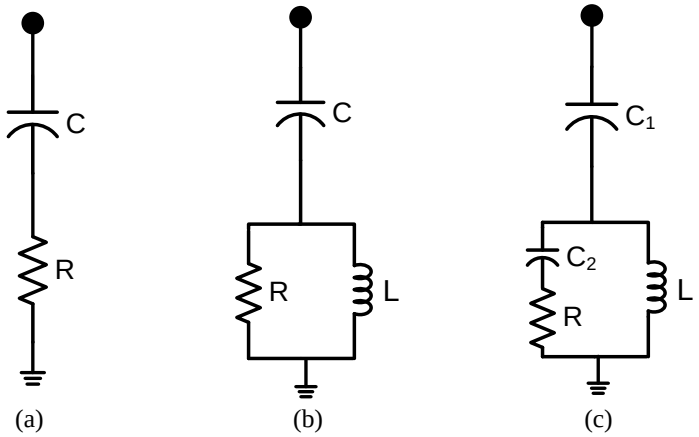


Fig. 1.2 Passive high pass filters: (a) first order (b) second order and (c) third order

1. Simple to implement and almost maintenance free.
2. High efficiency due to absence of switching and conduction losses.
3. Supporting voltage on critical buses and reactive power compensation.

However, passive filters have many disadvantages, which are mentioned below [14]:

1. The size of the passive filter is bulky and it is also expensive.
2. Passive filters do not support dynamic condition in the power system.
3. The resonance between system and passive filter components may damage the equipment because of amplification of current or voltage at resonance condition.

The disadvantages with the passive filters as compensator has encouraged the development of power electronic devices based compensator, which is commonly referred to as Active Power Filters (APF) [14]–[17].

1.3.2 Active power filters

The active power filters are classified into series active power filters and shunt active power filters with respect to the circuit configuration [14]–[16]. Out of these two configurations, shunt active power filter is used for current related power quality problems and its circuit is shown in Fig. 1.3. Still, the Active Power Filter (APF) technology has been under research for providing solutions for power quality problems, such as reactive power compensation, mitigation of harmonics, and neutral current minimization [14]–[17]. In starting stages, the APFs are fabricated by using Bipolar Junction Transistor (BJTs), thyristors, power MOSFETs, Gate Turn-off thyristors (GTOs) and Static Induction Thyristors (SITs). Later, with introduction of Insulated Gate Bipolar Transistors (IGBTs), the APF technology got a real boom for many applications. An important factor for promoting APF technology is the advent of solid state devices of fast self-commutating nature.

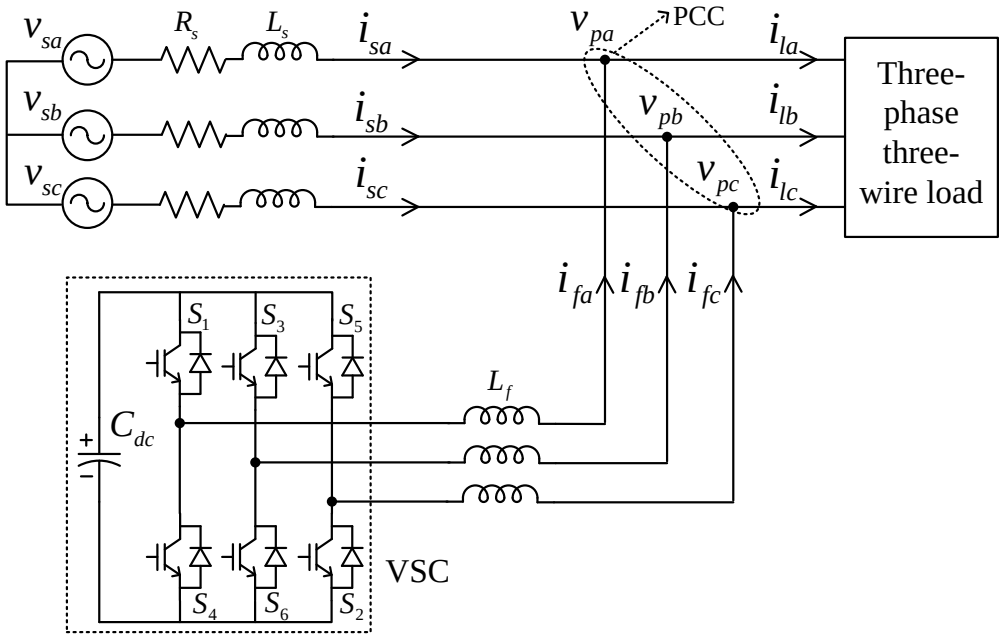


Fig. 1.3 Shunt active power filter in three-phase three-wire distribution system

1.3.3 Hybrid power filters

The combination of passive and active power filters is termed as hybrid power filters. Out of several possible combinations, a typical combination of shunt passive filter and shunt active filter topology is shown in Fig. 1.4. Hybrid power filters improve the

compensation characteristics of passive filters, and allow the use of relatively low rating active power filters in high-power applications at a relatively low cost. Moreover, compensation characteristics of already installed passive filters can be significantly improved by installing an active power filter at its terminals, giving more flexibility to the compensation scheme [13], [18]–[20].

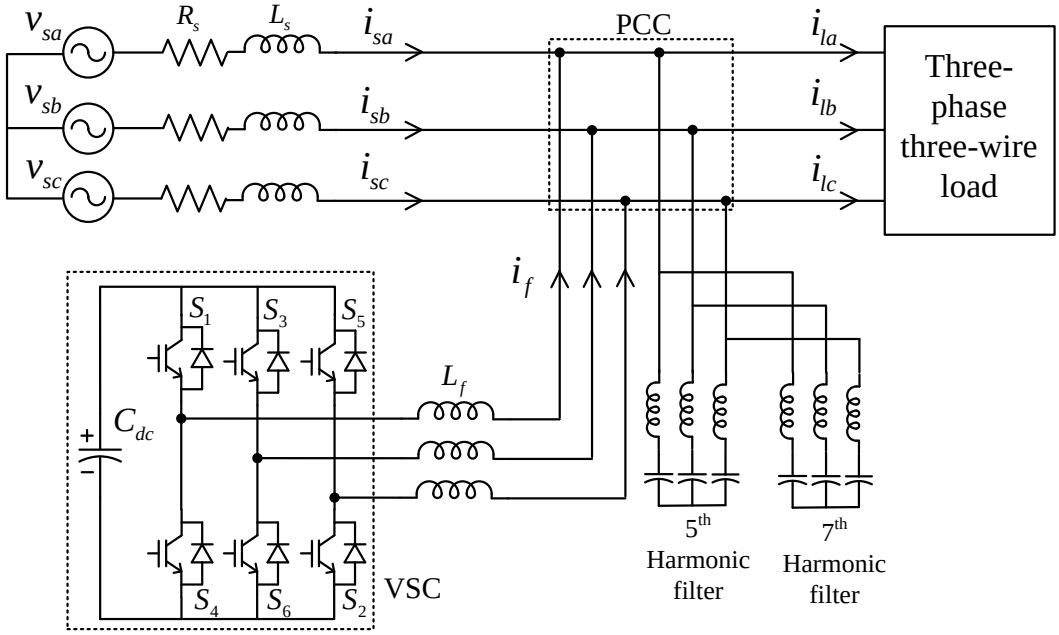


Fig. 1.4 Hybrid power filter with combination of shunt passive and shunt active power filters

The above discussed conventional power quality mitigation equipments (passive filters, active power filters and hybrid power filters) do not provide an adequate solution for an increasing number of applications in distribution system. This fact has attracted the attention of electrical engineers to develop dynamic and adjustable solutions to power quality problems. One modern and very promising group that deals with load current and supply voltage imperfections is Custom Power Devices (CPDs) [21], which are discussed in the next chapter.

1.4 Motivation

Custom power devices solve most of the power quality problems in distribution system because of their versatile functions, and also cost effective. Among CPDs, DSTATCOM is connected in shunt with load to solve current related PQ issues in distribution system

[22]–[28]. DSTATCOM consists of a voltage source converter (VSC) supported by dc-link capacitor voltage and interfacing inductor. Based on literature review on different DSTATCOM topologies, the following observations are made.

1. In existing DSTATCOMs, the required dc-link voltage magnitude is selected from a rated load condition and maintained for all load operating conditions. Due to this, the switching devices of voltage source converter are subjected to more voltage stress under reduced load condition. A continuous high voltage stress across switching devices reduces the life span of switches. The switching losses in voltage source converter depends on dc-link voltage, which appears across switch and current passing through switch. As the dc-link voltage is high during reduced load condition, the switching losses are high in conventional fixed dc-link voltage methods.

2. In a general circuit of DSTATCOMs, the VSC is connected to PCC through the interfacing unit, which consists of high value of inductance (L-filter), which is expensive and bulky. The DSTATCOM with LCL-filter as an interfacing unit consists of low value of inductance, but it requires a proper design, which is a crucial and sensitive task in power quality applications. Because, the DSTATCOM is ideally designed to operate within the possible wide frequency bandwidth of the load.

3. The rating of VSC in DSTATCOM depends on dc-link voltage and filter current injected by compensator. In case of more reactive power compensation, the required rating of VSC is high, which increases the system cost. Therefore, a proper selection of hybrid DSTATCOM topology is necessary to reduce the rating of VSC, and which in turn reduces the required dc-link voltage. As the dc-link voltage is reduced, the device voltage stress and switching losses are reduced.

4. DSTATCOM can be used for multi-functional applications, such as solar PV power injection to grid, power quality improvement and active rectification operation. In solar PV applications with DSTATCOM, the reliable and efficient operation is considerable in low power applications. To improve the efficiency,

conversion stages need to be reduced and for energy management, battery energy storage system is required. In reduced conversion stages method (single-stage), the MPPT operation and power injection to grid along with battery charging or discharging are not achieved simultaneously.

From the above discussions, there is an adequate scope for further research in the area of development of DSTATCOM in the distribution system.

The proposed research work focuses on the enhancement of DSTATCOM performance for power quality improvement in the distribution system. It aims to reduce the switching losses and switching voltage stress in along with the reactive power compensation and harmonics mitigation. Also, it aims to reduce the interfacing inductance without compromising DSTATCOM performance. The multi-functional capability of DSTATCOM for real power injection to grid is implemented for the energy management scheme.

1.5 Objectives

This research is focused on improvisation of DSTATCOM performance in terms of reduction of switching losses and voltage stress across switching devices. To achieve this an adaptive dc-link voltage regulation method is proposed. An *LCL*-filter based DSTATCOM is implemented to improve the performance with the system operated in current and voltage control modes. The work is extended to hybrid DSTATCOM to reduce VSC rating and thereby performance is improved. In addition to power quality improvement by DSTATCOM, the real power injection into grid from solar PV system and active rectification operation are implemented based on energy management scheme. In this regard, the main objectives of the present work are as follows:

1. To minimize voltage stress across switching devices (IGBT switches) and switching losses without compromising compensation capabilities, an adaptive DC-link voltage regulation method is proposed. For that, an adaptive dc-link voltage reference calculation method is implemented based on the constraints. The proposed adaptive method is validated by simulation and experimental studies.

2. To minimize the interfacing inductance value of DSTATCOM, an *LCL*-filter based DSTATCOM is proposed, and the filter parameters are designed based on the switching dynamics. The proposed design of *LCL*-filter parameters gives better performance when compared to existing methods. This work is extended to operate *LCL*-filter based DSTATCOM in Current Control Mode (CCM) and Voltage Control Mode (VCM). In CCM operation, the current related power quality issues are minimized, and voltage disturbances such as sag and swell effect are minimized by operating in VCM. Further, simulation and experimental studies have been carried out to investigate the performance of the algorithm.

3. A Hybrid DSTATCOM having combination of *LCL*-filter with series ac-capacitor is proposed to reduce the voltage stress across switches and switching losses. To enhance the performance of the proposed hybrid DSTATCOM, an adaptive dc-link voltage control method is implemented. The effectiveness of the proposed hybrid DSTATCOM is verified with simulation and experimental results.

4. A Solar Photo-Voltaic DSTATCOM (SPV-DSTATCOM) with battery storage system is proposed for real power injection along with power quality improvement features. The efficiency and reliability of the SPV-DSTATCOM are increased by single-stage conversion system with energy management scheme. The single-stage conversion system is achieved by the proposed coordinated control algorithm. In this algorithm, the MPPT operation and real power injection to grid along with battery charging or discharging are achieved simultaneously. To show the efficacy of the proposed system, simulation and experimental studies are performed.

1.6 Organization of Thesis

In this Chapter, the power quality issues in the distribution system are introduced. A brief introduction has been given to improve power quality by traditional passive filters. This is followed by a description on shunt connected active power filters and hybrid

power filters to mitigate the current related power quality problems. Motivations and objectives of the thesis are also presented.

Chapter 2, provides introduction of custom power devices and detailed literature survey of DSTATCOM topologies in distribution system for power quality improvement. This is followed by reference current generation technique and design of DSTATCOM parameters.

In **Chapter 3**, a new method to select the reference dc-link voltage is proposed so that the control of DSTATCOM is achieved with improved performance. The switching loss calculation in conventional and proposed method is discussed. Further, simulation and experimental results are provided to verify the steady-state and dynamic performance of the DSTATCOM with different load conditions.

In **Chapter 4**, the design of *LCL*-filter based DSTATCOM for power quality improvement in 3P4W distribution system is discussed. Further, an algorithm to operate DSTATCOM in voltage control mode and current control mode is implemented. Also, detailed simulation and experimental studies for different load conditions are presented.

Chapter 5 presents the hybrid DSTATCOM for power quality improvement with reduced rating of VSC. Also, variable DC-link voltage is implemented and detailed simulation and experimental studies for different load conditions are presented.

Chapter 6 is dedicated to solar PV-DSTATCOM for real power injection and power quality improvement. The reliability of the SPV-DSTATCOM is increased by implementing single-stage solar PV-DSTATCOM with battery storage system. The proposed co-ordinated control for single-stage SPV-DSTATCOM achieves MPPT and real power injection to the grid along with charging or discharging of battery, simultaneously. An energy management scheme during PV and non-PV hours is explained. The proposed method has been validated by simulation and experimental studies.

Finally, **Chapter 7** is summarized the main conclusions of the research work and the possible scope for further research in this area.

CHAPTER 2

LITERATURE ON DSTATCOM TOPOLOGIES

Custom Power Devices (CPDs) solve most of the power quality problems in the distribution system and the existing compensating devices can be replaced by CPDs because of their versatile functionalities [21]. The compensating types of CPDs include the Dynamic Voltage Restorer (DVR) [29], DSTATCOM [30] and Unified Power Quality Conditioner (UPQC) [31]. Out of the CPDs, DSTATCOM is a shunt connected device and it gives better solution for compensation of current related power quality problems. DSTATCOM is a very popular and successful device in the distribution system because of its acceptable cost, flexibility of control and fast in response [23]–[28], [30]. The reactive power compensation, current harmonic mitigation and neutral current minimization in 3P4W system are achieved by DSTATCOM. The research work exploits DSTATCOM for power quality improvement in 3P4W distribution system. For completeness and better understanding of the thesis, different DSTATCOM topologies, control algorithms, and design parameters of DSTATCOM are briefly discussed in this chapter.

2.1 Configuration of DSTATCOM Topologies

DSTATCOM mainly consists of two distinct blocks, one is the converter circuit (also called power circuit), and the other one is DSTATCOM controller. The converter is responsible for synthesizing the compensating currents. DSTATCOM controller is responsible for signal processing in order to determine the compensating currents. The DSTATCOM topologies can be broadly classified based on its power circuit and the type of the distribution system.

2.1.1 Converter based DSTATCOM topologies

The power circuit of DSTATCOM can be made either with Voltage Source Converter (VSC) or Current Source Converter (CSC). The VSC approach shown in Fig. 2.1(a)

uses a dc-capacitor (C_{dc}) with a regulated dc-link voltage (V_{dc}), while the CSC, displayed in Fig. 2.1(b) uses a reactor (L_{dc}) supplied with regulated dc current (I_{dc}) [14].

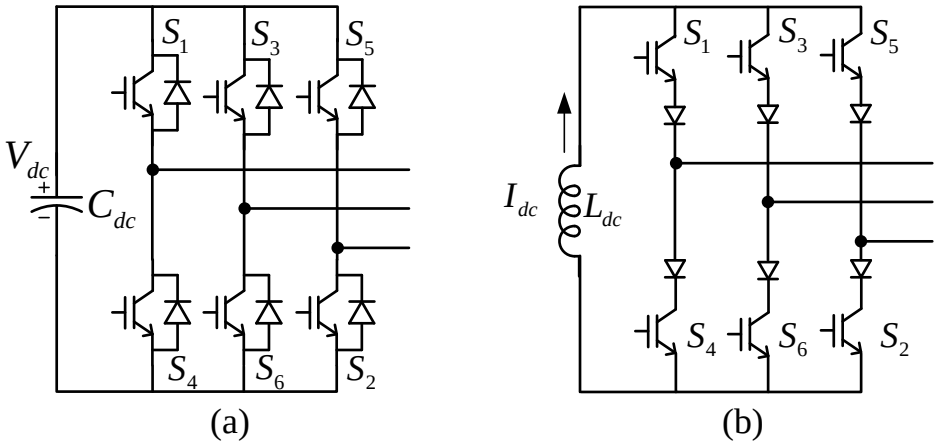


Fig. 2.1 (a) Voltage source converter and (b) current source converter

2.1.2 Distribution supply based DSTATCOM topologies

Based on the distribution supply and/or load system, DSTATCOMs are classified as single-phase system, three-phase three-wire (3P3W) system and three-phase four-wire (3P4W) system.

Single-phase DSTATCOMs

The single-phase (two-wire) DSTATCOMs are used for the compensation of reactive power and harmonics generated by the operation of non-linear loads, such as domestic appliances, connected to single-phase supply system. In single-phase system, H-bridge and split-capacitor DSTATCOMs are present. The H-bridge consists of two switching legs supported by one dc-link capacitor (or one dc source) as shown in Fig. 2.2. The split-capacitor DSTATCOM consists of one switching leg supported by two dc sources (or two capacitors) as shown in Fig. 2.3.

Three-phase three-wire DSTATCOMs

In three-phase three-wire (3P3W) distribution systems, the neutral wire is absent and these systems are used to supply high-power loads such as arc furnaces, adjustable

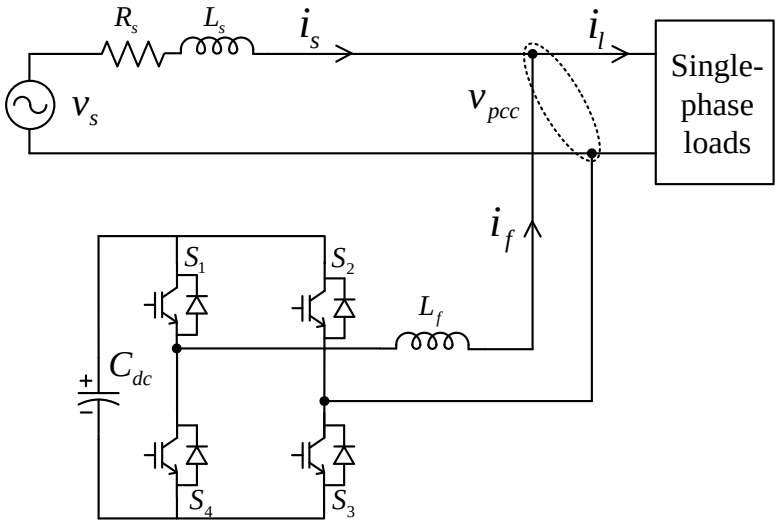


Fig. 2.2 Single-phase H-bridge DSTATCOM topology

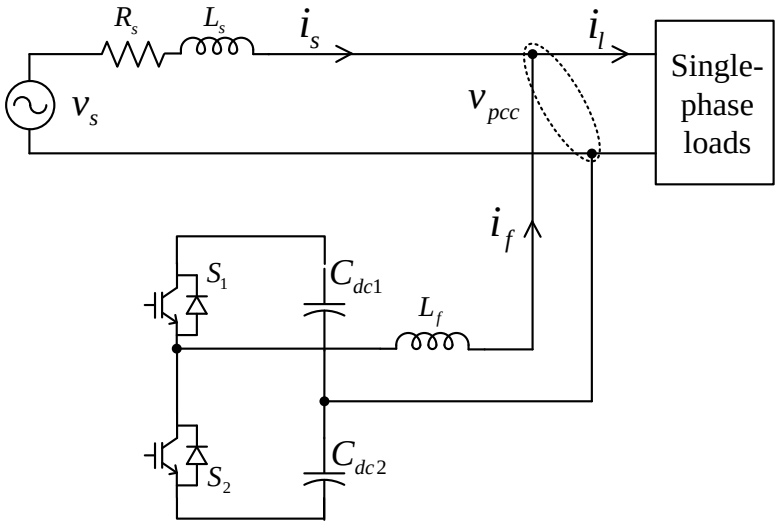


Fig. 2.3 Single-phase split-capacitor DSTATCOM topology

speed drives, tractions and other industrial applications [32]. To compensation reactive power and harmonics in these systems, a 3P3W DSTATCOM is used. The 3P3W DSTATCOMs consist of three-legs supported by one dc-link capacitor. Fig. 2.4, shows the connection of DSTATCOM in 3P3W distribution system.

Three-phase, four-wire DSTATCOMs

The DSTATCOMs in 3P4W systems are specially designed for compensating neutral current along with compensation of reactive power and harmonic mitigation. The available topologies in 3P4W systems are:

- Three single-phase H-bridge DSTATCOM topology

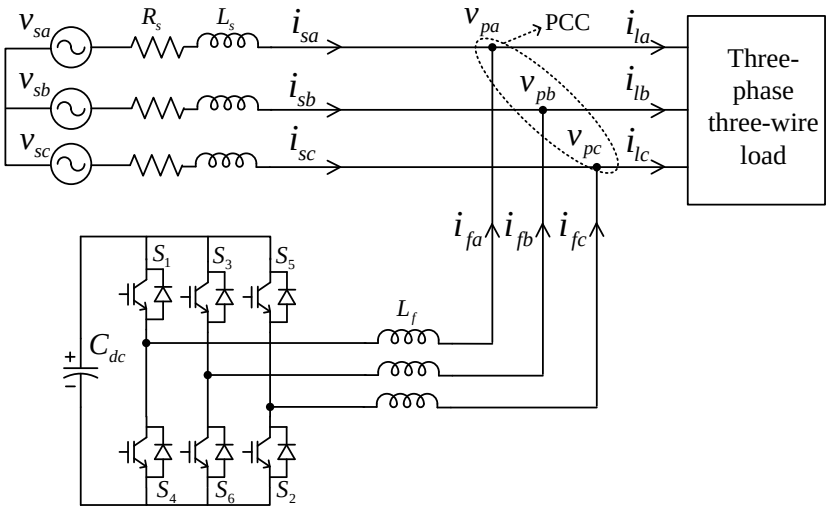


Fig. 2.4 Three-leg DSTATCOM in three-phase three-wire distribution system

- 3P4W four-leg DSTATCOM topology
- Three-leg split-capacitor DSTATCOM topology.

The three single-phase H-bridge DSTATCOM topology is shown in Fig. 2.5, and it consists of three single-phase H-bridges with a common dc-link voltage. [22]. These single-phase H-bridge inverters are connected to a 3P4W system by three single-phase isolation transformers. Considering the structural advantage of this topology, the control can be done either through a three-phase unit or three separate single-phase units. But, the main disadvantage of this topology is the increased number of switching devices.

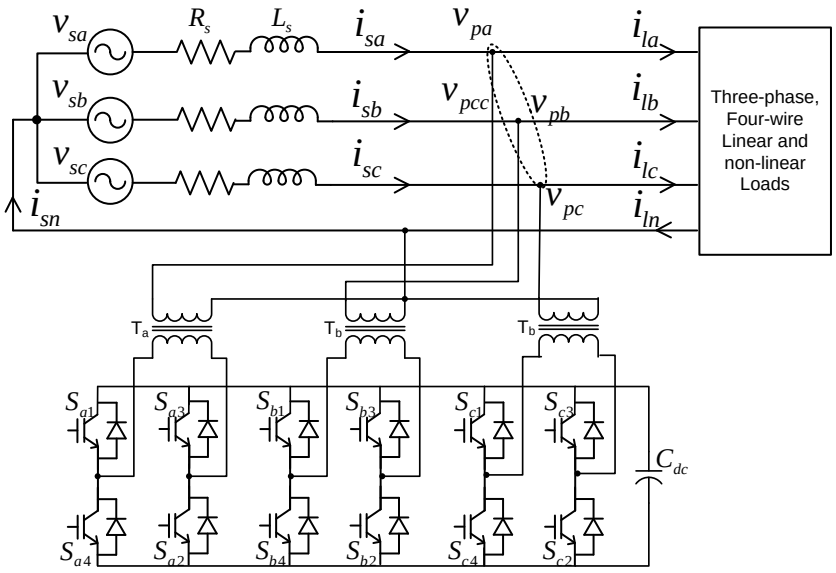


Fig. 2.5 Three single-phase H-bridge DSTATCOM topology in 3P4W distribution system

Three-phase, four-wire four-leg DSTATCOM topology is shown in Fig. 2.6. It consists of four-legs, in which three-legs are connected to three phases of supply through the series inductance while the fourth leg is connected to a neutral line with an optional inductor [23]. The three-legs and neutral-leg are supported by a dc-link voltage for compensation. This topology is most suitable for compensation of high neutral currents. In this topology, the switches in neutral leg require an extra switching control algorithm, which will be burden on the controller.

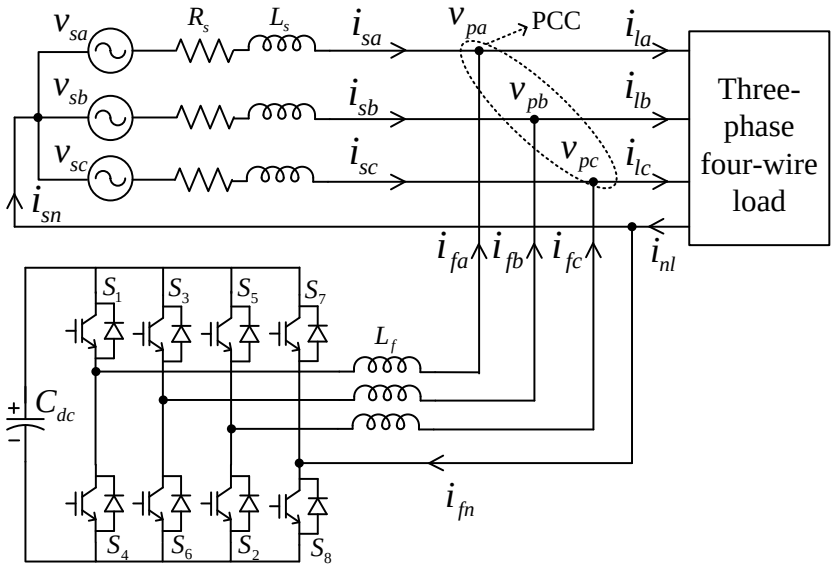


Fig. 2.6 Four-leg DSTATCOM topology in 3P4W distribution system

The schematic diagram of three-leg split-capacitor DSTATCOM topology in distribution system is shown in Fig. 2.7. It consists of three-legs, supported by the two dc-link capacitors [24]. The split-capacitors allow load neutral current to flow through one of the dc-link capacitors C_{dc1}, C_{dc2} and return. Because of that, the three-phase source currents become balanced.

In case of dc off-set present in the system or more unbalance operation condition, the voltages across two dc-link capacitors are not equal. Due to which, the compensation performance is affected. To balance the dc-link capacitor voltages, balanced circuit for split-capacitor DSTATCOM topology is proposed [25], which is shown in Fig. 2.8. The voltage balancing circuit consists of two extra switches S_7 and S_8, supported by inductor (L_1) connected in series with resistor (R_1). The inductor is charged by taking energy from the capacitor having more energy out of two capacitors, and discharged to the capacitor which has lower energy.

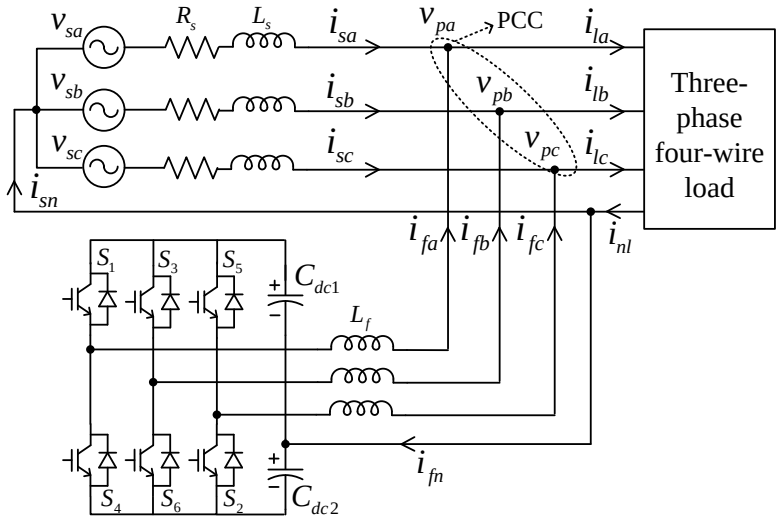


Fig. 2.7 Three-phase split-capacitor DSTATCOM topology in 3P4W distribution system

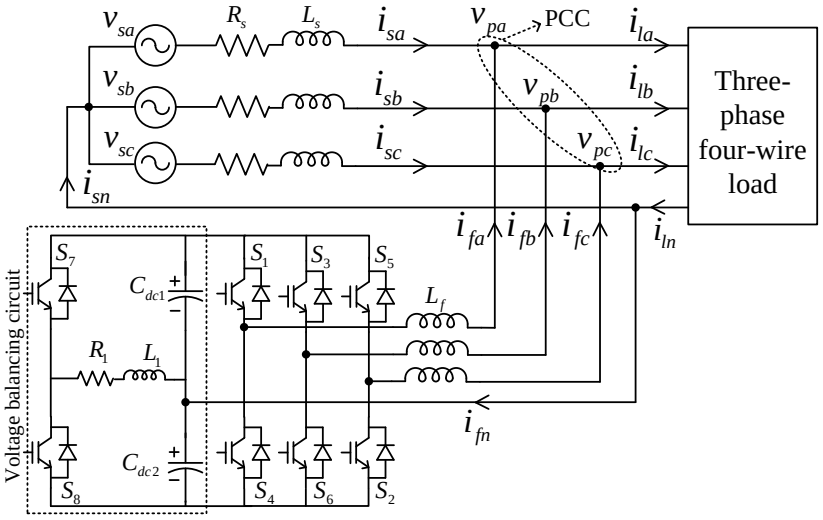


Fig. 2.8 Three-leg split-capacitor DSTATCOM topology with voltage-balancing circuit in 3P4W distribution system

The comparison between different three-phase DSTATCOM topologies are briefly given in Table 2.1. In H-bridge topology, the maximum voltage that appears across each H-bridge is the line-to-neutral voltage, but in other topologies line-to-line voltage will appear. This results in a reduction of dc-link voltage by a factor of $\sqrt{3}$ and thus the required dc-link voltage for proper operation of DSTATCOM also reduces by a maximum factor of $\sqrt{3}$. This, in turn, reduces the switch rating of VSC. The H-bridge and four-leg DSTATCOM topologies require more number of switching devices, which leads to increase in cost. The split-capacitor DSTATCOM topology suffers from dc-link capacitors voltage unbalancing due to the dc-offset present in the loads. However, there are several techniques proposed in literature to overcome the capacitor voltage unbalancing

problem [25]. The switching losses and voltage stress across switches will be more in three-leg split-capacitor DSTATCOM, because of high dc-link voltage requirement.

Table. 2.1 Comparison between three-phase DSTATCOM topologies

Topology features	H-bridge DSTATCOM [22]	3-leg DSTATCOM [32]	Four-leg DSTATCOM [33]	3-leg split-capacitor DSTATCOM [34]
Number of switches	12	6	8	6
No.of DC capacitors	1	1	1	2
Network suitability	3P3W, 3P4W	3P3W	3P3W, 3P4W	3P3W, 3P4W
Voltage stress across each switch	$2\ V_{pm}$	$\frac{2}{\sqrt{3}}\ (V_{pm})_{L-L}$	$\frac{2}{\sqrt{3}}\ (V_{pm})_{L-L}$	$\frac{3.2}{\sqrt{3}}\ (V_{pm})_{L-L}$
Switching loss	Comparatively low	Low	Moderate	High
Unbalance compensation	Yes	No	Yes	Yes
Total cost	Highest	Low	High	Medium

where $(V_{pm})_{L-L}$ is peak of line to line PCC voltage.

2.1.3 Design of Split-Capacitor DSTATCOM parameters

The important parameters of DSTATCOM are dc-link voltage, value of dc-link capacitors, value of interfacing inductor, switching frequency, hysteresis band and rating of VSC. A systematic procedure on the design of these parameters of a three-phase split-capacitor DSTATCOM topology is presented in the following sub-sections.

DC-link voltage selection

The dc-link voltage plays a very important role in designing the DSTATCOM parameters. In literature, the reference dc-link voltage of DSTATCOM is selected as two times the peak of PCC voltage [34], [35]. That is given as,

$$V_{dc} = \frac{2\sqrt{2}V_{LL}}{\sqrt{3}m_a} \tag{2.1}$$

where, V_{dc} is dc-link voltage, V_{LL} is line-to-line voltage at PCC and m_a is amplitude modulation index.

In [28], a detailed simulation study is carried out by varying dc-link voltage and interfacing inductor and arrive an empirical relationship between the dc link voltage and tracking performance of the compensator. If the dc-link voltage is not sufficient, then the compensator currents cannot be tracked by DSTATCOM. Whereas, if the dc-link voltage is higher than required, the compensator currents exceeds the upper and lower limits of the reference currents, thereby increasing THDs of the source currents. The author in [28], observed from the simulation studies that when the selected dc-link voltage is approximately 1.6 times the peak of PCC voltage, the percentage THD in the compensated source current is minimum. Therefore, in [28], the dc-link voltage is considered as,

$$V_{dc} = \frac{1.6\sqrt{2}V_{LL}}{\sqrt{3}m_a} \tag{2.2}$$

DC-link capacitor (C_{dc})

The dc-link capacitor is designed based on Unit Capacitor Constant (UCC), which is similar to that of unit inertia constant in synchronous rotary condenser [36].

$$UCC = \frac{\frac{1}{2}C_{dc}V_{dc}^2}{Q} \tag{2.3}$$

where, Q is assumed as maximum reactive power demanded by load (i.e., poor power factor condition), C_{dc} is dc-link capacitor and V_{dc} is dc-link voltage.

On the other side with consideration of ability to regulate voltage under load transients, the dc-link capacitors are designed based on the following procedure. Let us assume that the compensator is connected to a system of rating x kVA. The energy of the system in Joules per second is given by x kJ/s. Assume that, the VSC compensator deals with half (i.e., $x/2$) and twice (i.e., $2x$) kVA handling capacity under transient conditions for n cycles with time period (T) of the system voltage. Then the change in energy (ΔE) to be dealt with the dc-link capacitor is given as,

$$\Delta E = \left(2x - \frac{x}{2}\right)nT \tag{2.4}$$

Now this change in energy should be supported by the dc-link capacitor. Let us allow the dc-link capacitor to change its total dc-link voltage from 1.4 to 1.8 during the

transient conditions [37]. Then, the following relation is obtained.

$$\frac{1}{2}C_{dc}[(1.8V_m)^2 - (1.4V_m)^2] = (2x - \frac{x}{2})nT \tag{2.5}$$

where, V_m is peak of PCC voltage. Finally, the calculated dc-link capacitor value from (2.5) with respect to transient conditions is,

$$C_{dc} = \frac{2(2x - \frac{x}{2})nT}{(1.8V_m)^2 - (1.4V_m)^2} \tag{2.6}$$

Interfacing inductor (L_f)

The interfacing inductor is designed from the switching dynamics of controller which is explained below [28]. Fig. 2.9, shows the switching dynamics of the hysteresis controller. In which, the dotted-line represents reference filter current (i_{fref}), and solid-line

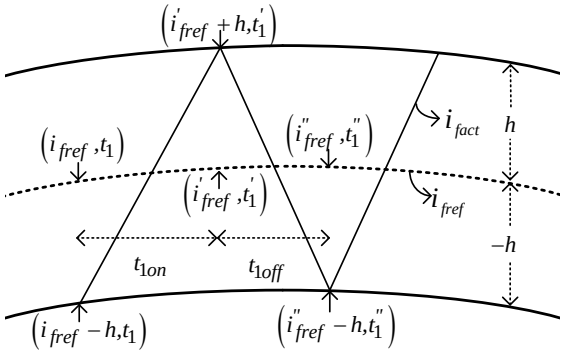


Fig. 2.9 Switching dynamics of hysteresis controller for *L*-filter design

represents actual filter current (i_{fact}) varying between hysteresis band ($\pm\, h$). The analysis is carried out by considering time instants t_1, t'_1 and t''_1 having reference filter currents of i_{fref}, i'_{fref} and i''_{fref}, respectively. From Fig. 2.9, the rate of change of actual filter current during the rising and falling slopes are given as:

$$\left.\begin{aligned} \frac{\mathrm{d}i_{fact}}{\mathrm{d}t_{on}} &= \frac{(i'_{fref} - i_{fref}) + 2h}{t_{on}} \\ \frac{\mathrm{d}i_{fact}}{\mathrm{d}t_{off}} &= \frac{(i''_{fref} - i'_{fref}) - 2h}{t_{off}} \end{aligned}\right\} \tag{2.7}$$

During the conduction of upper switches of VSC, the upper dc-link capacitor voltage is supported. Similarly, the lower dc-link capacitor voltage support during conduction of lower switches of VSC. Applying Kirchhoff Voltage Law (KVL) from VSC to PCC,

gives the following equations:

$$\left.\begin{aligned} m_a V_{dc} - V_m \sin\omega t &= L_f \frac{\mathrm{d}i_{fact}}{\mathrm{d}t_{on}} + R_f i_{fact} \\ -m_a V_{dc} - V_m \sin\omega t &= L_f \frac{\mathrm{d}i_{fact}}{\mathrm{d}t_{off}} + R_f i_{fact} \end{aligned}\right\} \tag{2.8}$$

where, R_f is internal resistance of inductor L_f and its value is very low so the drop $R_f i_{fact}$ is neglected. After simplification of (2.7) and (2.8),

$$t_{on} = \frac{2hL_f}{m_a V_{dc} - V_m \sin\omega t - i_{fact} R_f} \tag{2.9}$$

$$t_{off} = \frac{2hL_f}{m_a V_{dc} + V_m \sin\omega t + i_{fact} R_f} \tag{2.10}$$

From the above equations, the switching frequency (f_{sw}) is derived as,

$$\left.\begin{aligned} f_{sw} &= \frac{1}{t_{on} + t_{off}} \\ &= \frac{1}{4hL_f}\left(m_a V_{dc} - \frac{V_m^2}{m_a V_{dc}} \sin^2\theta\right) \end{aligned}\right\} \tag{2.11}$$

where, $\theta = \omega$t and ω=2πf. It is observed from (2.11) that, the switching frequency becomes maximum when θ value is zero. Therefore, the inductance value for maximum switching frequency is given as,

$$L_f = \frac{m_a V_{dc}}{4h f_{sw,max}} \tag{2.12}$$

where, $f_{sw,max}$ is maximum switching frequency. The interfacing inductance is used to reduce the high-frequency components in the filter current injected by DSTATCOM and to provide the necessary tracking requirement of filter current. The selected interfacing inductor must be capable of compensating the current change at conduction time interval in one switching period. If the inductance is not sufficiently large, then the error between reference and actual currents is maximum and this will affect compensation performance for a finite interval of each cycle. If the inductance is too large to track the reference signal, the drop across inductor will increase, and which demands high dc-link voltage for satisfactory operation. The selection of the inductor depends on the dc-link voltage, switching frequency, and hysteresis band of controller.

Switching frequency

The switching frequency of the VSC is given by equation (2.11). It is seen that the switching frequency is a function of various system parameters. Practically, the maximum switching frequency of the VSC depends on the type of power switches used. To achieve higher switching frequency in the range of 100 kHz, MOSFET switches should be used, but their voltage and current rating are smaller compared to IGBT switches. However, a high value of current cannot be switched at high frequency as it leads to electromagnetic interference problems and considerable switching losses. The IGBT switches are generally preferred due to their higher power handling capacity, fast switching and low gating power. Typically, the switching frequency of the IGBT switches is around 20 kHz [38]. But it is recommended to operate at 10 kHz range, and which is considered in this thesis for design of DSTATCOM parameters.

Hysteresis band

The selection of hysteresis band in current control technique is very important. To track the reference currents properly by actual current, a suitable value of hysteresis band (h) has to be selected. The relation between hysteresis band and other VSC parameters is given in (2.12). An important observation can be drawn from (2.12) and that is selection of h value. For example, if a low value of hysteresis band is chosen, the switching frequency requirement of VSC becomes high. Similarly, when interface inductance is quite large, for a given bandwidth of VSC, a small hysteresis band is required to maintain the product $L_f f_{sw,max}$ constant. If the switching frequency is very high, switching losses will go up. Therefore, for better performance the value of h is considered in between 5% to 15% of rated filter current [28].

Rating of VSC

The rating of VSC depends on power rating of switches used. The voltage supported by each switch is equal to the maximum dc bus voltage ($V_{dc,m}$). And the current supported by each switch is equal to the maximum current flowing through the switch, that is

$$i_{f,m} = i_l - i_s \tag{2.13}$$

Where, $i_{f,m}$ is the maximum filter current injected by VSC, i_s is source current and i_l is the load current. Then, the rating of VSC is,

$$\text{VSC}_{rating} = \sqrt{3}\frac{V_{dc,m}}{\sqrt{2}}\frac{I_{f,m}}{\sqrt{2}} \tag{2.14}$$

Once the circuit parameters are chosen, the switching frequency of the controller will be selected based on a compromise between the required filtering performance and the allowable power dissipation in the filter.

The operation of the designed split-capacitor DSTATCOM, depends on control technique implemented for reference current generation, which are discussed below.

2.2 Control Techniques for DSTATCOM Operation

In literature, numerous papers are available to describe the reference current generation techniques used for reactive power compensation and harmonics mitigation [30], [39]–[49]. The classification of the reference current generation methods can be done depending on the mathematical analysis involved [39]. In general, the reference generation methods are classified into frequency-domain and time-domain. The frequency-domain methods mainly use Fourier analysis for calculating the reference currents generation [39]. The commonly used frequency-domain methods are discrete Fourier transform (DFT) [40], recursive discrete Fourier transform (RDFT) [41] and fast Fourier transform (FFT) [42]. The drawbacks with frequency-domain based harmonic detection methods are proper design of the anti-aliasing filter, large memory requirements to store the achieved samples, careful synchronization between sampling time and fundamental frequency of the inverter, large computation burden on controller, and imprecise results in transient conditions [39].

But on the other hand, time-domain methods offer increased speed, ease of implementation, and fewer calculations compared to the frequency-domain methods [39]. There are numerous time-domain approaches reported in the literature, and some of them are, instantaneous *abc* theory [43], unit template theory [44], Instantaneous Reactive Power (IRP) or *p*-*q* theory [30], Synchronous Reference Frame (SRF) or i_d-i_q theory [50], Instantaneous Symmetrical Component (ISC) theory [45], I$\cos\phi$ control technique [46],

and a scheme based on neural network techniques [47]. These control schemes are widely used in DSTATCOM applications and they are explained in this chapter. However, in this thesis, ISC theory is used because of its ease of implementation, excellent transient response and ability to work for different source conditions [48].

2.2.1 Instantaneous *abc* Theory

Instantaneous *abc* Theory consists of a minimized instantaneous active current component of load current. For that, two minimization techniques are discussed in literature:

1. Active and non-active currents minimization method.
2. Generalized fryze currents minimization method.

In active and non-active minimization method, non-active current component is determined by applying minimization method. Let the original load current be i_l, which consists of active and non-active portions, that is,

$$i_l = i_p + i_q \tag{2.15}$$

where, i_p and i_q are active and non-active current components of load current, respectively. This method involves minimizing load current under the constraint that, the three-phase non-active current components do not contribute instantaneous active current. Thus, finding the minimization of,

$$\mathcal{L}(i_{qa}, i_{qb}, i_{qc}) = (i_{la} - i_{pa})^2 + (i_{lb} - i_{pb})^2 + (i_{lc} - i_{pc})^2 \tag{2.16}$$

constrained by $g(i_{qa}, i_{qb}, i_{qc}) = v_a i_{qa} + v_b i_{qb} + v_c i_{qc} = 0$ is necessary. Where, $\mathcal{L}$ is considered as function of i_{qa}, i_{qb} and i_{qc} currents. i_{la}, i_{lb} and i_{lc} are three-phase load currents; i_{pa}, i_{pb} and i_{pc} are three-phase active current components of load currents; i_{qa}, i_{qb} and i_{qc} are three-phase non-active current components of load currents; v_{sa}, v_{sb} and v_{sc} are three-phase source voltages.

By applying Lagrange Multiplier method, the following relation is obtained from above

equation.

$$\begin{bmatrix} 2 & 0 & 0 & v_{sa} \\ 0 & 2 & 0 & v_{sb} \\ 0 & 0 & 2 & v_{sc} \\ v_{sa} & v_{sb} & v_{sc} & 0 \end{bmatrix} \begin{bmatrix} i_{qa} \\ i_{qb} \\ i_{qc} \\ \lambda \end{bmatrix} = \begin{bmatrix} 2i_{la} \\ 2i_{lb} \\ 2i_{lc} \\ 0 \end{bmatrix} \tag{2.17}$$

where, the λ is Lagrange multiplier, and it value is given as,

$$\lambda = \frac{2(v_{sa}i_{la} + v_{sb}i_{lb} + v_{sc}i_{lc})}{v_{sa}^2 + v_{sb}^2 + v_{sc}^2} = \frac{2P_{3\phi}}{v_{sa}^2 + v_{sb}^2 + v_{sc}^2} \tag{2.18}$$

where, $P_{3\phi}$ is instantaneous active power in three-phase system. The following relations are obtained from (2.17)

$$\left.\begin{aligned} 2i_{qa} + v_{sa}\lambda = 2i_{la} \\ 2i_{qb} + v_{sb}\lambda = 2i_{lb} \\ 2i_{qc} + v_{sc}\lambda = 2i_{lc} \end{aligned}\right\} \tag{2.19}$$

By substituting λ in (2.19), i_{qa}, i_{qb} and i_{qc} are given as,

$$i_{qa} = i_{la} - \frac{v_{sa}P_{3\phi}}{v_{sa}^2 + v_{sb}^2 + v_{sc}^2} \tag{2.20}$$

$$i_{qb} = i_{lb} - \frac{v_{sb}P_{3\phi}}{v_{sa}^2 + v_{sb}^2 + v_{sc}^2} \tag{2.21}$$

$$i_{qc} = i_{lc} - \frac{v_{sc}P_{3\phi}}{v_{sa}^2 + v_{sb}^2 + v_{sc}^2} \tag{2.22}$$

From (2.15) and (2.22), the instantaneous active currents are,

$$\begin{bmatrix} i_{pa} \\ i_{pb} \\ i_{pc} \end{bmatrix} = \frac{2P_{3\phi}}{v_{sa}^2 + v_{sb}^2 + v_{sc}^2} \begin{bmatrix} v_{sa} \\ v_{sb} \\ v_{sc} \end{bmatrix} \tag{2.23}$$

In the above equation, for balanced and sinusoidal system, $P_{3\phi}$ and $v_{sa}^2 + v_{sb}^2 + v_{sc}^2$ are constant. It gives a linear relation between i_{pk} and v_{sk}, where k= a, b and c. This method will not give an appropriate solution to a distorted supply system [43]. This can be rectified by generalized fryze currents minimization method.

Fryze currents minimization method is the extension of the active and non-active minimization method, in which the linearity between voltage and current is maintained even

under distorted and/or unbalanced source voltages. The linearity relation in this method is given as,

$$i_{pk} = G_e v_{sk} \tag{2.24}$$

where, G_e is equivalent conductivity. The value of G_e is calculated from the concept of aggregate voltage [51].

$$G_e = \frac{\overline{P}_{3\phi}}{\sum V_{sk}^2} \tag{2.25}$$

where, $\overline{P}_{3\phi}$ is average active power and $\sum V_{sk}^2$ is sum of the squared rms values of voltages. Therefore, the value of equivalent conductivity (G_e) in (2.24) is an average value, therefore it ensures linearity between voltage and current.

These minimization methods given in *abc* theory are inappropriate to deal with zero sequence components. Some extra efforts have to be made with the above described minimization methods in order to deal properly with zero sequence components. The compensation algorithm establishes through minimization methods are relatively simple to implement, but they are inapplicable to three-phase four-wire system, and also cannot guarantee constant active power from the source [43].

2.2.2 Instantaneous Reactive Power (IRP) Theory

The instantaneous reactive power theory was proposed by Akagi H., Kanazawa Y., and Nabae A [30], [43]. This theory is also called as $p-q$ theory. The main aim of this theory is to derive compensating currents corresponding to instantaneous reactive power, such that the reactive power can be compensated. As this theory is based on a set of instantaneous reactive power defined in time domain, it is valid not only in steady state conditions but also in transient conditions.

Let, the system voltages are,

$$\left.\begin{aligned} v_{sa} &= \sqrt{2}V_m \sin\omega t \\ v_{sb} &= \sqrt{2}V_m \sin(\omega t - \frac{2\pi}{3}) \\ v_{sc} &= \sqrt{2}V_m \sin(\omega t - \frac{4\pi}{3}) \end{aligned}\right\} \tag{2.26}$$

and, the respective load currents are,

$$\left.\begin{aligned} i_{la} &= \sqrt{2} I_m \sin(\omega t - \theta) \\ i_{lb} &= \sqrt{2} I_m \sin(\omega t - \frac{2\pi}{3} - \theta) \\ i_{lc} &= \sqrt{2} I_m \sin(\omega t - \frac{4\pi}{3} - \theta) \end{aligned}\right\} \tag{2.27}$$

where, V_m and I_m peak values of voltage and current, respectively. The $p-q$ theory starts with the transformation of three-phase voltage and currents into $\alpha\beta 0$ stationary reference frame. This transformation is well known as Clarke transformation. The instantaneous three-phase voltages (v_{sa}, v_{sb}, v_{sc}) into the instantaneous voltages on the $\alpha\beta 0$-axes are,

$$\begin{bmatrix} v_\alpha \\ v_\beta \\ v_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} v_{sa} \\ v_{sb} \\ v_{sc} \end{bmatrix} \tag{2.28}$$

Similarly, the instantaneous three-phase load currents (i_{la}, i_{lb}, i_{lc}) on $\alpha\beta 0$-axes are,

$$\begin{bmatrix} i_\alpha \\ i_\beta \\ i_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} i_{la} \\ i_{lb} \\ i_{lc} \end{bmatrix} \tag{2.29}$$

One advantage of applying $\alpha\beta 0$ transformation is the separation of zero-sequence components from the abc-phase components. The α and β axes do not have contribution to the zero-sequence component.

The components v_0 and i_0 can be neglected in $\alpha\beta 0$-frame when zero-sequence component is absent in the system. Elimination of v_0 in (2.28) leads to,

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_{sa} \\ v_{sb} \\ v_{sc} \end{bmatrix} \tag{2.30}$$

and elimination of i_0 in (2.29) leads to,

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} i_{la} \\ i_{lb} \\ i_{lc} \end{bmatrix} \tag{2.31}$$

The instantaneous real and reactive powers in $\alpha\beta 0$ reference frame from instantaneous voltages (v_α, v_β) and instantaneous currents (i_α, i_β) are,

$$p = v_\alpha i_\alpha + v_\beta i_\beta, \quad \text{and} \quad q = -v_\beta i_\alpha + v_\alpha i_\beta \tag{2.32}$$

The representation of the above equation in matrix form is,

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} v_\alpha & v_\beta \\ -v_\beta & v_\alpha \end{bmatrix}\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \tag{2.33}$$

These instantaneous real and reactive powers have average and oscillatory components. Therefore, the real and reactive powers in (2.32) are represented as,

$$p = \overline{p} + \tilde{p}, \qquad q = \overline{q} + \tilde{q} \tag{2.34}$$

where, $\overline{p}$ and $\overline{q}$ are average values of real and reactive powers, respectively. $\tilde{p}$ and $\tilde{q}$ are oscillatory components in real and reactive powers, respectively.

The currents in $\alpha\beta$-frame from (2.33) are,

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \frac{1}{v_\alpha^2 + v_\alpha^2}\begin{bmatrix} v_\alpha & v_\beta \\ v_\beta & -v_\alpha \end{bmatrix}\begin{bmatrix} p \\ q \end{bmatrix} \tag{2.35}$$

Once the real and reactive powers are separated into their average and oscillating parts, the undesired components of the real and reactive powers can be selected for compensation with DSTATCOM, which is explained below.

Reference currents generation

The undesired current components corresponding to powers, $\tilde{p}$ and $\tilde{q}$ of the load along with harmonics and reactive power must be compensated. As a result, the three-phase

source currents become sinusoidal and balanced. The separation of $\tilde{p}$ from p can be done by using a second order low-pass filter [43]. Then, from (2.33), the compensating currents in $\alpha\beta$-frame are given as,

$$\begin{bmatrix} i^*_{f\alpha} \\ i^*_{f\beta} \end{bmatrix} = \frac{1}{v_\alpha^2 + v_\beta^2} \begin{bmatrix} v_\alpha & v_\beta \\ v_\beta & -v_\alpha \end{bmatrix} \begin{bmatrix} -\tilde{p} \\ -q \end{bmatrix}$$

The reason for including negative signs in the compensating powers is to emphasize the fact that DSTATCOM should draw a compensating current that produces the exact negative of the undesirable powers drawn by the non-linear or reactive load. The representation of reference currents in abc-frame from $\alpha\beta$-frame are,

$$\begin{bmatrix} i^*_{fa} \\ i^*_{fb} \\ i^*_{fc} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i^*_{f\alpha} \\ i^*_{f\beta} \end{bmatrix} \tag{2.36}$$

Reference currents generation in case of dc-link voltage control

In practice, the DSTATCOM has switching losses associated with the switching operation. If this losses is supplied by the dc-link capacitors, then their voltages would progressively reduce, and thereby the performance of the DSTATCOM effected adversely. In order to maintain the dc-link voltage at a constant value, a small amount of average real power (P_{loss}) must be drawn continuously from the power system to supply switching and ohmic losses present in the voltage source converter. This can be done by adding a dc-link voltage regulator in the control strategy and which is shown in Fig. 2.10.

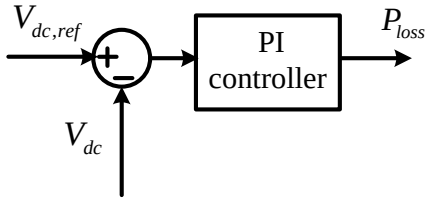


Fig. 2.10 DC-link voltage regulation loop in IRP theory

In dc-link voltage regulator, reference dc-link voltage ($V_{dc,ref}$) and the actual dc-link voltage (V_{dc}) are compared and the error is processed through a PI controller. The output

of the PI controller gives the real power component to be drawn by the DSTATCOM to compensate for power losses in the voltage source converter thereby maintaining the dc-link voltage at their reference value. In this case, the reference compensating currents in $\alpha\beta$-frame are given as,

$$\begin{bmatrix} i^*_{f\alpha} \\ i^*_{f\beta} \end{bmatrix} = \frac{1}{v_\alpha^2 + v_\beta^2} \begin{bmatrix} v_\alpha & v_\beta \\ v_\beta & -v_\alpha \end{bmatrix} \begin{bmatrix} -\tilde{p} + p_{loss} \\ -q \end{bmatrix}$$

these reference currents in *abc*-frame are,

$$\begin{bmatrix} i^*_{fa} \\ i^*_{fb} \\ i^*_{fc} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i^*_{f\alpha} \\ i^*_{f\beta} \end{bmatrix} \tag{2.37}$$

The block diagram of complete control algorithm with IRP theory is shown in Fig. 2.11. Once, after reference filter currents are generated, these values are compared to actual filter currents and the error is given to hysteresis controller for switching pulse generation to IGBTs.

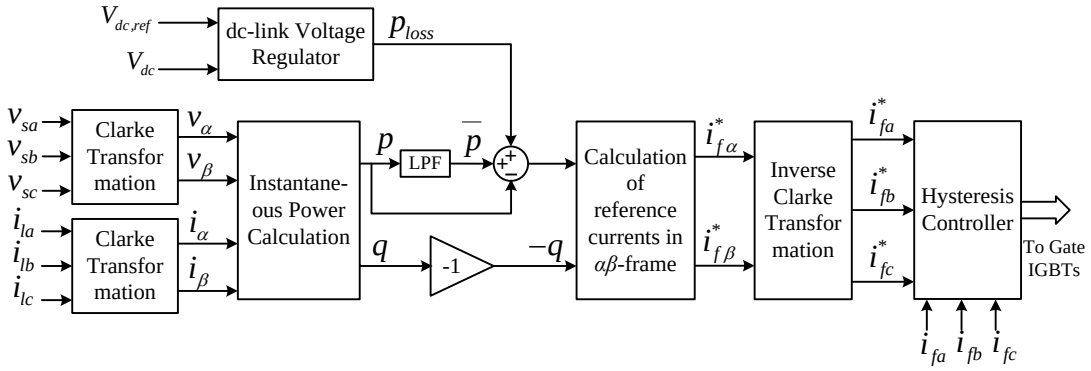


Fig. 2.11 Control algorithm for DSTATCOM with IRP theory

The compensation algorithm based on $p-q$ theory is very flexible to select undesirable powers to be compensated. The $\alpha\beta 0$-transformation in $p-q$ theory, can allow three-phase loads to provide constant instantaneous active power even if supply voltages are unbalanced and/or distorted. However, it is more complex than the instantaneous *abc*-theory [43].

2.2.3 Synchronous Reference Frame (SRF) Theory

This theory is also called $d-q$ axes theory, because d-axis and q-axis current components are derived from the measured phase voltages and load currents. Let the load currents in three-phase system be i_{la}, i_{lb} and i_{lc}, then the representation of these currents in $dq0$-frame are,

$$\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos\theta & \cos(\theta-120) & \cos(\theta+120) \\ -\sin\theta & -\sin(\theta-120) & -\sin(\theta+120) \\ 1/2 & 1/2 & 1/2 \end{bmatrix} \begin{bmatrix} i_{la} \\ i_{lb} \\ i_{lc} \end{bmatrix} \tag{2.38}$$

where, the angle θ is calculated from three-phase phase voltages by using Phase Locked Loop (PLL). The d-axis current and q-axis current component consist of average and oscillatory components. Therefore, i_d and i_q are represented as,

$$i_d = \bar{i}_d + \tilde{i}_d, \qquad i_q = \bar{i}_q + \tilde{i}_q \tag{2.39}$$

The instantaneous currents in abc-components are,

$$\begin{bmatrix} i_{la} \\ i_{lb} \\ i_{lc} \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta & 1 \\ \cos(\theta-120) & -\sin(\theta-120) & 1 \\ \cos(\theta+120) & -\sin(\theta+120) & 1 \end{bmatrix} \begin{bmatrix} i_d \\ i_q \\ 0 \end{bmatrix} \tag{2.40}$$

Once the d-axis and q-axis currents are separated into their average and oscillating parts, then the undesired current components can be selected for compensation with DSTATCOM, which is explained below.

Reference currents generation

The reference current generation for compensating harmonic and reactive current components contained in the load current is explained here. The three-phase source currents are expected as sinusoidal, balanced and in-phase with phase voltages after compensation. This can be achieved by making d-axis current as oscillatory free and q-axis current as zero. The oscillatory d-axis current ($\tilde{i}_d$) is separated from i_d, by using a second order low-pass filter. Then, from (2.38), the reference three-phase source currents for

compensation in *abc*-frame are,

$$\begin{bmatrix} i_{sa}^* \\ i_{sb}^* \\ i_{sc}^* \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta & 1 \\ \cos(\theta-120) & -\sin(\theta-120) & 1 \\ \cos(\theta+120) & -\sin(\theta+120) & 1 \end{bmatrix} \begin{bmatrix} \bar{i}_d \\ 0 \\ 0 \end{bmatrix} \tag{2.41}$$

The angle θ is same as calculated before from three-phase PLL. The reference compensating currents are then obtained from,

$$i_{fa}^* = i_{la} - i_{sa}^* \tag{2.42}$$

$$i_{fb}^* = i_{lb} - i_{sb}^* \tag{2.43}$$

$$i_{fc}^* = i_{lc} - i_{sc}^* \tag{2.44}$$

Reference currents generation in case of dc-link voltage control

The source has to deliver dc-component of current in addition to average active current component ($\bar{i}_d$) of the load current for meeting the losses (i_{loss}) in the VSC of DSTATCOM. The control diagram of dc-link voltage regulation loop in SRF theory is shown in Fig. 2.12.

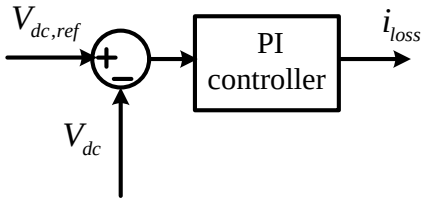


Fig. 2.12 DC-link voltage regulation loop in SRF theory

The reference three-phase source currents during dc-link voltage control are,

$$\begin{bmatrix} i_{sa}^* \\ i_{sb}^* \\ i_{sc}^* \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta & 1 \\ \cos(\theta-120) & -\sin(\theta-120) & 1 \\ \cos(\theta+120) & -\sin(\theta+120) & 1 \end{bmatrix} \begin{bmatrix} \bar{i}_d + i_{loss} \\ 0 \\ 0 \end{bmatrix} \tag{2.45}$$

The block diagram of complete control algorithm for DSTATCOM with synchronous reference frame theory is shown in Fig. 2.13. After reference filter currents are generated, these values compared to actual filter currents and the error is given to hysteresis

controller for switching pulses generation to IGBTs.

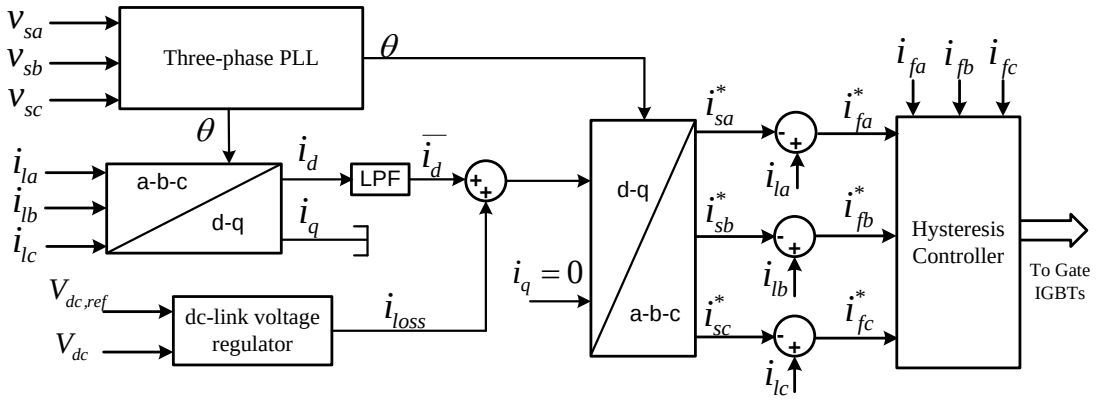


Fig. 2.13 Control algorithm for DSTATCOM with SRF theory

2.2.4 Instantaneous Symmetrical Component (ISC) Theory

The reference filter currents generation by using instantaneous symmetrical component theory is explained below [24]. The positive sequence currents and voltages are,

$$\begin{bmatrix} i_{s+} \\ i_{s-} \\ i_{s0} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 1 & a & a^2 \\ 1 & a^2 & a \\ 1 & 1 & 1 \end{bmatrix}\begin{bmatrix} i_{sa} \\ i_{sb} \\ i_{sc} \end{bmatrix} \qquad \begin{bmatrix} v_{s+} \\ v_{s-} \\ v_{s0} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 1 & a & a^2 \\ 1 & a^2 & a \\ 1 & 1 & 1 \end{bmatrix}\begin{bmatrix} v_{sa} \\ v_{sb} \\ v_{sc} \end{bmatrix}$$

where $a = e^{j120^\circ}$ and where $a^2 = e^{j240^\circ}$, i_{s+}, i_{s-} and i_{s0} are positive, negative and zero sequence currents, respectively. v_{s+}, v_{s-} and v_{s0} are positive, negative and zero sequence voltages, respectively.

The first objective in either three-phase three-wire or four-wire unbalanced and non-linear load system, is to provide balanced supply currents such that its zero sequence component becomes zero. That means, the sum of the three-phase source currents is zero.

$$i_{sa} + i_{sb} + i_{sc} = 0 \tag{2.46}$$

The second objective is, for a predefined power factor, the relation between instanta-

neous positive sequence voltage (v_{s+}) and current (i_{s+}) is given as,

$$\angle v_{s+} = \angle i_{s+} + \theta_+ \tag{2.47}$$

$$\frac{1}{3}\angle(v_{sa} + av_{sb} + a^2 v_{sc}) = \frac{1}{3}\angle(i_{sa} + ai_{sb} + a^2 i_{sc}) + \theta_+ \tag{2.48}$$

where, θ_+ is power factor angle. After solving and rearranging the terms in (2.48)

$$\begin{aligned}\{(v_{sb} - v_{sc}) + \beta\,(v_{sb} + v_{sc} - 2v_{sa})\}\, i_{sa} + \{(v_{sc} - v_{sa}) + \beta\,(v_{sc} + v_{sa} - 2v_{sb})\}\, i_{sb} \\ + \{(v_{sa} - v_{sb}) + \beta\,(v_{sa} + v_{sb} - 2v_{sc})\}\, i_{sc} = 0\end{aligned} \tag{2.49}$$

where, $\beta = \tan^{-1}(\frac{\theta_+}{\sqrt{3}})$. Equation (2.49) is modified as,

$$\{(v_{sb} - v_{sc}) + \beta A\}\, i_{sa} + \{(v_{sc} - v_{sa}) + \beta B\}\, i_{sb} + \{(v_{sa} - v_{sb}) + \beta C\}\, i_{sc} = 0 \tag{2.50}$$

where, $A = v_{sb} + v_{sc} - 2v_{sa}$, $B = v_{sc} + v_{sa} - 2v_{sb}$ and $C = v_{sa} + v_{sb} - 2v_{sc}$.

The third objective of compensation is that the load required active power (P_{lavg}) is only supplied by three-phase supply, which means that the load required reactive power is to be supplied by the compensator (DSTATCOM). Then,

$$v_{sa}i_{sa} + v_{sb}i_{sb} + v_{sc}i_{sc} = P_{lavg} \tag{2.51}$$

Equations (2.46), (2.49) and (2.51) are represented in matrix form,

$$\begin{bmatrix} 1 & 1 & 1 \\ (v_{sb} - v_{sc}) + \beta A & (v_{sc} - v_{sa}) + \beta B & (v_{sa} - v_{sb}) + \beta C \\ v_{sa} & v_{sb} & v_{sc} \end{bmatrix} \begin{bmatrix} i_{sa} \\ i_{sb} \\ i_{sc} \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ P_{lavg} \end{bmatrix}$$

The above matrix is in the form of, $[X][i] = [P]$. Then, $[i] = [X]^{-1}[P]$.

$$\begin{bmatrix} i_{sa} \\ i_{sb} \\ i_{sc} \end{bmatrix} = \frac{1}{\left(\Sigma_{j=a,b,c}\, v_{sj}^2 - 3v_{s0}^2\right)} \begin{bmatrix} (v_{sa} - v_{s0}) + \beta(v_{sb} - v_{sc}) \\ (v_{sb} - v_{s0}) + \beta(v_{sc} - v_{sa}) \\ (v_{sc} - v_{s0}) + \beta(v_{sa} - v_{sb}) \end{bmatrix} \begin{bmatrix} P_{lavg} \end{bmatrix}$$

$$i_{sa} = \frac{(v_{sa} - v_{s0}) + \beta(v_{sb} - v_{sc})}{\Sigma_{j=a,b,c}\, v_{sj}^2 - 3v_{s0}^2} P_{lavg} \tag{2.52}$$

$$i_{sb} = \frac{(v_{sb} - v_{s0}) + \beta(v_{sc} - v_{sa})}{\Sigma_{j=a,b,c}\, v_{sj}^2 - 3v_{s0}^2} P_{lavg} \tag{2.53}$$

$$i_{sc} = \frac{(v_{sc} - v_{s0}) + \beta(v_{sa} - v_{sb})}{\Sigma_{j=a,b,c}\, v_{sj}^2 - 3v_{s0}^2} P_{lavg} \tag{2.54}$$

where, $v_{s0} = \frac{1}{3}(v_{sa} + v_{sb} + v_{sc})$. Applying Kirchhoff's Current Law (KCL) at Point of Common Coupling (PCC), the reference filter currents ($i_{fa}^*, i_{fb}^*, i_{fc}^*$) are given as follows.

$$i_{fa}^* = i_{la} - i_{sa}; \qquad i_{fb}^* = i_{lb} - i_{sb}; \qquad i_{fc}^* = i_{lc} - i_{sc} \tag{2.55}$$

For unity power factor, the value of θ_+=0, then β value becomes zero. After substituting i_{sa}, i_{sb}, i_{sc} and $\beta = 0$ in (2.55), the reference filter currents are,

$$\left.\begin{aligned} i_{fa}^* &= i_{la} - \left(\frac{v_{sa} - v_{s0}}{\triangle}\right) P_{lavg} \\ i_{fb}^* &= i_{lb} - \left(\frac{v_{sb} - v_{s0}}{\triangle}\right) P_{lavg} \\ i_{fc}^* &= i_{lc} - \left(\frac{v_{sc} - v_{s0}}{\triangle}\right) P_{lavg} \end{aligned}\right\} \tag{2.56}$$

where, $\triangle = (\Sigma_{j=a,b,c}\, v_{sj}^2 - 3v_{s0}^2)$ or $(v_{sa}^2 + v_{sb}^2 + v_{sc}^2 - 3v_{s0}^2)$. The power loss term, P_{loss} in the compensator (DSTATCOM) is supplied by three-phase supply so that P_{loss} term is added to P_{lavg}, and equation (2.56) becomes,

$$\left.\begin{aligned} i_{fa}^* &= i_{la} - \left(\frac{v_{sa} - v_{s0}}{\triangle}\right)\left(P_{lavg} + P_{loss}\right) \\ i_{fb}^* &= i_{lb} - \left(\frac{v_{sb} - v_{s0}}{\triangle}\right)\left(P_{lavg} + P_{loss}\right) \\ i_{fc}^* &= i_{lc} - \left(\frac{v_{sc} - v_{s0}}{\triangle}\right)\left(P_{lavg} + P_{loss}\right) \end{aligned}\right\} \tag{2.57}$$

The block diagram of control algorithm of ISC theory is shown in Fig. 2.14. The moving average filter is used for getting average active power from instantaneous value. After getting the reference filter currents from ISC theory, the error is calculated between reference filter currents and actual filter currents injected at PCC. The error is given to hysteresis controller, having inherent hysteresis band to generate the switching signal. If the error is positive, top switch (S_1 or S_3 or S_5) of the leg is ON. If the error is negative, bottom switch (S_4 or S_6 or S_2) of the leg is ON.

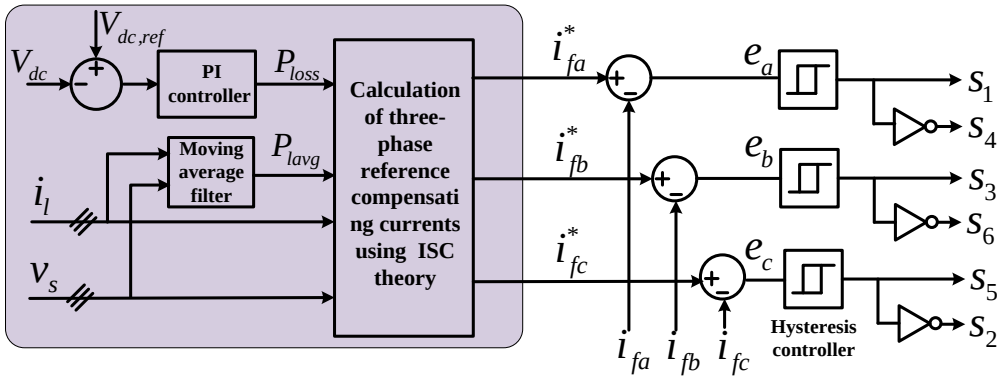


Fig. 2.14 Control algorithm for DSTATCOM with ISC theory

The cost comparison of different DSTATCOM topologies for a rating of 1200 V, 50 A is given in Table 2.2. It is observed that the three-leg DSTATCOM is low cost compared to other topologies, but it is not suitable for 3P4W distribution system. Among other topologies, the three-leg split-capacitor DSTATCOM is comparatively low cost and is suitable for 3P4W distribution system for neutral current compensation. But, the switching losses and the device voltage stress are more in this topology, as discussed in Table 2.1. Therefore, this thesis has sought to look for work to minimize these disadvantages in split-capacitor DSTATCOM and effective utilization of it.

Table. 2.2 Cost comparison of different DSTATCOM topologies for a rating of 1200 V, 50 A

Device name	H-bridge DSTATCOM [22]	3-leg DSTATCOM [32]	Four-leg DSTATCOM [33]	3-leg split-capacitor DSTATCOM [34]
Switches cost	(3*85.48)$	(3*59.11)$	(4*59.11)$	(3*59.11)$
DC capacitors cost	14.12 $	14.12 $	14.12 $	(2*14.12) $
Heat sink cost	(2*70.47)$	70.47$	70.47$	70.47$
Skyper board	(6*148.65)$	(3*148.65)$	(4*148.65)$	(3*148.65)$
Cooling fan	40.52$	40.52$	40.52$	40.52$
Snubber capacitor	(6*10.75)$	(3*10.75)$	(4*10.75)$	(3*10.75)$
Total cost	1408.4$	780.6$	999.2$	794.78$

Reference: https://www.semikron.com.

2.3 Summary

Different DSTATCOM topologies in distribution system for power quality improvement are presented in this chapter. The comparison between these topologies in terms of parameters, device voltage stress, switching losses and cost are tabulated. The design of DSTATCOM parameters: dc-link voltage, dc-link capacitors, interfacing inductance, switching frequency, hysteresis band and rating of VSC are derived. The relationships between these quantities are given and explained in this chapter. Different reference current generation techniques for DSTATCOM operation are discussed. From the discussion, instantaneous symmetrical component theory is selected, and the equations in this method are used in further chapters for the reference current generation.

CHAPTER 3

POWER QUALITY IMPROVEMENT USING SPLIT-CAPACITOR DSTATCOM WITH DYNAMIC DC-LINK VOLTAGE REGULATION

In the previous chapter, different DSTATCOM topologies and the control algorithms were discussed along with reference current generation techniques and design of DSTATCOM parameters. In these topologies, the dc-link voltage is kept constant (i.e., rated value) and this value has been selected based on the rated reactive load condition [24], [27]. Because of that, the switching device voltage stress and switching losses are more during reduced load conditions. Under light load or reduced load conditions, the compensator works perfectly even though the dc-link voltage is reduced from its rated value. Therefore, in this chapter, a variable dc-link voltage method is proposed for dynamic dc-link voltage regulation of DSTATCOM. The proposed algorithm maintains more appropriate value of dc-link voltage corresponding to reactive load condition without compromising the performance of DSTATCOM. Therefore, the voltage stress across the switching devices is reduced during reduced reactive load conditions, which in turn reduces the switching loss and increases inverter reliability. The effectiveness of the proposed method is validated through simulation and experimental studies, which were carried out on the three-leg split-capacitor DSTATCOM. To appraise the proposed method, the conventional method has also been explained.

3.1 Conventional Control Algorithm of Split-Capacitor DSTATCOM

The three-leg split-capacitor DSTATCOM topology in distribution system is shown in Fig. 3.1. In this topology, the three-phase source voltages and source currents are represented as v_{sa}, v_{sb} and v_{sc}, and i_{sa}, i_{sb} and i_{sc}, respectively. DSTATCOM consists of VSC, dc-link capacitors (C_{dc1}, C_{dc2}) and interfacing inductor (L_f), which is connected

at Point of Common Coupling (PCC). During the operation of DSTATCOM, the filter

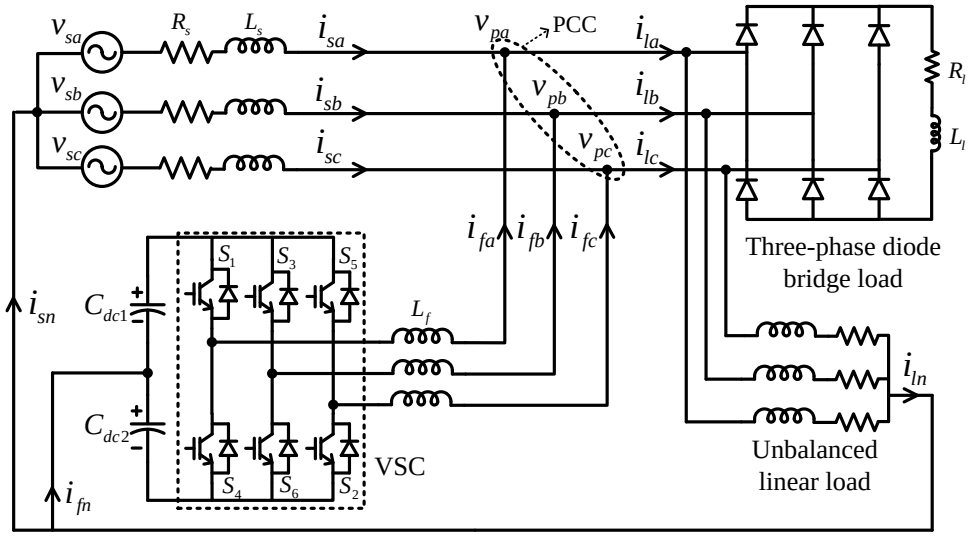


Fig. 3.1 Three-leg split-capacitor DSTATCOM in three-phase distribution system for power quality improvement

currents i_{fa}, i_{fb} and i_{fc} are injected into the system such that source currents become sinusoidal, balanced and in-phase with respective to source voltages. The filter currents injected by DSTATCOM depend on control algorithm, which is explained with the help of single-line diagram of the split-capacitor DSTATCOM as shown in Fig. 3.2.

Initially, the reference filter currents are calculated from Instantaneous Symmetrical Component (ISC) theory, which requires PCC voltages (v_{pa}, v_{pb}, v_{pc}), load currents (i_{la}, i_{lb}, i_{lc}), and average real power (P_{lavg}) drawn by the load [45]. Here, ISC theory is considered for a three-phase four-wire system supplying star-connected load. Then, the reference filter currents are given as,

$$\left.\begin{aligned} i^*_{fa} &= i_{la} - \left(\frac{v_{pa} - v_{p0}}{\Sigma_{j=a,b,c}\, v^2_{pj} - 3v^2_{p0}}\right)(P_{lavg} + P_{loss}) \\ i^*_{fb} &= i_{lb} - \left(\frac{v_{pb} - v_{p0}}{\Sigma_{j=a,b,c}\, v^2_{pj} - 3v^2_{p0}}\right)(P_{lavg} + P_{loss}) \\ i^*_{fc} &= i_{lc} - \left(\frac{v_{pc} - v_{p0}}{\Sigma_{j=a,b,c}\, v^2_{pj} - 3v^2_{p0}}\right)(P_{lavg} + P_{loss}) \end{aligned}\right\} \tag{3.1}$$

where, $v_{p0} = \frac{1}{3}\Big(v_{pa} + v_{pb} + v_{pc}\Big)$, is zero sequence voltage, and P_{loss} indicates the losses in VSC. If P_{loss} is not supplied from the source during compensation, the dc-link voltage will be reduced continuously because of dc-link capacitor discharging. This will deteriorate the performance of the DSTATCOM. To overcome this, the dc-link voltage (V_{dc}) is maintained constant with respect to a fixed reference dc-link voltage (V^*_{dc}) by

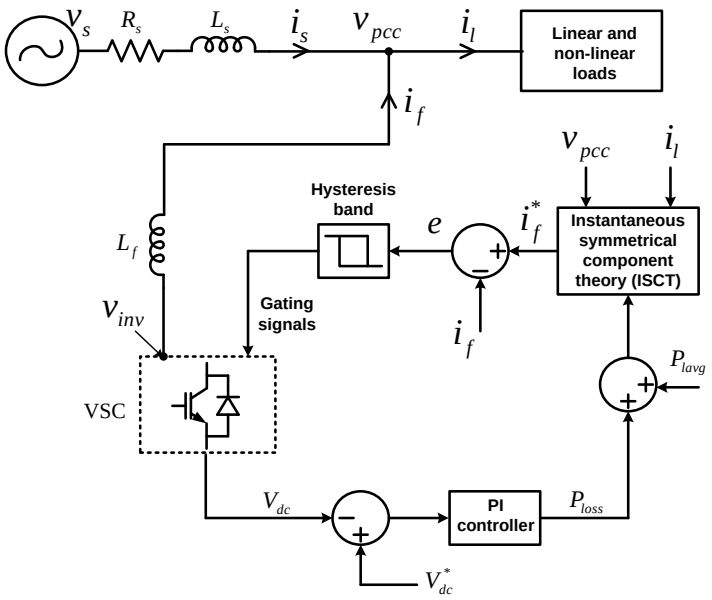


Fig. 3.2 Single-line diagram of split-capacitor DSTATCOM with fixed dc-link voltage (conventional method)

means of Proportional Integral (PI) controller, in which the power loss is supplied from the grid. The output of the PI controller is considered as real power component (P_{loss}), which is included in the control algorithm, as shown in Fig. 3.2. In order to track the reference filter current, hysteresis current control technique is implemented. The input for hysteresis controller is current error (e), which is the difference between the reference filter current (i_f^*) and actual filter current (i_f). Depending on the current error (e), the hysteresis controller generates switching pulses, which are applied to Insulated Gate Bipolar Transistor (IGBT) switches of VSC. According to switching pulses, the DSTATCOM injects filter currents into the system to achieve perfect compensation.

In conventional method, the dc-link voltage is maintained constant throughout compensation, therefore this method can be called as fixed dc-link voltage regulation [24], [27]. In [27], the fixed dc-link voltage is selected as twice the peak of PCC voltage for four-leg DSTATCOM operation. In case of split-capacitor DSTATCOM topology, the upper and lower dc-link voltages are maintained at 1.6 times the peak of PCC voltage individually [24]. The fixed dc-link voltage method increases the device voltage stress and switching losses under reduced load conditions. Therefore, to overcome these problems, a variable dc-link voltage method is proposed, which is explained in the next section.

3.2 Proposed Control Algorithm of Split-Capacitor DSTATCOM

3.2.1 Reference dc-link voltage calculation

In the proposed method, the dc-link voltage is varied dynamically based on load but the maximum dc-link voltage is limited to twice the peak of PCC voltage. This is because, DSTATCOM injects maximum reactive power at $V_{dc} = 2V_{pcc}$, which is explained from the power flow between VSC and PCC. The single-line diagram of power flow circuit of a three-phase system with DSTATCOM is shown in Fig. 3.3. Here, P_s and Q_s are real and reactive powers supplied by the source; P_l and Q_l are real and reactive powers drawn by the load; P_f and Q_f are real and reactive powers injected by DSTATCOM, respectively.

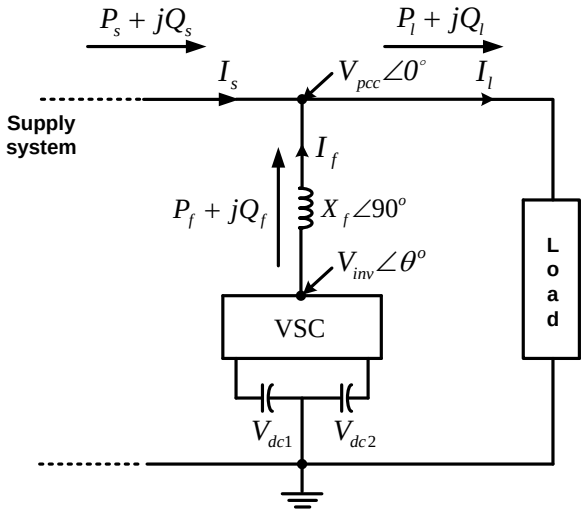


Fig. 3.3 Single-line diagram of power flow circuit of three-phase system

From Fig. 3.3, the current (rms) injected by DSTATCOM is,

$$I_f = \frac{V_{inv}\angle\theta^\circ - V_{pcc}\angle 0^\circ}{X_f\angle 90^\circ} \tag{3.2}$$

and the power injected by DSTATCOM to PCC is,

$$P_f + jQ_f = V_{pcc}I_f \tag{3.3}$$

By substituting (3.2) in (3.3) and rearranging the real and imaginary parts, the obtained

real (P_f) and reactive (Q_f) powers are given below.

$$P_f = \frac{V_{pcc}V_{inv}}{X_f}\sin\theta \tag{3.4}$$

$$Q_f = \frac{V_{pcc}V_{inv}}{X_f}\cos\theta - \frac{V_{pcc}^2}{X_f} \tag{3.5}$$

where, θ is the angle between fundamental output voltage of VSC and PCC voltage. In general, the dc-link voltage design is carried out based on the reactive power injection (Q_f) by DSTATCOM into the system. In power quality applications, the DSTATCOM will not inject any real power into the system; therefore by ignoring the term P_f in (3.4), the calculated θ value is zero. By substituting $\theta = 0^\circ$ in (3.5), the obtained reactive power (Q_f) is,

$$Q_f = \frac{V_{pcc}V_{inv}}{X_f} - \frac{V_{pcc}^2}{X_f} \tag{3.6}$$

In VSC, the ac-side voltage (V_{inv}) and dc-side voltage are related by amplitude modulation index (m_a). That is, V_{inv} is m_a times the dc-side voltage (V_{dc}) of VSC. By substituting, $V_{inv} = m_a V_{dc}$ in (3.6), Q_f is expressed as,

$$Q_f = \frac{V_{pcc}(m_a V_{dc})}{X_f} - \frac{V_{pcc}^2}{X_f} \tag{3.7}$$

It is observed from above equation, that the reactive power (Q_f) is positive when $m_a V_{dc} > V_{pcc}$, which means DSTATCOM injects reactive power to PCC. Depending on the amount of reactive power injected by DSTATCOM, the magnitude of PCC voltage (V_{pcc}) will vary. Therefore, by computing $dQ_f/dV_{pcc} = 0$, the condition for maximum reactive power injected by DSTATCOM is obtained, which is,

$$V_{pcc} = \left(\frac{m_a}{2}\right)V_{dc} \tag{3.8}$$

In (3.8), when m_a value is considered as unity, the dc-link voltage of VSC is equal to twice the peak of PCC (i.e., $V_{dc} = 2V_{pcc}$). Thus, the maximum dc-link voltage is limited to twice the peak of PCC voltage in the proposed method. The maximum reactive power ($Q_{f,max}$) compensated by DSTATCOM is obtained by substituting maximum dc-link

voltage, ($V_{dc} = 2V_{pcc}$) in (3.7) and is given as:

$$Q_{f,max} = \frac{V_{pcc}^2}{X_f} = V_{pcc} I_{f,max} \tag{3.9}$$

where, $I_{f,max} = \frac{V_{pcc}}{X_f}$, is maximum filter current corresponding to $Q_{f,max}$.

In general, the reactive power required by load is not always $Q_{f,max}$. During the reduced reactive load conditions, the required reactive power injection by DSTATCOM is achieved with reduced value of dc-link voltage. The reactive power injected by DSTATCOM depends on dc-link voltage, which can be observed from (3.7). This compels the reduction of the dc-link voltage whenever the reactive load is less than the $Q_{f,max}$, which reduces the voltage stress across the switching devices and switching losses. For that, an algorithm is proposed to calculate the reference dc-link voltage corresponding to reactive load, so that dc-link voltage is forced to maintain this voltage. The procedure for reference dc-link voltage calculation is explained below.

In the case of reduced load condition, the required reactive power injected by DSTATCOM and dc-link voltage are considered as Q_f^* and V_{dc}^*, respectively. From (3.7), Q_f^* is expressed as,

$$Q_f^* = \frac{V_{pcc}(m_a V_{dc}^* - V_{pcc})}{X_f} = V_{pcc} I_f^* \tag{3.10}$$

Where, I_f^* is the reference filter current corresponding to Q_f^*. Using (3.9) and (3.10), I_f^* is expressed in-terms of $I_{f,max}$ and is given below.

$$I_f^* = \frac{(m_a V_{dc}^* - V_{pcc})}{V_{pcc}} I_{f,max} \tag{3.11}$$

After rearranging the above equation, the reference dc-link voltage is expressed as,

$$V_{dc}^* = \frac{V_{pcc}}{m_a}\left(\frac{I_f^* + I_{f,max}}{I_{f,max}}\right) \tag{3.12}$$

3.2.2 Dynamic dc-link voltage regulation method

The single-line diagram of DSTATCOM connected in distribution system with the proposed method is shown in Fig. 3.4. Here, the dc-link voltage is varied dynamically when compared to conventional method shown in Fig. 3.2. In the proposed method,

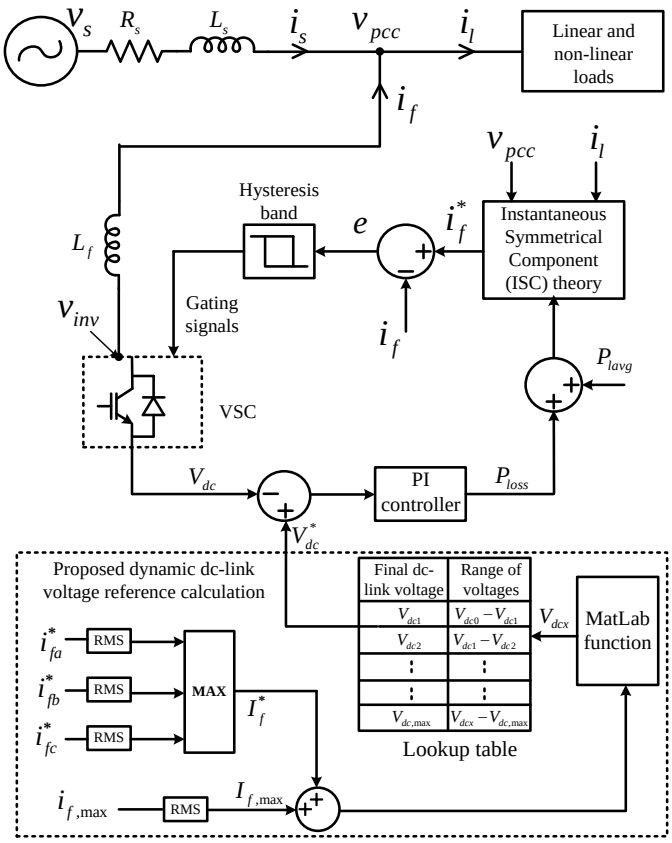


Fig. 3.4 Single-line diagram of split-capacitor DSTATCOM with dynamic dc-link voltage regulation (proposed method)

the calculated reference dc-link voltage (V_{dc}^*) from (3.12) depends on reference filter current. In general, due to frequent changes in load, there will be a change in reference filter currents. Because of that, the proposed method requires a frequent change of reference dc-link voltage, this will affect the performance of DSTATCOM. In order to eliminate this problem, the final dc-link voltage is selected from look-up table in step variations. These step variations are between the minimum and maximum dc-link voltages. If the calculated reference dc-link voltage falls between the specified step variation, then the higher value is selected as final dc-link voltage reference. For better understanding, the dynamic dc-link voltage reference generation is explained with the help of flow-chart which is shown in Fig. 3.5.

First, initialize $V_{dc,max}$ and $I_{f,max}$ corresponding to the rated reactive load. Among three reference filter currents generated from ISCT, the maximum reference filter current is selected to calculate the reference dc-link voltage. If the difference between the maximum filter current $I_{f,max}$ and the reference filter current (I_f^*) is less than voltage tolerance value (ε_v), then the maximum dc-link voltage (i.e., $V_{dc,max} = 2V_{pcc}$) is considered as reference dc-link voltage. Otherwise, the more suitable V_{dc}^* is computed from (3.12) and

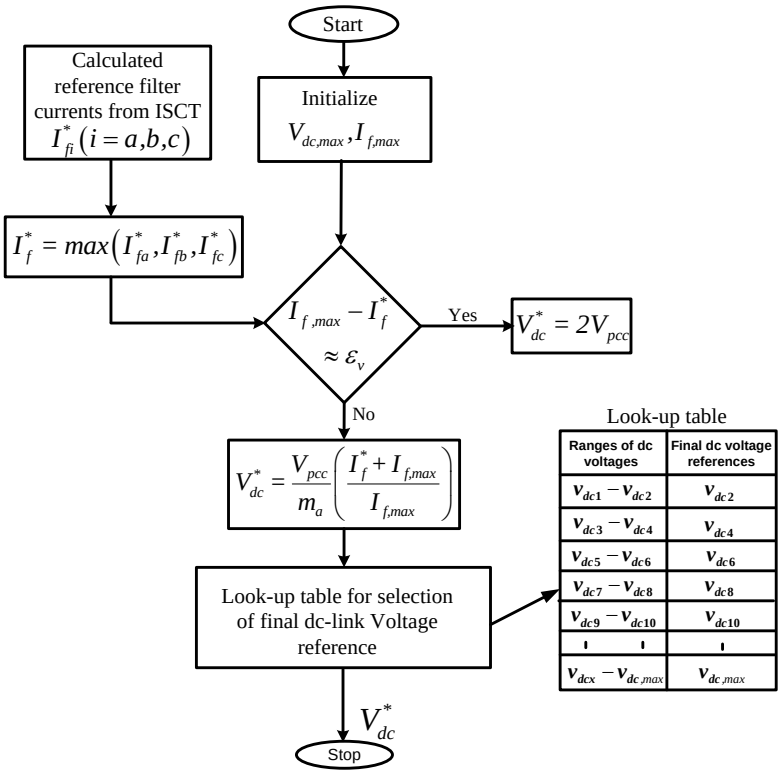


Fig. 3.5 Flow-chart for the selection of reference dc-link voltage

the final value is selected from the look-up table. The advantage of the proposed method is evaluated based on the IGBT switching losses, and the calculation of switching losses is explained below.

3.3 Switching Loss Calculation

The switching (IGBT) loss is calculated from switching frequency (f_{sw}) and energy dissipation (E_{sw}) of the switch, i.e., $P_{sw} = E_{sw} f_{sw}$. The energy dissipation of switch is dependent on the current through switch (I_f), voltage across switch (V_{dc}) during OFF-state and junction temperature (T_j). The energy dissipation under working condition with respect to nominal test condition is calculated from [52], [53] and is given as,

$$E_{sw} = E_{sw,n}\left(\frac{I_f}{I_{f,n}}\right)^{k_i}\left(\frac{V_{dc}}{V_{dc,n}}\right)^{k_v}\left(1 + TC_{sw}(T_j - T_{j,n})\right) \tag{3.13}$$

where, $I_{f,n}$, $V_{dc,n}$, $T_{j,n}$ and energy dissipation $E_{sw,n}$ are reference values at nominal test condition; based on the data sheet of IGBT switch (SKM 75GB123D), k_i is the current dependency (for IGBT ≃ 1, diode ≃ 0.5), k_v is the voltage dependency (for IGBT ≃ 1.2

or 1.4, diode ≃ 0.6), TC_{sw} is the temperature coefficient of switching losses (for IGBT ≃ 0.003, diode ≃ 0.005).

The switching losses are calculated from (4.34) to show the effectiveness of the proposed method and comparison with the conventional method is given in the next section.

3.4 Simulation Studies

In order to verify the proposed dynamic dc-link voltage regulation, simulation is carried out in MATLAB simulink software. The parameters used for simulation studies are given in Table 3.1.

Table. 3.1 Simulation parameters of the system with DSTATCOM for dynamic dc-link voltage regulation method

Symbol	System parameters	Values
V_s	Supply voltage	440 V, 50 Hz
L_f	Interfacing inductance	12 mH
C_{dc1}, C_{dc2}	dc-link capacitances	1600 μF
k_p, k_i	PI controller gains	10, 0.01
h	Hysteresis band	± 0.1 A
V_{dc}	Rated dc-link voltage	1200 V
Load	Unbalanced linear load	a-ph : 20 Ω , 32 mH
	(star connected load)	b-ph : 16 Ω , 42 mH
		c-ph : 10 Ω , 60 mH
	Three-phase diode bridge	36 Ω , 128 mH
	(RL load)	
Non-stiff source parameters: R_s, L_s: 0.8 Ω and 3.5 mH, Ripple filter: 28 Ω and 5 μF.		

The simulation results for both conventional and proposed dynamic dc-link voltage methods are presented here. In simulation results, the variables are named as : PCC voltages (v_p); source currents (i_s); load currents (i_l); filter currents (i_f); source side neutral current (i_{sn}); total dc-link voltage (V_{dc}); voltage across switch (V_{sw}); inverter ac-side line voltage (V_{inv}).

3.4.1 Simulation results under stiff voltage source

The simulation results with conventional split-capacitor DSTATCOM in 3P4W distribution system supplying unbalanced star-connected linear load and three-phase diode bridge load are shown in Fig. 3.6. In order to study the performance of DSTATCOM, the following events are considered to occur in the system for simulation.

1) At t = 0.04 s, an unbalanced star-connected linear load is connected without DSTATCOM.

2) At t = 0.12 s, DSTATCOM is connected to PCC.

3) At t = 0.3 s, load is increased by connecting three-phase diode bridge with *RL*-load.

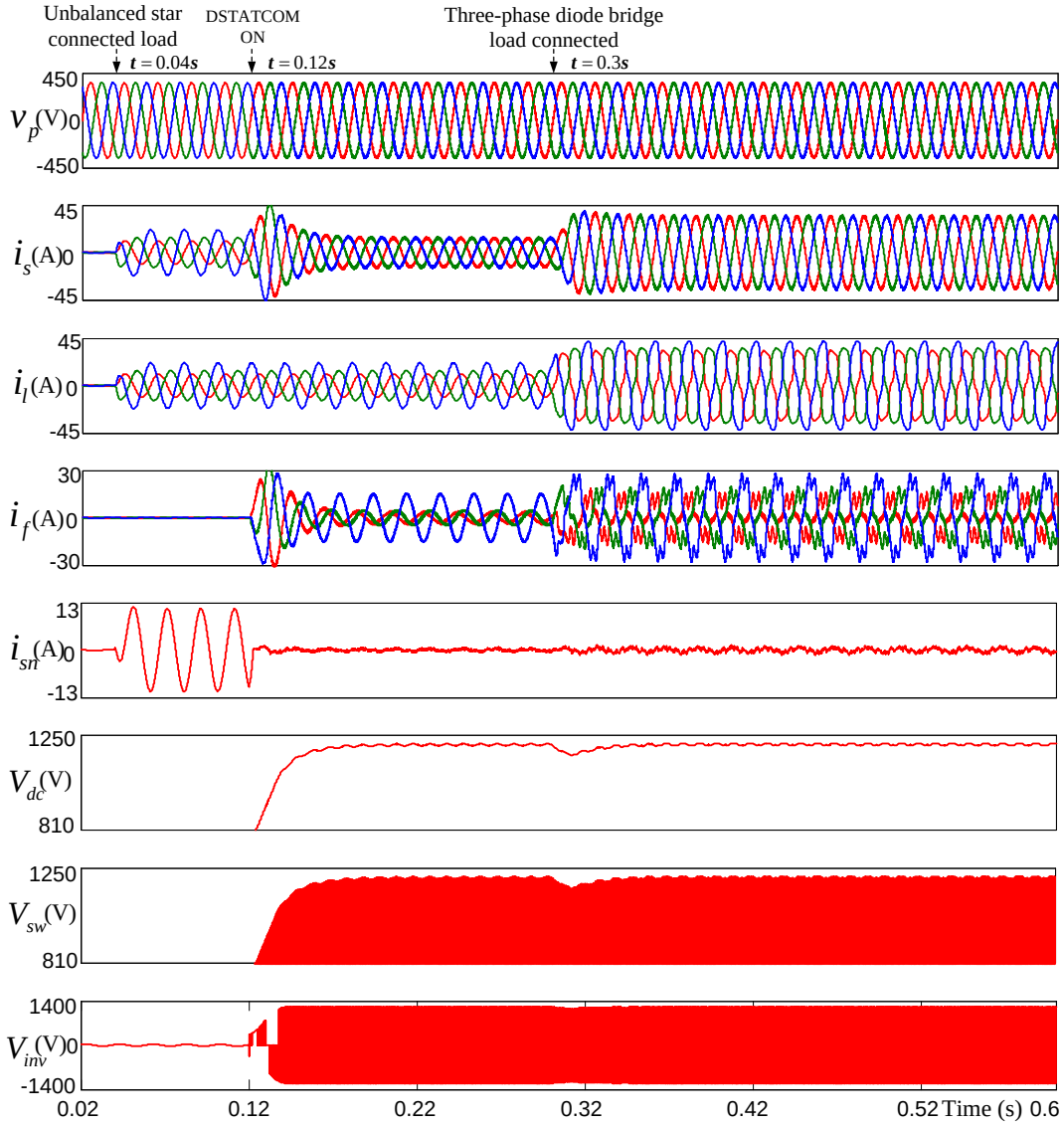


Fig. 3.6 Performance of DSTATCOM with fixed dc-link voltage regulation (conventional method)

It is observed from Fig. 3.6 that during the period between t = 0.04 s to t = 0.12 s,

the load and source currents are same, and the unbalance load current flow through neutral conductor. At t = 0.12 s, DSTATCOM is connected at PCC and compensation started, therefore the three-phase source currents become balanced, sinusoidal and in-phase with corresponding PCC voltages. As the three-phase source currents are balanced, the source side neutral current becomes zero. The dc-link capacitors are charged to fixed reference dc-link voltage (i.e., 1200 V) by PI controller loop. At t = 0.3 s, the load is increased by connecting three-phase diode bridge load; during this load condition also the dc-link voltage is maintained to 1200 V. It is observed from the waveforms that the voltage across the switch (V_{sw}) and the magnitude of voltage across inverter ac-side line voltage (V_{inv}) are maintained fixed for both the load conditions, because of fixed dc-link voltage regulation. From the above simulation studies, it is concluded that, in conventional fixed dc-link voltage method, the voltage across switch is constant (i.e., equal to 1200V) irrespective of the load variation. It leads to high voltage stress across the switching devices during reduced or light loaded conditions. This problem is addressed in the proposed method and to show the effectiveness of proposed dynamic dc-link voltage regulation method, the same simulation events (i.e., in conventional method) are considered.

The simulation waveforms with the proposed dynamic dc-link voltage regulation are shown in Fig. 3.7. It is observed from Fig. 3.7, that during the DSTATCOM operation, the source currents become sinusoidal, balanced and in-phase with PCC voltages. If the load is increased by connecting a three-phase diode bridge load at t = 0.3 s, the compensation is not affected. The required dc-link voltages for both the load conditions are calculated from the proposed method and are given in Table 3.2.

Table. 3.2 Calculated reference dc-link voltages corresponding to the loads

Type of connected load	Load current (A)			Filter current (A)			Conventional	Proposed (V^*_{dc})	
	I_{la}	I_{lb}	I_{lc}	I^*_{fa}	I^*_{fb}	I^*_{fc}	(V^*_{dc})	#Cal	+Final
Unbalanced linear load	7.5	10	16	2.2	3.4	10.4	1200 V	868 V	880 V
Unbalanced plus diode bridge loads	24.5	26.8	31	8.7	11.6	18	1200 V	961 V	980 V

#Cal: calculated value from (3.12), +Final: selected from the look-up table.

In case of unbalanced star-connected linear load, the required dc-link voltage is computed from (3.12) as 868 V. However, the final dc-link voltage is selected from the

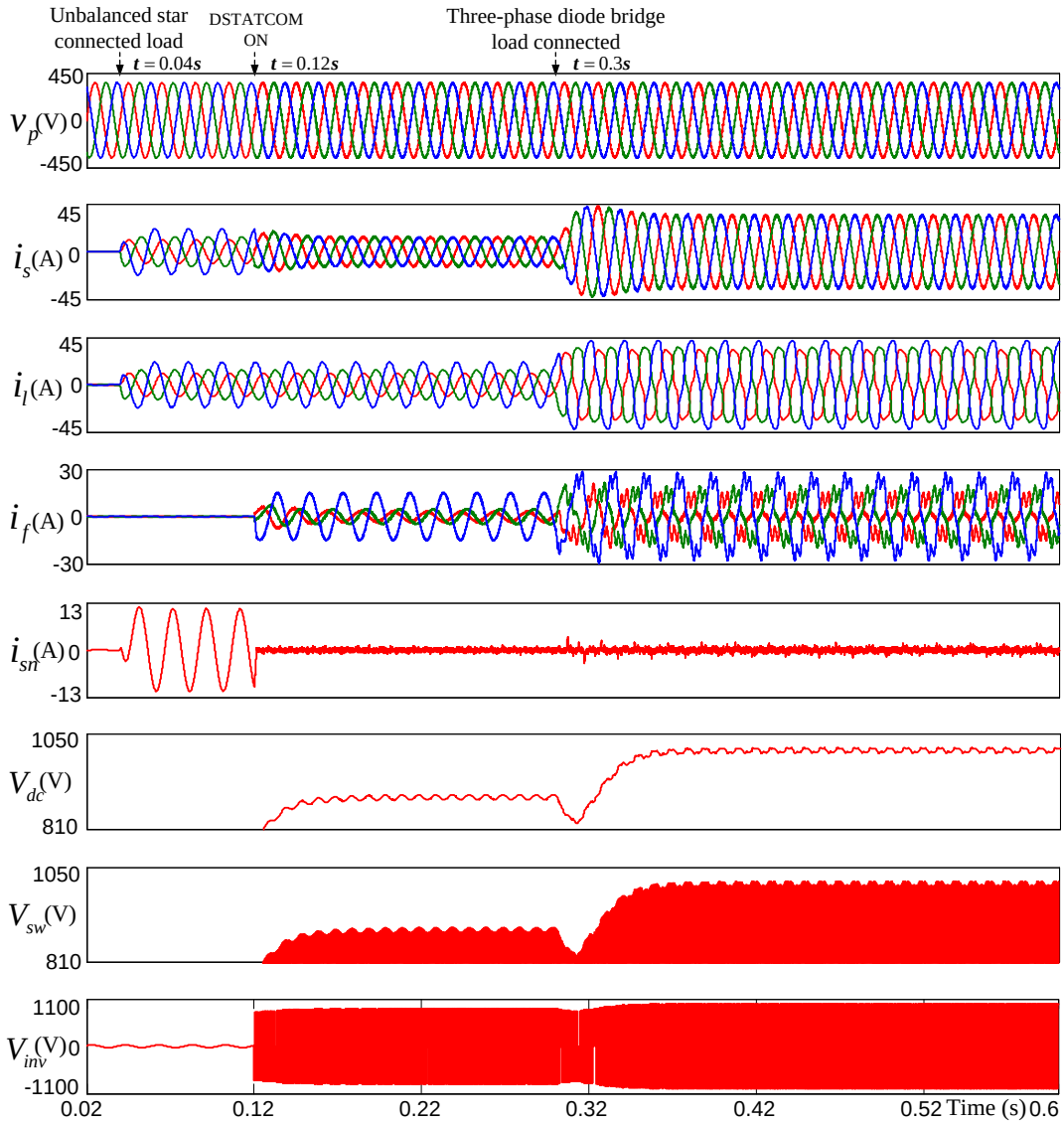


Fig. 3.7 Performance of DSTATCOM with dynamic dc-link voltage regulation (proposed method)

look-up table, which is equal to 880 V. At t = 0.3 s, the load is increased by connecting a three-phase diode bridge, then the dc-link voltage is computed from the proposed algorithm is 961 V. But, the final dc-link voltage is selected from look-up table, which is equal to 980 V. The same voltage magnitude will appear across the switching device, which is labeled as V_{sw}. This shows that the dc-link voltages (i.e., 880 V and 980 V) in the proposed method are low when compared to dc-link voltage of 1200 V in fixed dc-link voltage regulation (conventional method).

The variation of switching energy dissipation with respect to variation of dc-link voltage and filter current, is shown in Fig. 3.8. It is observed that in the proposed method for the filter current of 18 A and dc-link voltage of 980 V, the switching energy dissipation is 6.27 mJ, which is less when compared to 9.09 mJ in conventional method for the

same load condition. The energy dissipation and switching loss are related by switching frequency, that is $P_{sw} = f_{sw}E_{sw}$. Therefore, the corresponding switching loss (P_{sw}) in the proposed method is 31.35 W, which is less when compared to 45.48 W in conventional method.

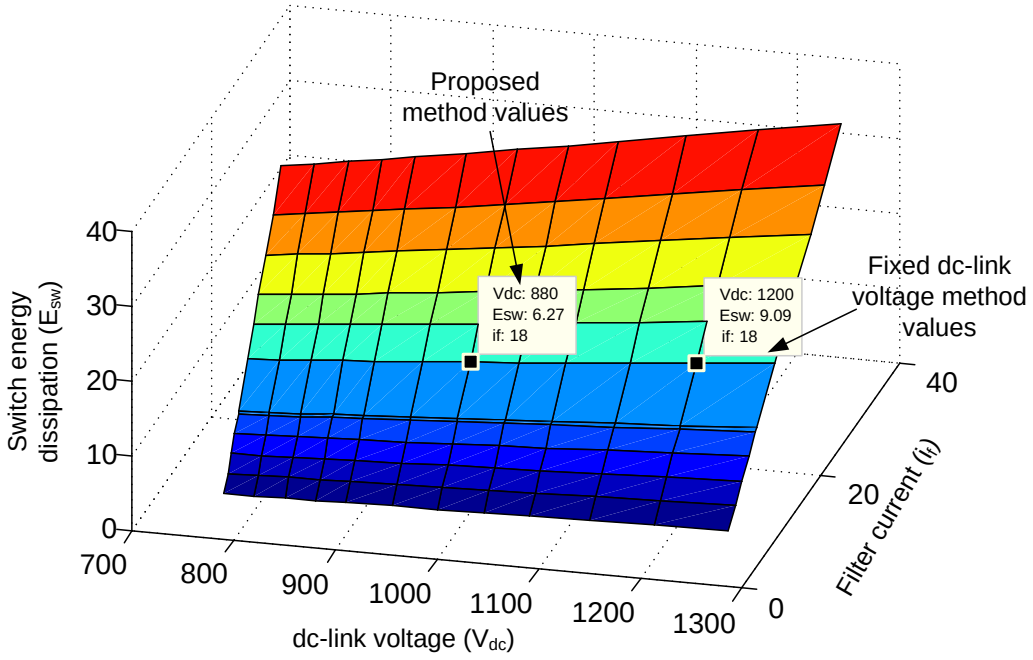


Fig. 3.8 Variation of energy dissipation of switch with respect to dc-link voltage and filter current

3.4.2 Simulation results under non-stiff voltage source

The considered non-stiff source parameters for simulation are given in Table 3.1. For the considered non-stiff source, the simulation results in conventional and proposed method are shown in Fig. 3.9(a) and Fig. 3.9(b), respectively. It is observed from Fig. 3.9(a) that, before DSTATCOM connection, PCC voltages are distorted and non-sinusoidal. After DSTATCOM is ON at t = 0.06 s, the PCC voltages and source currents become sinusoidal and in-phase with the corresponding PCC voltages. Initially, the dc-link capacitors are charged to 85% of rated dc-link voltage to improve starting performance. After DSTATCOM is ON, the total dc-link voltage is maintained at 1200 V with fixed dc-link voltage regulation loop.

It is observed from the proposed results shown in Fig. 3.9(b), that the compensation performance in case of PCC voltage and source current are the same as that of conventional method. During the transient period, that is DSTATCOM is ON at t = 0.06 s,

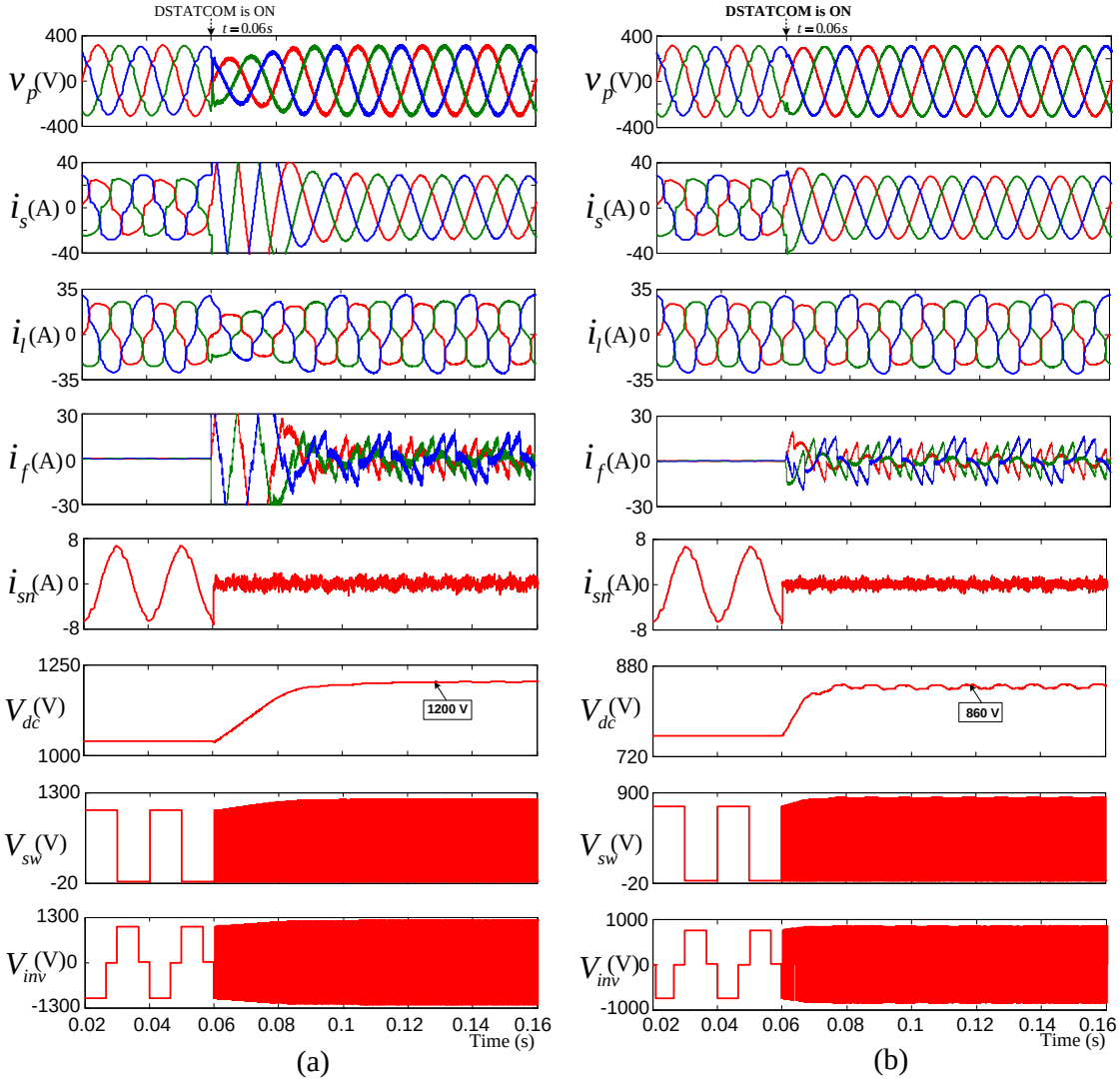


Fig. 3.9 Simulation results with non-stiff voltage source (a) fixed dc-link voltage method and (b) dynamic dc-link voltage method

the magnitude of source and filter currents are high and it takes more time to settle in conventional method when compared to the proposed method because of higher dc-link voltage. Initially, the dc-link capacitor is charged to 65% of rated dc-link voltage. When DSTATCOM is ON at t = 0.06 s, the dc-link voltage is maintained at 860 V, which is derived from the proposed adaptive dc-link voltage regulation method. Therefore, the voltage stress appearing across switch is 860 V in proposed method, which is less when compared to 1200 V in conventional method.

3.5 Experimental Studies

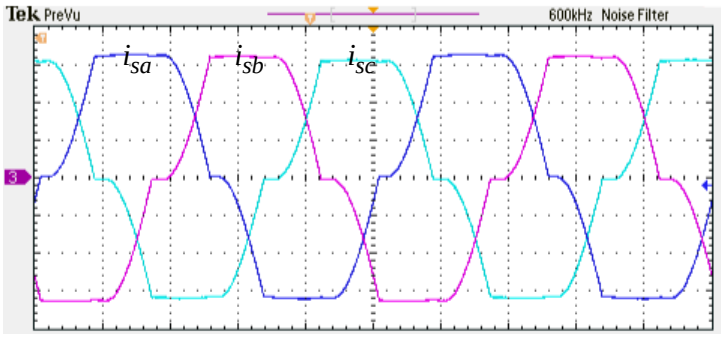
The performance of the proposed dynamic dc-link voltage regulation method is also verified with experimental studies. dSPACE DS-1202 is used to implement the control algorithm of DSTATCOM. The experimental parameters are given in Table 3.3. The experimental setup consists of three-leg split-capacitor voltage source converter with IGBTs as switching devices. The required feedback signals such as PCC voltages, load currents, filter currents and dc-link voltages are measured using Hall-effect voltage and current transducers. dSPACE DS-1202 acquires current and voltage signals from transducers and processes to generate reference filter currents, reference dc-link voltage and thereby switching signals to IGBTs. The switching command signals are taken out from the master I/O pins of dSPACE and are given to converter switches with proper isolation.

Table. 3.3 Experimental parameters for dynamic dc-link voltage regulation method

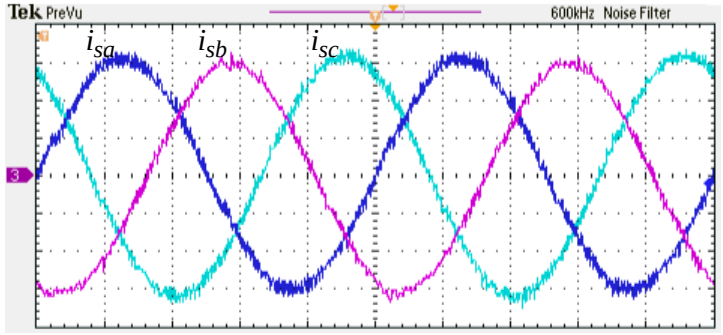
Symbol	System parameters	Values
V_s	Supply voltage	110 V (L-L)
L_f	Interfacing inductance	26 mH
C_{dc1}, C_{dc2}	dc-link capacitances	3600 μF each
k_p, k_i	PI controller gains	20, 0.04
h	Hysteresis band	± 0.2 A
Load-1	3-phase diode bridge load	22 Ω, 48 mH
Load-2	Unbalanced linear load	a-ph : 18 Ω , 18 mH
		b-ph : 14 Ω , 32 mH
		c-ph : 14 Ω , 25 mH
V_{dc}	Rated dc-link voltage	145 V each

3.5.1 Steady state performance of the proposed dynamic dc-link voltage regulation method

The steady state performance for harmonic mitigation, reactive power compensation and three-phase source currents balancing is tested in the presence of three-phase non-linear diode bridge with *RL*-load and unbalanced load. Before compensation, the three-phase source currents with only non-linear diode bridge load are shown in Fig. 3.10(a). It is observed that, the source currents are non-sinusoidal and distorted because of non-linear nature of load. After compensation, the three-phase source currents become sinu-



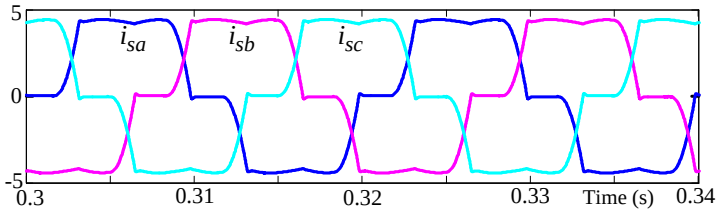
(a)



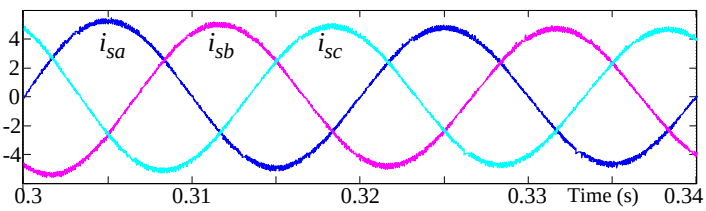
(b)

Fig. 3.10 Experimental waveforms of three-phase source currents (i_{sa}, i_{sb}, i_{sc}) for non-linear diode bridge load condition (a) before compensation and (b) after compensation (scale: current 1 A/div)

soidal and balanced and are shown in Fig. 3.10(b). For the same power rating condition, the simulation results from before and after compensation are shown in Fig. 3.11(a) and Fig. 3.11(b), respectively. It is observed that the simulation and experimental results are almost equal for the same power rating condition.



(a)



(b)

Fig. 3.11 Simulation waveforms of three-phase source currents (i_{sa}, i_{sb}, i_{sc}) for non-linear diode bridge load condition (a) before compensation and (b) after compensation

During the above operation, the phase-a source current, dc-link voltages (V_{dc1}, V_{dc2}) and phase-a load current are shown in Fig. 3.12. The individual dc-link voltage required for this load condition is 105 V, calculated from the proposed method and maintained by a PI controller. For this power rating condition, the simulation results are shown in Fig. 3.13. It is observed from Fig. 3.12 and Fig. 3.13 that the experimental and simulation results are almost equal for the same power rating condition.

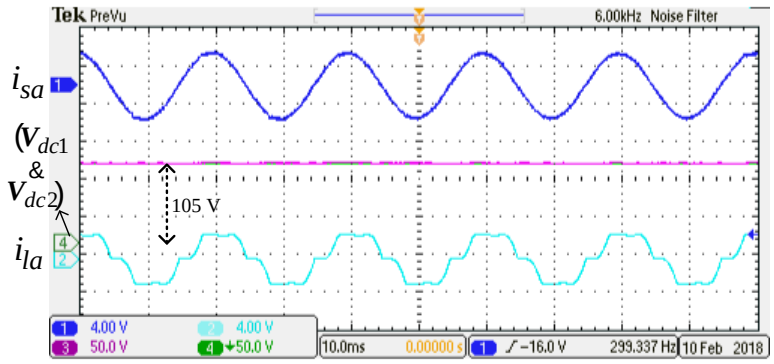


Fig. 3.12 Experimental waveforms of phase-a source current (i_{sa}), dc-link voltages (V_{dc1}, V_{dc2}) and phase-a load current (i_{la}) for non-linear load condition (scale: current 4 A/div, voltage 50 V/div)

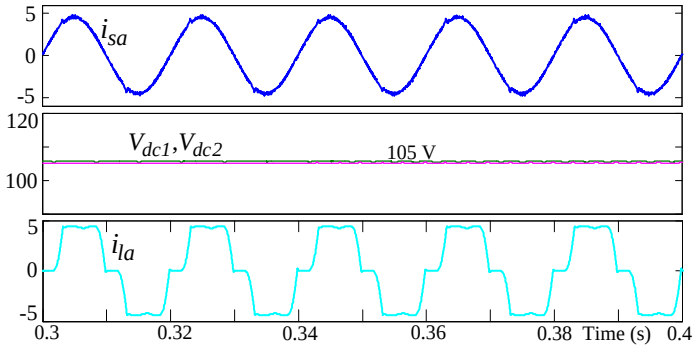
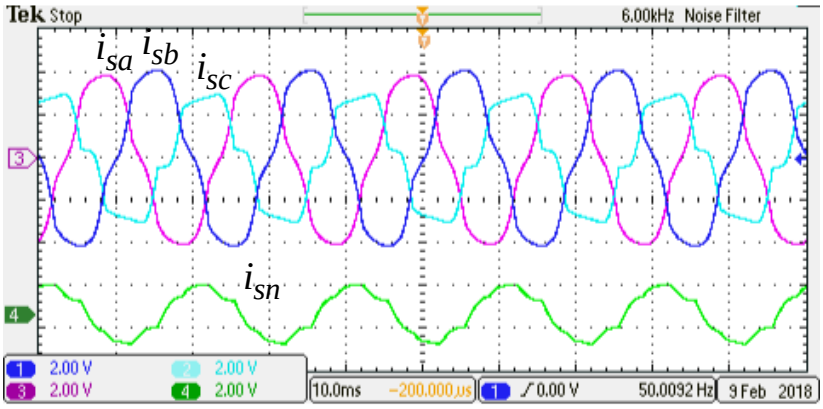


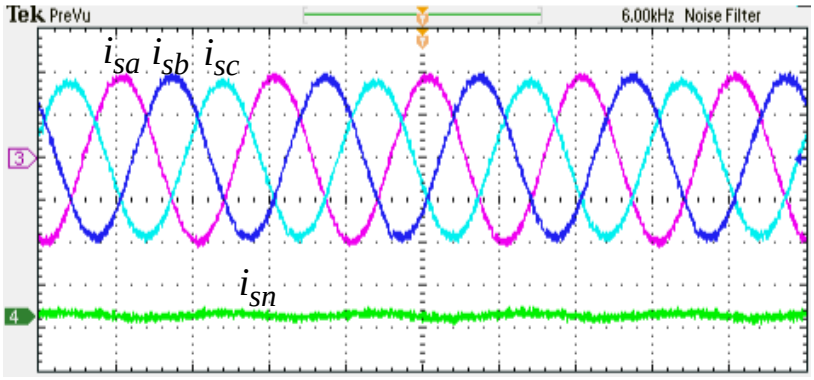
Fig. 3.13 Simulation waveforms of phase-a source current (i_{sa}), dc-link voltages (V_{dc1}, V_{dc2}) and phase-a load current (i_{la}) for non-linear load condition

Similarly, for unbalanced non-linear load condition, the three-phase source currents and source side neutral current before compensation are shown in Fig. 3.14(a). It is observed that, the three-phase source currents are non-sinusoidal, distorted and unbalanced, therefore neutral current is present. After compensation, the source currents are shown in Fig. 3.14(b). It is observed that the source currents become sinusoidal, balanced and thereby the neutral current at source side becomes zero.

During the unbalanced non-linear load condition, phase-a source current, dc-link voltages (V_{dc1}, V_{dc2}) and phase-a load current are shown in Fig. 3.15. The individual dc-link



(a)



(b)

Fig. 3.14 Experimental waveforms of three-phase source currents (i_{sa}, i_{sb}, i_{sc}) and source side neutral current (i_{sn}) for unbalanced non-linear load condition (a) before compensation and (b) after compensation (scale: current 2 A/div)

voltage required for this load condition is 140 V, calculated from the proposed method and maintained by a PI controller.

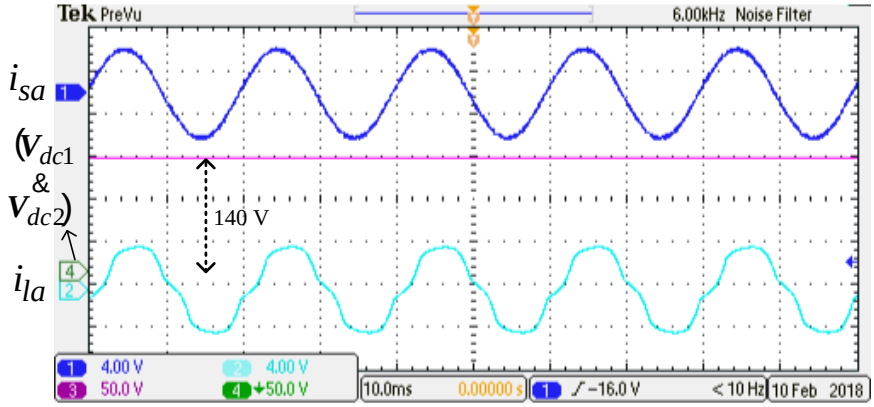


Fig. 3.15 Phase-a source current (i_{sa}), dc-link voltages (V_{dc1}, V_{dc2}) and phase-a load current (i_{la}) for unbalanced non-linear load condition (scale: current 4 A/div, voltage 50 V/div)

The harmonic spectra of three-phase source currents before compensation are shown in

Fig. 3.16. Before compensation, the THDs of three-phase source currents are 20.2%, 20.6% and 20.1%, respectively. After compensation, the harmonic spectra of three-phase source currents are shown in Fig. 3.17. It is observed that, the source currents THDs are reduced to 3.6%, 4.1% and 3.8%, respectively. These THD values are well within the IEEE-519 recommended standard value (i.e., less than 5%).

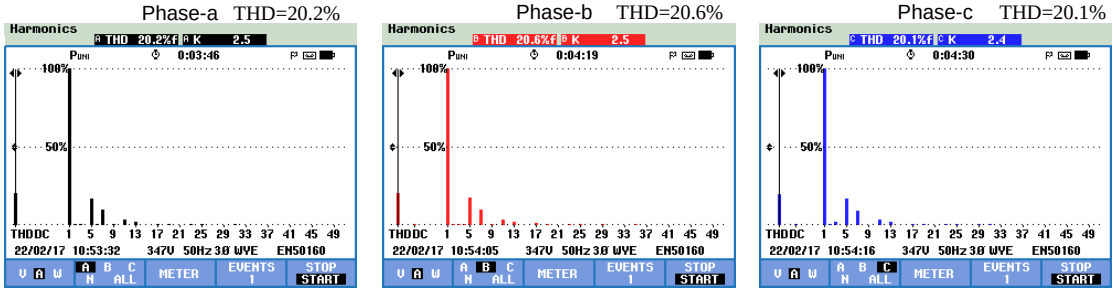


Fig. 3.16 Before compensation the harmonic spectra of three-phase source currents for non-linear diode bridge load condition

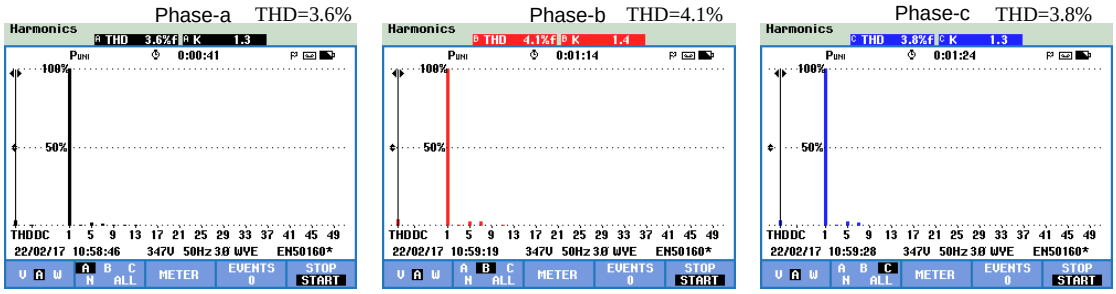


Fig. 3.17 After compensation the harmonic spectra of three-phase source currents for non-linear diode bridge load condition

The phasor diagram of PCC voltages and source currents for non-linear diode bridge load before compensation are shown in Fig. 3.18. It is observed that the three-phase source currents lag behind the respective phase voltages by 15°, 15° (255-240) and 16° (136-120), and corresponding fundamental source current magnitudes are 1.9 A, 1.8 A and 1.9 A. The phasor diagram of PCC voltages and source currents after compensation are shown in Fig. 3.19. It is observed that the source currents are in-phase with respective PCC voltages, and the corresponding fundamental source current magnitudes are 1.8 A, 1.8 A and 1.8 A. This shows that unity power factor is achieved on the source side and three-phase source currents are balanced.

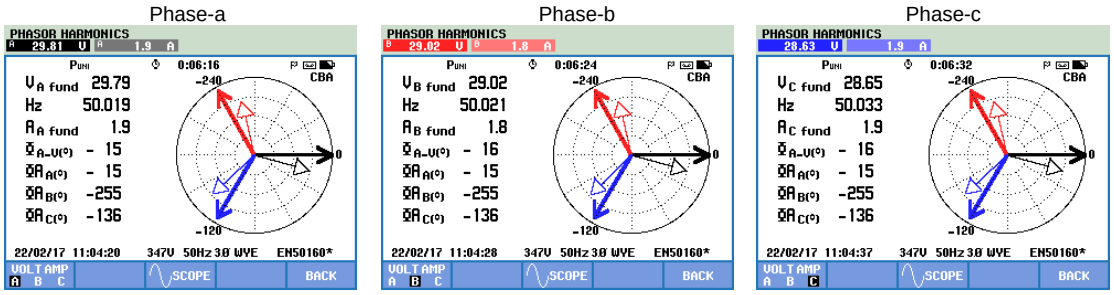


Fig. 3.18 Before compensation the phasor diagram of three-phase PCC voltages and source currents for non-linear diode bridge load condition

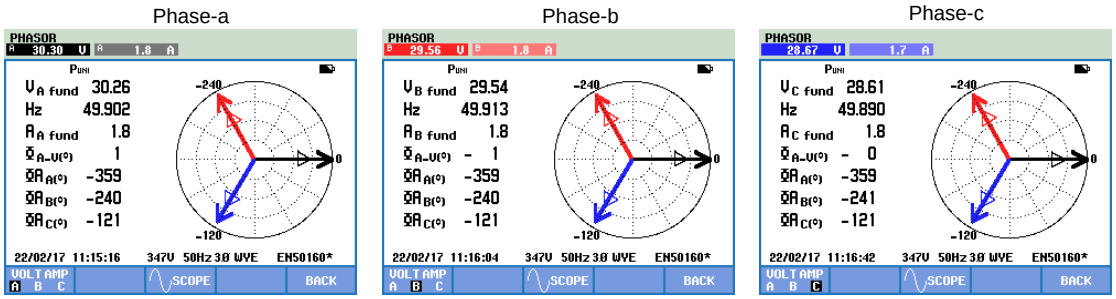
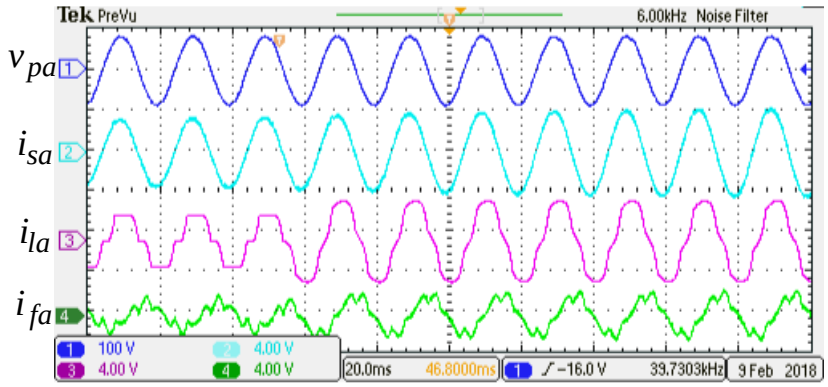


Fig. 3.19 After compensation the phasor diagram of three-phase PCC voltages and source currents for non-linear diode bridge load condition

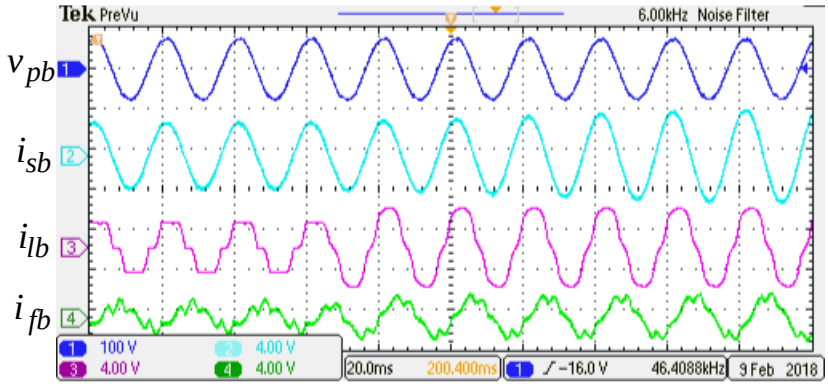
3.5.2 Transient performance of the proposed dynamic dc-link voltage regulation method

The proposed dynamic dc-link voltage regulation for DSTATCOM has been tested under transient load condition for harmonic mitigation, reactive power compensation and source currents balancing. In this case, the load is increased by connecting an additional three-phase unbalanced linear load to the previous non-linear diode bridge load. In both the load conditions, the PCC voltage, source current, load current and filter current of individual phases are shown in Fig. 3.20. It is observed that the source currents are sinusoidal and in-phase with respective PCC voltages even for transient load variation.

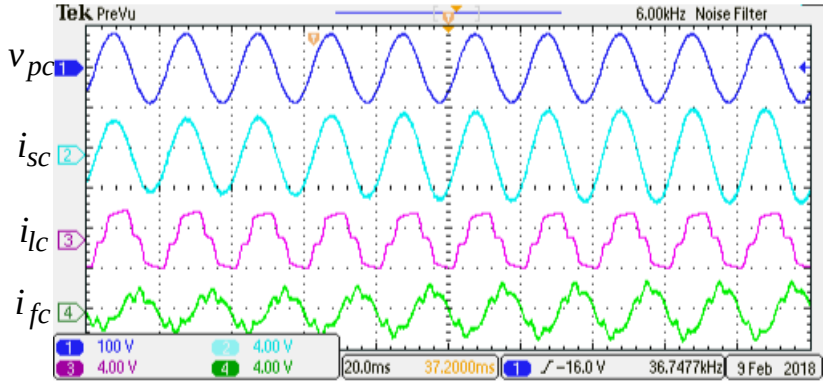
Before compensation, three-phase source currents and source side neutral current during transient load variation are shown in Fig. 3.21(a). It is observed that the source currents are non-sinusoidal, distorted, unbalanced while neutral current is flowing for load-2 condition. After compensation, the source currents become sinusoidal and balanced, and thereby neutral current becomes zero shown in Fig. 3.21(b). For the same power rating, the simulation results for before and after compensation are shown in Fig. 3.22(a) and Fig. 3.22(b), respectively.



(a)



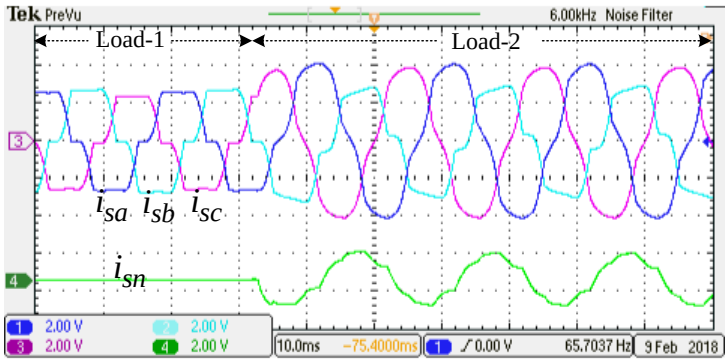
(b)



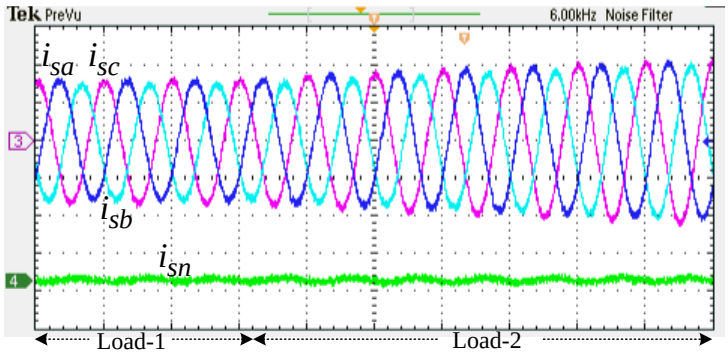
(c)

Fig. 3.20 PCC voltages (v_{pa}, v_{pb}, v_{pc}), source currents (i_{sa}, i_{sb}, i_{sc}), load currents (i_{la}, i_{lb}, i_{lc}) and filter currents (i_{fa}, i_{fb}, i_{fc}) for transient load variation with the proposed method (a) phase-*a* (b) phase-*b* and (c) phase-*c* (scale: voltage 100 V/div, current 4 A/div)

During the above operation of transient load variation from load-1 to load-2, the phase-*a* source current, dc-link voltages (V_{dc1}, V_{dc2}) and phase-*a* load current are shown in Fig. 3.23. The individual dc-link voltages required for load-1 and load-2 conditions are 105 V and 140 V, respectively. These dc-link voltages are calculated from the proposed method and are maintained by PI controller. These dc-link voltage magnitudes appear across the switches. In case of conventional split-capacitor DSTATCOM, the total dc-

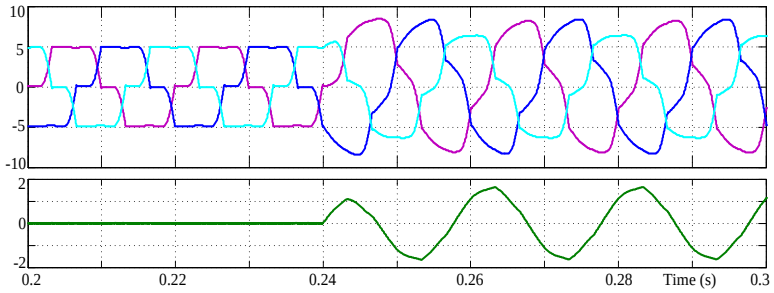


(a)

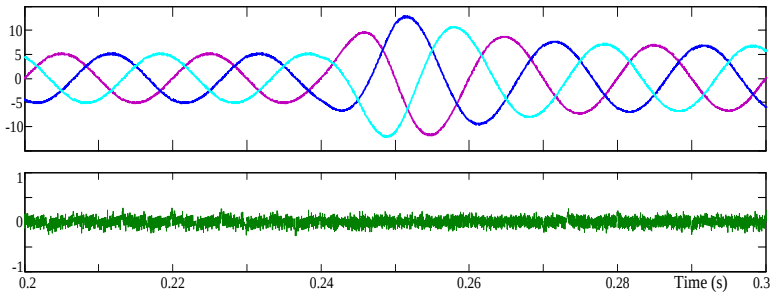


(b)

Fig. 3.21 Experimental waveforms of three-phase source currents (i_{sa}, i_{sb}, i_{sc}) and source side neutral current (i_{sn}) for load-1 and load-2 (a) before compensation and (b) after compensation (scale: current 2 A/div)



(a)



(b)

Fig. 3.22 Simulation waveforms of three-phase source currents (i_{sa}, i_{sb}, i_{sc}) and source side neutral current (i_{sn}) for load-1 and load-2 (a) before compensation and (b) after compensation

link voltage is maintained at 160 V (i.e., 1.6 times peak of PCC voltage across each dc-link capacitor) independent on the load condition. Because of that, in the proposed method, the voltage stress across switches is reduced to 105 V and 140 V for the same load conditions. It leads to reduction of switching losses. For the same power rating condition, the simulation results during load variation are shown in Fig. 3.24. It is observed from Fig. 3.24 and Fig. 3.23 that the simulation and experimental results are almost equal for the same power rating condition.

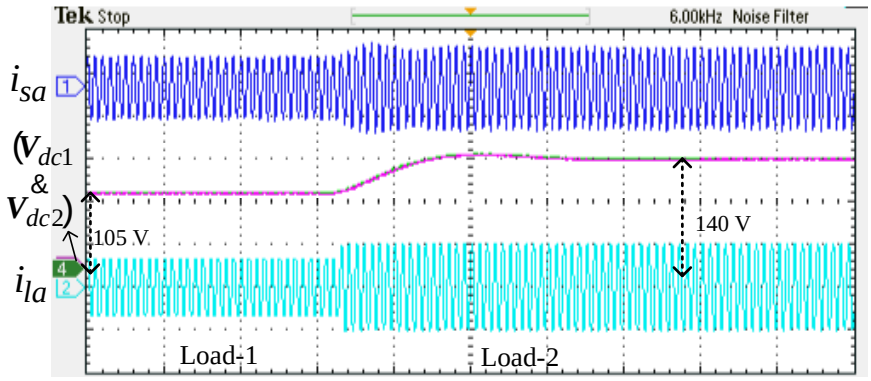


Fig. 3.23 Experimental waveforms of phase-*a* source current (i_{sa}), dc-link voltages (V_{dc1}, V_{dc2}) and phase-*a* load current (i_{la}) for transient load variation (scale: current 4 A/div, voltage 50 V/div)

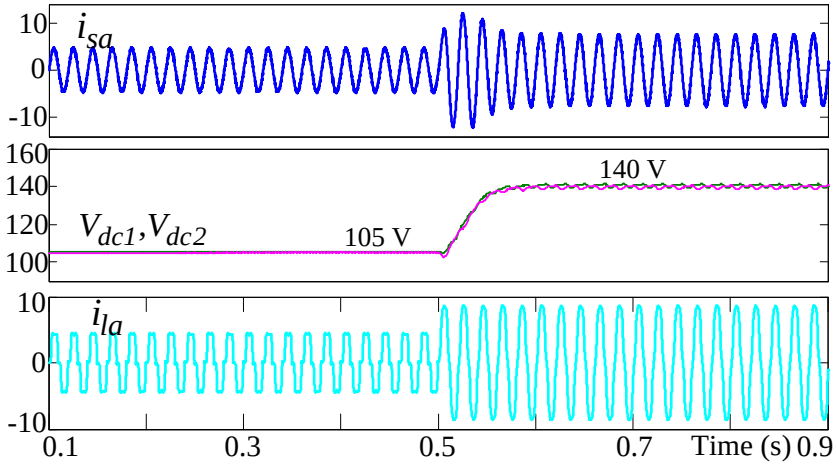


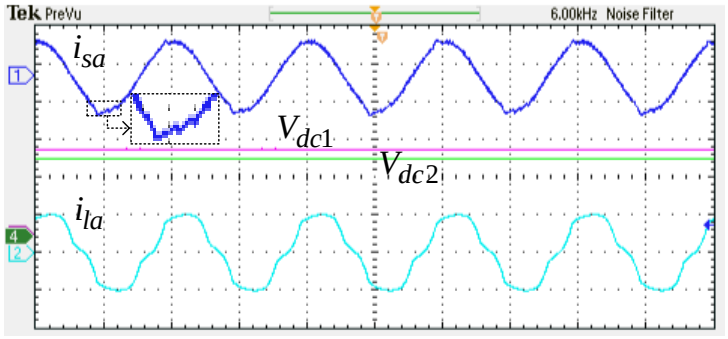
Fig. 3.24 Simulation waveforms of phase-*a* source current (i_{sa}), dc-link voltages (V_{dc1}, V_{dc2}) and phase-*a* load current (i_{la}) for transient load variation

3.5.3 Balancing of dc-link voltages

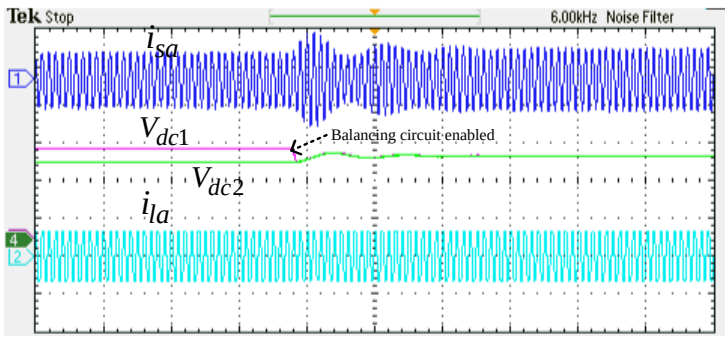
In split-capacitor DSTATCOM topology, the two dc-link voltages deviate from equal value due to off-set present in the circuit operation or measurement parameters or un-equal switching of devices in the same leg. The need for balancing capacitors and

its effect on compensation is explained here, with the inclusion of off-set present in measured load current. The phase-a source current, dc-link voltages (V_{dc1}, V_{dc2}) and phase-a load current during unbalanced load condition are shown in Fig. 3.25. It is observed from the zoomed part of the source current in Fig. 3.25(a), that the compensation performance is affected during negative cycle because lower dc-link voltage (V_{dc2}) is reduced and is lower than required dc-link voltage. Fig. 3.25(b) shows the results before and after dc-link voltage balancing circuit is enabled. After voltage balancing, the lower dc-link voltage (V_{dc2}) is increased, upper dc-link voltage (V_{dc1}) is reduced to the required value and both reach the same voltage value.

The experimentally obtained %THD of three-phase source currents for load-1 and load-2 conditions, before compensation and after compensation, in conventional and the proposed methods are shown in Table 3.4. It is observed that after compensation the %THDs in the proposed method are lower when compared to conventional method, and in both the cases %THDs are less than 5% (IEEE-519 standard).



(a)



(b)

Fig. 3.25 Phase-a source current (i_{sa}), dc-link voltages (V_{dc1}, V_{dc2}) and phase-a load current (i_{la}) during unbalanced non-linear load condition (a) before voltage balancing and (b) after voltage balancing

Table. 3.4 THDs of source currents in conventional and proposed methods

Type of load		Before compensation (%THD)	After compensation (%THD)	
			Conventional	Proposed
*Load-1	i_{sa1}	20.2	4.6	3.6
	i_{sb1}	20.6	4.5	4.1
	i_{sc1}	20.1	4.4	3.8
#Load-2	i_{sa2}	10.1	3.9	3.1
	i_{sb2}	10.9	4.2	3.2
	i_{sc2}	14.0	3.8	3.6

*Load-1: three-phase non-linear diode bridge load, #Load-2: unbalanced non-linear load.

3.6 Advantages and disadvantages of existing and proposed methods

In the proposed method, the dc-link voltage is varied, such that the switching voltage stress and losses are reduced when compared to existing methods. The advantages and disadvantages of existing methods in literature and the proposed method for power quality improvement are given in Table 3.5.

3.7 Summary

This chapter presents an algorithm of dynamic dc-link voltage regulation for DSTATCOM to compensate unbalanced and non-linear loads in 3P4W distribution system. The performance of the proposed dynamic dc-link voltage method has been investigated through simulation and experimental studies. It is observed that the proposed method compensates the reactive power, source current harmonics and neutral current with dynamic dc-link voltage variations. A significant amount of reduction in switching losses with the proposed method is observed when compared to the conventional method. The voltage stress across the switching devices also reduced, which in turn extends the life-span of the switching devices.

Table. 3.5 Advantages and disadvantages of existing and proposed methods for power quality improvement

Topologies	Advantage	Disadvantage
Singh B [27]	• Better compensation at full load.	• Higher dc-link voltage (i.e., two times peak of PCC voltage). • Switching losses are more.
Mishra M K [54]	• Better compensation performance. • dc-link voltage is reduced to 1.6 times peak of PCC voltage.	• Switching losses are more during reduced or light load condition.
Lam CS [55], [56]	• Reactive power compensation with optimum dc-link voltage. • Switching losses are reduced.	• Limited to reactive power and fifth harmonic compensation. • It requires three extra ac capacitors. • Resonance problem.
Lam CS [57]	• Reduced dc-link voltage. • Switching losses are reduced.	• More number of switches required. • Complex control and cost high.
Wei T [58]	• Low cost. • DSTATCOM rating is low.	• More number of switches. • Higher rating of Thyristor Switched Capacitors (TSC) required. • Compensation fails in the presence of dc off-set in load current.
Proposed method	• Dynamic dc-link voltage regulation. • Switching losses are minimized. • Easy to implement the control algorithm.	• During full load condition, the switching losses are high when compared to hybrid reduced dc-link voltage topologies [56]–[58].

CHAPTER 4

POWER QUALITY IMPROVEMENT USING *LCL*-FILTER BASED DSTATCOM

In the previous chapter, power quality improvement by DSTATCOM with dynamic dc-link voltage regulation method is implemented. In which, the VSC of DSTATCOM is connected at PCC through an interfacing unit consists of high value of inductance (i.e., *L*-filter). Due to high value of inductance, the size of filter is bulky and it is also expensive.

In this chapter, the design of *LCL*-filter DSTATCOM based on the switching dynamics of controller is implemented for smooth reference tracking. The total interfacing inductance value required in *LCL*-DSTATCOM is low when compared to *L*-filter based DSTATCOM. The lower value of interfacing inductance reduces the voltage drop and thus the required dc-link voltage is also reduced. Further, a control algorithm to operate *LCL*-DSTATCOM in both Current Control Mode (CCM) and Voltage Control Mode (VCM) is proposed.

4.1 Introduction

The conventional *L*-filter based DSTATCOM requires high value of interfacing inductance to attenuate switching frequency components generated by Voltage Source Converter (VSC). As the inductance value is high, the voltage drop across it is also high; therefore the required dc-link voltage for satisfactory compensation is more. In [59], DSTATCOM with series *LC*-filter is presented, in which the voltage across the series capacitor supports the inverter ac side voltage, and then the required dc-link voltage is decreased. The impedance offered by capacitor of *LC*-filter for switching frequency components is almost zero. Therefore, the interfacing inductance required to attenuate switching frequency components is the same in both *L*-filter and *LC*-filter based DSTATCOMs.

The expensive and bulky *L*-filter is replaced by higher order *LCL*-filter with low inductance value for better current tracking. The design of *LCL*-filter parameters for different applications are presented in literature. In [60], an analytical design procedure of *LCL*-filter in active rectifier applications is proposed for the elimination of switching frequency. Later, many authors proposed *LCL*-filter design in grid connected applications [61]–[65]. However, only a few authors have discussed the *LCL*-filter for Shunt Active Power Filter (SAPF) applications, and these are summarized in Table 4.1.

Table. 4.1 Literature review on *LCL*-filter based DSTATCOM topologies

Author	Application/ Topology	Purpose	Observation
Yi Tang, *et al.* [66]	High performance shunt active power filter (Three-phase three-wire topology)	1) SAPF provides better filtering without using large passive components. 2) This method has high slew rate for accurate harmonic compensation without entering over modulation mode during transient. 3) Harmonic currents compensated up to 25^{th} order.	1) Active damping is considered. 2) PCC voltages are considered as sinusoidal and balanced. 3) Grid and converter side inductances are equal.
Qian Liu, *et al.* [67]	Shunt active power filter (Single-phase topology)	1) Proposed an optimized design method of *LCL*-filter parameters based on graphical approach. 2) Harmonic currents compensated up to 49^{th} order. 3) Attenuation co-efficient is introduced to decouple the mutual relation between the filter parameters and the SAPF performance indices.	1) Active damping is considered. 2) This method eliminates repeated trial and error method in the design process.
Nagesh Geddada, *et al.* [68]	DSTATCOM with PI and HC regulators (Three-phase four-wire split-capacitor topology)	1) Compensation of unbalanced nonlinear load. 2) Harmonic currents compensated up to 19^{th} order. 3) Allowable ripple current by converter side inductor and grid side inductor are 25% and 5% of rated filter current, respectively.	1) Passive damping is considered. 2) The converter side inductance is double the value of grid side inductance.
Mihaela Popescu, *et al.* [69]	Shunt active power filter in active DC-traction substation (Three-phase three-wire topology)	1) A new design method for *LCL*-filter parameter is proposed. 2) Power loss in damping resistor is also considered for design criteria. 3) Harmonic currents compensated up to 51^{th} order.	1) Passive damping is considered. 2) Magnitude Performance Indicator (MPI) and power losses indicator are considered to analyze the filter performance.

The resonance problem associated with *LCL*-filter can be minimized by active damping [66], [67], [70], [71] or passive damping [60], [61], [68], [69], [72] methods and they are addressed in literature. An experimental comparative study between *LCL*-filter and *L*-filter based SAPFs is presented in [73]. This study lacks the conceptual explanation

of *LCL*-filter design criteria. A repetitive control scheme coupled to a one-beat-delay current controller is proposed for *LCL*-filter based SAPF [74]. Even though this controller exhibits fine dynamic and steady state performance, the design of *LCL*-filter and resonance damping are not specifically addressed. Proper design and configuration of the *LCL*-filter parameters for DSTATCOM applications is a crucial and sensitive task. This is because, the DSTATCOM is ideally designed to operate within the possible wide frequency bandwidth of the load.

The modes of operation for the designed *LCL*-DSTATCOM are discussed here. DSTATCOM operating in CCM for reactive power compensation and current harmonics mitigation is discussed in [75]–[78]. In CCM operation, reference filter currents (direct control) or reference source currents (indirect control) are generated to control source currents. In [79], [80], DSTATCOM is operated in VCM for voltage profile improvement, where DSTATCOM regulates load voltage to the reference voltage value by supplying appropriate fundamental reactive current to the source. In the above algorithms [75]–[80], either current control or voltage control is achieved, but not both. In [81], both CCM and VCM modes of operation by DSTATCOM are presented. In this method, both CCM and VCM of operations are achieved by generating reference filter currents and reference PCC voltages, respectively. In the proposed method, both current and voltage control are achieved by generating reference PCC voltages only.

4.2 *LCL*-filter based DSTATCOM Topology in Distribution System

The schematic diagram of the *LCL*-filter based split-capacitor DSTATCOM in distribution system is shown in Fig. 4.1. The source is represented by v_{sa}, v_{sb} and v_{sc} with feeder resistance and inductance as R_s and L_s, respectively. v_{pk}, i_{sk}, i_{lk} and i_{fk} are the voltage at PCC, source current, load current and filter current, respectively, where $k = a, b$ and c phases. C_{dc1} and C_{dc2} are dc-link capacitors of VSC, which support energy exchange. L_{fi} and L_{fg} are inverter side and grid side interfacing inductors, having internal resistances R_{fi} and R_{fg}, respectively. C_r is capacitor of *LCL*-filter and r_d is damping resistor.

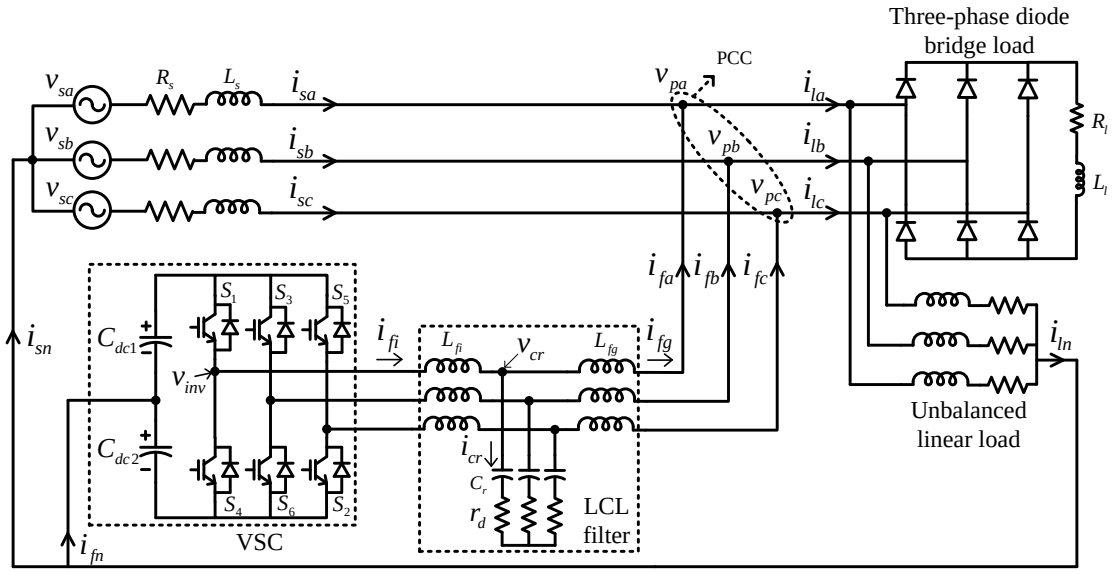


Fig. 4.1 Schematic diagram of *LCL*-filter based DSTATCOM connection in three-phase four-wire (3P4W) distribution system for power quality improvement

Design of *LCL*-filter parameters:

The *LCL*-filter parameters are designed based on the switching dynamics of controller, and the harmonic order to be compensated by DSTATCOM, which is explained here. Fig. 4.2 shows the switching dynamics of the hysteresis controller, and in which the dotted line represents reference filter current (i_{fref}) while the solid line represents actual filter current (i_{fact}) varying between hysteresis band ($\pm\, h$). The analysis is carried out by considering time instants t_1, t_1' and t_1'' with corresponding reference filter currents of i_{fref}, i'_{fref} and i''_{fref}, respectively.

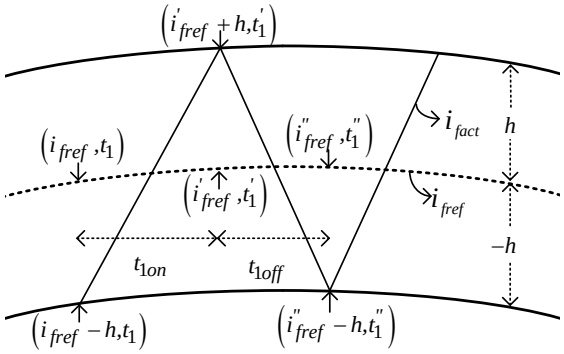


Fig. 4.2 Switching dynamics of controller for *LCL*-filter design

From Fig. 4.2, the rate of change of actual filter current during rising and falling slopes

of the current are,

$$\left.\begin{aligned}\frac{\mathrm{d}i_{fact}}{\mathrm{d}t_{on}} &= \frac{(i'_{fref} - i_{fref}) + 2h}{t_{on}} \\ \frac{\mathrm{d}i_{fact}}{\mathrm{d}t_{off}} &= \frac{(i''_{fref} - i'_{fref}) - 2h}{t_{off}}\end{aligned}\right\} \tag{4.1}$$

During the conduction of upper switches of VSC, the upper dc-link capacitor voltage is supported. Similarly, the lower dc-link capacitor voltage supports during conduction of lower switches of VSC. Applying Kirchoff Voltage Law (KVL) from VSC to PCC gives the following equations:

$$\left.\begin{aligned}m_a V_{dc} - V_m \sin\omega t &= L_{fi}\frac{\mathrm{d}i_{fi}}{\mathrm{d}t_{on}} + L_{fg}\frac{\mathrm{d}i_{fg}}{\mathrm{d}t_{on}} + R_{fi}i_{fi} + R_{fg}i_{fg} \\ -m_a V_{dc} - V_m \sin\omega t &= L_{fi}\frac{\mathrm{d}i_{fi}}{\mathrm{d}t_{off}} + L_{fg}\frac{\mathrm{d}i_{fg}}{\mathrm{d}t_{off}} + R_{fi}i_{fi} + R_{fg}i_{fg}\end{aligned}\right\} \tag{4.2}$$

where, m_a is amplitude modulation index. The total internal resistance ($R_{fi} + R_{fg}$) of inductors L_{fi} and L_{fg} is considered as R_f. The current (i_{cr}) flowing through capacitor (C_f) is small in magnitude, so that for simplicity of calculation i_{cr} is neglected. Then, currents i_{fi} and i_{fg} are equal and it is considered as i_{fact}. With the above considerations, (4.2) becomes,

$$\left.\begin{aligned}m_a V_{dc} - V_m \sin\omega t &= (L_{fi} + L_{fg})\frac{\mathrm{d}i_{fact}}{\mathrm{d}t_{1on}} + R_f i_{fact} \\ -m_a V_{dc} - V_m \sin\omega t &= (L_{fi} + L_{fg})\frac{\mathrm{d}i_{fact}}{\mathrm{d}t_{1off}} + R_f i_{fact}\end{aligned}\right\} \tag{4.3}$$

After simplification of (4.1) and (4.3), the turn-on and turn-off periods of switch are obtained as,

$$t_{on} = \frac{2h(L_{fi} + L_{fg})}{m_a V_{dc} - V_m \sin\omega t - i_{fact}R_f} \tag{4.4}$$

$$t_{off} = \frac{2h(L_{fi} + L_{fg})}{m_a V_{dc} + V_m \sin\omega t + i_{fact}R_f} \tag{4.5}$$

From (4.4) and (4.5), the calculated switching frequency (f_{sw}) is,

$$\left.\begin{aligned}f_{sw} &= \frac{1}{t_{on} + t_{off}} \\ &= \frac{1}{4h(L_{fi} + L_{fg})}\left(m_a V_{dc} - \frac{V_m^2}{m_a V_{dc}}\sin^2\theta\right)\end{aligned}\right\} \tag{4.6}$$

where, $\theta = \omega t$. The observations from (4.6) are,

1. The switching frequency (f_{sw}) is maximum when $V_m \sin\theta$ is zero.
2. f_{sw} is minimum when $V_m \sin\theta$ is maximum.

In general, interfacing inductances are designed for maximum switching frequency, therefore from (4.6),

$$f_{sw,max} = \frac{m_a V_{dc}}{4h(L_{fi} + L_{fg})} \tag{4.7}$$

$$L_{fi} + L_{fg} = \frac{m_a V_{dc}}{4h f_{sw,max}} \tag{4.8}$$

The rated dc-link voltage in the proposed *LCL*-DSTATCOM is considered as 550 V (for 400 V supply voltage), amplitude modulation index (m_a) is unity, hysteresis band (h) is assumed to be 5% of rated filter current and $f_{sw,max}$ is assumed as 10 kHz. After substituting these values in (4.8), the sum of inductances, $L_{fi} + L_{fg}$ value is 13.75 mH.

From Fig. 4.1, the dynamic equations of *LCL*-DSTATCOM are given in (4.9), and its block diagram is shown in Fig. 4.3.

$$\left.\begin{aligned} i_{fi}(s) = \frac{v_{inv}(s) - v_{cr}(s)}{R_{fi} + sL_{fi}},\ i_{fg}(s) = \frac{v_{cr}(s) - v_{pcc}(s)}{R_{fg} + sL_{fg}} \\ v_{cr}(s) = r_d i_{cr}(s) + \frac{i_{cr}(s)}{sC_r}, \quad i_{cr}(s) = i_{fi}(s) - i_{fg}(s) \end{aligned}\right\} \tag{4.9}$$

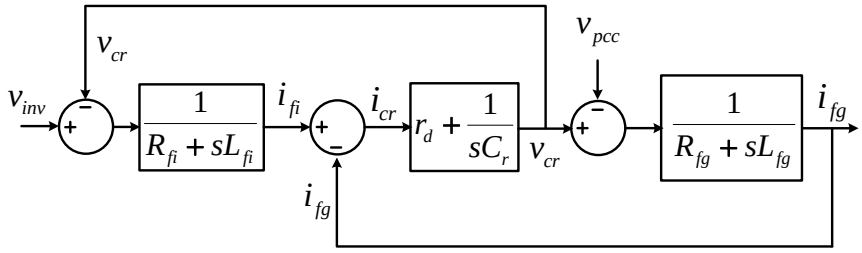


Fig. 4.3 Block diagram representation of *LCL*-filter based system

The transfer function $i_{fg}(s)/v_{inv}(s)$ of the system from Fig. 4.3 is given as,

$$\frac{i_{fg}}{v_{inv}} = \frac{1 + sr_d C_r}{B_0 s^3 + B_1 s^2 + B_2 s + B_3}, \tag{4.10}$$

where, $B_0 = L_{fi}L_{fg}C_r,\ B_1 = R_{fi}C_r L_{fg} + L_{fi}C_r R_{fg} + L_{fi}r_d C_r + r_d C_r L_{fg}, B_2 = R_{fi}R_{fg}C_r +$

$R_{fg}r_dC_r + r_dC_rR_{fi}C_f + L_{fi} + L_{fg}B_3 = R_{fi} + R_{fg}$. To simplify the analysis, internal resistances R_{fi} and R_{fg} are neglected. This is a valid assumption because the resistance values are very small and their influence on the stability of the system is limited. If damping resistance (r_d) is not provided, the transfer function (4.10) becomes:

$$\frac{i_{fg}}{v_{inv}} = \frac{1}{L_{fi}L_{fg}C_rs^3 + (L_{fi} + L_{fg})s}. \tag{4.11}$$

Applying unity feedback control for (4.11) gives overall closed loop system, and characteristic equation of closed loop system is,

$$L_{fi}L_{fg}C_rs^3 + (L_{fi} + L_{fg})s + 1 = 0 \tag{4.12}$$

The s^2 term is missing in the closed-loop characteristic equation (4.12), which indicates the unstable nature of the system according to Routh Hurwitz stability criterion. Therefore, damping is necessary to stabilize the system.

The resonance frequency expression from (4.11) is,

$$f_r = \frac{1}{2\pi}\sqrt{\frac{L_{fi} + L_{fg}}{L_{fi}L_{fg}C_r}}. \tag{4.13}$$

In (4.13), the resonance frequency is selected based on the harmonic order to be compensated by *LCL*-DSTATCOM. Here, the highest order harmonic to be compensated by DSTATCOM is selected as 49^{th} order for 50 Hz supply system with 10 % variation. As a trade-off between the above requirements, the value of C_r is chosen as 8 μF. Therefore, the product of $L_{fi}L_{fg}$ value from (4.13) is given as,

$$L_{fi}L_{fg} = \frac{L_{fi} + L_{fg}}{\omega_r^2C_r}. \tag{4.14}$$

By substituting the values $(L_{fi} + L_{fg})$, ω_r^2 and C_r in (4.14), $L_{fi}L_{fg}$ value is 0.829×10^{-6}. The difference between two inductances in terms of sum and product of inductors is,

$$L_{fi} - L_{fg} = \sqrt{(L_{fi} + L_{fg})^2 - 4L_{fi}L_{fg}} \tag{4.15}$$

From $(L_{fi} + L_{fg})$ and $(L_{fi} - L_{fg})$ values, the individual value of L_{fi} and L_{fg} are obtained

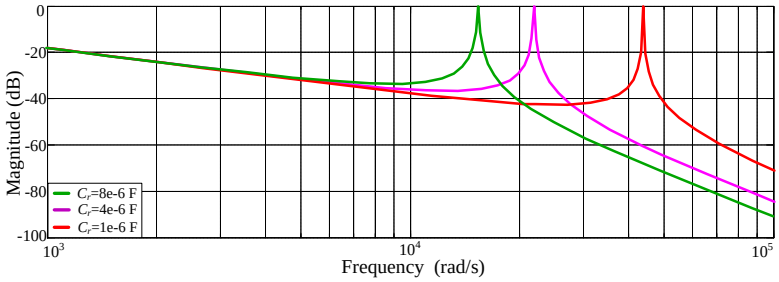
as 13.63 mH, 0.12 mH, respectively. For the designed inductance values, the *LCL*-filter frequency response is analyzed by varying C_r and r_d.

The frequency response for different values of C_r is shown in Fig. 4.4(a). It is observed that the resonance frequency increases with decreasing C_r value, which results in allowing switching frequency components to grid. Therefore, the selected C_r value (i.e., 8 μF) is most suitable for compensation. The frequency response of *L*-filter, and *LCL*-filter with different passive damping values are shown in Fig. 4.4(b). The *LCL*-filter introduces a resonant peak if damping resistor is absent, which causes instability of the system. The resonant peak can be damped by using passive damping resistor r_d in series with capacitor (C_r) as shown in Fig. 4.1. It is observed that when increasing r_d value, the resonance peak reduces, which makes the system stable. Above the resonance frequency (i.e., 49*50 = 2450 Hz), the attenuation of switching frequency harmonics is high in *LCL*-filter when compared to *L*-filter.

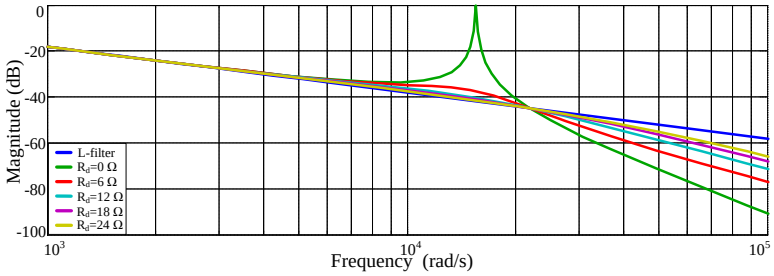
The comparison between *L*-filter and *LCL*-filter in terms of inductance value, attenuation of switching frequency components and resonance peak occurrence for different damping resistances is given in Table 4.2. It is clear from Fig. 4.4(b) and Table 4.2 that for r_d = 6 Ω, there is no resonance peak and the attenuation is more after resonance frequency. Therefore, a damping resistance (r_d) value of 6 Ω is chosen in the proposed method.

Table. 4.2 Comparison between *L*-filter and *LCL*-filter

Parameter	*L*-filter	*LCL*-filter
Total interfacing inductance value	26 mH	14 mH
Resonance peak occurrence		
for C_r = 8 μF	No resonance peak	2463 Hz
C_r = 4 μF		3485 Hz
C_r = 1 μF		6972 Hz
Harmonic attenuation after resonance frequency		
for r_d = 0 Ω	-18 db, and independent on r_d	-60 db
r_d = 6 Ω		-46 db
r_d = 12 Ω		-32 db
r_d = 18 Ω		-28 db
r_d = 24 Ω		-26 db



(a)



(b)

Fig. 4.4 Frequency response of LCL-filter (a) for different C_r values without damping (i.e., $r_d = 0\ \Omega$) and (b) for different r_d values when $C_r = 8\ \mu$F

4.3 Operation of LCL-DSTATCOM in Current and Voltage Control Modes

The operation of LCL-DSTATCOM in CCM and VCM with the proposed control algorithm is explained here. The relation among source voltage (V_s), PCC voltage (V_{pcc}) and load current (I_l) without connecting DSTATCOM is given as,

$$I_l\angle{-\alpha} = \frac{V_s\angle\delta - V_{pcc}\angle 0}{Z_s\angle\theta} \tag{4.16}$$

Without DSTATCOM, the source current is the same as load current; therefore (4.16) can also be written as,

$$I_s\angle{-\alpha} = \frac{V_s\angle\delta - V_{pcc}\angle 0}{Z_s\angle\theta} \tag{4.17}$$

where, α is angle between PCC voltage and source current. After simplification of (4.17), the below equation is obtained.

$$\left.\begin{aligned}(V_{pcc} + I_sZ_s\cos(\theta-\alpha))^2 + (I_sZ_s\sin(\theta-\alpha))^2 = V_s^2\\ V_{pcc}^2 + (I_sZ_s)^2 + 2V_{pcc}I_sZ_s\cos(\theta-\alpha) = V_s^2\end{aligned}\right\} \tag{4.18}$$

where, Z_s is source impedance and is equal to $\sqrt{R_s^2 + X_s^2}$. To measure source impedance, different schemes are present in literature [82], [83]. During compensation with DSTATCOM, only real component of the load current flows between source and PCC point, and the source current is in-phase with PCC voltage. Therefore, in (4.18), α becomes zero. The above equation (4.18) is second order quadratic equation in V_{pcc}. Therefore, the solution for (4.18) is given as,

$$V_{pcc} = \sqrt{V_s^2 - (I_s Z_s \sin\theta)^2} - I_s Z_s \cos\theta \tag{4.19}$$

It is observed from (4.19) that, the PCC voltage (load voltage) magnitude can be decreased by increasing the source current (i.e., I_s value), and the maximum reduction occurs at the allowed rated source current. Depending on the value of PCC voltage (V_{pcc}) calculated from (4.19), the mode of operation of DSTATCOM is selected. The reference PCC voltages (v_{pcc}^*) generation in CCM and VCM modes of operation is explained below.

4.3.1 Reference voltage generation for CCM mode

The estimated source currents i_{sa}, i_{sb} and i_{sc} are calculated from Instantaneous Symmetrical Component (ISC) theory and they are given as follows [24].

$$\left.\begin{aligned} i_{sa} &= \frac{v_{pa} - v_{p0}}{\sum_{j=a,b,c} v_{pj}^2 - 3v_{p0}^2} P_{lavg} \\ i_{sb} &= \frac{v_{pb} - v_{p0}}{\sum_{j=a,b,c} v_{pj}^2 - 3v_{p0}^2} P_{lavg} \\ i_{sc} &= \frac{v_{pc} - v_{p0}}{\sum_{j=a,b,c} v_{pj}^2 - 3v_{p0}^2} P_{lavg} \end{aligned}\right\} \tag{4.20}$$

where, $v_{p0} = \frac{1}{3}\left(v_{pa} + v_{pb} + v_{pc}\right)$ is zero-sequence voltage, and P_{lavg} is real power injected by source to load. These estimated source currents are sinusoidal, balanced and in-phase with respect to PCC voltages. Therefore, the magnitude of source current (I_m) and unit templates are given as,

$$I_m = \sqrt{\frac{2}{3}\left(i_{sa}^2 + i_{sb}^2 + i_{sc}^2\right)} \tag{4.21}$$

$$\sin\omega t_1 = \frac{i_{sa}}{I_m},\ \ \sin(\omega t_1 - 120) = \frac{i_{sb}}{I_m},\ \ \sin(\omega t_1 + 120) = \frac{i_{sc}}{I_m} \tag{4.22}$$

The reference PCC voltages in CCM mode are:

$$\left.\begin{aligned} v^*_{pa} &= V_{pcc}\sin\omega t_1 \\ v^*_{pb} &= V_{pcc}\sin(\omega t_1 - 120) \\ v^*_{pc} &= V_{pcc}\sin(\omega t_1 + 120) \end{aligned}\right\} \tag{4.23}$$

where, voltage magnitude of V_{pcc} is calculated from (4.19).

4.3.2 Reference voltage generation for VCM mode

The v^*_{pcc} reference voltage selection is explained below to operate DSTATCOM in VCM mode. If, the PCC voltage calculated from (4.19) is out of the load operating limits (i.e., 0.9 $V_{rat} \leq V_{pcc} \leq$ 1.1 V_{rat}), then the DSTATCOM is operated in VCM mode. Here, V_{rat} is peak of rated PCC voltage. In this case, the three-phase PCC voltage references are given as,

$$\left.\begin{aligned} v^*_{pa} &= V_{rat}\sin(\omega t - \delta) \\ v^*_{pb} &= V_{rat}\sin(\omega t - 120 - \delta) \\ v^*_{pc} &= V_{rat}\sin(\omega t + 120 - \delta) \end{aligned}\right\} \tag{4.24}$$

where, δ is load angle, which is obtained from the dc-link voltage control loop. The overall control algorithm of the proposed method is shown in Fig. 4.5. A Second Order Generalized Integrator (SOGI) is implemented for fundamental peak voltage (V_m) detection from source voltage. From the peak and instantaneous source voltages, the unit templates are derived. The performance of SOGI is satisfactory even though the source voltages experience distortions.

After initialization of system parameters, the magnitude of PCC voltage is calculated from (4.19). If V_{pcc} magnitude is between 0.9 V_{rat} and 1.1 V_{rat}, then DSTATCOM is operated in CCM mode and the reference voltages during this period are obtained from (4.23). If V_{pcc} magnitude is less than 0.9 V_{rat} or greater than 1.1 V_{rat}, then DSTATCOM is operated in VCM and the references during this period are obtained from (4.24). The calculated PCC voltage references (*i.e.*, v^*_{pk}) are compared with actual PCC voltages

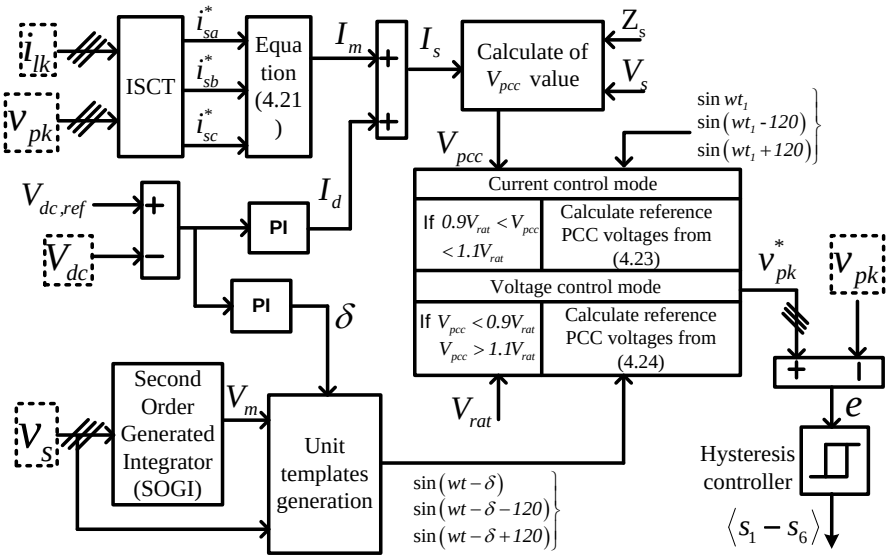


Fig. 4.5 Control algorithm for CCM and VCM modes of operation

(v_{pk}). The error between v^*_{pk} and v_{pk} is passed through hysteresis controller to generate the switching pulses for VSC. In CCM mode of operation, the real power required by load is supplied from ac source, which implies the load current harmonics and reactive power are compensated by DSTATCOM. During DSTATCOM operation, due to losses in VSC and interfacing inductor, the dc-link capacitor takes some real power from source which is considered as current component, I_d. This component is obtained from the dc-link voltage control loop.

4.3.3 Control of dc-link voltage

In conventional method of CCM operation, the reference filter currents are calculated to achieve current control [24]. In this approach, the dc-link capacitor voltage is maintained constant by PI controller and the output is taken as P_{loss}. In the proposed method, the current control is achieved by generating PCC voltage references (v^*_{pcc}). Here, the dc-link voltage is maintained constant by PI controller and the output is taken as real component current drawn from source, I_d.

$$I_d = K_p e_{vdc} + K_i \int e_{vdc} dt \tag{4.25}$$

where, K_p and K_i are proportional and integral gains, respectively, and e_{vdc} is the voltage difference between reference dc-link voltage and measured dc-link voltage. The current,

I_d is added to the peak of fundamental load current (I_m), which gives total current drawn from the source, (I_s). Therefore, to achieve current control, I_s real current is allowed between source and PCC voltage.

Once the operation mode of DSTATCOM is transferred to VCM, the dc-link voltage is regulated by generating a suitable value of δ. The dc-link voltage is compared with reference voltage, and the error is passed through a PI controller. The output of the PI controller is considered as δ and is given as,

$$\delta = K_p e_{vdc} + K_i \int e_{vdc} dt \tag{4.26}$$

4.4 Advantages of the Proposed Method Over Conventional Method

The proposed method has the following advantages while compared to conventional methods.

4.4.1 Reduction in dc-link voltage of VSC

Case 1: (Comparison between *L*-DSTATCOM and *LCL*-DSTATCOM)

In *L*-filter based DSTATCOM, the following Kirchoff Voltage Law (KVL) equation is obtained.

$$m_a V_{dc1} = V_{pcc} + I_f X_{f1} \tag{4.27}$$

where, V_{dc1} is required dc-link voltage for proper compensation. In conventional split-capacitor DSTATCOM topology, the dc-link voltage is considered to be 1.6 times the peak of PCC voltage [45]. Therefore, (4.27) becomes as,

$$1.6V_m = V_m + I_f X_{f1} \tag{4.28}$$

where, X_{f1} is reactance of interfacing inductor in *L*-DSTATCOM. In case of *LCL*-filter DSTATCOM, the following equation is obtained.

$$m_a V_{dc2} = V_m + I_f X_{f2} \tag{4.29}$$

where, X_{f2} is total interfacing inductance of LCL-filter, and V_{dc2} is the dc-link voltage required in LCL-filter. From (4.28) and (4.29), the percentage reduction of dc-link voltage in the proposed method is given by,

$$\%\text{reduction}, x = 0.625\left(1 - \frac{X_{f2}}{X_{f1}}\right) \tag{4.30}$$

It is observed from (4.30) that the reduction of dc-link voltage depends on the reactance of the interfacing inductor.

Case 2: (Comparison between existing and proposed LCL-DSTATCOMs)

In the existing method [68], the dc-link voltage is fixed and is selected based on the rated filter current ($I_{f,rat}$). Therefore, dc-link voltage is given by,

$$V_{dc1} = V_m + I_{f,rat}X_{f1} \Rightarrow 1.6V_m = V_m + I_{f,rat}X_{f1} \tag{4.31}$$

In the proposed method, the dc-link voltage is varied based on the load condition (i.e., working filter current, $I_{f,w}$), and is equal to,

$$V_{dc2} = V_m + I_{f,w}X_{f2} \tag{4.32}$$

From (4.31) and (4.32), the percentage reduction of dc-link voltage in the proposed method is,

$$\frac{V_{dc1} - V_{dc2}}{V_{dc1}} = 0.6\left[\frac{1-y}{1+0.6y}\right] \tag{4.33}$$

where, $y = \left(\frac{X_{Lf2}}{X_{Lf1}}\right)\left(\frac{I_{f,w}}{I_{f,rat}}\right)$. It is observed from (4.33) that the percentage reduction of dc-link voltage will be more in the proposed method, if the working filter current is lower than rated filter current.

4.4.2 Reduction in energy dissipation (E_{sw})

The energy dissipation of the switch depends on the voltage that appears across the switch (i.e., V_{dc}), current flowing through the switch (i.e., I_f) and junction temperature (T_j). The energy dissipation under working condition with respect to nominal test

condition is given as follows: [52]

$$E_{sw} = E_{sw,n}\left(\frac{I_f}{I_{f,n}}\right)^{k_i}\left(\frac{V_{dc}}{V_{dc,n}}\right)^{k_v}\Big(1 + T_c(T_j - T_{jn})\Big) \tag{4.34}$$

where, $I_{f,n}$, $V_{dc,n}$, T_{jn} and $E_{sw,n}$ are the reference values at nominal test condition obtained from the data sheet of Insulated Gate Bipolar Transistor (IGBT) switch (SKM 75GB123D). k_i is the current dependency (for IGBT $\simeq$ 1, diode $\simeq$ 0.5), k_v is the voltage dependency (for IGBT $\simeq$ 1.2 or 1.4, diode $\simeq$ 0.6), T_c is the temperature coefficient (for IGBT $\simeq$ 0.003, diode $\simeq$ 0.005).

Let $V_{dc,c}$ and $V_{dc,p}$ are the dc-link voltages required in the conventional [68] and the proposed methods, respectively. The corresponding energy dissipations for the same filter current are calculated from (4.34), and they are expressed as $E_{sw,c}$ and $E_{sw,p}$, respectively. Then, the percentage reduction in energy dissipation of switch in the proposed method is given by,

$$\%\text{reduction} = 1 - \left(\frac{V_{dc,p}}{V_{dc,c}}\right)^{k_v}, \quad \text{where} \quad (V_{dc,p} \leq V_{dc,c})$$

4.4.3 Reduction in resistive losses

The resistive losses in the feeder resistance and interfacing resistor are given by:

$$P_{L,f} = 3I_d^2R_s \qquad P_{L,i} = 3I_d^2R_f \tag{4.35}$$

where, $P_{L,f}$ and $P_{L,i}$ are losses in feeder resistance and interfacing resistance, respectively. As, the dc-link voltage is reduced in the proposed method, the charging current I_d drawn from the source is also reduced. Therefore, from (4.35) the losses are also reduced.

4.4.4 Damping losses calculation

The passive damping loss (P_d) is expressed as follows [69],

$$P_d = 3r_d I_{cr} = 3r_d \frac{(\omega_{sw} L_{fg} C_r)^2}{(1 - \omega_{sw} L_{fg} C_r)^2 + \omega_{sw}^2 r_d^2 C_r^2} I_{fi}^2 \tag{4.36}$$

where, ω_{sw} is switching frequency in rad/sec. In conventional method [68], the values ω_{sw}, r_d, L_{fg} and C_r are 10 kHz, 22 Ω, 3 mH and 2 μF, respectively. By substituting these values in (4.36), the damping loss is expressed as $P_{d1} = 70.9 I_{fi}^2$.

In the proposed method, the values ω_{sw}, r_d, L_{fg} and C_r are 10 kHz, 6 Ω, 0.12 mH and 8μF, respectively. After substituting these values in (4.36), the damping loss is expressed as $P_{d2} = 15.32 I_{fi}^2$. For the same filter current, the percentage reduction of power loss in the proposed method when compared to conventional method [68] is given as,

$$\%\text{reduction} = 1 - \frac{P_{d2}}{P_{d1}} = 78\%$$

Finally, the comparisons between the proposed *LCL*-DSTATCOM and existing *LCL*-DSTATCOMs (or *LCL*-shunt active power filter) are discussed here. In [66], [67], active damping method is implemented to minimize the resonance problem in *LCL*-filter. For that, extra current sensors are required, which will increase the complexity of the controller. In [68], passive damping method is discussed, in which, damping loss is present because of the dissipating damping resistor (r_d). Though losses exist, the following advantages are obtained with passive damping: 1) There is no need of additional current sensors, 2) It is a simple and straightforward method, and 3) There is no need to change the control algorithm (i.e., same algorithm for both *L*-DSTATCOM and *LCL*-DSTATCOM). Therefore, passive damping is considered in the proposed method. In case of non-stiff source, ripple filter is required at PCC to minimize the switching frequency components in PCC voltages. But, in the proposed method, the resonance circuit of *LCL*-filter minimizes the switching frequency components in the PCC voltage.

The performance of *LCL*-DSTATCOM with the designed parameters and the proposed control algorithm is validated by simulation and experimental studies.

4.5 Simulation Studies

The proposed control scheme is implemented for 3P4W split-capacitor *LCL*-DSTATCOM using MATLAB simulink. The simulation parameters are given in Table 4.3.

Table. 4.3 Simulation parameters for *LCL*-DSTATCOM

Symbol	System parameters	Values
V_s	Supply voltage	230 V
Z_s	Source impedance	1 Ω, 0.1 mH
L_{fi}	Converter side Inductance	13.63 mH
L_{fg}	Grid side Inductance	0.12 mH
C_{dc1}, C_{dc2}	dc-link capacitances	2400 μF each
C_r	Resonance capacitor	8 μF
r_d	Damping resistor	6 Ω
V_{dc1}, V_{dc2}	Rated dc-link voltages	550 V each

4.5.1 Current control mode

In order to check the performance of the proposed method in current control mode, two loads are considered; Load-1 is unbalanced linear load of phase-*a*: 26 Ω, 20 mH, phase-*b*: 34 Ω, 40 mH; phase-*c*: 60 Ω, 60 mH in parallel with three-phase diode bridge *RL* load of 170 Ω, 65 mH. Load-2 consists of unbalanced linear load of phase-*a*: 26 Ω, 20 mH, phase-*b*: 34 Ω, 40 mH, phase-*c*: 60 Ω, 60 mH in parallel with three-phase diode bridge *RL* load of 20 Ω, 150 mH.

The simulation results for the proposed algorithm in CCM mode of operation are shown in Fig. 4.6. Fig. 4.6(a) shows reference PCC voltage (v^*_{pcc}) and actual PCC voltage (v_{pcc}). It is observed from the zoomed part of Fig. 4.6(a) that the actual PCC voltage follows the reference PCC voltage within half cycle during load variation. It shows the fastness of control algorithm for dynamic conditions. The source current (i_s) becomes sinusoidal as shown in Fig. 4.6(b), even though the load current (i_l) has distortions as shown in Fig. 4.6(c). The dc-link voltage (V_{dc}) is varied according to load condition and maintained constant in steady state as shown in Fig. 4.6(d). It is observed that the dc-link voltage settles at 0.023 s during load variation. During load-1 and load-2, the dc-link voltages are maintained to 710 V and 900 V, respectively, whereas in fixed dc-link voltage method, 1100 V is maintained for supply voltage of 230 V. Due to variable

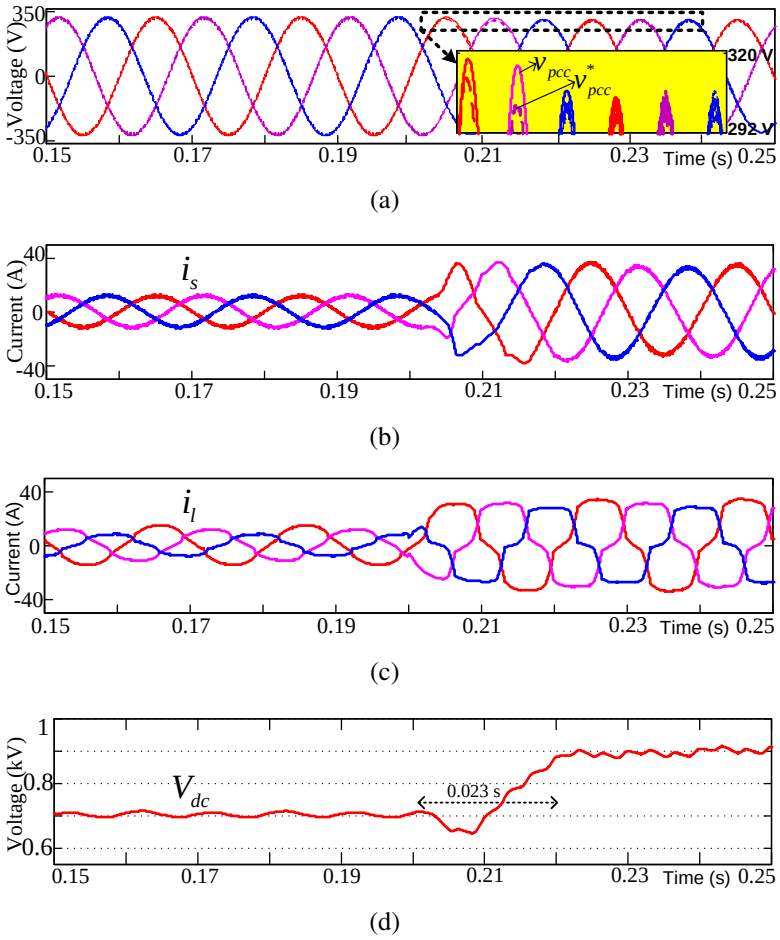


Fig. 4.6 Results in CCM mode of operation (a) PCC voltages (v^*_{pcc} and v_{pcc}) (b) source current (i_s) (c) load current (i_l) and (d) dc-link voltage (V_{dc})

dc-link voltage approach, the percentage reduction of energy dissipation in switches is mentioned in Table. 4.4. In the proposed method, the percentage reduction of energy dissipation in switches are 31.8 % and 13.5 % for load-1 and load-2 conditions when compared to fixed dc-link voltage method.

Table. 4.4 Calculation of percentage reduction of energy dissipation (Esw)

Method	DC-link voltage (V)		Energy dissipation (mJ)		% reduction in E_{sw}	
	Load-1	Load-2	Load-1	Load-2	Load-1	Load-2
Fixed dc-link voltage *LCL*-DSTATCOM	1100	1100	27	43	0	0
Proposed	710	900	18.4	37.2	31.8	13.5

4.5.2 Voltage control mode

In order to study the performance of *LCL*-DSTATCOM operation in voltage control mode, non-linear load drawing high current is considered. The non-linear load parameters are three-phase diode bridge with *RL*-load of 10 Ω, 32 mH. The results during voltage control mode are shown in Fig. 4.7. It consists of three-phase source voltages (v_s), PCC voltages (v_{pcc}), load currents (i_l) and source currents (i_s). Fig. 4.7(a), shows

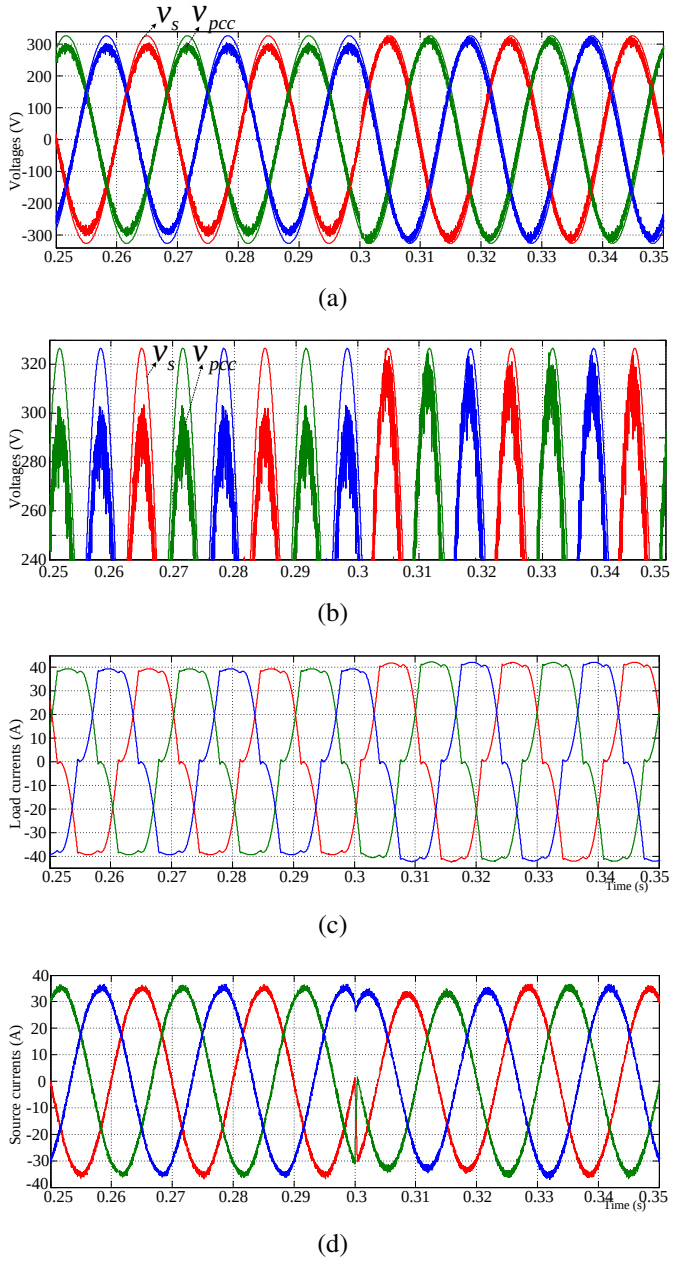


Fig. 4.7 Results in VCM mode of operation: (a) source voltages (v_s) and PCC voltages (v_{pcc}), (b) vertically zoomed figure of (a), (c) load currents and (d) source currents

the three-phase source voltages (v_s) and three-phase PCC voltages (v_{pcc}). The vertically zoomed figure of Fig. 4.7(a) is shown in Fig. 4.7(b). It is observed from Fig. 4.7(b)

that, up to t=0.3 s the peak magnitude of three-phase PCC voltages (v_{pcc}) is less than the three-phase source voltages (v_s), because of feeder impedance drop. During this period, that is from t=0.25 s to t=0.3 s the DSTATCOM is still operated in CCM only. But after time t=0.3 s, the DSTATCOM is operated in the voltage control mode, therefore the PCC voltage magnitude is improved. It can be observed from t=0.3 s to t=0.35 s that the peak magnitude of three-phase PCC voltages (v_{pcc}) almost equal to the three-phase source voltages (v_s). This is due to the real and reactive power injection from DSTATCOM to PCC. During above operating conditions, the three-phase load currents (i_l) and three-phase source currents (i_s) are shown in Fig. 4.7(c) and Fig. 4.7(d), respectively.

The comparisons of the proposed control method with conventional control methods are mentioned in Table. 4.5. The sensing parameters required in the proposed method are low when compared to conventional interactive current and voltage control method [81]. Because, in the proposed method, CCM and VCM operations are achieved by generating only PCC voltage reference. Therefore, the computational burden on the control algorithm is reduced. The switching losses are lower in the proposed method when compared to conventional methods [77], [80], [81], because of adaptive dc-link voltage regulation.

Table. 4.5 Comparison of the proposed control method with conventional control methods

Parameter	Current control method [77]	Voltage control method [80]	Interactive current and voltage control [81]	Proposed control method
Sensing parameters	v_{pcc}, i_l i_f, V_{dc}	v_s, v_{pcc} i_l, V_{dc}	v_s, v_{pcc} i_l, i_f, V_{dc}	v_s, v_{pcc} i_l, V_{dc}
References	i_f^*	v_{pcc}^*	i_f^*, v_{pcc}^*	v_{pcc}^*
PLL required	Optional	Yes	Yes	No
Complexity	Less	Less	More	Moderate
Switching loss	High	–	High	Low
Sample time	20 μs	20 μs	40 μs	30 μs

4.6 Experimental Studies

The performance of the proposed CCM and VCM modes of operation is verified with experimental studies for a reduced voltage of 60 V by considering load-1 (non-linear load) and load-2 (unbalanced load). The control algorithm is implemented by dSPACE MicroLabBox DS-1202. The main experimental components to implement the experiment setup and the corresponding specifications are given in Table 4.6.

Table. 4.6 Components required and their specifications for experimental implementation

Circuit	Component	Specification type
Sensing devices	Voltage transducer	LEM LV 25-P
	Current transducer	LEM LA 55-P
Controller	dSPACE MicroLabBox	DS 1202, FPGA based controller
	Sampling time (T_s)	30 μs
VSC circuit	IGBT with anti-parallel diode	SKM 75GB123D
	dc-link capacitors	Electrolytic 1200 V 4400 μF
±15 V dc power supply	Diode bridge	IN4007,
	Capacitors	Electrolytic 2000 μF
	Regulator (ICs)	LM7815, LM7915
Driver circuit	IC's	Opto-isolator 3120
Waveforms capturing device	Mixed Signal Oscilloscopes (MSO)	Tektronix-2014B, 100 MHz, 1 GS/s
THD measurement	Power quality analyzer	FLUKE-435 series II

4.6.1 Current control mode

The performance of DSTATCOM in CCM mode is validated in steady state and transient load conditions. Also, the *LCL*-DSTATCOM performance with adaptive dc-link voltage method is discussed.

Steady state performance:

The experimental results with non-stiff source before compensation are shown in Fig. 4.8. It is observed that the PCC voltage is distorted because of nonlinear current flowing through feeder impedance. After compensation, the experimental waveforms are shown in Fig. 4.9. It consists of source voltage (v_{sa}), PCC voltage (v_{pa}), source current (i_{sa}) and load current (i_{la}) of phase-a. It is observed from Fig. 4.9 that, the source current becomes sinusoidal and in-phase with voltage even though load current is non-sinusoidal and distorted. The DSTATCOM is operated in current control mode as the PCC voltage magnitude is between limits 0.9 $V_{rat} \leq V_{pcc} \leq 1.1\ V_{rat}$. It is also observed that PCC voltage becomes sinusoidal and harmonic free.

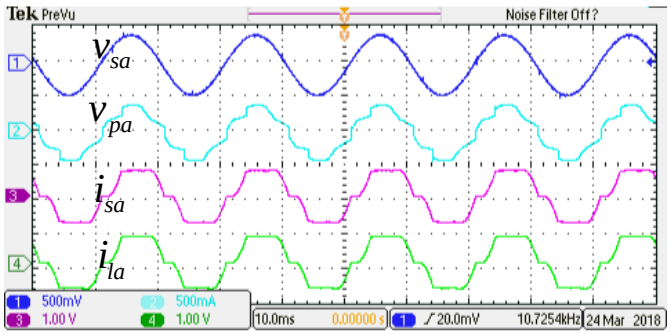


Fig. 4.8 Before compensation: source voltage (v_{sa}), PCC voltage (v_{pa}), source current (i_{sa}) and load current (i_{la}) (scale: voltage 80 V/div, current 2 A/div)

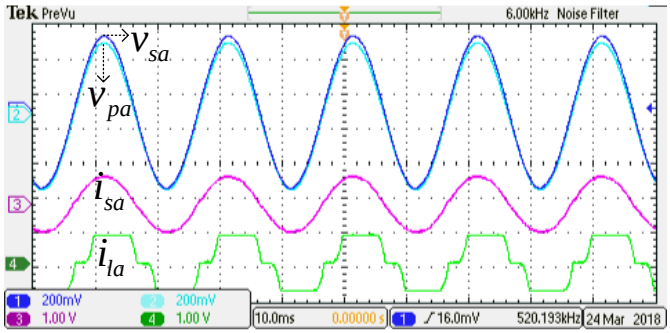


Fig. 4.9 After compensation: source voltage (v_{sa}), PCC voltage (v_{pa}), source current (i_{sa}) and load current (i_{la}) with the proposed LCL-DSTATCOM (scale: voltage 40 V/div, current 2 A/div)

Transient performance

The transient performance is validated for a) before and after operation of DSTATCOM, and b) during load variation. Before and after the operation of DSTATCOM, the results

are shown in Fig. 4.10. It consists of source voltage (v_{sa}), PCC voltage (v_{pa}), source current (i_{sa}) and load current (i_{la}) of phase-a. Before the operation of DSTATCOM, the source current is same as load current (i.e., non-sinusoidal and distorted). After DSTATCOM operation, the PCC voltage follows the reference PCC voltage such that source current becomes sinusoidal and in-phase with voltage even though load current is distorted.

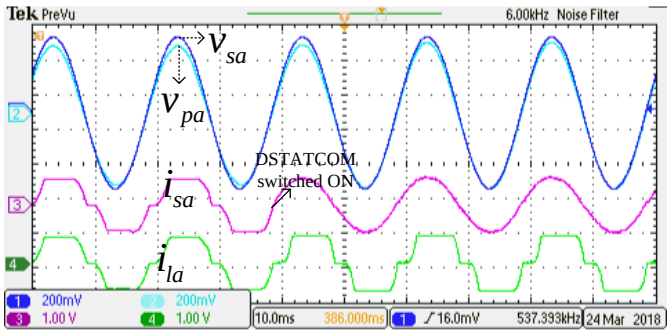


Fig. 4.10 Before and after DSTATCOM operation: source voltage (v_{sa}), PCC voltage (v_{pa}), source current (i_{sa}) and load current (i_{la}) (scale: voltage 40 V/div, current 2 A/div)

The results during transient load variation are shown in Fig. 4.11, which consist of source voltage (v_{sa}), PCC voltage (v_{pa}), source current (i_{sa}) and load current (i_{la}) for load variation. It is observed that, even though the load current is changed, the source current becomes sinusoidal and in-phase with PCC voltage.

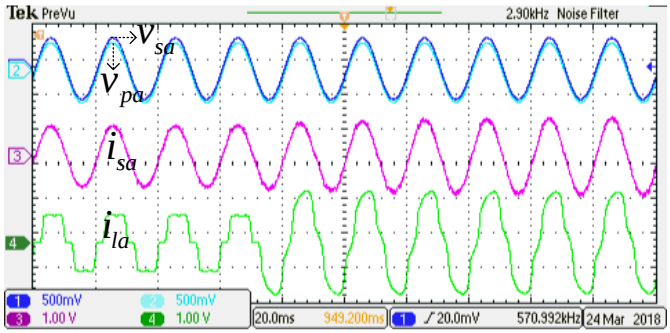


Fig. 4.11 Performance of the proposed *LCL*-DSTATCOM during transient load variation: source voltage (v_{sa}), PCC voltage (v_{pa}), source current (i_{sa}) and load current (i_{la}) (scale: voltage 80 V/div, current 2 A/div)

During the load variation, the dynamics of dc-link voltage for load-1 and load-2 are shown in Fig. 4.12. It consists of PCC voltage (v_{pa}), source current (i_{sa}), load current (i_{la}) and dc-link voltage (V_{dc}) during transient load variation. It is observed that when the load is varied, the dc-link voltage is also varied according to control algorithm. For a better understanding of the compensation performance in the proposed method,

Fig. 4.12 is zoomed during load-1 and load-2, and shown separately as Fig. 4.13 and Fig. 4.14, respectively. It is observed that in both load conditions, the source current becomes sinusoidal and in-phase with voltage.

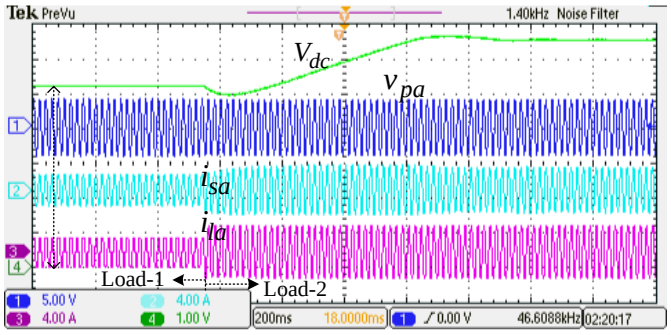


Fig. 4.12 Performance of the proposed *LCL*-DSTATCOM with variable dc-link voltage regulation during transient load variation: PCC voltage (v_{pa}), source current (i_{sa}), load current (i_{la}) and dc-link voltage (V_{dc}) (scale: PCC voltage 80 V/div, dc-link voltage 20 V/div, current 2 A/div)

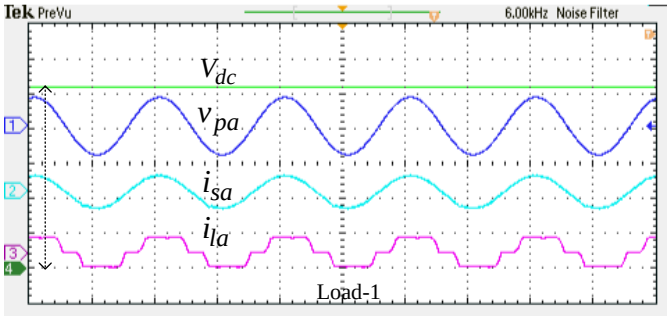


Fig. 4.13 Zoomed figure of 4.12 during load-1 condition (scale: PCC voltage 80 V/div, dc-link voltage 20 V/div, current 2 A/div)

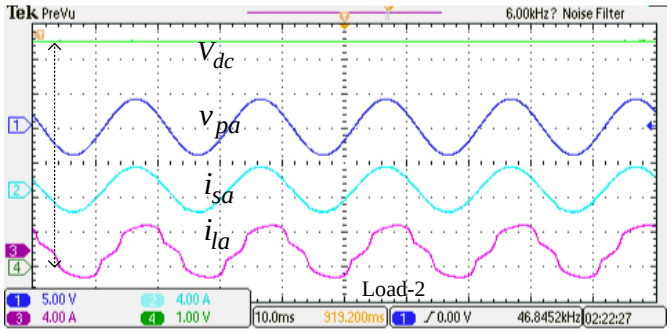


Fig. 4.14 Zoomed figure of 4.12 during load-2 condition (scale: PCC voltage 80 V/div, dc-link voltage 20 V/div, current 2 A/div)

The three-phase source currents before and after compensation for unbalanced load condition (load-2) are shown in Fig. 4.15. It is observed that before compensation, the three-phase source currents are distorted and unbalanced, while after compensation they becomes balanced and sinusoidal.

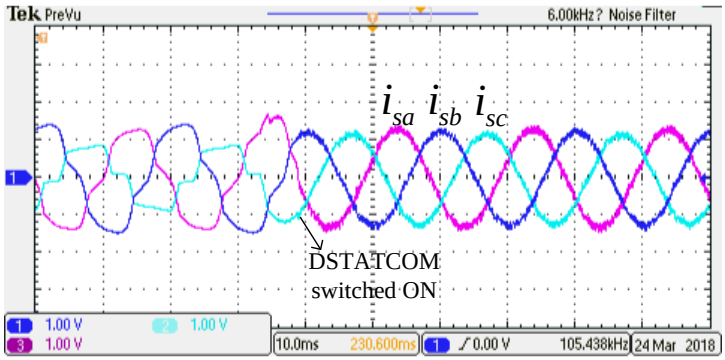
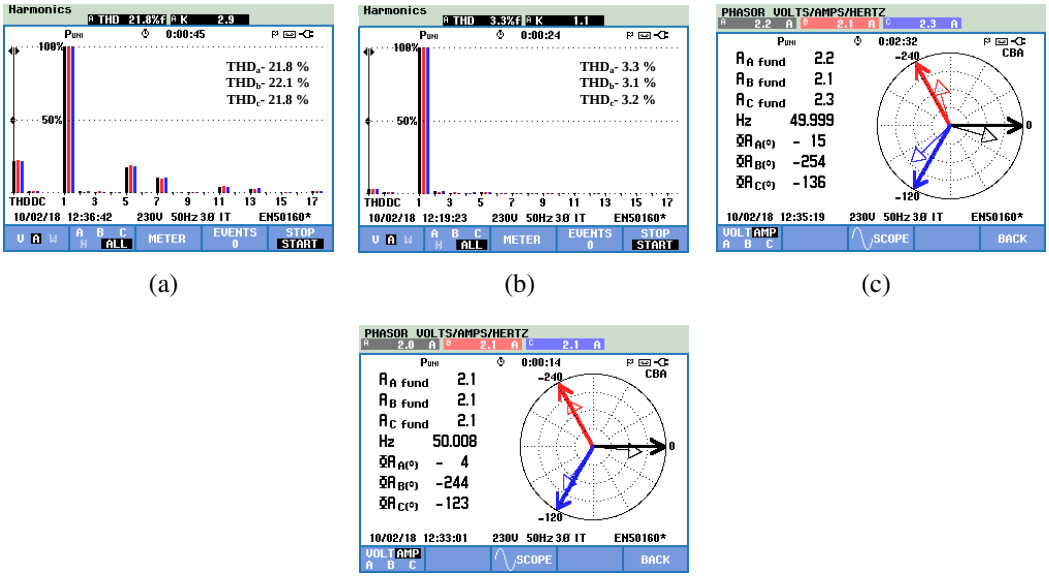


Fig. 4.15 Three-phase source currents (i_{sa}, i_{sb}, i_{sc}) before and after compensation with the proposed method (scale: current 4 A/div)

The three-phase source currents harmonics spectrum and the phasor diagram for load-1 (non-linear load) are shown in Fig. 4.16. Before compensation, the source currents have THDs of 21.8%, 22.1%, 21.8%, respectively as shown in Fig. 4.16(a). After compensation, the harmonic spectra of three-phase source currents are shown in Fig. 4.16(b). It is observed that, the source currents THDs are reduced to 3.3%, 3.1% and 3.2%, respectively. The source currents THD values are well within the IEEE-519 recommended standard value (i.e., less than 5%).



(a) (b) (c)

(d)

Fig. 4.16 (a) and (b) Harmonic spectrum of three-phase source currents before and after compensation for load-1 condition, (c) and (d) phasor diagrams of source voltages and source currents before and after compensation for load-1 condition

The phasor diagram of PCC voltages and source currents for non-linear diode bridge load before compensation are shown in Fig. 4.16(c). It is observed that the three-phase source currents lag behind the respective phase voltages by 15°, 14° (254-240) and

16° (136-120), respectively, and corresponding fundamental source current magnitudes are 2.2 A, 2.1 A and 2.3 A. The phasor diagram of PCC voltages and source currents after compensation are shown in Fig. 4.16(d). It is observed that the source currents are in-phase with respective PCC voltages, and the corresponding fundamental source current magnitudes are 2.1 A, 2.1 A and 2.1 A. This shows that unity power factor is achieved on the source side and three-phase source currents are balanced.

4.6.2 Voltage control mode

In experiment to test the voltage control mode operation, voltage sag is created in source voltage by connecting impedance in the circuit. Here, voltage sag of magnitude 20% of rated voltage is created in source voltage. Fig. 4.17 shows the phase-a source voltage (v_{sa}), PCC voltage (v_{pa}), source current (i_{sa}) and dc-link voltage (V_{dc}). It is observed from the waveform of v_{sa} that, during sag period the magnitude is reduced. However sag is present in source voltage (v_{sa}), the PCC voltage magnitude is not reduced, because of voltage control mode operation. During this period, the phase-a source current (i_{sa}) and dc-link voltage (V_{dc}) are also shown in Fig. 4.17. It is observed that the source current magnitude increases because of the reactive power injected by DSTATCOM during sag period. It is also observed that the dc-link voltage magnitude is maintained constant except small oscillations by dc-link voltage regulation loop. Hence, the proposed scheme is able to provide fast voltage regulation.

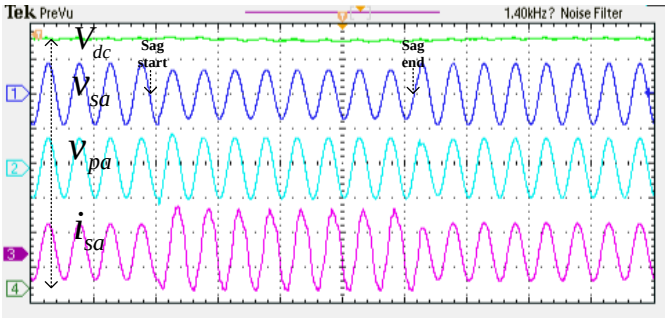


Fig. 4.17 VCM mode of operation during 20% sag in supply voltage: source voltage (v_{sa}), PCC voltage (v_{pa}), source current (i_{sa}) and dc-link voltage (V_{dc}) (scale: PCC voltage and source voltage 80 V/div, dc-link voltage 20 V/div, current 2 A/div)

4.7 Summary

The proposed control algorithm to operate *LCL*-DSTATCOM in CCM and VCM based on the voltage references have been demonstrated through simulation and experimental studies. This method shows an improvement over other methods in the performance of DSTATCOM for power quality improvement. The proposed control algorithm has the advantages of (1) reduction of sensing elements, (2) reduction of computational burden on control algorithm, (3) reduction in switching losses when compared to traditional method, (4) assurance of unity power factor operation, harmonics mitigation and neutral current compensation in CCM mode. Moreover, the results obtained from the experimental setup further establish the viability and effectiveness of the proposed *LCL*-DSTATCOM.

CHAPTER 5

POWER QUALITY IMPROVEMENT BY HYBRID DSTATCOM WITH ADAPTIVE CONTROL SCHEME

In this chapter, a shunt connected hybrid DSTATCOM for power quality improvement is implemented. The hybrid DSTATCOM consists of *LCL*-filter in series with ac-capacitor as an interfacing unit between VSC and PCC. To improve the performance of hybrid DSTATCOM, an adaptive dc-link voltage control scheme is proposed. The proposed method improves the steady state and transient performances, and also having low THD of source current in steady state condition. Also, the control scheme reduces switching losses in VSC and voltage stress across switches by maintaining more appropriate dc-link voltage corresponding to load condition.

5.1 Introduction

A combination of passive and active filter, named as hybrid DSTATCOM is presented in literature for PQ improvement with reduced rating of VSC. In [59], an *L*-filter in series with capacitor as interfacing unit between VSC and PCC is proposed. In this model, the voltage across series ac-capacitor supports VSC, such that the dc-link voltage as well as rating of VSC are reduced. In [84], a hybrid power filter is discussed, which is capable of harmonic compensation under unbalanced operation. But, the range of reactive power compensation is narrow because of fixed series capacitor and dc-link voltage. A Thyristor controlled *LC* filter (TC*LC*) based hybrid active filter in [85], [86], and Static Var Compensator (SVC) based hybrid active filter in [87], [88] are proposed for power quality improvement. These topologies are well supported for a wide range of reactive power compensation, however the generation of pulses for both active filter and TC*LC* or SVC switches makes the algorithm complex. Moreover, the losses due to the switches in the TC*LC* or SVC, reduce the efficiency of the system. An adaptive fuzzy hysteresis band current control for switching losses reduction in hybrid active power filter is discussed [89]. In which the voltage stress across switches of VSC is

high under reduced load conditions, since the dc-link voltage is constant. In the above discussed hybrid topologies, the dc-link voltage is maintained constant forcefully by adopting dc-link voltage control loop. Different voltage control techniques to improvise the performance of dc-link voltage are discussed in the literature.

Traditionally, fixed gains for Proportional Integral (PI) control technique has been adopted for dc-link voltage regulation [28], [59]. But, the dynamic performance of fixed gains PI-controller is sluggish for load changes. A combination of the PI controller and the feed-forward compensation method is discussed in [90]. This method gives excellent improvement in the dynamic performance of the system. But, the oscillations in grid current creates ripple in dc-link voltage, because of the coupling between controlled dc-link voltage and grid current. In [91], [92], a fuzzy PI control method is proposed to tune PI controller gains. A state feedback design based on zero set concept in [93] and a linear optimal control based on the Linear Quadratic Regular (LQR) control in [94] are proposed. The control techniques in [91]–[94], depend on the designer's experience to obtain optimal parameters. An adaptive PI controller to improve the dynamic performance of dc-link voltage is discussed in [95]. In which, voltage and current control gains are coupled to each other; therefore settling time required is more. In the above discussed controlling methods, the dc-link voltage is kept constant, and this value is selected based on the rated load demand condition.

In general, the system may not always be operated at rated load condition. Then, the required dc-link voltage during reduced or light loaded condition is low when compared to fixed dc-link voltage as in conventional method. Therefore, for maintaining fixed dc-link voltage during reduced load condition increases the switching losses and makes high voltage stress across switches. The switching losses and voltage stress during reduced load conditions, can be minimized by implementing an adaptive dc-link voltage control method, which is explained in the next section followed by hybrid DSTATCOM design.

5.2 Structure of Hybrid DSTATCOM

The schematic diagram of the hybrid DSTATCOM in distribution system is shown in Fig. 5.1. The source currents, load currents and filter currents injected by compensator

are labeled as i_{sk}, i_{lk} and i_{fk}, respectively (where: k=a, b and c phases). The grid side and converter side interfacing inductors are labeled L_{fg} and L_{fi}, respectively, and these two inductors are responsible for smoothing the filter currents. A resonant capacitor (C_r) is connected between interfacing inductors for switching frequency harmonics elimination. The damping resistor, r_d is connected in series with C_r to improve the stability of the system. A series capacitor (C_f) is connected between LCL-filter and PCC to reduce the required rating of VSC. V_{pcc} (rms) and V_{inv} (rms) are the voltages at PCC and VSC output, respectively. C_{dc1} and C_{dc2} are upper and lower dc-link capacitors, respectively. The design of hybrid DSTATCOM parameters C_f, L_{fi}, C_r and L_{fg} are explained below.

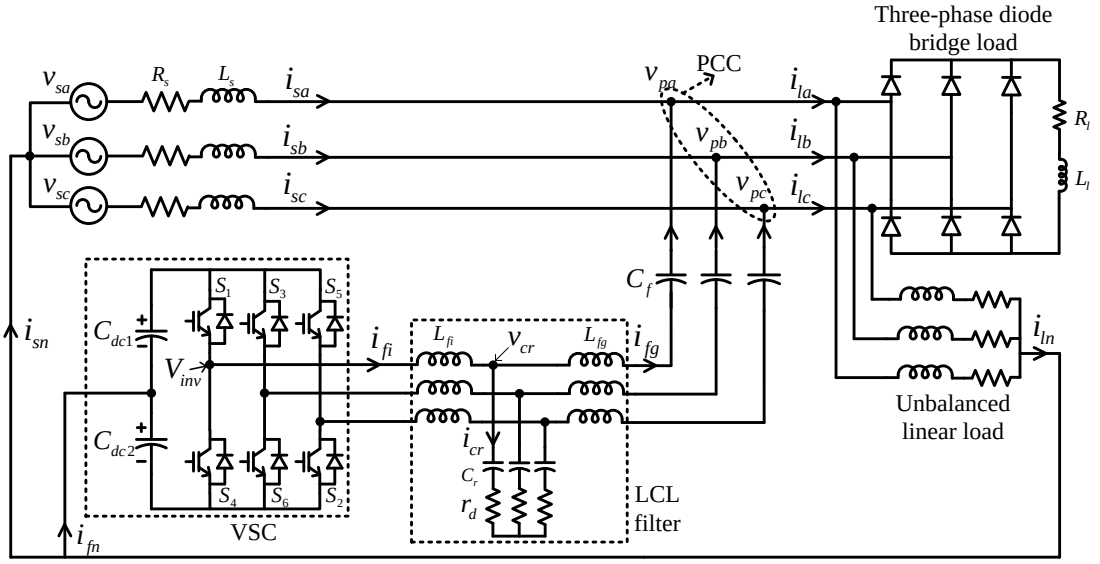


Fig. 5.1 Hybrid DSTATCOM topology for power quality improvement in three-phase four wire (3P4W) distribution system

5.2.1 Design of series capacitor (C_f)

The design of series ac capacitor, C_f depends on reactive power demand. The reactive power supported by series capacitor is given below.

$$Q_r = 3V_{c_f}^2 \omega C_f \quad \text{or} \quad 3V_{c_f} I_{c_f} \tag{5.1}$$

where, $\omega = 2\pi f$, V_{c_f} (rms) is voltage across series ac-capacitor, I_{c_f} (rms) is current flowing through ac-capacitor and f is the supply frequency. The ac-capacitor voltage

varies with respect to the current flowing through it.

$$V_{c_f} = \frac{1}{C_f} \int I_{c_f} dt \tag{5.2}$$

As the load current is increased, the filter current flowing through series ac-capacitor also increases, therefore from (5.2) the ac-capacitor voltage is increased. The ac-capacitor voltage is maximum at maximum allowed filter current. From (5.1) and (5.2), the value of ac-capacitance is calculated for a given reactive power and allowable maximum filter current. In the proposed method, the over compensation problem is eliminated by varying dc-link voltage. At higher frequencies, the impedance offered by the series ac-capacitor (C_f) will be much lower. Therefore, C_f can be neglected during the design of remaining parameters (L_{fi}, C_r and L_{fg}).

5.2.2 Design of parameters L_{fi}, C_r and L_{fg}

The following relations are obtained from Fig. 5.1, by applying Kirchhoff Voltage Law (KVL) from VSC to PCC assuming that current flowing through C_r is very small in magnitude (i.e., negligible).

$$\left.\begin{aligned} m_a V_{dc} + V_{cf} - V_m \sin\omega t &= L_{fi}\frac{\mathrm{d}i_{fi}}{\mathrm{d}t_{on}} + L_{fg}\frac{\mathrm{d}i_{fg}}{\mathrm{d}t_{on}} \\ -m_a V_{dc} + V_{cf} - V_m \sin\omega t &= L_{fi}\frac{\mathrm{d}i_{fi}}{\mathrm{d}t_{off}} + L_{fg}\frac{\mathrm{d}i_{fg}}{\mathrm{d}t_{off}} \end{aligned}\right\} \tag{5.3}$$

where, m_a is amplitude modulation index considered as unity. With negligible current flowing through C_r, the currents i_{fi} and i_{fg} become equal, and this value is considered as i_f. Then (5.3) modified as,

$$\left.\begin{aligned} m_a V_{dc} + V_{cf} - V_m \sin\omega t &= (L_{fi} + L_{fg})\frac{\mathrm{d}i_f}{\mathrm{d}t_{on}} \\ -m_a V_{dc} + V_{cf} - V_m \sin\omega t &= (L_{fi} + L_{fg})\frac{\mathrm{d}i_f}{\mathrm{d}t_{off}} \end{aligned}\right\} \tag{5.4}$$

The rate of change of filter current ($\mathrm{d}i_f/\mathrm{d}t_{on}$ and $\mathrm{d}i_f/\mathrm{d}t_{off}$) during turn-on and turn-off of switches is obtained from the hysteresis controller. During turning ON of upper

switches of VSC, the rate of change of filter current is,

$$\frac{\mathrm{d}i_f}{\mathrm{d}t_{on}} = \frac{(i'_{fref} - i_{fref}) + 2h}{t_{on}} \tag{5.5}$$

Similarly, during turning OFF lower switches of VSC,

$$\frac{\mathrm{d}i_f}{\mathrm{d}t_{off}} = \frac{(i''_{fref} - i'_{fref}) - 2h}{t_{off}} \tag{5.6}$$

Here, i_{fref}, i'_{fref} and i''_{fref} are reference filter currents at different time instants. As the time instants are very small, the change in currents, $(i'_{fref} - i_{fref})$ and $(i''_{fref} - i'_{fref})$ are very small in magnitude. Therefore, for simplification $(i'_{fref} - i_{fref})$ and $(i''_{fref} - i'_{fref})$ are neglected in further calculation. By substituting (5.5) and (5.6) in (5.3), the turn-on time (t_{on}) and turn-off (t_{off}) times are,

$$t_{on} = \frac{2h(L_{fi} + L_{fg})}{m_a V_{dc} + V_{cf} - V_m \sin \omega t} \tag{5.7}$$

$$t_{off} = \frac{2h(L_{fi} + L_{fg})}{m_a V_{dc} - V_{cf} + V_m \sin \omega t} \tag{5.8}$$

From (5.7) and (5.8), the switching frequency (f_{sw}) is given as,

$$\left.\begin{aligned} f_{sw} &= \frac{1}{t_{on} + t_{off}} \\ &= \frac{m_a V_{dc}}{4h(L_{fi} + L_{fg})}\left[1 - \left(\frac{V_{cf} - V_m \sin\theta}{m_a V_{dc}}\right)^2\right] \end{aligned}\right\} \tag{5.9}$$

where, $\theta = \omega t$. The observations from equation (5.9) are:

1. The switching frequency (f_{sw}) is maximum when the difference between $(V_{cf} - V_m \sin\theta)$ is zero.
2. f_{sw} is minimum when difference of $(V_{cf} - V_m \sin\theta)$ is maximum.

The interfacing inductances are designed at maximum switching frequency, therefore from (5.9),

$$L_{fi} + L_{fg} = \frac{m_a V_{dc}}{4h f_{sw,max}} \tag{5.10}$$

where, $f_{sw,max}$ is maximum switching frequency. In the proposed method, the inductor value is designed at rated dc-link voltage even-though the dc-link voltage varied. For

example, the rated dc-link voltage in the proposed hybrid DSTATCOM is considered as 300 V. Therefore, by substituting the values of rated dc-link voltage, h = 0.85 A and $f_{sw,max}$ = 10 kHz in (5.10), the calculated $L_{fi} + L_{fg}$ value is 8.82 mH. To find out individual inductor values, the dynamics of the system are considered.

For the hybrid DSTATCOM shown in Fig. 5.1, the following dynamics of current and voltage equations are derived.

$$\left.\begin{aligned} i_{fi}(s) &= \frac{v_{inv}(s) - v_{cr}(s)}{sL_{fi}}, \qquad i_{fg}(s) = \frac{v_{cr}(s) + v_{cf}(s) - v_{pcc}(s)}{sL_{fg}} \\ v_{cr}(s) &= r_d i_{cr}(s) + \frac{i_{cr}(s)}{sC_r}, \qquad i_{cr}(s) = i_{fi}(s) - i_{fg}(s) \end{aligned}\right\} \tag{5.11}$$

From (5.11), the transfer function $i_{fg}(s)/v_{inv}(s)$ is given as,

$$\frac{i_{fg}}{v_{inv}} = \frac{1 + sr_dC_r}{B_0s^3 + B_1s^2 + B_2s} \tag{5.12}$$

where, $B_0 = L_{fi}L_{fg}C_r$, $B_1 = L_{fi}r_dC_r + r_dC_rL_{fg}$, $B_2 = L_{fi} + L_{fg}$. If damping resistance, $r_d = 0$, then the transfer function (5.12) becomes:

$$\frac{i_{fg}}{v_{inv}} = \frac{1}{L_{fi}L_{fg}C_rs^3 + (L_{fi} + L_{fg})s} \tag{5.13}$$

The overall closed loop transfer function of (5.13) is obtained by applying unity feedback control. In the closed loop characteristic polynomial, s^2 term is missing, which infers the system is unstable according to Routh Hurwitz stability criterion. Therefore, damping is compulsory to stabilize the system. The resonance frequency expression from (5.13) is,

$$f_r = \frac{1}{2\pi}\sqrt{\frac{L_{fi} + L_{fg}}{L_{fi}L_{fg}C_r}} \tag{5.14}$$

In (5.14), the resonance frequency is selected based on higher order harmonic compensated by DSTATCOM. In this work, the highest order harmonic to be compensated by hybrid DSTATCOM is selected as 49^{th} order for 50 Hz supply system with consideration of 5% variation. As a trade-off between the above requirements, the value of C_r is chosen as 8 μF. Therefore, the product of $L_{fi}L_{fg}$ value from (5.14) becomes,

$$L_{fi}L_{fg} = \frac{L_{fi} + L_{fg}}{\omega_r^2C_r} \tag{5.15}$$

By substituting the values (L_{fi}+L_{fg}), ω_r^2 and C_r in (5.15) gives $L_{fi}L_{fg}$ value as 4.65×10^{-6}. The difference between two inductances is given as,

$$L_{fi} - L_{fg} = \sqrt{(L_{fi} + L_{fg})^2 - 4L_{fi}L_{fg}} \tag{5.16}$$

From ($L_{fi} + L_{fg}$) and ($L_{fi} - L_{fg}$) values, the individual value of L_{fi} and L_{fg} are obtained as 8.25 mH, 0.56 mH, respectively. With the designed values, the hybrid DSTATCOM with adaptive control scheme is implemented, which is explained below.

5.3 Proposed Adaptive Control Scheme for Hybrid DSTATCOM

The dc-link voltage magnitude of VSC plays a very important role in the compensation performance. In conventional DSTATCOM, the dc-link voltage is maintained constant at, (a) twice the peak of PCC voltage as in [96] or (b) 1.6 times peak of PCC voltage as in [28], based on the rated load condition. Hybrid DSTATCOM topologies with reduced dc-link voltage other than conventional methods are discussed by connecting a series ac-capacitor in series with VSC [59]. However, for fixed ac-capacitor value, the choice of dc-link voltage magnitude is fixed and is selected based on the rated load condition. But, there is no specific dc-link voltage selection process based on load operating point. The variable dc-link voltage selection based on load condition is discussed below.

5.3.1 Proposed variable dc-link voltage reference selection

In literature, very few authors have discussed the variable dc-link voltage control. The following disadvantages are noticed with the existing method [56], [57].

1. The calculation of reactive power involve *abc* to $\alpha\beta$ transformations and vice versa, which increases the computational burden.
2. The transient response of the dc-link voltage variation is not discussed, which will affect the compensation performance.
3. Over compensation of reactive power occurs during reduced load conditions, and due to this the source current is distorted.
4. Steady state error is present because of fixed controller gains.

5. An extra ripple filter is required in case of non-stiff voltage source for PCC voltage smoothing.

The above problems are addressed in the proposed adaptive control scheme. The dc-link voltage reference is calculated from the simple algorithm based on the reference filter currents, which is explained as follows. The reference dc-link voltage (V_{dc}^{*}) in the proposed method is given as,

$$V_{dc}^{*} = \frac{1}{m_a} V_{inv}^{*} \tag{5.17}$$

where, amplitude modulation index (m_a) is considered as unity and V_{inv}^{*} is VSC ac side voltage and which is calculated from,

$$V_{inv}^{*} = V_{pcc} - V_{c_f} + X_{L_f} I_f \tag{5.18}$$

The above equation is advisable only for reactive power compensation. But, in case of both harmonic current mitigation and reactive power compensation, the reference dc-link voltage is calculated from,

$$V_{inv}^{*} = \sqrt{\left(V_{pcc} - V_{c_f} + X_{L_f} I_f\right)^2 + \sum_{H=5}^{49} (X_{L_{fH}} I_{fH})^2} \tag{5.19}$$

where, H indicates order of harmonics. X_{L_f} and $X_{L_{fH}}$ are total reactances offered by interfacing inductors corresponding to fundamental and harmonic frequencies, respectively. I_f and I_{fH} are fundamental and harmonic component filter currents, respectively. The limits for harmonic order are taken from 5^{th} to 49^{th}, because the dominant harmonic in load current is 5^{th} and mitigating harmonics up to 49^{th} order is considered. In case of non-stiff source, harmonics present in the PCC voltage also, then (5.19) modified as,

$$V_{inv}^{*} = \sqrt{A^2 + \sum_{H=5}^{49} (V_{pcc,H} + X_{L_{fH}} I_{fH})^2} \tag{5.20}$$

where, A = $(V_{pcc} - V_{cf} + X_{L_f} I_f)$. It is observed from the above equations, that the dc-link voltage depends on I_f, which will vary depending on load current. The reference dc-link voltage calculated in the proposed method is less when compared to conventional method for reduced load conditions [59], [84], [85]. Therefore, the switching losses are reduced and the losses are calculated from energy dissipation in switching device.

5.3.2 Adaptive control scheme for dc-link voltage regulation

An adaptive dc-link voltage control method is implemented for better performance, in which the PI gains are tuned based on error between reference dc-link voltage (V_{dc}^{*}) and actual dc-link voltage (V_{dc}). The block diagram of the proposed adaptive dc-link voltage controller is shown in Fig. 5.2. i_d, is current flowing through VSC, i_{dc}^{m} is average value of dc-side current of VSC. The relation between i_d and i_{dc}^{m} is represented with gain (G), which is obtained by equating ac-side and dc-side powers of VSC. The product of average dc-current and dc-voltage is considered as power losses in VSC.

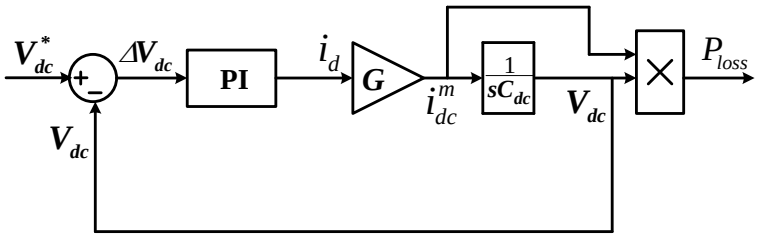


Fig. 5.2 Block diagram of the dc-link voltage controller

From Fig. 5.2, the transfer function of V_{dc}/V_{dc}^{*} is given as,

$$\frac{V_{dc}}{V_{dc}^{*}} = \frac{\frac{G}{C_{dc}}k_p s + \frac{Gk_i}{C_{dc}}}{s^2 + \frac{G}{C_{dc}}k_p s + \frac{Gk_i}{C_{dc}}} \tag{5.21}$$

In the proposed method, the reference dc-link voltage is varied in steps according to load variations. Therefore, (5.21) can be written as,

$$\frac{V_{dc} - V_{dc,0^+}}{V_{dc}^{*} - V_{dc,0^+}^{*}} = \frac{\frac{G}{C_{dc}}k_p s + \frac{Gk_i}{C_{dc}}}{s^2 + \frac{G}{C_{dc}}k_p s + \frac{Gk_i}{C_{dc}}} \tag{5.22}$$

where, k_p and k_i are PI controller gains, C_{dc} is dc-link capacitance value, $G = 3\mathbf{V}_m/2V_{dc}^{*}$. $V_{dc,0^+}$ and $V_{dc,0^+}^{*}$ are actual and reference dc-link voltages at the starting of transient, respectively. By comparing the denominator of (5.22) with the general second order system, the following relations are obtained.

$$k_p = \frac{2\zeta\omega_n C_{dc}}{G}, \quad k_i = \frac{\omega_n^2 C_{dc}}{G} \quad \text{where, } 0 < \zeta < 1 \tag{5.23}$$

The reference dc-link voltages involve step variation function. Therefore, (5.22) becomes,

$$\boldsymbol{V}_{dc} = \boldsymbol{V}_{dc,0^+} + \frac{1}{s}\left(\frac{\frac{G}{C_{dc}}k_p s + \frac{Gk_i}{C_{dc}}}{s^2 + \frac{G}{C_{dc}}k_p s + \frac{Gk_i}{C_{dc}}}\right)(\boldsymbol{V}^*_{dc} - \boldsymbol{V}^*_{dc,0^+}) \tag{5.24}$$

The solution for above equation in time domain is,

$$\left.\begin{aligned}\boldsymbol{V}_{dc}(t) = \boldsymbol{V}_{dc,0^+} + \left(1 - e^{-\zeta\omega_n t}\cos\omega_d t + \frac{\zeta e^{-\zeta\omega_n t}}{\sqrt{1-\zeta^2}}\sin\omega_d t\right)\\ *(\boldsymbol{V}^*_{dc} - \boldsymbol{V}^*_{dc,0^+})\end{aligned}\right\} \tag{5.25}$$

$$\left.\begin{aligned}&\text{If } \ t = 0^+ \Rightarrow \boldsymbol{V}_{dc}(t) = \boldsymbol{V}_{dc,0^+}\\ &\text{If } \ t = \infty \Rightarrow \boldsymbol{V}_{dc}(t) = \boldsymbol{V}_{dc,0^+} + (\boldsymbol{V}^*_{dc} - \boldsymbol{V}^*_{dc,0^+})\end{aligned}\right\} \tag{5.26}$$

The conditions of $t = 0^+$ and $t = \infty$ indicates, the start of transient and steady state periods, respectively. It is observed from steady state condition, that the actual dc-link voltage follows the reference dc-link voltage but the time taken to reach steady state depends on rise time and settling time, which is dependent on damping ratio (ζ) and natural frequency (ω_n). Also, it can be observed from (5.23) that k_p and k_i values depend on ζ and ω_n. To simplify the design of controller gains, the damping ratio (ζ) value is selected as 0.707. The selection of ω_n for gains tuning is a trade-off between the following points.

1. The increase of ω_n will result in better dynamic performance during transient state operation and higher grid-side current THD during steady state operation.
2. The decrease of ω_n will result in lower dynamic performance during transient state operation and lower grid-side current THD during steady state operation.

To overcome this trade-off, ω_n is selected from look up table, which consists of different ranges of ω_n bands from $\omega_{n,min}$ to $\omega_{n,max}$ based on error, ΔV_{dc} [95]. Therefore, for the selected value of ω_n, k_p and k_i gains are continuously updated from (5.23).

The analysis based on design parameters for different series ac-capacitor values and for different filter currents are discussed here. The graph between required dc-link voltage and filter current for different series ac-capacitor values is shown in Fig. 5.3. It is observed that, the higher value of ac-capacitor supports more current compensation. But, for the same filter current, the required dc-link voltage is high when compared to

lower ac-capacitor required case. Therefore, the choice of series ac-capacitor depends upon maximum filter current to be compensated by hybrid DSTATCOM.

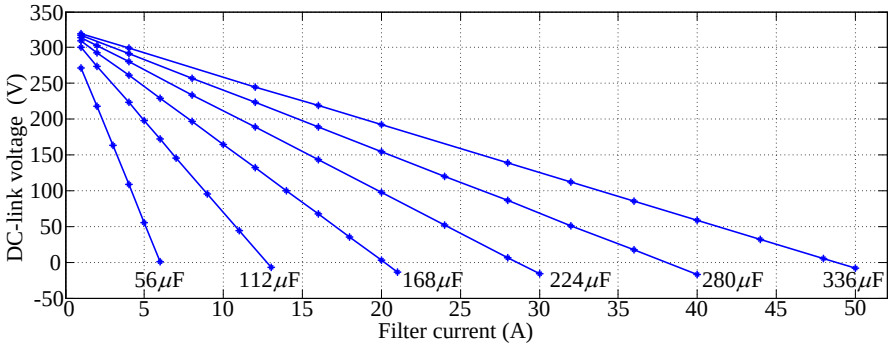
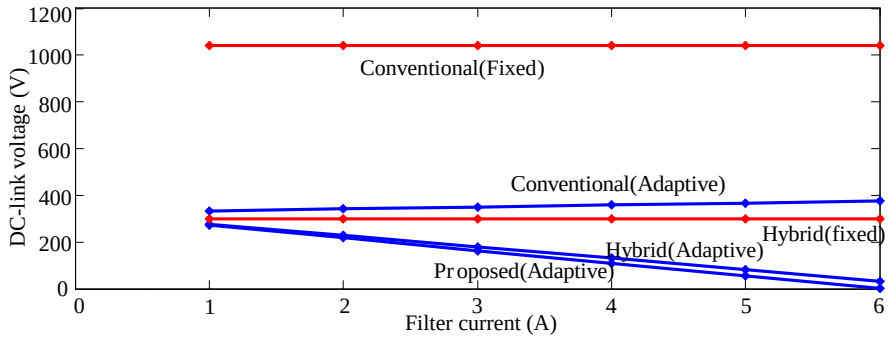


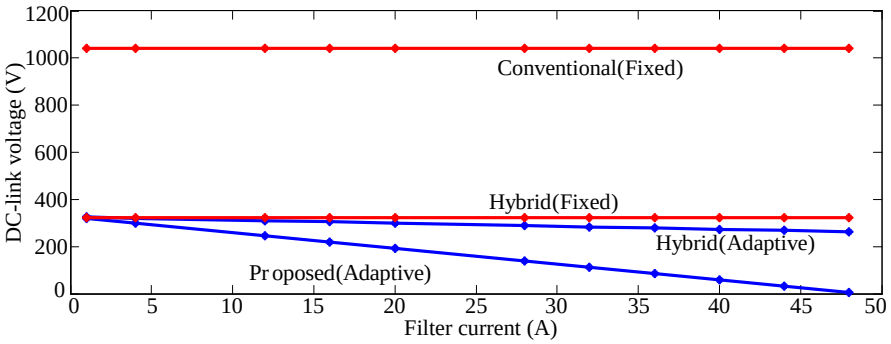
Fig. 5.3 Graph between dc-link voltage and filter current for different series ac-capacitor values

The required dc-link voltage corresponding to filter current in fixed and adaptive dc-link voltage methods for different topologies when C_f=56 μF and C_f=336 μF are shown in Fig. 5.4(a) and Fig. 5.4(b), respectively. The topologies considered for comparison are 1) *L*-filter DSTATCOM (conventional), 2) *LC*-filter DSTATCOM (hybrid) and 3) *LCLC*-filter DSTATCOM (proposed). It is observed from Fig. 5.4(a), that the required dc-link voltage is high in fixed dc-link when compared to adaptive method in all topologies. But, when compared among the adaptive methods, the required dc-link voltage is less in the proposed method. It is observed from Fig. 5.4(b), that for hybrid DSTATCOM, the required dc-link voltage in adaptive and fixed methods are almost equal, therefore adaptive method is not suggestible in this case. The proposed method still supports more filter current as well as requires less dc-link voltage compare to other methods.

The graph between switching losses and filter current for different topologies is shown in Fig. 5.5. For hybrid topologies, two different series ac-capacitor values are considered for analysis. In case of C_f = 56 μF, the graph is shown in Fig. 5.5(a). It is observed that the switching losses are high in conventional topology (*i.e.*, *L*-filter based DSTATCOM with fixed dc-link voltage) when compared to other topologies. Also, the losses are almost same in hybrid (adaptive) and proposed (adaptive) methods. In case of C_f = 336 μF, the graph is shown in Fig. 5.5(b) and the following conclusions are drawn from these graphs. 1) The adaptive method for conventional topology is suggestible up to 20 A. This is because the switching losses are more in adaptive method when compared to fixed method. 2) The adaptive hybrid method is not suggestible as the losses



(a)



(b)

Fig. 5.4 Graph between filter current and required dc-link voltage for different topologies (a) when C_f=56 μF and (b) when C_f=336 μF

are almost same in both fixed and adaptive methods. 3) The proposed method is recommended for high currents because of lower switching losses as shown in Fig. 5.5(b). The above analysis of the graphs were done by considering rms values of fundamental filter current.

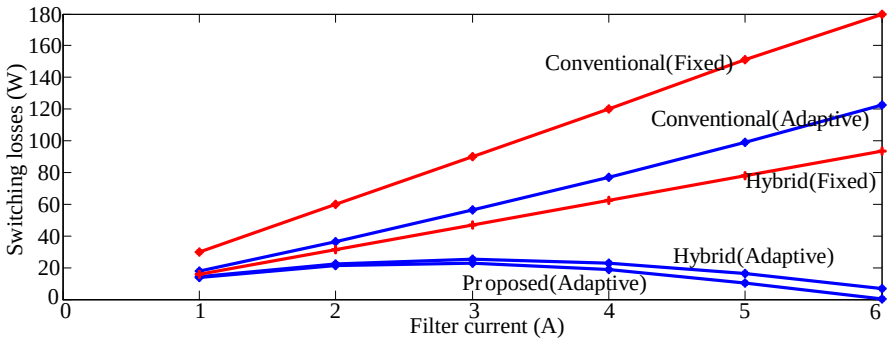
The proposed hybrid DSTATCOM performance with the designed parameters and adaptive control algorithm is validated with simulation and experimental studies in the next section.

5.4 Simulation Studies

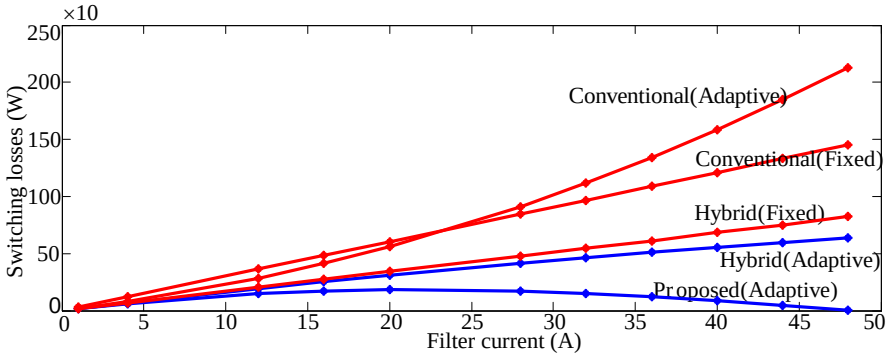
The three-phase four-wire (3P4W) split-capacitor hybrid DSTATCOM with the adaptive dc-link voltage scheme is simulated using MATLAB simulink. The simulation parameters are given in Table 5.1. To check the performance of the proposed method, two different loads are considered:

1) Load-1 is a three-phase diode bridge load of 50 Ω, 300 mH.

2) Load-2 is a combination of three-phase unbalanced linear load of phase-*a*: 34 Ω, 150



(a)



(b)

Fig. 5.5 Graph between filter current and switching losses in VSC (a) for C_f=56 μF and (b) for C_f=336 μF

mH, phase-*b*: 81 Ω, 126 mH, phase-*c*: 31 Ω, 226 mH, and three-phase diode bridge load of 250 Ω, 300 mH.

The calculated reference dc-link voltages for load-1 and load-2 are shown in Table. 5.2 and Table. 5.3, respectively. In case of load-1, the three-phase load currents are same, therefore only one phase calculation is sufficient. In case of load-2, the three-phase load currents are unbalanced, therefore calculation of all phases is required. Out of three-phase calculations, maximum value is selected to choose dc-link voltage. From the calculated inverter voltages in each phase for fundamental and harmonics orders, the resultant inverter rms voltage is calculated from (5.17). The resultant inverter voltages for load-1 is 157.44 V and for load-2 is 238.73 V; the corresponding dc-link voltages calculated from (5.17) are 160 V and 240 V, respectively.

The following events are considered to occur in the system for simulation studies.

1) During t=0 s to 0.06 s, compensator is not switched-ON (i.e., without compensation) and dc-link capacitors are pre-charged to 130 V.

2) At t = 0.06 s, compensator is in operation (with compensation) and load-1 is present.

3) At t = 0.22 s, unbalanced non-linear load is connected at PCC (i.e., load-2).

Table. 5.1 Simulation parameters for hybrid DSTATCOM operation

Symbol	**System parameters**	**Values**
V_s	Supply voltage	230 V
L_{fi}	Converter side inductance	8.25 mH
L_{fg}	Grid side inductance	0.56 mH
C_f	Series ac-capacitance	56 μF
C_r	Resonance capacitance	8 μF
r_d	Damping resistance	6 Ω
C_{dc1}, C_{dc2}	dc-link capacitances	2400 μF each
Load-1: Three-phase diode bridge load of 50 Ω, 300 mH.		
Load-2: Unbalanced linear load of phase-*a*: 34 Ω, 150 mH, phase-*b*: 81 Ω, 126 mH, phase-*c*: 31 Ω, 226 mH; plus three-phase diode bridge load of 250 Ω, 300 mH.		

Table. 5.2 Reference dc-link voltage calculation for diode bridge load (Load-1)

H	X_{LfH}	I_{fH}(rms)	$X_{LfH}I_{fH}$	$V_{cf,H}$	$V_{inv,H}$
1^{st}	2.8	3.12	8.8	177.4	156.8
5^{th}	14.1	1.32	18.6	15	3.6
7^{th}	19.78	0.72	14.2	5.85	8.35
11^{th}	31	0.24	7.4	1.2	6.2
13^{th}	36.7	0.16	5.88	0.7	5.18
17^{th}	48	0.13	6.2	0.4	5.8
19^{th}	53.7	0.09	4.8	0.27	4.53

Table. 5.3 Reference dc-link voltage calculation for unbalanced load (Load-2)

H	I_{fH}(rms)			$V_{cf,H}$			$V_{inv,H}$			max
	a	*b*	*c*	*a*	*b*	*c*	*a*	*b*	*c*	($V_{inv,H}$)
1^{st}	3.4	1.6	3	191.5	91.5	170	143.5	238.6	159.8	238.6
5^{th}	0.32	0.36	0.3	3.6	4.1	3.4	0.9	0.9	0.83	0.9
7^{th}	0.19	0.23	0.2	1.54	1.87	1.62	2.22	2.68	2.28	2.68
11^{th}	0.13	0.14	0.13	0.67	0.72	0.67	3.36	3.62	3.36	3.62
13^{th}	0.1	0.12	0.1	0.44	0.52	0.44	3.23	3.88	3.23	3.88
17^{th}	0.07	0.08	0.07	0.23	0.27	0.23	3.13	3.57	3.09	3.57
19^{th}	0.06	0.07	0.06	0.18	0.21	0.18	3.02	3.55	3.02	3.55

The simulation waveforms without and with operation of the compensator are shown in Fig. 5.6. The three-phase PCC voltages are balanced and sinusoidal as shown in Fig. 5.6(a). The three-phase source currents and neutral current are shown in Fig. 5.6(b). The compensator is not in operation up to t = 0.06 s, therefore the source currents are non-sinusoidal. After compensator is switched at t = 0.06 s, the compensation starts and source currents become sinusoidal. During this process, the filter currents injected by DSTATCOM are shown in Fig. 5.6(c), and dc-link voltages are shown in Fig. 5.6(d). It is observed that, initially the dc-link capacitors are charged to 130 V. Once after the compensator is switched-ON at t = 0.06 s, the dc-link capacitors are charged to 160 V. This voltage is sufficient for satisfactory compensation for a given load condition, and which is calculated from the proposed algorithm.

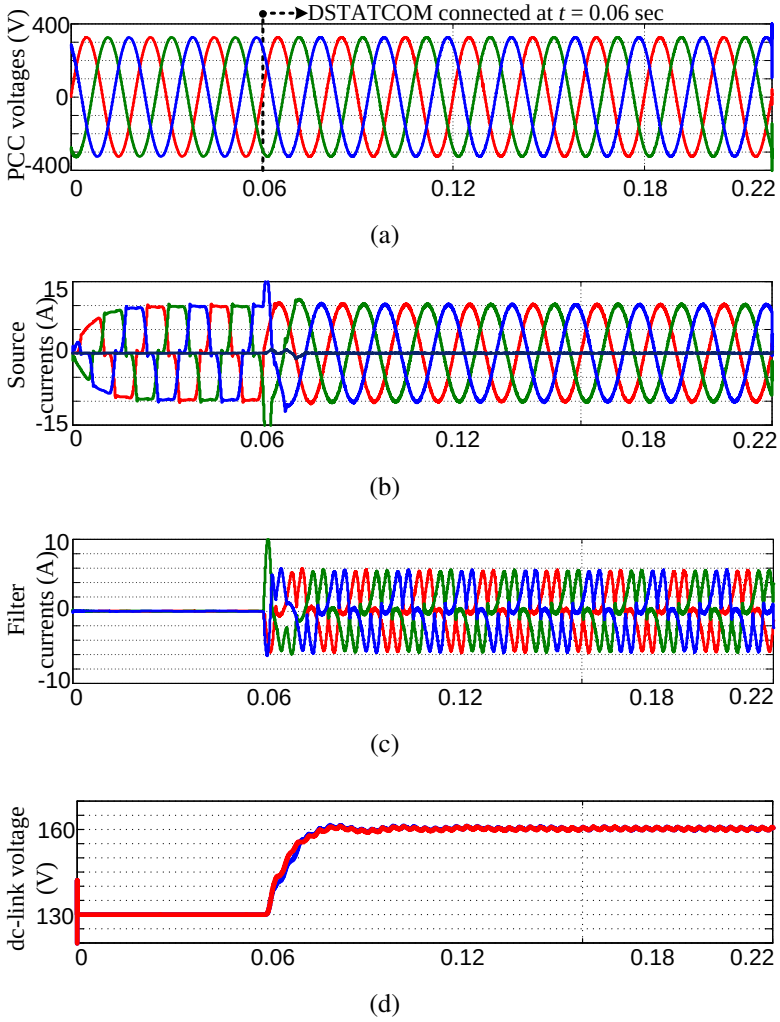


Fig. 5.6 Simulation results of the proposed method for hybrid DSTATCOM switching at t = 0.06 s: (a) PCC voltages (v_{pcc}), (b) source currents (i_s), (c) filter currents (i_f) and (d) dc-link voltages (V_{dc1}, V_{dc2}).

The simulation results of the proposed method during dynamic load variation are shown

in Fig. 5.7. Fig. 5.7(a) shows three-phase PCC voltages, which are balanced and sinusoidal. The three-phase source currents and source side neutral current are shown in Fig. 5.7(b). It is observed that source currents are balanced and sinusoidal before and after load variation at t = 0.22 s, therefore the source side neutral current is also zero. The load currents for both load conditions are shown in Fig. 5.7(c). The filter currents injected by compensator for both load conditions are shown in Fig. 5.7(d). The voltage across dc-link capacitors are maintained to reference dc-link voltages calculated from the proposed algorithm and are shown in Fig. 5.7(e).

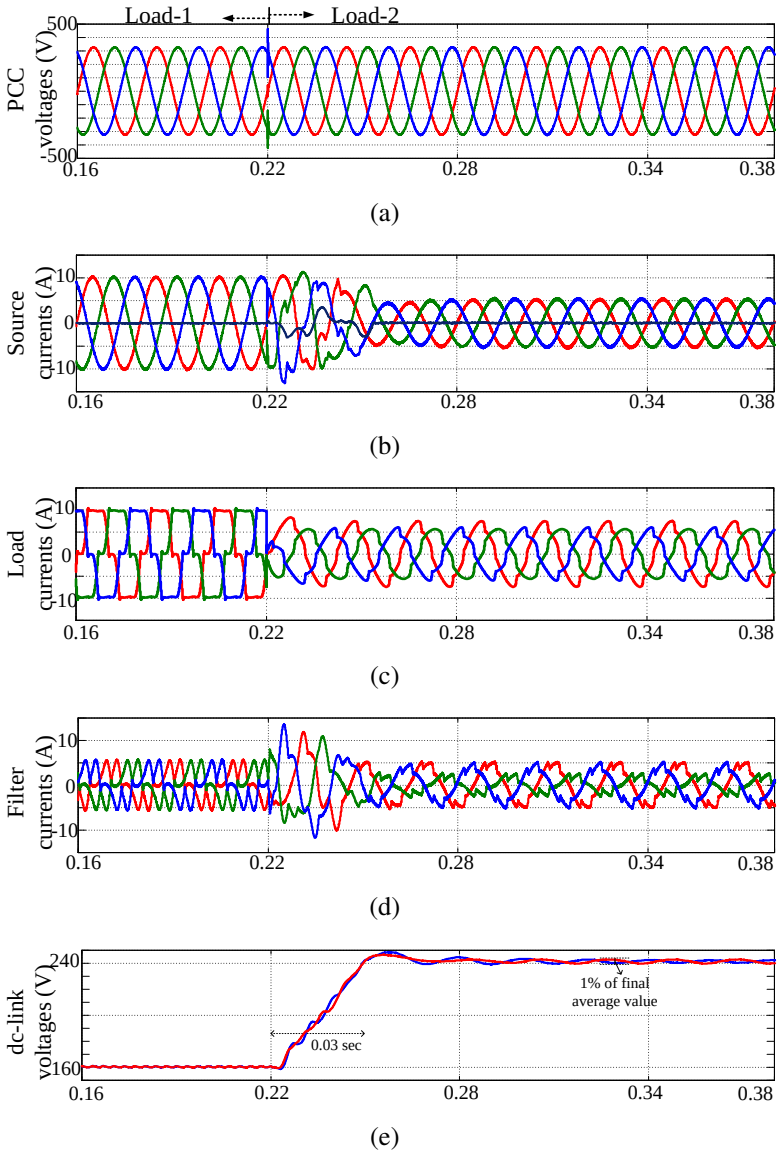


Fig. 5.7 Simulation results of the proposed method during dynamic load variation at t=0.22 s: (a) PCC voltages (v_{pcc}), (b) source currents (i_s), (c) load currents (i_l), (d) filter currents (i_f) and (e) dc-link voltages (V_{dc1}, V_{dc2}).

The dc-link voltage dynamics with fixed PI controller and the proposed adaptive PI

controller are shown in Fig. 5.8. The dc-link voltage magnitude is same in both the methods up to t = 0.22 s, because of same gains considered for initial load (load-1). The load is changed at t = 0.22 s, and the dc-link voltage is changed to 240 V, which is the reference dc-link voltage calculated from the proposed algorithm. The dc-link voltage settle faster in the adaptive PI controller compared to fixed PI controller method, which indicates the improvisation of the transient response of dc-link voltage. The steady state error is zero with adaptive PI control method, but with fixed PI method it is 10 V.

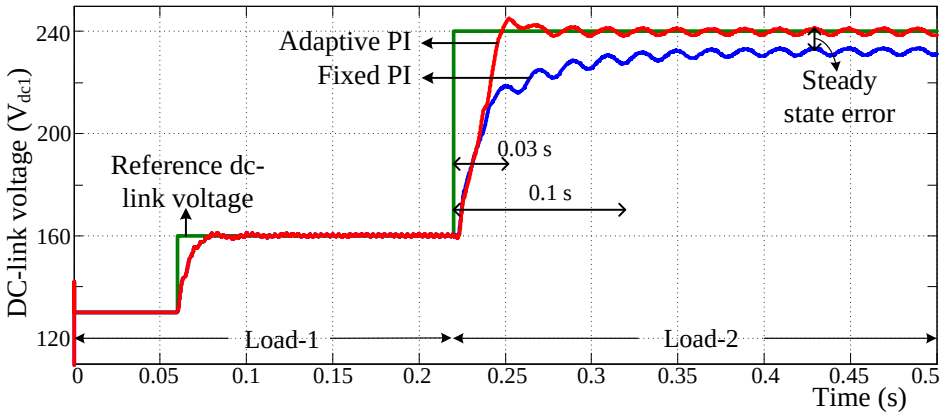


Fig. 5.8 DC-link voltage dynamics with fixed and adaptive PI controllers

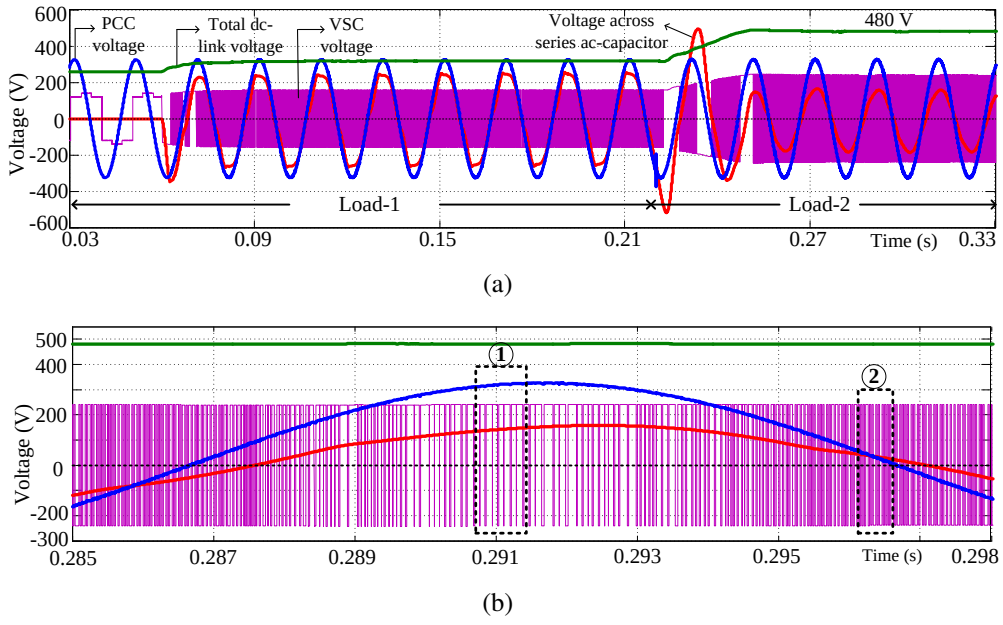


Fig. 5.9 (a) Phase-*b* PCC voltage (v_{pcc}), VSC voltage (v_{inv}), series ac-capacitor voltage (v_{cf}) and total dc-link voltage ($V_{dc1} + V_{dc2}$) and (b) zoomed figure of (a) from t = 0.285 s to 0.298 s

The phase-*b* PCC voltage, VSC voltage, voltage across series ac-capacitor and total dc-link voltage are shown in Fig. 5.9. The dc-link capacitors are pre-charged to 130

V without switching the compensator up to $t = 0.06$ s. Therefore, the voltage across series ac-capacitor is zero. Once after the compensator is switched-ON, the series ac-capacitor voltage builds up and it is lower than PCC voltage. During load-2 condition from $t = 0.22$ s, the ac-capacitor voltage is reduced when compared to voltage during load-1, because of less filter current flowing through the ac-capacitor present in phase-*b*. This demands total dc-link voltage of 480 V (each dc-link voltage 240 V) for proper compensation as shown in Fig. 5.9(a). The zoomed part of Fig. 5.9(a) from $t = 0.285$ s to $t = 0.298$ s is shown in Fig.5.9(b). It is observed from Fig. 5.9(b) that, the switching frequency (f_{sw}) is minimum when the difference between ac-capacitor voltage and PCC voltage is maximum and it is indicated as ①. The f_{sw} is maximum when ac-capacitor voltage and PCC voltage are equal and it is indicated as ②. These two are validated points as mentioned in the design of compensator parameter.

The simulation waveforms of PCC voltages for conventional [56] and the proposed methods with non-stiff voltage source are shown in Fig. 5.10(a) and (b), respectively. In both the methods, the DSTATCOM is switched at $t = 0.06$ s. It is observed from Fig. 5.10(a), that up to $t = 0.06$ s, the PCC voltages are distorted and non-sinusoidal. In conventional method, after $t = 0.06$ s, the PCC voltages become sinusoidal but have switching frequency component. These switching frequency components are minimized by connecting a ripple filter at PCC [96], [97]. It increases the cost and makes the system bulky. But, in the proposed method, the switching frequency components are not present in PCC voltages after DSTATCOM is connected at $t = 0.06$ s. Therefore, an additional ripple filter is not required in the proposed method.

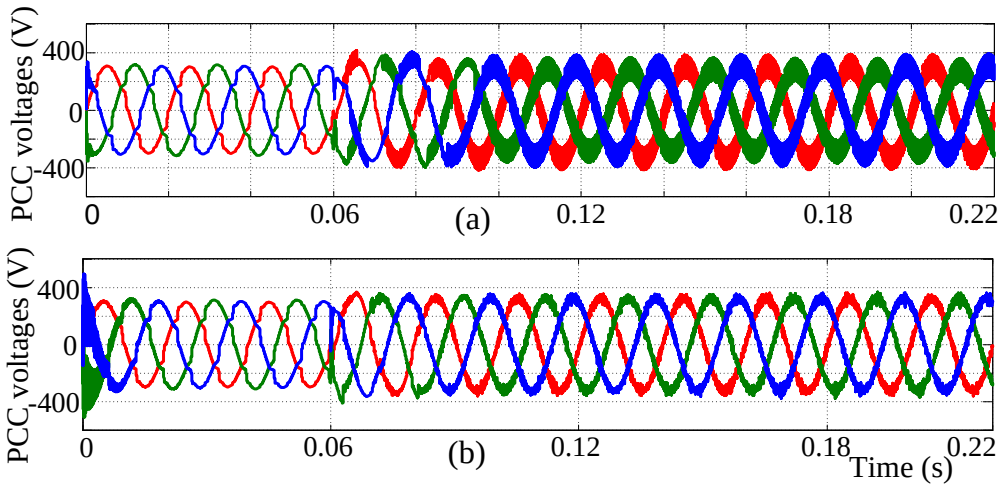


Fig. 5.10 PCC voltages under non-stiff voltage source (a) conventional method and (b) hybrid DSTATCOM with proposed method

5.5 Experimental Studies

The performance of the proposed method is verified with experimental studies for reduced line to line voltage of 100 V. The photograph of the experimental setup is shown in Fig. 5.11. The experimental setup specifications are given in Table 5.4. The proposed adaptive control scheme has been implemented in dSPACE. The adaptive control scheme has been tested for reactive power compensation, source current balancing and harmonic mitigation in the presence of three-phase unbalanced load and non-linear load of three-phase diode bridge with RL-load.

Table. 5.4 Experimental parameters for hybrid DSTATCOM operation

Symbol	System parameters	Values
V_s	Supply voltage	100 V (L-L)
L_{fi}	Converter side inductance	11.3 mH
L_{fg}	Grid side inductance	1.16 mH
C_f	Series ac-capacitance	40 μF
C_r	Resonance capacitance	4 μF
C_{dc1}, C_{dc2}	dc-link capacitances	2400 μF each

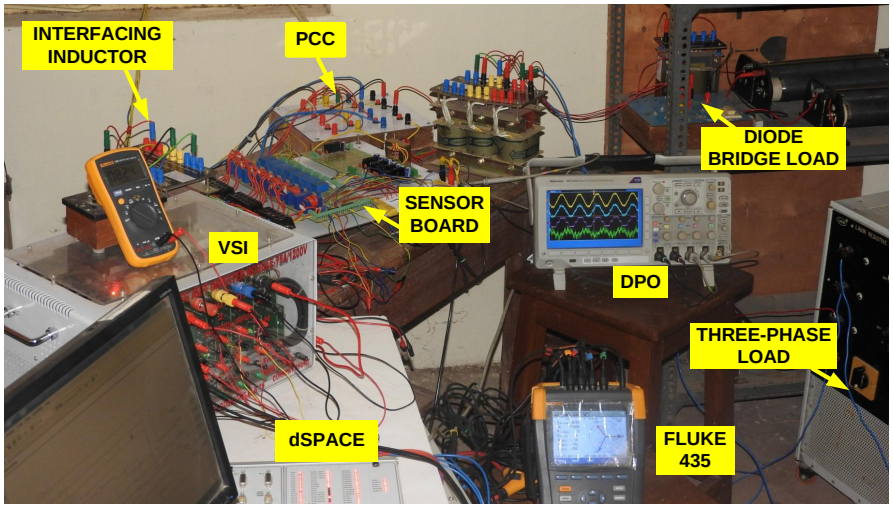


Fig. 5.11 Experimental set-up photograph

The experimental waveforms of PCC voltage (v_{pa}), source current (i_{sa}), load current (i_{La}) and filter current (i_{fa}) for load-1 and load-2 are shown in Fig. 5.12 and Fig. 5.13, respectively. It is observed from Fig. 5.12 that, the load current lags the PCC voltage but the source current is in-phase with PCC voltage because of the filter current injected by the hybrid DSTATCOM. Even though the load current is non-sinusoidal as shown in Fig. 5.13, the source current becomes sinusoidal and in-phase with PCC voltage. The reason is that, the source current harmonics are mitigated by filter current injected by the

hybrid DSTATCOM. This shows that, the proposed method is suitable for compensation of reactive loads and non-sinusoidal loads.

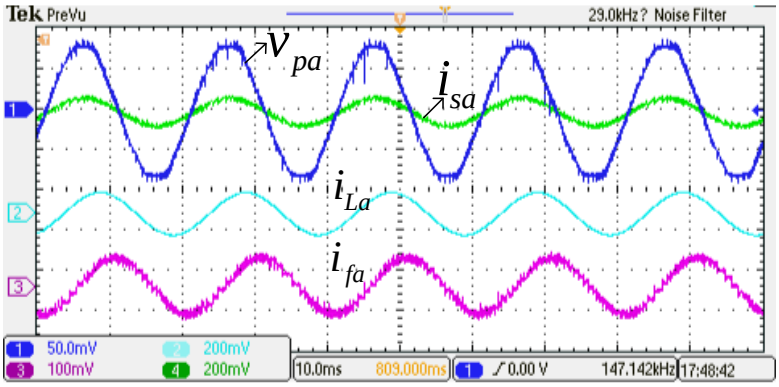


Fig. 5.12 Compensation performance with hybrid DSTATCOM during load-1 (scale: voltage 50 V/div, current 2 A/div)

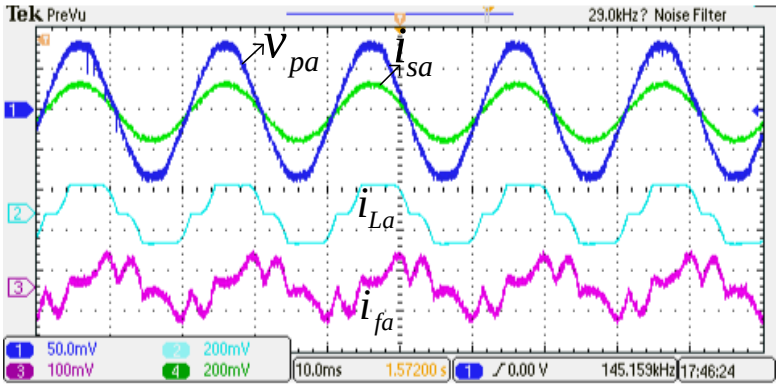


Fig. 5.13 Compensation performance with hybrid DSTATCOM during load-2 (scale: voltage 50 V/div, current 2 A/div)

The dc-link voltage dynamics for load variation with the proposed method is shown in Fig. 5.14. It consists of PCC voltage (v_{pa}), source current (i_{sa}), load current (i_{La}) and dc-link voltage ($\boldsymbol{V}_{dc}$). It is observed from Fig. 5.14, that the dc-link voltage magnitude of VSC is different for load-1 and load-2, and are equal to 136 V and 92 V, respectively. Due to this, the switching loss and voltage stress across switches of VSC are reduced. To show the compensation performance with different dc-link voltage conditions, the zoomed figures of Fig. 5.14 are shown in Fig. 5.15 and Fig. 5.16, respectively. It is observed from Fig. 5.15 and Fig. 5.16 that the source current is sinusoidal and in-phase with PCC voltage.

The experimental waveforms of PCC voltage (v_{pa}), series ac-capacitor voltage (V_{cf}), VSC ac side voltage (V_{inv}) and dc-link voltage (V_{dc}) are shown in Fig. 5.17. The dc-link voltage is varied when load is changed from load-1 to load-2. This is because, in the

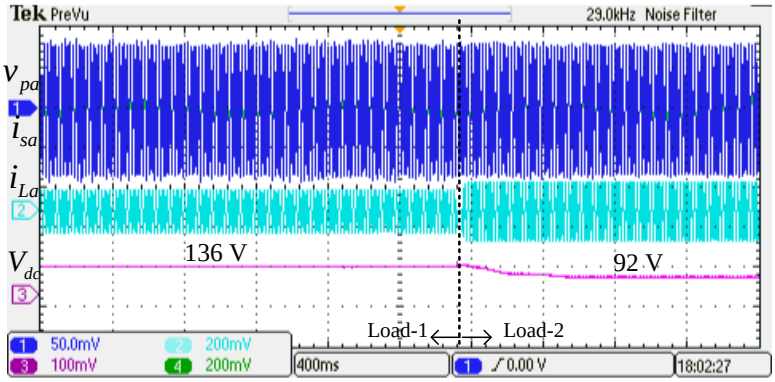


Fig. 5.14 Dynamics of PCC voltage (v_{pa}), source current (i_{sa}), load current (i_{La}) and dc-link voltage (V_{dc}) during compensation

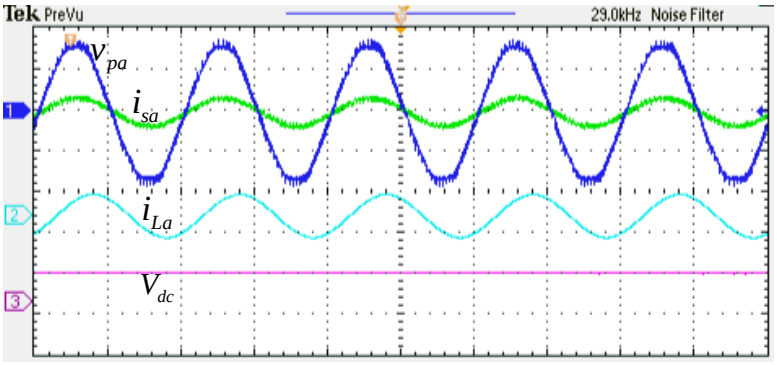


Fig. 5.15 Zoomed figure of Fig. 5.14 during load-1

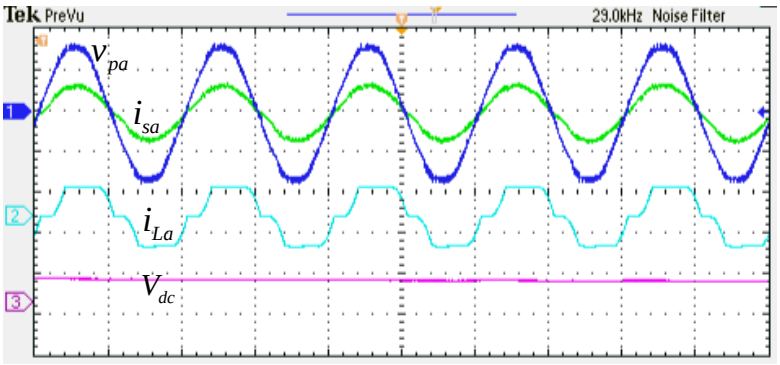


Fig. 5.16 Zoomed figure of Fig. 5.14 during load-2

proposed method, according to load variation, the dc-link voltage is varied as discussed in Section 5.3. Accordingly, the voltage (V_{inv}) also varies and it is observed that the inverter voltage reduced in load-2 compared to load-1 condition because of series ac-capacitor voltage support. The zoom figures of Fig. 5.17 during load-1 and load-2 conditions are shown in Fig. 5.18 and Fig. 5.19, respectively.

The magnitude of three-phase PCC voltages, source currents and supply frequency for load-1 without compensation are shown in Fig. 5.20(a). It is observed that the three-phase source currents are unbalanced with magnitudes of 1.8 A, 1.5 A and 2.1 A. The

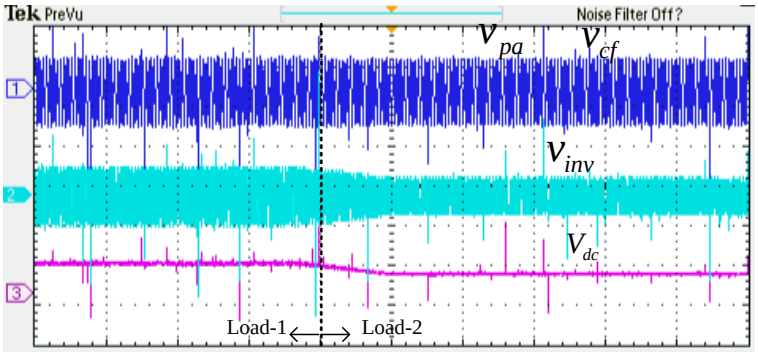


Fig. 5.17 Dynamics of instantaneous PCC voltage (v_{pa}), series ac-capacitor voltage (v_{cf}), inverter output voltage (v_{inv}) and dc-link voltage (V_{dc}) during compensation

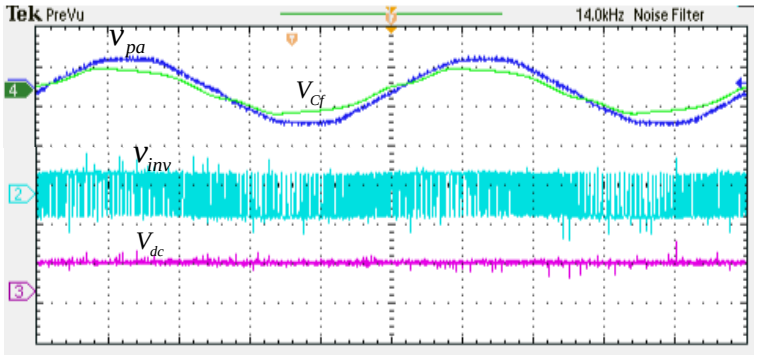


Fig. 5.18 Zoomed figure of Fig. 5.17 during load-1

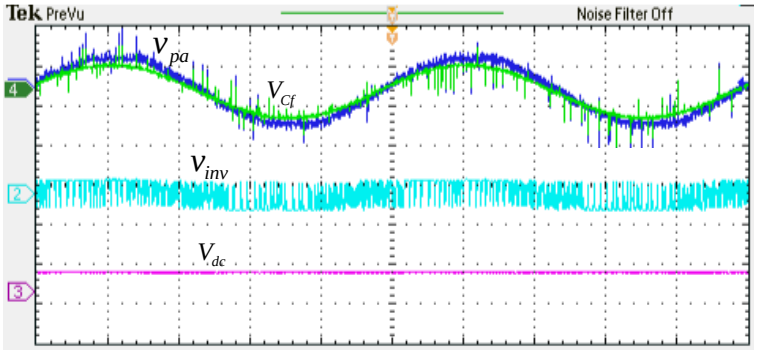
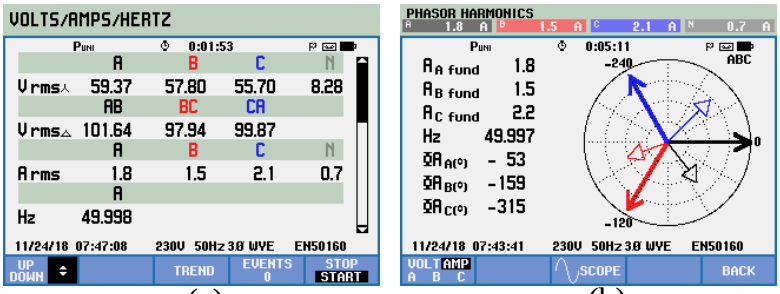


Fig. 5.19 Zoomed figure of Fig. 5.17 during load-2

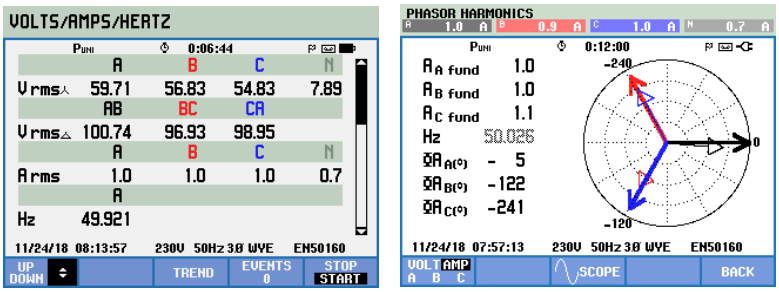
corresponding phasor diagram is shown in Fig. 5.20(b). It is observed that the source current phasors lags respective voltage phasors by -30°, -29°(120-159) and -34°(240-315), respectively.

After compensation, the magnitude of three-phase PCC voltages, source currents and supply frequency are shown in Fig. 5.21(a). It is observed that the three-phase source currents are balanced with magnitudes of 1 A, 1 A and 1A. The corresponding phasor diagram is shown in Fig. 5.21(b). Fig. 5.21(b) shows that, the source current phasors almost in-phase with corresponding voltage phasors. This indicates that, after compensation unity power factor is achieved on source side.



(a) (b)

Fig. 5.20 Before compensation: (a) Magnitude of three-phase PCC voltages (V_{rms}), source currents (A_{rms}) and supply frequency (Hz) and (b) phasor diagram

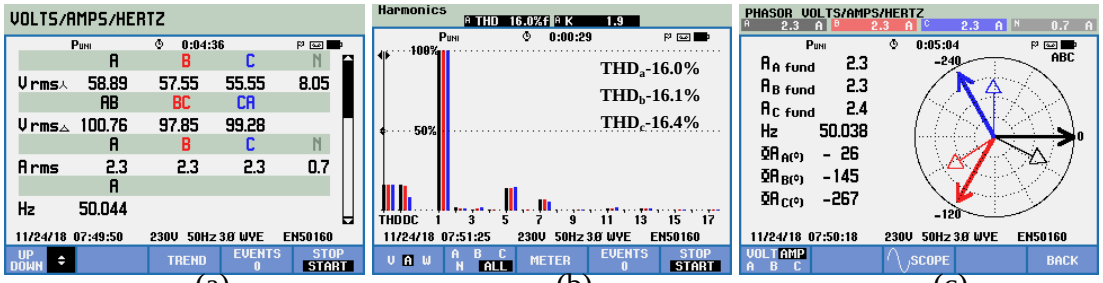


(a) (b)

Fig. 5.21 After compensation: (a) Magnitude of three-phase PCC voltages (V_{rms}), source currents (A_{rms}) and supply frequency (Hz) and (b) phasor diagram

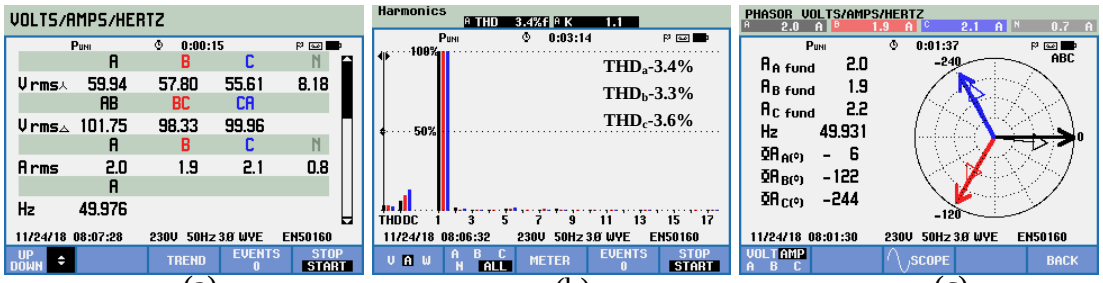
Load-2 consists of three-phase diode bridge with RL-load having non-linear in nature. For this load condition, the magnitude of three-phase PCC voltages, source currents and supply frequency without compensation are shown in Fig. 5.22(a). The corresponding harmonic spectrum and phasor diagram are shown in Fig. 5.22(b) and Fig. 5.22(c), respectively. It is observed from Fig. 5.22(b), that the THDs of three-phase source currents before compensation are 16.0%, 16.1% and 16.4%. The source current phasors lag respective voltage phasors by -26°, -25°(120-145) and -27°(240-267), and are shown in Fig. 5.22(c).

After compensation, the load draws only real component current from supply and these magnitudes are shown in Fig. 5.23(a). The corresponding harmonic spectrum and phasor diagram are shown in Fig. 5.23(b) and Fig. 5.23(c), respectively. The THDs of source currents are reduced to 3.4%, 3.3% and 3.6% and source current phasors lag respective voltage phasors by -6°, -2°(120-122) and -4°(240-244). This indicates that, after compensation unity power factor is achieved on source side and source currents THDs are with in specified limit (below 5% according to IEEE-519 standards).



(a) (b) (c)

Fig. 5.22 Before compensation: (a) Magnitude of three-phase PCC voltages (V_{rms}), magnitude of source currents (A_{rms}) and supply frequency (Hz), (b) source current harmonic spectrum and (c) phasor diagram



(a) (b) (c)

Fig. 5.23 After compensation: (a) Magnitude of three-phase PCC voltages (V_{rms}), magnitude of source currents (A_{rms}) and supply frequency (Hz), (b) source current harmonic spectrum and (c) phasor diagram

5.6 Summary

In this chapter, an adaptive dc-link voltage control for hybrid DSTATCOM is proposed to compensate the unbalanced and non-linear loads in 3P4W distribution system. The performance of adaptive dc-link voltage control algorithm for reactive power compensation, load current balancing and harmonic mitigation is demonstrated through simulation and experimental studies. The proposed method maintains an appropriate dc-link voltage corresponding to load condition. The proposed scheme adjusts the gains of controller corresponding to load operating condition such that the steady state and transient response of dc-link voltage are improved. Also, the dc-link voltage required in the proposed method is low when compared to existing methods. Therefore, the voltage stress across IGBT switches of VSC and switching losses are reduced.

CHAPTER 6

ENERGY MANAGEMENT AND CONTROL OF SINGLE-STAGE SOLAR PV-DSTATCOM WITH BES SYSTEM

In previous chapters, *L*-filter based DSTATCOM, *LCL*-filter based DSTATCOM, and hybrid DSTATCOM topologies were discussed for power quality improvement. In addition to power quality improvement, DSTATCOM is also capable of solar PV power injection to grid. Therefore, in this chapter, Solar Photo-voltaic (SPV) is integrated to grid through DSTATCOM for real power injection along with power quality improvement features. To improve efficiency and reliability of the system, a co-ordinated control of single-stage grid connected SPV and BES system is proposed along with energy management. In this method, the algorithm co-ordinates VSC and BES system based on the State of Charge (SoC) of the battery such that MPPT and power injection are achieved simultaneously. Further, an active rectification operation during non-SPV hours is discussed for better utilization of VSC capacity. The multi-functional features of the proposed method are explained using simulation studies and are also validated through experimental studies.

6.1 Introduction

Solar Photo-voltaic (SPV) energy is one of the most important renewable energies, and now-a-days it has been widely used in distributed generation systems [98]. The rapid growth in development of SPV technologies and applications of SPVs in grid-connected systems indicate that SPVs are an attractive option to produce environmental friendly electricity for diversified purposes [99]. In grid connected SPV system, the maximum available power is delivered to the grid by operating the SPV system at Maximum Power Point (MPP) [100]. The conventional Voltage Source Converter (VSC) along with the interfacing inductor (called DSTATCOM) is the most commonly used interfacing unit in grid-connected SPV system technology due to its simplicity and availability [101].

In three-phase systems, two-stage and single-stage grid connected SPV systems are commonly used topologies. The two-stage system consists of two conversion stages as shown in Fig. 6.1(a): a DC-DC converter stage for MPP tracking and voltage boosting, and a DC-AC inverter stage for interfacing the SPV system to the grid [102], [103]. The two-stage method suffers from reduced efficiency and higher cost; therefore it is not attractive for efficient grid-connected system. On the other hand, a single-stage topology (shown in Fig. 6.1(b)) has gained attention, especially in low voltage applications due to its high efficiency when compared to two-stage conversion. Different single-stage topologies have been proposed, and a comparison of the available conversion units are presented in [104], [105]. In a single-stage grid-connected system, the SPV system utilizes a single conversion unit (dc-ac power inverter) to track MPP and interface the SPV system to the grid. In such a topology, the maximum SPV power is delivered into the grid with high efficiency, small size, and low cost.

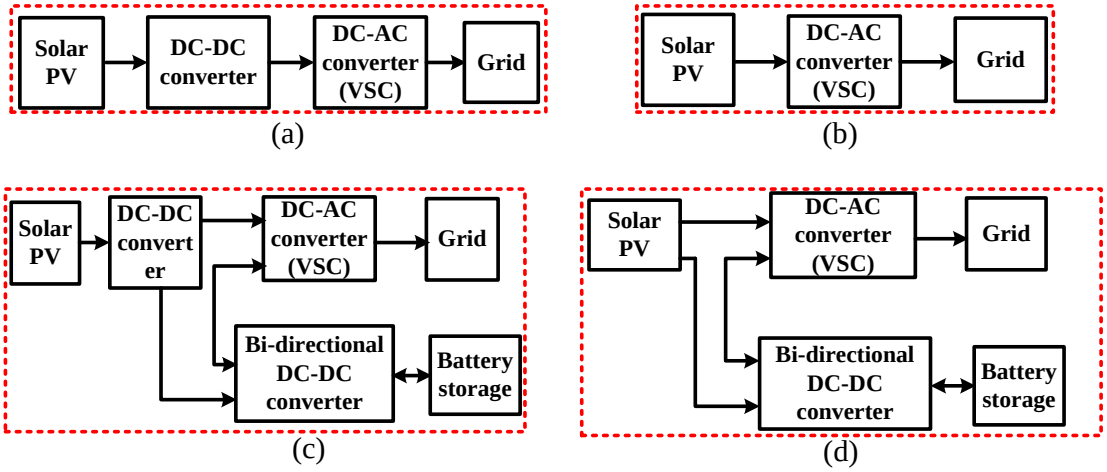


Fig. 6.1 Grid connected SPV systems: (a) two stage (b) single-stage (c) two-stage with BES and (d) single-stage with BES

However, the efficiency of conversion stage is improved, the dynamic load variations and intermittent energy production nature of SPV affect the performance of the grid connected SPV system. To overcome this, energy storage system is added to the grid connected SPV system [106], but it requires energy management schemes. In [107], a two-stage grid connected SPV and battery system with optimum power flow management is discussed for the system shown in Fig. 6.1(c). In [108], an energy management control was proposed for hybrid storage system for different operating modes. A two-stage grid connected SPV system with hybrid energy storage system is discussed with energy management scheme in [109], [110]. However, these systems have hybrid en-

ergy storage devices, where the power conversion is implemented based on two-stage. The schematic diagram of a single-stage SPV with BES is shown in Fig. 6.1(d). A Reconfigurable Solar Converter (RSC) for Photovoltaic (PV) and battery application with single-stage conversion is implemented [111]. The MPP is achieved only during charging of battery or injecting power to grid, but simultaneous charging battery and injecting power to grid is not possible. Also, while charging the battery, the inverter is disconnected from grid. Again for grid connection, synchronization control technique has to be carried out which is burden on the controller.

The above problems are addressed in the proposed method, which is discussed in the next section.

6.2 Proposed Single-Stage SPV-DSTATCOM with BES System

The configuration of the proposed grid connected SPV with battery energy storage system in three-phase four-wire distribution system is shown in Fig. 6.2. It consists of SPV string, VSC, bi-directional DC-DC converter, battery, source and loads. The SPV string consists of series and parallel combination of photo-voltaic modules to match the required voltage and power ratings. VSC is mainly employed for real power injection to grid with MPP tracking of SPV. The additional services provided by VSC in the proposed method are reactive power compensation, balancing of grid currents, and active rectification. In the proposed method, battery energy storage is connected to dc-link of VSC through a bi-directional DC-DC converter to meet the requisite of power management in the grid and load environment.

The overall control algorithm of the proposed method is shown in Fig. 6.3. It mainly consists of reference current generation, power management algorithm, current control and switching pulse generation for DC-DC converter and VSC. The sensor signals of SPV voltage (v_{pv}) and SPV current (i_{pv}) are given to Perturb and Observe (P & O) algorithm. The outputs of P & O algorithm are; estimated voltage ($V_{dc,ref}$) and current (I_{mp}) corresponding to maximum power point, which are derived from voltage and current perturb algorithm, respectively. To operate the SPV at MPP, the dc-link voltage

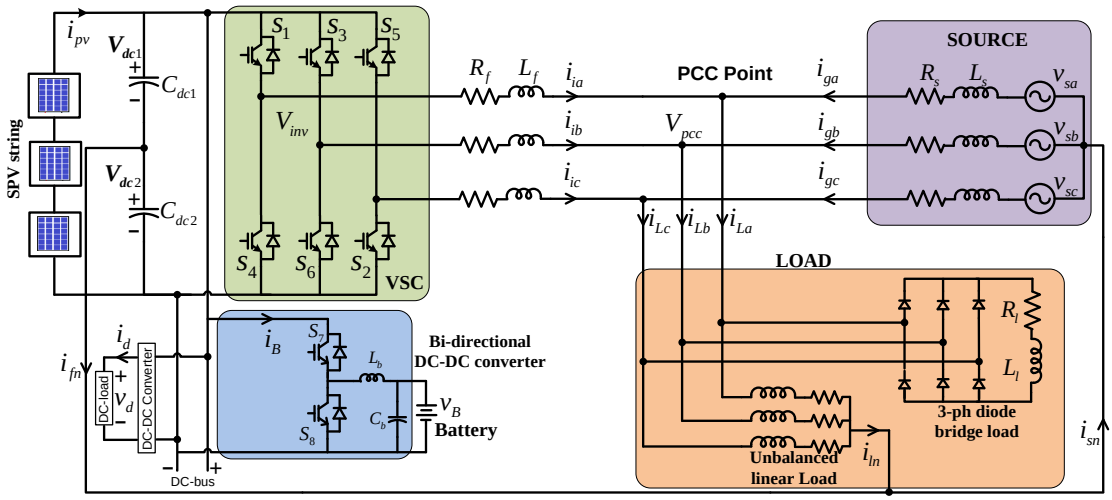


Fig. 6.2 Grid connected SPV and BES system in a three-phase four-wire distribution system

(V_{dc}) of VSC is forcefully maintained at the reference voltage ($V_{dc,ref}$) by PI controller. The output of PI controller is considered as power loss (P_{loss}), which is supplied by grid. The co-ordinated control algorithm is implemented based on the SoC of battery between Low (L) and High (H) conditions. The calculation of SoC of battery is shown in Fig. 6.3 [112].

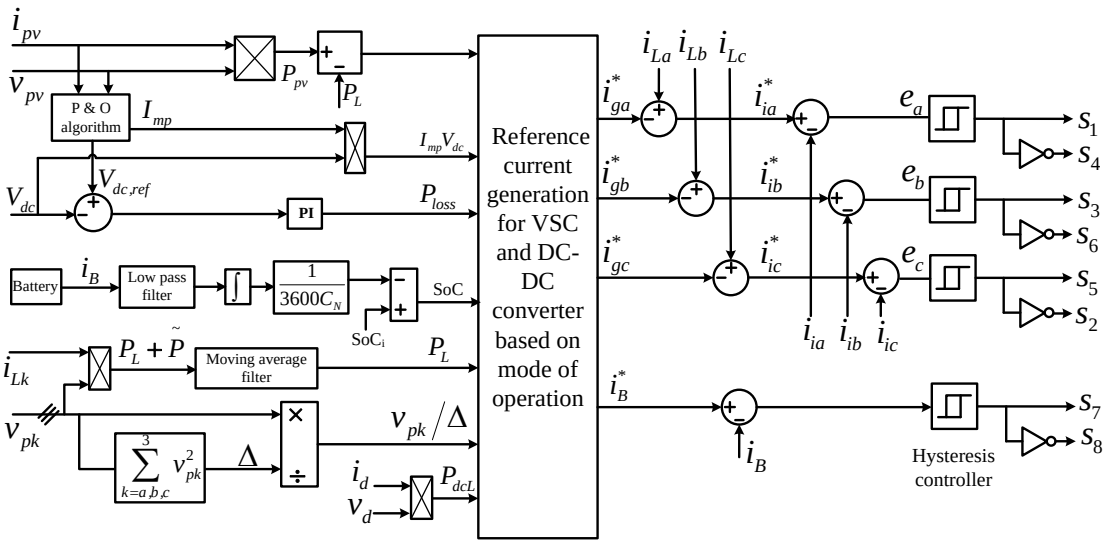


Fig. 6.3 Overall control algorithm for switching pulses generation in the proposed method

The average load real power (P_L) is calculated from the measured instantaneous load currents (i_{Lk}) and PCC voltages (v_{pk}). A Moving Average Filter (MAF) is implemented to eliminate oscillation in average real power. Depending on the difference between available SPV power (P_{pv}) and load real power demand (P_L), the modes of operation are decided. In the proposed energy management, three different modes of operation; Sur-

plus Power Mode (SPM), Deficit Power Mode (DPM), Balanced Power Mode (BPM) are explained. After selecting the mode of operation, the reference currents (i^*_{ga}, i^*_{gb} and i^*_{gc}) on the grid side are generated. These reference currents are in phase opposition to the grid voltage in case of power injection to the grid and in-phase with grid voltage in case of power drawn from the grid. The reference current generation in each mode of operation is explained below.

6.3 Reference Current Generation in Proposed method

Based on the power difference between the solar power and load real power, three modes are identified in the system as follows: 1) Surplus Power Mode (SPM; $P_{pv} > P_L$); 2) Balanced Power Mode (BPM; $P_{pv} = P_L$); 3) Deficit Power Mode (DPM; $P_{pv} < P_L$). In each mode, the reference currents of VSC and DC-DC converter are calculated as follows.

6.3.1 SPM operation during SPV hours

In this mode, the battery is charged until it reaches higher limit of SoC. During this period both DC-DC converter and VSC are co-ordinated with each other to track MPP and power injection to grid. Once the battery SoC reaches the higher limit (i.e., SoC>H), the battery is disconnected and excess power is injected into the grid. The DC-DC converter and VSC reference currents are given below.

Step 1: If L<SoC< H, the battery is charging. During this time the reference currents for VSC and DC-DC converter are,

$$i^*_{ia} = i_{La} - i^*_{ga}; \quad i^*_B = P_B/v_B \tag{6.1}$$

where, i^*_{ga}=$\frac{v_{pa}}{\Delta}[P_L + P_{loss} - I_{mp}V_{dc} + P_B]$ and Δ=$v^2_{pa} + v^2_{pb} + v^2_{pc}$.
Step 2: If SoC>H, the battery is disconnected and the reference current for VSC is,

$$i^*_{ia} = i_{La} - \frac{v_{pa}}{\Delta}[P_L + P_{loss} - I_{mp}V_{dc}]\ ; \quad i^*_B = 0 \tag{6.2}$$

6.3.2 BPM operation during SPV hours

In this mode, the total solar power is supplied to load through VSC. The reference currents at the time of power supplied to the load are as follows:

Step 1: If SoC <L, the battery is disconnected and reference current for VSC is,

$$i_{ia}^{*} = i_{La} - \frac{v_{pa}}{\Delta}[P_L + P_{loss} - I_{mp}V_{dc}]\ ; \quad i_B^{*} = 0 \tag{6.3}$$

Step 2: If L<SoC<H, the battery is discharging. The reference currents in case of battery power is injecting to grid are,

$$i_{ia}^{*} = i_{La} - \frac{v_{pa}}{\Delta}[P_L + P_{loss} - I_{mp}V_{dc} - P_B]\ ; \quad i_B^{*} = \frac{P_B}{v_B}. \tag{6.4}$$

Instead of injecting to grid, if battery power is supplied to dc-loads, the losses in VSC are absent. In this case, the reference current are,

$$i_{ia}^{*} = i_{La} - \frac{v_{pa}}{\Delta}[P_L + P_{loss} - I_{mp}V_{dc}]\ ; \quad i_B^{*} = \frac{P_B}{v_B} \tag{6.5}$$

6.3.3 DPM operation during SPV hours

In this mode, the deficit power is drawn from the battery by discharging if available, otherwise it is drawn from the grid. The battery power has to include in the VSC references to track MPP; otherwise it operates the SPV other than MPP. The references for DC-DC converter and VSC are,

Step 1: If SoC<L, the battery is disconnected, and the reference currents for VSC is,

$$i_{ia}^{*} = i_{La} - \frac{v_{pa}}{\Delta}[P_L + P_{loss} - I_{mp}V_{dc}]\ ; \quad i_B^{*} = 0 \tag{6.6}$$

Step 2: If L<SoC<H, the battery is discharging. The reference currents are,

$$i_{ia}^{*} = i_{La} - \frac{v_{pa}}{\Delta}[P_L + P_{loss} - I_{mp}V_{dc} - P_B]\ ; \quad i_B^{*} = \frac{P_B}{v_B} \tag{6.7}$$

In BPM and DPM, the battery operated in discharging mode is preferred to that of charging mode, due to better efficiency of operation. However, if the DC-DC converter

is implemented with soft switching methods, and the grid has low transmission loss, the battery charging mode is also preferred.

6.3.4 Reference current generation during non-SPV hours

During non-SPV hours, if the load reactive power (Q_L) is equal to the VSC rating ($S_{vsc,r}$), DSTATCOM is operated as a compensator only and the reference currents are given as,

$$i_{ia}^{*} = i_{La} - \frac{v_{pa}}{\Delta}[P_L + P_{loss}]; \quad i_B^{*} = 0 \tag{6.8}$$

Otherwise, DSTATCOM is operated in active rectification mode apart from compensation. Under this condition, the dc-loads draw power from the grid by rectification action as per demand. But, the battery charging or discharging from or to the grid depends on SoC and is discussed below.

Step 1: If SoC>H, the battery is disconnected. During this time, the dc-loads are supplied from grid by rectification action of VSC and the reference currents are,

$$i_{ia}^{*} = i_{La} - \frac{v_{pa}}{\Delta}[P_L + P_{loss} + P_{dcL}]; \quad i_B^{*} = 0 \tag{6.9}$$

Step 2: If L<SoC<H, the battery is charged from grid by active rectification action of VSC. In this case, the reference currents for VSC and DC-DC converter are given as,

$$i_{ia}^{*} = i_{La} - \frac{v_{pa}}{\Delta}[P_L + P_{loss} + P_B]; \; i_B^{*} = \frac{P_B}{v_B} \tag{6.10}$$

The reference currents (i_{ia}^{*}, i_{ib}^{*} and i_{ic}^{*}) in each mode are compared with measured currents (i_{ia}, i_{ib} and i_{ic}), and errors (e_a, e_b and e_c) are given to hysteresis controller. The gate pulses generated by hysteresis controller are given to switches of VSC as S_1 to S_6 and DC-DC converter as S_7 and S_8 shown in Fig. 6.2.

For better understanding of the proposed energy management scheme, the SPV and non-SPV hours modes of operations along with reference current in each mode are specified in flow-chart shown in Fig. 6.4.

The comparison between existing and the proposed methods for energy conversion in grid connected SPV is given in Table 6.1. The advantages of the proposed method when compared to existing single-stage method are 1) Better utilization of VSC capacity dur-

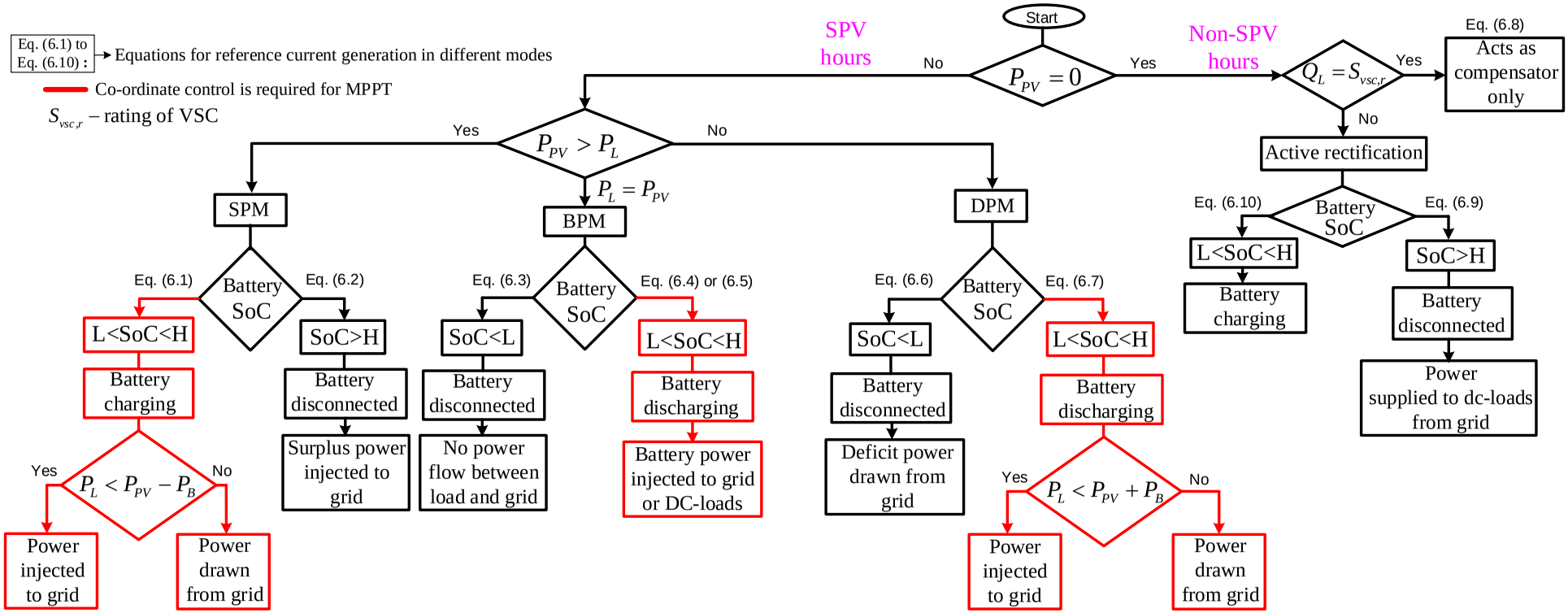


Fig. 6.4 Flow-chart for different modes of operation in SPV and BES system with the proposed energy management scheme

Table. 6.1 Comparison between different grid connected solar PV systems with respect to power conversion stages

Topology⟶ Parameter ↓	Two-stage [113]	Single-stage [114]	Two-stage with BES [107]	Single-stage with BES [111]	Proposed single-stage with BES
Uni-directional dc-dc converter (C_1) rating	P_{pv}	absent	P_{pv}	absent	absent
Bi-directional dc-dc converter (C_2) rating	absent	absent	P_B	P_B	P_B
VSC rating	P_{pv}+Q_L	P_{pv}+Q_L	P_{pv}+P_B+Q_L	P_{pv}+P_B+Q_L	P_{pv}+P_B+Q_L
VSC utilization (SPV hours)	P_{pv}+Q_L	P_{pv}+Q_L	P_{pv}+P_B+Q_L	P_{pv}+P_B+Q_L	P_{pv}+P_B+Q_L
VSC utilization (non-SPV hours)	Q_L	Q_L	Q_L	Q_L	Q_L+P_{dc}
MPPT operating point achieved by	C_1	VSC	C_1	VSC	co-ordinated control of C_2 and VSC
Resynchronization requirement	No	No	No	Yes	No
Active rectification (during non-SPV)	not present	not present	not present	not present	Achieved by VSC

P_{pv}-SPV power, P_B-battery power, Q_L-load reactive power, P_{dc}-dc-load power.

ing non-SPV hours. 2) Non-requirement of resynchronization algorithm because of simultaneous achievement of MPP tracking and power conversion by co-ordinated control of VSC and BES system. 3) Achievement of active rectification with the proposed algorithm to feed power to dc-loads.

6.4 Simulation Studies

Detailed simulation studies of single-stage SPV-DSTATCOM and BES are carried out using MATLAB/Simulink software with the proposed energy management scheme. The simulation parameters are given in Table 6.2. The performances of the proposed method under various operating modes are presented in this section.

Table. 6.2 Simulation parameters for single-stage SPV with BES system

Symbol	System parameters	Values
V_s	Supply voltage	230 V
Z_s	Source impedance	0.2 Ω, 0.1 mH
L_f	Interfacing inductance	32 mH
C_{dc1}, C_{dc2}	DC-link capacitances	1100 μF each
h	Hysteresis band	± 0.2 A
V_{dc1}, V_{dc2}	Rated dc-link voltages	550 V each
Battery converter parameters: L_b= 5 mH, C_b= 100 μF		
PI controller parameters: k_p=60, k_i= 0.1		
Solar PV parameters: MPP voltage is 17.4 V, MPP current is 6.2 A. Number of panels in series are 64, MPP power is 6904 W.		
Load-1: Three-phase balanced load : 28 Ω, 60 mH Load-2: Combination of load-1 and unbalanced linear load of phase-*a*: 16 Ω, 40 mH; phase-*b*: 36 Ω, 40 mH; phase-*c*: 22 Ω, 40 mH DC-load: 3400 W on dc-side of VSC		

6.4.1 Performance during SPV hours with variable load

The dynamics of real power flow corresponding to the modes of operation in the proposed method is shown in Fig. 6.5. Up to the period t=1 s, only VSC is operated, because of which SPV power (P_{pv}) is equal to converter injecting power (P_{vsc}). During this period, the load power (P_L) is less than P_{pv}, and thus excess power is injected into the grid, which is represented as P_g. From t=1 s to t=5 s, both VSC and DC-DC converters are operated and the mode of operation is selected based on available powers, P_{pv} and P_L. In each mode, the power management is decided depending on SoC of the battery and explained below. Two modes of operation are identified from Fig. 6.5, and these are: 1) SPM from t=1 s to t=3 s, 2) DPM from t=3 s to t=5 s.

SPM ($P_{pv} > P_L$):

During the period t=1 s to t=2 s, SPV power is more than load power and the SoC of battery is L<SoC<H, and part of the surplus power is utilized for charging the battery. As the battery is charging, the power injected through VSC (i.e., P_{vsc}) is reduced, which also reduces the power injection to grid, that is P_g. At t=2 s, the SoC of battery is SoC>H; this condition forces the controller to make battery current to zero (i.e., nothing

but P_B=0). As the battery is charged fully, excess power is injected to grid only, which is observed from t=2 s to t=3 s (increase of P_g in the negative direction), shown in Fig. 6.5.

DPM ($P_{pv} < P_L$):

The load is increased at t=3 s, which makes the load power more than SPV power and SoC of battery is L<SoC<H. During this condition both P_{pv} and P_B (battery discharging) are supplied to load through VSC, taken as P_{vsc}. It is observed that the load power is remaining more than the sum of battery and SPV powers; therefore the required remaining power for the load is drawn from the grid, and is shown as positive power P_g from t=3 s to t=4 s. At t=4 s, the SoC of the battery is SoC<L, this condition stops the discharging of battery and the controller forces P_B to zero.

The dynamics of battery for the above operations from t=0 s to t=5 s is shown in Fig. 6.6. It consists of SoC curve of battery, battery current (i_B) and battery voltage (v_B).

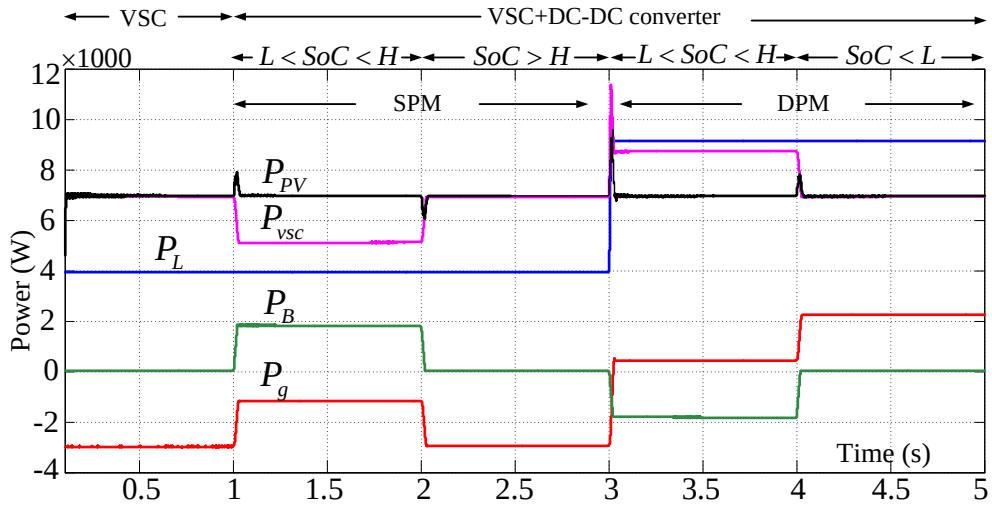


Fig. 6.5 Dynamics of real powers flow during SPV hours (P_{pv}: SPV power, P_{vsc}: VSC injecting power, P_L: load real power, P_B: battery power, P_g: grid power)

During the time period t=0 s to t=5 s, the dynamics of DC-link voltages is shown in Fig. 6.7. It is observed from Fig. 6.7, that the dc-link voltages are maintained constant at 550 V except for a small variation at t=3 s, because of the dynamic load variation. But, the control algorithm makes the dc-link voltages balanced with ripple voltage of 2 V peak to peak.

The combination of instantaneous grid voltage-load current and grid voltage-grid cur-

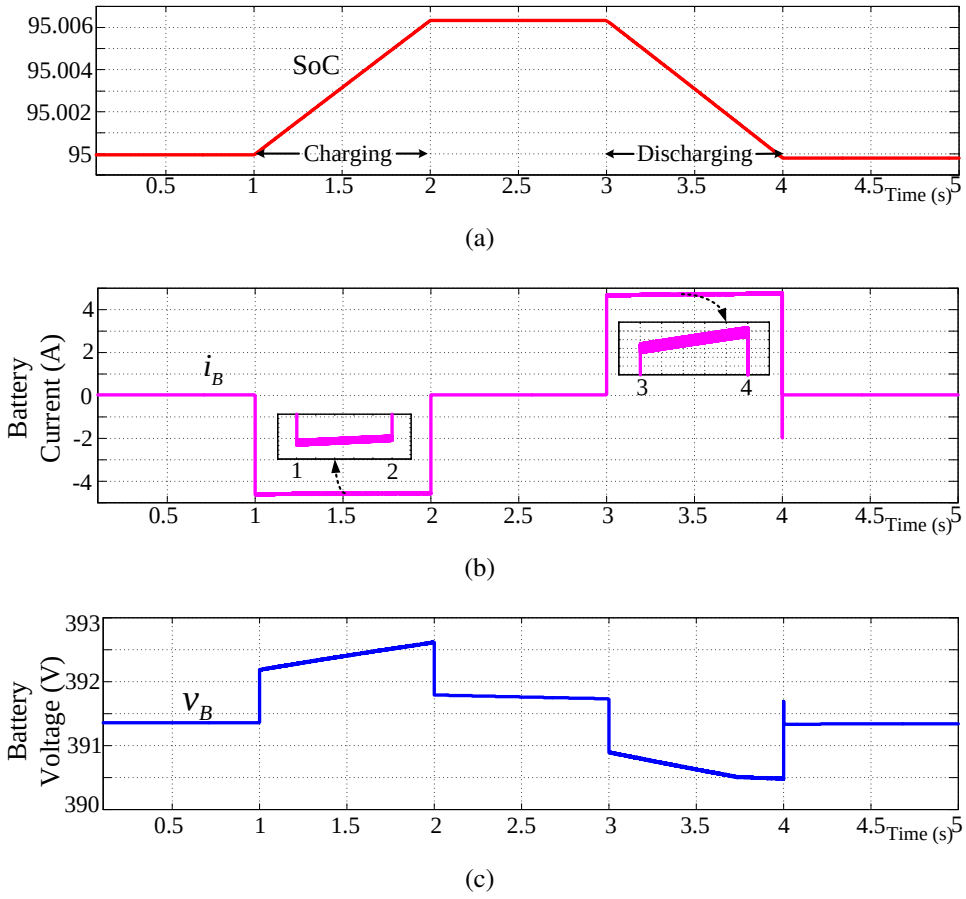


Fig. 6.6 Dynamics of battery during SPV hours (a) SoC curve (b) battery current (i_B) and (c) battery voltage (v_B)

rent are shown in Fig. 6.8. Fig. 6.8(a) shows phase-a grid voltage (v_{pa}) and load current (i_{La}) for load variation at t=3 s. In both the load conditions, the load current lags the grid voltage, which is observed from the zoomed figure from t=2.92 s to t=3.08 s. During SPV power injection and reactive power compensation by DSTATCOM, phase-a grid voltage (v_{pa}) and grid current (i_{ga}) are shown in Fig. 6.8(b). The following points are observed from Fig. 6.8(c): 1) At t=1 s, battery is in charging state, so that the current injection to grid is reduced, which is observed from the zoomed figure from t=0.92 s to t=1.08 s. 2) At t=2 s, the battery is fully charged, therefore the grid current increases again. 3) From t=3 s onwards, the load draws real power from the grid to meet the load real power requirement. Therefore, the grid current is in-phase with voltage as shown in zoomed figure from t=2.92 s to t=3.08 s. 4) At t=4 s, the battery SoC reaches lower value (i.e., SoC<L), and the power drawn from the grid increases. Therefore, the grid current increases and it is in-phase with grid voltage as shown in the zoomed figure from t=4.44 s to t=4.52 s.

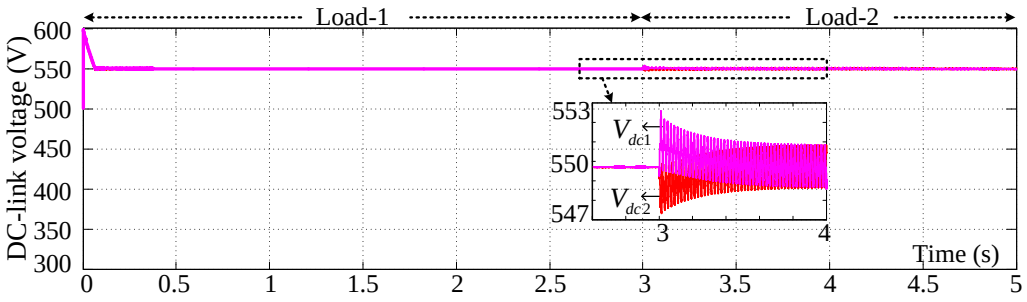
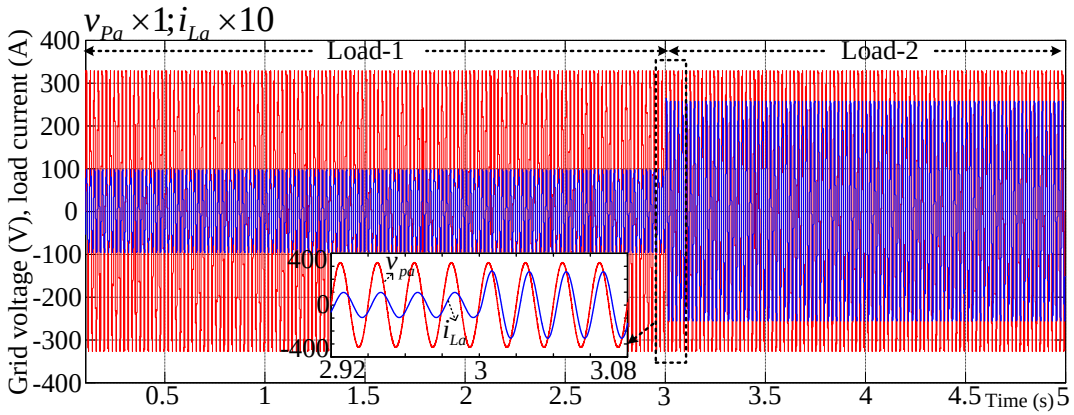
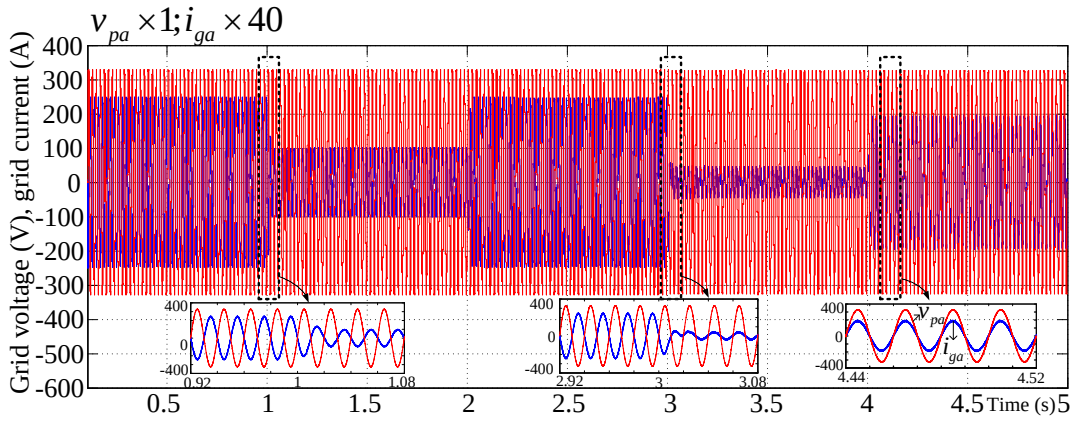


Fig. 6.7 Dynamics of dc-link voltages (V_{dc1}, V_{dc2})



(a)



(b)

Fig. 6.8 (a) Grid voltage (v_{pa}) and load current (i_{La}) (b) grid voltage (v_{pa}) and grid current (i_{ga})

6.4.2 Performance during non-SPV hours with variable load

In case of non-SPV hours, the dynamics of real power flow in the system with the proposed method is shown in Fig. 6.9(a). It is observed from Fig. 6.9(a) that initially ac-load is connected to the system and some time later, from t=3 s to t=4 s, an additional dc-load is connected. The modes of operation in this case are explained below with respect to Fig. 6.9(a).

Mode-1: Reactive power compensation only during t=(0-1) s and t=(2-3) s; During this period, DSTATCOM acts as compensator and the load required real power is supplied by grid, therefore $P_L = P_g$. The battery is not in operation and VSC is not injecting any real power, therefore $P_B = 0$ and $P_{vsc} = 0$.

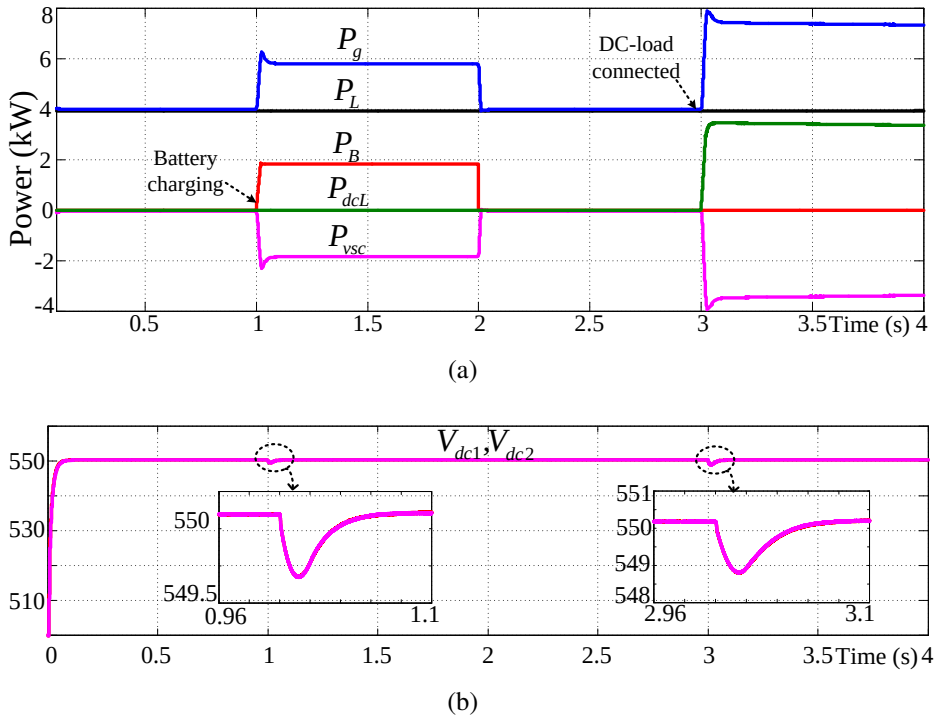


Fig. 6.9 (a) Dynamic of real powers flow during non-SPV hours (P_{dcL}: dc load power, P_{vsc}: VSC injecting power, P_L: ac load power, P_B: battery power, P_g: grid power) and (b) dc-link voltages

Mode-2: Active rectification along with compensation mode during t=(1-2) s and t=(3-4) s; At t=1 s, the battery starts charging and it takes real power of P_B from grid by rectification action. During this period, from t=1 s to t=2 s, $P_g = P_L + P_B$ and $P_{vsc} = -P_B$. At t=3 s, an additional dc-load is connected to DC-bus as shown in Fig. 6.2. The dc-load draws power from the grid through active rectification action of VSC and during this period from t=3 s to t=4 s, $P_g = P_L + P_{dcL}$ and P_{vsc} =-P_{dcL}.

The dynamics of dc-link voltages during non-SPV hours is shown in Fig. 6.9(b). At t=1 s, a dip in the dc-link voltage is observed because battery load is connected at this instant. Again one more dip is observed at t=3 s, because of an additional dc-load connection at this instant. Except these dips at t=1 s and t=3 s, the dc-link voltages are maintained constant with the proposed method during non-SPV hours. The dynamics of battery during non-SPV hours with respect to Fig. 6.9(a) is shown in Fig. 6.10. It consists of SoC curve, battery current (i_B) and battery voltage (v_B). The quantified

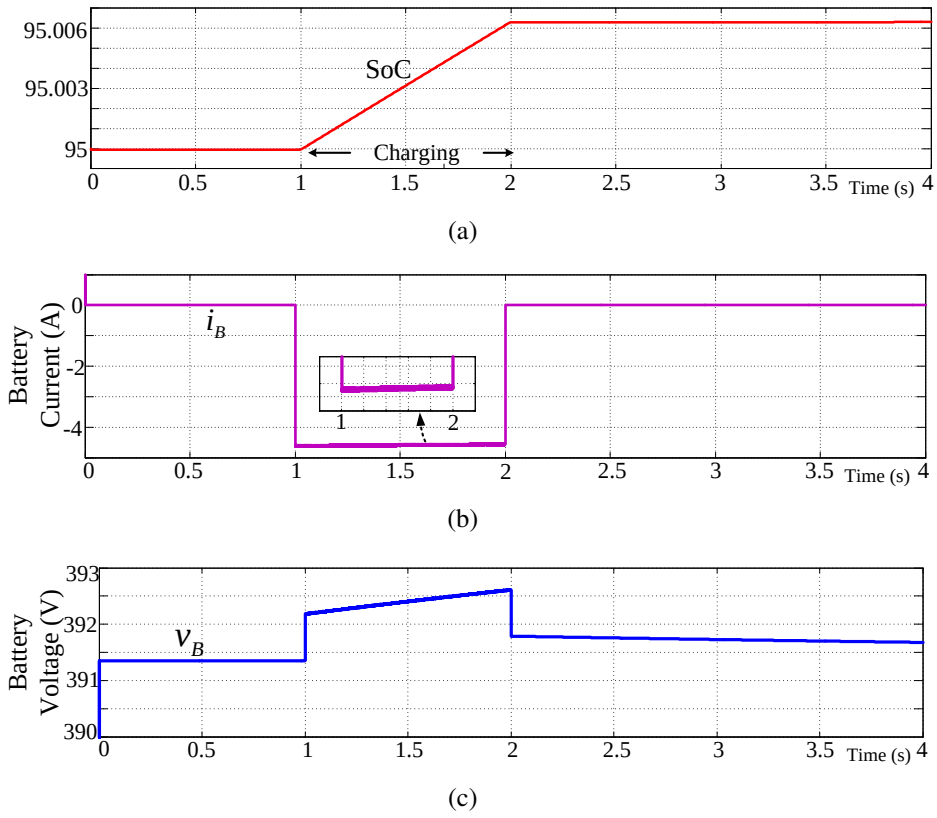


Fig. 6.10 Dynamics of battery during non-SPV hours (a) SoC curve (b) battery current (i_B) and (c) battery voltage (v_B)

values of real and reactive power flow in the system are given in Table 6.3 with respect to power curves shown in Fig. 6.5 and Fig. 6.9 during SPV hours and non-SPV hours, respectively.

6.5 Experimental Studies

The performance of the proposed method is verified for a reduced line-line voltage of 60 V. The experimental parameters are given in Table 6.4. Here, two loads are considered to examine the power flow dynamics with SPV power injection and battery charging or discharging conditions. The control algorithm is implemented by dSPACE MicroLabBox DS-1202. The following modes of operations are performed.

The experimental waveforms on grid side without real power injection from SPV and without compensation are shown in Fig. 6.11. It consists of phase-a grid voltage (v_{ga}), load current (i_{La}), three-phase average load reactive power (Q_L) and average load real power (P_L) drawn from grid.

Table. 6.3 Power flow in the proposed energy management scheme (with reference to Fig. 6.5 and Fig. 6.9(a))

	SPV hours (P_{pv}= 6910 W)					Non-SPV hours (P_{pv}= 0 W)			
	VSC	VSC+DC-DC converter				M-1*	M-2#	M-1*	M-2#
Time⟶ Power ↓	(0-1) s	(1-2) s	(2-3) s	(3-4) s	(4-5) s	(0-1) s	(1-2) s	(2-3) s	(3-4) s
P_g(W)	-2958	-1155	-2958	425	2248	3974	5780	3974	7360
P_L(W)	3937	3935	3937	9141	9137	3930	3928	3930	3927
P_{vsc}(W)	6900	5090	6900	8720	6890	-42	-1850	-40	-3440
P_B(W)	4	1818	4	-1820	4	1810	0	0	0
P_{dcL}(W)	0	0	0	0	0	0	0	0	3400
Q_g(var)	-44	-38	-45	-47	-42	-20	-14	-22	-1
Q_L(var)	2649	2648	2649	5771	5768	2644	2643	2644	2642
Q_{vsc}(var)	2696	2687	2696	5818	5811	2644	2643	2644	2642

* Mode-1, # Mode-2, P_g=P_L-P_{vsc}, P_{vsc}=P_{pv}±P_B+P_{dcL}.

Table. 6.4 Experimental parameters for single-stage SPV-DSTATCOM with BES system

Symbol	System parameters	Values
V_s	Supply voltage	60 V (L-L)
V_{dc}	Rated dc-link voltage	156 V
L_f	Interfacing inductance	12 mH
C_{dc1}, C_{dc2}	DC-link capacitances	2400 μF each
Solar PV parameters: MPP voltage is 17.4 V, MPP current is 3.2 A. Number of panels in series are 9, MPP power is 501 W.		
Load-1: Three-phase inductive-resistive load of 12 Ω and 8 mH. Load-2: Combination of three-phase diode bridge load of 15 Ω, 50 mH and load-1.		

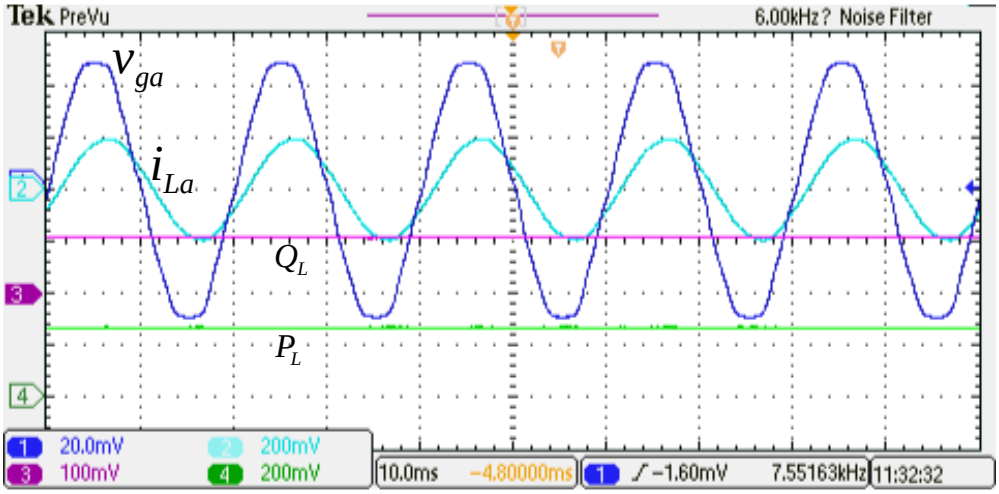


Fig. 6.11 Experimental waveforms on grid side without real power injection from SPV and without compensation (v_{ga} 20 V/div, i_{La} 4 A/div, Q_L 100 var/div and P_L 200 W/div)

6.5.1 Performance during SPV hours

Two modes of operations are considered in experimental validation of the proposed method. These modes of operation are explained below.

SPM operation:

The dynamics of average real power variations in the system for load-1 is shown in Fig. 6.12. It consists of SPV injecting power (P_{pv}), grid power (P_g), battery power (P_B), load average power (P_L) and VSC injecting power (P_{vsc}).

- During t_1 period: P_{pv}=0 W, P_g=262 W (supplied by grid), P_B=0 W, P_L=262 W and P_{vsc}=0 W.
- During t_2 period: P_{pv}=500 W, P_g=−238 W (delivered to grid), P_B=0 W, P_L=262 W and P_{vsc}=500 W.

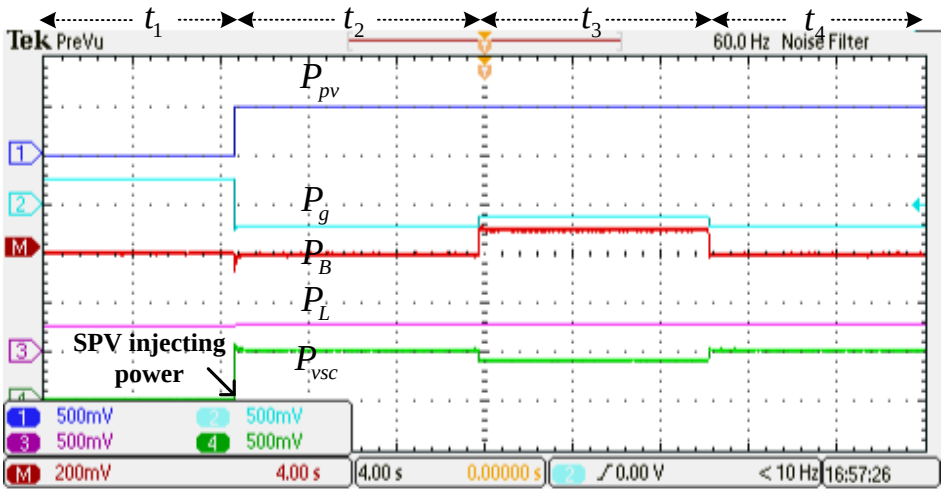
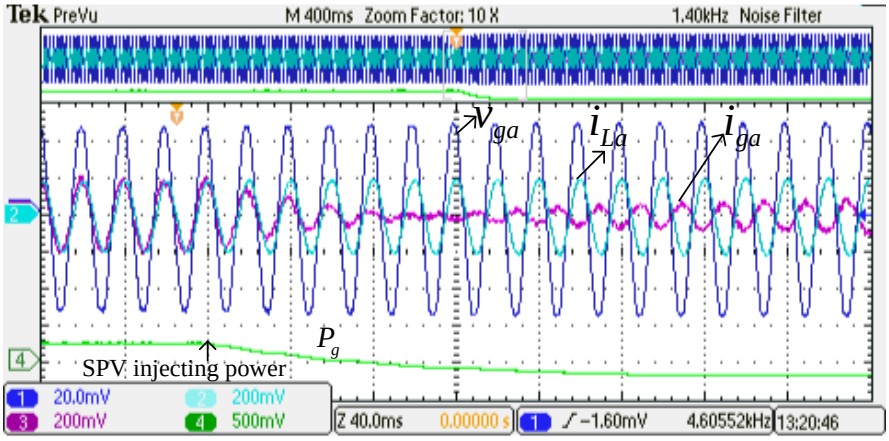


Fig. 6.12 Dynamics of real powers in the system during SPM operation (P_{pv}, P_g, P_L, P_{vsc} 500 W/div, P_B 200 W/div)

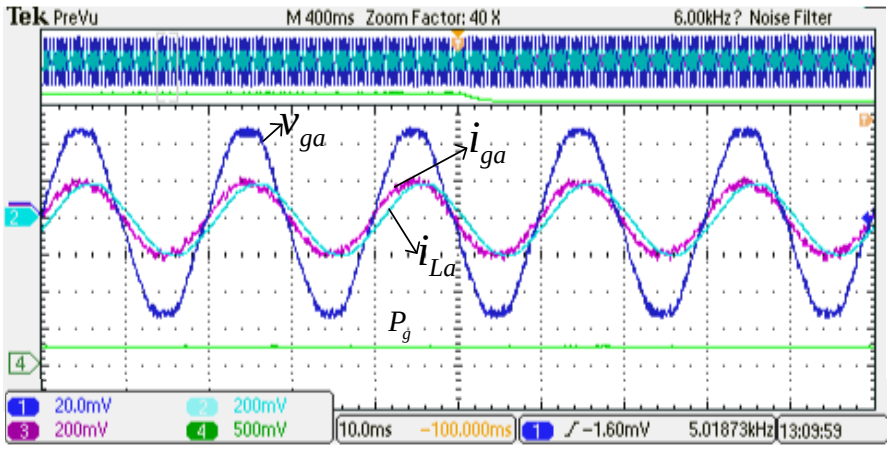
- During t_3 period: P_{pv}=500 W, P_g=−135 W (delivered to grid), P_B=100 W (charging), P_L=262 W & P_{vsc}=400 W.
- During t_4 period: P_{pv}=500 W, P_g=−235 W (delivered to grid), P_B=0 W, P_L=262 W & P_{vsc}=500 W.

During the transition from t_1 period to t_2 of Fig. 6.12, the grid voltage (v_{sa}), load current (i_{La}), grid current (i_{ga}) and grid side real power (P_g) are shown in Fig. 6.13(a). Before SPV power injection, load required reactive power is supplied by DSTATCOM, and real power is drawn from grid, therefore grid current (i_{ga}) is in-phase with grid voltage (v_{sa}), which is observed from Fig. 6.13(b). After SPV starts injecting power, the excess real power other than that required by the load is fed to the grid and this mode is named as surplus power mode. During this mode, the grid current (i_{ga}) is out of-phase with grid voltage (v_{sa}) and grid power (P_g) is negative, an evident from Fig. 6.13(c).

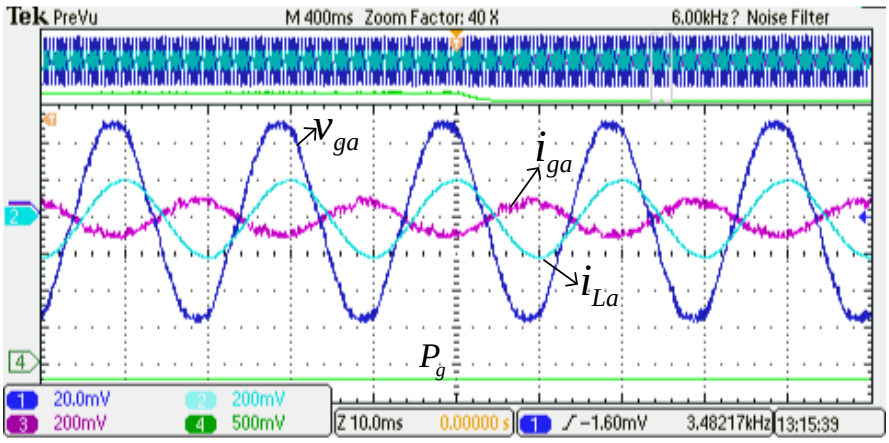
The three-phase grid voltage and grid current phasors before and after compensation without SPV injecting power for load-1 are shown in Fig. 6.14(a) and Fig. 6.14(b), respectively. It is observed that, before compensation, the grid currents lag the corresponding grid voltages by −24°, −23°(−143+120) and −22°(−262+240), respectively as shown in Fig. 6.14(a). After compensation, the grid currents are almost in-phase with the corresponding grid voltages as shown in Fig. 6.14(b). Fig. 6.15(a) shows the phasor diagram during SPV injection power. In this case, SPV power is more than load power, therefore the excess power is injected to the grid, and the current phasors are out of phase with grid voltages. As the battery is charging from SPV power, the power injection into the grid is reduced. During this period, the phasor diagram is shown in Fig.



(a)



(b)



(c)

Fig. 6.13 SPM operation (a) dynamics of system before and after solar power injection, (b)&(c) are zoomed figures of (a) before and after SPV injection, respectively (v_{ga} 20 V/div, i_{ga}, i_{La} 4 A/div and P_g 500 W/div)

6.15(b). It is observed that the current injecting into the grid is reduced when compared to current magnitudes in Fig. 6.15(a), because of the charging of battery.

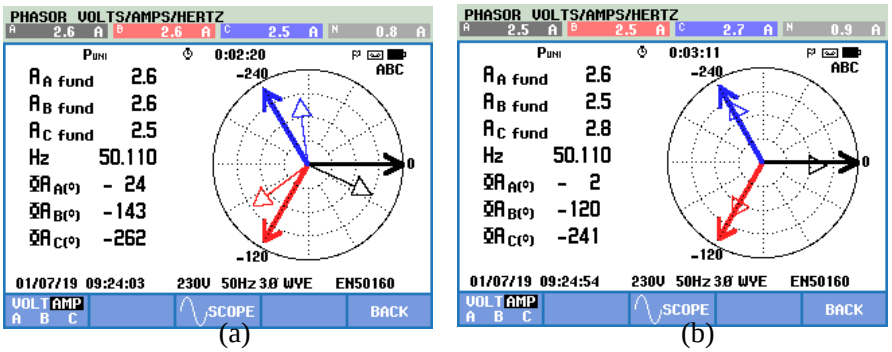


Fig. 6.14 Three-phase grid voltages and grid currents phasors without SPV injecting power for load-1 (a) before compensation and (b) after compensation

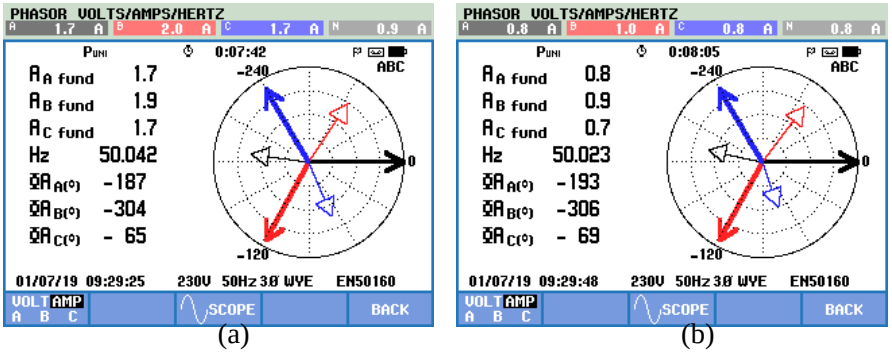


Fig. 6.15 Three-phase grid voltages and grid currents phasors with SPV power injection during SPM operation (a) without charging or discharging of battery and (b) with charging battery during the time period of t_3 shown in Fig. 6.12

DPM operation:

The dynamics of average real power variations in the system for load-2 is shown in Fig. 6.16. It consists of SPV injecting power (P_{pv}), grid power (P_g), battery power (P_B), load average power (P_L) and VSC injecting power (P_{vsc}). It is observed that SPV injecting power is lower than load required power, and as a result it is operated in deficit power mode.

- During t_1 period: P_{pv}=0 W, P_g=−362 W (supplied by grid), P_B=0 W, P_L=362 W and P_{vsc}=0 W.
- During t_2 period: P_{pv}=200 W, P_g=−162 W (supplied by grid), P_B=0 W, P_L=362 W and P_{vsc}=200 W.
- During t_3 period: P_{pv}=200 W, P_g=−62 W (supplied by grid),P_B=100 W (discharging), P_L=362 W, P_{vsc}=300 W.
- During t_4 period: P_{pv}=200 W, P_g=−162 W (supplied by grid), P_B=0 W, P_L=362 W & P_{vsc}=200 W.

During the transition from t_1 period to t_2 of Fig. 6.16, the grid voltage (v_{ga}), load current

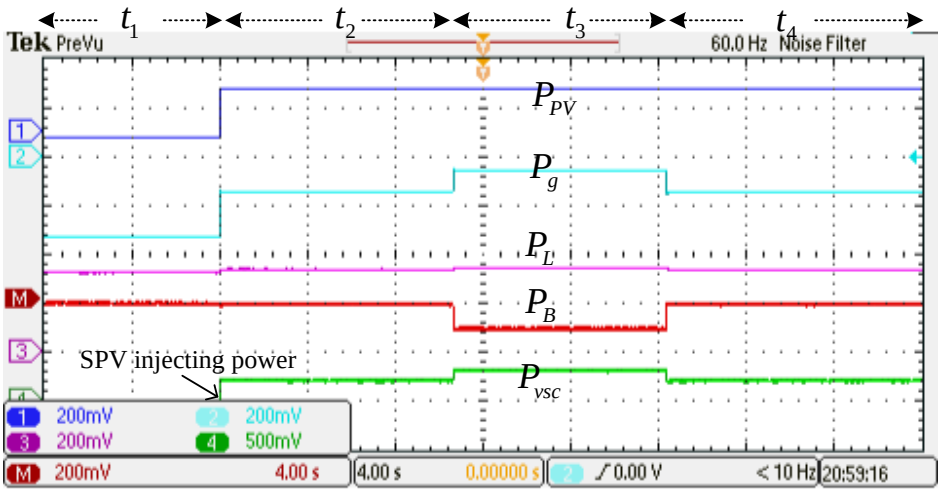
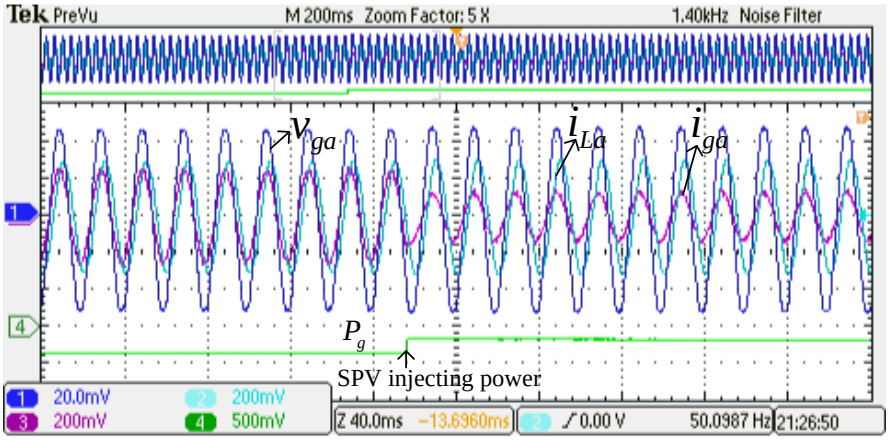


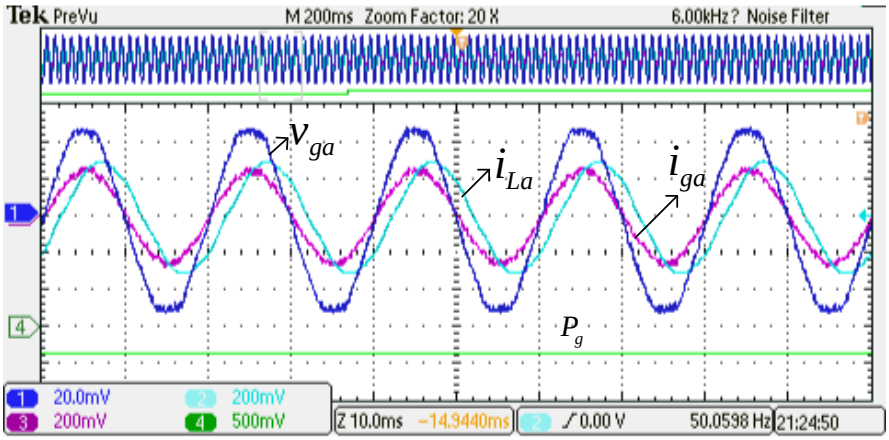
Fig. 6.16 Dynamic of real powers in the system during DPM operation (P_{pv}, P_g, P_B, P_L 200 W/div, P_{vsc} 500 W/div)

(i_{La}), grid current (i_{ga}) and grid side real power (P_g) are shown in Fig. 6.17(a). Before SPV power injection, load reactive power is supplied by DSTATCOM, and real power is drawn from grid; therefore grid current (i_{ga}) is in-phase with grid voltage (v_{ga}), which is observed from Fig. 6.17(b). After SPV starts real power injection, grid current (i_{ga}) is still in-phase with grid voltage (v_{ga}) as shown in Fig. 6.17(c). This is because the injecting power of SPV is not sufficient to meet real power demand by load.

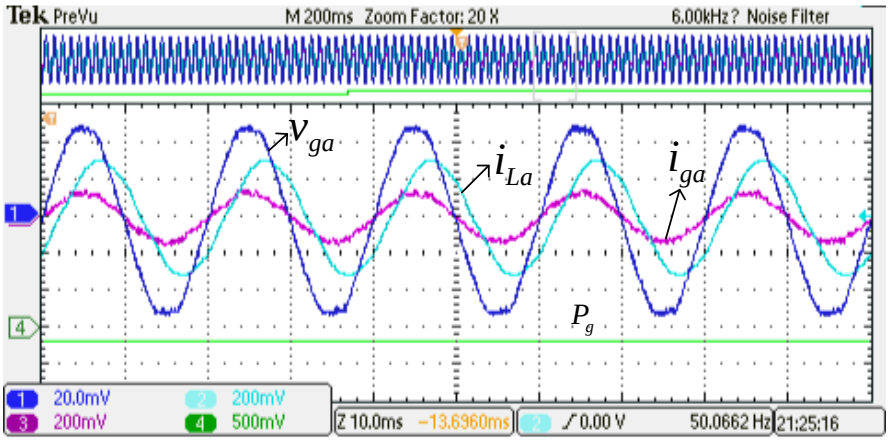
The three-phase grid voltage and grid current phasors before and after compensation without SPV power injection for load-2 are shown in Fig. 6.18(a) and Fig. 6.18(b), respectively. It is observed that, before compensation, the grid currents lag the corresponding grid voltages by $-39°$, $-40°(-160+120)$ and $-39°(-279+240)$, respectively, as shown in Fig. 6.18(a). After compensation, the grid currents are almost in-phase with the corresponding grid voltages as shown in Fig. 6.18(b). Fig. 6.19(a) shows the phasor diagram during SPV injection power in DPM. In this case, the deficit power is drawn from grid such that the source current phasors are in-phase with grid voltage phasors. As the battery is discharging, the power drawn from the grid is reduced. The phasor daigram during this period is shown in Fig. 6.19(b). It is observed that the currents drawn from grid are reduced to 0.9 A, 0.8 A, 1 A when compared to currents of 1.7 A, 1.6 A, 1.9 A in Fig. 6.19(a), because of discharging of battery.



(a)



(b)



(c)

Fig. 6.17 DPM operation (a) dynamics of system before and after solar power injection, (b)&(c) are zoomed figures of (a) before and after SPV power injection, respectively (v_{ga} 20 V/div, i_{ga}, i_{La} 4 A/div and P_g 500 W/div)

6.5.2 Performance during non-SPV hours

The dynamics of the system during non-SPV hours is shown in Fig. 6.20. It consists of load average power (P_L), grid current (i_{ga}), grid power (P_g) and VSC power (P_{vsc}).

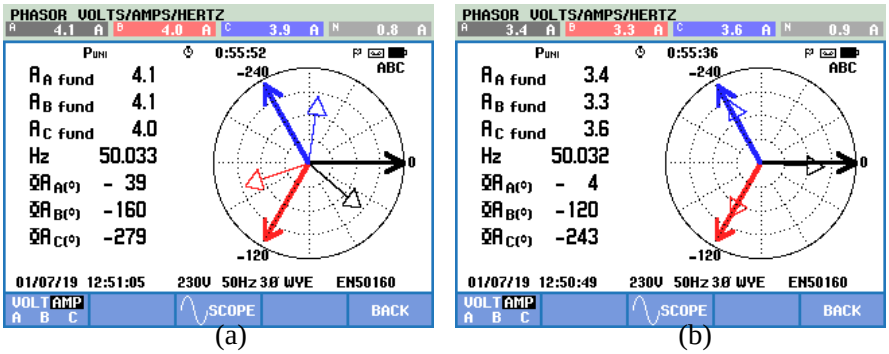


Fig. 6.18 Three-phase grid voltage and grid current phasors without SPV injecting power for load-2 (a) before compensation and (b) after compensation

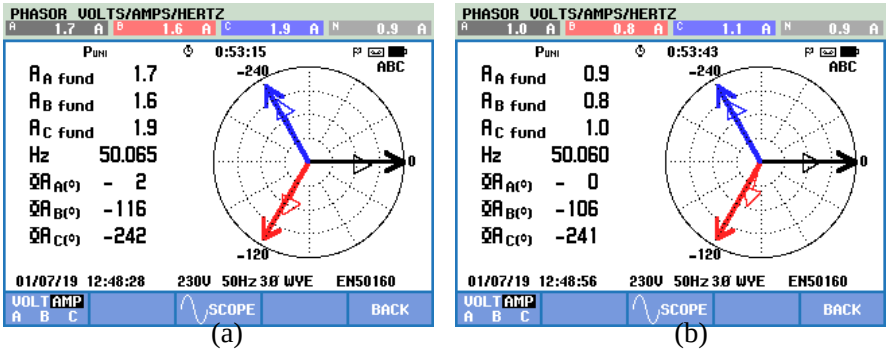


Fig. 6.19 Three-phase grid voltages and grid currents phasors with SPV power injection during DPM operation (a) without charging or discharging of battery and (b) with discharging battery during periods of t_3 shown in Fig. 6.16

- During t_1 period: DSTATCOM is not connected, therefore grid current is same as load current (non-sinusoidal). The real powers during this period are: P_L=235 W, P_g=−235 W, P_{vsc}=0 W.
- During t_2 period: DSTATCOM is connected, therefore grid current becomes sinusoidal because of reactive power compensation and harmonic mitigation. During this period the real powers are: P_L=235 W, P_g=−235 W, P_{vsc}=0 W.
- During t_3 period: dc-load is connected on dc-link side of VSC. As this load also draws power from grid by rectification action, such that the grid current increases. The real powers during this period are: P_L=235 W, P_g=−385 W, P_{vsc}=150 W.

During non-SPV hours, the three-phase grid voltage and grid current phasors without and with compensation, and during active rectification operations are shown in Fig. 6.21(a), Fig. 6.21(b) and Fig. 6.21(c), respectively. It is observed from Fig. 6.21(a) that, before compensation the grid currents lags the corresponding grid voltages by −31°, −32°(−152+120) and −29°(−269+240), respectively. After compensation, the grid currents are almost in-phase with the corresponding grid voltages as shown in Fig. 6.21(b). During rectification action, dc-load draws real power from grid, and the three-phase grid current magnitudes increase to 3.7 A, 3.7 A, 3.9 A as shown in Fig. 6.21(c)

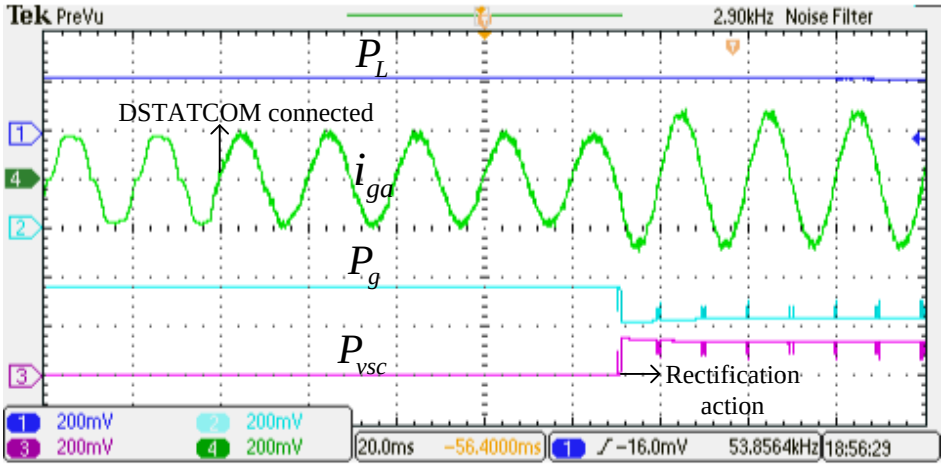
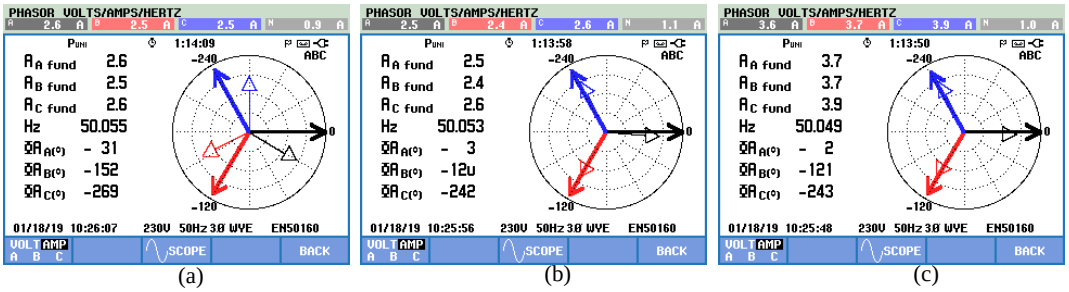


Fig. 6.20 Dynamics of real power in the system during non-SPV hours (P_L, P_g, P_{vsc} 200 W/div, i_{ga} 4 A/div)



(a) (b) (c)

Fig. 6.21 Three-phase grid voltages and grid currents phasors (a) without compensation (b) with compensation and (c) with compensation plus rectification (i.e., during periods of t_1, t_2 and t_3 shown in Fig. 6.20, respectively)

when compared to magnitudes of grid currents (2.5 A, 2.4 A, 2.6 A) as shown in Fig. 6.21(b).

The grid voltage (v_{sa}), grid current (i_{ga}), load current (i_{La}) and DSTATCOM current (i_{ia}) during the transition from compensation mode to active rectification mode (both compensation plus rectification) are shown in Fig. 6.22. When rectification action starts, the grid current increases and this also reflects on the DSTATCOM current as it is supplying power to dc-load through VSC.

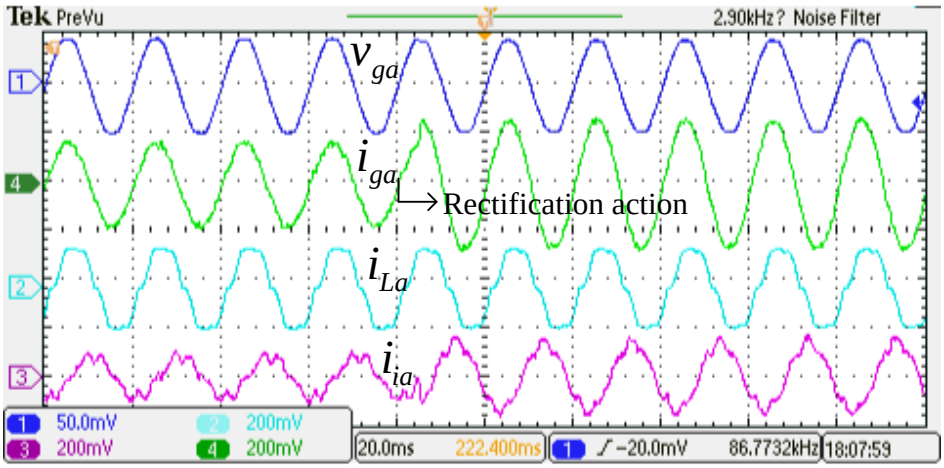


Fig. 6.22 Before and after rectification action during non-SPV hours (v_{ga} 50 V/div, i_{ga}, i_{La}, i_{ia} 4 A/div)

6.6 Summary

In this chapter, a single-stage SPV-DSTATCOM with co-ordinated control algorithm is proposed for MPP tracking and real power injection to grid along with charging or discharging operation of battery. It has multi-functional features, like real power injection, reactive power compensation and active rectification with VSC and DC-DC converter. The performance of the proposed method with energy management scheme is demonstrated by operating it in three different modes of operation (SPM, DPM and BPM). The advantages from the proposed method are: 1) During SPV hours, in addition to compensation of reactive power, real power injection to grid by operating SPV at MPP is possible along with charging or discharging of battery. 2) During non-SPV hours, rectification action is discussed for better utilization of VSC capacity. 3) Reliability of system increases with batter energy storage system. 4) The efficiency of the system is improved with single-stage conversion.

CHAPTER 7

CONCLUSIONS AND FUTURE SCOPE OF RESEARCH

7.1 Conclusions

The main objectives of the research work in this thesis is mitigation of current harmonics, reactive power compensation and neutral current compensation in three-phase four-wire distribution system. These are achieved by connecting DSTATCOM in shunt with the load. After comparing various DSTATCOM configurations, the three-phase four-wire split-capacitor shunt DSTATOCM configuration is selected for compensation in this research. The design and operation of DSTATCOM for compensation of reactive power and harmonics mitigation have been explained. The instantaneousness symmetrical component theory based hysteresis controller has been implemented for controlling DSTATCOM. An adaptive dc-link voltage method has been proposed for harmonics mitigation and reactive power compensation. The proposed method is compared with the existing method, and the main difference is as follows. In the existing method, the dc-link voltage is maintained constant for any load condition, which leads to high device voltage stress and switching losses. In the proposed method, mitigation of harmonics and reactive power compensation for different load conditions are achieved with adaptive dc-link voltage regulation method. To achieve this, an objective function for reference dc-link voltage in terms of filter current has been formulated. Extensive simulation results are presented to investigate the performance of 3P4W split-capacitor DSTATCOM in both steady-state and transient conditions under stiff and non-stiff source voltages. After compensation with DSTATCOM, the percentage THDs of source currents are reduced below 5% and the power factor on the source side is found to be unity not only in steady-state condition but also in transient condition.

An *LCL*-filter based DSTATCOM operating in current control mode and voltage control mode is implemented. In current control mode, the compensation of reactive power, current harmonic mitigation and neutral current minimization are achieved. The voltage

disturbances at PCC voltage are compensated by operating DSTATCOM in voltage control mode. The specific *LCL*-filter design approach presented in this work requires low value of interfacing inductance when compared to inductance in *L*-filter DSTATCOM, and therefore the cost and size of the DSTATCOM are reduced. The effectiveness of the proposed method is validated based on simulation and experimental studies. The application of DSTATCOM has been extended to grid connected SPV systems for simultaneous real power injection to grid and power quality improvement. To accomplish this, a single-stage SPV-DSTATCOM in 3P4W distribution system with battery storage system has been proposed. The complete arrangements considered in this topology comprise a 3P4W DSTATCOM and DC-DC bi-directional converter. This single-stage approach significantly improves the performance of the overall system leading to better utilization of VSC rating during PV and non-PV hours. The significant contribution of this work is outlined below:

- The switching losses and voltage stress across switching devices of VSC are reduced with the proposed adaptive dc-link voltage regulation method.

- The required interfacing inductance value is reduced in *LCL*-filter based DSTATCOM, so that the filter size and cost are reduced when compared to conventional *L*-filter based DSTATCOM. Further, the operation of *LCL*-DSTATCOM in Current Control Mode (CCM) and Voltage Control Mode (VCM) are achieved with the proposed algorithm.

- The required kVA rating of the VSC is reduced by implementing the hybrid DSTATCOM. Further, an adaptive dc-link voltage regulation of hybrid DSTATCOM improves the performance of compensator.

- In addition to power quality improvement by DSTATCOM, real power injection to grid from solar PV supported by battery storage is proposed. The real power injection by operating solar PV at MPP and battery charging or discharging are achieved simultaneously with the proposed co-ordinated control algorithm. An efficient utilization of rating of VSC is achieved with the proposed energy management scheme.

7.2 Future Scope of Research

- Implementation of multi-level inverter based DSTATCOM topologies for high power application is a potential area of research.
- Design of the controller of the DSTATCOM using advanced control techniques such as model predictive control is an active area of research.
- Implementation of power management scheme between dc-bus and ac-bus systems with co-ordinated control algorithm in the distribution system.
- Another interesting topic could be the research on hybrid energy storage system based energy management scheme for SPV-DSTATCOM. This research could include the selection of inverter topology, MPPT tracking techniques, compensation characteristics and cost of the system, and would indeed contribute significantly to the study in this area.

REFERENCES

[1] R. Subramaniam, G. Wacker, and R. Billinton, "Understanding commercial losses resulting from electric service interruptions," *IEEE Transactions on Industry Applications*, vol. 29, no. 1, pp. 233–237, Jan.-Feb. 1993.

[2] M. Sullivan, T. Vardell, and M. Johnson, "Power interruption costs to industrial and commercial consumers of electricity," *IEEE Transactions on Industry Applications*, vol. 33, no. 6, pp. 1448–1458, Nov.–Dec. 1997.

[3] R. Lamedica, G. Esposito, E. Tironi, D. Zaninelli, and A. Prudenzi, "A survey on power quality cost in industrial customers," in *IEEE Power Engineering Society Winter Meeting*, 2001.

[4] T. J. E. Miller, *Reactive power control in electric systems*. John Wiley & Sons, 1982.

[5] R. C. Dugan, M. F. McGranaghan, H. W. Beaty, and S. Santoso, *Electrical power systems quality*. McGraw-Hill, New York, 1996.

[6] J. Arrillaga and N. R. Watson, *Power system harmonics*. John Wiley & Sons, 2004.

[7] T. M. Gruzs, "A survey of neutral currents in three-phase computer power systems," *IEEE Transactions on Industry Applications*, vol. 26, no. 4, pp. 719–725, 1990.

[8] A. C. Liew, "Excessive neutral currents in three-phase fluorescent lighting circuits," *IEEE Transactions on Industry Applications*, vol. 25, no. 4, pp. 776–782, 1989.

[9] "IEEE Recommended Practice and Requirements for Harmonic Control in Electric Power Systems," *IEEE Std 519-2014 (Revision of IEEE Std 519-1992)*, pp. 1–29, June 2014.

[10] K. Sakthivel, S. K. Das, and K. Kini, "Importance of quality AC power distribution and understanding of EMC standards IEC 61000-3-2, IEC 61000-3-3 and IEC 61000-3-11," in *8th International conference on electromagnetic interference and compatibility*. IEEE, 2003, pp. 423–430.

[11] D. A. Gonzalez and J. C. McCall, "Design of Filters to Reduce Harmonic Distortion in Industrial Power Systems," *IEEE Transactions on Industry Applications*, vol. IA-23, no. 3, pp. 504–511, May 1987.

[12] J. Das, "Passive filters-potentialities and limitations," *IEEE Transactions on Industry Applications*, vol. 40, no. 1, pp. 232–241, 2004.

[13] H. Fujita and H. Akagi, "A practical approach to harmonic compensation in power systems-series connection of passive and active filters," *IEEE Transactions on industry applications*, vol. 27, no. 6, pp. 1020–1025, 1991.

[14] H. Akagi, "Active harmonic filters," *Proceedings of the IEEE*, vol. 93, no. 12, pp. 2128–2141, 2005.

[15] H. Akagi, "New trends in active filters for power conditioning," *Industry Applications*, vol. 32, no. 6, pp. 1312–1322, 1996.

[16] W. M. Grady, M. J. Samotyj, and A. H. Noyola, "Survey of active power line conditioning methodologies," *IEEE Transactions on Power Delivery*, vol. 5, no. 3, pp. 1536–1542, 1990.

[17] F. Peng, M. Kohata, and H. Akagi, "Compensation characteristics of shunt active and series active filters," in *Proc. Chinese-Japanese Power Electron Conf., Beijing, People's Republlic of China*, 1990, pp. 381–387.

[18] H. Akagi, S. Srianthumrong, and Y. Tamai, "Comparisons in circuit configuration and filtering performance between hybrid and pure shunt active filters," in *38th IAS Annual Meeting on Conference Record of the Industry Applications Conference, 2003.*, vol. 2. IEEE, 2003, pp. 1195–1202.

[19] S. Bhattacharya, , and D. M. Divan, "Hybrid solutions for improving passive filter performance in high power applications," *IEEE Transactions on Industry Applications*, vol. 33, no. 3, pp. 732–747, May 1997.

[20] V. S. R. V. Oruganti, A. S. Bubshait, V. S. S. S. S. Dhanikonda, and M. G. Simoes, "Real-time control of hybrid active power filter using conservative power theory in industrial power system," *IET Power Electronics*, vol. 10, no. 2, pp. 196–207, 2017.

[21] N. G. Hingorani, "Introducing custom power," *IEEE spectrum*, 1995.

[22] V. Khadkikar and A. Chandra, "An independent control approach for three-phase four-wire shunt active filter based on three H-bridge topology under unbalanced load conditions," in *2008 IEEE Power Electronics Specialists Conference*. IEEE, 2008, pp. 4643–4649.

[23] B. Singh, S. R. Arya, C. Jain, and S. Goel, "Implementation of four-leg distribution static compensator," *IET Generation, Transmission & Distribution*, vol. 8, no. 6, pp. 1127–1139, 2014.

[24] M. K. Mishra, A. Ghosh, A. Joshi, and H. M. Suryawanshi, "A novel method of load compensation under unbalanced and distorted voltages," *IEEE transactions on power delivery*, vol. 22, no. 1, pp. 288–295, 2007.

[25] S. Srikanthan and M. K. Mishra, "DC capacitor voltage equalization in neutral clamped inverters for DSTATCOM application," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 8, pp. 2768–2775, 2010.

[26] S. P. Gawande and M. R. Ramteke, "State feedback-based capacitor voltage equalisation scheme in distribution static compensator for load compensation," *IET Generation, Transmission Distribution*, vol. 9, no. 15, pp. 2188–2197, 2015.

[27] B. Singh, P. Jayaprakash, and D. Kothari, "A T-connected transformer and three-leg VSC based DSTATCOM for power quality improvement," *IEEE Transactions on Power Electronics*, vol. 23, no. 6, pp. 2710–2718, 2008.

[28] M. K. Mishra and K. Karthikeyan, "An investigation on design and switching dynamics of a voltage source inverter to compensate unbalanced and nonlinear loads," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 8, pp. 2802–2810, 2009.

[29] A. Ghosh and G. Ledwich, "Structures and control of a dynamic voltage regulator (DVR)," in *2001 IEEE Power Engineering Society Winter Meeting. Conference Proceedings (Cat. No. 01CH37194)*, vol. 3. IEEE, 2001, pp. 1027–1032.

[30] H. Akagi, Y. Kanazawa, and A. Nabae, "Instantaneous reactive power compensators comprising switching devices without energy storage components," *IEEE Transactions on Industry Applications*, vol. IA-20, no. 3, pp. 625–630, May 1984.

[31] M. Basu, S. Das, and G. K. Dubey, "Investigation on the performance of UPQC-Q for voltage sag mitigation and power quality improvement at a critical load point," *IET generation, transmission & distribution*, vol. 2, no. 3, pp. 414–423, 2008.

[32] J. Dixon, L. Moran, J. Rodriguez, and R. Domke, "Reactive power compensation technologies: State-of-the-art review," *Proceedings of the IEEE*, vol. 93, no. 12, pp. 2144–2164, 2005.

[33] V. George and M. K. Mishra, "Design and analysis of user-defined constant switching frequency current-control-based four-leg dstatcom," *IEEE Transactions on Power Electronics*, vol. 24, no. 9, pp. 2148–2158, Sep. 2009.

[34] B. Singh, P. Rastgoufard, B. Singh, A. Chandra, and K. Al-Haddad, "Design, simulation and implementation of three-pole/four-pole topologies for active filters," *IEE Proceedings-Electric Power Applications*, vol. 151, no. 4, pp. 467–476, 2004.

[35] B. Singh, P. Jayaprakash, T. Somayajulu, and D. Kothari, "Reduced rating VSC with a zig-zag transformer for current compensation in a three-phase four-wire distribution system," *Power Delivery, IEEE Transactions on*, vol. 24, no. 1, pp. 249–259, 2009.

[36] H. Fujita, S. Tominaga, and H. Akagi, "Analysis and design of a dc voltage-controlled static var compensator using quad-series voltage-source inverters," *Industry Applications, IEEE Transactions on*, vol. 32, no. 4, pp. 970–978, 1996.

[37] D. M. Vilathgamuwa, H. M. Wijekoon, and S. S. Choi, "Interline dynamic voltage restorer: a novel and economical approach for multi-line power quality compensation," in *38th IAS Annual Meeting on Conference Record of the Industry Applications Conference, 2003.*, vol. 2, Oct 2003, pp. 833–840 vol.2.

[38] Mitsubishi Intelligent Power Module Data Manual, "PM50RVA120," *Mitsubishi Electric and Electronic USA, Cypress, CA*, 2003.

[39] L. Asiminoael, F. Blaabjerg, and S. Hansen, "Detection is key - harmonic detection methods for active power filter applications," *IEEE Industry Applications Magazine*, vol. 13, no. 4, pp. 22-33, July 2007.

[40] O. M. Solomon, "The use of DFT windows in signal-to-noise ratio and harmonic distortion computations," *IEEE Transactions on Instrumentation and Measurement*, vol. 43, no. 2, pp. 194–199, April 1994.

[41] A. A. Girgis, W. B. Chang, and E. B. Makram, "A digital recursive measurement scheme for online tracking of power system harmonics," *IEEE Transactions on Power Delivery*, vol. 6, no. 3, pp. 1153–1160, July 1991.

[42] S. M. Williams and R. G. Hoft, "Adaptive frequency domain control of PWM switched power line conditioner," *IEEE Transactions on Power Electronics*, vol. 6, no. 4, pp. 665–670, Oct 1991.

[43] H. Akagi, E. H. Watanabe, and M. Aredes, *Instantaneous power theory and applications to power conditioning*. John Wiley & Sons, 2017, vol. 62.

[44] B. Singh, A. Chandra, and K. Al-Haddad, *Power quality: problems and mitigation techniques*. John Wiley & Sons, 2014.

[45] A. Ghosh and A. Joshi, "A new approach to load balancing and power factor correction in power distribution system," *IEEE Transactions on Power Delivery*, vol. 15, no. 1, pp. 417–422, Jan 2000.

[46] G. Bhuvaneswari and M. G. Nair, "Design, Simulation, and Analog Circuit Implementation of a Three-Phase Shunt Active Filter Using the I cos Φ Algorithm," *IEEE Transactions on Power Delivery*, vol. 23, no. 2, pp. 1222–1235, April 2008.

[47] G. van Schoor, J. D. van Wyk, and I. S. Shaw, "Training and optimization of an artificial neural network controlling a hybrid power filter," *IEEE Transactions on Industrial Electronics*, vol. 50, no. 3, pp. 546–553, June 2003.

[48] U. K. Rao, M. K. Mishra, and A. Ghosh, "Control strategies for load compensation using instantaneous symmetrical component theory under different supply voltages," *IEEE Transactions on Power Delivery*, vol. 23, no. 4, pp. 2310–2317, Oct 2008.

[49] F. Harirchi and M. G. Simes, "Enhanced instantaneous power theory decomposition for power quality smart converter applications," *IEEE Transactions on Power Electronics*, vol. 33, no. 11, pp. 9344–9359, Nov 2018.

[50] S. Bhattacharya, T. M. Frank, D. M. Divan, and B. Banerjee, "Active filter system implementation," *IEEE Industry Applications Magazine*, vol. 4, no. 5, pp. 47–63, Sep. 1998.

[51] M. Depenbrock, "The FBD-method, a generally applicable tool for analyzing power relations," *IEEE Transactions on Power Systems*, vol. 8, no. 2, pp. 381–387, 1993.

[52] W. T. A.Wintrich, U. Nicolai and T. Reimann, *Application manual power semiconductors*, 2015.

[53] U. Nicolai and A. Wintrich, "Determining switching losses of SEMIKRON IGBT Modules," *SEMIKRON Application Note, AN*, vol. 1403, 2014.

[54] M. V. Manoj Kumar and M. K. Mishra, "Three-leg inverter-based distribution static compensator topology for compensating unbalanced and non-linear loads," *IET Power Electronics*, vol. 8, no. 11, pp. 2076–2084, 2015.

[55] C. Lam, W. Choi, M. Wong, and Y. Han, "Adaptive DC-Link Voltage-Controlled Hybrid Active Power Filters for Reactive Power Compensation," *IEEE Transactions on Power Electronics*, vol. 27, no. 4, pp. 1758–1772, April 2012.

[56] C. S. Lam, M. C. Wong, W. H. Choi, X. X. Cui, H. M. Mei, and J. Z. Liu, "Design and performance of an adaptive low-DC-voltage-controlled *LC*-hybrid active power filter with a neutral inductor in three-phase four-wire power systems," *IEEE Transactions on industrial electronics*, vol. 61, no. 6, pp. 2635–2647, 2014.

[57] C. S. Lam, L. Wang, S. I. Ho, and M. C. Wong, "Adaptive thyristor-controlled *LC*-hybrid active power filter for reactive power and current harmonics compensation with switching loss reduction," *IEEE Transactions on Power Electronics*, vol. 32, no. 10, pp. 7577–7590, 2017.

[58] T. Wei, C. Mao, J. Lu, D. Wang, Q. Wang, and W. Wu, "Low cost hybrid reactive power compensator using coordination control strategies," *IET Generation, Transmission Distribution*, vol. 10, no. 8, pp. 1805–1814, 2016.

[59] S. B. Karanki, N. Geddada, M. K. Mishra, and B. K. Kumar, "A DSTATCOM Topology With Reduced DC-Link Voltage Rating for Load Compensation With Nonstiff Source," *IEEE Transactions on Power Electronics*, vol. 27, no. 3, pp. 1201–1211, March 2012.

[60] M. Liserre, F. Blaabjerg, and S. Hansen, "Design and control of an *LCL*-filter-based three-phase active rectifier," *IEEE Transactions on Industry Applications*, vol. 41, no. 5, pp. 1281–1291, Sep. 2005.

[61] A. Reznik, M. G. Simoes, A. Al-Durra, and S. M. Muyeen, "*LCL* Filter Design and Performance Analysis for Grid-Interconnected Systems," *IEEE Transactions on Industry Applications*, vol. 50, no. 2, pp. 1225–1232, March 2014.

[62] R. Pena-Alzola, M. Liserre, F. Blaabjerg, M. Ordonez, and Y. Yang, "*LCL*-filter design for robust active damping in grid-connected converters," *IEEE Transactions on Industrial Informatics*, vol. 10, no. 4, pp. 2192–2203, 2014.

[63] L. Zhou, Y. Chen, A. Luo, J. M. Guerrero, X. Zhou, Z. Chen, and W. Wu, "Robust two degrees-of-freedom single-current control strategy for *LCL*-type grid-connected DG system under grid-frequency fluctuation and grid-impedance variation," *IET Power Electronics*, vol. 9, no. 14, pp. 2682–2691, 2016.

[64] Y. Han, Z. Li, P. Yang, C. Wang, L. Xu, and J. M. Guerrero, "Analysis and Design of Improved Weighted Average Current Control Strategy for *LCL*-Type Grid-Connected Inverters," *IEEE Transactions on Energy Conversion*, vol. 32, no. 3, pp. 941–952, Sep. 2017.

[65] W. Wu, Y. Liu, Y. He, H. S. Chung, M. Liserre, and F. Blaabjerg, "Damping Methods for Resonances Caused by *LCL*-Filter-Based Current-Controlled Grid-Tied Power Inverters: An Overview," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 9, pp. 7402–7413, Sep. 2017.

[66] Y. Tang, P. C. Loh, P. Wang, F. H. Choo, F. Gao, and F. Blaabjerg, "Generalized Design of High Performance Shunt Active Power Filter With Output *LCL* Filter," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 3, pp. 1443–1452, March 2012.

[67] Q. Liu, L. Peng, Y. Kang, S. Tang, D. Wu, and Y. Qi, "A Novel Design and Optimization Method of an *LCL* Filter for a Shunt Active Power Filter," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 8, pp. 4000–4010, Aug 2014.

[68] N. Geddada, M. K. Mishra, and M. M. Kumar, "*LCL* filter with passive damping for DSTATCOM using PI and HC regulators in dq0 current controller for load compensation," *Sustainable Energy, Grids and Networks*, 2015.

[69] M. Popescu, A. Bitoleanu, and A. Preda, "A New Design Method of an *LCL* Filter Applied in Active DC-Traction Substations," *IEEE Transactions on Industry Applications*, vol. 54, no. 4, pp. 3497–3507, July 2018.

[70] X. Wang, F. Blaabjerg, and P. C. Loh, "Grid-Current-Feedback Active Damping for *LCL* Resonance in Grid-Connected Voltage-Source Converters," *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 213–223, Jan 2016.

[71] W. Yao, Y. Yang, X. Zhang, F. Blaabjerg, and P. C. Loh, "Design and Analysis of Robust Active Damping for *LCL* Filters Using Digital Notch Filters," *IEEE Transactions on Power Electronics*, vol. 32, no. 3, pp. 2360–2375, March 2017.

[72] J. C. Giacomini, L. Michels, H. Pinheiro, and C. Rech, "Design methodology of a passive damped modified *LCL* filter for leakage current reduction in grid-connected transformerless three-phase PV inverters," *IET Renewable Power Generation*, vol. 11, no. 14, pp. 1769–1777, 2017.

[73] O. Vodyakho and C. C. Mi, "Three-Level Inverter-Based Shunt Active Power Filter in Three-Phase Three-Wire and Four-Wire Systems," *IEEE Transactions on Power Electronics*, vol. 24, no. 5, pp. 1350–1363, May 2009.

[74] Z. Qiu, J. Kong, and G. Chen, "A novel control approach for *LCL*-based shunt active power filter with high dynamic and steady-state performance," in *IEEE Power Electronics Specialists Conference*, 2008.

[75] S. R. Arya, B. Singh, R. Niwas, A. Chandra, and K. Al-Haddad, "Power Quality Enhancement Using DSTATCOM in Distributed Power Generation System," *IEEE Transactions on Industry Applications*, vol. 52, no. 6, pp. 5203–5212, Nov 2016.

[76] M. Mangaraj and A. K. Panda, "Performance analysis of DSTATCOM employing various control algorithms," *IET Generation, Transmission Distribution*, vol. 11, no. 10, pp. 2643–2653, 2017.

[77] M. T. Ahmad, N. Kumar, and B. Singh, "Generalised neural network-based control algorithm for DSTATCOM in distribution systems," *IET Power Electronics*, vol. 10, no. 12, pp. 1529–1538, 2017.

[78] P. Chittora, A. Singh, and M. Singh, "Gauss 8211;Newton-based fast and simple recursive algorithm for compensation using shunt active power filter," *IET Generation, Transmission Distribution*, vol. 11, no. 6, pp. 1521–1530, 2017.

[79] R. Gupta, A. Ghosh, and A. Joshi, "Performance Comparison of VSC-Based Shunt and Series Compensators Used for Load Voltage Control in Distribution Systems," *IEEE Transactions on Power Delivery*, vol. 26, no. 1, pp. 268–278, Jan 2011.

[80] C. Kumar and M. K. Mishra, "A Voltage-Controlled DSTATCOM for Power-Quality Improvement," *IEEE Transactions on Power Delivery*, vol. 29, no. 3, pp. 1499–1507, June 2014.

[81] C. Kumar and M. K. Mishra, "Operation and Control of an Improved Performance Interactive DSTATCOM," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 10, pp. 6024–6034, Oct 2015.

[82] M. L. Gasperi, D. L. Jensen, and D. T. Rollay, "Method for AC Powerline Impedance Measurement," *IEEE Transactions on Industry Applications*, vol. 44, no. 4, pp. 1034–1037, July 2008.

[83] N. Hoffmann and F. W. Fuchs, "Minimal Invasive Equivalent Grid Impedance Estimation in Inductive x2013;Resistive Power Networks Using Extended Kalman Filter," *IEEE Transactions on Power Electronics*, vol. 29, no. 2, pp. 631–641, Feb 2014.

[84] A. A. Valdez-Fernandez, G. Escobar, P. R. Martinez-Rodriguez, J. M. Sosa, D. U. Campos-Delgado, and M. J. Lopez-Sanchez, "Modelling and control of a hybrid power filter to compensate harmonic distortion under unbalanced operation," *IET Power Electronics*, vol. 10, no. 7, pp. 782–791, 2017.

[85] L. Wang, C. S. Lam, and M. C. Wong, "Selective Compensation of Distortion, Unbalanced and Reactive Power of a Thyristor-Controlled *LC*-Coupling Hybrid Active Power Filter (TCLC-HAPF)," *IEEE Transactions on Power Electronics*, vol. 32, no. 12, pp. 9065–9077, Dec 2017.

[86] L. Wang, C. S. Lam, and M. C. Wong, "Modeling and parameter design of thyristor-controlled *LC*-coupled hybrid active power filter (TCLC-HAPF) for unbalanced compensation," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 3, pp. 1827–1840, 2017.

[87] L. Wang, C. S. Lam, and M. C. Wong, "Hybrid Structure of Static Var Compensator and Hybrid Active Power Filter (SVC//HAPF) for Medium-Voltage Heavy Loads Compensation," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 6, pp. 4432–4442, 2018.

[88] L. Wang, C. S. Lam, and M. C. Wong, "Minimizing Inverter Capacity Design and Comparative Performance Evaluation of SVC-Coupling Hybrid Active Power Filters," *IEEE Transactions on Power Electronics*, vol. 34, no. 2, pp. 1227–1242, 2019.

[89] E. Durna, "Adaptive fuzzy hysteresis band current control for reducing switching losses of hybrid active power filter," *IET Power Electronics*, vol. 11, no. 5, pp. 937–944, 2018.

[90] A. Luo, X. Xu, L. Fang, H. Fang, J. Wu, and C. Wu, "Feedback-feedforward PI-type iterative learning control strategy for hybrid active power filter with injection

circuit," *IEEE Transactions on industrial electronics*, vol. 57, no. 11, pp. 3767–3779, 2010.

[91] A. Luo, C. Tang, Z. Shuai, J. Tang, X. Y. Xu, and D. Chen, "Fuzzy-PI-based direct-output-voltage control strategy for the STATCOM used in utility distribution systems," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 7, pp. 2401–2411, 2009.

[92] I. Sefa, N. Altin, S. Ozdemir, and O. Kaplan, "Fuzzy PI controlled inverter for grid interactive renewable energy systems," *IET Renewable Power Generation*, vol. 9, no. 7, pp. 729–738, 2015.

[93] V. Spitsa, A. Alexandrovitz, and E. Zeheb, "Design of a robust state feedback controller for a STATCOM using a zero set concept," *IEEE Transactions on Power delivery*, vol. 25, no. 1, pp. 456–467, 2010.

[94] K. Wang and M. L. Crow, "Power system voltage regulation via STATCOM internal nonlinear control," *IEEE Transactions on power Systems*, vol. 26, no. 3, pp. 1252–1262, 2011.

[95] Y. Xu and F. Li, "Adaptive PI control of STATCOM for voltage regulation," *IEEE transactions on power delivery*, vol. 29, no. 3, pp. 1002–1011, 2014.

[96] M. T. Ahmad, N. Kumar, and B. Singh, "AVSF-based control algorithm of DSTATCOM for distribution system," *IET Generation, Transmission Distribution*, vol. 11, no. 13, pp. 3389–3396, 2017.

[97] M. Badoni, A. Singh, and B. Singh, "Adaptive recursive inverse-based control algorithm for shunt active power filter," *IET Power Electronics*, vol. 9, no. 5, pp. 1053–1064, 2016.

[98] S. Chakraborty and M. G. Simoes, "PV-Microgrid Operational Cost Minimization by Neural Forecasting and Heuristic Optimization," in *2008 IEEE Industry Applications Society Annual Meeting*, Oct 2008, pp. 1–8.

[99] J. Parikh and K. Parikh, "Growing pains: Meeting india's energy needs in the face of limited fossil fuels," *IEEE Power and Energy Magazine*, vol. 10, no. 3, pp. 59–66, 2012.

[100] R. Kadri, J. P. Gaubert, and G. Champenois, "An improved maximum power point tracking for photovoltaic grid-connected inverter based on voltage-oriented control," *IEEE transactions on industrial electronics*, vol. 58, no. 1, pp. 66–75, 2011.

[101] B. Singh, M. Kandpal, and I. Hussain, "Control of grid tied smart PV-DSTATCOM system using an adaptive technique," *IEEE Transactions on Smart Grid*, vol. 9, no. 5, pp. 3986–3993, 2018.

[102] N. Kumar, B. Singh, and B. K. Panigrahi, "LLMLF based Control Approach and LPO MPPT Technique for Improving Performance of a Multifunctional Three-Phase Two-Stage Grid Integrated PV System," *IEEE Transactions on Sustainable Energy*, 2019.

[103] N. R. Tummuru, M. K. Mishra, and S. Srinivas, "Multifunctional VSC controlled microgrid using instantaneous symmetrical components theory," *IEEE Transactions on Sustainable Energy*, vol. 5, no. 1, pp. 313–322, 2014.

[104] L. B. G. Campanhol, S. A. O. da Silva, A. A. de Oliveira, and V. D. Bacon, "Single-stage three-phase grid-tied PV system with universal filtering capability applied to DG systems and AC microgrids," *IEEE Transactions on Power Electronics*, vol. 32, no. 12, pp. 9131–9142, 2017.

[105] A. Yazdani, A. R. Di Fazio, H. Ghoddami, M. Russo, M. Kazerani, J. Jatskevich, K. Strunz, S. Leva, and J. A. Martinez, "Modeling guidelines and a benchmark for power system simulation studies of three-phase single-stage photovoltaic systems," *IEEE Transactions on Power Delivery*, vol. 26, no. 2, pp. 1247–1264, April 2011.

[106] P. Denholm and R. M. Margolis, "Evaluating the limits of solar photovoltaics (PV) in electric power systems utilizing energy storage and other enabling technologies," *Energy Policy*, vol. 35, no. 9, pp. 4424 – 4433, 2007.

[107] Y. Riffonneau, S. Bacha, F. Barruel, and S. Ploix, "Optimal Power Flow Management for Grid Connected PV Systems With Batteries," *IEEE Transactions on Sustainable Energy*, vol. 2, no. 3, pp. 309–320, July 2011.

[108] U. Manandhar, A. Ukil, H. B. Gooi, N. R. Tummuru, S. K. Kollimalla, B. Wang, and K. Chaudhari, "Energy management and control for grid connected hybrid energy storage system under different operating modes," *IEEE Transactions on Smart Grid*, vol. 10, no. 2, pp. 1626–1636, March 2019.

[109] N. Korada and M. K. Mishra, "Grid adaptive power management strategy for an integrated microgrid with hybrid energy storage," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 4, pp. 2884–2892, April 2017.

[110] S. Kotra and M. K. Mishra, "A Supervisory Power Management System for a Hybrid Microgrid With HESS," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 5, pp. 3640–3649, May 2017.

[111] H. Kim, B. Parkhideh, T. D. Bongers, and H. Gao, "Reconfigurable Solar Converter: A Single-Stage Power Conversion PV-Battery System," *IEEE Transactions on Power Electronics*, vol. 28, no. 8, pp. 3788–3797, Aug 2013.

[112] Z. Zou, J. Xu, C. Mi, B. Cao, and Z. Chen, "Evaluation of model based state of charge estimation methods for lithium-ion batteries," *Energies*, vol. 7, no. 8, pp. 5065–5082, 2014.

[113] P. Shah and B. Singh, "Kalman Filtering Technique for Rooftop-PV System under Abnormal Grid Conditions," *IEEE Transactions on Sustainable Energy*, 2018 (DOI:10.1109/TSTE.2018.2890600).

[114] B. Singh, C. Jain, and S. Goel, "ILST control algorithm of single-stage dual purpose grid connected solar PV system," *IEEE Transactions on Power Electronics*, vol. 29, no. 10, pp. 5347–5357, 2014.

LIST OF PAPERS BASED ON THESIS

Journals

1. **Hareesh Myneni**, G Siva Kumar and D Sreenivasarao, "Dynamic dc voltage regulation of split-capacitor DSTATCOM for power quality improvement," ***IET Generation, Transmission & Distribution***, vol. 11, no. 17, pp. 4373-4383, Aug. 2017.

2. **Hareesh Myneni** and G Siva Kumar, "Simple algorithm for current and voltage control of *LCL*-DSTATCOM for power quality improvement," ***IET Generation, Transmission & Distribution***, vol. 13, no. 3, pp. 423-434, Dec-2018.

3. **Hareesh Myneni**, G Siva Kumar and D Sreenivasarao, "Power Quality Enhancement by Hybrid DSTATCOM with Improved Performance in Distribution System," ***International Transactions on Electrical Energy Systems***, Wiley publications, e12153, 2019.

4. **Hareesh Myneni** and G Siva Kumar, "Energy Management and Control of Single-Stage Grid Connected Solar PV and BES System," ***IEEE Transactions on Sustainable Energy***, 2019. DOI: 10.1109/TSTE.2019.2938864

5. K. Kiran Prasad, **Hareesh Myneni** and G. Siva Kumar, "Power Quality Improvement and PV Power Injection by DSTATCOM with Variable DC-link Voltage Control from RSC-MLC," ***IEEE Transactions on Sustainable Energy***, vol. 10, no. 2, pp. 876-885, April 2019.

6. **Hareesh Myneni**, G Siva Kumar and D Sreenivasarao, "Cost effective single-phase DSTATCOM for low power applications," ***Electric Power Components and Systems, Taylor & Francis***, 47, no. 9-10, pp. 785-797, 2019.

Conferences

1. **Hareesh Myneni**, G. Siva Kumar and D. Sreenivasarao, "Power quality improvement by Shunt Active Filter for low cost applications," *International Conference on Computation of Power, Energy, Information and Communication (ICCPEIC)*, Chennai, pp. 0153-0158, 2015.

2. **Hareesh Myneni**, G. Siva Kumar and D. Sreenivasarao, "Power quality enhancement by current controlled Voltage Source Inverter based DSTATCOM for load variations," *IEEE IAS Joint Industrial and Commercial Power Systems / Petroleum and Chemical Industry Conference (ICPSPCIC)*, Hyderabad, pp. 182-188, 2015.

3. **Hareesh Myneni**, Amarnath C, G. Siva Kumar and D. Sreenivasarao, “Experimental implementation of 100 W Photo-voltaic Panel with DC-DC Boost Converter for Maximum Power Point Tracking,” ***The Journal of CPRI***, vol. 12, No. 4, Dec 2016.

4. **Hareesh Myneni**, G. Siva Kumar and D. Sreenivasarao, “Adaptive dc-link voltage regulation for DSTATCOM under load variations," *IEEE Region 10 Conference (TENCON)*, Singapore, pp. 2909-2913, 2016.

5. **Hareesh Myneni** and G. Siva Kumar, “A New Interactive Control Algorithm of DSTATCOM for Power Quality Improvement," *IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*, Chennai, India, pp. 1-5, 2018.

6. Kavita Kiran Prasad, **Hareesh Myneni** and G. Siva Kumar, “Reduced Switch Count Multi-level Converter Controlled DC-link Voltage of DSTATCOM for Power Quality Improvement," *2018 Biennial International Conference on Power and Energy Systems:Towards Sustainable Energy (PESTSE)*, Bangalore, India, 2018. (accepted for publication)

CURRICULUM VITAE

1. Name : Hareesh Myneni

2. Date of Birth : 04 Aug 1987

3. Educational Qualifications :

Bachelor of Engineering (B. Tech.) 2009

Institution : Vignan's Engineering College,
Guntur, Andhra Pradesh

University : Jawaharlal Nehru Technological University (JNTU),
Kakinada

Specialization : Electrical and Electronics Engineering

Master of Technology (M. Tech.) 2012

Institution : National Institute of Technology, Rourkela
Rourkela, Odisha

Specialization : Power Control and Drives

Doctor of Philosophy (Ph.D.) 2019

Institution : National Institute of Technology Warangal

Specialization : Electrical Engineering

Registration : 17 July 2014

DOCTORAL COMMITTEE

Chairman	:	Dr. S Srinivasa rao Professor and Head, Department of Electrical Engineering National Institute of Technology Warangal
Guide	:	Dr. G. Siva Kumar Assistant Professor, Department of Electrical Engineering National Institute of Technology Warangal
Members	:	Dr. M. Sydulu Professor, Department of Electrical Engineering National Institute of Technology Warangal
		Dr. D Sreenivasa Rao Assistant Professor, Department of Electrical Engineering National Institute of Technology Warangal
		Dr. D. Dinakar Professor, Department of Physics National Institute of Technology Warangal