SIGNAL INTEGRITY ANALYSIS OF ON-CHIP INTERCONNECTS USING MRTD

Submitted in partial fulfillment of the requirements
for the award of the degree of
DOCTOR OF PHILOSOPHY

by

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2019

Dedicated to

My family & Teachers

Approval Sheet

This thesis entitled "**Signal Integrity Analysis of On-Chip Interconnects using MRTD**" by **Rebelli Shashank** is approved for the degree of Doctor of Philosophy.

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DECLARATION

This is to certify that the work presented in the thesis entitled "**Signal Integrity Analysis of On-Chip Interconnects Using MRTD**" is a bonafide work done by me under the supervision of **Prof. N.Bheema Rao**, Professor, Department of Electronics and Communication Engineering, National Institute of Technology Warangal, India and was not submitted elsewhere for the award of any degree.

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CERTIFICATE

This is to certify that the thesis entitled "**Signal Integrity Analysis of On-Chip Interconnects Using MRTD**", which is being submitted by **Mr. Rebelli Shashank(Roll No: 715045)**, in partial fulfillment for the award of the degree of Doctor of Philosophy to the Department of Electronics and Communication Engineering of National Institute of Technology Warangal, is a record of bonafide research work carried out by him under my supervision and has not been submitted elsewhere for any degree.

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ACKNOWLEDGEMENTS

Firstly, I would like to express my sincere gratitude to Prof. N. Bheema Rao (Supervisor and Head of the department, ECE) for the continuous support of my Ph.D study and related research, for his patience, motivation, and guidance. My sincere thanks to him for providing me an opportunity to join the institute as a Ph.D. research scholar and giving me access to the research facilities. Without his precious support it would not have been possible to conduct this research.

Besides my supervisor, I would like to take this opportunity to thank my Doctoral Scrutiny Committee members, Prof. L. Anjaneyulu, Professor (Department of Electronics and Communication Engineering, NIT Warangal), Prof. J. V. Ramana Murthy, Professor (Department of Mathematics, NIT Warangal) and Dr. T.V.K. Hanumantha Rao, Associate Professor (Department of Electronics and Communication Engineering, NIT Warangal) for their continuous support, suggestions and advices during my research period whenever required.

I thank Dr. Atul Kumar Nishad, Assistant Professor, Electronics and communication Engineering Department, NIT Warangal for his support, suggestions and advices to carry out the research.

It is my pleasure to show my indebtedness to my co-scholars at NIT like Dr. P. Akhendra Kumar, Dr. Sudeep Surendran, Dr. Mudasir Bashir, Mr. M. A. Mushahhid Majeed, Mr. D. Pawan Kumar Sharma, Mr. T Sunil Kumar, Mr. V. Santhosh Kumar, Mr. R. Sahoo, Mr. B. Ravi, Mr. B. Roshan, Dr. Nagesh Deevi, Dr. A. Suresh, Mr. S. Subbarao, Mr. D. Kiran and Mr. Jailsingh Bookya for their help during the course of this work.

I find no words inadequate to express any form of acknowledgement to my parents, Mr. Rebelli Venkata Ramana and Mrs. Rebelli Sumithra Devi and my wife, Mrs. Rebelli Mrunalini for their love, support and patience for making my dream come true.

Finally, I thank God, for filling me every day with new hopes, strength, purpose and faith.

ABSTRACT

With the advent of technology scaling, the efficiency of the interconnects effect the overall performance of the circuit. Although active devices mostly benefited from scaling, the performance of intermediate and global interconnects has degraded because long interconnects do not scale with the technology. Apart from power dissipation and overshoot issues, signal integrity issues such as propagation delay of long interconnects become a bottleneck in high-speed operation of ICs. Also, functional/dynamic crosstalk result in malfunctions in the circuit leading to reliability problems. Hence, there is a great demand for estimation of propagation delay and crosstalk noise of coupled interconnect lines in the early stages of VLSI design.

This thesis focuses on the development of a novel time-domain numerical method with significant numerical dispersion characteristics based on the wavelet scaling functions to address the signal integrity issues of on-chip interconnects. The multiresolution time domain (MRTD) model with its unique features is tailored for modeling VLSI interconnects. To build further credence to this and its profound existence in the recent state-of-the-art, simulations for inclusive crosstalk noise, on driver-interconnect-load (DIL) system, using the MRTD model and conventional finite-difference-time-domain (FDTD) model are performed.

Initially, in this thesis, an attempt is made to derive an MRTD scheme for two coupled copper (Cu) interconnect lines driven by the linear resistive driver in 130 nm CMOS standard process to compute the effect of coupling parasitics (i.e., coupling capacitance and mutual inductance) on peak crosstalk noise and propagation delay. For different values of coupling parasitics, the variation in peak crosstalk noise and propagation delay is observed and a comparison is done between the obtained results with those of the conventional FDTD model with respect to HSPICE simulation results. Moreover, variation in accuracy of the proposed MRTD model for a range of frequencies is observed and encouragingly it is found that approximately 100 % accuracy is maintained for a broad frequency range although a slight perturbation does exist within a short range of frequencies.

However, in DIL systems, replacement of non-linear CMOS driver with a simple linear resistor leads to a discrepancy in the results as about half of the operating time of MOSFET is in the saturation region, whereas the other half is divided between the cutoff and the triode regions. Therefore, the proposed MRTD model is extended to include the non-linear characteristics of the CMOS driver in the DIL system for 32-nm technology node. The non-linear CMOS driver is analyzed by employing the n-th-power law model. For the robustness of the model, a different number of test cases in terms of input transition time are considered and the peak crosstalk

noise and peak noise timing are also computed for the two coupled Cu interconnects. Further, the model is extended to three mutually-coupled Cu interconnect lines.

Further scaling of interconnect dimensions have made surface scattering and grain boundary scattering more prominent, resulting in increased resistivity of Cu material. Therefore, the requirements of novel material as VLSI interconnect has increased. In recent times, carbon nanomaterials such as carbon nanotubes (CNTs) and graphene nanoribbons (GNRs) act as the most promising candidates proposed as a substitute for Cu interconnects in advanced VLSI circuits. Thus, the proposed MRTD method is extended to analyse the inclusive crosstalk effects in CMOS gate driven two and three mutually-coupled MWCNT interconnects at 32-nm technology node. It is observed that a peak overshoot/undershoot occurs in the response of line 2 (victim line) as the conventional FDTD method has higher dispersion errors. Nevertheless, the numerical dispersion properties in MRTD model acts as an added advantage over the conventional FDTD model for achieving better accuracy. Finally, it is concluded that the proposed MRTD method is in good agreement with HSPICE simulations and dominates the conventional FDTD method. Furthermore, the validation of the proposed model with future selective validation (FSV) proves its accuracy and efficiency for analyzing the crosstalk effects in mutually coupled MWCNT interconnects.

This thesis shows that the proposed MRTD method is more time efficient than HSPICE, although the elapsed CPU time of the proposed MRTD method is higher than the conventional FDTD method, due to an increased number of iterations for better accuracy. Hence, there exists a trade-off between simulation time and accuracy. The analysis has been carried out on two coupled and three-coupled interconnects, but can also be extended to N-mutually coupled interconnects.

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List of Abbreviations

3-D	Three Dimensional
2-D	Two Dimensional
BEM	Boundary Element Method
CAD	Computer Aided Design
CDF	Cohen-Daubechies-Feauveau
CFL	Courent-Friedrich-Lewy
CMOS	Complemtary Metal Oxide Semiconductor
CMS	Current-mode signaling
CNT	carbon nano-tube
CPU	Central Processing Unit
DSM	Deep Sub-micron
DIL	Driver-Interconnect-Load
ECAD	Electrical Computer Aided Design
EM	Electro Magnetic
ESC	Equivalent Single Conductor
FDTD	Finite Difference Time Domain
FMM	Fast Multi-pole Method
FSV	Feature Selective Validation
GDM	Global Difference Measure
GNR	graphene nano-ribbon
IC	Integrated Circuit
IP	Intellectual Property
ITRS	International Technology Roadmap for Semiconductors
MCB	Mixed-carbon nano-tube bundle
MEMs	Micro Electromechanical Systems
MFP	mean free path
MIT	Massachusetts Institute of Technology

MLGNR	multi-layer graphene nanoribbon
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MRTD	Multiresolution-time-domain
MWCNT	multi-walled carbon nanotube
nMOS	n-channel Metal-Oxide-Semiconductor
PCB	Printed Circuit Board
PDE	Partial Differential Equations
pMOS	p-channel Metal-Oxide-Semiconductor
p.u.l	per unit length
RC	Resistance Capacitance
RLC	Resistance Inductance Capacitance
SLGNR	single layer graphene nano-ribbon
SoC	System On-Chip
SPICE	Simulation Program with Integrated Circuit Emphasis
SWCNT	single walled carbon nano-tube
TEM	Transverse Electromagnetic
TL	Transmission Line
TSV	Through-Silicon Via
VLSI	Very Large Scale Integration
VMS	Voltage-mode signaling

List of Symbols

S	Scaling Factor
L_{ch}	Channel Length
t_{ox}	Gate Oxide Thickness
W	Channel Width
V_{DD}	Supply Voltage
τ_g	Gate Delay
w	Interconnect Width
s	Spacing between the two coupled interconnects
t	Interconnect Thickness
l	Length of the interconnect
A_c	Chip Area
τ	RC Delay
λ_d	Finite Drain Conductance Parameter
ε	Dielectric Constant
R	Line Resistance p.u.l
L	Line Inductance p.u.l
G	Line Conductance p.u.l
C	Line Capacitance p.u.l
C_{12}	Coupling Capacitance between Line 1 & Line 2
C_{23}	Coupling Capacitance between Line 2 & Line 3
M_{12}	Mutual Inductance between Line 1 & Line 2
M_{23}	Mutual Inductance between Line 2 & Line 3
M_{13}	Mutual Inductance between Line 1 & Line 3
C_L	Load Capacitance
R_D	Driver Resistance
Δz	Space discretization interval
Δt	Time discretization interval
Nz	Number of space segments
$\phi(z)$	Daubechies' scaling function
$h(t)$	Pulse function
$\delta_{n,n'}/\delta_{n,n'}$	Kronecker symbol
S_b	Effective support size
D_4	Daubechies' scaling function with four vanishing moments
$\hat{\phi}(\lambda)$	Fourier transform of a scaling function $\phi(z)$

$a(i)$	Connection Coefficient
q	Courant number
ϑ	phase velocity
C_d	Drain diffusion capacitance
C_m	Gate-to-Drain coupling capacitance
I_{DSAT}	Drain saturation current
V_{DSAT}	Drain saturation voltage
V_T	Threshold Voltage
δ	van der Waals gap
R_{lump}	Lumped Resistance
R_q	Quantum Resistance
R_{mc}	Imperfect contact Resistance
R_S	Scattering Resistance
L_M	Magnetic Inductance
C_E	Electrostatic capacitance
d_M	Outer-most diameter of MWCNT
d_1	Inner-most diameter of MWCNT
M	Number of concentric shells in the MWCNT

Chapter 1

Introduction

1.1 Background

The density and complexity of Very Large Scale Integrated (VLSI) circuits has increased exponentially over the last two decades resulting in high performance electronic systems for a wide range of applications such as reconfigurable computing, mobile and satellite communication, multimedia, micro-electromechanical systems (MEMS) and robotics. The count of active devices has reached hundreds of millions, while connecting wires among the devices tend to grow linearly with the transistor counts [1].

An integrated circuit (IC) comprises of several components and functional blocks, such as transistors, gates, sub-circuits etc., which are interconnected using aluminum (Al)/ copper (Cu) metals or graphene-based materials. Interconnects are capable of transmitting data from one block to the other, in the form of current or voltage. Ideally, the signal transmission/reception between the two interconnected blocks should be instantaneous with no delay. However, this cannot be achieved in practical situations, due to the fact that there always exists a signal propagation time during the transmission of data from one block to the other. If the signals vary rapidly (high frequency applications) compared to the propagation time, several effects may be observed such as Delay, Overshoot, and Crosstalk [2]. Currently in the deep submicron (DSM) regime, performance of electronic systems depends on these effects introduced by interconnections. Hence, it is very important to have accurate and efficient estimation models of the interconnection effects at the design phase itself to avoid pitfalls and to reduce the time to market of VLSI chips.

In the state of the art, there are several viable models developed (with variable degrees of accuracy), starting from a simple capacitor model to a frequency-dependent transmission line model. These models are more or less a simplified analysis of the fundamental physical event i.e., the propagation of an electromagnetic (EM) wave in the complex metal-dielectric structure formed by the interconnection network of an electronic circuit. Here, the complication is that a comprehensive EM analysis of an IC is beyond the present day computation capabilities. Hence, the EM phenomena are replaced with electrical models. Even complex electrical models are replaced with simpler electrical models when accuracy is not critical, because the simulation time of complete system would otherwise be extremely long [3].

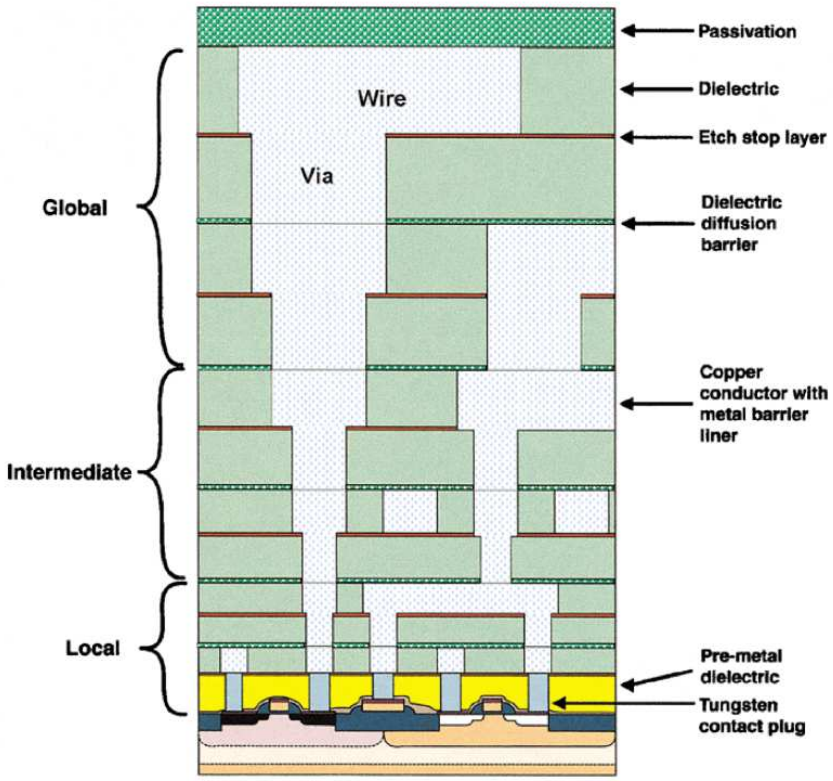


Figure 1.1: Cross sectional view on the stack of layers in an IC [1].

Depending on the length, interconnects are classified into local, intermediate and global interconnects [4]. Local interconnects are very thin wires and are used to connect gates and transistors within any block on a chip. This type of interconnects generally occupies the lower few metal layers in a multi-layered interconnect structure as shown in Figure 1.1. Intermediate interconnects are used to distribute clock/data signals within a functional block or between the adjacent blocks and where the typical length between the blocks can vary up to 2.5 mm. Generally, these types of interconnects occupy few layers above the local interconnects. Global interconnects are used to connect a large number of intellectual property (IP) blocks, such as filters, memory, processing elements and interfaces. As these IP blocks need to communicate

with each other over long distances, they need long wires that span most of the length of the entire chip size. Global interconnects are wide and long metal layers in a multi-layer structure and fill top few layers. Typical lengths of these global interconnects are greater than 2.5 mm and sometimes as long as half of the chip's perimeter. Generally, the top metal layers are reserved for routing of the power/ground/clock signals. The dimensions of local interconnects perfectly scale with technology scaling, whereas the dimensions of intermediate and global interconnects do not scale proportionally with technology scaling.

With the technology scaling the gate/transistor delay and wire delay of the local interconnects decreases, whereas the delay of the intermediate/global interconnects increases. Advanced scaling techniques such as the use of low K dielectric materials improves the delays of the local interconnect. However, with the scaling of every successive technology node below 0.25 μm, the delays of intermediate/global interconnect become much worse than gate delays [1]. In addition, as compared to the local interconnect, the length of global interconnect is not scaled with technology leading to an increase in delays as these wires need to run across the entire chip. Thus, as compared to the gate delay and local interconnect delay the global interconnect delay becomes a limiting factor in determining the overall circuit performance in the present day VLSI chips. Global wiring among the functional blocks provides the distribution of clock/signal and delivers ground/power to all functions on an IC. Figure 1.2 illustrates the local and global interconnect delay in future generations. To reduce the delay in global wiring, the repeaters can be incorporated by compromising the power consumption and chip area.

In DSM VLSI regime, the speed of any electrical signal depends on two factors, namely the transistor gate delay and the propagation delay of interconnects. The major challenges in VLSI circuits are global interconnect delays and crosstalk noise between multiple interconnects. These signal integrity problems in interconnects decide the overall performance of VLSI circuits. For the iterative layout design of densely populated IC's accurate analytical models are needed to efficiently predict signal degradation due to propagation delay, crosstalk noise, and signal overshoot in the early design cycles [5]–[7]. The existing computer aided design (CAD) tools for signal integrity analysis are more time-consuming and inefficient. Hence, interconnect simulations suffer from a number of signal integrity issues which require sophisticated CAD tools for analysis. Computationally high-speed and accurate interconnect models are needed at the initial stages of an IC design for design optimization and post-layout verification, respectively. During the physical design, interconnect area, propagation delay, overshoot, power and crosstalk noise estimations are the main performance metrics. This thesis addresses the estimation of propagation delay and crosstalk noise in the mutually coupled on-chip interconnects.

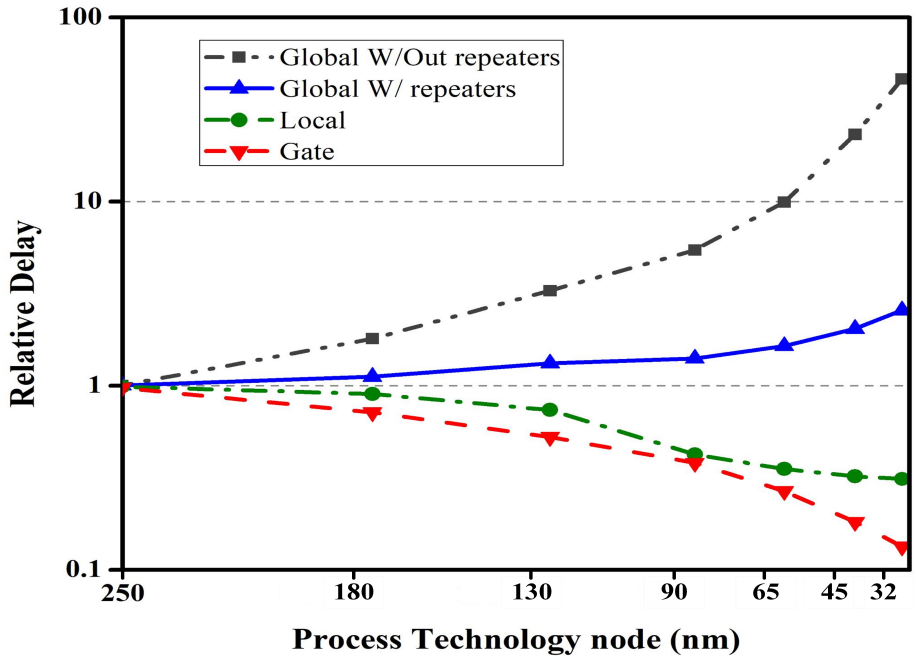


Figure 1.2: On-chip interconnect delay across different technology nodes [1]

In the early phase, the gate capacitance of transistors dominated the interconnect parasitic capacitance, which makes use of the assumption of modeling of interconnects as short circuits. Later on, with technology scaling, the interconnect parasitic capacitance dominates the gate capacitance and interconnect was modeled as a lumped capacitance [8, 9]. With the further technology downscaling, inclusion of resistance effect in on-chip interconnect became mandatory for global interconnects which increases the accuracy. This results in introduction of lumped resistance-capacitance (RC) models for the performance analysis of on-chip interconnects [10, 11]. However, the lumped RC models are treated as the distributed RC model [5] for better accuracy. Currently, because of the high switching frequencies and the adoption of low resistive interconnect materials, the parasitic inductance plays an important role in the performance of on-chip interconnects. To estimate the performance of the interconnects accurately, they must be considered as transmission lines or as distributed resistance-inductance-capacitance (RLC) interconnect lines [12].

Initially, crosstalk noise estimation models considered only capacitive coupling [13, 14]. However, inductive-crosstalk effects should be included at current high-frequency operations for the inclusive analysis of coupling noise. At high frequencies, the transient crosstalk, i.e., the undesired effect of a signal transmitted on one line over another, is produced due to closely packed interconnects [15]–[17]. The propagation delay of the signal is strongly influenced by

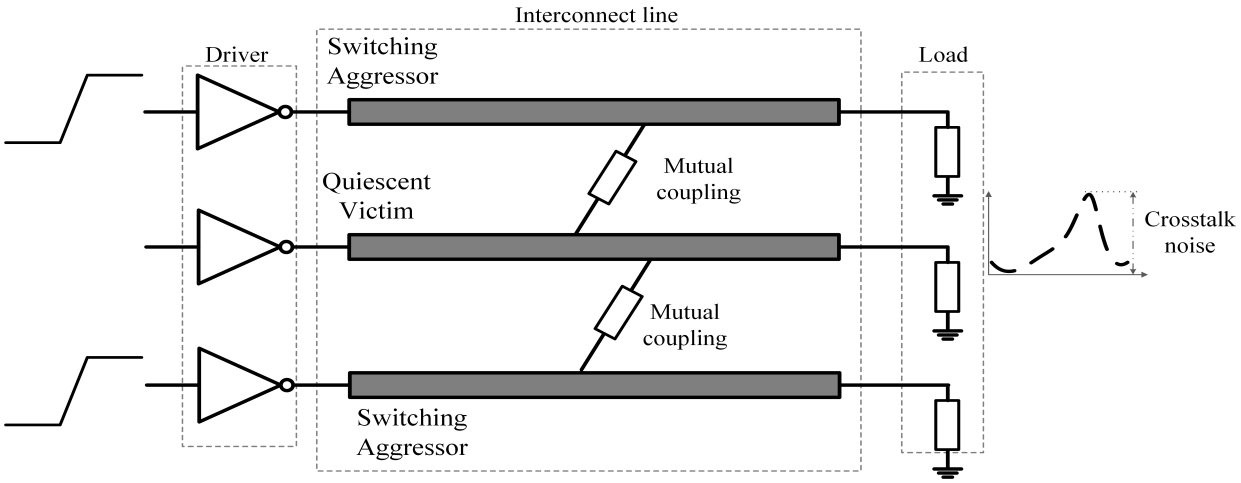


Figure 1.3: Crosstalk in closely placed interconnects

the crosstalk noise, which results in functional failure or circuit malfunction. The crosstalk between the coupled lines is considered to be dynamic and functional crosstalks, depending on the input switching transitions in the coupled interconnects. Dynamic crosstalk occurs when the adjacent lines are simultaneously switching either in-phase or out-phase. Whereas, the functional crosstalk appears as a voltage spike when the victim line is at quiescent while switching an aggressor line as shown on Figure 1.3. A change in propagation delay and logic value can be observed under dynamic and functional crosstalks, respectively. In addition, the crosstalk noise effects include ringing and signal overshoot/undershoot. Therefore, there is a need for an accurate estimation of performance parameters for designing high-performance on-chip interconnects incorporating the effect of crosstalk noise.

A noise model [18] was proposed for the analysis of noise effects in two coupled RLC lines, but it is limited to loosely coupled interconnect lines where coupling capacitance and mutual inductance are negligible as compared to ground capacitance and self-inductance, respectively. Similarly, another analytical model [19] was proposed for coupled on-chip RLC line, in which two lines were isolated. Further, each isolated line is approximated as a one-segment RLC $\pi-$circuit. The major limitation of this method is that it can be applied only to isolated lines with separated drivers. Agarwal et al. [20] proposed an analytical scheme to model crosstalk noise in the coupled RLC interconnects by considering the linear characteristics of CMOS (complementary metal oxide semiconductor) driver i.e., linear resistive driver. This model is further extended to a nonlinear CMOS driver considering $\alpha-$power law model to analyze dynamic crosstalk effects [21] and functional crosstalk effects [22] by Kaushik et al. The models that are purely limited to two coupled interconnect lines based on even-odd modes reported in [20]–[22]. Furthermore, only the ideal or lossless lines are considered for the transient analysis.

The modeling of CMOS driver based distributed RLC lines suffer from time/frequency domain conversion issue. This issue occurs because the CMOS driver is modeled in the time domain, whereas the partial differential equations (PDEs) are used to solve the transmission line (TL) model in the frequency domain. Therefore, many researchers [15], [20], [23] substitute the nonlinear CMOS driver with a linear resistive driver compromising the overall accuracy of the model. In the recent past, the TL equations in the time domain were solved using finite-difference time-domain (FDTD) method [24] to avoid the conversion problem.

1.2 On-chip interconnects in CMOS technology

CMOS is the most widely used technology for building of VLSI chips. In CMOS technology, transistors are fabricated in a doped silicon substrate, usually with a gate of polysilicon on the top of the oxide layer. Transistors can be connected to power, ground/clock lines, and a stack of metal layers [25]. Different metal layers are connected using Vias and the space between metal layers is filled with dielectric material.

1.2.1 Technology Scaling

The technology scaling reduces the dimensions of the MOSFET (Metal Oxide Semiconductor Field Effect Transistor) and associated interconnects, which enhances the performance and the component density per area. The constant electric field scaling scales down the dimensions of the MOSFETs by a factor of $\frac{1}{S}$ and the resultant first order effects are given in Table 1.1. This kind of scaling increases the device density by a factor of S^2 and decreases the gate delay and power dissipation by $\frac{1}{S}$ and $\frac{1}{S^2}$ factors, respectively [5]. Hence, the scaling of MOSFET dimensions increases the overall circuit performance.

The technology scaling poses major challenges to interconnects especially in high speed/performance ICs. As chip size grows larger and interconnect geometries are scaled, resistive, inductive and capacitive effects associated with the interconnects effects the performance of high-speed ICs in DSM regime.

Table 1.2 shows the ideal scaling of local interconnects, where all horizontal and vertical dimensions are reduced by the same factor [5]. Local interconnects length usually shrinks at the same rate of technology scaling. The other dimensions also shrink by the same factor of $\frac{1}{S}$.

Table 1.1: Scaling effects on MOS device

Parameter	Scaling factor
Channel Length (L_{ch}), Gate oxide thickness (t_{ox}), width (W) and Voltage (V_{DD})	$\frac{1}{S}$
Current per device (I_{DS})	$\frac{1}{S}$
Gate capacitance (C_g)	$\frac{1}{S}$
Transistor ON resistance (R_g)	1
Gate delay (τ_g)	$\frac{1}{S}$
Device area (A)	$\frac{1}{S^2}$
Power dissipation (P)	$\frac{1}{S^2}$

The parasitics such as capacitance decrease by a factor of $\frac{1}{S}$ and resistance increases by S. As a result, local interconnect delay remains unchanged in ideal scaling.

Table 1.2: Scaling of Local Interconnects

Parameter	Scaling factor
Local interconnect width (w), Substrate height (h), Spacing (s) and Thickness (t)	$\frac{1}{S}$
Local interconnect length (l)	$\frac{1}{S}$
Resistance (R)	S
Capacitance (C)	$\frac{1}{S}$
RC delay (τ)	1
Voltage drop ($I \times R$)	1
Current density (J)	S

Over the many years, scaling has become a problem of growing importance in case of intermediate/global interconnects. As the technology is scaled, the length of the intermediate/global interconnects increases instead of shrinking. This is because the chip area of each new technology generation keeps increasing to accommodate more functionalities and hence more components are needed to implement those extra functions. This causes an increase in intermediate/global interconnects lengths to connect all the devices.

Table 1.3 shows the ideal scaling effects of intermediate/global interconnects [5]. Scaling of the intermediate/global interconnects increases the delay in proportion to the wire length and wire resistance. Because intermediate/global interconnects length is dependent on the chip area (A_c) and the length of the longest global interconnect is related to the chip area approximately

Table 1.3: Ideal scaling of Intermediate/Global Interconnects

Parameter	Scaling factor
Intermediate/Global interconnect width (w), Substrate height (h), Spacing (s) and Thickness (t)	$\frac{1}{S}$
Intermediate/Global interconnect length (l_{gb})	S_C
Resistance (R_{gb})	$S^2 \cdot S_C$
Capacitance (C_{gb})	S_C
RC delay (τ)	$S^2 \cdot S_C^2$
Voltage drop ($I \times R$)	$S \cdot S_C$

by $\frac{\sqrt{A_c}}{2}$ [4]. Hence, scaling of these interconnects will not shrink in the same proportion as that of transistor gate length.

In summary, technology scaling decreases the gate delay (transistor delay) and local interconnects delay whereas intermediate/global interconnects delay increases. Advanced techniques of scaling such as usage of low-dielectric-constant-insulator and weak scaling of line thickness improve the situation, so that interconnect delays nearly track the gate/transistor delays. However, intermediate/global interconnect delays become much worse than gate delays for technology nodes below 0.25 μm as can be seen from Figure 1.2. Thus, the intermediate/-global interconnect delay becomes a limiting factor in determining the overall circuit performance in the present day VLSI chips.

1.2.2 ITRS Predictions

The ITRS 2012 [26] predictions on the future trend of interconnect dimensions, delay, technology nodes etc. are given in Table 1.4. The total length of on-chip interconnects increases linearly with technology down scaling and it will approach approximately 16700 $\frac{m}{cm^2}$ by 2027. In addition, the delay of intermediate and global interconnects will increase quadratically with technology and it will reach to 310 ns and 110 ns, respectively.

As per the ITRS 2012 [26] and 2013 [27], feature sizes of the devices are scaling down roughly at a rate of 0.7 in every two years, which results in the doubling of gate density, reduction of gate delay by 30% and reduction of energy per switching by 65%. Thus, scaling the transistor dimensions lead to improvements in both performance and cost.

Table 1.4: ITRS prediction on scaling trends[26, 27]

Parameter \ Year	2012	2015	2018	2021	2024	2027
Technology None (nm)	36	25	18	12	9	6
Number of metal levels	12	13	14	15	15	16
Total interconnect length (m/cm^2)	3,125	4,762	6,667	9,434	13,333	16,779
Intermediate wiring pitch (nm)	64	42	30	21	15	12
Aspect Ratio (AR) of intermediate interconnects	1.9	1.9	2.0	2.1	2.1	2.2
Intermediate interconnects RC delay (ps)	4,814	13,716	29,761	64,552	141,966	310,000
Global interconnect wire pitch (nm)	96	63	45	32	23	17
Aspect Ratio (AR) of global interconnects	2.34	2.34	2.34	2.34	2.34	2.40
Global interconnects RC delay (ps)	1,528	4,005	9,127	21,542	44,064	110,000
Effective dielectric constant (k)	2.8 - 3.2	2.5 - 3.0	2.4 - 2.8	2.1 - 2.5	1.8 - 2.3	1.6 - 2.0
Copper effective resistivity ($\mu\Omega$-cm)	4.53	5.58	6.7	8.51	12.91	14.06
Wafer diameter (mm)	300	450	450	450	450	450

The lengths of the local interconnect and transistor gate lengths scale down similarly, whereas intermediate/global interconnects tend to track the dimensions of a chip. Generally, in consecutive technology generations, the die area should decrease by 50% but advanced designs integrate more transistors and functionalities per chip, results in a requirement for more die area. Over the years, die area and total interconnect length has increased by approximately 13% and 6% per year, respectively, resulting in an overall increase of interconnect delay by approximately 120% [28]. More delay implies increased power consumption, signal attenuation, ringing effects etc. Hence, intermediate/global interconnects play a major role in determining the performance of the present-day ICs. In DSM VLSI designs the global interconnect lengths may run to several hundreds of meters.

1.3 Evolution of Interconnect Materials

The continuous growth in an IC technology leads to reduced device dimensions, increased complexity and larger chip sizes. Also, a tremendous increase in the demand for the IC's with component density and higher speed [29]. Initially, IC designers adopted Al metal as a VLSI interconnect due to its compatibility with silicon (Si). Later on, with the downscaling of device dimensions the reliability of Al interconnect decreased. In the recent past, Cu is considered as a interconnect material alternative to Al due to its high current density. Further, as the high frequency of operations are becoming more intense, researchers are forced to look for new and reliable materials such as optical [30], Graphene [31] material based interconnects in the near future.

1.3.1 Aluminum Interconnects

Recent IC's require a large number of closely separated wires that integrate the components on a single chip. To achieve lesser transit delays and higher packing densities, the multi-layer interconnections must be considered with the growing IC technology [32].

For several generations of semiconductor technology, Al has been considered to form metal interconnects due to its compatibility with Si and low resistivity. With the downscaling of device dimensions the current density increases. This has a negative impact on the reliability of IC's that is due to the formation of hillock and electromigration, which causes electrical shorts between consecutive levels of Al.

1.3.2 Cu as a substitute for Al Interconnect

With the advancement in technology, Al was unable to fulfil the demands due to its demerits. Thus, the researcher's lookout for promising options with lower electrical resistivity such as gold (Au), silver (Ag) and copper (Cu) as replacement of Al metal. Table 1.5 shows the resistivity of these potential metals.

Au has low resistivity than Al, but it shows larger resistance to electromigration. Major demerit is that gold establishes deep-levels in the bandgap due to the diffusion of gold in silicon and thus badly influence the electronic characteristic of the device. Similarly, Ag establishes deep-levels in the bandgap of silicon and diffuses in silicon dioxide (SiO_2) consecutively due

Table 1.5: Resistivity of conductor materials [30]

Material	**Thin-film resistivity** ($\mu\Omega$ cm)	**Bulk resistivity** ($\mu\Omega$ cm)
Al	2.7	2.65
Au	4.1	2.4
Cu	**2.1**	**1.7**
Ag	-	1.6

to its lower resistivity. Moreover, Ag exhibits a low melting point results in low resistance to electromigration. However, Cu with low resistivity, higher melting point compared to Al delivers better performance with respect to electromigration effects and stress. Today, Cu is broadly used on-chip interconnect material in advanced IC's.

1.3.3 Necessity of Future Interconnects

Further scaling down of interconnect dimensions have made surface scattering and grain boundary scattering more prominent, resulting in increased resistivity of Cu material [16]. In addition to this, the skin effect, electromigration effect, low thermal and electrical conductivity, small mean free path (MFP) and limited current density also degrade the performance of an IC [33]–[35]. Therefore, the requirements of new and reliable materials for IC interconnects has increased. In the recent times, graphene-based nanomaterials such as carbon nanotubes (CNTs) and graphene nanoribbons (GNRs) are considered as the most promising candidates proposed as a substitute for Cu interconnects in advanced VLSI circuits [36, 37].

1.3.3.1 Carbon Nanotubes (CNTs)

CNTs are cylindrically rolled up single layered graphene sheets having diameters varing from 1 to 5 nm. CNTs with their outstanding thermal and electrical properties, such as high melting point (3800 K), higher thermal stability, large mean free paths and the maximum current density (10^{10} A/cm^2), outperform the conventional Cu interconnect [38]. Based on the physical properties, carbon nanotubes are classified into two types: single-walled CNTs (SWCNTs) and multi-walled CNTs (MWCNTs) [39, 40]. The MWCNTs have few concentric shells of rolled up graphene sheets with their diameter ranging from few nanometers to tens of nanometers. Based on the chirality of graphene sheets, the SWCNT exhibits either metallic or semiconductor be-

haviour whereas the MWCNT exhibits only metallic behaviour [37]. Due to the large diameter and considering all the shells adequately connected to the metal contacts, MWCNTs have long electron MFPs and a great number of conducting channels compared to SWCNTs. Although the MWCNTs provide similar current carrying capability as SWCNTs, they are simpler to fabricate due to their greater control over the growth process [41].

1.3.3.2 Graphene Nanoribbons (GNRs)

GNRs are strips of graphene layer with ultra-thin width. They are attracting many researchers as a powerful alternative material for next generation VLSI interconnects [42, 43]. Most of the electrical and physical properties of GNRs are identical to the CNTs. However, the advantage of GNRs over CNTs is that the fabrication of both interconnects and transistors can be done on the same graphene layer [44]. Based on the number of stacked layers of graphene, GNRs are categorized into two types: single-layer GNRs (SLGNRs) and multi-layered GNRs (MLGNRs). Compared to SLGNRs, MLGNRs are mostly preferred as interconnect material because of the easy fabrication process and lower resistivity. However, the major demerit is that the fabricated MLGNRs show a little edge roughness [45, 46], resulting in decreased electron MFP that considerably reduces the conductance of MLGNRs.

1.4 Motivation

In the early days of very large scale integration design, the relatively low integration density and low frequency of operation have suppressed the crosstalk-induced signal integrity effects. However, owing to the technology scaling in the submicron regime, there were significant changes in the electrical characteristics and overall structure of interconnects [47, 48]. Thus, the overall performance and robustness of an IC mainly depend on the interconnect lines and the electrical behavior of the interconnect model is in turn influenced by the line parasitic elements. Therefore, there is a need for accurate models to analyze the crosstalk-induced signal integrity effects in the driver-interconnect-load (DIL) system.

To analyze the signal integrity issues, such as functional crosstalk and dynamic crosstalk effects, there are several methods, such as analytical and SPICE solutions have been proposed to model a DIL system as reported in [22]. However, in the present state of the art, most of the researchers rigorously studied the crosstalk effects based on the conventional FDTD

algorithm due to its accuracy [24]. The conventional FDTD model is a significant numerical model for solving electromagnetic (EM) problems and partial differential equations. However, the conventional FDTD method with better accuracy causes numerical dispersion error during the propagation along the discretization [49, 50], leading to discrepancy in the results. Hence, there is an extensive requirement of a novel method with an advantage in numerical dispersion properties.

1.5 Problem statement

To model and analyze the crosstalk noise effects in DSM VLSI interconnects, in the recent state of the art, most of the researchers used the conventional FDTD algorithm due to its accuracy. However, the conventional FDTD model with better accuracy causes a numerical dispersion error during the propagation along the discretization, leading to discrepancy in the results.

1.6 Objectives

The objectives of the work are:

1. A novel mathematical model with an added advantage in numerical dispersion properties need to be proposed for achieving better accuracy with respect to present state of the art.
2. To analyze the effect on propagation delay and crosstalk noise by varying coupling parasitics in resistive driven coupled Cu interconnects using the proposed method.
3. To analyze the crosstalk noise effects in CMOS driven coupled Cu interconnects based on the proposed model.
4. To analyze the inclusive crosstalk effects in CMOS driven multiple coupled MWCNT interconnects using the proposed model.

1.7 Organization of Work

The thesis is organized into six chapters. The following section gives a summary of chapters.

Chapter I presents a brief introduction to the importance of VLSI interconnects, various delay and crosstalk models. The motivation behind this research work and the thesis objectives and contributions are also presented. In the end, the organisation of the thesis is elaborated.

Chapter II reviews the recent related state of the arts available in the literature and a brief outline of the thesis is also presented.

Chapter III explains the proposed MRTD model for signal integrity analysis of coupled copper interconnects driven by the linear resistive driver at the 130-nm technology node. The proposed model captures the behaviour of propagation delay and peak crosstalk noise on victim line against coupling parasitics (M_{12} and C_{12}), which is in close agreement with those of HSPICE simulation results and dominates over the FDTD method.

In chapter IV, the proposed MRTD model is extended to non-linear CMOS driver for the analysis of crosstalk noise in the coupled copper interconnects at the 32-nm technology node. The non-linear characteristics of the CMOS gate are analyzed using the nth-power law model. The robustness of the model is tested for the peak noise voltage and peak noise timing at different input transition times for two coupled interconnects. Further, the model is extended to three mutually coupled interconnect lines. Moreover, for the transient analysis, the MRTD method is more time efficient than HSPICE.

Chapter V deals with an advanced interconnect material, i.e., multi-walled carbon nanotube (MWCNT) interconnect. The proposed MRTD model is used for the inclusive crosstalk noise analysis of the CMOS-gate driven coupled MWCNT interconnects at 32 nm technology node. The n-th-power law model is used to model the non-linear CMOS driver. The robustness of the model is validated by testing it for dynamic crosstalk effects over different capacitive load (C_L) values. Then, the proposed model is extended to three mutually coupled MWCNT interconnects and the same is validated for different input switching modes. Furthermore, the validation of the proposed model with future selective validation (FSV) proves its accuracy and efficiency for analyzing the crosstalk effects in mutually coupled MWCNT interconnects.

The conclusions and future scope of the thesis are presented in Chapter VI.

Chapter 2

Literature Survey

This chapter provides the literature on interconnect parasitic extraction methods and different modeling approaches for analyzing delay and noise in on-chip interconnects. The recent modeling techniques based on analytical and numerical methods are discussed.

2.1 Introduction

Interconnects are the physical links between electrical devices in ICs, printed circuit boards (PCB), electrical packages, multiple circuit blocks, backplanes in an electronic system. In VLSI, interconnect is a connecting path, usually a metal (Al/Cu) line, that joins different points in the circuit. Whenever any signal propagates through the circuit, interconnect responds in such a way that signal integrity suffers. The interconnect responds against the propagation of any signal in terms of delay, noise, reflection and these depend on many factors which can be classified into two groups. One group includes the factors associated with physical issues such as interconnect dimensions and its material. Another group consists of factors related to signal dependent issues such as the signal's amplitude and transition time. Interconnects behave as short circuit at low frequencies while at higher frequencies they behave as transmission lines (TLs). At higher frequencies, the interconnects are more responsible for majority of the signal degradation effects such as distortion, ringing, attenuation, signal delay, and crosstalk.

2.2 Extraction of interconnect electrical parameters

The primary requirement for interconnect modeling is mapping the physical parameters of the interconnect such as cross-sectional dimension, dielectric, length, and metal properties into relevant electrical parameters (R, L, G, C per unit length (p.u.l)). This process is called as parasitic extraction of interconnects. Extraction of interconnect electrical parameters using physical parameters can be done in two ways. One way makes use of analytical expressions developed by Golzar et al. [51]. Another way for finding per unit length electrical parameters is using 2-D field solvers, 2.5-D field solvers and 3-D field solvers [52, 53]. These field solvers provide good accuracy as compared to the analytical expressions at the expense of computational complexity.

2.2.1 Analytical Capacitance Extraction

In the past, there are comparatively few analytical models available for the capacitance extraction. The most popular model presented in [54] estimates the ground and coupling capacitances. The formulae presented in [54] have an accuracy of 10-15% when compared with the system level performance simulators [55]. In addition, a new model [56] includes inter-layer (or crossover) capacitance evaluation and achieves 5% error as compared to numerical field solvers [55].

It is essential to figure out the advantages and disadvantages associated with the use of analytical capacitance models. The main advantage is that the estimation of fast capacitance due to their closed-form nature. However, with technology scaling, the accuracy of closed-form equations becomes poor. Also, these expressions are restricted to a small set of structures. In these closed-form expressions, the numerical coefficients are retrieved by adopting the least-mean-squares-errors approach fitting from numerical models or experimental results that also contain errors. Although the accuracy is good still these models cannot be compared with field solvers extractions.

To compute the efficient capacitance and inductance of the interconnect segment, a powerful three-dimensional (3-D) field solver tools were developed at Massachusetts Institute of Technology (MIT) namely, FastCap [57] and FastHenry [58]. FastCap is used for the extraction of 3-D capacitance that calculates ground capacitance and coupling capacitance for ideal conductors of arbitrary shape, size, and orientation embedded in arbitrary dielectric regions. Similarly, FastHenry is used for the extraction of 3-D inductance that calculates self and mutual inductances and resistances between conductors of arbitrary shape.

2.2.2 FastCap

The field solver tool, FastCap, is particularly suitable to solve Maxwell's equations. This software helps users to reduce complicated structures to electromagnetically equivalent ones in terms of capacitive elements. In the particular case, this equivalence is valid up to a frequency bound of the harmonic content of the signals involved. Usually, this limitation is referred to as the Quasi-Static approximation against the full-wave approach. In the field solvers, the first distinction is observed at the dimensions of the geometries based on extraction. In the literature, there exist three levels of parasitic extractors as follows:

2-D Extraction: In this process, the effect of lateral capacitance along the wire is assumed to be uniform. The capacitance p.u.l. matrices are calculated by modeling the wires with infinite length along the 3-D.

2.5-D Extraction: In this process, a combination of two orthogonal 2-D structures are considered to model the 3-D effects. Once each section is transferred to a 2-D solver, the corresponding results are combined based on matrix operations.

3-D Extraction: This solver can calculate the ground and coupling capacitances of a set of 3-D structures sunk in a dielectric. The open source software, FastCap, belongs to this category.

To summarize, FastCap offers an excellent accuracy and is applicable for a wide range of structures as compared to analytical models. But the accuracy comes with a price of higher computation time and more hardware.

2.2.3 FastHenry

The FastHenry tool is developed for the extraction of 3-D inductance that calculates self and mutual inductances, conductance, and resistances between conductors of arbitrary shape. Rather than the rectangular panels, geometries of the conductor are represented as linear segments connecting endpoint nodes. Segments and nodes are assigned to the input file in the general form.

The fast multipole method (FMM) [59] was initially developed for the problems of particle simulation. This is used with recursive methods to solve the dense integral equation matrices resulting from the Laplace expressions. The tools for parameter extraction like FastCap [60]

and FastHenry [61] adopts the FMM for accelerating the dense matrix-vector products required by a recursive solver.

The freely available FastCap and FastHenry 3-D field solvers are accurate and powerful tools for VLSI interconnect modeling, simulation, and parasitic extraction. However, their application is restricted to simple structures and layouts, because layout extraction interface or non-commercial graphical modeling to these tools are currently not available, and input model files must be developed manually.

2.2.4 W-Model and TL Parameters Extractor

Another important ECAD (Electrical Computer Aided Design) tool, Avant Star-HSPICE [62] is used to extract electrical parameters and to perform electrical simulations. This tool typically computes the accuracy of the electrical timing simulator in two ways:

2.2.4.1 Field Solver

It is based on the upgraded version of the filament approach (for extraction of inductance) and boundary-element method (BEM) (for extraction of capacitance). These models are also included in Avant Raphael [63], a commercial EM field-solver, RLGC matrices are obtained from a quasi-static analysis, in which TLs support only pure transverse electromagnetic (TEM) waves. Arbitrary polygonal shaped conductors embedded in a vertically multilayered medium, with various viable configurations of meshes and ground planes can be simulated with this software. Complete verification of this field-solver is presented in [64].

2.2.4.2 W-Element

It is one of the HSPICE transmission line models, used to simulate simple lossless lines as well as lossy coupled lines with better accuracy and efficiency. The model can be applied to non-uniform and uniform TLs that are represented with ad-hoc approaches in order to obtain the transfer function. The W-element with $(N + 1)$ ports are specified with N number of inputs and outputs, and two reference terminals is illustrated in Figure 2.1. There is no limit on the number of coupled conductors. The main limitation of the W-element model is it can work only for symmetric RLGC matrices per unit length.

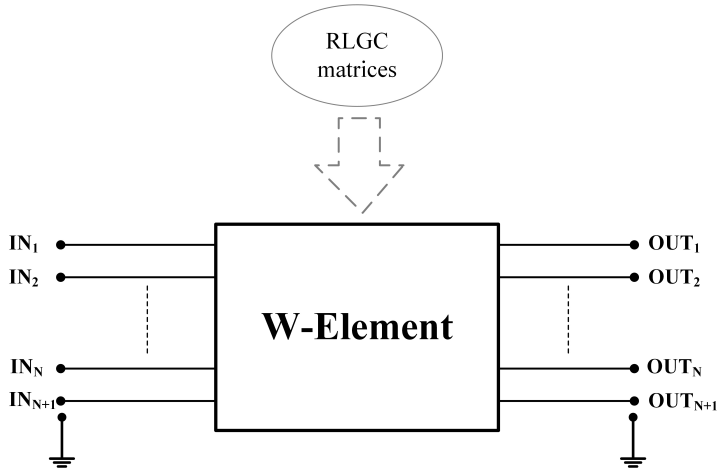


Figure 2.1: The star-HSPICE W-Element method

The advantages of HSPICE field solver are mainly represented by reduced simulation time and more accuracy when compared to other 3-D parameter extractors. Additionally, with just one W-element model tool, a complete characterization of RLGC can be retrieved and that can be imported easily into more complex HSPICE netlists. This is the motivation for using HSPICE field solver for extraction of parasitics in this research work.

2.3 Various interconnect models

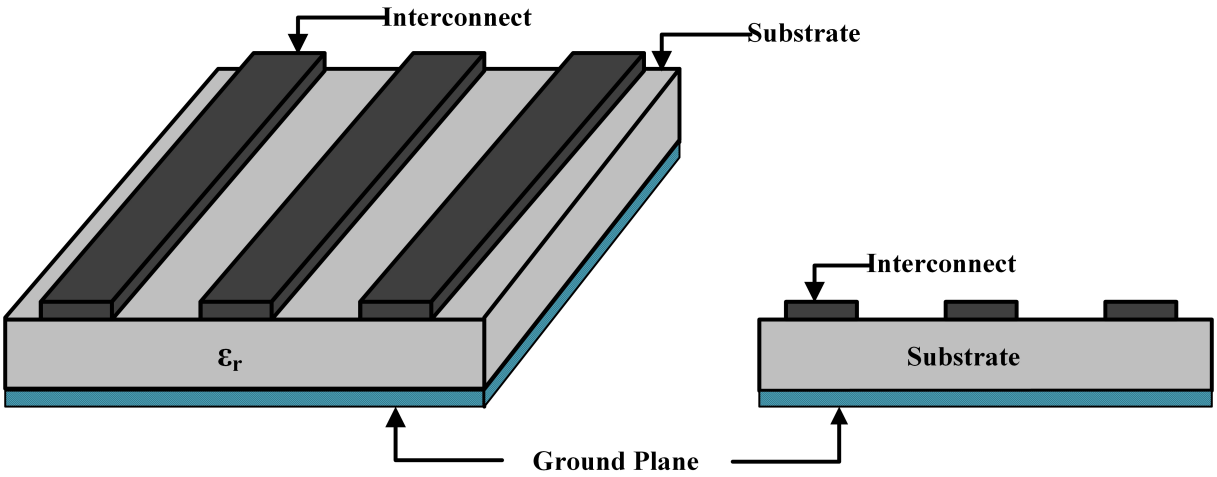


Figure 2.2: 3-D and cross sectional view of an interconnect structure

The per unit length electrical parameters (e.g. p.u.l R, L, G, C) are obtained using the geometry of interconnects (Figure 2.2), there is a need for accurate models to estimate delay, overshoot and crosstalk. Accurate interconnect models are needed to characterize the interconnect behavior accurately to estimate the real behavior. Interconnect models can be broadly

classified into lumped and distributed models based on the signal wavelength and the physical length of line. If the interconnect is shorter than the one-tenth of wavelength then it is considered as short interconnect otherwise it is a long interconnect. In general, electrically short interconnects can be modeled using lumped models, while distributed models are needed for electrically long interconnects.

There are various possible models starting from a simple capacitor to a frequency-dependent parameter TL with varying degrees of accuracy. There is no perfect model for the detailed EM analysis of a complete digital circuit with millions of interconnections and these are beyond the computation capabilities possible today. In general, the EM phenomena of interconnects are therefore reduced to simple electrical models. Even complex electrical models are reduced to further simpler electrical models like lumped capacitance model wherever accuracy is not important. However, the simulation time of a complete system of millions of interconnections would be excessively long. Hence, there is a need to assign a proper model to each interconnection sub-system, which can predict only those effects significant for that sub-system, without much computational complexity.

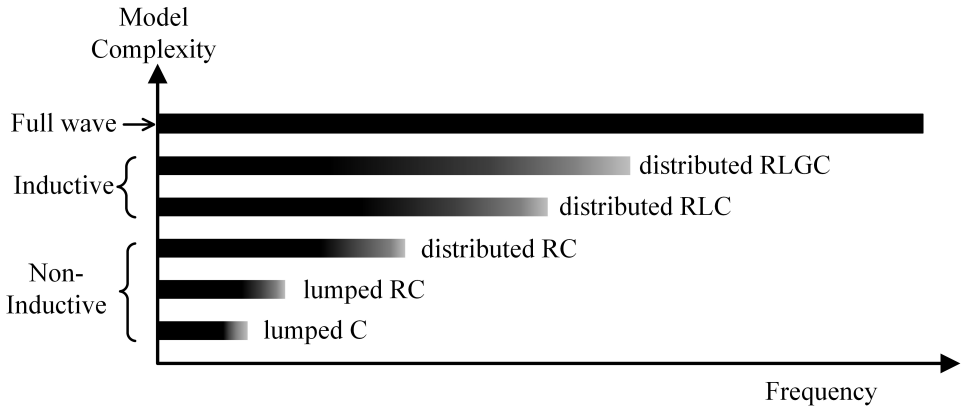


Figure 2.3: Validity of different interconnect models with respect to frequency [3].

The validity range of various models qualitatively in terms of frequency of the signal propagating inside the interconnect is shown in Figure 2.3. It also includes the computational complexity of each model. It is noticed that, the validity of maximum frequency operation of any model is not exact, because the user can decide the required accuracy. For example, digital circuit simulations in the early stages of physical design require an approximate estimate of delay and therefore lumped capacitive model accuracy is enough. For iterative layout design of densely populated ICs, accurate analytical models (distributed RLC/RLGC models) of delay and crosstalk noise estimations are required.

2.3.1 Analytical models for estimation of delay and peak crosstalk noise in the interconnects

In 1948, Elmore [10] developed an analytical model based on the first moment for estimating the delay of amplifier circuits, later this model was used for fast extraction of delay in simple RC interconnects. For IC's composed of millions of gates, it is often impractical to use highly accurate and computationally efficient models to estimate delay at each and every node in the circuit. Hence, the Elmore delay model is used as a quick estimator of relative delay calculation of different paths in the circuit. Figure 2.4 shows an interconnect tree network composed of resistance and capacitance elements. The delay of any path of tree network using this model is written as equation (2.1).

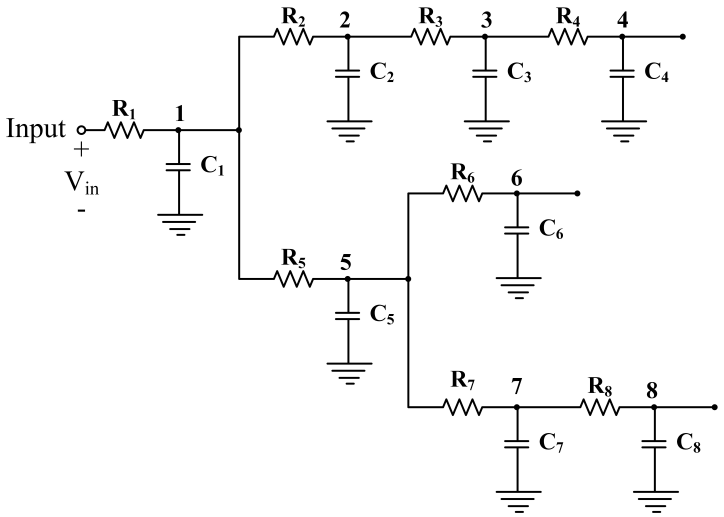


Figure 2.4: RC interconnect tree network.

$$\tau_{DK} = \sum_{j=1}^{K} C_j R_{jj} \Rightarrow \tau_{Dj} = C_1 R_1 + C_2 (R_1 + R_2) + \cdots + C_j \left(R_1 + R_2 + \cdots + R_j\right) \tag{2.1}$$

For noise analysis between two coupled lines, Sicard and Rubio [65] proposed a simplified model, which evaluates the effects of parasitic capacitive coupling. But this is applicable only for the interconnects when they are considered as simple capacitor models. Also, Vittal and Malgorzata [66] have considered the lumped capacitor model for appropriate channels and derived bounds for noise expressions using the lumped model where the line resistance was ignored. Later, this work is further extended in [14] to incorporate lumped π-model for RC

interconnects. Besides, the extension of these generalized expressions to the distributed models is less complicated.

In order to achieve better accuracy the lumped RC model must be treated as the distributed RC model. In [11], Sakurai provided analytical delay calculations for distributed RC interconnects. This model uses the Heaviside expression for calculation of time domain response. Using these expressions, the optimized width is calculated to reduce the bus RC delay. This optimized width is about half of the pitch provided the pitch is less than 4 times the height. For various source and load capacitance values, 90% and 50% delay values were presented in equations (2.2) and (2.3), respectively. The heuristic delay equation in this model is identical to the Elmore delay equation, which has similar constraints of the Emore delay model [10].

$$\frac{t_{09}}{RC} = 1.02 + 2.3\,(R_T C_T + R_T + C_T) \tag{2.2}$$

$$\frac{t_{05}}{RC} = 0.377 + 0.693\,(R_T C_T + R_T + C_T) \tag{2.3}$$

Moreover, Sakurai [11] derived an expression to estimate the coupled noise voltage in the victim line of the distributed RC network and presented its step response in terms of power series. As this series is too complicated to solve analytically, this model approximates the circuit to its first-order and extended the expression for the output voltage of two-coupled lines.

Currently, because of the high operating switching frequencies and the adoption of low resistive interconnect materials, the parasitic inductance plays an important role in the performance of on-chip interconnects. To estimate the performance of the interconnects accurately, they must be considered as TLs or as distributed RLC lines [12].

Based on the moments of the first and second order, Kahng and Sudhakar [67] proposed an analytical delay model for distributed RLC lines under step input to include the effects of inductance. The estimated delay using this model are within 15% of SPICE delays. They also extended their model to estimate the delay values for various combinations of source and load parameters. In [68], Yu et al. developed a novel analytical approach, which is a second-order RLC interconnect model for estimating delay, crosstalk noise and overshoot, accurately. Depending on current return path identification, this model can be used to decouple a set of coupled interconnects. Ismail et al. [69] developed an equivalent Elmore model for estimation of 50% delay in an RLC interconnect tree. This closed form delay model includes all damping

conditions (both monotonic and non-monotonic nature) of an RLC interconnect, which mainly differs from the Elmore delay model non-monotonic nature. This model provides closed-form solutions for the settling time, rise time/fall time, 50% delay and overshoot of signals in the distributed RLC interconnect tree. Out of these expressions, the delay formula of an RLC interconnect tree has similar accuracy characteristics with respect to the Elmore delay model. Davis and James [70] proposed a new compact model for the accurate analysis of transient response, overshoot and delay in the single high-speed distributed RLC interconnect, and the same is extended to coupled interconnect lines [71] for accurate estimation of peak crosstalk noise and transient response. Another efficient coupled crosstalk noise estimation method based on the model-order reduction approach is developed by Martin and Sachin [72]. This method computes the noise according to the time constant of the aggressor signal, the conductances and sink capacitances of the victim and the aggressor nets, respectively, and the coupling capacitance between those two nets.

Moreover, most of the researchers described the distributed RLC interconnect line as a transmission line based on the ABCD matrix approach [73]–[77], [2]. Banerjee and Amit [73] introduced an efficient analysis of inductance effects for global interconnects and the time domain response of a DIL system. In this model, interconnect is driven by a series-resistance and output parasitic capacitance of a repeater and the same is terminated by a load capacitance. Using the ABCD matrix approach and Laplace domain techniques, they have presented the accurate expressions for the transfer function of these global interconnect lines and their delay calculations.

In [74], Chun Li et al. derived a new recursive model considering the ABCD matrix of transmission lines for accurate estimation of propagation delay and time-domain response of interconnect trees. This method provides the exact transfer function of a distributed RLC interconnect tree using second-order approximation and moment matching for propagation delay calculations and fast simulation time, respectively. The accuracy of the method is validated by comparing it with HSPICE simulations.

In [75], Palit et al. presented the ABCD modeling approach, which is used to model the crosstalk coupling noise on the victim interconnect due to single or multiple aggressors. The same author in another paper [76] developed a distributed RLGC and decoupled victim line model by considering all possible sources or coupling noise (mutual capacitance and mutual inductance between the two adjacent victim and aggressor lines).

Zhou et al. [77] presented an RLC model to improve the accuracy of interconnect delay predictions in IC's. Initially, using the ABCD matrix the first two moments of the circuit is derived. And then the total delay is estimated using the rise time delay and transport delay. Another analytical model based on a Fourier series representation of the periodic input signal is proposed by Chen and Friedman [2], for the estimation of delay in RLC interconnect trees and the analysis of crosstalk noise in multiple lines. In this model, a transfer function of the interconnect line is derived based on the ABCD parameters.

However, with the higher clock frequencies, the on-chip interconnect lines behave as lossy TLs. Therefore, some researchers estimated coupling noise and delay of on-chip interconnects by adopting the transmission line model. Agarwal et. al. [20] developed an analytical framework based on transmission line theory to model coupling noise in coupled RLC lines. This model is applied to coupled lines under the terminal conditions introduced by CMOS drivers and receivers. But, the nonlinear effects of CMOS driver is replaced with its equivalent linear resistor and a capacitive load is considered at the receiver. This model is further extended by Brajesh and Sarkar in [22],[78], to include the nonlinear characteristics of the CMOS driver. These authors have adopted α-power law model [79] to represent the CMOS driver characteristics. Then, Brajesh et. al [21] proposed the transmission line model with α-power law model for DIL system to analyze the dynamic in-phase and out-phase delay in coupled lines.

These models that are purely limited to two coupled interconnect lines based on even-odd modes are reported in [20]–[22]. The modeling of CMOS driver based distributed RLC lines suffer from time/frequency domain conversion problem. This problem arises because the CMOS driver is modeled in the time domain, whereas the partial differential equations are used to solve the transmission lines model in the frequency domain. Therefore, many researchers substitute the nonlinear CMOS driver with a linear resistive driver compromising the overall accuracy of the model. In the recent past, the transmission line equations in time domain are solved using the FDTD method [24] to avoid the conversion problem.

2.3.2 On-chip interconnect modeling based on FDTD method

The FDTD method is a suitable numerical approach for computational EM modeling. Initially, this method was developed by K. S. Yee [80] to solve Maxwell's equations in the time domain by discretizing the time-dependent PDEs in time and space considering central difference schemes. Later in 1994, C. R. Paul [81] analyzed multiconductor TLs by incorporating lumped boundary conditions into the FDTD method. Then, this work was extended to ana-

lyze the lossy TLs by J. A. Roden et al. [82]. Similarly, Li et al. [83] presented accurate numerical FDTD method for the analysis of the transient response of a single TL driven by CMOS inverter driver, which exhibits better accuracy with respect to SPICE simulation results. Therefore, the FDTD method with better accuracy has attracted many researchers to analyze the signal integrity issues in high-speed interconnects.

Li et al. [24] proposed FDTD-based model for the analysis of the transient response of CMOS-gate driven coupled RLGC interconnects at 180 nm technology node. This work presents the FDTD model with a second-order accuracy to solve Telegraphers equations, for analysis of coupled interconnects and the non-linear behavior of the CMOS-gates is modeled using α-power law model. Sharma et al. [84] adopted the FDTD method for both dynamic and functional crosstalk analysis in lossy RLC interconnects. The authors validated the computed results with respect to HSPICE simulations. But they considered the linear resistive driver to drive the interconnects. In [85], they have studied the effect of coupling parasitics on propagation delay and coupling noise in the coupled RLC lines.

Recently, Kumar et al. [86] developed an FDTD model for accurate analysis of dynamic crosstalk in CMOS-gate driven coupled on-chip Cu interconnects at 130 nm technology node. And the CMOS gate was represented using α-power law model. However, α-power law model becomes imprecise as the technology scales down below 180 nm, as the finite drain conductance parameter (λ_d) is ignored in the α-power law model. Therefore, in [87] they proposed the FDTD scheme for the analysis of on-chip Cu interconnects at 32 nm technology node, which uses the n-th-power law model [88] to represent the CMOS driver. The n-th-power law model is more accurate as it includes the λ_d and velocity saturation effect. Later on, Kumar et al. analyzed the inclusive crosstalk noise of coupled MWCNT interconnects driven by linear resistive driver [89] and the same is extended to CMOS driver [90] considering modified α-power law model. They developed a modified α-power law model such that the effect of λ_d is included. Further, they applied the same to MLGNR interconnects [91].

Similarly, Agarwal et al. [92] proposed an accurate model based on the FDTD model to analyze the crosstalk noise effects in current-mode signaling (CMS) and voltage-mode signaling (VMS) coupled on-chip interconnects at 32 nm technology node. They represented non-linear characteristics of CMOS-gate with n-th-power law model. Later, the same is extended to MWCNT [93] and MLGNR [94] interconnects. Recently, Amit et al. [95] adopted the FDTD method for transient analysis of crosstalk effects and temperature-dependent equivalent single conductor (ESC) modeling for mixed-carbon nanotube bundle (MCB) interconnects.

Many researchers considered the FDTD method as a significant numerical scheme for solving EM problems and PDEs owing to its better accuracy. However, the FDTD method with better accuracy causes a numerical dispersion error [49, 50] during the propagation along the discretization. Hence, there is an extensive requirement of a novel method with an advantage in dealing with numerical dispersion properties.

2.3.3 Review on Multiresolution time domain (MRTD) method

The multiresolution time domain (MRTD) scheme is a wavelet-based numerical method proposed by Krumpholz and Katehi [96], which provides an efficient model for computation of EM field. The numerical dispersion of the MRTD algorithm has shown great efficiency to approximate the most accurate solution with negligible error as compared to the conventional FDTD model. They have considered cubic spline Battle-Lemarie scaling and wavelet functions to derive the MRTD algorithm. The dispersion curves of the MRTD scheme based on Battle-Lemarie scaling function compared with ideal case and FDTD scheme are illustrated in Figure 2.5. Tentzeris et al. [50] performed stability and dispersion analysis of MRTD algorithm based on Battle-Lemarie scaling function for zero-resolution wavelets and different stencil sizes.

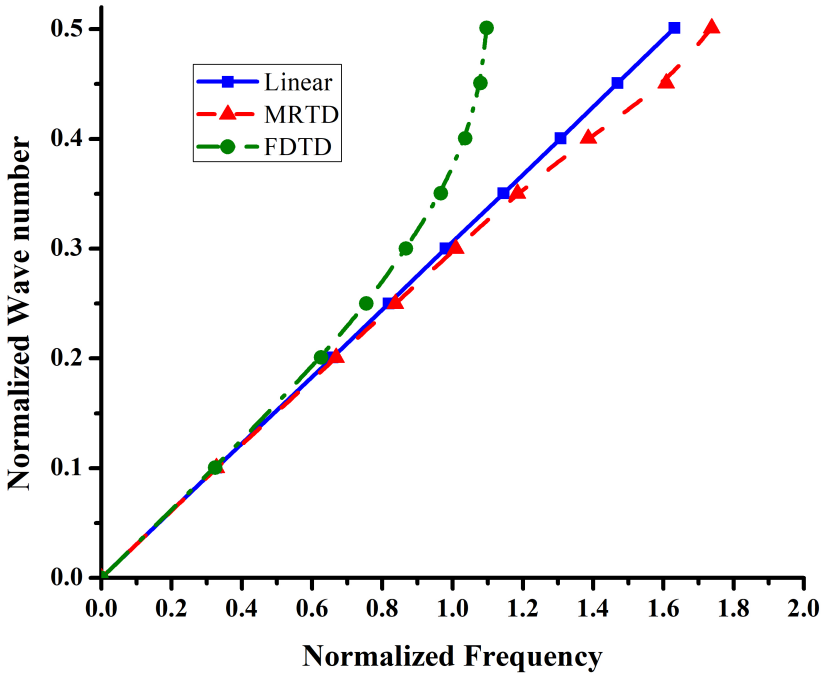


Figure 2.5: Dispersion curves of the MRTD scheme based on Battle-Lemarie scaling function and FDTD scheme with respect to ideal linear case [49]

In [97] and [98], the MRTD algorithm was derived considering Haar scaling and wavelet function to expand the EM field components in orthonormal bases. However, this model shows similar characteristics as the FDTD model. Fujii and Hoefer [99] expanded the MRTD model based on Daubechies' wavelet with two vanishing moments [100] to three and four vanishing moments for time-domain EM field modeling. Later on, other researchers used different scaling and wavelet functions such as Cohen–Daubechies–Feauveau (CDF) biorthogonal [101] and Coifman [102, 103] scaling functions to present dispersion analysis, as a solution to scattering problems, etc.

Recently, Tong et al [104] developed the MRTD model for the two-conductor lossless and lossy TL equations based on Daubechies' scaling functions. They performed stability and numerical dispersion analysis of this model which made evident that the developed model show better dispersion characteristics than the conventional FDTD model. Moreover, considering the high vanishing moment of the scaling function provides more accurate results. Later they extended their work to multiconductor TLs terminated with linear loads [105].

2.4 Summary

In this chapter, the interconnect electrical parameters extraction and the previous works done based on SPICE, analytical, and numerical methods in the area of on-chip interconnect modeling have been discussed. It provides the issues identified in the existing on-chip interconnect modeling techniques and the framework for the research work in the thesis.

Chapter 3

Signal Integrity Analysis of Resistive Driven Coupled Cu Interconnects using MRTD

In this chapter an attempt is made to derive an MRTD model for analyzing the effects of coupling parasitics on delay and crosstalk noise in the coupled interconnect lines driven by the linear resistive driver.

3.1 Introduction

In the current era of DSM technology, the high wire density at high clock frequencies results in significant coupling parasitics. Due to multiple effects of the parasitics, the circuit performance is severely affected [106]. With growing number of long on-chip interconnects and high operating frequencies, the role of mutual inductance (M_{12}) and coupling capacitance (C_{12}) on the performance are quite significant. One of the major factors on which the coupling parasitics depends is the switching pattern of inputs [107]. In the multilayer structure, the effect of coupling capacitance is restricted to adjacent layers and wires, whereas the mutual inductance is not just restricted to the adjacent layers and wires, and its influence extends to all parallel wires. These coupling parasitics lead to propagation delay and crosstalk noise, which forms a bottleneck in the transmission of high-speed signals [108].

The signal integrity affected by the crosstalk noise results in logic malfunctions or critical delays. The crosstalk induced peak can cause a logic error and false switching [22]. In high-speed interconnects, an accurate estimation of noise/delay is dependent on interconnect parasitics per unit length. Therefore, neglecting either M_{12} or C_{12} will result in an inaccurate noise/delay estimation.

3.2 Development of the proposed MRTD model

The MRTD model is the adaptive alternative to the FDTD method based on wavelets. This section deals with the implementation of the MRTD model, using Daubechies' scaling function as the basis function for analysing two coupled Cu interconnects driven by the linear resistor. Figure 3.1 shows the schematic of DIL system of two coupled Cu interconnects, where R_x is line resistance per unit length (p.u.l.), L_x is line inductance p.u.l., C_x is line capacitance p.u.l., C_{L1} and C_{L2} are load capacitances, R_{D1} and R_{D2} are driver resistances of line1 at x=1 and line2 at x=2, respectively. M_{12} is p.u.l. mutual inductance and C_{12} is p.u.l. coupling capacitance.

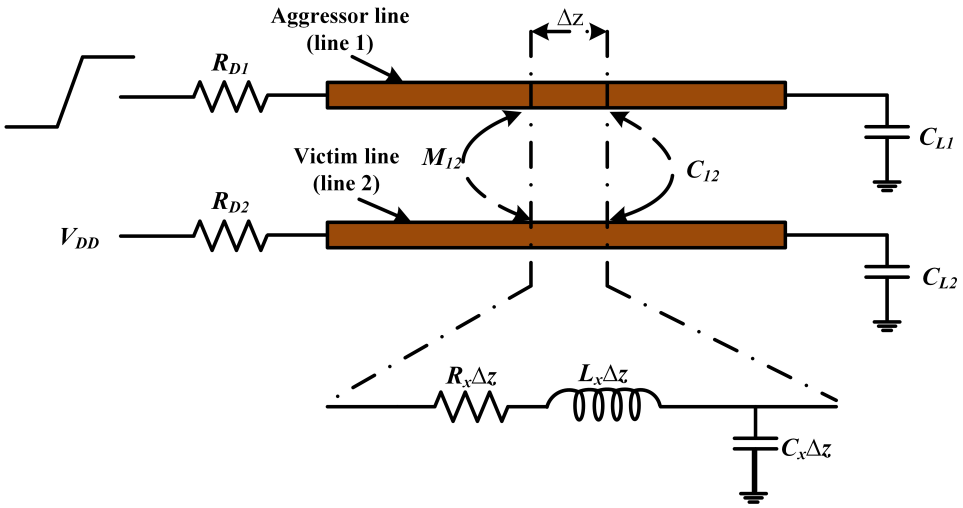


Figure 3.1: DIL system for coupled Cu interconnects

The coupled interconnect lines are considered as TLs which are described by telegrapher's equation [81] as

$$\frac{\partial \mathbf{V}(z,t)}{\partial z} + \mathbf{R}\mathbf{I}(z,t) + \mathbf{L}\frac{\partial \mathbf{I}(z,t)}{\partial t} = 0 \tag{3.1a}$$

$$\frac{\partial \mathbf{I}(z,t)}{\partial z} + \mathbf{C}\frac{\partial \mathbf{V}(z,t)}{\partial t} = 0 \tag{3.1b}$$

where the voltages ($\mathbf{V}$) and currents ($\mathbf{I}$) are expressed in 2x1 column vectors and line parasitics are represented in 2x2 matrices per unit length as shown below.

$$\mathbf{V} = \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}, \mathbf{I} = \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}, \mathbf{R} = \begin{bmatrix} R_1 & 0 \\ 0 & R_2 \end{bmatrix}, \mathbf{L} = \begin{bmatrix} L_1 & L_{12} \\ L_{12} & L_2 \end{bmatrix}, \mathbf{C} = \begin{bmatrix} C_1 + C_{12} & -C_{12} \\ -C_{12} & C_2 + C_{12} \end{bmatrix}$$

The accuracy and stability of the MRTD method for solving telegrapher's equations is achieved by considering the voltages and currents which are separated by $\frac{\Delta z}{2}$ in space and $\frac{\Delta t}{2}$ in time as shown in Figure 3.2, where Δz is the space discretization interval and Δt is the time discretization interval. Figure 3.2 is similar to the relation between the discretizations of space and time of the FDTD scheme. However, due to the different voltage/current expansions, the voltage/current components in the two methods are not identical.

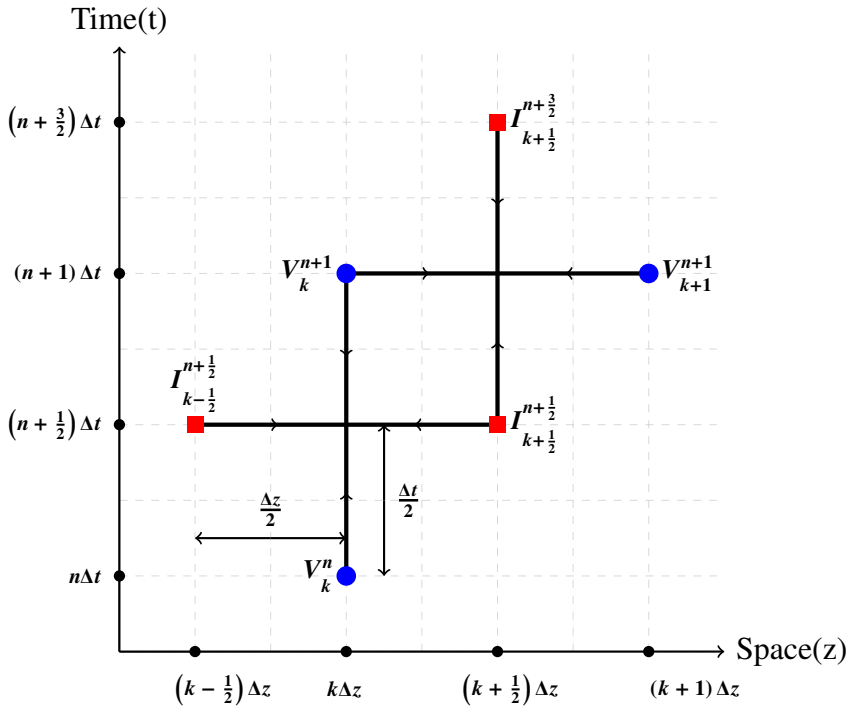


Figure 3.2: Relation between discretizations of space and time.

The interconnect line of length l is driven by a linear resistor and terminated by a capacitive load at $z = 0$ and $z = l$, respectively. The line is divided uniformly into Nz segments of length $\Delta z = \frac{l}{Nz}$, representing the discretized voltage and current nodes which are unknown coefficients as shown in Figure 3.3, where I_0 represent source current.

To solve (3.1a) and (3.1b), the voltage and current terms can be expanded using the known functions ($\phi_k(z)$ and $h_n(t)$) and the unknown coefficients following the method outlined in [96] as,

$$V(z,t) = \sum_{k,n=-\infty}^{+\infty} V_k^n \phi_k(z)\, h_n(t) \tag{3.2a}$$

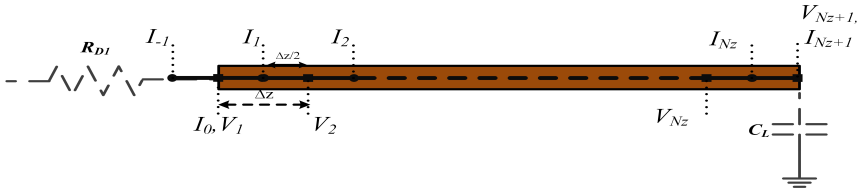


Figure 3.3: Spatial discretization of interconnect line for MRTD technique

$$I(z,t) = \sum_{k,n=-\infty}^{+\infty} I_{k+\frac{1}{2}}^{n+\frac{1}{2}} \phi_{k+\frac{1}{2}}(z)\, h_{n+\frac{1}{2}}(t) \tag{3.2b}$$

Where, V_k^n and $I_{k+\frac{1}{2}}^{n+\frac{1}{2}}$ are the coefficients for the expansion of the **V** and **I**, respectively, in terms of scaling functions. The indices n and k are indicated by temporally and spatially discretized indices relating to time and space coordinates by means of $t = n\Delta t$ and $z = k\Delta z$, respectively. The function $h_n(t)$ is defined as:

$$h_n(t) = h\left(\frac{t}{\Delta t} - n\right) \tag{3.3}$$

where $h(t)$ is a pulse function given as

$$h(t) = \begin{cases} 1 & for\,|t| < \frac{1}{2} \\ \frac{1}{2} & for\,|t| = \frac{1}{2} \\ 0 & for\,|t| > \frac{1}{2} \end{cases} \tag{3.4}$$

The function $\phi_k(z)$ is defined as

$$\phi_k(z) = \phi\left(\frac{z}{\Delta z} - k\right) \tag{3.5}$$

where $\phi(z)$ represents Daubechies' scaling function.

To derive the MRTD method for (3.1a) and (3.1b), we need the following equations ((3.6a)-(3.7b)) [109]:

$$\langle h_n(t), h_{n'}(t)\rangle = \delta_{n,n'}\Delta t \tag{3.6a}$$

$$\left\langle h_n(t), \frac{\partial h_{n'+\frac{1}{2}}(t)}{\partial t}\right\rangle = \delta_{n,n'} - \delta_{n,n'+1} \tag{3.6b}$$

$$\langle \phi_k(z), \phi_{k'}(z)\rangle = \delta_{k,k'}\Delta z \tag{3.7a}$$

$$\left\langle \phi_k(z), \frac{\partial \phi_{k'+\frac{1}{2}}(z)}{\partial z}\right\rangle = \sum_{i=-S_b}^{S_b-1} a(i)\,\delta_{k+i,k'} \tag{3.7b}$$

where $\delta_{n,n'}$, $\delta_{k,k'}$ represents the Kronecker symbol, S_b in (3.7b) denotes the effective support size of the basis functions. The coefficients $a(i)$ are called connection coefficients and can be computed using (3.8). Detailed derivation of the expressions (3.7a) and (3.7b) are presented in Appendix A. By considering Daubechies' scaling function having four vanishing moments (D_4) as the basis functions, Table 3.1 demonstrates the values of $a(i)$ for $1 \leq i \leq S_b$. The values of $a(i)$ for $i < 1$ can be obtained by using a symmetry relation $a(-1-i) = -a(i)$ and for $i > S_b \Rightarrow a(i) = 0$.

$$a(i) = \frac{1}{\pi} \int_0^\infty \left|\hat{\phi}(\lambda)\right|^2 \lambda sin\lambda \left(i + \frac{1}{2}\right) d\lambda \tag{3.8}$$

where $\hat{\phi}(\lambda)$ represents the Fourier transform of a scaling function $\phi(z)$.

Table 3.1: Connection coefficients $a(i)$ of Daubechies' scaling functions (D_4) [99].

i	**Connection Coeff. of** D_4
1	1.3110340773
2	-0.1560100110
3	0.0419957460
4	-0.0086543236
5	0.0008308695
6	0.0000108999
7	0.0000000041

Implementing the Galerkin method [96] with the test functions $\phi_{k+\frac{1}{2}}(z)\, h_n(t)$ and $\phi_k(z)\, h_{n+\frac{1}{2}}(t)$ to (3.1a) and (3.1b), respectively, the current and voltage iterative equations are obtained as:

$$I_{k+\frac{1}{2}}^{n+\frac{3}{2}} = B_1 I_{k+\frac{1}{2}}^{n+\frac{1}{2}} - B_2 \frac{\Delta t}{\Delta z} L^{-1} \sum_{i=1}^{S_b} a(i) \left(V_{k+i}^n - V_{k-i+1}^n\right) \tag{3.9a}$$

$$V_k^{n+1} = V_k^n - \frac{\Delta t}{\Delta z} C^{-1} \sum_{i=1}^{S_b} a(i) \left(I_{k+i-\frac{1}{2}}^{n+\frac{1}{2}} - I_{k-i+\frac{1}{2}}^{n+\frac{1}{2}}\right) \tag{3.9b}$$

Where

$$B_1 = \left(1 + \tfrac{\Delta t}{2} R L^{-1}\right)^{-1} \left(1 - \tfrac{\Delta t}{2} R L^{-1}\right)$$

$$B_2 = \left(1 + \tfrac{\Delta t}{2} R L^{-1}\right)^{-1}$$

In the iterative equations (3.9a) and (3.9b), not only the near-end boundary voltage V_1^{n+1} and far-end boundary voltage V_{Nz+1}^{n+1} are derived but also the iterative equations of the voltages and currents near the boundaries also need to be updated. Near the boundaries the voltages are represented by V_i^{n+1} and $V_{Nz+1-i}^{n+1}$for $i = 2, 3, \cdots, S_b$ and the currents by $I_{i+\frac{1}{2}}^{n+\frac{1}{2}}$ and $I_{Nz+1-i+\frac{1}{2}}^{n+\frac{1}{2}}$ $i = 1, 2, 3, \cdots, S_b - 1$. All these voltages and currents have some terms that exceed the index range in iterative equations (3.9a) and (3.9b).

For updating the iterative equations of voltages and currents, (3.9a) and (3.9b) need to be decomposed using the relation in [101], which satisfies the coefficients $a(i)$ given by

$$\sum_{i=1}^{S_b}(2i-1)a(i) = 1 \tag{3.10}$$

substituting (3.10) into (3.9b), we obtain

$$\sum_{i=1}^{S_b}(2i-1)\,a\,(i)\,V_k^{n+1} = \sum_{i=1}^{S_b}(2i-1)\,a\,(i)\,V_k^n - \sum_{i=1}^{S_b}\frac{\Delta t}{(2i-1)\,\Delta z}C^{-1}\left[(2i-1)\,a\,(i)\left(I_{k+i-\frac{1}{2}}^{n+\frac{1}{2}} - I_{k-i+\frac{1}{2}}^{n+\frac{1}{2}}\right)\right] \tag{3.11}$$

Considering the corresponding terms with i, (3.9b) can be decomposed as

$$(2i-1)\,a\,(i)\,V_k^{n+1} = (2i-1)\,a\,(i)\,V_k^n - (2i-1)\,a\,(i)\,\frac{\Delta t}{(2i-1)\,\Delta z}C^{-1}\left(I_{k+i-\frac{1}{2}}^{n+\frac{1}{2}} - I_{k-i+\frac{1}{2}}^{n+\frac{1}{2}}\right) \tag{3.12}$$

$$\text{for } i = 1, 2, 3, \cdots, S_b$$

3.2.1 Near-end terminal

The voltage and current node points at the near end terminal are represented by V_1 and I_0, respectively, where the nodal equation at the terminal is given by

$$V_s^n = R_D I_0 + V_1^n \tag{3.13}$$

At $k = 1$, the iterative equation of near end terminal voltage is given by

$$V_1^{n+1} = V_1^n - \frac{\Delta t}{\Delta z}C^{-1}\sum_{i=1}^{S_b}a\,(i)\left(I_{i+\frac{1}{2}}^{n+\frac{1}{2}} - I_{-i+\frac{3}{2}}^{n+\frac{1}{2}}\right) \tag{3.14}$$

Following the steps of (3.11) and (3.12), we can decompose (3.14) as

$$a\,(1)\,V_1^{n+1} = a\,(1)\,V_1^n - a\,(1)\,\frac{\Delta t}{\Delta z}C^{-1}\left(I_{\frac{3}{2}}^{n+\frac{1}{2}} - I_{\frac{1}{2}}^{n+\frac{1}{2}}\right) \tag{3.15a}$$

$$3a\left(2\right)V_1^{n+1} = 3a\left(2\right)V_1^n - 3a\left(2\right)\frac{\Delta t}{3\Delta z}C^{-1}\left(I_{\frac{5}{2}}^{n+\frac{1}{2}} - I_{-\frac{1}{2}}^{n+\frac{1}{2}}\right) \tag{3.15b}$$

$$\vdots$$

$$\left(2S_b-1\right)a\left(S_b\right)V_1^{n+1} = \left(2S_b-1\right)a\left(S_b\right)V_1^n - \left(2S_b-1\right)a\left(S_b\right)\frac{\Delta t}{\left(2S_b-1\right)\Delta z}C^{-1}\left(I_{S_b+\frac{1}{2}}^{n+\frac{1}{2}} - I_{-S_b+\frac{3}{2}}^{n+\frac{1}{2}}\right) \tag{3.15c}$$

Here, the iterative equations (3.15a), (3.15b) .... (3.15c) can be considered as the central difference equations. In these equations, the subscripts of the terms $I_{-\frac{1}{2}}^{n+\frac{1}{2}}, I_{-\frac{3}{2}}^{n+\frac{1}{2}}, \cdots, I_{-S_b+\frac{3}{2}}^{n+\frac{1}{2}}$ exceed the index range. To overcome this problem, forward difference approach is used to replace the central difference approach. Thus the iterative equations are obtained by keeping the weight coefficients unchanged in each equation :

$$a\left(1\right)V_1^{n+1} = a\left(1\right)V_1^n - a\left(1\right)\frac{\Delta t}{\Delta z}C^{-1}\left(I_{\frac{3}{2}}^{n+\frac{1}{2}} - I_0^{n+\frac{1}{2}}\right) \tag{3.16a}$$

$$3a\left(2\right)V_1^{n+1} = 3a\left(2\right)V_1^n - 3a\left(2\right)\frac{\Delta t}{3\Delta z}C^{-1}\left(I_{\frac{5}{2}}^{n+\frac{1}{2}} - I_0^{n+\frac{1}{2}}\right) \tag{3.16b}$$

$$\vdots$$

$$\left(2S_b-1\right)a\left(S_b\right)V_1^{n+1} = \left(2S_b-1\right)a\left(S_b\right)V_1^n - \left(2S_b-1\right)a\left(S_b\right)\frac{\Delta t}{\left(2S_b-1\right)\Delta z}C^{-1}\left(I_{S_b+\frac{1}{2}}^{n+\frac{1}{2}} - I_0^{n+\frac{1}{2}}\right) \tag{3.16c}$$

From the above equations (3.16a), (3.16b) .... (3.16c) the iterative equation of near-end boundary node voltage V_1^{n+1} is given by

$$V_1^{n+1} = V_1^n - \frac{\Delta t}{\Delta z}C^{-1}\sum_{i=1}^{S_b}2a\left(i\right)\left(I_{i+\frac{1}{2}}^{n+\frac{1}{2}} - I_0^{n+\frac{1}{2}}\right) \tag{3.17}$$

In (3.17), by substituting $I_0^{n+\frac{1}{2}} = \frac{I_0^n + I_0^{n+1}}{2}$ and modifying the equation (3.13) as $I_0^n = \frac{V_s^n - V_1^n}{R_D}$, we obtain (3.17) as

$$V_1^{n+1} = A_1\left(A_2V_1^n - R_D\sum_{i=1}^{S_b}2a\left(i\right)I_{i+\frac{1}{2}}^{n+\frac{1}{2}} + \sum_{i=1}^{S_b}a\left(i\right)\left(V_s^{n+1} + V_s^n\right)\right) \tag{3.18}$$

where,

$$A_1 = \left(\frac{\Delta z}{\Delta t}CR_D + \sum_{i=1}^{S_b}a\left(i\right)\right)^{-1}$$

$$A_2 = \left(\frac{\Delta z}{\Delta t} C R_D - \sum_{i=1}^{S_b} a\,(i)\right)$$

3.2.2 Far-end terminal

At $k = Nz + 1$, following the steps from Section 3.2.1, the iterative equations at the far-end boundary are obtained. The output current I_{Nz+1} of the capacitive load is given by

$$I_{Nz+1} = C_L \frac{dV_{Nz+1}}{dt} \tag{3.19}$$

The final iterative equation at the far-end terminal is given by

$$V_{Nz+1}^{n+1} = V_{Nz+1}^{n} - D_1 D_2 \left(\sum_{i=1}^{S_b} a\,(i)\, I_{Nz+1}^{n+\frac{1}{2}} - \sum_{i=1}^{S_b} 2a\,(i)\, I_{Nz+1-i+\frac{1}{2}}^{n+\frac{1}{2}} \right) \tag{3.20}$$

where,

$$D_1 = \left(1 + \frac{C_L}{\Delta z} C^{-1} \sum_{i=1}^{S_b} a\,(i)\right)$$

$$D_2 = \frac{\Delta t}{\Delta z} C^{-1}$$

In continuation with the algorithm, to derive and update the iterative equations, which have some terms whose indices exceed the index range for all nodes between the terminals, a truncation method is used.

Taking V_k^{n+1} as an example for $k = 2, 3, \cdots, S_b$ and following the steps of (3.11) and (3.12), we can decompose (3.9b) as

$$a\,(1)\, V_k^{n+1} = a\,(1)\, V_k^{n} - a\,(1)\, \frac{\Delta t}{\Delta z} C^{-1} \left(I_{k+\frac{1}{2}}^{n+\frac{1}{2}} - I_{k-\frac{1}{2}}^{n+\frac{1}{2}} \right) \tag{3.21a}$$

$$3a\,(2)\, V_k^{n+1} = 3a\,(2)\, V_k^{n} - 3a\,(2)\, \frac{\Delta t}{3\Delta z} C^{-1} \left(I_{k+\frac{3}{2}}^{n+\frac{1}{2}} - I_{k-\frac{3}{2}}^{n+\frac{1}{2}} \right) \tag{3.21b}$$

$$\vdots$$

$$(2k-3)\, a\,(k-1)\, V_k^{n+1} = (2k-3)\, a\,(k-1)\, V_k^{n} - (2k-3)\, a\,(k-1)\, \frac{\Delta t}{(2k-3)\,\Delta z} C^{-1} \left(I_{2k-\frac{3}{2}}^{n+\frac{1}{2}} - I_{1+\frac{1}{2}}^{n+\frac{1}{2}} \right) \tag{3.21c}$$

$$(2k-1)\,a(k)\,V_k^{n+1} = (2k-1)\,a(k)\,V_k^n - (2k-1)\,a(k)\,\frac{\Delta t}{(2k-1)\,\Delta z}C^{-1}\left(I_{2k-\frac{1}{2}}^{n+\frac{1}{2}} - I_{\frac{1}{2}}^{n+\frac{1}{2}}\right) \quad (3.21d)$$

$$(2k+1)\,a(k+1)\,V_k^{n+1} = (2k+1)\,a(k+1)\,V_k^n - (2k+1)\,a(k+1)\,\frac{\Delta t}{(2k+1)\,\Delta z}C^{-1}\left(I_{2k+\frac{1}{2}}^{n+\frac{1}{2}} - I_{-\frac{1}{2}}^{n+\frac{1}{2}}\right) \quad (3.21e)$$

$$\vdots$$

$$(2S_b-1)\,a(S_b)\,V_k^{n+1} = (2S_b-1)\,a(S_b)\,V_k^n - (2S_b-1)\,a(S_b)\,\frac{\Delta t}{(2S_b-1)\,\Delta z}C^{-1}\left(I_{k+S_b-\frac{1}{2}}^{n+\frac{1}{2}} - I_{k-S_b+\frac{1}{2}}^{n+\frac{1}{2}}\right) \quad (3.21f)$$

From the equations (3.21a)−(3.21f), it can be observed that for the first k terms, the indices of the equations doesn't exceed the index range, whereas, all the equations for which the index terms exceed the index range appear in the rest $S_b - k$ terms. As $S_b - k$ terms go out-of-bounds, these equations are unavailable for forming iterative equations in MRTD method. To avoid this problem, a truncation is made in the equations where the index range is exceeding.

By summing up the first k terms in equation (3.21a)−(3.21f), we can obtain the modified iterative equations for $k = 2, 3, \cdots, S_b$

$$V_k^{n+1} = V_k^n - \left(\sum_{i=1}^{k}(2i-1)\,a(i)\right)^{-1} D_2\left(\sum_{i=1}^{k} a(i)\left(I_{k+i-\frac{1}{2}}^{n+\frac{1}{2}} - I_{k-i+\frac{1}{2}}^{n+\frac{1}{2}}\right)\right) \quad (3.22)$$

Using the same steps illustrated in (3.21a)−(3.21f), we obtain modified iterative equations of voltages at interior points as shown in (3.23) and voltages near the load as shown in (3.24).

for $k = S_b + 1, S_b + 2, \cdots, Nz - S_b, Nz - S_b + 1$

$$V_k^{n+1} = V_k^n - D_2\left(\sum_{i=1}^{S_b} a(i)\left(I_{k+i-\frac{1}{2}}^{n+\frac{1}{2}} - I_{k-i+\frac{1}{2}}^{n+\frac{1}{2}}\right)\right) \quad (3.23)$$

for $k = Nz - S_b + 2, Nz - S_b + 3, \cdots, Nz$

$$V_k^{n+1} = V_k^n - \left(\sum_{i=1}^{Nz-k+1}(2i-1)\,a(i)\right)^{-1} D_2\left(\sum_{i=1}^{Nz-k+1} a(i)\left(I_{k+i-\frac{1}{2}}^{n+\frac{1}{2}} - I_{k-i+\frac{1}{2}}^{n+\frac{1}{2}}\right)\right) \quad (3.24)$$

The iterative equations of current can be updated by following the same steps of voltage iterative equations with a slight difference. As shown in Figure 3.3, it is observed that the

current nodes appear at the half-integer points, which means that all the currents are located at the interior points of terminals. So, the currents near the terminals need to be modified.

For the iterative equations of current near the terminals, we need to decompose (3.9a) by using the steps from voltage iterative equations. The final modified current iterative equations are obtained as

for $k = 1$, near the source

$$I_{1+\frac{1}{2}}^{n+\frac{3}{2}} = B_1 I_{1+\frac{1}{2}}^{n+\frac{1}{2}} - B_2 \frac{\Delta t}{\Delta z} L^{-1} \left(\sum_{i=1}^{S_b} a(i) \left(V_{i+1}^{n+1} - V_1^{n+1} \right) \right) \tag{3.25}$$

for $k = 2, 3, \cdots, S_b$

$$I_{k+\frac{1}{2}}^{n+\frac{3}{2}} = B_1 I_{k+\frac{1}{2}}^{n+\frac{1}{2}} - B_2 \left(\sum_{i=1}^{k} (2i-1)\, a(i) \right)^{-1} \frac{\Delta t}{\Delta z} L^{-1} \left(\sum_{i=1}^{k} a(i) \left(V_{k+i}^{n+1} - V_{k-i+1}^{n+1} \right) \right) \tag{3.26}$$

for $k = S_b + 1, S_b + 2, \cdots, Nz - S_b, Nz - S_b + 1$, iterative equations at interior points are

$$I_{k+\frac{1}{2}}^{n+\frac{3}{2}} = B_1 I_{k+\frac{1}{2}}^{n+\frac{1}{2}} - B_2 \frac{\Delta t}{\Delta z} L^{-1} \left(\sum_{i=1}^{S_b} a(i) \left(V_{k+i}^{n+1} - V_{k-i+1}^{n+1} \right) \right) \tag{3.27}$$

for $k = Nz - S_b + 2, Nz - S_b + 3, \cdots, Nz$, iterative equations near the load are

$$I_{k+\frac{1}{2}}^{n+\frac{3}{2}} = B_1 I_{k+\frac{1}{2}}^{n+\frac{1}{2}} - B_2 \left(\sum_{i=1}^{Nz-k+1} (2i-1)\, a(i) \right)^{-1} \frac{\Delta t}{\Delta z} L^{-1} \left(\sum_{i=1}^{Nz-k+1} a(i) \left(V_{k+i}^{n+1} - V_{k-i+1}^{n+1} \right) \right) \tag{3.28}$$

A bootstrapping approach is used for evaluating the updated voltage and current iterative equations. Foremost, the voltage iterative equations are solved at fixed time using (3.18), (3.20), (3.22), (3.23) and (3.24) in terms of past values of voltages and currents. Thereafter, the iterative equations of currents are solved from (3.25), (3.26), (3.27) and (3.28) in terms of voltages evaluated initially and form past values of currents. So, to get the stable output for the MRTD iterative equations, the Courant stability condition [101], [104] is considered as

$$\Delta t \leq \frac{q \Delta z}{\vartheta}$$

which amounts to the condition that the time step must be no greater than the propagation time over each cell. Here q is a Courant number given by $q = \frac{1}{\sum_{i=1}^{S_b}|a(i)|} = \frac{\vartheta\Delta t}{\Delta z}$ and ϑ is the phase velocity of propagation on the line.

3.3 Simulation setup

MRTD computations are carried out for the analysis of functional and dynamic crosstalk behaviour due to the coupling parasitics (M_{12} and C_{12}). The proposed model is validated using the W-element model in HSPICE. The simulation results obtained using HSPICE are compared with those of MRTD results. The functional crosstalk dependency is analyzed by considering the victim line at static low and switching the aggressor, whereas the dynamic crosstalk dependency behaviour is observed by switching the two lines simultaneously. The delay and crosstalk are measured at the far end of the line2.

To show the effects of coupling capacitance (C_{12}) and mutual inductance (M_{12}) on both delay and crosstalk noise, the signal integrity analysis is done with the global level interconnect length of 2 mm in 130 nm technology. Ramp signal is applied as input with a transition time of 50 ps. The thickness and width of the interconnect line are considered to be equal to the height from the ground plane and the space between the two interconnects, respectively. The relative permittivity of the interlayer dielectric medium is assumed to be 3.2. Using an aspect ratio of 1.5 and line width of 0.6 μm [86], the following line parasitic values are used for coupled-two interconnect lines. The load capacitance C_L is chosen as 10 fF.

$$R = \begin{bmatrix} 40 & 0 \\ 0 & 40 \end{bmatrix} k\Omega/m,\ L = \begin{bmatrix} 1.6775 & 1.422 \\ 1.422 & 1.6775 \end{bmatrix} \mu H/m,\ C = \begin{bmatrix} 121.57 & -78.78 \\ -78.78 & 121.57 \end{bmatrix} pF/m$$

For the DIL system, each CMOS driver is replaced by its equivalent linear resistor for the analysis.

3.4 Validation of the MRTD model and results

The proposed model is validated by considering the coupled two copper interconnect structure as shown in Figure 3.1. In the DIL system of Figure 3.1, line 1 is considered as

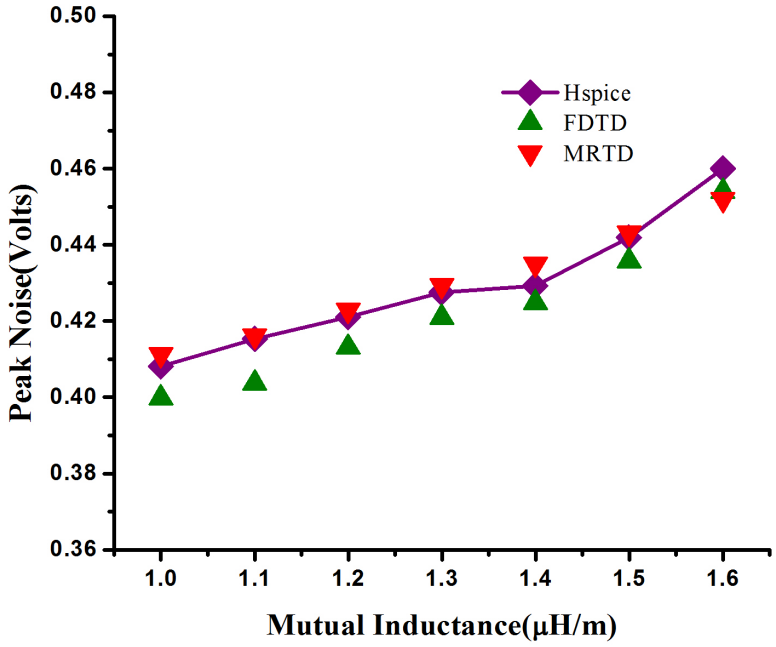


Figure 3.4: Dependency of crosstalk noise on mutual inductance

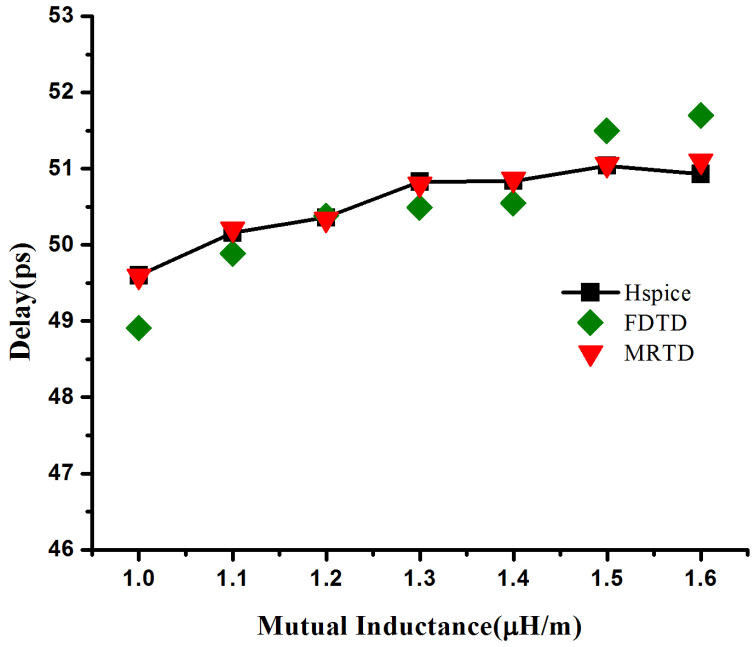


Figure 3.5: Dependency of in-phase delay on mutual inductance

aggressor and line 2 is considered as victim. The peak crosstalk voltage and propagation delay are measured at the far end terminal of victim line. Using the line parasitic values

from Section 3.3, the mode velocities for a lossless case are calculated as even mode velocity ($\vartheta_{m1} = 0.868\times10^{8} m/s$) and odd mode velocity ($\vartheta_{m2} = 1.397\times10^{8} m/s$). The space discretization (Δz) is computed by considering break frequency of $6.37\times10^{9} Hz$ and the even mode velocity as less than $13.626\times10^{-4} m$. The time discretization (Δt) is calculated by using the value of Δz and odd mode velocity for the Courant number $q = 0.7$ and is obtained as less than $6.8276\times10^{-12} s$.

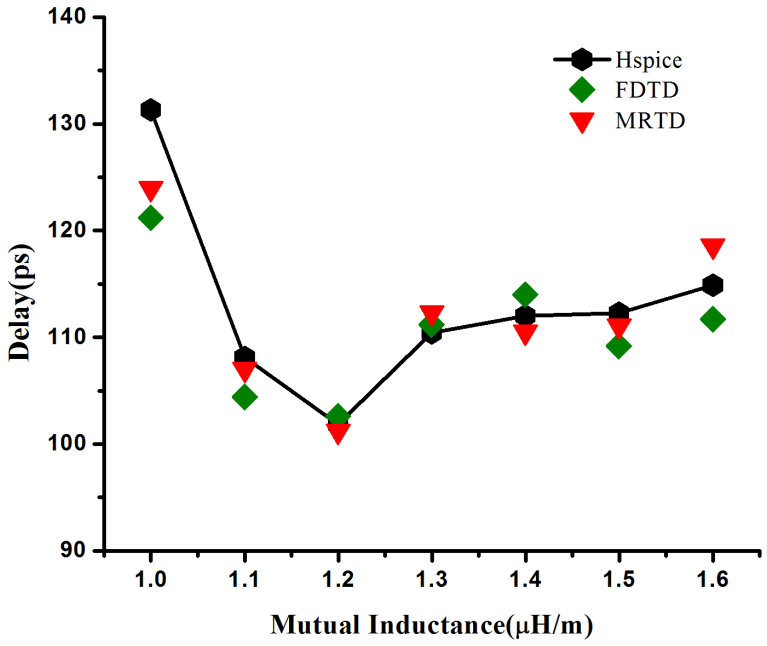


Figure 3.6: Dependency of out-phase delay on mutual inductance

The Mutual Inductance is varied from $(1-1.6)\mu H/m$ to capture its effect on the crosstalk noise and propagation delay. The crosstalk noise and propagation delay obtained from the proposed model and FDTD method are compared with HSPICE and are shown in Figs.3.4-3.6. The results show that the proposed model is in fine agreement with the HSPICE simulation and that it dominates over the FDTD method in terms of accuracy. In Figure 3.4 with the increase in mutual inductance the induced current increases leading to increase in peak noise voltage. Figure 3.5 shows that the in-phase delay increases with the mutual inductance, which is due to the fact that the effective inductance of the line increases with mutual inductance in the case of in-phase switching of inputs. From Figure 3.6 it is observed that the out-phase delay decreases with increase in mutual inductance since the mutual inductance introduces subtractive term of voltage in the case of out-phase switching.

Further, the HSPICE simulations are performed to validate the proposed model by capturing the effect of coupling capacitance on crosstalk noise and propagation delay. The effect of

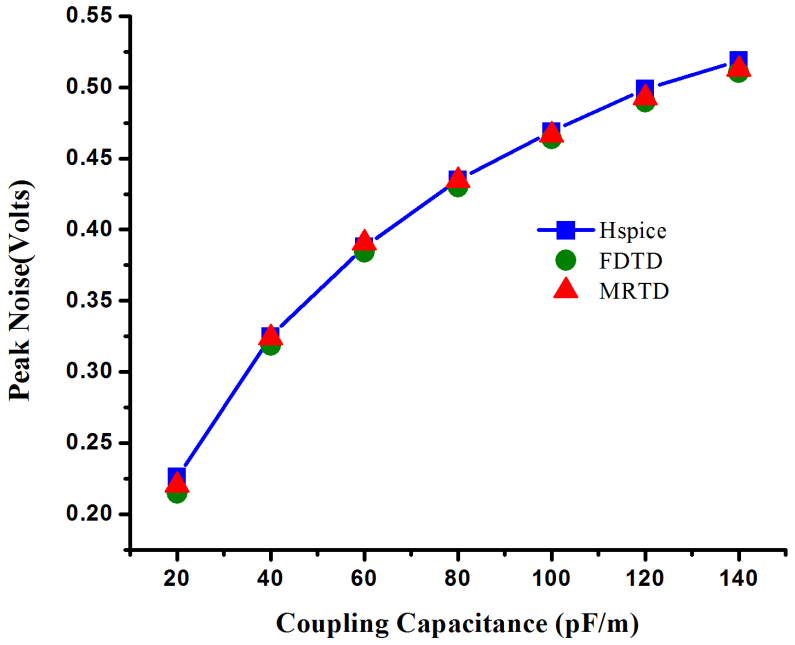


Figure 3.7: Variation of crosstalk noise as a function of coupling capacitance

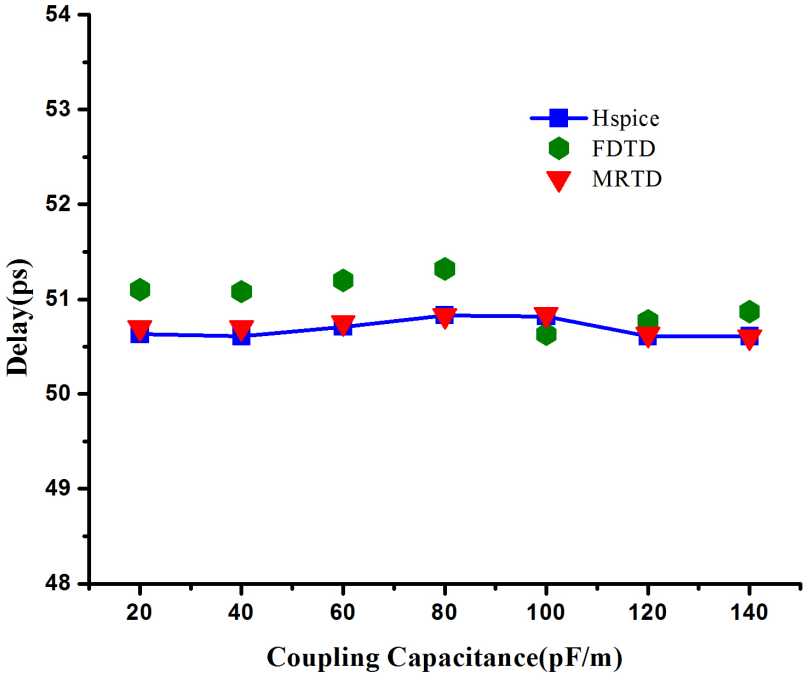


Figure 3.8: Variation of in-phase delay as a function of coupling capacitance

the coupling capacitance on peak noise, in-phase delay and out-phase delay are shown in Figure 3.7, Figure 3.8 and Figure 3.9, respectively. In Figure 3.7 with the increase in coupling capaci-

tance the effective capacitance increases when the victim line is at static low, thereby capacitive reactance decreases leading to increase the peak noise. From Figure 3.8 it is observed that, in-phase delay is almost uniform with increasing coupling capacitance since the effect of coupling capacitance is minimum for in-phase switching of lines. From Figure 3.9 it is observed that the out-phase delay increases with increasing coupling capacitance, since due to Miller effect, the coupling capacitance is effectively twice ($2C_{12}$) its original value.

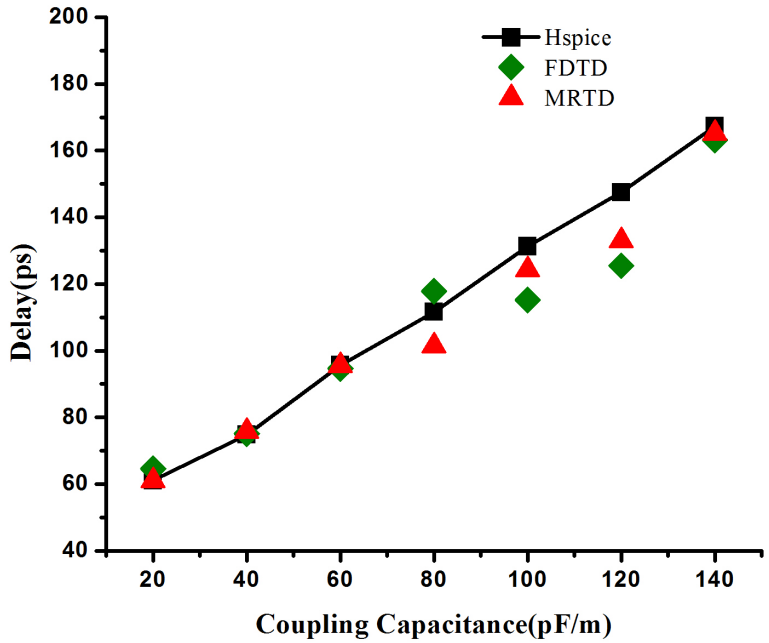


Figure 3.9: Variation of out-phase delay as a function of coupling capacitance

Table 3.2: Comparison of computational error involved in crosstalk noise due to the mutual inductance.

Mutual Inductance	**Peak Noise** (V)			**%error**	
$\mathbf{M_{12}}$(μH/m)	**HSPICE**	**Proposed**	**FDTD**	**Proposed**	**FDTD**
1	0.4082	0.4112	0.3998	-0.74	+2.06
1.1	0.4154	0.4161	0.4037	-0.17	+2.82
1.2	0.4211	0.4229	0.4131	-0.43	+1.89
1.3	0.42751	0.4294	0.4209	-0.44	+1.55
1.4	0.4273	0.4349	0.4248	-1.78	+0.60
1.5	0.441	0.4432	0.4358	-0.496	+1.18
1.6	0.460	0.452	0.454	+1.74	+1.304

Table 3.3: Comparison of computational error involved in crosstalk noise due to the coupling capacitance.

Coupling Capacitance	**Peak Noise** (V)			**%error**	
$\mathbf{C_{12}}$ (pF/m)	**HSPICE**	**Proposed**	**FDTD**	**Proposed**	**FDTD**
20	0.226	0.2203	0.215	+2.52	+4.86
40	0.325	0.3241	0.3187	+0.28	+1.94
60	0.388	0.3908	0.3841	-0.72	+1.01
80	0.435	0.4346	0.4297	+0.092	+1.22
100	0.469	0.4664	0.4639	+0.55	+1.087
120	0.499	0.4927	0.4897	+1.26	+1.86
140	0.519	0.5129	0.5103	+1.18	+1.68

Table 3.4: Comparison of Computational Efforts Between the Methods.

	Computational time (s)		
Methods / **No. of Coupled lines**	**HSPICE**	**MRTD**	**FDTD**
Two	$0.215 \approx 0.22$	$0.186 \approx 0.19$	$0.145 \approx 0.15$

The effect of varying mutual inductance and coupling capacitance on % error in peak cross talk noise is tabulated in Table 3.2 and Table 3.3, respectively. By varying coupling parasitics, FDTD method gives an average error of 1.79% and the proposed model gives an average error of 0.203% in peak crosstalk noise. Moreover, from the results, using MRTD method an average error of -0.64% in delay is observed for in-phase switching of inputs. Furthermore, by considering both in-phase as well as out-phase switching with varying coupling parasitics, an average error of 0.84% in delay is observed. Here, the MRTD model is giving more accurate results due to the better dispersion properties than FDTD method. It is also observed that the proposed MRTD algorithm estimates peak crosstalk noise and delay in close agreement with HSPICE results against variation in coupling parasitics.

The computational time for the HSPICE, the proposed MRTD and the FDTD model is measured using the Intel Core i7 processor - 3770 CPU@3.40 GHz. Table 3.4 shows the corresponding computational effort of each model. It is observed that the CPU run-time of HSPICE

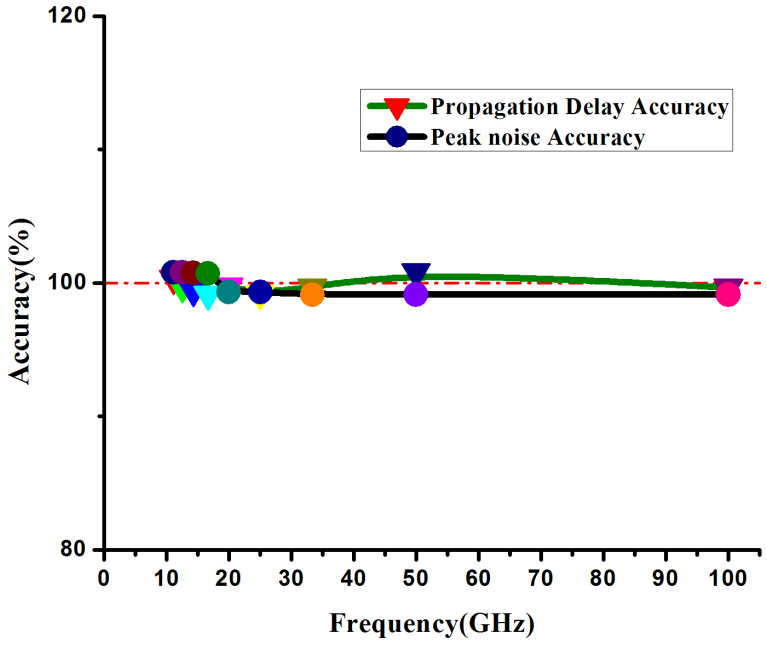


Figure 3.10: Effect of frequency on accuracy of the model

is higher than both MRTD and FDTD models, but MRTD is slightly slower than FDTD, due to increased number of iterations for better accuracy. Hence, there exists a trade-off between simulation time and accuracy.

Further, the impact of propagation delay and crosstalk noise on the accuracy of model for a range of frequencies is illustrated in the Figure 3.10. It is assured that approximately 100% accuracy is maintained for a broad frequency range although a slight perturbation does exist within a short range of frequencies.

3.5 Summary

In this chapter, multiresolution-time-domain method, employing Daubechies' scaling function with four vanishing moments is proposed to analyze 50% propagation delay and peak noise in the coupled driver-interconnect-load system.

Initially, the MRTD method is derived to solve telegraphers equations for copper interconnects by applying boundary conditions at near end terminal driven by a linear resistor and at far end terminal terminated by a load capacitance. Then, the crosstalk effects such as delay and

peak noise are analyzed with varying coupling parasitics. Further, the impact of delay and peak noise on the accuracy of the model for a range of frequencies is observed. The proposed MRTD model provides better accuracy as compared to conventional FDTD model.

Chapter 4

MRTD Model for the Analysis of Crosstalk in CMOS Driven Coupled Cu Interconnects

In this chapter, the non-linear characteristics of CMOS-gate driver are included employing n-th-power law model.

4.1 Introduction

With the evolution of deep sub-micron CMOS technology, the circuits in chips (SoCs) allow Giga-scale integration. In such circuits, the analysis of interconnects have become extremely important to determine the performance of a circuit such as power consumption and time delay. In addition to the delay, with the high operating frequencies, crosstalk is a pitfall in the design of interconnect structures for circuitry. As on-chip circuitry is gradually miniaturized, the adjacent interconnects are brought into closer proximity. Accordingly, the undesired signal coupling between the interconnects gets elevated [106]. So, the precise prediction of peak crosstalk noise and peak noise timing in a DIL system has become a critical design view for a long period [106].

For the analysis of the crosstalk noise, most of the earlier models have considered non-linear CMOS driver as a simple linear resistor [20] [23], which leads to a discrepancy in the

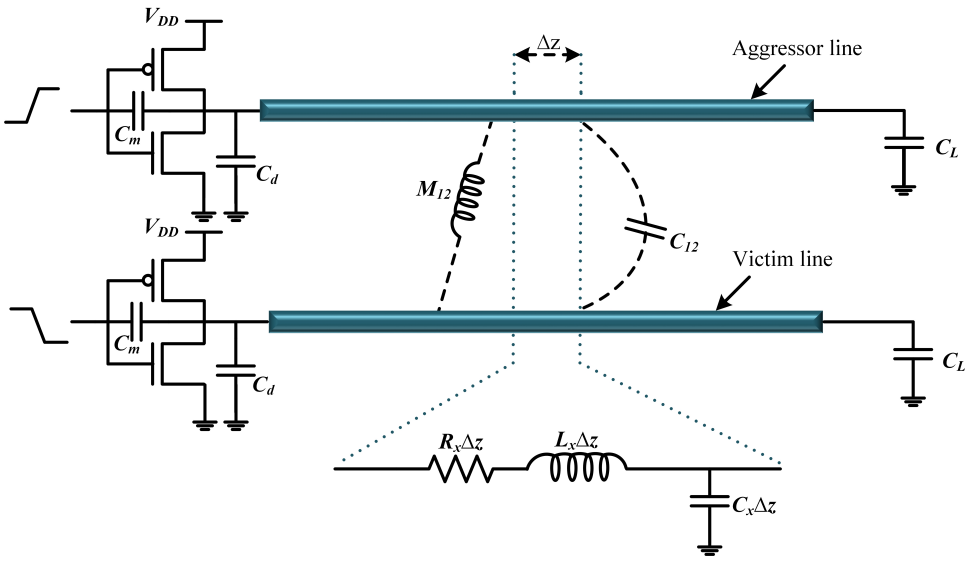


Figure 4.1: DIL system for CMOS driven coupled Cu interconnects.

results. Because, during the transient, MOSFET operates in saturation region about 50% of its operating time and rest of time in linear (or) cutoff regions [110].

4.2 Formulation of the MRTD Method

The proposed MRTD method is developed using Daubechies' scaling function as the basis function having four vanishing moments for coupled VLSI interconnects. In a more practical approach, CMOS drivers are considered for analyzing the performance more precisely. Capacitive loads are considered for the termination of interconnect lines. The schematic of the CMOS-driven coupled interconnect lines are shown in Figure 4.1. C_d and C_m are the parasitic capacitance of CMOS, where C_d represents drain diffusion capacitance and C_m represents gate-to-drain coupling capacitance.

Where R_x is the line resistance per unit length (p.u.l.), L_x is line inductance p.u.l. C_x is line capacitance p.u.l. The subscript 'x' represents aggressor line at x=1 and victim line at x=2. C_L is the load capacitance. The interconnect lines are coupled inductively M_{12} and capacitively C_{12}.

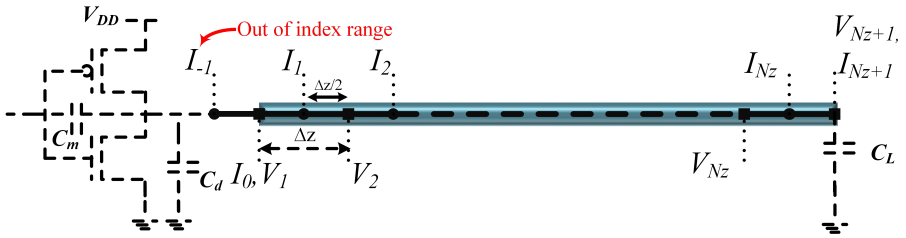


Figure 4.2: Spatial discretization of MRTD technique for DIL system.

4.2.1 Modeling of Coupled VLSI Interconnects

The coupled on-chip interconnects considered as distributed RLC transmission lines are described by telegrapher's equation [81].

$$\frac{\partial \mathbf{V}(z,t)}{\partial z} + \mathbf{R}\mathbf{I}(z,t) + \mathbf{L}\frac{\partial \mathbf{I}(z,t)}{\partial t} = 0 \tag{4.1a}$$

$$\frac{\partial \mathbf{I}(z,t)}{\partial z} + \mathbf{C}\frac{\partial \mathbf{V}(z,t)}{\partial t} = 0 \tag{4.1b}$$

where the voltages ($\mathbf{V}$) and currents ($\mathbf{I}$) are expressed in 2×1 column vector form $\begin{bmatrix} \mathrm{V}_1 & \mathrm{V}_2 \end{bmatrix}^{\mathrm{T}}$, $\begin{bmatrix} \mathrm{I}_1 & \mathrm{I}_2 \end{bmatrix}^{\mathrm{T}}$ and line parasitics are expressed in 2×2 matrices per unit length as shown below.

$$\mathbf{R} = \begin{bmatrix} \mathrm{R}_1 & 0 \\ 0 & \mathrm{R}_2 \end{bmatrix}, \mathbf{L} = \begin{bmatrix} \mathrm{L}_1 & \mathrm{M}_{12} \\ \mathrm{M}_{12} & \mathrm{L}_2 \end{bmatrix}, \mathbf{C} = \begin{bmatrix} \mathrm{C}_1 + \mathrm{C}_{12} & -\mathrm{C}_{12} \\ -\mathrm{C}_{12} & \mathrm{C}_2 + \mathrm{C}_{12} \end{bmatrix}$$

A CMOS driver drives the interconnect line of length l at $z = 0$ and capacitive load terminates it at $z = l$. The line is divided uniformly into Nz segments of length $\Delta z = \frac{l}{Nz}$, representing the discretized voltage and current nodes which are unknown coefficients as shown in Figure 4.2., where I_0 represents the source current.

Solving the equations (4.1a) and (4.1b) by using (3.2)-(3.7) produces exactly similar iterative equations of voltages and currents as in chapter 3 i.e., the equations (3.9)-(3.12).

$$I_{k+\frac{1}{2}}^{n+\frac{3}{2}} = B_1 I_{k+\frac{1}{2}}^{n+\frac{1}{2}} - B_2 \frac{\Delta t}{\Delta z} L^{-1} \sum_{i=1}^{S_b} a(i) \left(V_{k+i}^{n} - V_{k-i+1}^{n} \right). \tag{4.2a}$$

$$V_k^{n+1} = V_k^n - \frac{\Delta t}{\Delta z} C^{-1} \sum_{i=1}^{S_b} a(i) \left(I_{k+i-\frac{1}{2}}^{n+\frac{1}{2}} - I_{k-i+\frac{1}{2}}^{n+\frac{1}{2}} \right). \tag{4.2b}$$

Where,

$$B_1 = \left(\frac{L}{R} + \frac{\Delta t}{2}\right)^{-1}\left(\frac{L}{R} - \frac{\Delta t}{2}\right),$$

$$B_2 = \left(1 + \frac{\Delta t}{2} RL^{-1}\right)^{-1}.$$

In the iterative equations (4.2a) and (4.2b), not only the near-end boundary voltage V_1^{n+1} and far-end boundary voltage V_{Nz+1}^{n+1} are derived but also the iterative equations of the voltages and currents near the boundaries also need to be updated. Near the boundaries the voltages are represented by V_i^{n+1} and $V_{Nz+1-i}^{n+1}$for $i = 2, 3, \cdots, S_b$ and the currents by $I_{i+\frac{1}{2}}^{n+\frac{1}{2}}$ and $I_{Nz+1-i+\frac{1}{2}}^{n+\frac{1}{2}}$ $i = 1, 2, 3, \cdots, S_b - 1$. All these voltages and currents have some terms that exceed the index range in iterative equations (4.2a) and (4.2b).

For updating the iterative equations of voltages and currents, (4.2a) and (4.2b) need to be decomposed using the relation in [101], which satisfies the coefficients $a(i)$ given by

$$\sum_{i=1}^{S_b}(2i-1)a(i) = 1. \tag{4.3}$$

Substituting (4.3) into (4.2b), we get

$$\sum_{i=1}^{S_b}(2i-1)\,a\,(i)\,V_k^{n+1} = \sum_{i=1}^{S_b}(2i-1)\,a\,(i)\,V_k^{n} - \sum_{i=1}^{S_b}\frac{\Delta t}{(2i-1)\,\Delta z}C^{-1}\left[(2i-1)\,a\,(i)\left(I_{k+i-\frac{1}{2}}^{n+\frac{1}{2}} - I_{k-i+\frac{1}{2}}^{n+\frac{1}{2}}\right)\right]. \tag{4.4}$$

Considering the corresponding terms with i, we can decompose (4.2b) as:

$$(2i-1)\,a\,(i)\,V_k^{n+1} = (2i-1)\,a\,(i)\,V_k^{n} - (2i-1)\,a\,(i)\,\frac{\Delta t}{(2i-1)\,\Delta z}C^{-1}\left(I_{k+i-\frac{1}{2}}^{n+\frac{1}{2}} - I_{k-i+\frac{1}{2}}^{n+\frac{1}{2}}\right). \tag{4.5}$$

for $i = 1, 2, 3, \cdots, S_b$

Equation (4.5) is further modified by applying the boundary conditions as illustrated in section 4.2.2 and section 4.2.3, respectively.

4.2.2 Modeling of CMOS Driver

The CMOS drivers are modeled using n-th-power law model that considers the effect of finite drain conductance parameter (λ_d) along with velocity saturation. During transient

simulation the operation of the p-channel metal oxide semiconductor (pMOS) and n-channel metal oxide semiconductor (nMOS) transistors are in either linear, saturation (or) cutoff regions [110].

The pMOS and nMOS current equations using n-th-power law model are

$$I_p = \begin{cases} I_{DSATp}\left(1+\lambda_{d_p}\left(V_{DD}-V_{DS}\right)\right)\left(2-\frac{V_{DD}-V_{DS}}{V_{DSATp}}\right)\left(\frac{V_{DD}-V_{DS}}{V_{DSATp}}\right) & V_{DS} > V_{DD}-V_{DSATp} \\ & (linear) \\ I_{DSATp}\left(1+\lambda_{d_p}\left(V_{DD}-V_{DS}\right)\right) & V_{DS} \leq V_{DD}-V_{DSATp} \\ & (saturation) \\ 0 & V_{GS} \geq V_{DD}-\left|V_{Tp}\right| \\ & (cutoff) \end{cases} \tag{4.6a}$$

$$I_n = \begin{cases} I_{DSATn}\left(1+\lambda_{d_n}V_{DS}\right)\left(2-\frac{V_{DS}}{V_{DSATn}}\right)\left(\frac{V_{DS}}{V_{DSATn}}\right) & V_{DS} < V_{DSATn} \\ & (linear) \\ I_{DSATn}\left(1+\lambda_{d_n}V_{DS}\right) & V_{DS} \geq V_{DSATn} \\ & (saturation) \\ 0 & V_{GS} \leq V_{Tn} \\ & (cutoff) \end{cases} \tag{4.6b}$$

where I_{DSATp} (I_{DSATn}), λ_{d_p} (λ_{d_n}), V_{DSATp} (V_{DSATn}), and V_{Tp} (V_{Tn}) are the drain saturation current, finite drain conductance parameter, drain saturation voltage and the threshold voltage of pMOS (nMOS), respectively. The drain saturation voltages and currents of pMOS and nMOS are obtained from

$$V_{DSATp} = K_p\left(V_{DD}-V_{GS}-\left|V_{Tp}\right|\right)^{m_p}. \tag{4.7a}$$

$$V_{DSATn} = K_n\left(V_{GS}-V_{Tn}\right)^{m_n}. \tag{4.7b}$$

$$I_{DSATp} = \frac{W_p}{L_{eff}}B_p\left(V_{DD}-V_{GS}-\left|V_{Tp}\right|\right)^{n_p}. \tag{4.7c}$$

$$I_{DSATn} = \frac{W_n}{L_{eff}}B_n\left(V_{GS}-V_{Tn}\right)^{n_n}. \tag{4.7d}$$

The parameters K_p (K_n) and m_p (m_n) control the linear region, whereas B_p (B_n) and n_p (n_n) control the saturation region characteristics of pMOS (nMOS) transistor. The effective channel length is represented by L_{eff} and the width of pMOS (nMOS) represented by W_p (W_n). The

Table 4.1: Model parameters of pMOS and nMOS for 32-nm technology node [87].

Parameter	**pMOS**	**nMOS**
m	0.087	0.211
n	1.07	0.915
B	8.01×10^{-6}	35.5×10^{-6}
K	0.316	0.369
λ_d	3.11	0.867
V_T	0.366	0.36

model parameters [87] of pMOS and nMOS transistors are listed in Table 4.1 for 32-nm technology node.

4.2.3 Modeling of DIL System

Modeling of the DIL system is incorporated with the boundary conditions. The current equations incorporate near-end and far-end interconnect terminal conditions, where the nodal equation of the source current (I_0) at the near-end terminal (at $k = 1$) is given by:

$$I_0 = C_m \frac{dV_s}{dt} - (C_m + C_d) \frac{dV_1}{dt} + \left(I_p - I_n\right). \tag{4.8}$$

where $V_s = V_{GS}$ and $V_1 = V_{DS}$

By applying the Galerkin technique [96] to (4.8), we obtain

$$(\Delta z)(\Delta t) I_0^{n+1} = C_m (\Delta z)\left(V_s^{n+1} - V_s^n\right) - (C_m + C_d)(\Delta z)\left(V_1^{n+1} - V_1^n\right) + (\Delta z)(\Delta t) I_p^{n+1} - (\Delta z)(\Delta t) I_n^{n+1}. \tag{4.9}$$

So, the voltage at near-end terminal of interconnect is obtained by substituting $k = 1$ in (4.2b)

$$V_1^{n+1} = V_1^n - \frac{\Delta t}{\Delta z} C^{-1} \sum_{i=1}^{S_b} a(i) \left(I_{i+\frac{1}{2}}^{n+\frac{1}{2}} - I_{-i+\frac{3}{2}}^{n+\frac{1}{2}}\right). \tag{4.10}$$

Equation (4.10) is decomposed by following the steps from the (4.3)–(4.5). From the decomposition, we know that the subscript of the term $I_{-i+\frac{3}{2}}^{n+\frac{1}{2}}$ in (4.10) exceeds the index range, for $i = 2, 3, \cdots, S_b$. So, a forward difference scheme is used to overcome this difficulty. Therefore,

the final iterative equation for near-end terminal voltage $\left(V_1^{n+1}\right)$ is updated as

$$V_1^{n+1} = V_1^n - \frac{\Delta t}{\Delta z} C^{-1} \sum_{i=1}^{L_s} 2a\,(i) \left(I_{i+\frac{1}{2}}^{n+\frac{1}{2}} - I_0^{n+\frac{1}{2}}\right). \tag{4.11}$$

In (4.11), by substituting $I_0^{n+\frac{1}{2}} = \frac{I_0^n + I_0^{n+1}}{2}$ and I_0^{n+1} from (4.9) we get

$$V_1^{n+1} = V_1^n - A_1 A_2 \left(2 \sum_{i=1}^{S_b} a\,(i)\, I_{i+\frac{1}{2}}^{n+\frac{1}{2}} - \sum_{i=1}^{S_b} a\,(i) \left(I_0^n + C_m \left(\frac{V_s^{n+1} - V_s^n}{\Delta t}\right) + I_p^{n+1} - I_n^{n+1}\right)\right) \tag{4.12}$$

where,

$$A_1 = \left(1 + \tfrac{C^{-1}}{\Delta z} \left(C_m + C_d\right) \textstyle\sum_{i=1}^{S_b} a\,(i)\right)^{-1} \text{ and}$$

$$A_2 = \tfrac{\Delta t}{\Delta z} C^{-1}.$$

Similarly, at the far-end terminal ($k = Nz+1$), the nodal equation of the load current (I_{Nz+1}) is given by

$$I_{Nz+1} = C_L \frac{dV_{Nz+1}}{dt}. \tag{4.13}$$

The final iterative equation at the far-end terminal is given by

$$V_{Nz+1}^{n+1} = V_{Nz+1}^n - D_1 D_2 \left(\sum_{i=1}^{S_b} a\,(i)\, I_{Nz+1}^{n+\frac{1}{2}} - \sum_{i=1}^{S_b} 2a\,(i)\, I_{Nz+1-i+\frac{1}{2}}^{n+\frac{1}{2}}\right). \tag{4.14}$$

where,

$$D_1 = \left(1 + \tfrac{C_L}{\Delta z} C^{-1} \textstyle\sum_{i=1}^{S_b} a\,(i)\right), \text{ and}$$

$$D_2 = \tfrac{\Delta t}{\Delta z} C^{-1}.$$

In continuation with the algorithm, to derive and update the iterative equations, some term indices exceed the index range for all nodes between the terminal, therefore a truncation method is employed.

Taking V_k^{n+1} as an example for $k = 2, 3, \cdots, S_b$ and following the steps from (4.4) and (4.5), we can decompose (4.2b) as

$$a\,(1)\, V_k^{n+1} = a\,(1)\, V_k^n - a\,(1)\, \frac{\Delta t}{\Delta z} C^{-1} \left(I_{k+\frac{1}{2}}^{n+\frac{1}{2}} - I_{k-\frac{1}{2}}^{n+\frac{1}{2}}\right). \tag{4.15a}$$

$$3a\,(2)\,V_k^{n+1} = 3a\,(2)\,V_k^n - 3a\,(2)\,\frac{\Delta t}{3\Delta z}C^{-1}\left(I_{k+\frac{3}{2}}^{n+\frac{1}{2}} - I_{k-\frac{3}{2}}^{n+\frac{1}{2}}\right). \tag{4.15b}$$

$$\vdots$$

$$(2k-1)\,a\,(k)\,V_k^{n+1} = (2k-1)\,a\,(k)\,V_k^n - (2k-1)\,a\,(k)\,\frac{\Delta t}{(2k-1)\,\Delta z}C^{-1}\left(I_{2k-\frac{1}{2}}^{n+\frac{1}{2}} - I_{\frac{1}{2}}^{n+\frac{1}{2}}\right). \tag{4.15c}$$

$$\begin{aligned}(2k+1)\,a\,(k+1)\,V_k^{n+1} = {} & (2k+1)\,a\,(k+1)\,V_k^n \\ & - (2k+1)\,a\,(k+1)\,\frac{\Delta t}{(2k+1)\,\Delta z}C^{-1}\left(I_{2k+\frac{1}{2}}^{n+\frac{1}{2}} - I_{-\frac{1}{2}}^{n+\frac{1}{2}}\right)\end{aligned} \tag{4.15d}$$

$$\vdots$$

$$\begin{aligned}(2S_b-1)\,a\,(S_b)\,V_k^{n+1} = {} & (2S_b-1)\,a\,(S_b)\,V_k^n \\ & - (2S_b-1)\,a\,(S_b)\,\frac{\Delta t}{(2S_b-1)\,\Delta z}C^{-1}\left(I_{k+S_b-\frac{1}{2}}^{n+\frac{1}{2}} - I_{k-S_b+\frac{1}{2}}^{n+\frac{1}{2}}\right)\end{aligned} \tag{4.15e}$$

From the (4.15a)–(4.15e), it can be observed that for the first k terms, the indices of the equations doesn't exceed the index range, whereas, all the equations for which the index terms exceed the index range appear in the rest $(S_b - k)$ terms. As $(S_b - k)$ terms go out-of-bounds, these equations are unavailable for forming iterative equations in MRTD method. To avoid this problem, a truncation is made in the equations where the index range is exceeding.

By summing up the first k terms in (4.15a)–(4.15e), we can obtain the modified iterative equations for $k = 2, 3, \cdots, S_b$

$$V_k^{n+1} = V_k^n - \left(\sum_{i=1}^{k}(2i-1)\,a\,(i)\right)^{-1} D_2\left(\sum_{i=1}^{k} a\,(i)\left(I_{k+i-\frac{1}{2}}^{n+\frac{1}{2}} - I_{k-i+\frac{1}{2}}^{n+\frac{1}{2}}\right)\right). \tag{4.16}$$

Using the same steps illustrated in (4.15a)–(4.15e), a modified iterative equations of voltages at interior points as shown in (4.17) and voltages near the load as shown in (4.18).

for $k = S_b + 1, S_b + 2, \cdots, Nz - S_b, Nz - S_b + 1$

$$V_k^{n+1} = V_k^n - D_2\left(\sum_{i=1}^{S_b} a\,(i)\left(I_{k+i-\frac{1}{2}}^{n+\frac{1}{2}} - I_{k-i+\frac{1}{2}}^{n+\frac{1}{2}}\right)\right) \tag{4.17}$$

for $k = Nz - S_b + 2, Nz - S_b + 3, \cdots, Nz$

$$V_k^{n+1} = V_k^n - \left(\sum_{i=1}^{Nz-k+1} (2i-1)\, a(i) \right)^{-1} D_2 \left(\sum_{i=1}^{Nz-k+1} a(i) \left(I_{k+i-\frac{1}{2}}^{n+\frac{1}{2}} - I_{k-i+\frac{1}{2}}^{n+\frac{1}{2}} \right) \right) \tag{4.18}$$

The iterative equations of current can be updated by following the same steps of voltage iterative equations with a slight difference. As shown in Figure 4.2, it is observed that the current nodes appear at the half-integer points, which means that all the currents are located at the interior points of terminals. So, the currents near the terminals need to be modified.

For the iterative equations of current near the terminals, we need to decompose equation (4.2a) by using the steps from voltage iterative equations. The final modified current iterative equations are obtained as

for $k = 1$, near the source

$$I_{1+\frac{1}{2}}^{n+\frac{3}{2}} = B_1 I_{1+\frac{1}{2}}^{n+\frac{1}{2}} - B_2 \frac{\Delta t}{\Delta z} L^{-1} \left(\sum_{i=1}^{S_b} a(i) \left(V_{i+1}^{n+1} - V_1^{n+1} \right) \right). \tag{4.19}$$

for $k = 2, 3, \cdots, S_b$

$$I_{k+\frac{1}{2}}^{n+\frac{3}{2}} = B_1 I_{k+\frac{1}{2}}^{n+\frac{1}{2}} - B_2 \left(\sum_{i=1}^{k} (2i-1)\, a(i) \right)^{-1} \frac{\Delta t}{\Delta z} L^{-1} \left(\sum_{i=1}^{k} a(i) \left(V_{k+i}^{n+1} - V_{k-i+1}^{n+1} \right) \right) \tag{4.20}$$

for $k = S_b + 1, S_b + 2, \cdots, Nz - S_b, Nz - S_b + 1$, iterative equations at interior points are

$$I_{k+\frac{1}{2}}^{n+\frac{3}{2}} = B_1 I_{k+\frac{1}{2}}^{n+\frac{1}{2}} - B_2 \frac{\Delta t}{\Delta z} L^{-1} \left(\sum_{i=1}^{S_b} a(i) \left(V_{k+i}^{n+1} - V_{k-i+1}^{n+1} \right) \right) \tag{4.21}$$

for $k = Nz - S_b + 2, Nz - S_b + 3, \cdots, Nz$, iterative equations near the load are

$$I_{k+\frac{1}{2}}^{n+\frac{3}{2}} = B_1 I_{k+\frac{1}{2}}^{n+\frac{1}{2}} - B_2 \left(\sum_{i=1}^{Nz-k+1} (2i-1)\, a(i) \right)^{-1} \frac{\Delta t}{\Delta z} L^{-1} \left(\sum_{i=1}^{Nz-k+1} a(i) \left(V_{k+i}^{n+1} - V_{k-i+1}^{n+1} \right) \right) \tag{4.22}$$

A bootstrapping approach is used for evaluating the updated voltage and current iterative equations. Foremost, the voltage iterative equations are solved at fixed time using (4.12), (4.14), (4.16) – (4.18) in terms of past values of voltages and currents. Thereafter, the iterative equa-

tions of currents are solved from equation (4.19) – (4.22) in terms of voltages evaluated initially and form past values of currents. So, to get the stable output for the MRTD iterative equations, the courant stability condition [104], [101] is considered as

$$\Delta t \leq \frac{q\Delta z}{\vartheta} \tag{4.23}$$

which states that the propagation time must be greater than the time step, over each cell. Here q is a Courant number given by $q = \frac{1}{\sum_{i=1}^{L_s}|a(i)|} = \frac{\vartheta\Delta t}{\Delta z}$ and ϑ is the phase velocity of propagation on the line.

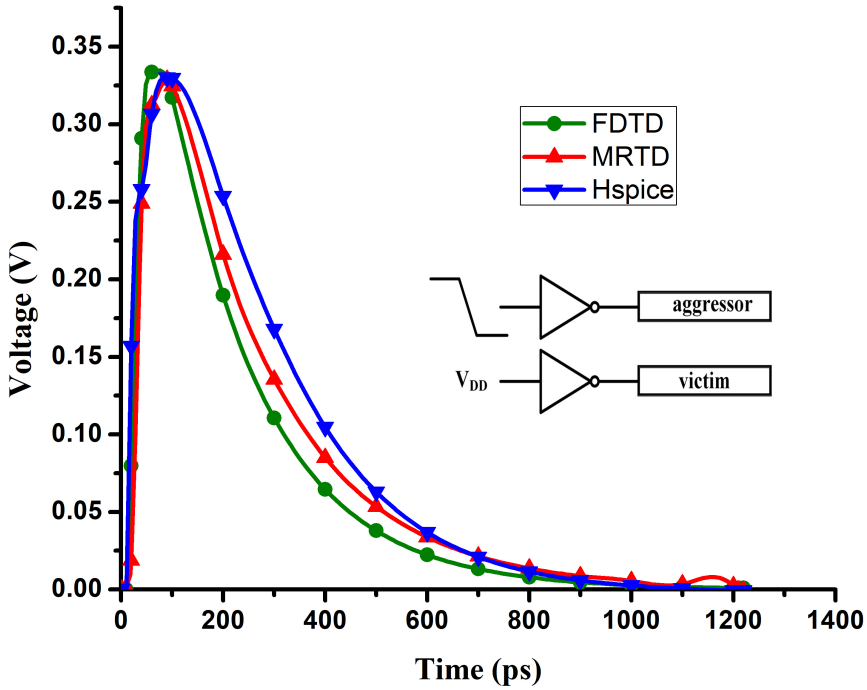
4.3 Simulation Setup and Validation of Results

The proposed MRTD method is validated in HSPICE using W-element method and compared with the conventional FDTD method. The coupled interconnect lines are driven using symmetric CMOS drivers. To maintain the symmetry in operation of CMOS inverter, the aspect ratio of W_p to W_n is chosen to be 2:1, with the width of pMOS (W_p) is chosen to be 3.2 μm. A ramp signal with a transition time of 10 ps, is considered as an input. The technology used is 32-nm with thickness and width of the interconnect line as 0.66 μm and 0.22 μm, respectively, with an aspect ratio of 3:1 [87]. The height from the ground plane is considered to be equal to the thickness of the interconnect line and the spacing between the two interconnect lines is assumed to be equal to its width. The global level interconnect length, load capacitance and inter-layer metal-insulator dielectric constant of the line are 1 mm, 2 fF and 2.2, respectively. The line parasitics extracted using the setup mentioned above are shown in Table 4.2.

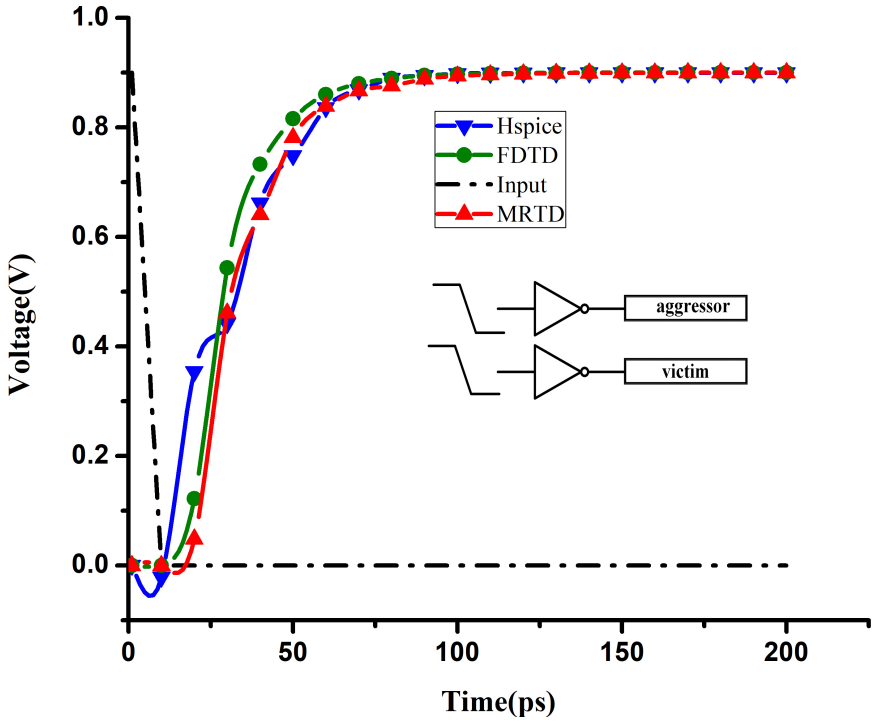
The corresponding mode velocities, for given line parasitics, are calculated as odd mode velocity $\vartheta_o = 1.71 \times 10^8$ m/s and even mode velocity $\vartheta_e = 1.45 \times 10^8$ m/s. To obtain high accuracy, the value of space discretization (Δz) is computed to be less than 0.46 mm, by considering break frequency of 32 GHz and even mode velocity. The time discretization (Δt) value is calculated to be 1.869 ps by using the value of (Δz) and odd mode velocity for the Courant number q=0.7.

4.3.1 Transient Analysis of coupled two interconnect lines

The analysis of inclusive crosstalk noise at far-end terminal of the victim line is performed using, HSPICE, conventional FDTD method and the proposed MRTD method. The transient re-

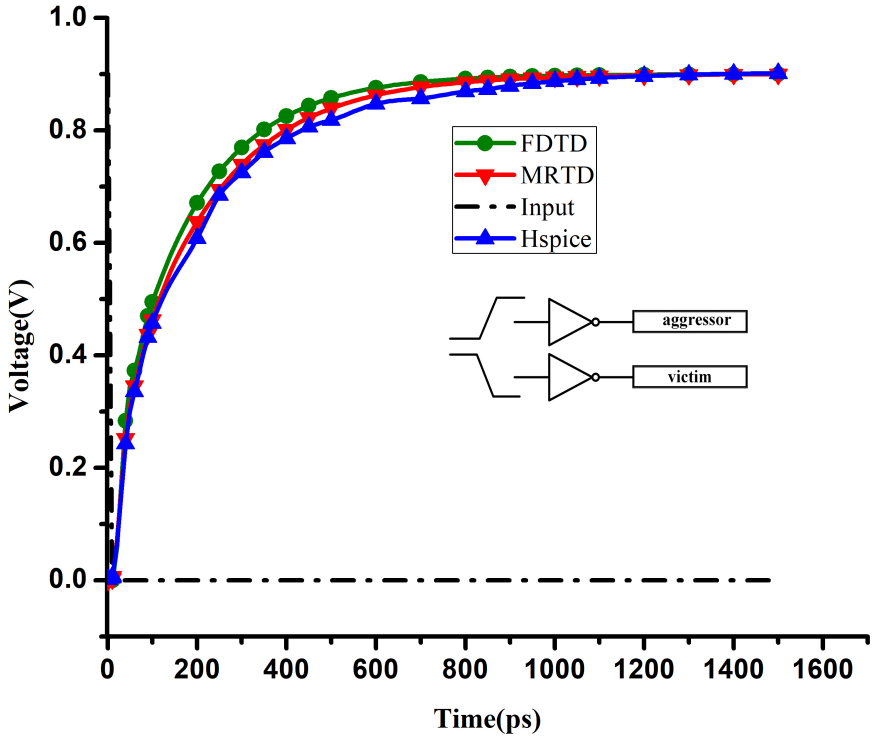


(a)



(b)

sponse of switching of functional crosstalk and dynamic in-phase as well as out-phase crosstalk, are illustrated in Figure 4.3a–4.3c. For functional crosstalk, the victim line remains at ground level, whereas, the aggressor line makes a transition from the ground to V_{DD}. For dynamic in-phase crosstalk, the switching from ground to V_{DD} takes place in both aggressor and victim lines. Finally, the transition takes place from V_{DD} to ground and ground to V_{DD} in aggressor and



(c)

Figure 4.3: Transient response at the far-end terminal of the victim line during the switching of (a) functional crosstalk (b) dynamic in-phase and (c) dynamic out-phase crosstalk.

victim lines, respectively for dynamic out-phase crosstalk. It is observed from Figure 4.3 that the proposed MRTD method dominates the existing conventional FDTD method and is in good agreement with HSPICE.

Table 4.3 presents the computational error in predicting the crosstalk induced peak voltage and timing, on quiescent victim line, using the proposed MRTD model and the conventional FDTD, with respect to HSPICE simulations. The percentage error can be calculated for the methods (M_{th}) with respect to HSPICE (H_{SPICE}) by using the equation (4.24).

$$error(\%) = \left(\frac{H_{SPICE} - M_{th}}{H_{SPICE}} \right) \times 100 \tag{4.24}$$

The model is tested for the robustness at different input transition times. It is observed from Table 4.3 that, for the proposed model, the average error in prediction of crosstalk peak voltage is 0.14 % when compared to that of 2.7 % for conventional FDTD method. It can also be inferred from the Table 4.3 that the peak noise timing is well predicted using proposed model with average error of 1.9 % when compared to that of 2.8 % using the conventional FDTD method. Here, the MRTD model is giving more accurate results due to the better dispersion properties than FDTD method.

Table 4.2: Interconnect parasitics for setup mentioned in section 4.3(A*–Aggressor, V*–Victim).

R [kΩ/m]	**L** [μH/m]	**C** [pF/m]	$\mathbf{C_{12}/C_{23}}$ [pF/m] (between A* line and V* line)	$\mathbf{M_{12}/M_{23}}$ [μH/m] (between A* line and V* line)	$\mathbf{M_{13}}$ [μH/m] (between two A* lines)
151.5	1.645	15.114	98.598	1.484	1.264

Table 4.3: Computational error involved for peak crosstalk noise and peak noise timing on victim line (conv.*–conventional).

Input Transition Time [ps]	**Peak Crosstalk Noise** [V]					**Peak Noise Timing** [ps]				
	HSPICE	**Proposed Model**	**conv.* FDTD**	**error(%)**		**HSPICE**	**Proposed Model**	**conv.* FDTD**	**error(%)**	
				Proposed	**FDTD**				**Proposed**	**FDTD**
10	0.33061	0.3288	0.34	0.55	-2.84	91.606	90	89.2	1.75	2.63
20	0.33002	0.3286	0.3398	0.43	-2.96	95.9	94	92.8	1.98	3.23
30	0.32917	0.3284	0.3392	0.234	-3.05	104.2	102.7	101	1.44	3.07
40	0.32875	0.3276	0.3385	0.35	-2.96	114.8	113.2	110.9	1.4	3.39
50	0.32834	0.3274	0.3376	0.29	-2.82	118	116.2	116	1.53	1.69
60	0.32785	0.3269	0.3366	0.49	-2.66	128.6	126.43	125	1.7	2.79
70	0.32635	0.3264	0.3355	-0.02	-2.80	134.56	132.8	131.4	1.31	2.35
80	0.32512	0.3259	0.3343	-0.24	-2.82	140.45	138.52	137.8	1.374	1.88
90	0.32382	0.3251	0.3328	-0.39	-2.77	150.2	144	142.96	4.13	4.82
100	0.32289	0.324	0.3296	-0.343	-2.07	158.31	154.83	153.6	2.19	2.98

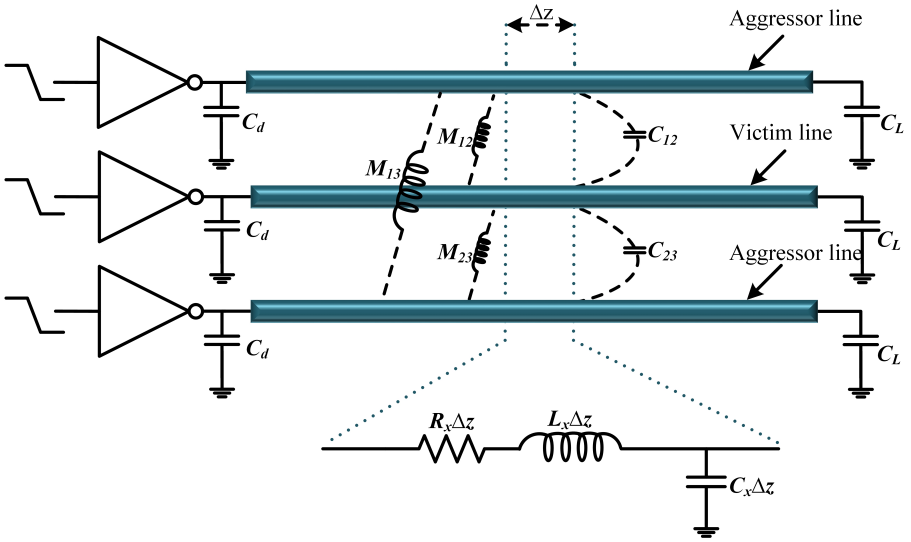


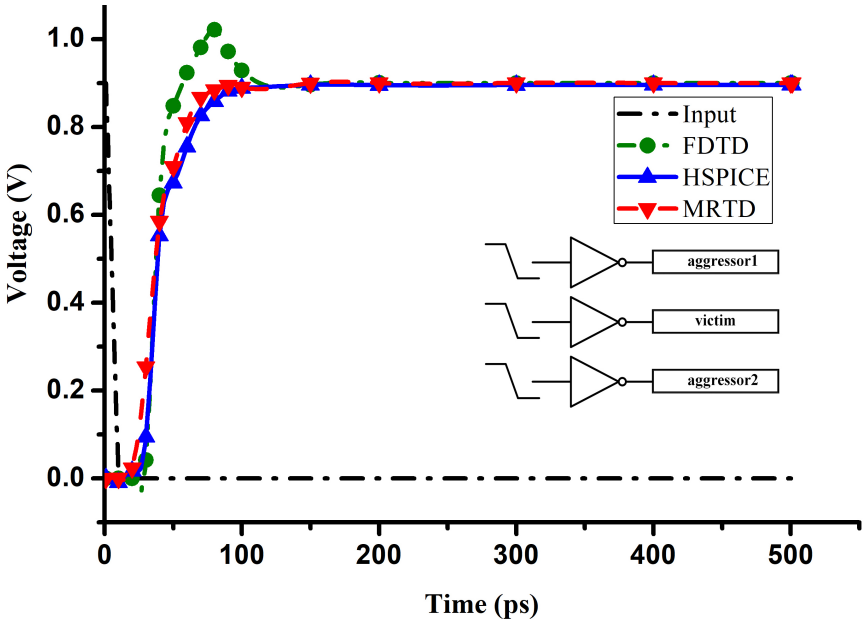
Figure 4.4: Schematic of CMOS driven three-coupled interconnect lines.

4.3.2 Transient Analysis of three mutually coupled interconnect lines

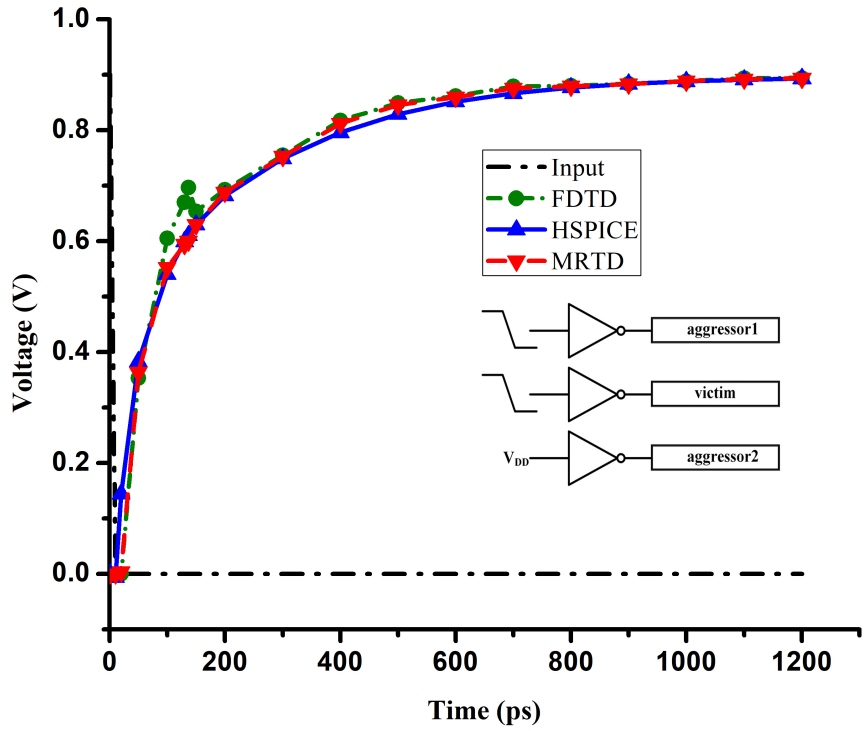
Further, the proposed MRTD method is extended to three-coupled interconnect lines as illustrated in Figure 4.4 and it is validated using HSPICE (W-element). The interconnect line parasitics for the analysis of the crosstalk of three-coupled lines can be extracted using the setup described in section 4.3. The coupling capacitance between the two aggressor lines can be neglected safely as the spacing between them is large [71].

$$\mathbf{R} = \begin{bmatrix} R_1 & 0 & 0 \\ 0 & R_2 & 0 \\ 0 & 0 & R_3 \end{bmatrix}, \mathbf{L} = \begin{bmatrix} L_1 & M_{12} & M_{13} \\ M_{12} & L_2 & M_{23} \\ M_{13} & M_{23} & L_3 \end{bmatrix}, \mathbf{C} = \begin{bmatrix} C_1 + C_{12} & -C_{12} & 0 \\ -C_{12} & C_2 + C_{12} + C_{23} & C_2 + C_{23} \\ 0 & -C_{23} & C_3 + C_{23} \end{bmatrix}$$

The comparison of the transient response of crosstalk switching on victim line for three-coupled interconnect lines between the proposed MRTD method, HSPICE and the conventional FDTD method for two different test cases are illustrated in Figure 4.5. It is observed that the proposed MRTD method is in good agreement with the HSPICE simulation results. From Figure 4.5a and 4.5b, it is also observed that a peak is resulted in the response using the conventional FDTD method due to its numerical dispersion properties. However, the proposed MRTD method with its great advantages in numerical dispersion properties [50][98, 99] dominates over the conventional FDTD method with respect to accuracy. Table 4.4 presents the computational error involved in predicting the crosstalk induced 50 % delay on victim line due to aggressor lines using the proposed MRTD method and the conventional FDTD method with respect to HSPICE. The proposed model has an average error less than 1 %, whereas, the conventional FDTD method has an average error more than 3 %.



(a)



(b)

Figure 4.5: Crosstalk induced 50% Delay analysis on victim line due to aggressor lines (a) test case-1, (b) test case-2 for three-coupled interconnect lines..

Table 4.4: Computational error involved for 50% Delay on victim line of three-coupled interconnects (Agg.*–Aggressor & conv.*–conventional).

Input Switching Mode				**50% Delay** [ps] **on Victim line**				
							error(%)	
Test Cases	**Agg.* line1**	**Victim line**	**Agg.* line2**	**HSPICE**	**MRTD**	**conv.* FDTD**	**MRTD**	**conv.* FDTD**
1	V_{DD} *to* 0	V_{DD} *to* 0	V_{DD} *to* 0	35	34.43	33.89	1.91	3.45
2	V_{DD} *to* 0	V_{DD} *to* 0	V_{DD}	66.088	66.88	64.2	-1.198	2.86

Table 4.5: Comparison of elapsed CPU time of the methods for two and three mutually coupled interconnects (conv.*–conventional).

	Elapsed CPU time (s)		
Methods / **No. of Coupled lines**	**HSPICE**	**MRTD**	**conv.* FDTD**
Two	0.2466 ≈ 0.25	0.19035	0.1699 ≈ 0.17
Three	0.382	0.3061	0.2827

The elapsed CPU time for the proposed MRTD method, the conventional FDTD method and the HSPICE (W-Element method) is determined using the Intel Core i7 processor - 3770 CPU (3.40 GHz). Table 4.5 shows the corresponding elapsed CPU times of each method. It is observed that the elapsed CPU time of HSPICE is higher than both MRTD and conventional FDTD methods, but MRTD is little bit slower than conventional FDTD, as more number of iterations are required for MRTD than the conventional FDTD to achieve more accuracy. Therefore, there is a trade-off between accuracy and simulation time.

4.4 Summary

This chapter deals with the modeling of DIL system, which includes the non-linear characteristics of a CMOS-gate-driver by employing *n*-th-power law model. The functional/dynamic crosstalk analysis is performed on two and three mutually coupled copper interconnect lines

driven by non-linear CMOS-gate. The results show the dominance of the proposed MRTD method over the conventional FDTD method. Also, the proposed scheme is more time efficient than HSPICE.

Chapter 5

Crosstalk Noise Modeling of CMOS-Gate Driven Coupled MWCNT Interconnects Using MRTD

This chapter focuses on the modeling of advanced interconnect material (i.e., multi-walled carbon nanotube interconnects) driven by non-linear CMOS-gate driver.

5.1 Introduction

One of the traditional interconnect materials used in deep-submicron VLSI integrated circuits is copper. The scaling down of interconnect dimensions has made surface scattering and grain boundary scattering more prominent, resulting in increased resistivity of Cu material [16]. In addition to this, the skin effect, electromigration effect, low thermal and electrical conductivity, small MFP and limited current density also degrade the performance of an IC [33]–[35]. Therefore, the requirements of new and reliable materials for IC interconnects has increased. In the recent times, carbon nanomaterials such as carbon nanotubes and graphene nanoribbons form one of the most promising candidates proposed as a substitute for Cu interconnects in advanced VLSI circuits [36, 37]. CNTs, with their outstanding thermal and electrical properties, such as high melting point (3800 K), higher thermal stability, large MFPs and the maximum current density ($10^{10}\ A/cm^2$) outperform the conventional Cu interconnect [38].

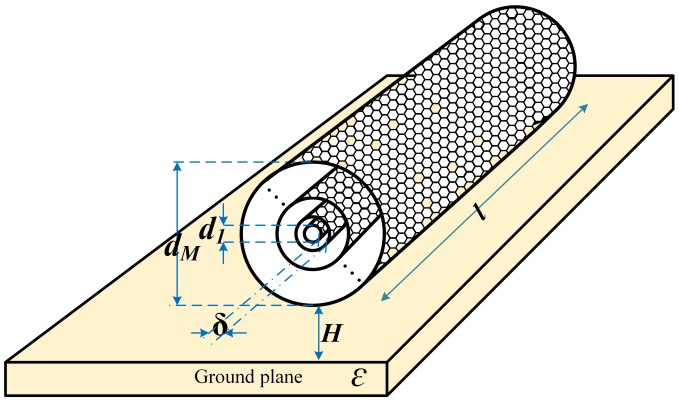


Figure 5.1: Geometry of the MWCNT over a ground plane.

Based on the physical properties, carbon nanotubes are classified into two types: SWCNTs and MWCNTs [39, 40]. The MWCNTs have few concentric shells of rolled-up graphene sheets with their diameter ranging from few nanometers to tens of nanometers. Based on the chirality of graphene sheets, the SWCNT exhibits either metallic or semiconducting behaviour whereas the MWCNT exhibits only metallic behaviour [37]. Due to the large diameter and considering all the shells adequately connected to the metal contacts, MWCNTs have long electron MFPs and a great number of conducting channels compared to SWCNTs. Although the MWCNTs provide similar current carrying capability as SWCNTs, they are simpler to fabricate due to their greater control over the growth process [41]. Therefore, in the present state of the art MWCNT has been considered as interconnect to analyze the signal integrity issues of DIL system.

5.2 ESC model for MWCNT interconnects

This section discusses an equivalent RLC model of an MWCNT interconnect line which is placed over a dielectric medium with dielectric constant ε and positioned above the ground plane at a distance H. The geometry of an isolated MWCNT interconnect having length 'l' positioned above the ground plane is illustrated in Figure 5.1. The MWCNT consists of M shells with the inner-most and the outer-most shells of diameters d_1 and d_M, respectively. In Figure 5.1, δ represents the van der Waals gap, which is a gap(~0.34 nm) between the two neighboring shells.

The schematic of the ESC model of mutually N-coupled MWCNT interconnects driven by CMOS driver is shown in Figure 5.2. Here C_m (gate-to-drain coupling capacitance), C_d (drain/source diffusion capacitance) are the parasitic capacitances of CMOS. R_{lump} represents

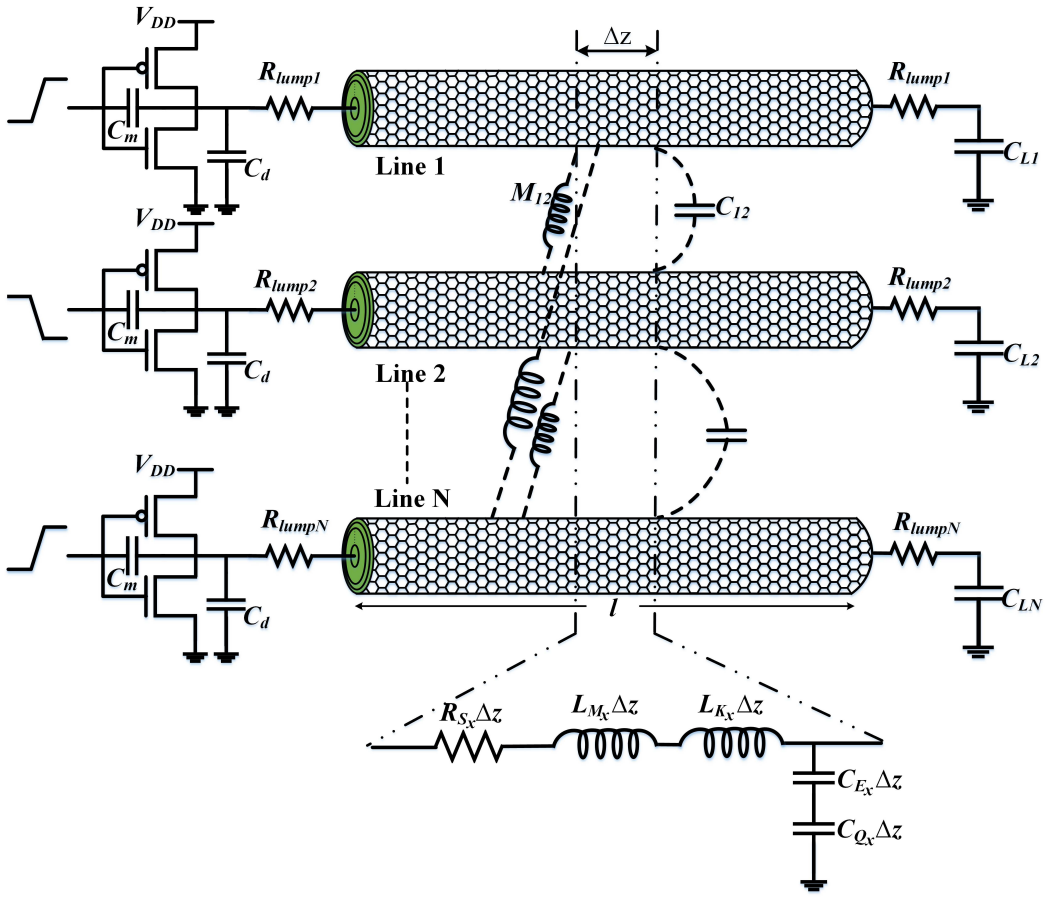


Figure 5.2: Schematic of the ESC model of mutually N-coupled MWCNT interconnects driven by CMOS driver

the average value of equivalent resistance introduced by the total imperfect contact resistance (R_{mc}) and the quantum resistance $\left(R_q\right)$, R_{S_x} is the per unit length (p.u.l) carrier scattering resistance. The distributive line inductance (L_{K_x}) is computed using mutual inductance between the shells and their kinetic inductance, and L_{M_x} is the magnetic inductance p.u.l. The distributive line capacitance (C_{Q_x}) is computed using coupling capacitance between shells and their quantum capacitance, C_{E_x} is the p.u.l electrostatic capacitance. The subscript x of the distributed line parameters represents the parameters corresponding to Line 1, Line 2, ... Line N at $x = 1, 2, \ldots N$, respectively. The values of L_{K_x} and C_{Q_x} can be calculated using the iterative expressions [38],[111], whereas, the values of C_{E_x}, L_{M_x}, and the mutual inductance (M_{12}) as well as coupling capacitance (C_{12}), between two MWCNT interconnect lines can be obtained using the industry preffered tools such as Raphael (Synopsys tool) and the Ansoft Maxwell electrostatic and magnetostatic field solvers [112]. C_L represents the load capacitance.

5.3 Development of the MRTD model for MWCNT interconnects

The MRTD model is developed based on Daubechies' scaling function with four vanishing moments (D_4) as a basis function for an on-chip mutually N-coupled MWCNT interconnects.

5.3.1 Modeling of mutually coupled MWCNT interconnects

The telegrapher's equations in the transverse electromagnetic mode [81] are used to express the coupled VLSI MWCNT interconnects as

$$\frac{\partial \mathbf{V}(z,t)}{\partial z} + \mathbf{R}\mathbf{I}(z,t) + \mathbf{L}\frac{\partial \mathbf{I}(z,t)}{\partial t} = 0. \tag{5.1a}$$

$$\frac{\partial \mathbf{I}(z,t)}{\partial z} + \mathbf{C}\frac{\partial \mathbf{V}(z,t)}{\partial t} = 0. \tag{5.1b}$$

Where $\mathbf{V}$ and $\mathbf{I}$ in (5.1a), (5.1b) represented as voltages and currents, respectively, which are expressed in $N \times 1$ column vector form $\begin{bmatrix} V_1 & V_2 & \cdots & V_N \end{bmatrix}^T$ and $\begin{bmatrix} I_1 & I_2 & \cdots & I_N \end{bmatrix}^T$. The line parasitics are expressed in $N \times N$ matrix per unit length as given in (5.2).

$$\mathbf{R} = \mathbf{diag}\begin{bmatrix} R_{S_1} & R_{S_2} & R_{S_3}, \cdots R_{S_{N-1}} & R_{S_N} \end{bmatrix},$$

$$\mathbf{L} = \begin{bmatrix} L_{K_1} + L_{M_1} & M_{12} & M_{13} & \cdots & M_{1(N-1)} & M_{1N} \\ M_{21} & L_{K_2} + L_{M_2} & M_{23} & \cdots & M_{2(N-1)} & M_{2N} \\ \vdots & \vdots & \ddots & \ddots & \vdots & \vdots \\ M_{N1} & M_{N2} & M_{N3} & \cdots & M_{N(N-1)} & L_{K_N} + L_{M_N} \end{bmatrix},$$

$$\mathbf{C} = \begin{bmatrix} \left(\frac{1}{C_{Q_1}} + \frac{1}{C_{E_1}}\right)^{-1} + \sum_{y=2} C_{1y} & -C_{12} & 0 & \cdots & 0 & 0 \\ -C_{21} & \left(\frac{1}{C_{Q_2}} + \frac{1}{C_{E_2}}\right)^{-1} + \sum_{y=1,3} C_{2y} & -C_{23} & \cdots & 0 & 0 \\ \vdots & \vdots & \ddots & \ddots & \vdots & \vdots \\ 0 & 0 & 0 & \cdots & -C_{N(N-1)} & \left(\frac{1}{C_{Q_N}} + \frac{1}{C_{E_N}}\right)^{-1} + \sum_{y=(N-1)} C_{Ny} \end{bmatrix} \tag{5.2}$$

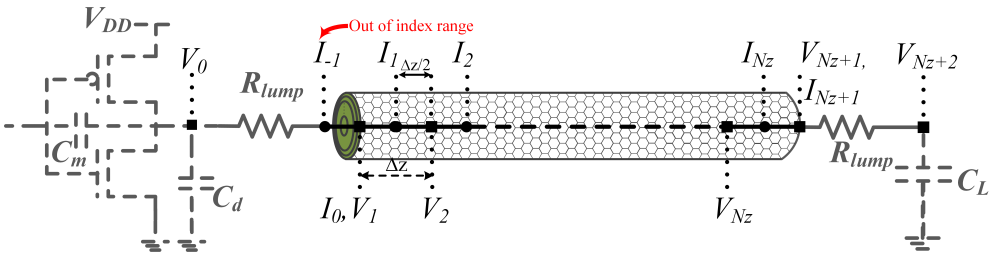


Figure 5.3: Spatial discretization of MRTD model for driver-interconnect-load system.

The interconnect line of length l is driven by a CMOS driver at $z = 0$ and is terminated by the load (C_L) at $z = l$. The line is discretized into current and voltage nodes which are unknown coefficients, by dividing it uniformly into Nz segments of length $\Delta z = \frac{l}{Nz}$, as shown in Figure 5.3. Here, I_0 represents the source current.

Solving equations (5.1a) and (5.1b) by using (3.2)-(3.7) produces exactly similar iterative equations of voltages and currents as in chapter 3 i.e., the equations (3.9)-(3.12).

$$I^{n+\frac{3}{2}}_{k+\frac{1}{2}} = B_1 I^{n+\frac{1}{2}}_{k+\frac{1}{2}} - B_2 \frac{\Delta t}{\Delta z} L^{-1} \sum_{j=1}^{S_b} a(j) \left(V^n_{k+j} - V^n_{k-j+1} \right). \tag{5.3a}$$

$$V^{n+1}_k = V^n_k - \frac{\Delta t}{\Delta z} C^{-1} \sum_{j=1}^{S_b} a(j) \left(I^{n+\frac{1}{2}}_{k+j-\frac{1}{2}} - I^{n+\frac{1}{2}}_{k-j+\frac{1}{2}} \right). \tag{5.3b}$$

Where,

$$B_1 = \left(\tfrac{L}{R} + \tfrac{\Delta t}{2} \right)^{-1} \left(\tfrac{L}{R} - \tfrac{\Delta t}{2} \right) \text{ and}$$

$$B_2 = \left(1 + \tfrac{\Delta t}{2} R L^{-1} \right)^{-1}.$$

In (5.3a) and (5.3b), the terminal voltages V^{n+1}_1 and V^{n+1}_{Nz+1} need to be derived besides updating the voltages and currents iterative equation near the boundaries also essential. The voltages and currents, near the boundary, are represented by V^{n+1}_j, V^{n+1}_{Nz+1-j} for $j = 2, 3, \cdots, S_b$ and $I^{n+\frac{1}{2}}_{j+\frac{1}{2}}$, $I^{n+\frac{1}{2}}_{Nz+1-j+\frac{1}{2}}$ for $j = 1, 2, 3, \cdots, S_b - 1$, respectively. Some of the terms in all these voltages and currents may exceed the index range in (5.3a) and (5.3b).

Therefore, (5.3a) and (5.3b) are decomposed using the relation in [101], for updating the voltages and currents iterative equation, satisfying the coefficients $a(j)$ given by

$$\sum_{j=1}^{S_b}(2j-1)a(j)=1. \tag{5.4}$$

Substituting (5.4) into (5.3b), results in

$$\begin{aligned}\sum_{j=1}^{S_b}(2j-1)\,a\,(j)\,V_k^{n+1} &= \sum_{j=1}^{S_b}(2j-1)\,a\,(j)\,V_k^{n}\\ &\quad-\sum_{j=1}^{S_b}\frac{\Delta t}{(2j-1)\,\Delta z}C^{-1}\left[(2j-1)\,a\,(j)\left(I_{k+j-\frac{1}{2}}^{n+\frac{1}{2}}-I_{k-j+\frac{1}{2}}^{n+\frac{1}{2}}\right)\right].\end{aligned} \tag{5.5}$$

Equation (5.3b) can be decomposed by considering the corresponding terms with j, as:

$$\begin{aligned}(2j-1)\,a\,(j)\,V_k^{n+1} &= (2j-1)\,a\,(j)\,V_k^{n}\\ &\quad-(2j-1)\,a\,(j)\,\frac{\Delta t}{(2j-1)\,\Delta z}C^{-1}\left(I_{k+j-\frac{1}{2}}^{n+\frac{1}{2}}-I_{k-j+\frac{1}{2}}^{n+\frac{1}{2}}\right).\end{aligned} \tag{5.6}$$

for $j=1,2,3,\cdots,S_b$,

Further, (5.6) can be modified by taking appropriate boundary conditions as detailed in Section 5.3.2.

5.3.2 Incorporating the boundary conditions in DIL system

The voltage and current equations at the driver and load are incorporated by interconnect terminal conditions. By applying the nodal analysis, the source voltage (V_0) and current (I_0) can be determined as

$$I_0=\frac{(V_0-V_1)}{R_{lump}} \tag{5.7a}$$

$$I_0=C_m\frac{dV_s}{dt}-(C_m+C_d)\frac{dV_0}{dt}+\left(I_p-I_n\right). \tag{5.7b}$$

where $V_s=V_{GS}$ and $V_0=V_{DS}$ and I_p represents the pMOS transistor current and I_n represents the nMOS transistor current. The n-th-power law model [88] is considered to defined the currents I_p and I_n.

By applying the discretization to (5.7a) and Galerkin technique [96] to (5.7b), we obtain

$$I_0^{n+1} = \frac{1}{R_{lump}}\left(V_0^{n+1} - V_1^{n+1}\right) \tag{5.8a}$$

$$\begin{aligned}(\Delta z)(\Delta t) I_0^{n+1} =& C_m(\Delta z)\left(V_s^{n+1} - V_s^n\right) \\ &- (C_m + C_d)(\Delta z)\left(V_0^{n+1} - V_0^n\right) + (\Delta z)(\Delta t) I_p^{n+1} - (\Delta z)(\Delta t) I_n^{n+1}\end{aligned}$$

$$\Downarrow$$

$$V_0^{n+1} = V_0^n + \left(\frac{C_m + C_d}{\Delta t}\right)^{-1}\left(\frac{C_m}{\Delta t}\left(V_s^{n+1} - V_s^n\right) + I_p^{n+1} - I_n^{n+1} - I_0^n\right) \tag{5.8b}$$

Here, the near-end terminal voltage is obtained by substituting $k = 1$ in (5.3b)

$$V_1^{n+1} = V_1^n - \frac{\Delta t}{\Delta z} C^{-1} \sum_{j=1}^{S_b} a(j)\left(I_{j+\frac{1}{2}}^{n+\frac{1}{2}} - I_{-j+\frac{3}{2}}^{n+\frac{1}{2}}\right). \tag{5.9}$$

The decomposition of (5.9) is done by following the steps from (5.4)–(5.6). From the decomposition, it can be observed that the index range for subscript of the term $I_{-j+\frac{3}{2}}^{n+\frac{1}{2}}$ in (5.9) is exceeding for $j = 2, 3, \cdots, S_b$. To overcome this difficulty, a forward difference scheme is utilized to update the near-end terminal voltage. Therefore, the updated terminal voltage $\left(V_1^{n+1}\right)$ is given by

$$V_1^{n+1} = V_1^n - \frac{\Delta t}{\Delta z} C^{-1} \sum_{j=1}^{L_s} 2a(j)\left(I_{j+\frac{1}{2}}^{n+\frac{1}{2}} - I_0^{n+\frac{1}{2}}\right). \tag{5.10}$$

In (5.10), by substituting $I_0^{n+\frac{1}{2}} = \frac{I_0^n + I_0^{n+1}}{2}$ and I_0^{n+1}, V_0^{n+1} from (5.8a), (5.8b) we get

$$V_1^{n+1} = A_1 A_2 V_1^n + A_1 A_3\left(\sum_{j=1}^{S_b} a(j)\left(\frac{V_0^{n+1} + V_0^n}{R_{lump}}\right) - 2\sum_{j=1}^{S_b} a(j) I_{j+\frac{1}{2}}^{n+\frac{1}{2}}\right) \tag{5.11}$$

where,

$$A_1 = \left(1 + \tfrac{\Delta t}{\Delta z} C^{-1} R_{lump}^{-1} \textstyle\sum_{j=1}^{S_b} a(j)\right)^{-1},$$

$$A_2 = \left(1 - \tfrac{\Delta t}{\Delta z} C^{-1} R_{lump}^{-1} \textstyle\sum_{j=1}^{S_b} a(j)\right) \text{ and}$$

$$A_3 = \tfrac{\Delta t}{\Delta z} C^{-1}.$$

Similarly, by applying nodal analysis at the far-end terminal ($k = Nz + 1$), load current (I_{Nz+1}) is given by

$$I_{Nz+1} = \frac{(V_{Nz+1} - V_{Nz+2})}{R_{lump}} \tag{5.12a}$$

$$I_{Nz+1} = C_L \frac{dV_{Nz+1}}{dt}. \tag{5.12b}$$

By applying discretization to (5.12a) and Galerkin technique [96] to (5.12b), we get

$$I^{n+1}_{Nz+1} = \frac{1}{R_{lump}} \left(V^{n+1}_{Nz+1} - V^{n+1}_{Nz+2} \right) \tag{5.13a}$$

$$V^{n+1}_{Nz+2} = V^{n}_{Nz+2} + \frac{\Delta t}{C_L} I^{n+1}_{Nz+1} \tag{5.13b}$$

Therefore, at the far-end terminal the updated voltage iterative equation is

$$V^{n+1}_{Nz} = A_1 A_2 V^{n}_{Nz} + A_1 A_3 \sum_{j=1}^{S_b} a(j) \left(\frac{V^{n+1}_{Nz+2} + V^{n}_{Nz+2}}{R_{lump}} \right) + 2 A_1 A_3 \sum_{j=1}^{S_b} a(j) I^{n+\frac{1}{2}}_{Nz+1-j+\frac{1}{2}} \tag{5.14}$$

5.3.3 Voltage and Current equations at the interior points of the boundary

To derive and update the iterative equations, there is a need for truncation of terms with indices exceeding the index range for all nodes between the terminals.

The decomposition of (5.3b) can be done by following the steps from (5.5) and (5.6) considering V^{n+1}_k as an example at $k = 2, 3, \cdots, S_b$.

$$a(1) V^{n+1}_k = a(1) V^{n}_k - a(1) \frac{\Delta t}{\Delta z} C^{-1} \left(I^{n+\frac{1}{2}}_{k+\frac{1}{2}} - I^{n+\frac{1}{2}}_{k-\frac{1}{2}} \right). \tag{5.15a}$$

$$3a(2) V^{n+1}_k = 3a(2) V^{n}_k - 3a(2) \frac{\Delta t}{3\Delta z} C^{-1} \left(I^{n+\frac{1}{2}}_{k+\frac{3}{2}} - I^{n+\frac{1}{2}}_{k-\frac{3}{2}} \right). \tag{5.15b}$$

$$\vdots$$

$$(2k-1) a(k) V^{n+1}_k = (2k-1) a(k) V^{n}_k - (2k-1) a(k) \frac{\Delta t}{(2k-1)\Delta z} C^{-1} \left(I^{n+\frac{1}{2}}_{2k-\frac{1}{2}} - I^{n+\frac{1}{2}}_{\frac{1}{2}} \right). \tag{5.15c}$$

$$(2k+1)\,a\,(k+1)\,V_k^{n+1} = (2k+1)\,a\,(k+1)\,V_k^n - (2k+1)\,a\,(k+1)\,\frac{\Delta t}{(2k+1)\,\Delta z} C^{-1}\left(I_{2k+\frac{1}{2}}^{n+\frac{1}{2}} - I_{-\frac{1}{2}}^{n+\frac{1}{2}}\right). \tag{5.15d}$$

$$\vdots$$

$$(2S_b-1)\,a\,(S_b)\,V_k^{n+1} = (2S_b-1)\,a\,(S_b)\,V_k^n - (2S_b-1)\,a\,(S_b)\,\frac{\Delta t}{(2S_b-1)\,\Delta z} C^{-1}\left(I_{k+S_b-\frac{1}{2}}^{n+\frac{1}{2}} - I_{k-S_b+\frac{1}{2}}^{n+\frac{1}{2}}\right). \tag{5.15e}$$

Equations (5.15a)–(5.15e) reveal that the indices of the equations does not exceed the index range only for the first k terms. For remaining $S_b - k$ terms with out of bound indices, formation of iterative equations becomes impractical in MRTD method. This issue is addressed by truncating the equations with out of bound indices.

The modified iterative equations can be obtained by summing up the first k terms from (5.15a)–(5.15e),

$$V_k^{n+1} = V_k^n - \left(\sum_{j=1}^{k} (2j-1)\,a\,(j)\right)^{-1} D_2\left(\sum_{j=1}^{k} a\,(j)\left(I_{k+j-\frac{1}{2}}^{n+\frac{1}{2}} - I_{k-j+\frac{1}{2}}^{n+\frac{1}{2}}\right)\right) \tag{5.16}$$

at $k = 2, 3, \cdots, S_b$.

The modified iterative equation for voltages at interior points and voltages near the load are shown in (5.17) and (5.18), respectively.

$$V_k^{n+1} = V_k^n - D_2\left(\sum_{j=1}^{S_b} a\,(j)\left(I_{k+j-\frac{1}{2}}^{n+\frac{1}{2}} - I_{k-j+\frac{1}{2}}^{n+\frac{1}{2}}\right)\right). \tag{5.17}$$

at $k = S_b + 1, S_b + 2, \cdots, Nz - S_b, Nz - S_b + 1$.

$$V_k^{n+1} = V_k^n - \left(\sum_{j=1}^{Nz-k+1} (2j-1)\,a\,(j)\right)^{-1} D_2\left(\sum_{j=1}^{Nz-k+1} a\,(j)\left(I_{k+j-\frac{1}{2}}^{n+\frac{1}{2}} - I_{k-j+\frac{1}{2}}^{n+\frac{1}{2}}\right)\right). \tag{5.18}$$

at $k = Nz - S_b + 2, Nz - S_b + 3, \cdots, Nz$.

Similarly, the current equations can be updated following the same steps that are used for voltage equations with a slight variation. It can be observed from Figure 5.3 that the current nodes appear at half-integer points i.e., all the current nodes are located at the interior points of

terminals. Therefore, only the currents near the terminals are modified by decomposing (5.3a) using the same approach as voltage iterative equations. So, the modified iterative equation of currents near the source are

$$I_{1+\frac{1}{2}}^{n+\frac{3}{2}} = B_1 I_{1+\frac{1}{2}}^{n+\frac{1}{2}} - B_2 \frac{\Delta t}{\Delta z} L^{-1} \left(\sum_{j=1}^{S_b} a(j) \left(V_{j+1}^{n+1} - V_1^{n+1} \right) \right). \tag{5.19}$$

at $k = 1$ and,

$$I_{k+\frac{1}{2}}^{n+\frac{3}{2}} = B_1 I_{k+\frac{1}{2}}^{n+\frac{1}{2}} - B_2 \left(\sum_{j=1}^{k} (2j-1)\, a(j) \right)^{-1} \frac{\Delta t}{\Delta z} L^{-1} \left(\sum_{j=1}^{k} a(j) \left(V_{k+j}^{n+1} - V_{k-j+1}^{n+1} \right) \right). \tag{5.20}$$

at $k = 2, 3, \cdots, S_b$.

The modified iterative equation for currents at interior points and currents near the load are shown in (5.21) and (5.22), respectively.

$$I_{k+\frac{1}{2}}^{n+\frac{3}{2}} = B_1 I_{k+\frac{1}{2}}^{n+\frac{1}{2}} - B_2 \frac{\Delta t}{\Delta z} L^{-1} \left(\sum_{j=1}^{S_b} a(j) \left(V_{k+j}^{n+1} - V_{k-j+1}^{n+1} \right) \right). \tag{5.21}$$

at $k = S_b + 1, S_b + 2, \cdots, Nz - S_b, Nz - S_b + 1$.

$$I_{k+\frac{1}{2}}^{n+\frac{3}{2}} = B_1 I_{k+\frac{1}{2}}^{n+\frac{1}{2}} - B_2 \left(\sum_{j=1}^{Nz-k+1} (2j-1)\, a(j) \right)^{-1} \frac{\Delta t}{\Delta z} L^{-1} \left(\sum_{j=1}^{Nz-k+1} a(j) \left(V_{k+j}^{n+1} - V_{k-j+1}^{n+1} \right) \right). \tag{5.22}$$

at $k = Nz - S_b + 2, Nz - S_b + 3, \cdots, Nz$.

The evaluation of the updated voltage and current iterative equations is done using a bootstrapping approach. Firstly, the equations of voltage (5.11), (5.14), (5.16)-(5.18) are solved at a particular time with respect to previous values of currents and voltages. Then, the equations of current (5.19)-(5.22) are solved with respect to previous values of currents and initially evaluated voltages. The output of MRTD iterative equations is stabilized considering the Courant-Friedrich-Lewy (CFL) stability condition [101], [104] as

$$\Delta t \leq \frac{q \Delta z}{\vartheta} \tag{5.23}$$

where q represents a courant number that is computed using $q = \frac{1}{\sum_{j=1}^{S_b} |a(j)|} = \frac{\vartheta \Delta t}{\Delta z}$ and ϑ represents the phase velocity of propagation on the line.

According to CFL stability condition, the propagation time must be higher than the time step, over each cell.

5.4 Comparison and validation of the proposed MRTD model

The proposed MRTD model is validated by comparing the results with the industry standard HSPICE simulator and with the conventional FDTD model. The interconnect-load is driven by considering the symmetric CMOS driver. For 32 nm technology node, an interconnect line of length 1 mm is chosen with a realistic global interconnect topology; the design parameters and interconnect dimensions of the DIL system are adopted from [90].

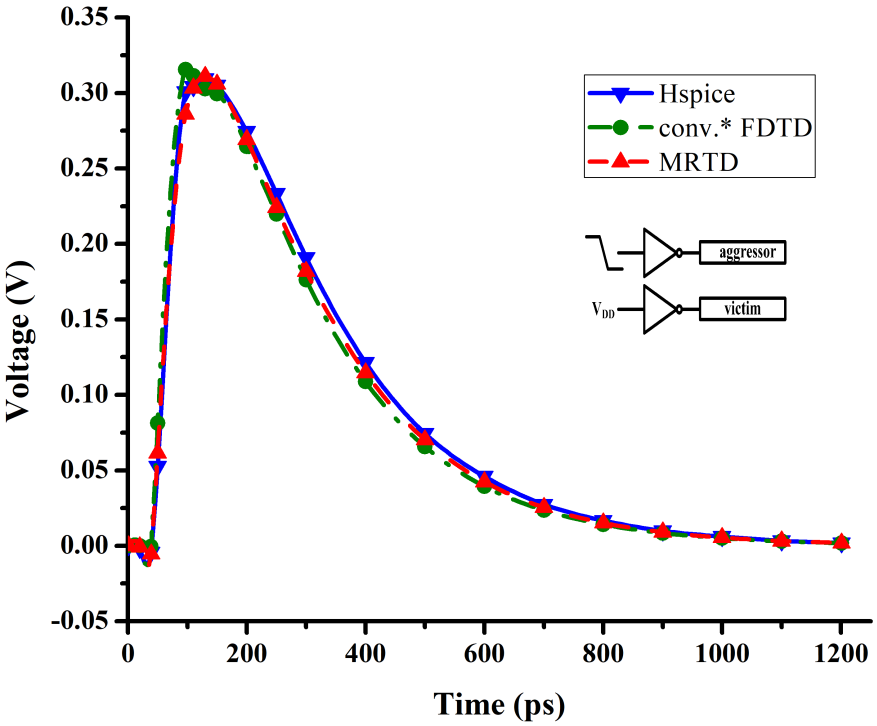
For an interconnect line width of 48 nm, the values of d_1, and d_M are considered to be 14.4 nm and 48 nm, respectively, from Figure 5.1. For MWCNT, the total number of shells ($M = 50$) is calculated using (5.24) [89].

$$M = 1 + int\left[\frac{(d_M - d_1)}{2\delta}\right] \tag{5.24}$$

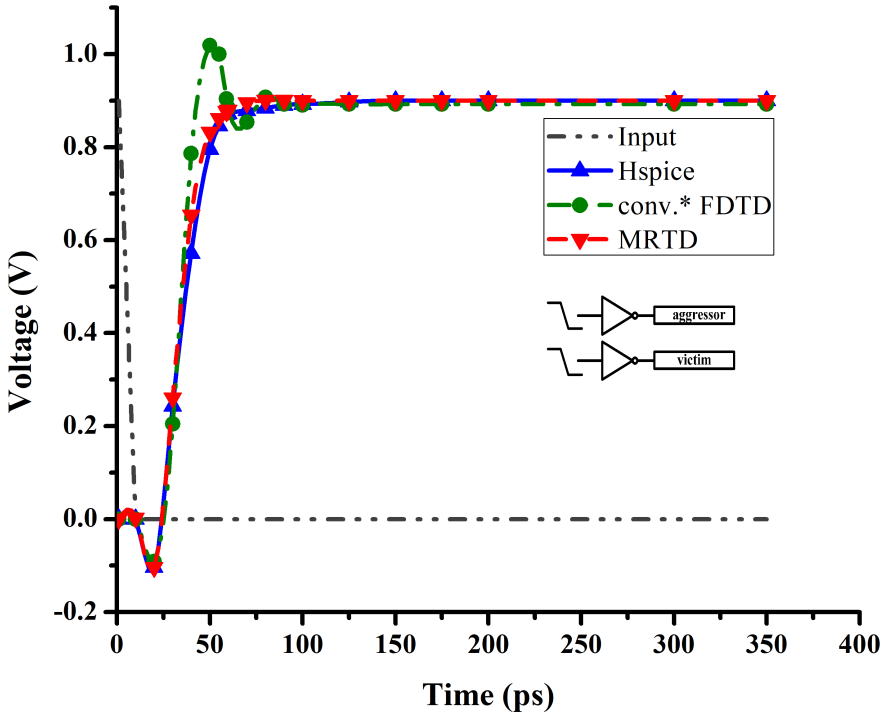
The metal contact resistance per shell is considered as 3.2 kΩ [90]. The line aspect ratio (T/W) is considered as 3 by using the design structure of practical global interconnect, i.e., each interconnect line comprises of three MWCNTs along its thickness. The value of inter-layer dielectric constant is 2.25 and load capacitance of the line is considered to be 2 fF. Using the setup mentioned above, for two mutually coupled interconnect lines, the following distributive RLC parasitics are used in the simulation.

$$\mathbf{R} = \begin{bmatrix} 653.67 & 0 \\ 0 & 653.67 \end{bmatrix} \frac{\text{k}\Omega}{\text{m}},\ \mathbf{L} = \begin{bmatrix} 14.83 & 0.61 \\ 0.61 & 14.83 \end{bmatrix} \frac{\mu\text{H}}{\text{m}},\ \mathbf{C} = \begin{bmatrix} 93.33 & -71.50 \\ -71.50 & 93.33 \end{bmatrix} \frac{\text{pF}}{\text{m}}$$

The space (Δz) and time (Δt) discretizations are computed to be less than 3.428×10^{-4} m and less than 4.9680×10^{-12} s for q=0.6, respectively, for MRTD. Similarly, Δz and Δt for FDTD are computed to be less than 3.428×10^{-4} m and less than 8.28×10^{-12} s, respectively.


Hspice
conv.* FDTD
MRTD
aggressor
V_{DD}
victim
Voltage (V)
Time (ps)
0.35
0.30
0.25
0.20
0.15
0.10
0.05
0.00
-0.05
0
200
400
600
800
1000
1200

(a)


Input
Hspice
conv.* FDTD
MRTD
aggressor
victim
Voltage (V)
Time (ps)
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0.8
0.6
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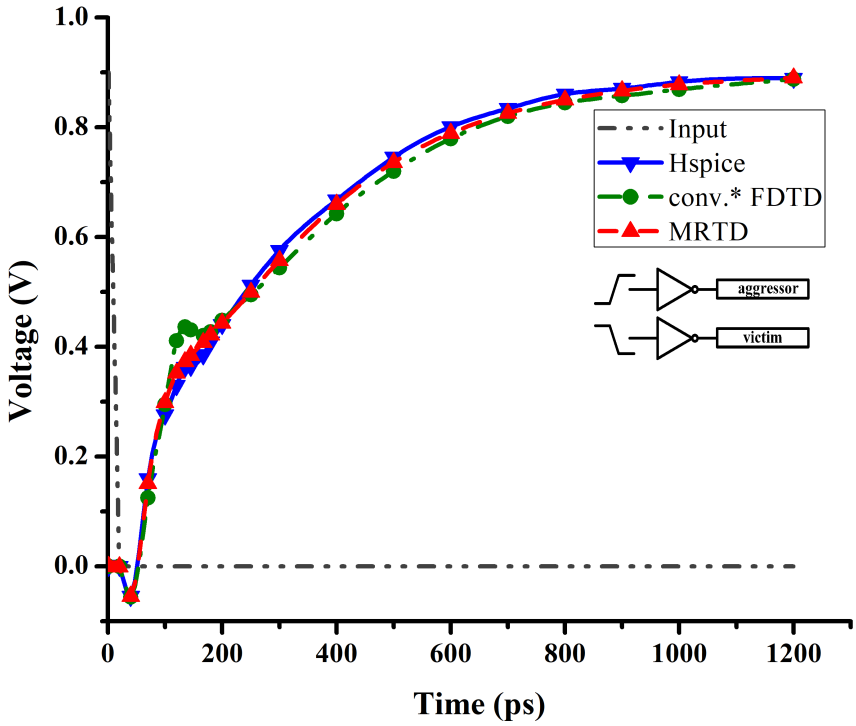
200
250
300
350
400

(b)



(c)

Figure 5.4: Comparison of the transient response of line 2 during the (a) functional switching (b) dynamic in-phase and (c) out-phase switching.

5.4.1 Inclusive crosstalk analysis of two mutually coupled MWCNT interconnects

The performance analysis of two mutually coupled MWCNT interconnects is conducted by considering line 1 as the aggressor line and line 2 as the victim line of Figure 5.2. The inclusive crosstalk effects such as functional and dynamic crosstalk effects are studied with HSPICE, conventional FDTD and the proposed MRTD model. The functional crosstalk effect is studied by switching the input of line 1 (aggressor) from 0.9 V (V_{DD}) to 0 V while maintaining the line 2 (victim) at quiescent mode. The effect of dynamic crosstalk by simultaneous switching of both lines , either in-phase or out-phase, is also studied. The transient waveforms resulted based on the above conditions are compared at the far end terminal on line 2 (victim). The functional, dynamic in-phase and out-phase transient response on line 2 (victim) are illustrated in Figure 5.4a-5.4c. From the Figure 5.4b and 5.4c, it can be seen that a peak results in the response of line 2 as the conventional FDTD method has higher dispersion errors. Nevertheless, with its significant advantages in numerical dispersion characteristics [98, 99], the proposed

MRTD model shows superiority over the conventional FDTD model in terms of accuracy. Figure 5.4c illustrates the effect of Miller coupling capacitance (C_{12}) resulting in more time for signal transition during the out-phase switching, than for in-phase switching. The simulation results of the proposed MRTD model matches accurately with those of HSPICE and dominates the conventional FDTD method for all the cases of input switching.

The computational error associated with the estimation of dynamic crosstalk effects over line 2 (victim) for the conventional FDTD and the proposed MRTD model with respect to HSPICE are demonstrated in Table 5.1. The robustness of the proposed model is validated by testing it for different load capacitance (C_L) resulting in the average error of less than 0.2% and less than 0.1% for the estimation of dynamic in-phase and out-phase delays, respectively.

5.4.2 Extensions and observations

The proposed MRTD model is also extended to three mutually coupled lines as shown in Figure 5.2 by considering line N as line 3 and the same is validated using HSPICE. Here, line 2 is considered as a victim line, whereas lines 1 and 3 are considered as aggressor lines, for the analysis. The three mutually coupled interconnect distributed line parameters are expressed as equation (5.2) in the form of 3×3 matrix.

Figure 5.5 illustrates the response of dynamic crosstalk switching on line 2 (victim) using HSPICE, conventional FDTD model and the proposed MRTD model for three coupled interconnect lines considering different test cases (test case-1 $\rightarrow$ test case-5). Also, the response of functional crosstalk switching on line 2 (victim) is illustrated as in test case-6 and test case-7 of Figure 5.5. The comparison shows that the simulation results of the proposed MRTD model are in good agreement with those of HSPICE. From Figure 5.5, it can be seen that a peak overshoot/undershoot occurs in the response of line 2 as the conventional FDTD method has higher dispersion errors. Nevertheless, the numerical dispersion properties [98, 99] in MRTD model acts as added advantage over the conventional FDTD model for achieving better accuracy. The computational error obtained using the proposed MRTD and conventional FDTD model with respect to HSPICE, for estimating the crosstalk induced 50% delay due to lines 1 and 3 (aggressors) on line 2 (victim) is presented in Table 5.2. Table 5.2 also shows that the average errors using the proposed MRTD and the conventional FDTD model are 0.23% and 0.6%, respectively. Also, it is observed that with an increase in the test case switching, the dynamic crosstalk delay increases. This happens since the propagation of the signal along the line is extremely affected by the Miller capacitance when the aggressor and the victim lines are switching

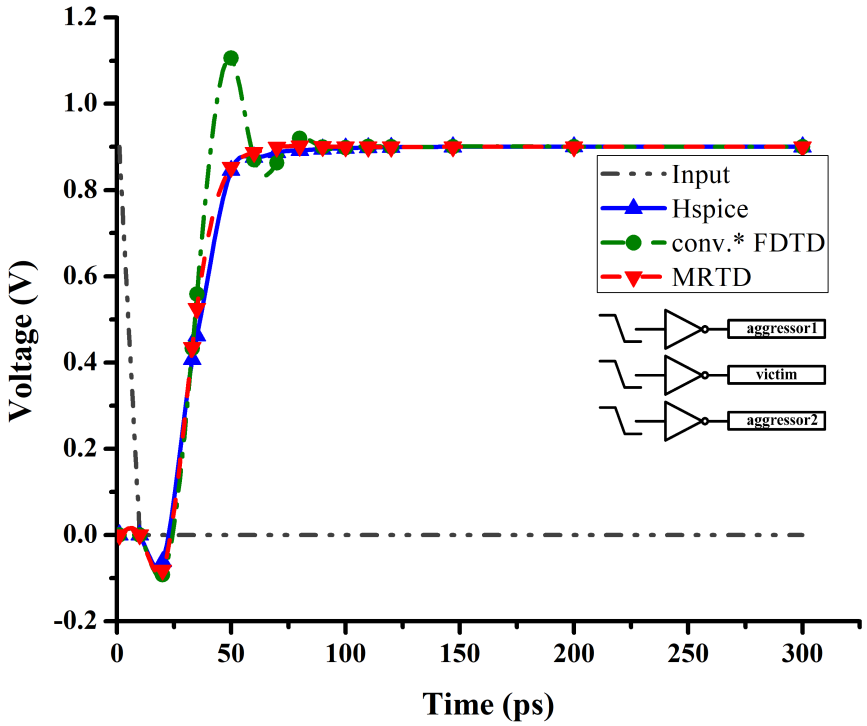
Table 5.1: Computational Error Associated with the Estimation of Dynamic Crosstalk Effects on Line 2 (Victim).

Load Capacitance C_L (fF)	**Dynamic in-phase delay (ps)**					**Dynamic out-phase delay (ps)**				
				error (%)					**error (%)**	
	HSPICE	**MRTD**	**conv.* FDTD**	**MRTD**	**FDTD**	**HSPICE**	**MRTD**	**conv.* FDTD**	**MRTD**	**FDTD**
2	29.1	28.85	28.8	0.86	1.03	199.5	200	201	−0.25	−0.75
10	44.1	43.92	43.8	0.41	0.68	212.5	212	211.5	0.24	0.47
20	60.9	61.4	60.35	−0.82	0.9	229.5	228.6	227.9	0.39	0.7
30	78.7	79	79.1	−0.38	−0.51	246.5	247.5	245.3	−0.4	0.49
40	107.5	107.1	106.95	0.37	0.51	261.5	260.7	260	0.31	0.57
50	123.5	123.1	123	0.32	0.41	279.5	280.7	278.25	−0.43	0.45

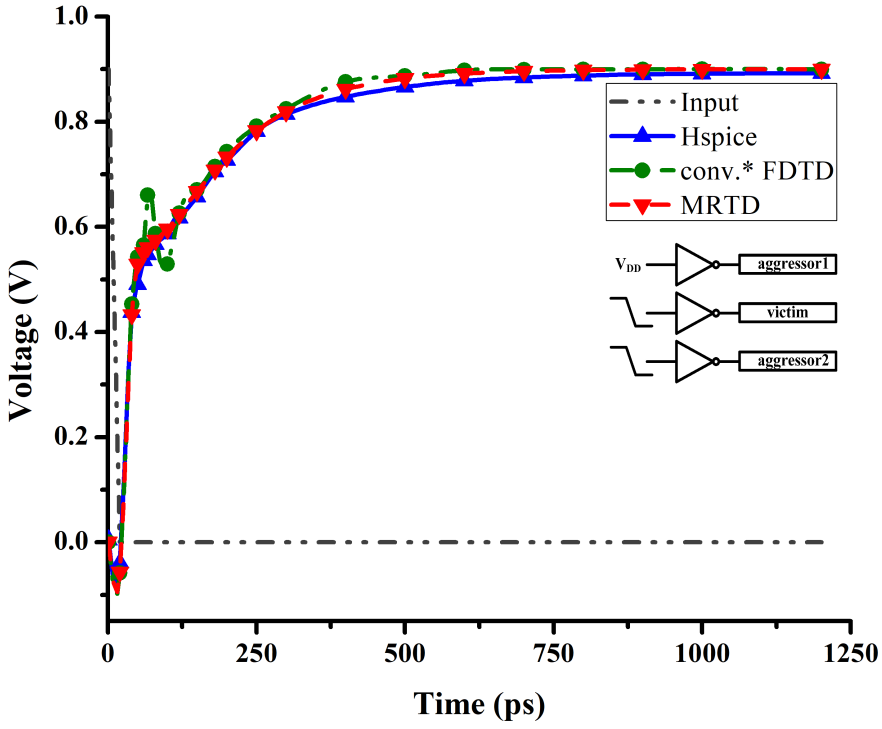
Table 5.2: Computational Error Involved for 50% Propagation Delay on Line 2 of Three Mutually Coupled Lines.

Input signal switching modes				**Propagation delay (ps) on Line 2 (Victim)**				
							error (%)	
Test Cases	**Line 1 (Aggressor)**	**Line 2 (Victim)**	**Line 3 (Aggressor)**	**HSPICE**	**MRTD**	**conv.* FDTD**	**MRTD**	**conv.* FDTD**
1	$V_{DD} \rightarrow 0$	$V_{DD} \rightarrow 0$	$V_{DD} \rightarrow 0$	27.9	27.84	27.65	0.22	0.9
2	V_{DD}	$V_{DD} \rightarrow 0$	$V_{DD} \rightarrow 0$	35.7	35.67	35.35	0.084	0.98
3	$0 \rightarrow V_{DD}$	$V_{DD} \rightarrow 0$	$V_{DD} \rightarrow 0$	66.2	65.85	65.81	0.53	0.59
4	V_{DD}	$V_{DD} \rightarrow 0$	$0 \rightarrow V_{DD}$	223.5	223.2	221.7	0.134	0.81
5	$0 \rightarrow V_{DD}$	$V_{DD} \rightarrow 0$	$0 \rightarrow V_{DD}$	320.5	319.9	321.5	0.19	−0.312

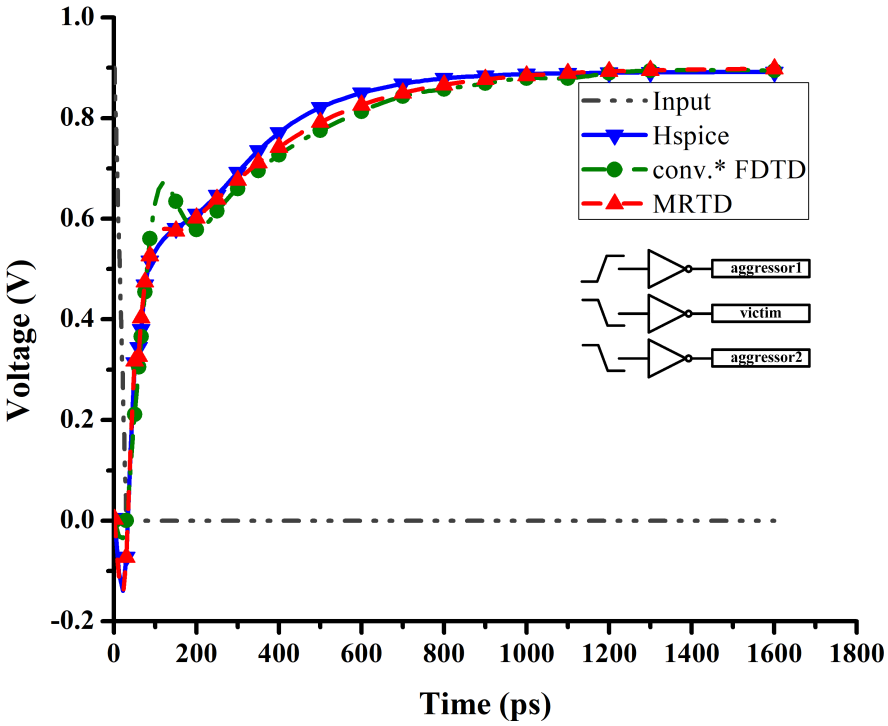
conv.*–conventional



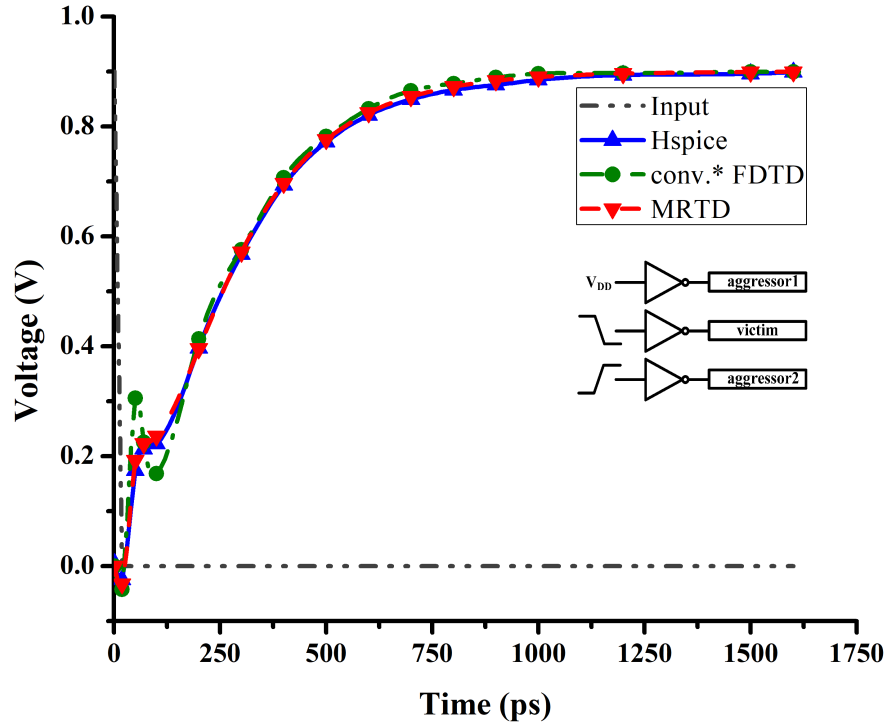
(a) test case-1



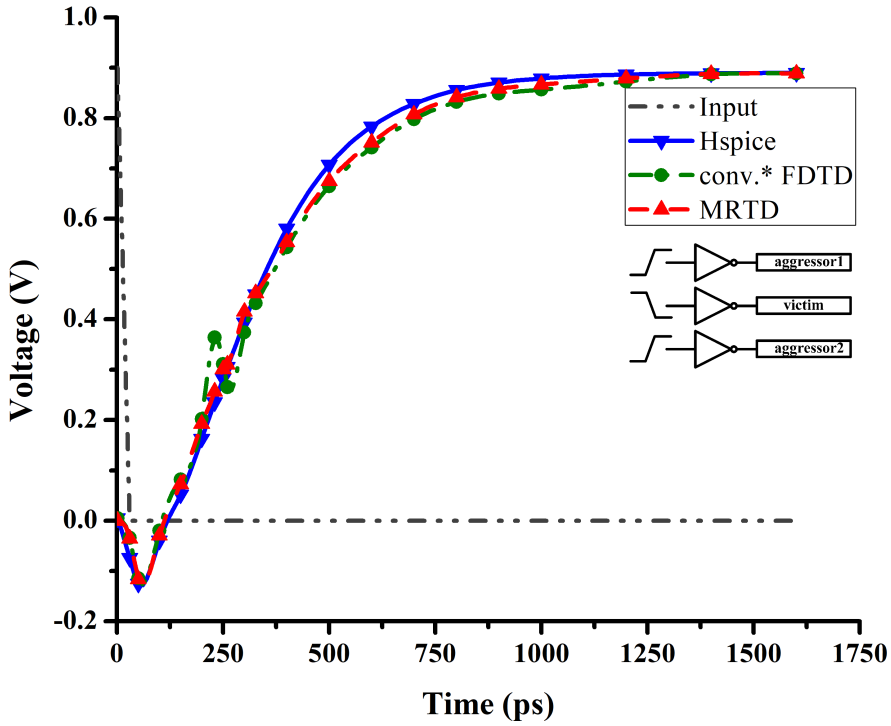
(b) test case-2



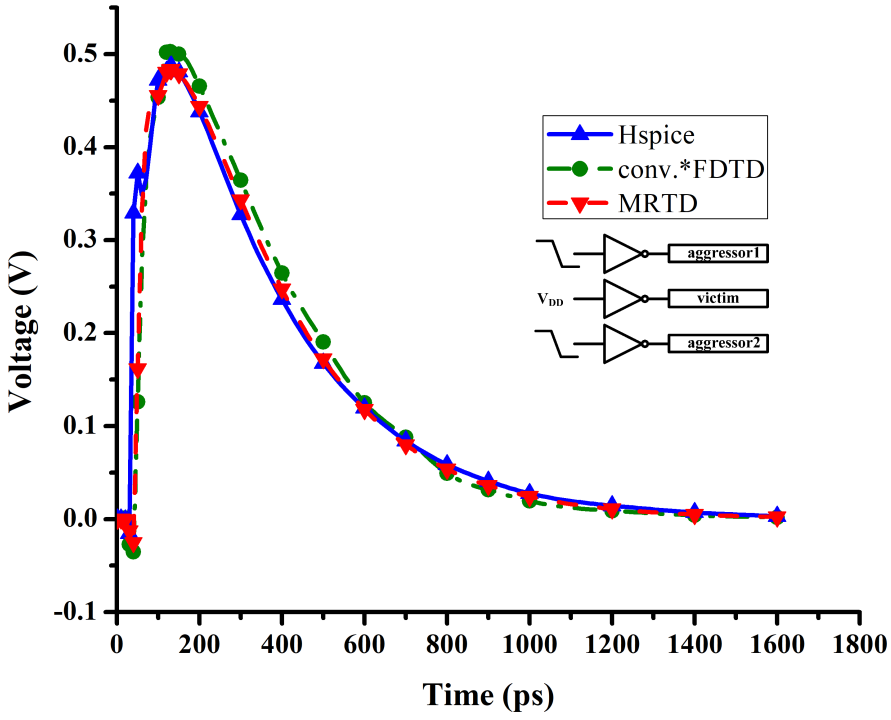
(c) test case-3



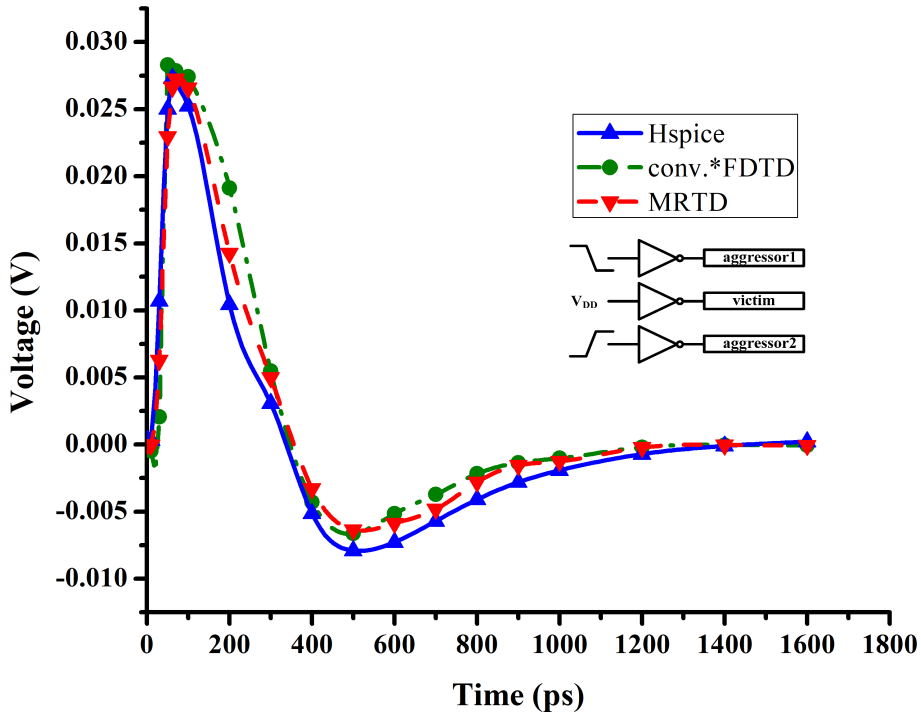
(d) test case-4



(e) test case-5



(f) test case-6



(g) test case-7

Figure 5.5: Transient response on line 2 (victim) due to lines 1 and 3 (aggressors) for three-coupled interconnects.

in the opposite directions. Therefore, for line 2 (victim), among all input switching modes, test case-5 must be the worst-case delay in high-speed VLSI interconnects. The computational time

Table 5.3: Comparison of Computational Efforts Between the Methods.

	Computational time (s)		
No. of Coupled lines \ **Methods**	**HSPICE**	**MRTD**	**conv.* FDTD**
Two	0.69	0.385	0.322
Three	0.78	0.565	0.496

conv.*–conventional

for the HSPICE, the proposed MRTD and the conventional FDTD model is measured using the Intel Core i7 processor - 3770 CPU@3.40 GHz. Table 5.3 shows the corresponding compu-

tational effort of each model. It is observed that the CPU run-time of HSPICE is higher than both MRTD and conventional FDTD models, but MRTD is slightly slower than conventional FDTD, due to increased number of iterations for better accuracy. Hence, there exists a trade-off between simulation time and accuracy.

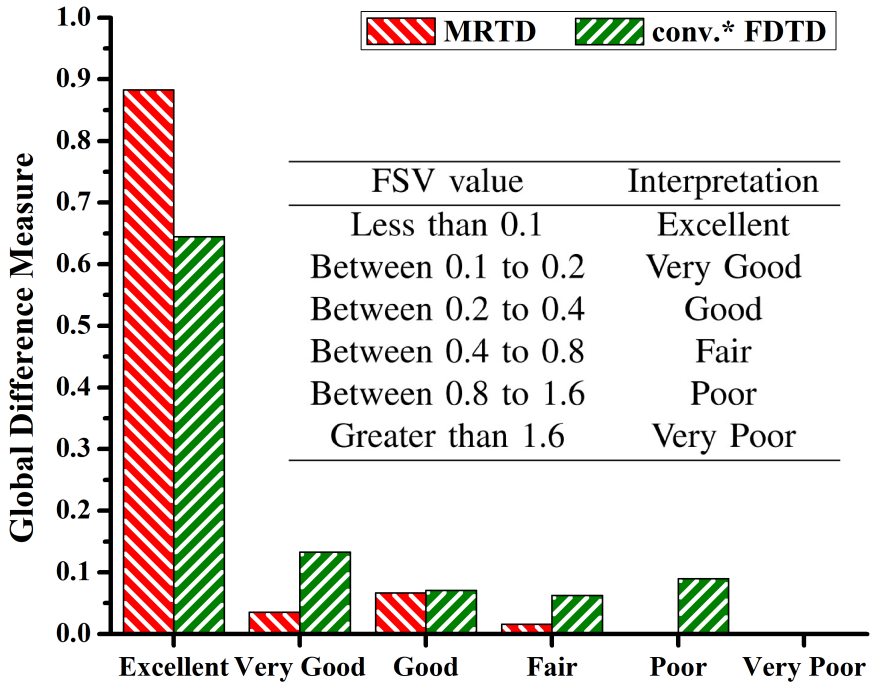


Figure 5.6: Histogram from the data-sets of Figure 5.5a using feature selective validation (FSV) tool.

Finally, for significant comparison of the quality, the data-sets from Figure 5.5a are represented in the form of natural language descriptor (excellent, very good, good, fair, poor, and very poor). The histogram of the global difference measure (GDM) is generated using the feature selective validation (FSV) tool [113] as shown in Figure 5.6. The simulation results of the proposed MRTD model demonstrates significant match with those of HSPICE when compared to conventional FDTD method.

5.5 Summary

This chapter presented an efficient MRTD method to analyze the inclusive crosstalk effects in a coupled MWCNT interconnect, which is considered for future VLSI interconnect applications, owing to their extraordinary mechanical, electrical and thermal properties. Therefore, in this work, the conventional copper interconnect is replaced with the MWCNT interconnect for

the analysis of crosstalk noise effects. It has been observed that the MRTD method is in close agreement with the result obtained using HSPICE and that it dominates over the FDTD in terms of accuracy. Moreover, the CPU run-time for the proposed model is observed to be significantly less when compared to HSPICE. Also, the validation of the MRTD model with feature selective validation tool proves its accuracy and efficiency.

Chapter 6

Conclusions And Future Scope

6.1 Conclusions

The thesis presents an accurate MRTD method for analyzing the effect of the performance parameters on propagation delay and crosstalk noise in mutually coupled on-chip interconnects. By using the proposed and FDTD method, the effect of the peak noise and delay as a function of coupling parasitics has been computed and compared with that of obtained results using the HSPICE tool for the two coupled copper interconnect lines driven by the linear resistive driver at 130-nm technology node. It is observed that the proposed MRTD model captures the behaviour of delay and crosstalk noise on victim line against coupling parasitics, which is in close agreement with the result obtained using HSPICE and that it dominates over the FDTD in terms of accuracy. Compared with HSPICE, average errors of <1 % and <2 % are obtained for the proposed method and FDTD, respectively. Furthermore, almost 100 % accuracy is maintained for a broad frequency range.

The proposed model is then extended to include the non-linear characteristics of the CMOS driver in the DIL system for 32-nm technology node. The CMOS driver analyzed using the *n*-th-power law model and coupled distributive RLC interconnects are modeled using the MRTD method. For a different number of test cases, the proposed method shows an average error of 0.14 % and 1.9 % with respect to the peak crosstalk noise and the peak noise timing, respectively, compared to HSPICE results. For three mutually-coupled interconnect lines, the average error for the proposed model is observed to be less than 1 % whereas the average error for the conventional FDTD method is more than 3 %. Also, a peak is resulted

in the response using the conventional FDTD method due to its numerical dispersion properties. However, the proposed MRTD method with its great advantages in numerical dispersion properties produces accurate results. It is observed that the proposed MRTD method is in good agreement with HSPICE simulations and dominates the conventional FDTD method in terms of accuracy. Besides, the proposed MRTD method is more time efficient than HSPICE, although the elapsed CPU time of the proposed MRTD method is higher than the conventional FDTD method. Further, the proposed method is highly useful for precise estimation of crosstalk in the next-generation VLSI interconnects.

Further down scaling of interconnect dimensions has made surface scattering and grain boundary scattering more prominent, resulting in increased resistivity of Cu material. Therefore, the requirements of novel material employed as VLSI interconnect have increased. In recent times, Carbon nanomaterials such as carbon nanotubes (CNTs) and graphene nanoribbons (GNRs) form one of the most promising candidates proposed as a substitute for Cu interconnects in advanced VLSI circuits.

So, we modeled the CMOS gate driven mutually coupled MWCNT interconnects at 32-nm technology node to analyze the crosstalk effects. The n-th-power law model is used to model the CMOS driver. The simulation results of the proposed MRTD and the conventional FDTD with respect to HSPICE validated that the MRTD method is in good agreement with HSPICE. The average error is observed to be less than 0.2% and 0.3% for two-coupled and three-coupled MWCNT interconnects, respectively. It can be seen that a peak overshoot/undershoot occurs in the response of line 2 as the conventional FDTD method has higher dispersion errors. Nevertheless, the numerical dispersion properties in MRTD model acts as an added advantage over the conventional FDTD model for achieving better accuracy. The CPU run-time for the MRTD model is observed to be significantly less when compared to HSPICE. The analysis has been carried out on two coupled and three-coupled interconnects, but can also be extended to N-mutually coupled interconnects. Furthermore, the validation of the proposed model with future selective validation (FSV) proves its accuracy and efficiency for analyzing the crosstalk effects in mutually coupled MWCNT interconnects.

6.2 Future Scope

As future work, the performance of Through Silicon Vias (TSVs) in ICs, i.e., typical time-domain effects include TSV delay, crosstalk, transmission line effects, and noise-on-delay

effects can be analyzed using the multi-resolution time-domain (MRTD) method. Also, it is possible to address the issues of electromagnetic compatibility (EMC) and electromagnetic interference (EMI) of on-chip interconnects.

Further, as the MRTD method is conditionally stable based on Courant-Friedrichs-Lewy (CFL) condition, a new scheme needs to be developed for unconditional stability of MRTD method to address the issues of on-chip interconnects.

Appendix A

Daubechies' scaling function is given as

$$\phi(z) = \begin{cases} 1 & for\,|z| < \frac{1}{2} \\ \frac{1}{2} & for\,|z| = \frac{1}{2} \\ 0 & for\,|z| > \frac{1}{2} \end{cases} \tag{A.1}$$

If $k \neq k'$, then there is no overlaps between $\phi_k(z)$ and $\phi_{k'}(z)$; so

$$\int_{-\infty}^{+\infty} \phi_k(z)\,\phi_{k'}(z)\,dz = 0 \tag{A.2}$$

If $k = k'$,

$$\begin{aligned} \int_{-\infty}^{+\infty} \phi_k(z)\,\phi_{k'}(z)\,dz &= \int_{-\infty}^{+\infty} \phi^2\left(\frac{z}{\Delta z} - k\right) dz \\ &= \Delta z \int_{-\infty}^{+\infty} \phi^2\left(\frac{z}{\Delta z} - k\right) d\left(\frac{z}{\Delta z}\right) \\ &= \Delta z \int_{-\frac{1}{2}}^{\frac{1}{2}} \phi^2(z')\,dz' \\ &= \Delta z \int_{-\frac{1}{2}}^{\frac{1}{2}} 1\,dz' \\ &= \delta_{k,k'}\Delta z \end{aligned} \tag{A.3}$$

The Fourier transform pair of Daubechies' scaling function is

$$\widehat{\phi}(\omega) = \int_{-\infty}^{\infty} \phi(z)\,e^{-j\omega z}dz \tag{A.4a}$$

and

$$\phi(z) = \frac{1}{2\pi}\int_{-\infty}^{\infty} \widehat{\phi}(\omega)\, e^{j\omega z} d\omega \tag{A.4b}$$

It can be verified that the Fourier transform of the scaling function [109]

$$\widehat{\phi}(\omega) = \left(\frac{\sin\frac{\omega}{2}}{\frac{\omega}{2}}\right)^4 \frac{1}{\sqrt{1-\left(\frac{4}{3}\right)\sin^2\left(\frac{\omega}{2}\right)+\left(\frac{2}{5}\right)\sin^4\left(\frac{\omega}{2}\right)-\left(\frac{4}{315}\right)\sin^6\left(\frac{\omega}{2}\right)}} \tag{A.5}$$

Using the properties of Fourier integral, it is possible to write

$$\begin{aligned}
\int_{-\infty}^{+\infty} \phi_k(z)\frac{\partial \phi_{k'+\frac{1}{2}}(z)}{\partial z} dz &= \int_{-\infty}^{+\infty} dz \left[\left(\frac{1}{2\pi}\int \widehat{\phi}(\omega)\, e^{-j\omega k + j\omega z} d\omega\right)\left(\frac{1}{2\pi}\int \frac{\partial}{\partial z}\widehat{\phi}(\omega')\, e^{-j\omega'\left(k'+\frac{1}{2}\right)} e^{j\omega' z} d\omega'\right)\right] \\
&= \int\int d\omega d\omega' \int_{-\infty}^{\infty} dz \left[\frac{1}{2\pi} e^{jz(\omega+\omega')}\right] \frac{j\omega'}{2\pi}\widehat{\phi}(\omega')\,\widehat{\phi}(\omega)\, e^{-j(\omega k)-j\omega'\left(k'+\frac{1}{2}\right)} \\
&= \frac{1}{2\pi}\left(\int_{-\infty}^{\infty}\widehat{\phi}(\omega)\, e^{-j\omega k} d\omega\right)\left(\int \delta(\omega+\omega')\, j\omega'\widehat{\phi}(\omega')\, e^{-j\omega'\left(k'+\frac{1}{2}\right)} d\omega'\right)
\end{aligned}$$

at $\omega' = -\omega$

$$\begin{aligned}
&= \frac{1}{2\pi}\int_{-\infty}^{\infty} \widehat{\phi}(\omega)\, e^{-j\omega k}\,(-j\omega)\,\widehat{\phi}(-\omega)\, e^{j\omega\left(k'+\frac{1}{2}\right)} d\omega \\
&= \frac{1}{\pi}\int_0^{\infty} \omega\left|\widehat{\phi}(\omega)\right|^2 \sin\left[\omega\left(k'-k+\frac{1}{2}\right)\right] d\omega \\
&= \sum_{-\infty}^{\infty} a(i)\,\delta_{k+i,k'}
\end{aligned} \tag{A.6}$$

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List of Publications

International Journals

1. R. Shashank and N. Bheema Rao,“A Multiresolution Time Domain (MRTD) method for crosstalk noise modeling of CMOS-gate-driven coupled MWCNT interconnects", *IEEE Transactions on Electromagnetic Compatibility*, 2019, DOI:10.1109/TEMC.2019.2903728. **(SCI-Indexed)**

2. R. Shashank and N. Bheema Rao,“An Efficient MRTD Model for the Analysis of Crosstalk in CMOS-Driven Coupled Cu Interconnects", *Radioengineering*,Vol 27, No 2, pp.532-540, 2018 DOI:10.13164/re.2018.0532. **(SCI-Indexed)**

3. R. Shashank and N. Bheema Rao,“A Novel MRTD model for Signal Integrity Analysis of Resistive Driven Coupled Copper Interconnects", *COMPEL - The international journal for computation and mathematics in electrical and electronic engineering*,Vol 37, No 1, pp.189-207, 2018, DOI:10.1108/COMPEL-12-2016-0521. **(SCI-Indexed)**