SOME INVESTIGATIONS ON HIGH SPEED SERIAL INPUT OUTPUT CIRCUIT STRATEGIES FOR BACKPLANE CHANNELS

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by

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Dedicated to

I dedicate this thesis to my mother**, Annamaraju *Shakunthala***, for her limitless love,prayers and blessings without which I would never stand here, to my father ***,Devulapalli Rajendra Prasad***, for standing by me during my difficult times and my Dear wife ***Devulapalli Lakshmi Kalyani*** and two precious gifts from almighty, ***Snigdha Sharma*** and ***Keshav Sharma***

DECLARATION

This is to certify that the work presented in this thesis entitled "**Some Investigations on High Speed Serial Input Output Circuit Strategies for Backplane Channels**" is a bonafide work done by me under supervision of **Dr. P Sreehari Rao**, Professor, Department of Electronics and Communication Engineering, National Institute of Technology Warangal, India and was not submitted elsewhere for the award of any degree.

I declare that this written submission represents my ideas in my words and where others' idea or words have been included, I have adequately cited and referenced the original sources. I also declare that I have adhered to all principles of academic honesty and integrity and have not misrepresented or fabricated or falsified any idea / data / fact / source in my submission. I understand that any violation of above will be a cause for disciplinary action by the Institute and can also evoke penal action from the sources which have thus not been properly cited or from whom proper permission has not been taken when needed.

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CERTIFICATE

This is to certify that the thesis entitled "**Some Investigations on High Speed Serial Input Output Circuit Strategies for Backplane Channels**", which is being submitted by **Mr . D Pavan Kumar Sharma (Roll no:701248),** in partial fulfillment for the award of the degree of Doctor of Philosphy to the Department of Electronics and Communication Engineering of National Institite of Technology,Warangal,is a record of bonafied research work carried out by his under my supervision and has not been submitted elsewhere for any degree.

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ABSTRACT

The technology scaling has increased the computational efficiency of on-chip devices while approaching almost the transistor transition frequency (f_T) on the data rate. However, this advantage is now constrained by the transfer medium which consists mostly of traces of wires on printed circuit board (PCB) of backplane channel. The high-speed serial links consists of transmitter, receiver, Phase Locked Loop (PLL), clock data recovery circuit and the channel. The channel or backplane consists of various materials such as line card and backplane trace and vias. The bandwidth required to transfer the data at high-speed can be intra-chip or inter-chip (high-speed serial link) depending upon the applications, such as server access across internet, display devices and gaming consoles, which is limited by dielectric loss, skin effect and impedance mismatches. The problems associated with high data transfer rate are conventionally addressed by employing parallel channels and logic duplication. However, both these options increase the pin count simultaneously increasing the overall power consumption which needs to be minimized for efficient data transfer. There is a need to transfer data at a very high rate (i.e., > 2GS/s) through single channel meeting constraints such as minimum power consumption, reflection loss, channel attenuation in addition to the errors induced by clock jitter and skew variations. This makes the design of high-speed serial link Input Output (I/O) for backplane channels a challenging field of research. In this thesis an attempt is made to develop circuit strategies for clock generation, clock recovery, on-die termination and equalization suitable for data-transfer at high speeds across backplane channels.

Equalization and termination matching can be easily achieved in feed forward equalizer with current mode logic(CML). However it suffers from poor efficiency, hence an open drain CML architecture is chosen with the termination implemented using cross coupled transistors minimizing power consumption. The designed on die termination is used to drive data across a 32inch backplane at 10Gb/s with swing of $0.6V_{p-p}$ and efficiency of 0.603pJ/bit and generate random jitter of 3.25ps which meets the jitter and swing specifications of 10BaseKR standard. This design achieves better performance by striking a tradeoff between power consumption of 0.6mW and jitter of 3.25ps on competing with state of art literature.

Comparator constitutes an important subsystem of the receiver corresponding to high speed serial data link. The receiver driver is primarily affected by the bit error rate and input referred noise of the comparator. Noise fed back(kick back noise) associated with regenerative comparators demands significant power without which eye opening is constrained leading to poor performance against noise. Hence, a gain boosted cascode amplifier is added to the cross coupled regenerative pair which further increases the output impedance which in turn decreases the input referred noise. This results in reduction of the output impedance of the pre-amplifier stage of the designed circuit. The designed gain boosted dynamic comparator has resolving capability of 5mV in 0.133ns. The gain boosted comparator has kick back noise of 29µ V with input referred noise of 1.75mV.

Serial data link operating at high speed require high frequency clock. The jitter associated with clock needs to comply with chosen 10base KR standard. When phase locked loop is employed in clock and data recovery circuitry, the initial phase acquisition loop needs to have a minimum phase error which is mainly dependent on minimum phase difference that can be detected by the phase detector. When reference less phase locked loop is used, the feedback clock transitions are to be in synchronous with data. A modified phase detector is presented to reduce the effects of phase error variation of the recovered clock. The modified phase detector has a mux which increases the minimum resettable delay in the feedback path. The addition of multiplexer increases the minimum width of up and down signals from the phase detector. The designed phase locked loop has a phase noise of -114dBc/Hz at an offset of 1MHz with power consumption of 6.64mW. It exhibits better FOM of -192.4 as compared to that of counterpart cited in the literature[-185] T.H Lee et .al.

A clock and data recovery circuit is presented that employs modified dual loop architecture. The proposed circuit employs a asynchronous input latch signal in addition to clock which aids to latch the input data. The main advantage of the modified latch is that the regeneration phase begins immediately after the sampling phase. The designed clock and data recovery circuit has recovered clock jitter of 4.2ps with power consumption of 27mW which is lower than the state of art cited in literature.

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List of Abbreviations

ADC	**A**nalog to **D**igital **C**onverter
AEQ	**A**daptive **E**qualizer
BGR	**B**and **G**ap **R**eference
BER	**B**it **E**rror **R**ate
CMOS	**C**omplementary **M**etal **O**xide **S**emiconductor
CDR	**C**lock and **D**ata **R**ecovery
CTLE	**C**ontinuous **T**ime **L**inear **E**qualizer
CP	**C**harge **P**ump
CGA	**C**ommon **G**ate **A**mplifier
CML	**C**urrent **M**ode **L**ogic
DMT	**D**iscrete **M**ulti-**T**one
DLL	**D**elay **L**ocked **L**oop
DAC	**D**igital to **A**nalog **C**onverter
DDJ	**D**ata **D**eterministic **J**itter
DFE	**D**ecision **F**eedback **E**qualizer
EOM	**E**ye **O**pening **M**onitor
FOM	**F**igure **O**f **M**erit
FO4	**F**an **O**ut of **4**
FFE	**F**eed **F**orward **E**qualizer
FIR	**F**inite **I**mpulse **R**esponse
FR4	**F**lame **R**etardant
FLL	**F**requency **L**ocked **L**oop
FD	**F**requency **D**etector
HF	**H**igh **F**requency
ITRS	**I**nternational **T**echnology **R**oadmap for **S**emiconductors
IC	**I**ntegrated **C**ircuit
ISI	**I**nter **S**ymbol **I**nterference
IIR	**I**nfinite **I**mpulse **R**esponse

I/O	**I**nput/**O**utput
KBN	**K**ick **B**ack **N**oise
LVZ	**L**ow **V**oltage **Z**ero
LF	**L**oop **F**ilter
MOSFET	**M**etal **O**xide **S**emiconductor **F**ield **E**ffect **T**ransistor
NC	**N**oise **C**ancellation
NLC	**N**on **L**inear **C**ancellation
NRZ	**N**on **R**eturn to **Z**ero
ODT	**O**n **D**ie **T**ermination
PLL	**P**hase **L**ocked **L**oop
PAM4	**P**ulse **A**mplitude **M**odulation **4**-level
PD	**P**hase **D**etector
PFD	**P**hase **F**requency **D**etector
PVT	**P**rocess **V**oltage **T**emperature
PAL	**P**hase **A**cquisition **L**oop
PSRR	**P**ower **S**upply **R**ejection **R**atio
PCB	**P**rinted **C**ircuit **B**oard
Q	**Q**uality **F**actor
RJ	**R**andom **J**itter
RL	**R**eflection **L**oss
SNR	**S**ignal to **N**oise **R**atio
SST	**S**elf **T**ermination
SS-LMS	**S**ign-**S**ign **L**east **M**ean **S**quare
SFF	**S**um **F**eedback **F**ilter
SB	**S**pectrum **B**alancing
UI	**U**nit **I**nterval
VCO	**V**oltage **C**ontrolled **O**scillator
VM	**V**oltage **M**ode

List of Symbols

c	Speed of light
D	Wire diameter
P_r	Wire resistivity
f_T	Transition Frequency of Transistor for specific Technology
tanα	Loss tangent
ε_r	Relative permittivity
α	Pre-emphasis coefficient

Chapter 1

Introduction

1.1 Motivation

The exponential growth of data computation on chip coupled by device scaling has boosted the performance of many digital circuits. High-speed data transfer with power efficiency forms the focus of many speed communications architectures. The performance of high-speed serial I/O circuits are measured in terms of bit error rate (BER). The bit error rate is limited by the bandlimited characteristics of the communication medium which requires compensation at both receiver and transmitter to improve the signal integrity aspects of the high-speed I/O design.

The explosive growth of many high-speed data computation applications such as cloud storage/computation, sensor networks, the required data rate computed from ITRS shows above >70Gb/s in a span of 10 years, which proportionally keeping lower power bounds has motivated the serial-link architects to look for energy-efficient high speed serial link.

The band-limited nature of the channel causes large inter-symbol interference (ISI) and in-addition to impedance mismatches causes reflections which degrade the signal reception at the receiver. To deal with attenuation caused by channel, equalizers are being implemented at the transmitter and receiver. At very high data-rates, the amount of pre-emphasis and reflection loss coefficient varies with both frequency and channel length, this motivated the high –speed serial link architects to model and design energy –efficient circuit topologies.

1.2 Backplane channel

The data-rates are previously very less attenuated by optical fiber cables. When being used for chip –to-chip data transfer it is limited by the performance of integrated photo detectors. The focus of this thesis is on copper channels. The backplane channels are composite of various materials such as line card trace, backplane trace, package and line card vias, and backplane connectors. The back-plane channel is shown in Fig.1.1.

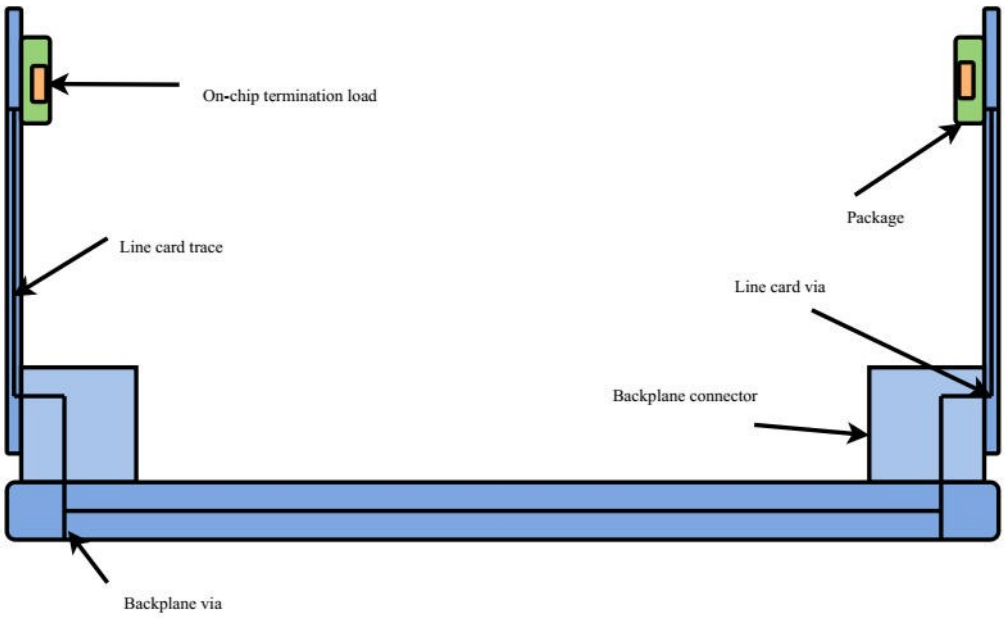

Fig 1.1 Backplane serial link model [33]

The frequency dependent loss varies with channel length and frequency and it is low-pass in nature. The channel attenuation increases more for with narrow width pulses when sent through the channel, which results in a broader pulse at the other end. This effect is called as ISI and is most important effects which is design bottleneck of high-speed backplane links

1.2.1 Inter-Symbol Interference

Pulse dispersion is one of the major issues associated with ISI. At multi-giga hertz frequency range, the back-plane characteristics resemble of transmission lines and the skin-effect and di-electric loss causes frequency dependent losses. At high frequencies, the current flowing through the conductor flows in outer cross-section of wires, which is limited in area and cross-section. This effect increases the resistance which in-turn causes losses which are non-linearly proportional to frequency[33].

$$R_{AC}(f) = \left(\frac{2.16*10^{-7}}{\pi D}\right)\left(\sqrt{P_r}*f\right) \tag{1.1}$$

D is wire diameter (Ω/in), Pr is wire resistivity.

The dielectric constant associated with the dielectric material encapsulates transmission line offers loss called di-electric loss, which varies linearly with frequency.

$$\alpha_D = \left(\frac{\pi\sqrt{\varepsilon_r}}{c}\right)(f\tan\delta) \tag{1.2}$$

Where $tan\delta$ is loss tangent, c and ε_r are speed of light and relative permittivity.

1.3 Organization of the work

The thesis the design of high speed serial link for backplane channels. The thesis is divided into eight chapters. The gist of each chapter is as follows:

Chapter 1 presents the introduction of high speed serial link followed by motivation, problem statement and contribution to the thesis.

Chapter 2 gives the overview of various circuit and block topologies of high speed serial links

Chapter 3 describes the design of on die termination circuitry with equalization functionality included used in the design of high speed serial links.

Chapter 4 demonstrates the design and results of high speed comparator employed used in receiver frontend.

Chapter 5 presents the design of clock generation and recovery circuits used in data transfer across backplane channels.

Chapter 6: Provides the summary of work and future work in design of high speed serial links.

Chapter 2

Literature Survey

2.1 Introduction

A high-speed serial link consists of basically three units such as transmitter, channel and the receiver as shown in Fig2.1.

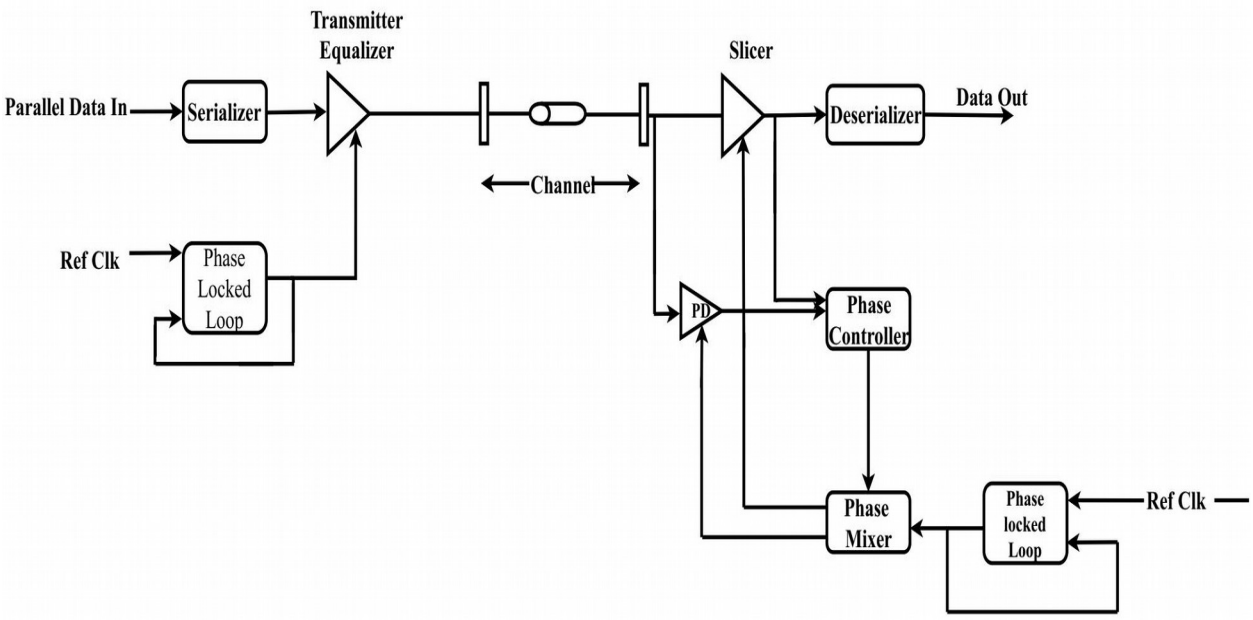

Fig 2.1 Block Diagram of High speed serial link [6]

The functions of transmitter and receiver are as follows.

1. To serialize the low frequency digital data into a high frequency streamlined data and send it across the channel.

2. To recover the clock and data from the random attenuated data.

The transmitter sends the data in different forms of signaling such as Non Return to Zero(NRZ), Pulse Level Modulation-4(PAM4) and duo-binary depending on constraints such as data-rate and channel-loss. The time difference between each high and low voltages levels is the bit duration or time. The critical design issue of transmitter lies in serializing random data in-order to deliver a clear high speed data signal.

Conventionally channels are realized using co-axial cable, unshielded twisted-pair, Printed Circuit Board (PCB) traces etc. A Channel that offers minimum data loss is very expensive and there exists a trade-off between production cost and quality of channel. Hence the cost is optimized by employing PCB traces along with necessary circuitry to compensate the loss.

The random data are received at the receiver unit are distorted after passing through the channel. The receiver needs to amplify the signals of lower voltage levels to enable it for further data processing and error correction in addition clock recovery from the resolved data efficiently.

The (SerDes) (composed of Serializer and De-seralizer) pairs. SerDes architectures opens the hatchway to immense rise in data-rate, developing a domain in which SerDes functions are expeditiously evolving to meet the demand for denser, high performance communications. By compressing populous inputs into differential pairs, accelerated throughput can also be universally actualize in a multitude of purposes [1].

The implementation of serial-links has become a challenging design with power analysis being performed on models before the design. In this direction the high speed link was analyzed by [2] and power hungry DFE was replaced by adaptive CTLE in the receiver with the CTLE eye opening being monitored and used as objective function in error minimization.

Serial I/O architectures with emphasis on signal integrity aspects were explored by [3] for power efficient circuit methodologies. To counter the power dissipation and to increase the throughput of serial-links, a voltage mode four-level pulse-amplitude modulation PAM4 serial link transmitter.

The PAM4 voltage-mode implementation consists of a pull up and down network, instead of constant tail current source, thereby having large swing at the transmitter. As the output impedance diverges with the PVT, the driver produces in-accurate output voltage levels. This topology employs calibrating control logic in order to reduce the reflection loss. The exponential increase in data-transfer rates across back-plane channels which of bandlimited nature necessitates, the designer to look for pre-emphasis/de-emphasis power-effective circuit implementation topologies keeping the design complexity low. An attempt was made by [4] to keep the design complexity low by using cascaded combination of two voltage mode drivers.

Designing an energy-efficient DFE for high-speed I/O is challenging task at high-data rates. This problem increases four-fold when the DFE are operated at transition frequency (f_T) limits of process technology. To solve the above problem [5] has proposed to merge the summer and latch blocks and further decreasing the settling time of latch. Loop speculative DFE architectures suffer from speed and voltage headroom issues in sub-micron technologies when data-rates are very high. To mitigate this issue, the CML mux logic was replaced by majority-voting architecture by [7].

As data-rates required by the application are exponentially increasing, the power consumption is to be kept at minimum with channel attenuation becoming the design bottleneck. The serial link architect needs to explore alternative design blocks with no or marginal change in channel material. To overcome this issue, [8] proposed adaptive DFE at the receiver. In-addition to cancellation of the post cursor ISI by taps implemented by the adaptive IIR filter for keeping the jitter minimum and maximizing receiver eye height. The optimal design of the adaptive receivers (DFE-IIR) can be used to minimize the reflection loss coefficient. The required number of IIR filter taps is a non-linear function of power dissipation and ISI cancellation.

The low-pass nature of channel attenuates fast varying signals which are composed of R and C circuits, where ‘R’ and ‘C’ are unit resistance and capacitance in the channel such as high density silicon interconnects where source synchronous I/O systems are being used. To make

up the channel losses under limited power budget, [9] has proposed the use of DFE-IIR architecture. The continuous time IIR filter is tuned by both varying the resistive and capacitive components. This architecture is particularly suitable for channels dominated by R and C elements, altogether reducing the power consumption by implementing all post-cursor ISI taps by continuous time IIR filter as it has exponentially decaying pulse response characteristics.

The design of high speed serial link becomes more critical with low power constraints. Such designs meeting the settling time issue of full rate DFE, which is further tightened by parasitic capacitance at the summation node of DFE has motivated serial link designers to increase the design space to explore more circuit topologies [10]. To decrease the effect of parasitic capacitance, the back-gate (bulk) was used as an input terminal which helps in systematic isolation between input and feedback paths present in the design of higher speed summer.

The maximum data-transfer rate across the back-plane is not only limited by channel-loss but also by the power dissipation for minimizing the effects of pulse-dispersion. To reduce the loss at high frequencies, a zero is introduced in the adaptive equalizer (AEQ) in the receiver by [11]. So the AEQ is adapted based on slope minimization between the data transition edges at input and output of slicer. An attempt was made to make the design independent of PVT. To increase the SNR even at high-frequencies, a NC was employed which offers noise cancellation for a wide range of frequencies with DC gain achieved by the high frequency [HF] boosting.

The power hungry circuits in a serial link are DFE, summer and slicer. To minimize the power consumption FFE uses half rate topology at the transmitter along with that a full rate DFE at the receiver. In this direction [12] proposed full-rate DFE architecture, the summer and comparator are merged into flip-flop meeting the settling time required remarkably increasing the operating speed of the main critical loop, thereby removing the speed bottleneck in design of high-speed I/O.

The power dissipation to compensate PCI express channel loss needs to be minimum with minimum hardware overhead. Towards this, various design methodologies were attempted A low-voltage zero (LVZ) is placed in equalizer at the receiver for high frequency gain boosting. A SB technique was employed[13] which tunes LVZ by minimizing the power difference between the high and low frequency components at the input and output of slicer .

Here an attempt was made to tune LVZ using power detector instead of using inductor for HF boosting in order to reduce area.

The attenuation provided by FR4 channel depends on the data-rate and channel length. To meet the ever increasing signal integrity issue as stated above, equalizers are implemented at both transmitters and receivers which are adapted at the receiver. To minimize the effect of post cursor ISI and minimize power consumption, an IIR filter was used by [14] in lieu of post cursor taps The topology is tuned to meet the settling time requirements increasing the serial-link efficiency.

The back-plane is very complex environment which is composed of various materials with diverse frequency characteristics. Any impedance mismatch between the channel and termination circuitry at both transmitter and receiver causes reflections and are quantified as reflection loss coefficient. The high frequency signals are attenuated by the channel due to its band-limiting nature in-turn causing ISI, which varies with frequency, PVT variations. To compensate the channel loss and retrieve the high-frequency signal from the corrupted signal, equalization is usually employed in the transceiver. To adapt the receiver equalizer, many techniques such as SB and EOM are being implemented. The SB technique mentioned above fails to perform for non-random data pattern in multi-rate applications and EOM burns huge power dissipation. To deal with above problem an adaptation strategy was proposed [15] in digital domain to reduce power consumption effectively.

The conventional resistance based summers in high-speed serial links are power hungry and have settling times constraints, So they are replaced by a resettable current integrating summer reduces the power consumption considerably as the output nodes are pre-charged during the sampling phase for low frequency data-signals. The integrating summers suffer from frequency dependency loss of about 3.9dB at higher frequencies, so to mitigate this issue [16] has proposed to design a transmission-gate based sample and hold topology used.

Signal-to-Noise ratio plays an important role in any serial communication link. Equalizers are employed to cancel post and pre-cursor ISI. The main problem with the FFE present at the transmitter is lack of its adaptability and introduction of noise. This necessitates to keep a front-end amplifier circuitry to improve the signal swing mostly for multi-level signaling schemes. To improve the data-transfer rate, at the receiver equalizer either CTLE or DFE can be adapted, that can reduce the noise introduced into the circuitry. Towards this end a

summer amplifier or integrator and DFE are both combined by [17] that reduces the noise generation and power consumption.

The power consumed by the I/O circuits needs to be fraction of data processing units on the IC. To further reduce the power consumption, different variations of equalizers were modeled to evaluate the power efficient architectures. In this direction an Infinite Impulse Response-Decision Feedback Equalizer (IIR-DFE) combination filters were used for a very power and area efficient serial I/O circuitry [18]. The pulse response of an IIR filter matches to the exponentially decaying nature of signal when sent across a back-plane channel. This idea changed the phase of design from two or more symbol spaced DFE to single tap DFE and an additional tap comprising of IIR filter which can be tuned by the error function at input of DFE. This novel architecture has not only reduced the power consumption but also reduced the overall area drastically.

Data transfer across back-plane or serial links of various flavors is not limited only by the operating frequency of signal but also by stub-length, receiver eye sensitivity and required BER vs power consumed trade-off. It was shown that it is highly efficient to send data using NRZ signaling when BER and power consumption are primarily important, whereas in case high-rates are demanded by the application, partial-response signaling or duo-binary signaling is preferred as appropriate choice for both long-distance and medium complexity. Further PAM4 is preferred when very high data rates and long-channel lengths are needed but the latter causes increased power consumption caused by the amplifier stages present at the front-end of comparator [19].

To compensate the channel loss due to traces of FR4, pre-emphasis technique was employed at the transmitter which causes reduction in dynamic range of signal for data-rates above 10Gb/s. To counter this effect and reduce the power consumption, various techniques such as 1) peaking by complex poles 2) peaking by passive networks and reverse scaling were proposed [20]. The receiver equalizer was tuned by Spectrum Balancing (SB) technique.

The second most power hungry circuit in the receiver block of serial link is the current integrating summer. To reduce the power consumption of the summer, a charge transfer mode summer topology was proposed [21]. Two reference voltages namely V_{CM}, V_{REF} are taken from a stable voltage reference generator such as band-gap reference (BGR). The summer acts as front end to loop unrolled DFE to generate the required voltages. The

capacitor Cs is charged to effective voltage of V_i-V_{CM} initially and during the evaluation phase, the charge across the output is $V_i \pm V_{REF}$.

To adapt a full-rate DFE at high data rates, the power consumed by the summer, comparator and coefficient adaptation logic are very high. To reduce the power consumption in full-rate DFE architecture, unrolled DFE, partial -response DFE, or loop speculative technique were employed. The power is further reduced when half-rate or quarter rate loop unrolling technique was used for cancelling only first tap used in DFE. However it increases the hardware requirement exponentially, So keeping this constraints as design objective, a time-interleaved soft decision technique was proposed by [22]. This technique not only mitigates the above problems but also increases the evaluation time required as the latch was used in place of power hungry and high-offset prone edge triggered slicer.

Band-limited channels attenuate fast varying signaling, which causes ISI. To reduce the impact of ISI, an adaptive DFE is categorically employed at the receiver, which may run at full-rate or half-rate depending up-on the power budget. The receiver DFE circuitry composes a summer in feedback-loop to cancel the ISI, without amplifying noise which is boon as Signal to Noise Ratio (SNR) is increased drastically. This causes the power consumption to shoot up in summer and comparator. To minimize the power consumption [23] proposed pre-charge based summer. The summer not only reduces power consumption but also lowers settling time requirement as the output nodes are pre-charged before sampling and decision making phase.

At data-rates above 2Gb/s, the attenuation provided by the channel needs to be compensated. To solve this problem [24] proposed a sum-feedback filter[SFF] which relaxes the timing requirement compared to FFE at the receiver. To further reduce the channel-loss, a PAM4 signaling was adopted which increases the data-rate 4- fold.

To decrease the power consumption and decrease the circuit design complexity of high speed serial link, continuous Time Linear Equalizer (CTLE) was adapted by [25]. The adaptive algorithm relies heavily on spectrum balancing technique where balancing the power components of both high and low frequency components of signal is the design objective, thereby boosting the gain and increasing the data spectrum judiciously.

Half-rate, quarter-rate loop speculative algorithms which are power efficient are used to aid while designing DFE but suffers from the drawback of causing additional pattern jitter. This motivates the designer to look for architectures[26] to decrease the DDJ. In this direction

LMS algorithm and edge equalization are both combined to create voltage margin and timing margin in DFE circuitry in the design of serial links.

The bandwidth to send a high-frequency signals over back-plane is primarily is limited by channel attenuation which is also called 'channel-loss'. The attenuation measured in decibels (dB) varies with many factors such as signal bandwidth required, channel-length and type of materials used during channel design. [27] proposed a power-efficient design in which duo-binary signaling was preferred signaling method which has the advantages of multi-level signaling. So more bits are sent through the channel in 1UI and the required bandwidth decreases to almost two thirds . The design uses an FIR filter which compensates the phase and amplitude distortion due varying nature of channel and thus power efficient realization of near duo-binary signaling scheme was made possible.

To increase the operating frequency range, an adaptive FIR equalizer with fractional spaced structure which has inverter with an active inductor as load element was proposed [28] for usage in high-speed data communication. A pulse extraction method was used as closed loop adaptation technique to demonstrate its inherent low-power and area efficient implementation.

To maximize the received voltage the equalizer employs several interpolator sampling phases, thereby decreasing the power consumption and design complexity. To further reduce the power consumption, zero-forcing and Sign-Sign Least Mean Square (SS-LMS) algorithms were modified to implement adaptive equalization in digital domain by [29] where-in the frequency of updates can be further reduced. The power consumption of receiver is proportional to receiver sensitivity, which mainly is contributed by offset component of comparator hence the offset of comparator is cancelled, and sampling clocks utilized by the comparator are de-skewed to take care of static mismatches which resulted in minor variations in filter coefficients.

Eye opening at the input of the receiver determines the BER of the transceiver. To measure the eye-opening, eye diagrams are measured on the fly using eye-opening monitors (EOM), which maps the received signal to high-speed signal. To generate EOM, phase rotators and digital-to-analog converters (DAC) are used in different sizes of rectangular masks which are overlapped with the received signal at the receiver. The worst case mismatch is determined by signal transitions at the middle of eye and thus can be used as error signal to adapt the receiver by means of co-efficient optimization. This method of BER detection using

EOM[30] is independent of decision at the output of receiver and does not depend on pattern matching, which in-turn reduces the complexity of the receiver design.

To increase the performance in serial links at higher frequencies, three equalization methods such as FFE at transmitter, discrete equalization and receiver equalization for high speed differential serial links was proposed by [31].

The back-plane environment is very complex since it is composed of different materials which causes not only reflections but also channel loss which varies with stub length, frequency and data -rate. The proposed architecture implements both NRZ and PAM4 with little change in the selection hardware which achieves high throughput in terms of low reflection loss and low power overhead over broad range of frequencies [32].

More complex signaling techniques such as PAM4, duo-binary are employed for meeting the BER specifications. A dual-mode architecture was by [33] proposed for implementing both the NRZ and PAM4 signaling with a minor modification for implementation. Loop-speculative single tap DFE was adopted as receiver equalization. The receiver equalizer is adapted by popular sign-sign LMS procedure, with maximum voltage swing as main problem objective with the data based filtering, which in-turn reduces the hardware at the front-end of the sampler thus reducing the power consumption in the receiver.

To meet the BER specifications in band-limited channels, the effective input referred noise plays a very important role in the design of high speed serial links [34].

To improve the bandwidth-power trade-offs, duo-binary signaling was implemented for the required bandwidth for efficient design of adaptive equalization technique [35].

The bandwidth required to implement multi-level signaling is less compared to the full-rate signaling schemes, as the gain boosting required to counter the channel loss decreases which makes the architecture power-efficient.

A data-look ahead technique was presented by [36] is used to drive the main tap current sources when reduced swing is preferred.

A back channel communication path was employed using common mode signaling in order to adapt FFE by [37] for a self-contoured adaptive differential high-speed transceiver cell. To minimize the hardware costs, an extra data update information from receiver to the

transmitter uses a three level return to zero signaling scheme with simultaneous voltage and timing references.

Duo-binary signaling exploited by [38] to improve sampling rates. Controlled amount of ISI was introduced so that it can be removed afterwards at the receiver. The data-rate is not only limited by the PCB traces and back-plane but also by data computation unit's on-chip.

A continuous time filter has advantages of wide tuning range. A tap continuous time filter is used to implement transmitter Finite Impulse Response (FIR) filter used for implementing pre-emphasis functionality for data rates above 1Gb/s data transfer rates[39] . Each tap on the pre-emphasis filter is implemented by a second order low-pass filter. The major challenge involved in design of tap filter is that it need to have constant amplitude and group delay response across the signal bandwidth.

Spectral efficiency is higher when more than one bit is transmitted per 1UI. In this direction [40], has attempted the use of PAM4 for data transfer across backplane. In this direction, to compensate the channel loss and reduce the distortion, the transmit equalizer is continuously adapted.

To keep up with increased data transfer rate across the back plane, [41] proposed usage of multi-level data transmission or usage of DFE. To maintain compatibility the same hardware can be used to implement both 4PAM and NRZ signaling using loop-speculative DFE at the receiver. To tackle ISI, FFE at the transmitter is tuned using back-channel. Data based updates are used to tune back channel and the receiver equalizer is adapted based on error signal from the summer, thus minimizing the hardware required at sampler-front end and this drastically encourages multi-level signaling.

To keep up with the demands of high data rates above 1Gb/s multi-level signaling such as PAM4 is usually preferred for meeting the trace attenuation or channel-loss which varies with both frequency and length. To show the effectiveness of this technique[42], a low cost BGA packing was employed. To counter the effects of signal interference transmitter equalization ,cross talk cancellation circuitry are used in parallel and current summing integrator topologies are employed at the receiver.

Data transmission at high data-rates is limited by transition frequency of technology used and the channel loss [43].The multi level signaling is proposed with half ,quarter and octave rates

for data transfer retrieved by[44] . Power dissipation can be reduced by using clock at lower operating frequencies.

A voltage-mode switched-capacitor based circuit as summer circuitry was proposed by [45]. to reduce the power consumption. A fixed co-efficient Feed Forward Equalizer (FFE) is used to cancel pre-cursor ISI. A timing function is created by using fully adaptive Decision Feedback Equalizer (DFE) and mixed signal current-summing circuit to cancel post-cursor and baseline wander.

Next generation of gaming applications requires very high speed data transfers between graphical processing units and gaming consoles. In this direction a high-speed transceiver was proposed by [46], wherein the multi-level signaling (4PAM) and pre-shaping are employed at transmitter along with adaptive equalization at the receiver.

Techniques for high-speed implementation of nonlinear cancellation were proposed by sanjay et al [47] .Non Linear Cancellation (NLC) significantly limits ISI in long haul direct-detection structures and thereby doubling the information rate limited by pulse dispersion. The ISI reduced through NLC which is carried out through subtracting the interference brought on by previously detected symbols. This subtraction, on the other hand requires previous selections to be sent-back to the comparator element. However delays in the feedback back loop can severely worsen the required signaling rate of a detector operating with NLC. The problem was addressed by modifying the feedback loop with help of analog signal switching through multiple decision feedbacks each with a unique threshold value. An associated look in advance computation facilitates the feedback loop to complete the computation within permissible time.

2.2 On Die Termination

To reduce the power consumption a voltage mode transmitter is proposed which performs both equalization and impedance matching to the channel. To further reduce the power, a low common mode signaling is employed [48] which requires complex finite state machines for impedance matching and the amount of required equalization to reduce the channel loss.

Signal integrity needs to be explored for large design space to transfer data across backplanes. Impedance mismatch between driver termination, vias and stub impedance mismatch which results in reflections leading to closed eye at the receiver front end. The is

further exacerbated degraded due to high attenuation of traces and cross talk between adjacent channels. To improve the BER specifications adaptive equalization is required at transmitter and/or at the receiver [49]-[58].

Transmit and receive equalizers are employed to compensate the channel loss, which in turn reduce ISI resulting from band-limited channels. To reduce the reflection coefficient, a transceiver was proposed [59] that employs a 4-tap FFE followed by DAC which is used for impedance matching while introducing programmability into the design. The calibration mechanism employed in the architecture is limited by quantization error of the calibration bits which increases proportionally to data rate for data transfer applications across multi data rates.

Power integrity analysis of serial-link drives the serial-link architect to explore the design space for possible power saving topologies meeting the required data rate required. In this direction [60], has modeled the power analysis of high speed serial links by employing SST drivers at transmitter in addition to enabling equalization capability at the transmitter. However FFE draws more power. The architecture can be made more power efficient by implementing adaptive CTLE at the receiver.

There are various problems associated with design link such as channel attenuation, reflection loss. The problem is further aggravated when multi-rate applications are to be designed in lower technology nodes with primary emphasis on low-power architectures. To deal with signal and power integrity issues in the context of transceiver termination in addition to boosting of high frequency signals, a combination of voltage-mode driver for transmitter termination and current mode driver implementing pre-emphasis called hybrid mode implementation was proposed[61]. The SST has advantage of power savings of 4X the current mode while the later offers low complexity and boosting the High Frequency (HF) signals. To avoid the loading effects, complex segmented drivers in case of voltage-mode implementation, in addition to provide signal isolation between the serializer block and signal transistors, a pre-driver circuitry is employed. The termination in transmitter is implemented by series termination where an impedance control loop which adjusts the output transistors in the driver's section to distribute the equivalent segmented tap weights which out-grow geometrically for higher resolutions. In the current-mode implementation the added advantage is high-resolution equalization without significant increase in pre-driver design complexity which is controlled by a current controlled DACs.

Impedance match for wide range of frequencies and for multi-standards with the lower power consumption has been a design challenge for transferring data across serial links in particular at lower technology nodes. To combat these bottle necks at lower voltages, a near ground termination is implemented in SST design style by using a common gate-amplifier (CGA) to match replica transconductance impedance which controls impedance matching in the presence of common mode noise. The impedance calibration control logic was presented by [62] to operate for multi-standard's which burns more power as calibrating effective transconductance across Process Voltage and Temperature [PVT] slows down the achievable data transfer rate.

There are two forms of on-die termination (ODT) Viz., current –mode and voltage mode. The current mode design style is power inefficient, so voltage mode is usually preferred as it consumes less than quadrant of power consumed by current mode. To increase the power efficiency a shunt branch is added in parallel to that of the channel impedance, this form of termination is called Impedance modulated pre-emphasis voltage-mode transmitter [63]. The topology achieves equalization at the cost of impedance mismatch , this situation further degrades for backplane channels as number of discontinuities are introduced due to packages and vias which were introduced for signal coupling across the backplane. The whole process introduces impedance mismatch which leads to high reflection loss coefficient which in turn takes away majority benefit when used for long haul backplanes.

The voltage mode ODT suffers from various issues such as degraded HF boosting at very high data rates coupled with high power dissipation incurred in pre-drivers and its digital logic control circuitry. To improve the performance of serial-link termination circuitry, a common-drain amplifier was proposed to be used [64] in place of resistors which act as load with a pseudo CML implementation. The above described technique has no impedance control over vast frequency range and multi data standards.

This thesis explores circuit strategies to implement power efficient on die termination with equalization.

2.3 Dynamic Comparator

To decrease the resolving time, a bandwidth modulation technique is employed that introduces negative feedback which also reduces the reset time of the regenerative stage of

dynamic comparator [65]. The above described bandwidth modulation technique when applied to comparators used in multi standards application like USB2,USB3 and PCI-express gen 4 under performs the power bandwidth product criteria as power quadratically increases with loop bandwidth.

Digitization has made signal processing an easy task but converting the analog signal to the equivalent digital code is cumbersome in power constrained architectures. The main component used in Analog to Digital Converter (ADC) is dynamic comparator which employs positive feedback to convert small input differential voltage to full-scale voltages. The peak-to-peak voltages are coupled back to the input node during regeneration, which causes spikes or some-times perturb the common-mode level which is called as kickback noise (KBN). To minimize KBN, various noise reduction techniques viz 1) Node isolation and 2) Neutralization techniques are being proposed [66].

Comparators act as decision making logic in many circuits, the performance of comparators are limited primarily by the offset voltage at the input of comparator, whose contribution is more in dynamic comparator relative to the static one due various mismatches such as threshold, transconductance and effective load capacitance at the output node during regenerative phase. To reduce the effect of offset, while trading carefully with power consumption, an offset cancellation (OC) was proposed [67] where the body voltages of the input transistors are tuned to capture the change in output voltage during regeneration phase. This scheme essentially requires a single clock phase. The above proposed technique is novel in nature which assumes the PVT across the design is constant which when inspected from yield point of view but the offset cancellation degrades as no on die trimming mechanism is employed to have threshold control across process corners.

The usage of high speed ADCs at the front end of high speed serial links is gaining momentum in the recent past. To resolve this tangle an attempt was made [68] through a topology in which dual tail dynamic comparator which has regenerative feedback in both pre-amplifier and output stage. To minimize KBN low impedance path is created from output of first stage to both input of output stage and ground.

This thesis attempts to design circuit strategy for comparators in order to minimize KBN and input referred noise suitable for high speed serial links.

2.4 Phase Locked Loop

As clock speeds have entered into Giga hertz regime, constraint on clock jitter and duty-cycle distortion has made specification more stringent.[69]. For meeting excessive tuning range specifications in LC-VCO, a multiplier pass loop ring oscillator structure with saturated gain approach was proposed[70]. The attractive aspects of this approach stems from its simplicity. The ring oscillator can be realized with ease in any Complementary Metal Oxide Semiconductor (CMOS) process node.

The output voltage of the ring oscillator is being affected generally by tail current source and besides tank loading effects. The effect of numerous noise sources in the circuit used were analyzed by [71] and it is shown that the cumulative noise added by means of the transistors in the differential pair can be scaled down at ease by exploiting cyclo-stationary effects of the sources.

A PLL is used at front-end to preserve synchronization in the serializer/de-serializer pair. The negative-feedback present in the PLL corrects any difference in time period detected at the input of Phase detector (PD). To grasp the SerDes technology, it is essential to have a basic perception of how a PLL operates. The underlying functionality of SerDes PLLs is to synchronize the input frequency (typically clkin) and a generate core frequency. The designed center frequency is accountable for the serialization timing generated from the PLL. A phase detector is used in the front of the loop to assign a small delta change which is generally fed into a filter, whose output voltage controls Voltage Controlled Oscillator (VCO) which in turn tunes the output frequency. A divide by means of switch function is then responsible for the last charge of the ‘clkin’ to the PLL frequency.

The evaluation of clock jitter has advanced as signaling rates have increased. In high pace serial links clock jitter influences the receiver efficiency. The emphasis is now on quantifying the relativeness of clock quality to device realization in terms of the BER [72].

A series of direct coupled cascaded chain of inverters is being proposed as a new delay generator. The delays achieved by circuit is proportional to the buffer delay. The advantage of this architecture is that the array of inverters have uniform offset in phase in constant fraction to the buffer delay [73] which varies across PVT and thus has degraded phase noise performance which is not suitable for designs which require minimum cycle to cycle jitter.

The timing jitter of entire design is proven to depend on the jitter generated the ring oscillator and its rate of accumulation is inversely proportional to the bandwidth of the phase locked loop (PLL)[74].

Charge pumps are utilized to convert the timed logic into analog quantities for controlling the locked oscillators [75]. Practical limits of multi-tone signaling over very high data-rate backplane electrical communication channels are presented in [76]. Application of discrete multi-tone (DMT) signaling to high speed backplane interconnects requires fundamental adjustments to the standard evaluation strategies utilized in wire line communication systems. Tight energy budgets in backplane links impose severe constraints on DMT block dimension and use of channel shortening filter in the system. First order evaluation of a linear oscillatory systems leads to a noise shaping function and a new definition of quality factor (Q). A linear mannequin of CMOS ring oscillator is used to calculate its phase noise along with three segment noise viz. additive noise, high frequency multiplication noise and low frequency multiplication noise [5].

There are three most important predicaments that can limit the overall performance of high-speed links namely clock frequency, channel bandwidth and timing accuracy. It makes use of the figure of merit of as (FO-4) inverter to measure the overall performance of circuits that must scale with technology. Since the quandary (in terms of FO4) remains roughly consistent with scaling, limitations that do not scale with technology are measured in pico-seconds and likely establish a closing bound to a serial-link performance [6].

The effect of numerous noise sources in the circuit used are analyzed and it is shown [78] that the cumulative noise added by means of the transistors in the differential pair can be scaled down by exploiting cyclo-stationary effects of the sources.

Initially state -equation methodology was adopted to analyze the large -signal lock acquisition process and small signal linear tracking behavior of a third-order charge-pump PLL. To have intuitiveness of the PLL, noise transfer function is analyzed in Z-domain and the non-linear state equations are worked out for small perturbations. Secondly, impulse-invariant transformation and s-domain methods are compared [79].

The spectral characteristics of PLL were analyzed using stochastic partial differential equations taking into boundary conditions caused by the loop filter, Phase-Frequency Detector (PFD) and VCO [80].

Power supply rejection ratio constitutes an important specification of PLL that influences PLL's jitter characteristic. A CMOS quad transceiver was proposed by [81], which has dual-loop PLL. To mitigate the jitter introduced by the supply, the dual-loop PLL was designed to have two supply regulators, whose band width is adaptive, one with high bandwidth and latter having low bandwidth for digitally controlled phase interpolator which reduces the power supply rejection ratio (PSRR). Current starved ring oscillator was being employed which has wide tuning range that can be used for robust integration with various serial-link interfaces.

A discrete-time open-loop dynamic model of PLL and DLL was presented by [82] that exhibits adaptive bandwidth optimizes the performance over wide frequency range over Process Voltage Temperature (PVT). This was characterized based on the sampled error from the response.

As discussed earlier Power supply rejection ratio (PSRR) forms an important specification in designing analog circuits especially, signal processing circuits with special emphasis on PLL. Deterministic jitter is caused by random variations in the circuits such as power supply hence the design of voltage regulator needs a special care in context of PLL. To decrease the jitter caused by PSRR, another compensation technique was proposed by [83], which employs replica based biasing and thus the stability of loop can further be improved. The main draw back of the proposed PLL with replica based biasing is that there is no control mechanism on effective transconductance of replica pair with process, which further needs to have a constant transconductance circuit that limits the tuning range.

Inverters are generally used as leaf cell in the design of ring oscillator (RO). To analyze the noise component in inverter, a time-domain jitter calculation method was proposed by [84] to quantize and simulate white noise and flicker noise component by VCO modulation.

Tuning range plays a very important role while integrating a PLL across different process nodes and serial link standards. A regulated tuned supply is being proposed to improve PSRR and satisfy the jitter specifications [85].

The channel attenuation and reflection loss play a pivotal role in design of a high speed serial transceivers. To mitigate the above affects, a 5-tap DFE and 4-tap FFE was proposed by [86] at the transmitter and receiver to reduce the BER. Further a low jitter PLL was synthesized using LC VCO in the transceiver which trades off being with lower tuning range, higher power consumption, area and mostly need additional fractional divider circuitry for multi standard which further reduces the gain of VCO.

To increase the program-ability and to have independent control on the loop bandwidth and settling time in PLL, [87] has proposed a dual-loop PLL architecture which replaces the resistor in proportional path with a sample-hold circuity which further decreases the noise. This proposed PLL reduces the thermal noise with increase in shot noise. In addition the designed circuit needs to have constant impedance control mechanisms within tolerable limits which further questions the system stability when used for multi standard applications.

Power optimization without compromising the signal integrity is the main focus of multi-rate data transfer over back-plane channels. To meet the power constraints, the design parameters such supply voltage and current are scaled based on the required signaling rate whose optimization is characterized by nonlinear cost function. To boost the signal across the receiver, PLL (which functions as frequency synthesizer) is shared across the transceiver, in addition to minimizing the offset at front-end of the receiver which now saves large chunk of power while adopting active inductor approach[88].

The jitter needs to made independent of both input and output clocks. The data dependent jitter was proposed to be minimized by[89]. Applying techniques such as minimizing the power consumption of VCO and loop filter. Also the loop bandwidth is chosen aptly that minimizing phase noise contribution of PD, LPF,VCO ad frequency divider.

Phase noise forms an important design specification in the design of CDR architectures, which may be degraded by limited acquisition range of frequency locked loop FLL, phase error caused by glitch in control voltages of VCO and high gain or VCO. To counter this, [90] a dual-loop CDR architecture was proposed which smoothly shifts the control from phase acquisition loop (PAL) to the frequency loop (FL), thereby minimizing the phase noise degradation and in addition maintaining the minimum phase margin to design a stable system. To increase the conversion efficiency of charge-pump (CP) and LF circuitry, the width of error signal from the PD is increased by modifying the half-rate PD there by reducing the phase error between the recovered clock and random data signals. The designed

PD increases the width of error , up and down pulses but when the circuit is used for full rate applications, the V-I converter which follows the PD may not settle suitably thereby creating ripples across the control voltage, losing the loop locking mechanism.

To meet the jitter, power and swing specifications of multi-standard PLL and CDR, [91] proposed an architecture with the following features such as employing an equalizer both at transmitter and receiver. The swing across the transmit FFE was made programmable while DFE was made adaptive.

A discrete-time delay cell was proposed by [92] to add a zero in the open loop transfer function of the phase-locked frequency synthesizer which also in-turn reduces the thermal noise introduced by the resistor in the loop filter. The introduction of zero stabilizes the loop in-addition to which eases the design cycle aspect pertaining to settling time and magnitude of spectral components outside the desired band of frequencies which are called as reference spurs.

The urge to decrease the power consumption in frequency synthesis has brought the PLL based clock multiplier and DLL(Delay Locked Loop) as available architectures of which PLL based topology generates less jitter while power consumption is more in DLL based ring oscillator. The jitter accumulation which determines the jitter tolerance when employed in CDR is less in VCO of PLL [93].

Power and speed constraints are important bottleneck of serial links. To obtain a tradeoff, a chain of interpolating inverters were proposed to be used to generate multi-phase clocks by [94]. This technique is employed in feedback loops to obtain higher speed of operation and precise phase spaced clocks which allow the feasibility of higher speed operation in CMOS based PLL.

Loop bandwidth plays a vital role which determines the settling time of a system. Adaptive control of reference clock frequency and frequency divide ratio extends the loop bandwidth considerably [95].

In this research, an attempt is made to design a PD used in the front end of PLL to improve the jitter characteristics.

2.5 Clock and Data Recovery

In order to reduce the systematic phase offset present in PD, a circuit strategy was proposed by [96] that exhibits linear characteristics, retiming and de-multiplexes. The proposed architecture also employs an interpolating VCO phase-locked CDR. A phase interpolator was introduced which needs to have a overlapping interval across process corners. This feature when evaluated across PVT limits the control voltage of the PLL which in turn reduces the tuning range and gain of VCO increasing jitter.

Jitter is defined as random movement of signal depending on the traversing path, generating source and interference. The data-dependent jitter (DDJ) is a time domain representation of multiple dispersed bits more than 1UI. The serial-link figure of merit (FOM) in terms of BER degrades for high-date signals due to limited bandwidth of the back-plane. A method to quantify DDJ was proposed by [97] which uses step response of current and preceding bits as the starting factor, seemingly the computation time grows linearly instead of exponential nature.

Jitter tolerance is an important specification in the design of CDR. The binary phase detector usually degrades the jitter specifications in design of single loop CDR. To balance the effects of jitter degradation and fast lock acquisition, a dual-loop CDR was proposed by [98] which consists of both PFD and frequency detector (FD). Thus it could control jitter transfer bandwidth even with usage of binary PD.

To tackle the ever growing demand for speed-power tradeoff's in high-speed serial link designs, low power-high efficient building blocks such as a programmable SST transmitter driver, phase rotator were proposed to be used by [99] in CDR. An LC-VCO based PLL for low jitter amplification and inductor loaded resonant clock distribution was employed in clock buffers to increase the gain at higher frequencies.

Power consumption and jitter amplification form a trade-off in the design of CDR design blocks used in high-speed data transfers. The error signal required to tune the data retiming circuitry and the charge-pump circuitry have been largely controlled by PD whose pulse width is small when data are transferred at very high rate. So a linear PD which runs at octave rate was proposed by [100] which enlarges the width of error signal and thus decreases the

complexity of CP and its controlling circuity in-addition addressing the maximum update rate bottle-neck on PD design. Another notable feature of this topology was that the performance improves with process scaling and increased data –rate but it introduces bimodal jitter which is very difficult to track and control when PD does not have enough gain to curtail metastability.

The recovered clock from the data in CDR circuitry was proposed to be used by [101] to generate phase error, which is proportional to phase difference between the clock edge and center of incoming data from DFE. The data transitions were exploited are being used to acquire frequency lock with no additional reference, However there is necessity to improve performance by striking balance between phase noise and power consumption.

In this direction, a dual loop clock and data recovery circuitry with modified CML D Latch is designed to improve FOM that takes into account both jitter performance and power dissipation.

Chapter 3

0.603pJ/bit On Die Termination Using Current Mode Logic in 130nm CMOS for 10Gb/s Backplane Channel

3.1 Introduction

On die termination plays a pivotal role in reducing the reflection loss across the transceiver circuitry. Inter symbol interference is caused by the band limiting nature of the channel. A circuit which reduces the effect of channel loss meeting the power budget specifications is needed. The proposed circuitry is designed in current mode logic with open drain configuration. The designed circuitry has power efficiency of 0.603pJ/bit in 130nm CMOS technology.

Even though technology scaling has brought much needed advantage for faster computation, this has been lagging in data transfer within the effective power budget allocated for I/O. Signal integrity poses a major concern while moving to higher data rate in strict power and jitter specifications. There has been considerable effort by fine tuning various circuits blocks in dealing with issues such as inter symbol interference, which came up during the design of ODT. In this direction various circuit techniques viz., current mode [49, 101, 102], voltage mode [44, 103] and hybrid mode [44] has been introduced to deal with the issues. Dynamic impedance modulation technique which optimally trades signal integrity with power has been demonstrated [105]. On chip termination employing pulse width modulation method was attempted [106]. Trans-impedance amplifier was also used for ODT at both receiver and transmitter without paying much attention towards pre emphasis. Attempts to achieve on die termination along with equalization in current mode were presented by [105], while the

power consumption still remained a design issue. Voltage mode, with N over N or P over N MOS structures give the advantage of lower power consumption about four folds [107]. The performance of voltage mode circuits are degraded when channel equalization is also included, so a reconfigurable driver was demonstrated by [46]. In P over N voltage mode implementation, complex digital encoding circuitry is used for controlling ODT, which adds the complexity in the implementation of feedforward equalizer.

3.2 Circuit operation

The proposed circuit is shown in Fig 3.1. The transistors in Fig3.1. M1, M2, M6, and M7 operate in linear region. They are designed keeping the swing consideration as shown below.

$$(W/L)_{1,2,6,7}=4*(I_1+I_2)/K_n*(V_{swing})^2 \qquad (3.1)$$

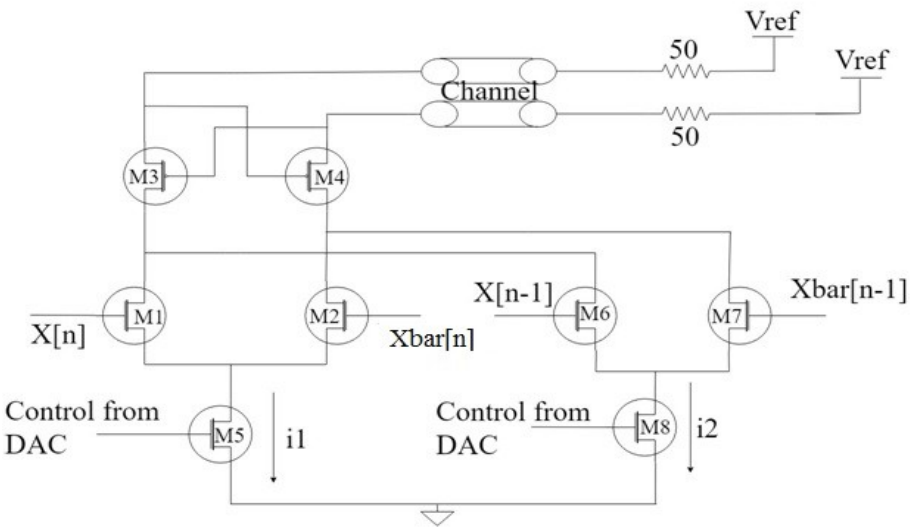

Fig.3.1. Proposed on die termination with pre-emphasis filter.

Let I_1, I_2 be the main and post cursor currents. V_{max} and V_{min} be the maximum and minimum voltages during equalization.

$$V_{max}=R_{term}(I_1+I_2) \qquad (3.2)$$

$$V_{min}=R_{term}(I_1-I_2) \quad (3.3)$$

Where α the pre-emphasis coefficient and Rterm is the channel terminating resistance. The transistors M3 and M4 are connected in positive feedback. The impedance looking from the drain of M3 and M4 is ($\sim 2/gm_{3,4}$). The output impedance is ~64Ω at 10GHz.The output impedance is plotted in Fig.3.2.

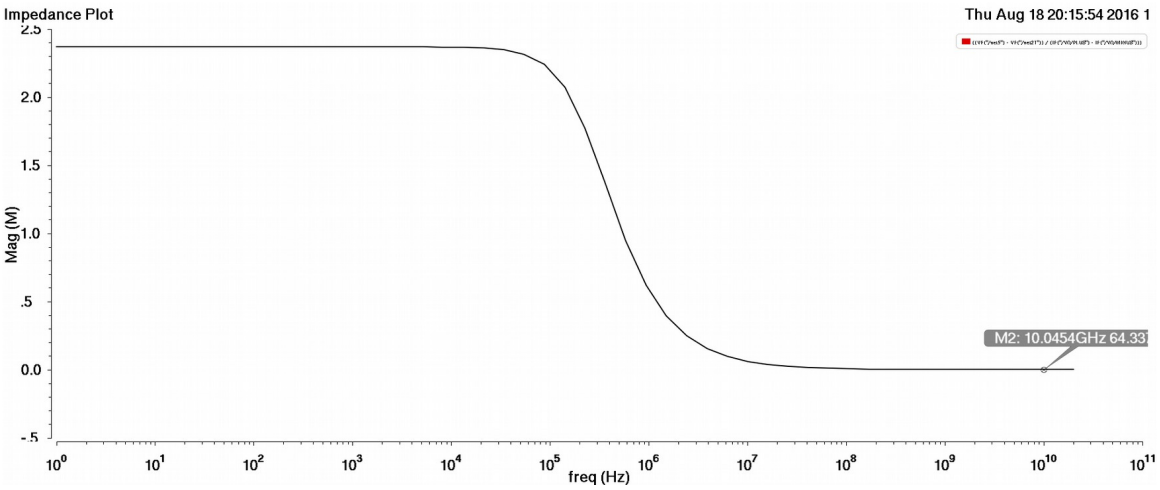

Fig.3.2 Output impedance of the circuit

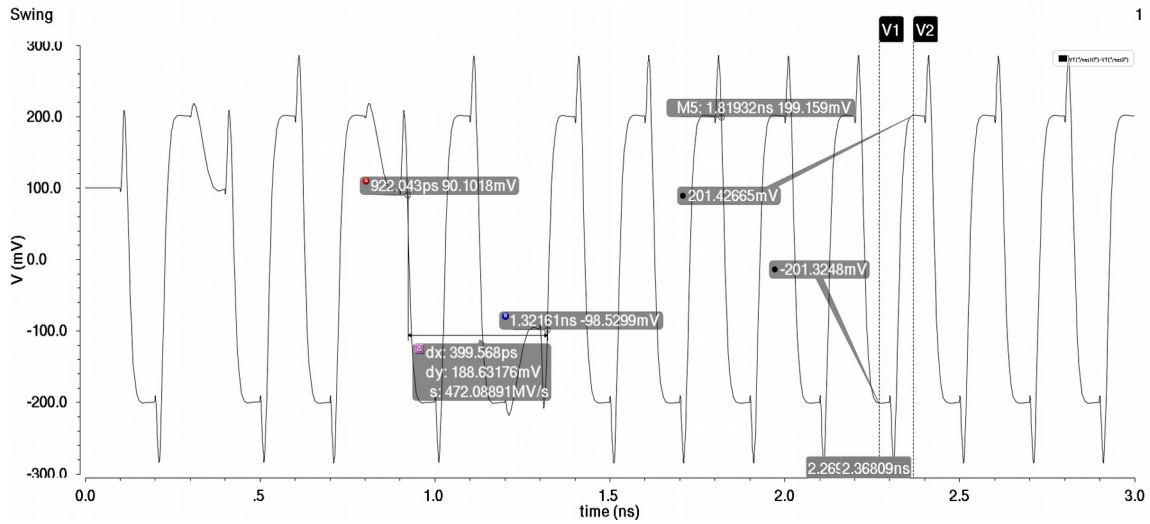

Fig.3.3 Output swing across the on die termination.

The proposed circuit has output swing of 0.4V as shown in Fig.3.3. The eye diagrams at the output of the circuit is shown in Fig.3.4. The circuit introduces 3.25ps random jitter.

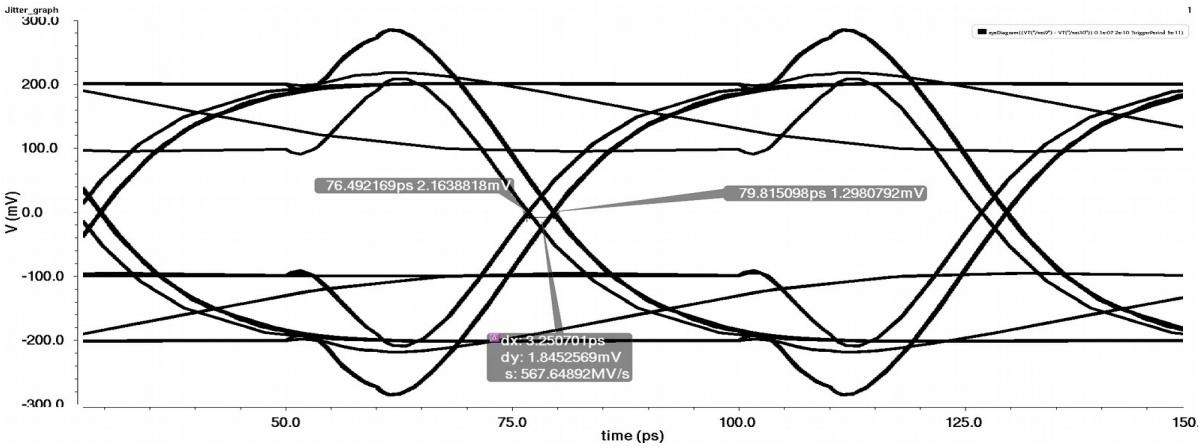

Fig.3.4 Eye diagram at the output of transmitter

Table 3.1 shows the comparison between the various circuits which were designed for on die termination and equalization.

Table 3.1: Performance comparison of various Feed forward equalizers

	[49]	[46]	[44]	[108]	[109]	This work
Tech. (μm)	0.065	0.065 LP	0.090	0.028	0.065	0.13
Supply (V)	-	1.2	0.8~1.2	1	0.6~0.8	1.2
Data rate (Gbps)	5~15	10	2~6	8.5~13	4.8~8	10
TX swing (V_{pp})	0.1	0.25	0.1~0.4	1	0.1~0.2	0.4
Equalizer	-	2 Tap FIR	2Tap FIR	4 Tap analog	None	1Tap FIR
Efficiency (pJ/bit)	2.8-6.5	≤1.1	1.26	3.8	0.3	0.61

3.3 Conclusion

Equalization and termination matching can be easily achieved in feed forward equalizer with current mode logic(CML). However it suffers from poor efficiency, hence an open drain CML architecture is chosen with the termination implemented using cross coupled transistors minimizing power consumption. The designed on die termination is used to drive data across a 32inch backplane at 10Gb/s with swing of $0.6V_{p-p}$ and efficiency of 0.603pJ/bit and generate random jitter of 3.25ps which meets the jitter and swing specifications of 10BaseKR standard. This design achieves better performance by striking a tradeoff between power consumption of 0.6mW and jitter of 3.25ps on competing with state of art literature.

Chapter 4

A Low Input Referred Noise Dynamic Comparator for High Speed Applications

4.1 Introduction

Comparators play an important role in design of analog and mixed signal circuits. Comparators that employ regenerative feedback both in input pre-amplifier stage and output stage are considered. The designed comparator resolves 5mV with resolution of 8 bits and dissipates 11mW of power using 1.2V supply in 130nm CMOS technology while operating at clock frequency of 1.25 GHz. Comparators are used in the design of analog to digital converters resolving the bits based on the required resolution. The main constraints involved in the design of comparator varies with application and resolving time. Operational transconductance amplifiers work as high speed comparators in open loop but with reduction of minimum channel length the available voltage headroom is reduced which reduces both gain and voltage swing. Circuit's topology such as cascode when use in output stage in Op-amps reduce the available swing. Conservation of power has opened the circuit design to look for topology such as dynamic comparator [107]-[111] relative to its counterpart i.e. static comparator.

4.2 Conventional dynamic comparator [68]

4.2.1. Operation

Dynamic comparators are realized in several ways [110]-[111]. The basic circuit of conventional dynamic comparator is shown in Fig.4.1 [68].

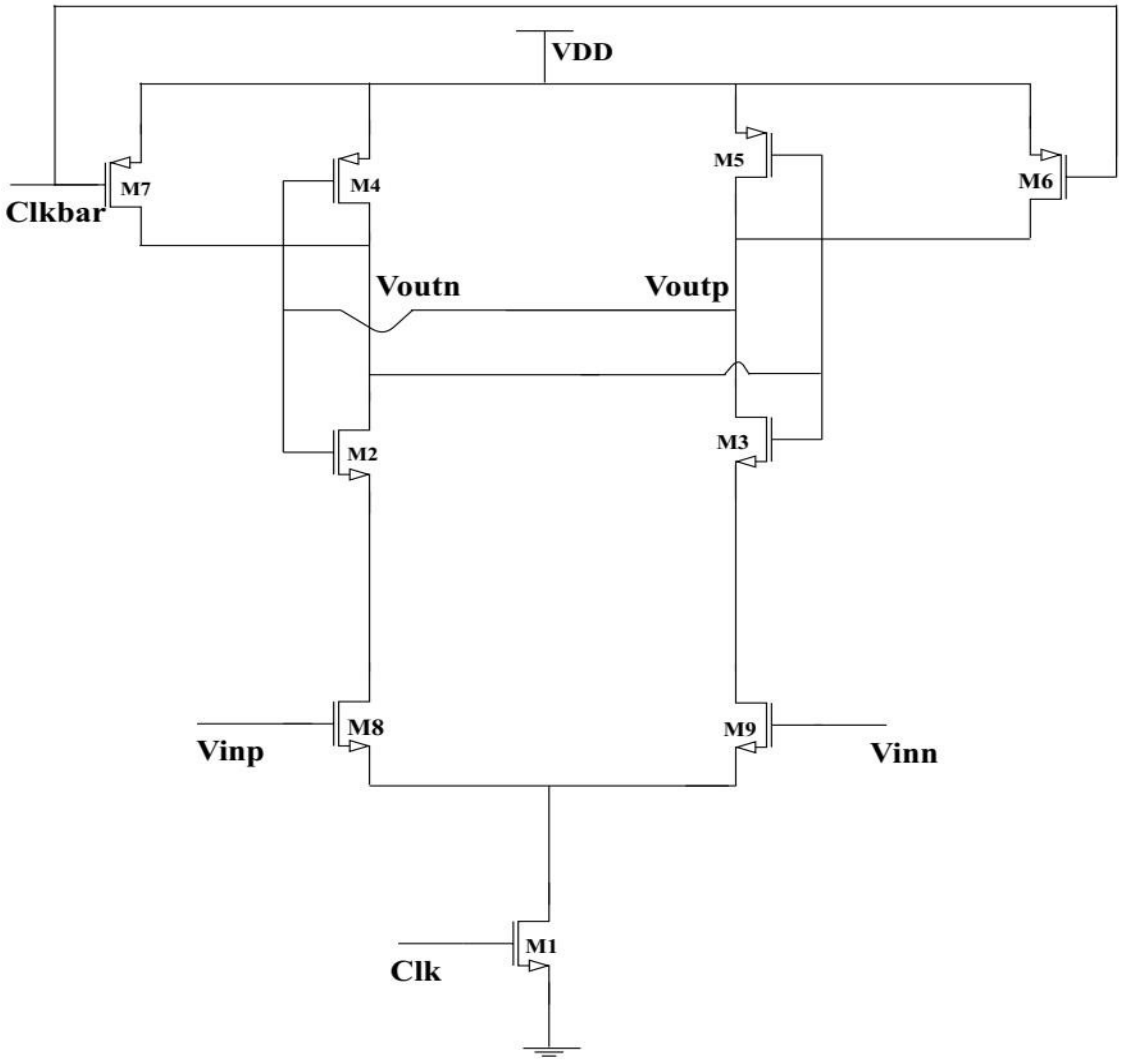

Fig.4.1 Schematic of conventional dynamic comparator

The operation of above circuit is as follows. Initially when clk is low, transistors M1, M8, M9 operate in cutoff region and transistors M7 and M6 are turned on. This phase of operation is reset phase. Nodes V_{outp} and V_{outn} are now pre charged to supply potential. In the next clock phase i.e. when clk is high transistors M1, M8 and M9 begin to turn on and draw current. The voltage stored across parasitic capacitance present at the output nodes begins to change according to the differential input voltage. After certain amount of time the cross coupled pair start to operate until one of the transistor turns off and other turns on completely. This is the regenerative phase. There are certain problems associated with the above circuitry such as kickback noise and limited gain. The kickback noise is due to low impedance path between the output nodes and inputs due to parasitic capacitance.

4.3 Conventional double tail dynamic comparator [68]

4.3.1 Operation

The circuit of conventional double tail dynamic comparator is shown in Fig.4.2. When clk is low the transistors M1, M2 M3 and M12 are in cutoff region, transistors M4, M5 are turned on. So there is no power dissipation. The intermediate nodes vp1,vn1 (gate nodes of transistors M6 and M7) pre-charged to supply voltage which in turn turns on transistors M6,M7 which pulls the output nodes Voutp and Voutn low. This is the reset phase of comparator. When clk is high transistors M1, M12 are turned on. The voltage stored across parasitic capacitance present at the intermediate output nodes vp1,vn1 begins to change according to the differential input voltage. According to difference of voltage across vp1,vn1 nodes transistors M6 and M7 start discharging the V_{outp} and V_{outn} nodes. As clkbar is low, transistor M12 is turned on. The two cross coupled transistors form a positive feedback loop and the voltages across nodes start to regenerate according to input voltage difference. The problem of kickback noise is reduced by adding M6 and M7 transistors.

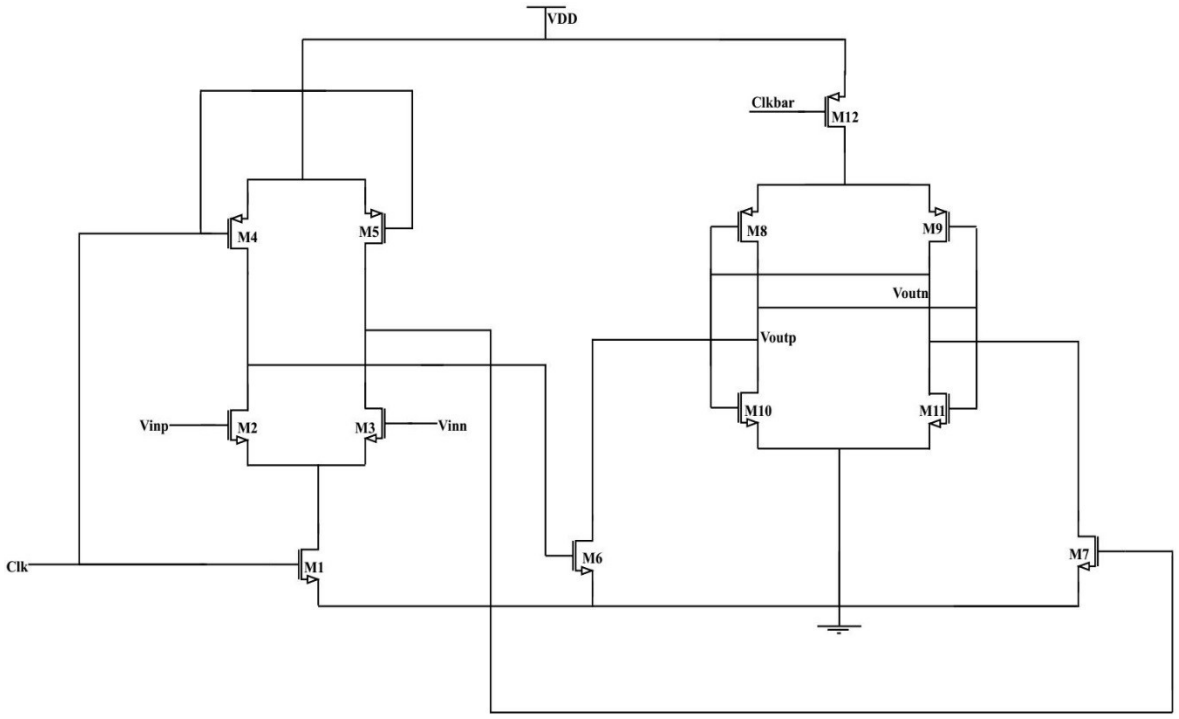

Fig.4.2 Schematic of Conventional dual tail dynamic comparator

The output of conventional dual tail dynamic comparator is shown Fig.4.3. An input differential voltage v_{id} 5mV applied at the input of comparator. When clk is low, the comparator is in reset phase, so both outputs are discharged to ground. When clk is high both

the output nodes start to rise until t_0 after which one of output discharges while other charges to the supply.

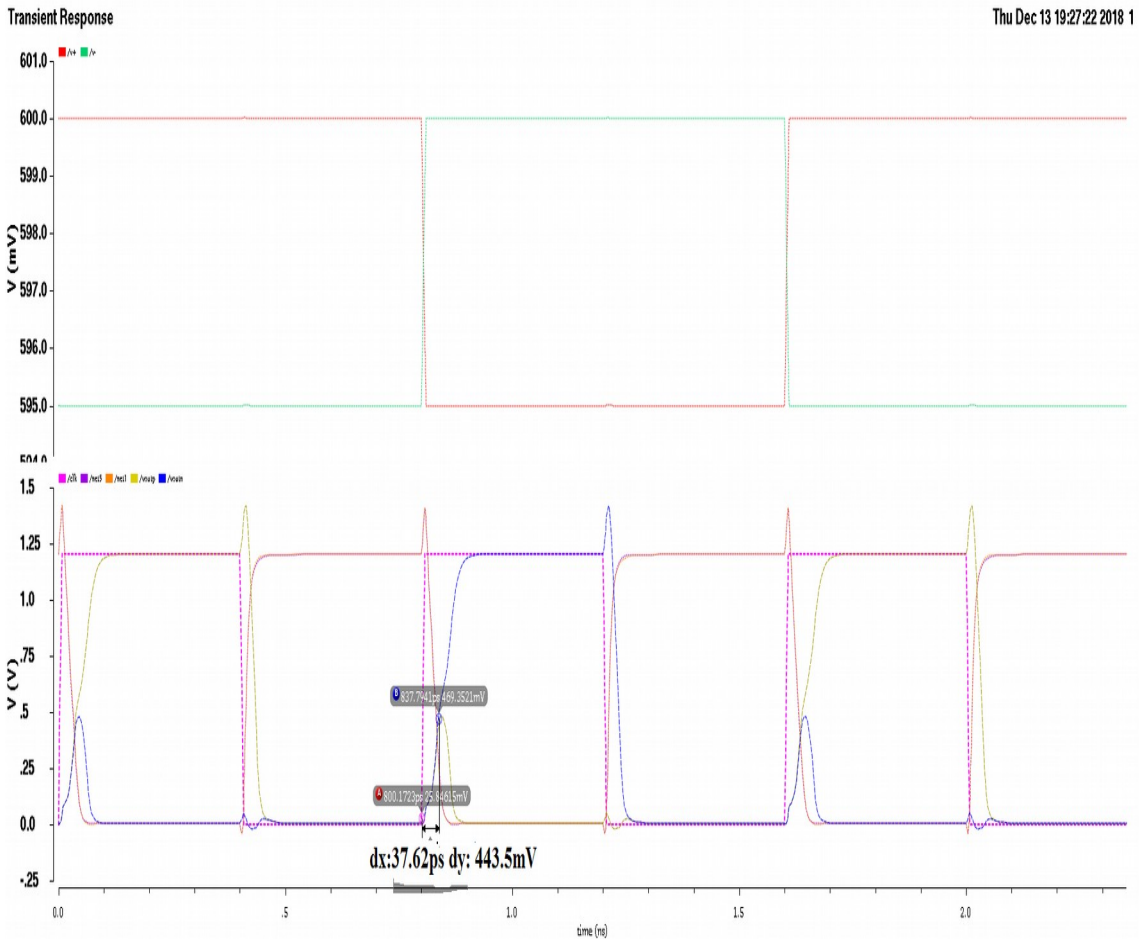

Fig.4.3 Output of conventional double tail comparator

4.4 Double regenerative double tail comparator [68]

4.4.1 Operation

The circuit of double regenerative double tail comparator is shown in Fig.4.4. The operation is as follows, when clk is low, transistors M16, M3, M4, M1, and M2 are turned off. The intermediated nodes v_{outp1}, v_{outn1} are pre charged high to the power supply which turns on the transistors M10, M11 that pulls the output nodes low. This is the reset phase. When clk is high, transistors M1, M3 are turned on. The voltage stored across parasitic capacitance present at the output nodes begins to change according to the differential input voltage. According to difference of voltage across V_{outp1}, Voutn1 nodes transistors M10 and M11 starts discharging the V_{outp} and V_{outn} nodes. As clkbar is low, the two cross coupled transistors

form a positive feedback loop and the voltages across nodes start to regenerate according to input voltage difference. When nodes voutp1 and voutn1 have discharged sufficiently low, transistors M14, M15 are turned on. The two transistors M14, M15 form a cross coupled pair. The potential across output nodes V_{outp} and V_{outn} start to increase until the two transistor M12 and M13 turn on. The two inverter pairs formed by transistors M14, M13 and M15, M12 form a cross coupled pair. This is regenerative phase. The time required to regenerate decreases as gain increases already in the input preamplifier stage due to the cross coupled pair formed due to transistors M2, M7 and M8, M3. The gain of this circuit is increased compared to circuit shown in Fig 4.2. The output of double regenerative double comparator is shown in Fig.4.5. The input v_{id} of 5mV is applied across gates of transistors M4.M5. The output nodes V_{outp},V_{outn} is low when clk is low. When clk is high, the both the outputs start to increase until the cross coupled pair regenerate after time $t_{0.}$.

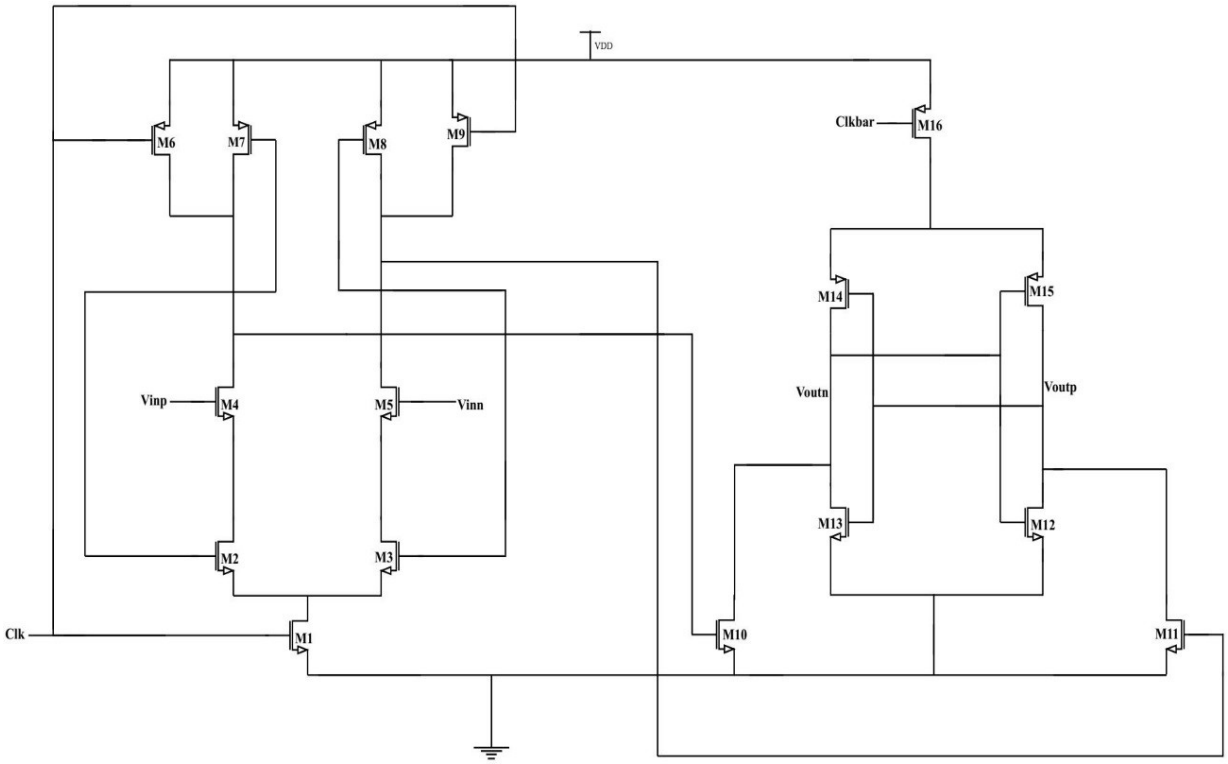

Fig.4.4 Double regenerative double tail comparator

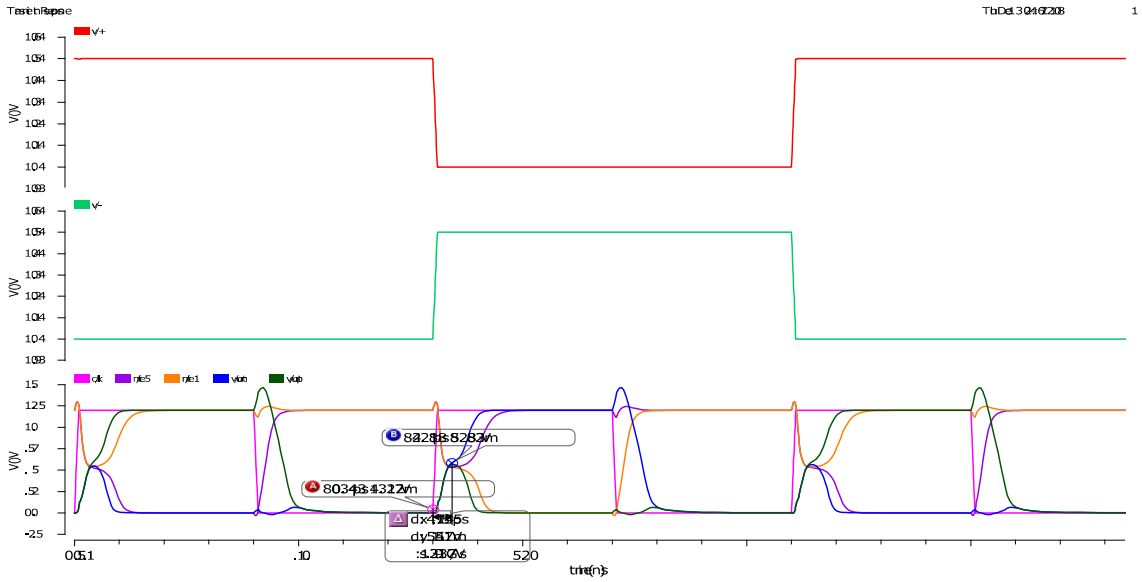

Fig.4.5 Output of double regenerative double tail comparator

4.5 Proposed regenerative dynamic comparator

4.5.1 Operation

The circuit of proposed regenerative dynamic comparator is shown in Fig.4.6. Initially when clk is low, transistors M1, M2, M3, M_{tail}, are turned off and transistors M7, M8 are turned on. The intermediate output nodes v_{outp1},v_{outn1} are pre-charged high. The output nodes are pull low as transistors M11, M12 are turned on. As clock is high, transistors M1,Mail is turned on. The transistors M6, M9 begin to turn on as the node voltages begin to drop, which in turn switches on the cross coupled pair formed by transistors M6,M9. When the intermediate node voltages begins to rise the transistors M2,M3 begin to turn on, the two inverter pair M6,M2 and M9,M3 form a cross coupled pair further boosting the gain. The gain is boosted in output stage by gain boosted cascode which is configured as class C inverter. The circuit here employ gain boosting technique which increases the output resistance. The back to back connected gain boosted cascode stages are in positive feedback loop which further increases the gain. The output wave forms of proposed regenerative dynamic comparator is shown in Fig.4.7. Input differential voltage v_{id} of 5mV is applied to input of comparator. When clk is low, the intermediate nodes v_{outp1}, v_{outn1} are pre-charged high, which pulls the output nodes low. This phase is reset phase of the comparator. When clk is high the tail current sources are turned on. The gain is increased in the input preamplifier stage, which reduces the kickback noise.

All the above discussed comparators have rail to rail signal excursions at the output nodes. This causes the kickback noise. The high speed and power efficient dynamic comparator architectures necessitate one to explore techniques to reduce the kickback noise. There are many circuit topologies present in the literature to minimize the effect of kickback noise. S. Babayan-Mashhadi et al [97] proposed neutralization technique to reduce kickback noise by coupling the signal across the drains of signal transistors which change in opposite direction to input. An attempt was made to reduce KBN by providing a low impedance path from the output pre-amplifier stage to ground during pre-charge phase. This disables the path between the regenerative stages and pre-amplifies stage.

The topology presented in this thesis uses class-C inverter stage as output to reduce kickback noise. As output resistance is increased the kickback noise is attenuated by as factor of gain. This reduces the kickback noise. The concept of increasing the output resistance can be understood from Fig.4.8.

The transistors M3,M1 form cascode amplifier, while transistor M2 is used for gain boosting. The currents i1,i2,i3 are the currents flowing through the transistors M1,M2,M3. As the current 'i' is a function of input gate to source voltage and drain to source voltage, the mathematical analysis is shown by equations. It can be seen that the output resistance is boosted by a factor of A2*A3, where A2 and A3 are the self -gains of M2 and M3 transistors.

$$i1 = gm1 * f(vgs) + gds1 * f(vds) \tag{4.1}$$

$$i1 = gm1 * 0 + gds1 * v1 \tag{4.2}$$

$$i1 = v1 * gds1 \tag{4.3}$$

$$i3 = gm3 * (v2 - v1) + gds3 * (v0 - v1)$$

$$i3 = gm3 * v2 - v1 * (gm3 + gds3) + gds3 * v0 \tag{4.4}$$

$$v1 = rds1 * i1$$

$$v2 = -v1 * gm2 * rds2 \tag{4.5}$$

$$as, i1 = i3 \tag{4.6}$$

$$\left(\frac{v0}{i1}\right) = rout = rds1 * (A3 + 1) + rds1 * A2 * A3 \tag{4.7}$$

$$rout \approx rds1 * A2 * A3$$

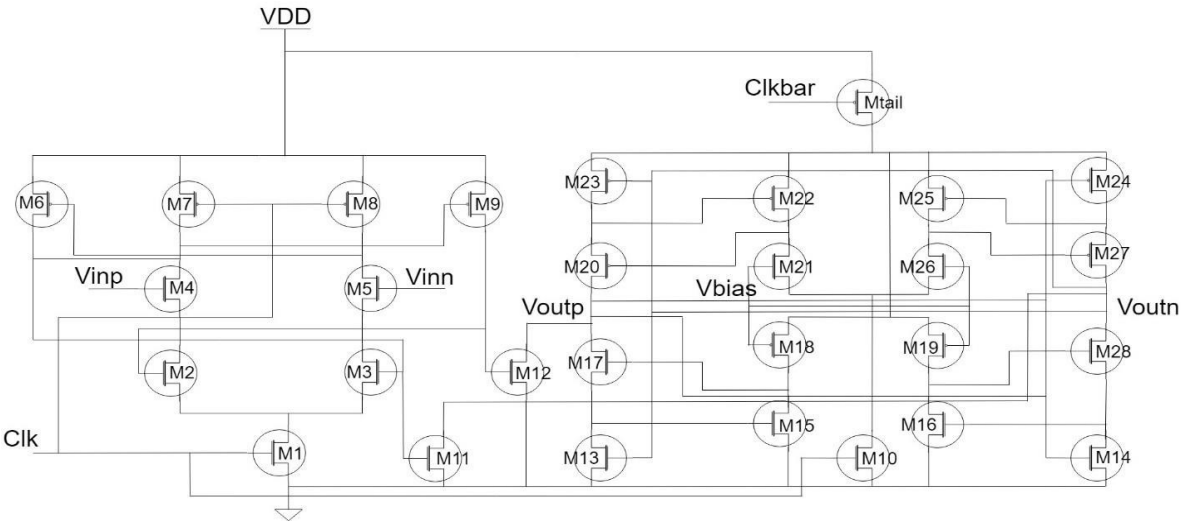

Fig.4.6 Proposed regenerative dynamic comparator

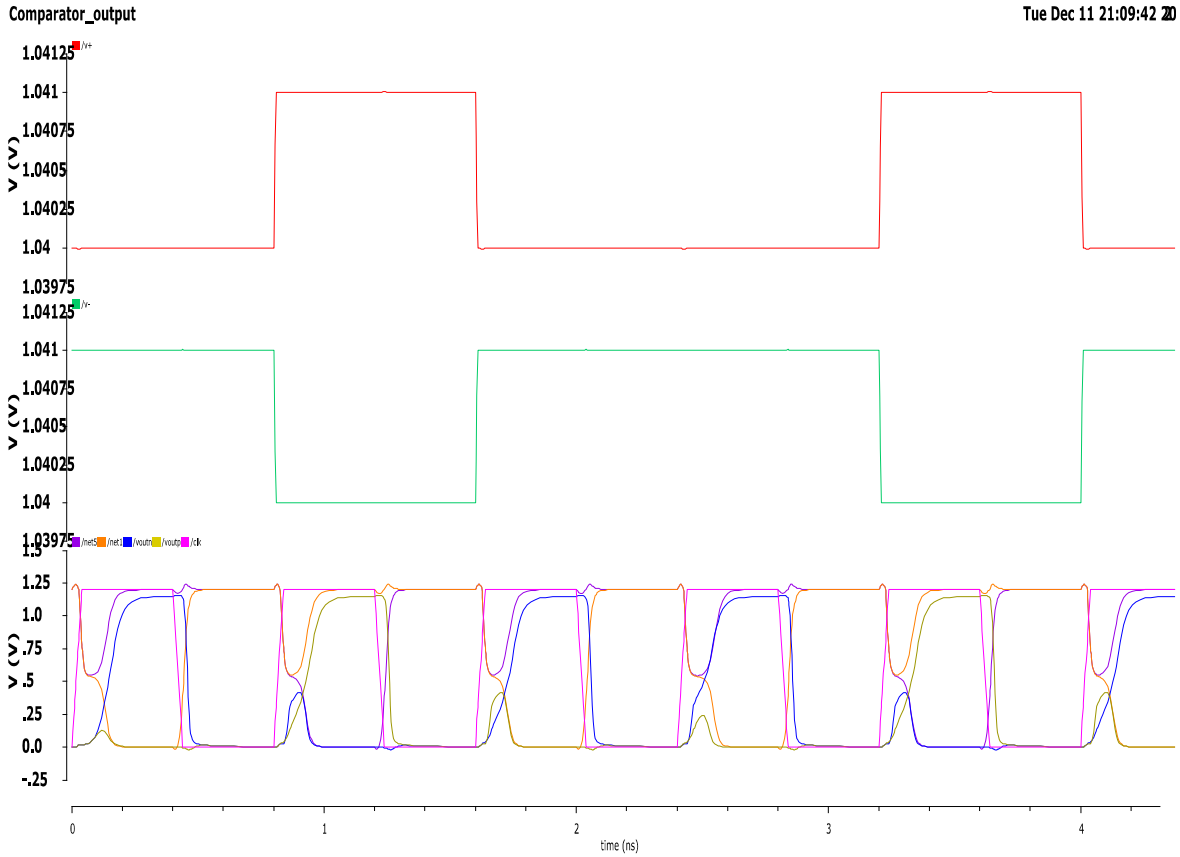

Fig.4.7 Output of proposed regenerative dynamic comparator

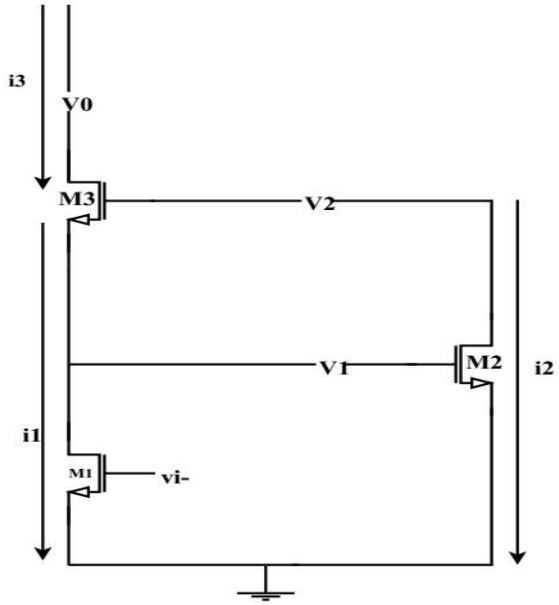

Fig 4.8 Circuit used calculating output resistance in proposed regenerative dynamic comparator

4.6 Results and Discussion

The designed comparator exhibits offset voltage of 0.59mV of offset without cancellation. The output is measured using Monte Carlo sampling method for 200 samples and can be seen in Fig.4.9.

The designed circuit shows a kickback noise of 25.6e-6V by following the procedure used in [89].

The sensitivity of high speed serial link at the receiver is given by eq 4.8. It can be seen the sensitivity is a linearly dependent on input referred noise,offset and latch resolving capability. For BER 10^{-12} $SNR^{0.5}$ =7, and V_n^{rms} =1mv, $V_{min}+V_{offset}$<2mV,gives the minimum eye opening of 20mV.

$$V_s^{PP} = 2V_n^{rms}\sqrt{SNR} + V_{\min} + V_{offset} \tag{4.8}$$

So by reducing the input referred noise and kickback noise, the sensitivity of receiver can be improved. The input referred noise of circuit is

$$\bar{v}_{n,in}^{2} = \left(\left(\frac{4kT}{gm} \right) + \left(\frac{k}{(c_{ox})(W * L)} \right) \frac{1}{f}) + \left(\frac{4KT}{(g_m^2) R_0} \right) \right) \tag{4.9}$$

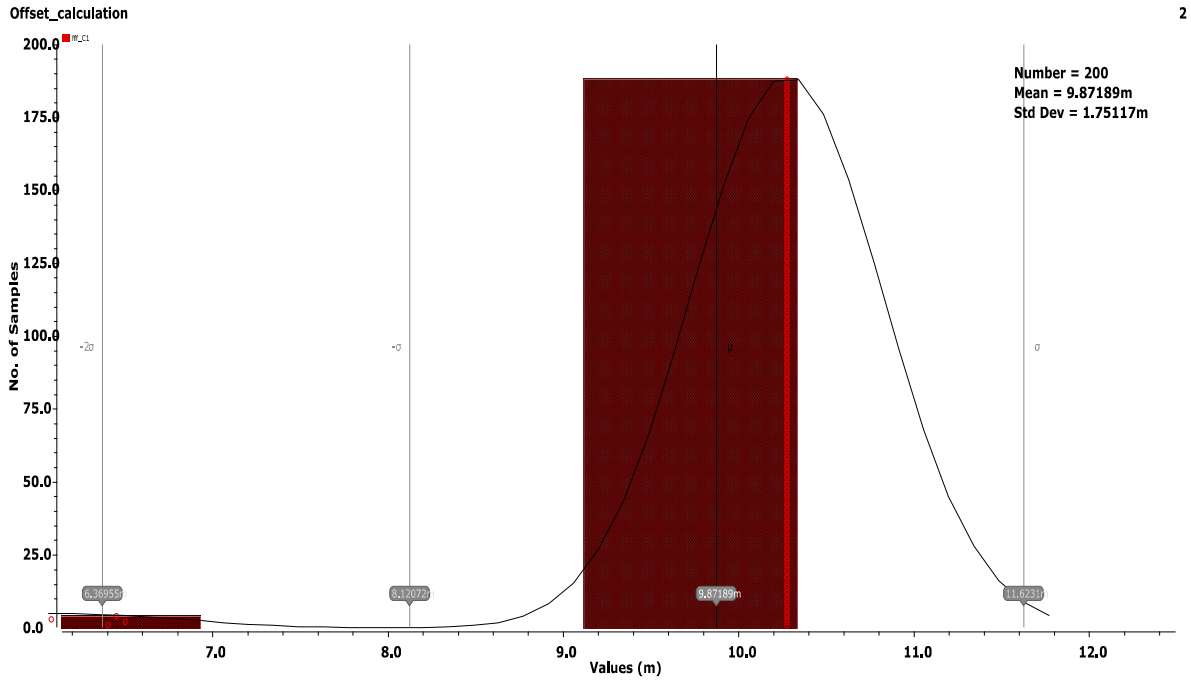

Fig.4.9 Output offset of proposed regenerative dynamic comparator

Where R_0 is the output resistance of gain boosted stage. The layout of proposed comparator is shown in Fig.4.10. It can be observed that increasing gain or output resistance decreases the input referred noise of the gain boosted comparator. Further it can observed from obtained results in TABLE 4.1 that the combined value of offset voltage and input referred noise is less than 2mV. A minimum gain of 240 is required to resolve the v_{id} which was achieved by employing gain boosting in the regenerative comparator stage.

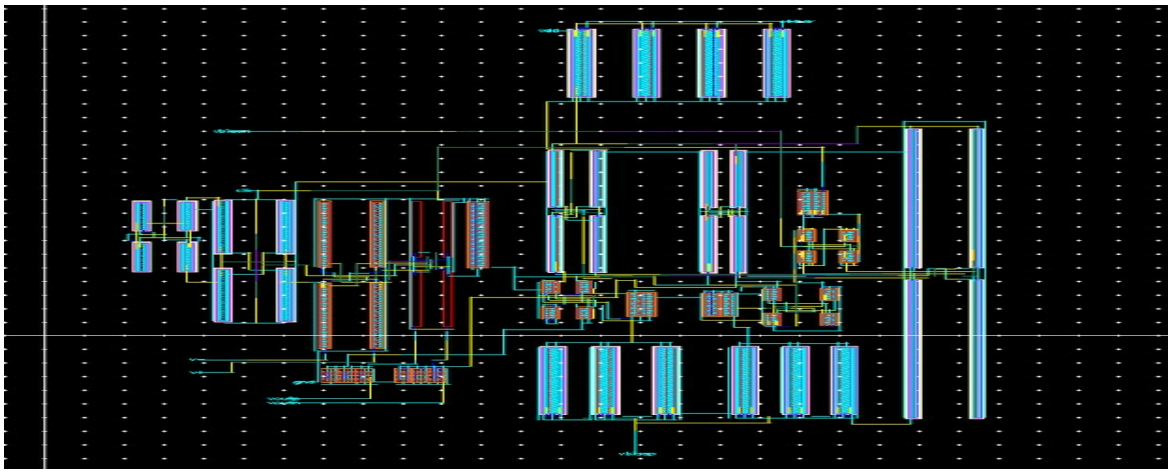

Fig.4.10 Layout of Proposed dynamic comparator

Table 4.1: Performance comparison of state of art dynamic comparators

Reference	[108]	[110]	[112]	[113]	This Work
Technology	180nm	65nm	65nm	180nm	130nm
Supply Voltage	0.8V	1.2V	0.6V	3.3V	1.2V
Clock Frequency	2.4GHz	500MHz	700MHz	250MHz	1.25GHz
Resolution	-	-	-	-	8 bits
Offset 3-sigma standard deviation	-	2.075mV	-	-	1.75mV
Output referred voltage	-	-	22mV	4mV	183.37µV
Kickback noise	43mV	-	-	1mV	29µV

4.7 Conclusion

Having identified the significance of comparator and its design tradeoffs, a gain boosted comparator is designed that achieves low input referred noise and reduced KBN which makes it very much suitable for high speed serial I/O circuit designs. The designed gain boosted dynamic comparator has resolving capability of 5mV in 0.133ns. The gain boosted comparator has kick back noise of 29µ V with input referred noise of 1.75mV

Chapter 5

Clock Generation and Recovery Circuits in High Speed Serial Links

5. Introduction

Interconnects play a vital role in communication between the sub blocks of a design. With the transistor scaling the processing speed of the individual subunit increased drastically but the communication between the subunits has not increased at the same pace. To mitigate the above problem, data are transferred through back-plane at high data rates.There are vaious design issues impact the efficiency of the high speed data transfer across back-planes. Circuit stategies to improve the performance of clock generation and recovery are presented in section 5.1 and 5.2 respectively.

5.1 A Low Jitter Phase Locked Loop for High Speed Serial Interfaces

This chapter presents a modified phase frequency detector which is used for clock generation designed in 130nm CMOS process technology. The phase locked loop is designed to meet the 10BaseKR wire line communication standards. All the circuits are designed in current mode logic for high speed operation by the virtue of advantages discussed in chapter 2. The designed circuit dissipates 6.6mW. The voltage controlled oscillator has phase noise of -114dBc/Hz at 1 MHz offset from center frequency. The designed phase locked loop has rms phase jitter of 44.17fs. Phase locked loop (PLL) plays an important role in many applications such as clock generation, clock and data recovery circuits, memory circuits, high speed

digital systems to generate very low jitter for on-chip clocks. Jitter has been an important design parameters in the design of PLL. Many factors such as loop bandwidth , damping ratio affect the jitter and stability of the phase locked loop(PLL).Very low bandwidth and high damping ratio are frequently used in obtaining low jitter [114]-[117]. This chapter presents circuit topologies to realize low jitter PLLs for backplane channels.

5.1.1 Phase Locked Loop

The performance of high speed systems is limited severely by clock skew, clock jitter and noise generated by various noise sources in circuits[119]. The block diagram of PLL is shown in Fig 5.1.1. There are various blocks in phase locked loop such as phase frequency detector (PFD), charge pump, loop filter, voltage controlled oscillator (VCO) and frequency divider. PFD compares the phase of reference clock and feedback clock.

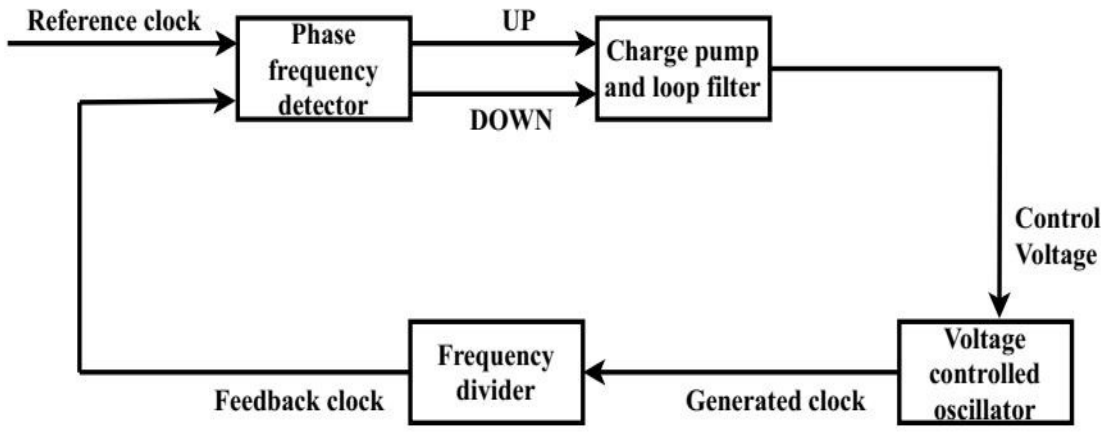

Fig 5.1.1 Block diagram of Phase Locked Loop [119]

5.1.2 Modified Phase Frequency Detector

There are two types of PD such as XOR PD and PFD [119]. The XOR PD has good noise rejection capabilities but locks onto harmonics of the clock thereby generating ripples even when loop is locked. This modulates the clock frequency which is an unwanted characteristic of PD. XOR PD has problems locking if the VCO duty cycle dithers around 50%. The block diagram of modified PFD is shown in Fig.5.1.2.

When both reference clock and feedback clock out of phase the up and signals tend to go high when feedback clock and low when feedback clock lags. When the phase difference between both the clocks is negligible, the loop ideally needs to be in locked state but drifts over time. So to counter it, a delay in the form of multiplexer and nand-gate is added to avoid the dead zone problem. When reference clock, feedback clock are in phase, the output of nand-gate is low, which sends the output of multiplexer to low, which resets the loop, for the clock cycle. So finite phase error is present in the loop which prevents the dead zone problem. It compares the leading edges of reference and feedback clock from the frequency divider. The rising edge of reference clock and feedback clock must be present to make a phase comparison. PFD does not lock onto harmonics. The up signal is high when the feedback clock lags the reference clock and down signal is high when reference clock leads the reference clock as shown in Fig.5.1.3.

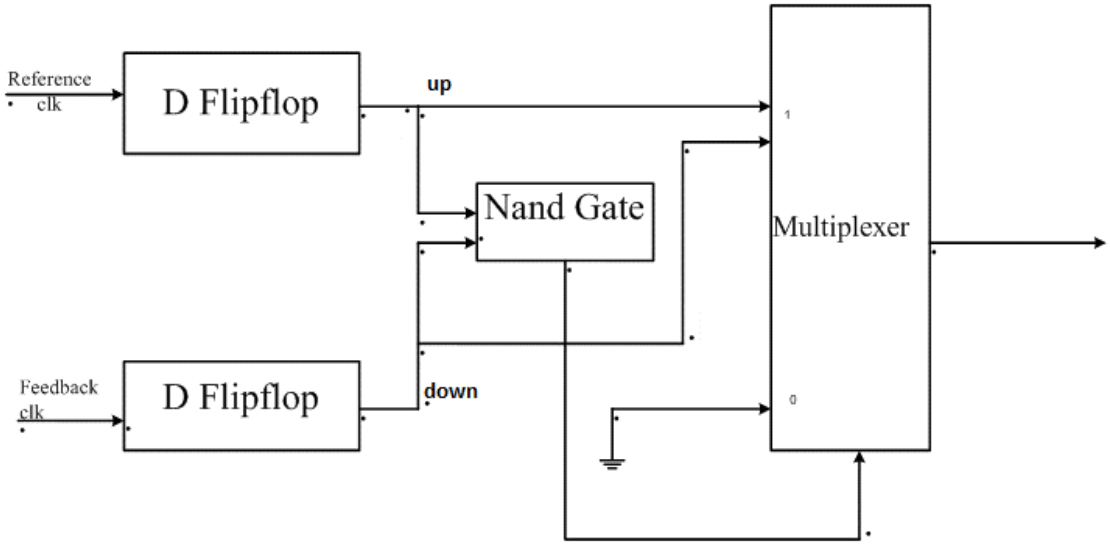

Fig.5.1.2. Block diagram of modified PFD

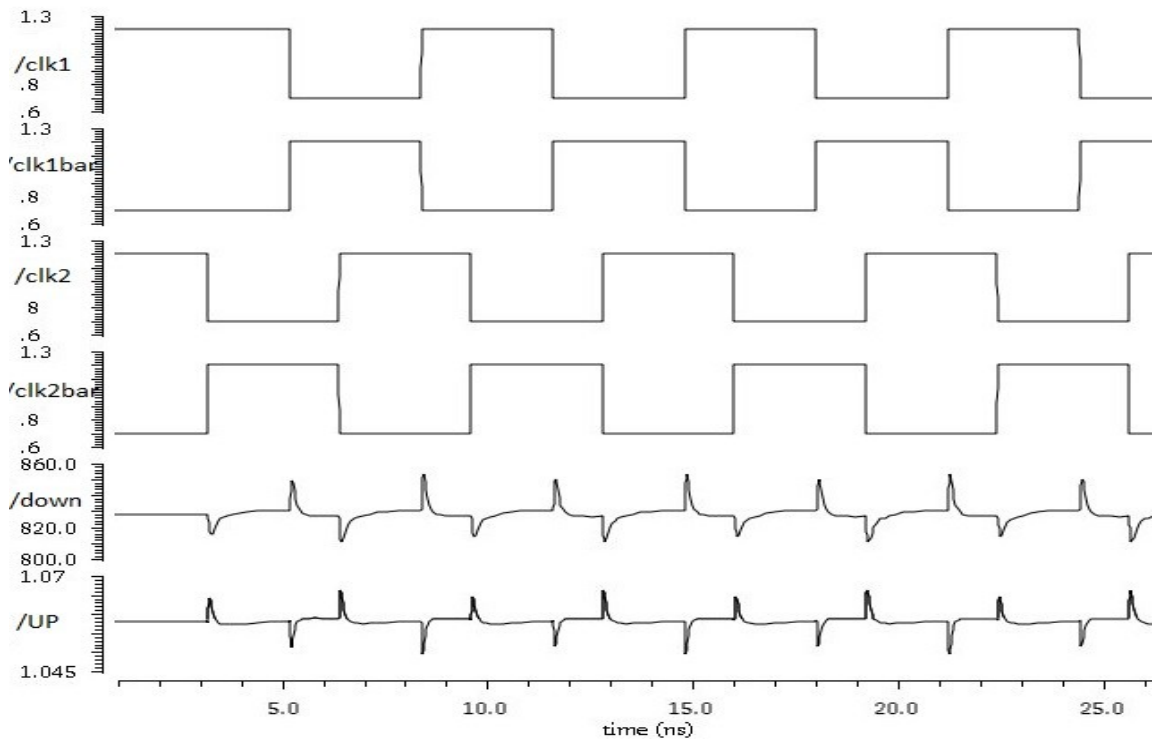

Fig 5.1.3 Output of Phase frequency detector

PFD converts the phase information to voltage signals that drives the VCO. This can be done in two methods as shown in Fig 5.1.4[119]. The main problem is that the output of charge pump shown in Fig 5.1.4[119] is dependent on supply. This dependency can be reduced by adding a current source as shown in Fig.5.1.4.b. Let I_{pump} represent the charge pump current. If the output of PFD uses the charge pump configuration of Fig5.1.4.b then the output current is given by $I_{PDI,}$ Where $\Delta\Phi$ represents the phase difference between the reference clock and feedback clock and K_{PDI} is the gain of PFD.

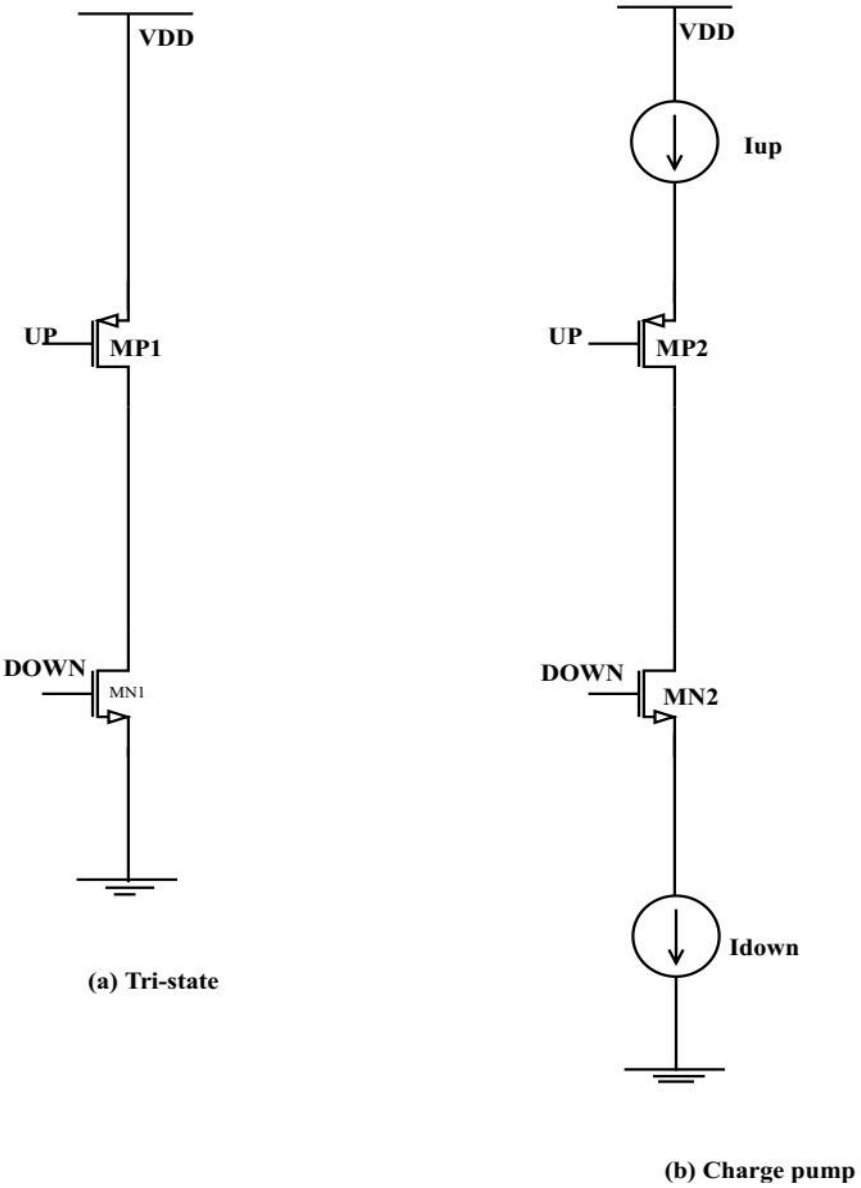

Fig 5.1.4 (a) Tri-sate (b) Charge pump outputs

$$I_{PDI} = (2I_{pump} / 4\pi)*\Delta\Phi = K_{PDI}*\Delta\Phi. \qquad (5.1.1)$$

It is assumed that equal current flows in the pull up and pull down structures. The second order effects such as channel length modulation which affects the MOS device to function as current source can be reduced by increasing the output impedance. The output impedance can be increased by cascode current mirror topology and by using gain boosting technique. Alternately current mismatch can be reduced by using reference charge pump method. The schematic of charge pump is shown in Fig.5.1.5 [119].

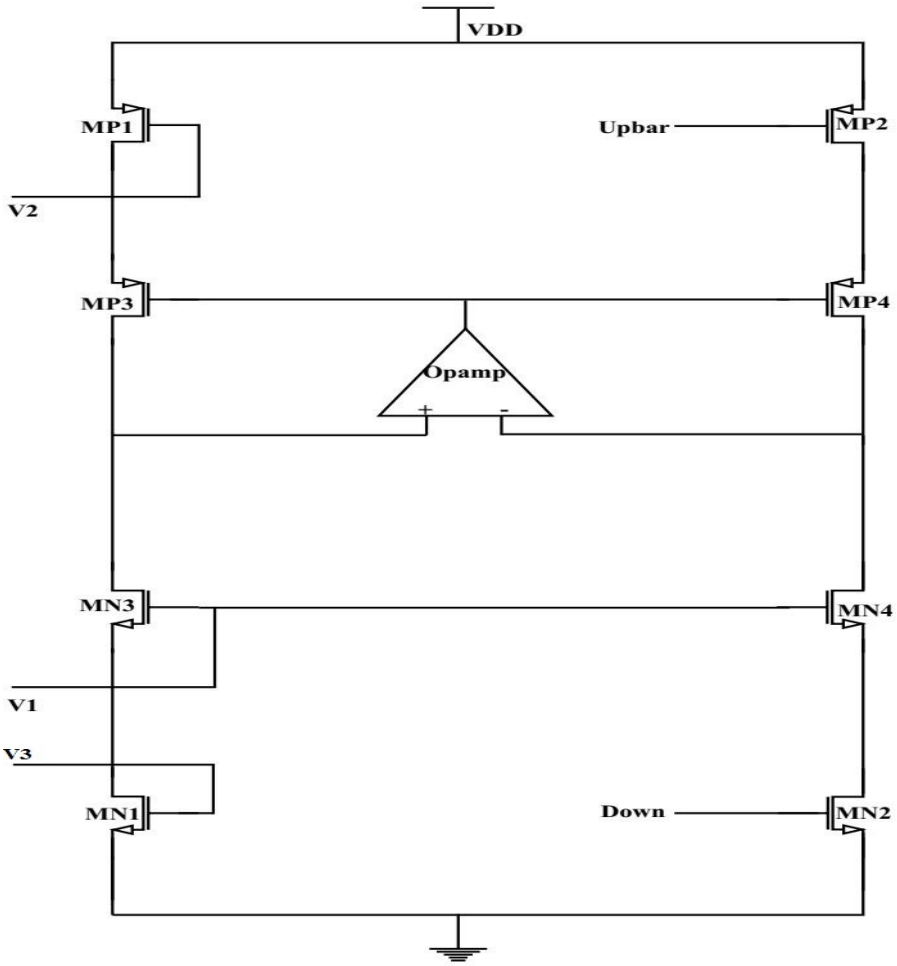

Fig.5.1.5 Schematic of charge pump [119]

The error amplifier compares the voltages at its input and generates an error voltage that drives transistors MP3, MP4 to minimize the current mismatch. The output of charge pump drives the LF circuit. The schematic of loop filter is shown in Fig.5.1.6. For slow variation in the output of charge pump the loop filter acts as integrator [119].

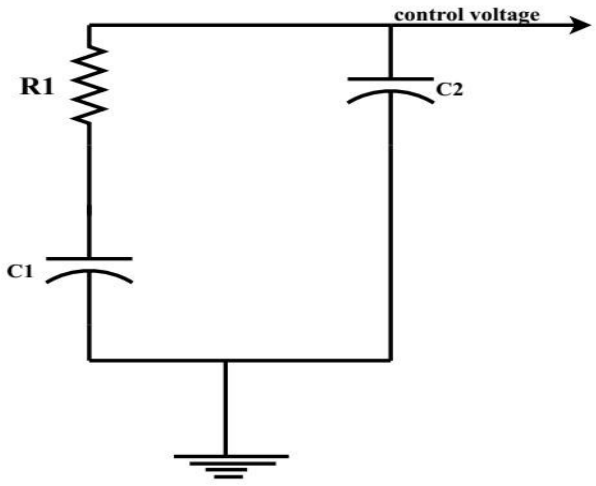

Fig 5.1.6 Loop filter

For fast variations the LPF acts as resistive divider which allows the loop to track fast variations. The output of LPF is shown in Fig.5.1.7.

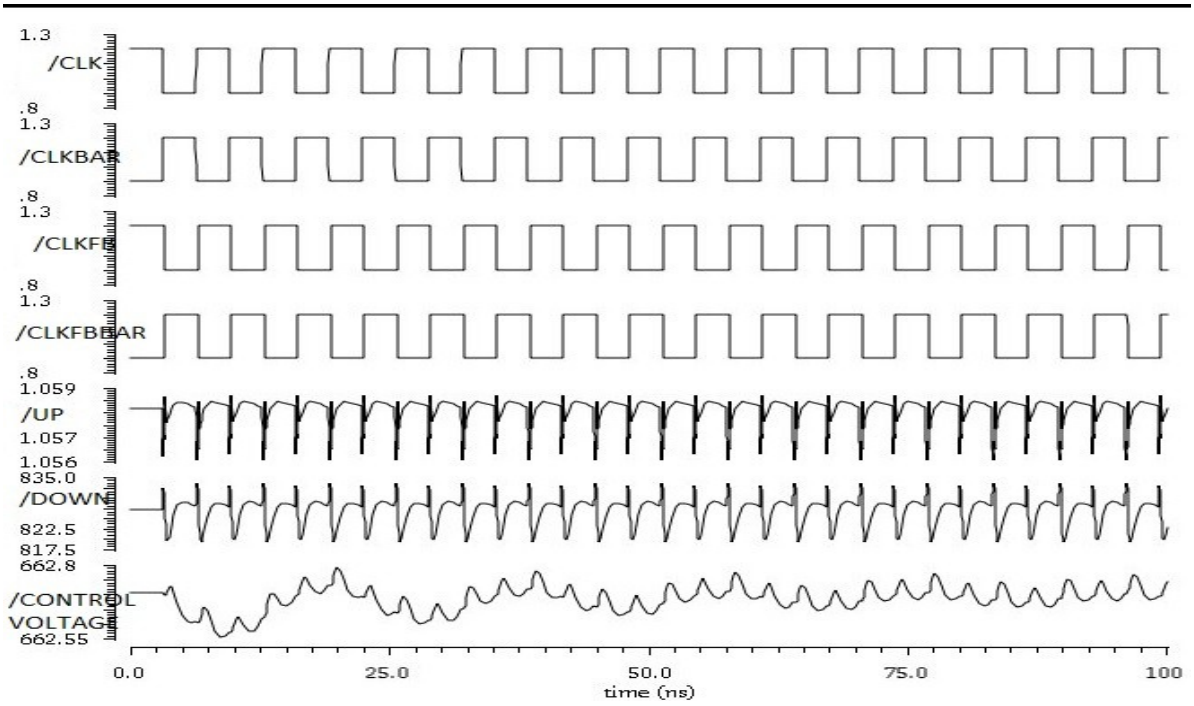

Fig.5.1.7 Output of loop filter

VCO can be realized through ring oscillators or LC oscillator. The output of ring oscillator is sensitive to supply voltage variations and noise in the circuit which favors LC oscillator as its phase noise is less compared to ring oscillator. For oscillations to begin a loop gain of greater than unity even in the presence of temperature and process variations is required. The schematic of LC oscillator is shown in Fig.5.1.8 [119]. The skin effect plays a vital role in design of the oscillator as the metal loss increases at higher frequency. Let R_s represent the series resistance of inductor. Let R_p be parallel equivalent of series resistance of the inductor,

$$R_p = Q^2 R_s. \quad (5.1.2)$$

$$V_{swing} = I_{bias} * R_{tank} \quad (5.1.3)$$

$$R_{tank} = 1/gm_{n,p} \quad (5.1.4)$$

$$gm_{n,p} = -2/R_p \quad (5.1.5)$$

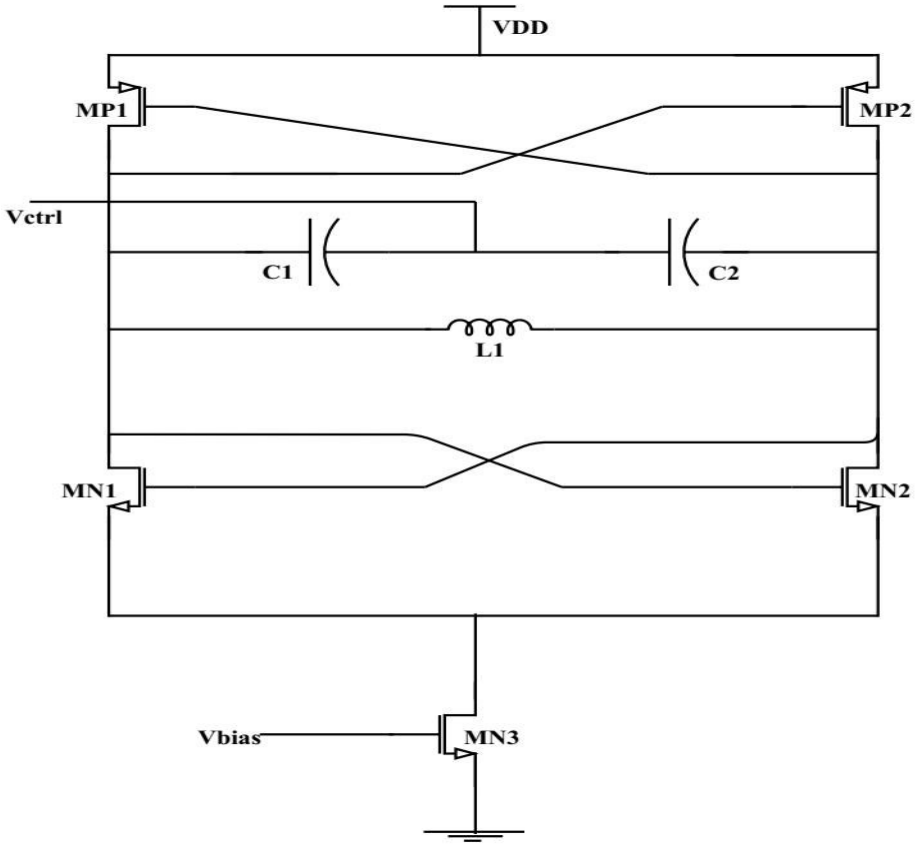

Fig 5.1.8 LC oscillator

Where Q is the quality factor of the inductor, $gm_{n,p}$ are the effective transconductance of N and P cross coupled transistors. The voltage sensitivity curve of VCO is shown in Fig.5.1.9, which shows VCO has gain of 1020Hz/V.

The figure of merit (FOM) of LC oscillator is used to compare the performance of VCOs [126].

$$FOM = 10\log\left(L\left(f_m\right)\right) + 10\log\left(\left(\frac{f_m^2}{f_{osc}^2}\right)\frac{P_{DC}}{1mW}\right) \tag{5.16}$$

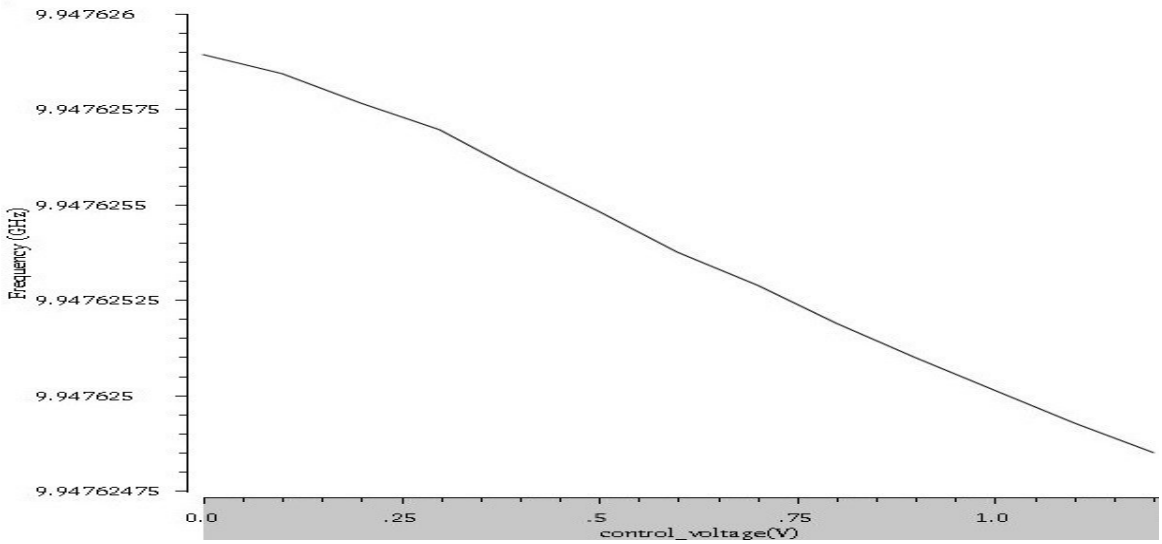

Fig 5.1.9 Tuning range of VCO

Where $L(f_m)$ is the phase noise , f_m is an offset frequency from center frequency f_{osc} , TR is the tuning range and P is the power dissipation. Table 5.1.1 shows the comparison among various LC oscillators designed.

TABLE 5.1.1 Performance comparison of LC VCO

Reference	Process	Freq (GHz)	Phase Noise (dBc/Hz)	Power (mW)	FOM_T
[120]	130nm	40	-110@1MHz	12	-184.9
[121]	130nm	59	-89@1MHz	9.8	-174.5
[123]	250nm	16.98	-108@1MHz	10.5	-184.2
[124]	350nm	9.8	-115@1MHz	11.61	-184
[125]	0.5µm	1.4	-107@1MHz	3	-185
This Work	130nm	10	-114@1MHz	6.64	-192.4

5.1.3 Conclusion

In this work an attempt is made to design PLL suitable for high speed serial links with reduced phase jitter of 44.17fs. This work explored the possibility of improving the LC-oscillator performance towards the better designs of PLL suitable for high speed serial links. The PLL designed offers a phase jitter of -114dBc/Hz at an offset frequency of 1MHz from the center frequency. The designed VCO consumes a low power of 4.6mW without buffer.

5.2 A 10-G bits/s Clock and Data-Recovery Circuit for Backplane Applications Using Dual Loop Architecture

5.2.1 Introduction

The increased data rates lead to increased bit error rates. The subunits on a chip communicate using input output pins. If there are more number of pins then all the parallel bus lines need to be synchronized along with meeting the design problems of clock skew, bit error rate (BER), setup time and hold time. The clock frequency is to be reduced in order to meet the timing specification which in turn lowers the data transfer rate. So the number of input output pins of design play an important role in the communication between the subunits. Reducing the input output pin count of each subunit necessitates the clock to run faster so that higher data rate is achieved. The data are to be serialized before transmission. Clock is embedded into the data. So, at the receiving unit the clock should be extracted from the data and data are to be sampled at the middle of each sample duration. Salient features of CDR include "clock retrieval from data with lower BER, lower clock jitter and phase noise. In CDR circuits phase locked loop is used for generating the clock required for sampling the incoming data. Linear phase detectors limit the maximum data rate which prompt the usage of half, quarter and octave phase detectors [127]-[130]. Unless initial frequency of VCO is close near to baud rate of incoming data, the bit error rate shoots to significantly larger value. Clock and data recovery are also designed using dual loop architectures [129], [133]. A novel idea for clock and data recovery circuit and a circuit for delay latch are implemented.

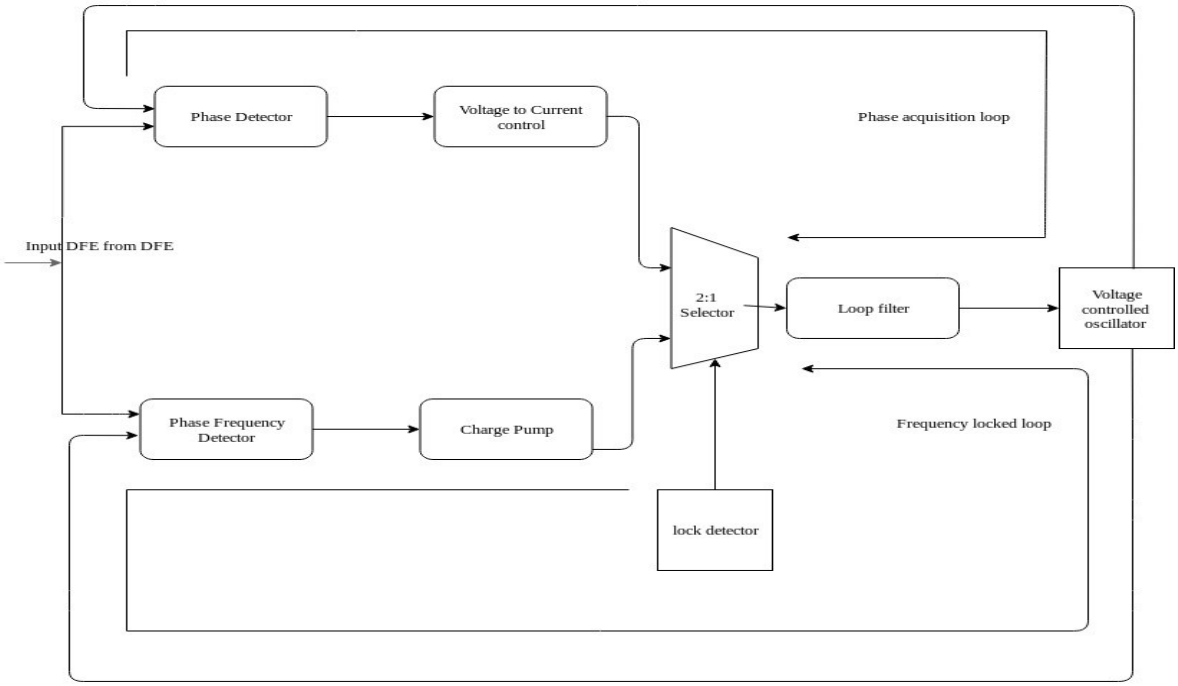

Fig 5.2.1 Block diagram of Dual Loop Clock and Data Recovery Circuit [84]

5.2.2 Architecture

The block diagram of designed CDR circuit uses dual loop architecture as shown in Fig. 5.2.1[84]. The lock detector transfers the control to phase tracking loop when frequency of clock is extracted from the data. The frequency acquisition loop consists of bang–bang phase detector. The phase detector controls the VCO.

The backplane has the characteristics of a low pass filter. The chip package limits the throughput. In dielectric the speed goes down by factor of $\sqrt{\varepsilon_r}$ where εr is the relative permeability of the dielectric. The channel is modeled by distributed components such as capacitance, inductance and resistance. The characteristic impedance is equal to ($\sqrt{L/C}$), where L and C denote the parasitic inductance and capacitance. There are various losses in channel such as reflections, skin effect and dielectric loss. Reflections may arise due to printed circuit board impedance mismatch, via impedance mismatch and connector impedance mismatch. At high frequencies the current crowds along the surface of the conductor causing skin effect. Skin depth is inversely proportional to $\sqrt{f}$. This effect starts when skin depth is equal to conductor radius. The dielectric loss is often specified in terms of loss tangent. Its transfer function is $e^{-(Gd*Lcon)}$ where L_{con} denotes the length of the conductor

or channel length and G_d denotes the conductivity of the dielectric [132]. Molex FR4 is used as backplane here. The frequency response shows a channel of 14.74dB as observed from Fig.5.2.2.

$$G_d = \pi * f * \tan\varepsilon * \sqrt{L * C} \tag{5.2.1}$$

$$\tan\varepsilon = \left(\frac{G}{(w * C)} \right) \tag{5.2.2}$$

Where G_d is the conductance of the dielectric, f is the frequency of the data measured in Hz. So from the Fig.5.2.2, it can be seen the channel loss is below 20dB which permits the realization of receiver circuit using NRZ signaling.

When CDR transits from frequency acquisition loop to phase tracking loop, there is no degradation in the phase margin and loop bandwidth remains constant. The CDR proposed in [133] changes the loop filter parameters to avoid the decrease in the phase margin and increase in loop bandwidth. The designed CDR circuit is solution to the above problems along with meeting the backplane specifications. When the loop changes from frequency acquisition to phase tracking mode, the loop bandwidth and phase margin are degraded which was compensated by varying the loop filter parameters [133].

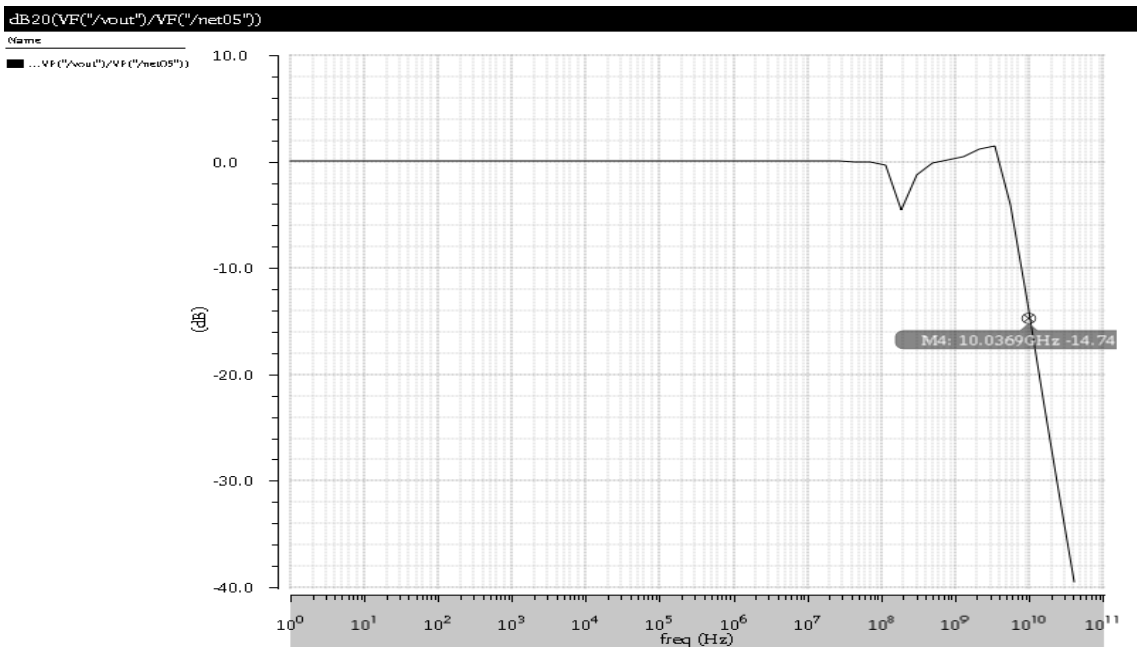

Fig 5.2.2 Frequency response characteristics of Molex FR4 21 inches back-plane

The novelty in designed CDR is the necessity of varying loop parameters is avoided. Since half rate phase detector is clocked by half the data rate, a voltage controlled oscillator which generates half the frequency is designed. Towards the end, many half rate phase detectors were designed [127],[128],[134] but the phase detectors have unbalanced load. A half rate phase detector can solve this issue [133]. The schematic of half rate phase detector is shown in Fig 5.2.3.

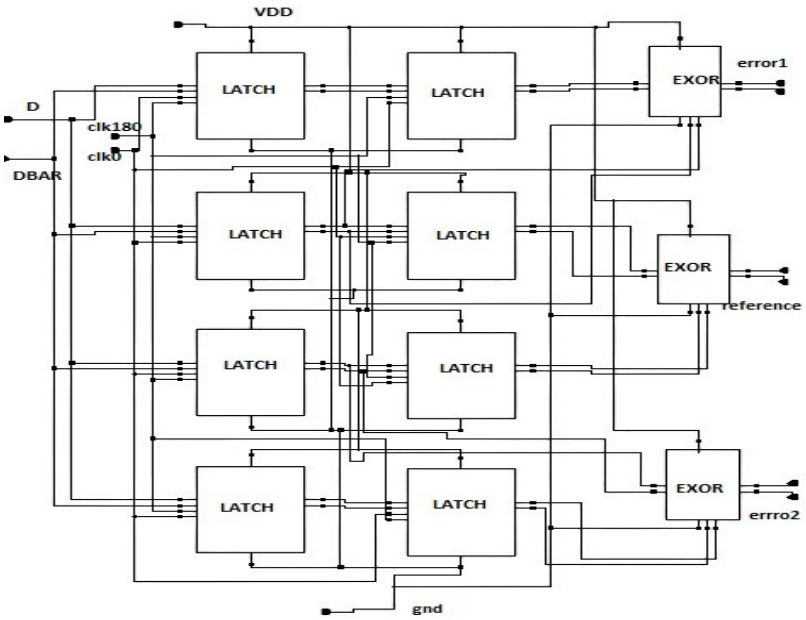

Fig 5.2.3 Schematic of half rate phase detector [127]

The error1 signal is used for detecting data transition when clock is high and error2 signal is used for detecting data transition when clock is low. The error signals are 3/2 times of the reference signal. The reference signal is used for detecting the transitions at both the clock edges. The output of phase detector is shown in Fig.5.2.5. Current is injected using a voltage to current converter (VIC)[134].

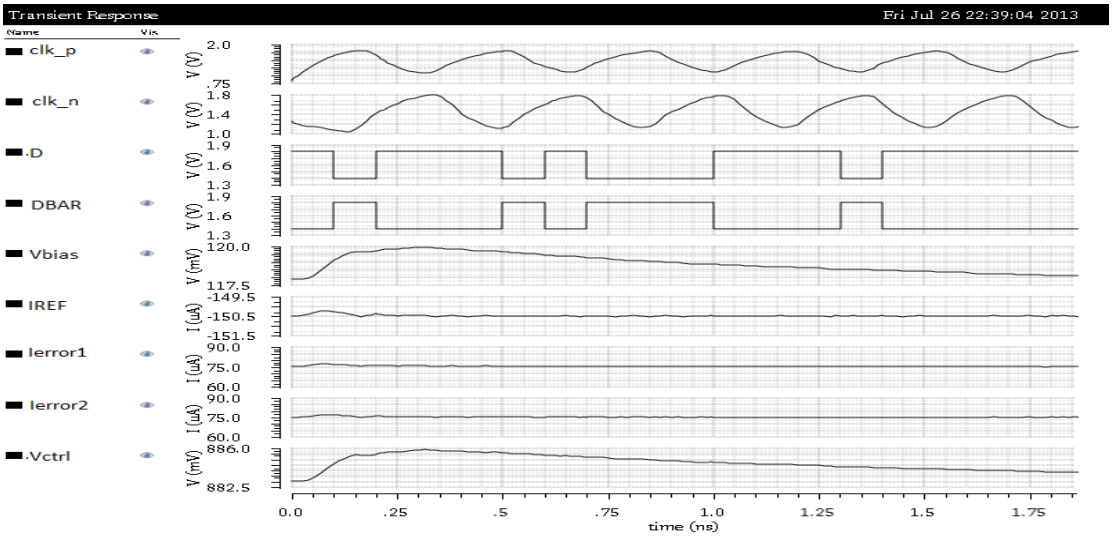

Fig 5.2.4 Output of Phase tracking loop

The signal clk is the output clock from phase tracking loop. D is the input data to CDR. V_{bias} is output of loop filter. I_{error1}, I_{error2} and I_{REF} are output currents for error1, error2 and REFERNCE voltages from half rate phase detector. The output of phase tracking loop is shown in Fig.5.2.4.

5.2.3 Frequency Tracking Loop

There are two types of phase detectors namely linear and nonlinear [129]. Bang- bang phase detector is a binary phase detector [129]. When the phase of incoming data is equal to feedback clock phase, the up and down signals are high .The flip flops are reset. A modified D-latch used in the design of modified bang-bang phase detector is shown in Fig.5.2.7. The circuit uses to two additional transmission gates T1, T2 and two additional transistors MZ1 and MZ2 in addition to conventional CML latch. When reset is low the transmission gates T1 and T2 offer low impedance path to inputs D and Dbar while MZ1 and MZ2 are in cutoff region. When reset goes high T1 and T2 offer high impedance to the differential inputs, MN1 and MP1 are turned on and operated in triode region of operation forcing input D to low ensuring output to logic low.

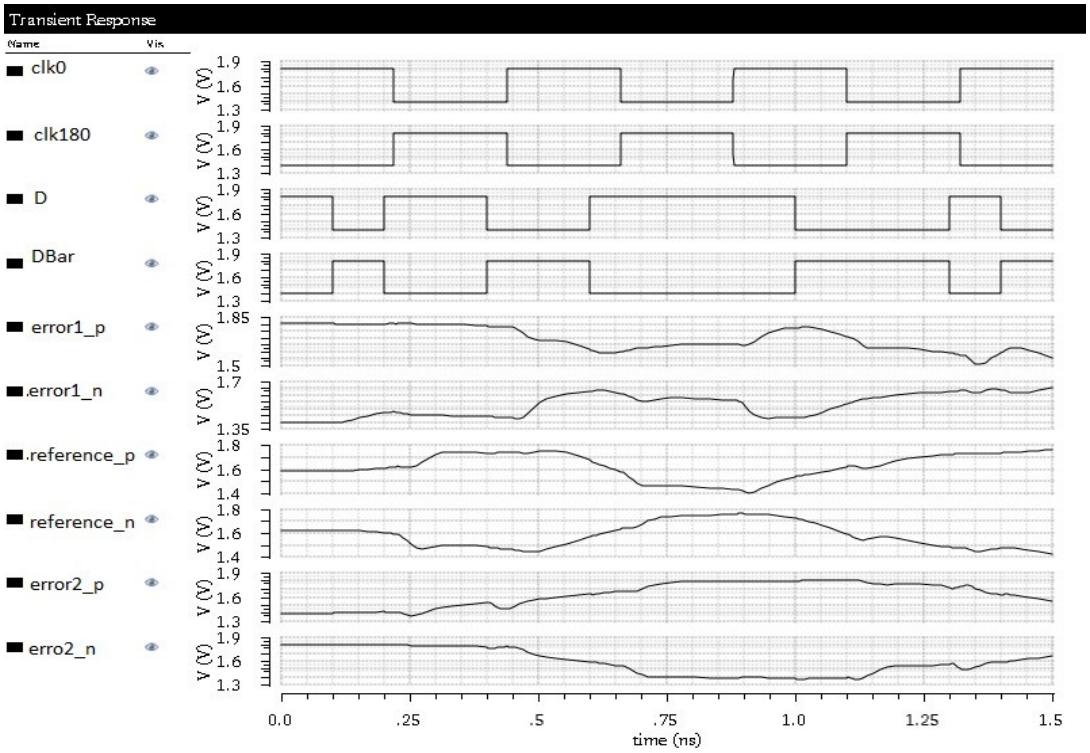

Fig 5.2.5 Output of half-rate Phase detector

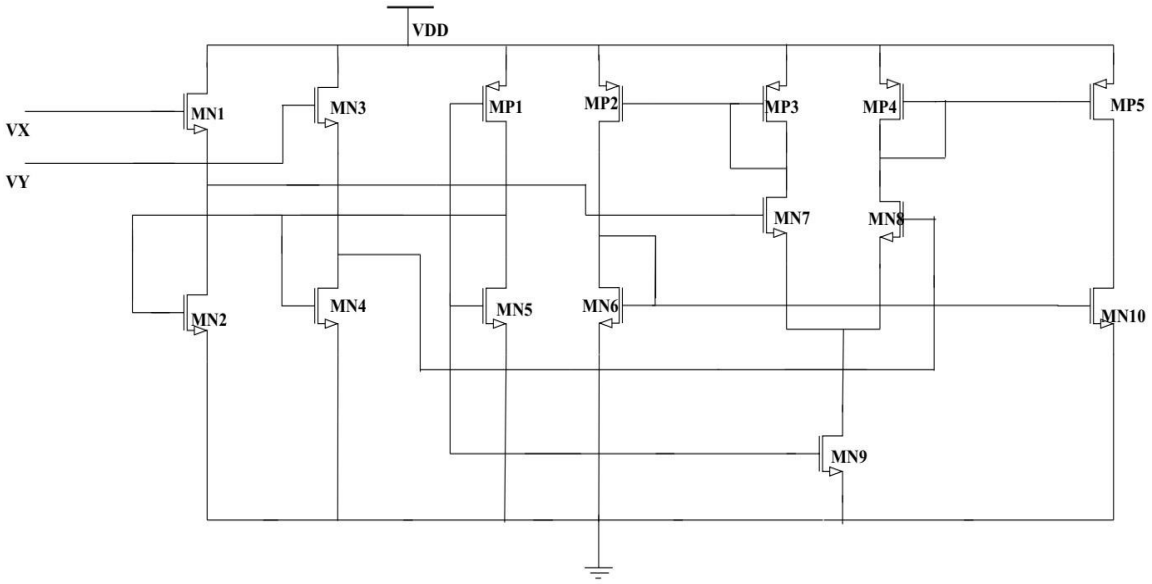

Fig 5.2.6 CML to CMOS converter

The logic levels are converted to CMOS logic levels using CML to CMOS logic converters shown in Fig.5.2.6.

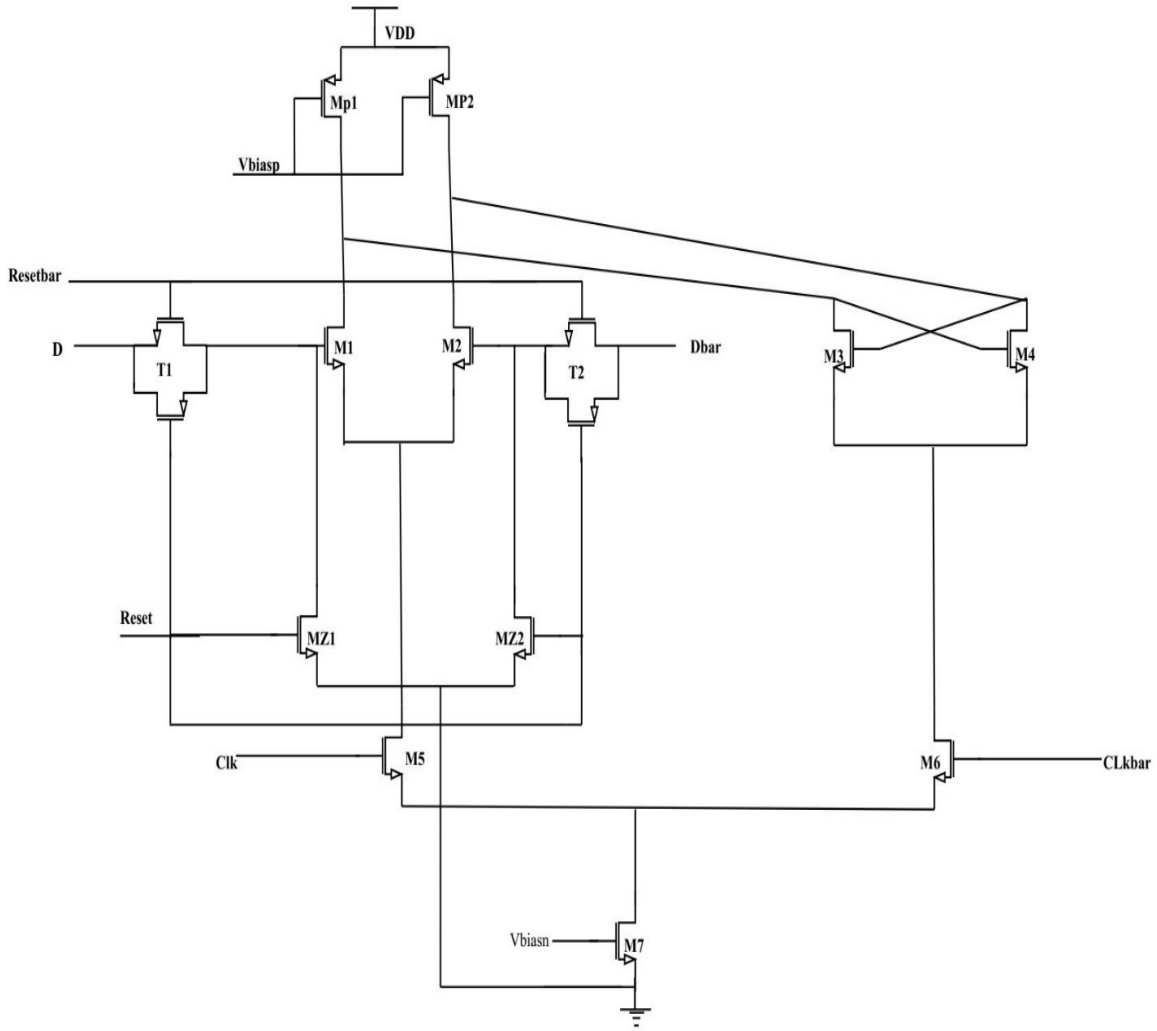

Fig 5.2.7 Modified D-latch

The true and complement inputs are tied to logic low and high during reset phase. For current injection a charge pump is designed [136] - [137]. The schematic of charge pump is shown in Fig.5.2.8.

Here signals ‘up’ and ‘down’ are used to control the charge pump. When the frequency of the feedback clock is less relative to the data the signal ‘up’ is high. When the frequency of the feedback clock is ‘high’ compared to the data, the ‘down’ signal is high. A loop controller is designed to stabilize the voltages of reference current path, charging and discharging paths.

5.2.4. Voltage Controlled Oscillator

A differential inverter is designed to serve as basic block for differential ring oscillator [136]. The schematic of differential inverter is shown in Fig.5.2.9.

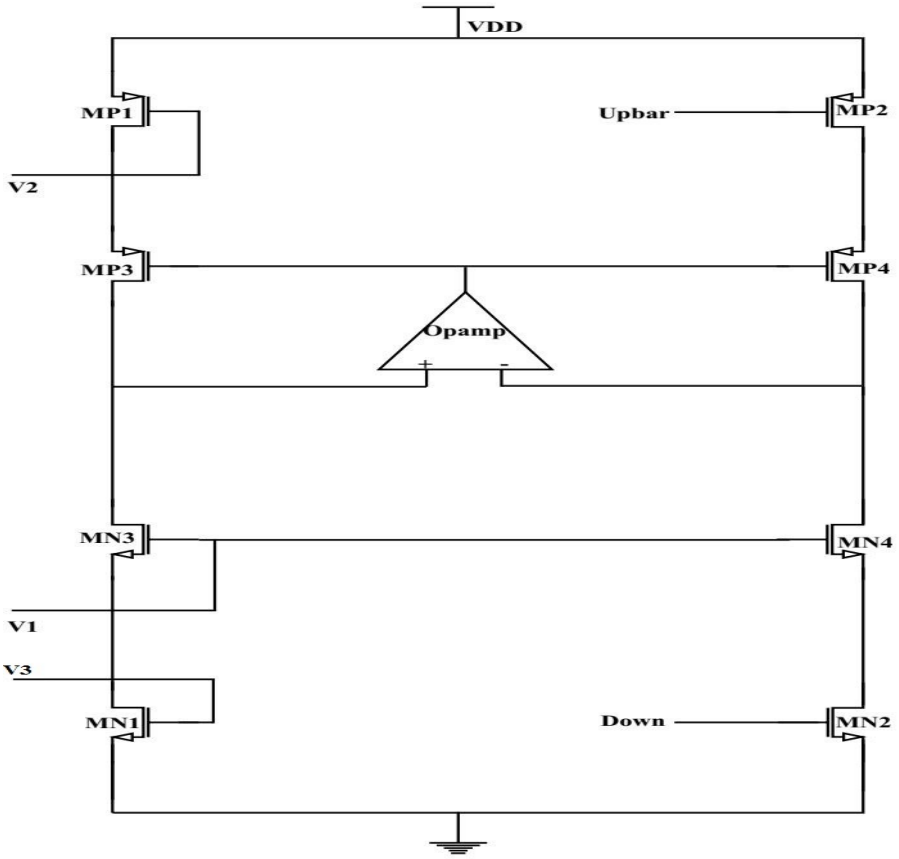

Fig 5.2.8 Schematic of charge pump

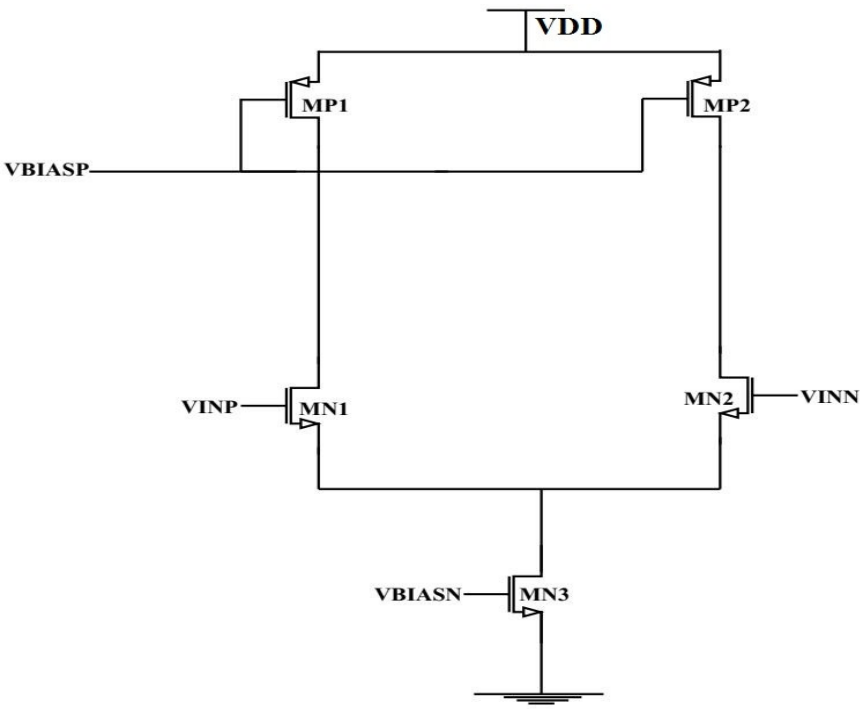

Fig 5.2.9 Schematic of differential CML Inverter

A loop controller is designed to bias the PMOS transistors in triode region which are used as resistors in differential inverters. The loop controller controls replica biasing circuit which increases the speed of operation of differential ring oscillator. The block diagram of the VCO [136], [137] is shown in Fig. 5.2.10. The frequency of voltage controlled oscillator is controlled by varying the tail current source.

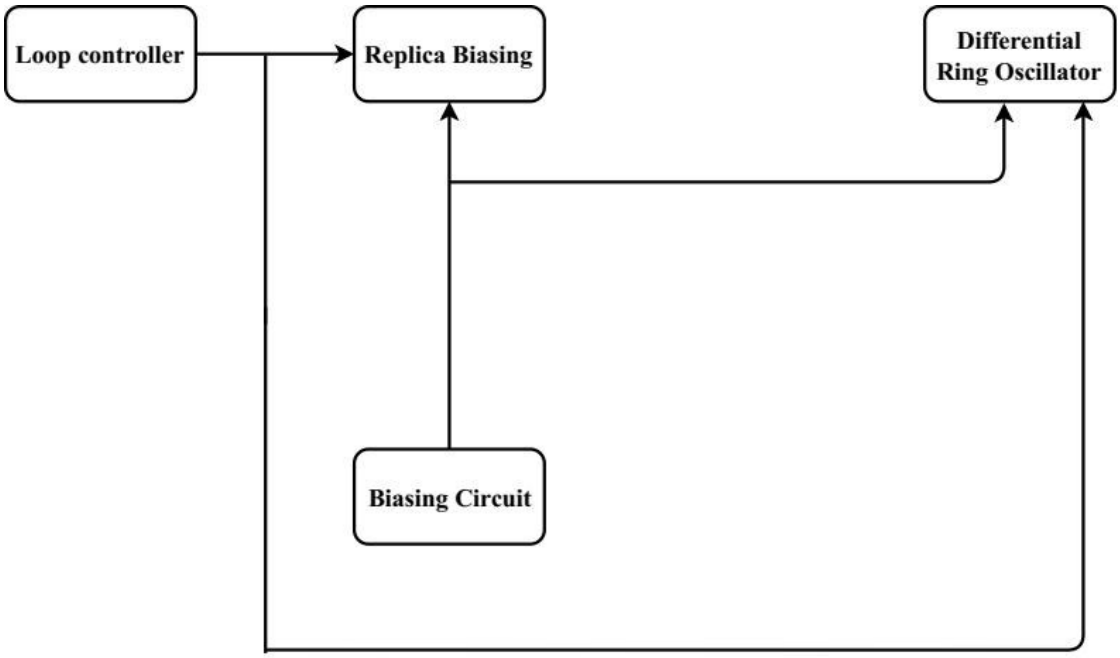

Fig 5.2.10 Block diagram of the voltage controlled oscillator

The voltage controlled oscillator has gain of 10GHz/V as shown in Fig. 5.2.11

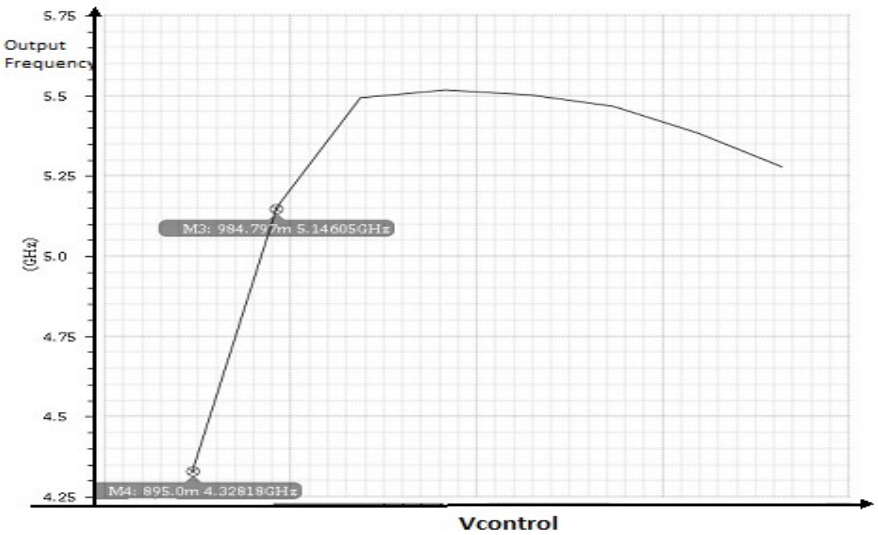

Fig 5.2.11 Gain curve of Voltage Controlled Oscillator

The phase noise of differential PLL is -114dBC/Hz as shown in Fig.5.2.12.

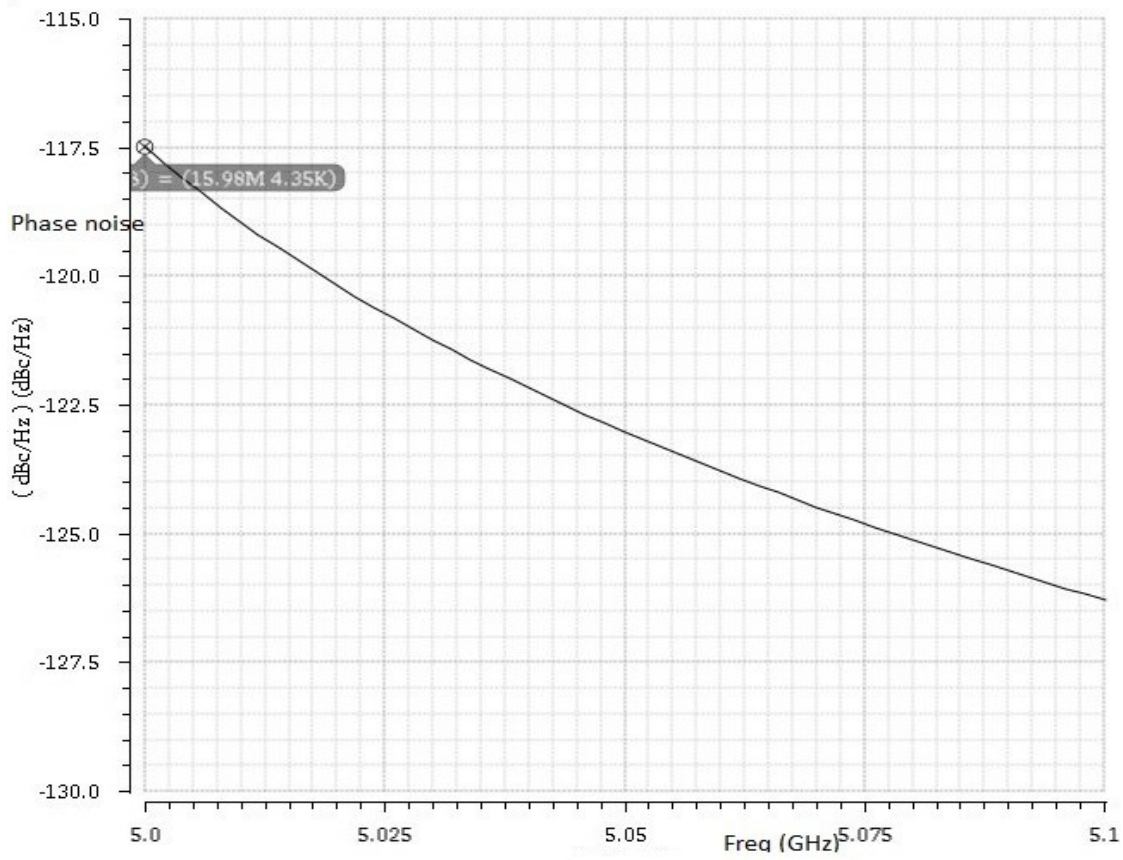

Fig 5.2.12 Phase noise plot of Phase locked loop

A miller compensated operational transconductance amplifier is employed as loop controller. CML logic is used for the design of inverter as the swing is less compared to static CMOS logic which translates to higher speed compared to CMOS logic implementation. The current is steered in one branch of the differential pair. The main advantage of differential configuration is common mode noise rejection. Replica biasing is used to bias each CML differential inverter configuration. The loop controller controls the replica circuit which has the same design parameters as the CML differential inverter. Each CML differential inverter pair has a gain of √2 which is required for sustained oscillations [130]. The differential voltage swing should be less than 800mV as per 10 BASE KR channel specifications. $V_{overdrive}$ of signal transistors is equal to $V_{swing}/\sqrt{(2)}$ which fixes the size of signal transistors while keeping a cap on power dissipation. As per UMC 0.180nm the delay for single inverter is 27ps. If differential signaling is used the delay is 54pS. If 8 such stages are cascaded then the delay is 0.216ns, so the frequency is 4.6 GHz. As the data rate is 10.3Gbps, 8 stage CML

differential inverters can realize voltage controlled oscillator which serves as clock for half rate PD. Here the resistances are implemented using PMOS transistors. The performance summary and comparisons with the previous works are presented in Table 5.2.1.

The frequency of operation of differential ring oscillator is given by equation 5.2.3[140].

$$f = \left(\frac{-I_{SS}}{2NV_{SW}\left(c_{in}+c_{pr}\right)} \right) \left[1 - \left(\frac{I_{ss}R_g}{V_{sw}} \right) \left[\left(\frac{c_{pr}}{c_{in}+c_{pr}} \right) \left[2 - N\left(\frac{1}{N} - \frac{1}{\pi} \right) \right] \right] + \frac{2\sqrt{2}I_{ss}}{\pi} \right] \quad (5.2.3)$$

The effect of process corners on the gain characteristics of VCO is shown in Fig.5.2.13. The variation in the frequency of a VCO is due to variation in process parameters of MOSFET.

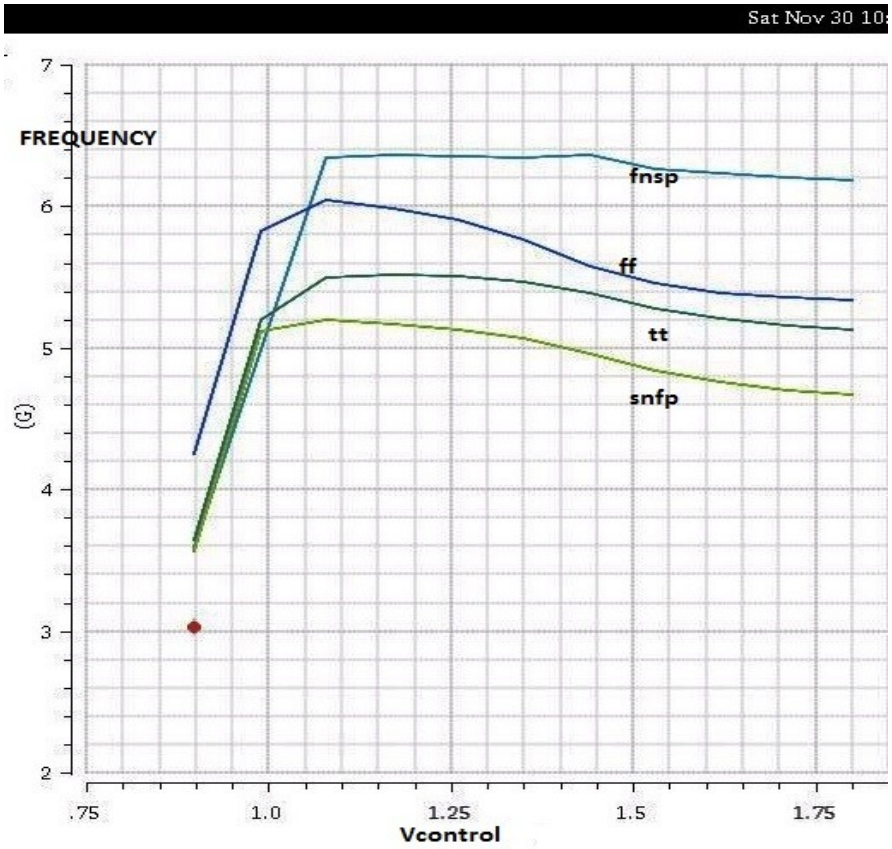

Fig 5.2.13 Effect of process corners on phase noise of Voltage Controlled Oscillator

In slow PMOS, slow NMOS corner, since the load resistor is implemented by PMOS biased in triode region of operation, the resistance of PMOS increases, and effective transconductance of MOSFET decreases which in turn leads to reduction of gain needed for sustaining oscillations.

The frequency of oscillator is influenced by gate resistance as can be seen from equation 5.2.3. It is assumed that no current in drawn by the MOSFET. To overcome the effect of

short channel MOSFETs, if the long channel MOSFETs are used, the effect of parasitic capacitance becomes the limiting factor. The results demonstrate that the designed CDR circuit exhibits lower jitter of 4.92ps. However artifacts due to process variations are insignificant as they are beyond the tuning range.

TABLE 5.2.1 Performance comparison of Various CDR topologies

	[139]	[140]	[141]	[142]	[143]	[135] *	This work
Process	0.18µm CMOS	0.18µm CMOS	0.13µm CMOS	65nm CMOS	65 nm CMOS	0.13µm CMOS	0.18um CMOS
Supply	1.8V	1.8V	1.2V	N.A	1.2V	1.2V	1.8V
Data rate	5 Gb/s	5 Gb/s	10 Gb/s	0.65-8 Gb/s	5 Gb/s	5.4 Gb/s	10 Gb/s
Power consumption	230 mW	144 mW	120 mW	88.6mW	178.4 mW	138 mW	27 mW
Recovered clock jitter	6.04 ps(rms)	6.8 ps(rms)	2.1 ps(rms)	9.7 ps(rms)	N.A	5.98 ps(rms)	4.92 ps(rms)

* Complete receiver with buffer, equalizer, and tuned LC VCO and mux logic included.

5.2.5 Conclusion

A 10.3-Gb/s clock and data recovery circuit is designed using dual loop architecture for FR4 backplane applications. Dual loop architecture and bang-bang phase detector are modified to meet the functionality requirements. The output recovered clock from simulations shows a total phase jitter of 0.14ps meeting the backplane specifications of 0.15UI between the frequencies 5GHz to 5.15GHz. The results also show a period jitter of 1.52 ps and cycle to cycle jitter of 2.63ps. This shows from the above results that designed CDR circuitry is suitable from high speed serial data transfer across backplane channels.

Chapter 6

Conclusion and Future Scope

High-speed serial links play a vital role in both inter-chip and intra-chip communication. Statistical analysis was performed to model the backplane channel. On-die termination besides the pre-emphasis with lower power consumption is designed suitably. The constraints of minimum bit error rate and jitter specifications are met with dual loop clock and data recovery circuitry. Identifying the fact that comparators play a major role in sensitivity of receiver, a low input referred noise dynamic comparator is proposed with lower kick-back noise.

6.1 Major Findings

To address signal integrity design challenges, the first contribution presents a feed-forward transmit equalizer that uses current-mode signaling along with a cross coupled technique to implement the on-die termination to improve power efficiency. A two-tap circuit is designed and simulated which achieves an overall efficiency of 0.603pJ/b working at data-rate of 10Gb/s with 300mV differential output signal amplitude.

An attempt is made to design of low input referred noise dynamic comparator suitable for high-speed serial I/O. The designed circuit employs gain boosting technique to reduce the kick-back noise which in-turn reduces the input referred noise of the comparator. The designed dual-tail dynamic comparator has a $61.13\mu V$ as input referred noise and $29\mu V$ as kick back noise with an input sensitivity of 5mV.

Another contribution is design of low phase noise dual-loop clock and data recovery circuit. Phase noise forms an important aspect of design of CDR. The phase-frequency detector is modified to reduce the dead-zone effect thereby improving the phase-noise. The circuit is designed for a data-rate of 10Gb/s in 180nm CMOS technology. It achieves a phase noise of

-82dBc/Hz at 1MHz offset from center frequency.

A phase locked loop is designed to improve jitter performance for a center frequency of 10GHz in 180nm CMOS technology. The designed Phase locked loop has a phase noise of

-114dBC/Hz.

6.2 Future Work

Some viable options to extend the work include but not limited to:

1. As data transfer rates across backplanes shall increase exponentially, other multi-level signaling schemes can be employed.
2. As process, voltage and temperature variations affect the analog circuitry compared to the digital counter parts, major signal processing circuitry can be pushed to digital domain.

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List of Publications

International Journals

1. D Pavan Kumar Sharma, P Sreehari Rao, "0.6pJ/bit ODT using CML in 130nm CMOS for 10Gb/s Backplane Channel" Accepted for publication Journal of Advanced Research in Dynamical and Control Systems (JARDCS) in Oct 2018. (Scopus Indexed).
2. D Pavan Kumar Sharma, P Sreehari Rao,"A low input referred noise dynamic comparator for High speed applications" Accepted for publication Modeling, measurement and control A Journal. (Scopus Indexed).
3. D Pavan Kumar Sharma, P Sreehari Rao ,"A Low Jitter Phase Locked Loop for High speed serial Interfaces" in International Journal of Computer applications, 2014.

International Conferences

1. D Pavan Kumar Sharma, P Sreehari Rao, "A 10-G bits/s Clock and Data-Recovery Circuit for Backplane Applications Using Dual Loop Architecture" in IEEE International Conference in VLSI and signal processing (ICVSP) 2014.

2. D Pavan Kumar Sharma, P Sreehari Rao, "A low jitter Phase locked loop for High Speed Serial Interfaces" at CCSN organized by International Association of Science, Technology and Management, Kolkata, 2014.

3. D Pavan Kumar Sharma, P Sreehari Rao, "Power optimized Phase locked loop" at IEEE VDAT, Coimbatore 2014.
4. D Pavan Kumar Sharma, P Sreehari Rao,"A Low Phase Noise 10-G bits/s Clock and Data-Recovery Circuit with modified D- Latch for Backplane Applications Using Dual Loop Architecture" IEEE International Conference on Advances in Electronics, Computers and Communication, 2014.