

Development of Soft-switched LED Drivers for Off-grid Lighting Applications

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Submitted in partial fulfillment of the requirements
for the award of the degree of

**Doctor of Philosophy
in
Electrical Engineering**

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Dedicated to
My beloved Parents and family
Shri Veeramallu Venkata Krishna Rao & Smt. Veeramallu Nagamani

APPROVAL SHEET

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CERTIFICATE

This is to certify that the thesis titled “**Development of Soft-switched LED Drivers for Off-grid Lighting Applications**”, submitted by **Mr. Venkata Kondala Satyakar Veeramallu** (Roll No. 716119), is a bonafide work submitted to National Institute of Technology Warangal in partial fulfilment of the requirements for the award of the degree of **Doctor of Philosophy** in Electrical Engineering. To the best of my knowledge, the work incorporated in this thesis has not been submitted elsewhere for the award of any degree.

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DECLARATION

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Venkata Kondala Satyakar Veeramallu

ABSTRACT

The development of renewable energy resources and energy efficiency are the two main strategies that can be implemented to meet the current challenges of increased energy demand and sustainable development. Nowadays, solar photovoltaic (SPV) systems are playing a vital role in energy utilization due to their various advantages. Also, electrical vehicles in automobiles are being encouraged by many countries due to the advanced technologies developed in battery storage systems (BSSs). Energy efficiency in lighting application can reduce energy consumption and hence, decreases the energy demand. Thus, the present modernization in the lighting system is the replacement of traditional lighting technology with Light Emitting Diodes (LED) in commercial, domestic and industrial installations due to its vast advantages. Hence, in this thesis, three different LED driver configurations are proposed for applications of off-grid LED lighting system (LS) such as SPV fed LED street lighting system (LED-SLS), SPV/battery fed high gain multiple load LED-LS, Battery fed automotive LED-LS.

The first work implements a novel soft-switched buck-boost bi-directional dc-dc converter, for single-stage SPV fed LED-SLS. A coupled inductor (CI) based auxiliary circuit is used in the proposed bi-directional dc-dc converter (BDC) to achieve soft switching, which leads to improved efficiency with reduced ripple. As SPV power is available during daytime alone, a BSS is also used. The BSS is charged from SPV during day time through the proposed CI-BDC. The BSS powers the LED-SLS during nighttime through the same CI-BDC. Pulse width modulation is used for voltage regulation. The proposed CI-BDC provides various advantages like: buck/boost operation in either direction of power flow, ZVS soft-switching, use of single magnetic core, high efficiency, reduced ripple in output current and simple control. Also, it provides an illumination control of the LED-SLS using PWM dimming. To maintain high efficiency even at light loads, the proposed CI-BDC works as conventional BDC by turning OFF the auxiliary circuit. Thus, avoiding the high conduction losses in it at light loads. The detailed working principle and design analysis are presented along with simulation results. A prototype of 40 W LED lighting system has been developed and experimental validation is presented.

SPV or battery fed multiple load LED lighting applications are gaining importance these days, which require independent voltage regulation and dimming control. Half-bridge reso-

nant converters are mostly used due to their simple structure. Therefore, in the second work, a buck-boost integrated high gain non-isolated symmetrical half-bridge series resonant converter is proposed for multiple load LED lighting applications. With the aid of integrated buck-boost operation, the output voltage can be regulated below and above the nominal input voltage effectively and can produce twice the gain as compared to classical half-bridge converters. Frequency modulation is implemented for output voltage regulation. PWM dimming has been adopted for illumination control. The proposed driver results in several advantages such as low cost, compact size, high gain, improved efficiency due to soft-switching, simple control, independent dimming and effective operation for multiple loads. Thus, the proposed non-isolated driver configuration is well suited for SPV/Battery fed multiple load LED lighting applications. The proposed configuration is tested with a single LED load of 22 W, 22.505 V and dual-LED loads of 22 W, 22.505 V & 43 W, 39.612 V. There is an excellent consensus between the simulation and the experimental outcomes.

The battery voltage varies widely especially during transients, in automobile applications. Hence, in the third work, a reconfigurable non-isolated buck-boost (BB) integrated full-bridge series resonant converter (FBSRC) based LED driver is proposed for wide input voltage automotive lighting applications. The proposed LED driver is derived by the integration of BB operation with FBSRC. It can be reconfigured into three different resonant converter topologies such as BB integrated FBSRC, BB integrated half-bridge series resonant converter (BB-HBSRC) and conventional HBSRC and hence, it produces 3 levels of voltage gains. By transformation from one topology to other based on the input voltage range and with asymmetric pulse width modulation (APWM) control, it can operate for a wide input voltage range while maintaining soft switching. The main advantages of the proposed configuration are smooth transformation into 3 different topologies without any additional switching devices, no topological transitions within a switching cycle in steady state, use of simple PI controller, soft switching and wider voltage gain with buck/boost operation. In addition, dimming control is also achieved using PWM technique. A detailed theoretical analysis of the proposed converter is presented. To verify the analysis and performance, a prototype of 22.7 W, 22.5 V LED driver is designed, simulated and tested for a wide input voltage range of 18 V to 120 V. The simulation and experimental results are in good agreement with each other.

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Abbreviations & Symbols

List of Abbreviations

AC	Alternating Current
ADC	Asymmetrical Duty Cycle
AJAY	Atal Jyoti Yojana
BB-FBSRC	BB integrated FBSRC
BB-HBSRC	BB integrated HBSRC
BBI	Buck-Boost Integrated
BB	Buck-Boost
BDC	Bi-directional DC-DC Converter
BSS	Battery Storage System
CCM	Continuous Conduction Mode
CI-BDC	CI based BDC
CI	Coupled Inductor
CRM	Critical Conduction Mode
C	Capacitor
DCM	Discontinuous Conduction Mode
DC	Direct Current
DDUGJY	Deen Dayal Upadhyaya Gram Jyoti Yojana
DSP	Digital Signal Processor

DST	Department of Science & Technology
D	Duty Ratio or Duty Cycle
EMI	Electromagnetic Interface
EV	Electric Vehicle
FAME	Faster Adoption and Manufacturing of (Hybrid &) Electric Vehicles
FBSRC	Full-bridge Series Resonant Converter
FB	Full-bridge
GoI	Government of India
HBSRC	Half-bridge Series Resonant Converter
HB	Half-bridge
HEV	Hybrid Electric Vehicle
HID	High intensity Discharge
HS	Hard Switching
IEA	International Energy Agency
LED	Light Emitting Diode
LLC-RC	LLC Resonant Converter
LS	Lighting System
L	Inductor
ML	Multiple Load
MPPT	Maximum Power Point Tracking
NEMMP	National Electric Mobility Mission Plan
PFM	Pulse-Frequency Modulation
PS	Phase Shift

PWM	Pulse Width Modulation
QSW	Quasi Square Wave
Q	Quality Factor
SDG	Sustainable Development Goal
SEED	Science for Equity, Empowerment and Development
SLNP	Street Lighting National Programme
SLS	Street Lighting System
SMPC	Switched Mode Power Converter
SPV	Solar Photovoltaic
SRC	Series Resonant Converter
SS	Soft Switching
T	Time period
UJALA	Unnati Jyoti by Affordable LEDs for All
ZVRT	Zero Voltage Resonance Transition
ZVS	Zero Voltage Switching

List of Symbols

k_i	Ripple coefficient of i_{L1}
C	Capacitor value
D	MOSFET body diode
D_a	Auxiliary diode
D_R	Rectifier diode
G	Voltage gain
I	Current

i	Current
I_{LED}	LED current
k	Coupling factor of CI
L	Inductor value
M	Mutual inductance
m	Slope of current
max	Maximum
R_{LED}	LED internal resistance
S	MOSFET switch
S_a	Auxiliary MOSFET switch
t	Time instant
t_d	Dead time
T_m	Time interval in particular mode
v	Voltage
V_{BAT}	Battery voltage
V_{LED}	LED voltage
V_{PV}	SPV voltage
V_{th}	LED threshold or cut-in voltage
Δi_L	Change of inductor current
Δi_{LBB}	Change of BB inductor current
δ_d	Duty cycle of dimming signal
Δ_1	Time duration
ω_r	Angular resonant frequency

ϕ	Phase angle
\bar{v}_{A1-A2}	Resonant tank input RMS voltage in R-BBI-FBSRC
\bar{v}_{A1-O}	Resonant tank input RMS voltage in BBI-HBSRC-ML
\bar{v}_{A2-O}	Resonant tank output RMS voltage in BBI-HBSRC-ML
\bar{v}_{A3-A2}	Resonant tank output RMS voltage in R-BBI-FBSRC
C_{BB}	Buck-Boost capacitor
C_{oss}	MOSFET output capacitance
C_r	Resonant capacitor
f_r	Resonant frequency
f_{sw}	Switching frequency
f_s	Switching frequency
$I_{Da_RMS_SS}$	Auxiliary diode AC or RMS current under SS
$I_{L1_Avg_HS}$	Inductor DC or average current under HS
$I_{L1_Avg_SS}$	Main inductor DC or average current under SS
$I_{L1_RMS_HS}$	Inductor AC or RMS current under HS
$I_{L1_RMS_SS}$	Main inductor AC or RMS current under SS
$I_{L2_RMS_SS}$	Auxiliary inductor AC or RMS current under SS
I_{LBB_AC}	RMS value of BB inductor current
I_{LBB_DC}	Average value of BB inductor current
i_{LBB}	Buck-Boost inductor current
i_{Lr}	Resonant current
$I_{Sa_RMS_SS}$	Auxiliary switch AC or RMS current under SS
$I_{sw_Avg_HS}$	DC or average current under HS

$I_{sw_Avg_SS}$	DC or average current under SS
$I_{sw_RMS_HS}$	AC or RMS current under HS
$I_{sw_RMS_SS}$	AC or RMS current under SS
L_{BBcrit}	Critical inductance
L_{BBcr}	Critical value of BB inductor
L_{BB}	Buck-Boost inductor
L_r	Resonant inductor
P	Power
P_{Da_SS}	AC conduction losses in auxiliary diode under SS
P_{L1AC_HS}	AC conduction losses in inductor under HS
P_{L1AC_SS}	AC conduction losses in main inductor under SS
P_{L1DC_HS}	DC conduction losses in inductor under HS
P_{L1DC_SS}	DC conduction losses in main inductor under SS
P_{L2AC_SS}	AC conduction losses in auxiliary inductor under SS
P_O	Output power
P_{Sa_SS}	AC conduction losses in auxiliary switch under SS
P_{swAC_HS}	AC conduction loss under HS
P_{swAC_SS}	AC conduction loss under SS
P_{swCa_HS}	Output capacitance loss under HS
P_{swCa_SS}	Output capacitance loss under SS
P_{swDC_HS}	DC conduction loss under HS
P_{swDC_SS}	DC conduction loss under SS
P_{swRR_HS}	Reverse recovery loss under HS

P_{swSW_HS}	Switching loss under SS
Q_{rr}	Diode reverse recovery charge
R	Resistance
R_{ac}	Non-linear output resistance offered by rectifier
R_{DSon}	MOSFET resistance across Drain and Source when it is ON
r_{DS}	MOSFET resistance across Drain and Source when it is ON
S_D	Dimming switch
T_d	Time period of dimming signal
t_{fall}	Fall time of MOSFET
t_{rise}	Rise time of MOSFET
V_{BB}	Buck-Boost output voltage
V_{DC}	Battery/DC Voltage
V_{FB}	Input voltage to resonant inverter in R-BBI-FBSRC
V_{fd}	Diode forward voltage
V_g	Gate voltage
V_{in}	Input voltage to resonant inverter in BBI-HBSRC-ML
V_O	Output voltage
v_s	Drain to Source voltage
X_{Cr}	Resonant capacitor reactance
X_{Lr}	Resonant inductor reactance
Z_{in}	Input impedance

Chapter 1

Introduction

Chapter 1

Introduction

1.1 General Overview

India is 2nd in population and 5th in electricity consumption, thus faces a wide gap in demand and supply of electrical energy. The two main strategies that are being implemented in India to meet the current challenges of increased energy demand and sustainable development are

- Development of renewable energy sources and
- Improvement of energy efficiency

Energy generation through renewable energy sources are encouraged in India, as the fossil fuels produce greenhouse gases (GHG) like CO_2 that have far-ranging environmental and health effects. Renewable energy contributed nearly 24% of the total power generation in India from last decade. The GoI set a renewable capacity goal of 175 GW by 2022, targeting 100 GW from solar photo-voltaic (SPV) system.

Energy efficiency is achieved, when energy in a specific product or process is reduced without affecting the useful output. Energy efficiency will also contribute to energy conservation. The various benefits that can be obtained with energy efficiency in industrial sector are reduction in energy bills, increase in production and profits. Nationwide, the benefits can be less importing of energy from outside countries, the saved amount can be utilized to overcome the poverty, etc. Globally, the benefits include reduction in GHG, thus maintaining a sustainable environment.

1.1.1 Energy Efficiency Using LED Lighting

Lighting sector accounts for about 20% of the total electricity consumption in India [1]. Light emitting diodes (LEDs) provide better light output than conventional lights and are 88% energy efficient as compared to incandescent bulbs and 50% energy efficient as compared to

conventional florescent Lamps (CFLs). It has been estimated that the use of LEDs in domestic and public lighting could result in up to 50% reduction in energy consumption.

GoI has taken significant steps to improve energy efficiency, reducing 15% of annual energy demand and 300 million tonnes of CO_2 emissions over the period 2000-18, according to International Energy Agency (IEA) analysis. As part of this process, GoI has facilitated wide scale implementation of LED lighting. Even though LED is costlier, bulk purchasing programmes made it affordable. The price of LEDs is reduced drastically through The Unnati Jyoti by Affordable LEDs for ALL (UJALA) programme and also created local manufacturing jobs to meet the demand for energy-efficient lighting [2]. Further, under the Street Lighting National Programme (SLNP), over 2.1 million conventional streetlights are being replaced with LED streetlights all over the country. This has resulted in annual energy savings of 295 million kWh, avoided the generation capacity of over 73 MW and reduced carbon emissions by 230,000 million tonnes annually [3].

1.1.2 Off-Grid LED Lighting Applications

Despite good progress in electrification, there are still around 100 million people in India without electricity access and they rely on fuel-based light sources [2]. Energy-efficient, off-grid lighting solutions offer the most promising and scalable means to eliminate adverse health outcomes associated with fuel based lighting and even they lower the costs and reduce GHG emissions. The GoI also targets the following points under United Nations Sustainable Development Goals (SDG) 7:

- Ensure clean, secure energy and full reliable access to electricity (with solar PV or batteries, notably in rural areas) (SDG 7.1)
- Increase the share of renewable energy consumption in the global energy mix (SDG 7.2)
- Double the rate of energy efficiency improvements (SDG 7.3).

Hence, there is a requirement of research on off-grid lighting systems like SPV/Battery fed LED lighting applications and this thesis mainly focused on the following three specific applications.

- SPV fed LED-SLS
- SPV/battery fed high gain multiple load LED-LS
- Battery fed automotive LED-LS

1.2 Introduction Of LED Lighting System

LEDs are versatile products that can be used for residential lighting, street lighting, downlights, landscaping, monument lighting, signage, traffic signals, security lights, industrial lighting, office space lighting, automotive lighting and much more [3]. The limitations of conventional lighting sources, main advantages of LEDs, its representation and electrical model of an LED are discussed further.

1.2.1 Limitations of Conventional Lighting Sources

The incandescent, fluorescent and high intensity discharge (HID) lamps are used conventionally for decades. The advantages and their limitations are illustrated as below [4]:

- **Incandescent lamps:** These are low cost, however, only 10% of electrical energy is converted into light and remaining energy is wasted as heat. Also, these have a short lifespan (1000-1500 hrs) and low efficacy (8-17 lm/W).
- **Fluorescent lamps:** Have Long life (6000-15000 hrs), high luminous efficacy (50-70 lm/W) and less heat, but harmful to environment and human health. Also, frequent switching can shorten their life.
- **HID Lamps:** Have high luminous efficacy (45-55 lm/W) and long life (20,000 hrs), but harmful to environment and human health. It takes several minutes to reach them to full brightness.

However, due to the following advantages, the conventional lighting sources are replaced with LEDs.

1.2.2 Advantages of LED

- **Long Life:** LED bulbs have an outstanding operational lifetime of over 50,000 hrs.
- **Energy Efficient:** They have estimated energy efficiency of 80%-90% when compared to conventional lighting.
- **Ecologically Friendly:** LED lights are free of toxic gases.
- **Frequent Switching:** Frequent ON and OFF will not affect the lifetime or light emission of LEDs.

- **Operational condition:** LEDs are ideal for operation under very cold and low outdoor temperature.
- **Operating voltage:** Low-voltage power supply is sufficient for LED illumination.
- **Shock Proof:** LEDs are shock proof as they are made of semiconductor devices.

LEDs also have some limitations like high initial cost, requirement of heat sink and LED driver. However, their numerous advantages made them the first choice in industrial, commercial and domestic applications [3].

1.2.3 LED Operation

LED is a semiconductor device that emits light due to electroluminescence (Fig. 1.1). Its fabrication is similar as normal p-n junction diode. When the LED junction is forward biased, the electrons from n-side cross the junction and recombine with holes. This recombination produces photons. If the wavelength of emitted photons is in visible spectrum, the exposed semiconductor area emits light. The light output from LED depends on the amount of forward current through it. LED transforms more than 90% of electrical energy into light energy when it is forward biased. The operation of reverse biased LED is not generally recommended. The materials used in the fabrication of LED determines the emitted light color.

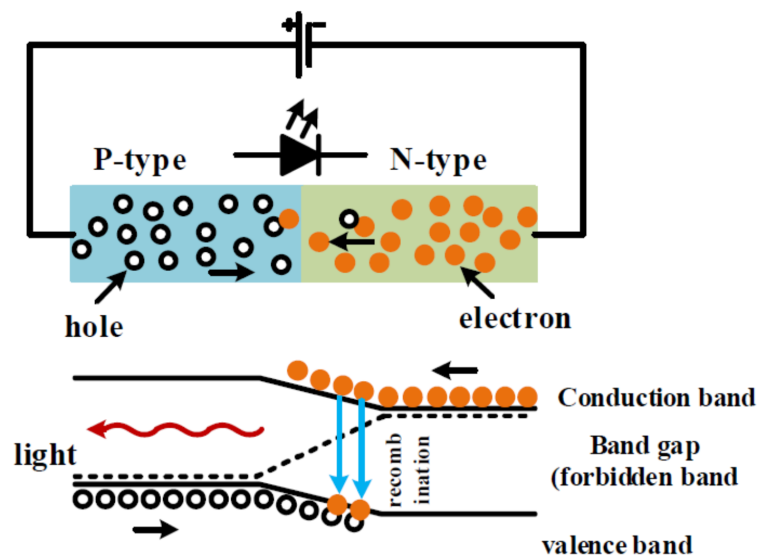


Figure 1.1: Light emission in LED

1.2.4 Equivalent Model and Characteristics of LED

Fig. 1.2a shows the LED symbol and its equivalent circuit, which consists of a series combination of threshold voltage V_{th} , internal resistance of LED, R_{LED} and an ideal diode. As shown in the characteristics of LED in Fig. 1.2b, when the voltage across LED is greater than V_{th} , LED current starts increasing. The standard knee or threshold voltage, V_{th} of an LED is around 2 to 4 V. In practice, to achieve the desired voltage in an LED lamp, the LEDs are connected in series in the form of a string. To achieve desired current rating of the lamp, the LED strings are connected in parallel as shown in Fig. 1.2c.

1.3 LED Drivers

LEDs are powered from DC source. LED lamp can be considered as constant voltage load. The illumination of the LED lamp depends on current. To get a steady illumination from

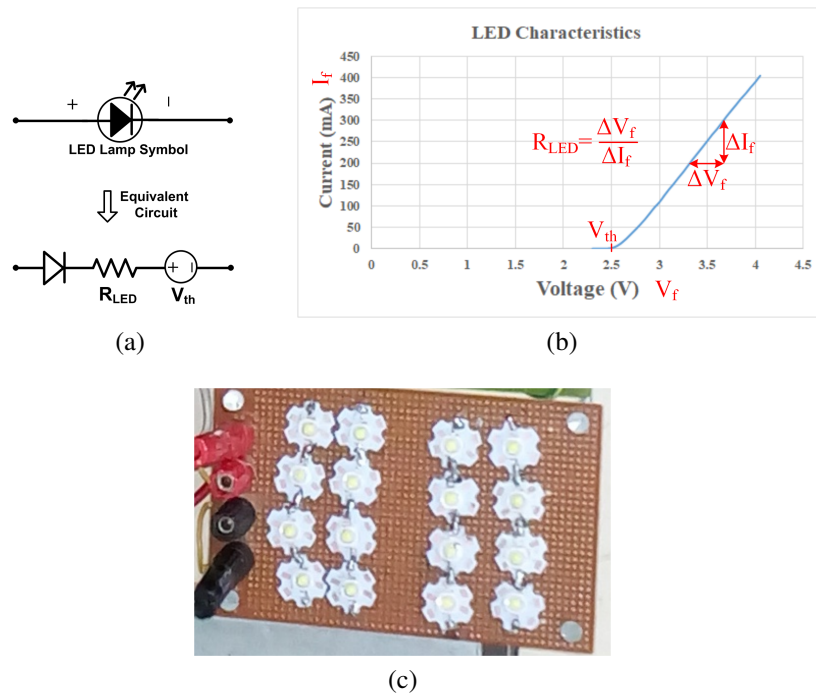


Figure 1.2: (a) LED symbol and its equivalent circuit (b) Characteristics of LED (c) LED lamp used in prototype

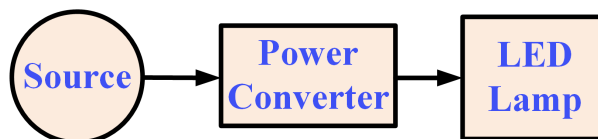


Figure 1.3: Schematic of LED driver

the LED lamp, a constant current is to be supplied, for which an LED driver is essential. LED driver is a converter as shown in Fig. 1.3 that needs to provide desired LED voltage and ripple-free current to the LED lamp irrespective of voltage fluctuations. The performance of the LED lighting system like overall efficiency, reliability, lifetime etc., are mainly dependent on the quality of LED driver used.

Different types of converters, used as LED drivers, are available in the literature. LED drivers can be classified as AC-DC LED drivers and DC-DC LED drivers. For SPV/Battery fed LED lighting applications, DC-DC converters are suitable and are discussed as below.

1.3.1 DC-DC LED Drivers

Passive LED drivers which use resistors are easy to implement. However, their efficiency is low. To overcome this, linear regulators were used as LED drivers [5] in the earlier days. But, their efficiency is affected due to the large power dissipation in the semiconductor device that occurs when the potential difference between the source and LED load is large. Switched Mode Power Converters (SMPC) have become popular as LED drivers [6–8] as they are compact in size, low cost and achieve high efficiency. But the high-frequency operation results in increased switching losses, which demands for soft-switched LED drivers.

LED drivers can also be classified as isolated and non-isolated LED drivers. For low power applications like LEDs, when there is no requirement of isolation, non-isolated LED drivers are the best choice to reduce the cost and size of the driver.

1.3.2 Soft-Switched DC-DC LED Drivers

The size of heat sinks, magnetics and filters determines volume, cost and weight of the SMPC. The low and medium power LED drivers are operated with high switching frequency and hence achieve compact size and reduced cost. However, the high-frequency operation results in increased switching losses as shown in Fig. 1.4 and hence demands for large heat sinks that further increases the size of the driver. In order to overcome this, LED drivers are operated with soft switching i.e., zero voltage switching (ZVS) or zero current switching (ZCS) as shown in Fig. 1.5. The soft switching can be achieved through the following techniques.

(a) Modulation Techniques:

- Using PWM control techniques like phase-shifted ZVS etc., the soft switching can be realized in the PWM converters.

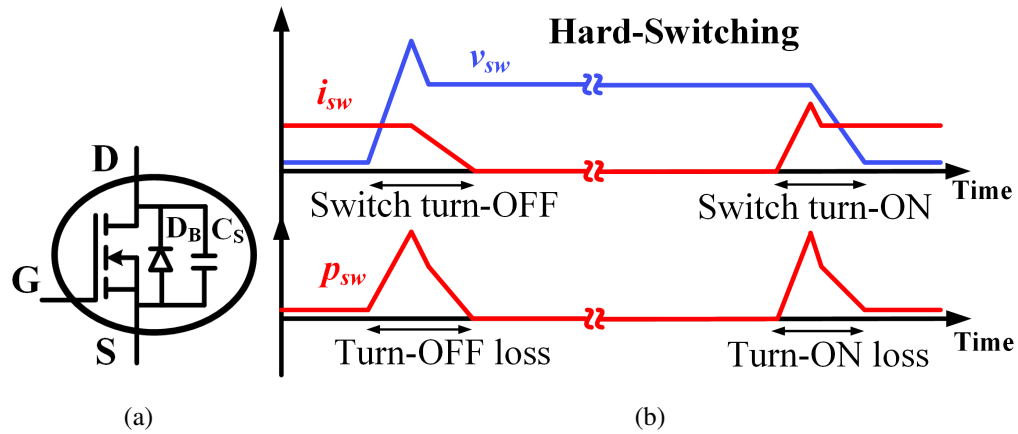


Figure 1.4: Hard-switching (a) MOSFET switch (b) Waveforms across MOSFET under hard-switching

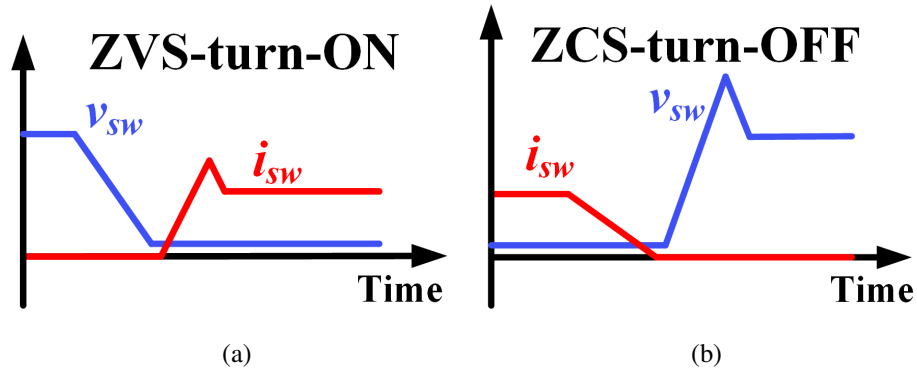


Figure 1.5: Soft-switching (a) ZVS turn-ON (b) ZCS turn-OFF

(b) **Auxiliary transition circuit (Zero current transition (ZCT) and zero voltage transition (ZVT)):**

- With the aid of additional components that include switches, passive components etc. soft switching can be implemented in the converters.

(c) **Resonance circuit (Resonant Converters):**

- By using L and C elements and operating the converter nearer to resonant frequency soft switching can be implemented in the resonant converters.
- The type of resonant converters can be series LC, parallel LC and series-parallel LC type.

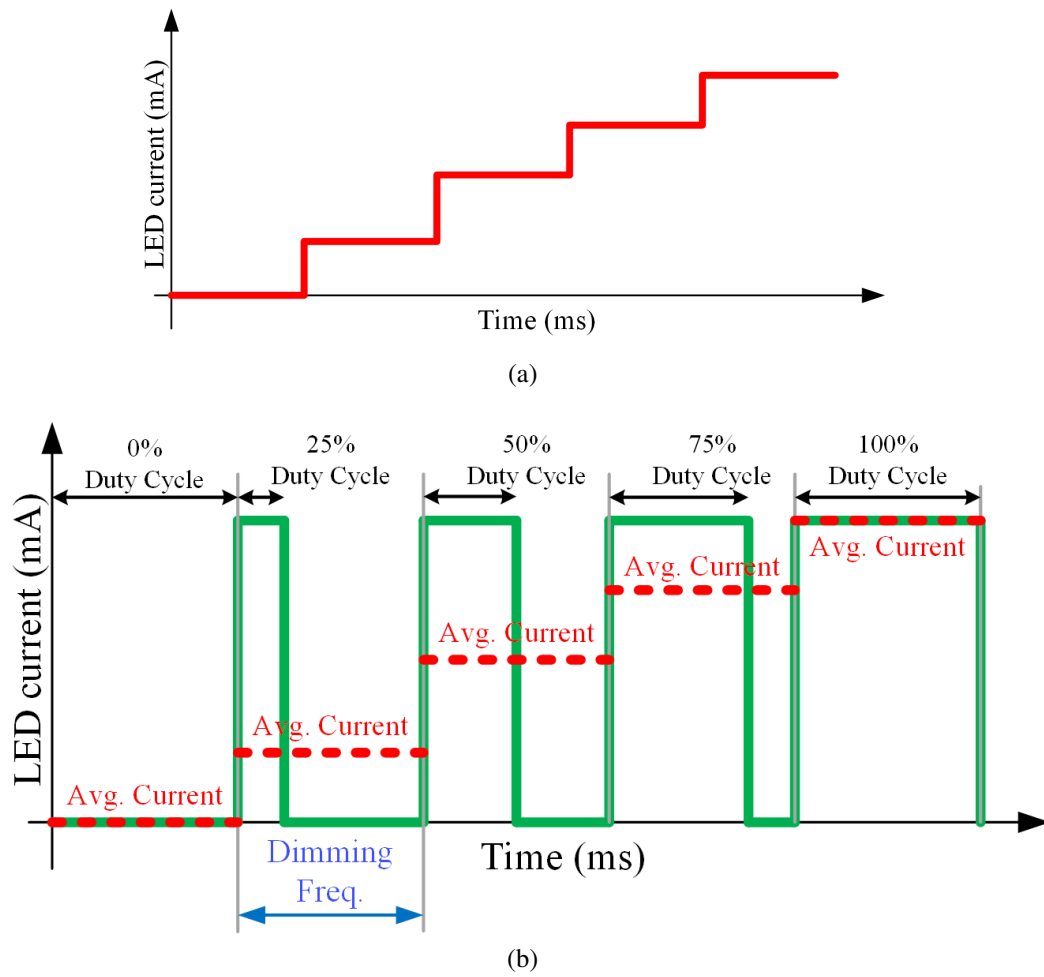


Figure 1.6: Dimming techniques (a) Analog dimming (b) PWM dimming

1.3.3 Dimming Feature

Dimming is the technique used in LED drivers to control the illumination level i.e., the amount of light emitted by LEDs. There are two types of dimming techniques available as shown in Fig. 1.6.

- **Analog Dimming:** In this, the peak current of LED is varied to control the illumination, which affects the operating point of the LED and thus, the color and temperature are affected.
- **PWM Dimming:** In this, the average LED current is varied without affecting the peak value of the current. Thus, the operating point is stable.

Therefore, PWM dimming is adopted in the proposed LED drivers, to control the illumination level.

1.3.4 Salient Features of an LED Driver

The essential features of an ideal LED driver are:

- Ability to supply constant current with reduced ripple to LED lamp
- Compact size, light weight and low cost
- Provide soft-switching and hence achieve high efficiency
- Provide good voltage regulation
- Provide illumination control with better dimming technique

1.4 LED Drivers for SPV/Battery fed LED Lighting Applications

The LED drivers should have the specific features discussed below based on the three main applications of SPV/battery fed LED LS.

1.4.1 LED Driver for SPV fed LED-SLS

SPV system have gained much interest as a less pollutant and a noise-free resource that has the capability to be expanded and utilized in rural areas [9]. Hence, SPV fed LED street lighting system (SLS) has gained importance where the SPV system charges the battery during day hours and the charged battery is used to drive the LED load during night hours. A bidirectional converter can be used for these applications that can charge the battery during day hours operating in one direction of power flow and can discharge the battery during night hours operating in other direction of power flow. Also, the buck/boost operating mode in either direction of power flow is an optimum choice due to the variation of voltage in SPV system and discharging nature of BSS. Hence, the LED driver should have bidirectional power flow capability and operating with buck/boost modes in either directions of power flow for the SPV fed LED-SLS application.

1.4.2 LED Driver for SPV/Battery fed High Gain Multiple Load LED-LS

As the SPV/battery voltage is low in many cases, a high gain driver configuration is required to drive the LED lights. Multiple LED lighting loads find applications in many fields. Thereby, the LED driver should have high gain and ability to drive multiple loads with independent dimming and voltage regulation.

1.4.3 LED Driver for Battery fed Automotive LED-LS

Automobile industry is having a vast growth these days due to the development of Electric vehicles (EVs), hybrid electric vehicles (HEVs), etc. But the battery voltage in the automotive applications may vary widely due to the transients. Thus, the driver configuration should be able to drive the LED lights in automobiles under wide input voltage variations.

1.5 Motivation

Based on the above brief discussion on energy efficiency and off-grid lighting applications and LED lighting system, there is enough scope for further research and the development of

- LED drivers suitable for SPV fed battery assisted LED SLS, that can charge the battery during day using SPV system and the same can discharge the battery to LED lighting load during night hours, operating in buck/boost modes in either directions.
- LED drivers suitable for SPV/battery fed LED lighting applications that can improve the voltage gain with reduced components and can feed multiple loads effectively.
- LED drivers suitable for battery fed automotive LED lighting applications which can operate for wide range of input voltages.

1.6 Contribution

The main contributions of the research work are discussed below:

- [I] A novel soft switched CI-BDC has been proposed for single stage SPV fed BSS assisted LED-SLS which provides ZVS and operates in buck/boost modes in either directions of power flow. In contrast to two-stage converters, the proposed converter provides the following advantages :

- Reduced converter stages and hence reducing the component count
- Buck/boost modes in either direction of power flow
- Reduced device density because of high switching frequency
- Soft switching across all devices including auxiliary circuit devices

Thus, it is well suitable for SPV fed LED-SLS.

[II] A high gain buck-boost integrated symmetrical half-bridge non-isolated LC series resonant converter is proposed for SPV/battery fed multiple load LED lighting applications. When compared with existing similar topologies, it provides the following advantages:

- Reduced device count
- Compact in size
- High gain for all LED loads
- Reduced switching loss due to soft-switching across all devices
- Improved efficiency
- Simple control technique
- Ability to drive multiple loads with equal or unequal voltages/wattages and independent voltage regulation & dimming control

Hence, it is well suitable for SPV/battery fed multiple load LED lighting applications.

[III] A non-isolated reconfigurable BB integrated FB SRC resonant converter based LED driver is proposed for wide input automotive applications. Compared with existing LED drivers, it provides the following benefits:

- Wider voltage gain
- ZVS under wide input variations
- Reduced switching losses
- Easy implementation
- High efficiency under wide input voltages and dimming levels

Therefore, it is well suitable for automotive LED lighting applications with wide input voltage variations.

1.7 Thesis Organization

The thesis has been organized into six chapters.

Chapter 1 briefly introduces the current trend and importance of LED lighting and SPV/Battery sources. It also discusses the motivation points that lead to the literature review on LED drivers for SPV/Battery fed LED lighting applications.

Chapter 2 presents a comprehensive literature review on LED drivers relevant to the proposed research work. Also, the problem identification has been carried out in LED driver configurations for improvised performance which suitable for particular application.

Chapter 3 describes the analysis and implementation of Soft Switched CI-BDC for SPV fed LED-SLS.

Chapter 4 describes the analysis and implementation of a high gain buck-boost integrated symmetrical HB non-isolated LC SRC for SPV/battery fed multiple load LED-LS.

Chapter 5 describes the analysis and implementation of a non-isolated BB integrated FB SRC based LED driver for wide input automotive applications.

Chapter 6 concludes the thesis which highlights the main findings of the research work reported in this thesis and suggests scope for future work.

Chapter 2

Literature Review

Chapter 2

Literature Review

2.1 Introduction

Different types of DC-DC converters are reported in the literature that are suitable for SPV/Battery fed LED lighting applications. A thorough literature review on these converters has been presented in this chapter for the three applications, viz. SPV fed LED-SLS, SPV/battery fed high gain multiple load LED-LS, Battery fed automotive LED-LS and discussed in detail as follows.

2.1.1 SPV fed LED-SLS

SPV fed LED-street lighting applications are gaining wide importance in order to reduce the energy consumption due to conventional lighting sources. Generally, two-stage power conversion is employed for such applications, as shown in Fig. 2.1. One stage is to convert SPV power suitable to charge battery storage system (BSS) while the other stage is to control the power from BSS to the load. Several architectures of a SPV fed LED street lighting systems (SLS) [10–14] are reported in the literature. Flyback and Cuk converters [10], buck converter and active clamp forward converter [11], two similar SEPIC converters [12], integrated sepic-forward converter [13] (Fig. 2.2) and integrated buck/boost & boost circuits [14] are some of the reported topologies for battery charging/discharging applications. However, these topologies suffer from some limitations like: two-stage conversion which leads to more component count, increased losses, hard switching, low efficiency and complex control. Due to bidirectional power capability, bidirectional dc-dc converter (BDC) is well suitable for single-stage charge/discharge applications like in case of a SPV based LED-SLS. Unless there is a requirement of high voltage gain and isolation, a non-isolated BDC is mostly preferred for charge/discharge applications due to its bidirectional power capability, simple structure and control schemes. High efficiency, low cost and good reliability are the key requirements of BDCs. The literature provides several BDCs, which operate either in buck or boost modes. A hard switched BDC based SPV fed LED lighting system is reported [14], which results in

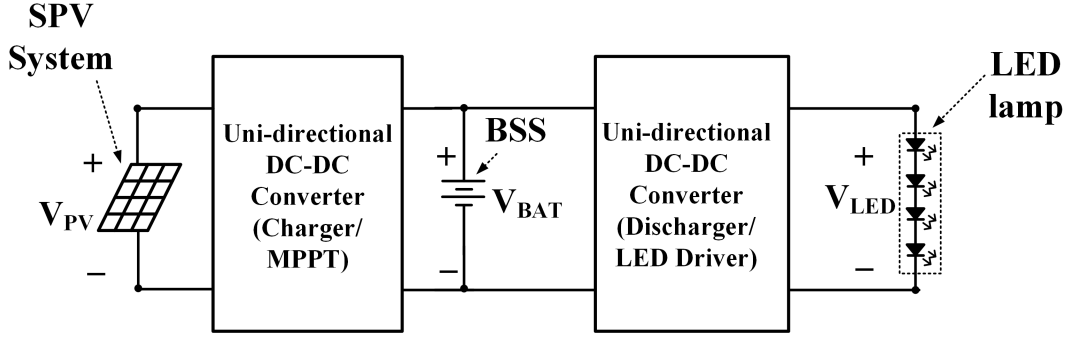


Figure 2.1: Block diagram of two-stage converter for SPV fed LED-SLS

increased switching losses. The coupled inductor (CI) based BDCs are developed to provide a wider range of conversion as well as the reduction in device voltage/current stress [15, 16]. But due to lack of soft switching feature, these converters have low efficiency. Generally, in the SPV and battery-powered applications, the source voltage is of intermittent and time varied in nature such that the input voltage may be higher or lower than the desired output voltage. Hence, the buck/boost mode operation is essential to meet the desired load voltage. Therefore, buck-boost derived BDC is an apt topology for such applications.

In higher switching frequency converters, soft switching techniques are used to improve efficiency and reduce electromagnetic interference (EMI). Several soft switched non-isolated DC-DC converters are reported in literature [17–32]. Active clamp ZVS converters [17–19] are developed to implement soft-switching, but in these converters, DC magnetizing current is large. Auxiliary network is used to achieve soft switching [20], however, it leads to high voltage/current stress across the switches, low efficiency due to hard-switched auxiliary devices and more control complexity. In some papers [21] (Fig. 2.4a), the auxiliary switches operate in ZVS and switching losses are reduced. However, a large circulating current in auxiliary circuit results in high conduction losses. Generally, to achieve ZVS with reduced ripple current, Zero Voltage Resonance Transition (ZVRT) based interleaved technique is used [22–25] (Fig. 2.3).

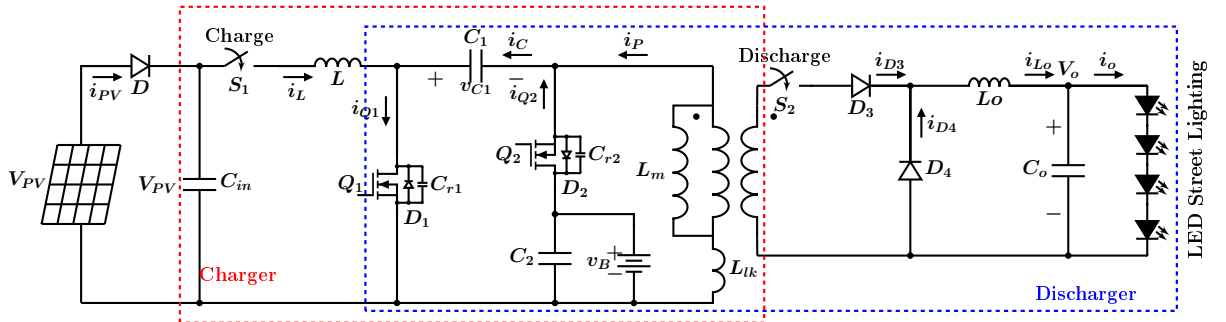


Figure 2.2: Integrated Sepic-Forward converter [13]

But, the component count is more for an increased number of phases and hence control is complex. However, a single auxiliary switch can achieve soft switching in interleaved converters to minimize the component count [26–30], but these topologies result in increased conduction loss due to high peak current. CI-based ZVRT converters are reported in some papers [31,32], which utilize leakage inductance to achieve ZVS. However, ZVS is difficult at light loads [31], due to more recycling energy, that in turn results in reduced efficiency and even they can operate only in either buck or boost in a particular direction but not in both the directions [32] (Fig. 2.4b). Some papers [33,34] (Fig. 2.5), focus on providing soft switching across all the devices in non-inverting bidirectional buck-boost converter [35]. But, the component count and conduction losses are more. They also require a complicated control system. Critical Conduction Mode (CRM) [36–41] is a control technique used to achieve soft switching across the switches by maintaining the current in the inductor operate at the boundary condition, i.e., between continuous conduction mode (CCM) and discontinuous conduction mode (DCM), with frequency variation. This CRM technique can be applied to any converter, to achieve soft switching across the devices without any auxiliary devices. But, it suffers from limitations [39] like the main switch experiences power stress as the power or switching frequency increases, there is a high ripple at input which creates problem especially in high step-up or step-down applications, high peak current flows in the main switch due to the use of small filter inductor that increases the switching and conduction losses. In addition, the discharging loss of parasitic junction capacitor increases as the switching frequency increases. Moreover, as an inductor is to be maintained at boundary condition irrespective of load or input variations, the switching frequency needs to be varied that results in complex closed-loop control and also makes the design complex. To reduce input ripple, many papers used interleaved technique [38,40,41], which increases the component count and also makes the control further complex. In [38], CRM technique is applied for a boost converter. For boost type converters, ZVS is possible only when the input voltage is lower than one half of the output voltage. In order to achieve ZVS in this range, the inductor is operated from CRM mode to Quasi Square Wave (QSW) mode [38], where it is allowed to carry some negative current within limits by using control circuit. Hence the design and control become complex to make the inductor carry the exact negative current required by it for all the loading conditions. This limitation can be overcome by using inverse coupled inductor CRM interleaved technique [41]. However, it will increase the component count. Also, the currents in inductors and main switches in each phase have a high ripple that increases switching and conduction losses.

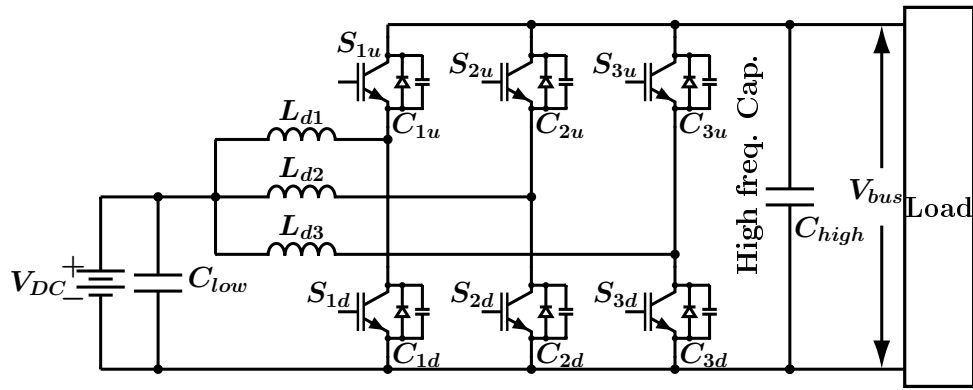
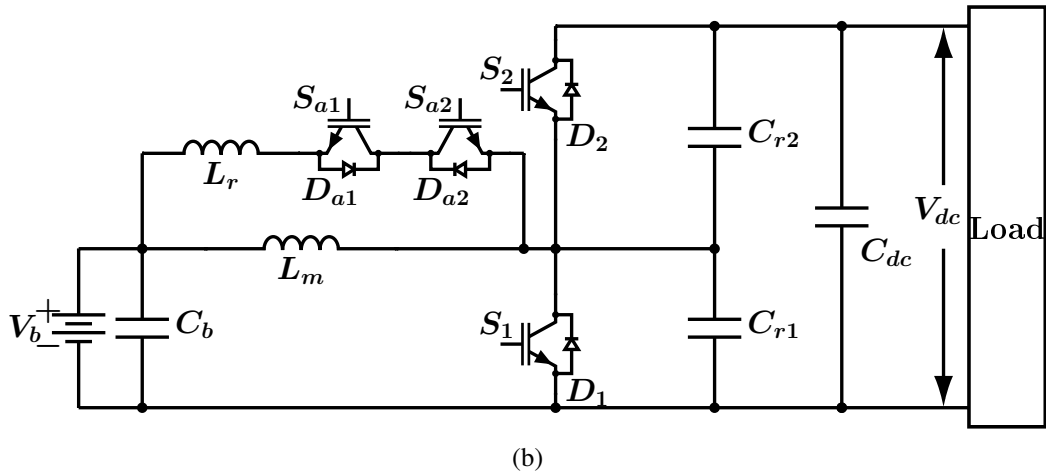
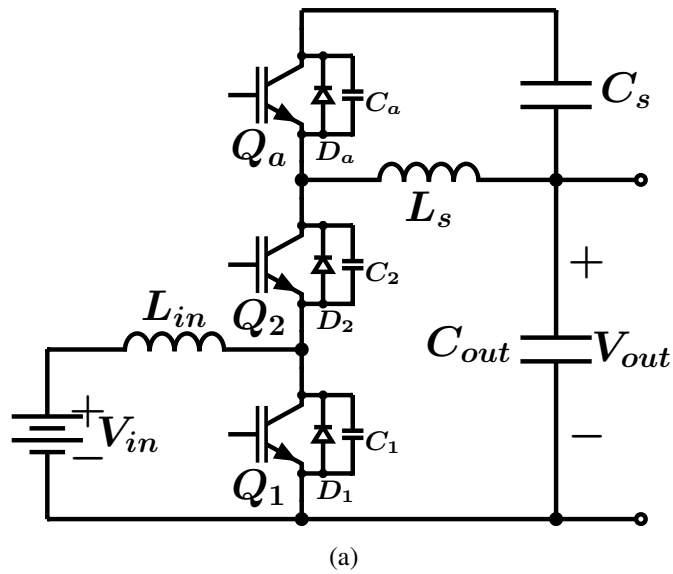


Figure 2.3: ZVRT based interleaved technique in BDC [22]

Figure 2.4: Existing soft-switched BDCs: (a) ZVS PWM converter with active clamping [21]
(b) Auxiliary switch controlled BDC [32]

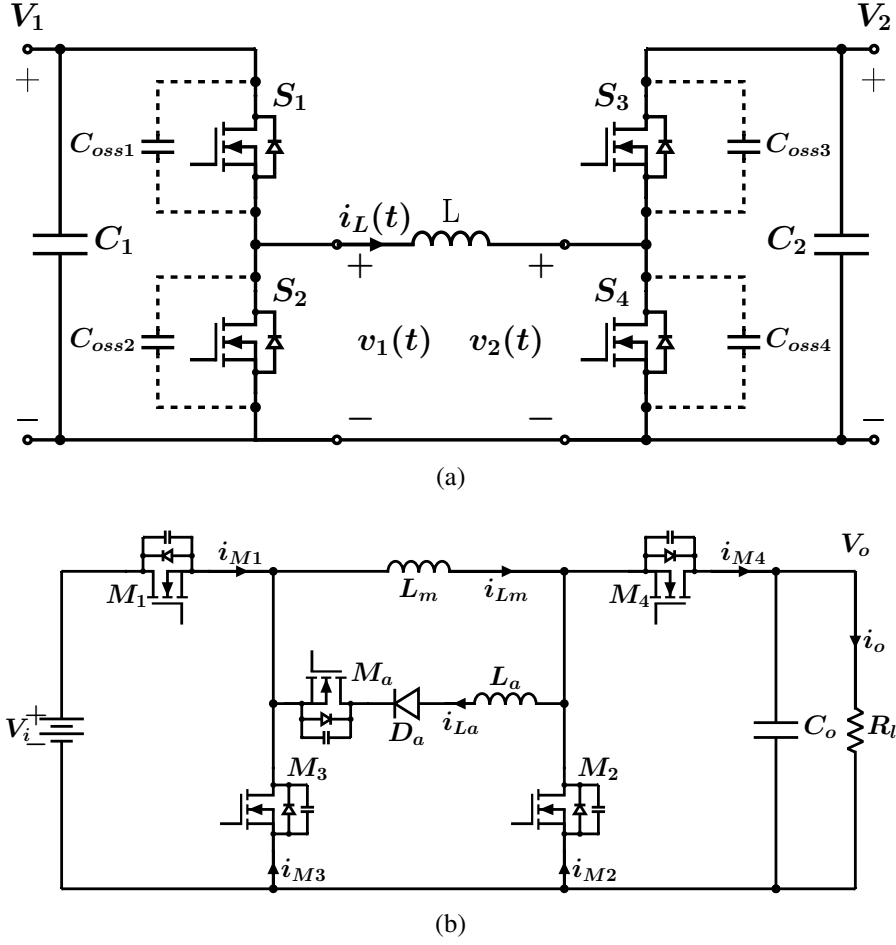


Figure 2.5: Different soft switching techniques in four switched non-inverting buck-boost BDC (a) Modulation strategy based BB-BDC [33] (b) Auxiliary component current sharing ZVT BB-BDC [34]

2.1.2 High Gain SPV/Battery fed Multiple Load LED-LS

The resonant converters are becoming more popular as they provide soft-switching which in-turn results in low EMI noise, high power density etc. Half-bridge and full-bridge based series, parallel & series-parallel resonant converters are widely employed for LED drivers. A multi-string LED driver using full-bridge resonant converter is presented in [42]. A novel current controlled LED driver is proposed in [43] using full-bridge resonant converter, which demands for an additional transformer, switch and three diodes. The input of the full-bridge series resonant converter is regulated using a buck-boost converter in [44], where the power processed in buck-boost converter is low. But it requires an additional input voltage source; the buck-boost converter is hard switched and also device count is high. Several other LED driver configurations [45–50] have adopted half-bridge resonant converter due to its simple structure, easy

implementation, small output filter size [45] and high efficiency due to zero voltage switching (ZVS), etc. Further, these half-bridge resonant converters are integrated with other converters and called as a single-stage AC-DC LED drivers [51–55] that achieve multi-task with reduced component count and improved efficiency.

Generally, SPV/battery fed LED drivers are used for low power LED lighting applications. In [56](Fig. 2.6a), half-bridge inverter with DC blocking capacitor is used as LED driver, where inductance is varied to control the LED illumination. In [57, 58], Buck-boost integrated isolated asymmetrical half-bridge resonant converter is presented, which is suitable for wide input voltage variations. When the power processed is small and isolation is not necessary, non-isolated converters are preferred for easier implementation and low cost. In [48], asymmetrical duty cycle (ADC) controlled half-bridge parallel resonant converter based LED driver is reported. In [49], ADC controlled half-bridge series resonant converter is presented for improved efficiency. In [59], buck-boost cascaded symmetrical half-bridge parallel LC resonant based LED driver is presented for doubling the gain, but the component count is more, thus increases overall cost and less efficient due to hard switched buck-boost converter.

LED drivers that can drive multiple loads are in need these days due to the multi-usage of LED lamps in every system. Independent control of these LED lamps and independent dimming are the essential features for these drivers. Many multiple load LED drivers are available in the literature [56, 60–65]. In [56](Fig. 2.6a), the number of transformers increases as the LED loads increase. In [60](Fig. 2.6b), the number of secondary windings of transformer increases as the LED loads increase. Even though a single transformer is used in [61], it needs a high-frequency AC bus, along with more number of inductors and capacitors. For such lighting applications, where isolation is not significant and essential, LED drivers presented in [56, 60, 61] may lead to increased cost. Several non-isolated LED drivers for multiple loads are reported in [62–65]. In [62](Fig. 2.7), the second load is driven from the leakage energy of coupled inductor used with first load. Thus, the wattage of second load must be less than that of the first load and hence, unable to drive equal loads. In addition, the output regulation is not possible and also, the reliability decreases with multiple loads. Further, independent dimming is not possible in [62, 63](Fig. 2.8). A high efficient input regulated multiple load LED driver is reported in [64](Fig. 2.9a) with reduced components. But this configuration can drive only loads with equal voltages and also independent dimming control is not possible. In [65](Fig. 2.9b), the LED driver provides unequal gains for multiple loads, thus can drive only loads with unequal voltages and ZVS is achieved partially across the switching devices.

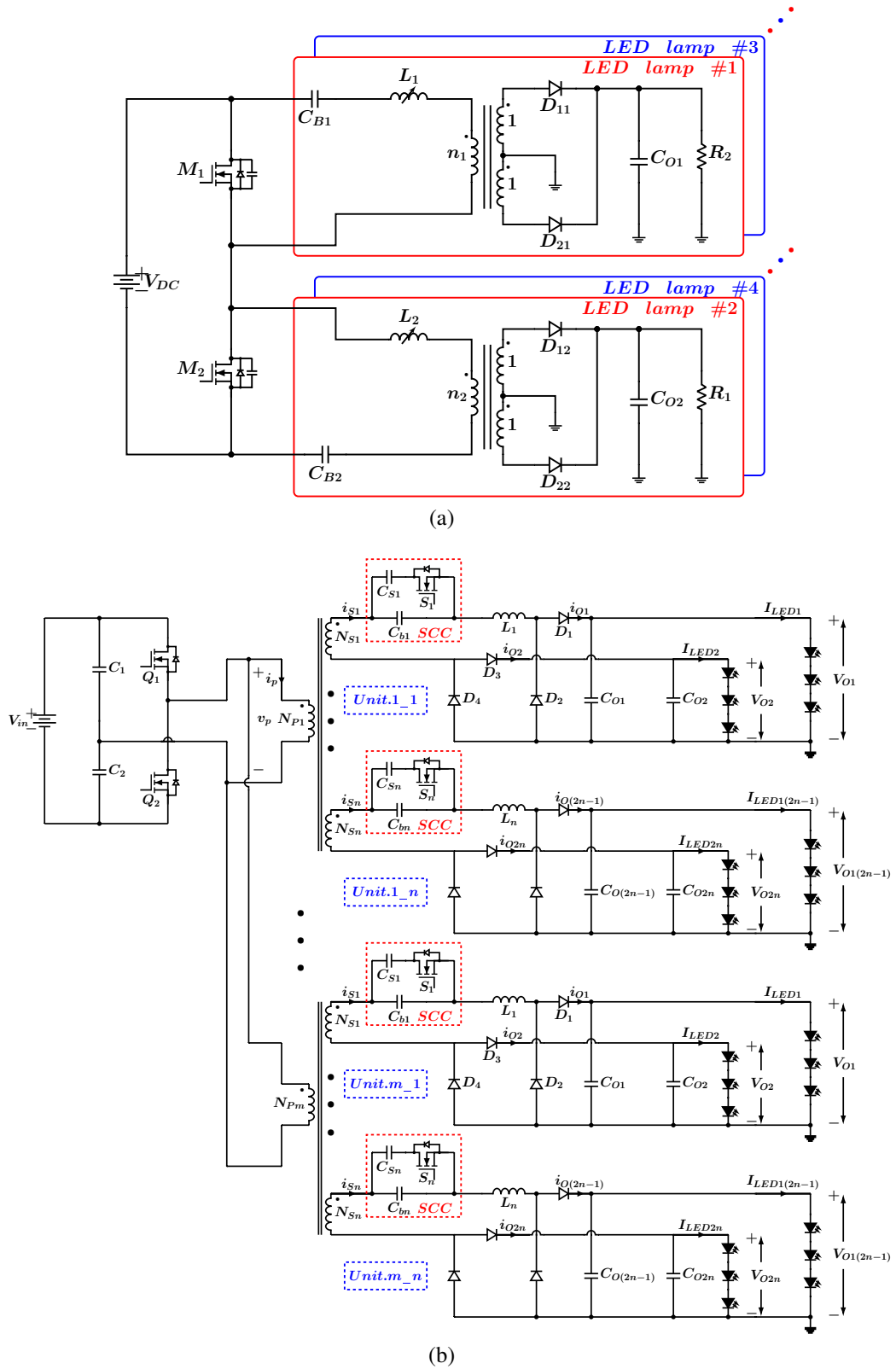


Figure 2.6: Multiple LED load configurations (a) Magnetic controlled single-inductor HB LED driver [56] (b) Switch-controlled capacitor based multi-channel LED driver [60]

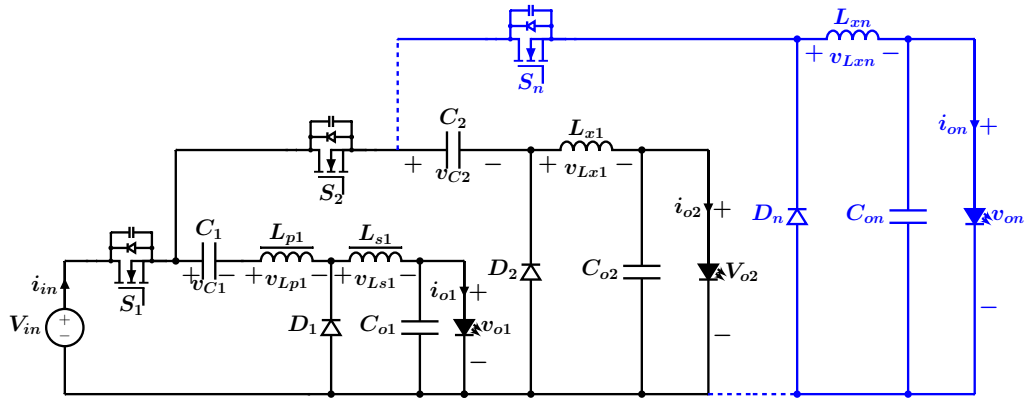


Figure 2.7: ZVS dual output LED driver [62]

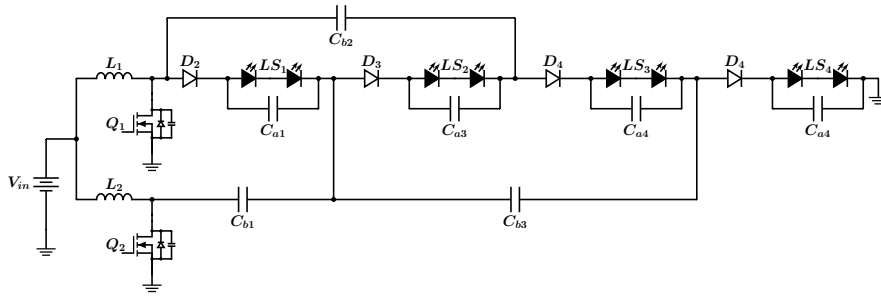


Figure 2.8: Two-phase interleaved LED driver with capacitive current sharing [63]

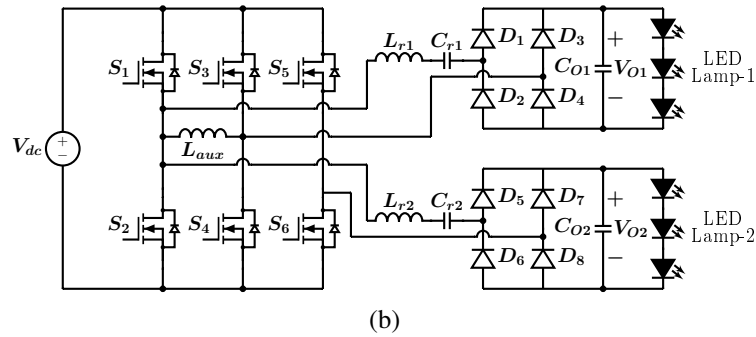
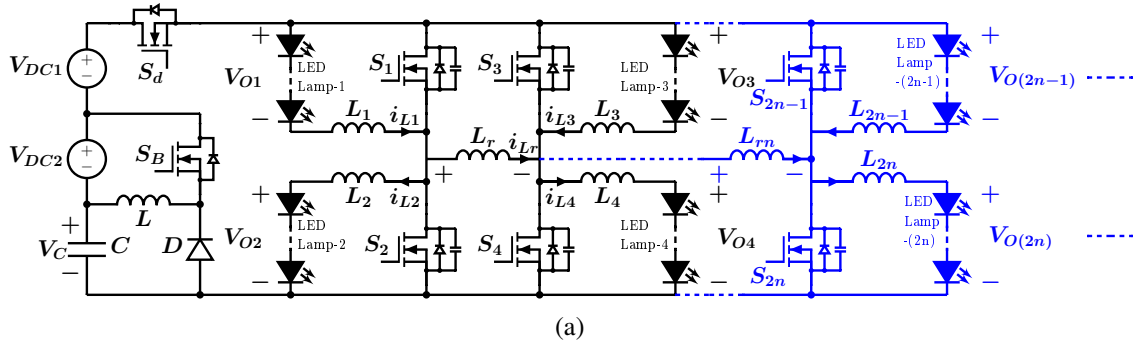


Figure 2.9: Multiple LED load configurations (a) Soft-switched full-bridge LED driver for SLS [64] (b) A three-leg resonant converter for two output LED LS [65]

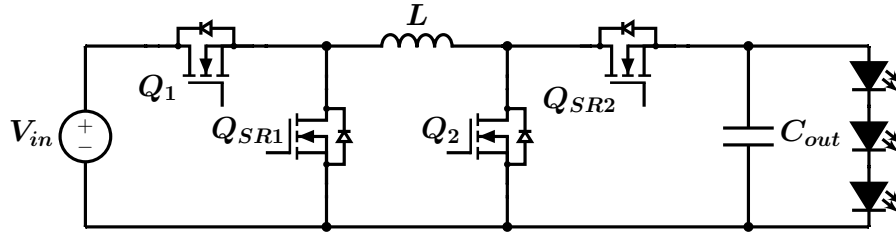


Figure 2.10: Topology-transition controlled 4-switch wide input NIBB LED driver [66]

2.1.3 A Wide Input Battery fed Automotive LED-LS

A battery of 12/24 V in automotive applications may vary up to 64 V during transients and can be even more [67, 68]. Further, there are different battery voltage systems available in the automotive system. Hence, there is a requirement of LED drivers that can operate for wide input voltage ranges. There are few LED drivers [66, 69–75] available with a wide input voltage range. LED drivers [66, 69–72] (Fig. 2.10) are hard switched, hence have limitations like reduced power density, increased switching losses and limited operating voltage range. The complex and costlier technologies like CMOS, BCDLite are employed in [69, 70, 73, 74].

Indeed, there are many wide input converters developed for PV, fuel cell applications, etc. High gain boost DC-DC converters [76, 77] are employed for wide input range fuel cell applications. An accurate adaptive constant on-time control scheme is used in [78] to improve the stability and performance under wide input / output voltage range applications. However, these converters are hard switched. Soft switched converters have become popular as they are compact in size with high efficiency. An isolated buck-boost converter with a hybrid three-level full-bridge primary side circuit is used in [79] to achieve wider voltage gain regulation. Resonant converter with APWM for voltage doubler rectifier is reported in [80] for wide input PV applications.

Resonant converters have become popular due to soft switching capability, high power density, etc. A multilevel LCC resonant converter with more control flexibility [82] and LLC resonant converters with two split branches and variable magnetizing inductance [83, 84] are presented, however, two transformers are employed which increases the size and cost. A double pulse duty cycle modulation that boosts the low input voltage and provides wide voltage regulation is reported for DC microgrid applications [85]. Several researchers have developed reconfigurable converters [86–91] to achieve wide voltage gain with soft switching by modifying the LLC resonant converters with respect to the configuration or modulation or both. A hybrid control with frequency modulation (FM) and phase shift modulation (PSM) is employed in [86]. In [87, 88], the diode bridge rectifier is replaced with semi-active rectifier. In [89]

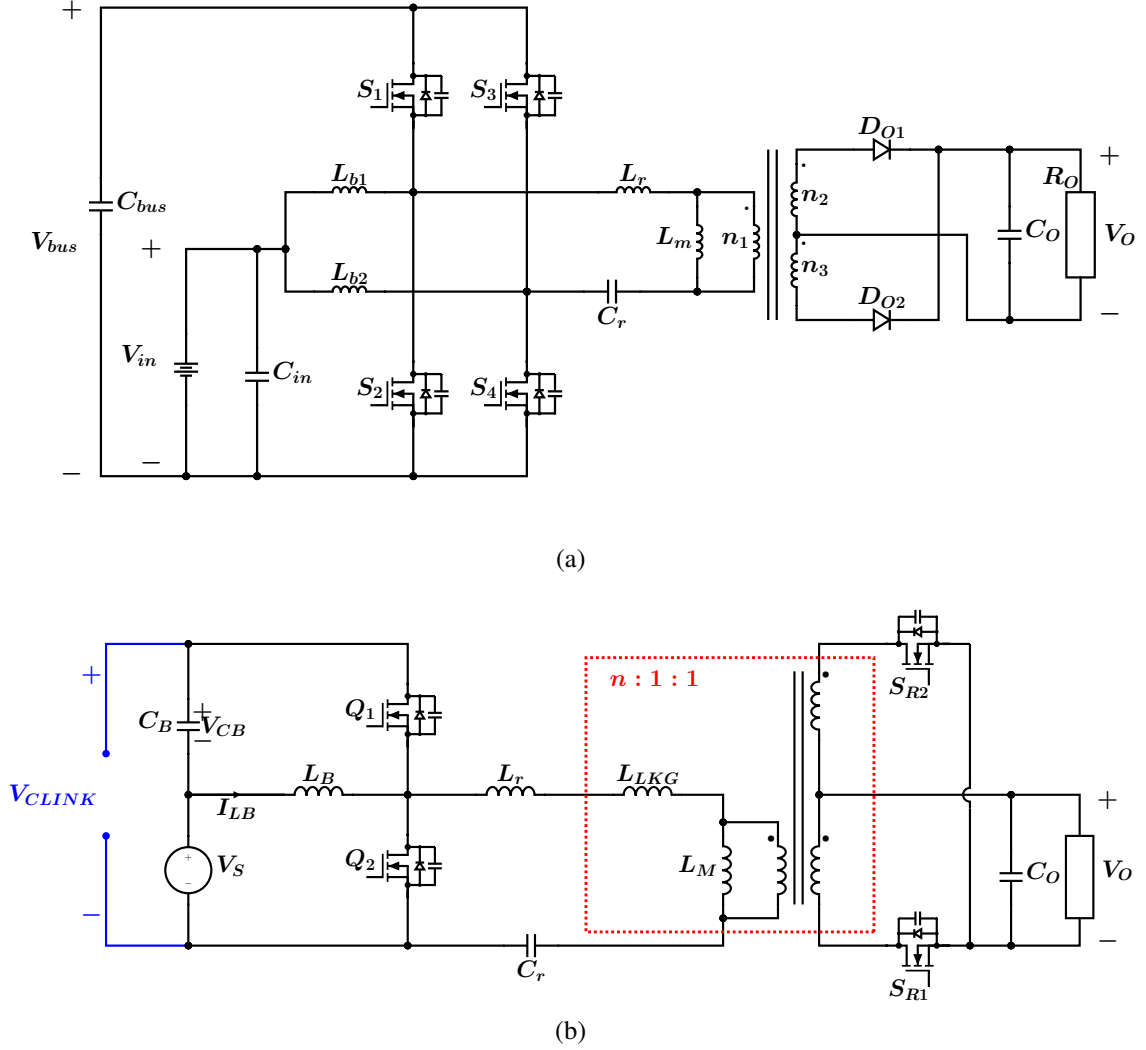


Figure 2.11: Wide input LED load configurations (a) Interleaved boost-integrated LLC resonant converter [81] (b) Asymmetric half-bridge resonant converter [57]

and [90], bidirectional switches are placed at the secondary side resonant tank and primary side respectively. The dual bridge LLC resonant converter [90] is a combination of half-bridge (HB) and full-bridge (FB) resonant converters, where the voltage is regulated by the transition between HB and FB with respective time durations in one cycle. A series resonant converter (SRC) that provides four configurable operation states depending on input and output voltage levels [91] is reported for grid-connected PV systems. Boost or buck-boost (BB) integrated resonant converters have become popular as they can produce a wide gain, thus suitable for wide input applications [57, 58, 81, 92, 93]. In [81](Fig. 2.11a), interleaved boost operation is integrated with FB LLC resonant converter and simple PWM control is employed. But there is a high start-up current in these converters due to the boost operation that results in high

switching stress across the devices. Thus, BB integrated resonant converters are gaining importance as they have a small start-up current due to the characteristics of BB operation [57]. In [57](Fig. 2.11b), BB operation is integrated with HB LLC resonant converter where both the primary side and secondary side switches are modulated to operate for wide input voltage applications without affecting the ZVS across devices. In [58](Fig. 2.12), BB operation is integrated with HB LCC resonant converter, where hybrid control combination of PWM and FM controls are employed. In [92](Fig. 2.13a), a four-switch non-inverting BB operation is integrated with FB LLC resonant converter. In [93](Fig. 2.13b), BB operation is integrated with dual bridge LLC resonant converter. PSM control is employed for adjusting the gains and FM control is employed to regulate the output voltage. All these converters are of isolated type. Some of them have control complexity either due to hybrid control or due to transition from one configuration to another in each cycle. Some topologies have increased component count that increases the conduction losses. Some topologies require additional gate driver circuits due to the replacement of switches with diodes.

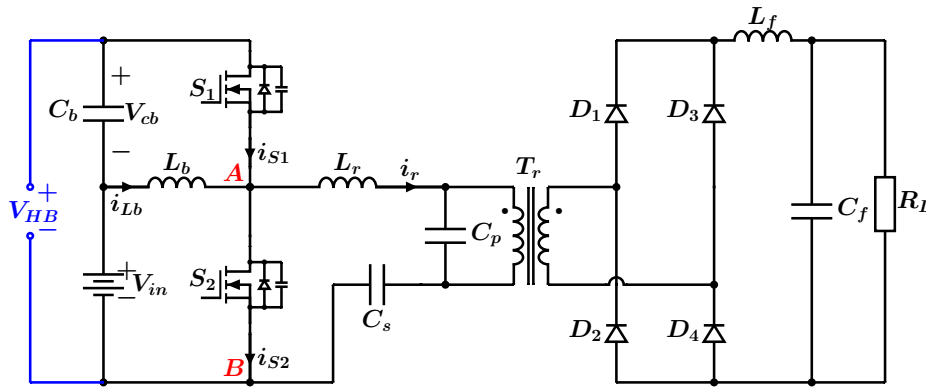


Figure 2.12: Asymmetrical hybrid-controlled half-bridge LCC resonant converter [58]

2.2 Problem Formulation & Objectives

Conventionally two-stage LED drivers are used for SPV/Battery fed LED SLS. However, the two-stage LED drivers have one or more of the following limitations

- More component count that increases the cost and size of the LED driver
- Hard switched operation that increases the switching losses and hence low efficient.
- Absence of buck/boost modes while charging and discharging as well.

Hence, there is a requirement of single-stage LED driver that are suitable for SPV fed LED-SLS having soft-switching feature and buck/boost modes in either directions.

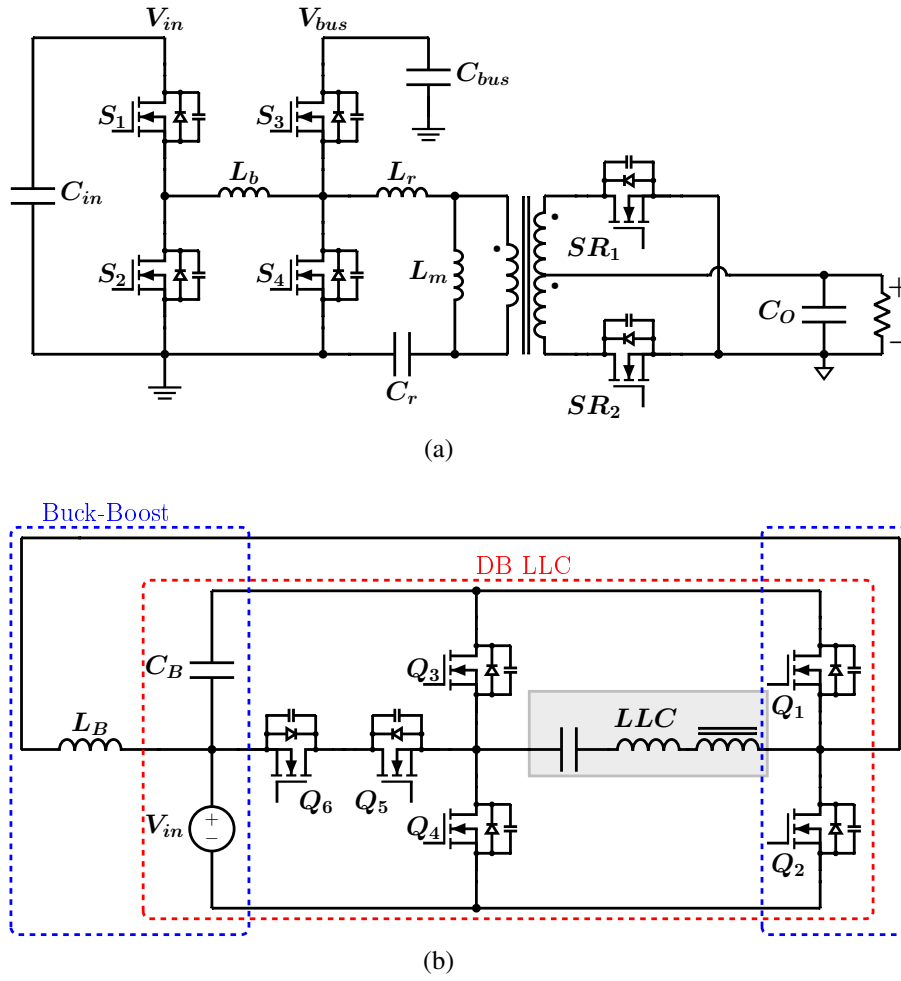


Figure 2.13: Wide input LED load configurations (a) A two-stage buck-boost integrated LLC converter [92] (b) A novel dual-bridge LLC resonant converter [93]

Also, even though, there are BDCs that suit for single stage PV fed LED-SLS, they suffer from one or more of the following drawbacks:

- Hard-switched operation that increases the switching losses and hence low efficient.
- Lack of buck/boost modes in both charging & discharging conditions.
- Larger in size
- High ripple current that increases the conduction losses and size of the filters.
- Not high efficient at all the loads.
- Absence of soft switching for all the devices
- Complex control

Hence, there is a requirement of soft switched-BDC for PV fed LED-SLS, that have buck/boost modes in either directions and overcoming all the above limitations.

Even though, conventional resonant converter based LED drivers have become popular due to their advantages like soft switching, high power density, high efficiency at all loads, etc., but they are unable to provide high gain for PV/Battery fed applications with reduced component count. Thus, there is a requirement of resonant converter based LED drivers that are suitable for PV/Battery fed applications overcoming the above drawbacks.

Also, there are few topologies that can drive multiple LED loads. Nevertheless, they suffer from one or many of the following limitations.

- Lack of high gain.
- Limited to loads with equal or unequal voltages but not both.
- Can only drive loads either with same rating or unequal ratings but not both.
- Cannot provide individual voltage regulation.
- Cannot provide independent dimming control.

Thus, there is a requirement of resonant converter based LED drivers that are suitable for multiple LED loads, overcoming the above drawbacks.

Even though there are LED drivers that are suitable for wide input automotive LED lighting applications, they suffer from one or many of the following limitations:

- Hard switched, thus increased conduction losses and hence reduced efficiency.
- Complex implementation.
- Narrow gain.
- More component count that increases the size and cost.
- Complex control.

Hence, there is a requirement of wide input LED drivers suitable for automotive applications that overcomes the above drawbacks.

2.3 Summary

In this chapter, a comprehensive literature review on different DC fed LED drivers have been presented. The short comings of existing LED drivers in specific SPV/Battery fed LED lighting applications are been identified, which motivates to propose improvised LED drivers.

Chapter 3

Bi-directional LED Driver for Solar PV fed Street Lighting Systems

Chapter 3

Bi-directional LED Driver for Solar PV fed Street Lighting Systems

3.1 Introduction

Soft switched BDC is well suitable for a single-stage SPV based LED-SLS. Even though many soft switched BDCs are available in the literature, they suffer from the drawbacks like: [high ripple](#), high conduction losses, complex control, etc. As CI-based soft switched converters are gaining focus for the LED lighting applications [62, 94], the main objective of this first work is to develop a single-stage soft switched CI based Buck Boost (BB) BDC (CI-BB-BDC) for a BSS assisted SPV powered LED-SLS that provides benefits like compact size, reduced ripple, high efficiency and buck-boost operation. The block diagram of proposed CI-BDC is shown in Fig. 3.1. The proposed CI-BDC operates in buck/boost mode during both charging and discharging of BSS. The CI along with auxiliary devices provide soft switching operation in either direction of power flow, thus improves the overall efficiency. Also, it provides additional advantages like reduced inductor size due to single magnetic core and less component count with single stage BDC operation. Dimming is used to control the brightness of the LED lighting. In this work, PWM dimming is adopted to control the LED illumination level as it offers advantages like high dimming ratio, constant operating point, etc. Followed by the detailed introduction of the proposed work, this chapter describes the proposed work-1 of CI-BB-BDC. The principle of operation and analysis of proposed CI-BDC topology are discussed in section 3.2. Design procedure of the CI-BDC is presented in section 3.3. The simulation & experimental analysis are discussed in section 3.4. In section 3.5, dimming procedure with simulation and experimental results are discussed. The power loss and efficiency analysis along with the performance of the proposed converter with other existing topologies are also discussed in section 3.5. Followed by conclusions in section 3.6.

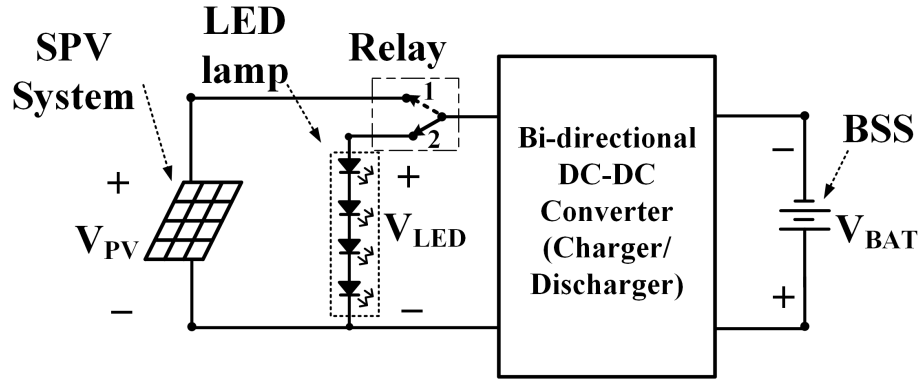


Figure 3.1: **Block diagram of single-stage converter for SPV fed LED lighting applications**

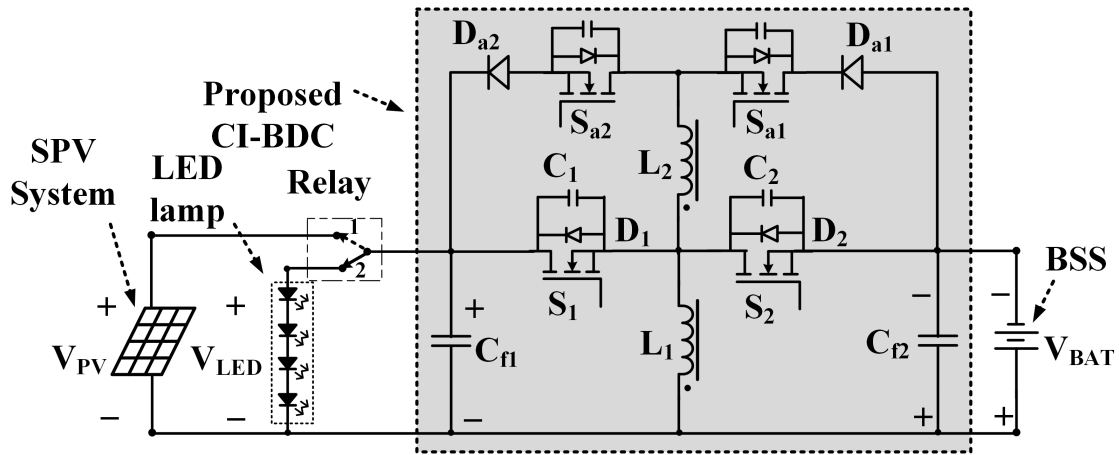


Figure 3.2: **Proposed CI-BDC for a SPV fed LED SLS**

3.2 Principle of Operation and Analysis

3.2.1 Proposed BDC and Its Principle of Operation

The circuit diagram of the proposed CI-BDC for a SPV fed LED SLS is shown in Fig. 3.2. It consists of inductances of main & auxiliary windings of CI (L_1 & L_2), main switches (S_1 & S_2), intrinsic body diodes (D_1 & D_2), auxiliary switches (S_{a1} & S_{a2}), auxiliary diodes (D_{a1} & D_{a2}), snubber capacitors (C_1 & C_2), filter capacitors (C_{f1} & C_{f2}), SPV system, BSS and LED lamp. The coupling factor of CI windings is 'k'. Values of C_1 and C_2 also include parasitic capacitances of the switches. The corresponding voltage and currents are represented as follows: gate voltages (v_{GS1} , v_{GS2} , v_{GSa1} & v_{GSa2}), switch voltages (v_{S1} & v_{S2}), switch currents (i_{S1} & i_{S2}), auxiliary diode voltages (v_{Da1} & v_{Da2}) and inductor currents (i_{L1} & i_{L2}). To facilitate the soft switching operation of the proposed SPV fed buck/boost CI-BDC in either direction of power flow, two auxiliary circuits are used. First auxiliary circuit consists of S_{a1} , D_{a1} and L_2 .

Second auxiliary circuit consists of S_{a2} , D_{a2} and L_2 . Here, L_2 is the common inductor for both the auxiliary circuits. These auxiliary circuits operate respectively during charging/discharging modes to achieve ZVS across main switches S_1 and S_2 . A relay is used to change the power flow direction of BDC. When it is in position-1, the BSS is charged from SPV power and when in position-2, the LED load is powered from BSS. As the relay operates only twice a day and is external to the proposed CI-BDC, it doesn't affect the efficiency of CI-BDC. Various **time intervals** of proposed CI-BDC during BSS charging and discharging operation are analyzed in subsequent sections. In this analysis, all the components are assumed ideal and slope of the device current is indicated as m_{i-j} , where 'i' represents the component and 'j' represents the **time interval** of operation.

3.2.2 CI-BDC in BSS Charging Mode

During day time, the relay is at position-1 to charge the battery from SPV power, during which S_{a1} is ON and S_{a2} is OFF as illustrated in Fig. 3.3. Fig. 3.4 depicts the key waveforms of the charging mode. The charging process is divided into seven **time intervals** and an equivalent circuit of each **time interval** is shown in Fig. 3.5 and explained as follows:

Let t_0 be the starting time interval for one cycle. **Time interval-1** starts at $t = t_0$. Prior to **interval-1**, switch, S_1 is in conduction. Current, i_{L2} decreases to zero with a slope of $m_{L2.7}$ and the diode, D_{a1} stops conducting at $t = t_0$.

3.2.2.1 Time Interval-1 [t_0 - t_1]

During this **interval**, S_1 is in conduction, as shown in Fig. 3.5(a). The main winding of CI will magnetize and current, i_{L1} which is same as i_{S1} , raises linearly with a slope of

$$m_{L1.1} = m_{S1.1} = \frac{V_{PV}}{L_1} \quad (3.1)$$

where V_{PV} is the SPV system voltage. The voltage across the auxiliary winding of CI is $V_{L2} = V_{L1} \sqrt{L_2/L_1}$ and the voltage across auxiliary diode, D_{a1} is $V_{D_{a1}} = V_{L2} + V_{L1} - V_{BAT}$ where $V_{D_{a1}} < 0$ and hence the diode is reverse biased and no current flows in auxiliary inductor and thereby $i_{L2} = 0$. At the end of this **interval**, i_{S1} reaches I_1 and S_1 is turned OFF.

3.2.2.2 Time Interval-2 [t_1 - t_2]

When S_1 is turned OFF at t_1 , snubber capacitors, C_1 starts charging and C_2 starts discharging. In this short duration, i_{L1} is assumed to be constant and is I_1 . Each capacitor carries a current of

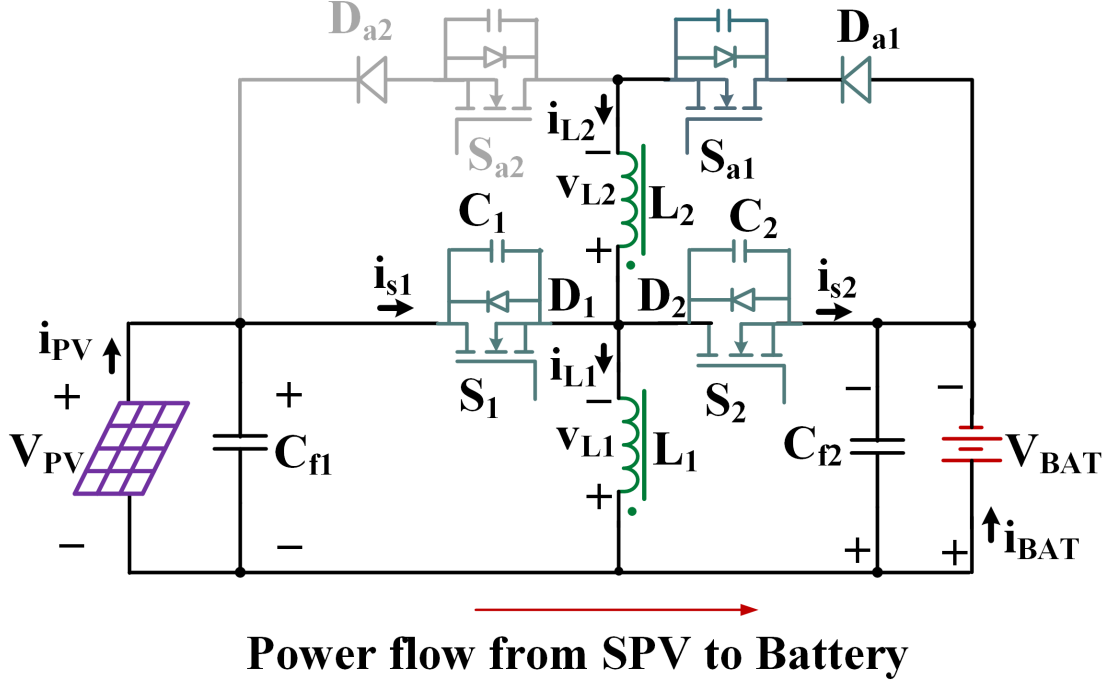


Figure 3.3: CI-BDC in BSS charging mode

$I_1/2$ as illustrated in Fig. 3.5(b). Time duration, T_{m2} can be expressed as

$$T_{m2} = t_2 - t_1 = \left(\frac{C_1 C_2}{C_1 + C_2} \right) \left(\frac{V_{PV} + V_{BAT}}{I_1/2} \right) \quad (3.2)$$

This interval ends at $t = t_2$ when C_1 and C_2 are completely charged and discharged, respectively.

3.2.2.3 Time Interval-3 [t_2 - t_3]

At $t = t_2$, diode, D_2 is forward biased. Assuming initially D_{a1} is not conducting, the voltage across it is expressed as

$$V_{D_{a1}} = V_{BAT} \sqrt{(L_2/L_1)} \quad (3.3)$$

Since $V_{BAT} > 0$, D_{a1} starts conducting when D_2 conducts as shown in Fig. 3.5(c). Presence of current i_{L2} leads to conduct D_{a1} with ZCS condition. The total time duration of interval-2 and interval-3 together constitute the dead time. Current in D_2 starts raising from negative value. Also, CI windings, L_1 demagnetize and L_2 magnetize; therefore, their corresponding currents decrease & increase, respectively, as described in (3.6). This interval ends when S_2 is given the gate pulse.

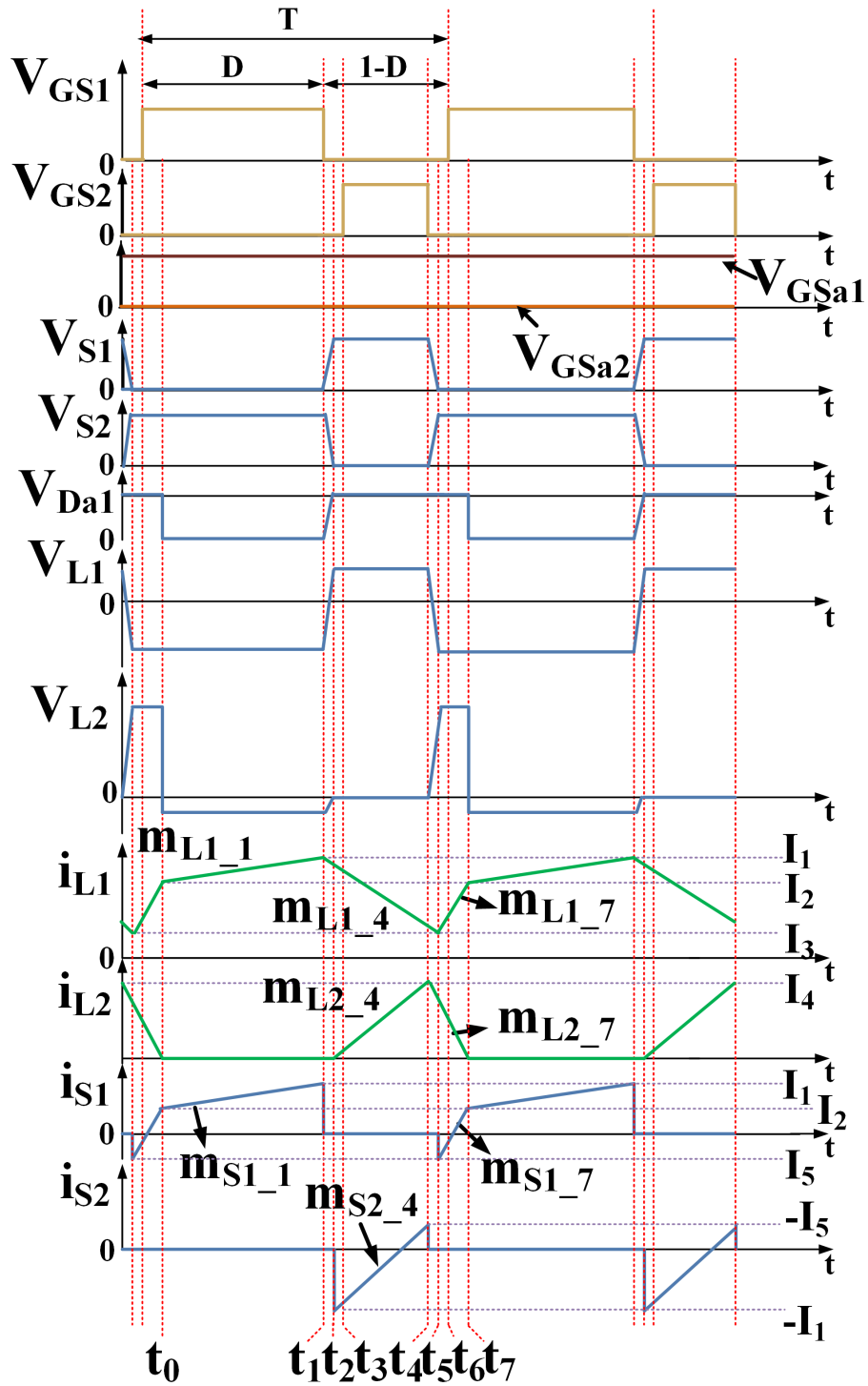


Figure 3.4: Key waveforms of BDC in charging mode

3.2.2.4 Time Interval-4 [t_3 - t_4]

Prior to interval-4, diode D_2 was in conduction and hence the voltage across S_2 is zero. The gate pulse provided at t_3 ; makes S_2 turn-ON with ZVS condition. The device current i_{S2} increases

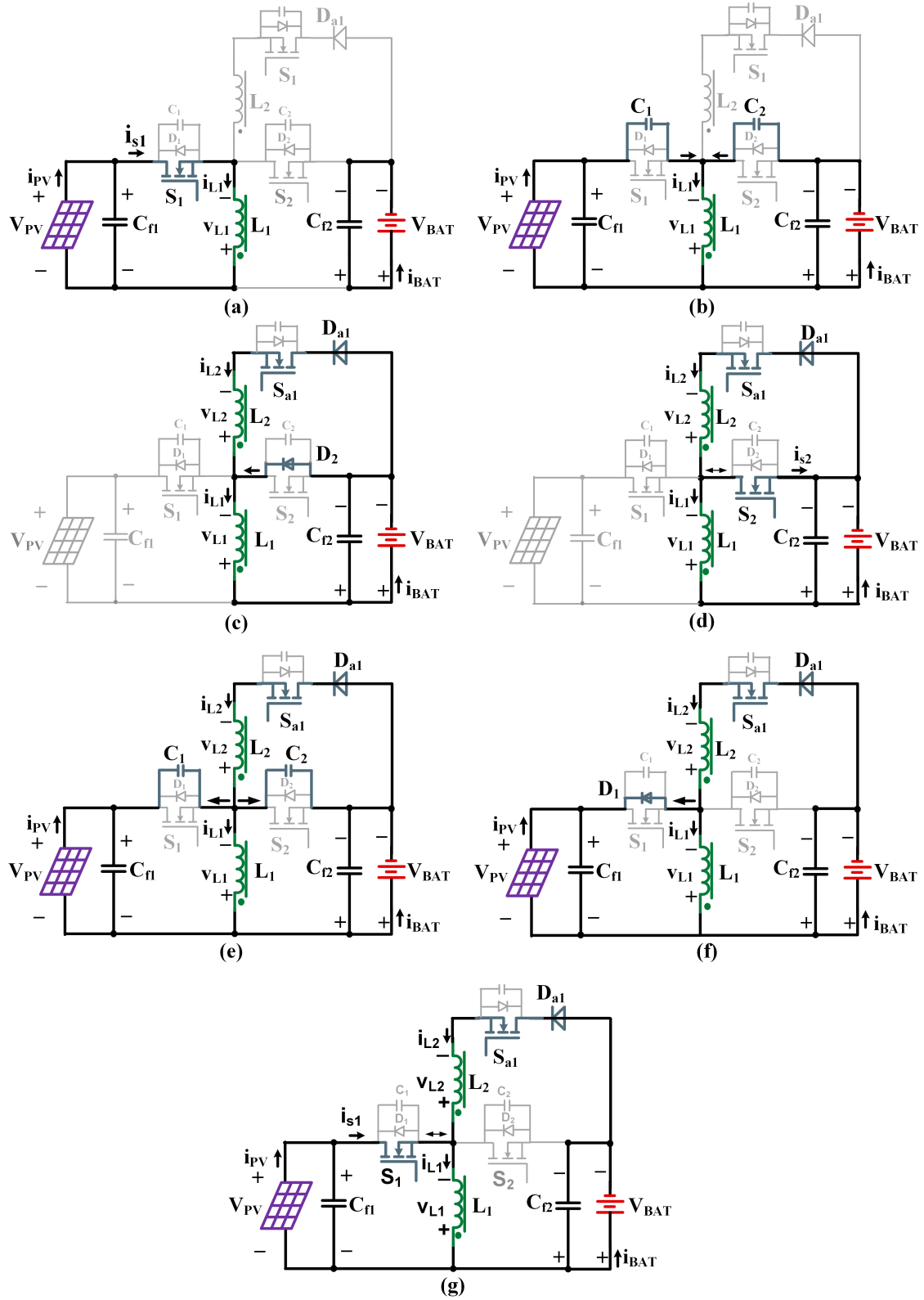


Figure 3.5: Time intervals of operation during BSS charging mode in BDC

linearly with a positive slope of $m_{S2.4}$. The voltages V_{L1} , V_{L2} , and mutual inductance M are given by

$$\left. \begin{aligned} V_{L1} &= -L_1 \frac{di_{L1}}{dt} - M \frac{di_{L2}}{dt} \\ V_{L2} &= -L_2 \frac{di_{L2}}{dt} - M \frac{di_{L1}}{dt} \\ M &= k * \sqrt{L_1 L_2} \end{aligned} \right\} \quad (3.4)$$

KCL and KVL equations of Fig. 3.5(d) will provide

$$i_{L1} = i_{L2} - i_{S2}; \quad V_{L1} - V_{BAT} = 0; \quad V_{L2} = 0 \quad (3.5)$$

By substituting (3.4) into (3.5), the current slopes are obtained as

$$m_{L1.4} = \frac{-V_{BAT}L_2}{L_1L_2 - M^2}; \quad m_{L2.4} = \frac{V_{BAT}M}{L_1L_2 - M^2}; \quad m_{S2.4} = \frac{V_{BAT}(M + L_2)}{L_1L_2 - M^2} \quad (3.6)$$

Substituting (3.6) in (3.4), the voltages across the two inductors can be obtained as

$$\left. \begin{aligned} V_{L1} &= V_{BAT} \\ V_{L2} &= 0 \end{aligned} \right\} \quad (3.7)$$

Also, from (3.6), it can be observed that i_{L1} decreases and both i_{L2} , i_{S2} increases. This interval ends when S_2 is turned OFF, and the current, i_{S2} reaches I_5 (negative), which is critical for ZVS turn-ON of S_1 and the currents, i_{L1} & i_{L2} reach I_3 & I_4 respectively.

3.2.2.5 Time Interval-5 [t_4 - t_5]

At t_4 , when S_2 is turned OFF, C_1 and C_2 are discharged and charged respectively at the same rate as shown in Fig. 3.5(e). Hence, currents i_{L1} & i_{L2} are assumed constant and each capacitor carries a current of $-I_5/2$. Time duration, T_{m5} can be expressed as

$$T_{m5} = t_5 - t_4 = \left(\frac{C_1 C_2}{C_1 + C_2} \right) \left(\frac{V_{PV} + V_{BAT}}{-I_5/2} \right) \quad (3.8)$$

This interval ends at $t = t_5$ when C_1 and C_2 are respectively completely discharged and charged.

3.2.2.6 Time Interval-6 [t_5 - t_6]

At $t = t_5$, D_1 starts conducting, as shown in Fig. 3.5(f). The diode current starts increasing from negative value. Also, the CI windings start magnetizing and demagnetizing, respectively; therefore, corresponding currents increase and decrease as described in (3.10 & 3.11). The total duration of interval-5 and interval-6 constitute the dead time. This interval ends when the gate pulse is provided to switch S_1 .

3.2.2.7 Time Interval-7 [t_6 - t_7]

Prior to interval-7, diode D_1 was in conduction and hence the voltage across S_1 is zero. The gate pulse provided at t_6 ; makes S_1 turn-ON with ZVS condition. The current i_{S1} increases linearly with a positive slope of $m_{S1.7}$. KCL and KVL equations of Fig. 3.5(g) will provide

$$i_{L1} = i_{S1} + i_{L2}; \quad V_{PV} - V_{L1} = 0; \quad V_{L2} - V_{PV} - V_{BAT} = 0 \quad (3.9)$$

By using (3.4) & (3.9), the current slopes are obtained as

$$m_{L1.7} = \frac{di_{L1}}{dt} = \frac{V_{PV}(M + L_2) + V_{BAT}M}{L_1L_2 - M^2} \quad (3.10)$$

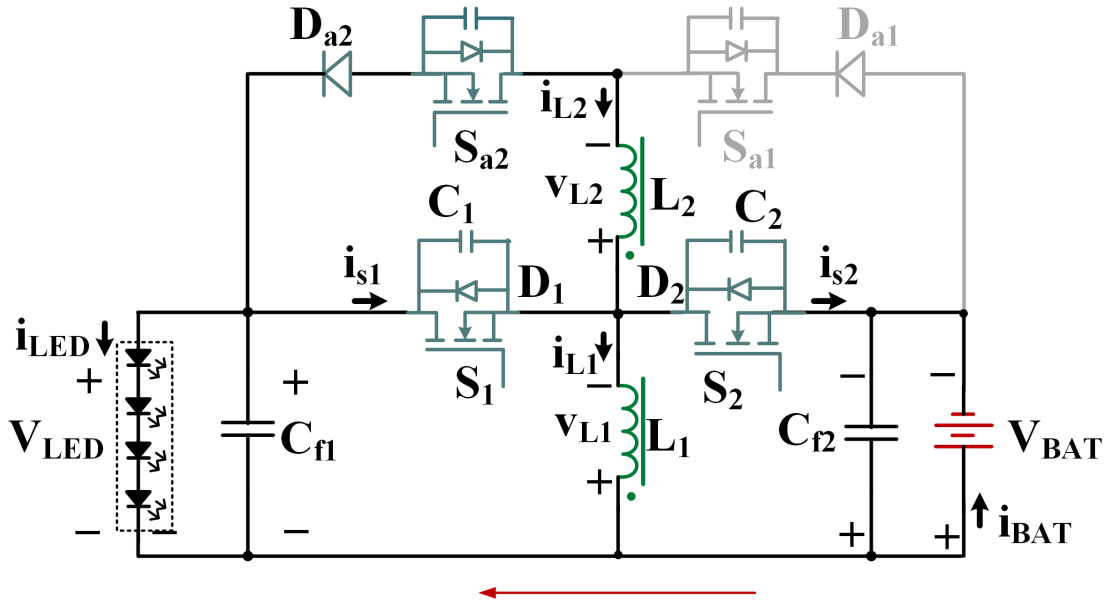
$$m_{L2.7} = \frac{di_{L2}}{dt} = -\frac{V_{BAT}L_1 + V_{PV}(M + L_1)}{L_1L_2 - M^2} \quad (3.11)$$

$$m_{S1.7} = \frac{di_{S1}}{dt} = \frac{V_{PV}(L_1 + L_2 + 2M) + V_{BAT}(L_1 + M)}{L_1L_2 - M^2} \quad (3.12)$$

Substituting (3.10) and (3.11) in (3.5), the voltages across the two inductors can be obtained as

$$\left. \begin{aligned} V_{L1} &= -V_{PV} \\ V_{L2} &= V_{PV} + V_{BAT} \end{aligned} \right\} \quad (3.13)$$

Also, from (3.10), (3.11) and (3.12), it can be observed that current i_{L2} decreases and currents i_{L1} and i_{S1} increase. This interval ends and continues to interval-1 when i_{L2} decreases to zero, making the diode D_{a1} to turn-OFF with ZCS condition and the currents i_{L1} and i_{S1} reach to I_2 value.



Power flow from Battery to LED lighting load

Figure 3.6: CI-BDC in BSS discharging mode

3.2.3 Power Flow from Battery to LED Lighting Load During Discharging

During night time, the relay is changed to position 2, so that BSS can discharge to drive the LED load during which S_{a2} is ON and S_{a1} is OFF as shown in Fig. 3.6. Fig. 3.7 shows the key waveforms of discharging mode. The discharging process is divided into seven **time intervals** and the corresponding equivalent circuit of each **interval** is shown in Fig. 3.8. The **time intervals** of operation in this direction of power flow is similar to the **time intervals** which have been discussed earlier, except that the direction of currents in CI windings is reversed.

3.3 Design Procedure

To make a generalized procedure, let the input voltage be V_{in} and output voltage be V_{out} . In order to achieve ZVS condition in either direction of power flow at all the load levels, proper designs of inductors and capacitors are essential. As the operation of the BDC is similar in both the directions of power flow, the SPV to BSS charging operation is considered for the analysis as the worst-case criteria for ZVS condition. Hence $V_{in} = V_{PV}$ and $V_{out} = V_{BAT}$.

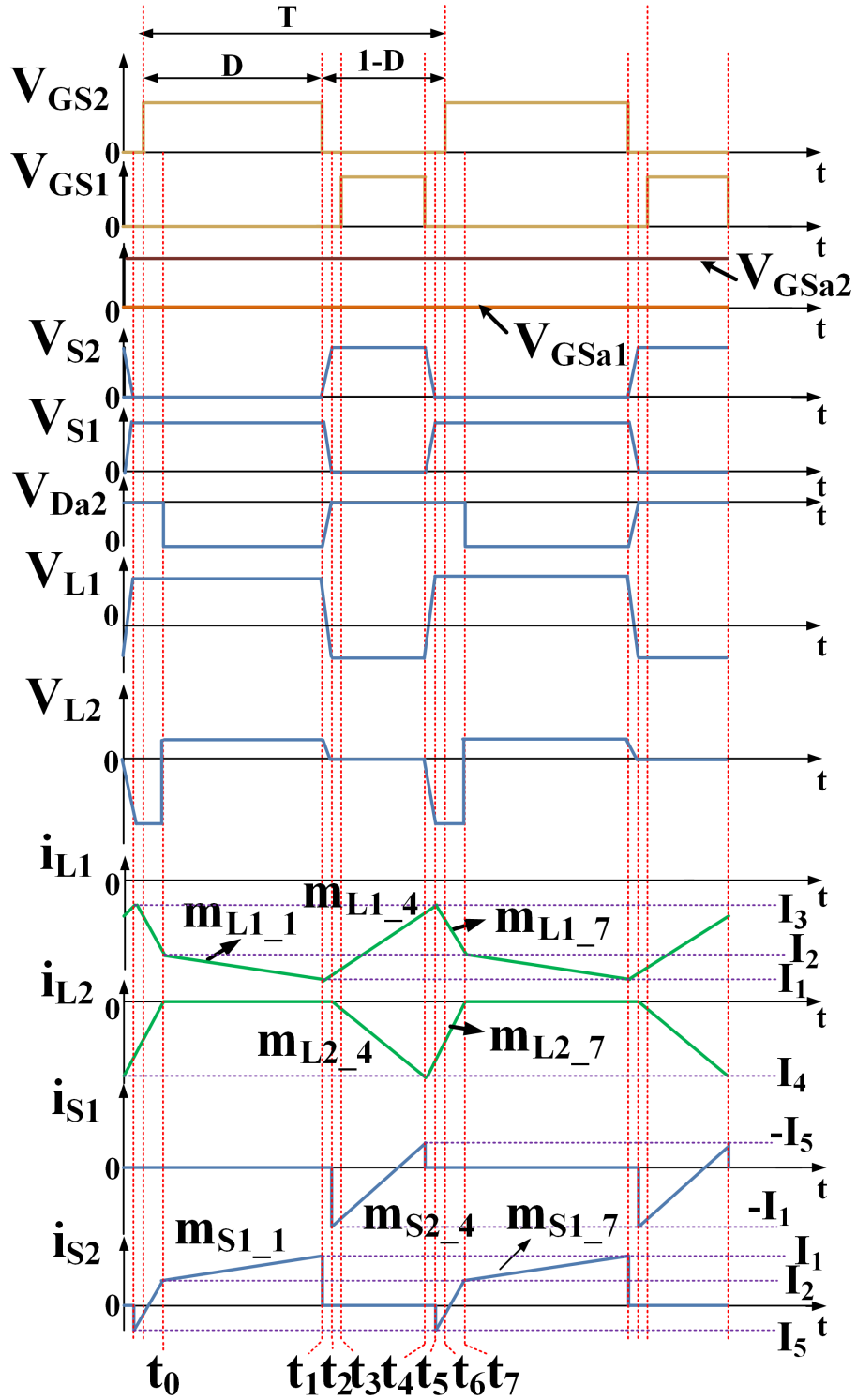


Figure 3.7: Key waveforms of BDC in discharging mode

3.3.1 ZVS Criteria

ZVS is achieved during **interval-2** and **interval-5** operations in charge/discharge modes. Based on (3.2), $T_{m2} \propto 1/I_1$ where I_1 is proportional to load current. For ZVS turn-OFF in

interval 2, period T_{m2} determined by load current, which is always higher than minimum turn-

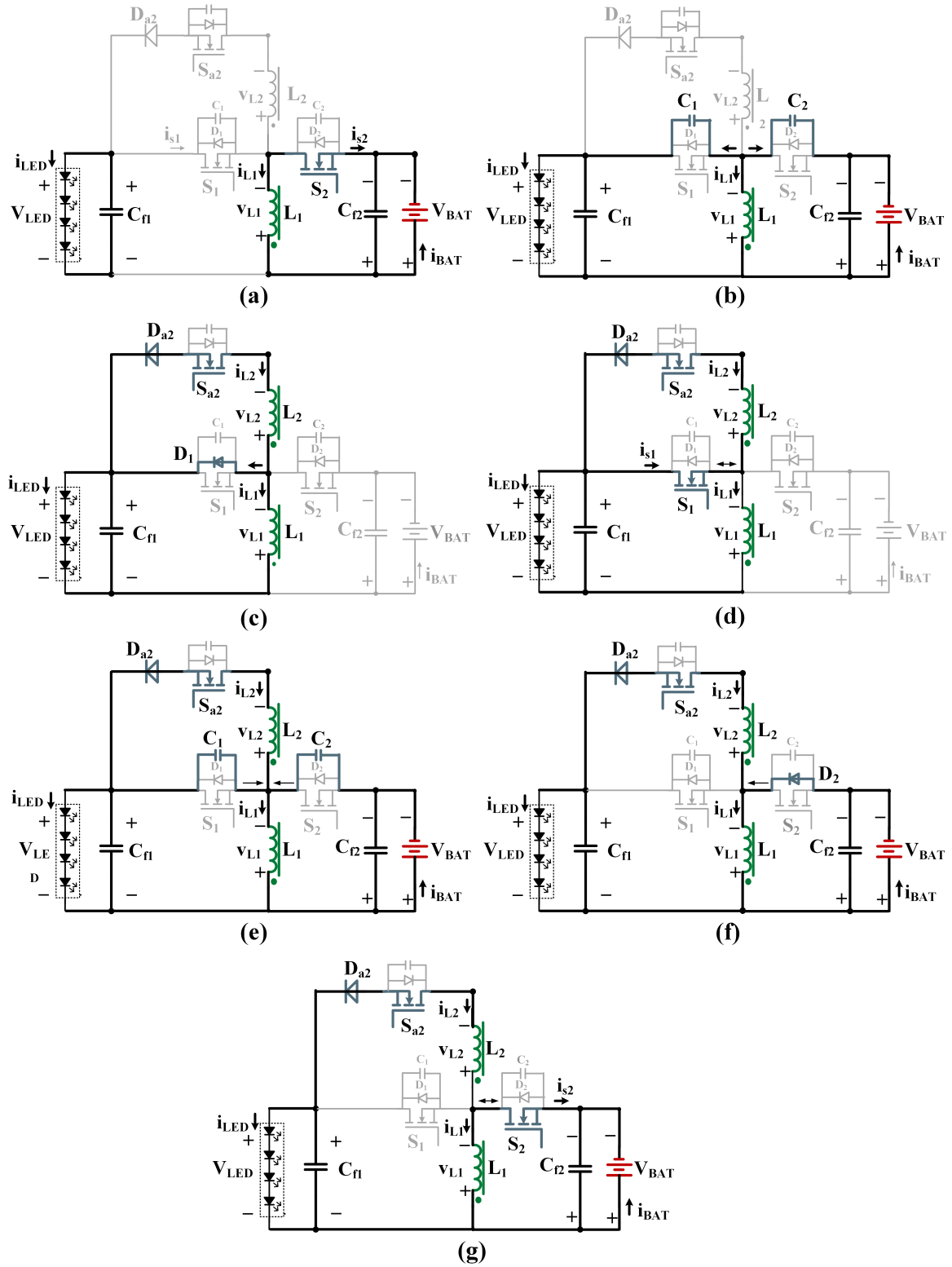


Figure 3.8: Time intervals of operation during BSS discharging mode in BDC

OFF time ($t_{min-OFF}$) of switching device. For ZVS turn-ON in **interval-5**, the dead time (t_d) is higher than T_{m5} . Based on (3.8), $T_{m5} \propto 1/|-I_5|$ and its maximum value can be obtained for I_{5min} at **maximum load current**. Thus, it confirms that the **maximum load current** is the critical condition for both ZVS turn-OFF and ZVS turn-ON.

3.3.2 Duty Ratio

The winding L_2 of CI is to achieve soft switching as a part of the auxiliary network; hence, the voltage gain of the proposed BDC is determined by the main winding of CI. Thereby, the duty ratio (D) of CI-BDC is same as in conventional buck/boost BDC and expressed as

$$D = \frac{|V_{out}|}{|V_{out}| + V_{in}} \quad (3.14)$$

The switching period is considered as T and the duration of **interval-4**, T_{m4} can be expressed as

$$T_{m4} = (1 - D) \times T = \frac{V_{in}}{|V_{out}| + V_{in}} \times T \quad (3.15)$$

3.3.3 Design of Capacitors C_1 & C_2

The capacitors need to be designed optimally such that they are neither large nor too small to achieve effective ZVS turn-ON and turn-OFF. Based on the analysis of ZVS criteria, the design relation of capacitors is obtained as follows. According to switching characteristics of MOSFET, its turn-OFF time, $t_{min-OFF}$, is considered as 100 ns. Therefore for achieving ZVS turn-OFF, $T_{m2} \geq T_{m2min} = T_{m2}|_{I_{1max}} > 100 \text{ ns}$. Based on (3.2), the capacitor C_r is

$$C_r = C_1 = C_2 \geq \left(\frac{100 \times 10^{-9} \times I_1}{V_{in} + V_{out}} \right) \quad (3.16)$$

For turn-ON, dead time, t_d is considered as 300 ns. Hence, for achieving ZVS turn-ON, $T_{m5} < 300 \text{ ns}$. Based on (3.8) and (3.14), current, I_5 is

$$I_5 = I_3 - I_4 \leq -\frac{(V_{in} + V_{out})C_r}{300 \times 10^{-9}} \quad (3.17)$$

3.3.4 Slope of Current, i_{L1} in **Interval-4**

Current in main winding at **maximum load current** can be expressed as

$$I_{L1max} = \frac{P_{omax}}{V_{in}D} \quad (3.18)$$

Let ripple coefficient of i_{L1} is k_i . The peak and valley values of i_{L1} are expressed as

$$I_1 \approx I_{L1max} \times \left(1 + \frac{k_i}{2}\right); I_3 \approx I_{L1max} \times \left(1 - \frac{k_i}{2}\right) \quad (3.19)$$

Hence, the current ripple of i_{L1} is obtained as

$$\Delta I_{L1} = I_3 - I_1 = -I_{L1max} \times k_i \quad (3.20)$$

By using (3.20) & (3.15), slope $m_{L1.4}$ is

$$m_{L1.4} = \frac{\Delta I_{L1}}{T_{m4}} = -\frac{(I_{L1max} \times k_i)}{T} \times \frac{|V_{out}| + V_{in}}{V_{in}} \quad (3.21)$$

3.3.5 Slope of Current, i_{L2} in **Interval-4**

The current ripple of i_{L2} is obtained as

$$\Delta I_{L2} = I_4 = I_3 - I_5 = I_{L1max} \times \left(1 - \frac{k_i}{2}\right) - I_5 \quad (3.22)$$

By using (3.22) & (3.15), slope $m_{L2.4}$ is

$$m_{L2.4} = \frac{\Delta I_{L2}}{T_{m4}} = \frac{I_{L1max} \times \left(1 - \frac{k_i}{2}\right) - I_5}{T} \times \frac{|V_{out}| + V_{in}}{V_{in}} \quad (3.23)$$

3.3.6 Slope of Current, i_{L2} in **Interval-7**

In this converter, the duration of **interval-7**, T_{m7} is considered as $T/20$. The current ripple of i_{L2} is obtained as

$$\Delta I_{L2} = -I_4 = -I_3 + I_5 = -I_{L1max} \times \left(1 - \frac{k_i}{2}\right) + I_5 \quad (3.24)$$

By using (3.24) & considering T_{m7} as $T/20$, slope $m_{L2.7}$ is

$$m_{L2.7} = \frac{\Delta I_{L2}}{T_{m7}} = - \frac{\left[I_{L1max} \times \left(1 - \frac{k_i}{2} \right) - I_5 \right]}{T/20} \quad (3.25)$$

3.3.7 Calculating L_1 , L_2 and M

Substituting $m_{L1.4}$, $m_{L2.4}$ from (3.6) and $m_{L2.7}$ from (3.11) into (3.21), (3.23) and (3.25), corresponding simplified equations as follows

$$\frac{V_{out}L_2}{L_1L_2 - M^2} = \frac{I_{L1max}k_i}{T} \times \frac{|V_{out}| + V_{in}}{V_{in}} \quad (3.26)$$

$$\frac{V_{out}}{L_1L_2 - M^2} = \frac{I_{L1max} \left(1 - \left(\frac{k_i}{2} \right) \right) - I_5}{T} \times \frac{|V_{out}| + V_{in}}{V_{in}} \quad (3.27)$$

$$\frac{V_{out}L_1 + V_{in}(M + L_1)}{L_1L_2 - M^2} = \frac{I_{L1max} \left(1 - \left(\frac{k_i}{2} \right) \right) - I_5}{T/20} \quad (3.28)$$

L_1 , L_2 and M can be determined from the above equations, by using which k from (3.21) can be computed.

3.4 Simulation & Experimental Analysis

In the proposed CI-BDC, the system is loaded more during the discharging operation of BSS to the LED load. The CI-BDC circuit elements are designed for ZVS operation based on the above mentioned critical load condition.

TMX HP-3W LEDs are used in the prototype. The total LED load in the proposed CI-BDC is composed of 4 LED strings connected in parallel, with 4 series-connected LEDs in each string. Each LED is operated at 4.5 V, 544 mA and 2.448 W with a threshold voltage of 2.4 V. Thereby, the total LED load voltage (V_{LED}) is 18 V, power (P_{LED}) is 39.168 \approx 40 W, current (I_{LED}) is 2.176 A \approx 2.2 A, with a threshold voltage (V_{th}) of 9.6 V.

Two Lead-Acid Batteries, connected in series, are used with total rated voltage, V_{BAT} of 26 V and Ah rating of 7 Ah. With these batteries, the LED lamps can be operated for 5 hours per day. By increasing the Ah rating of the battery, the duration of operation of the LED lamps can further be increased. $V_{in} = V_{BAT} = 26V$ and $V_{out} = V_{LED} = 18V$ are considered for

the design of converter. Switching frequency is selected as 100 kHz. The ripple coefficient, k_i is considered as 0.4. Based on (3.14), (3.18) and (3.19), values of D , I_{L1max} and hence, I_1 are calculated respectively. Using (3.16), value of C_r and thereby values of C_1 and C_2 are calculated as 5 nF. By using (3.17), I_5 at maximum load current is calculated as -1.5 A. By using (3.26) to (3.28) with the above parameters, the parameters of the CI, ie., L_1 , L_2 and M are calculated. However, the practical realization of the coupled inductor, in the proposed configuration, with exact calculated mutual inductance is difficult to achieve. The M value with $\pm 2\%$ tolerance should be realized, and if not possible, M value with little higher than the desired value can be realized such that ZVS is always possible in the proposed configuration with minimum conduction losses. Compared with the calculated value, if designed M value is very low, ZVS is not possible and if it is too high, ZVS is possible but with little higher conduction losses. The parameter values of the experimental circuit are shown in Table 3.1. E42/21/15 ferrite core is used in CI. The proposed CI-BDC is simulated using OrCAD PSpice and the implemented prototype is shown in Fig. 3.9. The control signals are generated using Basys3 Artix-7 FPGA board, which can also be generated using Analog circuit with IC-SG3525 PWM controller. Fig. 3.10 shows the control logic of the converter implemented in FPGA. ‘countMax’ value is to be set based on the desired switching frequency. As the FPGA used has 100 MHz clock frequency, to set the switching frequency of 100 kHz, the ‘countMax’ is to be set for a value of (100 MHz / 100 kHz). The operation of each block in the figure is enabled for every positive edge of the clock. The duty cycle is compared with the sawtooth waveform developed by the counter. When the duty cycle is less than the magnitude of sawtooth waveform, the main switch control signal is high, otherwise zero. Similarly, when the magnitude of the sawtooth waveform is less than (duty cycle + deadtime) value, then it is compared with the value of (countMax - deadtime). If it is less, the synchronous switch control signal is high; otherwise, it is zero. Also, based on the toggle switch position (0 or 1), the switching pulses for all the devices are interchanged for either direction of power flow. With a switching frequency of 100 kHz, the time period is 10 μs . Hence, in the proposed circuit, PWM signals can also be generated with a simple low-cost MCU like Launchpad-TMS320F28379D, which runs on 200 MHz crystal that gives 5 ns resolution with 0.05% duty cycle accuracy for good voltage regulation. Thereby, the FPGA controller can also be replaced by a simple low-cost MCU, which results in overall cost reduction. In the experimentation, a programmable power supply is used as an emulated SPV source. To evaluate the performance of proposed CI-BDC, a conventional hard switched buck-boost BDC is also implemented with inductor, $L = 232 \mu H$. The various test conditions considered are discussed in the following section.

Table 3.1: Specifications of the CI-BDC

Parameters	Values
V_{PV}	36 V
V_{BAT}	26 V
V_{LED}	18 V
f_{SW}	100 kHz
L_1	232.8 μH
L_2	39.4 μH
k	0.92
C_1, C_2	5 nF
Switches S_1, S_2, S_{a1}, S_{a2}	IRF540N
Diodes D_{a1}, D_{a2}	MBR20200CT

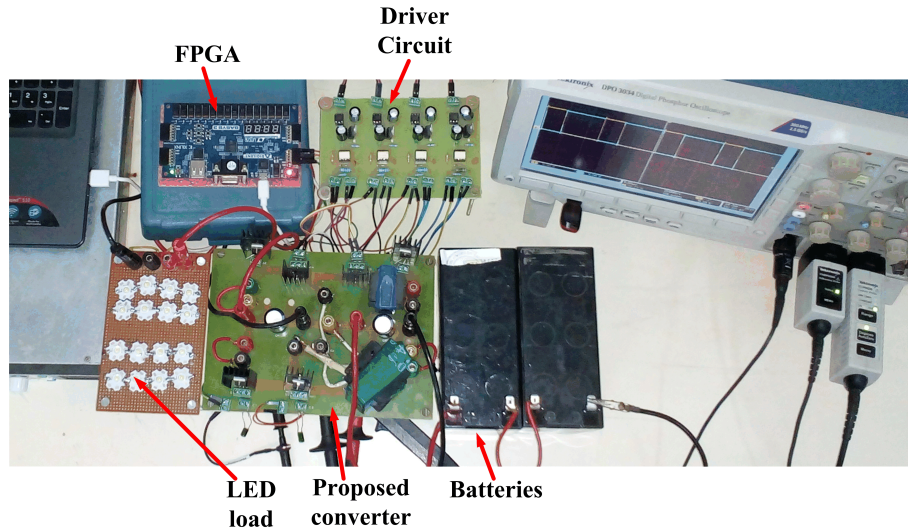


Figure 3.9: Experimental prototype of proposed CI-BDC

3.4.1 Case 1: Discharging of BSS (26 V) to the LED SLS (18 V) in Buck Mode

The CI-BDC operates in buck mode while discharging the BSS power to the LED lighting load. Fig. [3.11] to Fig. [3.15] depict the corresponding simulation & experimental waveforms at full load of 40W. Fig. 3.11 shows the experimental gate signals of switches S_2 and S_1 . Fig. 3.12a & Fig. 3.12b show the simulation & experimental waveforms of CI winding currents. Fig. 3.13a to Fig. 3.13d show the simulation and experimental waveforms of voltage and current at main switches. Perfect ZVS turn-ON is achieved and near ZVS turn-OFF condition is achieved and can be observed from these figures. Fig. 3.14a and Fig. 3.14c shows the simu-

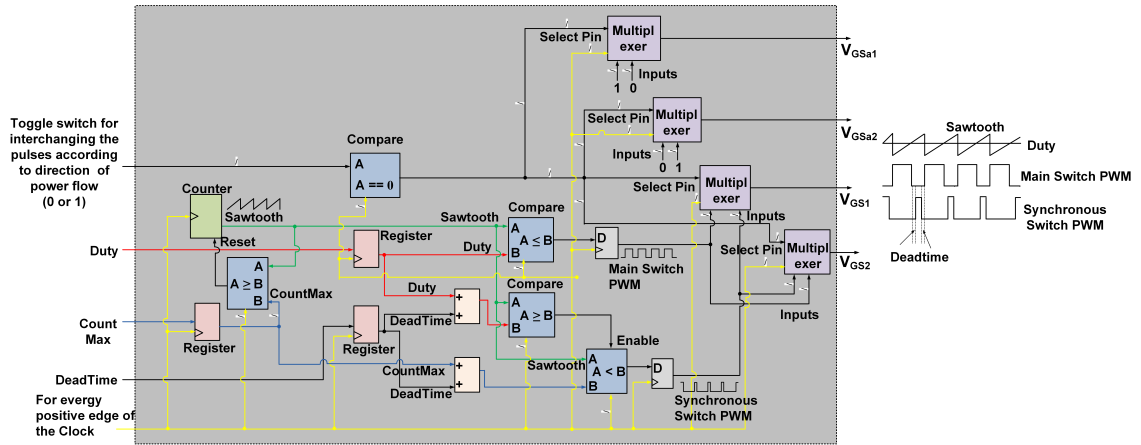


Figure 3.10: Block diagram of control logic implemented in FPGA for generating switching signals

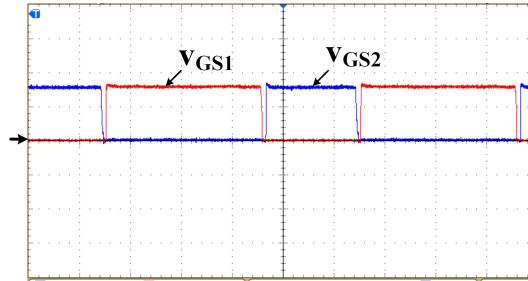
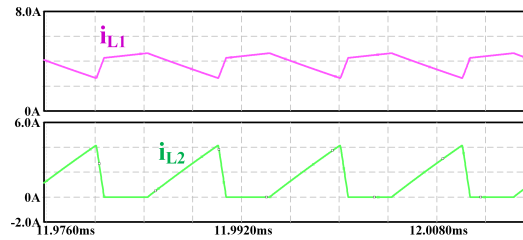
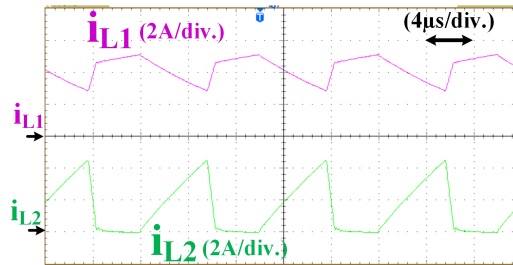


Figure 3.11: Experimental waveforms of gate signals of BDC in discharging mode, v_{GS1} & v_{GS2}



(a)



(b)

Figure 3.12: Simulation & experimental waveforms of inductor currents of BDC in discharging mode (a) Simulation waveforms of i_{L1} and i_{L2} (b) Experimental waveforms of i_{L1} and i_{L2}

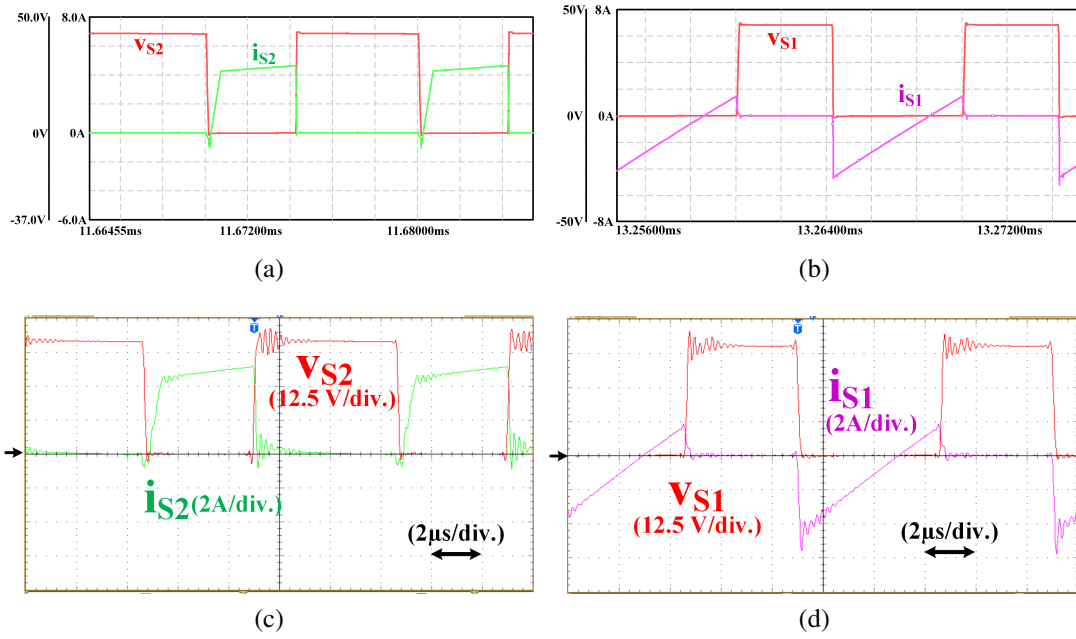


Figure 3.13: Simulation & experimental voltage and current waveforms of main switches of BDC in discharging mode: (a) Simulation waveforms of v_{S2} and i_{S2} (b) Simulation waveforms of v_{S1} and i_{S1} (c) Experimental waveforms of v_{S2} and i_{S2} (d) Experimental waveforms of v_{S1} and i_{S1}

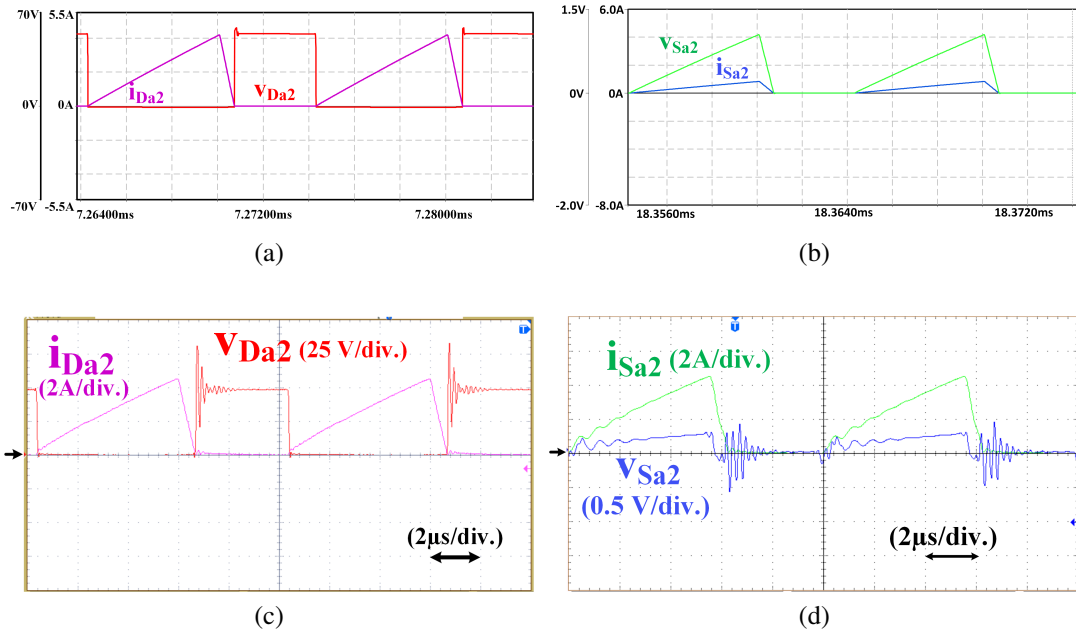


Figure 3.14: Simulation & experimental waveforms of v_{Da2} , i_{Da2} , v_{Sa2} , i_{Sa2} in discharging mode: (a) Simulation waveforms of v_{Da2} and i_{Da2} (b) Simulation waveforms of v_{Sa2} and i_{Sa2} (c) Experimental waveforms of v_{Da2} and i_{Da2} (d) Experimental waveforms of v_{Sa2} and i_{Sa2}

lation & experimental voltage and current waveforms of the auxiliary diode, D_{a2} in which ZCS turn-ON and ZCS turn-OFF can be observed. Fig. 3.14b and Fig. 3.14d show the simulation & experimental voltage and current waveforms of the auxiliary switch, S_{a2} . With continuous gate signal, the auxiliary switch is always ON that leads to only conduction losses but zero switching losses. Thus, ZVS operation is not necessary for auxiliary switch S_{a2} . Fig. 3.15a & Fig. 3.15b illustrate experimental voltage and current waveforms of the SPV system with an LED load. The efficiency of the proposed CI-BDC is 90.68% whereas conventional counterpart is 87.71%. The ripple of LED current is 8.58% with CI-BDC, which is well within limits. The auxiliary switch S_{a2} is in continuous conduction, hence there are no switching losses. The auxiliary diode D_{a2} is operated in ZCS condition and hence the associated switching losses are minimum. Thereby, the auxiliary circuit used is also operated under soft switching, which results in improved efficiency. Fig. 3.16a shows the experimental CI winding currents for different LED loads, which shows that i_{L1} magnitude decreases with the load while i_{L2} remains unchanged. Fig. 3.16b shows the resultant current, i_{Lr} due to i_{L1} & i_{L2} that flows through the switches. It can be observed that as the load varies, i_{Lr} also varies and the absolute value of negative peak current increases as the load decreases. This implies that the recycling energy in CI increases as load decreases, which affects the efficiency at light loads. The CI-BDC can also be operated in boost mode if needed, in this direction of power flow.

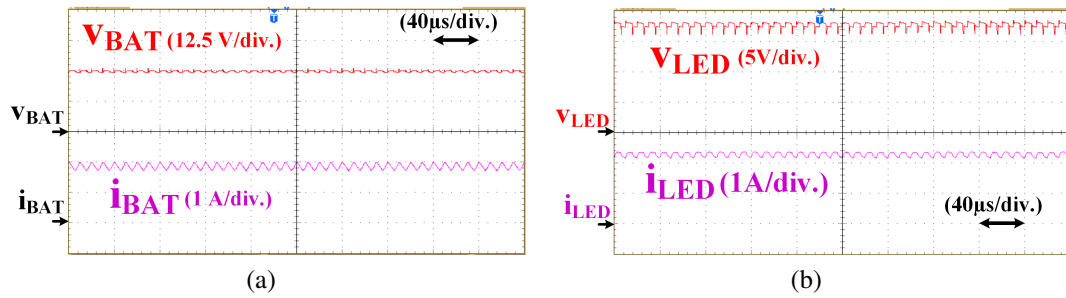


Figure 3.15: Experimental input & output waveforms of BDC in discharging mode: (a) Waveforms of v_{BAT} & i_{BAT} (b) Waveforms of v_{LED} & i_{LED}

3.4.2 Case 2: SPV System (36 V) to BSS Charging (26 V) in Buck Mode

The battery charging current is in the range of 0.3 to 1 A. Hence, the charging power level is under the light load condition. This increases recycling energy in CI, which leads to reduced efficiency. In order to overcome this limitation, an external inductance of 19.3 μ H, is used in series with L_2 . This facilitates ZVS operation and hence provides advantages like reduced current rating of CI windings, resulting in less recycling energy, improved efficiency

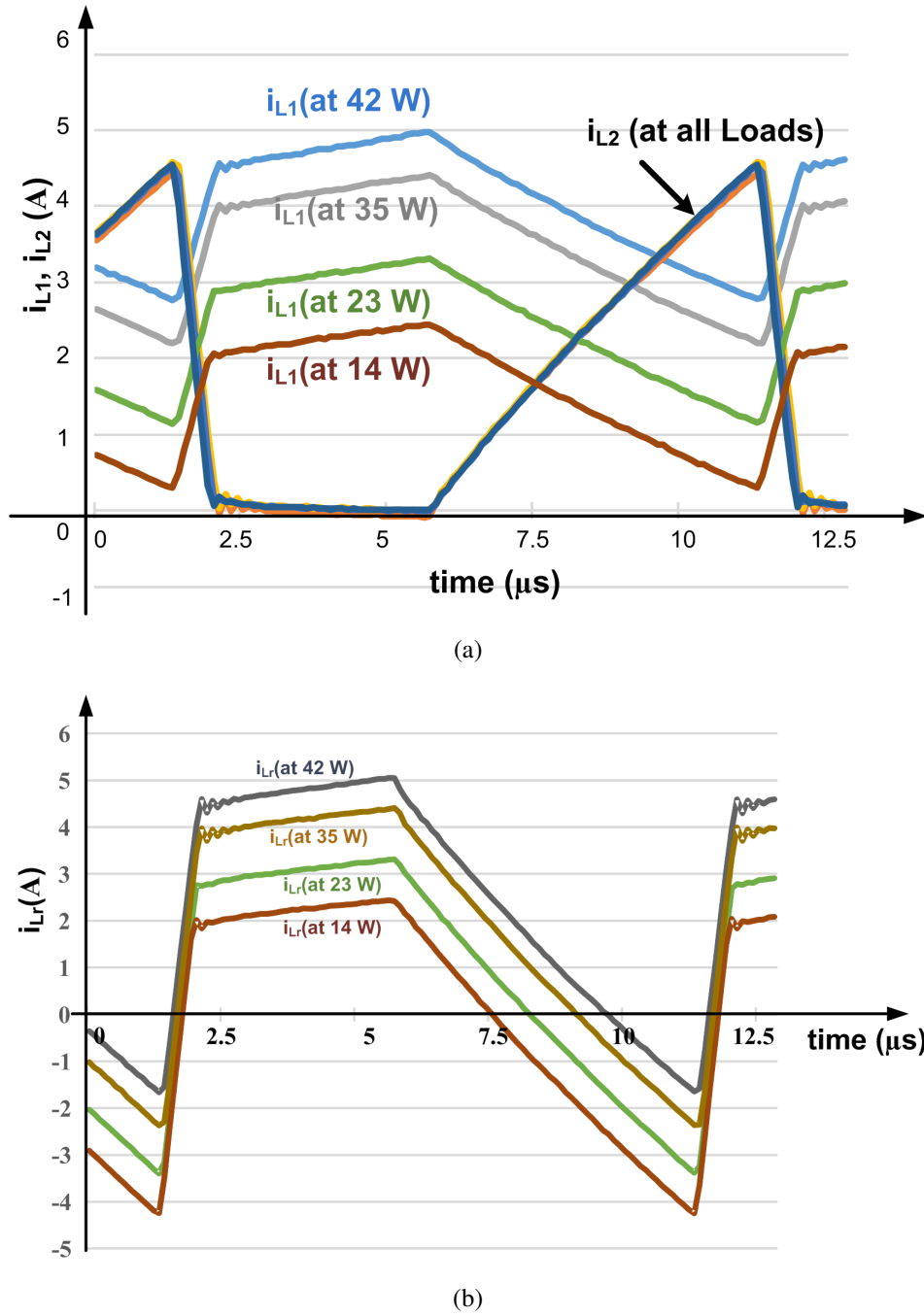


Figure 3.16: (a) Experimental waveforms of i_{L1} & i_{L2} at various LED loads (b) Resultant waveform, i_{Lr} obtained from i_{L1} & i_{L2}

and reduced switch peak currents.

The SPV system voltage is considered as 36 V and battery is to be charged to 26 V, thereby buck operation is essential. Fig. 3.17 to Fig. 3.19 show simulation & experimental waveforms of BSS charging from the SPV system in buck mode. Fig. 3.17 shows the voltage and current simulation and experimental waveforms of switches S_1 & S_2 . In this case also, ZVS

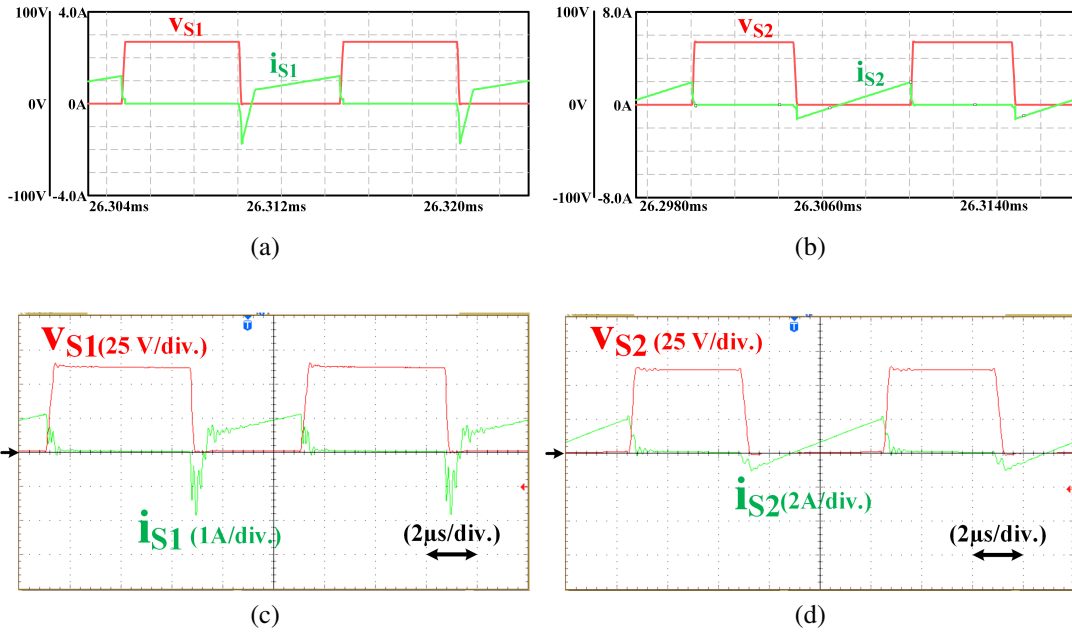


Figure 3.17: Simulation & experimental voltage and current waveforms of main switches of BDC in charging mode (buck operation): (a) Simulation waveforms of v_{S1} & i_{S1} (b) Simulation waveforms of v_{S2} & i_{S2} (c) Experimental waveforms of v_{S1} & i_{S1} (d) Experimental waveforms of v_{S2} & i_{S2}

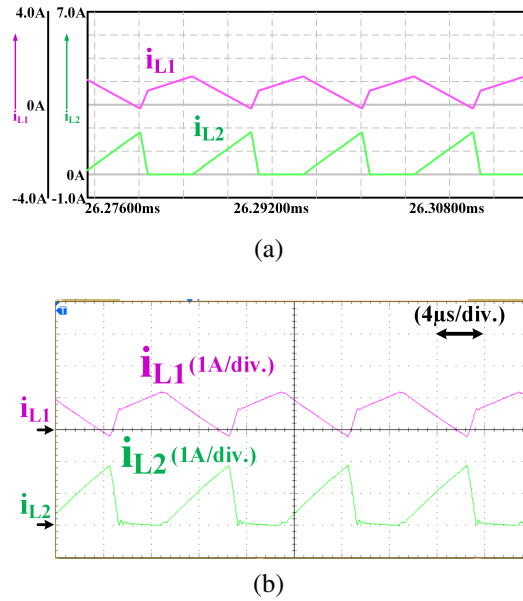


Figure 3.18: Simulation & experimental waveforms of inductor currents in charging mode (buck operation): (a) Simulation waveforms of i_{L1} & i_{L2} (b) Experimental waveforms of i_{L1} & i_{L2}

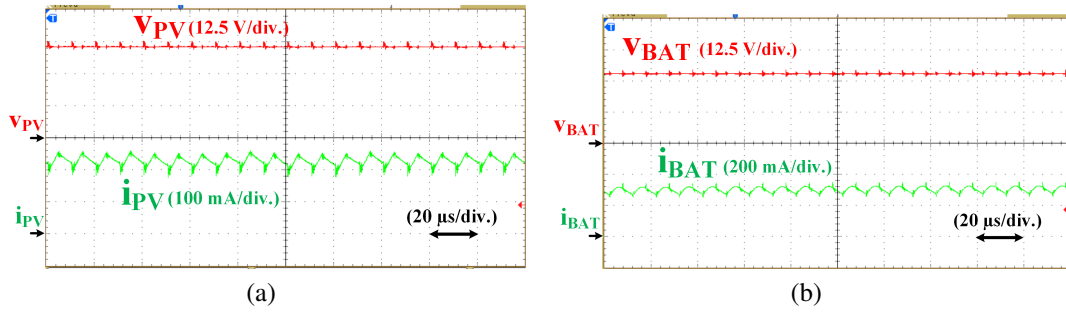


Figure 3.19: Experimental input & output waveforms of BDC in charging mode (buck operation) : (a) waveforms of v_{PV} & i_{PV} (b) waveforms of v_{BAT} & i_{BAT}

turn-ON is achieved and near ZVS turn-OFF condition is achieved. Fig. 3.18 shows simulation and experimental waveforms of CI winding currents i_{L1} and i_{L2} . It can be observed that there is a reduction in the peak current of i_{L2} , which reduces the recycling energy. Fig. 3.19 shows the experimental waveforms of the SPV system and the battery voltages and currents. The auxiliary switches used for soft switching do not have any switching losses. Hence, compared to hard switched BDC (83.2%), the efficiency of the proposed CI-BDC is high (86.78%).

3.4.3 Case 3: SPV System (18 V) to BSS Charging (26 V) in Boost Mode

A special case is considered for showing the advantage of CI-BDC having the capability of buck/boost modes in either direction. In this case, the SPV system voltage is considered as 18 V which is less than the battery charging voltage, hence boost operation is essential. Fig. 3.20 to Fig. 3.22 show the simulation & experimental results of this boost operation. Fig. 3.20 shows the voltage and current simulation & experimental waveforms of switches, S_1 and S_2 . ZVS operation can be observed in the waveforms. Fig 3.21 shows simulation & experimental waveforms of currents, i_{L1} and i_{L2} . The peak current of i_{L2} is less, which reduces the recycling energy and hence ZVS is achieved. The experimental **voltage** and current waveforms of the SPV and battery are shown in Fig. 3.22. The auxiliary devices are operated with no switching losses. Hence, the efficiency of the proposed CI-BDC during this operation (92.45%) is more than that of hard switched BDC (85.88%).

3.5 Dimming Control, Efficiency and Performance Analysis

3.5.1 Dimming

In the proposed CI-BDC, PWM dimming frequency is set as 250 Hz. The high frequency (100 kHz) PWM switching pulses are ANDed with a low dimming frequency (250 Hz) PWM

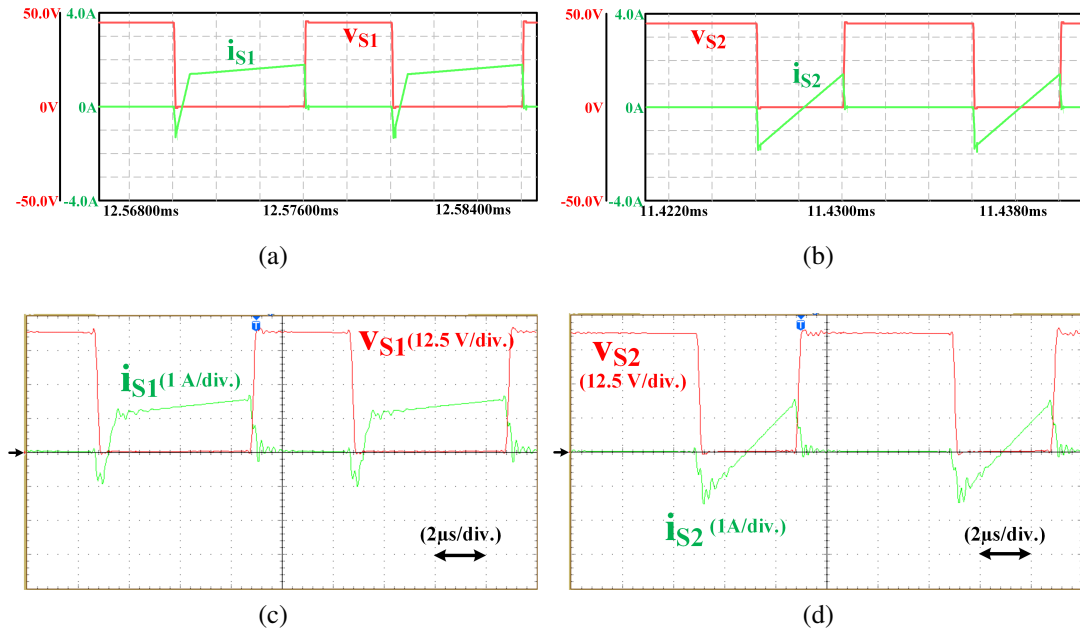


Figure 3.20: Simulation & experimental voltage and current waveforms of main switches of BDC in charging mode (boost operation): (a) Simulation waveforms of v_{S1} & i_{S1} (b) Simulation waveforms of v_{S2} & i_{S2} (c) Experimental waveforms of v_{S1} & i_{S1} (d) Experimental waveforms of v_{S2} & i_{S2}

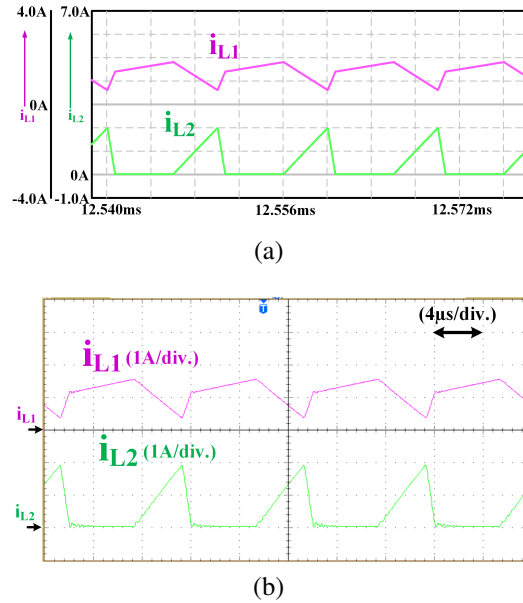


Figure 3.21: Simulation & experimental waveforms of inductor currents in charging mode (boost operation): (a) Simulation waveforms of i_{L1} & i_{L2} (b) Experimental waveforms of i_{L1} & i_{L2}

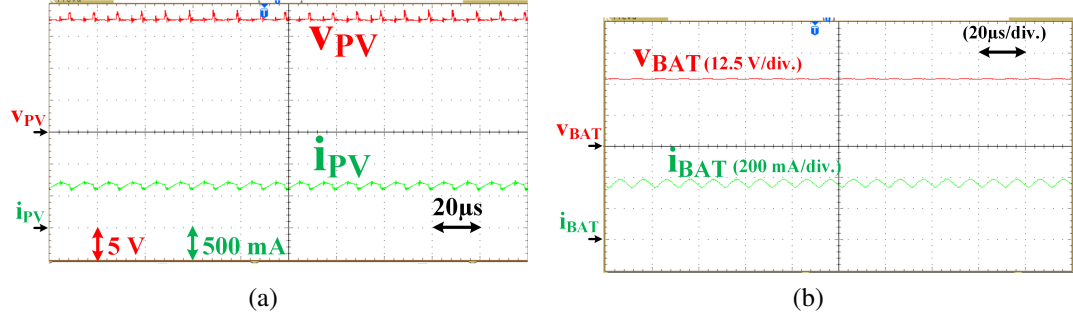


Figure 3.22: Experimental input & output waveforms of BDC in charging mode (boost operation) : (a) Waveforms of v_{PV} & i_{PV} (b) Waveforms of v_{BAT} & i_{BAT}

pulse, which controls the average LED current as shown in Fig. 3.23. δ_d , T_d are duty cycle and time period of dimming signal respectively. As per Energy Star Program Requirements Product Specifications for Luminaries (Light Fixtures) Version 2.1 (Effective date: March 15, 2018) the preferable dimming level is from (20% to 100%). Thus, by controlling δ_d from 20% to 100%, the average LED current is adjusted to control the illumination level. Fig. 3.24 shows the gate signals applied for main switches with dimming. Fig. 3.25a and Fig. 3.25c show simulation & experimental waveforms of LED voltage and current at 80% dimming. Fig. 3.25b and Fig. 3.25d show simulation & experimental waveforms of LED voltage and current at 40% dimming. The efficiency under dimming is also high with CI-BDC compared to hard switched BDC.

Table 3.2: Parameters of the devices

<i>Parameters</i>	<i>Values</i>	<i>Parameters</i>	<i>Values</i>
$V_{in} = V_{BAT}$	36 V	Q_{rr}	505 nC
$V_o = V_{LED}$	26 V	t_{rise}	35 ns
P_o	40 W	t_{fall}	35 ns
R_{DSon}	44 mΩ	R_{L1}, R_L	500 mΩ
C_{oss}	250 pF	R_{L2}	50 mΩ

3.5.2 Power Loss Analysis and Efficiency

Fig. 3.26a shows the waveforms of coupled inductor currents, i_{L1} & i_{L2} at full load in discharging condition. Fig. 3.26b shows the waveform of resultant current i_{Lr} , due to i_{L1} & i_{L2} which flows through the main switches. Fig. 3.16a and Fig. 3.16b show the waveforms of i_{L1} , i_{L2} and i_{Lr} at various loads. It can be observed that the DC component (average value) of i_{L1} and i_{Lr} vary as the load changes, whereas the AC component (peak to peak ripple) remains

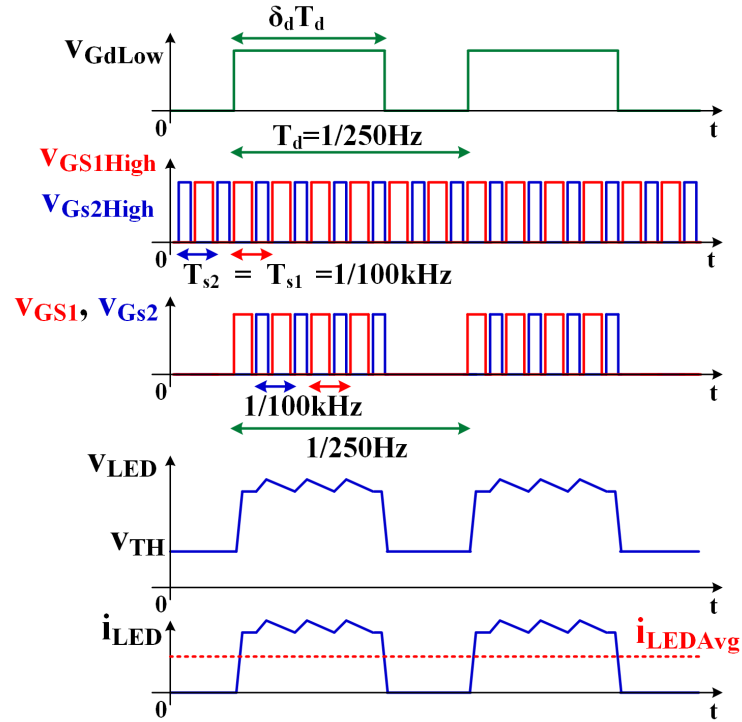


Figure 3.23: Schematic waveforms of switching signals generated using PWM dimming control and corresponding LED output voltage and current

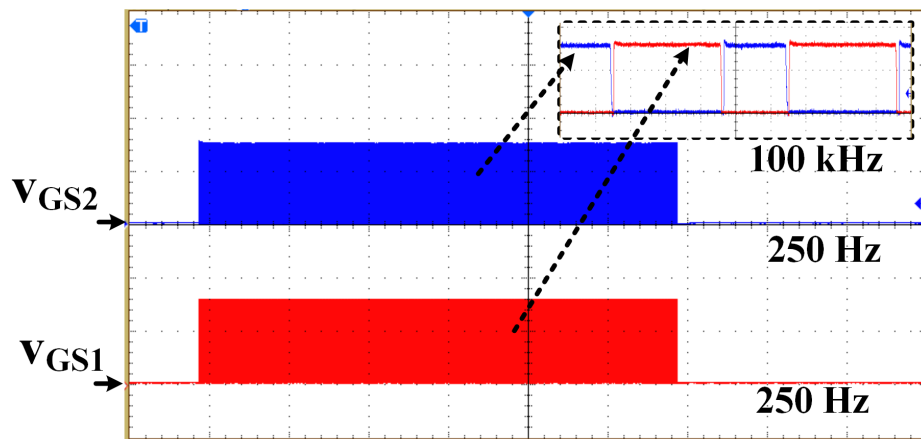


Figure 3.24: Experimental switching signals of main switches under dimming

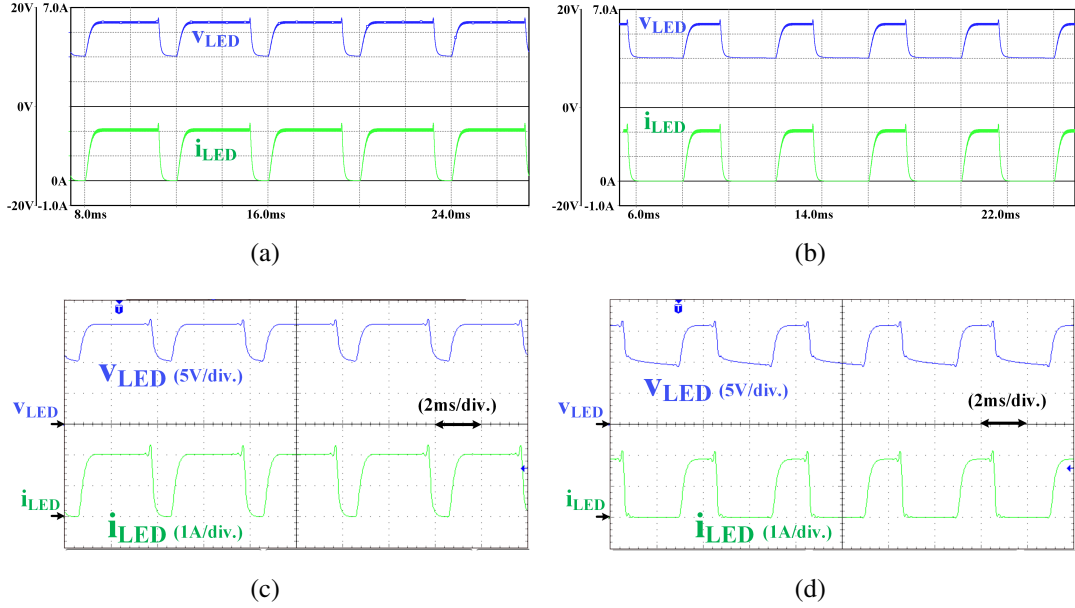
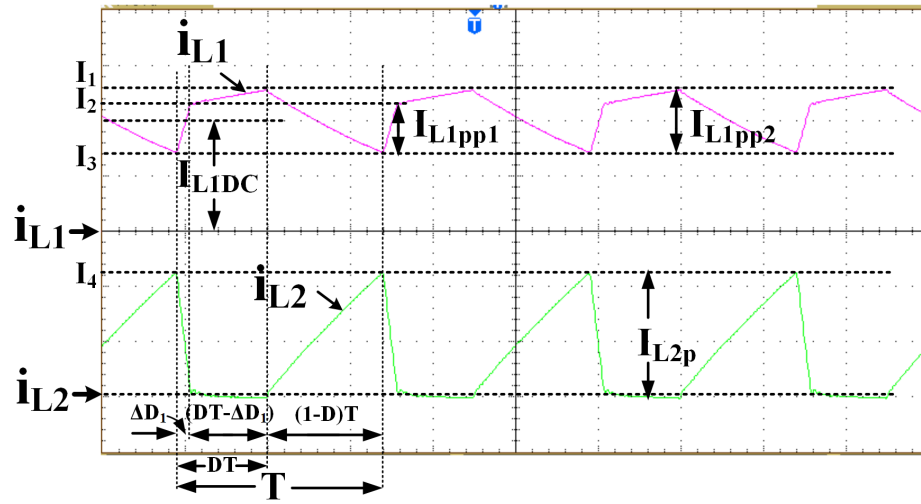


Figure 3.25: Simulation & experimental waveforms of v_{LED} & i_{LED} in discharging mode (a) Simulation waveforms at 80% dimming (b) Simulation waveforms at 40% dimming (c) Experimental waveforms at 80% dimming (d) Experimental waveforms at 40% dimming

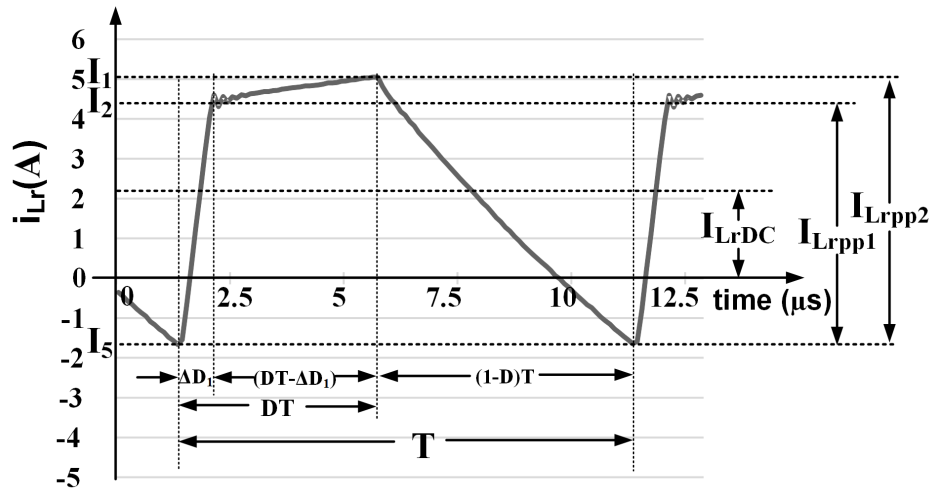
the same. i_{L2} remains constant irrespective of load variations. Hence the conduction losses in the auxiliary devices (S_{a1}/S_{a2} , D_{a1}/D_{a2} & L_2) and the AC conduction losses in the switches (S_1 , S_2) and the main inductor (L_1) are always constant irrespective of load. These losses can be called as constant losses. The DC conduction losses in switches (S_1 , S_2) and the main inductor (L_1) vary as the load changes and can be called as variable losses. At light load, the variable losses are less as the load is less, but the constant losses remain the same and thereby dominate the variable losses. This makes the converter efficiency reduced at light loads compared to the conventional converter. Hence, in order to have high efficiency at light loads, the proposed converter switches over to conventional hard switched converter by turning OFF the corresponding auxiliary switch. To know the exact change over point in terms of the fraction of load, below which the efficiency of the proposed converter reduces, loss analysis [95–97] of the proposed CI-BDC and conventional hard switched BDC is done as below.

The losses in main switches and main inductor are divided into AC and DC losses. Let the duration, $(t_5 - t_7)$ in Fig. 3.4 be ΔD_1 . At the end of this interval, both i_{L1} and i_{S1} reach the same value. Hence, ΔD_1 can be expressed as

$$\Delta D_1 = \frac{I_5 - I_3}{m_{L1.7} - m_{S1.7}} \quad (3.29)$$



(a)



(b)

Figure 3.26: (a) Experimental waveforms of i_{L1} & i_{L2} (b) Waveform of i_{Lr} obtained from i_{L1} & i_{L2}

Let $\Delta D_1 = T/t_f$ in Fig. 3.26, where $1/t_f$ is the fraction of total time period obtained as below.

$$t_f = \frac{1}{(f_{sw}\Delta D_1)} \quad (3.30)$$

By using (3.4), (3.6) and (3.19), I_5 can be determined from (3.31) below

$$I_5 = I_1 - m_{S2.4} \left(\frac{1-D}{f_{sw}} \right) \quad (3.31)$$

By using (3.4), (3.10), (3.12), (3.19) and (3.31), ΔD_1 is determined from (3.29).

I_2 is expressed as

$$I_2 = I_3 + \left(m_{L1.7} D_1 \right) \quad (3.32)$$

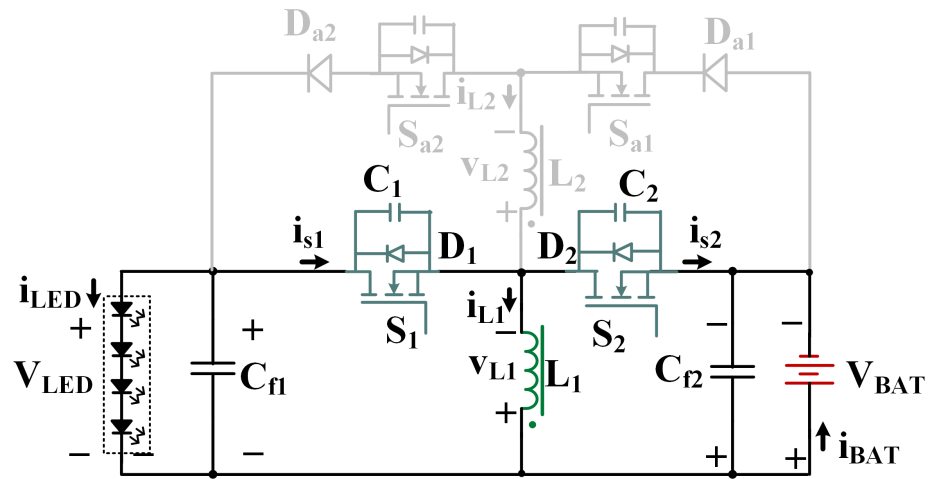
By using (3.32), (3.16), (3.19) and (3.31), the peak-peak currents mentioned in Fig. 3.26 are determined from (3.33) below.

$$\left. \begin{aligned} I_{L1pp1} &= I_2 - I_3; & I_{L1pp2} &= I_1 - I_3; & I_{L2p} &= I_4 \\ I_{swpp1} &= I_2 - I_5; & I_{swpp2} &= I_1 - I_5 \end{aligned} \right\} \quad (3.33)$$

For operating the proposed CI-BDC as conventional hard-switched BDC, the auxiliary circuit is disabled by turning OFF the auxiliary switches as shown in Fig. 3.27a. Now the circuit comprises of switches S_1 & S_2 , the main inductor L_1 only. Fig. 3.27b shows the schematic waveform of inductor current (i_{L1}) in the conventional hard-switched BDC. This current flows through both the switches (S_1 & S_2). This inductor current contains both AC and DC components. The AC component remains constant irrespective of load variations whereas DC component changes with variations in load.

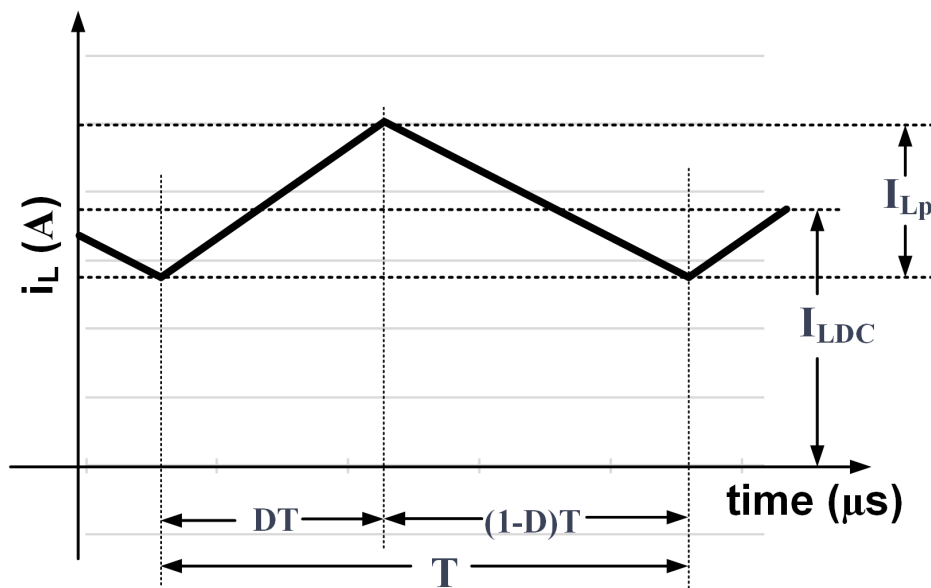
Table A in appendix-A shows the expressions for the total losses of proposed CI-BDC and conventional hard-switched BDC. To know the exact change over point in terms of the fraction of load, the total losses of proposed CI-BDC are compared with that of conventional hard-switched BDC as given in (3.34). At changeover point these losses are equal, hence

$$\left. \begin{aligned} &P_{swAC_SS} + P_{swDC_SS} + P_{swCA_SS} + P_{L1AC_SS} + P_{L1DC_SS} + P_{L2_SS} + P_{Sa_SS} + P_{Da_SS} \\ &= P_{swAC_HS} + P_{swDC_HS} + P_{swSW_HS} + P_{swRR_HS} + P_{swCa_HS} + P_{LAC_HS} + P_{LDC_HS} \end{aligned} \right\} \quad (3.34)$$



Power flow from Battery to LED lighting load

(a)



(b)

Figure 3.27: (a) Proposed CI-BDC as conventional hard-switched BDC (b) Schematic waveform of the inductor current in conventional hard-switched BDC

P_{swDC_SS} is further simplified in terms of load current as below.

$$\begin{aligned}
 P_{swDC_SS} &= I_{sw_Avg_SS}^2 R_{DSon} \\
 &= \left[\left(\frac{I_o}{1-D} \right) - \frac{I_{L2p}}{2} \left((1-D) + \frac{1}{t_f} \right) \right]^2 R_{DSon} \\
 &= P_A - P_{AB} + P_B
 \end{aligned} \tag{3.35}$$

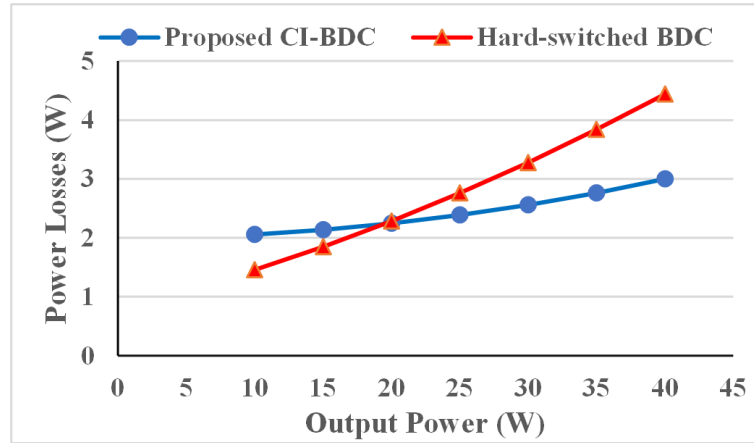


Figure 3.28: Theoretical power Loss curves of proposed CI-BDC and conventional BDC

where

$$P_A = (AI_o)^2 R_{DSon}; \quad P_B = B^2 R_{DSon}; \quad P_{AB} = 2ABI_o R_{DSon}$$

and

$$A = \frac{1}{(1-D)}; \quad B = \frac{I_{L2p}}{2} \left((1-D) + \frac{1}{t_f} \right)$$

Substitute (3.35) in (3.34).

Let current at any load be xI_o where x is the fraction of load that ranges from 0 to 1 and I_o is the full load current. For any load, (3.34) can be expressed as below.

$$\left. \begin{aligned} &P_{swAC_SS} + x^2 P_A - x P_{AB} + P_B + P_{swCA_SS} + P_{L1AC_SS} + x^2 P_{L1DC_SS} + P_{L2_SS} + P_{Da_SS} \\ &= P_{swAC_HS} + x^2 P_{swDC_HS} + x P_{swSW_HS} + P_{swRR_HS} + P_{swCa_HS} + P_{LAC_HS} + x^2 P_{LDC_HS} \end{aligned} \right\} \quad (3.36)$$

After rearranging the above equation and solving for x , we get change over point in terms of the fraction of load as

$$x = -\frac{a}{b} \quad (3.37)$$

where

$$\begin{aligned} a &= P_{swAC_SS} + P_B + P_{swCA_SS} + P_{L1AC_SS} + P_{L2_SS} + P_{Sa_SS} + P_{Da_SS} \\ &\quad - P_{swAC_HS} - P_{swRR_HS} - P_{swCa_HS} - P_{LAC_HS} \\ b &= -P_{AB} - P_{swSW_HS} \end{aligned}$$

Table 3.2 shows the parameters of the proposed CI-BDC. The inductance (L) in hard-switched BDC is same as main inductance (L_1) of CI-BDC. Based on Table 3.1 & Table 3.2, the losses of proposed CI-BDC and hard-switched BDC in discharging mode are found theoretically for various loads and illustrated, as shown in Fig. 3.28. It can be observed that the CI-BDC results in reduced losses as compared with hard-switched BDC for higher load con-

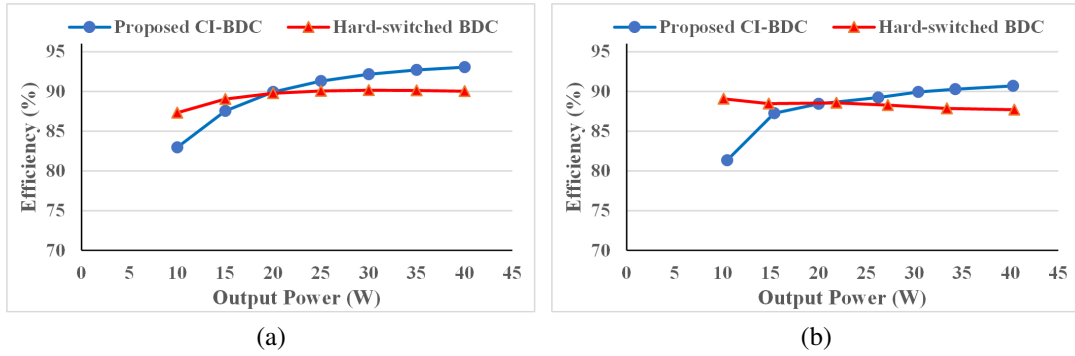


Figure 3.29: Efficiency curves of proposed CI-BDC and conventional BDC (a) Theoretical (b) Experimental

ditions. Fig. 3.29a shows the comparison of theoretical efficiencies of the CI-BDC and the conventional BDC. At moderate and higher load conditions, CI-BDC provides high efficiency compared to conventional BDC. However, in order to improve efficiency at light load conditions, the auxiliary switches can be turned OFF; thus, the CI-BDC operates with conventional hard switching during which conduction losses are less. This change over point obtained theoretically is 0.4697 from (3.37). Fig. 3.29b shows the comparison of experimental efficiency curves of the CI-BDC and conventional counterpart. The change over point is found as 0.475 experimentally. As can be observed, experimental and theoretical efficiencies are similar, except that the practical efficiencies are little less than the theoretical efficiencies as there will be other losses like core losses, driver losses, etc. which are not considered in theoretical power loss analysis. Hence by using (3.34), the changeover point in terms of the fraction of load can be predetermined and therefore, through suitable control technique, the proposed CI-BDC can be switched over to conventional hard-switched BDC in order to have high efficiency at light loads also.

3.5.3 Comparative Study

Table 3.3 shows the comparison of the proposed configuration with the existing soft switched bidirectional configurations [21, 22, 32–34, 41]. In [21] and [22], the main inductors used should be of low value such that they allow negative current to achieve soft switching, but the ripple content is increased and the conduction losses are also increased. In [22], no additional auxiliary device is used for soft switching. However, in order to reduce the ripple content of the load current, a three-phase interleaved circuit is employed, which increases the conduction losses and the component count. In [32], ZVT is used to minimize conduction losses and improve efficiency. However, the control is complex. Even though [33, 41] does

Table 3.3: Comparison between different soft-switched bi-directional configurations

ZVS converters		Ref. [22]	Ref. [21]	Ref. [32]	Ref. [33]	Ref. [34]	Proposed CI-BDC
Inductors		3	2	2	2	2	2
Magnetic core component		3	2	2	2	2	1
Main Inductor ripple current		Large	Large	Small	Medium	Small	Small
Nominal Inductor (Main-M, Aux.-A) Peak Currents (p.u)	M	4.01	2	3.8	2	2.33	2.3
	A	—	—	1.875	—	2.5	1.91
Switches (S) and diodes (D) (Main + auxiliary, A)	S	6	$2+1A=3$	$2+2A=4$	8	$4+1A=5$	$2+2A=4$
	D	—	—	—	—	1A	2A
Operating Mode (Charge-C, Discharge-D)	C	Buck	Boost	Buck	Buck/Boost	Buck/Boost	Buck/Boost
	D	Boost	Buck	Boost	Buck/Boost	Buck/Boost	Buck/Boost

not require any auxiliary device for soft switching, the number of components required is more as they use multi-phase concept. The circulating current and individual phase ripple will be large, that increases the losses across the devices. In [34], the synchronous non-inverting buck-boost converter is soft switched by sharing the auxiliary devices for both directions of power flow. More switches are required in [34] compared with proposed topology. There are 4 main switches in the non-inverting buck-boost topology compared with the proposed topology which contains only 2 main switches. As all these main switches operate continuously, the conduction losses are more in [34]. Also, topologies in [21, 33, 34, 41] require closed-loop control, which makes the control complex and thus increases the cost. The proposed CI-BDC inductor peak currents are also compared in the table and it can be observed that they are within limits. The two auxiliary switches along with main switches in the proposed CI-BDC are floating in nature. Even though the cost is increased due to auxiliary components and floating gate drivers, when compared with existing solutions [21, 22, 32–34], it can be observed that the proposed CI-BDC requires only a single inductor core. This reduces the cost considerably. Compared to the existing topologies, the proposed CI-BDC also provides the benefits like buck/boost modes in

Table 3.4: Comparison between two-stage and proposed single-stage converter for the LED-SLS

PV fed LED Street Lighting Topologies		Integrated Two Stage converter [13]	Proposed Single Stage CI-BDC
Converters	Charging	Sepic	Single bidirectional Buck-Boost converter
	Discharging	Forward	
Components	Switches, Diodes	2, 2	4, 2
	Inductors, Transformers	2, 1	1, 0
	Capacitors	6	4
Maximum Efficiency	Charging (%)	88.1	92.45
	Discharging (%)	90.4	90.68
Operating Modes	Charging	Buck / Boost	Buck / Boost
	Discharging	Either Buck or boost mode only	Buck / Boost
Device Operation	Charging	Hard Switched	Soft switched
	Discharging	Soft Switched	Soft switched

either direction, soft switching across all devices in either direction, compact size due to single magnetic core of CI, reduced ripple current, high efficiency at all loads and simple control. Owing to these overall benefits provided by the proposed CI-BDC, cost of auxiliary components and floating gate drivers is less significant. The additional inductor used during charging is not considered in the comparison as its presence is not necessary if a battery of high rating is used.

A conventional two-stage converter in PV fed LED-SLS generally employs two separate converters for charging and discharging. The proposed CI-BDC is used as a single-stage converter in the LED-SLS along with one extra relay as a change-over switch between charging and discharging conditions. Table 3.4 shows the comparison of the proposed single-stage CI-BDC with two-stage converter [13] for PV fed LED-SLS. The two-stage converter uses a hard-switched Sepic converter for charging the battery from PV source during daytime and uses a soft switched active-clamp forward converter for discharging the battery to LED lighting during nighttime. Also, two electronic switches are used other than the regular switching devices to select the charging and discharging modes. The efficiency of the two-stage converter with hard

switching is 85% during charging and with snubber circuit, it is 88.1%, whereas the proposed single-stage CI-BDC has an efficiency of 86.78% in buck mode and 92.45% in boost mode. The efficiency of the two-stage converter in discharging mode is 90.4% and the efficiency of the proposed CI-BDC is 90.68%. As with existing two-stage converter, in the proposed CI-BDC also the relay losses have not been considered in efficiency calculation. The relay switching losses need not be considered as the relay toggles only twice a day. However, the relay has conduction losses during charging or discharging operation. The effect of efficiency has been analyzed with two different change over switches as below:

The relay 'SONGLE RELAY ISO9002 SRD' has a coil power consumption of 0.36 W and coil resistance of 0.1 ohms. If it is considered for analysis, the conduction losses may reduce the efficiency of the proposed CI-BDC by 0.1% to 2% depending on the mode of operation and the current flowing in the relay. A toggle switch can be used instead of a relay. The toggle switch '2M1-SP4-T1-B1-M1QE' has 10 milli ohms as contact resistance. If it is considered for analysis, the efficiency may be reduced by 0.005% to 0.2%. The effect of conduction losses on efficiency due to change over switch can be minimized by using a toggle switch. Also, the existing two-stage converter efficiency in [13] is measured at 100 W. If the proposed converter is also tested at same power level, the efficiency will still increase as the conduction losses are not considerably increased in proportion with the increase in wattage. The proposed single-stage CI-BDC has the following advantages compared with two-stage converters in the LED-SLS: reduced converter stages and hence reducing the component count, buck/boost modes in either direction of power flow, reduced device density because of high switching frequency, soft switching across all devices including auxiliary circuit devices.

3.6 Summary

In this chapter, a novel soft switched CI-BDC has been proposed for single stage SPV fed BSS assisted LED-SLS which provides ZVS and operates in buck/boost modes in either direction of power flow. The BSS gets charged through proposed CI-BDC from the SPV source during daytime, while the same CI-BDC discharges the stored power in BSS to the LED load during nighttime. The principle & modes of operation, analysis and design procedure are presented. BDC operation in buck/boost mode is simulated and tested for charging condition using programmable DC source as a SPV system. Also, BDC operation in buck mode is simulated and tested for discharging mode with the LED lighting system. A prototype of 40 W LED driver is built and tested experimentally. The simulation and experimental results are in good agreement with each other. In addition, LED dimming is implemented using PWM technique and simulated and tested for 40% and 80% dimming conditions. The efficiency of proposed

CI-BDC is measured and compared with the conventional hard switched counterpart for various load conditions. The proposed single-stage CI-BDC has an efficiency of 86.78% in buck mode and 92.45% in boost mode. Also, the proposed configuration is compared with two-stage LED SLS and with soft-switched BDCs. Compared to the existing topologies, the proposed CI-BDC also provides the benefits like buck/boost modes in either direction, soft switching across all devices including auxiliary circuit devices, compact size due to single magnetic core of CI, reduced ripple current, high efficiency at all loads and simple control.

Chapter 4

High Gain LED Driver for Multiple Load LED Lighting Systems

Chapter 4

High Gain LED Driver for Multiple Load LED Lighting Systems

4.1 Introduction

The conventional resonant converter based LED drivers have become popular due to their advantages like soft switching, high power density, high efficiency at all loads, etc., but they are unable to provide high gain for PV/Battery fed applications with reduced component count. Thus, there is a requirement of resonant converter based LED drivers that are suitable for PV/Battery fed applications overcoming the above drawbacks. LED drivers that can drive multiple loads are in need these days due to the multi-usage of LED lamps in every system. Independent control of these LED lamps and independent dimming are the essential features for these drivers. Many multiple load LED drivers are available in the literature. However, they suffer from one or more of the following limitations: lack of high gain, cannot drive equal voltage LED loads, cannot provide individual voltage regulation, cannot provide independent dimming control, etc. Hence, in this second work, a new buck-boost integrated high gain non-isolated symmetrical half-bridge resonant converter based LED driver for multiple loads (BBI-HBSRC-ML) is proposed which overcomes the above drawbacks. The proposed configuration is the integration of a synchronous buck-boost converter and half-bridge series LC resonant converter. It provides the same voltage gain as that of the full-bridge converter using less number of switches with effective utilization of switching devices and source voltage. The proposed configuration can be extended for multiple loads which provides advantages such as [the ability](#) to drive multiple loads with equal or unequal voltages/wattages, independent dimming control, etc. Thus, the proposed converter is best suitable for SPV or battery source fed multiple LED Lighting systems (LED-LS). The duty cycle is limited to 50% in order to achieve symmetrical operation and to ensure ZVS operation. To provide output voltage regulation against variations in the battery or SPV source voltage, frequency modulation has been implemented. In addition, [the illumination](#) level of LED lighting is controlled using pulse width modulation (PWM) dimming in which the average LED current is regulated without affecting the LED characteristics. This

proposed converter configuration is described in detail in section 4.2. Section 4.3 explains its operating principle and analysis. The design procedure is discussed in section 4.4. Simulation and practical results are discussed in section 4.5. Section 4.6 discusses about voltage regulation and dimming techniques. In section 4.7, the efficiency analysis and performance evaluation are discussed and the conclusion is presented in section 4.8.

4.2 Proposed Converter Configuration

The circuit diagram of the proposed synchronous buck-boost integrated half-bridge series resonant converter based LED driver with a single load is shown in Fig. 4.1a, where S_1 and S_2 are MOSFET switches, L_r & C_r are series resonant elements, and C_{BB} & L_{BB} are buck-boost capacitor & buck-boost inductor, used under buck-boost operation. The supply voltage of the converter is V_{DC} . V_{BB} is the buck-boost output voltage obtained due to buck-boost operation. $i_{L_{BB}}$ & i_r are the currents flowing in L_{BB} and resonant elements respectively. \bar{v}_{A1-O} & \bar{v}_{A2-O} are respectively the input and output voltages of the resonant tank. The LED load output voltage and output current are represented by V_O & I_O respectively. The proposed configuration with two loads is shown in Fig. 4.1b, where additionally two more switches and one rectifier are added for the second load. An inherent dimming capability is available for Load-2. But for dimming control in Load-1, an external dimming switch, S_D is added in series with the output as shown in Fig. 4.1b. Thus, independent dimming control is possible with two loads. The proposed configuration can be extended for multiple (n) loads as shown in Fig. 4.1c where independent dimming and output regulation are possible. The key waveforms of the proposed configuration with a single load as well as two loads are shown in Fig. 4.2.

4.3 Operating Principle and Analysis

The principle of operation and analysis are similar for both single load and multiple load configurations. Hence, only a single load operation is described in the following section.

4.3.1 Operating Principle

The proposed buck-boost integrated half-bridge converter is operated with a 50% duty cycle, thus provides an output voltage V_{BB} same as input voltage V_{DC} . Having two equal voltages of V_{BB} & V_{DC} , the symmetrical half-bridge resonant converter produces an output voltage (V_O) of twice that of conventional half-bridge counterpart. Fig. 4.2a illustrates the key waveforms of the proposed configuration, where V_{g1} & V_{g2} are the gate voltages applied to the half-bridge converter, which results in a symmetrical resonant current. The resonant current is rectified with

full-bridge rectifier and after filtering, it is applied to the LED load. Due to series resonance, ZVS turn ON is achieved across the switches S_1 & S_2 , which leads to reduced switching losses and increased efficiency. With the integrated buck-boost operation, the proposed half-bridge

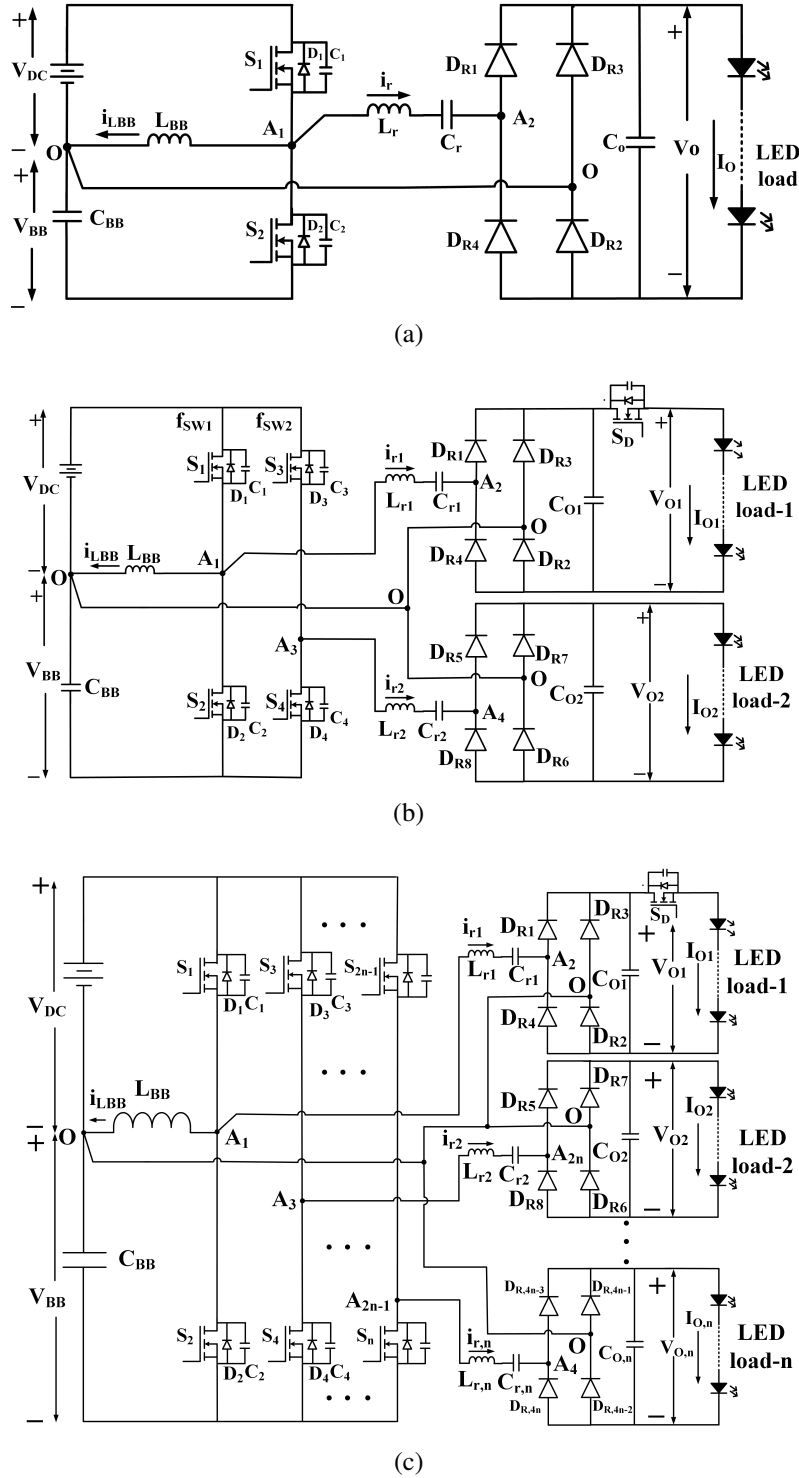


Figure 4.1: Proposed LED driver for (a) Single load (b) Two loads (c) Multiple loads

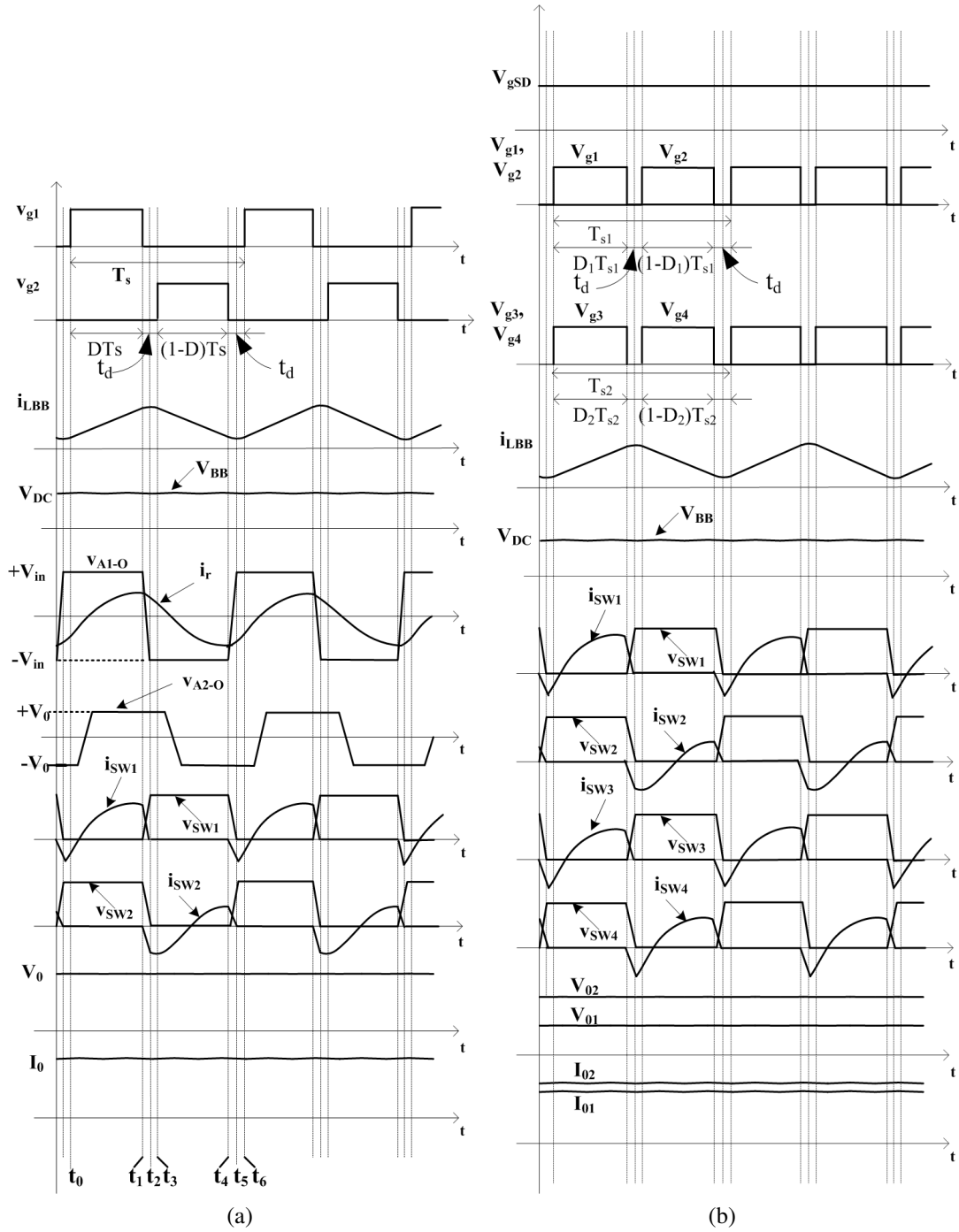


Figure 4.2: Key waveforms of proposed configuration for: (a) Single load (b) Two loads

converter can produce an output voltage equal to that of a full-bridge resonant converter with reduced switch count.

The operating **intervals** of the proposed configuration are shown in Fig. 4.3 and discussed as follows:

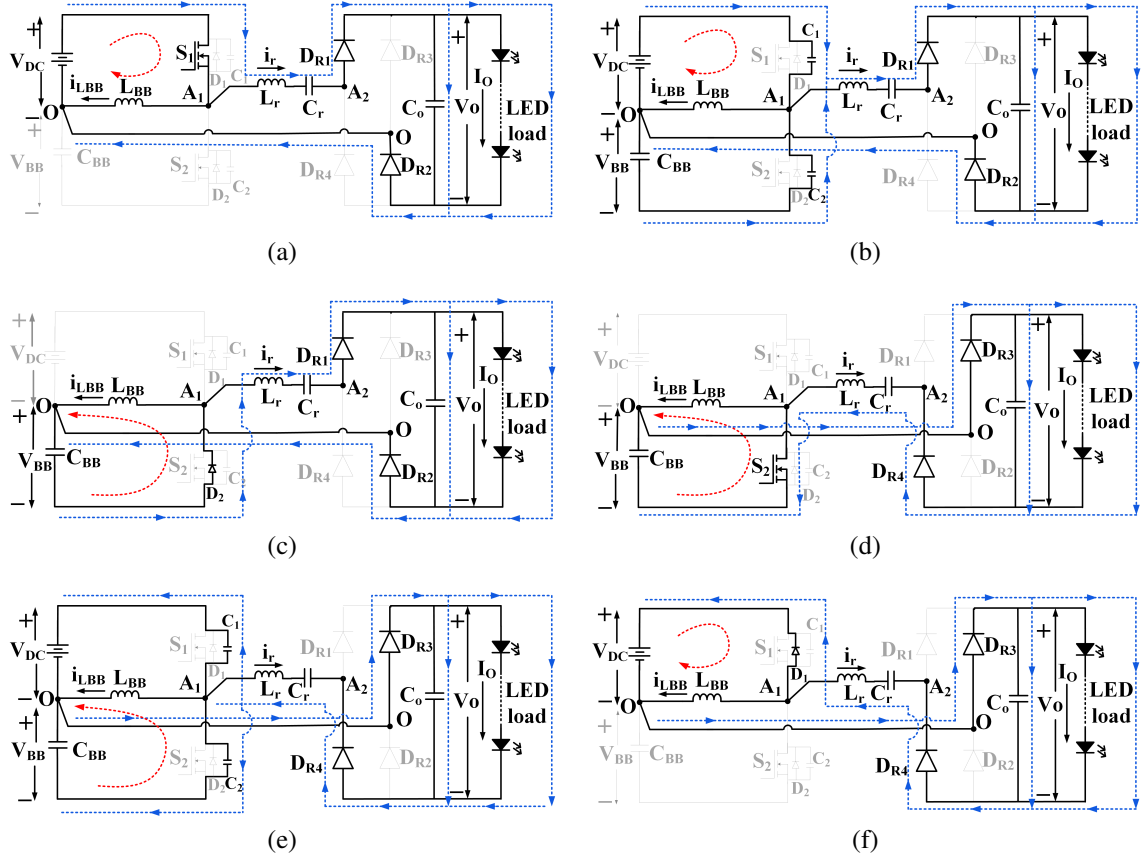


Figure 4.3: Various intervals of operation of proposed converter with single load configuration: (a) Interval-1 (b) Interval-2 (c) Interval-3 (d) Interval-4 (e) Interval-5 (f) Interval-6

4.3.1.1 Time Interval-1 [t_0 - t_1]

Prior to this **interval**, diode D_1 was in conduction and hence the voltage across S_1 is zero. The gate pulse provided at t_0 ; makes S_1 turn-ON with ZVS condition as illustrated in Fig. 4.3a. Buck-boost inductor, L_{BB} gets magnetized and current, i_{LBB} raises linearly. The resonant current, i_r continues to increase in the positive direction. The total current flowing in the switch, S_1 is given as

$$i_{S1} = i_{LBB} + i_r \quad (4.1)$$

At the end of this **interval**, i_{LBB} reaches to its maximum value given by

$$i_{LBB,max} = I_L + \frac{\Delta i_L}{2} \quad (4.2)$$

and i_r is obtained as

$$i_r(t_1) = \left(\frac{\pi}{2}\right) I_O \sin(\omega t_1 - \phi) \quad (4.3)$$

where

$$\phi = \tan^{-1} \left(\frac{X_{Lr} - X_{Cr}}{R_{ac}} \right) \quad (4.4)$$

R_{ac} is the non-linear output resistance offered by the rectifier and X_{Lr} , X_{Cr} are the reactances offered by L_r , C_r respectively which are expressed as

$$\left. \begin{aligned} X_{Lr} &= 2\pi f_s L_r \\ X_{Cr} &= \frac{1}{2\pi f_s C_r} \\ R_{ac} &= \frac{8}{\pi^2} R_O \end{aligned} \right\} \quad (4.5)$$

where R_O is the LED output resistance.

Hence, the current i_{S1} , at the end of this **interval**, is given by

$$i_{S1}(t_1) = i_r(t_1) + i_{LBB_max} \quad (4.6)$$

This **interval** ends when switch S_1 is turned OFF.

4.3.1.2 Time Interval-2 [t_1 - t_2]

When S_1 is turned OFF at $t = t_1$, C_1 starts charging and C_2 starts discharging. Resonance occurs between the capacitors and inductors L_r & L_{BB} . This duration is very short; hence, i_r is assumed to be constant and the capacitors C_1 and C_2 carry half of the currents of i_r & i_{LBB} as illustrated in Fig. 4.3b. This **interval** ends at $t = t_2$ when C_1 and C_2 are completely charged and discharged respectively.

4.3.1.3 Time Interval-3 [t_2 - t_3]

At $t = t_2$, as C_2 is completely discharged to zero, D_2 becomes forward biased. The total time duration of **interval-2** and **interval-3** together constitute the dead time. The buck-boost inductor, L_{BB} starts demagnetizing. Therefore, the current i_{LBB} decreases linearly and i_r starts decreasing. The resultant negative current due to the sum of i_{LBB} and i_r , flows through D_2 as illustrated in Fig. 4.3c. This **interval** ends when gate pulse is provided to S_2 at $t = t_3$.

4.3.1.4 Time Interval-4 [t_3 - t_4]

Prior to **interval-4**, diode D_2 was in conduction and hence the voltage across S_2 is zero. The gate pulse provided at t_3 ; makes S_2 turn-ON with ZVS condition. The current i_{S2} is the resultant of the two currents, i_{LBB} and i_r as illustrated in Fig. 4.3d. At the end of this **interval**, the current i_r

reaches to negative value given by $i_r(t_4) = -i_r(t_1)$ and i_{LBB} reaches to its minimum value given by

$$i_{LBB.min} = I_L - \frac{\Delta i_L}{2} \quad (4.7)$$

Hence, the current i_{S2} , at the end of this **interval**, is given by

$$i_{S2}(t_4) = -[i_r(t_4) + i_{LBB.min}] \quad (4.8)$$

This **interval** ends when S_2 is turned OFF at $t = t_4$.

4.3.1.5 **Time Interval-5** [t_4 - t_5]

At t_4 , when S_2 is turned OFF, C_1 discharges and C_2 charges as shown in Fig. 4.3e. Resonance occurs between capacitors and inductors for a short duration of t_4 - t_5 . The resultant current is assumed constant in this short duration and is shared equally by the capacitors C_1 and C_2 , as illustrated in Fig. 4.3e. This **interval** ends at $t = t_5$ when C_1 and C_2 are completely discharged and charged respectively.

4.3.1.6 **Time Interval-6** [t_5 - t_6]

At $t = t_5$, C_1 is completely discharged; hence, D_1 starts conducting, as shown in Fig. 4.3f. The buck-boost inductor starts magnetizing. Therefore, i_{LBB} increases linearly and the current i_r starts increasing from negative value. The resultant of the two currents, i_{LBB} & i_r , flows through D_1 as illustrated in Fig. 4.3f. The total duration of **interval-5** and **interval-6** constitutes the dead time. This **interval** ends when the gate pulse is provided to switch S_1 at $t = t_6$.

4.3.2 Analysis of Proposed Converter

The assumptions considered for the analysis are as follows:

- The converter operates in steady mode.
- Power MOSFETs and diodes are ideal.
- LED parameters remain constant.

With 50% duty cycle, the integrated buck-boost operation results in $V_{BB} = V_{DC}$. Hence, the input voltage developed across the half-bridge inverter is $V_{in} = V_{DC} + V_{BB} = 2V_{DC}$. This results a square wave voltage, with a peak value of V_{DC} , from the inverter, which is the input voltage \bar{V}_{A1-O} across $L_r - C_r$ network. The static gain of the proposed resonant converter can

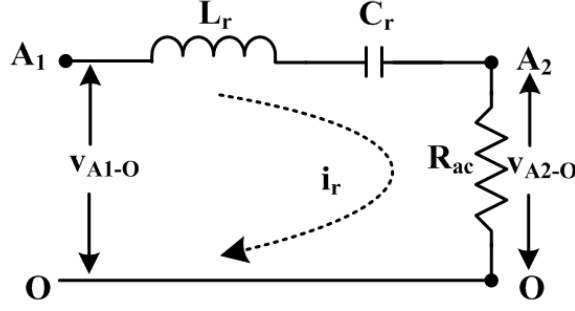


Figure 4.4: AC equivalent circuit

be obtained using conventional ac analysis in [98]. The ac equivalent circuit of the resonant tank is shown in Fig. 4.4.

From Fig. 4.4, the static gain of the resonant tank is expressed as:

$$\frac{\bar{V}_{A2-O}}{\bar{V}_{A1-O}} = \frac{R_{ac}}{R_{ac} + j(X_{Lr} - X_{Cr})} \quad (4.9)$$

where \bar{V}_{A1-O} and \bar{V}_{A2-O} are input and output **RMS** voltages of the resonant network respectively.

The static voltage gain of the proposed converter, in terms of converter parameters, can be expressed as

$$\frac{V_O}{V_{DC}} = \frac{1}{\left[1 + j \left(\frac{X_{Lr} - X_{Cr}}{R_{ac}} \right) \right]} \quad (4.10)$$

Quality factor (Q) that measures the sharpness in the current can be defined as

$$Q = \frac{\omega_r L_r}{R_{ac}} = \frac{1}{\omega_r C_r R_{ac}} \quad (4.11)$$

The angular resonant frequency ω_r is given by

$$\omega_r = 2\pi f_r = \frac{1}{\sqrt{L_r C_r}} \quad (4.12)$$

where f_r is resonant frequency in Hz. By substituting (4.5) and (4.11) into (4.10), the gain is obtained as

$$\frac{V_O}{V_{DC}} = \frac{1}{\left[1 + j \frac{\pi^2}{8} Q \left(\frac{f_s}{f_r} - \frac{f_r}{f_s} \right) \right]} \quad (4.13)$$

The duty ratio, D is expressed as

$$D = \frac{|V_{BB}|}{V_{DC} + |V_{BB}|} \quad (4.14)$$

The average source current can be approximated in terms of average inductor and resonant currents as

$$I_{DC} \approx (I_{LBB} + I_r) \approx I_{LBB} \quad (4.15)$$

For 100% efficiency,

$$\begin{aligned} V_{DC}I_{DC} &= V_O I_O \\ &= \frac{V_O^2}{R_O} \\ \text{Hence, } I_{DC} &= \frac{V_O^2}{V_{DC}R_O} \end{aligned} \quad (4.16)$$

The minimum current in L_{BB} , I_{LBBmin} can be expressed as

$$I_{LBBmin} = I_{LBB} - \frac{\Delta i_{LBB}}{2} \quad (4.17)$$

where Δi_{LBB} can be expressed as

$$\Delta i_{LBB} = \frac{V_{DC}DT}{L_{BB}} \quad (4.18)$$

Thus, by substituting (4.15), (4.16) & (4.18) in (4.17) and making $I_{LBBmin}=0$, the critical inductance of buck-boost inductor, L_{BBcrit} is expressed as

$$L_{BBcrit} = \frac{V_{DC}^2 D R_O}{2 V_O^2 f_s} \quad (4.19)$$

where f_s is the switching frequency.

For continuous inductor current, $L_{BB} > L_{BBcrit}$.

For two loads, $D_1 = D_2 = 50\%$ and I_{DC} in (4.16) is modified as

$$\begin{aligned} V_{DC}I_{DC} &= V_{O1}I_{O1} + V_{O2}I_{O2} = \frac{V_{O1}^2}{R_{O1}} + \frac{V_{O2}^2}{R_{O2}} \\ \text{Hence, } I_{DC} &= \frac{V_{O1}^2 R_{O2} + V_{O2}^2 R_{O1}}{V_{DC} R_{O1} R_{O2}} \end{aligned} \quad (4.20)$$

Thus, L_{BBcrit} for two loads can be expressed as

$$L_{BBcrit} = \frac{V_{DC}^2 D_1 R_{O1} R_{O2}}{2(V_{O1}^2 R_{O2} + V_{O2}^2 R_{O1})f_{s1}} \quad (4.21)$$

4.4 Design Considerations

TMX HP3W white LEDs are used in the experimental prototype. The threshold voltage of each LED is 2.321 V. In order to realize the LED lamp of 22.77 W, 22.505 V with a current of 1.012 A and having a threshold voltage of 16.247 V, the operating point of LED is selected as 3.215 V and 506 mA. Thus, the total LED load comprises of two LED strings in parallel where each string contains seven LEDs in series.

4.4.1 Selection of Input DC Voltage, V_{DC}

The input voltage, V_{DC} for the converter is chosen as 48 V. Hence, to obtain the required V_o of 22.5 V with V_{DC} of 48 V, the Q-factor, frequency ratio are selected as 4.14 and 1.2 respectively in a similar way that discussed in Chapter-5 at section-5.4.2, from the graph between output voltage and frequency ratio at different Q values.

4.4.2 Calculation of L_{BB}

By using (4.14) and (4.19), the inductance L_{BBcrit} is calculated, and to maintain the continuous conduction and reduced peak current in switches, inductance L_{BB} is chosen higher than L_{BBcrit} as 120 μH .

4.4.3 Calculation of Resonant Elements

The product of L_r and C_r is obtained from (4.12) and it is expressed as

$$L_r C_r = \left[\frac{1}{2\pi f_r} \right]^2 \quad (4.22)$$

With f_s of 200 kHz and the ratio f_s/f_r as 1.2, (4.22) can be expressed as

$$L_r C_r = 0.91344 \times 10^{-12} \quad (4.23)$$

From (4.23) and (4.11), the elements L_r and C_r are obtained as 88 μH and 10.31 nF, respectively.

Further, the proposed configuration is also extended and tested for two different LED loads with Load-1 of 22.5 W and Load-2 of 43 W. The schematic of the extended two load configuration is illustrated in Fig. 4.1b and its design is similar to the single load configuration. The first load considered is the same load which is used in the single load configuration. In order

Table 4.1: Design parameters

	Parameters	Values for Single Load	Values for Two loads
Input	DC input Voltage	$V_{DC} = 48 \text{ V}$	$V_{DC} = 48 \text{ V}$
Common	Buck-Boost inductor	$L_{BB} = 120 \mu\text{H}$	$L_{BB} = 50 \mu\text{H}$
	Buck-Boost capacitor	$C_{BB} = 10 \mu\text{F}$	$C_{BB} = 10 \mu\text{F}$
	Snubber capacitors	$C_{sb} = 0.1 \text{ nF}$	$C_{sb} = 0.1 \text{ nF}$
Devices used	Switching devices	IRF 540N	IRF 540N
	Power diodes	MBR20200CT	MBR20200CT
Load-1	Switching frequency	$f_s = 200 \text{ kHz}$	$f_{s1} = 200 \text{ kHz}$
	Output voltage	$V_O = 22.5 \text{ V}$	$V_{O1} = 22.5 \text{ V}$
	Output current	$I_O = 1.012 \text{ A}$	$I_{O1} = 1.012 \text{ A}$
	Output power	$P_O = 22.77 \text{ W}$	$P_{O1} = 22.77 \text{ W}$
	Resonant frequency	$f_r = 166.53 \text{ kHz}$	$f_{r1} = 166.53 \text{ kHz}$
	Resonant inductor	$L_r = 88 \mu\text{H}$	$L_{r1} = 88 \mu\text{H}$
	Resonant capacitor	$C_r = 10 \text{ nF}$	$C_{r1} = 10 \text{ nF}$
	Output capacitor	$C_O = 4 \mu\text{F}$	$C_{O1} = 4 \mu\text{F}$
	Dimming frequency	$f_{Dim} = 200 \text{ Hz}$	$f_{Dim1} = 200 \text{ Hz}$
Load-2	Switching frequency		$f_{s2} = 200 \text{ kHz}$
	Output voltage		$V_{O2} = 39.6 \text{ V}$
	Output current		$I_{O2} = 1.096 \text{ A}$
	Output power		$P_{O2} = 43.41 \text{ W}$
	Resonant frequency	NA	$f_{r2} = 178.63 \text{ kHz}$
	Resonant inductor		$L_{r2} = 77 \mu\text{H}$
	Resonant capacitor		$C_{r2} = 10 \text{ nF}$
	Output capacitor		$C_{O2} = 4 \mu\text{F}$
	Dimming frequency		$f_{Dim2} = 200 \text{ Hz}$

to design the second LED load for 43.41 W, 39.612 V with a current of 1.096 A and threshold voltage of 27.852 V, the operating point of LED is selected as 3.301 V and 548 mA. Thus, the total LED load-2 comprises of two LED strings in parallel where each string contains twelve LEDs in series. After computing L_{BBcrit} with two loads from (4.21), the value of inductor L_{BB} is chosen a little higher than L_{BBcrit} as $50\mu\text{H}$.

4.5 Simulation and Experimental Results

To confirm the feasibility of the proposed configuration, a prototype has been built and tested with a single load of 22.5 W and with two loads of 22.5 W and 43 W. A snubber capacitor C_{sb} is connected across each MOSFET switch of the inverter. Table 4.1 shows the parameters of the proposed LED driver for the single load as well as two loads. The experimental results are validated with OrCAD PSpice simulation counterparts. Fig. 4.5a shows the experimental setup of the proposed LED driver. The control logic is implemented using PWM ICs as shown

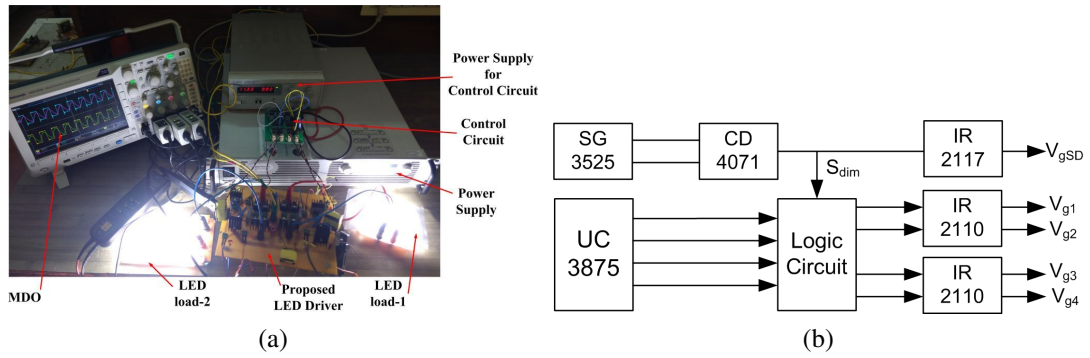


Figure 4.5: (a) Experimental Setup of proposed configuration (b) Schematic of the control circuit

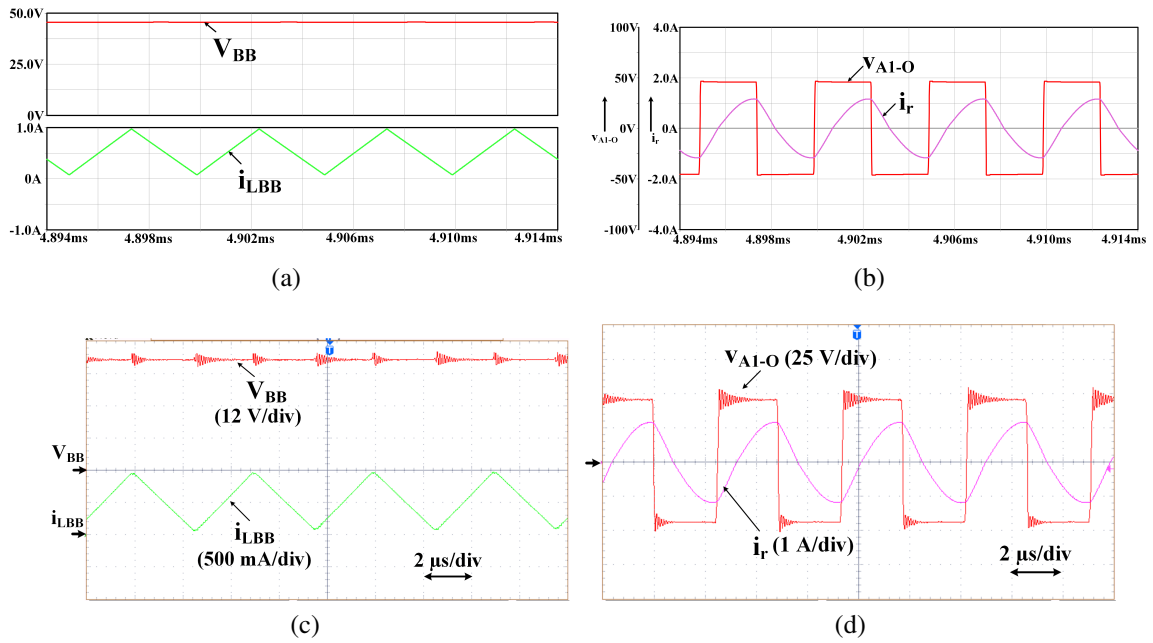


Figure 4.6: Waveforms with single load configuration: (a) Simulation waveforms of V_{BB} and i_{LBB} (b) Simulation waveforms of \bar{V}_{A1-O} and i_r (c) Experimental waveforms of V_{BB} and i_{LBB} (d) Experimental waveforms of \bar{V}_{A1-O} and i_r

in Fig. 4.5b.

Fig. 4.6 - Fig. 4.8 depict the simulation and experimental results of the proposed configuration with single load for 100% dimming. Fig. 4.6a & Fig. 4.6c depict simulation and experimental waveforms of i_{LBB} and V_{BB} , which evident that $V_{BB} \approx V_{DC}$ with 50% duty cycle. Fig. 4.6b & Fig. 4.6d show the simulation and experimental waveforms of i_r and \bar{V}_{A1-O} . Fig. 4.7 shows simulation and experimental waveforms of switch voltages and currents. **From these figures, ZVS turn-ON is observed in all the switches.** It can also be noticed from Fig. 4.7 that peak currents in both switches are not similar, as these switches carry the resultant current due to i_{LBB} and i_r . Fig. 4.8a & Fig. 4.8b show simulation and experimental waveforms of V_O and I_O

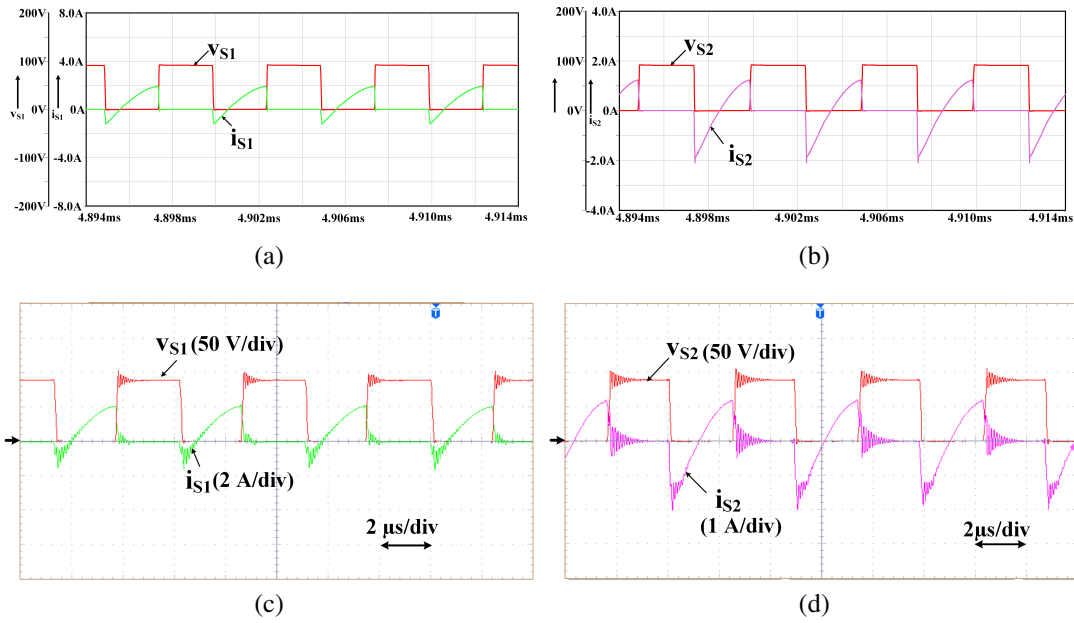


Figure 4.7: Waveforms of switch current and voltages with single load: (a) Simulation waveforms of switch S_1 (b) Simulation waveforms of switch S_2 (c) Experimental waveforms of switch S_1 (d) Experimental waveforms of switch S_2

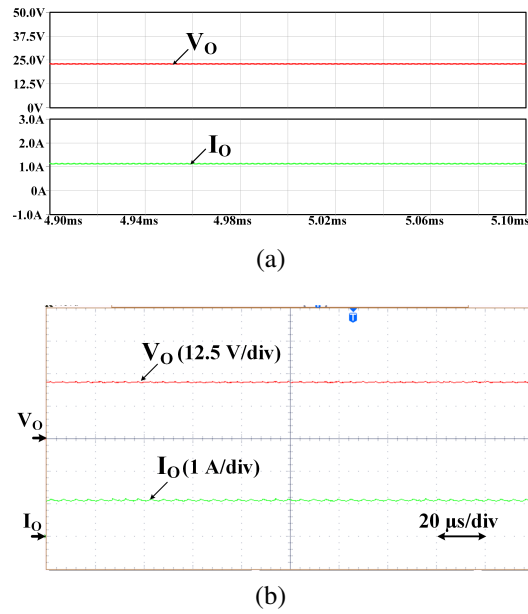


Figure 4.8: Waveforms of LED output voltage and current with single load: (a) Simulation (b) Experimental

at full illumination level.

For two load configuration, shown in Fig. 4.1b, in order to operate for full illumination level, the dimming switch S_D must be always ON as shown in Fig. 4.2b. The simulation and

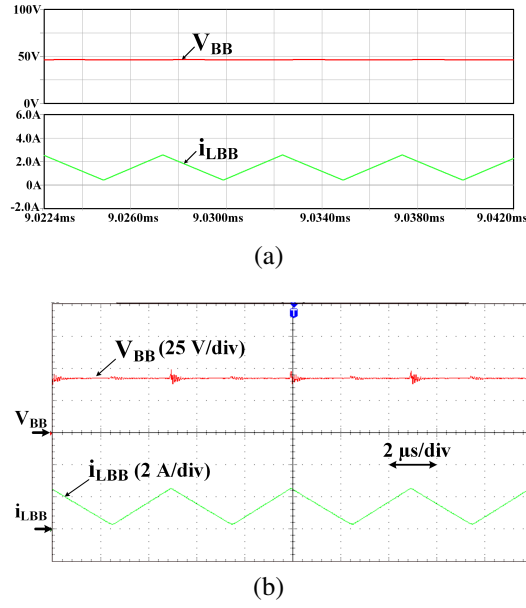


Figure 4.9: Waveforms of V_{BB} and i_{LBB} for two load configuration: (a) Simulation (b) Experimental

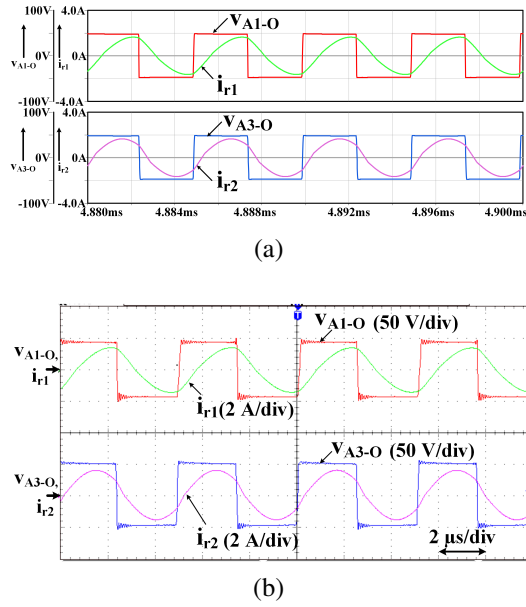


Figure 4.10: Waveforms of resonant current and voltages of load-1 and load-2: (a) Simulation (b) Experimental

experimental results of the proposed configuration for two loads with 100% dimming are shown in Fig. 4.9 - Fig. 4.13. Fig. 4.9 shows the simulation and experimental waveforms of V_{BB} & i_{LBB} . Fig. 4.10a and Fig. 4.10b show simulation and experimental waveforms of the resonant currents and voltages of two loads. Fig. 4.11a shows simulation voltage and current waveforms of S_1 & S_2 . The corresponding experimental waveforms are shown in Fig. 4.11b. ZVS turn-ON

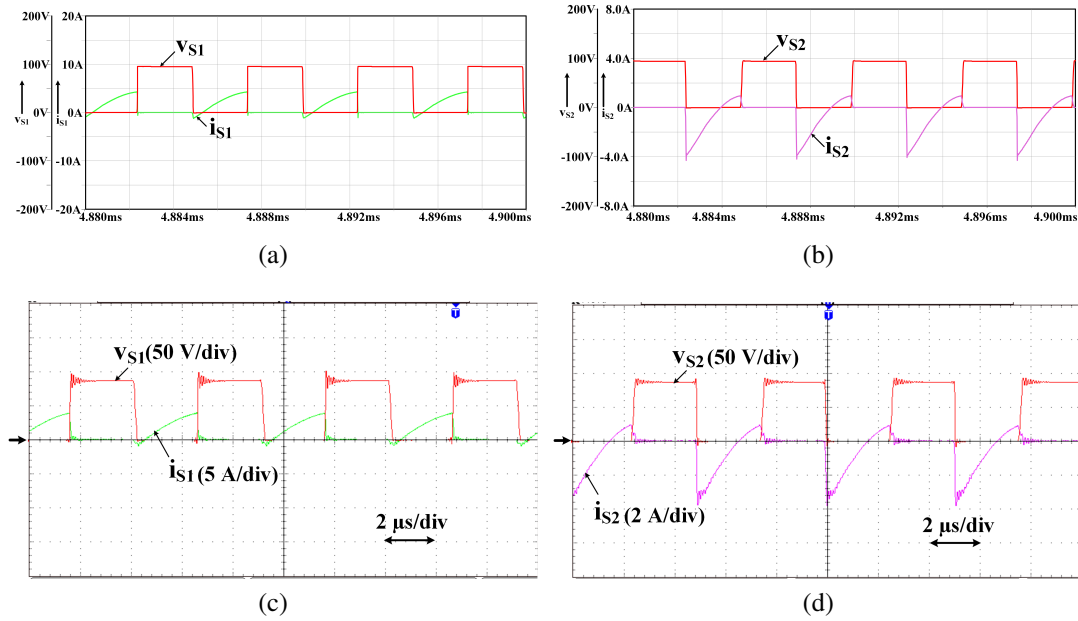


Figure 4.11: Waveforms of inverter switch current and voltages of load-1: (a) Simulation waveforms of switch S_1 (b) Simulation waveforms of switch S_2 (c) Experimental waveforms of switch S_1 (d) Experimental waveforms of switch S_2

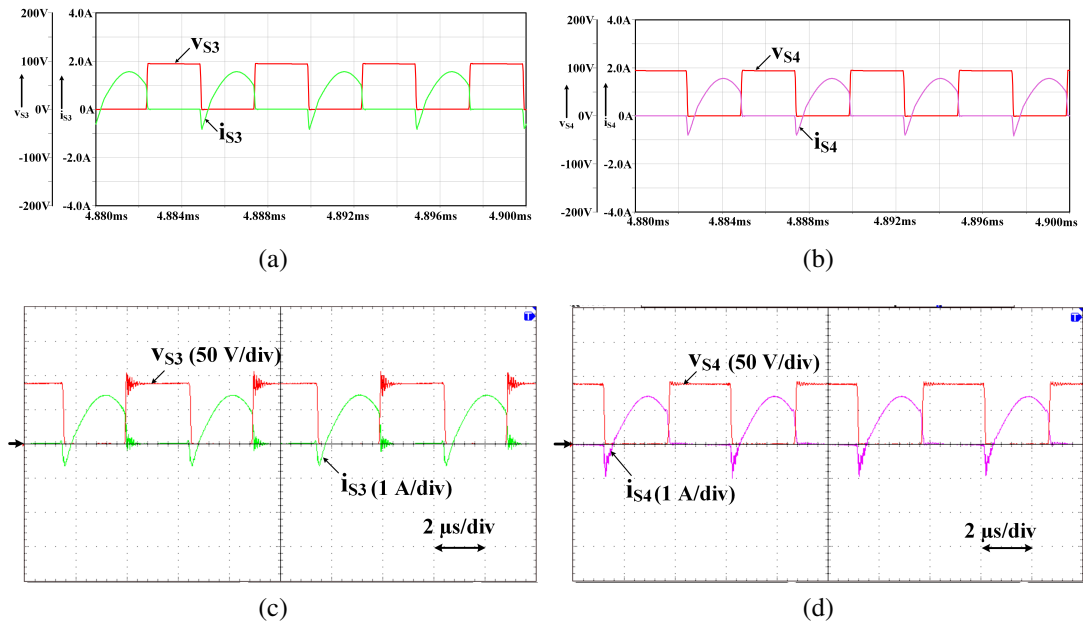


Figure 4.12: Waveforms of inverter switch current and voltages of load-2: (a) Simulation waveforms of switch S_3 (b) Simulation waveforms of switch S_4 (c) Experimental waveforms of switch S_3 (d) Experimental waveforms of switch S_4

across both the switches can be observed. Fig. 4.12a shows the simulation voltage and current waveforms of S_3 & S_4 and the corresponding experimental waveforms are shown in Fig. 4.12b.

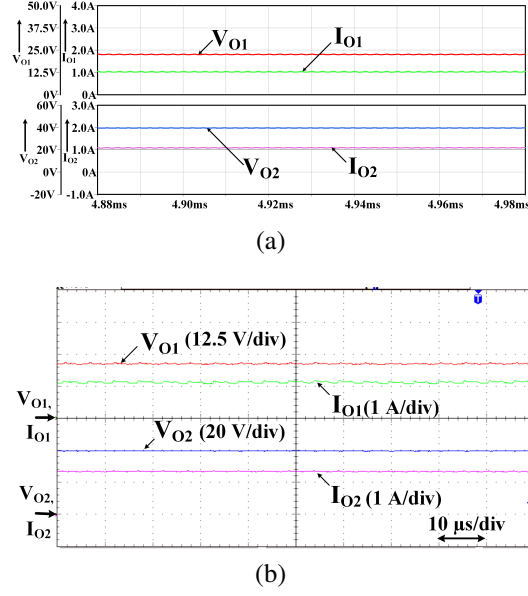


Figure 4.13: Waveforms of LED output voltage and current of both loads: (a) Simulation (b) Experimental

Table 4.2: Regulation of output current with the variation of switching frequency for input voltage variations

Variation of V_{DC} (V)	Single Load	Two Loads	
	f_s	f_{s1}	f_{s2}
	(kHz)	(kHz)	(kHz)
52	204	204	206
50	202	202	203
48	200	200	200
46	198	198	197
44	196	196	194

ZVS turn-ON across both the switches can be observed. The peak values of currents in S_1 & S_2 are not similar, as they carry both i_{LBB} and i_{r1} . But S_3 & S_4 carry only i_{r2} and no effect of buck-boost inductor current i_{LBB} , thus results in equal peak currents. Fig. 4.13a & Fig. 4.13b show simulation and experimental waveforms of output voltage and currents of Load-1 & Load-2 at full illumination level.

4.6 Regulation of LED Voltage and Illumination

In the proposed configuration, inverter switches are operated with 50% duty cycle. The output LED load voltage is regulated using frequency control against input voltage variations. The proposed converter is tested for input voltage variations from 44 V to 52 V. Table 4.2 shows the corresponding frequency control with a single load and two loads. With two loads,

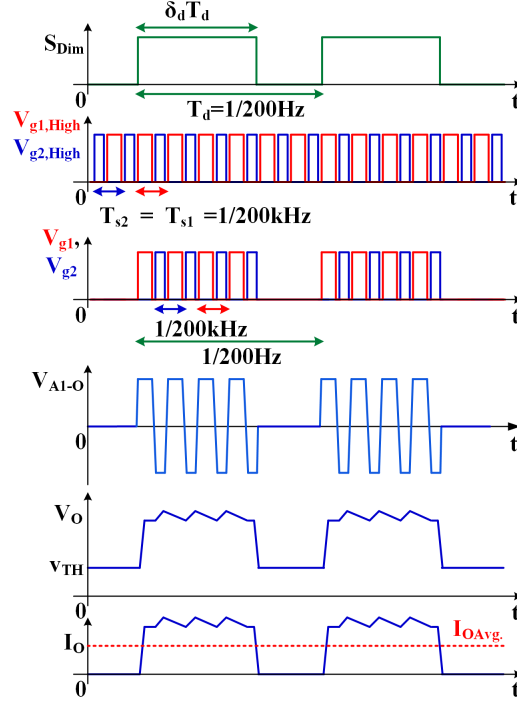


Figure 4.14: Dimming control of the proposed converter for a single load

independent control of voltage regulation is possible by controlling the switching frequency of switching devices of the corresponding inverter leg. For example, as shown in the table 4.2, when $V_{DC} = 44V$, f_{S1} of 196 kHz and f_{S2} of 194 kHz are required to maintain constant voltages in Load-1 and Load-2 respectively. Thus, independent output voltage regulation is possible with the proposed configuration.

Further, a low frequency (200 Hz) PWM dimming is implemented for illumination control, as illustrated in Fig. 4.14, where δ_d , T_d are duty cycle and time period of dimming signal. Thus, controlling the δ_d from 20% to 100%, the average current in the LED lamp is regulated without affecting the operating point of LED lamp. Fig. 4.14 depicts the schematic waveforms under dimming for single load. From Fig. 4.14, it can be observed that V_O reduces below threshold voltage when input voltage for resonant tank, \bar{V}_{A1-O} is zero and thereby, I_O reduces to zero respectively. Fig. 4.15 & Fig. 4.16 show the simulation and experimental waveforms of i_{LBB} , V_{BB} , V_O and I_O at 40% and 80% dimming levels dimmed with a low dimming frequency of 200 Hz.

Schematic waveforms of dimming signals for two loads is shown in Fig. 4.17. When the dimming level of load-1 is equal to or greater than the dimming level of load-2, inverter leg of particular load is turned ON-OFF based on required dimming levels. The input voltages for Load-2 are V_{DC} & V_{BB} ; buck-boost operation is always essential for the operation of Load-2.

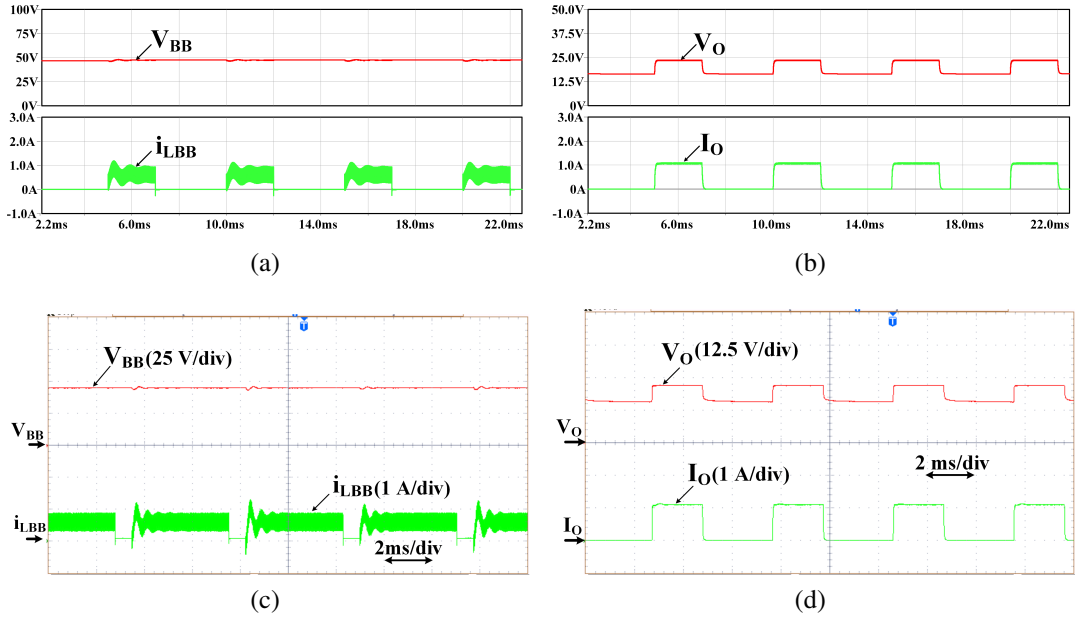


Figure 4.15: Dimming waveforms at 40% dimming with single load configuration: (a) Simulation waveforms of V_{BB} and i_{LBB} (b) Simulation waveforms of V_O and I_O (c) Experimental waveforms of V_{BB} and i_{LBB} (d) Experimental waveforms of V_O and I_O

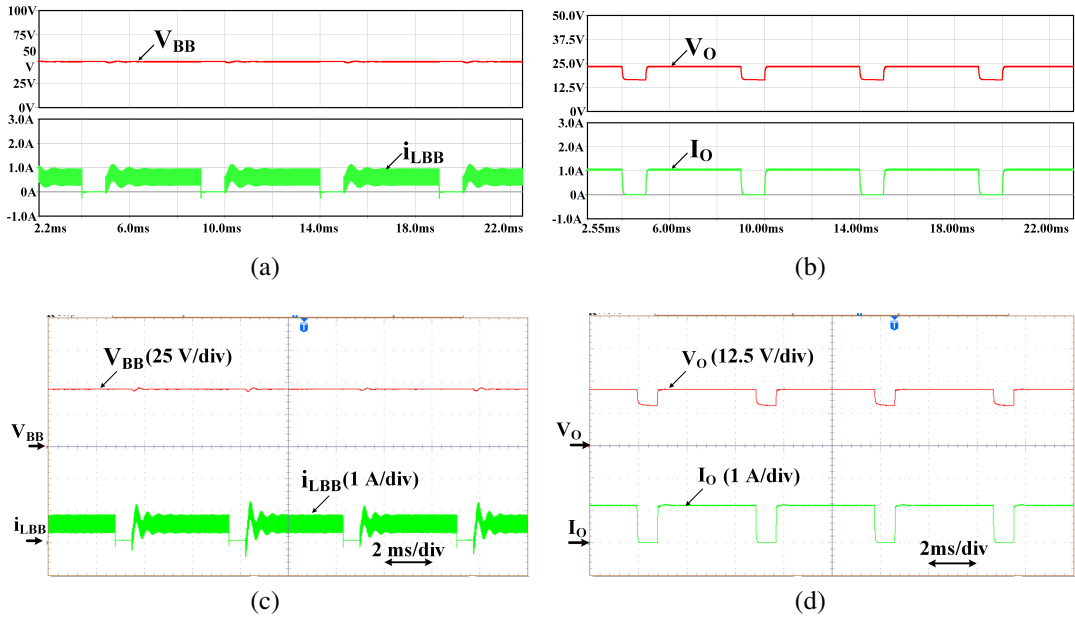


Figure 4.16: Dimming waveforms at 80% dimming with single load configuration: (a) Simulation waveforms of V_{BB} and i_{LBB} (b) Simulation waveforms of V_O and I_O (c) Experimental waveforms of V_{BB} and i_{LBB} (d) Experimental waveforms of V_O and I_O

Hence, for the effective operation of Load-2, the switches (S_1 & S_2) integrated with buck-boost operation should be always ON. Thus, to control the dimming operation of Load-1 for lower

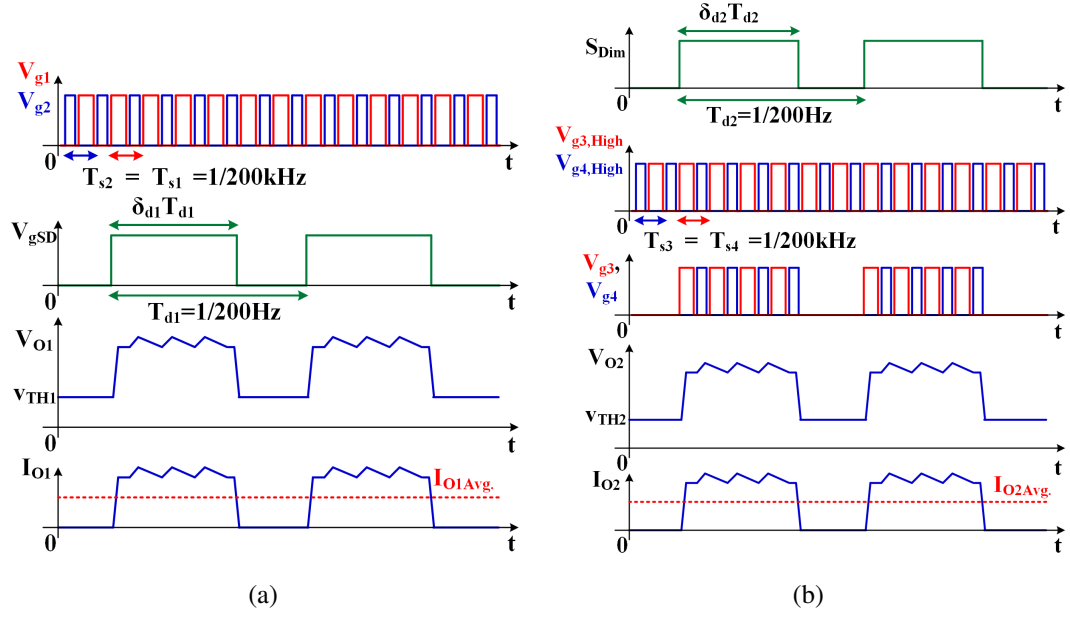


Figure 4.17: Dimming control of the proposed converter for two loads: (a) for load-1 (b) for load-2

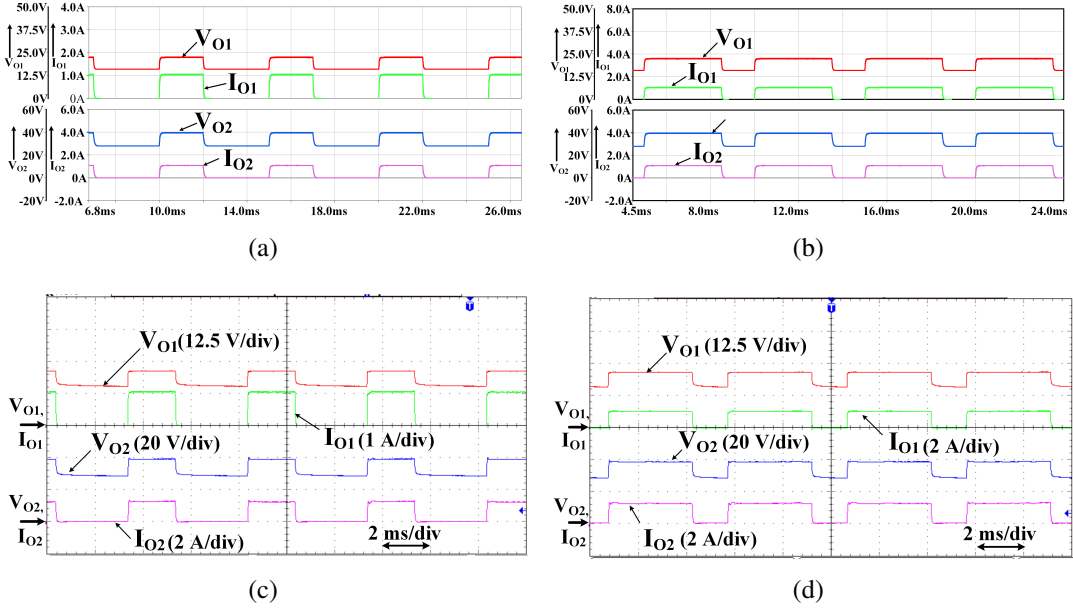


Figure 4.18: Dimming waveforms of V_{O1} , I_{O1} , V_{O2} and I_{O2} for two load configuration with equal dimming levels: (a) Simulation waveforms at 40% dimming (b) Simulation waveforms at 70% dimming (c) Experimental waveforms at 40% dimming (d) Experimental waveforms at 70% dimming

dimming level than Load-2 counterpart, the switch S_D is turned ON-OFF with low dimming frequency as shown in Fig. 4.17b. Thereby, independent dimming is possible with both loads.

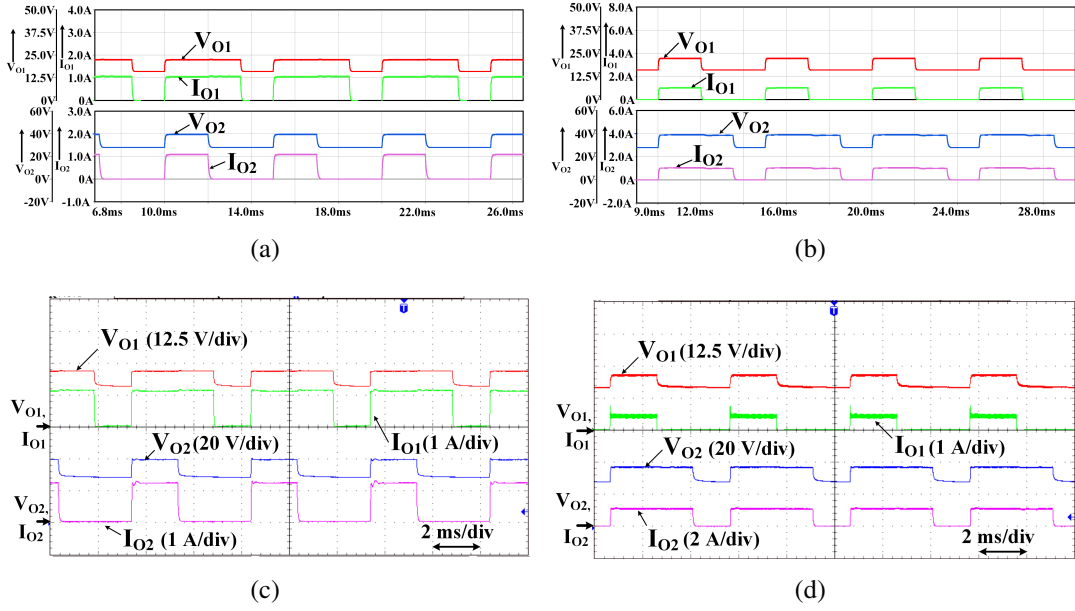


Figure 4.19: Dimming waveforms of V_{O1} , I_{O1} , V_{O2} and I_{O2} for two load configuration with unequal dimming levels: (a) Simulation waveforms with load-1 70% and load-2 40% dimming (b) Simulation waveforms with load-1 40% and load-2 70% dimming (c) Experimental waveforms with load-1 70% and load-2 40% dimming (d) Experimental waveforms with load-1 40% and load-2 70% dimming

Fig. 4.18 & Fig. 4.19 show the simulation and experimental waveforms of LED output voltage and currents of two loads with equal and unequal dimming levels respectively. Fig. 4.18 shows dimming waveforms with equal dimming levels. Fig. 4.18a & Fig. 4.18c show the simulation and experimental dimming waveforms with 40% dimming. Fig. 4.18b & Fig. 4.18d show the simulation and experimental dimming waveforms with 70% dimming. Fig. 4.19 shows dimming waveforms with independent dimming levels. Fig. 4.19a & Fig. 4.19c show the simulation and experimental dimming waveforms when load-1 operated with 70% dimming and load-2 operated with 40% dimming. Fig. 4.19b & Fig. 4.19d show the simulation and experimental dimming waveforms when load-1 operated with 40% and load-2 operated with 70% dimming respectively. Thereby, independent dimming is also achieved across the two loads using the proposed configuration.

4.7 Efficiency and Comparison

In order to maintain constant output voltage against input voltage variations, frequency control is employed in the proposed configuration. Fig. 4.20a shows the efficiency curve with frequency control for a single load. Efficiency is above 91% for the entire frequency range and maximum efficiency is 93.23%. Fig. 4.20b shows the efficiency curve for different dimming

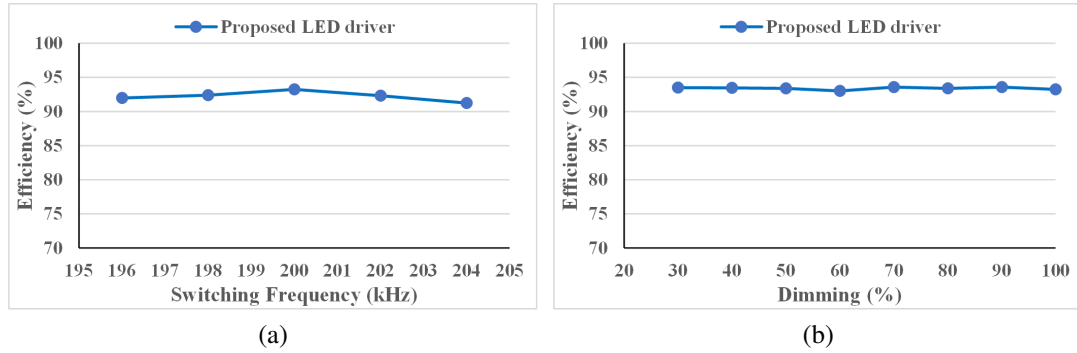


Figure 4.20: Efficiency curves: (a) Efficiency vs switching frequency (b) Efficiency vs dimming level

levels, where, the proposed converter maintains high efficiency of 93% to 94% at all dimming levels. The two load configuration also provides an overall high efficiency of 92.3%.

When compared with a conventional half-bridge converter, the proposed configuration doubles its gain with an extra inductor for a single load. However, only one additional dimming switch is required to achieve independent dimming control of multiple loads. When compared with a conventional full-bridge converter, the proposed configuration reduces the switch count by $(2n-1)$ where n is the number of loads. In [59], a non-isolated LED driver is proposed with high gain by cascading buck-boost converter with a half-bridge resonant converter. But, it leads to more component count and hence increased cost. Also, due to hard switching of buck-boost converter, the switching losses increase and hence, the efficiency is less.

Table 4.3 describes the comparative study of the proposed configuration in contrast to existing similar LED drivers for multiple loads [56, 60–65]. LED drivers in [56, 60, 61] use transformers, thus suitable for isolated applications, but have limitations like more number of transformers, secondary windings, inductors & capacitors respectively. Non-isolated LED drivers with multiple loads, reported in [62–65], suffer from drawbacks like no independent dimming, less reliable, unequal output voltage gains, unable to drive loads with equal or unequal wattages/voltages. Further, the LED driver in [65] requires one extra switch which increases cost and power losses as compared to the proposed configuration. Hence, when compared with conventional and existing similar topologies, the proposed configuration provides various advantages such as: reduced device count, less cost, high gain for all LED loads, reduced switching loss due to soft-switching across all devices, improved efficiency, simple control technique, ability to drive multiple loads with equal or unequal voltages/wattages and independent voltage regulation & dimming control. Thus, the proposed non-isolated half-bridge high gain configuration is well suitable for SPV/battery fed multiple load LED lighting applications.

Table 4.3: Comparison of proposed configuration with existing similar multiple load LED drivers

Features	Ref. [56]	Ref. [60]	Ref. [61]	Ref. [62]	Ref. [63]	Ref. [64]	Ref. [65]	Proposed
ZVS	Yes	Yes	Yes	Yes	No	Yes	Yes	Yes
Input voltage (V)	380	48	400	150	12	66	48	48
Total output power (W)	50	20	200	30	24	145	126	65
Peak efficiency (%)	90.5	93.4	92.8	95.5	91.7	94.96	92.45	93
No. of Switches (multiple loads, n)	2	2+n	4	n	2	2+n	2+2n	1+2n
No. of Diodes (multiple loads, n)	2n	4n	4n	n	2n	1	4n	4n
No. of Inductors (multiple loads, n)	n (variable inductors)	n	2+2n	n (one is coupled)	2	$n+[(2n-4)/4]$	1+n	1+n
No. of Capacitors (multiple loads, n)	2n	2+4n	2+2n	2n	3n-1	1	2n	1+2n
No. of Transformers (multiple loads, n)	n (centre tapped)	1 (with n sec. windings)	1	0	0	0	0	0
Total component for each lamp	Moderate	High	High	Moderate	Low	Low	Moderate	Moderate
No. of LED loads tested	1	4	2	2	2	4	2	2
Power rating of all Lamps	-	Different	Different	Different	Same	Same	Different	Different
Non-Isolated	No	No	No	Yes	Yes	Yes	Yes	Yes
Dimming	Yes	Yes	Yes	Yes	No	Yes	Yes	Yes
Suitable for multiple loads	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Independent dimming	-	Yes	Yes	No	No	No	Yes	Yes

4.8 Summary

In this chapter, a high gain buck-boost integrated symmetrical half-bridge non-isolated LC series resonant converter has been proposed for SPV/battery fed multiple load LED lighting applications. The integrated buck-boost operation provides optimum utilization of input voltage and results in twice the gain of the conventional half-bridge converter. Frequency modulation has been used to regulate the output voltage against input voltage variations. The principle & the time intervals of operation, analysis and design procedure have been presented. The proposed converter configuration for single load and its extended version for two loads have been realized and tested. Independent voltage regulation and dimming control were achieved for both the loads. Also, the proposed configuration has been compared with similar multiple-load LED drivers and it provides various advantages such as: reduced device count, less cost, high gain for all LED loads, reduced switching loss due to soft-switching across all devices, improved efficiency, simple control technique, ability to drive multiple loads with equal or unequal voltages/wattages and independent voltage regulation & dimming control.

Chapter 5

Wide Input LED Driver for Automotive LED Lighting Systems

Chapter 5

Wide Input LED Driver for Automotive LED Lighting Systems

5.1 Introduction

A battery of 12/24 V in automotive applications may vary up to 64 V during transients and can be even more. Further, there are different battery voltage systems available in the automotive system. Hence, there is a requirement of LED drivers that can operate for wide input voltage ranges. Even though there are LED drivers that are suitable for wide input automotive LED lighting applications, they suffer from one or many of the following limitations: hard switched, complex implementation, have narrow gain and more component count that increases the size and cost. Hence, there is a requirement of wide input LED drivers suitable for automotive applications that overcome the above drawbacks. For low power applications, a non-isolated SRC is a better choice due to its easier implementation, reduced cost and size. Thereby, in this third work, a reconfigurable non-isolated BB integrated FB SRC (R-BBI-FBSRC) based LED driver is proposed for automotive LED lighting applications with wide input voltage variations which overcomes the above drawbacks. By proper switch configurations, it can be re-configured as BB integrated FB SRC (BB-FBSRC), BB integrated HB SRC (BB-HBSRC) and conventional HBSRC. Thus, when compared with conventional HBSRC, it can produce three levels of gain, viz. four times the gain with BB-FBSRC configuration, two times the gain with BB-HBSRC configuration and the same gain with HBSRC configuration. By transformation from one topology to other based on the input voltage range and with APWM control, the proposed configuration can operate for a wide input voltage range while maintaining soft switching. As LED load is constant, and automotive applications have wide input voltage variations, the proposed configuration is well suitable as an LED driver in automotive applications. PWM dimming is used for illumination control that controls the average LED current. The description of the proposed configuration and its working principle are presented in section 5.2. Analysis of the converter is presented in section 5.3. Design aspects of the converter are discussed in section 5.4. Simulation and experimental results are presented in section 5.5. Efficiency analysis

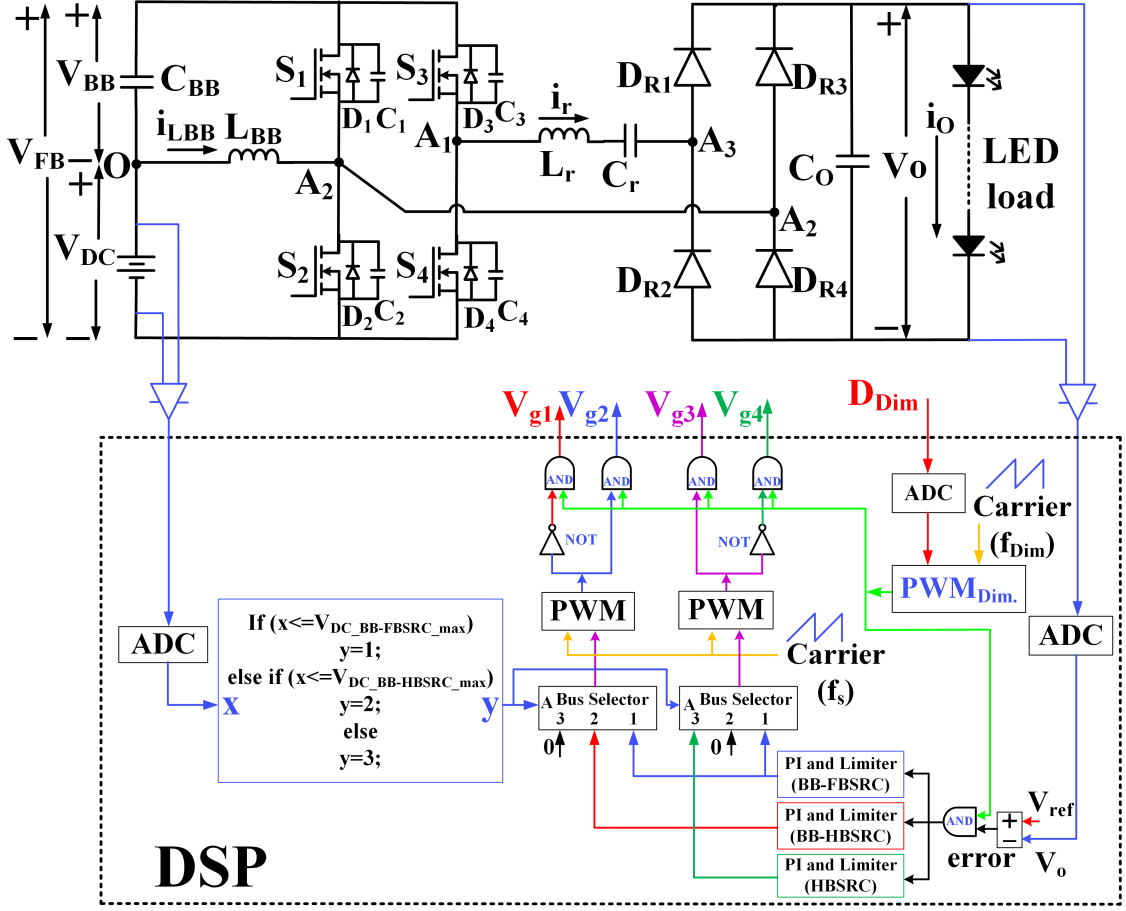


Figure 5.1: Proposed wide input voltage LED driver

and comparative study are carried out in section 5.6 and section 5.7 summarizes the chapter.

5.2 Proposed Configuration and Working Principle

5.2.1 Description of Proposed Topology

The circuit diagram of the proposed LED driver is shown in Fig. 5.1, that consists of a synchronous BB converter integrated with FBSRC. S_1 to S_4 are the four MOSFET switches with body diodes and snubber capacitors. D_{R1} to D_{R4} are the diodes that constitute the diode bridge rectifier. L_r and C_r are the series resonant elements. C_o is the output capacitor. C_{BB} , S_1 , S_2 and inductor L_{BB} are the elements of integrated synchronous BB converter. V_{DC} , V_{BB} and i_{LBB} are the input, output voltages and inductor current corresponding to the BB operation. V_{FB} is the input voltage applied to the SRC and i_r is the resonant current. V_o and I_o are respectively the LED voltage and current.

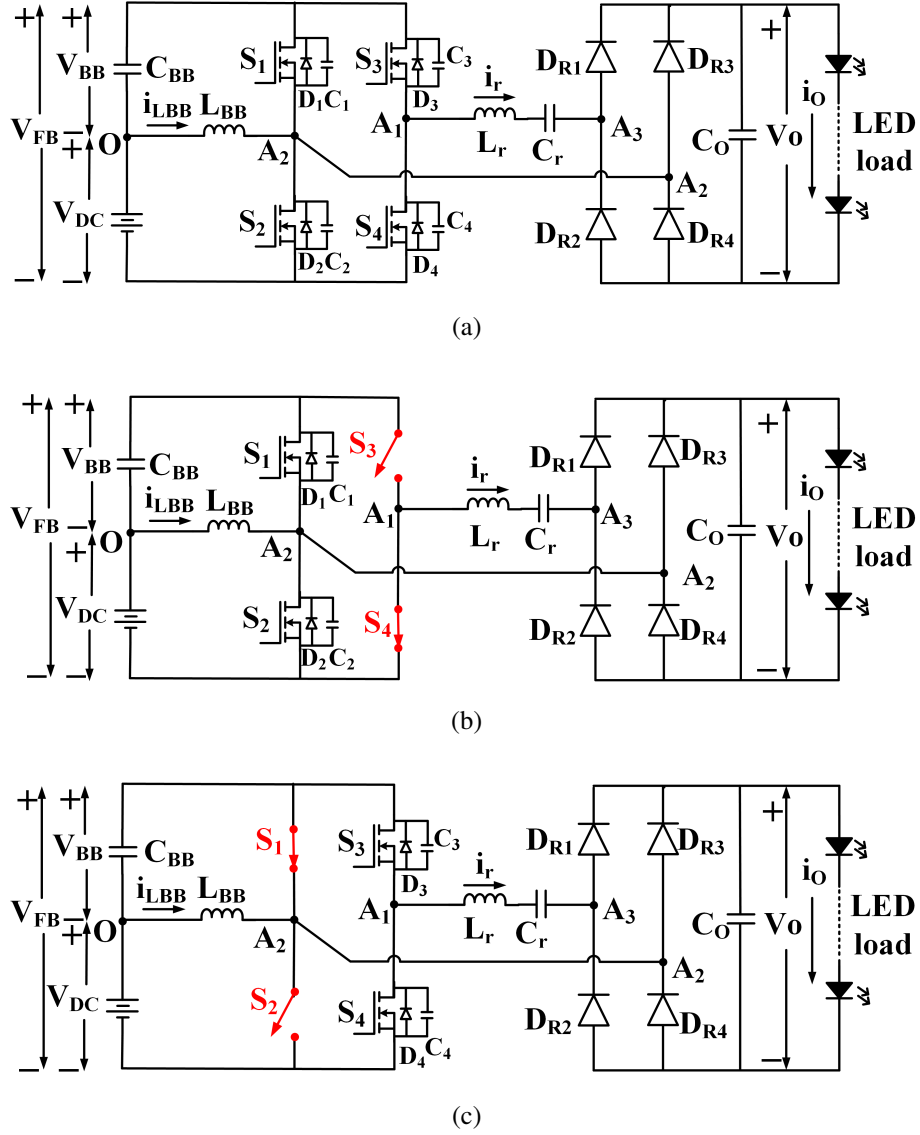


Figure 5.2: Different reconfigurations of proposed LED driver under different input voltage ranges: (a) BB-FBSRC (b) BB-HBSRC (b) HBSRC

5.2.2 Different Reconfigurations

In order to operate for a wide input voltage range, the input voltage and switches of FB converter are effectively utilized in the proposed configuration. The two switches S_1 and S_2 in the FB resonant converter are also shared for BB operation. Hence, the proposed configuration can be reconfigured into three different resonant converter topologies based on the input voltage ranges. The first configuration is BB-FBSRC topology as shown in Fig. 5.2a, where BB operation is integrated with FBSRC. Thus, with the voltage $V_{FB} = V_{DC} + V_{BB}$, BB-FBSRC produces four times the voltage gain compared to conventional HBSRC. The second configura-

tion is BB-HBSRC topology, which is obtained by continuously maintaining switch S_3 in OFF state and switch S_4 in ON state as shown in Fig. 5.2b, where BB operation is integrated with HBSRC. Thus, with the voltage $V_{FB} = V_{DC} + V_{BB}$, BB-HBSRC produces two times the voltage gain compared with conventional HBSRC. The third configuration is conventional HBSRC topology, which is obtained by continuously maintaining switch S_1 in ON state and switch S_2 in OFF state as shown in Fig. 5.2c, where the voltage $V_{FB} = V_{DC}$. Thus, the three levels of voltage gains obtained are well utilized for operating under wide input voltage.

5.2.3 APWM Control Using PI Controller

Generally, FM, PSM and APWM control schemes are employed in resonant converters. Compared with FM control, PSM and APWM control can achieve a wide voltage conversion ratio [91]. In the proposed converter, PSM control can only be implemented in BB-FBSRC configuration as the remaining two configurations are half-bridge based topologies. Hence, a simple APWM control is optimal and is employed in all the three configurations of the proposed converter for output voltage regulation. The schematic of the closed-loop control is shown in Fig. 5.1. Digital control is employed using Digital Signal Processor (DSP). Three different PI controllers are employed for the three configurations. The input and output voltages are measured and fed to the DSP. The required illumination level is set in terms of dimming signal duty cycle D_{Dim} and corresponding low-frequency dimming signal is generated. Based on the input voltage range, the switches are configured to one of the three configurations and the corresponding PI output is enabled. The PI controller develops the required duty cycle (D) of high-frequency PWM signals based on the actual output voltage and reference voltage. These PWM signals and the dimming signal are combined using AND logic, producing the gate signals V_{g1} to V_{g4} for the switches S_1 to S_4 respectively.

5.2.4 Principle of Operation

The operations of BB-FBSRC and BB-HBSRC are similar and HBSRC is the conventional converter. Hence, the principle and the time intervals of operation are discussed only for BB-FBSRC. The key waveforms of BB-FBSRC are shown in Fig. 5.3. The gate signals V_{g1} and V_{g2} are complementary to each other and the gate signals V_{g3} and V_{g4} are complementary to each other. V_{FB} is the sum of two voltages, V_{DC} and V_{BB} , which is applied across the FB inverter. The FB inverter output voltage \bar{v}_{A1-A2} results in i_r that flows through the LED load after rectification.

The operation of BB-FBSRC, is divided into six time intervals and the equivalent circuit

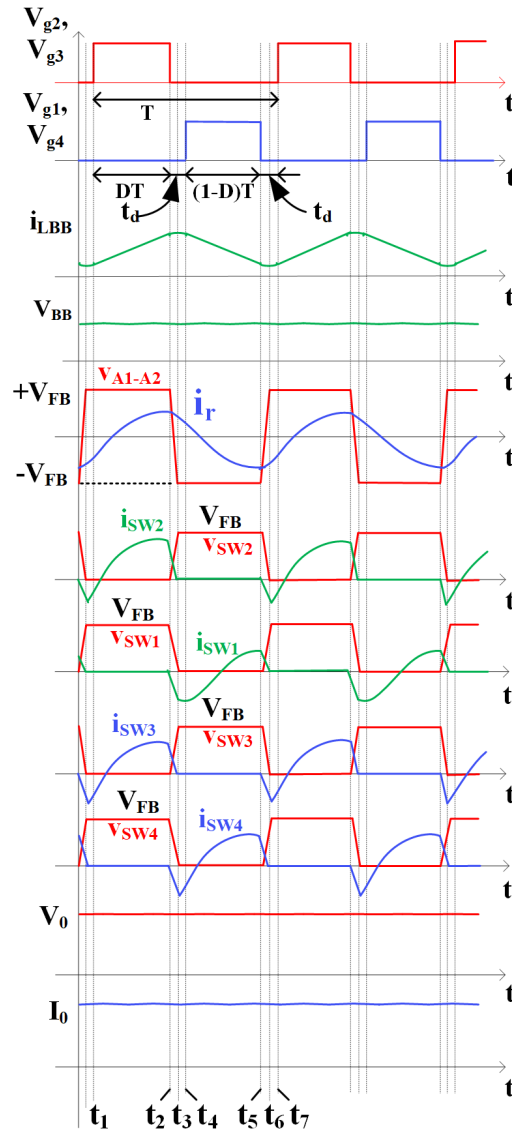


Figure 5.3: Key waveforms of BB-FBSRC

of each **interval** is shown in Fig. 5.4 and explained as follows:

5.2.4.1 Time Interval-1 [t_1 - t_2]

The zero voltage across S_2 and S_3 due to the prior conduction of diodes D_2 and D_3 results in ZVS turn-ON when the gate signals are provided at $t = t_1$. The currents, i_{LBB} and i_r continue to rise in the positive direction and their resultant flows in S_2 as shown in Fig. 5.4a.

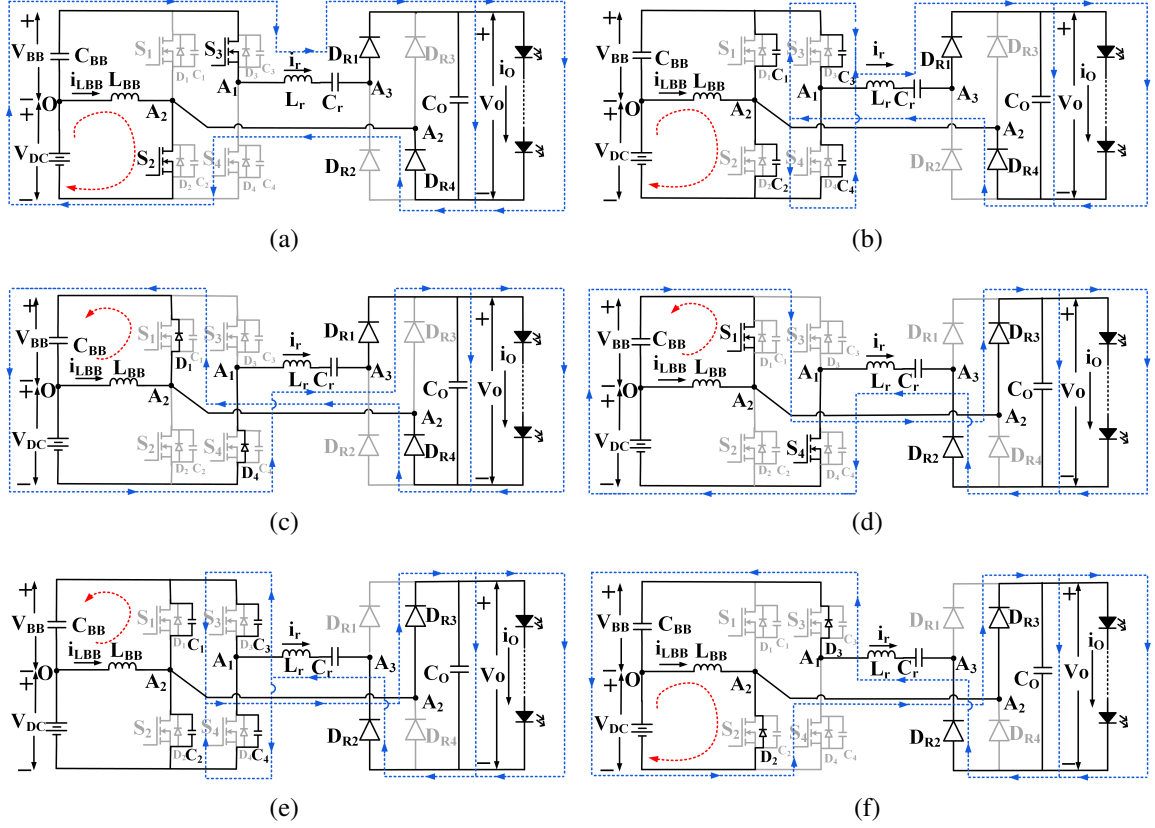


Figure 5.4: Various intervals of operation of BB-FBSRC: (a) Interval-1 (b) Interval-2 (c) Interval-3 (d) Interval-4 (e) Interval-5 (f) Interval-6

5.2.4.2 Time Interval-2 [t_2 - t_3]

When S_2 and S_3 are turned OFF at $t = t_2$, C_2 , C_3 charge and C_1 , C_4 discharge respectively. Resonance condition takes place between the inductors and capacitors for a short duration. Assuming i_r and i_{LBB} to be constant during this short interval of operation, half of their resultant current flows through each capacitor as illustrated in Fig. 5.4b.

5.2.4.3 Time Interval-3 [t_3 - t_4]

At $t = t_3$, as C_1 and C_4 are completely discharged thus, D_1 and D_4 become forward biased. The inductor L_{BB} starts demagnetizing and also, i_r starts decreasing. Thus, the current in the diodes starts raising from negative value. The diode D_1 current is the sum of i_{LBB} and i_r as illustrated in Fig. 5.4c. The duration [t_2 - t_4] can be considered as dead time (t_d).

5.2.4.4 Time Interval-4 [t_4 - t_5]

The zero voltage across S_1 and S_4 due to the prior conduction of diodes D_1 and D_4 results in ZVS turn-ON when the gate signals are provided at $t = t_4$. i_{LBB} and i_r continue to decrease and their resultant flows in S_1 as shown in Fig. 5.4d.

5.2.4.5 Time Interval-5 [t_5 - t_6]

At $t = t_5$, when S_1 and S_4 are turned OFF, C_2 , C_3 discharge and C_1 , C_4 charge respectively. Resonance condition takes place between the inductors and capacitors for a short duration. Assuming i_r and i_{LBB} to be constant in this short duration, half of the resultant current shared by each capacitor as illustrated in Fig. 5.4e.

5.2.4.6 Time Interval-6 [t_6 - t_7]

At $t = t_6$, C_2 and C_3 are completely discharged and hence, D_2 and D_3 start conducting. The current, i_r starts raising. Also, due to magnetization, the current i_{LBB} increases linearly. Thus, the diode currents start increasing from negative value. The resultant current due to i_{LBB} and i_r flows in D_2 as illustrated in Fig. 5.4f. The duration [t_5 - t_7] can be considered as dead time (t_d). This interval ends when gate signals are provided to switches S_2 and S_3 .

5.3 Analysis of Proposed Converter

5.3.1 Voltage Gain

Analysis of BB-FBSRC is carried out under steady-state with the assumption of ideal devices (MOSFETs and Diodes) and constant output current. The voltage, V_{BB} due to integrated BB operation is obtained as

$$V_{BB} = \frac{D}{(1-D)} V_{DC} \quad (5.1)$$

The total input voltage, V_{FB} applied to the BB-FBSRC is expressed as

$$V_{FB} = V_{DC} + V_{BB} = V_{DC} + \frac{D}{(1-D)} V_{DC} = \frac{V_{DC}}{(1-D)} \quad (5.2)$$

Square wave voltage with a magnitude of V_{FB} that is obtained from FB inverter is applied across $L_r - C_r$ network. As the fundamental components of the voltage and current of the resonant network is sinusoidal in nature, classical AC analysis can be carried out [98]. The AC equivalent circuit of the proposed configuration is shown in Fig. 5.5.

From Fig. 5.5, the voltage gain can be expressed as:

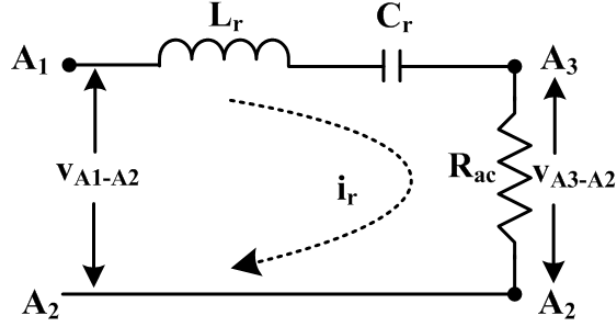


Figure 5.5: AC equivalent circuit

$$\frac{\bar{V}_{A3-A2}}{\bar{V}_{A1-A2}} = \frac{R_{ac} \sin(\pi D)}{R_{ac} + j(X_{Lr} - X_{Cr})} \quad (5.3)$$

where

$$X_{Lr} = 2\pi f_s L_r; X_{Cr} = \frac{1}{2\pi f_s C_r}; R_{ac} = \frac{8}{\pi^2} R_O \quad (5.4)$$

\bar{V}_{A1-A2} and \bar{V}_{A3-A2} are input and output **RMS** voltages of the resonant network respectively.

The voltage gain of BB-FBSRC, can be expressed in terms of circuit parameters as

$$G_1 = \frac{V_O}{V_{DC}} = \frac{\sin(\pi D)}{(1-D) \left[1 + j \left(\frac{X_{Lr} - X_{Cr}}{R_{ac}} \right) \right]} \quad (5.5)$$

Quality factor (Q) can be defined as

$$Q = \frac{\omega_r L_r}{R_{ac}} = \frac{1}{\omega_r C_r R_{ac}} \quad (5.6)$$

The angular resonant frequency ω_r is given by

$$\omega_r = 2\pi f_r = \frac{1}{\sqrt{L_r C_r}} \quad (5.7)$$

where f_r is the resonant frequency in Hz. By substituting (5.4) and (5.6) into (5.5), the gain of BB-FBSRC is obtained as

$$G_1 = \frac{V_O}{V_{DC}} = \frac{\sin(\pi D)}{(1-D) \left[1 + j \frac{\pi^2}{8} Q \left(\frac{f_s}{f_r} - \frac{f_r}{f_s} \right) \right]} \quad (5.8)$$

Similarly the gain of BB-HBSRC is obtained as

$$G_2 = \frac{V_O}{V_{DC}} = \frac{\sin(\pi D)}{2(1-D) \left[1 + j \frac{\pi^2}{8} Q \left(\frac{f_s}{f_r} - \frac{f_r}{f_s} \right) \right]} \quad (5.9)$$

and the gain of HBSRC is obtained as

$$G_3 = \frac{V_O}{V_{DC}} = \frac{\sin(\pi D)}{2 \left[1 + j \frac{\pi^2}{8} Q \left(\frac{f_s}{f_r} - \frac{f_r}{f_s} \right) \right]} \quad (5.10)$$

5.3.2 Switch Currents and Critical Inductance, L_{BBcr}

Analysis of soft switching operation and device peak current stress is based on the instantaneous values of switch currents. The current in resonant inductor, i_r at any instant for BB-FBSRC can be given as

$$i_{r1}(t) = \frac{4V_{DC}\sin(\pi D)\sin(\omega_s t + \alpha - \phi)}{(1-D)\pi Z_{in}} \quad (5.11)$$

where

$$\left. \begin{aligned} \phi &= \tan^{-1} \left(\frac{X_{Lr} - X_{Cr}}{R_{eff}} \right) \\ \alpha &= \tan^{-1} \left(\frac{\sin(2\pi D)}{1 - \cos(2\pi D)} \right) \\ Z_{in} &= R_{ac} + j(X_{Lr} - X_{Cr}) \end{aligned} \right\} \quad (5.12)$$

Similarly, the current, i_r at any instant for BB-HBSRC can be given as

$$i_{r2}(t) = \frac{2V_{DC}\sin(\pi D)\sin(\omega_s t + \alpha - \phi)}{(1-D)\pi Z_{in}} \quad (5.13)$$

and the current, i_r at any instant for HBSRC can be given as

$$i_{r3}(t) = \frac{2V_{DC}\sin(\pi D)\sin(\omega_s t + \alpha - \phi)}{\pi Z_{in}} \quad (5.14)$$

The average source current can be expressed in terms of average inductor current as [57]

$$I_{DC} \approx (I_{LBB} + I_r) \approx I_{LBB} \quad (5.15)$$

For 100% efficiency,

$$\begin{aligned} V_{DC}I_{DC} &= V_o I_o = P_o \\ \text{Hence, } I_{DC} &= \frac{P_o}{V_{DC}} \end{aligned} \quad (5.16)$$

The minimum and maximum currents in L_{BB} , are expressed as

$$I_{LBBmin} = I_{LBB} - \frac{\Delta i_{LBB}}{2} \quad (5.17)$$

$$I_{LBBmax} = I_{LBB} + \frac{\Delta i_{LBB}}{2} \quad (5.18)$$

where the inductor ripple, $\Delta i_{LBB} = (I_{LBBmax} - I_{LBBmin})$ is expressed as

$$\Delta i_{LBB} = \frac{V_{DC}DT}{L_{BB}} \quad (5.19)$$

Thus, by substituting (5.15), (5.16) and (5.19) in (5.17) and making $I_{LBBmin} = 0$, the critical inductance of BB inductor, L_{BBcr} is expressed as

$$L_{BBcr} = \frac{V_{DC}^2 D}{2P_o f_s} \quad (5.20)$$

where f_s is the switching frequency.

For continuous conduction, $L_{BB} > L_{BBcr}$.

The instantaneous current of L_{BB} can be expressed as

$$i_{LBB}(t) = \begin{cases} \frac{\Delta i_{LBB}}{DT}t + I_{LBBmin}, & 0 \leq t < DT \\ \frac{\Delta i_{LBB}}{(D-1)T}(t-DT) + I_{LBBmax}, & DT \leq t < T. \end{cases} \quad (5.21)$$

From Fig. 5.4a, the instantaneous currents in the switches can be expressed as below:

$i_{S1}(t)$ in BB-FBSRC and BB-HBSRC operation is

$$i_{S1}(t) = \begin{cases} 0, & 0 \leq t < DT \\ -(i_r(t) + i_{LBB}(t)), & DT \leq t < T \end{cases} \quad (5.22)$$

$i_{S1}(t)$ in HBSRC operation is

$$i_{S1}(t) = -i_r(t) \quad (5.23)$$

$i_{S2}(t)$ in BB-FBSRC and BB-HBSRC operation is

$$i_{S2}(t) = \begin{cases} (i_{LBB}(t) + i_r(t)), & 0 \leq t < DT \\ 0, & DT \leq t < T \end{cases} \quad (5.24)$$

$i_{S2}(t)=0$ in HBSRC operation.

$i_{S3}(t)$ in BB-FBSRC and HBSRC operation is

$$i_{S3}(t) = \begin{cases} i_r(t), & 0 \leq t < DT \\ 0, & DT < t \leq T \end{cases} \quad (5.25)$$

$i_{S3}(t)=0$ in BB-HBSRC operation.

$i_{S4}(t)$ in BB-FBSRC and HBSRC operation is

$$i_{S4}(t) = \begin{cases} 0, & 0 \leq t < DT \\ -i_r(t), & DT \leq t < T \end{cases} \quad (5.26)$$

$i_{S4}(t)$ in BB-HBSRC operation is

$$i_{S4}(t) = -i_r(t) \quad (5.27)$$

5.3.3 ZVS Condition

Due to the BB integration, along with resonant current i_r , the inductor current i_{LBB} also flows in the switches S_1 and S_2 . As both the currents are positive, the turn-ON current of switch S_1 , from (5.22) at $t = t_2 \approx DT$ is more negative. Thus, ZVS turn-ON can be inherently achieved by it. But, due to the difference of currents, i.e., positive current of i_{LBB} and negative current of i_r , the turn-ON current of switch S_2 from (5.24) at $t = t_5 \approx T$ is affected. Thus, for achieving ZVS turn-ON across the switches S_1 and S_2 , the ZVS criteria is considered with switch S_2 at $t = t_5 \approx T$ and is expressed as

$$C_{oss}V_{FB}^2 < \frac{1}{2}L_{BB}i_{LBB}^2(t_5) - \frac{1}{2}L_r i_r^2(t_5) \quad (5.28)$$

where C_{oss} is the output capacitance of MOSFET switches.

The condition of ZVS in (5.28) must be satisfied for all the voltage ranges in order to achieve ZVS turn-ON across S_1 and S_2 devices.

The switches S_3 and S_4 are independent of buck-boost operation. However, due to PWM control, ZVS turn-ON is affected for the switch operating for duration $<(T/2)$. For $D < 0.5$,

ZVS turn-ON of switch S_3 is affected and for $D > 0.5$, ZVS turn-ON of switch S_4 is affected. Thus, the ZVS criteria for $D < 0.5$, is considered with switch S_3 at $t = t_2 \approx DT$ in Fig. 5.4a and is expressed based on (5.25) as

$$C_{oss}V_{FB}^2 < \frac{1}{2}L_r i_r^2(t_2) \quad (5.29)$$

Similarly the ZVS criteria for $D > 0.5$, is considered with switch S_4 at $t = t_5 \approx T$ in Fig. 5.4a and is expressed as based on (5.26)

$$C_{oss}V_{FB}^2 < \frac{1}{2}L_r i_r^2(t_5) \quad (5.30)$$

If one of the above two equations which is having lower duty cycle among all the three configurations is satisfied, then S_3 and S_4 have ZVS turn-ON for all other configurations with different input voltages. Thus, if (5.28), (5.29) and (5.30) are satisfied, ZVS can be achieved across all the switches.

5.3.4 Conduction Losses

In the proposed converter, the rectifier diodes are soft switched and ZVS turn-ON is achieved in the switches due to the series resonance. The switch turn-OFF losses are less. Hence, the main losses in the proposed converter are conduction losses in the switches and diodes. These conduction losses play a vital role in estimating the efficiency of the converter. The current expressions for estimating the conduction losses are expressed as below. The peak current of i_r in BB-FBSRC is given by

$$I_{r1_max} = \frac{4V_{DC}\sin(\pi D)}{(1-D)\pi Z_{in}} \quad (5.31)$$

Similarly for BB-HBSRC

$$I_{r2_max} = \frac{2V_{DC}\sin(\pi D)}{(1-D)\pi Z_{in}} \quad (5.32)$$

and for HBSRC

$$I_{r3_max} = \frac{2V_{DC}\sin(\pi D)}{\pi Z_{in}} \quad (5.33)$$

The inductor current, i_{LBB} flowing in BB-FBSRC and BB-HBSRC can be split into AC rms and DC currents and expressed as below.

$$I_{LBB_DC} = I_{LBB} = \frac{P_o}{V_{DC}}; \quad I_{LBB_AC} = \Delta i_{LBB} \sqrt{\frac{1}{12}} \quad (5.34)$$

In BB-FBSRC, the currents i_r and i_{LBB} flows in S_2 for a duration of DT and then flows in S_1 for the remaining duration. Similarly, the current i_r flows in S_4 for a duration of DT and then flows in S_3 for the remaining duration. Thus, the total conduction losses of the 4 switching devices can be given as [99]

$$P_{1_cond_Switches} = (I_{r1_max}^2 + I_{LBB_DC}^2 + I_{LBB_AC}^2)r_{DS} \quad (5.35)$$

where r_{DS} is the MOSFET drain to source ON resistance.

In BB-HBSRC, the currents i_r and i_{LBB} flows in S_2 for a duration of DT and then flows in S_1 for the remaining duration. Further, the S_3 is continuously OFF and S_4 is continuously ON carrying the current of i_r in it. Thus, the total conduction losses of the three switching devices can be given as

$$P_{2_cond_Switches} = (I_{r2_max}^2 + I_{LBB_DC}^2 + I_{LBB_AC}^2)r_{DS} \quad (5.36)$$

In HBSRC, S_1 is continuously ON carrying the current of i_r in it and S_2 is continuously OFF. Also, the current i_r flows in S_4 for a duration of DT and then flows in S_3 for the remaining duration. Thus, the total conduction losses of the three switching devices can be given as

$$P_{3_cond_Switches} = (I_{r3_max}^2)r_{DS} \quad (5.37)$$

The rectifier diode conduction losses in all the three configurations can be expressed as

$$P_{cond_Diodes} = 2V_f I_o + \frac{\pi^2 I_o^2 R_f}{4} \quad (5.38)$$

where V_f and R_f are the diode forward offset voltage and diode forward resistance respectively.

5.4 Design Considerations

5.4.1 Design Parameters for LED Lamp

The LEDs used for experimentation are TMX HP3W white LEDs. Each LED considered is having a V_{th} of 2.321 V. Two strings of 7 LEDs each are considered to design a load of 22.77 W/22.505 V that results in a V_{th} of 16.247 V and a current of 1.012 A.

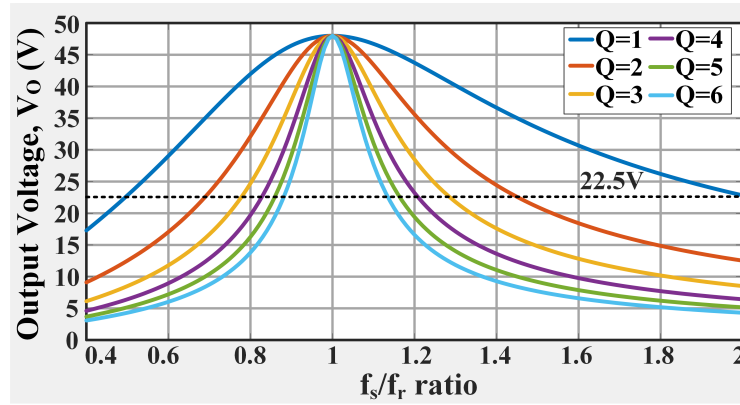


Figure 5.6: LC resonance characteristics

5.4.2 Resonant Elements and D Limits of HBSRC

The input voltage and resonant elements are selected based on HBSRC configuration, as this topology is simple without buck-boost operation integrated. In order to operate an LED load with voltage V_o of 22.5 V in all the three configurations, the input voltage V_{DC} is selected as 96 V with the converter operating as HBSRC at $D=50\%$. The design of resonant elements is similar to conventional procedure. From (5.10), the output voltage versus nominal frequency, $\left(\frac{f_s}{f_r}\right)$ has been plotted at $D = 50\%$ with different Q values as shown in Fig. 5.6. To obtain the required V_o of 22.5 V with V_{DC} of 96 V, from the graph, the Q -factor, frequency ratio $\left(\frac{f_s}{f_r}\right)$ are selected as 4.14 and 1.2 respectively. With f_s of 200 kHz and the ratio f_s/f_r as 1.2, L_r is obtained as 88 μH from (5.4) and (5.6). From (5.7), the L_r and C_r product can be expressed as

$$L_r C_r = 0.91344 \times 10^{-12} \quad (5.39)$$

From (5.39), C_r is obtained as 10.31 nF. The turn-ON currents of switches S_3 and S_4 are estimated from the instantaneous current equations (5.25) and (5.26) at $t \approx DT$ and $t \approx T$ respectively. Fig. 5.7a shows the variation of switch turn-ON currents of S_3 and S_4 with duty cycle variation. As can be observed, ZVS turn-ON is affected for the switch operating for duration $<(T/2)$. As the switch currents are symmetrical to each other, for $D < 0.5$, ZVS turn-ON of switch S_3 is affected and for $D > 0.5$, ZVS turn-ON of switch S_4 is affected. The safe duty cycle operating region for ZVS turn-ON for the switches S_3 and S_4 is $0.2 < D < 0.8$ as shown in Fig. 5.7a with HBSRC and is true even for BB-FBSRC and BB-HBSRC. Thus, the HBSRC is operated from 96 V at $D=0.5$ to 120 V at $D=0.3$.

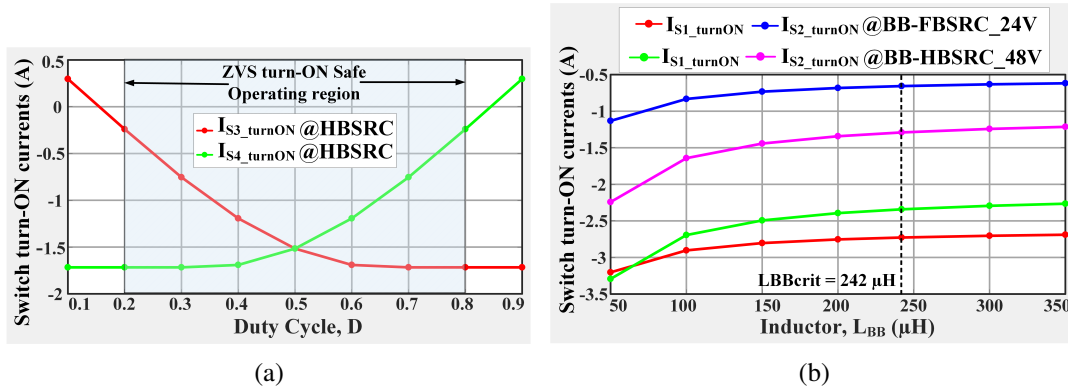
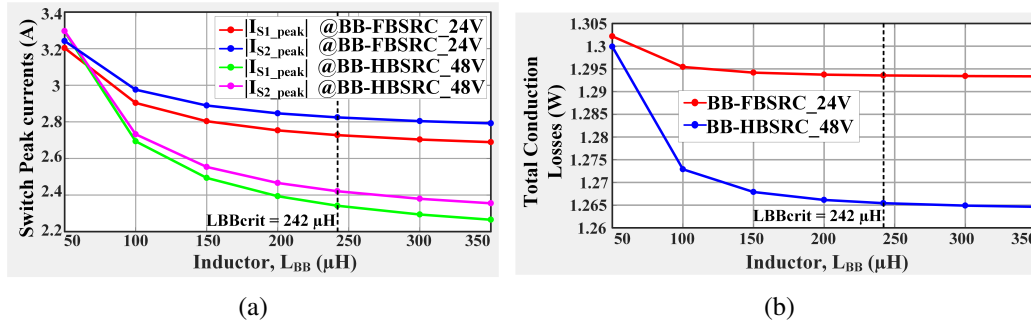
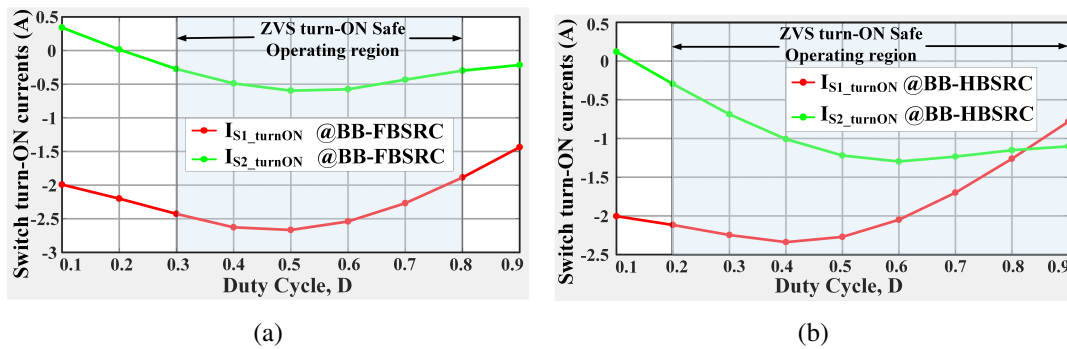


Figure 5.7: ZVS condition of switches (a) S_3 and S_4 under duty cycle variation in HBSRC (b) S_1 and S_2 with different L_{BB} values in BB-FBSRC and BB-HBSRC at $D = 50\%$

5.4.3 Computing L_{BB} , and D Limits of BB-FBSRC and BB-HBSRC

The input voltage V_{DC} of BB-FBSRC and BB-HBSRC at $D=50\%$ is computed from (5.8) and (5.9) respectively with same resonant circuit parameters to produce V_o of 22.5 V.

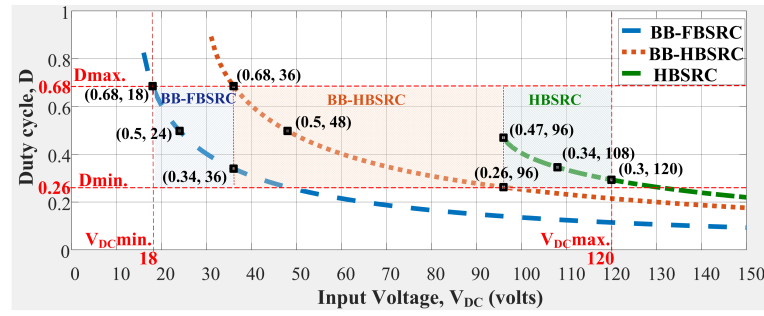
In BB-FBSRC and BB-HBSRC configurations, the ZVS operation of switches S_1 and S_2 is affected as these devices are integrated with BB operation. Fig. 5.7b shows the turn-ON currents of switches S_1 and S_2 for different values of L_{BB} under BB-FBSRC and BB-HBSRC operation with $V_{DC}=24$ V and 48 V respectively at $D = 0.5$. The turn-ON currents of switches S_1 and S_2 are estimated from the instantaneous current equations (5.22) and (5.24) at $t \approx DT$ and $t \approx T$ respectively. It can be observed from Fig. 5.7b that the switch S_2 is having less negative current compared to S_1 and hence, ZVS turn-ON in S_2 ensures the same in S_1 . Also, it can be observed that as L_{BB} increases beyond L_{BBcr} the turn-ON currents remain almost constant. But, as L_{BB} decreases less than L_{BBcr} , the switch currents decrease and become more negative. Hence, ZVS turn-ON capability increases. The absolute values of peak currents in the switches S_1 and S_2 are estimated from (5.22) and (5.24) in the range of $0 \leq t < T$ and using which, the corresponding conduction losses are estimated from (5.35), (5.36) and (5.38). Fig. 5.8 shows the peak currents of S_1 and S_2 and the total conduction losses of the converter for different values of L_{BB} under BB-FBSRC and BB-HBSRC operation with $V_{DC}=24$ V and 48 V respectively at $D = 0.5$. It can be observed that even though ZVS capability increases with $L_{BB} < L_{BBcr}$, the switch peak currents and hence, the conduction losses are increasing. Beyond L_{BBcr} , the switch peak currents and conduction losses are almost constant. This is true even with other input voltages. Thus, to have better efficiency, L_{BB} is chosen as $262 \mu H$ which is a little more than L_{BBcr} . However, even a lesser value of L_{BB} can be chosen if the converter is to be compact in size as there is no much deviation in the losses. Fig. 5.9 shows the turn-ON currents in

Figure 5.8: With different values of L_{BB} (a) Switch peak currents (b) Total conduction lossesFigure 5.9: ZVS condition with duty cycle variation across switches (a) S_1 and S_2 in BB-FBSRC (b) S_1 and S_2 in BB-HBSRC

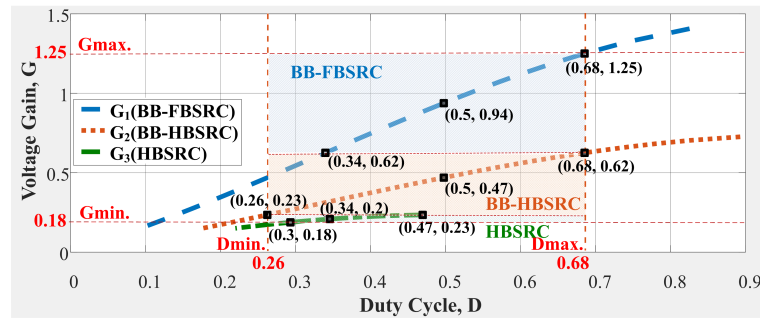
switches S_1 and S_2 with BB-FBSRC and BB-HBSRC operation at different duty cycles with $L_{BB} = 262 \mu H$. It can be observed from Fig. 5.9a, the safe range of duty cycle for ZVS turn-ON for BB-FBSRC is $0.3 < D < 0.8$. Similarly, from Fig. 5.9b, this range is obtained for BB-HBSRC as $0.2 < D < 0.9$. Hence, the range of input voltage for BB-FBSRC is selected as 18 V to 36 V with $D=0.68$ to 0.34 . The range of input voltage for BB-HBSRC is selected as 36 V to 96 V with $D=0.68$ to 0.26 . Fig. 5.10a shows the input voltage, V_{DC} vs duty cycle, D variation for all the three configurations. Hence, the selected duty cycle limits result in better control of the input voltages and provide ZVS turn-ON of the switches in all the three configurations. Fig. 5.10b shows the duty cycle vs gain variation, in which it can be observed that there is a wide variation in the voltage gain and even it is above and below unity, producing buck/boost modes. Thus, the converter is operated optimally.

5.4.4 Selection of MOSFET Switches

The drain-source peak voltage of the switches is the voltage, V_{FB} applied to the inverter. Fig. 5.11a shows the switch drain-source peak voltages in the entire input voltage range under

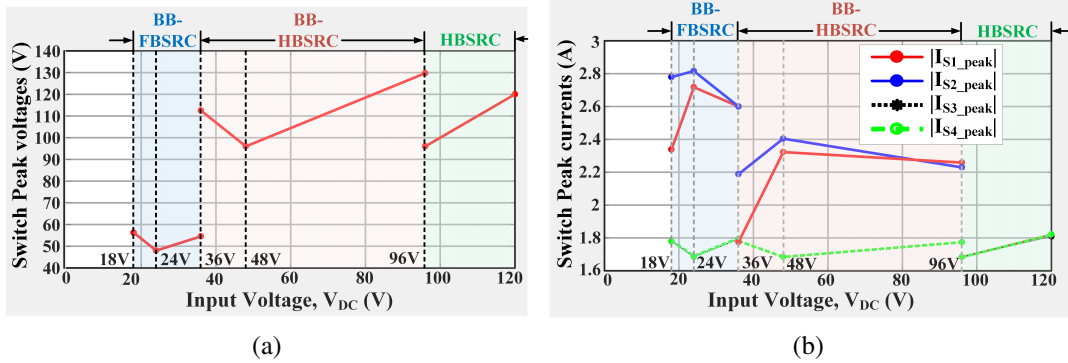


(a)



(b)

Figure 5.10: (a) Variation of duty cycle with respect to input voltage variation (b) Variation of voltage gain with respect to duty cycle variation



(a)

(b)

Figure 5.11: In all the voltage ranges (a) Variation of switch drain-source peak voltages (b) Variation of switch drain-source peak currents

different configurations. The peak voltages are equal for all the switches at particular input voltage level and zero for the switch which is continuously ON. In BB-FBSRC, the switches (S_1 to S_4) have a maximum drain to source voltage of $V_{FB} = 56.25V$ at $V_{DC} = 18V$ and $D = 0.68$. Similarly in BB-HBSRC, the switches (S_1, S_2, S_4) have a maximum drain to source voltage of $V_{FB} = 131V$ at $V_{DC} = 96V$ and $D = 0.26$. However, in HBSRC, the drain to source voltage applied is only $V_{FB} = V_{DC}$ as $V_{BB} \approx 0$. Thus, in HBSRC, The maximum voltage across the switches (S_2, S_3, S_4) is the maximum input voltage, V_{DC} i.e., 120 V. Hence, the switches, S_1 ,

Table 5.1: Design parameters

Parameters	Values
DC Input voltage, V_{DC}	18-120 V
Switching frequency, f_s	200 kHz
Resonant frequency, f_r	166.53 kHz
Resonant inductor, L_r	88 μ H
Resonant capacitor, C_r	10 nF
Output capacitor, C_o	5 μ F
Output voltage, V_o	22.505V
Output current, I_o	1.012 A
Output power, P_o	22.77 W
Buck-boost inductor, L_{BB}	260 μ H
Buck-boost capacitor, C_{BB}	15 μ F
PWM dimming frequency	200 Hz
MOSFETs	IRFP250N
Diodes	MBR20200CT

S_2 and S_3 have maximum peak voltage stress of 131 V and the switch S_4 has maximum peak voltage stress of 120 V. Hence, the peak voltage stress across switches is not high, and is on par with the input voltage applied. The absolute values of peak currents in the switches S_1 and S_4 are estimated from (5.22), (5.23), (5.24), (5.25), (5.26) and (5.27) in the range of $0 \leq t < T$. Fig. 5.11b shows the absolute values of switch peak drain currents in the entire input voltage range under different configurations. It can be observed that the switch peak currents are more in BB-FBSRC configuration due to the increased buck-boost average current, I_{LBB} with less input voltage. The maximum peak currents in the switches are in the range of 1.8 A to 2.8 A. Thus, it can be observed from the figure that the variation in peak currents in switches S_3 and S_4 is very less in each configuration and they are almost the same magnitude in all the configurations. As buck-boost current also flows in switches S_1 and S_2 , the peak currents increase a bit, compared with currents in S_3 and S_4 , however, they are not of high value. Thus, the peak current stress in the switches is not high and it is at a reasonable value. Based on the peak voltages and currents, the MOSFET switches IRFP250NPbF are selected in the proposed configuration having r_{DS} of 75 m Ω .

5.5 Simulation and Experimental Results

The proposed configuration is simulated and tested for the input voltage range of 18 V to 120 V. The corresponding operating voltage range and duty cycle of particular configuration are considered as in Fig. 5.10a with the parameters shown in Table 5.1. Fig. 5.12 shows the

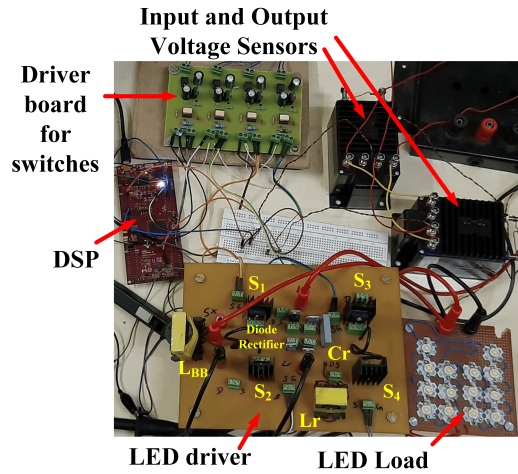
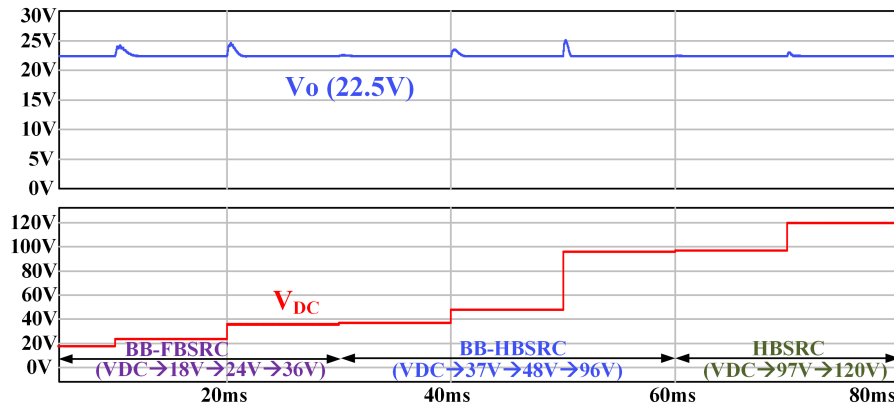


Figure 5.12: Experimental setup of the proposed LED driver

Figure 5.13: Simulated dynamic behavior of proposed configuration with $V_{DC} = 18 \text{ V}$ to 120 V

experimental setup of the proposed LED driver. CV 3-200/SP6 and CV 3-500 voltage sensors are used for input and output voltage sensing. DSP-TMS320F28379D is used for generating the gate signals using closed loop control. Proposed converter closed loop behavior is simulated in PSim Software. Fig. 5.13 shows the simulated dynamic behavior of the proposed configuration with V_{DC} varying from 18V to 120V, where the proposed configuration shows that it can well re-configure in different configurations based on the input voltage range and well regulated within particular reconfiguration. Fig. 5.14 shows the experimental dynamic behavior of the proposed configuration while transforming from one configuration to another based on the input voltage. Fig. 5.15 shows the experimental dynamic behavior of proposed converter in each configuration. As can be observed, there is significantly less overshoot and faster response compared with simulation results which indicate that the proposed converter is stable even under dynamic conditions. Thus, proposed converter can smoothly transform from one configuration to another and can well regulate the output voltage in each configuration, thus regulates the output voltage

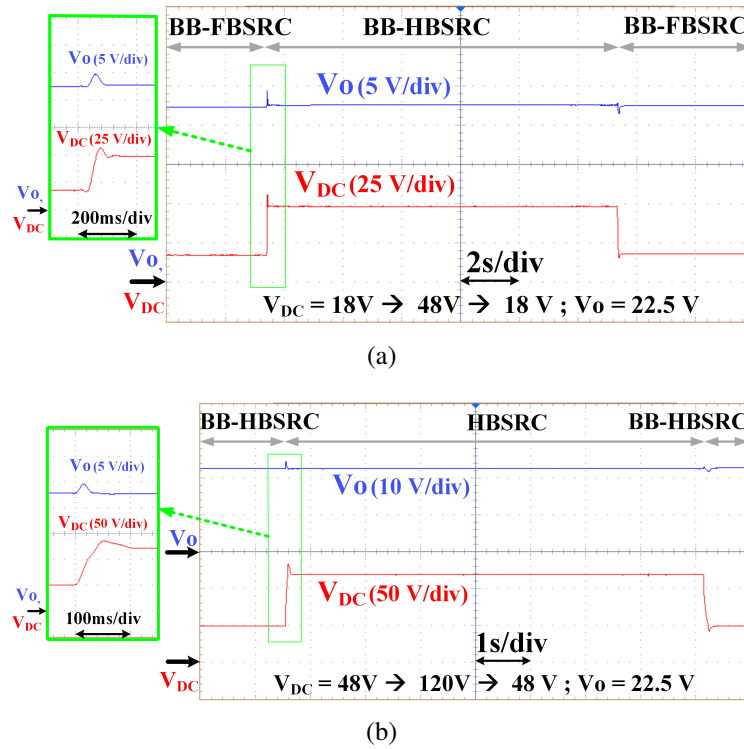
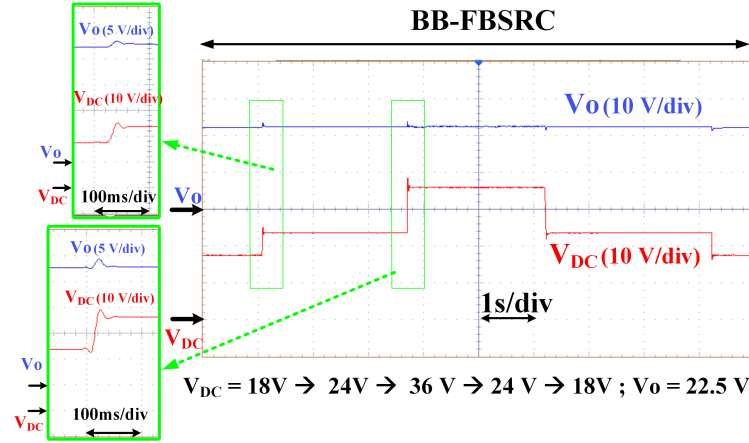
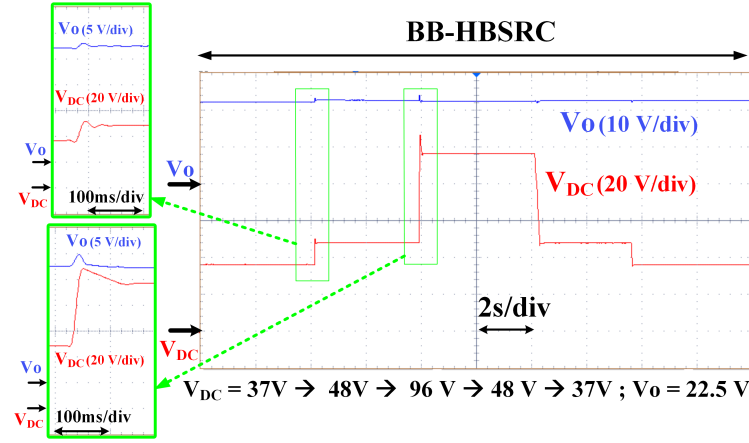


Figure 5.14: Experimental dynamic behavior of proposed configuration under different reconfigurations with: (a) $V_{DC} = 18V-48V-18V$ (BB-FBSRC to BB-HBSRC to BB-FBSRC) (b) $V_{DC} = 48V-120V-48V$ (BB-HBSRC to HBSRC to BB-HBSRC)

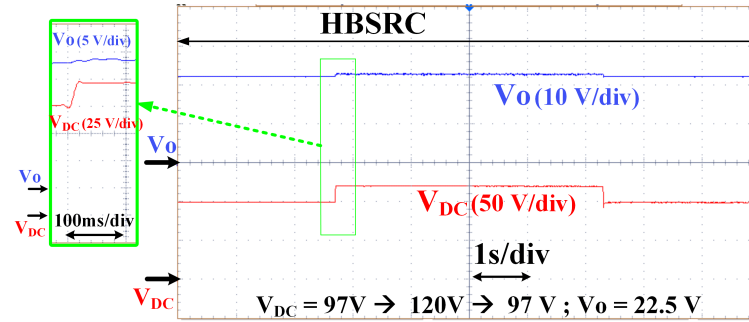
for the wide input voltage variation from 18V to 120V. To know the exact behavior of the proposed converter in steady state, it is simulated in PSpice software. Fig. 5.16 to Fig. 5.24 show the simulation and experimental waveforms of the proposed converter in steady state. The simulation and experimental results of BB-FBSRC with $V_{DC} = 24V, 18V, 36V$ and corresponding duty cycle as 50%, 68%, 34% respectively are shown in Fig. 5.16 to Fig. 5.19. Fig. 5.16 shows the waveforms of v_{BB} , i_{LBB} , \bar{v}_{A1-A2} and i_r at various input voltages. Fig. 5.17 to Fig. 5.19 shows the waveforms of Drain to Source voltages, $v_{S1}-v_{S4}$ and Drain currents, $i_{S1}-i_{S4}$ of switches S_1-S_4 at various input voltages. The ZVS turn-ON across the devices is observed and ZCS turn-OFF is partially achieved for the above voltages, thus soft-switching is achieved by the BB-FBSRC for the voltage range of 18 V to 36 V. The simulation and experimental results of BB-HBSRC with $V_{DC} = 48V, 36V, 96V$ and corresponding duty cycle as 50%, 68%, 26% respectively are shown in Fig. 5.20 to Fig. 5.22. As ZVS turn-OFF across the devices is observed and ZCS turn-ON is partially achieved for the above voltages, thus soft-switching is achieved by the BB-HBSRC for the voltage range of 36 V to 96 V. The simulation and experimental results of HBSRC with $V_{DC} = 96V$ and 120 V, corresponding duty cycle as 50% and 30% respectively are shown in Fig. 5.23 and Fig. 5.24. As ZVS turn-OFF across the devices is observed and



(a)



(b)



(c)

Figure 5.15: Experimental dynamic behavior of proposed configuration in: (a) BB-FBSRC with $V_{DC} = 18V-24V-36V-24V-18V$ (b) BB-HBSRC with $V_{DC} = 37V-48V-96V-48V-37V$ (c) HBSRC with $V_{DC} = 96V-120V-96V$

ZCS turn-ON is partially achieved for the above voltages, thus soft switching is achieved by the HBSRC for the voltage range of 96 V to 120 V. As discussed in section-III(c), the peak currents of S_1 and S_2 are varying in BB-FBSRC and BB-HBSRC as they have to carry i_{LBB} along with

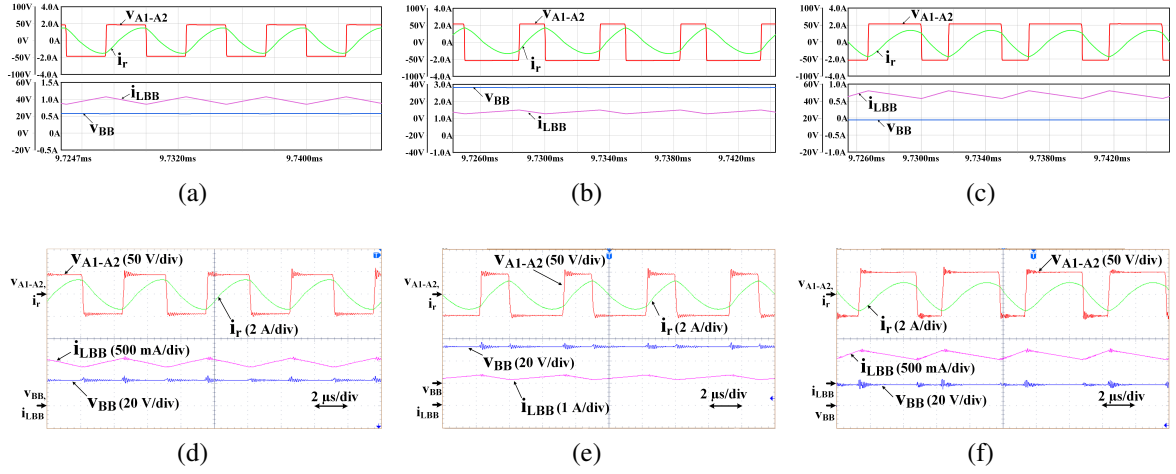


Figure 5.16: Waveforms of \bar{v}_{A1-A2} , i_r , v_{BB} and i_{LBB} in BB-FBSRC at V_{DC} : (a) 24 V through simulation (b) 18 V through simulation (c) 36 V through simulation (d) 24 V through experimentation (e) 18 V through experimentation (f) 36 V through experimentation

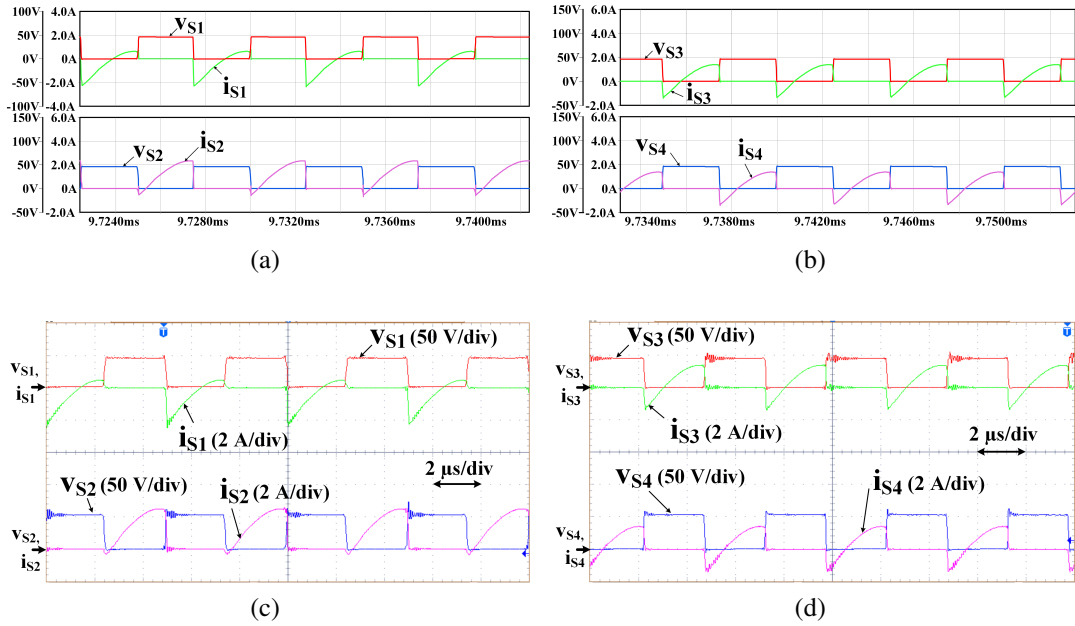


Figure 5.17: Voltage and current waveforms of switches in BB-FBSRC at V_{DC} of 24V through: (a) S_1 , S_2 through Simulation (b) S_3 , S_4 through Simulation (c) S_1 , S_2 through Experimentation (d) S_3 , S_4 through Experimentation

i_r and the switch S_2 is more sensitive to ZVS turn-ON. Also, as discussed, the switches S_4 for $D > 50\%$ and S_3 for $D < 50\%$ are sensitive with respect ZVS turn-ON in BB-FBSRC and HB-SRC configuration. However, irrespective of inductor current and duty cycle modulation, the proposed converter achieves ZVS turn-ON across all the switches. Further, the simulation and experimental results are in good agreement.

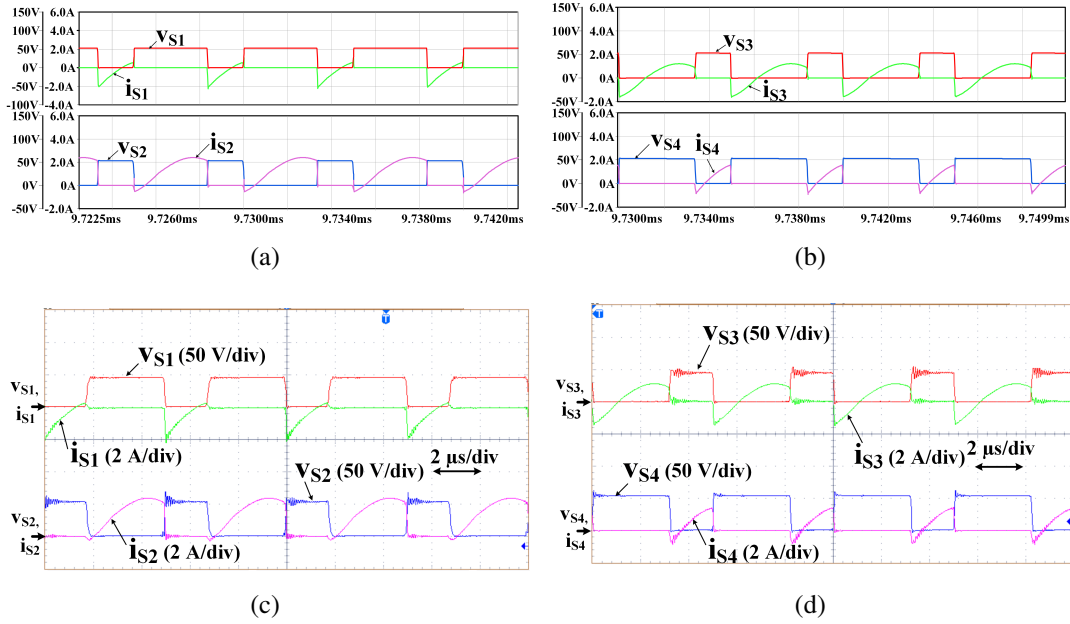


Figure 5.18: Voltage and current waveforms of switches in BB-FBSRC at V_{DC} of 18V through: (a) S_1, S_2 through Simulation (b) S_3, S_4 through Simulation (c) S_1, S_2 through Experimentation (d) S_3, S_4 through Experimentation

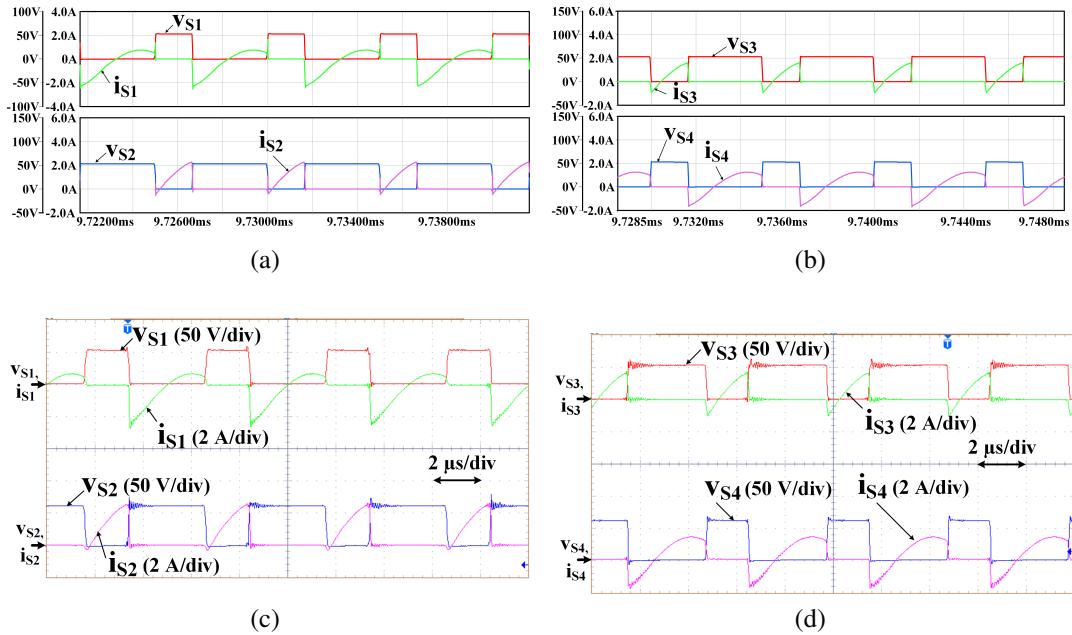


Figure 5.19: Voltage and current waveforms of switches in BB-FBSRC at V_{DC} of 36V through: (a) S_1, S_2 through Simulation (b) S_3, S_4 through Simulation (c) S_1, S_2 through Experimentation (d) S_3, S_4 through Experimentation

In the proposed LED driver, dimming is implemented using PWM technique to regulate the illumination of the LED lamp, where the inverter is turned ON and OFF with a low dimming

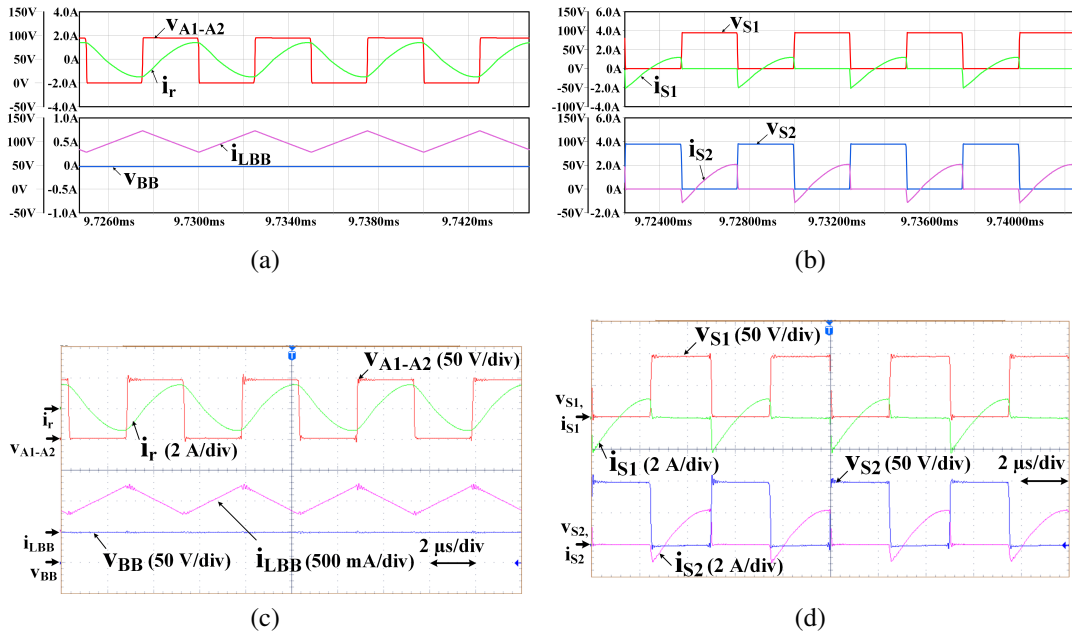


Figure 5.20: Waveforms of voltages, currents in BB-HBSRC at $V_{DC}=48V$: (a) \bar{v}_{A1-A2} , i_r , v_{BB} , i_{LBB} through simulation (b) S_1 , S_2 through simulation (c) \bar{v}_{A1-A2} , i_r , v_{BB} , i_{LBB} through experimentation (d) S_1 , S_2 through experimentation

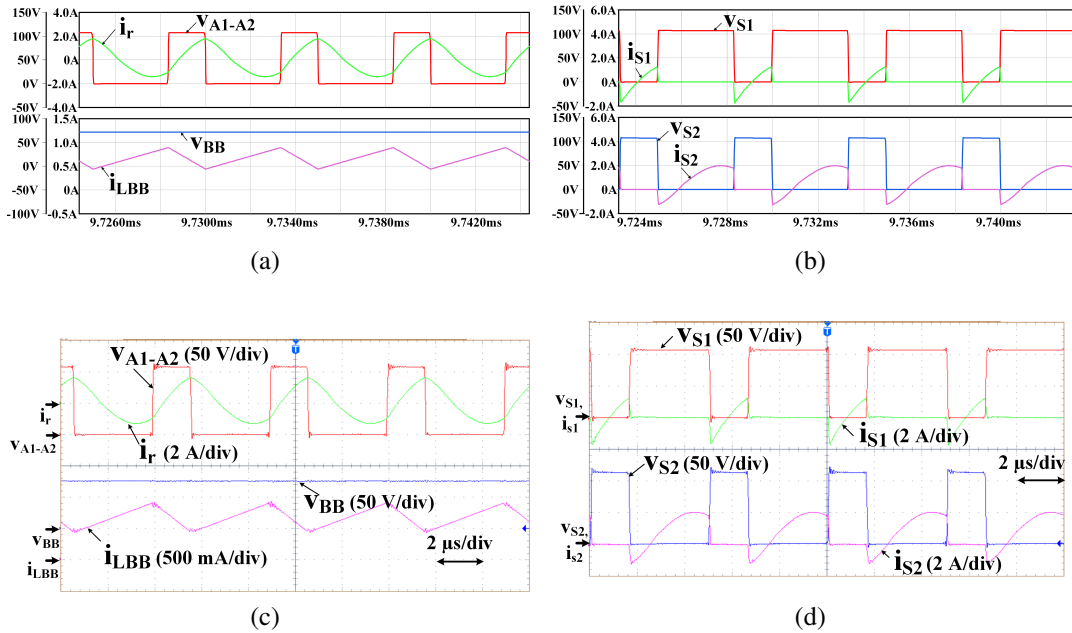


Figure 5.21: Waveforms of voltages, currents in BB-HBSRC at $V_{DC}=36V$: (a) \bar{v}_{A1-A2} , i_r , v_{BB} , i_{LBB} through simulation (b) S_1 , S_2 through simulation (c) \bar{v}_{A1-A2} , i_r , v_{BB} , i_{LBB} through experimentation (d) S_1 , S_2 through experimentation

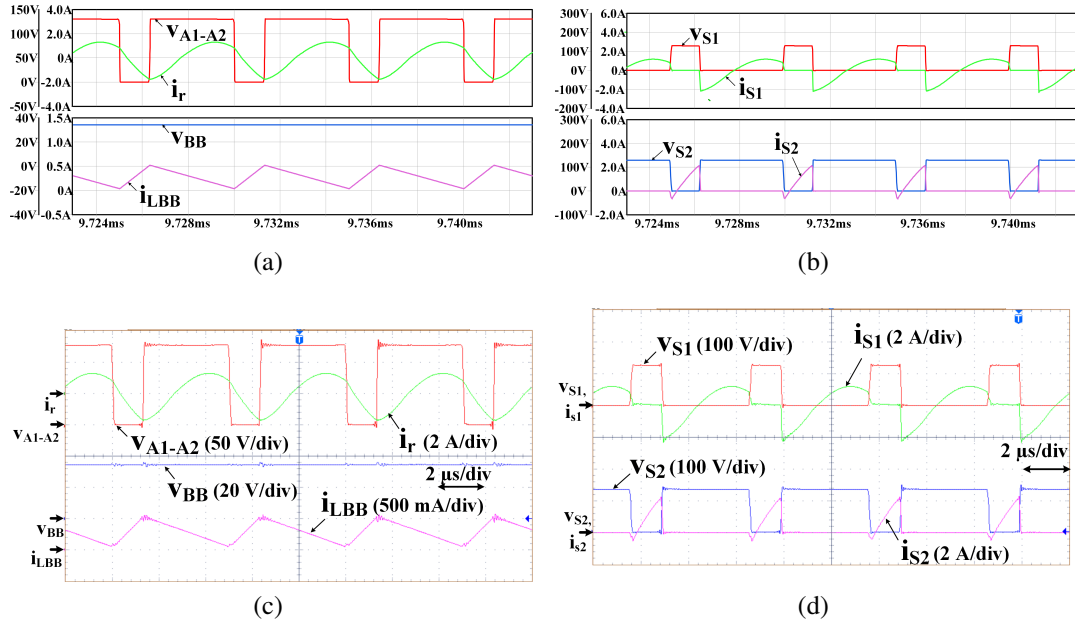


Figure 5.22: Waveforms of voltages, currents in BB-HBSRC at $V_{DC}=96V$: (a) \bar{v}_{A1-A2} , i_r , v_{BB} , i_{LBB} through simulation (b) S_1 , S_2 through simulation (c) \bar{v}_{A1-A2} , i_r , v_{BB} , i_{LBB} through experimentation (d) S_1 , S_2 through experimentation

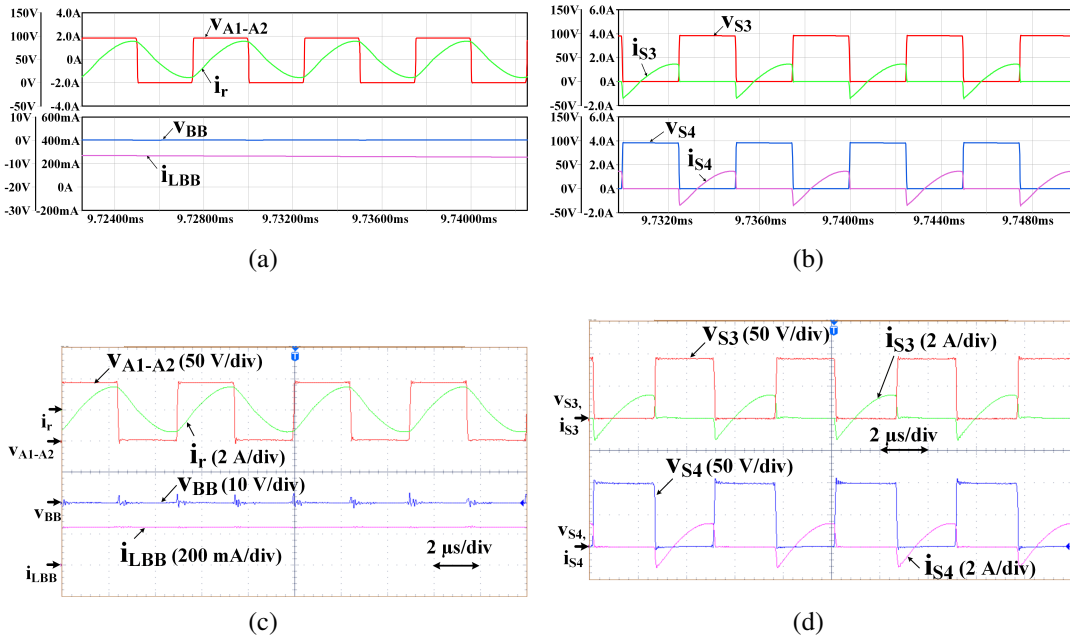


Figure 5.23: Waveforms of voltages, currents in HBSRC at $V_{DC}=96V$: (a) \bar{v}_{A1-A2} , i_r , v_{BB} , i_{LBB} through simulation (b) S_3 , S_4 through simulation (c) \bar{v}_{A1-A2} , i_r , v_{BB} , i_{LBB} through experimentation (d) S_3 , S_4 through experimentation

frequency. Thus, without disturbing the operating point of the LED lamp, its average current is regulated. The dimming operation is achieved in all the three configurations with a frequency

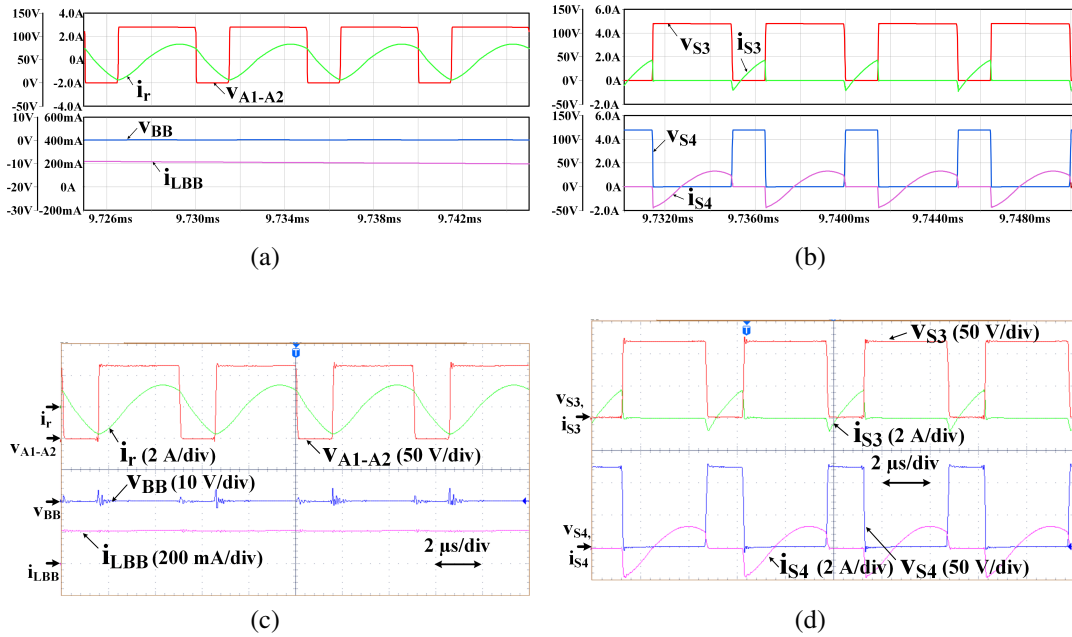


Figure 5.24: Waveforms of voltages, currents in HBSRC at $V_{DC}=120V$: (a) \bar{V}_{A1-A2} , i_r , V_{BB} , i_{LBB} through simulation (b) S_3 , S_4 through simulation (c) \bar{V}_{A1-A2} , i_r , V_{BB} , i_{LBB} through experimentation (d) S_3 , S_4 through experimentation

of 200 Hz. Fig. 5.25 shows the experimental results of LED voltage and current at 40% and 80% dimming levels for BB-FBSRC, BB-HBSRC and HBSRC at $V_{DC}= 24 V$, 48 V and 96 V respectively. Similarly, dimming control can be implemented when the converter operated for other input voltage ranges.

5.6 Efficiency and Comparative Study

The total conduction losses of the switches and diodes are estimated using (5.35)-(5.38) and efficiency curve for the entire input voltage range of 18V to 120V has been plotted as shown in Fig. 5.27a. Further, loss analysis using thermal modeling has been carried out in PSim Software. Fig. 5.26 shows the simulated loss analysis across switches for the entire input voltage range. The total diode losses obtained through simulation is same in entire voltage range and is 1.33 W. Corresponding efficiency curve is shown in Fig. 5.27a. As the turn-OFF switching losses are also accounted in simulation, the simulated efficiency is low compared with theoretical efficiency. Fig. 5.27a also shows the practical measured efficiency. As there are core and winding losses also in practical, the experimental efficiency is little less compared to simulation efficiency. The efficiency is around 92% to 94%. Thus, the proposed converter achieves high efficiency in all the configurations. Fig. 5.27b shows the efficiency curve of all the three configurations with 50% duty cycle at different dimming levels. It can be noticed that

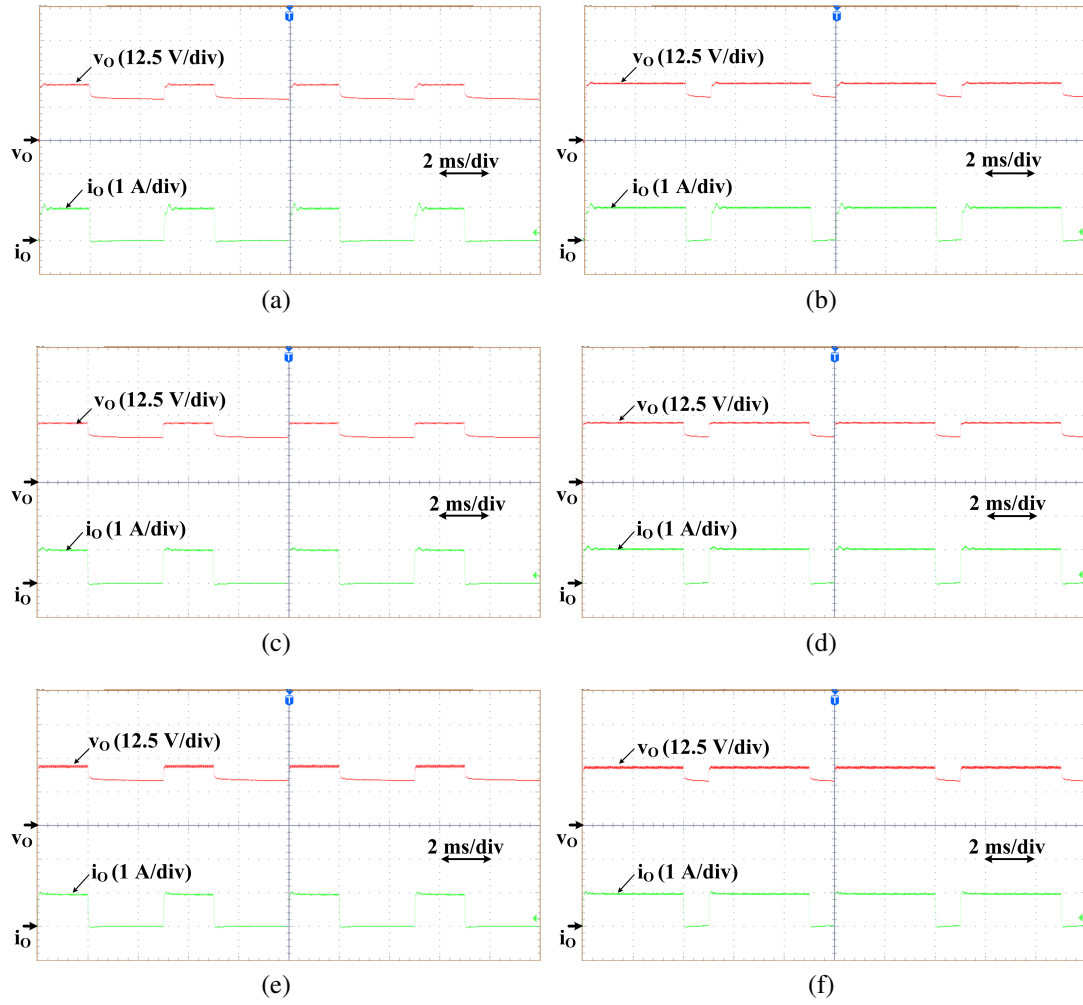


Figure 5.25: Experimental dimming waveforms of v_O , i_O : (a) BB-FBSRC with 24 V input: 40% dimming (b) BB-FBSRC with 24 V input: 80% dimming (c) BB-HBSRC with 48 V input: 40% dimming (d) BB-HBSRC with 48 V input: 80% dimming (e) HBSRC with 96 V input: 40% dimming (f) HBSRC with 96 V input: 80% dimming

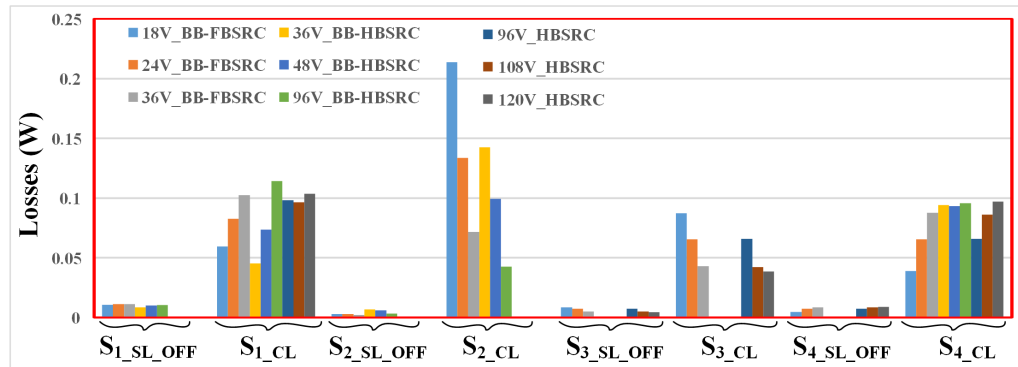


Figure 5.26: Simulated loss analysis of proposed configuration under different input voltages in different reconfigurations

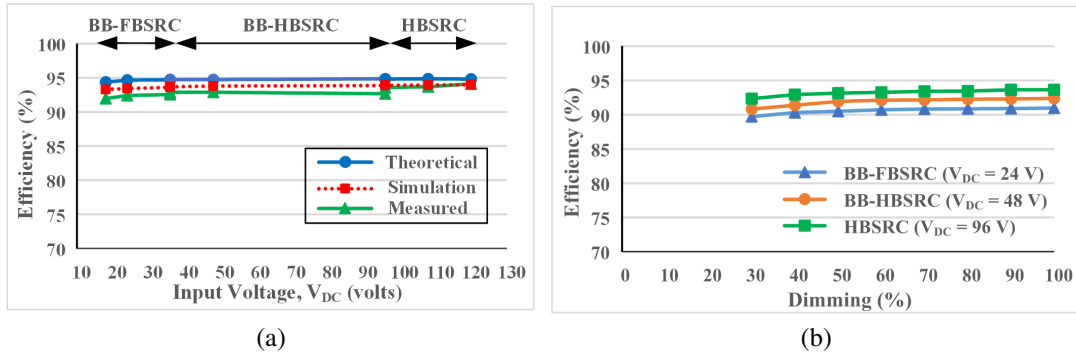


Figure 5.27: Efficiency curve with respect to (a) input voltage variations under different recon-figurations (b) dimming with all the three configurations for 50% duty cycle

Table 5.2: Comparison of wide input LED drivers

Topologies	JSSC 2015 [71]	LM3405 2016 [72]	TIE 2017 [66]	TCAS1 2018 [74]	TPE 2019 [75]	Proposed
Process	0.35 μ m CMOS	N.A.	NA	0.5 μ m CMOS	0.13 μ m BCDLite	NA
Input Voltage (V)	5-45	3-15	7-45	5-115	6-18	18-120
Switching Mode	Hard-Switching	Hard-Switching	Hard-Switching	Auto Configurable Hard/Soft Switching	Soft-Switching	Soft-Switching
Average LED current (mA)	700	1000	1000	350	500-1300	1000
Max. Output Power (W)	26	15	25	25	12	22.77
Switching Frequency	4MHz	1.6MHz	500kHz	2.2MHz and 1.6MHz	2.8MHz	200 kHz
Inductor (μ H)	8.2-39	6.8 & 22	10	10	0.68-1	88 & 260
Dimming Frequency	20kHz	20kHz	1kHz	20kHz	20kHz	200 Hz
Max. Power Efficiency	97.2	91	82-96	92.6 and 94.4	96.1	91.8-94.19

the efficiency is nearly constant in all the three configurations.

The proposed configuration is compared with existing LED drivers that operate for wide input applications as shown in table 5.2. The component count is less in these topologies. But in [66,69,70,100], the converters are operated with hard switching, that either reduces the power density or increases the switching losses. Also, in [69,70,73], CMOS, BDCLite technologies are implemented that increases the cost and complexity. Thus, compared with existing LED drivers, the proposed driver provides benefits like wider voltage gain and ZVS under wide input

Table 5.3: Comparison of wide input soft switched converters

Structure	S	D	L	C	T/F	Sec. Win.	Mod.	Rated Power	Input Voltage Range (V)	Range of Switching Frequency	Eff. (%)	Gain Range
Isolated Buck-Boost Converter [79]	8	4	1	4	1	1	PS	380 V/ 800 W	100-400	60 kHz	97.61	0.35-1.4
PWM Resonant Converter [80]	5	1	2	4	1	1	PWM	380 V/ 300 W	25-35	135 kHz	98.9	1.97-2.76
Multilevel LCC Resonant Converter [82]	8	4	1	3	2	1	PWM	5k V/ 100 kW	40-75	50 kHz	–	0.95-2.85
Active Boost Rectifier based Converter [85]	6	0	2	3	1	1	Double Pulse	380 V/ 300 W	25-35	140 kHz	98.61	1.73-2.43
Structure-Reconfigurable Series Resonant Converter [91]	7	3	1	3	1	1	PWM	200 V, 400 V/ 500 W	30-60	100 kHz	95.4	0.5-2
Interleaved Boost+ FB LLC [81]	4	2	3	4	1	2	PWM	24 V/ 600 W	120-240	100 kHz	96	0.007-0.014
Buck-boost + HB LLC [57]	4	0	2	3	1	2	PWM	15 V/ 300 W	36-72	100 kHz	93.96	0.8-1.64
Buck-Boost+ HB LCC [58]	2	4	3	4	1	1	PWM+ PFM	48 V/ 500 W	100-200	98-118 kHz	94	0.432-0.864
4-switch Buck-Boost + FB LLC [92]	6	0	2	3	1	2	PWM	24 V/ 720 W	250-420	1 MHz	96.4	0.116-0.224
Proposed Converter	4	4	2	3	0	0	PWM	22.5 V/ 22 W	18-120	200 kHz	94.19	0.18-1.25

S -No. of Switches, D -No. of Diodes, L -No. of Inductors, C -No. of Capacitors, T/F -No. of Transformers
Sec. Win. -No. of Secondary Windings, Mod. - Modulation, Eff. - Efficiency

variations, thus, results in reduced switching losses and high efficiency with easier implementation. Also, the proposed configuration is compared with existing wide input soft-switched converters as shown in table 5.3, where the internal voltage gain of the converters without transformer is compared along with the component count, modulation, voltage range, efficiency, etc. It is evident from the table 5.3, that the proposed configuration provides various benefits such as: smooth transformation into 3 different topologies without any additional switching devices, no topological transitions within a switching cycle in steady state, transformer less, compact in size, soft switching and wider voltage gain with buck/boost operation and use of simple PI controller in contrast to these topologies.

5.7 Summary

In this chapter, a reconfigurable non-isolated BB integrated FB SRC resonant converter based LED driver has been proposed for wide input automotive applications. BB converter

operation has been integrated with FBSRC and hence can be reconfigured as BB-FBSRC, BB-HBSRC and HBSRC achieving three different levels of voltage gains. APWM technique has been employed for voltage regulation. Based on the input voltage range, the converter transforms to one of the three configurations and the corresponding PI controller regulates the output voltage against variations in the input voltage. The proposed converter has been analyzed with respect to the design, conduction losses and voltage and current stress in the devices. The performance has been verified with both simulation and experimental results. It is observed that the proposed configuration smoothly transforms from one configuration to other and can provide voltage regulation with soft switching across the devices in the entire voltage range. Also, the proposed configuration has been compared with existing wide input LED drivers and with similar wide input soft-switched converters. It provides various benefits such as: smooth transformation into 3 different topologies without any additional switching devices, no topological transitions within a switching cycle in steady state, transformer less, compact in size, soft switching and wider voltage gain with buck/boost operation and use of simple PI controller.

Chapter 6

Conclusions

Chapter 6

Conclusions

6.1 General Summary

The off-grid LED lighting applications are gaining importance these days. Three specific applications are identified under this, viz. SPV fed LED-SLS, SPV/battery fed high gain multiple load LED-LS, Battery fed automotive LED-LS. Different kinds of LED drivers are reported in the literature that are suitable for each of these applications. However, there exist some limitations in them, which demand for improvised LED drivers. Hence, three different LED drivers, suitable for these applications, are proposed in this thesis.

6.1.1 Summary of Important Findings

The following conclusions have been arrived from the thesis research work.

6.1.1.1 LED Driver-1 (CI-BB-BDC)

A novel soft switched CI-BDC has been proposed for single stage SPV fed BSS assisted LED-SLS which provides ZVS and operates in buck/boost modes in either direction of power flow

Table 6.1: Advantages of proposed configuration-1 (CI-BB-BDC) with existing converters

Compared with two-stage converters in the LED-SLS:	Compared with existing soft switched BDCs:
<ul style="list-style-type: none">• Reduced converter stages and hence reducing the component count• Buck/boost modes in either directions of power flow• Reduced device density because of high switching frequency• Soft switching across all devices including auxiliary circuit devices	<ul style="list-style-type: none">• Compact size due to the single magnetic core of CI• Reduced ripple current• High efficiency at all loads• Simple control

Table 6.2: Advantages of proposed configuration-2 (BBI-HBSRC-ML) with existing converters

Compared with existing multiple load LED drivers	
<ul style="list-style-type: none"> • Reduced device count • Compact in size • High gain for all LED loads • Reduced switching loss due to soft-switching across all devices 	<ul style="list-style-type: none"> • Improved efficiency • Simple control technique • Ability to drive multiple loads with equal or unequal voltages/wattages and independent voltage regulation & dimming control

(CI-BB-BDC). The BSS gets charged through proposed CI-BDC from the SPV source during daytime, while the same CI-BDC discharges the stored power in BSS to the LED load during nighttime. BDC operation in buck/boost mode has been simulated and tested for charging condition using programmable DC source as a SPV system. Also, BDC operation in buck mode has been simulated and tested for discharging mode with the LED lighting system. A prototype of 40 W LED driver has been built and tested experimentally. The simulation and experimental results were in good agreement with each other. In addition, LED dimming has been implemented using PWM technique and simulated and tested for 40% and 80% dimming conditions. The efficiency of proposed CI-BDC has been measured and compared with the conventional hard switched counterpart for various load conditions. Table 6.1 shows the advantages of proposed configuration compared with two-stage LED drivers and with similar soft switched BDCs. Thus, it is well suitable for SPV fed LED-SLS.

6.1.1.2 LED Driver-2 (BBI-HBSRC-ML)

A high gain buck-boost integrated symmetrical half-bridge non-isolated LC series resonant converter has been proposed for SPV/battery fed multiple load LED lighting applications (BBI-HBSRC-ML). The integrated buck-boost operation provides optimum utilization of input voltage and results in twice the gain of the conventional half-bridge converter. Frequency modulation has been used to regulate the output voltage against input voltage variations. The proposed converter configuration for single load and its extended version for two loads are realized and tested. Independent voltage regulation and dimming control were achieved for both loads. When compared with existing similar topologies, the proposed configuration provides various advantages listed in Table 6.2. Hence, the proposed non-isolated half-bridge high gain configuration is well suitable for SPV/battery fed multiple load LED lighting applications.

Table 6.3: Advantages of proposed configuration-3 (R-BBI-FBSRC) with existing converters

Compared with wide input LED drivers:	Compared with wide input soft-switched converters:
<ul style="list-style-type: none"> • Wider voltage gain • ZVS under wide input variations • Reduced switching losses • Easy implementation • High efficiency under wide input voltages and dimming levels 	<ul style="list-style-type: none"> • Buck/Boost operation • Transformer less • Wider gain • Less component count • Simple control

Table 6.4: Features of all the three LED drivers

Configuration\ Feature	LED Driver-1 (CI-BB-BDC)	LED Driver-2 (BBI-HBSRC-ML)	LED Driver-3 (R-BBI-FBSRC)
Source	SPV	SPV/Battery	Battery
Bidirectional Power Flow capability	Yes	No	No
Multiple load capability	No	Yes	No
Wide input voltage applications	No	No	Yes
Gain compared with their conventional ones	Normal	High	Very High and Wider
Modes of operation	Buck/Boost	Buck	Buck/Boost
Circuit component count per lamp	Medium	Medium	Less
Control	PWM	FMC	ADC (PWM)
Switching Frequency (kHz)	100	200	200
Rating of LED load	40 W, 26 V	Load1: 22.77 W, 22.5 V Load2: 43.41 W, 39.6 V	22.77 W, 22.5 V
Peak Efficiency (%)	92.45	93.23	94
Dimming Feature	Yes	Yes	Yes
Dimming Frequency (Hz)	250	200	200
Main Feature	buck/boost modes in either directions with soft switching	has high gain and can drive multiple loads with independent control and soft switching	wide gain, soft switching under wide input voltage
Application	SPV fed Battery assisted LED SLS	SPV/Battery fed Multiple LED load LS	Battery fed LED LS in automotive applications

6.1.1.3 LED Driver-3 (R-BBI-FBSRC)

A reconfigurable non-isolated BB integrated FB SRC resonant converter based LED driver (R-BBI-FBSRC) has been proposed for wide input automotive applications. BB converter operation has been integrated with FBSRC and hence can be reconfigured as BB-FBSRC, BB-

HBSRC and HBSRC achieving three different levels of voltage gains. APWM technique has been employed for voltage regulation. Based on the input voltage range, the converter transforms to one of the three configurations and the corresponding PI controller regulates the output voltage against variations in the input voltage. The proposed converter has been analyzed with respect to the design, conduction losses and voltage and current stress in the devices. The performance has been verified with both simulation and experimental results. It was observed that the proposed configuration smoothly transforms from one configuration to other and can provide voltage regulation with soft switching across the devices in the entire voltage range. The advantages of proposed configuration compared with existing wide input LED drivers and compared with similar wide input soft-switched converters is listed in Table 6.3. Therefore, proposed LED driver is well suitable for automotive LED lighting applications with wide input voltage variations.

6.1.1.4 Different Features of All the Proposed LED Drivers

The different features of the three proposed LED drivers are tabulated as shown in Table 6.4, where it can be observed that each configuration is versatile and suits for the three specific applications. LED driver in configuration-1 is a CI based BB-BDC that can provide soft switching with buck/boost modes in either directions, and best suitable as a single stage converter for SPV fed LED SLS. LED driver configuration-2 is BB-HBSRC that provides high gain and can drive multiple loads of different ratings with independent load control and dimming control. Thus, it is well suitable for SPV/Battery fed LED LS. LED driver in configuration-3 is a reconfigurable BB-FBSRC that provides wide gain and can drive the LED load with wide input voltage range without affecting soft switching. Thus, it is well suitable for Battery fed automotive LED LS. Thus, all the three configurations are improvised LED drivers compared with existing ones.

6.2 Suggestions for Future Research

As an extension to the current research work, there is scope for exploring further for a prospective researcher:

- Small signal analysis of all the proposed configurations can be carried out for all the works.
- MPPT techniques along with closed loop control can be implemented in the configura-

tions proposed in work-1 and work-2.

- Proposed configurations can be further analysed with the aim of further reduction of component count, etc.

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Appendix

Appendix A

Total Losses of the proposed CI-BDC and Hard-switched BDC

Table A.1: Total Losses of the proposed CI-BDC and Hard-switched BDC

Losses	Losses in Detail		Proposed Converter	Conventional converter
Switches, S_1 and S_2 losses (combined)	AC losses	Conduction	$P_{swAC_SS} = I_{sw_RMS_SS}^2 R_{DSon}$	$P_{swAC_HS} = I_{sw_RMS_HS}^2 R_{DSon}$
	DC losses	Conduction	$P_{swDC_SS} = I_{sw_Avg_SS}^2 R_{DSon}$	$P_{swDC_HS} = I_{sw_Avg_HS}^2 R_{DSon}$
	Switching losses		—	$P_{swSW_HS} = 2(V_{in} + V_o)I_{sw_Avg_HS}(t_{rise} + t_{fall})f_{sw}$
	Output Losses	Capacitance	$P_{swCa_SS} = C_{oss}(V_{in} + V_o)^2 f_{sw}$	$P_{swCa_HS} = C_{oss}(V_{in} + V_o)^2 f_{sw}$
	Reverse Losses	Recovery	—	$P_{swRR_HS} = Q_{rr}(V_{in} + V_o)f_{sw}/3$
Inductor losses	AC losses	Conduction in main inductor	$P_{L1AC_SS} = I_{L1_RMS_SS}^2 R_{L1}$	$P_{LAC_HS} = I_{L_RMS_HS}^2 R_L$
	DC losses	Conduction in main inductor	$P_{L1DC_SS} = I_{L1_Avg_SS}^2 R_{L1}$	$P_{LDC_HS} = I_{L_Avg_HS}^2 R_L$
	Conduction losses in auxiliary inductor		$P_{L2_SS} = I_{L2_RMS_SS}^2 R_{L2}$	—
Auxiliary Switch, S_{a1}/S_{a2} losses	Auxiliary Conduction losses	Switch	$P_{Sa_SS} = I_{Sa_RMS_SS}^2 R_{DSon}$	—
Auxiliary Diode, D_{a1}/D_{a2} losses	Auxiliary Conduction losses	Diode	$P_{Da_SS} = I_{Da_RMS_SS} V_{fD}$	—
The RMS value of waveforms like i_{Lr} and i_{L1} can be obtained as $I_{RMS_SS} = \sqrt{\frac{N_1}{D_1}}$ where $N_1 = (-3D^2t_f^2 + 2Dt_f(2t_f + 3) - 6)I_{pp1}^2 + (-6D^2t_f^2 + 4Dt_f(t_f + 3) - 2(2t_f + 3))I_{pp1}I_{pp2} + (-6D^2t_f^2 + 6Dt_f(t_f + 1) + (t_f^2 - 4t_f - 3))I_{pp2}^2$ and $D_1 = 12t_f^2$ In above equation, for finding $I_{sw_RMS_SS}$, $I_{pp1} = I_{Lr_pp1}$ & $I_{pp2} = I_{Lr_pp2}$				and for finding $I_{L1_RMS_SS}$, $I_{pp1} = I_{L1_pp1}$ & $I_{pp2} = I_{L1_pp2}$ $I_{sw_Avg_SS} = \left[\left(\frac{I_o}{1-D} \right) - \frac{I_{L2p}}{2} \left((1-D) + \frac{1}{t_f} \right) \right]$ $I_{L1_Avg_SS} = \left(\frac{I_o}{1-D} \right)$ $I_{L2_RMS_SS} = I_{L2p} \sqrt{\left(\frac{(1-D)}{3} + \frac{1}{3t_f} \right)}$ $I_{Sa_RMS_SS} = I_{Da_RMS_SS} = I_{L2_RMS_SS}$ $I_{sw_RMS_HS} = I_{L_RMS_HS} = I_{Lpp} \sqrt{\frac{1}{12}}$ $I_{sw_Avg_HS} = I_{L_Avg_HS} = \frac{I_o}{1-D}$

Appendix B

Conference Papers presented with resonant converter based LED drivers

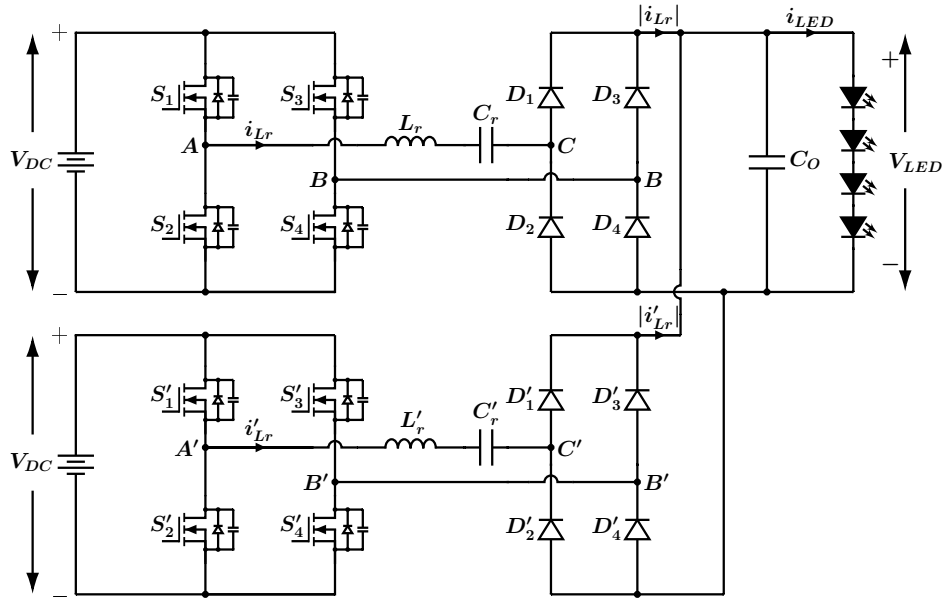


Figure B.1: Proposed reduced ripple resonant converter based LED driver [101]

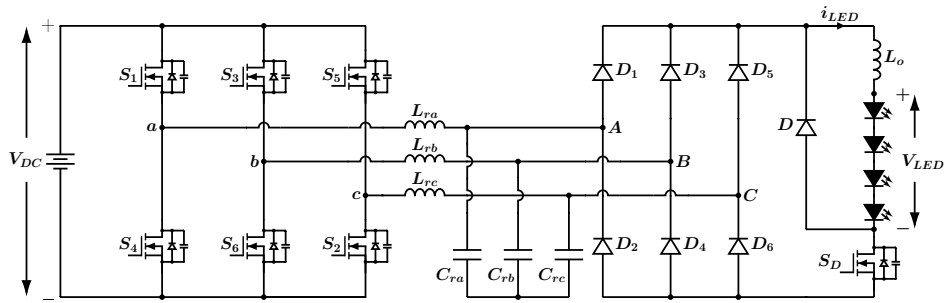


Figure B.2: Proposed reduced ripple resonant converter based LED driver [102]

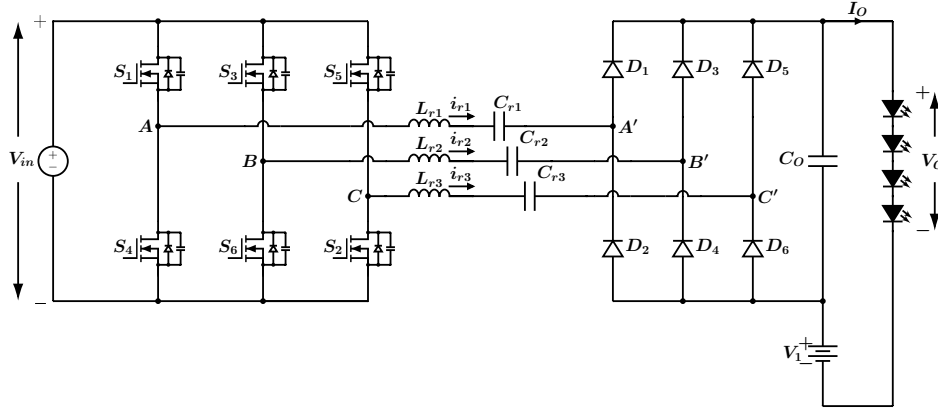


Figure B.3: Proposed reduced power three phase series resonant converter [103]

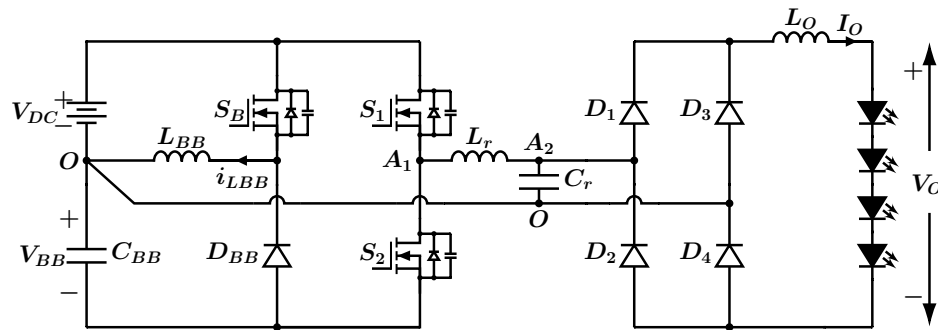


Figure B.4: Proposed buck-boost cascaded resonant converter based LED driver [59]

Publications

Refereed International Journal Publications:

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