Investigation on Fault-tolerant Multilevel Inverters for Open-End Winding Induction Motor Drives

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in
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by

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CERTIFICATE

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DECLARATION

This is to certify that the work presented in the thesis entitled **"Investigation on Fault-tolerant Multilevel Inverters for Open-End Winding Induction Motor Drives"** is a bonafide work done by me under the supervision of **Dr. P. Srinivasan**, Assistant Professor, Department of Electrical Engineering, National Institute of Technology Warangal, India and was not submitted elsewhere for the award of any degree.

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Narender Reddy Kedika

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ABSTRACT

Multilevel inverters (MLIs) have been an area of research over the past few decades and have received encouraging acceptance from industry as well. Multilevel concept has emerged as an alternative, economical and efficient solution for medium and high power applications. Multilevel voltage source inverters (VSI) exhibit many advantages compared to conventional two-level inverters. Some of the advantages are: 1) higher voltage can be generated using lower rating devices, 2) increase in the number of voltage levels produces better voltage waveforms, 3) improves harmonic performance with lower switching frequencies.

MLIs with a high number of levels in the output voltage are desired in drive applications, as the increase in the number of levels decreases harmonic distortions and avoids the need of filters. Employing MLIs in drive applications would add certain advantages such as: 1) lower dv/dt across the machine phase windings, 2) ripple free shaft torque, 3) elimination of filter requirements. Owing to these advantages, MLI fed drive systems are becoming exceedingly popular in industrial and electric vehicular applications.

Multilevel voltage generation using dual inverter configuration feeding an open-end winding induction motor (OEWIM) drive has received wide acceptance from industry. An OEWIM fed by two VSIs from both ends offer several advantages when compared to a standard wye or delta connected induction motor. Apart from dual inverter configuration with conventional two-level inverters, several topologies were proposed for OEWIM drive with increased number of levels in the output voltage. However, the increase in the levels in the output voltage is obtained at a cost of an increased number of components which makes the system bulky, less reliable and complex. The reliability of the system depends on the working of power switches and failure of any one switch may lead to a complete shutdown of the system. Therefore, MLIs with reduced components and tolerance for switch faults are preferred in drive applications.

Hence this thesis aims to investigate on the design of MLI topologies for induction motor with open-end windings. This thesis presents five MLI topologies with twenty four switches which is minimum number of switches for any nine level inverters present in literature. Three star-connected three-phase H-bridge voltage source inverters are employed to construct these topologies and are capable of producing a maximum voltage of twice the

DC supply voltage of the three-phase inverters. Hence for a given induction motor voltage, these topologies permits the use of lower voltage rating DC sources and therefore power semiconductors with lower voltage and higher switching frequency can be employed.

The proposed topologies are controlled with conventional sinusoidal pulse width modulation (SPWM) techniques. Level shifted carrier and multi reference SPWM techniques are employed to generate gate pulses for the proposed topologies. Reduced carrier PWM scheme with logical expressions are the simplest among the modified SPWM techniques. However, these logical expressions are not generalized and depends on number of levels and vary with topology. Another advantage of the proposed topologies is their reliability. The ability of an inverter to work under fault conditions plays a vital in ensuring the safety and uninterrupted operation of the overall system. There are several reasons for occurrence of fault in inverters, and every fault will end up with either open-circuit (OC) or short-circuit (SC) of a particular switch or associated unit/bridge. SC fault results in dangerously high current and cause a possible damage to the inverter. To avoid these faults, a fast acting over-current protection circuits are required to bypass the faulty phase-leg or inverter. On the other hand, OC faults are not severe and can be compensable.

Hence, this thesis presents operation of the proposed topologies during switch faults which do not require any additional hardware components but by altering the modulation strategy, which adding fault-tolerant capability to these topologies. Comparative analysis of the proposed topologies in terms of number of components employed and cost involved is done and presented. Since the number of components involved in designing this is lesser than their counterparts, the proposed topologies are proven to be cost effective.

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Abbreviation

APOD	Alternate Phase Opposite Disposition
ASDs	Adjustable Speed Drives
BEVs	Battery Electric Vehicles
CHB	Cascaded H-Bridge
CMV	Common Mode Voltage
DC	Direct Current
DSP	Digital Signal Processor
dSPACE	Digital Signal Processing and Control Engineering
EV	Electric Vehicle
FC	Flying Capacitor
FCB	Floating-Capacitor Bridge
FCLBT	Flying Capacitor Leg Based Topology
FFT	Fast Fourier Transform
FSW	Switching Frequency
FTS	Fault Tolerant Strategy
IGBT	Insulated Gate Bipolar Transistor
IGCT	Integrated Gate-Commutated Thyristor
IPD	In-Phase Disposition
MATLAB	MATrix LABoratory
MHBT	Modified H-Bridge Based Topology
MLBBT	Modified-Leg Bridge Based Topology
MLI	Multi-Level Inverter
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MSL	Modified Switching Logic
NPC	Neutral Point Clamped
OC	Open Circuit
OEWIM	Open End Winding Induction Motor
OPD	Opposite-Phase Disposition
PIV	Peak Inverse Voltage
PSPWM	Phase Shifted Pulse Width Modulation
PT	Proposed Topology

PV	Photo Voltaic
SC	Short Circuit
SCBT	Switched Capacitor Based Topology
SCR	Silicon Controlled Rectifier
SPWM	Sinusoidal Pulse Width Modulation
SVM	Space Vector Modulation
TBV	Total Blocking Voltage
THD	Total Harmonic Distortion
VSI	Voltage Source Inverter

List of symbols

f_c	Carrier Frequency
I_A, I_B, I_C	Phase Currents
L_m	Mutual inductance
L_r	Rotor inductance
L_s	Stator inductance
M_a	Modulation Index
R_r	Rotor resistance
R_s	Stator resistance
T_S	Switching Time
$V_{AA'}$, $V_{BB'}$, $V_{CC'}$	Phase Voltages
V_C	Capacitor Voltage
V_{DC} or V_{dc}	DC Link Voltage
V_M	Modulating Wave
V_{REF}	Reference Voltage

Chapter 1

Introduction

Chapter 1

Introduction

1.1 Research Background

For the last two decades, advances in science and technology have increased humanity's quality of life. Power electronics, which deals with the applications of solid-state power semiconductor devices for the energy-efficient conversion and control of electric power, is one of the main contributing technologies to this improvement. The energy efficiency and flexibility of various industrial processes, motor drives, and hundreds of different applications ranging from a few Watts to hundreds of megawatts have greatly benefited from the enabling technology of power electronics [1] – [3]. With the development of quick and powerful power devices and advances in control techniques, the energy efficiency and versatility of various industrial processes, motor drives, and hundreds of different applications ranging from a few Watts to hundreds of megawatts have greatly benefited from the enabling technology of power electronics.

The development of power electronics can be traced back to signal amplifier innovations that were then industrialized for high-power applications. The ability to regulate electrical motor drives and handle power flow is one of the most important benefits that power electronics has brought. Electric motor drive applications use more than 60% of global electrical energy, and the inverter power stage [4] is the most critical factor of this device. Figure 1.1 depicts the major components of an electric motor. It consists of a three-phase mains supply, a rectifier to transform the three-phase AC to DC, and an inverter to control the motor. Despite the fact that inverter-fed motor drives were first reported in the early 1930s, it was the development of Silicon Controlled Rectifiers (SCRs) in the 1950s that gave inverter-fed electric motor drives a major boost [5] – [7]. SCRs are being transitioned out in lieu of modern power devices such as Gate Turn-off Thyristors (GTOs), Metal Oxide Semiconductor Field Effect Transistors (MOSFETs), Insulated-Gate Bipolar transistors (IGBTs), and integrated gate commutated thyristors (IGCTs) in low and medium power applications due to advancements in material science technology. [8] - [10].

Power electronic converters can link systems with various electrical characteristics, such as choppers connecting two DC systems with different voltage levels, and inverters converting voltage (current) from DC to AC with variable amplitude and frequency. AC-AC converters,

on the other hand, change the amplitude and frequency of ac voltage (current). Because of improved system performance, reduced energy consumption, improved product quality, and good maintenance, power electronics applications in converters, especially dc/ac inverters, have expanded their range of use in industry.

Induction motors, on the other hand, are preferred over other motors for the majority of industrial uses, and they are known as the work horse of industry [11], [12]. The magnitude and frequency of the applied three-phase voltages [13] – [15] must be regulated by the induction motor drives. Induction motors can be used as the primary source of propulsion in electric vehicles in both existing and future projects. To meet the high power demands (>250 kW) of heavy duty trucks and many military combat vehicles with large electric drives, advanced power electronic inverters would be necessary [4], [16]. The production of electric drive trains for these large vehicles would result in increased fuel consumption, lower emissions, and most likely improved vehicle performance (acceleration and braking).

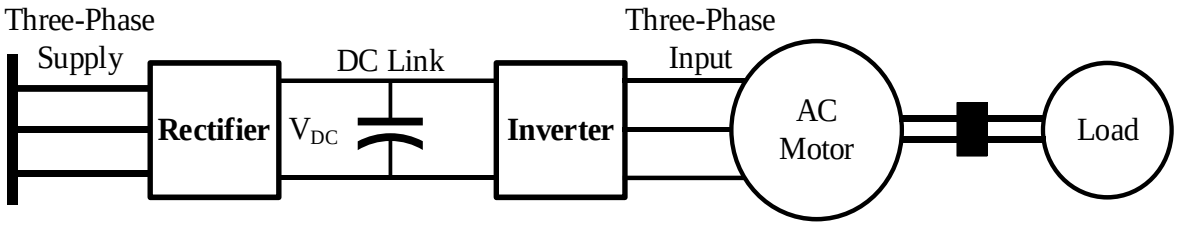


Figure 1. 1 Basic modules in an electric drive

Due to intrinsic limitations of semiconductor switching devices, simple two-level inverter fed induction motor drives were unable to fulfill the power demands as industrial drive applications for bulk power outputs increased [17]. Due to the limitations of semiconductor switches current carrying and voltage blocking capabilities, inverter fed drives would be restricted to low-power applications, necessitating the development of an alternative approach for high-power industrial applications.

High power demands can be fulfilled by opting to use a three-phase machine, but the machine's per-phase power is distributed over a larger number of semiconductor devices than a two-level inverter. Multilevel inverters (MLIs) achieve output voltage with more than two levels [18], [19], and they are known as such inverters. MLIs provide a higher-quality output voltage waveform, but they need a larger number of semiconductor devices to incorporate, necessitating a more complicated switching technique. However, in high-power and medium-voltage applications such as laminators, mills, conveyors, motors, fans, blowers, and compressors, MLIs systems have emerged as a viable solution. MLIs were first used in

locomotives and track-side static converters [20]. Power device converters for VAR compensation and reliability improvement [21], active filtering [22], high-voltage motor drive [23], high-voltage dc transmission [24], and, most recently, medium voltage induction motor variable speed drives [25] are some of the more recent implementations. Industrial medium-voltage motor drives [23], [26], utility interface for renewable energy systems [27], flexible AC transmission system (FACTS) [28], and traction drive systems [29] are among the various MLI applications.

MLIs were first used in 1975. The cascade MLI was proposed for the first time in 1975 [30]. To generate a staircase AC output voltage, separate DC-sourced full-bridge cells are connected in sequence. The three-level inverter [17] gave rise to the term "multilevel." The diode-clamped MLI, also known as the Neutral-Point Clamped (NPC) inverter, was proposed in 1981 [31]. Capacitor-clamped (or flying capacitor) MLIs [32] were proposed in 1992, and cascaded MLIs [33]–[34] were proposed in 1996. The cascade MLI was invented earlier, but it was not widely used until the mid-1990s. These three basic configurations of MLIs are considered as conventional topologies.

There are several different ways to implement a MLI. To construct multilevel waveforms, the easiest techniques involves linking traditional topologies in parallel or in series [18], [34]. The power rating of the converter will surpass the limit set by the individual switching devices since the voltage or current rating of the MLI becomes a multiple of the individual switches. The basic principle of a MLI is to perform power conversion by producing a staircase voltage waveform [35] – [38] using a sequence of power semiconductor switches with many lower voltage dc sources. Multiple dc voltage sources can be made from capacitors, batteries, and renewable energy sources. The power switches' commutation combines these different dc sources to produce a high voltage at the output; however, the rated voltage of the power semiconductor switches is solely determined by the rating of the dc voltage sources to which they are associated.

A MLI has several advantages over a conventional two-level inverter that uses high switching frequency pulse width modulation (PWM). The attractive features of a MLI can be briefly summarized as follows.

1. MLIs can not only produce very low-distortion output voltages, but they can also minimise dv/dt stresses, limiting electromagnetic compatibility (EMC) concerns.
2. Since MLIs deliver lower CM voltage, the stress on a motor's bearings when attached to a multilevel motor drive can be minimised.

3. MLIs can draw low-distortion input current.
4. MLIs may use both fundamental and high switching frequency PWM to run. Lower switching frequency normally translates to lower switching loss and higher performance.

MLIs have a few drawbacks. One drawback is the increased amount of power semiconductor switches involved. In a MLI, lower voltage rating switches can be used, but each switch needs its own gate drive circuit. This may increase the total expense and complexity of the system [39]. MLIs are desired in drive applications because they minimise overall harmonic distortions and alleviate the need for larger filters by increasing output voltage levels. In certain applications, the drive must run continuously to meet safety regulations. Aerospace, chemical industry, medical applications, power plants, automobile industry, railway locomotives, and military applications are only a few of the industries that need a high-reliability drive mechanism [40]. However, MLIs built for a higher number of voltage levels become complicated and cumbersome as a result of the increased part count, which has a significant effect on system reliability. As a result, the industry is cautious of such MLIs because reliability is still a major concern. As a result, MLIs must be designed for a larger number of voltage levels by using the least number of components [41], [42]. MLIs become less stable as the number of components grows, because a single switch failure will result in unbalanced voltage being supplied to the motor or even a complete system shutdown. A slight unbalance in the induction motor's voltage can result in significant unbalanced currents in the phase windings. Overheating, increased losses, shakes, acoustic disturbances, and a reduction in rotating torque are all detrimental consequences of unbalanced currents [43].

In MLIs, electrolyte capacitors and semiconductor switches are said to have the highest failure rates [44]. According to [45], variable speed drives would be to account for 63 percent of drive failures in the first year of use. Short-circuit, open-circuit, and gate-misfiring faults account for roughly 70% of all faults. Thermal tension, ageing, overloading, over voltage, and over current all cause power electronic switches to fail [46] - [48]. Electromagnetic spikes, electrostatic discharge, unanticipated operating conditions, or transient device or atmospheric conditions such as lightning [49] can all contribute to the failure. The switch's high instantaneous power dissipation boosts the semiconductor temperature, which is one of the most frequent causes of switch failure [50].

One of the most frequent defects in semiconductor switches is short-circuit (SC) faults, also known as transistor latch-ups. The switch remains closed and stays in the on state when a

SC fault happens, independent of the gate control voltage. As soon as the other switch on the leg is switched on, a very high current flows in the two switches of one phase leg and the dc source. These faults can cause severe damage to the load connected to the inverter. Open-circuit (OC) faults generally do not cause shutdown in the VSIs [51], however, they cause unbalance operation in the three-phase system and reduces the efficiency of the three-phase motor and causes failure to the motor drive and the mechanical load connected to it.

During the post-fault period, particularly when a switch fault has occurred, fault-tolerant operation is critical for inverter reliability. All system faults, including both OC and SC faults, should be accepted by a fault-tolerant MLI. Software-based fault-tolerant control strategies [52], [53], hardware-based redundant architecture principles, or a solution incorporating both software and hardware changes [54], [55] may both be used to achieve such fault-tolerant characteristics. Software-based fault-tolerant operation of MLIs is normally only suitable for those types of inverters with more redundant switching states that can be used during the post-fault stage to achieve satisfactory output voltages. For nearly all power converters, a hardware-based redundant architecture is a universal option. To provide backup solutions to any faulty switches or inverter legs, a basic fault-tolerant power converter may be built by simply adding one or more redundant inverter legs, or even parallel connecting one additional converter. However, industry adoption of redundant design methodologies is hindered by drastic cost increases, increased physical length, and increased hardware circuit complexity [56].

Aside from the cost and physical volume increases for fault-tolerant power converters, another issue is output performance loss during post-fault operation, such as output voltage and current deratings, harmonic distortions, and decreased reliability, among other things. The production efficiency of the MLIs should ideally be maintained at the same level as during normal service. However, owing to the lack of such switching states associated with the faulty switch and the switching/conduction of redundant devices/phase legs, achieving this goal in practice is exceedingly difficult. Almost all current fault-tolerant solutions [57] – [59], either need derated operation or have reduced converter performance or harmonic distortion during post-fault operations.

In drive applications, MLI configurations with a higher number of voltage levels are preferred since a higher number of levels reduces harmonic distortions and eliminates the need for costly and bulky filters. However, since the rise in levels comes at the expense of a larger range of parts, the industry is reluctant of such structures because they make the device bulkier, less stable, and complex. As a result, an increased number of levels in the inverter output voltage

must be achieved without an immense increase in the number of components, because system reliability is also important [60]. With fewer switching devices, the complexity of the power circuit can be minimised, and the control complexity can be reduced proportionally. The system's efficiency declines as the number of MLI components grows. Any single switch failure could cause the whole system to shut down. As a result, fault-tolerant reduced device count MLI topologies are becoming increasingly important in drive applications.

1.2 Inverter Topologies

1.2.1 Two Level inverters

A two-level inverter topology is seen in Figure 1.2. Every leg is made up of two switches that act together in a complementary manner. Each switch must be rated for the DC link voltage in this case. MOSFETs are used to implement the switches in low-voltage systems, while IGBTs are preferred in medium-voltage applications. SCRs are the perfect option for high-power applications. Since high frequency switching current cannot be extracted directly from the mains due to line inductance, a DC link capacitor is required. Each switch unit must be realised using two or three IGBTs or GCTs connected in series for high-power applications. The switching frequency is usually limited to 1 kHz for high power applications as well. For 2-level inverter operation, there are many modulation schemes. The three most popular PWM techniques are sinusoidal PWM, third harmonic injection PWM, and space vector PWM.

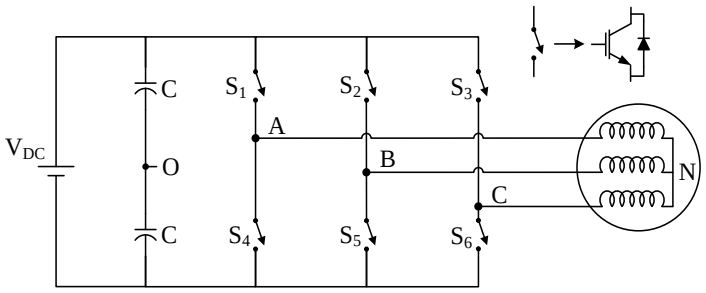


Figure 1. 2 Conventional three-phase two level inverter feeding an induction motor.

1.2.2 Multilevel inverter configurations

The output nodes of a MLI can be switched between different voltage or current levels. The performance THD decreases as the number of levels increases to infinity. Voltage-imbalance challenges, voltage clamping conditions, controller circuit configuration and packaging limitations, and, of course, capital and operating costs all restrict the amount of voltage levels that can be reached.

The dc link voltage V_{DC} is collected in a multilevel VSI from any equipment that can provide a reliable dc source. The inverter's energy tank is made up of series connected

capacitors, which provide several nodes to which a MLI can be connected. Initially, all voltage sources with the same magnitude would be considered to be series connected capacitors. $V_C = V_{DC}/(n-1)$, where n denotes the number of steps, is the voltage of each capacitor.

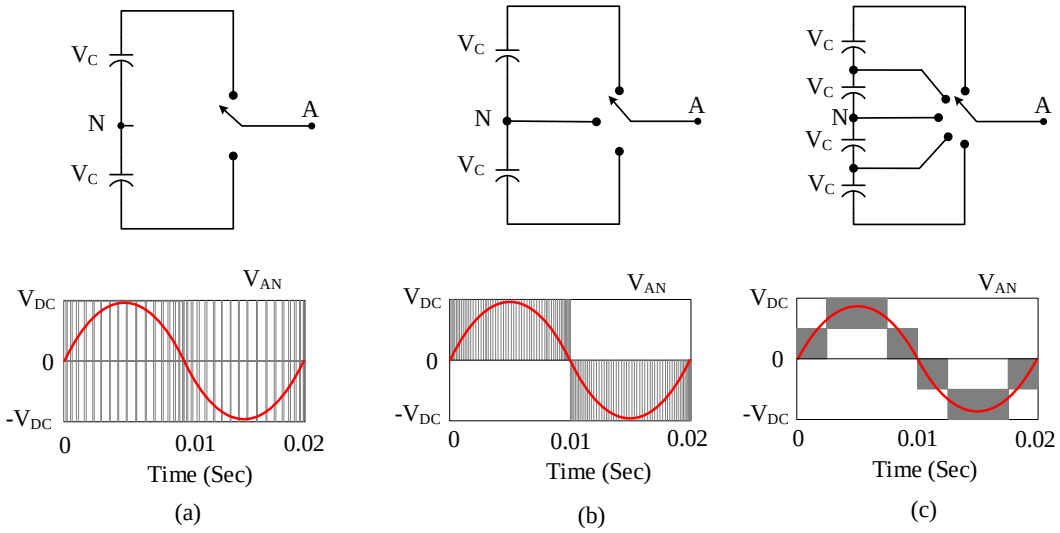


Figure 1. 3 One phase leg of an inverter with (a) two levels, (b) three levels, and (c) Five levels.

Figure 1.3 depicts a schematic diagram of one phase leg of an inverter with a range of degrees, with the operation of the power semiconductors depicted by an ideal switch with multiple locations. The output voltage of a two-level inverter has two values (levels) with respect to the neutral terminal (N), whereas the output voltage of a three-level inverter has three levels, and so on.

1.3 A Brief Review of Multilevel Inverters

1.3.1 Neutral Point Clamped Inverter

The dc link voltage is split into a number of equivalent voltage levels using series connected capacitors in this form of MLI topology. In 1981, Nabae, Takahashi, and Akagi proposed a neutral point clamped inverter that was basically a three-level diode-clamped inverter [17]. The voltage over the switching devices is limited by clamping diodes to safe blocking voltages. The neutral point (mid-point) is clamped to the output terminal by diodes, as seen in Figure 1.4(a), and the reverse voltages across the switches are clamped to $0.5V_{DC}$. The positive and negative nodes of the dc side circuit are connected by the association of the phase terminals A, B, and C with respect to switching states.

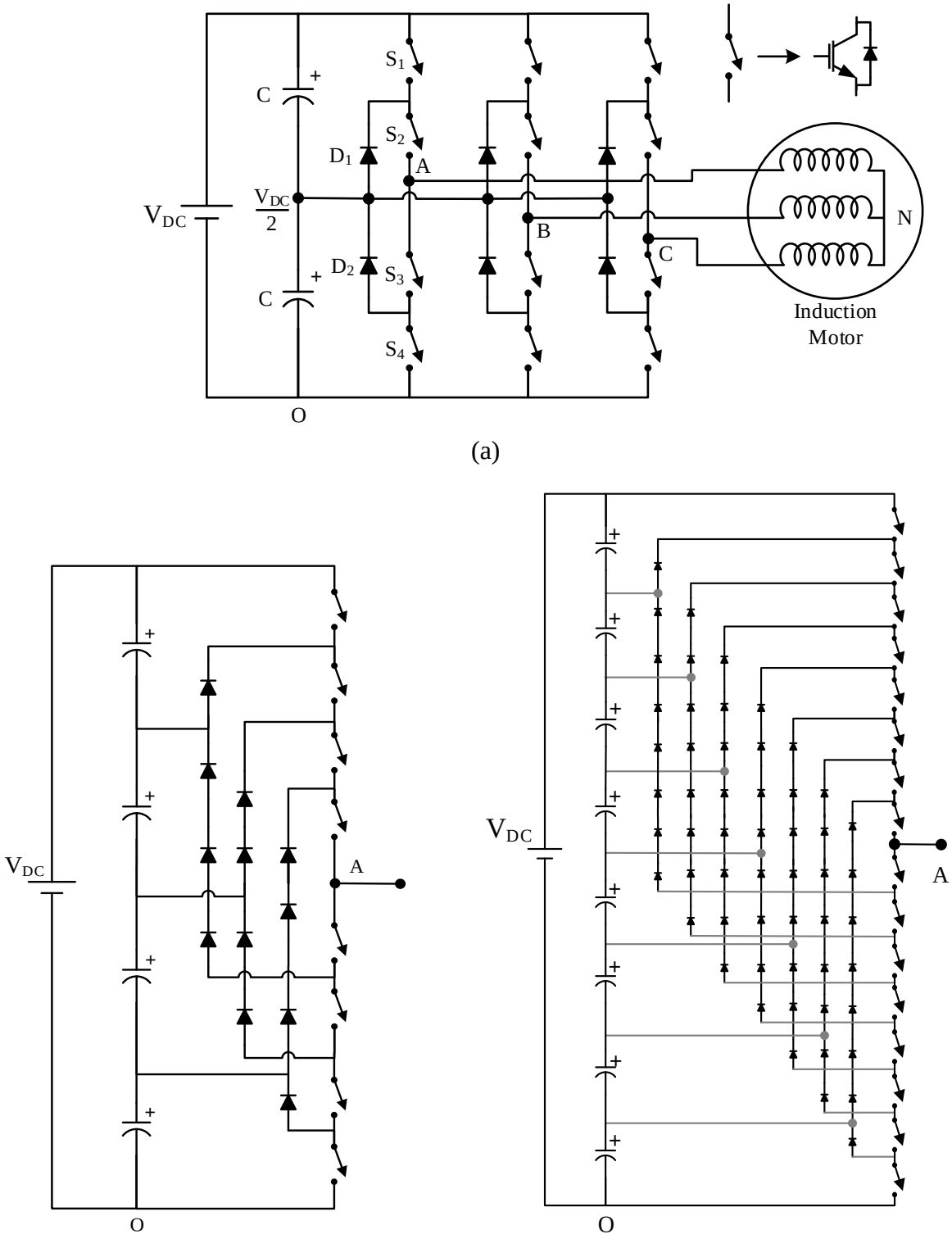


Figure 1. 4 NPC multilevel inverter scheme (a) three-level topology, (b) five-level topology, (c) nine-level topology.

In phase-A, we get $+V_{DC}$ at the output when the switches S_1 and S_2 are on (S_3 and S_4 are off), and zero voltage at the output when the switches S_3 and S_4 are on (S_1 and S_2 are off) with respect to terminal O. The output node A is clamped to the neutral point ($0.5V_{DC}$) when the

inner switches, S_2 or S_3, are switched on, depending on the direction of the load current. Thus this topology is generally known as neutral-point-clamped inverter (NPC). Because of the diodes D_1 and D_2, the voltage stress across all switching devices during off-states is only $0.5V_{DC}$ (the same as the voltage across the capacitors), indicating that the capacitor voltages are well controlled. As a result, with this three-level structure, the switch voltage stress is just half that of a two-level inverter with the same dc-link voltage. The clamping diodes must also have a voltage level of just $0.5V_{DC}$. This three-level inverter scheme has been promoted by a range of drive manufacturers and has proven to be the most successful MLI scheme.

The capacitor voltages will differ from their nominal value based on the current drawn from the capacitors by the load, which is a drawback of the NPC inverter. As a consequence, the load current has harmonic distortion, and the devices are now forced to block higher voltages than they should be. Neutral point voltage fluctuation applies to the shift of capacitor voltages, and it is a major concern for higher-level inverters unless sophisticated compensation schemes are used [61].

One phase-leg of a five- and nine-level NPC inverter is seen in Figure 1.4(b) and Figure 1.4(c). The large number of series connected clamping diodes with similar characteristics that block the higher voltage stress is a significant aspect of these circuits. While NPC inverters are popular for three-level applications, they are less appealing for applications with more levels. This is due to the clamping diodes' unnecessary conduction and reverse recovery losses, as well as the difficulties of regulating the capacitor voltages as the number of levels increases. The unequal distribution of losses in the outer and inner devices is another problem with the NPC inverter. This can be solved with complex modulation schemes [62].

1.3.2 Flying Capacitor Inverter Topology

In 1992, Meynard and Foch [32] proposed the capacitor clamped inverter, also known as the flying capacitor (FC) inverter. A three-level FC inverter's topology is presented in Figure 1.5(a). This inverter has a similar configuration to the NPC inverter, with the exception that instead of clamping diodes, capacitors are used. A series connection of capacitor clamped switching cells is used in the FC inverter. The voltage on the capacitor ladder varies from that on the next capacitor ladder in this topology, which has a ladder configuration of dc side capacitors. The voltage increment between two adjacent capacitor legs gives the size of the voltage steps in the output waveform [63] - [65]. FC inverters are easier to stretch to more degrees of multilevel operation than NPC inverters. The switches S_1 and S_4 must be operated in complementary order to prevent a short circuit of the capacitor around the source. Similarly

switches S_2 and S_3, which must be operated in complementary to prevent a capacitor short circuit. This form of precaution should be taken in all step legs.

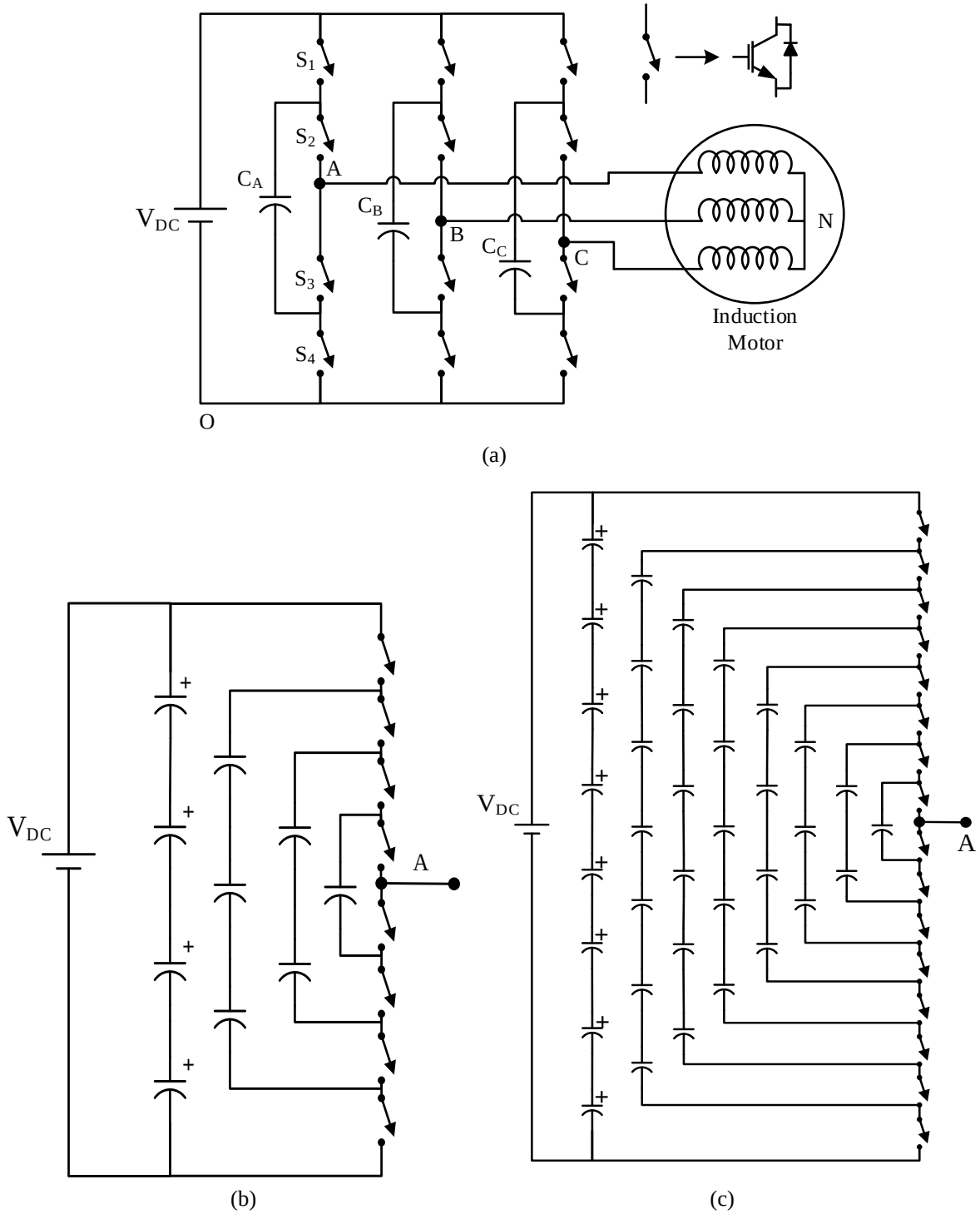


Figure 1.5 Flying-Capacitor inverter scheme (a) three-level topology, (b) five level topology, (c) nine-level topology

For the phase-A, when the switches S_1 and S_2 are on (S_3 and S_4 are off), a voltage of $+V_{DC}$ is obtained at the output and when S_3 and S_4 are on (S_1 and S_2 are off) we get zero voltage with respect to terminal O. Similarly when the switches S_1 and S_3 are on (S_2 and S_4 are off), pole

voltage of $0.5V_{DC}$ is obtained. The same voltage can be realized with switches S_2 and S_4 are on (S_1 and S_3 are off). As a result, there are two redundant switch combinations for the pole voltage level of $0.5V_{DC}$. As the number of levels increases, one of the main advantages of the FC topology is the huge number of switching state redundancies. The capacitor voltages can be controlled in each switching cycle using switching state multiplicities like this. Due to the phase-shifted carriers, the capacitor voltage can be retained to some degree by using phase-shifted carrier PWM. The pre-charging of capacitors is one of the big disadvantages of the FC topology. Another drawback is that to keep the capacitors well balanced, switching frequencies of the order of 1 kHz are needed, which is not feasible in very high-power applications due to high switching losses. Many studies are being conducted to address the drawbacks of FC inverters. One phase-leg of a five- and nine-level FCinverter is seen in Figure 1.5(b) and Figure 1.5(c).

1.3.3 Cascaded H-Bridge Inverter Topology

The cascaded H-Bridge inverter (CHB) or series H-bridge inverter first appeared in 1975, but it wasn't fully realised until 1997, when two physicists, Lai and Peng, patented it and introduced its multiple benefits [66]. The CHB inverter has been used in a number of applications since then. As seen in Figure 1.6(a) it uses a series connection of H-bridge cells. Each cascaded H-bridge cell is made up of a complete bridge inverter that is normally fed from an isolated source and generates $+V_{DC}$, 0, or $-V_{DC}$ at the output depending on the status of the switches.

When switches S_2 and S_3 are turned on in a full bridge for phase A, the output voltage (V_{AN}) is equal to $-V_{DC}$, and when switches S_1 and S_4 are switched on, the output voltage is equal to V_{DC}. The output voltage of the cell is zero volt when both S_1 and S_3 are turned on or both are turned off. It's worth noting that two switches in each leg of a cell, such as S_1 and S_2, form a complementary pair to prevent the cell's dc-link from being short-circuited. When the number of series linked H-bridge cells in a phase is ‘n’, the phase leg output will have (2n +1) switching levels. The average device switching frequency is much lower than the carrier frequency, and as the number of levels increases, individual devices are only expected to block lower voltages. Because of its modular, simple, and identical nature, the topology is suitable for high-power applications. Furthermore, without a lot of power-bus complexity, higher voltage levels can be extended.

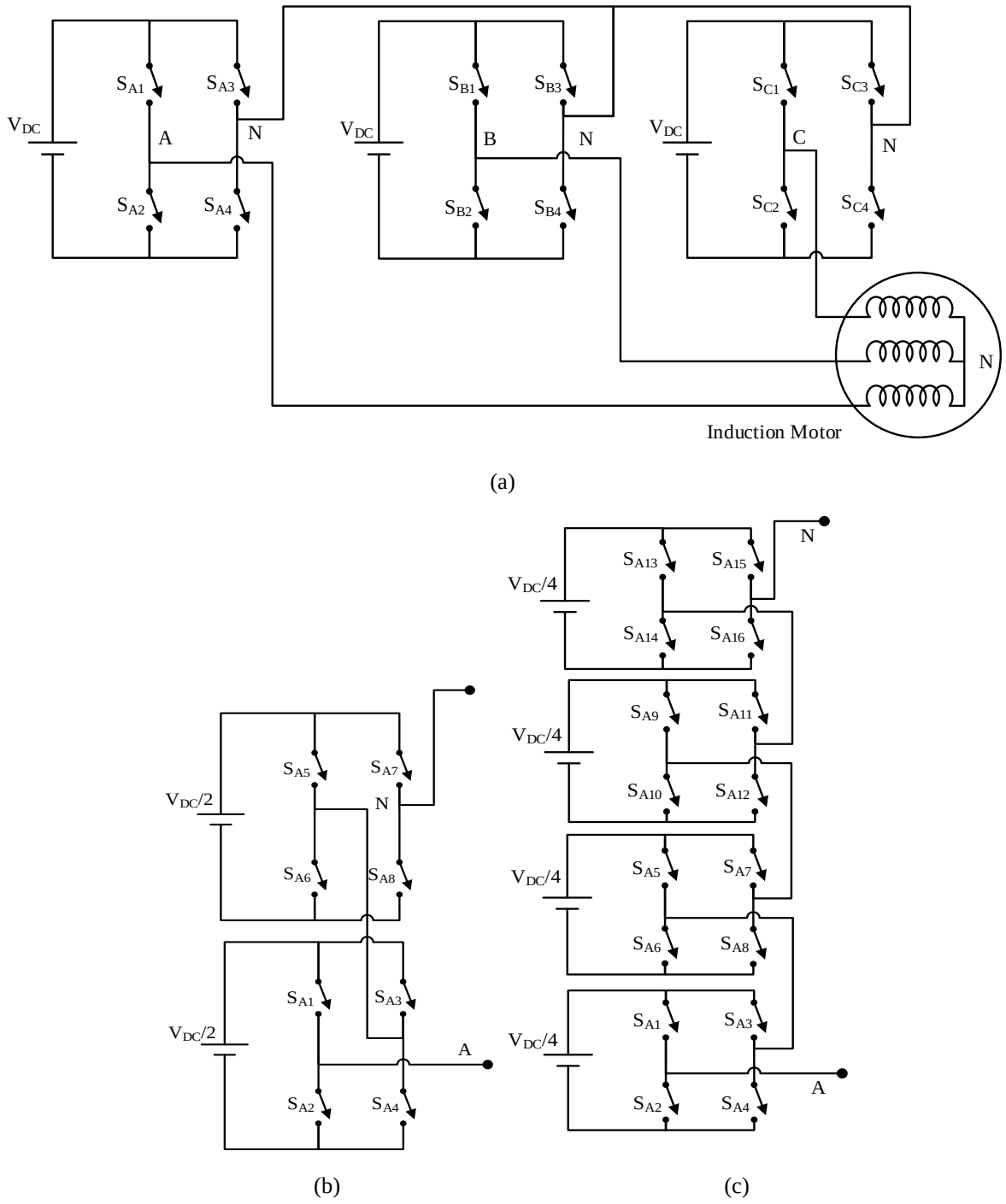


Figure 1. 6 Cascaded H-bridge inverter (a) three-level topology, (b) five-level topology, (c) nine-level topology.

Since each cell is fed from different voltage sources, this topology is free of voltage balancing problems, and the need of separated dc sources serves certain applications, such as grid convergence of green and dispersed energy like solar photovoltaics. The inverter's modular construction increases its reliability and fault tolerance capabilities. This topology is commonly used in high-power drives with ratings of up to 30MW [19], [29], [67]. The cascaded MLI topology, on the other hand, is not widely used in low-power applications due to the need for a

large number of isolated sources. Different voltages should be used instead of the same dc supply voltage for all H-bridge cells to get more voltage levels for the same number of H-bridge cells [68]. To limit switching losses, cells with higher dc-link voltages operate at a lower switching frequency than cells with lower dc-link voltages. However, the benefits of the modular system are compromised, and the voltage stress on the modules in various cells is unequal. The number of redundant states has also decreased significantly. As a result, asymmetric dc-link MLI schemes termed as asymmetrical CHB (ACHB) are not very popular. One phase-leg of a five- and nine-level CHB inverter is presented in Figure 1.6(b) and Figure 1.6(c).

1.3.4 Multilevel Inverter Configurations for Open-End Winding Motors

The idea of feeding the induction motor from both ends of the machine windings was suggested by H. Stemmler and P. Guggenbach [69]. This open end winding connection scheme can be conveniently achieved by merely opening the neutral connection of a conventional induction motor [70], [71]. The key benefit is that the inverters need lower dc-link voltages. Some benefits include the absence of clamping diodes and the absence of neutral point fluctuation in the push. To make a three-level inverter, use two simple two-level inverters feeding from both ends of the motor, as seen in Figure 1.7. Due to their redundancy and multilevel properties, dual inverter topologies are commonly used for motor drive applications [72], [73].

The persistence of interest in open-end multilevel drives is due to certain issues with single-sided multilevel drives. Capacitor voltage balancing in FC inverters and uneven voltage sharing among the power semiconductors in both FC and NPC inverters, for example, become very interesting issues as the amount of voltage levels increases [16]. The open end drive design can limit, and in some cases totally remove, these issues since the same amount of phase voltage levels can be accomplished with simplified inverter topologies.

The dual inverter arrangement has a number of advantages, including: 1. Equal power input from both ends of the winding, resulting in each VSI being measured at half the machine's power rating. 2. The phase current of each stator may be independently regulated. 3. Multiphase induction machines should be used if current reduction is required, so they can be extended to further stages. 4. Improved switching redundancy and a certain amount of fault tolerance 5. Diodes with clamping diodes are not permitted to be used (as related to NPC), 6. Less capacitors (as a result of FC), 7. Fewer DC sources (as related to CHB). The dual inverter fed open-end

winding induction motor (OEWIM) is commonly used in MLI drive applications because of these advantages.

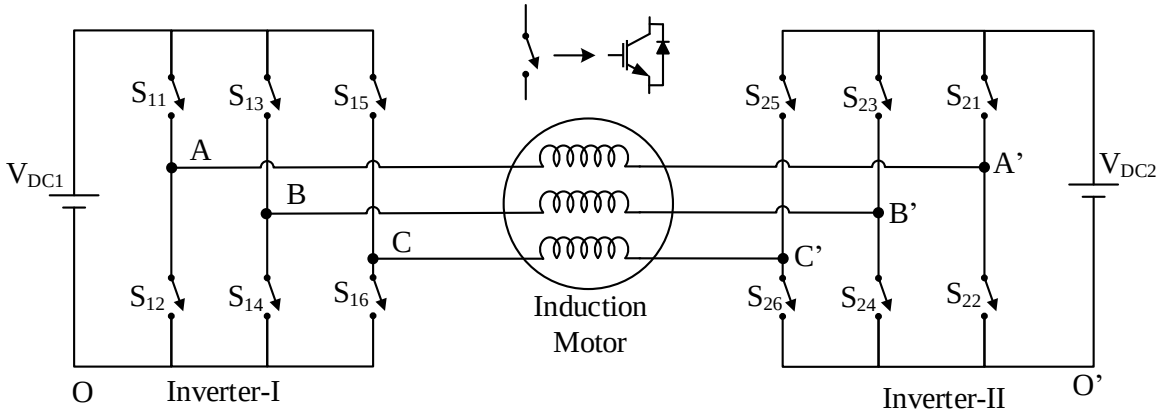


Figure 1. 7 Dual inverter topology for Induction motor with open-end windings.

Two types of connections exist in the dual inverter-fed open-end winding topology: one dc source that supplies both inverters with a path linking both inverters, and two inverters disconnected from each other with their own individual dc supply [72], [74], [75]. With just one dc source, the dual inverter-fed open-end winding configuration has a common dc-link between the two inverters. Since any voltage discrepancy between the terminals of a phase winding during zero voltage inverter states is clamped to zero volts, the zero sequence voltage has a low impedance direction, allowing zero sequence currents to flow through the motor windings and the dc link relation between the inverters. Each phase current contributes zero sequence current, which has an effect on the phase current waveform. To resolve these problems, several modulation methods have been suggested [76] - [79].

In a dual-inverter system, the dc-link voltage ratio for two inverters can be used to maximise the amount of voltage levels available. In [80] – [82], a drive with two two-level inverters and a dc-link voltage ratio of 2:1 is investigated. The first step is to look at two different space vector PWM methods. Decoupled control of the inverters is used in both techniques. According to the chosen dc-link voltages, the first one, equal-duty-PWM, is based on sharing the overall phase voltage sinusoidal relation between two inverters in the same 2:1 ratio. The switching frequencies in both inverters are the same. The second technique switches the two inverters at switching frequencies equal to their dc-link voltage relative to the total dc-link voltage. Overall energy losses are seen to be minimised in this manner. Interestingly, the second approach also does well in terms of phase voltage harmonics. In [80], an extension of this work is presented with an emphasis on hardware improvements. Three passive rectifiers

are used to create dc voltage sources, which are driven by a centre tapped transformer with a secondary winding ratio of 1:2:1. The dc-link source for one inverter is nested in this manner, since it is made from the rectifier output supplied from the middle secondary winding. The second inverter is driven by the double dc-link voltage, which is calculated as the difference between the rectifier outputs' maximum and lowest potentials. While the number of components is raised, their ratings are smaller and the total cost is lower as compared to the conventional realisation. Unfortunately, the nested rectifier method lacks separation between two dc-link sources, which is always necessary to eliminate the zero-sequence current circulation path. However, the use of an asymmetric DC link voltage ratio for a dual inverter configuration has the disadvantage of triggering DC link voltage deviation. Unless regulated, the lower DC connection voltage can charge to a higher voltage than desired. One simple solution is to avoid the charging switching sequences to balance the lower DC link voltage [80], [83], [84].

As compared to a single four-level inverter supply, an important benefit of open-end configuration is that the same multilevel output is obtained by using simpler and thus more robust inverters, resulting in improved drive efficiency. In addition, if a fault condition occurs, the faulted inverter may be short-circuited, allowing the drive to run at half of its maximum power. Another significant benefit of open-end winding three-phase drives is the lower average manufacturing cost, which is achieved by eliminating the need for extra diodes and capacitors in MLIs, as well as the option to use off-the-shelf three-phase two-level inverter modules[85].

For a multilevel OEWIM drive fed from two two-level inverters supplied from two isolated dc sources, certain control techniques have been suggested to achieve two objectives such as minimization of commutation frequency per inverter leg and reduction of common mode voltage by selecting suitable space vectors [86], [87].A similar dual-inverter configuration is presented in [88]-[92], where only one two-level inverter termed as primary inverter has an active dc source, while the second two-level inverter, termed as secondary inverter is used as an active filter. The overall drive complexity is reduced and also demonstrated better harmonic performance compared to the three- and four-level single-sided supplies. The total dc-link voltage, on the other hand, is limited to the voltage of the active dc source, negating one of the open-end winding configuration's intended benefits. The overall dc-link voltage is supposed to be equal to the total of the dc-link voltages of two inverters, with the maximum phase voltage amplitude being one half of that magnitude. If the overall dc-link voltage is determined as the sum of two dc-link voltage values, [91] proved that normal drive operation is only possible up to 60% of the overall dc-link voltage. To put it another way, in

order to use this topology, the primary inverter (which has an active dc source) must be designed for the maximum voltage rating, while in a configuration with two dc sources, the total voltage stress is shared by both inverters. This is not a concern since the inverter with an active dc source only performs low frequency switching, while the filtering inverter runs with a dc-link voltage that is many times lower. The total dc-link voltage boosting is illustrated in the topology suggested by [89], which is dependent on the primary inverter phase angle change. This topology allows for the use of high-voltage drives because the semiconductor blocking parameters are compatible with existing technology: the primary inverter with an active dc source can be implemented with IGCTs or thyristors, while the filtering Inverter can be implemented with traditional IGBTs or power MOSFETs.

Another degree of independence to think of when designing an OEWIM drive is the amount of voltage levels each inverter provides. An inverter is constructed as a cascade of two two-level inverters in [93], resulting in a three-level counterpart. One two-level inverter is mounted on the other side of the OEWIM. Due to the unequal dc-link voltages, six-level modulation of 91 space vectors is used, with a 4:1 dc-link voltage ratio. A supply for three-phase OEWIM drive is provided by four two-level inverters in [94]. A five-level drive is developed by providing each inverter with the same dc voltage and cascading two inverters on each end of the motor windings. This drive has 25 percent more switching components and one voltage level less than that in [93]. This topology, on the other hand, necessitates a lower power rating of the semiconductors, lowering their cost. Despite the fact that multilevel operation is accomplished, no clamping diodes or external active switches are required for NPC inverters, nor is capacitor voltage balancing required for FC inverters. As compared to CHB topologies, it is shown that the topology needs fewer dc voltage sources with the same number of voltage levels. In [95], the same topology is extended to cascaded inverters, but with unequal dc-link voltages. The hardware approach proposed in [96] for dc-link voltage elimination using non-isolated dc-link voltages is also used in [94]. As a result, the number of dc voltage sources is limited once again. Similar findings for two three-level inverter drives are published in [97]. The inverters are built as a cascade of two two-level inverters with two bulk capacitors to provide equivalent voltage splitting between the two inverters, both driven by a single dc voltage source. Both sides' upper and lower inverters are attached to the same dc-link rails. As a consequence, the common mode voltage is no longer present. Further simplification is also shown, both in the drive topology and in the semiconductor gating circuits. The capacitor voltage balancing is a disadvantage that must be considered during the formulation of the

modulation algorithm, so it is given special consideration. In [98], where 18-step space vector PWM is investigated, the cascade connection of converters is used once more. Three two-level converters are used, two of which are connected in a cascade to provide three voltage levels for one pair of stator windings, while the other side is driven by a two-level inverter. Three unequal dc-link voltages are used to generate eighteen large space vectors, resulting in a finer step voltage than a twelve-sided polygon [95].

In [99], [100], MLI topologies were presented with improvement for CMV removal and dc-link capacitor voltage balance performed at the cost of a decrease in the number of voltage levels, as discussed in [101], [102]. Two five-level inverters were used in the three-phase open-end motor, which were linked in a cascade by two-level and three-level inverters. Following the concept of the switching pattern that eliminates CMV, the total number of switches is decreased by removing two two-level inverters from the circuit and replacing them with only two dc voltage sources. In [100], the same principles are used. There are thirteen voltage ranges present in this study since four two-level and two three-level inverters are used. Since the common mode voltage removal algorithm and dc connection capacitor voltage balancing were implemented as secondary goals for the modulation strategy, the number of voltage levels was reduced to seven, as anticipated. Also if an analogous topology with a smaller number of dc voltage sources is used, both targets are still achievable as presented.

There have been reports of even more complicated MLIs for OEWIM drives [103]-[105]. By cascading flying capacitor and floating capacitor H-bridge systems, [105] achieves a seventeen-level three-phase drive. Two three-level NPC inverters and six H-bridge structures are used in [103], [104]. Cascading two sets of asymmetric three stage inverters with isolated H-bridges on both sides of an open-end winding three-phase machine allows for a large number of voltage levels. The waveform generated by the proposed modulation is a 24-step staircase waveform. Unfortunately, only experiments with exceptionally low voltages are recorded in [103] – [105], where average dc-link voltages are many times smaller than real voltage ratings of individual semiconductors. This raises the question of whether this level of drive complexity is suitable and efficient for high-power applications, which are sensitive to isolation issues.

Di Wu Xiaojie Wu *et al.*, suggested a dual inverter configuration with three-level NPC structures for generating five-level voltages from a single source. To ensure the elimination of zero sequence currents, a better regulation is suggested and implemented for this topology [106]. K. Sivakumar et al., proposed a five-level inverter topology for OEWIM drive. A two-level inverter in series with a capacitor-fed H-bridge cell feeds one end of the OEWIM, while

a conventional two-level inverter feeds the other end [107]. The voltage space-vector positions generated by the combined inverter device are exactly the same as those produced by a traditional five-level inverter. Under all operating conditions, including over modulation area, switching state redundancies are used to balance the H-bridge capacitor voltages. In the event that a switch in the capacitor-fed H-bridge cell fails, the proposed inverter topology can be used as a three-level inverter for maximum modulation range. The most of the switching components employed for this topology are of lesser voltage rating but the number of components involved are high.

V. F. Pires et al., proposed a fault tolerant five-level inverter based on three phase H-bridge inverters for an OEWIM drive [108]. Three star-connected three-phase H-bridge inverters are employed to build this topology and is capable of producing a maximum voltage of twice the DC supply voltage of the three-phase inverters. Hence for a given induction motor voltage, this topology permits the use of lower voltage rating DC sources and therefore power semiconductors with lower voltage and higher switching frequency can be employed. Fault-tolerant operation under an open-switch fault without adding any extra components and without changing the modulation strategy is also proposed, adding fault-tolerant capability to the topology.

P.P.Rajeevan *et al.,* suggested a seven-level inverter structure based on two traditional two-level inverters and six capacitor-fed H-bridge cells [109]. Just two independent dc-voltage sources with a voltage rating of V_{DC} /2 are required for this topology, where V_{DC} is the voltage magnitude required by the standard NPC seven-level topology. By using switching state redundancies, this topology is capable of retaining the H-bridge capacitor voltages at the appropriate level of V_{DC}/6 under all operating conditions, covering the entire linear modulation and over modulation regions. This inverter will run in three-level mode in the event of any switch breakdown in H-bridges, which improves the drive system's reliability. Switching loss is reduced since the two level inverters, which run at a higher voltage level of V_{DC}/2, switch less than the H-bridges, which operate at a lower voltage level of V_{DC}/6. The same topology can be used to generate nine levels of voltage by changing the voltage across the H-Bridges cell in a 1:2 ratio [110].

Using two three-level inverters with two separated DC connections in a 3:1 ratio, Abhijit Kshirsagar *et al.,* suggested a nine-level inverter topology involving only eight switches per phase [111]. Two three-level flying-capacitor inverters are attached to the two ends of an OEWIMD in this nine-level inverter topology. This topology necessitates proper switching

state selection in order to keep the floating capacitors balanced independent of switching frequency, modulation index, or load current, while also minimising dead-time transients. With an additional switched capacitor circuit [112], the same topology can be generalised to produce 17 level output voltage.

For inverter switch faults, a dual inverter system provides fault tolerance. Switch faults in either of the inverters cannot totally shut down the operation of the drive because half of the power is supplied from either end. In a dual inverter configuration, whenever an OC fault occurs in the inverter switch, namely upper switch in inverter-1, all upper switches in such an inverter are opened, and all bottom switches are switched on continuously. The phase windings will be able to form a star configuration, and the healthy inverter will supply power from the other end. The drive production will be split in half, but the process will continue until the faulty switches are removed or fixed. This function applies to all of the topologies mentioned previously in this section. A few OEWIM drives inverter topologies were even suggested to supply the motor rated power even in the case of a switch fault.

A dual three-level inverter has been proposed by A Karthik *et al.,* for open-end winding motor drive applications achieving higher fault tolerance [113]. This topology is fully modular and can be built entirely out of half-bridge blocks. This topology has been shown to be capable of surviving the primary collapse of either of its systems or flying capacitors without losing control or common-mode elimination. This topology's post-failure operation necessitates the use of additional hardware components.

M. G. Majumder *et al.,* proposed a fault-tolerant 5-Level inverter scheme for OEWIMD applications that uses a single DC-link [114]. A main inverter (a 2-Level inverter cascaded with a capacitor fed H-bridge inverter) feeds one end of the motor, while a secondary inverter (capacitor fed 2-Level inverter) feeds the other. In the H-bridge and secondary 2-Level inverter, the DC-link voltage to nominal capacitor voltage ratio is held at 4:2:1. Space Vector redundancy is used to balance the capacitors. This topology allows for the operation of a 5-Level inverter with fewer components while also having fault tolerance against failure of the power switches in the H-bridges and the secondary 2-Level inverter. Any failure in the primary inverter switches would cause the system to shut down completely.

1.4 Modulation Techniques

For MLIs, abundant modulation techniques and control models such as sinusoidal pulse width modulation (SPWM), selective harmonic elimination (SHE-PWM), space vector modulation (SVM), and others have been developed. SPWM (sinusoidal pulse width

modulation) is used in this thesis. In 1964, the sine-triangle PWM scheme was introduced, in which the gate signals were obtained by comparing a sinusoidal voltage with a triangular voltage. When compared to existing schemes, this PWM scheme was readily accepted by the industry due to its superior harmonic performance and ease of control [115].

With this invention, the analysis of PWM schemes for inverter-fed drive applications began, and many PWM techniques such as harmonic elimination schemes, common mode injection schemes, and discontinuous PWM followed. Given the variety of topologies available for MLIs, the PWM scheme chosen should also take into account the kind of topology used for multilevel voltage generation. Selective harmonic elimination schemes and phase disposed carrier PWM schemes, for example, are well suited for cascade H-bridge inverters, while a phase-shifted carrier-based PWM scheme is better suited for natural capacitor balance in flying capacitor inverters. The general motivation for designing new modulation techniques can be summarised as reaching sinusoidal voltages through stator phases (eliminating low order harmonics and lowering unit losses), lowering converter losses caused by high frequency switching, and increasing dc-link voltage utilisation.A brief review of the various PWM techniques used for MLIs are presented in this section.

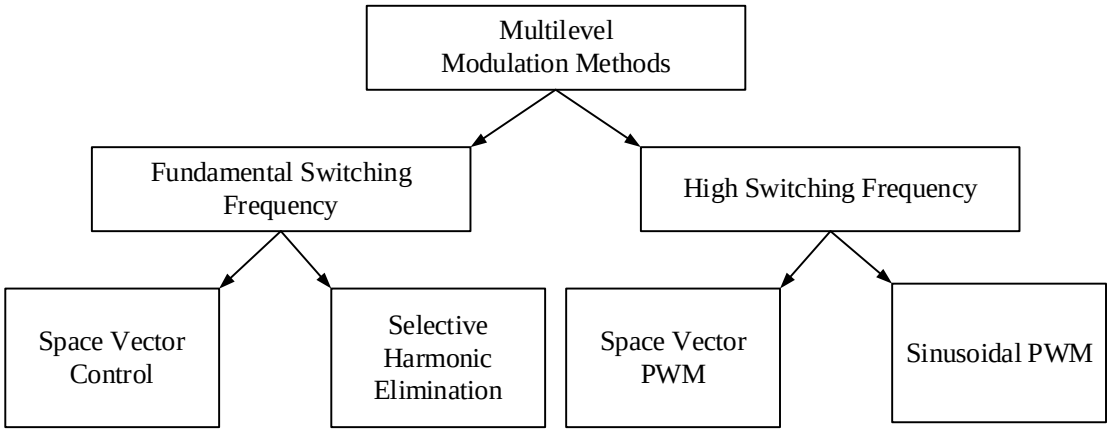


Figure 1. 8 Classification of modulation methods

The modulation methods are split into two groups based on the switching frequency of MLIs, as seen in Figure 1.8 [116], [117]. Space vector modulation (SVM) and selective harmonic elimination (SHE) are the two most common switching modulation methods [118], [119]. Space vector pulse width modulation (SVPWM) and sinusoidal pulse width modulation (SPWM) are two high switching frequency modulation approaches [24], [62].

1.4.1 Space vector modulation

Space vector modulation (SVM) is one of the most commonly used real-time modulation techniques for digital control of voltage source inverters [115]. Switching states reflect the working status of the switches in a two-level inverter. In a two-level inverter, each pole voltage with respect to O will take on one of two values: $-V_{DC}/2$ or $+V_{DC}/2$, as seen in Figure 1.9**.** The switching states of the inverter V1 (+--), V2 (++-), V3 (-+-), V4 (-++), V5 (--+), V6 (+-+), V7 (---), V8 (+++) are the eight probable variations of switching states in the two-level inverter. The symbols '+' and '-' respectively indicate that the top switch and the bottom switch in a given phase leg are turned on.

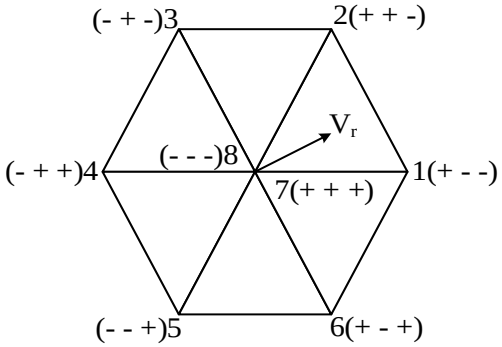


Figure 1. 9 Voltage space vector diagram.

Space vector (V_r) is the resultant of all the three phase voltage phasors given as [118], [119]

$$V_r = V_{AO} + V_{BO}e^{j120^0} + V_{CO}e^{j240^0} \tag{1.1}$$

The two dimensional representation of such space vector is represented as

$$V_r = V_\alpha + jV_\beta \tag{1.2}$$

The relation between V_α, V_β and instantaneous phase voltages given as (1.3) and inverse transformation represented in (1.4).

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_{AO} \\ V_{BO} \\ V_{CO} \end{bmatrix} \tag{1.3}$$

$$\begin{bmatrix} V_{AO} \\ V_{BO} \\ V_{CO} \end{bmatrix} = \begin{bmatrix} \frac{2}{3} & 0 \\ -\frac{1}{3} & \frac{1}{\sqrt{3}} \\ -\frac{1}{3} & -\frac{1}{\sqrt{3}} \end{bmatrix} \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} \tag{1.4}$$

For voltage vectors V_7 and V_8, all three poles of the inverter are connected to the same node. As a result, the load is essentially shorted, and no power is transferred between the dc-link and the load. As a consequence, V_7 and V_8 are referred to as zero voltage vectors. Power is transferred between the DC-link and the load in the remaining six vectors. These voltage vectors (V_1, V_2, V_3, V_4, V_5, and V_6) are therefore referred to as active voltage vectors.

1.4.2 Carrier based Sinusoidal Pulse Width Modulation technique

The Sinusoidal Pulse Width Modulation (SPWM) technique is a commonly used method for producing multilevel output voltage in industry [120], [121]. For the carrier based SPWM technique, more than one carrier is expected due to the presence of leg voltages with more than two voltage levels. They can be structured in a variety of ways, giving the multilevel topology a new dimension of flexibility. To produce pulses to the semiconductor switches, the sinusoidal reference signal is compared to the triangular carrier signal in this SPWM. Figure 1.10 depicts four distinct carrier modulation methods for producing a five-level output voltage.

Among the conventional schemes, SPWM is very popular due to its easiness in implementation and is further classified into level shifted carrier pulse width modulation (LSCPWM) and phase shifted pulse-width modulation (PSPWM). The LSCPWM in two-level inverters has been extended to MLIs with the carriers properly arranged leading to schemes such as

1. In-phase disposition (IPD),
2. Opposite-phase disposition (OPD) and
3. Alternate-phase disposition (APD).

In LSC-PWM, the carriers are in phase alignment, but with different dc-offsets as presented in Figure 1.10. The number of triangular carriers required in LSC-PWM is equal to (n-1), where n is the number of voltage levels. The carriers are arranged in contiguous bands, and a sinusoidal reference voltage is compared with these carriers to obtain the PWM.

In APD, 180^0 phase-shifted carriers are used in adjacent bands whereas in OPD, the carriers above the zero reference point are in-phase, but are 180^0 phase-shifted to those below the zero reference as presented in Figure 1.10(b) and Figure 1.10(c) . It has been proven that the level-shifted PWM gives the best harmonic performance as the zero periods are placed better off in a carrier cycle [122] – [124]. Hence LSPWM-IPD scheme is employed for generation of switching pulses for the proposed topologies. However, since all switches do not operate at the same average switching frequency in a fundamental cycle, and the number of switchings is therefore dependent on the modulation index, this advantage comes at the cost of

uneven loss distribution among the switches. The carrier frequency of each group can be varied depending on the time duration that the reference waveform remains in the group in order to balance the number of switching activities equally on all switches [62].However, the carrier frequencies then depend on the modulation index, M_a and the implementation is complex.

The fundamental output voltage component can be controlled using a modulation index, M_a as defined in equation 1.5.

$$M_a=V_m/V_c \qquad (1.5)$$

Where, V_m is the amplitude of the modulating wave and V_c is the amplitude of carrier waves.

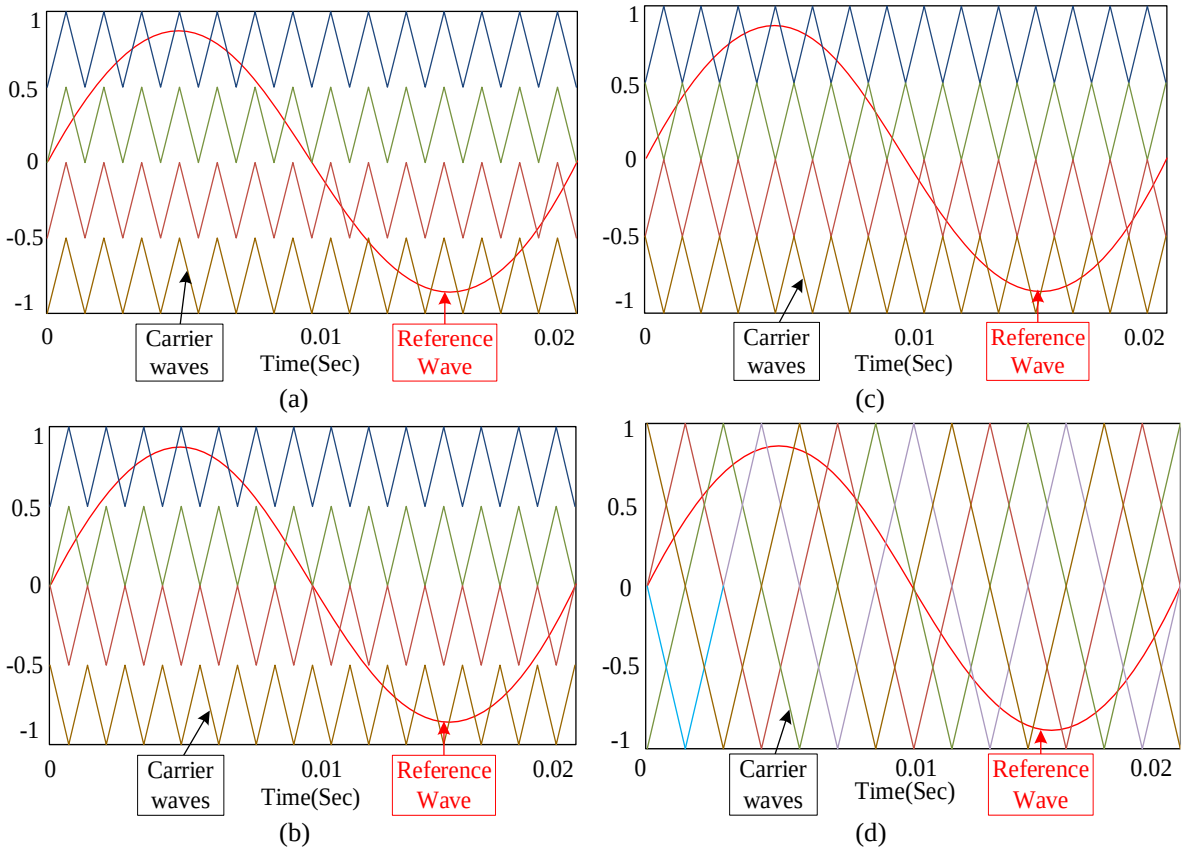


Figure 1.10 Sinusoidal pulse width modulation schemes (a) In-phase disposition, (b) opposite-phase disposition, (c) alternate-phase disposition, (d) phase shifted modulation

In phase shifted carrier scheme, all carriers have equal amplitudes, but they are phase-shifted by an angle of $2\pi = (n-1)$ between adjacent carriers where `n' is the number of levels in a MLI. The carrier based phase shifted PWM scheme for a five-level inverter is illustrated in Figure 1.9(d). To get output voltage with maximum amplitude, either two 180^0 phase shifted reference voltages with a single carrier or one reference voltage with two 180^0 phase shifted carriers are to be used. The latter approach is preferred as it is easier to generate triangular signals than sinusoids.

As cascaded MLI schemes are used, such carrier phase shifts help to eliminate further carrier sideband harmonics in a natural way [122]. The dominant sideband harmonics are now centred around (n-1)*f_c, where f_c is the carrier frequency and n is the MLI's number of levels. However, it should be noted that system switching frequency has increased. Since the vectors switched are not necessarily the closest vectors to the reference voltage, the harmonic output is identical to the APD scheme but inferior to the IPD and OPD carrier schemes for the same number of unit switchings [125].In a fundamental cycle, all of the power devices have the same switching frequency and conduction time, which is a significant benefit in this system. As a result, the losses are spread evenly among the power units. In flying capacitor inverters, this function of an equal conduction time for all components in a fundamental cycle is useful for balancing capacitor voltages.

Higher frequency switching and space vector algorithms can provide significantly improved performance. In comparison to two-level three-phase drives, which have only eight space vectors, MLIs have a significantly larger number of voltage vectors. For example, a three-level NPC inverter has $3^3 = 27$ vectors (including redundant ones), while a four-level NPC inverter has $4^3 = 64$; as the number of levels increases, the number of voltage vectors increases as well. However, due to the numerical burden, space vector algorithms are difficult to implement. Sector determinate algorithms are the most computationally difficult components of space vector PWM algorithms.Sector determination and trigonometric equations, as well as contact with memory where look-up tables are processed, are the most computationally challenging aspects of space vector PWM algorithms.

1.5 Motivation

From the extensive literature survey, it is noticed that the MLIs have been an area of research over the past few decades and have received encouraging acceptance from industry as well. Hence the multilevel concept emerges as an alternative, economical and efficient solution for medium and high power applications. Multilevel voltage source inverters (VSI) exhibit many advantages compared to conventional two-level inverters. Some of the advantages are: 1) higher voltage can be generated using lower rating devices, 2) increase in the number of voltage levels produces better voltage waveforms, 3) improves harmonic performance with lower switching frequencies.

MLIs with a high number of levels in the output voltage are desired in drive applications, as the increase in the number of levels decreases harmonic distortions and avoids the need of

filters. Employing MLIs in drive applications would add certain advantages such as: 1) lower dv/dt across the machine phase windings, 2) ripple free shaft torque, 3) elimination of filter requirements. Owing to these advantages, MLI fed drive systems are becoming exceedingly popular in industrial and electric vehicular applications.

Multilevel voltage generation using dual inverter configuration feeding an open-end winding induction motor (OEWIM) drive has received wide acceptance from industry.An OEWIM fed by two VSIs from both ends offer several advantages when compared to a standard wye or delta connected induction motor. Apart from dual inverter configuration with conventional two-level inverters, several topologies were proposed for OEWIM drive with increased number of levels in the output voltage. However, the increase in the levels in the output voltage is obtained at a cost of an increased number of components which makes the system bulky, less reliable and complex. The reliability of the system depends on the working of power switches and failure of any one switch may lead to a complete shutdown of the system. Therefore, MLIs with reduced components and tolerance for switch faults are preferred in drive applications.

Hence this thesis works out on designing of MLI topologies with reduced number of components with simple construction and exhibit tolerance for faults in the semiconductor switching devices. Conventional sinusoidal pulse width modulation techniques are employed for switch gate-pulse generation, which lowers the control complexity. The proposed topologies can deliver peak output voltage of twice the source voltage magnitude in nine-levels across each phase winding of the OEWIM drive. The proposed topologies will continue to operate even under switch fault condition with post processing of switching pulses and does not require any additional hardware.

1.6 Thesis Objectives

The focus of this thesis work is to propose MLI topologies with reduced power and control complexity for OEWIM drives. The objectives are as provided below:

1. Designing of MLI topologies with reduced component-count for OEWIM drives. The decrease in the number of components in designing the MLI topology will reduce the power circuit complexity.
2. To increase the peak output voltage delivered to the phase windings of the OEWIM drive employing lower rating voltage sources.

3. Employment of basic modulation techniques such as sinusoidal pulse width modulation (SPWM) techniques with level shifted carrier and phase shifted modulation techniques for control of the MLI topologies to deliver balanced three-phase voltage during normal and post-fault operation. The usage of conventional SPWM techniques with optimization in modulating and carrier waves will reduce the computational burden on the digital platforms such as digital signal processors and dSPACE.
4. Continuity in operation of the MLI topologies even during the inverter switch faults. Proposing modified switching logics for operation of the MLIs with available healthy switches in the inverter to deliver balanced three-phase output voltage across the phase winding of OEWIM drives.

1.7 Organisation of the Thesis

The organization of thesis work on the proposed fault tolerant MLI topologies for open end winding induction motor drive are divided into overall six chapters and each chapter's brief outlook is presented below:

Chapter 1 describes the complete view of topic which includes background of MLIs, conventional topologies, literature survey on existing MLI topologies for OEWIM drives, their fault tolerance properties, merits and demerits. The motivation of research work on fault tolerant MLIs for OEWIM drives and thesis objectives are presented.

Chapter 2 presents the Modified H-Bridge based topology (MHBT) for OEWIM drive with fault-tolerance. The control technique for operation of the proposed MHBT during normal operating conditions is presented. A fault tolerant strategy is proposed for the operation of the inverter topology during open-circuit and short-circuit faults in various switches is presented. The performance of the proposed MHBT is verified by performing simulation and experimentation. A comparative analysis in terms of cost and component count of proposed topology with conventional topologies and existing MLI topologies for OEWIM drive are presented.

Chapter 3 presents modified leg H-bridges based topology (MLBBT) to produce nine-level voltage across the phase windings of an OEWIM. The proposed MLBBT is designed to deliver balanced three phase output voltage across the phase windings of the OEWIM under normal operation and even during inverter switch fault conditions. Conventional sinusoidal pulse width modulation (SPWM) techniques such as level shifted carrier in-phase disposition

and phase shifted PWM techniques are employed to generate switch gate-pulses. Performance of the proposed topology is validated by MATLAB simulations and results are presented.

Chapter 4 presents two MLI topologies designed to feed OEWIM drives. First topology is flying capacitor leg based topology (FCLBT) and the second is a switched capacitor based topology (SCBT). FCLBT is designed with three inverters in which each inverter consists of one three-level flying-capacitor inverter leg and single phase H-bridge connected across a dc source. Similarly, SCBT is designed with three three-phase H- bridge inverters and three switched-capacitors. The operation of these proposed topologies during normal operation is presented and conventional SPWM techniques are employed for switch gate-pulse generation. A modified switching logic is presented for operation of these topologies during inverter switch faults. The simulation and experimental results validate the proposed topologies. Comparative analysis of these topologies in terms of blocking voltage of components used in conventional topologies and various MLI topologies feeding OEWIM drives are presented.

Chapter 5 introduces a floating-capacitor bridge based topology (FCBBT) for OEWIM drives. The FCBBT comprises of three three-phase two-level voltage source inverters fed from isolated dc sources and a floating-capacitor bridge. Switch gate pulses are produced using level shifted carrier SPWM techniques. For operation of the proposed topology during inverter switch faults, a modified switching logic is presented. Comparative analysis of the proposed topology for component count and control complexity of various MLI topologies feeding OEWIM drives are presented. The proposed FCBBT is validated by experimental results.

At the end, **Chapter 6** concludes the overall key achievements accomplished in this thesis along with the future scope of work.

Chapter 2

Modified H-bridge Inverter based Fault-Tolerant Multilevel Topology for Open-End Winding Induction Motor Drive

Chapter 2

Modified H-bridge Inverter based Fault-Tolerant Multilevel Topology for Open-End Winding Induction Motor Drive

2.1 Introduction

The voltage generated by a greater number of steps with nearness to a sinusoidal wave is the better quality waveform. Increasing the number of levels in the output improves harmonic profile of the voltage, but requires the complex power and control system involving a greater number of power semiconductor switches with gate-drive circuit. Conventional multilevel inverters (MLIs) namely neutral point clamped (NPC), flying-capacitor (FC) and cascaded H-bridge (CHB) topologies has received acceptance from the industry and are being used extensively for various applications. The drawback of these topologies is that the number of circuit's components intensely increase even with small increase in number of voltage levels. For example, for a three-phase N-level inverter, the number of clamping diodes required by the NPC topology are $3(N-1)(N-2)$, the number of flying-capacitors required by the FC topology are $1.5(N-1)(N-2)$ and the isolated sources required by the CHB topology are $1.5(N-1)$. Hence with increase in number of voltage levels, the circuit complexity of these topologies becomes very high. The cost of the inverter will not be economical with such bulky power circuit and the reliability will become the major concern.

In this chapter, an approach is taken to overcome the disadvantages of conventional topologies without increasing the number of power switches. The suggested solution employs least number of switches as like the other nine-level inverters feeding open-end winding induction motor (OEWIM) drive. The proposed MLI topology is designed with a modification in a conventional three-phase H-bridge by a bidirectional switch. Three of such modified H-bridges each fed from an isolated dc source are employed for the proposed topology (PT). Every first leg of the three-phase H-bridge and the mid-point of DC link capacitors are bridged with a bidirectional switch realized with anti-series connection of two IGBTs with common-emitter configuration. The balanced switching of the inverters will ensure balanced voltage across the DC link capacitors. Modulation strategies such as sinusoidal pulse width modulation (SPWM) technique can be applied directly for the PT. The modulation techniques such as level-shifted-

carriers SPWM and multi-reference SPWM with carriers in-phase disposition (IPD) are adopted. This topology ensures Fault tolerance operation of the drive under fault conditions such as a switch open-circuit (OC) or short-circuit (SC) condition with the same modulation techniques employed for normal operation.

2.2 Analysis of the proposed topology

A MLI topology is proposed for OEWIM drive that can produce a maximum output voltage of twice the input voltage (V_{dc}). The PT is designed with modified H-bridges and hence is termed as modified H-bridge based topology (MHBT). The MHBT is designed based three modified-three-phase two-level voltage source inverters (VSIs) each with an isolated DC source connected in a star configuration as depicted in Figure 2.1. The switches S_{a1} through S_{a8} represent inverter-a. Similarly, the switches S_{b1} through S_{b8} and S_{c1} through S_{c8} represent inverter-b and inverter-c respectively. Out of three output terminals of each three phase inverters, the midpoint of first legs (between S_{a1} & S_{a4}), (between S_{b1} & S_{b4}) and (between S_{c1} & S_{c4}) is connected to the midpoint between the capacitors of the corresponding inverters using a bi-directional switch, this leg is termed as modified leg of the inverter. The bi-directional switch is realized with two switches (here IGBTs) connected in anti-series. From Figure 2.1, S_{a7} & S_{a8} denote the anti-series switches connected in inverter-a. Similarly, S_{b7} & S_{b8} and S_{c7} & S_{c8} represent the anti-series switches for inverter-b and inverter-c respectively. Though, two switches S_{x7} and S_{x8} are used in all three inverters, from now on they will be treated as a bidirectional switch S_{x7} (where x ϵ a, b, c) since they are operated by the same switching signal with common-emitter configuration.

The output terminals of the modified legs of all the inverters are shorted which will create a neutral point by forming a star configuration of the three inverters. The other two output terminals of each VSI are connected to two different windings of the stator of the OEWIM drive. Comparing the MHBT with dual inverter, an extra VSI along with a DC source is required additionally but provides increased maximum output voltage, i.e., $2V_{dc}$ whereas $1.33V_{dc}$ in case of dual inverter. This result in increased output power or for the same power rating, the voltage ratings of the DC sources used can be reduced which would lower the blocking voltages of the switches. This gives more scope for using lower power rating high frequency switching semiconductor switches such as MOSFETs, which is an added advantage. Another advantage with the MHBT is the possibility of direct application of conventional PWM schemes such as level shifted PWM, multi carrier PWM schemes, even for fault tolerance operating conditions.

The topology connection considering only phase-A of the OEWIM drive is shown in Figure 2.2.

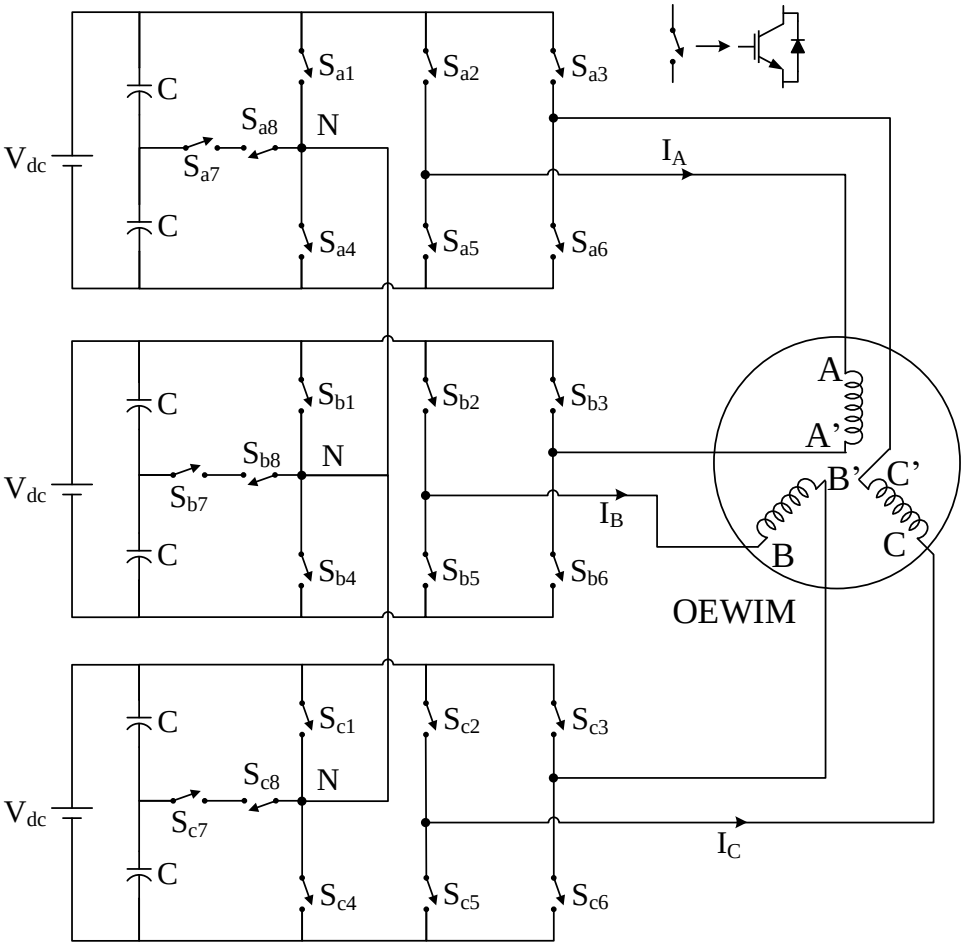


Figure 2. 1 Proposed Modified H-bridge based topology (MHBT).

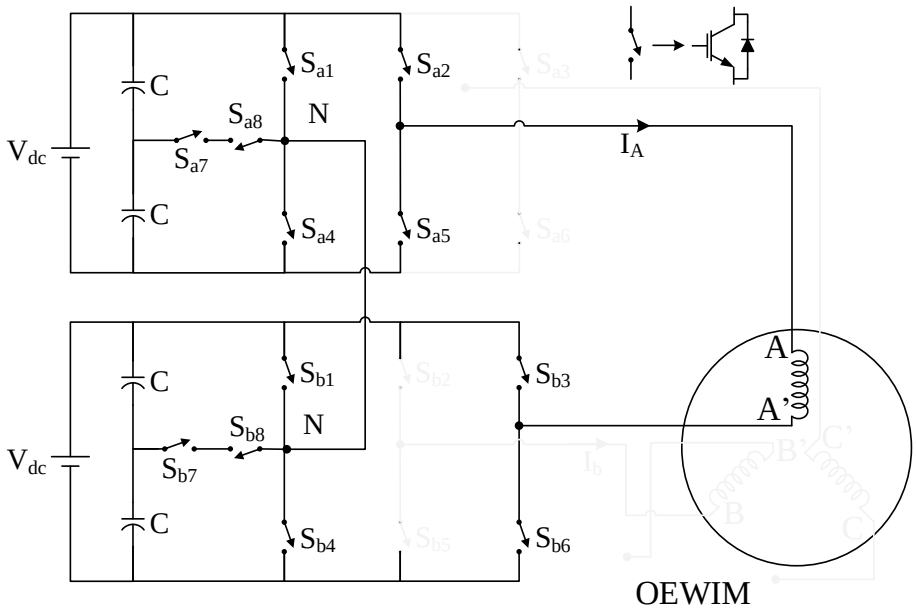


Figure 2.2 Inverter connection for phase-A winding of OEWIM

Table 2. 1 Voltage of phase-A winding ($V_{AA'}$) according to switching states

$V_{AA'}$	Inverter-a					Inverter-b				
	S_{a1}	S_{a2}	S_{a4}	S_{a5}	S_{a7}	S_{b1}	S_{b3}	S_{b4}	S_{b6}	S_{b7}
$2V_{dc}$	0	1	1	0	0	1	0	0	1	0
$1.5V_{dc}$	0	1	1	0	0	0	0	0	1	1
	0	1	0	0	1	1	0	0	1	0
V_{dc}	0	1	1	0	0	1	1	0	0	0
	0	1	1	0	0	0	0	1	1	0
	1	1	0	0	0	1	0	0	1	0
	0	0	1	1	0	1	0	0	1	0
$0.5V_{dc}$	0	1	0	0	1	1	1	0	0	0
	0	1	0	0	1	0	0	1	1	0
	1	1	0	0	0	0	0	0	1	1
	0	0	1	1	0	0	0	0	1	1
0	1	1	0	0	0	0	0	1	1	0
	0	0	0	0	0	0	0	0	0	0
	1	1	0	0	0	1	1	0	0	0
	0	0	1	1	0	1	1	0	0	0
	0	0	1	1	0	0	0	1	1	0
$-0.5V_{dc}$	0	0	0	1	1	1	1	0	0	0
	0	0	0	1	1	0	0	1	1	0
	1	1	0	0	0	0	1	0	0	1
	0	0	1	1	0	0	1	0	0	1
$-V_{dc}$	1	0	0	1	0	1	1	0	0	0
	1	0	0	1	0	0	0	1	1	0
	1	1	0	0	0	0	1	1	0	0
	0	0	1	1	0	0	1	1	0	0
$-1.5V_{dc}$	1	0	0	1	0	0	1	0	0	1
	0	0	0	1	1	0	1	1	0	0
$-2V_{dc}$	1	0	0	1	0	0	1	1	0	0

Note: V_{DC} is the DC-link voltage required by a conventional three-phase inverter, whereas V_{dc} mentioned in the proposed circuit configuration is half the DC-link voltage i.e., $V_{dc}=V_{DC}/2$.

From the analysis of Figure 2.2, the different output voltage levels that can be obtained across the terminals of the motor phase-A winding for various combinations of switching states are presented in Table 2.1. The combination of second leg of inverter-a and third leg of inverter-b along with modified legs of both the inverters are presented since these legs affect the voltage that is applied across the motor phase-A winding. From Table 2.1 and Figure 2.2, it can be observed that the maximum voltage across the terminals of phase-Aobtained is twice the supply voltage V_{dc} resulted by connecting the two DC sources in series.

The output voltages across the terminals are dependent on the states of the power switches. Consider the switches are ideal, their conduction and blocking states are represented by binary variables as 1 and 0 respectively.

i.e., if S_{xy}= 1 then S_{xz}= 0, -switch S_{xy} is ON and switch S_{xz} is OFF

ifS_{xz}= 1 then S_{xy}= 0, -switch S_{xz} is ON and switch S_{xy} is OFF.

Where x ϵ a, b, c & y ϵ 2, 3 & z ϵ 5, 6.

Likewise for switches 1, 4 & 7 of all the inverters, the switching condition would be

if $S_{x1} = 1$, then $S_{x4}=S_{x7} = 0$, -switch S_{x1} is ON, S_{x4} and S_{x7} are OFF,

if $S_{x4} = 1$, then $S_{x1}=S_{x7} = 0$, -switch S_{x4} is ON, S_{x1} and S_{x7} are OFF,

if $S_{x7} = 1$, then $S_{x1} = S_{x4} = 0$, -switch S_{x7} is ON, S_{x1} and S_{x4} are OFF,

and $S_{x7}=\hat{S}_{x1}+\hat{S}_{x4}$.

With this representation, output voltages undergoing various voltage levels can be written in accordance with,

$$V_{AA'} = (1/2)V_{dc}* (V_{AN}- V_{NA'}); \quad (2.1)$$

where, $V_{AN}=[\hat{S}_1 (S_2 \hat{S}_4 \hat{S}_5 S_7 + 2 S_2 S_4 \hat{S}_5 \hat{S}_7) +(S_4 - 1)*(\hat{S}_1 \hat{S}_2 S_5 S_7 + 2 S_1 \hat{S}_2 S_5 \hat{S}_7)]_a$ and

$$V_{NA'} = [\hat{S}1(S_3 \hat{S}_4 \hat{S}_6 S_7 + 2 S_3 S_4 \hat{S}_6 \hat{S}_7) +(S_4 - 1)*(\hat{S}_1 \hat{S}_2 S_6 S_7 + 2 S_1 \hat{S}_3 S_6 \hat{S}_7)]_b$$

Similarly, $V_{BB'} = (1/2)V_{dc}* (V_{BN}- V_{NB'});$ (2.2)

$$V_{CC'} = (1/2)V_{dc}* (V_{CN}- V_{NC'}); \quad (2.3)$$

Here, $\hat{S}_x$- represents complementary of switch S_x switching signal.

2.3 Modulation Strategies

The proposed MHBT can be controlled by conventional SPWM techniques, which are usually used for controlling multilevel topologies. Therefore, SPWM techniques such as level shifted carriers (In-Phase Disposition) and Multi-Reference level shifted carrier SPWM techniques are employed for the PT.

2.3.1 Level-Shifted-Carrier SPWM

Level Shifted Carrier In-Phase Disposition (LSC-IPD) SPWM scheme is used to generate switching pulses for the proposed MLI. This switching scheme's operating principle applied to inverter-a of the PT is illustrated in Figure 2.3.For the other two inverters *b* and *c,* the sinusoidal reference and carrier waves are phase shifted by 120^o and 240^o respectively. This operation scheme is identical to conventional SPWM schemes used for multilevel topologies. A sinusoidal reference will be compared with four level shifted carriers. The carriers V_{cr1} and V_{cr2} are level shifted above zero and carriers V_{cr3} and V_{cr4} are level shifted below zero as shown in the Figure 2.3(a). The switching pulses are generated by comparison and with the logic circuits. The switches S_{x2}-S_{x3} and switches S_{x5}-S_{x6} are switched simultaneously. The switching

pulses for switches S_{x2}-S_{x3} and switches S_{x5}-S_{x6} are complementary and will be active high (switch on) for half cycle and active low (switch off) for another half cycle of sinusoidal reference. These switches (legs) are directly connected to phase windings of stator of OEWIM.

The switches connected in neutral leg are driven with pulses generated by comparing sinusoidal reference with level shifted carriers. Comparison of reference wave with carriers V_{cr2} and V_{cr4} will generate pulses for switch S_{x1} and comparison of reference wave with carriers V_{cr1} and V_{cr3} will generate pulses for switch S_{x4}. The complementary pulses of switches S_{x1} and S_{x4} are given to bidirectional switch S_{x7}. With this configuration of modified three-phase H-bridge, each inverter generates voltages in five levels between each phase leg and neutral leg. The connections of the stator windings in this PT are transposed such that nine voltages levels are obtained across each phase winding given by equations (2.1) – (2.3)

2.3.2 Multi-Reference SPWM

Level Shifted Multi-Reference In-Phase Disposition (LSMR-IPD) SPWM scheme is applied for the PT. Figure 2.3(b) shows the modulation scheme adopted for inverter-a of the PT. Like in LSC-IPD technique mentioned in the above section, the switching of devices S_{x2}-S_{x3} and S_{x5}-S_{x6} are simultaneously done and switching pulses will be complementary and will be active high for half cycle and active low for another half cycle of the sinusoidal reference V_{ref1}. These switches (legs) are directly connected to phase windings of stator of OEWIM. In this scheme, two sinusoidal reference waves (V_{ref1} and V_{ref2}) and three level shifted Carrier waves (V_{cr1}, V_{cr2} and V_{cr3}) are employed. Carriers V_{cr1} is level shifted above zero and carriers V_{cr2} and V_{cr3} are level shifted below zero. Two references used are level shifted, where the shift is equal to magnitude of one carrier used. These references are compared with level shifted carriers to generate switching pulses as shown in Figure 2.3(b). Comparison of reference V_{ref1} with carrier V_{cr1} and V_{cr3} will yield the switching pulses for switch S_{x1} and comparison of reference V_{ref1} with carrier V_{cr2} and reference V_{ref2} with carrier V_{cr1} will generate pulses for switch S_{x4}. The complementary pulses of switches S_{x1} and S_{x4} are summed up and given to bidirectional switch S_{x7}. Figure 2.4(a) and Figure 2.4(b) illustrate the block diagram for switching signals generation for one of the inverter using LSC-IPD technique and LSMR-IPD respectively.

The connections of the stator windings here are transposed such that nine voltages levels are obtained across each phase winding. Since the resultant voltage across any phase is the phasor sum of two voltages, which are phase shifted by 120^{o}, its fundamental component value

will be equal to $\sqrt{3}V_{dc}$, which is faintly less than $2V_{dc}$. Figure 2.5 shows the switching signals for two cycles for switches in one inverter generated from dSPACE 1104.

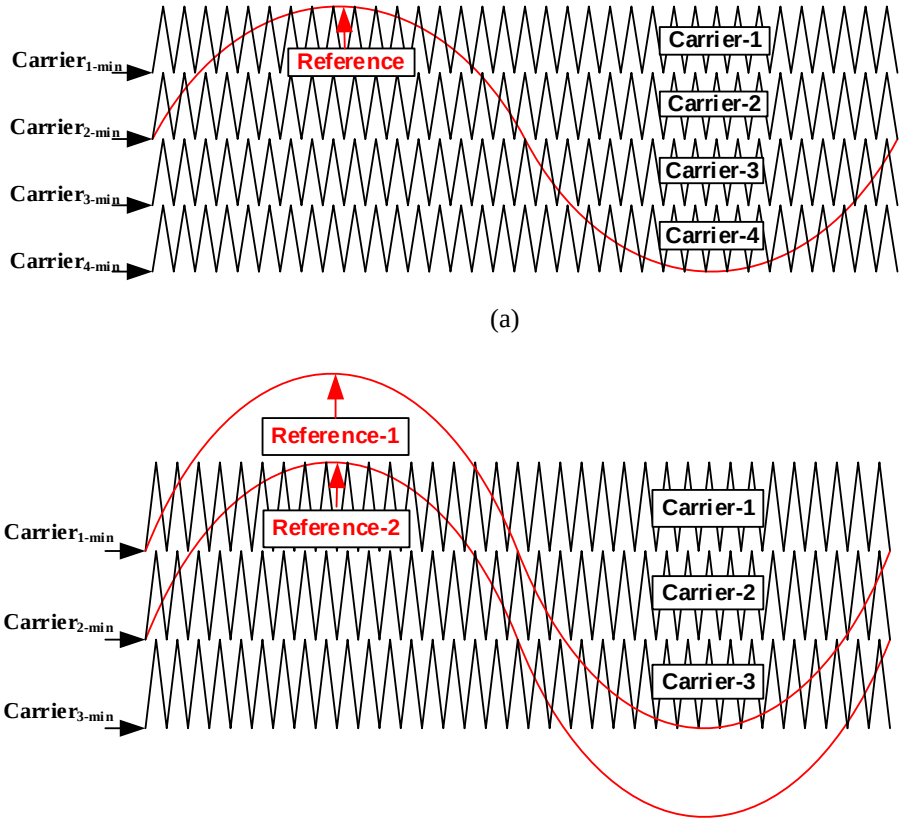


Figure 2.3 Modulation schemes (a) Level shifted carrier (LSC-IPD) SPWM, (b) Level shifted Multi-Reference (LSMR-IPD) SPWM

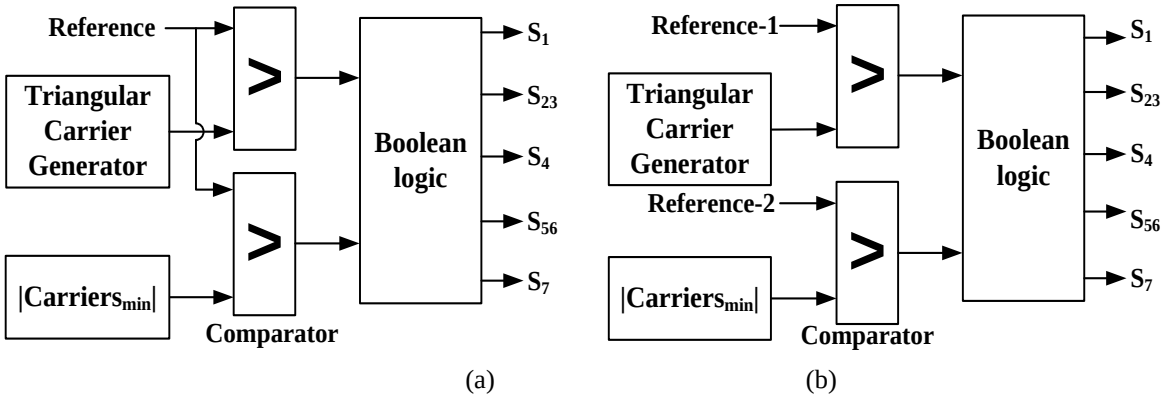


Figure 2.4 Block diagram of switching circuit for the proposed inverter (a) using LSC-IPD SPWM technique (b) using LSMR-IPD SPWM technique.

2.4 Proposed fault-tolerant strategy

The PT is characterized by fault tolerance capability under switch OC and SC conditions without requirement of any additional hardware, but requires post-processing of the switching

PWM signals. During switch OC or SC condition in any of the inverter switches, the converter topology continues to operate without any changes in the modulation technique that is being used before the fault has occurred.

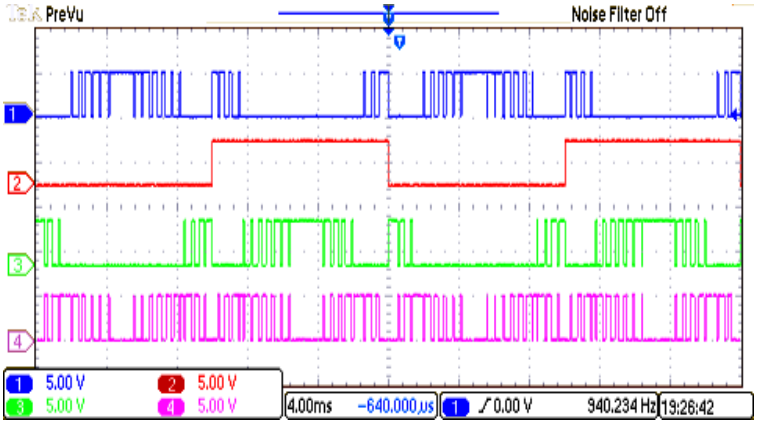


Figure 2.5 Switching pulses for switches S_1 (blue trace), S_{23} (or) $\hat{S}_{56}$ (red trace), S_4 (green trace), S_7 (pink trace) for inverter-a obtained from dSPACE.

2.4.1 For switch open-circuit faults

For switch OC faults in legs, which are connected to motor phase windings in any of the inverters, the number of levels in the output voltage will reduce from nine to seven and the maximum output voltage applied across the phase windings are reduced from $2V_{dc}$ to V_{dc} or $-2V_{dc}$ to $-V_{dc}$. This will affect only the winding connected to the faulty leg of the inverter, which will result in unbalanced supply voltage for the OEWIM drive. For switch OC faults in switches S_{x1} and S_{x4} in modified leg, which are connected to neutral, the number of levels in the output voltage, are reduced from nine to eight and the maximum output voltage gets reduced from $2V_{dc}$ to $1.5V_{dc}$ or from $-2V_{dc}$ to $-1.5V_{dc}$. This will affect two windings connected to that faulty inverter. If the switch OC fault occurs in bidirectional switch, then the output voltage gets distorted and the currents in the two windings connected to such faulty inverter gets affected.

Therefore, with Fault Tolerance Strategy (FTS) for OC fault in any switch except bidirectional switch S_7, in any of the inverter, the switches in the position of faulty switch in other inverters are to be turned-off completely. Along with this, the switching signals of both faulty switch and healthy switch are to be given to the healthy switch in all the inverters. For example, if the switch S_{a2} or switch S_{a3} gets open circuited then switches S_{b2}& S_{b3} and S_{c2} & S_{c3} has to be turned-off. The switching pulses of S_{a2} and S_{a3} have to be given to S_{a5} and S_{a6} respectively along with switching pulses of S_{a5} and S_{a6} as shown in Figure 2.6(a). Likewise, switching pulses of S_{b23} and S_{b56} has to be given to S_{b5} and S_{b6} and switching pulses of S_{c23} and S_{c56} has to be given to S_{c56}. Figure 2.6(b) illustrate working of the PT after applying FTS for

switch S_{a2} OC fault condition. Similarly, if switch S_7 gets open-circuited, then all the switches in similar position in other inverters have to be open circuited, i.e., if S_{a7} gets open circuited then switches S_{b7} and S_{c7} are also open circuited. This will provide identical switching of inverters and balanced voltage for the OEWIM drive.

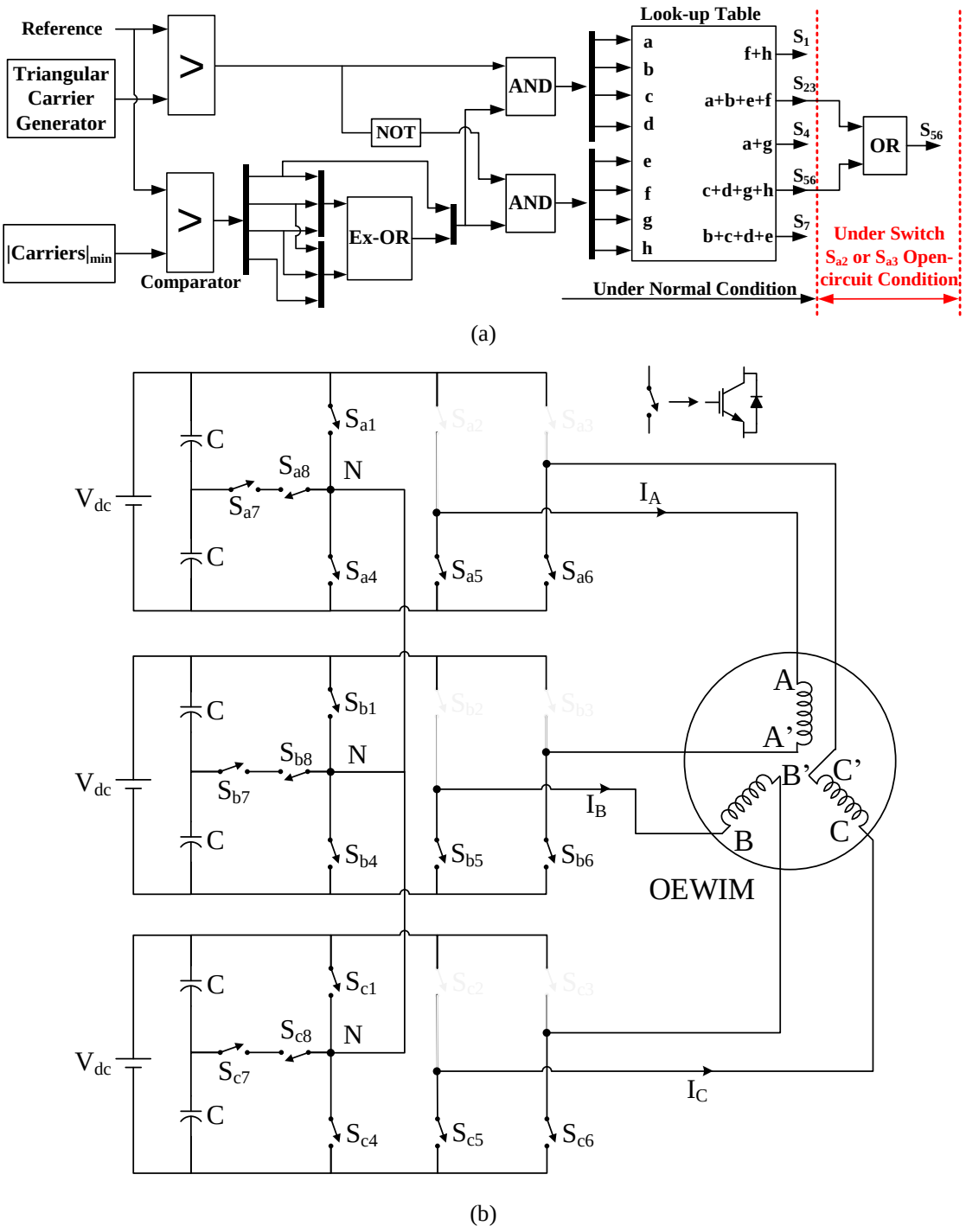


Figure 2.6 (a) Schematic diagram of switching circuit for inverter-a with LSC-IPD for normal and post-fault condition. (b) Working state circuit of proposed topology after applying FTS.

2.4.2 For switch short-circuit faults

If a SC fault occurs in any one switch of the leg, then the inverter leg will create a short circuit across the source and draws heavy currents. It will result in reduced levels in output voltage. Hence, if any switch gets short-circuited, then immediately other switch in the corresponding leg has to be turned-off.

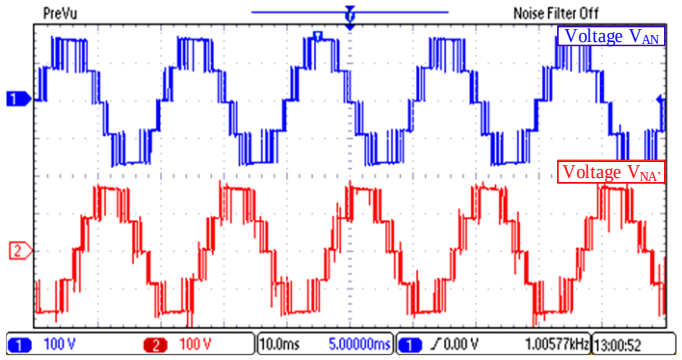
FTS for switch SC faults will be opposite to the one mentioned in FTS for OC fault, i.e., instead of turning-off of the switches in similar positions of the other inverters, here switches are turned-on completely and healthy switches are turned-off completely. For example, if switch S_{a2} gets short-circuited, then switch S_{a5} has to be turned-off. The switches S_{b5} and S_{c5} are to be turned-off completely and switches S_{b2} and S_{c2} are to be turned-on completely. For SC faults in any switch of modified leg, the other two healthy switches have to be turned-off completely. In addition, the switches in similar position of the other inverters have to be turned-on completely and other two healthy switches in other inverters have to be turned-off completely. For example, if switch S_{a1} gets short circuited, then switches S_{a4} and S_{a7} are to be turned-off completely and switches S_{b1} and S_{c1} are to be turned-on completely and switches S_{b4}, S_{b7}, S_{c4} and S_{c7} are to be turned-off.

2.5 Experimental Results

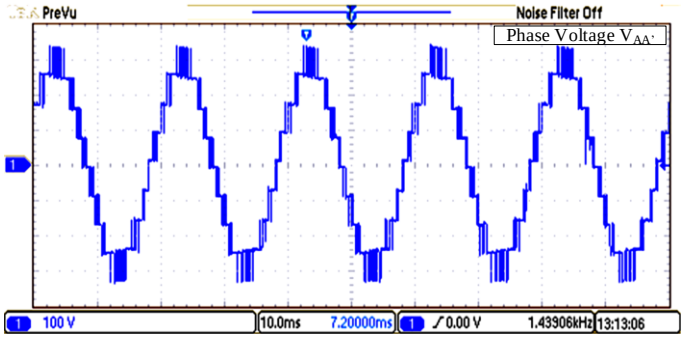
The PT based on three modified-three-phase H-Bridge inverters, each with isolated 100V DC source is experimentally implemented to feed 1-hp OEWIM. The PT is simulated with the conventional SPWM techniques. The OC and SC fault conditions of the switches are then introduced at a suitable interval of time and its response is captured in oscilloscopes. The application of the proposed FTS algorithm is simulated in the MATLAB/Simulink environment. The switching pulses for the prototype are dispensed using dSPACE 1104. A sinusoidal reference wave of 50Hz is compared with the triangular carrier signal of 1.5 kHz to generate switching pulses. The experimentally obtained waveforms for the voltages and currents from the star connected VSI MLI topology using LSPWM strategy is illustrated in Figure 2.7 and Figure 2.8. Figure 2.7(a) represent voltage V_{AN}, the voltage across points 'A' and neutral, whereas voltage $V_{NA'}$, is the potential across the point 'A'' and neutral (from inverter-b) and Figure 2.7(b) represents the voltage $V_{AA'}$ across phase-A winding.

The output voltage waveforms of the inverter-a & inverter-b have five possible voltage levels ($+2V_{dc}$, $+V_{dc}$, 0, $-V_{dc}$ and $-2V_{dc}$). Hence the load voltage across any phase winding will have nine output voltages ($-4V_{dc}$, $-3V_{dc}$, $-2V_{dc}$, $-V_{dc}$, 0 $+V_{dc}$, $+2V_{dc}$, $+3V_{dc}$ and $+4V_{dc}$) because

the load voltage is the difference between the output voltages of inverter-a and inverter-b. This is evident for the multilevel operation of the PT with the output voltage magnitude twice that of the DC source. Figure 2.8 depicts the experimentally obtained waveforms of three-phase motor phase voltages and no-load currents of the OEWIM. From Figure 2.9(a), the top trace indicates the motor phase voltage $V_{AA'}$. The bottom traces in Figure 2.9(a) and Figure 2.9(b) depicts the motor phase currents for a load current of 2 amperes and full load rated current of 3.2 amperes, respectively, with a current scale of 2A/div.



(a)



(b)

Figure 2.7 Experimental results of (a) voltages V_{AN} and $V_{NA'}$ (b) Phase Voltage $V_{AA'}$

Figure 2.10(a) shows the harmonic spectrum of the phase-A load voltage ($V_{AA'}$) and Figure 2.10(b)shows the harmonic spectrum of current in phase-A for LSPWM-IPD strategy. It is clear from the spectrum that the dominant harmonics are crowded around the range of carrier frequency and its integral multiples. The measured THD of the unfiltered output voltage was THD_v=11% similarly the THD of load current was THD_i=3%, confirming very low distortion of the currents in the load. Since both the switching strategies, when applied this PT will yield identical output for all operating conditions. Hence, LSPWM-IPD is explicitly considered in the experimental analysis of the PT.

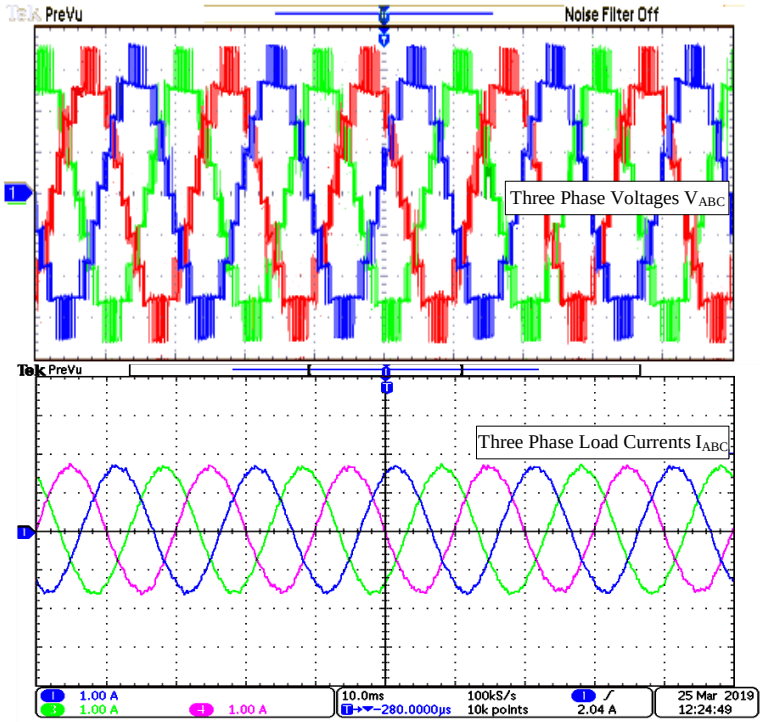


Figure 2.8 Motor phase voltages with 50V/div in top trace: $V_{AA'}$ (red), $V_{BB'}$ (blue), $V_{CC'}$ (green); and no-load motor phase currents in bottom trace: I_A (blue), I_B (green), I_C (pink)

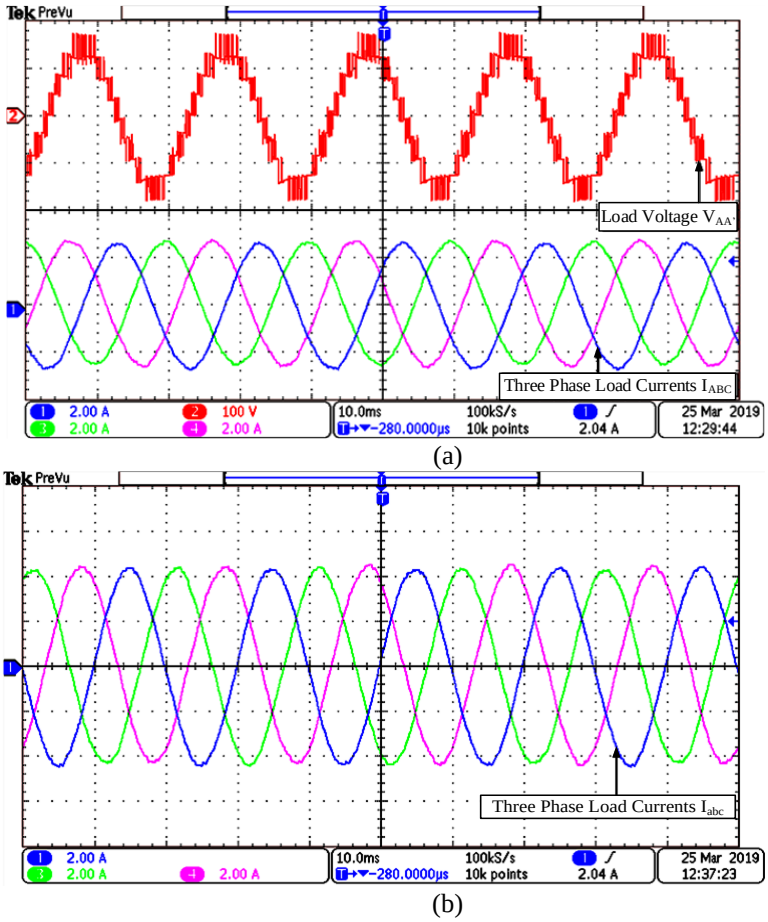
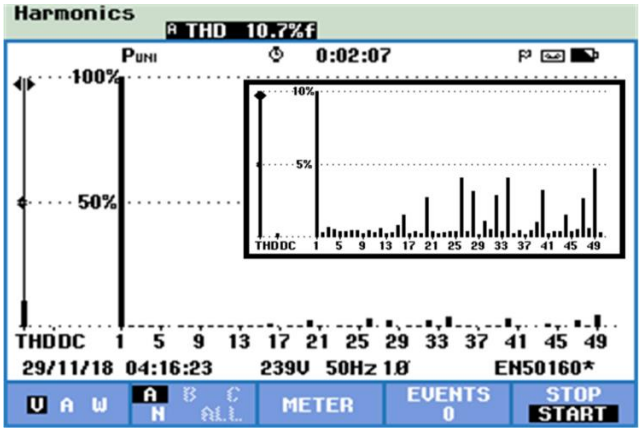
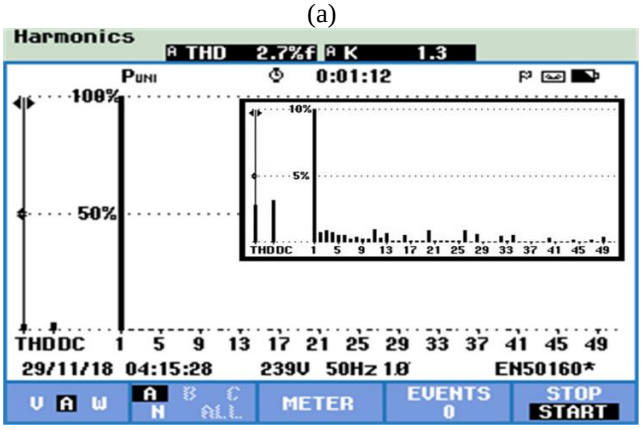


Figure 2.9 Experimental results of (a) load voltage $V_{AA'}$ and three phase load currents I_{ABC} for 2 amperes of load current (b) three phase load currents I_{ABC} for 3.2 amperes of load current.



(a)



(b)

Figure 2.10 FFT Analysis of (a) Motor phase voltage, $V_{AA'}$ and its zoomed view (inside). (b) Motor phase current I_A and its zoomed view (inside).

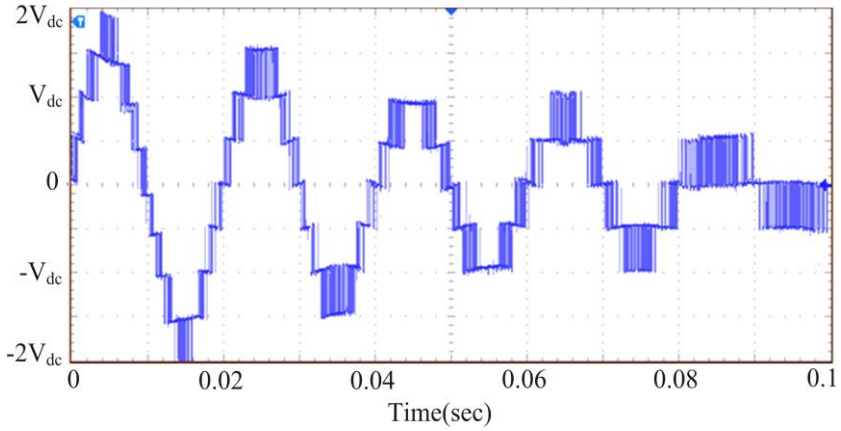


Figure 2.11 Phase voltage $V_{AA'}$ with modulation indices, M_a= 1 from 0 to 0.02 sec, M_a = 0.8 from 0.02 to 0.04 sec, M_a = 0.6 from 0.04 to 0.06 sec, M_a= 0.4 from 0.06 to 0.08 sec, M_a= 0.2 from 0.08 to 0.1sec.

The output load voltage across phase-A winding ($V_{AA'}$) for various values of modulation indices is illustrated in Figure 2.11. From this it is observed that the PT can operate at any modulation index (for M_a=1, 0.8, 0.6, 0.4, 0.2). Reduction in the value of M_a will reduce the levels in the output voltage.

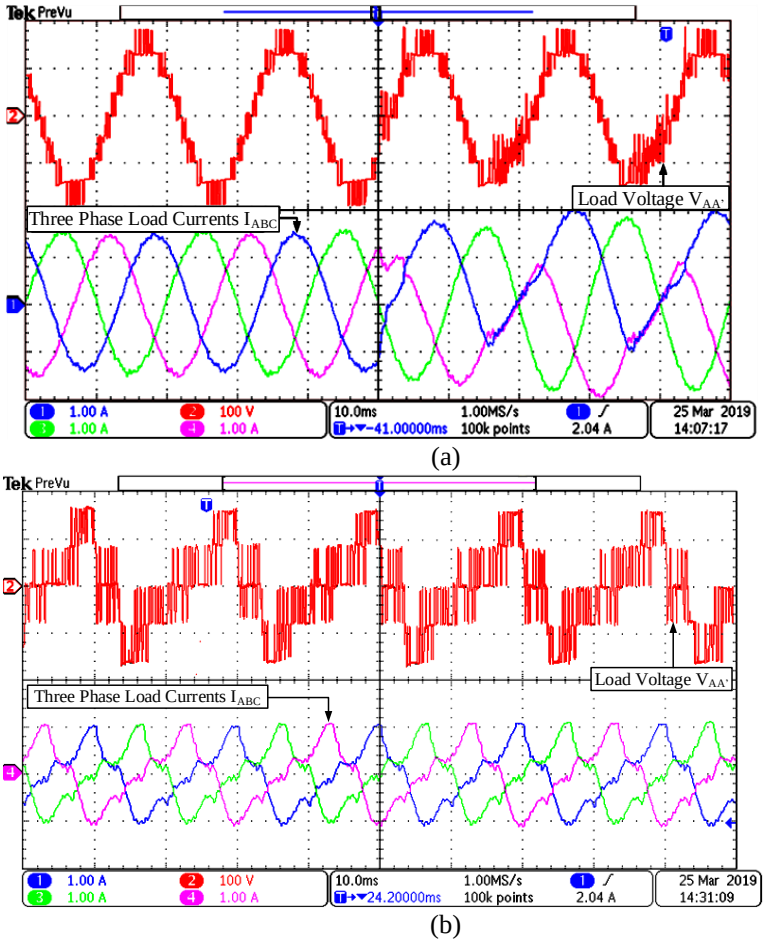


Figure 2.12 Waveforms of $V_{AA'}$ (top trace in red) and no-load phase currents I_A (blue), I_B (green), I_C (pink) (a) with S_{a1} open-circuited at t=50ms, (b) with FTS for S_{a1} open-circuit fault.

2.5.1 For switch open-circuit faults

The PT is tested under switch OC and SC conditions with LSPWM-IPD strategy. For the sake of clarity, two cases of OC faults are considered. Firstly, if the fault occurs in any one switch (S_{x1} or S_{x4}) of the first leg of the inverter, which formed the neutral point (V_N). To affect the supposedly considered open-circuited fault condition of S_{a1}, the switching pulses are disengaged from S_{a1} and the corresponding results were presented in Figure 2.12. The phase-A voltage across the motor winding ($V_{AA'}$) and three-phase no-load motor phase currents I_A(blue trace), I_B (green trace) and I_C (pink trace) under with switch S_{a1} open circuited at time t = 50ms are presented in Figure 2.12(a). The waveform of $V_{AA'}$ appears to have reduced voltage levels in the negative cycle with distortions. From the current traces of I_A and I_C, it is observed that they are unbalanced and possess DC component, while the I_b is undisturbed. For S_{a1} open-circuited condition, the proposed FTS is applied to the switching pulses of the inverters and the experimental results were presented in Figure 2.12(b). Phase voltage $V_{AA'}$ and no-load currents across the three phase windings of the motor appears to be balanced. The current waveforms

may not be sinusoidal, but are balanced and symmetrical without DC component. Applying FTS will ensure continuous operation of the OEWIM drive without any circuit hardware alterations.

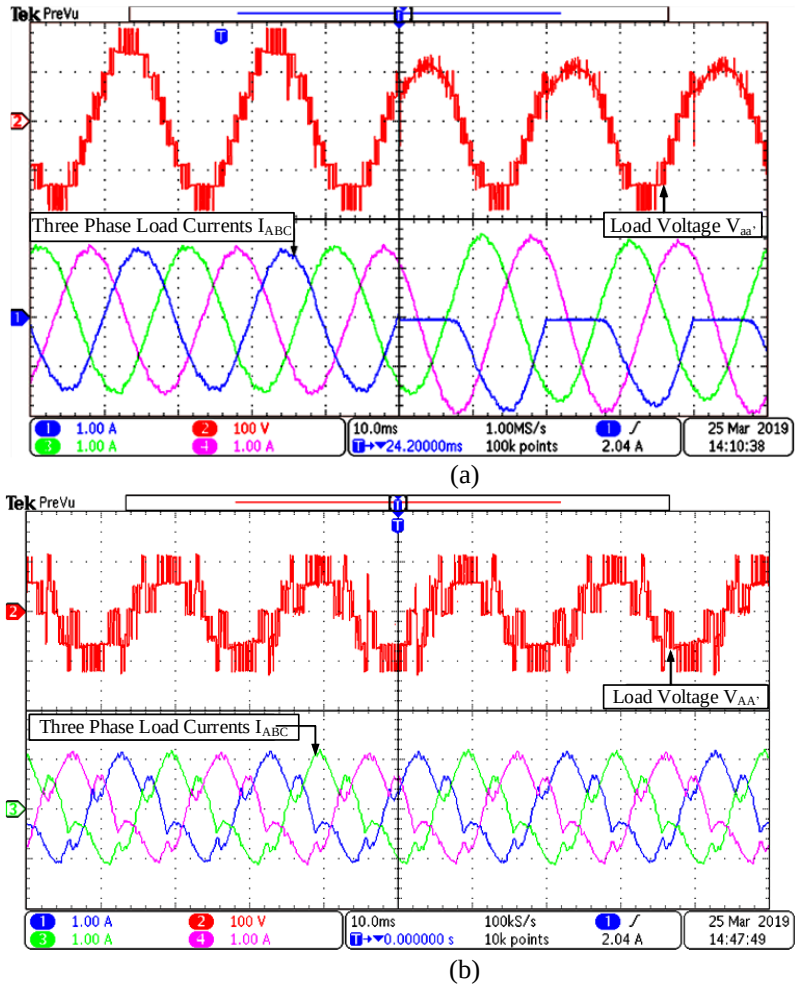


Figure 2.13 Waveforms of $V_{AA'}$ (top trace) and no-load phase currents I_A (blue), I_B (green), I_C (pink) (a) with S_{a2} open-circuited at t=50ms, (b) with FTS for S_{a2} open-circuit fault.

On the other hand, consideration is the occurrence of an OC fault in any switch (S_{x2} through S_{x6}) of the legs from where the motor phase windings are connected. For simplicity, assuming the OC fault on switch S_{a2} of the second leg of inverter-a, from where one of the phase-a terminal of the OEWIM is connected. Figure 2.13(a) depicts the phase-a voltage across the motor winding ($V_{AA'}$) and the three phase currents under no-load condition with switch S_{a2} open circuited at time t = 50ms. The waveform of $V_{AA'}$ appears to have reduced voltage levels in the positive half cycle with distortions. Again from the same figure, the three-phase no-load motor phase currents I_A (blue trace), I_B (green trace) and I_C (pink trace) are depicted. At the occurrence of a fault, both I_B and I_C are undisturbed, while the phase-a current (I_A) appears to have high DC content. It is observed from I_A trace, the nature of current waveform in the motor

phase-A winding of OEWIM is similar to a half-wave rectifier output, which is not desirable. This undesirable current waveform may cause further complications affecting the power circuit configuration and the performance of the OEWIM drive system. To address this situation, the proposed FTS algorithm is applied, i.e., the switching pulses supplied to the healthy switches of the inverters are amended. Figure 2.13(b) depicts the results of the proposed FTS algorithm to the PT. It is observed that the motor phase voltage across phase-a winding and the traces of no-load currents I_A (blue), I_B (green) and I_C (pink) are symmetrical in nature.

2.5.2 For switch short-circuit faults

In the event of a SC fault in any of the switches, then the healthy switch of that particular leg has to be turned-off and FTS algorithm has to be applied. Turning-off the healthy switch in the leg of faulty switch prevents SC across the source. Applying FTS for switch SC fault in legs connected to windings will yield the same results as FTS applied to switch OC fault. However, for SC faults in switches of modified leg the strategy is explained.

To infer the characteristics of the PT with FTS for the short-circuited switch S_{a1}, the switch S_{a1} is completely turned-on and switches S_{a4}& S_{a7} are completely turned-off. As mentioned in FTS the switches S_{b1} and S_{c1} are turned-on completely and switches S_{b4}, S_{b7}, S_{c4} and S_{c7} are turned-off completely. The experimental results for $V_{AA'}$ and the no-load three phase currents I_A(blue trace), I_B (green trace) and I_C (pink trace) are depicted in Figure 2.14 after adopting FTS for switch S_{a1}SC fault. The output voltages and load currents resemble the same even for other two switches (S_{a4} and S_{a7}) under SC conditions.

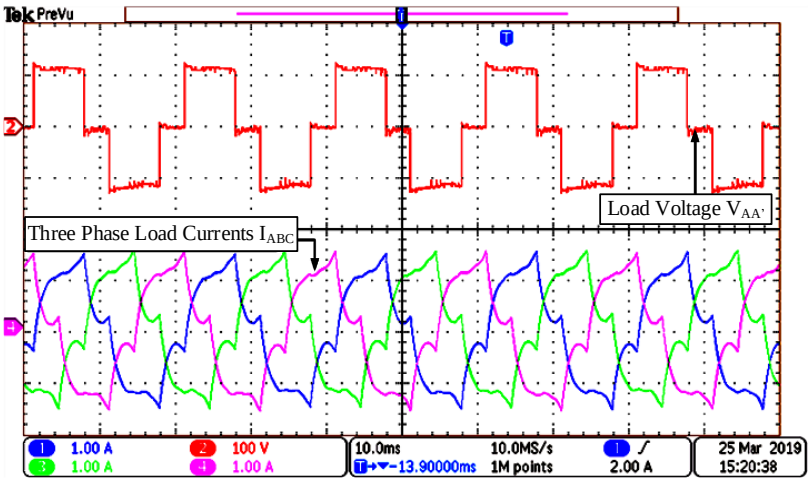


Figure 2.14 Waveforms of $V_{AA'}$ (top trace) and no-load phase currents I_A (blue), I_B (green), I_C (pink) with FTS for S_{a1} short-circuit fault

The voltage of the DC-link capacitors is at balance during normal operating condition with the switching strategy used. The PT may be subjected to different fault conditions such as switch OC and SC conditions. These types of fault affect the voltage balance in the capacitors. The nature of capacitor voltages under normal operating conditions, during switch OC fault condition and during FTS condition are depicted in Figure 2.15(a). The upper trace indicates the voltage across the upper capacitor and lower trace indicates the voltage across lower capacitor of the inverter-a. The voltage across upper capacitor during switch OC condition sees a voltage rise from $V_{dc}/2$ to V_{dc} (top trace of Figure 2.15(a)). The capacitor unbalance occurs because of OC fault. Under normal operating conditions due to symmetry in switching pattern of switches, load current flowing through both the upper and lower capacitor is equal and hence voltage across the capacitors will be equal. Due to OC in switch S_{a2}, the switching symmetry gets affected and hence the current flowing through the capacitors and therefore the voltage across capacitors gets affected. Voltage across upper capacitor gets increase near to source voltage V_{dc} whereas the voltage across lower capacitor decreases near to zero.

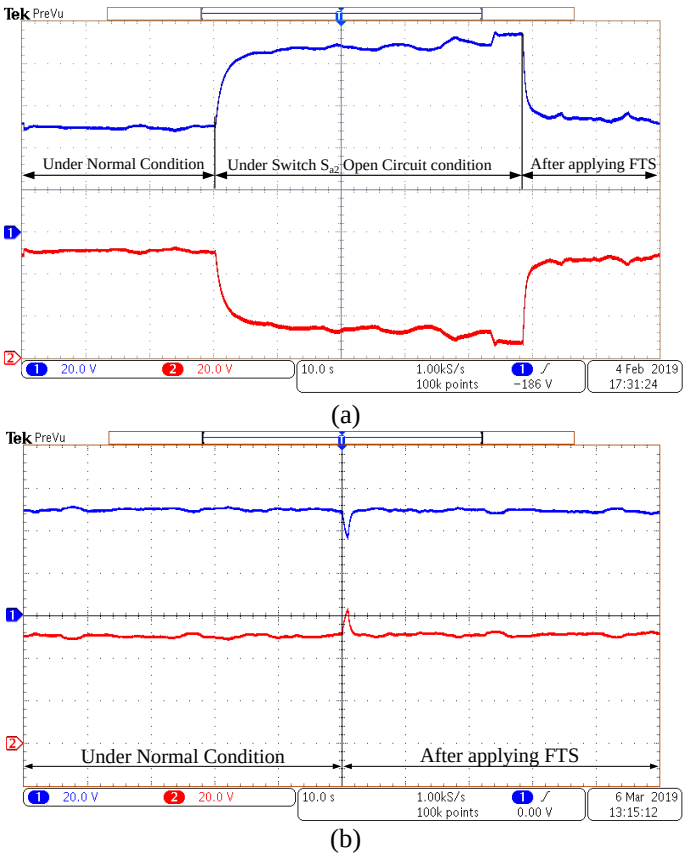


Figure 2.15 Voltage across capacitors (a) during normal operation, during switch S_{a2} open circuit condition and after application of FTS, (b) during normal operation and after application of FTS for switch S_{a2} short circuit.

Once the fault tolerance strategy (FTS) is applied, the symmetry in switching pattern is regained and the voltage across capacitors is equalized. Since the voltage across upper capacitor

during switch OC condition has increased from a value of $V_{dc}/2$ to V_{dc}, the capacitors used should of sufficiently high capacity to withstand increase in voltage during fault conditions until the FTS is applied. Therefore, the voltage rating of the capacitors should be equal to source voltage such that the topology can sustain during switch OC faults. Figure 2.15(b) depicts the pre-fault and post-fault voltages across the capacitors for switch S_{a2}SC condition. Figure 2.16 shows the experimental setup for the proposed H-Bridge MLI topology for a 1-hp OEWIM drive.

2.6 Comparative analysis

A comparison of component count of the PT with existing nine-level topologies in terms of various parameters such as number of levels in the output voltage (N_L), number of switches (N_{sw}), number of DC sources (N_{source}), number of gate drivers (N_{driver}), number of diodes (N_{diode}), number of capacitors ($N_{capacitor}$), Total Blocking Voltage (TBV) in p.u. and total component count and is illustrated in Table 3.2. As can be seen from Table 3.2, both NPC and FC topologies require only one DC source with voltage rating of $V_{DC;}$ whereas conventional CHB requires twelve isolated DC sources of voltage rating of $V_{DC}/8$. Similarly, Asymmetrical CHB requires three isolated DC sources of voltage rating $3V_{DC}/8$ and three controlled DC sources of voltage rating $V_{DC}/8$. The topology proposed by P. P. Rajeevan *et al.,* and V. F. Pires *et al.,* requires two and three isolated DC sources respectively of voltage rating $V_{DC}/2$. Similarly, the topology proposed by K. Sivakumar *et al.,* also requires two dc sources of voltage rating $V_{DC}/2$ for satisfactory operation of the topology. The topology proposed by A. Kshirsagar *et al.,* requires isolated DC sources of voltage rating $3V_{DC}/4$ and $V_{DC}/4$ and the seven level inverter topology proposed by G. Mondal *et al.,* requires six sources of voltage rating $V_{DC}/12$. The PT requires three isolated DC sources of voltage rating $V_{DC}/2$. From Table 3.2, the component count for topology proposed by V. F. Pires *et al.,* is least of all but the number of levels in the output are five and the number of components required for the PT is less when compared with other existing nine-level topologies. The TBV remain same as the switch count for NPC, FC and conventional CHB topologies because the Maximum Blocking Voltage and Peak Inverse Voltage (PIV) of switches are same as the source voltage of the topology.

To further asses the lucrative merits of the PT, a cost comparison based on the cost-influencing factors that dictates the overall cost of the inverter is done and illustrated in Table3.3. In order to evaluate the merits a case study with a load of 2kW with an input voltage V_{DC} of 200V is considered. The ratings of the components are chosen in accordance with the

configuration of the topologies under comparison. The total cost for each topology is enlisted in Table 3.3**.** The cost evaluation assigns an equal importance to the number of components, TBV and PIV while considering voltage rating and current rating of the components without margin. However, components of lower voltage rating are selected considering rated current parameters. It can be seen from Table 3.3that the cost of the inverter circuit in V. F. Pires *et al.,* is less comparatively and the cost of the PT is lower than all other nine-level topologies except Asymmetrical CHB**.** However, the Asymmetrical CHB is to be operated with controlled and uncontrolled DC sources, which makes it operation typical. Therefore the PT has least component count and has comparatively low cost for the nine level inversion that makes its usage viable.

Table 2. 2 Component Count Comparison of the PT with other MLI topologies feeding OEWIM drives

MLI Type	**N_L**	**N_{sw}**	**N_{driver}**	**N_{diode}**	**N_{source}**	**$N_{capacitor}$**	**TBV(p.u.)**	**Component Count**
NPC	9	48	48	168	1	9	48	274
FC	9	48	48	48	1	85	48	230
Conventional CHB(CCHB)	9	48	48	48	12	12	48	168
Asymmetrical CHB(ACHB)	9	24	24	24	6	6	24	84
P. P. Rajeevan *et al.*,(2013) {1}	9	36	36	36	2	12	36	122
V. F. Pires *et al.*,(2017) {2}	5	18	18	18	3	0	18	57
K. Sivakumar *et al.*,(2010) {3}	5	24	24	24	1	3	24	76
A. Kshirsagar *et al.*, (2018) {4}	17	36	36	36	2	9	36	121
G. Mondal *et al.*,(2009) {5}	7	48	48	60	6	6	48	168
Proposed Topology [PT]	9	24	24	24	3	6	24	81

Table 2. 3 Cost comparison of the proposed topology with other MLI topologies feeding OEWIM drives

Part	Part Number	Ratings	Unit Price*($)	NPC	FC	CCHB	ACHB	{1}	{2}	{3}	{4}	{5}	PT
MOSFETs	IRFP240PBF	200 V, 20 A	2.1					12	18		12		
	IRFP140PBF	100 V, 20 A	1.93				12	12		24	12		24
	IRFIZ34GPBF	60 V,20 A	1.28	48	48	48	12	12			12	48	
Diodes	STPS20SM60D	60 V,20 A	1.24	168								12	
Capacitor	LLG2D222-MELC40	200 V, 2.2 mF	6										6
	LLS2A222-MELA	100 V, 2.2 mF	3.93	9	85	12	6	12		3	9	6	
Gate Driver	IR2110STRPBF		1.34	48	48	48	24	36	18	24	36	48	24
Total cost ($)				369.4	459.8	172.9	94.26	159.12	61.92	90.27	147.3	164.2	114.5

Courtesy: www.galco.com, www.digikey.in. * Price may vary subjected to market growth.

The PT ensures its operation under normal conditions with nine levels in the output voltage across each of the phase winding with a voltage level of $V_{dc}/2$. Under switch fault conditions such as switch OC or SC conditions, the PT will ensure continuous operation with reduction in output power level as the voltage levels gets decreased due to fault in the switches. This continuous operation of the PT accomplished by modifying the switching pulses fed to the switches. With the analysis of PT under normal and abnormal conditions with pre and post-

fault analysis, it can be justified that the PT exhibits fault tolerance property for all possible faults in switches.

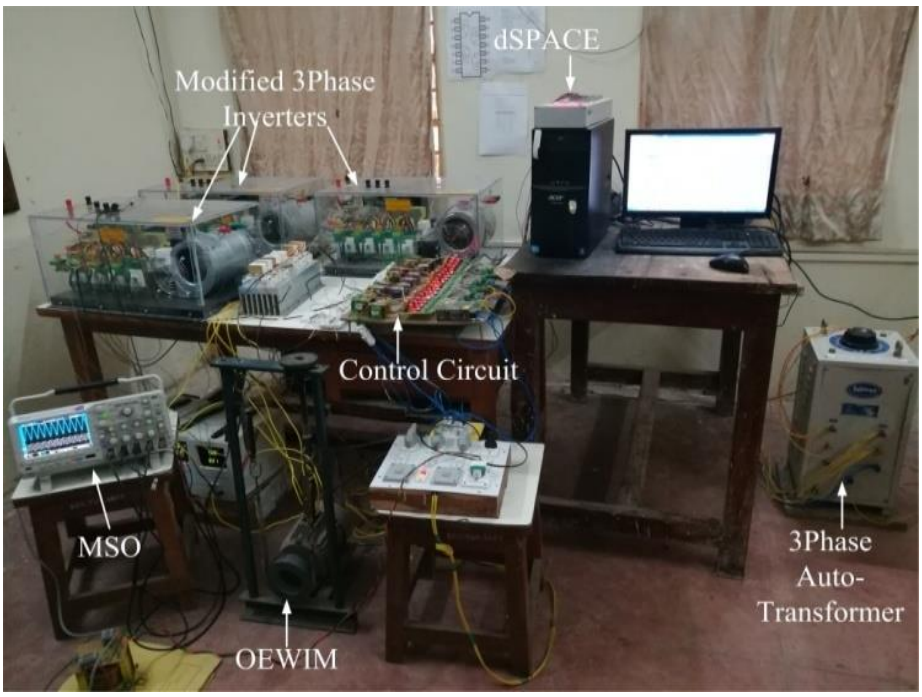


Figure 2.16 Experimental setup of the proposed topology

Every MLI topology has its own merits and demerits depending on the field of application. The PT is not an exception. Compared to the conventional topologies like NPC topology, FC topology and CHB topologies, the PT has some demerits like its non-modular structure and this requires three DC sources. Nevertheless, in applications such as battery driven electric vehicles fed by solar PV panels or fuel cells the PT suits well because of its low supply voltage requirement and its fault tolerant property. Since the PT can also be used with Volt/Hertz control of induction motor and hence finds application in industries such as steel rolling mills, paper rolling mills, etc.,.

2.7 Summary

This chapter presents a new star connected MLI topology for OEWIM drive. The proposed model employs three modified H-Bridge inverters connected in star configuration. This arrangement attains output voltage of twice the DC link voltage in nine levels for the OEWIM drive. The PT ensures the fault tolerance capability for switch OC faults and switch SC faults without using any external hardware but by simple post processing of the PWM signals. PT can employ conventional PWM techniques that add additional advantage when implemented in digital platforms such as dSPACE or DSP. In this work, to generate switching

pulses level-shifted carrier SPWM (with IPD) is used. Component count of the topology is comparatively less whereas, effective cost of the inverter is less when compared with other nine-level inverter topologies except asymmetrical CHB topology. The drawback of this topology is that it employs capacitors of voltage rating equal to source which will increase the cost and size of inverter. The behaviour of the PT is analysed under various possible switch OC and switch SC fault conditions. A fault-tolerance strategy (FTS) is proposed for switch OC and SC faults, which adds fault tolerance capability to the PT. Implementation of FTS does not require any additional hardware, hence no increase in the cost of the topology. This topology is capable of providing balanced three-phase output voltage for OEWIM drive even under switch fault conditions. Although the inverter operates at reduced power rating, it ensures continuity in operation of the drive with balanced three-phase supply and reduced DC component in output voltage.

Chapter 3

A Nine-Level Inverter for Open Ended Winding Induction Motor Drive with Fault-Tolerance

Chapter 3

A Nine-Level Inverter for Open Ended Winding Induction Motor Drive with Fault-Tolerance

3.1 Introduction

Advances in material science has changed the face of the power systems with increased involvement of power electronic components. The extended operating range of power semiconductor switches aids in designing of MLIs (MLIs) for medium and high voltage applications. However, owing to the advantages such as increased voltage levels, enhanced harmonic profile, reduced voltage stress on power semiconductor devices, flexibility of operation, reduced interference with the communication signals, lower slew rates in output voltages compared to conventional two level or three level VSIs make their application inevitable. With these advantages, MLIs find vast applications in power system transmission and electric drive applications. MLIs with increased number of voltage levels reduces harmonic distortions and elude the need for expensive and bulky filters, hence such MLIs are preferred in drive applications. Nevertheless, the increase in voltage levels are attained with increased number of components, hence the industry is reluctant for such MLIs because of uncertainty of reliability and control complexity. This provides the need for designing MLIs with high number of voltage levels but with fewer components. With increase in component count, the reliability of the system decreases. Failure of a single switch may lead to a complete shutdown of the system. Hence reduced switch-count MLIs with fault tolerance capability find better applications in industrial drives these days. MLIs with increased output voltage levels and reduced control complexity were proposed to extract the best performance of the induction motors in the drive applications.

This chapter presents a nine level inverter for an open ended winding induction motor (OEWIM) drive with fault-tolerance property for switch faults. The proposed topology (PT) consists of three three-phase inverters with an isolated DC source for each inverter, three bi-directional switches and three capacitors. The three inverters are configured such that they all have a common neutral connection between them. Such configuration provides the advantage of producing peak output voltage twice the source voltage magnitude and hence lower rating voltage sources can be employed. Conventional SPWM techniques are employed for generating

gate pulses for the switches in the PT for normal and post-fault operation. A fault-tolerance strategy is proposed for the post-fault operation of the inverter to produce balanced three phase supply.

3.2 Analysis of proposed topology

The PT employs three three-phase voltage source inverters (VSIs) each with an isolated DC source connected in a star configuration. Additionally, a branch consisting of a capacitor with a bidirectional switch in series is connected across the lower switch of the first leg in in each VSI as illustrated in Figure 3.1. The bi-directional switch is realized with two switches (here IGBTs) connected in anti-series with common emitter configuration. The switches S_{11} through S_{17} represent inverter-1. Similarly, the switches S_{21} through S_{27} and S_{31} through S_{37} represent inverter-2 and inverter-3 respectively.

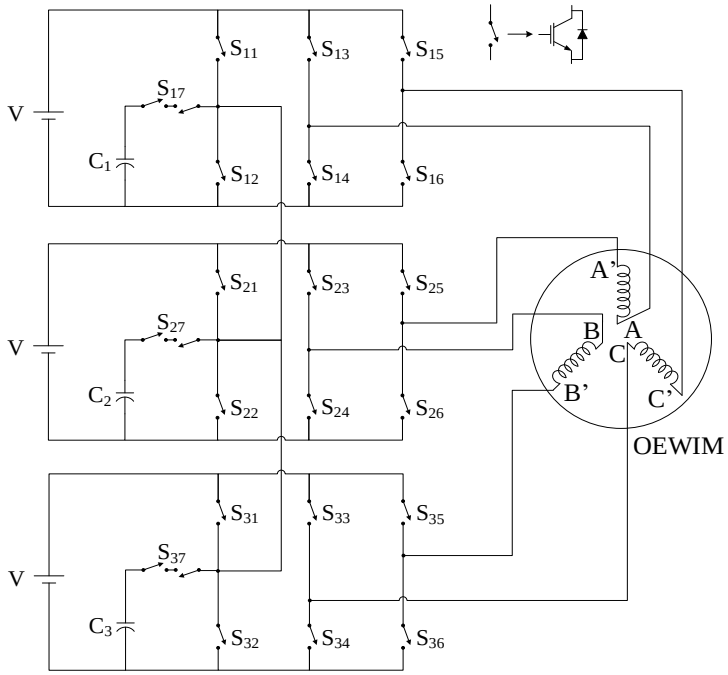


Figure 3. 1 Proposed modified-leg H-bridge based topology (MLBBT).

The PT is configured such that each inverter will give out three output connecting terminals. First terminal is from the mid-point of switches S_{x1} and S_{x2} (where x ϵ 1, 2, 3), the same point where one end of bidirectional switch is connected. The second and third terminals are taken from mid-points of switches S_{x3}-S_{x4} and S_{x5}-S_{x6} respectively. The first terminals of all the three inverters are connected together and forms the neutral connection of the inverters. The second and the third terminals are connected to phase windings of the OEWIM and the connections are made such that each inverter feed two distinct phases at distinct ends.

For example, inverter-1 second terminal is connected to phase-A winding at end A whereas the third terminal is connected to phase-C winding at end C'. Other two inverters are also connected in the similar manner. The idea behind such configuration is that each phase winding is connected between two inverters that are fed from separate sources and switched with 120^0 phase shift. This will allow the phase winding to experience a resultant fundamental voltage magnitude of $\sqrt{3}$ times of the source voltage with a peak voltage magnitude of twice the source voltage.

Table 3.1 Switching states of inverters and corresponding voltage levels across phase winding-A ($V_{AA'}$)

Voltage $V_{AA'}$	Inverter-1				Inverter-2				Capacitor state
	S_{11}	**S_{12}**	**S_{13}**	**S_{17}**	**S_{21}**	**S_{22}**	**S_{25}**	**S_{27}**	
2V	0	1	1	0	1	0	0	0	No change
3V/2	0	0	1	1	1	0	0	0	C_1-Charging
	0	1	1	0	0	0	0	1	C_2-Discharging
V	0	1	1	0	0/1	1/0	0/1	0/0	No change
	0/1	1/0	0/1	0/0	1	0	0	0	
V/2	0	0	1	1	1/0	0/1	1/0	0/0	C_1-Charging
	0/1	1/0	0/1	0/0	0	0	0	1	C_2-Discharging
0	1	0	1	0	1/0	0/1	1/0	0/0	No change
	0	1	0	0	1/0	0/1	1/0	0/0	
	1/0	0/1	1/0	0/0	1	0	1	0	
	1/0	0/1	1/0	0/0	0	1	0	0	
-V/2	0	0	0	1	1/0	0/1	1/0	0/0	C_1-Discharging
	1	0	0	0	0	0	0	1	C_2-Charging
-V	1/0	0/1	1/0	0/0	0	1	1	0	No change
	1	0	0	0	1/0	0/1	1/0	0/0	
-3V/2	0	0	0	1	0	1	1	0	C_1-Discharging
	1	0	0	0	0	0	1	1	C_2-Charging
-2V	1	0	0	0	0	1	1	0	No change

Comparing with dual inverter configuration, the PT requires an additional DC source but delivers increased peak output voltage, i.e., $2V_{dc}$ whereas $1.33V_{dc}$ in case of dual inverter. Owing to this property of the PT, DC sources with lower voltage rating can be employed which would reduce the blocking voltage capacity of the switching devices. This offers further scope for employing lower power rating high frequency semiconductor switches (such as MOSFETs), which will be an additional advantage. The direct applicability of the conventional SPWM technique is another advantage because the computational burden on the digital processors reduces.

The possible switching states of the inverter-1 and inverter-2 feeding phase-A winding and corresponding voltage levels obtained are presented in Table 3.1. The switches S_{11}, S_{12}, S_{13}, S_{14} and S_{17} of inverter-1 and S_{21}, S_{22}, S_{25}, S_{26} and S_{27} of inverter-2 determine the voltage magnitude across the phase-A winding. Since switches S_{13} and S_{14} operate in complementary with each other, only switching states of S_{13} are presented. Similarly, for switches S_{25} and S_{26}, only switching states of S_{25} are presented in Table 3.1.

The voltages across the winding terminals are dependent on the switching states of the switching devices. Considering the switches are ideal, their blocking and conduction states are represented by binary variables as 0 and 1 respectively. Considering inverter-1, the following conditions can be depicted from the switching states as

If S_{13}= 1 then S_{14} = 0, i.e., if switch S_{13} is ON then switch S_{14} is OFF

if S_{14} = 1 then S_{13} = 0, i.e., if switch S_{14} is ON then switch S_{13} is OFF

Similarly, if S_{11} = 1, then S_{12} = S_{17} = 0,

if S_{12} = 1, then S_{11} = S_{17} = 0,

if S_{17} = 1, then S_{11} = S_{12} = 0.

These conditions are also applicable for the other two inverters as well and with this representation the equation for output voltage across the phase-A winding can be written in terms of the switching states as

$$V_{AA'} = [S_{13}(S_{12}+0.5S_{17}) - S_{14}(S_{11}+0.5S_{17})] - [S_{25}(S_{22}+0.5S_{27}) - S_{26}(S_{21}+0.5S_{27})] \quad (3.1)$$

3.3 Modulation Scheme

The PT exploit the benefit of employing conventional SPWM techniques for generating switching pulses. The operation of the PT can be categorized as normal and post-fault operation. Hence to deliver balanced three phase supply in both the pre- and post-fault conditions two types of SPWM techniques are employed for the PT. In-phase disposition (IPD) level-shifted carrier technique is used in normal operating conditions and the phase-shifted SPWM technique (PS-SPWM) is employed for the post-fault operation.

3.3.1 In-Phase disposition SPWM technique

IPD SPWM technique is employed for normal operating conditions because this modulation technique has the advantage of producing better harmonic profile compared to its counter parts. Triangular waves with in-phase disposition are employed as carriers and a modified sinusoidal wave is employed as reference wave. The triangular carrier waves with switching frequency are compared with a sinusoidal reference signal of power frequency to generate the switching pulses as illustrated in the Figure 3(a). The boolean logic for switching pulses for the switches in the inverter-1 are presented in Figure 3(b).

The scheme of generating switching pulses for inverter-2 and inverter-3 remains the same except that the reference signal is displaced by 120^0 and 240^0 respectively. Hence the switching pulses are generated by comparison and the logic circuits. Consider the inverter-1: the switches S_{13} and S_{15} operate simultaneously and will be in turned-on condition for complete first half cycle and will be turned-off for next half cycle of the reference wave. The same will be repeated throughout the operation. Similarly the switches S_{14} and S_{16} operate simultaneously and complementary with switches S_{13} or S_{15}. These switches are directly connected to phase windings of the OEWIM. The switches S_{11} and S_{12} operate in complementary with S_{17}. The corresponding switches in other inverters will operate in the similar manner.

3.3.2 Phase shifted SPWM technique

This modulation technique is employed for post-fault operation of the PT. PS-SPWM technique employs a single carrier and two reference signals that are 180^0 out of phase. The reference signal for inverter-1 can be labelled as Ref_1 and the out of phase reference signal as $–Ref_1$. Similarly, the reference signals for inverter-2 and inverter-3 can be labelled as Ref_2 and Ref_3 that are displaced by 120^0 and 240^0 from Ref_1 respectively. The reference signals are compared with carrier wave to generate the switching pulses. The comparison of carrier wave and Ref_1 will produce switching pulses for switches S_{11} and its complementary pulses are given to switch S_{12}. In the same manner, the comparison of carrier wave with $-Ref_1$ wave will produce switching pulses for switches S_{13} and its complementary pulses are given to switch S_{14} of inverter-1. Similarly for inverter-2, Ref_2 and $– Ref_2$ are used to produce switching pulses for S_{21} and S_{23} respectively. Ref_3 and $-Ref_3$ are utilized to produce switching pulses for the switches S_{31} and S_{33} respectively. In the post-fault operation for switch OC faults, to obtain symmetrical and balanced output voltage, the use of capacitor is restricted hence no pulses are fed for switch

S_{17}. The scheme of PS-SPWM and the obtained pulses for switches S_{11} and S_{13} are illustrated in Figure 3.3.

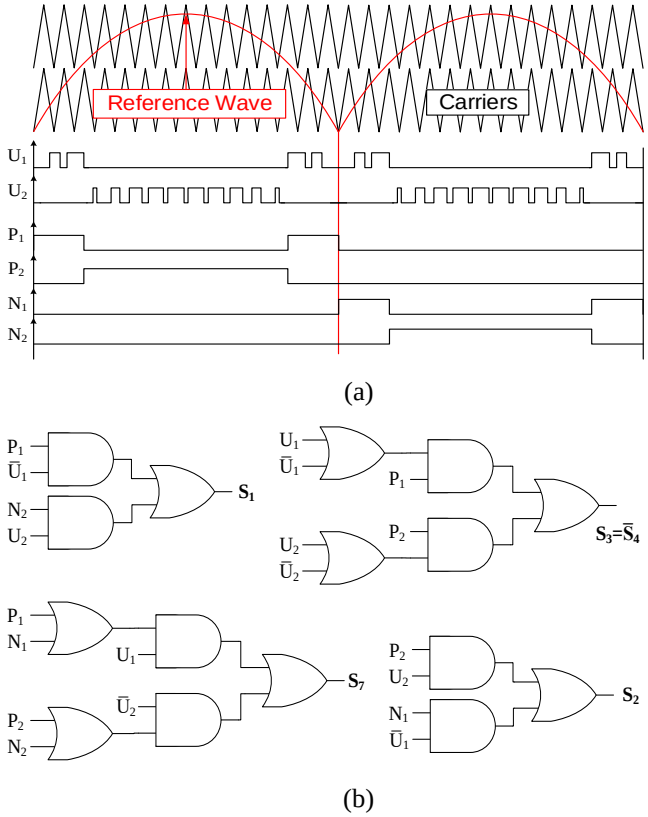


Figure 3. 2 Modulation scheme (a) Sinusoidal PWM with modified reference signal and corresponding switching pulses, (b) Boolean logics employed to generate pulses for the switches.

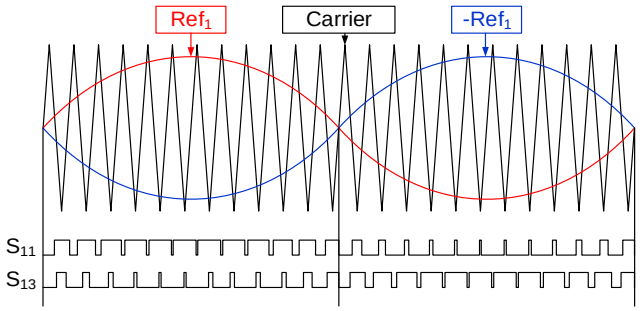


Figure 3. 3 Phase-shifted PWM technique and corresponding pulses

3.4 Proposed fault-tolerance strategy

The PT can still be operated with a switch fault, either an open-circuit (OC) or a short-circuit (SC) without requirement of any additional hardware, but by post-processing of the switching PWM signals. For post-fault operation with switch OC or SC in any of the inverter, the PT continues to operate with change in modulation technique from IPD-SPWM to PS-SPWM delivering balanced three-phase supply with three-levels in the output voltage. PS-

SPWM technique will yield lower harmonic distortion and near to sinusoidal average voltage compared to IPD technique in post fault operation. Hence the application of PS-SPWM technique is limited for post-fault operation of the PT.

3.4.1 For switch open-circuit faults

The PT employs minimum number of switching devices compared to other nine-level inverter feeding OEWIM drives and hence the redundant states for producing various voltage levels are very less. Hence fault in one of the switch will have a considerable impact on the number of levels in the output voltage. The OC fault in switch S_{x7} (where x ϵ 1, 2, 3) will reduce the levels in the output voltage from nine to five keeping the peak output voltage magnitude unaffected. For example, if an OC fault occurs in S_{17}, then the modulation technique is shifted to PS-SPWM and the switching pulses produced (as illustrated in Figure 3.3) are applied to switches S_{11} and S_{13}. The switches S_{12} and S_{14} are fed with complementary pulses of S_{11} and S_{13} respectively and the same is done for corresponding switches in the other inverters as well. But OC fault in the other switches in any inverter will result in reduction of voltage levels from nine to three and the peak output voltage is reduced to half. This will reduce the output power delivered but ensures the continuity in the supply for reliable operation of the OEWIM drive. The capacitors and bidirectional switches are not involved in post-fault operation i.e., the switching pulses for the switch S_{x7} are disengaged in the post-fault operation.

The fault-tolerance strategy (FTS) for the OC faults in the switches S_{11} or S_{12} is that the switching pulses of the faulty switch are to be fed to healthy switch in the same leg. For example, if the OC fault occurs in switch S_{11}, then the switching pulses of S_{11} and S_{12} are given to switch S_{12}. This will connect the switch S_{12} to negative rail of source throughout the operation. The same has to be done for the corresponding switches in the other inverters as well. If OC fault occurs in S_{11}, then the switching pulses to switch S_{21} are disengaged and added to the switching pulses of S_{22} and similarly, the switching pulses of S_{31} and S_{32} are given to S_{32}. This will create balanced switching of the inverters and hence produce balanced output voltages. For switches S_{13} and S_{15}, if OC faults occur in switch S_{13}, the switching pulses of the switches S_{13} and S_{14} are applied to S_{14} and also the switching pulses to switch S_{15} are disengaged and are added to the switching pulses of S_{16}. This has to be done for all the corresponding switches in all the inverters. The strategy remains same for the OC fault in any switch in the corresponding positions in other inverters as well.

3.4.2 For switch short-circuit faults

If a SC fault occurs in any of the switch, the source gets short-circuited when the other switch in the corresponding leg is turned-on. Hence, if a SC fault occurs in a switch, then immediately other switch in the corresponding leg has to be turned-off. The FTS for switch SC faults will be contradictory to the strategy for OC fault, i.e., instead of turning-off of the switches in similar positions of the other inverters, here switches are turned-on completely and the switches in similar positions of the healthy switches are turned-off completely.

For example, consider switches S_{13} and S_{14}, if S_{13} gets shorted, then S_{14} has to be turned-off and also the switches S_{24} and S_{34} are to be turned-off and switches S_{23} and S_{33} are to be turned-on completely. The same strategy is applicable for SC faults in switches S_{13}, S_{14}, S_{15}, S_{16} and switches in corresponding positions in other inverters. But if SC fault occurs in any of the switches (S_{x1}, S_{x2} and S_{x7}) that are in the neutral connection of the PT, then the strategy is to turn-off the other two switches completely. If SC fault occurs in the bidirectional switch S_{17}, then the switches S_{11} and S_{12} are to be turned-off completely. Similarly the switches S_{21}, S_{22}, S_{31} and S_{32} are to be turned-off and the switches S_{27} and S_{37} are turn-on throughout the operation.

3.5 Simulation results

To demonstrate the feasibility of the PT and the control scheme, the models are developed and simulated in MATLAB/Simulink environment. The parameters considered for the simulation are source voltage V=130 volts, capacitance, C_x=1000μF (where x ϵ 1, 2, 3) and frequency of carriers is taken as 1500Hz. The capacitance required is evaluated using fundamental relation I_c=C ($\Delta V * f_{sw}$), where I_c is the peak current, ΔV is the permissible peak to peak voltage ripple and f_{sw} is the switching frequency.

The simulations results of three-phase output voltage and currents are presented in Figure 3.4(a) and Figure 3.4(b) respectively. The capacitors are charged to half the source voltage and hence ensures equal magnitude of voltage levels in the output. The voltage across the capacitors in all the three inverters are presented in Figure3.4(c). The PT can deliver output voltage with reduced modulation index as well. The output voltages with changes in modulation index (M_a) are presented in Figure 3.4(d). The fast Fourier transform (FFT) analysis for the total harmonic distortion (THD) in the phase voltage and current are presented in Figure 3.4(e) and Figure 3.4(f) respectively.

The performance of the PT with switch faults are analysed by disengaging switching pulses for the corresponding switch to realize the OC fault. The effect on the three phase output voltage and currents due switch S_{11} OC are presented in the Figure 3.5(a). The windings of phase-A and phase-C that are connected to the inverter-1 will be effected due to OC in switch S_{11}. The positive peak of phase-C voltage and negative peak of Phase-A voltage are reduced and hence the currents in these two phases are decreased and distorted. The effect of OC in switch S_{13} on inverter performance is presented in Figure 3.5(b).

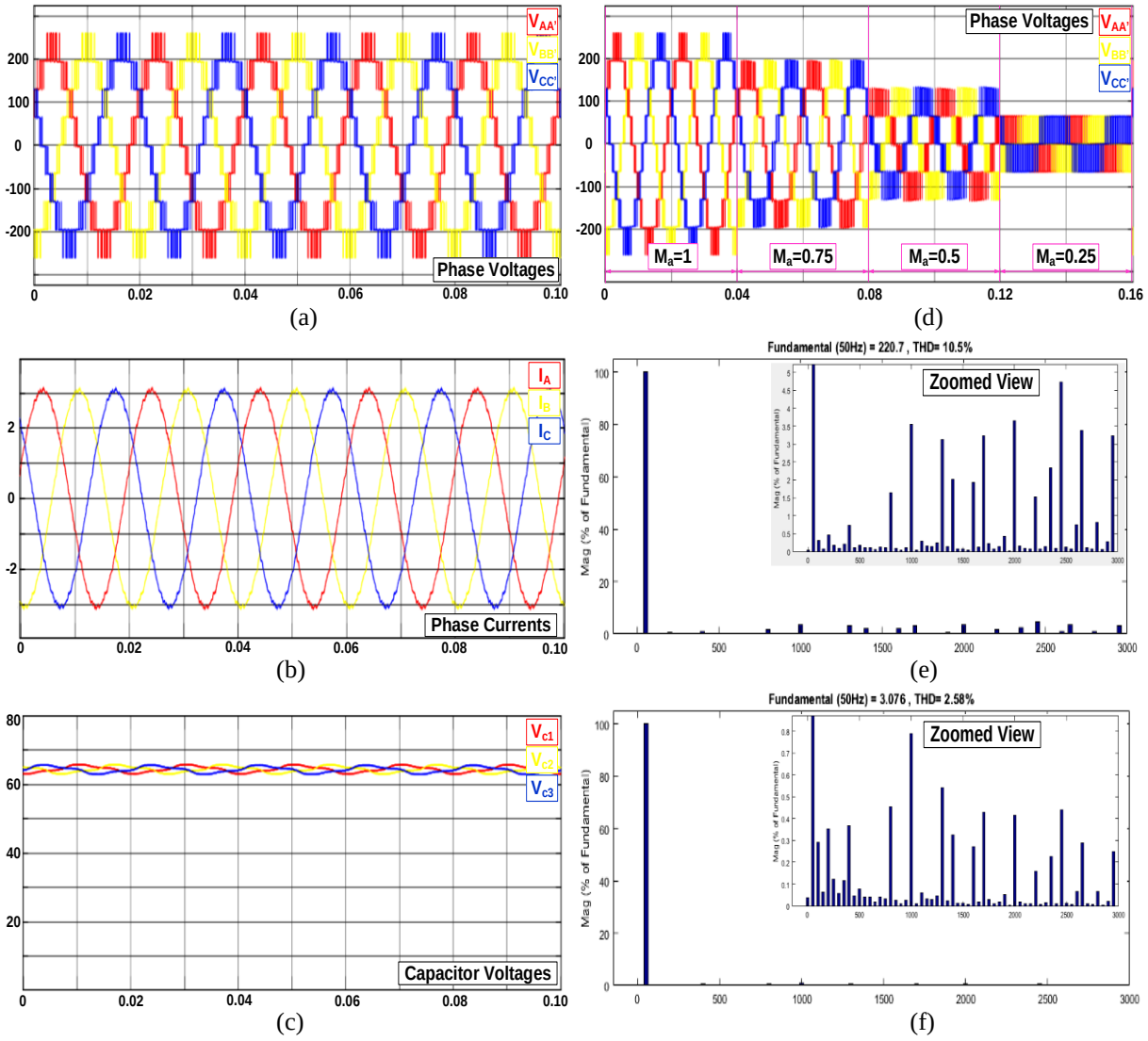
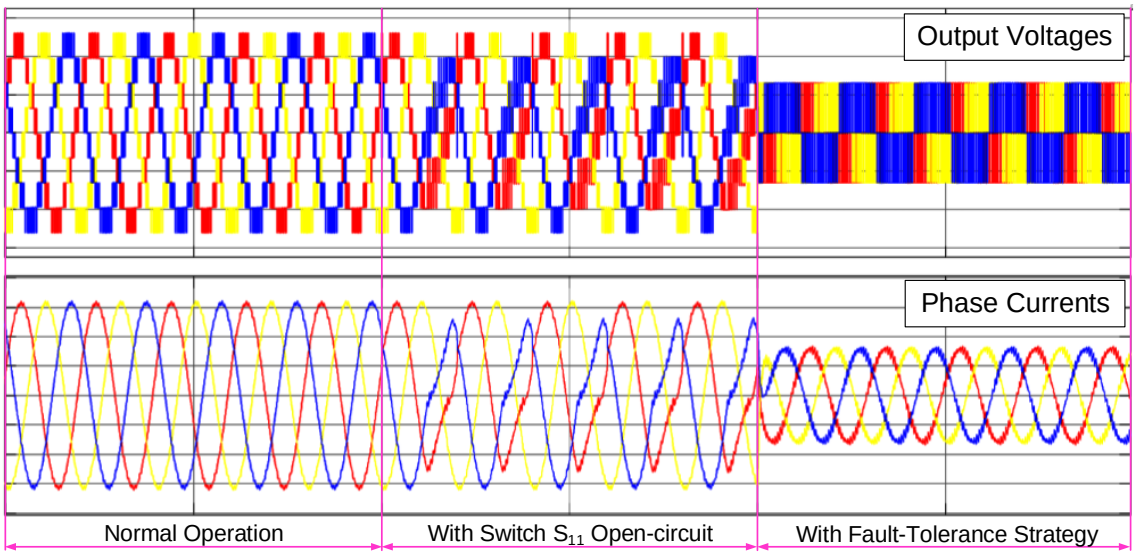


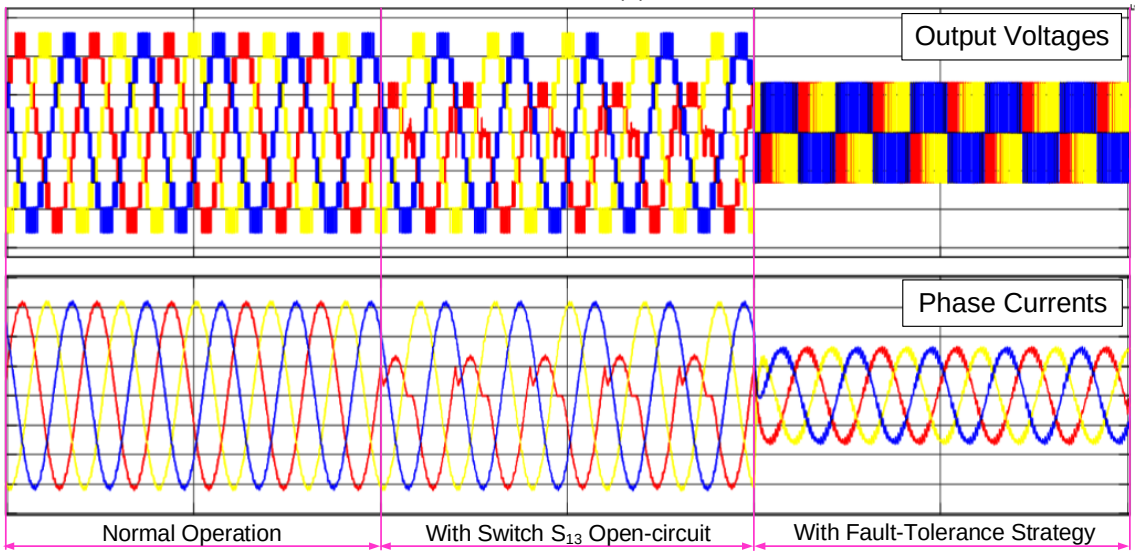
Figure 3. 4 Simulation results of (a) three-phase output voltages, (b) three-phase currents at no-load (c) voltage across capacitors C1, C2 and C3, (d) three-phase voltages with variation in modulation index, (e) FFT analysis for THD in output voltage (f) FFT analysis for THD in phase current.

Since the switches S_{13}, S_{14}, S_{15} and S_{16} are connected to phase windings and hence OC in these switches will clamp the currents in respective phases to which they are connected. The positive wave of voltage is reduced and current is clamped in phase-A winding due to OC in

switch S_{13}. Similarly, an OC fault in switch S_{15} will reduce the voltage peak and clamp the current in negative cycle for phase-C. The peak magnitude of output voltage remains same but the number of levels decreases with OC fault in bidirectional switch S_{17} as illustrated in Figure 3.5(c). The output voltages and currents with OC in switches S_{12} and S_{14} will be the vertical flip of the waveforms presented for switch S_{11} and S_{13} OC conditions. The PT is tolerant for switch SC faults as well and the output results with FTS for switch SC faults will be same as the results presented for the complementary operating switches. For example, the outputs yielded with FTS for switch S_{11} OC will same as the results obtained with FTS for the switch S_{12} SC conditions. Hence the results with FTS for switch S_{17} SC fault condition are alone presented in Figure 3.5(d).



(a)



(b)

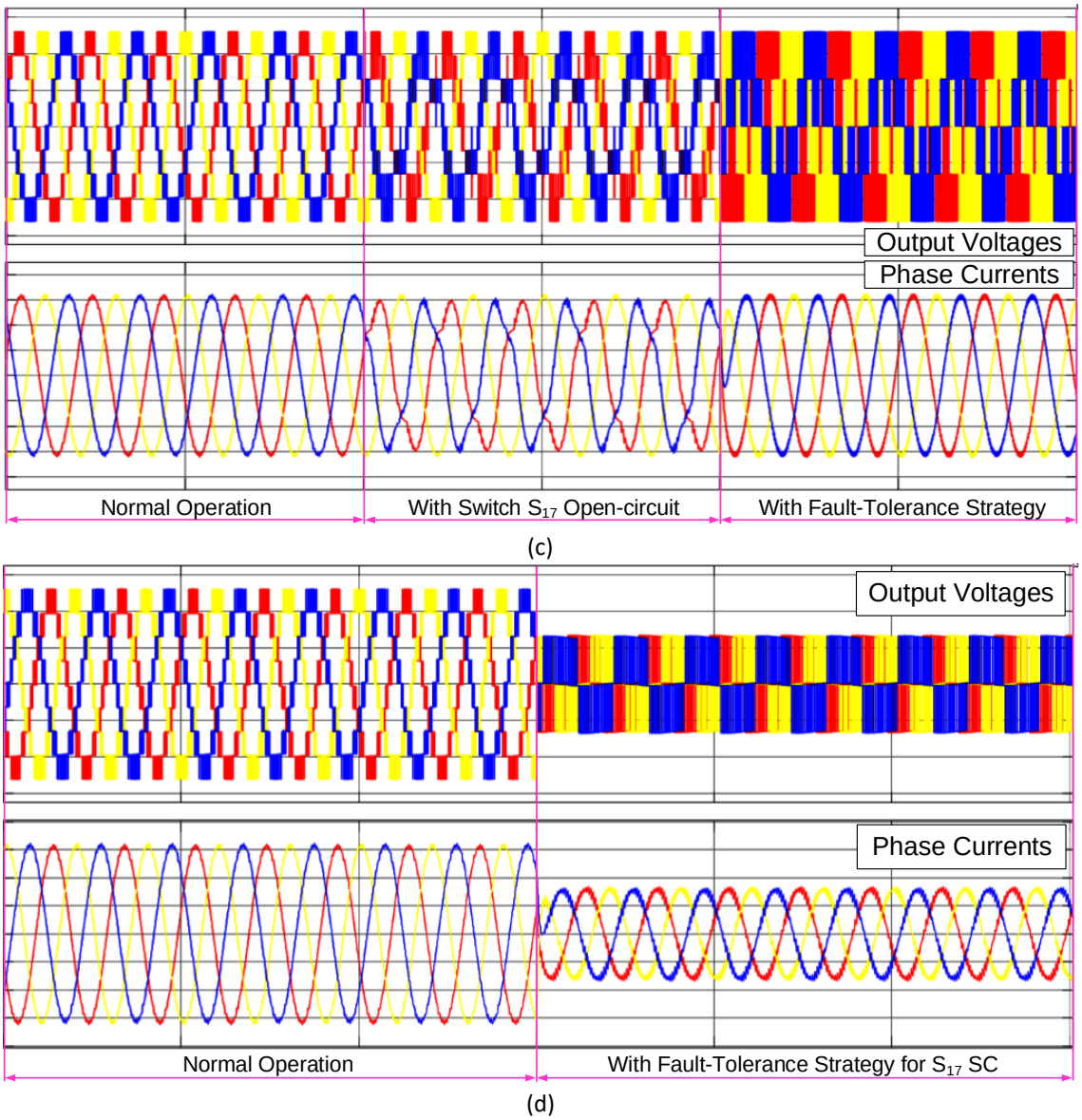


Figure 3. 5 Simulation results of three-phase output voltage and currents during normal, fault and with FTS (a) for OC in switch S_{11}, (b) for OC in switch S_{13}, (c) for OC in switch S_{17} OC, (d) for SC in switch S_{17}.

The performance of the induction motor with the change in load torque is presented in Figure 3.6. The effect of load torque variation on the three-phase currents are presented in Figure 3.6(a) and the variation of load torque is presented in Figure 3.6(b). The changes in motor speed and voltage across the capacitors in all three inverters due to variation in load torque are presented in Figure3.6(c) and Figure 3.6(d).

3.6 Comparison of the proposed topology

An assessment of the PT in terms of various parameters such as the levels in the output voltage (N_L), required number of switches (N_{sw}), DC sources (N_s), gate drivers (N_d), diodes (N_D), capacitors (N_{cap}), total component count and control complexity is done and is illustrated in Table

3.2. As can be seen from Table 3.2, it is clear that the component count for the PT are minimum and control complexity is low in comparison with conventional topologies such as neutral-point clamped (NPC), flying-capacitor (FC), cascaded H-bridge (CHB) inverters and with other existing nine-level topologies in literature feeding OEWIM drives.

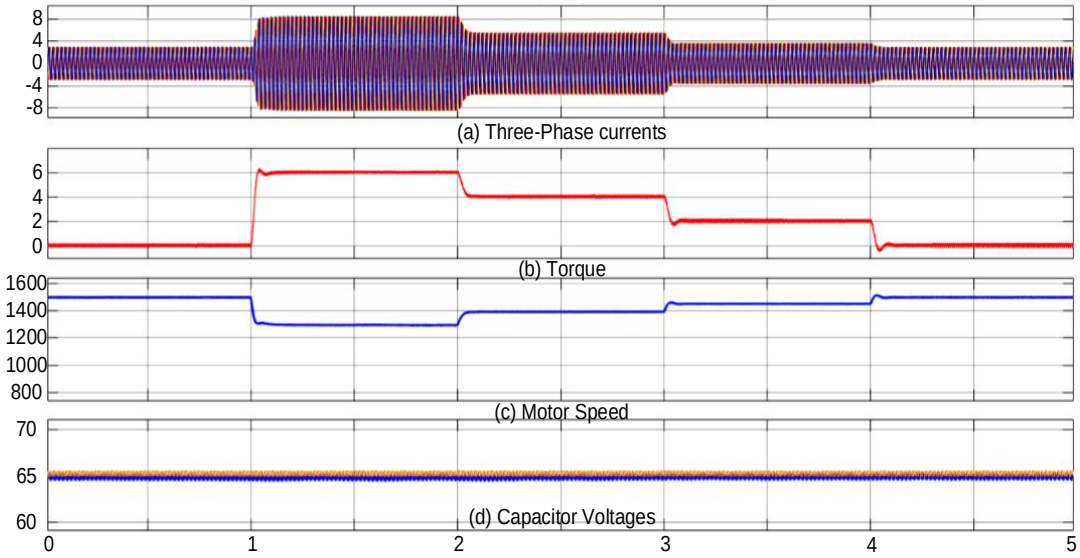


Figure 3. 6 Simulation results for change in load torque (a) three-phase currents, (b) motor torque, (c) motor speed, (d) voltage across the capacitors.

Table 3.2 Comparison of the proposed topology with existing topologies feeding OEWIM drives

MLI Type	**N_L**	**N_{sw}**	**N_d**	**N_D**	**N_s**	**N_{cap}**	**Component Count**	**Control complexity**
NPC	9	48	48	168	1	9	274	Very high
FC	9	48	48	48	1	85	230	High
CHB	9	48	48	48	12	12	168	Low
K. Wang *et al.*,2017	9	36	36	36	1	8	126	High
P. P. Rjeevan *et al.*,2013	9	36	36	36	2	12	122	High
G. Mondal *et al.*,2009	7	48	48	60	6	6	168	Very high
MHBT	9	24	24	24	3	6	81	Low
PT (MLBBT)	9	24	24	24	3	3	78	Low

The Proposed MLBBT exhibit advantages such as peak output voltage twice the source voltage and acceptance of conventional SPWM techniques for generating switching pulses but also suffers from shortcomings such as requirement of three isolated sources and non-modular construction. But the PT can find application in battery electric vehicles (BEVs) designed with more number of batteries known as split battery technique for extending the drive range. However, the results presented prove that the PT can be operated even with switch OC or SC

fault conditions without need of any additional hardware and hence can be employed for drives applications for reliable operation.

3.7 Summary

A nine-level inverter topology with fault-tolerance capability for switch faults designed with minimum number of switching devices is presented in this chapter. The output voltage may be reduced during switch-fault conditions but safeguards continuousness in supply for reliable operation without the necessity of extra hardware. Sinusoidal modulation techniques which does not over burden digital processors for generating switching pulses are employed for the PT. The performance of induction motor with possible faults in switches and variation in load torque are observed and the results are presented. The PT finds applications in renewable energy generation systems such as solar cell or fuel cells fed electric drive applications where multiple sources with lower voltage ratings are employed.

Chapter 4

Fault tolerant multilevel inverter topologies for open-end winding induction motor drive

Chapter 4

Fault tolerant multilevel inverter topologies for open-end winding induction motor drive

4.1 Introduction

Recent days, multilevel voltage-source inverters have been receiving greater acceptance from industry in the range of medium and high power induction-motor (IM) drive applications. Owing to the advantages of multilevel inverters (MLIs), such as, in particular, their operation with higher dc link voltages using lower rating semiconductor switching devices and producing output voltage with superior harmonic profile marks their importance in industrial applications. Conventional topologies such as (a) neutral point clamped (NPC) inverter, (b) flying-capacitor (FC) inverter and (c) cascaded H-bridge (CHB) inverter belong to early era of MLIs and are employed in applications with lower levels of output voltage. These topologies have their own advantages and disadvantages based on their control and operation. NPC and FC topologies will have capacitor voltage balancing issues and requires complex control techniques when designed for higher levels in the output. CHB topology can be designed for any level of output voltage but requires increased number of isolated sources. Though these topologies can be configured for increased number of levels in the output, the power and control circuit complexity increases as the number of switching devices required are high. Hence this provides the scope of research for developing MLI topologies with reduced complexity in power and control circuits. Recent years have witnessed vast research in areas of MLI topologies and many of such topologies that are present in literature are the blend of conventional topologies. Several topologies were proposed to satisfy the desires of industry such as reduced device count and fault-tolerance.

Certain MLI topologies are designed based on the application, such as, the topologies for open end winding induction motor (OEWIM) drive in which the load terminals will be six for a three phase system. The three phase stator winding terminals of IM are brought out and are fed from both ends to achieve multilevel output voltage across the phase windings. MLIs with high number of levels in the output voltage is desired in drive applications as the increase in the number of levels decreases harmonic distortions and hinders the need for expensive and bulky filters. However, the increase in the levels in the output voltage is obtained at a cost of increased number of components, hence the industry is reluctant for higher number of levels as

it makes the system bulky, less reliable and complex. Therefore, there is a necessity to attain an increased number of levels in the inverter output voltage without an enormous rise in the number of components and reliability of the system is also important. The power circuit complexity can be reduced with lower switching devices and hence control complexity can be reduced proportionally. As the component count of MLIs increase, the reliability of the system decreases. Failure of any one switch may lead to a complete shutdown of the system. Hence, fault tolerant reduced device topologies find importance in the MLI family.

Hence, this chapter presents two nine-level inverter topologies for OEWIM drive with fault tolerance capability to switch fault conditions. The proposed topologies are designed with minimum number of switching devices. The two nine-level inverter topologies proposed are envisioned for an induction motor with open-end stator winding construction. In this topologies, the six terminals of the three-phase windings of the induction motor are fed from three three-phase voltage source inverters along with the flying-capacitors (FC). The modulation techniques employed can effectively charge and discharge the capacitors to realize middle voltage levels throughout its modulation range. The proposed topologies employ a reduced number of switches and lower voltage rating isolated dc sources than conventional topologies.

4.2 Description of the proposed topologies

The proposed topologies are designed to feed an open-end winding induction motor (OEWIM) with lower-rated voltage sources. Three inverters are configured to feed the three-phase induction motor stator windings from both the ends to yield nine-levels in the output voltage across each phase. This configuration produces increased voltage levels with reduced devices and the output voltage peak will be twice the magnitude of input source voltage. This allows to employ lower voltage renewable energy sources as input elements. The scheme of connection employed exhibit inherent fault tolerance for certain switch faults as well. The scheme of connection employed for the proposed topologies is illustrated in Figure 4.1. Figure 4.1(a) presents a FC leg based topology (FCLBT) and Figure 4.1(b) presents a Switched-Capacitor based topology (SCBT). The FCLBT is designed with three inverters in which each inverter consists of a FC leg and a conventional H-bridge and are connected across an isolated DC source. SCBT is designed with three three-phase inverters and each of these inverters are fed from an isolated DC source and also are provided with a capacitor with two series-connected switches across it. In the proposed topologies, switches S_{1A} through S_{8A} constitute inverter-A.

Similarly, switches S_{1B} through S_{8B} constitute inverter-B and switches S_{1C} through S_{8C} constitute inverter-C.

In FCLBT, the circuit configuration for inverter-A is done in the following manner: the series connection of switches S_{1A}, S_{2A}, S_{3A} and S_{4A} constitute a leg of the inverter and a capacitor is connected across the switches S_{2A} and S_{3A}. The mid-point of switches S_{2A} and S_{3A} is taken as output terminal-1 of inverter-A. Similarly, the mid-point of switches S_{5A} and S_{6A} is considered as output terminal-2 and mid-point of switches S_{7A} and S_{8A} is considered as output terminal-3. In SCBT, the switches S_{1a} and switch S_{2a} constitute a leg of the inverter and to the point between these two switches the negative terminal of the capacitor is connected. The switches S_{7a} and S_{8a} constitute a leg and are connected across the capacitor. The mid-point of switches S_{7a} and S_{8a} is taken as output terminal-1 of inverter-a. Similarly, the mid-point of switches S_{3a} and S_{4a} is considered as output terminal-2 and mid-point of switches S_{5a} and S_{6a} is considered as output terminal-3. Hence, in both the proposed topologies, each inverter has three output terminals and output terminal-1 of all the three inverters are shorted to form a neutral connection. The phase-A winding of OEWIM is connected between output terminal-2 of inverter-a and output terminal-3 of the inverter-b. Similarly, the phase-B and phase-C windings are connected in the same configuration. The scheme of connection and the components required for both the topologies are same.

The proposed topologies are proficient of generating output voltage across any phase winding with nine levels, namely $\pm$2V, $\pm$3V/2, $\pm$V, $\pm$V/2, 0. The possible switching states to generate nine level output voltage across the terminals of phase winding A-A' of OEWIM are presented in Table 4.1 for FCLBT and in Table 4.2 for SCBT. However, the reduction in number of switching devices has a divergent influence on the number of overall redundant switching states as evident from Table 4.1 and Table 4.2. However, an observation of switching tables depict the information that the charging and discharging times of FC in both the proposed topologies are equivalent over one complete cycle of output voltage.

Considering the output voltage and also current have half-wave symmetry, the average current (Average[i_c]) that flow through the capacitor during output voltage levels $\pm$3V/2 and $\pm$V/2 with the load impedance of Z can be given as:

$$\text{Average}[i_c^+]_{V/2} = \frac{V - v_c}{Z}; \qquad (4.1)$$

$$\text{Average}[i_c^-]_{3V/2} = \frac{V + v_c}{Z}; \qquad (4.2)$$

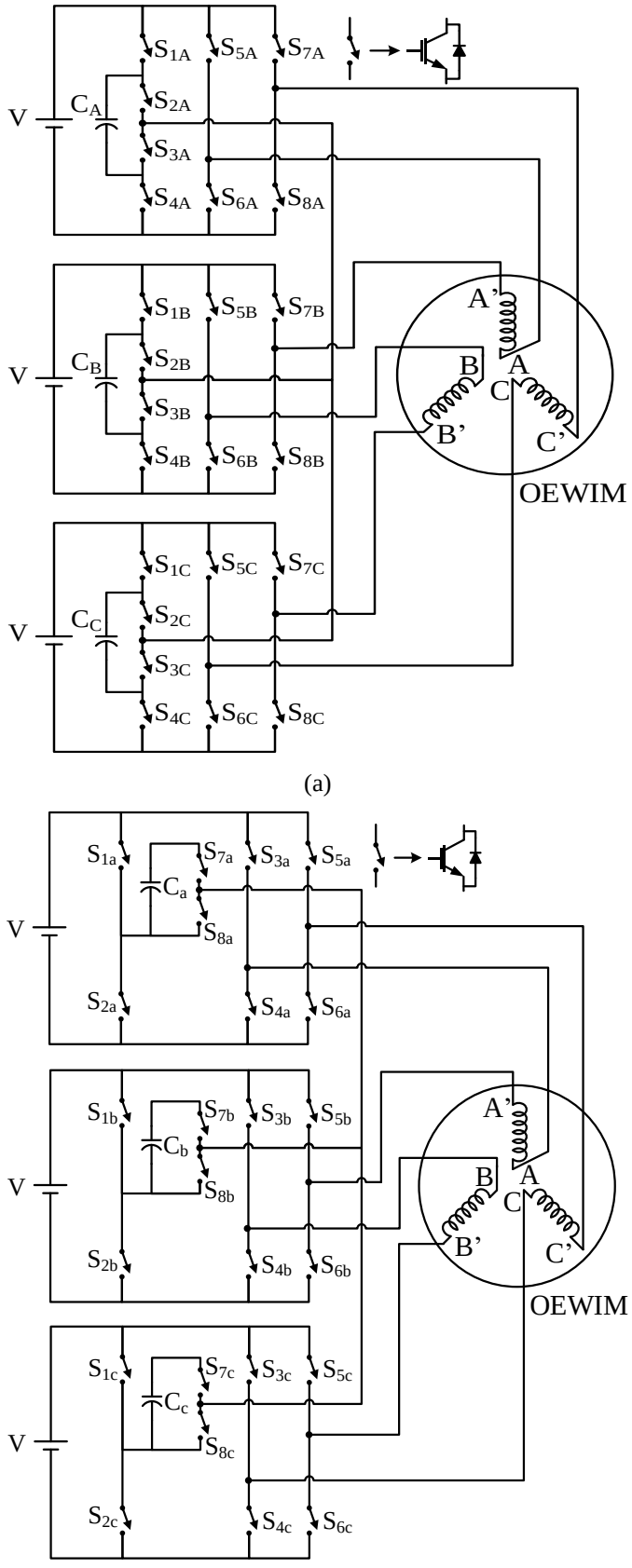


Figure 4. 1 Proposed topologies (a) Flying-Capacitor Leg Based Topology (FCLBT) (b) Switched Capacitor Based Topology (SCBT).

Table 4.1 Possible switching states to generate different voltage levels for FCLBT

Voltage level	Inverter-A			Inverter-B			Capacitor State
	S_{1A}	S_{2A}	S_{5A}	S_{1B}	S_{2B}	S_{7B}	
2V	0	0	1	1	1	0	No change
3V/2	0	0	1	1	0	0	C_B-Charging
	0	1	1	1	1	0	C_A-Charging
V	0	0	1	0/1	0/1	0/1	No change
	0/1	0/1	0/1	1	1	0	
V/2	0	0	1	1	0	1	C_B-Charging
	0	1	0	1	1	0	C_A-Charging
0	1	1	1	0/1	0/1	0/1	No change
	0	0	0	1/0	1/0	1/0	
-V/2	0	1	0	0/1	0/1	0/1	C_A-Discharging
	0/1	0/1	0/1	1	0	1	C_B-Discharging
-V	1	1	0	0/1	0/1	0/1	No change
	0/1	0/1	0/1	0	0	1	
-3V/2	1	1	0	1	0	1	C_B-Discharging
	0	1	0	0	0	1	C_A-Discharging
-2V	1	1	0	0	0	1	No change

Table 4.2 Possible switching states to generate different voltage levels for SCBT

Voltage	Inverter-a			Inverter-b			Capacitor
level	S_{1a}	S_{3a}	S_{7a}	S_{1b}	S_{5b}	S_{7b}	State
2V	0	1	0	1	0	0	No change
3V/2	0	1	1	1	0	0	C_a – Charging
	0	1	0	0	0	1	C_b – Discharging
V	0	1	0	0/1	0/1	0	No change
	0/1	0/1	0	1	0	0	
V/2	0	1	1	1	1	0	C_a – Charging
	0	0	0	0	0	1	C_b – Discharging
0	0	0	0	0/1	0/1	0	No change
	1	1	0	0/1	0/1	0	
-V/2	0	1	1	0	0	1	C_a - Discharging
	0	0	1	0	0	0	C_b – Charging
-V	1	0	0	1/0	1/0	0	No change
	0/1	0/1	0	0	1	0	
-3V/2	0	0	1	0	1	0	C_a – Discharging
	1	0	0	0	1	1	C_b – Charging
-2V	1	0	0	0	1	0	No change

$$\text{Average}[i_c^+]_{3V/2} = \frac{2V - v_c}{Z}; \qquad (4.3)$$

$$\text{Average}[i_c^-]_{V/2} = \frac{v_c}{Z} \qquad (4.4)$$

Therefore, the net charge (Q) absorbed/supplied for a time period (T) can be expressed as

$$Q = \left\{\text{Average}[i_c^+]_{V/2} + \text{Average}[i_c^+]_{3V/2} - \text{Average}[i_c^-]_{V/2} - \text{Average}[i_c^-]_{3V/2}\right\} * T$$

$$= \left\{\frac{2V-4v_c}{Z}\right\} \quad (4.5)$$

Owing to the symmetric property of the output current in steady-state, the average charge Q over a complete cycle is zero, substituting charge (Q) as zero in equation (4.5) will result in a relation of V_c=0.5V.The voltage across the FC is maintained as 0.5V where V is the voltage rating of each source in the proposed topologies. This self-balancing property of maintaining voltage 0.5V across the FC is achieved without any additional circuitry or closed loop control that expedites lowered overall inverter design cost.

The voltage at the output terminals are reliant on the switching states of the power switches. Considering the switches as ideal, let the binary variables 0 and 1 represent their blocking and conduction states, respectively. In other words

i.e., if S_{vu} = 0 then S_{wu} = 1, switch S_{vu} is OFF and switch S_{wu} is ON

ifS_{wu} = 0, then S_{vu} = 1; switch S_{wu} is OFF and switch S_{vu} is ON

-Where u ε A, B, C &v ε 1, 2, 5, 7 &w ε 4, 3, 6, 8 for FCLBT

-Where u ε a, b, c &v ε 1, 3, 5, 7 &w ε 2, 4, 6, 8 for SCBT

With this depiction and considering $\hat{S}_{1A} = S_{4A}$, $\hat{S}_{2A} = S_{3A}$, $\hat{S}_{5A} = S_{6A,}$ $S_{5A} = S_{7A}$ and $\hat{S}_{7A} = S_{8A,}$ for FCLBT and similarly $\hat{S}_{1a} = S_{a2}$, $\hat{S}_{3a} = S_{4a}$, $\hat{S}_{5a} = S_{6a}$, $S_{3a} = S_{5a}$, $S_{4a}=S_{6a}$ and $\hat{S}_{7a}=S_{8a}$ for SCBT, the output voltage across the terminals of OEWIM for the proposed topologies can be written as

For FCLBT

$$V_{AA'} = V\begin{bmatrix} S_{5A}\left(\hat{S}_{1A}\hat{S}_{2A} + 0.5\hat{S}_{1A}S_{2A}\right) + \hat{S}_{7B}\left(S_{1B}S_{2B} + 0.5\hat{S}_{1B}S_{2B}\right) \\ -\hat{S}_{5A}\left(S_{1A}S_{2A} + 0.5\hat{S}_{1A}S_{2A}\right) - S_{7B}\left(\hat{S}_{1B}\hat{S}_{2B} + 0.5\hat{S}_{1B}S_{2B}\right) \end{bmatrix} \quad (4.6)$$

For SCBT

$$V_{AA'} = V\begin{bmatrix} S_{3a}\left(\hat{S}_{1a}\hat{S}_{7a} + 0.5\hat{S}_{1a}S_{7a}\right) + \hat{S}_{5b}\left(S_{1b}\hat{S}_{7b} + 0.5\hat{S}_{1b}S_{7b}\right) \\ -\hat{S}_{3a}\left(S_{1a}\hat{S}_{7a} + 0.5\hat{S}_{1a}S_{7a}\right) - S_{5b}\left(\hat{S}_{1b}\hat{S}_{7b} + 0.5\hat{S}_{1b}S_{7b}\right) \end{bmatrix} \quad (4.7)$$

The proposed topologies are capable of providing balanced three phase output voltage even under switch fault conditions. This makes the proposed topologies reliable when used for low-voltage medium-power applications such as feeding motors in an electrical vehicle. For operation of the proposed topologies during switch fault conditions does not require any additional hardware, but requires modification of switching pulses. To obtain balanced output voltage across all the phases, the switching of the inverters should also be identical. Hence when switch fault occurs in any of the switches, some of the healthy switches are also turned-off in post-fault operation to ensure symmetrical switching of the inverters. Under normal operation of the proposed topologies, nine level voltage is fed to the windings of the OEWIM drive

whereas with switch fault, the levels in the output voltage reduces to five and the power delivered will also be reduced to half for most of the switch faults. The output power supplied might be reduced during switch fault conditions but it ensures continuity in operation of the OEWIM drive.

4.3 Modulation scheme

The gate pulses for the switches in the proposed topologies are produced by the conventional sinusoidal pulse width modulation (SPWM) technique. A fundamental frequency sinusoidal reference signal, V_{Ref} is compared with the high frequency level shifted triangular carrier signals to generate the gate pulses. In general, the magnitude of the sinusoidal reference signal is taken as unity that represents the modulation index, Ma=1, where the magnitude of level shifted carriers is half the reference voltage magnitude. For such a modulation scheme the number of level shifted carriers required for an N-level inverter will be (N-1). To reduce the number of carrier signals required, the reference wave can be modified in such a way that the negative cycle is flipped as positive cycle which reduces the number of carrier waves required. The reference wave can be further modified as shown in Figure 4.2(a), in such a way that the number of carriers required is only one. This reduces the computational burden on the controllers while implementing on digital platforms like dSPACE and digital signal processors (DSP). The gate pulses for the proposed topologies are generated using dSPACE 1104.

The connection of phase windings is done such that two ends of each winding is fed from two different inverters. For example, considering SCBT, the phase winding terminal-A is connected to inverter-a and winding terminal-A' is connected to inverter-b. Similarly, phase winding terminals B-B' are also connected between two different inverters. Three inverters are operated by gate pulses generated by SPWM technique. The reference waves used for three inverters are displaced by 120^o. Therefore, each terminal of every phase winding is operating with a phase difference of 120^o with respect to its other terminal. This scheme of connection permits the phase winding to experience the output voltage with nine levels with maximum output voltage as twice the source voltage. The modified reference PWM used to produce gate pulses for the proposed topologies is illustrated in Figure 4.2(a). Figure 4. 2(b) illustrates the logic of generating nine levels in the output voltage with two reference waveforms displaced by 120^0. The switching logics employed for FCLBT and SCBT are presented in Figure 4.2(c) and Figure 4.2(d) respectively.

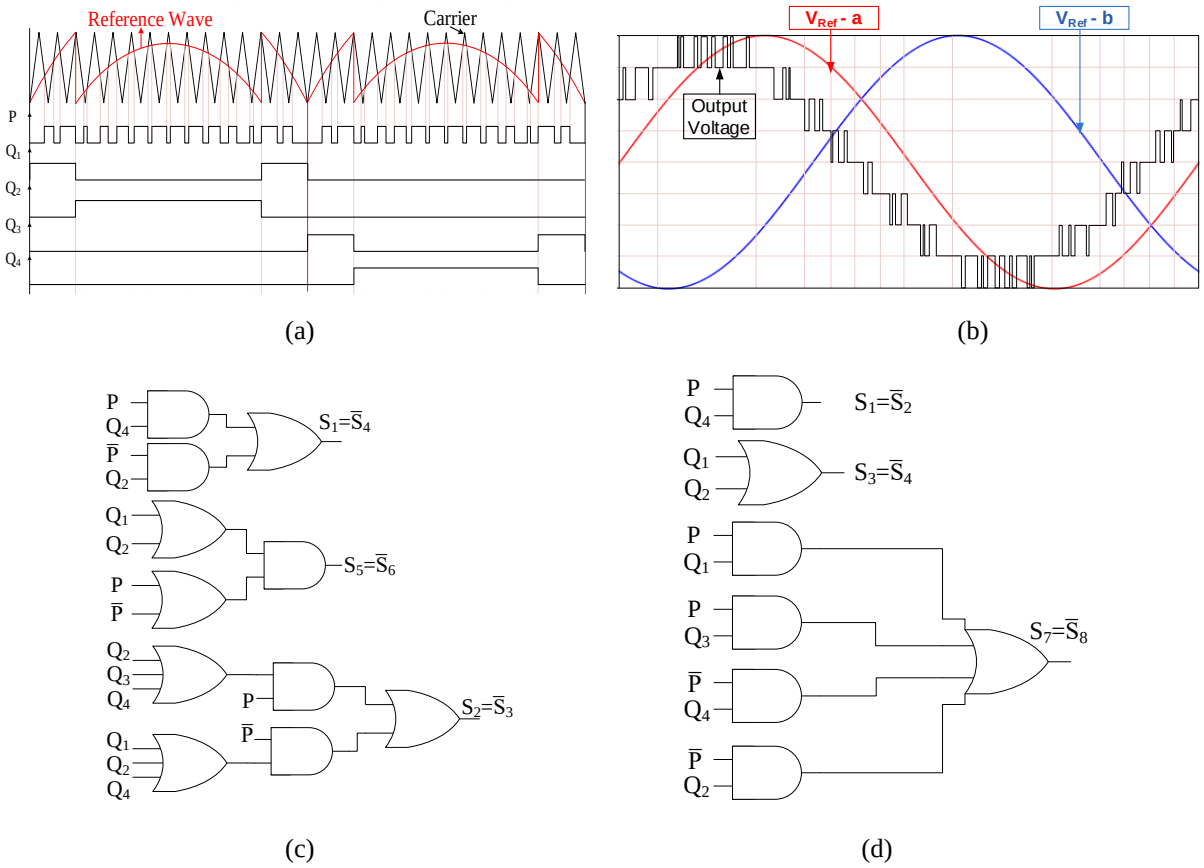


Figure 4. 2 Modulation scheme employed to generate gate pulses for the proposed topologies (a) modified-reference wave with a single carrier wave to generate gate pulses (b) representation of nine-level generation with two reference signals $V_{Ref\text{-}a}$ and V_{Refb} displaced by 120^0(c) switching logics for switches in FCLBT (d) switching logics for switches in SCBT.

4.4 Determination of capacitance

The proposed topologies are designed based on FC. So it is important to determine the value of capacitance of such a capacitor which depends upon the peak value of load current, ripple voltage and discharging period. Capacitors designed for lower ripple will yield lower power loss and work with higher efficiency.

The value of capacitance of the capacitor can be determined as

$$I_p = C\frac{dv}{dt} = C\frac{\Delta V}{\Delta T}$$

$$C = I_p\frac{\Delta T}{\Delta V} = \frac{I_p}{\Delta V * f_{sw}} \qquad (4.8)$$

Where C is the minimum capacitance of capacitance required, I_p is the maximum value of load phase current, ΔT is the inverter switching time period (T_s), and ΔV is the maximum permissible peak-to-peak voltage ripple in the FC. For a switching frequency of 1.5 kHz, if the

capacitor peak-to-peak ripple voltage has to be limited to 4 V, capacitance required is 666 μF. To be on the safe side, the capacitance for the experimental prototype is taken as 1000μF.

4.5 Operation of the proposed topologies

To demonstrate the viability of the proposed topologies and the control scheme, the models are developed and simulated in the MATLAB/Simulink environment. The simulation results of three-phase output voltage and currents, total harmonic distortion (THD) of the phase voltage and current, FC voltages during normal operating conditions of FCLBT and SCBT are presented in Figure 4.3 and Figure 4.4 respectively. The parameters considered for the simulation and experimentation are presented in Table 4.4.

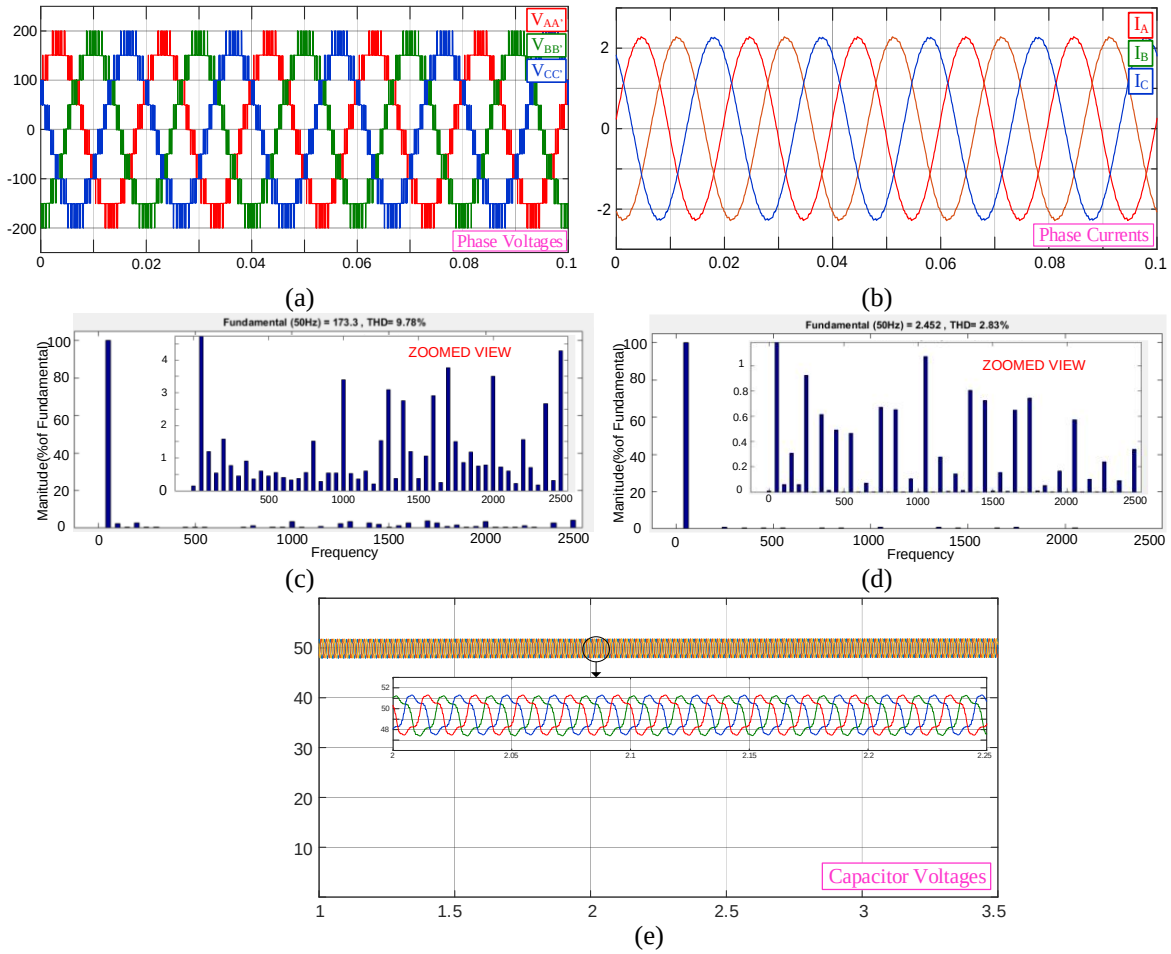


Figure 4. 3 Simulation results of FCLBT (a) Three phase output voltages $V_{AA'}$, $V_{BB'}$ and $V_{CC'}$ (b) Three phase currents I_A, I_B and I_C (c) THD for phase voltage (d) THD of phase current and (e) Voltages across the capacitor in each inverter.

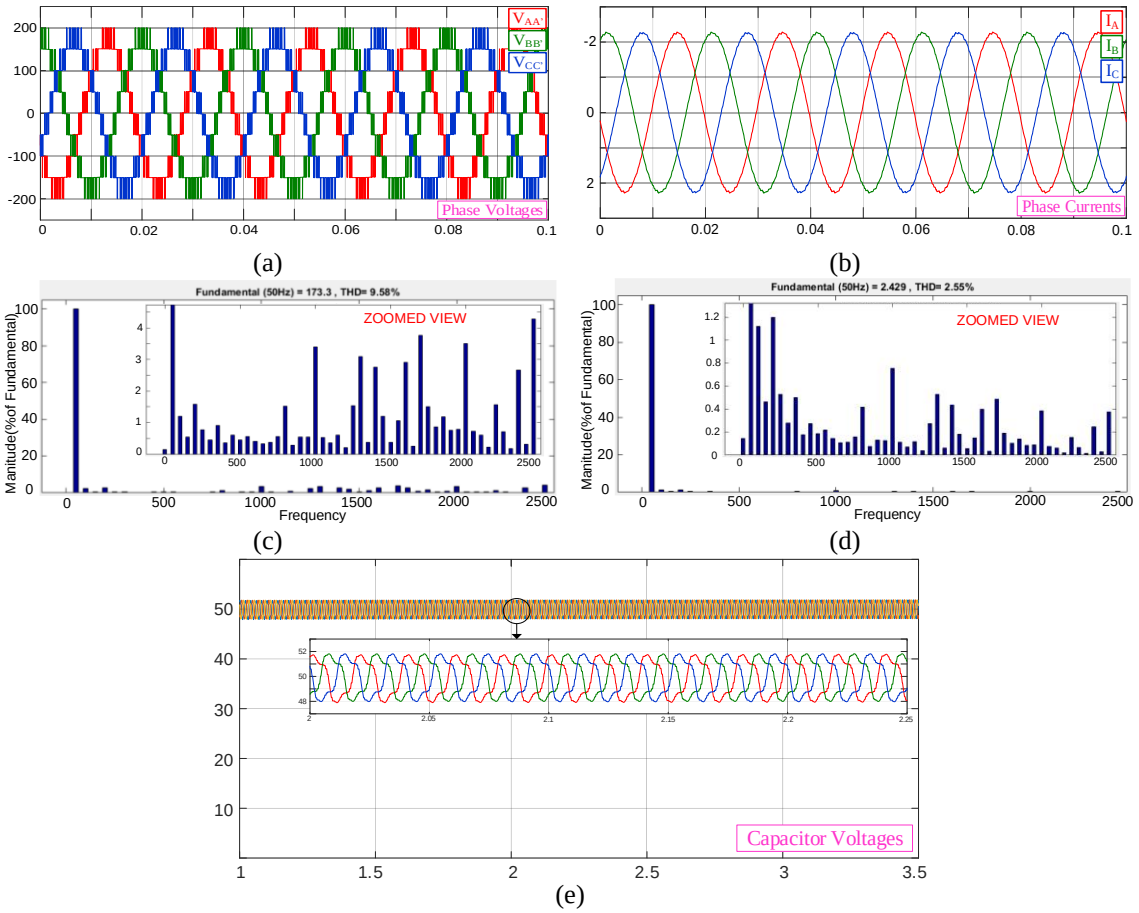


Figure 4. 4 Simulation results of SCBT (a) Three phase output voltages $V_{AA'}$, $V_{BB'}$ and $V_{CC'}$ (b) Three phase currents I_A, I_B and I_C (c) THD for phase voltage(d) THD of phase current and (e) Voltages across the capacitor in each inverter.

4.5.1 Inverter operation during switch faults

The proposed topologies employ three-phase inverters and the total number of switches employed are twenty four for each topology. Each winding is associated with six switches at least to deliver the output power. The switches in the inverters can be faulted either with an open-circuit (OC) or with a short circuit (SC). The proposed topologies can still be operated under such switch fault conditions with rated or reduced output power depending upon the switch under fault and the type of fault (SC or OC). Simulation results for various switch OC faults in proposed topologies are presented in Figure 4.5 and Figure 4.6. From the results presented in Figure 4.5 and Figure 4.6, it is evident that both the topologies behave identical during switch faults (introduced at time 0.04 seconds) as well depending upon the switch position in their respective topologies. The switches S_{2A} and S_{3A} in FCLBT are identical to switches S_{7a} and S_{8a} in SCBT and are meant for charging and discharging of the FC. And switches S_{1A} and S_{4A} in FCLBT are identical to switches S_{1a} and S_{2a} in SCBT and are meant for

neutral connection. Hence OC fault in such switches will yield similar output voltages and currents and hence experimental validation can be done with any of the topologies.

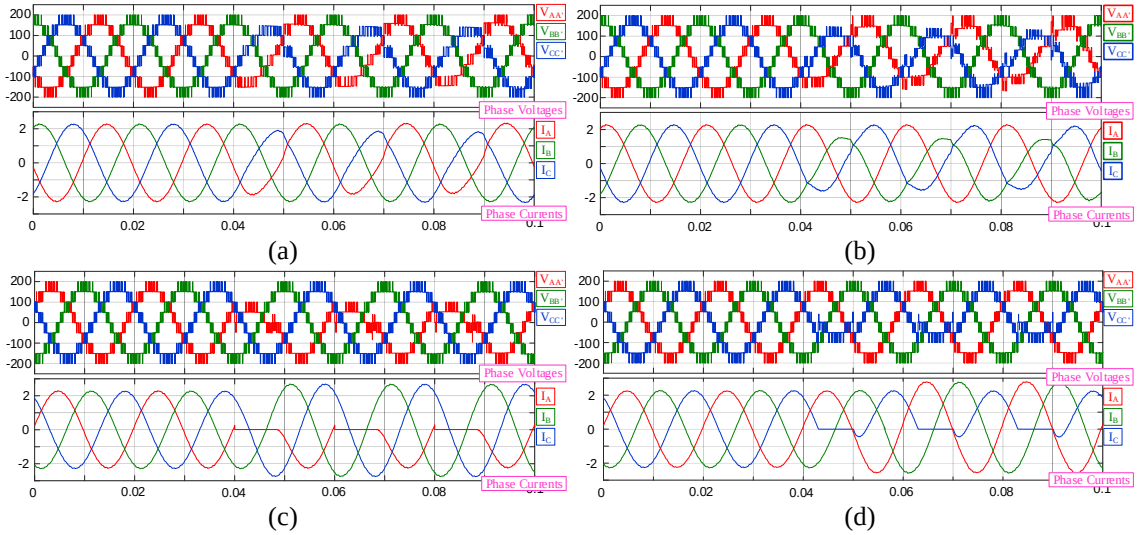


Figure 4. 5 Simulation results of three-phase voltages and currents of FCLBT with open-circuit fault in switch(a) S_{1A}(b) S_{2A}(c) S_{5A} (d) S_{7A}

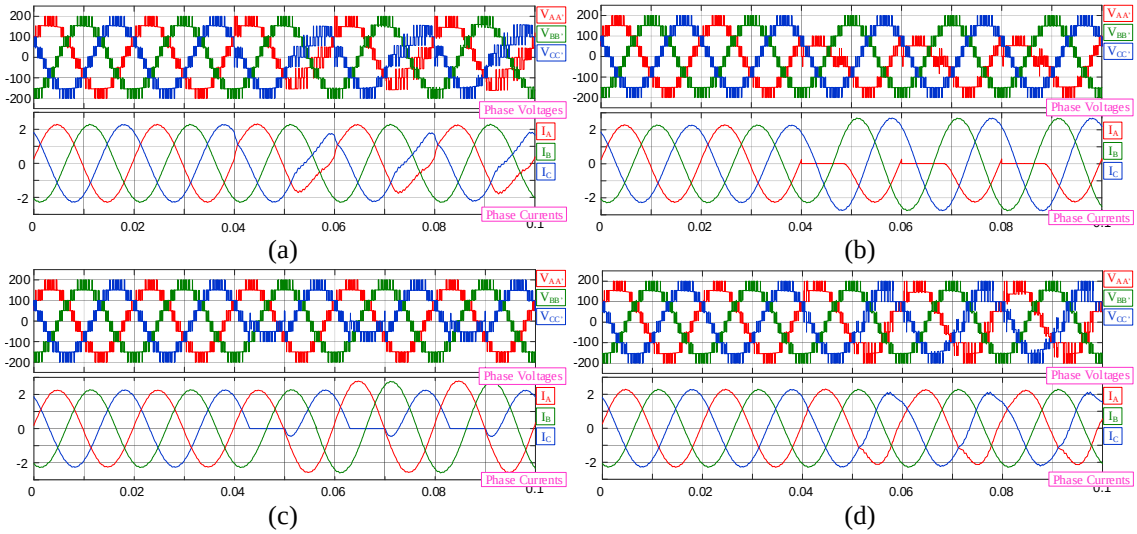


Figure 4. 6 Simulation results of three-phase voltages and currents of SCBT with open-circuit fault in switch: (a) S_{1a} (b) S_{3a} (c) S_{5a} (d) S_{7a}

In FCLBT, switch S_{1A} operates in complimentary with S_{4A} and switch S_{2A} operates in complimentary with S_{3A}. Hence the results are presented only for S_{1A} and S_{2A} OC faults. Similarly switches S_{5A} and S_{7A} operate in complementary with S_{6A} and S_{8A} respectively. Therefore waveforms of output voltage and current for switches S_{5A} and S_{7A} OC fault are presented. The output waveforms for OC faults in switch S_{6A} (or S_{8A}) would be the same as the vertical flip of results presented for OC fault of switch S_{5A} (or S_{7A}). Similarly, in SCBT switches S_{1a}, S_{3a}, S_{5a} and S_{7a} are operated in complementary with switches S_{2a}, S_{4a}, S_{6a} and

S_{8a}respectively. Hence waveforms for OC faults in switches S_{1a}, S_{3a}, S_{5a} and S_{7a} are presented in Figure 4.6.

4.5.2 Fault tolerant operation

The proposed topologies are capable of operating even under switch fault conditions. The switching logic has to be modified when a fault occurs in a switch in any of the inverters. If the fault occurred in the switch is an OC fault, then the switching strategy is that the gate pulses of the faulty switch are to be withdrawn and the switching logic has to be designed for the available healthy switches only. For the proposed topologies, out of twenty four switches if any of the switches is either open circuited or short circuited, then the modulation index has to be reduced to half (i.e., $M_a = 0.5$) and the inverter continue to operate as five level inverter with modified switching logic (MSL).

Table 4.3 Modified switching logic for FCLBT during switch OC fault conditions

Inverter -A	Open-Circuited Switch					
Switch	I. S_{1A}	II. S_{4A}	III. S_{2A}	IV. S_{3A}	V. S_{5A} or S_{7A}	VI. S_{6A} or S_{8A}
S_{1A}	0	$P*(Q_1+Q_2)+\overline{P}*(Q_1+Q_2)$	$\overline{P}*(Q_1+Q_2)$		$P*Q_1$	
S_{2A}	$P*(Q_1+Q_2)$		0	$P*(Q_1+Q_2)+\overline{P}*(Q_1+Q_2)$	$P*Q_2$	
S_{3A}	$\overline{P}*(Q_1+Q_2)$		$P*(Q_1+Q_2)+\overline{P}*(Q_1+Q_2)$	0	$P*Q_1+\overline{P}*(Q_1+Q_2)$	
S_{4A}	$P*(Q_1+Q_2)+\overline{P}*(Q_1+Q_2)$	0	$P*(Q_1+Q_2)$		$P*Q_2+\overline{P}*(Q_1+Q_2)$	
S_{5A} & S_{7A}	$P*Q_1$		$P*Q_1+P*(Q_1+Q_2)$		0	$P*(Q_1+Q_2)+\overline{P}*(Q_1+Q_2)$
S_{6A}& S_{8A}	$P*Q_2+\overline{P}*(Q_1+Q_2)$		$P*Q_2$		$P*(Q_1+Q_2)+\overline{P}*(Q_1+Q_2)$	0

Table 4.4 Modified switching logic for SCBT during switch OC fault conditions

Inverter –a	Open-Circuited Switch					
Switch	I. S_{1a}	II. S_{2a}	III. S_{3a} or S_{5a}	IV. S_{4a} or S_{6a}	V. S_{7a}	VI. S_{8a}
S_{1a}	0	$P*(Q_1+Q_2)+\overline{P}*(Q_1+Q_2)$	$P*Q_2+\overline{P}*(Q_1+Q_2)$		$P*Q_2$	
S_{2a}	$P*(Q_1+Q_2)+\overline{P}*(Q_1+Q_2)$	0	$P*Q_1$		$P*Q_1+\overline{P}*(Q_1+Q_2)$	
S_{3a}& S_{5a}	$P*Q_1$		0	$P*(Q_1+Q_2)+\overline{P}*(Q_1+Q_2)$	$P*Q_1$	
S_{4a}& S_{6a}	$P*Q_2+\overline{P}*(Q_1+Q_2)$		$P*(Q_1+Q_2)+\overline{P}*(Q_1+Q_2)$	0	$P*Q_2+\overline{P}*(Q_1+Q_2)$	
S_{7a}	$P*(Q_1+Q_2)$		$P*(Q_1+Q_2)$		0	$P*(Q_1+Q_2)+\overline{P}*(Q_1+Q_2)$
S_{8a}	$\overline{P}*(Q_1+Q_2)$		$\overline{P}*(Q_1+Q_2)$		$P*(Q_1+Q_2)+\overline{P}*(Q_1+Q_2)$	0

Note: where $\overline{P}$ is the complementary of gate pulse P.

For example, if the switches S_{xa} or S_{yA} (where x ϵ 2 or 3, y ϵ 7 or 8), are faulty, still the rated output power can be delivered with five levels in the output voltage and for faults in any other switches than these, the power delivered will decrease. The maximum output voltage is restricted to source voltage (V) under these conditions. The SPWM with reduced M_a for MSL is shown in Figure 4.7. Whenever an OC fault occurs in any of the switches, instead of complete shutdown of the supply system, the proposed topologies are made to operate with MSL provided in Table 4.4 and Table 4.5. If the OC fault occurs in switch S_{1A}, then the switching logic is designed for the healthy switches in the inverter-A and such logic is given in column-I in Table 4.4 for FCLBT and in Table 4.5 for SCBT. The switching logic for other switches when switch S_{1A} is open-circuited in inverter-A as presented in column-I in the Table 4.4, the same switching logic has to be applied for all the corresponding switches in the inverter-B and inverter-C as well to make the switching identical in all the inverters. Identical switching of inverters results in identical output voltages in all the phases.

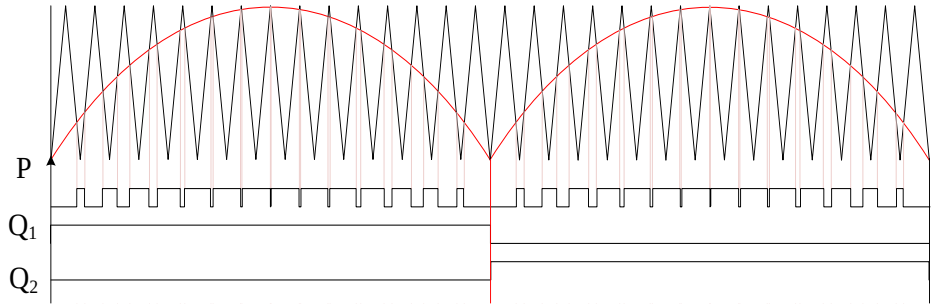


Figure 4. 7 Modulation scheme with M_a=0.5 and corresponding gate pulses

Similarly, if the SC fault occurs in any switch, the healthy switch in such leg is completely turned-off and the gate pulses for the other switches are dispensed as given in the Table 4.4. For example, if a SC fault occurs in switch S_{1A} then the switching logic provided in column-II for switch S_{4A} open circuit condition is employed. This clearly shows that the switching logic for SC fault in any switch is the switching logic of the OC fault condition of its complementary switch in the same leg. The strategy applied to the OC and SC faults in any switch are the same for both the topologies. The proposed topologies are capable of operating under switch faults, hence are more reliable compared to conventional topologies.

4.6 Results and discussions

The proposed topologies are designed such that the switches in neutral path act as level generators whereas the switches connected to the windings act as polarity generators. As a result of this, the output voltages obtained across every phase have nine levels ($\pm$2V, $\pm$3V/2, $\pm$V,

±V/2, 0) in it and the maximum output voltage is twice the source voltage (V) i.e., 2V. The proposed topologies are fed from three isolated DC sources each of 100V to feed 1-hp OEWIM. The Modified-reference PWM technique is employed to produce switching pulses for the proposed topologies and are dispensed using dSPACE 1104. A modified sinusoidal reference of the fundamental frequency is compared with the triangular carrier of frequency 1.5 kHz to generate switching pulses.

4.6.1 Experimental results

The three-phase output voltages, currents at no-load through three phase windings and the voltage across the FCs in the inverters feeding the OEWIM from SCBT are illustrated in Figure 4.8. Figure 4.8(a) presents the phase voltages $V_{AA'}$ (blue trace), $V_{BB'}$ (red trace). $V_{CC'}$ (green trace) across the load terminals A-A', B-B' and C-C'. The terminals A-A', B-B' and C-C' represent phase-A, phase-B and phase-C windings of the OEWIM respectively. Figure 4.8(b) represents three phase currents i_A (blue trace), i_B (red trace) and i_C (green trace) drawn by the OEWIM at no-load condition. Figure 4.8(c) presents the voltages V_{Ca} (blue trace), V_{Cb} (red trace) and V_{Cc} (green trace) that represents the voltage across the FC in inverter-a, inverter-b and inverter-c respectively. The output voltage $V_{AA'}$ for various values of modulation index (Ma=1, 0.75, 0.5, 0.25) are presented in Figure 4.8(d). The Fast Fourier Transform (FFT) of total harmonic distortion (THD) in the output phase voltage ($V_{AA'}$) and current (i_A) in phase-A are presented in Figure 4.8(e) and Figure 4.8(f) respectively.

The behaviour of the system during starting with an increase in modulation index from 0.2 to 1 is illustrated in Figure 4.9(a). The reference wave magnitude is determined by constant voltage per frequency ratio and speed requirement of the motor. The transition of output voltage from three levels to nine-levels can be observed clearly. During starting the current drawn by the induction motor is high and as the motor speed approaches the rated value, the current approaches the rated value. Figure 4.9(b) illustrates the behaviour of the system for a change in modulation index from 1 to 0.5. Decrease in modulation index will decrease the number of levels from nine to five in the output voltage, hence the output voltage magnitude reduces to half. The speed of the motor also reduces from 1440 rpm to 1270 rpm.

4.6.2 Performance of SCBT during switch faults

The SCBT delivers nine level output voltage across all the three phases under normal operating conditions. The balanced and identical output voltage across all the three phases is obtained from the inverters owing to symmetrical switching of the switching devices. However,

if any if the switch fails (either OC or SC), then it leads to loss of symmetry in switching and results in unbalance in the voltage fed to the OEWIM drive. Therefore, the unbalance in the supply fed to the motor will result in unbalanced currents that leads to excessive heating of the winding.

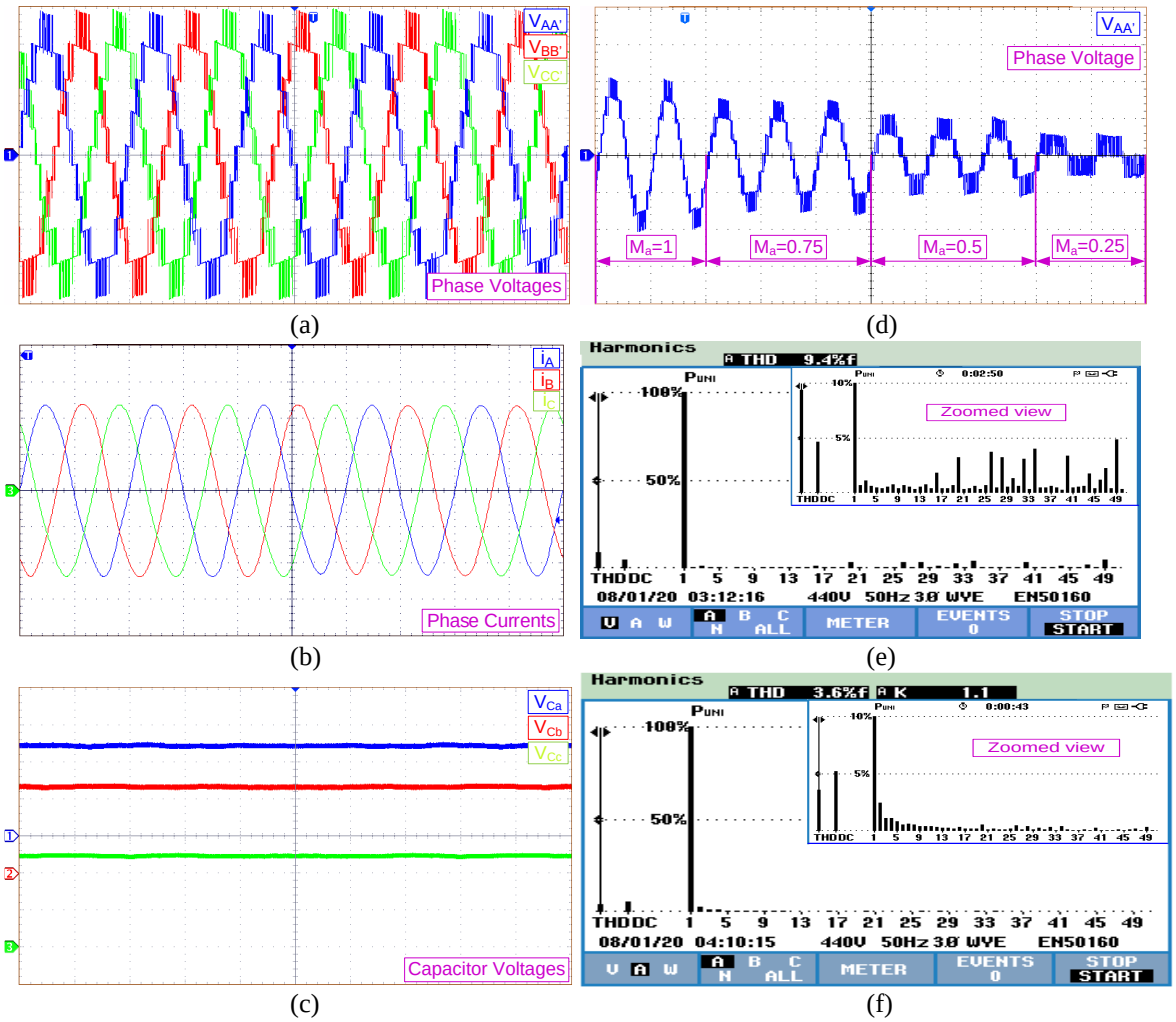
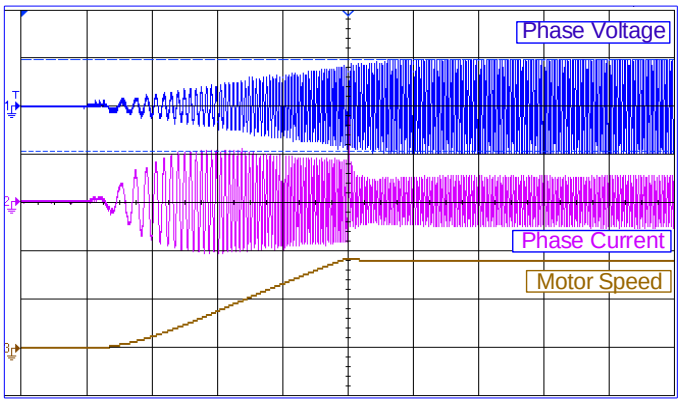


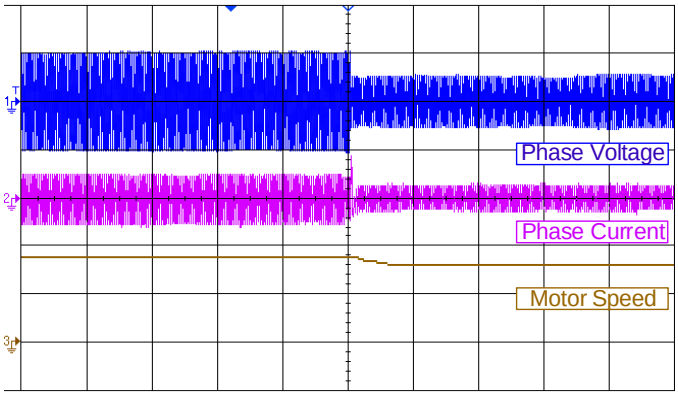
Figure 4. 8 Experimental results of SCBT (a) Three phase output voltages $V_{AA'}$, $V_{BB'}$ and $V_{CC'}$ (X-axis:10ms/div, Y-axis: 50V/div) (b) Three phase currents (X-axis:10ms/div, Y-axis: 500mA/div) (c) Voltages across capacitor in each phase (X-axis:1s/div, Y-axis: 20V/div) (d) Output voltage $V_{AA'}$ with variation in modulation index (e) THD for phase voltage (f) THD of phase current.

The effect of OC fault in switches on three phase output voltages, no-load currents and the voltage across the FCs are to be analysed. The OC fault is created by disengaging switching pulses to the switch. Since each inverter is provided with a FC, then the variation of capacitor voltages due to switch faults will be substantial depending upon the fault location. To clearly understand the variation in the FC voltages during switch faults the scale for X-axis of capacitor voltages is taken as 1sec/div. The waveforms of the output voltages and currents for OC of switch S_{1a} in inverter-*a* are presented in Figure 4.10(a) and Figure 4.10(b). The effect of switch

S_{1a} OC on FC voltages are presented in Figure 4.10(c). Switch S_{1a} is in the neutral path of the inverter topology and is linked with phase-A and phase-C. Hence the OC of the switch S_{1a} will affect the output of two phases. The negative peak of voltage $V_{AA'}$ and the positive peak of the voltage $V_{CC'}$ are affected. The voltages across FCs also get affected with this switch fault. The voltage across FC in inverter-*a* increases to 60V and the voltage across FC in inverter-*b* and inverter-*c* decrease to 10V and 20V respectively.



(a)



(b)

Figure 4. 9 Experimental results for SCBT (a) Output voltage across phase-A winding(X-axis:1sec/div, Y-axis: 50V/div), current through phase-A winding (Y-axis: 5A/div) and speed of the motor during starting(Y-axis: 800 rpm/div) (b) Output voltage across phase-A winding(X-axis:2secs/div, Y-axis: 50V/div), current through phase-A winding (Y-axis: 5A/div) and speed of the motor(Y-axis: 800 rpm/div) with change in modulation index from 1 to 0.5 after 5 secs.

Similarly if OC fault occurs in switch S_{2a}, since the switch S_{2a} is operating in complementary to the switch S_{a1}, therefore the positive peak of the voltage $V_{AA'}$ and the negative peak of the voltage $V_{CC'}$ will be affected. Consequently, the OC fault in switch S_{2a} would produce outputs as a vertical flip version of the results presented for OC of switch S_{1a}. Hence the faults in lower switches in the inverter legs that operate in complementary with upper switches are not produced. Figure 4.11 presents the output voltages, no-load currents and FC voltages when switch S_{3a} is open-circuited. Since the switch S_{3a} in inverter-*a* is connected to

phase-A winding, fault in such switch will affect the phase voltage $V_{AA'}$ and limits the flow of current during positive half cycle as illustrated in Figure 4.11(a) and Figure 4.11(b). The current i_A will be a positive clamped wave with this switch fault. The FC voltage V_{Cc} is least affected with this fault whereas the voltage V_{Ca} decreases slightly from 50V to 46V and the voltage V_{Cb} rises to 60V as illustrated in Figure 4.11(c).

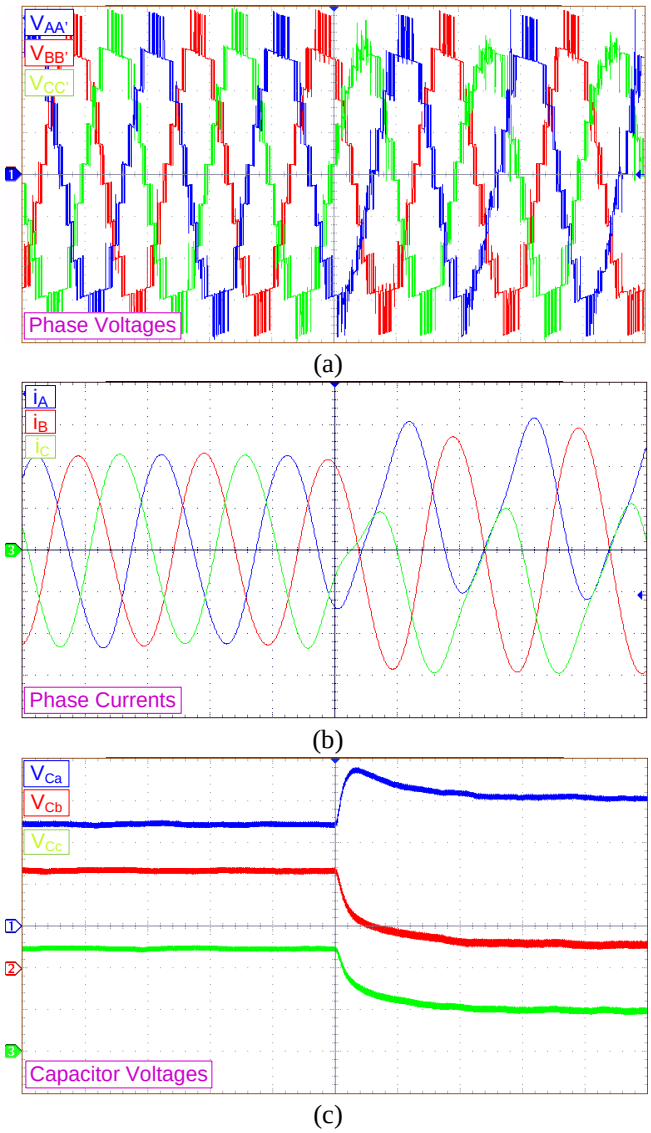
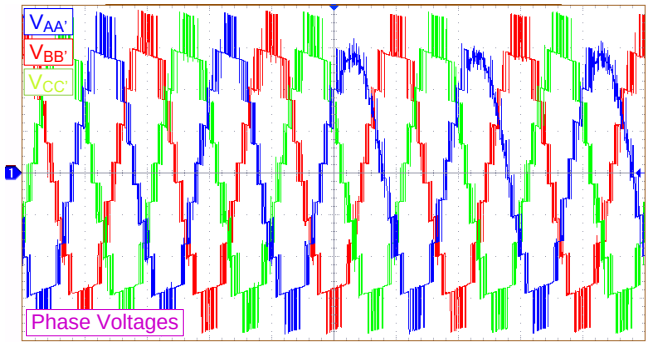


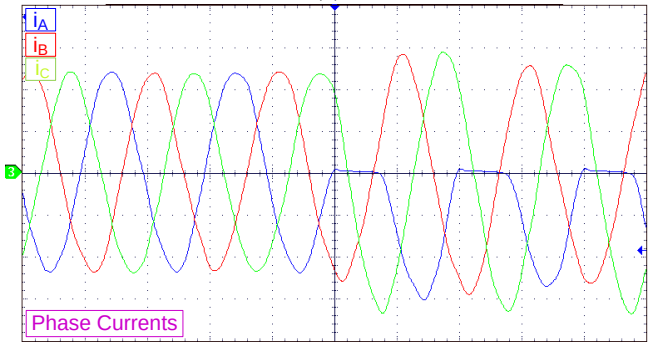
Figure 4. 10 Experimental results of (a) Three phase output voltage (X-axis:10ms/div, Y-axis: 50V/div) (b) No-load currents (X-axis:10ms/div, Y-axis: 500mA/div) (c) Voltage across capacitor in each phase (X-axis:1s/div, Y-axis: 20V/div) for OC fault in switch S_{a1}.

Similarly, if OC fault occurs in switch S_{5a} in inverter-*a*, the output voltages, no-load currents and the voltage across FCs will be as illustrated in Figure 4.12(a). As the switch S_{5a} is connected to phase-C, then the OC fault in S_{5a} will affect the negative peak of voltage $V_{CC'}$ and does not allow any current in the negative cycle as illustrated in Figure 4.12(a) and Figure 4.12(b). The voltage across all the three FCs will be affected as illustrated in Figure 4.12(c).The

output voltages, no-load currents and voltage across FCs when switch S_{7a} gets OC are presented in Figure 4.13. The OC fault in S_{7a} will avoid FC C_a from charging and discharging, hence the number of levels in the output voltage will gradually decrease to five levels keeping the maximum voltage the same as that with nine-levels in the output voltage as illustrated in Figure 4.13(a) and Figure 4.13(b). The voltages $V_{AA'}$ and $V_{CC'}$ will get affected with this fault and the voltage V_{Ca} will rise to source voltage $V_{DC}/2$ as the switch S_{7a} is open circuited. The FC voltage V_{Cb} rise marginally and V_{Cc} increase from 50V to 60V as illustrated in Figure 4.13(c). Hence the withstanding voltage of the FCs used for this topology should be same as that of the source voltage ($V_{DC}/2$) such that the capacitors can withstand the voltage under such fault conditions without any damage.



(a)



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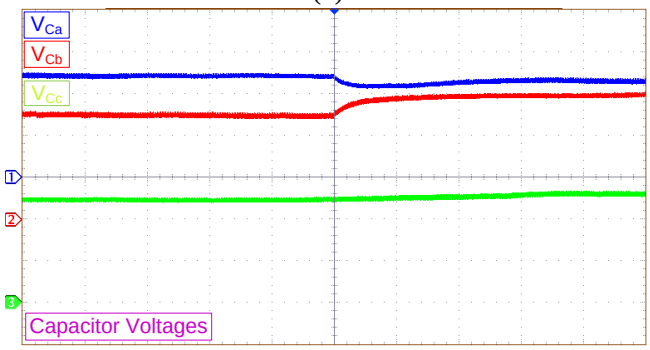


(c)

Figure 4. 11 Experimental results of (a) Three phase output voltage (X-axis:10ms/div, Y-axis: 50V/div) (b) No-load currents (X-axis:10ms/div, Y-axis: 500mA/div) (c) Voltage across capacitor in each phase (X-axis:1s/div, Y-axis: 20V/div) for OC fault in switch S_{a3}.

4.6.3 Performance of the proposed topologies with Modified Switching Logic (MSL)

The proposed topologies are capable of operating even under switch fault conditions. Whenever OC fault occurs in any of the switches, instead of complete shutdown of the supply system, the proposed topologies are made to operate with MSL provided in Table 4.4 and Table 4.5 designed considering the available switches exempting the faulty switch. Lowering the value of M_a not only reduces the number of levels in the output voltage, its magnitude also reduces to half and hence the output power reduces.

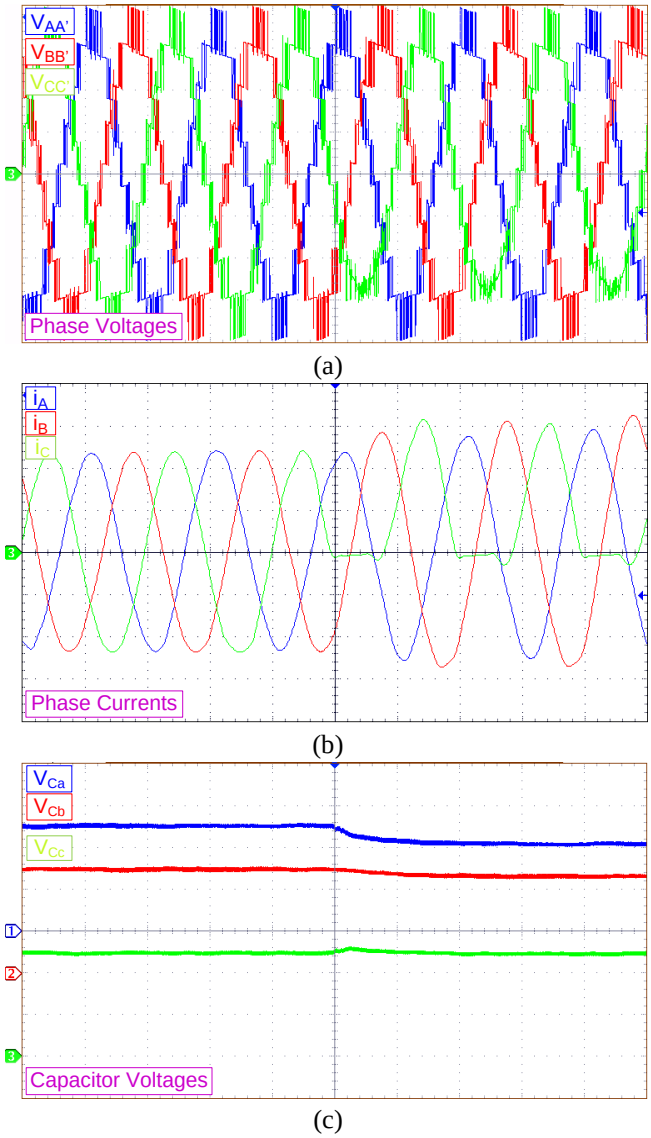


Figure 4. 12 Experimental results of (a) Three phase output voltage (X-axis:10ms/div, Y-axis: 50V/div) (b) No-load currents (X-axis:10ms/div, Y-axis: 500mA/div) (c) Voltage across capacitor in each phase (X-axis:1s/div, Y-axis: 20V/div) for OC fault in switch S_{a5}.

The FCs are charged to the same voltage level of V/2 with MSL as illustrated in Figure 4.14. However, for the faults in switches S_{x7} and S_{x8} (where x ϵ a, b, c), the application of MSL

will result in five level output voltage with maximum output voltage twice the source voltage as depicted in Figure 4.15. Since the FCs have no role to play in the post-fault operation the voltages across the FCs drop near to zero as illustrated in Figure 4.15(c). Therefore, the presented results prove that the proposed topologies work satisfactorily as five level inverters with rated power even if the fault occurs in FC or the switches across the FC.

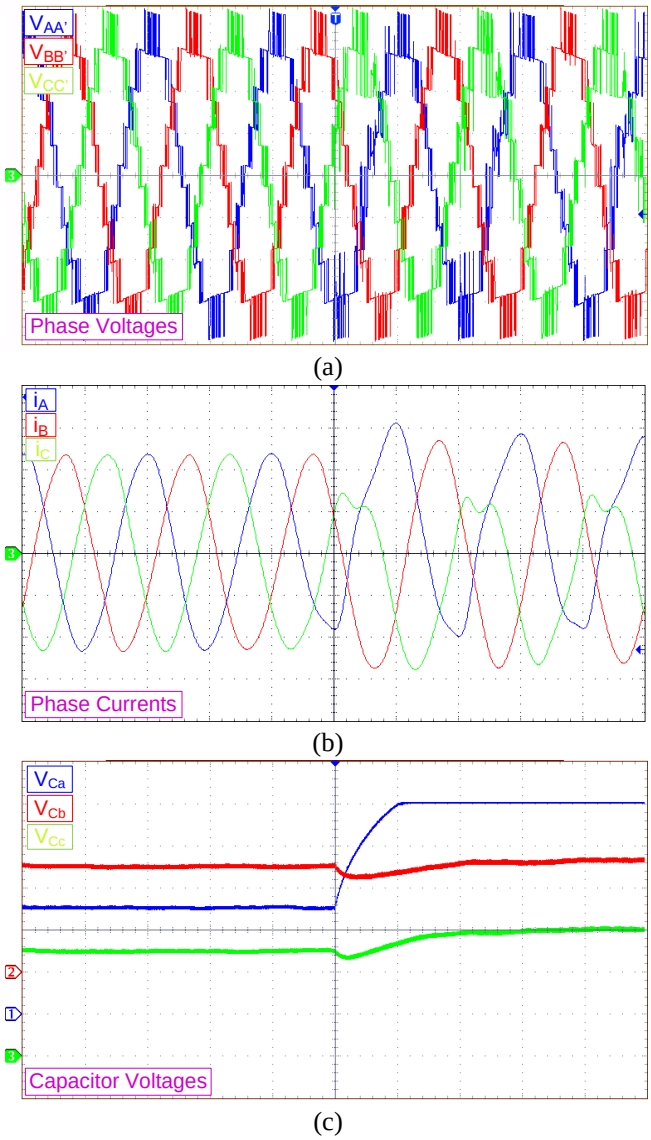


Figure 4. 13 Experimental results of (a) Three phase output voltage (X-axis:10ms/div, Y-axis: 50V/div) (b) No-load currents (X-axis:10ms/div, Y-axis: 500mA/div) (c) Voltage across capacitor in each phase (X-axis:1s/div, Y-axis: 20V/div) for OC fault in switch S_{a7}.

The proposed topologies ensure operation through normal conditions with nine level output voltage with each step level as V/2 across each phase winding. During fault conditions such as switch OC or SC, the proposed topologies still ensure uninterrupted operation with the decrease in levels in the output voltage as well as power. This uninterrupted operation of the proposed topologies is ensured by amending the switching pulses fed to the switches for post

fault operation. Through this study of proposed topologies over normal and abnormal conditions with pre and post-fault analysis, it can be justified that the proposed topologies exhibit fault-tolerance property for switch faults. The experimental setup of the PT (SCBT) feeding 1-hp OEWIM is presented in Figure 4.16.

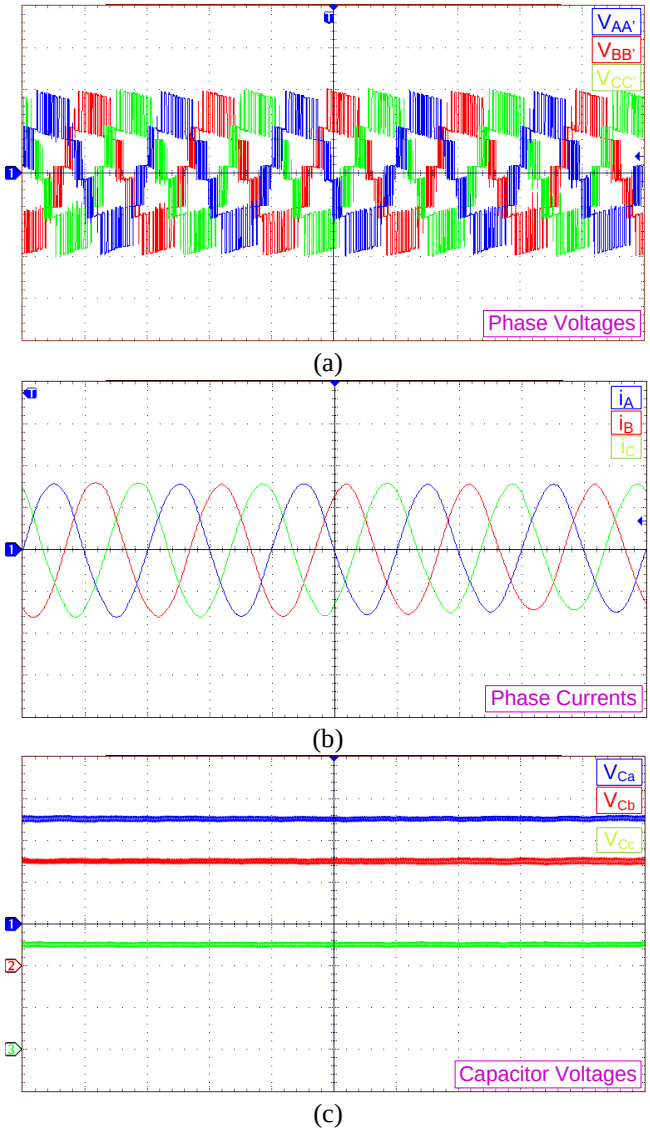


Figure 4. 14 Experimental results of (a) Three phase output voltage (X-axis:10ms/div, Y-axis: 50V/div) (b) No-load currents (X-axis:10ms/div, Y-axis: 500mA/div) (c) Voltage across capacitor in each phase (X-axis:1s/div, Y-axis: 20V/div) with MSL for S_{a1} OC in SCBT.

4.7 Comparison of the proposed topologies

The proposed topologies are compared with other similar topologies in terms of blocking voltage capability (V_B) of switches, DC capacitors, clamping diodes and number of sources required along with their rating and are presented in Table 4.3. The comparison is done

based on the assumption that the voltage blocking capability of the components is calculated when all these topologies are excited with a source voltage of V_{DC} and the actual source voltages required with their rating are mentioned under sources column. From Table 4.3, it is evident that the proposed topologies employ least number of switches as that in ACHB, out of total switches used, in FCLBT half of the switches have a blocking voltage equal to $0.5V_{DC}$ and the other half have a blocking voltage of $0.25V_{DC.}$ Whereas in SCBT three-fourth of the switches have a blocking voltage equal to $0.5V_{DC}$ and rest have a blocking voltage of $0.25V_{DC}$ (since the source voltage used for proposed topologies is only $0.5V_{DC}$).It implies that the total switch count is low and that the rating required is also low for the proposed topologies.

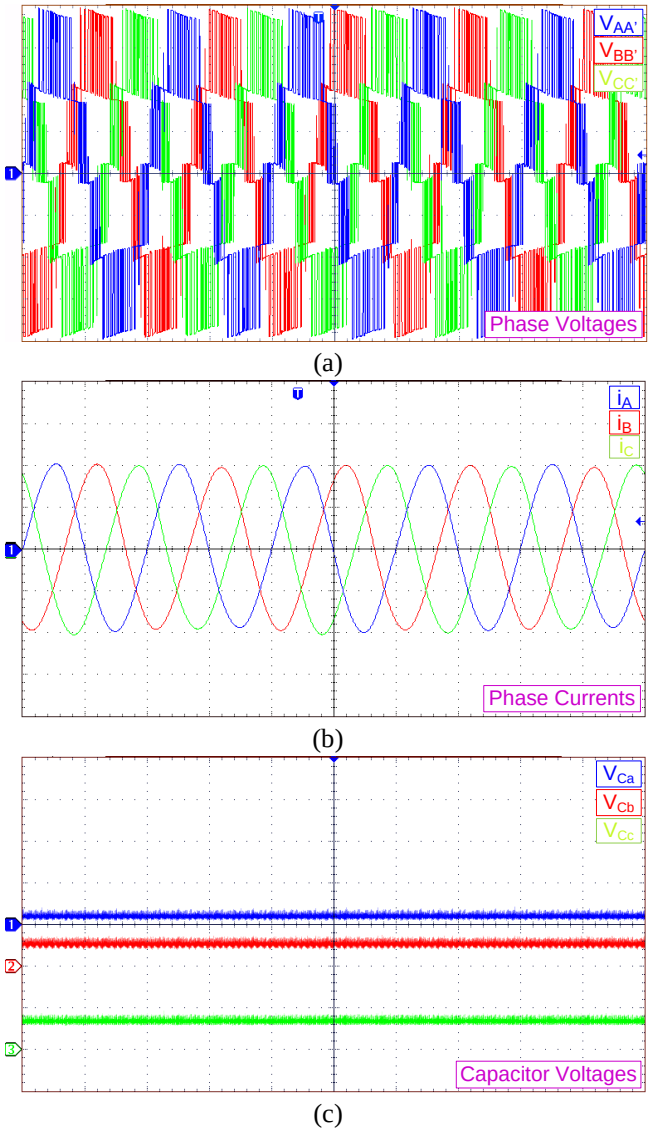


Figure 4. 15 Experimental results of (a) Three phase output voltage (X-axis:10ms/div, Y-axis: 50V/div) (b) No-load currents (X-axis:10ms/div, Y-axis: 500mA/div) (c) Voltage across capacitor in each phase (X-axis:1s/div, Y-axis: 20V/div) with MSL for S_{a7} OC in SCBT.

Table 4.5 Comparison of proposed topologies with other similar topologies feeding OEWIM drives.

Type of inverter	Active switches		DC capacitors		Clamping diodes		Sources	
	N	V_B	N	V_B	N	V_B	N	Rating
NPC	48	$0.25V_{DC}$	8	$0.125V_{DC}$	42	6 Diodes-$0.125V_{DC}$ 6 Diodes-$0.25V_{DC}$ 6 Diodes-$0.375V_{DC}$ 6 Diodes-$0.5V_{DC}$ 6 Diodes-$0.625V_{DC}$ 6 Diodes-$0.75V_{DC}$ 6 Diodes-$0.875V_{DC}$	1	V_{DC}
FC	48	$0.25V_{DC}$	108	$0.125V_{DC}$	0	-	1	V_{DC}
Conventional CHB(CCHB)	48	V_{DC}	0	-	0	-	12	$V_{DC}/8$
Asymmetrical CHB(ACHB)	24	12 switches – $0.75V_{DC}$ 12 switches – $0.25V_{DC}$	0	-	0	-	3 3	$3V_{DC}/8$ $V_{DC}/8$
P.P. Rajeevan *et al.*, 2013.	36	12 switches – V_{DC} 12 switches – $0.5V_{DC}$ 12 switches – $0.25V_{DC}$	6	-	0	-	2	V_{DC}
P.P. Rajeevan *et al.*, 2011.	36	12 switches – V_{DC} 24 switches – $0.33V_{DC}$	6	$0.33V_{DC}$	0	-	2	V_{DC}
G. Mondal *et al.*, 2009.	48	$0.166V_{DC}$	6	$0.0833V_{DC}$	12	$0.083V_{DC}$	6	$V_{DC}/12$
A.Kshirsagar *et al.*, 2018.	36	12 switches – $0.125V_{DC}$ 12 switches – $0.375V_{DC}$ 12 switches – $0.75V_{DC}$	9	3 Cap's-$0.125V_{DC}$ 3 Cap's-$0.375V_{DC}$ 3 Cap's-$0.75V_{DC}$	0	-	3 3	$3V_{DC}/4$ $V_{DC}/4$
FCLBT	24	12 switches – V_{DC} 12 switches – $0.5V_{DC}$	3	$0.5V_{DC}$	0	-	3	$V_{DC}/2$
SCBT	24	18 switches – V_{DC} 6 switches – $0.5V_{DC}$	3	$0.5V_{DC}$	0	-	3	$V_{DC}/2$

Note: N represents Number, V_B – Blocking voltage, Cap's- Capacitors.

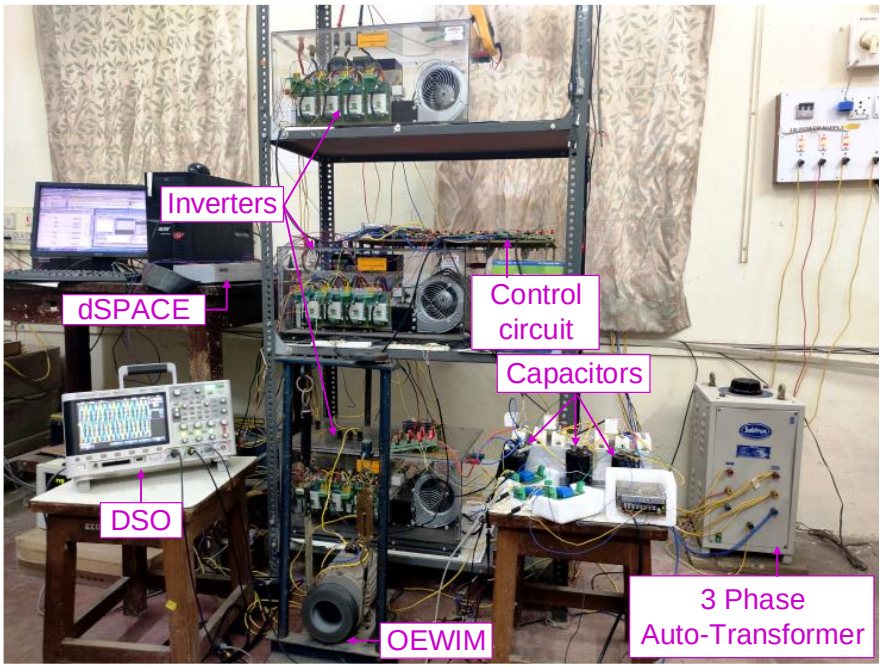


Figure 4. 16 Experimental setup

Every single MLI topology possesses both advantages and shortcomings based on the area of application and the proposed topologies are not an exemption. Compared with the conventional topologies the proposed topologies have certain shortcomings such as non-modular structure and require three isolated DC sources. However, with the advantages of low source voltage requirement, simple construction and its fault-tolerance property, the proposed topologies find applications in low voltage applications such as solar PV or fuel cell fed battery driven electric vehicles or in industries such as steel rolling mills, paper rolling mills, etc.

4.8 Summary

This chapter presents FC based fault-tolerant MLI topologies that can deliver nine-level output voltage. The proposed topologies employs a configuration that requires three three-phase inverters with an isolated DC source, FCs and additional active switches for each inverter. The FCs are charged and discharged to generate intermediate levels of the output voltage. Conventional SPWM techniques can be employed to generate switching pulses for these topologies. The proposed topologies are designed with fewer components compared to other nine-level topologies feeding OEWIM drive that are present in the literature. The magnitude of voltage sources required are also less compared to conventional topologies, hence the proposed topologies find good scope in renewable energy source applications and industry as well. The voltage rating of the FCs required is only half the source voltage rating, but to withstand the voltage during certain switch faults, the rating of the FCs should be made equal to source voltage. Both the topologies are capable of delivering power to the load during switch-fault conditions. In the post-fault operation, the inverters are run with modified switching logic and can deliver balanced three-phase output voltage with reduced number of levels thereby ensuring continuity of supply to load even under switch fault conditions. The proposed topologies suit better for medium and high-power traction and industrial drive applications.

Chapter 5

Floating-capacitor based inverter for open-ended winding induction motor drive with fault-tolerance

Chapter 5

Floating-capacitor based inverter for open-ended winding induction motor drive with fault-tolerance

5.1 Introduction

In drive applications MLIs are preferred because with an increase of levels in the output voltage the total harmonic distortions will be reduced and eliminate the need of larger sized filters. However, MLIs when designed for higher number of voltage levels become complex and bulky due to larger component count which shows huge impact on reliability of the system, hence the industry is reluctant to such MLIs since reliability is also an important concern. This necessitates the designing of MLIs for higher number of voltage levels with least possible components. Increase in components count of MLIs makes it less reliable because fault in even a single switch leads to supplying unbalanced voltage to the motor or complete system shutdown. A small unbalance in the voltage applied to the induction motor will induce large unbalanced currents in the phase windings. These unbalanced currents will result to adverse effects such as over-heating, increase in losses, vibrations, acoustic noises and decrease of the rotating torque.

MLI topologies with fault-tolerance capability based on redundant and non-redundant elements are presented in the literature. In non-redundant topologies, if fault occurs in any switch of the inverter, the entire leg of the inverter is to be isolated and the corresponding motor terminal is to be opened. As a consequence, the motor operates with an unbalanced supply and hence requires change in control scheme to continue the operation of the drive. Topologies with redundant elements are expensive, require larger space and are less reliable due to more component count. Hence a nine-level inverter topology for OEWIM drive with fault-tolerance to switch open-circuit (OC) and short-circuit (SC) is presented in this chapter. The proposed topology (PT) is designed with a minimum number of components and is intended for an induction motor with six terminals of stator winding brought out. In this topology, the three-phase windings of the induction motor are fed from three three-phase two-level inverters along with the floating capacitor bridge (FCB). The PT employs three isolated DC voltage sources each of a voltage $V_{DC}/2$ and the FC is utilized to realize intermittent voltage levels. The conventional modulation techniques are employed for switch gate-pulse generation and the

control scheme is designed to obtain intermittent voltage levels by charging and discharging the capacitor from all the three-phases. The PT employs lower voltage rating isolated dc sources and lower number of components than conventional topologies.

5.2 Proposed floating capacitor bridge based fault-tolerant MLI topology

The PT is a nine-level inverter topology for OEWIM drive designed based on conventional three-phase two-level voltage source inverters (VSIs) and floating capacitor bridge (FCB) as illustrated in Figure 5.1. The PT is designed with four VSIs and out of these four inverters, three inverters are directly connected to phase windings of the OEWIM drive and each inverter is fed from an isolated dc source whereas the fourth inverter is connected across a capacitor. Advantage of the PT is that the maximum output voltage is twice the magnitude of source voltage which is obtained by connecting the sources in series to realize the maximum output voltage across each phase. Hence the magnitude of the dc sources required will be $V_{DC}/2$ (where V_{DC} is the magnitude of the source voltage required by a conventional two level inverter), hence energy sources with low output voltage such as solar photovoltaic systems or fuel cells can be employed. Also the number of active switching elements is only twenty-four which are minimum for nine-level inverters feeding OEWIM drives.

In PT, the six switches (S_{a1} to S_{a6}) in the three-phase two-level VSI along with switches (S_{a7} and S_{a8}) in the first leg of FCB constitute inverter-a. Likewise, switches S_{b1} through S_{b8} constitute inverter-b and switches S_{c1} through S_{c8} constitute inverter-c. The connections in the PT are done as: the mid-point of the switches S_{x1} and S_{x2} of inverter-x is considered as connection port-1, likewise the mid-point of the switches S_{x3} and S_{x4} is considered as connection port-2 and the mid-point of the switches S_{x5} and S_{x6} is considered as connection port-3. The midpoint of the switches S_{x7} and S_{x8} is considered as connection port-4 of inverter-x (where x ϵ a, b, c). The connection port-1 of each inverter is connected to its connection port-4. Connection port-2 of each inverter is connected to one end of phase windings (namely A, B and C) and port-3 is connected to the other ends of the windings (A', B' and C'). The scheme of connection for phase windings is that the end terminals of each winding are connected to two adjacent inverters so as to receive supply from both ends from two different inverters to produce nine-level voltage across each winding of the OEWIM. For example, consider phase winding-A, terminal A is connected to connection port-2 of inverter-a and terminal A' is connected to connection port-3 of inverter-b. Likewise, the other two phase windings are also connected in the same method.

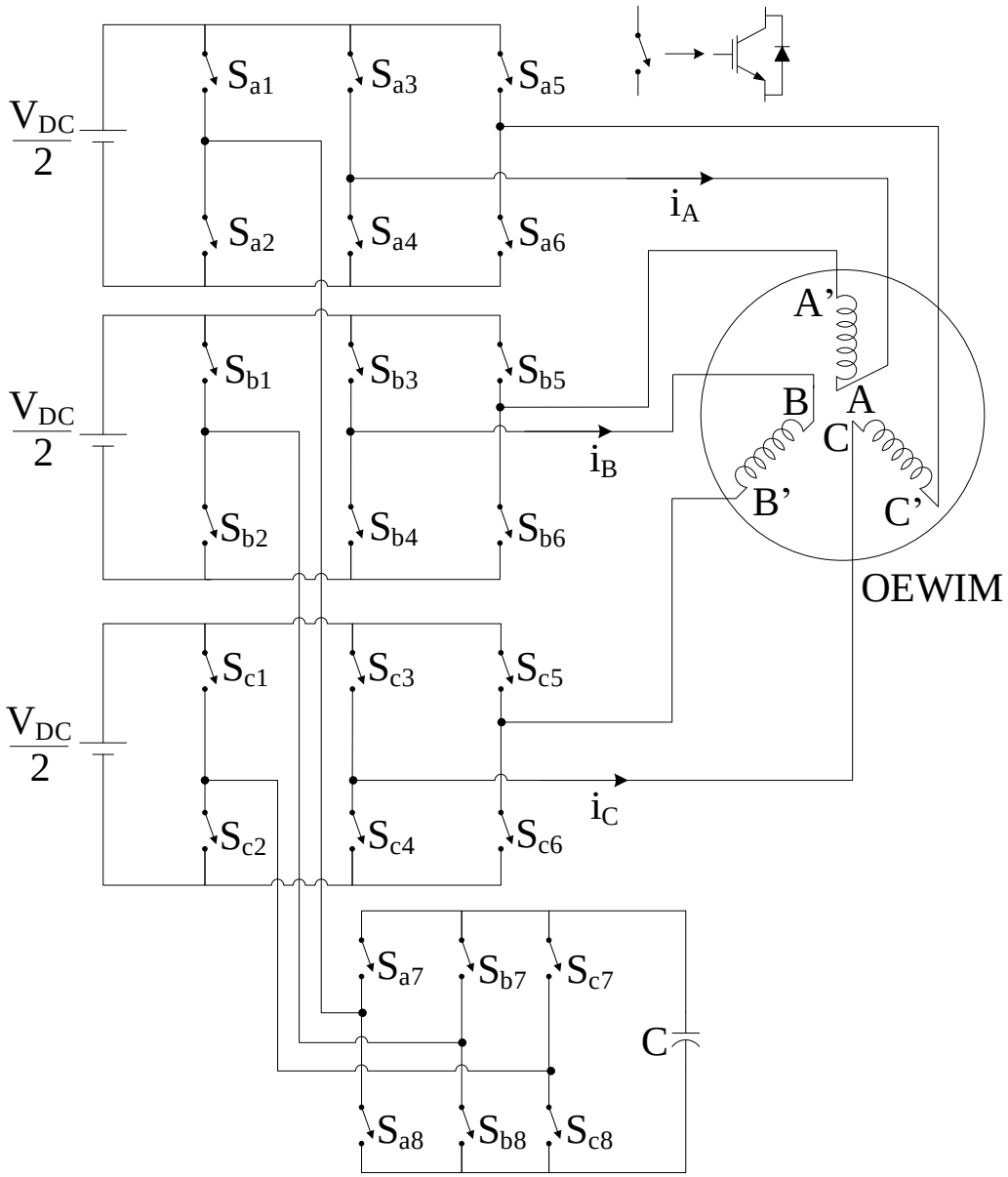


Figure 5. 1 Proposed Floating Capacitor Bridge Based MLI Topology

The switching states to generate output voltage with nine levels, namely $\pm V_{DC}$, $\pm 3V_{DC}/4$, $\pm V_{DC}/2$, $\pm V_{DC}/4$, 0, across the phase winding terminals A-A' of OEWIM drive are illustrated in Table 5.1. It can be clearly observed from Table 5.1 that the capacitor is charged and discharged during the voltage levels $\pm 3V_{DC}/4$ and $\pm V_{DC}/4$ of output voltage across phase winding-A. The switching states are selected such that the time-period is maintained equally for charging and discharging of the capacitor within a complete cycle of voltage waveform. For the satisfactory operation of the PT, the capacitor is charged and discharged to realize the intermittent voltages. The capacitor is charged during the positive cycle of the output voltage and is discharged for the same duration of time in the negative cycle as presented in Table 5.1.

Table 5. 1 Switching states for nine-level voltage generation across phase winding-A

Voltage level	Inverter-a			Inverter-b			Capacitor state
	S_{a1}	S_{a3}	S_{a7}	S_{b1}	S_{b5}	S_{b7}	
V_{DC}	0	1	0	1	0	0	No change
$3V_{DC}/4$	0	1	0	1	0	1	Charging
	0	0	1	1	0	0	Discharging
$V_{DC}/2$	0/1	0/1	1	1	0	0	No change
	0/1	0/1	0	1	0	1	
$V_{DC}/4$	1/0	1/0	1/0	1/0	1/0	0	Discharging
	0/1	1	1/0	1	1/0	0/1	Charging
0	1/0	1/0	1/0	1/0	1/0	1/0	No change
	0/1	0/1	1/0	0/1	0/1	1/0	
$-V_{DC}/4$	1	0/1	1/0	0/1	0	0/1	Charging
	0	0	0	0/1	0/1	1	Discharging
$-V_{DC}/2$	1	0/1	0	0	0/1	0	No change
	1/0	0	1	1/0	1	1	
$-3V_{DC}/4$	1	0	0	0	0	1	Discharging
	1	0	1	0	1	0	Charging
$-V_{DC}$	1	0	0	0	1	0	No change

Considering that the output voltage and the current are symmetrical, the average current (AVG[i_c]) flowing through the capacitor during the voltage levels $\pm 3V_{DC}/4$and $\pm V_{DC}/4$ with a load impedance of Z can be given as:

$$\mathrm{AVG}[i_c^+]_{V_{DC}/4} = \frac{\frac{V_{DC}}{2} - V_c}{Z}; \quad (5.1)$$

$$\mathrm{AVG}[i_c^-]_{3V_{DC}/4} = \frac{\frac{V_{DC}}{2} + V_c}{Z}; \quad (5.2)$$

$$\mathrm{AVG}[i_c^+]_{3V_{DC}/4} = \frac{V_{DC} - V_c}{Z}; \quad (5.3)$$

$$\mathrm{AVG}[i_c^-]_{V_{DC}/4} = \frac{V_c}{Z} \quad (5.4)$$

Hence, the resultant charge (Q) that is supplied or absorbed during a time period (T) can be expressed as

$$Q = \left\{\mathrm{AVG}[i_c^+]_{V_{DC}/4} + \mathrm{AVG}[i_c^+]_{3V_{DC}/4} - \mathrm{AVG}[i_c^-]_{V_{DC}/4} - \mathrm{AVG}[i_c^-]_{3V_{DC}/4}\right\} * T$$
$$= \left\{\frac{V_{DC} - 4V_c}{Z}\right\} \quad (5.5)$$

Assuming half wave symmetry of the output current, the average charge Q over a cycle is zero. Considering the value of Q as zero in the equation (5) will result as $V_c = 0.25V_{DC}$, where the voltage rating of each source is $0.5V_{DC}$ in the PT. The direction of load current defines the charging and discharging states of capacitor and does not require any additional complex

control circuit. A constant voltage of $0.25V_{DC}$ is maintained across the FCB by selecting proper switching states that will provide equal time-periods for charging and discharging.

The voltage across the phase windings of the OEWIM is determined by the switching states of the switches. Considering that the blocking state of a switch is represented by binary variable 0 and its conduction state is represented by variable 1. Considering $\hat{S}_{a1}=S_{a2}$, $\hat{S}_{a3}=S_{a4}$, $\hat{S}_{a5}=S_{a6}$, $\hat{S}_{a7}=S_{a8}$, $S_{a3}=S_{a5}$ and $S_{a4}=S_{a6}$, the voltage across the phase winding terminals A-A' of OEWIM can be written as

$$V_{AA'} = \frac{V_{DC}}{4}\begin{Bmatrix} 2\hat{S}_{a7}\left[\hat{S}_{a1}S_{a3} - S_{a1}\hat{S}_{a3}\right] + \hat{S}_{a3}S_{a7}\left[S_{a1} - \hat{S}_{a1}\right] + 2\hat{S}_{b7}\left[S_{b1}\hat{S}_{b5} - \hat{S}_{b1}S_{b5}\right] + \\ \hat{S}_{b5}S_{b7}\left[\hat{S}_{b1} - S_{b1}\right] \end{Bmatrix} \quad (5.6)$$

5.3 Modulation scheme

Sinusoidal pulse width modulation (SPWM) technique with modified reference wave and level shifted carriers is employed to generate gating pulses for the switches in the PT. The high frequency carrier waves are compared with the sinusoidal reference signal (V_{Ref}) of fundamental frequency to generate the gating pulses. In conventional SPWM technique, the modulation index (M_a) is defined by the magnitude of the sinusoidal reference signal. If the magnitude of the V_{Ref} is taken as unity, then $M_a=1$ and the magnitude of the carrier waves, here in this case, is half the magnitude of the reference voltage. With sinusoidal reference wave, the PT requires four level shifted carriers with phase disposition. Hence to reduce the computational burden on the processors of digital platforms such as dSPACE and DSPs the number of carriers required can be reduced. The sinusoidal reference signal is modified to reduce the need of carriers and is employed to generate the gating signals and are dispensed using dSPACE 1104 for the switches in the PT. The SPWM with modified reference employed to produce switch gate pulses is illustrated in Figure 5.2(a). Switching logics involved to generate gating pulses for the switches of the PT are illustrated in Figure 5.2(b).

5.4 Operation of the inverter during switch faults

In the PT, switches S_{a1} through S_{a8} constitute inverter-a and out of these eight switches, four switches i.e., switches S_{a3} through S_{a6} will guide the polarity generation of the output voltage. Similarly the other four switches will act as level generating elements and are connected together to form the neutral path for the PT. Since the number of switches employed are least, fault in any one switch will greatly affect the output voltage and current fed to the OEWIM. If a fault occurs in switches in FCB, then the PT can be made to operate with rated

output power as a five level inverter and if fault occurs in any other switch, then the PT is operated as a five-level inverter with half the rated power. Therefore to continue the operation of the PT with switch-faults, M_a has to be reduced to 0.5 and hence operated as a five-level inverter with modified switching logic (MSL) presented in Table 5.2 to ensure continuity in the supply for the OEWIM. The SPWM scheme with M_a=0.5 and the corresponding pulses are presented in Figure 5.3.

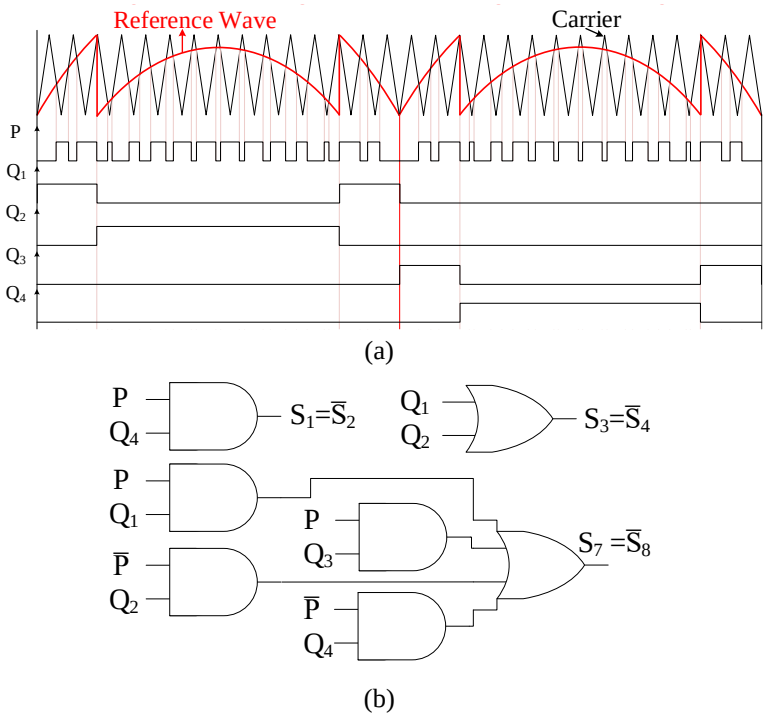


Figure 5. 2 Modulation scheme (a) SPWM with modified sinusoidal reference and single carrier wave, (b) switching logics for switch-gate pulses.

The faults in power switches in the inverters may be either an OC or a SC. The PT is capable of feeding the load even under such switch fault conditions. If an OC fault occurs in any of the switches in any of the inverters, the MSL is designed in such a way that the modulation index is reduced to 0.5 and the healthy switch in the leg of faulty switch is to be turned on completely. The MSL produces switching pulses for the available healthy switches to produce balanced three-phase output voltage across all the phase windings of the OEWIM. For example, if switch S_{a1} is faulted with OC, then the remaining switches in the inverter-a are fed with switching logics presented in column-I in the Table 5.2. Likewise, the same switching logic would be given to corresponding switches in other two inverters as well to create identical switching of the inverters to produce balanced three phase output voltages.

Similarly, if any switch in any of the inverters is faulted with a SC, immediately the healthy switch in such leg is turned-off to prevent a dead short across the source. The PT is

made to run as a five-level inverter by applying MSL provided in Table 5.2. The switching logics that are to be applied for the available healthy switches in such an inverter are the same switching logics that are applied for OC faults in other switches in the same leg. For example, if switch S_{a1} is faulted with a SC, then the switching logic for S_{a2} OC provided in column-II of Table 5.2 is to be employed because switches S_{a1} and S_{a2} operate in complementary to each other. Therefore the switching logic for SC fault in a switch is the same as the switching logic employed for OC fault of its complementary switch.

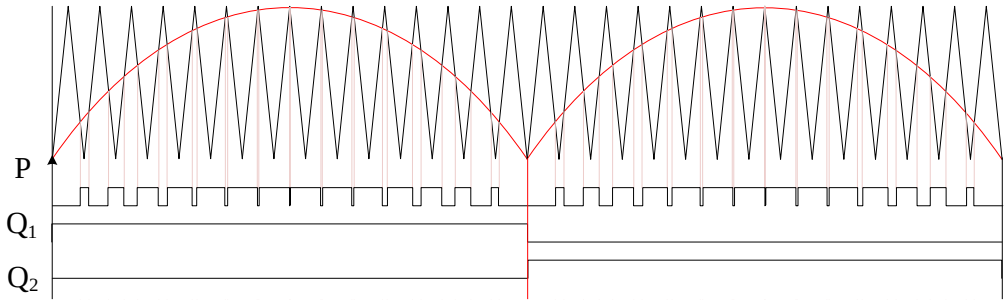


Figure 5. 3 Modulation switching scheme with Ma=0.5 and corresponding gate pulses

Table 5. 2 Modified switching logic under switch fault conditions

Inverter-a	Switch with Open-circuit fault					
Switch	I. S_{a1}	II. S_{a2}	III. S_{a3} or S_{a5}	IV. S_{a4} or S_{a6}	V. S_{a7}	VI. S_{a8}
S_{a1}	0	$P*(Q_1+Q_2) + \bar{P}*(Q_1+Q_2)$	$P*Q_2$	$P*Q_1+ \bar{P}*(Q_1+Q_2)$	$P*Q_2+ \bar{P}*(Q_1+Q_2)$	$P*Q_2+ \bar{P}*(Q_1+Q_2)$
S_{a2}	$P*(Q_1+Q_2) + \bar{P}*(Q_1+Q_2)$	0	$P*Q_1+ \bar{P}*(Q_1+Q_2)$	$P*Q_2$	$P*Q_1$	$P*Q_1$
S_{a3}& S_{a5}	$P*Q_2+ \bar{P}*(Q_1+Q_2)$	$P*Q_2+ \bar{P}*(Q_1+Q_2)$	0	$P*(Q_1+Q_2) + \bar{P}*(Q_1+Q_2)$	$P*Q_1+ \bar{P}*(Q_1+Q_2)$	$P*Q_1+ \bar{P}*(Q_1+Q_2)$
S_{a4}& S_{a6}	$P*Q_1$	$P*Q_1$	$P*(Q_1+Q_2) + \bar{P}*(Q_1+Q_2)$	0	$P*Q_2$	$P*Q_2$
S_{a7}	$P*(Q_1+Q_2)$	$P*(Q_1+Q_2)$	$P*(Q_1+Q_2)$	$P*(Q_1+Q_2)$	0	$P*(Q_1+Q_2) + \bar{P}*(Q_1+Q_2)$
S_{a8}	$\bar{P}*(Q_1+Q_2)$	$\bar{P}*(Q_1+Q_2)$	$\bar{P}*(Q_1+Q_2)$	$\bar{P}*(Q_1+Q_2)$	$P*(Q_1+Q_2) + \bar{P}*(Q_1+Q_2)$	0

Note: where P is the switching pulse and $\bar{P}$ is its complementary.

5.5 Determination of the capacitance

The intermittent voltage levels are realized by a FCB, hence the value of capacitance required is to be evaluated. The peak value of load current (I_p), peak-to-peak ripple voltage (ΔV) and switching time period (ΔT) define the value of capacitance required. Considering these parameters, the minimum capacitance value (C) required and can be determined as

$$I_p = C\frac{dv}{dt} = C\frac{\Delta V}{\Delta T}$$

$$C = I_p\frac{\Delta T}{\Delta V} = \frac{I_p}{\Delta V * f_{sw}} \qquad (5.7)$$

Where f_{sw} is the inverter switching frequency. If ΔV is to be limited to 4 V with a switching frequency of 1500 Hz, then the value of capacitance required will be 666 μF. Therefore a capacitor of 1000μF is employed in experimental setup.

5.6 Results and discussion

The PT is designed such that the switches S_{x3}, S_{x4}, S_{x5} and S_{x6} (where x ϵ a, b, c) constitute polarity generator and the rest of the switches (S_{x1}, S_{x2}, S_{x7} and S_{x8}) with FC acts as level generator circuit. All these level generator circuits are assembled as a star connection and form the neutral path for the inverters. With this scheme of connection, the voltages across each phase winding will have nine levels ($\pm V_{DC}$, $\pm 3V_{DC}/4$, $\pm V_{DC}/2$, $\pm V_{DC}/4$, 0) in it with the peak value of twice the source voltage. For experimental validation, the PT is fed from three isolated DC sources each of 100V to feed 1-hp OEWIM. The sinusoidal PWM technique with modified-reference wave employing single carrier wave of 1500 Hz is employed to produce gate pulses for the PT. The required switch gate-pulses are generated using dSPACE 1104. Simulations are performed in the MATLAB/Simulink environment.

The experimental results for the PT are illustrated in Figure 5.4. Figure 5.4(a) presents the phase voltages $V_{AA'}$ (blue trace), $V_{BB'}$ (red trace). $V_{CC'}$ (green trace) across the terminals A-A', B-B' and C-C' which represents phase windings A, B and C of the OEWIM respectively. The capacitor voltage (V_C) across the FCB (pink trace) and currents i_A (blue trace), i_B (red trace) and i_C (green trace) flowing through the phase windings of the OEWIM at no-load condition is presented in Figure 5.4(b). The phase voltage $V_{AA'}$ for change in modulation index, Ma with values of 1, 0.75, 0.5, 0.25 are presented in Figure 5.4(c). The fast fourier transform (FFT) analysis for total harmonic distortion (THD) in the output phase voltage ($V_{AA'}$) and current (i_A) in phase-A are illustrated in Figure 5.4(d) and Figure 5.4(e) respectively. The voltage stress across the switches of inverter-a are illustrated in Figure 5.5(a) and Figure 5.5(b). From Figure 5.5(a) and Figure 5.5(b), it can be observed that the switches in FCB with lower blocking voltage are switched at higher frequency and switches in neutral path such as S_{a1} and S_{a2} are switched at fundamental frequency. However, switches S_{a3} to S_{a6} are switched for longer time in one half cycle and remains constant for longer time in other half cycle. In other words, relatively these switches have switching instants only in one half cycle of the fundamental frequency that ensures reduced switching losses in the inverter in the post-fault operation.

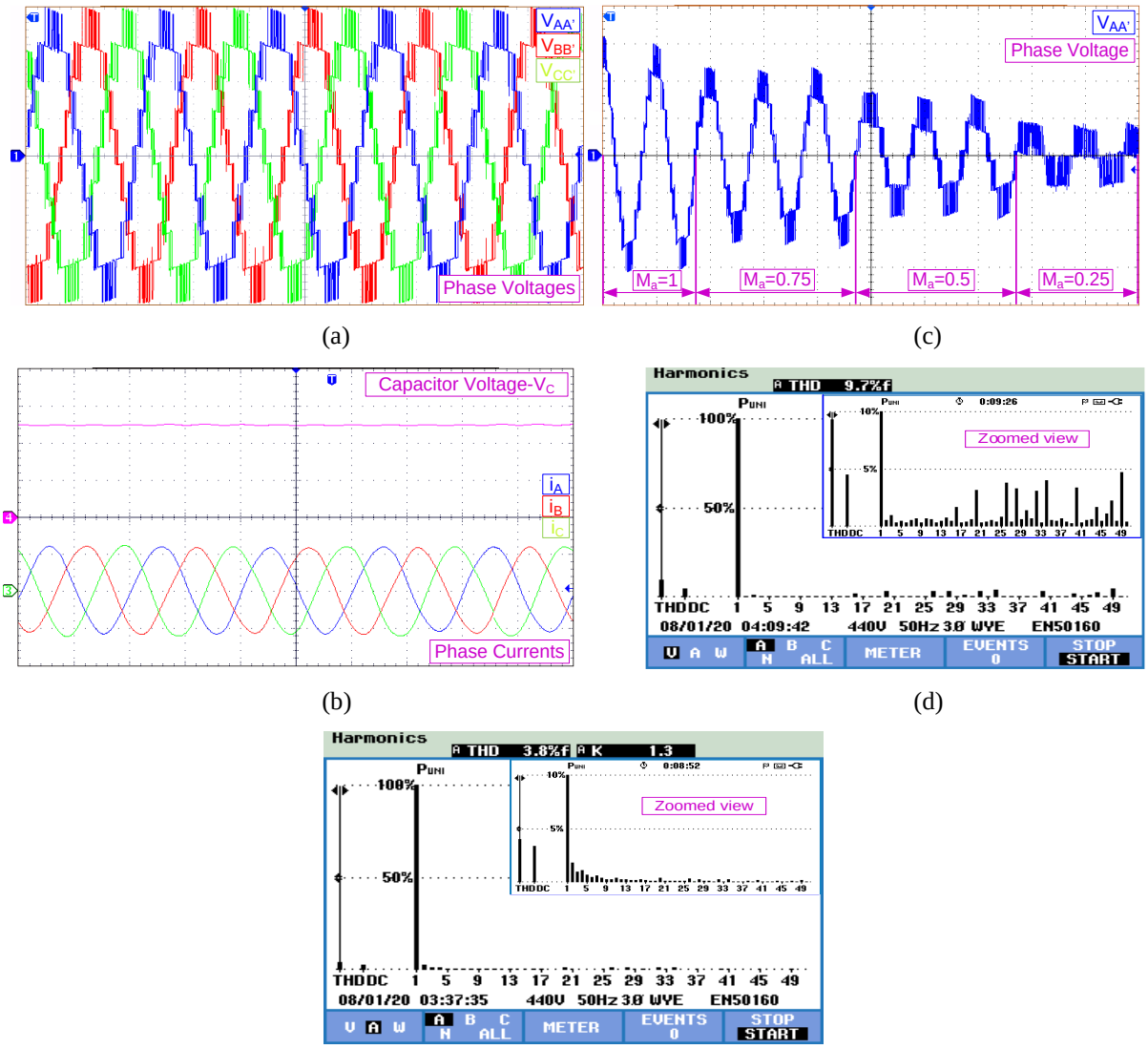


Figure 5. 4 Experimental results of (X-axis:10ms/div) (a) Phase voltages $V_{AA'}$, $V_{BB'}$ and $V_{CC'}$ (Y-axis: 50V/div) (b) Voltage (upper trace) across the floating capacitor bridge (Y-axis: 20V/div) and currents through three phase-windings (Y-axis: 1A/div) (c) Output voltage $V_{AA'}$ with decrease in M_a (d) FFT of voltage $V_{AA'}$ (e) FFT of current i_A.

The PT is made to operate with MSL during switch-faults and does not require any extra hardware which avoids the need for redundant switching units. In the post- fault operation, a balanced output voltage is obtained across all the phase windings by maintaining switching symmetry in all the inverters. To ensure symmetrical switching, some of the healthy switches are also left unused in post-fault operation. The PT ensures balanced three-phase supply to the OEWIM even during faults in the switches in the inverters and hence makes it reliable when used for low voltage medium power applications such as feeding motors in industrial and electric vehicular applications.

5.6.1 Performance of the proposed topology under switch OC faults

The PT is designed to yield nine-level output voltage by employing only one capacitor. The capacitor is charged and discharged through all the phases according to the switching logic and a fault in any switch will not disturb the capacitor voltage much. The OC fault in any one switch of this topology will result in unbalanced output voltages and thereby producing unbalanced currents in the load. The output voltages across the three phases ($V_{AA'}$, $V_{BB'}$ and $V_{CC'}$), no-load three phase currents (i_A, i_B and i_C) and voltage (V_C) across FCB for OC faults in various switches of the inverter-a in the PT are presented in this section.

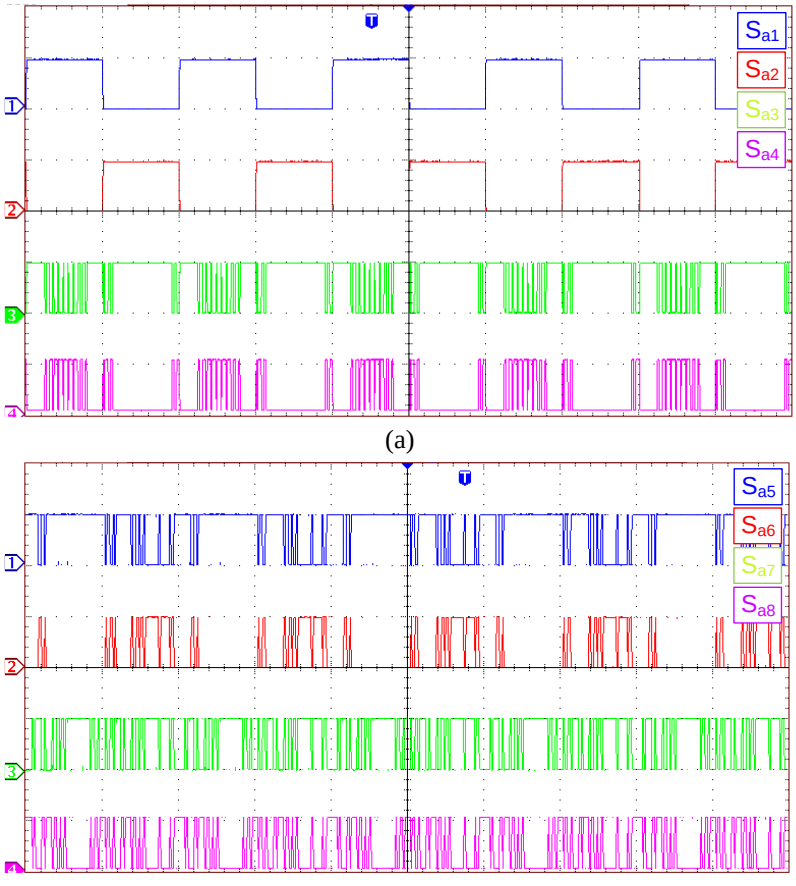
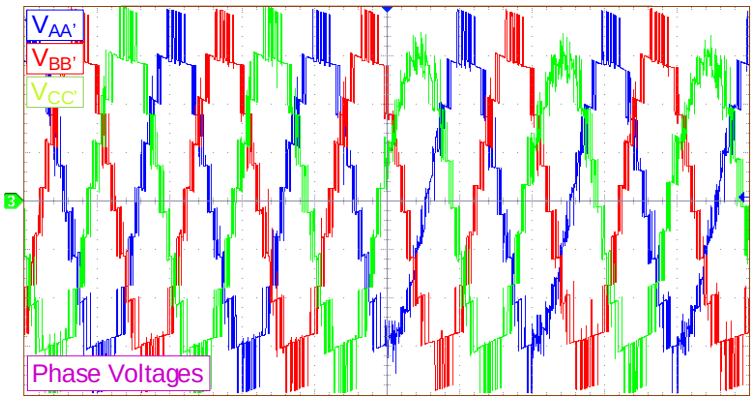


Figure 5. 5 Experimental results for voltage stress across (X-axis:10ms/div) (a) switches S_{a1}, S_{a2}, S_{a3} and S_{a4} (Y-axis: 100V/div) (b) Switches S_{a5}, S_{a6} (Y-axis: 100V/div) and S_{a7}, S_{a8} (Y-axis: 50V/div).

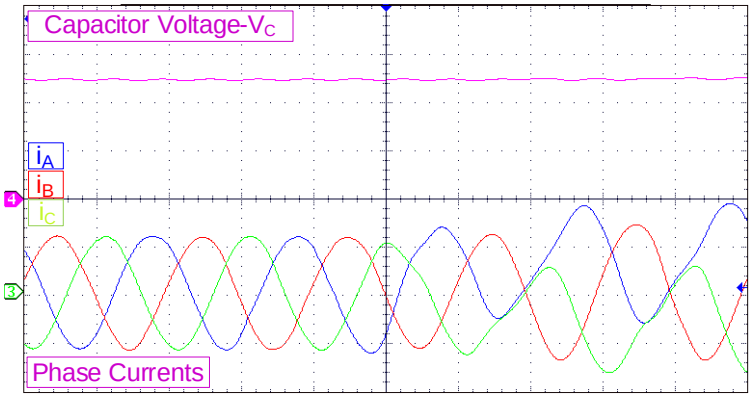
If switch S_{a1} is faulted with OC, then the voltages $V_{AA'}$ and $V_{CC'}$ gets affected since the switch S_{a1} is in the neutral path of phase-A and phase-C. The three phase voltages during normal and switch S_{a1} OC condition will be as illustrated in Figure 5.6(a). The capacitor voltage, V_C and the three phase no-load currents are presented in Figure 5.6(b). Similarly, Figure 5.7 presents the effect of switch S_{a3} OC on the output voltages, currents and FC voltage. Figure 5.7(a) presents the output phase voltages with S_{a3} OC initiated at 50ms. Since the switch S_{a3}

connects the source to phase-A winding, OC in S_{a3} affects the positive peak of $V_{AA'}$. The FCB voltage and three phase no-load currents are illustrated in Figure 5.7(b). Since the switch S_{a3} is OC, the current i_A will be a positive clamped wave.

Figure 5.8 depicts the output voltages and currents along with FC voltage when an OC fault occurs in switch S_{a5}. Figure 5.8(a) presents the three phase output voltages with switch S_{a5} open-circuited at 50ms and Figure 5.8(b) presents capacitor voltage in the upper trace and the three phase currents at no-load in the lower traces. Figure 5.9 illustrates the output voltages and currents along with capacitor voltage when an OC fault occurs in switch S_{a7}. Figure 5.9(a) presents the three phase output voltages with switch S_{a7} open-circuited at 50ms. The output voltages $V_{AA'}$ and $V_{CC'}$ get affected with this fault. Figure 5.9(b) presents capacitor voltage in the upper trace and the three phase currents at no-load in the lower traces. As like voltages, currents in phase-A and phase-C get affected with this fault. Faults in inverter switches will produce unbalanced voltages which will cause unbalanced currents in the phase windings of OEWIM drive. Unbalanced currents will have impact on its performance such as increased losses, temperature rise, a reduction in torque, efficiency and the life of the motor insulation.



(a)



(b)

Figure 5. 6 Waveforms of (X-axis:10ms/div) (a) Three phase voltages (Y-axis: 50V/div) (b) Capacitor voltage (Y-axis: 20V/div) and three-phase no-load currents (Y-axis: 1A/div) with OC in switch S_{a1}.

5.6.2 Performance of the proposed topology under switch SC faults

In the PT, switch OC faults will result in unbalanced voltage at the output but a SC fault of switch in any of the inverter legs will result in a dead SC across the source when the healthy switch is turned-on. Hence, whenever a SC fault occurs in any switch, then the healthy switch in such leg should be turned-off completely to avoid SC of the source. This will disturb the identical switching of the inverters and unbalanced voltages will be produced at the output. To overcome this, the switching logic provided in Table 5.2 is to be employed. The switching logic provided is for switch OC faults in which the logic is designed such that the healthy switch in the leg in which OC fault occurs is turned-on completely in the post-fault operation. This gives an advantage in employing the same logic for switch SC faults but the complementary switch switching logic has to be employed under SC fault condition. Consider a SC fault in switch Sa1 of inverter-a, then the switching logic under fault condition for switch Sa2 given in column II of Table 5.2 is to be employed as switching logic. Similarly, the same logic is employed for SC faults in other switches in the PT.

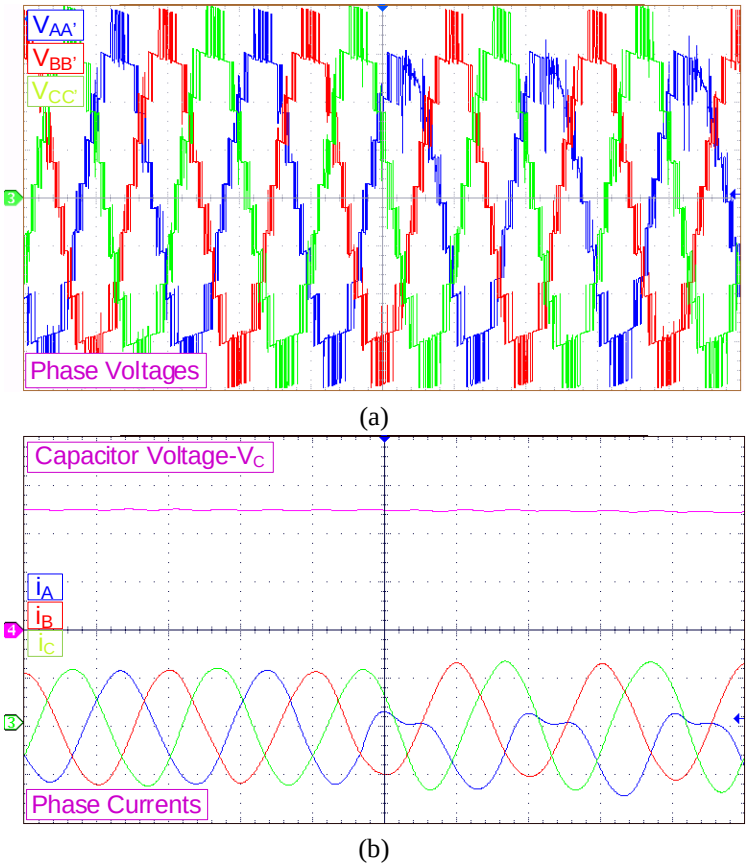


Figure 5. 7 Waveforms of (X-axis:10ms/div) (a) Three phase voltages (Y-axis: 50V/div) (b) Capacitor voltage (Y-axis: 20V/div) and three-phase no-load currents (Y-axis: 1A/div) with OC in switch S_{a3}.

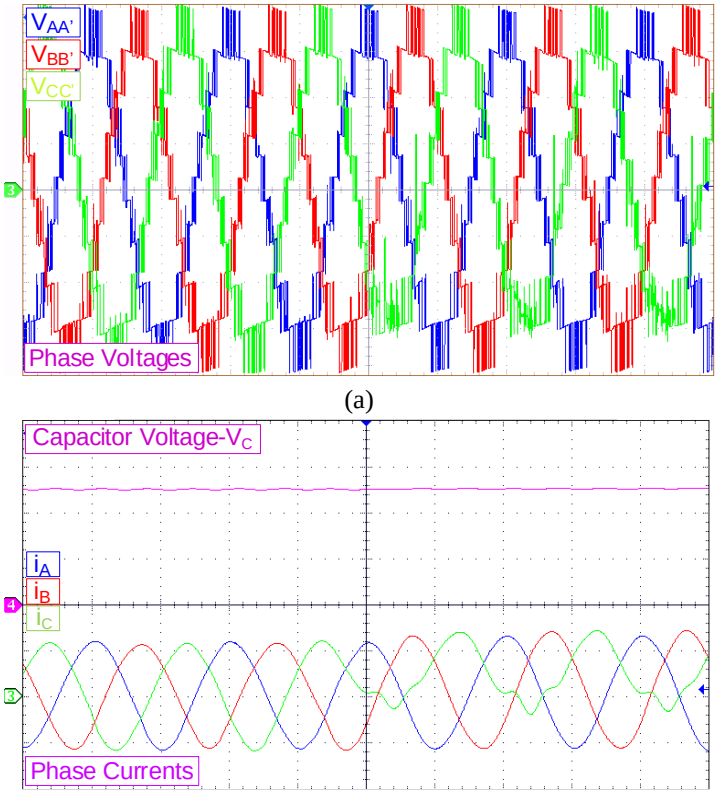


Figure 5. 8 Waveforms of (X-axis:10ms/div) (a) Three phase voltages (Y-axis: 50V/div) (b) Capacitor voltage (Y-axis: 20V/div) and three-phase no-load currents (Y-axis: 1A/div) with OC in switch S_{a5}.

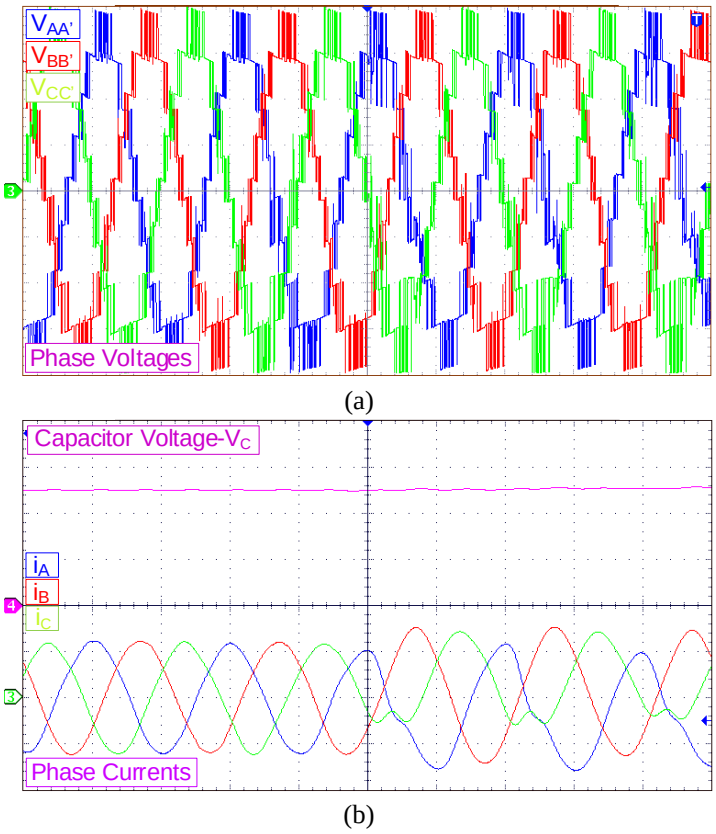


Figure 5. 9 Waveforms of (X-axis:10ms/div) (a) Three phase voltages (Y-axis: 50V/div) (b) Capacitor voltage (Y-axis: 20V/div) and three-phase no-load currents (Y-axis: 1A/div) with OC in switch S_{a7}.

5.6.3 Performance of the proposed topology with MSL

The PT is capable of operating and feeding the windings of OEWIM drive even with fault in switches with MSL. The waveforms of the three phase output voltages, currents and capacitor voltage with switch S_{a1} OC and with MSL for switch S_{a1} OC are presented in Figure 5.10. Due to OC fault in switch S_{a1}, the output voltages of phase windings connected to inverter-a namely phase-A and phase-C will be affected. The voltage across the FCB is least affected because the other two phases still feed the FC. Due to fault in switch S_{a1}, in the post fault operation the PT produces five level output voltage with reduced magnitude as illustrated in Figure 5.10(a). The capacitor voltage increases slightly more than the rated value due to OC in switch S_{a1} and after applying the MSL the FCB voltage drops to the rated value and remains the same throughout the operation as illustrated in Figure 5.10(b).

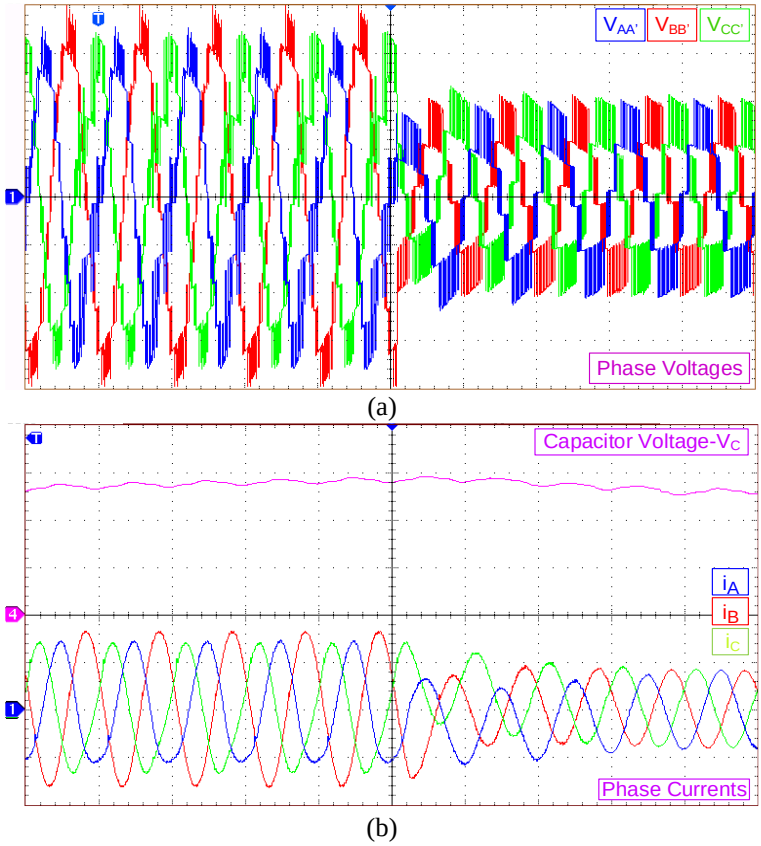


Figure 5. 10 Waveforms of (X-axis:10ms/div) (a) Three phase output voltage (Y-axis: 50V/div) (b) Capacitor voltage (Y-axis: 20V/div) and three-phase no-load currents (Y-axis: 1A/div) with MSL for S_{a1} OC.

Faults in switches in FCB i.e., S_{x7} and S_{x8} (where x ϵ a, b, c) will reduce the number of levels from nine to five in the output phase voltage with peak value twice the source voltage as illustrated in Figure 5.11(a). With switch S_{a7} OC fault, the voltage across the FCB is increased from 50V to 75V with greater than before voltage ripples. The rise in voltage is due to the fact that the capacitor gets charged from other two inverters but the current path for phase windings

of phase-A and phase-C during intermittent voltage levels is opened due to OC fault in S_{a7}. This rise in capacitor voltage will also affect the other phase winding voltages as illustrated in Figure 5.11(b). Whenever fault occurs in either switches S_{x7} or S_{x8} (where x ϵ a, b, c), then the top three switches (S_{a7}, S_{b7} and S_{c7}) or the bottom three switches (S_{a8}, S_{b8} and S_{c8}) of the FCB are turned-on continuously throughout the operation. Subsequently in the post fault operation with faults in switches S_{a7} or S_{a8}, the capacitor has no role to play and hence the voltage across the capacitor drops to zero over a period of time due to its internal impedance. Figure 5.12 presents the experimental setup of the PT feeding 1-hp OEWIM.

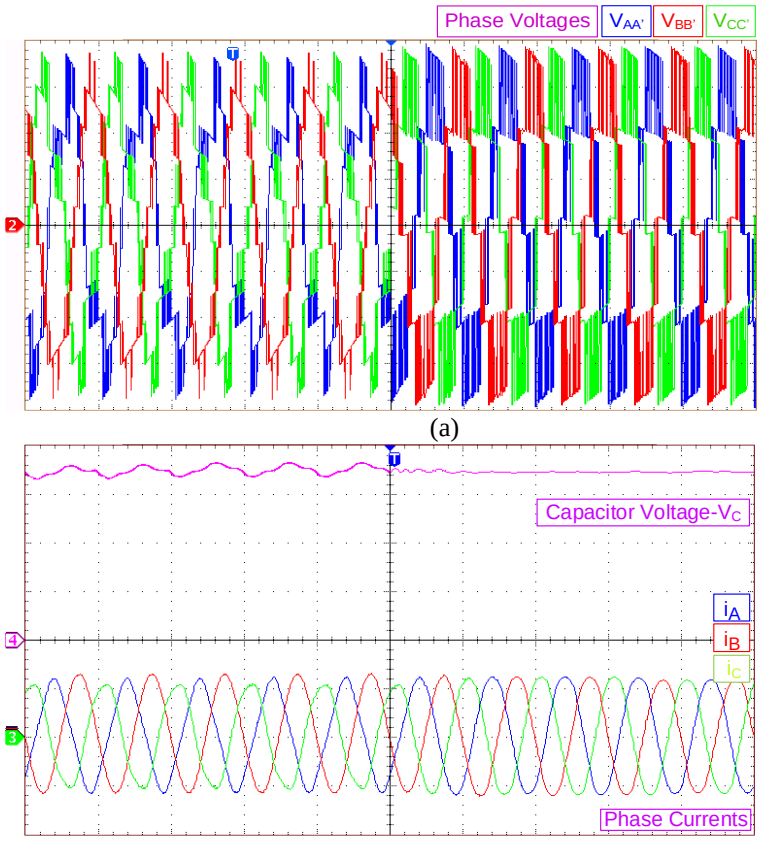


Figure 5. 11 Waveforms of (X-axis:10ms/div) (a) Three phase output voltage (Y-axis: 50V/div) (b) Capacitor voltage (Y-axis: 20V/div) and three-phase no-load currents (Y-axis: 1A/div) with MSL for S_{a7} OC.

5.7 Assessment of the proposed MLI topology

The PT is compared with conventional topologies and also with similar existing topologies feeding OEWIM drives in terms of total component count and control complexity and is illustrated in Table 5.3. From Table 5.3, it is clear that the component count for the PT are minimum and control complexity is low in comparison with other existing nine-level MLI topologies feeding OEWIM drives. Additionally to evaluate the lucrative advantage of the PT regarding inverter cost, an assessment depending on the components cost involved in the inverter

design is carried out and is presented in Table 5.4. For this assessment a case study is carried out considering a 2kW load fed with an input voltage of 200V. The component ratings are chosen according to the topology configuration considered for comparison. The cost of each component used and overall cost of the topologies under comparison are enlisted in Table-4. This evaluation gives the same significance to the total number of components, their total blocking voltage (TBV) and peak inverse voltage (PIV) while considering voltage and current ratings without any margin. On the other hand, components with lower voltage rating are selected in view of their current ratings. From Table 5.3 and Table 5.4, it is clear that the PT employs the least number of components with which the cost of the inverter and the control complexity are lowered and makes its usage viable.

Table 5.3 Comparison of the proposed topologies with existing MLI topologies feeding OEWIM drives

MLI Type	No. of Levels	No. of Switches	No. of Drivers	No. of Diodes	No. of Sources	No. of Capacitors	Component Count	Control Complexity
NPC	9	48	48	168	1	9	274	Very high
FC	9	48	48	48	1	85	230	High
CHB	9	48	48	48	12	12	168	Low
Mondal *et al.,* 2009 {A}	7	48	48	60	6	6	168	Very high
Rajeevan *et al.,* 2011 {B}	7	36	36	36	2	12	122	Low
Rajeevan *et al.,* 2013 {C}	9	36	36	36	2	12	122	Low
Wang*et al.,* 2017 {D}	9	36	36	36	1	8	117	High
Kshirsagar *et al.,* 2017 {E}	9	24	24	24	2	6	80	Very High
MHBT	9	24	24	24	3	6	81	Low
MLBBT	9	24	24	24	3	3	78	Low
FCLBT	9	24	24	24	3	3	78	Low
SCBT	9	24	24	24	3	3	78	Low
FCBT	9	24	24	24	3	1	76	Low

Table 5.4 Cost comparison of the proposed topologies with existing MLI topologies feeding OEWIM drives

Part	MOSFETs			Diodes	Capacitor		Gate Driver	Total cost ($)
Part Number	IRFP240PBF	IRFP140PBF	IRFIZ34GPBF	STPS20SM60D	LLG2D222MELC40	LLS2A222MELA	IR2110STRPBF	
Ratings	200 V, 20 A	100 V, 20 A	60 V, 20 A	60 V, 20 A	200 V, 2.2mF	100 V, 2.2mF		
Unit Cost ($)	2.1	1.93	1.28	1.24	6	3.93	3.48	
NPC	0	0	48	168	0	8	48	468.24
FC	0	0	48	0	0	84	48	558.6
CHB	0	0	48	0	0	0	48	228.48
{A}	0	0	48	12	0	6	48	266.94
{C}	0	12	12	0	0	12	36	210.96
{D}	12	12	12	0	0	6	36	212.58
{E}	0	12	12	0	2	3	24	145.83
MHBT	0	24	0	0	0	6	24	138.06
MLBBT	0	18	6	0	0	3	24	137.73
FLCBT	0	12	12	0	0	3	24	133.83
SCBT	0	18	6	0	0	3	24	137.73
FCBT	0	18	6	0	0	1	24	129.87

Based on the construction and area of application, every MLI topology exhibits certain merits and demerits. The PT suffers from some demerits such as non-modular construction compared to conventional topologies and requires three isolated DC sources. However integration of the PT with renewable energy sources such as solar photovoltaics or fuel cells will overcome this demerit. The PT also has certain advantages such as simple construction, requirement of less number of components, lower voltage rating source requirements and tolerance to switch faults. These merits make the PT find applications in medium and high power traction, industrial and electric vehicular applications.

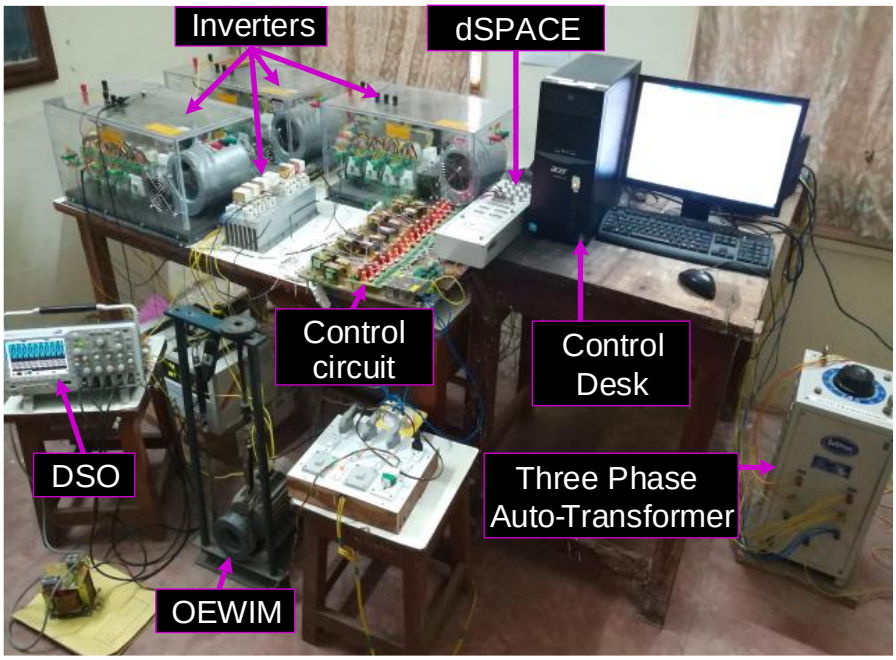


Figure 5. 12 Experimental setup

5.8 Summary

A nine-level inverter based on FCB for OEWIM drive is presented in this chapter. The PT employs three-phase VSIs, isolated dc sources and a FCB. The capacitor is charged and discharged with load current from all the three-phases to realize nine-levels in the output voltage across the phase windings of the OEWIM drive. Conventional SPWM techniques with modified reference wave and single carrier wave are employed for producing switch gate-pulses. The PT is capable of producing balanced three phase voltage across the phase windings even under switch fault conditions. A MSL is proposed for the post-fault operation of PT which ensures reliable operation without requirement of any redundant switching units. The effect of switch faults on three-phase output voltages, currents and capacitor voltage are presented. The dynamic behaviour of the PT during fault and after application of the MSL is also presented. A brief

comparison of the PT with similar existing topologies in terms of components count, control complexity and inverter cost is done which prove that the PT is cost effective with lower number of components and can be operated with reduced control complexity.

Chapter 6

Conclusion and Future Scope

Chapter 6

Conclusion and Future Scope

6.1 Introduction

In this thesis, fault-tolerant nine - level inverter topologies for OEWIM drives are presented. Conventional three-phase two-level inverter with few additional components such as bidirectional switches and capacitors are used to design these topologies. The proposed topologies are controlled with modified switching logic for operation in the post fault conditions without any need of additional hardware equipment. In this chapter, the overall conclusions are presented for this thesis work in section 6.2. The subsequent future scope of these exhibited works is discussed in section 6.3.

6.2 Conclusion

This thesis presents the research work carried out on MLI topologies for an induction motor with open-end windings. An open-end winding induction motor is realized by opening the neutral point of the stator windings of a conventional three-phase induction motor. The motor is then fed from both the ends with MLIs to witness the voltage across phase windings of the motor near to ideal sinusoidal waveform. With increase in voltage levels the harmonic performance can be improved but increase in voltage levels is associated with increase in circuit components. MLI topologies with larger number of components are not encouraged in applications in industrial and electric vehicle due to reliability issues. Hence MLI topologies with lower number of circuit components and tolerance to switch faults are required. This thesis presents five such MLI topologies for open-end winding induction motor with tolerance to possible switch faults.

A detailed background of evolution of power electronics converter and their applications in drives is discussed in chapter-1. The advantages of MLIs and need for fault tolerance for inverter switch-faults are presented. The conventional two-level and MLI topologies are detailed as well. The dual inverter configurations for induction motor with open-end windings and advantages of such topology are also highlighted. The advances in dual inverter topology for generation of higher voltage levels and fault tolerant multilevel topologies for open-end winding induction motor are presented. In addition to this, the motivation of research work on fault tolerant MLIs for OEWIM drives and thesis objectives are presented.

A modified H-Bridge based topology (MHBT) for OEWIM drive with fault-tolerance is presented in chapter-2. This MHBT is designed with conventional three-phase two-level inverter bridges with a modified-leg in each bridge. This proposed topology employs least number of components in the power circuit and is cost effective compared to other similar nine-level inverter topologies. The control technique for operation of the proposed MHBT during normal operating conditions based on conventional SPWM techniques is presented. A fault tolerant strategy is proposed for the operation of the proposed MHBT during open-circuit and short-circuit faults in various switches. The performance of the proposed MHBT is verified by performing simulation and experimentation.

A fault-tolerant inverter for OEWIM to produce output voltage with nine-levels across the phase windings is presented in chapter-2. The modified-leg H-bridges based topology (MLBBT) presented employs half the capacitors as that employed in MHBT to produce nine-level voltage across the phase windings of an OEWIM. Under normal operation and also under inverter switch-fault scenarios, the proposed MLBBT is configured to produce balanced three phase output voltage across the phase windings of the OEWIM. To produce switch gate-pulses, traditional sinusoidal pulse width modulation (SPWM) techniques like level shifted carrier in-phase disposition and phase shifted PWM techniques are used. MATLAB simulations are used to verify the proposed topology's performance, and the results are presented.

Two nine-level inverter topologies with tolerance to inverter switch-faults designed to feed OEWIM drives are presented in chapter-4. Topology-1 is a flying-capacitor leg based topology (FCLBT) and the topology-2 is a switched capacitor based topology (SCBT). The FCLBT is composed of three inverters, each of which has a single phase H-bridge connected across a dc source and one three-level flying-capacitor inverter leg. SCBT, on the other hand, is composed of three three-phase H-bridge inverters and three switched-capacitors. The operation of these proposed topologies during regular operation is shown, and switch gate-pulse generation is accomplished using conventional SPWM techniques. For operation of these topologies during inverter switch faults, a modified switching logic is presented. The proposed topologies are validated by simulation and experiment. The blocking voltage of components used in conventional topologies and different MLI topologies feeding OEWIM drives is compared with these topologies.

A fault-tolerant floating-capacitor bridge-based topology (FCBBT) for nine-level voltage generation across the phase windings of an OEWIM is presented in chapter-5. Three three-phase two-level voltage source inverters fed from isolated dc sources and a floating-

capacitor bridge make up the FCBBT. Level shifted carrier SPWM techniques are used to generate switch gate pulses. A modified switching logic is provided to enable the proposed topology to operate during inverter switch faults. The proposed topology is compared to different MLI topologies feeding OEWIM drives in terms of part count and control complexity. Experiments back up the proposed FCBBT.

At the end, it can be stated that the thesis presents fault-tolerant MLI topologies for open-end winding induction motor drives designed with fewer components.

6.3 Scope for Future Work

From the proposed inverter switch-fault tolerant topologies presented in this thesis, the scope for the future work can be stated as:

1. The proposed topologies are designed with least number of switching components, hence few redundant switches can be employed to restore rated power in post fault operation. However, care should be taken that the redundant units should be in permissible limit.
2. Reconfiguration of the proposed topologies for operation under power source failure can be investigated. Since multiple sources are employed for the proposed topologies, tolerance for the one of the source failures can be investigated. Reconfiguration of the proposed topologies for feeding continuous power to the load in the post-fault condition can be suggested.
3. The proposed configurations can be examined for switch faults in multiple locations or for complete leg faults.
4. These configurations can be extended for multi-phase induction motors drive which could ensure increased reliability of drive operation.

Appendix

Table A.1 Circuit Parameters used for simulation and experimentation

Particulars	**Value**	
Source Voltage	100V	
Flying Capacitors	1000uf	
Fundamental Frequency	50Hz	
Switching Frequency	1500Hz	
Load	Open-End Winding Induction Motor (OEWIM)	
	Specifications	3-phase, 4 Pole, 50 Hz, 400V, 1440 rpm, 1hp.
	Rated Torque	3.5 Nm
	Stator & Rotor Resistance	8.45 Ω & 7.2 Ω
	Stator & Rotor leakage Inductance	0.025 H & 0.025 H
	Mutual inductance	0.615 H
	Moment of Inertia	0.06816 kg/m^2

Table A.2 VSI Specifications

Particulars	**Value**
Make	SEMIKRON
Switch model	SKM-4M7-45A-3
Voltage rating	600 V
Current rating	75 A
DC link capacitor	2200mF, 450 V
Additional switches	
IGBT Switches - Make	SEMIKRON
Model	SKM75GB063D
Voltage rating	600 V
Current rating	75 A
Additional capacitors	1000mF, 200V.

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- Kedika Narender Reddy, Pradabane Srinivasan, “*A nine-level inverter for open ended winding induction motor drive with fault tolerance*," in the *First IEEE International Conference on Smart Technologies for Power, Energy and Control* (STPEC) 2020, VNIT, Nagpur, Sep 25-26, 2020.

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