Analytical modeling and simulation of gate material and channel engineering of DG Strained-Si MOSFET with interface charges

Submitted in partial fulfillment of the requirements
for the award of the degree of
DOCTOR OF PHILOSOPHY

by

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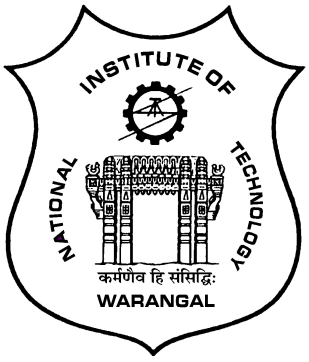

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Approval Sheet

This thesis entitled "**The analytical modeling and simulation of gate material and channel engineering of DG Strained-Si MOSFET with interface charges**" by **SUDDAPALLI SUBBA RAO** is approved for the degree of Doctor of Philosophy.

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DECLARATION

This is to certify that the work presented in the thesis entitled "**The analytical modeling and simulation of gate material and channel engineering of DG Strained-Si MOSFET with interface charges**" is a bonafide work done by me under the supervision of **Prof. N. Bheema Rao**, Professor, Department of Electronics and Communication Engineering, National Institute of Technology Warangal, India and was not submitted elsewhere for the award of any degree.

I declare that this written submission represents my ideas in my own words and where others' ideas or words have been included, I have adequately cited and referenced the original sources. I also declare that I have adhered to all principles of academic honesty and integrity and have not misrepresented or fabricated or falsified any idea / data / fact / source in my submission. I understand that any violation of the above will be a cause for disciplinary action by the Institute and can also evoke penal action from the sources which have thus not been properly cited or from whom proper permission has not been taken when needed.

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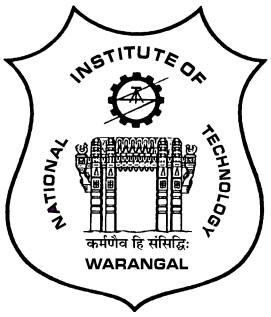

CERTIFICATE

This is to certify that the thesis entitled "**The analytical modeling and simulation of gate material and channel engineering of DG Strained-Si MOSFET with interface charges**", which is being submitted by **Mr. Suddapalli Subba Rao (Roll No: 717028)**, in partial fulfillment for the award of the degree of Doctor of Philosophy to the Department of Electronics and Communication Engineering of National Institute of Technology Warangal, is a record of bonafide research work carried out by him under my supervision and has not been submitted elsewhere for any degree.

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ABSTRACT

Non-conventional field effect transistor have captivated researchers' attention for upcoming ULSI applications as channel length of MOSFETs reached physical limit. Out of the nonconventional MOS devices that are presently being followed for the next generation ULSI, double gate (DG) strained-Silicon (s-Si) MOSFET is an important contender as the DG s-Si MOSFETs have a few unique characteristics, such as improved higher driving capability, low subthreshold current, and adaptability with CMOS technology. However, due to the high electric field in the nano-scaled device, interface charges are introduced at s-Si/SiO_2 interface. As a result, the electrical characteristics of the DG s-Si MOSFETs deteriorate due to the hot carrier effects (HCEs). Moreover, channel potential, position of minimum threshold voltage, channel potential, and subthreshold characteristics of the DG s-Si MOSFET are altered because of interface traps at s-Si/SiO_2 interface. To reduce this HCEs problem, the gate material engineering, such as dual metal gate and triple metal gate structures are incorporated into the DG s-Si MOSFET. Moreover, the lateral electric field at drain side decreases, thereby decreasing the interface charges at s-Si/SiO_2 interface. To further reduce HCEs, the channel engineering is employed into the DG s-Si MOSFET. The main objective of the thesis is to introduce with the analytical simulation and modeling of the graded channel dual material (GC-DM) DG s-Si MOSFET with interface charges with the help of the two-dimensional Poisson's equation. Moreover, analytical models are developed with the help of center potential based natural length to evaluate the exact short-channel characteristics of the MOSFET.

In this thesis, the analog/RF performance of GC-DMDG s-Si MOSFET with interface charges is presented. Besides, the analog/RF figures of merit of the proposed s-Si GC-DMDG MOSFET, including the intrinsic voltage gain, transconductance generation factor, early voltage, unity-current gain frequency, transconductance frequency product, gainâĂŞfrequency product, and gain transconductance frequency product, are evaluated for different values of device parameters. Also, the analog/RF performance of the proposed GCGS-TMDG s-Si MOSFET is further improved by employing the gate stack with high-k dielectric material and triple material gate engineering. Furthermore, variability analysis of GC-DMDG s-Si MOSFET with fixed charges is thoroughly analyzed. By varying the different device parameters, the variability analysis of the proposed GCDM-DG s-Si MOSFET is performed with respect to variations in threshold voltage and drain current while considering the line edge roughness and fluctuations in random dopant, contact resistance, and oxide thickness. And also, the performance of CMOS inverter using GC-DMDG s-Si MOSFET is evaluated for different device parameters. It is investigated that the proposed GC-DMDG s-Si MOSFET has better noise margin than GC-DG

s-Si MOSFET. The proposed analytical models are verified against numerical results obtained from TCAD simulations obtained from Sentaurus, which is a device simulator from Synopsys.

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List of Abbreviations

2D	Two Dimensional
BJT	Bipolar junction transistor
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central processing Unit
DIBL	Drain-induced barrier-lowering
DMG	Dual-metal-gate
FD	Fully-depleted
FOM	Figure of merit
Ge	Germanium
HCEs	Hot-carrier effects
IC	Integrated Circuit
ITRS	International Technology Roadmap for Semiconductors
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MuGFETs	Multi-gate field effect transistors
nMOSFET	n-channel MOSFET
pMOSFET	p-channel MOSFET
PD	Partially-depleted
QMEs	Quantum mechanical effects
RF	Radio Frequency
SCEs	Short-channel effects
Si	Silicon
SOI	Silicon-on-insulator
s-Si	Strained-silicon
SoC	System On-Chip
VLSI	Very large scale integration
ULSI	Ultra-large scale integration
UTB	Ultra-thin body

List of Symbols

ϵ_{Si}	Permittivity of Si (F cm^{-1})
ϵ_{ox}	Permittivity of SiO_2 (F cm^{-1})
t_{s-Si}	Strained-Silicon channel thickness (nm)
t_{ox}	Oxide thickness (nm)
L	Channel length (nm)
q	Charge of electron ($1.6e^{-19}$ C)
Na	Acceptor doping concentration of channel (cm^{-3})
Nsd	Source/drain doping concentration (cm^{-3})
V_{fb}	Flat-band voltage (V)
χ_{Si}	Electron affinity of Si (eV)
E_g	Silicon energy band gap (eV)
$N_{V,s-Si}$	Density of states in the valence band of s-Si
$m^*_{h,s-Si}$	Hole effective masses of s-Si
V_T	Thermal voltage (V)
ni	Intrinsic carrier density (cm^{-3})
$\psi_{cr}(x))$	Center channel potential (V)
m	Ge mole fraction
V_{GS}	Gate to source voltage (V)
V_{DS}	Drain to source voltage (V)
N_f	Interface charge density (cm^{-2})
$V_{bi,s-Si}$	Built in voltage of s-Si (V)
k	Boltzmann's constant ($1.38e^{-23}$ JK^{-1})
T	Temperature (300K)
C_{gg}	Total gate capacitance (fF)
V_{th}	Threshold voltage (V)
x_{min}	Minimum channel potential (V)
E	Electric field (V cm^{-3})
SS	Subthreshold swing (mV/Dec.)
μ	Mobility of the free carrier (cm^2 V^{-1} sec^{-1})
λ	Natural length
V_{th}	Threshold Voltage
$J_n(y)$	Current density (A/μm)

Chapter 1

Introduction

1.1 Overview

The semiconductor manufacturing company has been playing a major role in digital world since 1970 and is one of the world's big companies. The development of semiconductor company has not been uniform but has a enormous influence on other companies such as smart homes, communication, security, transportation, surveillance, health care, etc. Such a remarkable growth was not at all seen earlier in any industry in the past. World semiconductor commerce census predict its worldwide semiconductor trading as $440 billion in 2020, which is 6.8% more than the sales in 2019. Semiconductor materials, which have electrical conductivity that lies in between conductivity of conductors and insulators, are categorized into extrinsic (impure) and intrinsic (pure) semiconductors. Moreover, a few pure elements and various compounds show semiconductor characteristics of germanium, silicon, and compounds of gallium, which are most frequently utilized in electronic components. Besides, based on type of impurity, impure materials are classified into p-type and n-type semiconductors. Applications of semiconductors have been growing gradually from radio to almost each electronic component that has controlled switch. Semiconductor components are extensively studied to achieve better performance in terms of low power consumption, high speed, high efficiency, and small area with good functionality. The continual requirement of performance enhancement has the inspiring drive behind the investigation of advanced semiconductor MOSFETs and drive this area truly interesting also difficult.

1.2 History of Transistors

In 1940s, the transistor was invented and is a semiconductor component it can switch or strengthen the electrical signals [1]. The vacuum tubes transformed the domain of electronic components and give rise to portable and cost effective computers, calculators, and radios. The concept of field-effect component was demonstrated in 1926 [2]. In 1952, junction field-effect transistor was proposed based on the unipolar concept with three electrodes by Shockley [3]. In 1960, the most essential unipolar component, which was called as the metal oxide semiconductor field effect transistor (MOSFET) has four electrodes adding a body to handle the electrical characteristics more effective manner[4]. However, for most of the analog circuits, the BJT has been transistor of choice even after the invention of MOSFET, since it has better driving capability and ease of process flow.

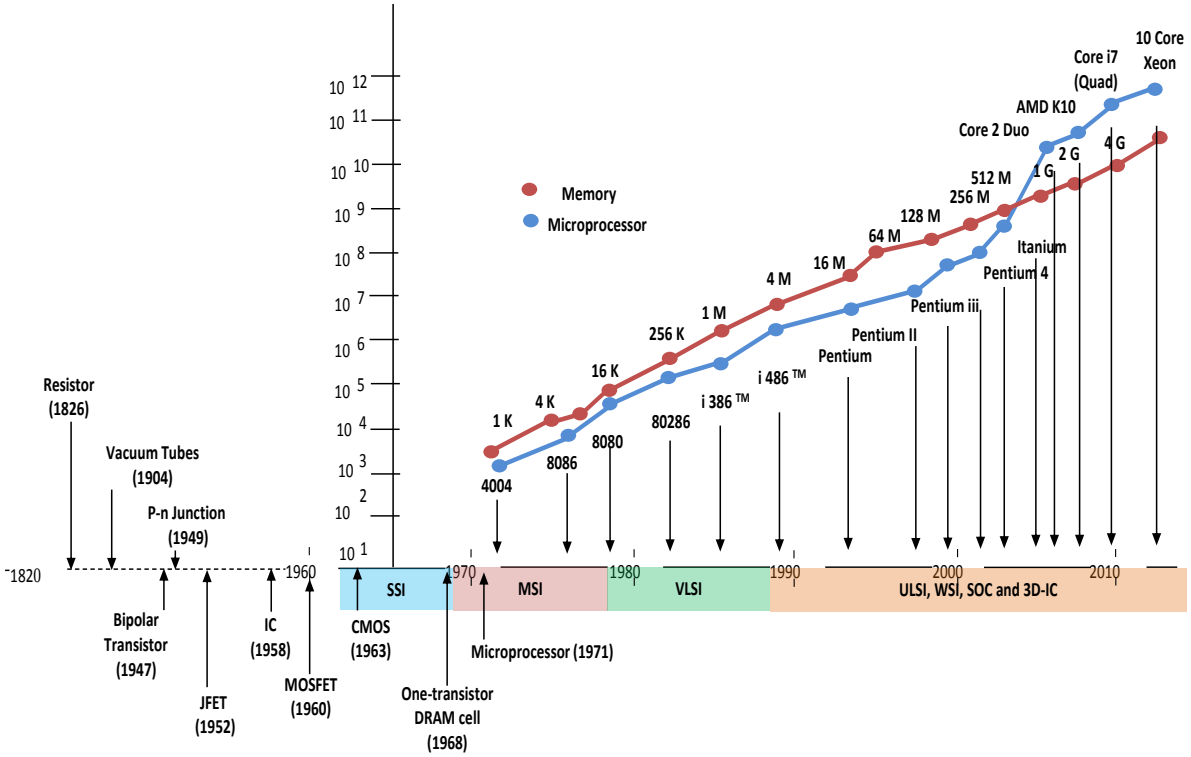

Figure 1.1: A brief time line of the important events in the advancement of Semiconductor technology

In 1957, proposed an integrated circuit (IC) that comprises of resistors, capacitors, and transistors [5]. The major milestone in the enhancement of integration onto the semiconductor chip, which is a complementary metal oxide semiconductor (CMOS) technology, was marked in 1963. With the help of CMOS process, researchers have capable to integrate thousands of billions of devices on a substrate. Nowadays, the CMOS technology has become the most used technology in semiconductor industry and is used for the fabrication of micro-controllers,

memories, and other analog (digital) circuits due to high packing density. Fig. 1.1 shows the important milestones in the development of semiconductor industry. Moore's law states that number of devices per square inch on the IC double in each 18 months [6]. In semiconductor industry, two major milestones are noticed in 1989 and 2005. In 1989, the million and billion devices were integrated onto a semiconductor wafer. In 2005, ultra large scale integration (ULSI) was possible due to the MOSFET scaling and advanced semiconductor manufacturing process.

1.3 MOSFET Scaling

The electronic industry has been extremely benefiting from scaling down the dimensions of MOSFET for the last four decades. The shrinking of MOSFETs to sub-nano meter scale enables integration of the billions of the components on a small substrate area. Initially, the constant electric field scaling theory was introduced in 1974 [7]. In this theory, the scaling was done to the dimensions and voltage of the device with same scaling factor S while keeping electric field constant. Hence, the speed of device increases by a factor S and the power dissipation of the device decreases by a factor of S^2. The other major scaling is constant voltage scaling. In this theory, the operating voltage of the device is unchanged and scaling is applied to all other parameters of the device.

In 2015, International Technology Roadmap for Semiconductors (ITRS) presented that the scaling of the MOSFET more Moore beyond CMOS technology node could be a challenging task since the planar MOSFET has already reached its scaling limit [8]. Moreover, more Moore beyond CMOS Further continuing the scaling of MOSFETs leads to high hot carrier effects (HCEs) and short channel effects (SCEs) such as subthreshold swing, drain induced barrier lowering (DIBL), threshold voltage roll-off, and interface charges [9]. Hence, the performance of MOSFET deteriorates in terms of leakage current, non ideal switching characteristics, and power dissipation. Therefore, the elimination of HCEs and SCEs till allowable amount is of importance in device scaling. To further continue the MOSFET scaling in sub 30 nm, we need to come up with novel device structures and new materials (i.e., CMOS technology boosters).

1.4 CMOS boosters

As explained in preceding section, a major challenging task in nano-scaled CMOS scaling is eliminating the SCEs and HCEs. To suppress SCEs and HCEs, CMOS boosters are incorporated into the nano-scaled device. They are strained-silicon (s-Si), channel engineering, gate material engineering, high-k dielectric material, non-conventional MOSFET structures, etc. Some of them are illustrated below.

1.4.1 Strained-silicon material

Traditionally, s-Si layer is included for its advantageous characteristics such as enhanced carrier mobility, overshoot of carrier velocity, and high ON current [10]-[12]. With the help of layer transfer technique [13], biaxial-tensile strain is induced in Silicon material by developing the Silicon material over a $Si_{1-X}Ge_X$ buffer material with bigger in plane lattice constant than the Silicon material, which is grown on silicon on insulator (SOI) body. Later, by selective etching process, the s-Si layer is transferred on the surface of the SOI substrate by removing the $Si_{1-X}Ge_X$ layer. However, the removal of $Si_{1-X}Ge_X$ layer does not change the amount of strain in Silicon material [14]. Consequentially, the strain in Silicon material turns out to be a function of X (X is a Germanium mole fraction in Silicon material) of the relaxed $Si_{1-X}Ge_X$, as observed in the Silicon material that is directly grown on the $Si_{1-X}Ge_X$ interface.

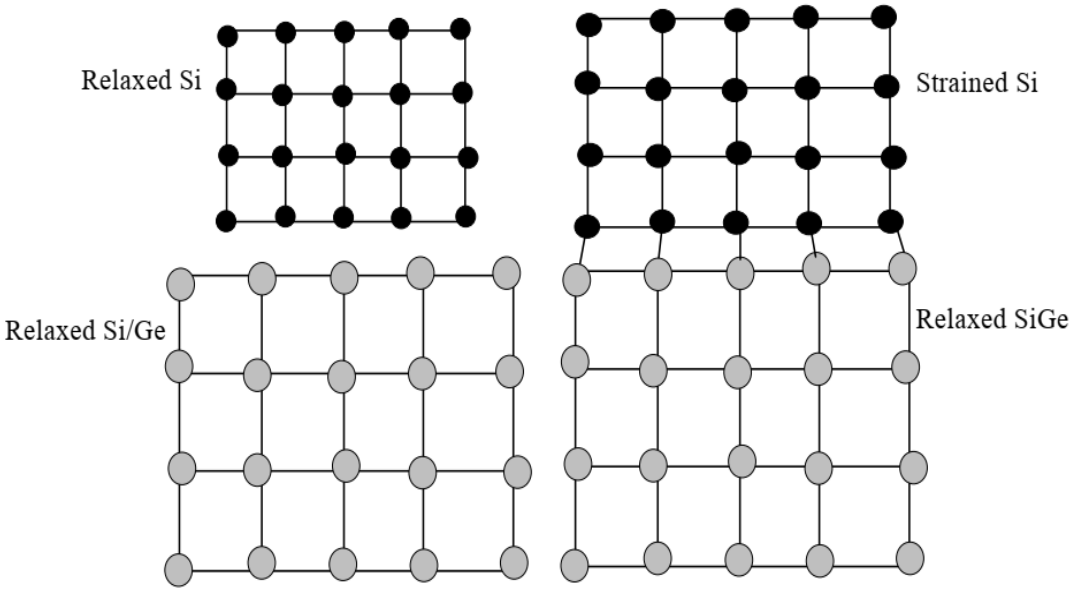

Figure 1.2: Lattice structure of relaxed silicon, relaxed SiGe, and s-Si on relaxed SiGe

1.4.2 Gate material engineering

Dual-Metal-Gate (DMG) structure, which is one of the notable CMOS technology boosters, was proposed by Long et al. [15]. The gate material of the DMG MOSFET consists of control gate work function is ϕ_{m1} and screen gate work function is ϕ_{m2}. $\phi_{m1} > \phi_{m2}$ for n-type device, and vice versa for p-type device. Consequently, the step-equivalent curve is attained in the channel potential. When device operates in the saturation region, the channel region under control gate layer is screened from a drain to source voltage (V_{ds}) as the channel region under screening gate layer absorbs any excess V_{ds}. Therefore, the SCEs and HCEs of the MOSFET are suppressed by employing DMG structure.

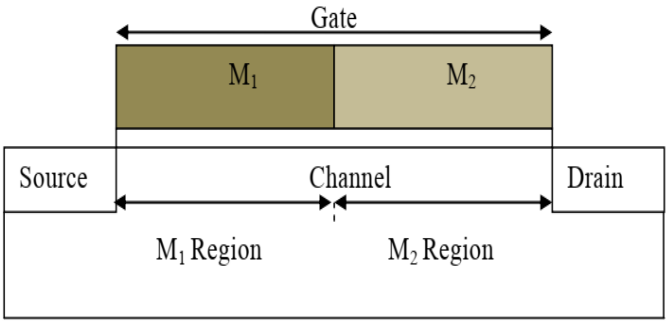

Figure 1.3: 2-D diagram of DMG structure of MOSFET.

1.4.3 Graded channel engineering

If the doping profile in the Silicon channel decreases uniformly in a stepwise manner from the source/channel interface to the drain/channel interface then it is considered as graded-channel (GC) structure [16]. By employing GC structure in the MOSFET, high threshold voltages and low SCEs are obtained. Moreover, the HCEs are also reduced due to the lower built-in potential at the drain/channel interface.

1.4.4 High-k insulating material

In a process of scaling CMOS devices, the thickness of the dielectric material has reached 10 Angstrom. With the reduction of channel length below 32 nm, the gate dielectric thickness has to be scaled down to an ultra-thin size (i.e., less than 1 nm approximately, which is equivalent to five atomic layers). This very thin dielectric layer results in a huge amount of OFF current, thereby increasing the standby power consumption. Therefore, a need of thick dielectric material is required in order to prevent electrons tunneling through gate oxide [17],

i.e., the physical thickness of the dielectric material has to be high, whereas its electrical thickness has to be low. Hence, high-k dielectric materials could be one of the best solutions for the issues discussed. The effective oxide thickness of the high-k dielectric material is given as $t_{eff} = t_{high-k}\frac{\epsilon_{SiO_2}}{\epsilon_{high-k}}$, where ϵ_{SiO_2} and ϵ_{high-k} are permittivities of silicon dioxide material and high-k dielectric layer, respectively. t_{high-k} is thickness of high-k dielectric layer. Researchers have found a few suitable high-k dielectric materials, such as HfO_2, ZrO_2, and Ta_2O_5 to suppress the SCEs and gate tunneling current simultaneously.

1.4.5 Non-conventional MOSFETs

The multiple-gate (MuG) MOSFETs are categorized as the double gate (DG) conventional SOI MOSFET, DG non-conventional FinFET, Tri-gate MOSFET, Quadruple Gate MOSFET, surrounding gate MOSFET, and Nanowire MOSFET. The MuG-MOSFET structures can have high gate control over the silicon channel [18]. Consequently, reduction of leakage current and SCEs of the device can be attained. Nevertheless, several process flow issues of MuG-MOSFETs must be resolved before using the MuG-MOSFETs in VLSI systems. Moreover, MuG-MOSFETs require modern fabrication methods such as enhanced etching accuracy, corner effects, reliability, and ultra-thin fin effects, etc.

1.5 Motivation

In nano-scaled regime, DG s-Si MOSFETs suffer from SCEs and HCEs. To suppress SCEs and HCEs, both DMG with GC engineering and gate stack structure are employed in DG s-Si MOSFET. In the light of above discussion, an effort is done to investigate the subthreshold performance of DG s-Si MOSFET. Therefore, theoretical models of the subthreshold characteristics are developed for DG s-Si MOSFET. Moreover, the effect of various device parameters on the subthreshold characteristics of DG s-Si MOSFET is investigated using the derived theoretical models. Besides, CMOS technology boosters like DMG with GC engineering and high-k dielectric material help to enhance ON current of DG s-Si MOSFET. Therefore, these techniques are employed in the DG s-Si MOSFET to examine their effects on subthreshold behavior of the MOSFET.

1.6 Problem statement

The aim of this thesis is to introduce a comprehensive simulation and modeling based investigation on subthreshold performance of DG s-Si MOSFET with interface charges, including the CMOS technology boosters such as DMG with GC engineering and high-k dielectric material.

1.7 Objectives

- Modeling of center potential and threshold voltage of GC-DMDG s-Si MOSFET with interface charges
- Modeling of sub-threshold current and swing of GC-DMDG s-Si MOSFET with interface charges
- Analog/RF performance of GC-DMDG s-Si MOSFET with interface charges
- Variability analysis of GC-DMDG s-Si MOSFET with interface charges
- Analog/RF performance of GCGS-TMDG s-Si MOSFET with interface charges

1.8 Organization of Work

The main aim of this thesis is to demonstrate a exhaustive modeling and the simulation based analysis of the subthreshold performance of DG s-Si MOSFET with interface charges including the CMOS technology boosters. The thesis comprises six chapters containing the present Chapter. The contents of other chapters of the thesis are outlined as follows:
Chapter 2 reviews the notable amount of most updated literature of the modeling and simulation of DG MOSFET and DG s-Si MOSFET with interface charges in detail.
Chapter 3 deals with the analytical simulation and modeling of subthreshold characteristics of GC-DMDG s-Si MOSFET with interface charges.
Chapter 4 presents a detailed analysis of analog/RF performance evaluation of GC-DMDG s-Si MOSFET and GCGS-TMDG s-Si MOSFET with interface charges.
Chapter 5 presents a detailed study of variability analysis of GC-DMDG s-Si MOSFET with interface charges and CMOS inverter's performance.
Chapter 6 review the work done in thesis and provides some direction for the upcoming work.

Chapter 2

Literature Survey

2.1 Introduction

MOSFET miniaturization has several advantages, such as high switching speed, high density, good functionality and low cost of microprocessors. However, the problems related with miniaturization of the planar MOS transistors increase as the transistor density in ICs increases. The CMOS boosters, which have already been discussed in Chapter 1, are extremely helpful to address the issues related with miniaturization. Also, double gate s-Si device is one of the MOSFETs that are scaled down to the higher degree compared to the conventional device due to their reduced SCEs. However, when DG s-Si MOSFET is scaled down to nano-scaled regime, it still exhibits HCEs and SCEs. In order to reduce these effects, gate and channel engineering techniques are applied to DG s-Si MOSFET.

The objective of this thesis is to carry out the two dimensional (2-D) modeling and simulation of sub-threshold analysis of proposed DG s-Si device structures. As the upcoming research methods in any domain could be estimated with the help of detailed study of the up to date research in a specific domain of interest, this chapter is devoted to describe a thorough review of the up to date work on different features of DG s-Si MOSFETs and gate and channel engineering of DG s-Si MOSFETs to verify the scope of thesis mentioned in previous chapter.

2.2 Review on strained-silicon MOSFETs

strained-silicon MOSFETs have been reported by many researchers due to their better performance over conventional Si MOSFETs [19]-[26].

In [27], utilizing the exact solution of 2-D Poisson's equation, surface potential, subthreshold current, threshold voltage, and subthreshold swing have been modeled for gate stack DG s-Si MOSFETs. In addition this, it not only provides the physical perspective into MOSFET physics but also offers the simple designing method of further immunity of SCEs of CMOS based MOSFET in the nanoscale regime.

In [28], with the help of 2-D simulation, the effect of the strain in the conduction path of cylindrical s-Si MOSFETs was demonstrated. For low values of the strain, the conduction path is created in center of the cylindrical SiGe pillar and there is no conduction path at s-Si layer surface. However, for large values of strain, the conduction path obtains in s-Si layer, thereby enabling the benefit of mobility improvement of carriers in MOSFET operation.

In [29], ultralow on-resistance s-Si-on-insulator lateral double-diffused MOSFET with silicon-germanium and trench gate was presented. In OFF state, both trench gate and P-top layer help in depleting N-drift region, which turns to an allowable heavily doped N-type drift region. Furthermore, the improved electric field in trench oxide increases the breakdown voltage.

In [30], the BSIM3 model was developed for biaxially strained p-MOSFETs with the help of a suitable parameter extraction technique. The obtained model parameters were calibrated by comparing the results with numerical TCAD simulations and a basic analytical model. The mean error in the alternating current and direct current characteristics of a model were predicted to be less than 1.5%.

In [31], the impact of uniaxial-strain on energy band structure, mobility of a carrier, effective masses of carrier, density of states, and high-field saturation on the ON current, leakage current and switching speed in nano-scale, Silicon and Germanium, DG p-MOSFETs were exhaustively investigated.

2.2.1 Review on s-Si MOSFETs with interface charges

The electric field in nano-scaled MOSFET introduces trap charges at the Si/SiO_2 region, which degrade the electrical behavior of s-Si MOSFET due to HCEs. Thereby, the damaged region at Si/SiO_2 interface of the DG MOSFET is expanded from drain end to source end with interface charges owing to HCEs. Until now, so many researchers have explored HCEs in the DG MOSFETs [32], [33], which are attributed to the electron type (acceptor) or hole type (donor) trap generation at Si/SiO_2 region can be transformed into the corresponding interface trap charges (positive or negative localized charges).

In [34], a surface potential model was presented for s-Si on Silicon-Germanium MOSFET with interface charges. The 2-D Poisson's equation was solved in damaged and undamaged s-Si regions to get the surface potential of the channel. The impacts of different values of damaged length and interface charges on channel potential were presented in detail. The channel potential dependency on the effect of strain was also investigated.

In [35], a surface potential based threshold voltage model for performance analysis of gate stack dual-metal-insulated-gate source-engineered fully-depleted (FD) SOI MOSFET was demonstrated. Also, the parametric investigation was done to optimize the MOSFET dimensions for enhanced nanoscaled MOS design. Furthermore, a six transistor SRAM cell was developed using gate stack dual-metal-insulated-gate source-engineered FD SOI MOSFET and static noise margin was calculated.

In [36], the effects of oxide charges induced by various SOI thicknesses on the performance and reliability of a strained SOI device with SiN-capped contact etch stop layer were presented. Compared to thick thickness of SOI MOSFET, the thin thickness of SOI MOSFET with high strain contact etch stop layer possesses higher interface trap density, thereby degrading the MOSFET performance.

In [37], the border trap characterization of $TaN/HfO_2/Si$ and $TaN/HfO_2/s\text{-}Si/Si_{0.8}Ge_{0.2}$ MOSFET was illustrated. Drain current hysteresis technique was used to obtain the border traps. It is noticed that border traps are greater in the case of high-k films on $s\text{-}Si/Si_{0.8}Ge_{0.2}$.

In [38], the impacts of silicon back trap state density between silicon channel and buried oxide layer on memory characteristics were presented. The back trap states of FD strained SOI substrate were deliberately obtained by varying the temperature of rapid thermal annealing method and the value of back trap was estimated with the help of back gated MOSFET method.

In [39], a 2-D threshold voltage analytical model of a DMG FD strained SOI MOSFET was developed by employing the interface charge effects. The presented threshold voltage model includes both positive and negative trap charges. Finally, the analytical model was validated with 2-D numerical device simulator.

2.2.2 Review on gate stack and gate engineering of s-Si MOSFETs

The dual metal gate structure was introduced in DG MOSFETs to suppress the HCEs and to further increase the immunity against SCEs [40]-[42]. Which has the control gate (source end) having greater work-function than at the screening gate (drain end). Consequently, the step-equivalent curve is attained in the channel potential. After the saturation region, the channel region under control gate layer is screened from the V_{ds} as the channel region under screening gate layer absorbs any excess V_{ds}. Therefore, the SCEs of DG MOSFET are suppressed by employing DMG structure [43]. Moreover, this gate engineering increases the average electric field in the channel due to the reduced peak electric field at the drain end in turn reducing the HCEs.

The triple material gate (TMG) engineering is incorporated by few authors in DG MOSFET to reduce the HCEs and SCEs [44]-[45]. Where TMG structure has three different work functions used for control and screen gates. Hence, a step profile in the channel potential is attained and the improved average electric field in the channel.

In [46], the impact of strain on a linearly graded work-function engineered surrounding gate MOSFET was demonstrated. From the result analysis, it is noticed that the inclusion of strain shifts the minimum channel potential toward the source side, which in-turn gives a shielding to the drain voltage. Moreover, it is observed that linearly graded gate has better performance compared to the single metal gate in low power applications.

High-k dielectric with SiO_2 used as gate stack (GS) is employed in DG MOSFET, so enhanced sub-threshold characteristics are attained due to the reduction in the gate leakage current of DG MOSFET. In [47], the transconductance of the s-Si p-MOSFETs with high-k dielectric material as gate oxide was estimated. Moreover, transconductance improvement factors of 2.73 and 2.97 are noticed for s-Si p-type MOSFETs in comparison with conventional Si p-type MOSFETs with high-k and SiO_2 dielectric materials, respectively. The transconductance of s-Si MOSFET at low temperature was also simulated.

In [48], a theoretical model to present the s-Si nanoscale DG MOSFET along with high-k dielectric material was proposed. By including the effects of s-Si and high-k dielectrics in devices, alteration of energy band diagram and increase in conduction band offset are noticed. The mobility can also be enhanced while maintaining the effective gate control.

In [49], SCEs of high-k GS dual material tri-gate s-Si-on-nothing MOSFET with dual material bottom gate were demonstrated. Moreover, the channel potential of the MOSFET was derived along with its electric field and threshold voltage. The effect of the MOSFET performance owing to the varying of various MOSFET parameters was also discussed.

In [50], the 2-D analytical modeling of high-k triple material gate stack DG s-Si on nothing MOSFET with a ion-implanted doping profile was proposed. The surface potential was developed by using the 2-D Poisson's equation and including the parabolic channel potential approximation. The threshold voltage and electric field were also derived for the device. Besides, comprehensive studies of the MOSFET response regarding the different SCEs were also presented.

In [51], strained SiGe p-MOSFETs with high-k dielectric were fabricated and characterized. The s-Si/s-$Si_{0.5}Ge_{0.5}$/strained SOI heterostructure MOSFETs offer good transfer and output characteristics with an ON and OFF current ratios of 105. The obtained hole mobility exhibits an improvement of about 2.5 times over Silicon hole mobility and no deterioration in hole mobility compared to SiO_2 or even HfO_2 gate dielectric MOSFETs.

2.2.3 Review on channel engineering of s-Si MOSFETs

Lateral graded channel engineering have been used in DG MOSFETs to achieve higher threshold voltage and decreased SCEs [52]-[54]. In GC structure, doping profile in the Silicon channel decreases from the source/channel interface to drain/channel interface. Besides, the peak electric field at drain side is reduced due to the lower built-in potential at drain/channel interface, thereby reducing the HCEs through lateral GC engineering.

In [55], an asymmetric DG single halo doped SOI MOSFET were investigated theoretically and compared with an asymmetric DG SOI MOSFET. The 2-D simulation studies illustrate that the inclusion of single halo in the DG structure results in reduced DIBL, threshold voltage roll-up, kink free in output characteristics, high output resistance and higher breakdown voltage when compared to simple DG structure. Moreover, the incorporation of single halo in

DG MOSFET results in step like potential profile, which screens the channel potential at source side from the drain voltage.

2.3 Review on DG MOSFETs

So far, many analytical models have been reported on DG MOSFETs with high transconductance and double drive current. Here, a higher degree of gate control over channel than drain reduces the SCEs [56, 57].

In [56], a 2-D analytical model for electrostatic potential was developed for undoped DG MOSFETs. The threshold voltage roll-off, subthreshold current and swing of DG MOSFETs are in good agreement with the TCAD simulation results. Besides, this model not only provides useful physics related to SCEs but is also used as basis for compact modeling of the DG MOSFETs.

In [57], an analytical model of threshold voltage for DG MOSFETs with fixed charges was developed. With the aid of 2-D Poisson's equation and parabolic potential approximation, threshold voltage model for device was derived. Moreover, it can be helpful to estimate hot carrier induced MOSFET deterioration for different MOSFET dimensions.

In [58], deterioration in the performance of the device due to HCEs in nano-scale DG MOSFETs was noticed. Besides, the hot carrier degradation effects on threshold voltage, surface potential, and DIBL of DG MOSFETs were also investigated. It is also observed that the deterioration in the performance of device becomes severe when the channel length decreases and the position of minimum channel potential is affected by the localized charge density.

In [59], a surface potential model of DMG MOSFETs by considering a channel depletion layer and depletion layers around the source (drain) junctions was developed. It can also be used in current models to estimate the subthreshold current.

In [60], based on the 2-D Poisson's equation, a subthreshold model consists of channel potential, threshold voltage, and subthreshold swing for the short-channel asymmetrical DMDG MOSFETs was presented. To reduce the SCEs, the MOSFET parameters such as thin substrate, thin oxide, and high ratio of control to screen gate are preferred.

2.4 Review on multiple gate MOSFETs

The electrostatic control of double and triple-gate devices can be enhanced by expanding the sidewall regions of the gate terminal to some level in buried oxide and bottom channel region. From an electrostatic perspective, the triple-gate and omega-gate MOSFETs comprise three and four gates, respectively. Furthermore, the electrostatic control can be improved by the surrounding-gate device. The surrounding-gate MOSFET was fabricated by wrapping a gate terminal around a silicon substrate [61].

In [62], multiple-gate (MG) MOSFETs with short channel length are evaluated using device Monte Carlo simulation. From the result analysis, the DG MOSFET has higher current drive capability and less leakage current than non-planar devices. However, source and drain regions have to be cautiously scaled to get optimal values of resistance and fringe capacitance.

In [63], the analytical modeling and simulation of output characteristics, transconductance, and output conductance of dual metal quadruple gate MOSFET were presented by changing the ratios of gate length and work function. Moreover, it is noticed that the better performance of a fixed channel length device can be attained by maintaining the length of control gate higher than the screen gate.

In [64], analytical model for the capacitance-voltage (C-V) characteristics of s-Si gate all around MOSFETs for different operating regions was developed. The effects of MOSFET dimensions, doping concentration, fixed charges, and strain on C-V characteristics of S-Si gate all around (GAA) MOSFETs were investigated. It is noticed that the proposed device performance becomes better by employing high-k dielectrics.

In [65], the authors presented the electrothermal characterization of various nanoscale MG MOSFETs, such as quadruple-gate, π-gate, and ω-gate MOSFETs. Moreover, the temperature profile of a ω-gate device with GC width was also investigated. Finite difference method was used to solve the 3-D time-dependent heat conduction equations. Besides, the transient temperature characteristics of MG MOSFETs were also studied.

2.5 Review on subthreshold characteristics models of DG s-Si MOSFETs

Till now, so many researchers have developed the different models to attain subthreshold performance of SOI and DG MOSFETs [66]-[68].

[69], a 2-D surface potential model for a FD DG s-Si MOSFET with interface charges was developed. The interface charges in the damage region owing to the HCE is a common phenomenon in short-channel MOSFETs. The developed analytical model contains effect of both negative and positive fixed charges. The effects of fixed charge density with damaged length and strain on the surface potential were examined comprehensively.

[70], a threshold voltage model of undoped DG MOSFET interface charges near the drain end was illustrated. In subthreshold region, the analytical model was developed based on solution of the potential distribution in the channel. Moreover, both the surface potential and threshold voltage models are in good agreement with the Atlas simulation results for different interface charge density with damaged lengths.

In [68], the substrate bias voltage dependent three dimensional subthreshold models of threshold voltage, channel potential, DIBL, current, and subthreshold swing of tri-gate SOI MOSFETs were developed. Moreover, a three dimensional approach had been used to derive the minimum of potential, which was later used to derive models of various device parameters.

In [52], the GC GS DG MOSFET was examined in view of improving device characteristics and immunity to SCEs. The MOSFET has a advantage of enhanced gate-oxide reliability, reduced parasitic bipolar-effect, improved cut off frequency and lower DIBL.

In [71], a 2-D subthreshold model was presented for a GC DG FD-SOI MOSFET, including the gate misalignment effect. The conformal mapping conversion method was used to give an accurate estimation of electric field, surface potential, and subthreshold behavior of the MOSFET by employing the gate misalignment effects on both drain and source side.

2.5.1 Review on threshold voltage models of DG s-Si MOSFETs

In [72], a analytical model for threshold voltage of nano-scale s-Si on insulator and s-Si on SiGe on insulator MOSFETs was presented. Moreover, this model considers the effects of strain and different device parameters. It can also be used to estimate the DIBL effects.

To model the threshold voltage for s-Si MOSFETs analytically, the authors developed a surface potential based the threshold voltage model of single-layer FD s-Si on insulator MOSFETs [73]. In this model, the effects of MOSFET parameters such as strain, SCEs, gate work function, s-Si thin film doping and thickness on threshold voltage were demonstrated. This model offers reduction in threshold voltage by increasing the strain and s-Si thickness.

In [74], the authors presented surface potential based analytical model of the threshold voltage for s-Si on Si-Ge On-Insulator MOSFET with localized charges using 2-D Poisson's equation. Moreover, the effects of strain and positive/negative interface charge on surface potential and threshold voltage were demonstrated. Besides, deterioration in the performance of the device due to hot carriers was discussed for different device dimensions and charge profiles.

In [75], the surface potential based threshold voltage model of s-Si dual material DG MOSFETs with vertical-gaussian doped channel was developed. The effects of strain and gaussian profile parameters on surface potential, threshold voltage, and lateral electric field were presented.

In [16], the authors proposed the surface potential based threshold voltage model for graded channel-dual material DG (GC-DMDG) MOSFET. Moreover, SCEs of the device were analyzed using the surface potential based natural length. Further, in [16], although the model provided effective results, it failed to estimate short channel behavior of the device accurately. In fact for short channel symmetrical DG MOSFET, the leakage path is created early at the center rather than surface of the channel [76]. Thus, SCEs are accurately estimated by center potential based natural length than surface potential.

2.5.2 Review on subthreshold current models of DG s-Si MOSFETs

In [66], surface potential based models of subthreshold current (SC) and subthreshold swing (SS) of the s-Si on silicon germanium on insulator MOSFETs were developed. The subthreshold performance was evaluated by varying the different device parameters.

In [67], a physics based compact SC model of nano-scale DG MOSFETs was demonstrated. The channel potential was developed with the help of conformal mapping method and parabolic approximations. In the proposed model, the electrostatics are influenced by capacitive coupling between the body electrodes that are considered in subthreshold region.

In [77], the authors presented a 2-D analytical model of asymmetric 4T and 3T DG MOSFETs to evaluate the subthreshold performance. In the proposed model, it is observed that there is a change in position of charge centroid with respect to a difference in the front/back gate bias. The subthreshold behavior with asymmetry in the gate voltage, oxide thickness, and work function was presented. Also, a model for the subthreshold characteristics of 3T DG MOSFETs was demonstrated.

In [78], 2-D analytical models of the SC and SS of gaussian doped s-Si double-material double-gate (DMDG) MOSFET were presented. The SS and SC of device were optimized by selecting the projected range/straggle parameter value. Moreover, Gaussian doping profile offers an advantage of gaining better control on the subthreshold performance of the MOSFET with out altering the geometry of device.

In [79], a subthreshold current model of FD asymmetrical DG MOSFETs was developed. Moreover, the variations in subthreshold performance owing to structure's asymmetry such as difference in oxide thickness or bias voltage between front and back gate were presented.

2.5.3 Review on subthreshold swing models of DG s-Si MOSFETs

In [80], the authors presented a 2-D analytical model to analyze the channel conductance and subthreshold swing of a channel and gate engineered DG MOSFET. Here, the diffusion equation was considered to to derive the drain to source current of the MOSFET in subthreshold region. Variations in subthreshold swing of the MOSFET for different materials, and oxide layer thickness were also presented.

In [81], physics based models of threshold voltage with the DIBL and subthreshold swing of undoped DG MOSFETs were developed. These models were obtained from a solution of 2-D Poisson's equation by considering a electron concentration.

In [82], the subthreshold characteristics of GC-DMDG MOSFET were analyzed with the help of analytical models of SC and SS. The variations in SS against various MOSFET parameters were observed with the aid of effective-conduction path parameter. The SC and SS of the

GC-DMDG MOSFET offers better performance when compared to a dual-material double-gate and GC DG MOSFETs.

In [45], analytical models of SC and SS of triple material DG MOSFET were presented. Both diffusion and drift components of current densities were included for modeling of SC. Virtual cathode idea of DG MOSFETs was employed to model a SS of triple material DG MOSFETs. The dependencies of SC and SS on various device dimensions were explored.

In [83], the surface potential based 2-D analytical models of SC and SS DMG s-Si on SGOI MOSFETs were investigated. The effects of different MOSFET parameters on SC and SS, such as strain, Si substrate thickness, gate-length ratio, and different control/screen gate work-functions were described.

2.5.4 Review on analog/RF performance of DG s-Si MOSFETs

The 2-D analytical model of cylindrical surrounding-gate (SRG) MOSFET was developed in [84] to assess the analog performance. To develop this model, a pseudo 2-D model using Gauss's law in the silicon channel region was utilized for cylindrical SRG MOSFET. By using the surface potential approach, analytical models of differential capacitances and drain current were obtained. Moreover, analog parameters were evaluated in ballistic and diffusive regimes.

In [85], for the first time, the analog/RF performance of a negative capacitance (NC) SOI junctionless (JLT) MOSFET with quantum effects was presented. Its parameters such as the transconductance, transfer characteristics, and unity-gain frequency were enhanced by the negative capacitance of the device. In this device, ferroelectric oxide materials were used in gate stack to enhance the switching performance. The metal ferroelectric metal insulator semiconductor gate stack structure was simulated with the aid of 1-D Landau Khalatnikov equation to include the effect of NC with SOI JLT.

In [86], the effect of device engineering on analog/RF performances of SOI MOSFETs was illustrated. The analog performance was estimated in terms of transconductance generation factor and early voltage. Besides, the RF performance of device is measured by means of the gain, transition and maximum frequencies.

In [87], the impact of different high-k dielectric gate insulating materials on analog/RF characteristics of nanoscale DG MOSFET was demonstrated. It is noticed that the Silicon

Nitride has better analog/RF performance when compared to other Tantalum pentoxide and Hafnium oxide.

The analog/RF performance evaluation of nano-scale DG MOSFET was presented in [42]. Moreover, optimum performance of nano-scale DG MOSFET was obtained by employing gate and channel engineering. Besides, gain transconductance frequency product (GTFP) of the device that contains both the intrinsic gain and switching speed of the MOSFET was presented and is an important parameter in designing the circuits.

In [52], the effects of channel length and high-k dielectric thickness on analog/RF performance of GC and GS DG-MOSFET were demonstrated. The parameters such as transconductance, gate-source capacitance, and unity gain frequency were enhanced by incorporating graded channel with gate stack in DG MOSFET.

2.5.5 Review on variability analysis of DG s-Si MOSFETs

The threshold voltage model of FD-SOI MOSFET with random dopant fluctuations (RDF) was demonstrated in [88]. RDF provides nonuniform doping in channel. As a result, there is a deviation in threshold voltage of the device, which can be evaluated using this analytical model. Moreover, the dependence of different device parameters, such as channel length, thicknesses of gate oxide, and silicon film on deviation of threshold voltage was studied.

In [89], the effect of RDF in undoped channel silicon gate all around nanowire was demonstrated. Besides, it is noticed that the random dopant fluctuation in the source/drain extension and channel regions disturbs the carrier potential and initiates random variations in electrical characteristics of nanowire.

In [90], the impact of RDF in source and drain on performance of DG MOSFETs was presented. Also, the effect of high doping clusters on the charge injection was examined in detail using quantum simulation based on non-equilibrium Green function coupled self consistently to the Poisson's equation.

In [91], a study on impact of random dopant variations in the source/drain extension (SDE) of Strained SiGe FinFETs was presented. Moreover, increasing SDE's length and decreasing SDE's doping concentration reduce the variations in threshold voltage, ON-current, and OFF-current.

In [92], the effect of RDFs, metal gate work function variations, and line edge roughness were numerically examined for U-shaped FD-SOI MOSFET and compared with conventional FD SOI MOSFET. Immunity to variability sources makes U- FD-SOI MOSFET a suitable architecture for upcoming CMOS logic applications.

2.6 Summary

Based on literature survey discussed in above sections, Chapter 2 can be concluded with a few major observations as follows:

The DG s-Si MOSFET can outperform planar MOSFET due to its striking features such as good SCEs immunity, high drive current capability, high effective carrier mobility, and high transconductance. Thus making it appropriate for a numerous applications like subthreshold circuit operation, low-power circuits, radio frequency, memory, and systems-on-a-chip. Hence, there is an ample scope in the simulation and modeling of gate material and channel engineering of DG s-Si MOSFET with interface charges. The scope of the thesis defined in Chapter 1 is found out from the above discussed literature survey.

Chapter 3

Analytical simulation and modeling of subthreshold characteristics of GC-DMDG s-Si MOSFET with interface charges

3.1 Introduction

As stated in Chapters 1 and 2, the dual metal gate structure was introduced in DG MOSFETs to suppress the HCEs and increase the immunity against SCEs. Furthermore, lateral GC engineering is employed in DG MOSFETs to achieve high threshold voltage and low SCEs. Besides, the HCEs are reduced due to lower built-in potential at drain/channel interface.

To the best of authors' knowledge, the center potential based model for symmetrical GC-DMDG s-Si MOSFET incorporating interface charges has not been presented in the literature so far. In this chapter, natural length, the threshold voltage, subthreshold current and swing of the device are derived based on the center potential of the channel by solving 2-D Poisson's equation. Moreover, based on interface charge density with damaged length at SiO_2/s-Si interface, the position of minimum center potential is determined.

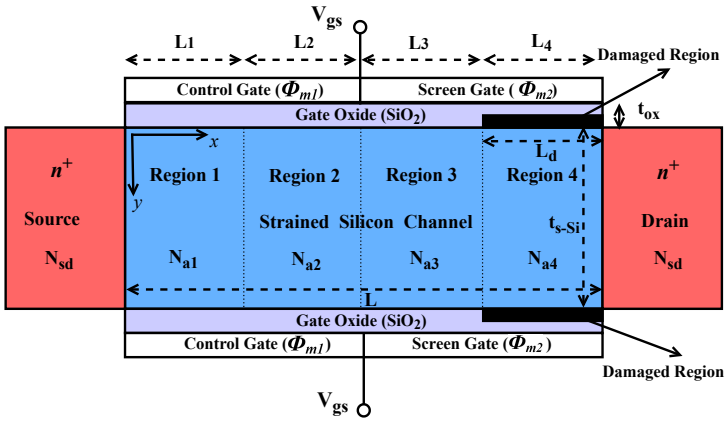

Figure 3.1: Structure of symmetrical GC-DMDG s-Si MOSFET with interface charges.

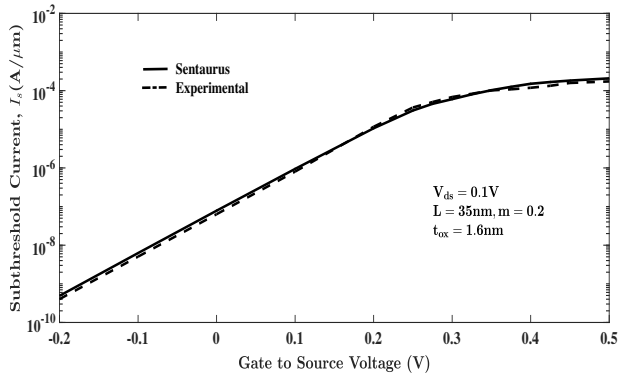

Figure 3.2: Calibration of s-Si MOSFET against experimental data of [93].

3.2 Device structure and simulation setup

The structure of the proposed symmetrical GC-DMDG s-Si MOSFET with interface charge density is shown in Fig. 3-1, where L, t_{s-Si}, L_d, and t_{ox} denote channel length, s-Si channel thickness, damaged length, and gate oxide thickness, respectively. As shown in Fig. 3-1, the x-axis and y-axis of the 2-D diagram are taken at the front SiO_2/s-Si channel interface and the source-to-channel interface, the device is symmetrical along the vertical direction (y-axis), respectively. The p-type s-Si GC region of length, L, is equally separated into four non-overlapped regions (L_r) whose lengths are L_1, L_2, L_3, and L_4 with different uniform doping concentrations N_{a1}, N_{a2}, N_{a3}, and N_{a4}, respectively. The source and drain regions are doped with N_{sd}. Due to HCEs, damaged region at SiO_2/s-Si interface at the drain end is approximated by positive/negative fixed charge density as N_f cm^{-2}. The control gate and screen gate has work functions ϕ_{m1} and ϕ_{m2}, are used over the channel regions 1, 2 and regions 3, 4, respectively. The range of values for various parameters and device dimensions of GC-DMDG s-Si MOSFET used in TCAD simulation are listed in Table 3-1.

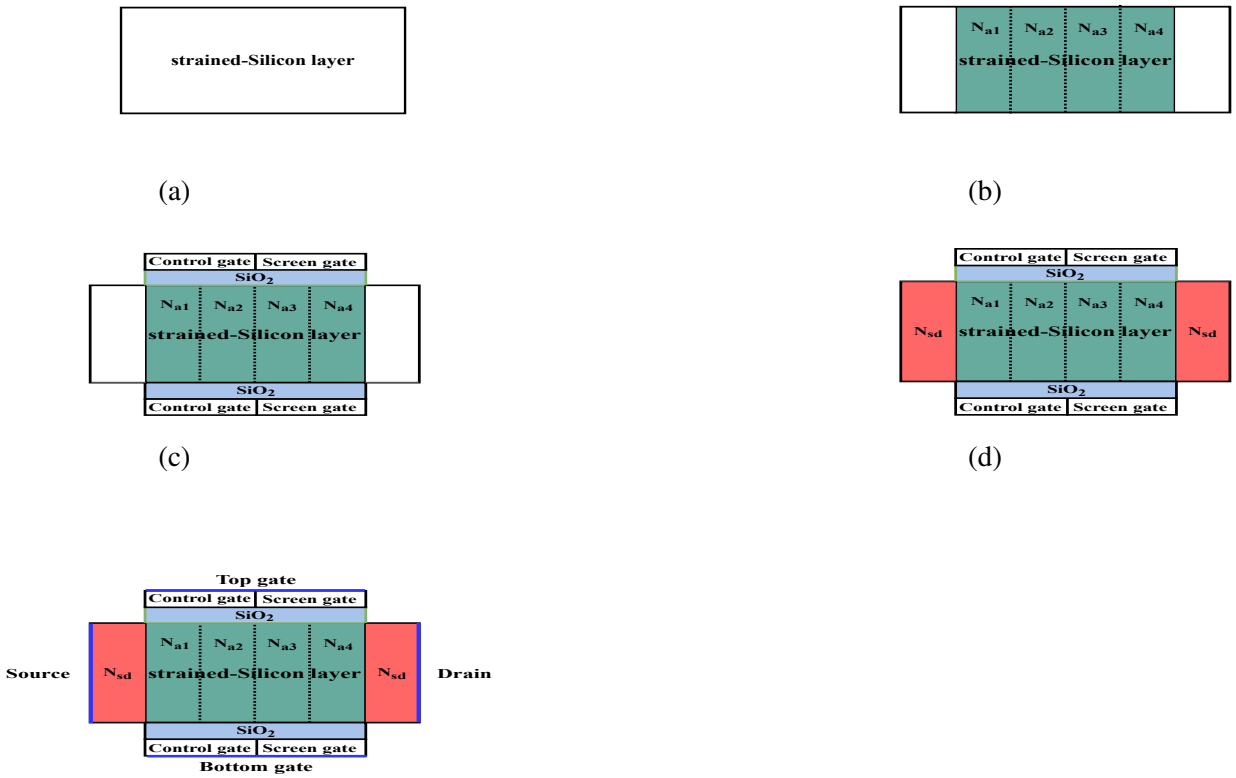

Figure 3.3: Fabrication flow of the proposed s-Si GC-DMDG MOSFET, a. strained-Si layer, b. Graded channel ion implantation, c. Top and bottom gate stack deposition, d.Source/Drain ion implantation, and e. Metal contacts formation

Table 3.1: Dimensions and parameters used in simulation of GC-DMDG s-Si MOSFET

S. No.	Parameter	Symbol	Values
1	s-Si channel length	L	20 - 60 nm
2	s-Si channel doping	$N_{a1}, N_{a2}, N_{a3}, N_{a4}$	10^{17}, 7×10^{16}, 4×10^{16}, 10^{16} cm^{-3}
3	Source/Drain doping	N_{sd}	10^{20} cm^{-3}
4	s-Si thickness	t_{s-Si}	10 - 12 nm
5	Oxide thickness	t_{ox}	1 - 2 nm
6	Work function of control gate, screen gate	ϕ_{m1}, ϕ_{m2}	4.8, 4.6 eV
7	Gate to source voltage	V_{gs}	0 - 1 V
8	Drain to source voltage	V_{ds}	0 - 1 V
9	Ge mole fraction	m	0.1 - 0.3
10	Interface charge density	N_f	-4×10^{12} - 4×10^{12} cm^{-2}

The fabrication flow of the proposed s-Si GC-DMDG MOSFET is shown in Fig. 2. Initially, the SiGe-free strained-Si substrate is fabricated by using the wafer bonding and hydrogen-induced layer transfer of s-Si grown on bulk relaxed SiGe graded layers [7], [8], as shown in Fig. 2(a). In the second step, P-type GC s-Si is obtained by using four different ion implantations (N_{a1}, N_{a2}, N_{a3}, and N_{a4}) with the help of four different mask layers (M_1, M_2, M_3, and M_4), as depicted in Fig. 2(b). In the third step, top and bottom gate stacks are formed by the growth of oxide layer using the dry thermal oxidation process at moderate temperatures, followed by the deposition of dual metal gates [26] in which control and screening gates are deposited by tilt angle evaporation method and normal evaporation method, respectively, as illustrated in Fig. 2(c). In the fourth step, the top and bottom gate stacks are patterned and etched, followed by Source/Drain regions are created by ion implantation (N_{sd}) and activation energy at high temperatures (Rapid thermal activation process), as demonstrated in Fig. 2(d). Finally, the metal contacts at source, drain, top gate, and bottom gate are created at high temperatures, as shown in Fig. 2(e).

In the device simulation setup, the following physical models are incorporated to analyze the analog/RF performance of the GC-DMDG s-Si MOSFET with interface charges. The volt-ampere characteristics are estimated by the drift-diffusion model and the mobility of carriers is determined with the help of high-field saturation and Enormal mobility model. Also, the effect of recombination of carriers is predicted by SRH and Auger recombination models and energy band-gap narrowing effects are also taken into account by the OldSlotboom model. Moreover, s-Si characteristics are considered by using the MoleFraction model and HCEs of the device are included by the Traps model. The TCAD simulation results are calibrated with the experimental date of subthreshold current of s-Si MOSFET of [93], as shown in Fig. 3-2. It is clear from Fig. 3-2 that the TCAD simulation results of s-Si MOSFET is in good agreement with the [94].

3.3 Analytical modeling

3.3.1 Effect of strain on silicon energy band and flat-band voltage

By applying strain to the silicon substrate, the band structure of the silicon will be affected due to biaxial tension. Further, as the electron affinity (χ_{Si}) of silicon increases, both band-gap and the effective mass of carriers decrease simultaneously, which are modeled as follows [95, 96]

$$(\Delta E_c)_{s-Si} = 0.57X, \qquad (\Delta E_g)_{s-Si} = 0.4X$$

$$V_T \ln\left(\frac{N_{V,Si}}{N_{V,s-Si}}\right) = V_T \ln\left(\frac{m^*_{h,Si}}{m^*_{h,s-Si}}\right)^{\frac{3}{2}} \approx 0.075X$$

Where V_T, $(\Delta E_c)_{s-Si}$, and $(\Delta E_g)_{s-Si}$, represent the thermal voltage, increase in electron affinity and decrease in band-gap of s-Si channel. $N_{V,Si}$ and $N_{V,s-Si}$ are the density of states (DOS) in the valence band, $m^*_{h,Si}$ and $m^*_{h,s-Si}$ are the hole effective masses in Si and s-Si, respectively. The effect of strain on the channel flat-band voltage of GC-DMDG s-Si MOSFET can be modeled as follows [96]

$$\left(V_{fbr}\right)_{s-Si} = \left(V_{fbr}\right)_{Si} + \Delta V_{fb}$$

where $\Delta V_{fb} = -\frac{E_c}{q} + \frac{E_g}{q} - V_T \ln\left(\frac{N_{V,Si}}{N_{V,s-Si}}\right)$

$\left(V_{fbr}\right)_{Si} = \phi_{mk} - \phi_{Sir}$, considering $r = 1, 2$ for k =1 and r= 3, 4 for k= 2.

$$\phi_{Sir} = \frac{\chi_{Si}}{q} + \frac{E_g}{2q} + \phi_{F,Sir}, \quad \phi_{F,Sir} = V_T \ln\left(\frac{N_{ar}}{n_{i,Si}}\right)$$

where $\left(V_{fbr}\right)_{s-Si}$ or $\left(V_{fbr}\right)_{Si}$ represents the flat-band voltage of s-Si or Si, ϕ_{Sir} and $\phi_{F,Sir}$ are work function and fermi potential of Si, respectively, corresponding to region r. ΔV_{fb} and q are the change in channel flat-band voltage and electronic charge. E_g, E_c, and $n_{i,Si}$ are energy band-gap, conduction band energy, and intrinsic carrier concentration of Si, respectively. The effect of strain on built-in potential at source (drain)/channel junction can be modeled as [73]

$$V_{bi,s-Si} = V_{bi,Si} + \Delta V_{bi} = V_T \ln\left(\frac{N_{sd}N_a}{n^2_{i,Si}}\right) + \Delta V_{bi}$$

where $\Delta V_{bi} = V_T \ln\left(\frac{N_{V,Si}}{N_{V,s-Si}}\right) - \frac{E_g}{q}$ is the decrease in built-in potential of source (drain)/channel junction. $V_{bi,s-Si}$ and $V_{bi,Si}$ are the built-in potentials at source (drain)/channel junction of s-Si and Si.

3.3.2 Center potential modeling

Let us assume the channel potential $\psi_r(x,y)$ to be a 2-D potential distribution in s-Si channel corresponding to region r, which can be derived by solving the 2-D Poisson's equation in sub-threshold region (where inversion charges are neglected) can be written as [97]

$$\frac{\partial^2\psi_r(x,y)}{\partial x^2} + \frac{\partial^2\psi_r(x,y)}{\partial y^2} = \frac{qN_{ar}}{\epsilon_{Si}}, \quad \text{for} \quad L_{r-1} \le x \le L_r,\ 0 \le y \le t_{s-Si} \tag{3.1}$$

where L_0= 0 and subscript r =1, 2 and 3, 4 represents the two channel regions under control gate and the other two channel regions under screen gate. In the s-Si channel, the potential distribution along the source/channel interface direction can be approximated by a parabolic profile [97]

$$\psi_r(x,y) = C_{0r}(x) + C_{1r}(x)\,y + C_{2r}(x)\,y^2 \tag{3.2}$$

where $C_{0r}(x), C_{1r}(x)$, and $C_{2r}(x)$ are the functions of x. As the electric flux at the interface of s-Si/front and back SiO_2 is continuous in the undamaged and damaged regions, the following boundary conditions can be obtained

$$C_{ox}\left[V_{gs} - \left(V_{fbr,oc}\right)_{s-Si} - \psi_r(x,0)\right] = -\epsilon_{si}\frac{\partial\psi_r(x,y)}{\partial y}\Big|_{y=0} \tag{3.3}$$

$$C_{ox}\left[V_{gs} - \left(V_{fbr,oc}\right)_{s-Si} - \psi_r(x,t_{s-Si})\right] = \epsilon_{si}\frac{\partial\psi_r(x,y)}{\partial y}\Big|_{y=t_{s-Si}} \tag{3.4}$$

where $\left(V_{fbr,oc}\right)_{s-Si} = \left(V_{fbr}\right)_{s-Si} + \frac{qN_f}{C_{ox}}$ is the flat-band voltage of s-Si channel with oxide interface charge density of corresponding region r. V_{gs} is the gate-to-source voltage, C_{ox}=$\frac{\epsilon_{ox}}{t_{ox}}$, ϵ_{si}, and ϵ_{ox} are the gate capacitance per unit area, permittivities of the Si and SiO_2 materials, respectively. $C_{0r}(x)$ is obtained by putting y= 0 in (3.2)

$$C_{0r}(x) = \psi_r(x,y)\big|_{y=0} = \psi_{sr}(x) \tag{3.5}$$

By using the above mentioned boundary conditions (3.3) and (3.4) in (3.2), $C_{r1}(x)$ and $C_{r2}(x)$ can be obtained as

$$C_{1r}(x) = \frac{-C_{ox}}{\epsilon_{Si}}\left[V_{gs} - \left(V_{fbr,oc}\right)_{s-Si} - \psi_{rs}(x)\right] \tag{3.6}$$

$$C_{2r}(x) = \frac{C_{ox}}{\epsilon_{Si} t_{s-Si}} \left[V_{gs} - \left(V_{fbr,oc} \right)_{s-Si} - \psi_{rs}(x) \right] \tag{3.7}$$

The surface and center channel potential distributions ($\psi_{sr}(x)$ and $\psi_{cr}(x)$) of the channel corresponding to region r are obtained by putting $y = 0$ and $y = t_{s-Si}/2$ in (3.2) and the relation between them is

$$\psi_{cr}(x) = \psi_{sr}(x)\left(1 + \frac{C_{ox} t_{s-Si}}{4\epsilon_{Si}}\right) - \frac{C_{ox} t_{s-Si}}{4\epsilon_{Si}} \left(V_{gs} - \left(V_{fbr,oc} \right)_{s-Si} \right) \tag{3.8}$$

Using (3.2) and (3.8) in (3.1), we can obtain,

$$\frac{\partial^2 \psi_{cr}(x)}{\partial x^2} - \frac{1}{\lambda^2} \psi_{cr}(x) = -\frac{1}{\lambda^2} \sigma_r \tag{3.9}$$

where $\lambda = \sqrt{\frac{t_{s-Si}(4\epsilon_{Si} + C_{ox} t_{s-Si})}{8 C_{ox}}}$, $\sigma_r = V_{gs} + W_r$

$$W_r = -\left(V_{fbr,oc} \right)_{s-Si} - \frac{q N_{ar} t_{s-Si}}{2 C_{ox}} - \frac{q N_{ar} t_{s-Si}^2}{8 \epsilon_{Si}} \tag{3.10}$$

λ is the Natural length (distance of penetration of drain electric field in the channel). By solving (3.9), $\psi_{cr}(x)$ in general form can be expressed as

$$\psi_{cr}(x) = A_r \exp\left(\frac{x}{\lambda}\right) + B_r \exp\left(\frac{-x}{\lambda}\right) + \sigma_r \tag{3.11}$$

where A_r $\{r = 1, 2, 3, 4\}$ and B_r $\{r = 1, 2, 3, 4\}$ are the arbitrary constants derived by using the corresponding boundary conditions

$$\psi_{c1}(L_1) = \psi_{c2}(L_1), \quad \psi_{c2}(L_1 + L_2) = \psi_{c3}(L_1 + L_2) \tag{3.12}$$

$$\psi_{c3}(L_1 + L_2 + L_3) = \psi_{c4}(L_1 + L_2 + L_3) \tag{3.13}$$

$$\frac{\partial \psi_{c1}(x,y)}{\partial x}\Big|_{x=L_1} = \frac{\partial \psi_{c2}(x,y)}{\partial x}\Big|_{x=L_1} \tag{3.14}$$

$$\frac{\partial \psi_{c2}(x,y)}{\partial x}\Big|_{x=L_1+L_2} = \frac{\partial \psi_{c3}(x,y)}{\partial x}\Big|_{x=L_1+L_2} \tag{3.15}$$

$$\frac{\partial \psi_{c3}(x,y)}{\partial x}\Big|_{x=L_1+L_2+L_3} = \frac{\partial \psi_{c4}(x,y)}{\partial x}\Big|_{x=L_1+L_2+L_3} \tag{3.16}$$

$$\psi_{c1}(0) = V_{bi1,s-Si}, \quad \psi_{c4}(L) = V_{bi4,s-Si} + V_{ds} \tag{3.17}$$

Using (3.12) to (3.17) in (3.11) and rearranging the terms, we may write

$$A_r = A_{r-1} - \frac{(W_r - W_{r-1})}{2} \prod_{j=1}^{r-1} \exp\left(\frac{-L_j}{\lambda}\right), \quad \text{for} \quad 2 \le r \le 4 \tag{3.18}$$

$$B_r = B_{r-1} - \frac{(W_r - W_{r-1})}{2} \prod_{j=1}^{r-1} \exp\left(\frac{L_j}{\lambda}\right), \quad \text{for} \quad 2 \le r \le 4 \tag{3.19}$$

$$A_1 = \frac{1}{2P}\left[V_{bi4} + V_{ds} - \sigma_4 - (V_{bi1} - \sigma_1)\, R + K\right] \tag{3.20}$$

$$B_1 = V_{bi1} - \sigma_1 - A_1 \tag{3.21}$$

where $P = \sinh\left(\frac{L}{\lambda}\right), \quad R = \exp\left(\frac{-L}{\lambda}\right)$

$$K = (W_4 - W_3)\cosh\left(\frac{L_4}{\lambda}\right) + (W_3 - W_2)\cosh\left(\frac{L_3+L_4}{\lambda}\right) + (W_2 - W_1)\cosh\left(\frac{L_2+L_3+L_4}{\lambda}\right)$$

3.3.3 Electric field modeling

The electric field at the center of channel corresponding to region r is obtained by differentiating eq. (3.11) as follows

$$E_{cr}(x) = -\frac{\partial \psi_{cr}(x)}{\partial x} = \frac{A_r}{\lambda}\exp\left(\frac{x}{\lambda}\right) - \frac{B_r}{\lambda}\exp\left(\frac{-x}{\lambda}\right) \tag{3.22}$$

3.3.4 Threshold voltage modeling

Threshold voltage (V_{th}), is defined as the V_{gs} at which minimum center potential is equal to the twice the fermi potential of Bulk Si [97]. When HCEs are not considered in GC-DMDG s-Si MOSFET, the position of minimum center potential is in region 2 due to higher work function of control gate. Otherwise, it is in one of the regions 2, 3, or 4, based on the presence of the magnitude and polarity of the charge density with damaged length in the affected region. Therefore, depending upon the position of minimum center potential in region r, modified V_{th} condition of GC-DMDG s-Si MOSFET can be defined as follows [96]

$$\psi_{cr,min}|_{V_{gs}=V_{th}} = \psi_{cr}(x_{min})|_{V_{gs}=V_{th}} = 2\phi_{F,Sir} + \Delta V_{bi} = F_r \tag{3.23}$$

where $\psi_{cr,min}$ is the minimum center potential corresponding to region r and is obtained by substituting x_{min} in (3.11). x_{min} represents the position of minimum center potential, it can be estimated by solving $\frac{\partial \psi_{cr}(x)}{\partial x}|_{x=x_{min}} = 0$, From this,

$$x_{min} = \frac{\lambda}{2}\ln\left(\frac{B_r}{A_r}\right), \quad \psi_{cr,min} = 2\sqrt{A_r B_r} - \sigma_r \tag{3.24}$$

Solving (3.23) for V_{th}, the generalized form of threshold voltage equation is

$$V_{th,r-1} = \frac{-H_r + \sqrt{H_r^2 - 4IG_r}}{2I}, \quad \text{for} \quad 2 \le r \le 4 \tag{3.25}$$

$$\text{where } I = 1 + 4\left(1 - \tfrac{(1-R)}{2P}\right)\left(\tfrac{R-1}{2P}\right)$$

$$H_r = -2F_r + 2W_r + 4\left(1 - \frac{(1-R)}{2P}\right)S_r + \frac{2(1-R)}{P}D_r \tag{3.26}$$

$$G_r = F_r^2 - 2F_rW_r + W_r^2 - 4S_rD_r \tag{3.27}$$

$$S_r = S_{r-1} - \left(\frac{W_r - W_{r-1}}{2}\right)\prod_{j=1}^{r-1}\exp\left(\frac{-L_j}{\lambda}\right) \tag{3.28}$$

$$S_1 = \frac{1}{2P}\left[V_{bi4} + V_{ds} - W_4 - (V_{bi1} - W_1)R + K\right] \tag{3.29}$$

$$D_r = D_{r-1} - \left(\frac{W_r - W_{r-1}}{2}\right)\prod_{j=1}^{r-1}\exp\left(\frac{L_j}{\lambda}\right) \tag{3.30}$$

$$D_1 = V_{bi1} - W_1 - S_1 \tag{3.31}$$

3.3.5 Subthreshold current modeling

Subthreshold current (SC), I_s is an leakage current flowing from source to drain when device is in OFF state (i.e., the current passing through the transistor when V_{gs} is less than V_{th} of device). In the subthreshold region of operation, diffusion current is considered as it has a dominance over drift current. The SC of the GC-DMDG s-Si MOSFET can be modeled as follows [77], [98]

$$I_s = \int_0^{t_{s-Si}} J_n(y)\,dy \tag{3.32}$$

where $J_n(y)$ denotes current density (A/μm) and can be expressed as

$$J_n(y) = \frac{qD_n n_{min}(y)}{L_e}\left(1 - \exp\left(\frac{-V_{ds}}{V_T}\right)\right) \tag{3.33}$$

where D_n and L_e, denote diffusion constant of carrier and effective channel length, respectively. $n_{min}(y)$ is the carrier concentration at virtual cathode [99]. With the help of Boltzmann approximation, $n_{min}(y)$ is expressed as follows

$$n_{min}(y) = \frac{n_i^2}{N_{ar}}\exp\left(\frac{\psi_{r,min}(y)}{V_T}\right) \tag{3.34}$$

where $\psi_{r,min}(y) = \frac{\partial \psi_r(x,y)}{\partial x}|_{x=x_{min}}$ is the minimum channel potential at the virtual cathode corresponding to region r. x_{min} is varied from region 2 to region 4 with respect to work function of gate materials and positive (negative) interface charge density with damaged length. Therefore, depending upon the x_{min} in region r, the SC can be represented as $I_{s,r}$. The effective channel length is obtained by considering lateral depletion widths of source and drain as [98]

$$L_e = L - L_{s,dep} - L_{d,dep} + 2L_{Dy} \tag{3.35}$$

$$L_{Dy} = \left(\frac{\epsilon_{Si} V_T}{q N_{a1}}\right)^{\frac{1}{2}} \tag{3.36}$$

where L_{Dy} is the debye length and the depletion widths of source to channel ($L_{s,dep}$) and drain to channel ($L_{d,dep}$) can be modeled as [100],

$$L_{s,dep} = \left(\frac{2\epsilon_{Si} N_{sd} (V_{bi1} - \psi_{1,min}(y_{min}))}{N_{a1}(N_{a1} + N_{sd})}\right)^{\frac{1}{2}} \tag{3.37}$$

$$L_{d,dep} = \left(\frac{2\epsilon_{Si} N_{sd} (V_{bi4} + V_{ds} - \psi_{4,min}(y_{min}))}{N_{a4}(N_{a4} + N_{sd})}\right)^{\frac{1}{2}} \tag{3.38}$$

where V_{bi1}/V_{bi4} is the source/drain to channel built-in potential and y_{min} represents the position of virtual cathode in y-axis, which can be obtained from $\frac{\partial \psi_{r,min}(y)}{\partial y}|_{y=y_{min}} = 0$.

$$\psi_{1,min}(y_{min}) = \psi_{1,min}(y)|_{y=y_{min}},$$

$$\psi_{4,min}(y_{min}) = \psi_{4,min}(y)|_{y=y_{min}}$$

Subthreshold current can be derived by integrating eq. (3.33) along the channel thickness by splitting it into two parts ($I_{sf,r}$ and $I_{sb,r}$), where $I_{sf,r}$ and $I_{sb,r}$ represent the front current component of $I_{s,r}$ ($0 \le y \le y_m$) and the back current component of $I_{s,r}$ ($y_m \le y \le t_{s-Si}$), respectively.

$$I_{s,r} = I_{sf,r} + I_{sb,r}, \qquad \text{for} \quad 2 \le r \le 4 \tag{3.39}$$

$$\text{where} \quad I_{sf,r} = C \int_0^{y_m} \exp\left(\frac{\psi_{r,min}(y)}{V_T}\right) dy \tag{3.40}$$

$$I_{sb,r} = C \int_{y_m}^{t_{s-Si}} \exp\left(\frac{\psi_{r,min}(y)}{V_T}\right) dy \tag{3.41}$$

$$\text{where} \quad C = \frac{q D_n n_i^2}{N_{a1} L_e}\left(1 - \exp\left(\frac{-V_{ds}}{V_T}\right)\right) \tag{3.42}$$

$$I_{sf,r} = \frac{CV_T}{E_{f,r}}\left(\exp\left(\frac{\psi_{r,min}(y_m)}{V_T}\right) - \exp\left(\frac{\psi_{r,min}(0)}{V_T}\right)\right) \tag{3.43}$$

$$I_{sb,r} = \frac{CV_T}{E_{b,r}}\left(\exp\left(\frac{\psi_{r,min}(t_{s-Si})}{V_T}\right) - \exp\left(\frac{\psi_{r,min}(y_m)}{V_T}\right)\right) \tag{3.44}$$

where $E_{f,r}$ and $E_{b,r}$ are the electric fields corresponding to front and back surfaces of the device, corresponding to region r, respectively.

$$E_{f,r} = \frac{\psi_{r,min}(y_m) - \psi_{r,min}(0)}{y_m} \tag{3.45}$$

$$E_{b,r} = \frac{\psi_{r,min}(t_{s-Si}) - \psi_{r,min}(y_m)}{t_{s-Si} - y_m} \tag{3.46}$$

3.3.6 Modeling of effective conductive path

Let us consider $d_{eff,f}$ and $d_{eff,b}$ as the effective conductive path variables of front and back regions of s-Si channel, respectively, which are expressed as follows

$$d_{eff,f} = \frac{\int_0^{y_m} y \exp\left(\frac{\psi_{r,min}(y)}{V_T}\right) dy}{\int_0^{y_m} \exp\left(\frac{\psi_{r,min}(y)}{V_T}\right) dy} \tag{3.47}$$

$$d_{eff,b} = \frac{\int_{y_m}^{t_{s-Si}} y \exp\left(\frac{\psi_{r,min}(y)}{V_T}\right) dy}{\int_{y_m}^{t_{s-Si}} \exp\left(\frac{\psi_{r,min}(y)}{V_T}\right) dy} \tag{3.48}$$

$$d_{eff,f} = \frac{\left(y_m - \frac{V_T}{E_f}\right)\exp\left(\frac{\psi_{r,min}(y_m)}{V_T}\right) + \left(\frac{V_T}{E_f}\right)\exp\left(\frac{\psi_{r,min}(0)}{V_T}\right)}{\exp\left(\frac{\psi_{r,min}(y_m)}{V_T}\right) - \exp\left(\frac{\psi_{r,min}(0)}{V_T}\right)} \tag{3.49}$$

$$d_{eff,b} = \frac{\left(t_{s-Si} - \frac{V_T}{E_b}\right)\exp\left(\frac{\psi_{r,min}(t_{s-Si})}{V_T}\right) - \left(y_m - \left(\frac{V_T}{E_b}\right)\right)\exp\left(\frac{\psi_{r,min}(y_m)}{V_T}\right)}{\exp\left(\frac{\psi_{r,min}(t_{s-Si})}{V_T}\right) - \exp\left(\frac{\psi_{r,min}(y_m)}{V_T}\right)} \tag{3.50}$$

With the help of $d_{eff,f}$ and $d_{eff,b}$, we can write the expression for d_{eff} as follows

$$d_{eff} = \frac{I_{sf}\left|d_{eff,f}\right| + I_{sb}\left|d_{eff,b}\right|}{I_s} \tag{3.51}$$

From eq. (3.51), d_{eff} is obtained at middle of the s-Si thickness ($y = t_{s-Si}/2$) for symmetrical GC-DMDG s-Si MOSFET [54]. Whereas for asymmetrical GC-DMDG s-Si MOSFET, it is located either at the region between front s-Si/SiO_2 interface and middle of the s-Si thickness or the region between back s-Si/SiO_2 interface and middle of the s-Si thickness. The position

of leakage path in vertical direction (along y-axis) of channel region can be obtained with the help of d_{eff}.

3.3.7 Subthreshold swing modeling

Subthreshold swing (SS) represents the switching speed of the device when device operates in the subthreshold region. It is the amount of V_{gs} required to change the subthreshold current by a decade and calculated from the reciprocal of the slope of $\log(I_s)$ v_s V_{gs} characteristics of GC-DMDG s-Si MOSFET. It can be expressed as follows

$$SS = \left(\frac{\partial \log I_s}{\partial V_{gs}}\right)^{-1} = \ln(10)\left(\frac{\partial \ln I_s}{\partial V_{gs}}\right)^{-1} \tag{3.52}$$

From eq. (3.52), obtaining a closed form of the subthreshold swing is tedious due to the existence of the complex terms in the expression of I_s. Therefore, the SS is represented in terms of the minimum center channel potential ($\psi_{r,min}(y)$), where $\psi_{r,min}(y)$ exists in any one of the regions (r) depending upon the work function of gate materials, doping of the graded channel and interface charge density with damaged length. Thus, SS of GC-DMDG s-Si device with interface charges is expressed as follows [101]

$$SS_r = V_T \ln(10)\left(\frac{\partial \psi_{r,min}(y)}{\partial V_{gs}}\right)^{-1}, \text{ for } 2 \le r \le 4 \tag{3.53}$$

The subthreshold swing is a function of y, which is undesirable since it is a device parameter. Hence, it is modified by replacing y with d_{eff} as follows [101]

$$SS_r = V_T \ln(10)\left(\frac{\partial \psi_{r,min}(d_{eff})}{\partial V_{gs}}\right)^{-1} \tag{3.54}$$

$$= \frac{V_T \ln(10)}{(OM)_r(1+K_1) - K_1} \tag{3.55}$$

$$\text{where} \quad (OM)_r = \frac{K_2 K_3 2V_{gs} + (MO_r)}{\sqrt{A_r B_r}} + 1 \tag{3.56}$$

$$K_1 = \frac{C_{ox} d_{eff}}{\epsilon_{si}} - \frac{C_{ox} d_{eff}^2}{\epsilon_{si} t_{s-Si}}, \quad K_2 = \frac{(1-R)}{2P} - 1 \quad \text{and} \quad K_3 = \frac{R-1}{2P}$$

$$(MO)_r = K_2 M_r + K_3 O_r \tag{3.57}$$

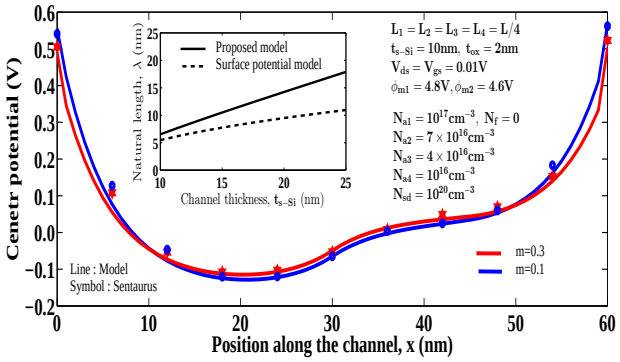

Figure 3.4: Variation of center potential of the GC-DMDG s-Si MOSFET with m= 0.1 and 0.3 for L= 60 nm. Inset: Variation of natural length of GC-DMDG s-Si MOSFET for different values of s-Si thickness.

$$M_r = M_{r-1} - \frac{(W_r - W_{r-1})}{2} \prod_{j=1}^{r-1} \exp\left(\frac{-L_j}{\lambda}\right) \tag{3.58}$$

$$O_r = O_{r-1} - \frac{(W_r - W_{r-1})}{2} \prod_{j=1}^{r-1} \exp\left(\frac{L_j}{\lambda}\right) \tag{3.59}$$

$$M_1 = \frac{1}{2P}\left[V_{bi4} + V_{ds} - W_4 - (V_{bi1} - W_1)R + K\right] \tag{3.60}$$

$$O_1 = V_{bi1} - W_1 - M_1 \tag{3.61}$$

3.4 Result Analysis

In this section, the analytical results of the proposed model for GC-DMDG s-Si device and GC-DG s-Si device are compared with the numerical simulation results obtained using a 2-D numerical simulator TCAD. Where GC-DG s-Si MOSFET, single gate material is considered whose work function is average of ϕ_{m1} and ϕ_{m2}. In Sentaurus simulation, threshold voltage is extracted using the constant current method, i.e., V_{th} is taken from the drain current (I_d) v_s V_{gs} curve by considering the value of the V_{gs} at drain current $I_d = (\frac{W}{L})10^{-7}$ A/μm [39], where W and L are width and length of the channel. Further, as the t_{s-Si} is considered to be $\geq$ 10 nm, the quantum mechanical effects are neglected [102].

Firstly, as shown in Fig. 3-3 (inset), natural length of the proposed center potential model is compared with the surface potential model [16] along the channel thickness. It is observed that center potential based natural length of the proposed model is greater than the surface potential model. Due to this increase in the natural length of GC-DMDG s-Si MOSFET, it

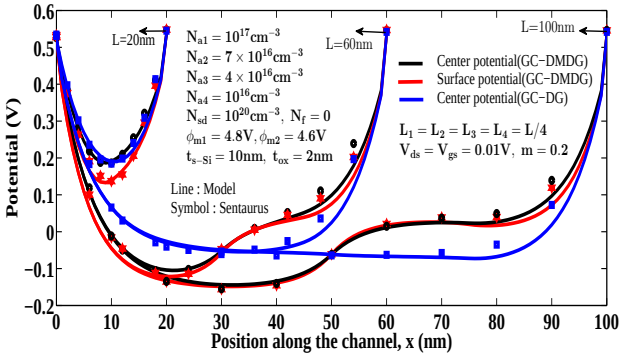

Figure 3.5: Variation of center and surface potentials of GC-DMDG and GC-DG s-Si MOSFETs for L= 20 nm, L= 60 nm and L= 100 nm.

suffers from more SCEs than those predicted by surface potential based model [16], owing to the increase in the drain control over the channel when compared to gate control [103]. Therefore, SCEs are accurately estimated by the proposed model. The variation of the center potential of GC-DMDG s-Si MOSFET along the channel length for m= 0.1 and 0.3 is demonstrated in Fig. 3-3. By increasing the strain in the channel, center potential near source (drain) end decreases and $\psi_{cr,min}$ increases, linearly, due to reduced source (drain) to channel potential barrier and flat-band voltage of the channel. Hence, V_{th} is expected to decrease.

Fig. 3-4 shows comparison of the center potentials of GC-DMDG s-Si MOSFET and GC-DG s-Si MOSFET along the channel length. It is clear from Fig. 3-4 that the x_{min} of the step-like potential profile is in region 2 for GC-DMDG s-Si structure, whereas for GC-DG s-Si structure, it is in region 3. Moreover, $\psi_{cr,min}$ of GC-DMDG s-Si MOSFET is lower than GC-DG s-Si MOSFET due to DMG structure of GC-DMDG s-Si. Therefore, GC-DMDG s-Si device has a higher source/channel potential barrier than GC-DG s-Si device. Thus, the proposed device offers better immunity to SCEs as x_{min} is closer to the source side and higher source/channel potential barrier. In GC-DMDG s-Si MOSFET, it is noticed that minimum potential is lower at the surface ($y = 0$) than at the center ($y = t_{s-Si}/2$) for shorter channel length and for the longer channel length it is observed to be equal. Therefore, channel inversion is formed at $y = t_{s-Si}/2$ due to the lower source (drain)/channel potential barrier. Hence, the model for V_{th} is derived based on center potential, $\psi_{cr}(x)$.

Fig. 3-5 shows the effect of interface charge density with $L_d = L/4$ and V_{ds} on center potential of GC-DMDG s-Si structure for different channel lengths. When V_{ds}= 0.1 V, for interface charge density of $-2\times10^{12} \leq N_f \leq 4\times10^{12}$ and channel length of $20\,nm \leq L \leq 100\,nm$, for $N_f = -3 \times 10^{12}$ and $20\,nm \leq L < 80\,nm$, and for $N_f = -4 \times 10^{12}$ and $20\,nm \leq L < 60\,nm$, x_{min} is in region 2. However, for N_f=-3×10^{12} and $80\,nm \leq L \leq 100\,nm$, for N_f=-4×10^{12}

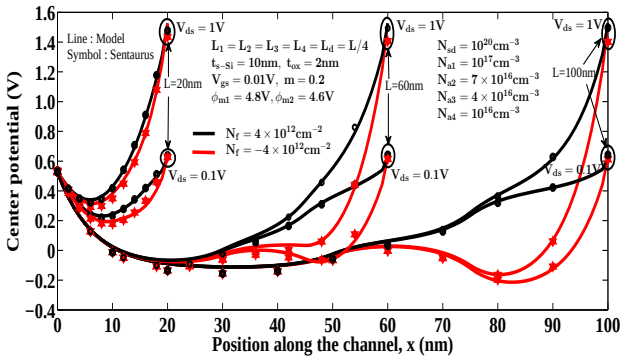

Figure 3.6: Variation of center potential of the GC-DMDG s-Si MOSFET with damaged length, $L_d = L/4$ for different channel lengths.

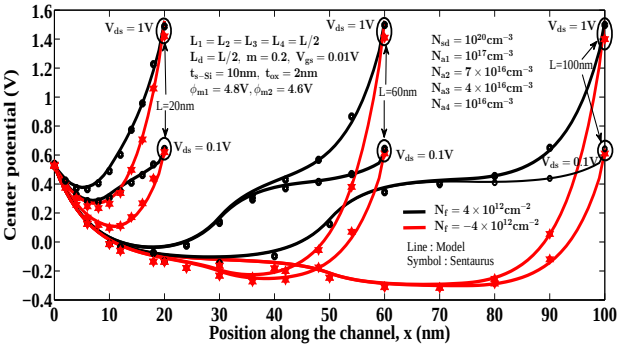

Figure 3.7: Variation of center potential of the GC-DMDG s-Si MOSFET with damaged length, $L_d = L/2$ for different channel lengths.

and 60 $nm \leq L \leq 100$ nm, x_{min} shifts from region 2 to region 4. Simultaneously, $\psi_{cr,min}$ shifts upwards/downwards for positive/negative interface charge density. It is also observed that when V_{ds}= 1 V and $N_f = -4 \times 10^{12}$, x_{min} does not change for channel length of 100 nm, x_{min} shifts from region 4 to region 2 for channel length of 60 nm. Therefore, the effect of V_{ds} on x_{min} and $\psi_{cr,min}$ are more at shorter channel lengths, consequently V_{th} and drain-induced barrier lowering (DIBL) are affected accordingly.

Fig. 3-6 depicts the effect of interface charge density with $L_d = L/2$ and V_{ds} on center potential of GC-DMDG s-Si structure for different channel lengths. When V_{ds}= 0.1 V, for interface charge density of $-2\times10^{12} \leq N_f \leq 4\times10^{12}$ and channel length of 20 $nm \leq L \leq 100$ nm, x_{min} is in region 2. Moreover, for $-4\times10^{12} \leq N_f \leq -3\times10^{12}$ and 20 $nm \leq L < 80$ nm, x_{min} shifts from region 2 to region 3. In addition, for $-4\times10^{12} \leq N_f \leq -3\times10^{12}$ and 80 $nm \leq L < 100$ nm, x_{min} shifts from region 3 to region 4. Simultaneously, $\psi_{cr,min}$ is varied linearly based on charge density and the effect of V_{ds}= 1 V on center potential is significant at channel length of 20 nm.

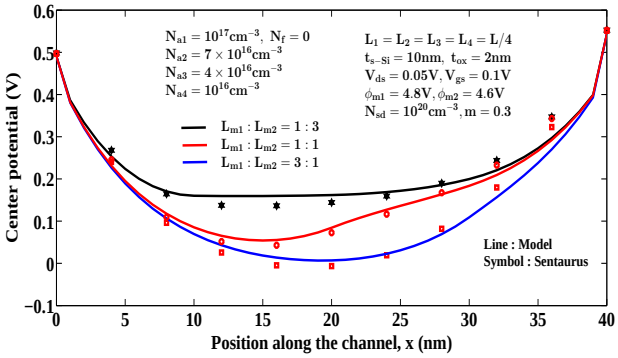

Figure 3.8: Variation of center potential of the GC-DMDG s-Si MOSFET for different gate length ratios of control/screen.

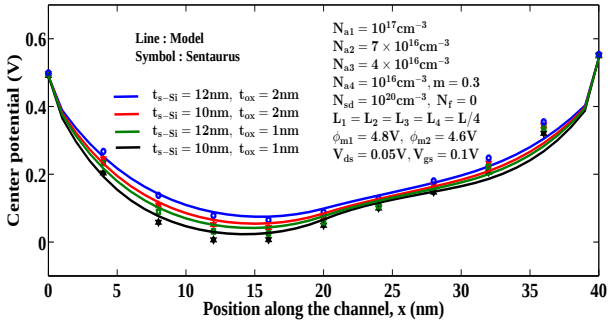

Figure 3.9: Variation of center potential of the GC-DMDG s-Si MOSFET for different values of t_{ox} and t_{s-Si} .

The center channel potential of GC-DMDG s-Si MOSFET for various ratios of the control/screen gate lengths is demonstrated in Fig. 3-7. Drain terminal control over graded s-Si channel is improved by increasing the ratios of the control/screen gate lengths owing to a change in position of the minimum channel potential in the direction of drain side. Also, the barrier potential of the source/channel interface of GC-DMDG s-Si MOSFET increases (higher V_{th}) as the ratios of control/screen gate lengths increase. As a result, the subthreshold leakage current of the proposed GC-DMDG s-Si MOSFET decreases. Therefore, the optimum value among the different ratios of control/screen gate lengths is chosen for better performance of the device.

Fig. 3-8 depicts the effects of t_{ox} and t_{s-Si} on center channel potential of GC-DMDG s-Si MOSFET. In Fig. 3-8, it is noticed that the source/channel interface barrier potential is enhanced by lowering values of t_{s-Si} and t_{ox}, as such higher control over s-Si graded channel is obtained by gate terminal than the drain terminal, consequentially, SCE's are suppressed. Moreover, threshold voltage of GC-DMDG s-Si MOSFET increases as decreasing the values of t_{ox} and t_{s-Si} due to the minimum center channel potential decreases.

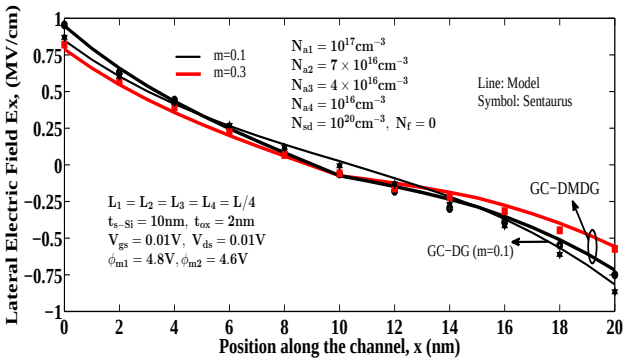

Figure 3.10: Variation of lateral electric field along the channel length of GC-DMDG and GC-DG s-Si MOSFETs with m= 0.1 and 0.3.

$E_{cr}(x)$ of GC-DG and GC-DMDG s-Si MOSEFTs are compared along the channel length as shown in Fig. 3-9. It is observed that HCEs are reduced in GC-DMDG s-Si device as peak value of lateral electric field at drain/source side is lower/higher than at drain/source side of GC-DG s-Si device due to DMG structure of GC-DMDG s-Si MOSFET. Moreover, increased average lateral electric field is observed in the proposed GC-DMDG s-Si device, which reduces the propagation delay of the device due to increase in the average speed of the carrier. Besides, by increasing the strain, the peak lateral electric field decreases at drain and source side due to the reduced built-in potential at drain/source to channel resulting in the reduced HCEs in the proposed GC-DMDG s-Si MOSFET.

For GC-DMDG and GC-DG s-Si MOSFETs, the effect of V_{ds} on threshold voltage is plotted along the channel length in Fig. 3-10. It is observed that GC-DMDG s-Si structure offers a larger V_{th} than GC-DG s-Si structure due to the higher potential barrier at the source to channel junction, as shown in Fig. 3-4. Moreover, the impact of V_{ds} on the V_{th} of GC-DMDG s-Si device is less when compared to GC-DG s-Si due to step-function in potential profile of GC-DMDG s-Si device, as shown in Fig. 3-4. Hence, lower DIBL value is achieved for GC-DMDG s-Si device.

In Fig. 3-11, the effect of strain on center and surface potentials based threshold voltage of GC-DMDG s-Si MOSFET are plotted along the channel length. It is quite evident from Fig. 3-11, simulation results are exactly matched with center potential based V_{th1} model compared to the surface potential based V_{th1} model, because leakage path is formed at the center of the channel. In this case, center potential based V_{th1} model is used as x_{min} is in region 2, shown in Fig. 3-4. Moreover, V_{th} decreases as the channel length is reduced because of lower gate control over the channel than the drain control (charge sharing between drain and gate terminal).

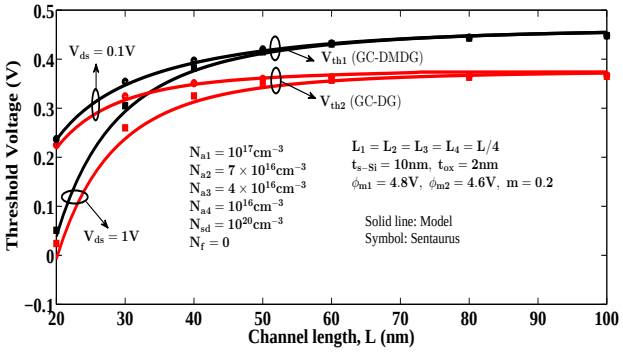

Figure 3.11: Variation of threshold voltage along channel length of the GC-DMDG and GC-DG s-Si MOSFETs for different values of V_{ds}.

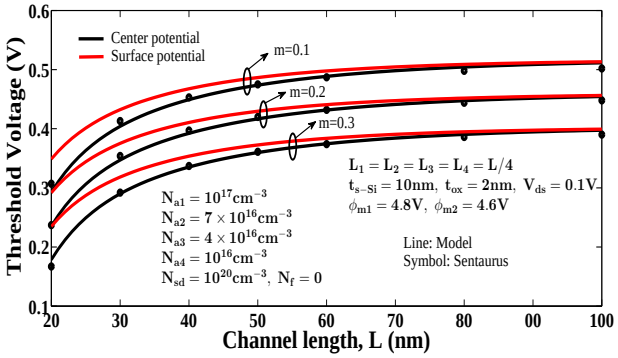

Figure 3.12: Variation of ψ_{cr} and ψ_{sr} based threshold voltage along channel length of the GC-DMDG s-Si MOSFET for different Ge mole fractions.

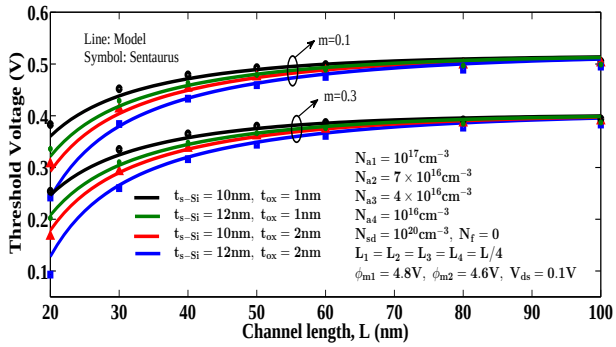

Figure 3.13: Variation of threshold voltage along channel length of the GC-DMDG s-Si MOSFET for different values of t_{ox} and t_{s-Si}.

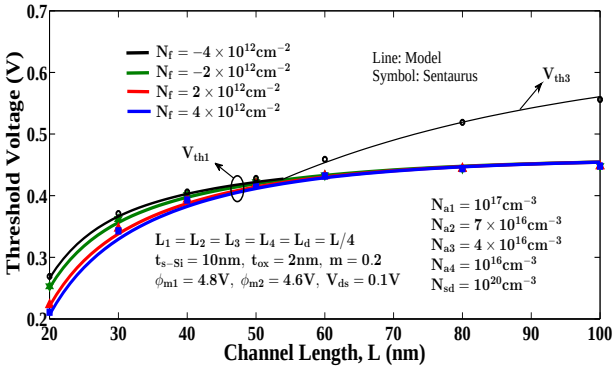

Figure 3.14: Variation of threshold voltage along channel length of the GC-DMDG s-Si MOSFET for interface charge density with $L_d = L/4$.

Influence of strain on threshold voltage along the channel length of the GC-DMDG s-Si device with different values of t_{ox} and t_{s-Si} are shown in Fig. 3-12. It is noticed that the effects of t_{ox} and t_{s-Si} values on V_{th} is more at shorter channel lengths compared to longer channel lengths. Among different values of t_{ox} and t_{s-Si}, t_{ox}= 1 nm and t_{s-Si}= 10 nm, shows reduced V_{th} roll-off due to better gate control over the channel than drain control. In addition, V_{th} decreases with increasing strain in the channel due to reduced flat-band voltage and built-in potential at source (drain)/channel junction, as shown in Fig. 3-3.

Fig. 3-13 shows the effect of interface charge density limited to SiO_2/s-Si interface of region 4 on the threshold voltage of GC-DMDG s-Si MOSFET along the channel length. For positive/negative interface charge density, the V_{th} decreases/increases due to donor/acceptor-type traps in SiO_2/s-Si interface. Hence, holes or electrons are attracted into the oxide interface, thereby resulting the channel inversion formed at lower or higher values of V_{th}, respectively. Here, for $-2\times10^{12} \leq N_f \leq 4\times10^{12}$ and channel length of 20 $nm \leq L \leq$ 100 nm, for N_f=-4×10^{12} and 20 $nm \leq L <$ 60 nm, simulation data of V_{th} is exactly coincide with V_{th1} model curves as x_{min} is in region 2. On the other hand, for $N_f = -4 \times 10^{12}$ and 60 $nm \leq L \leq$ 100 nm, simulation

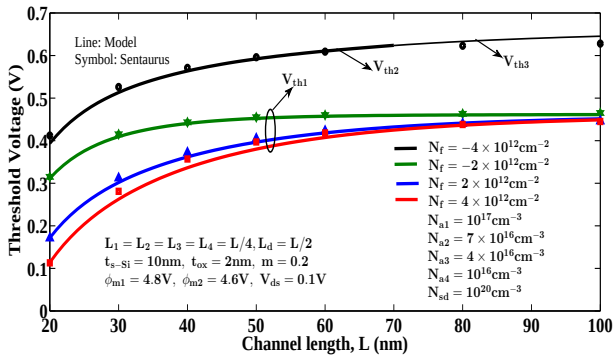

Figure 3.15: Variation of threshold voltage along channel length of the GC-DMDG s-Si MOSFET for interface charge density with $L_d = L/2$.

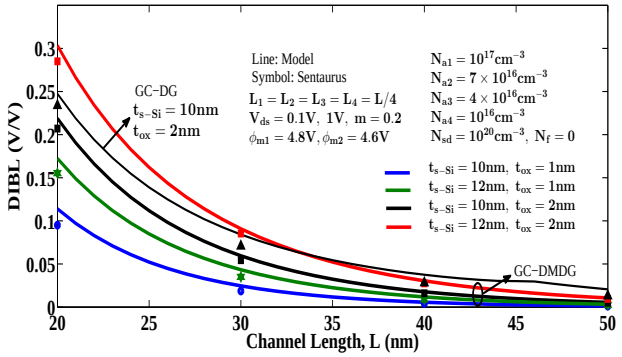

Figure 3.16: Variation of DIBL along channel length of GC-DMDG and GC-DG s-Si MOSFETs with m= 0.2.

data accurately matches with V_{th3} model curves as x_{min} is in region 4, as explained with respect to Fig. 3-5.

Fig. 3-14 depicts the effect of interface charge density limited to SiO_2/s-Si interface of region 3 and 4 on threshold voltage of GC-DMDG s-Si MOSFET along channel length. In this case, for $-2\times10^{12} \leq N_f \leq 4\times10^{12}$ and channel length of 20 $nm \leq L \leq$ 100 nm, simulation data of V_{th} exactly coincides with V_{th1} model curves as x_{min} is in region 2. Moreover, for N_f=-4×10^{12} and 20 $nm \leq L <$ 80 nm, simulation data of V_{th} matches with V_{th2} model curves as x_{min} is in region 3. Besides, for $N_f = -4\times10^{12}$ and 80 $nm \leq L \leq$ 100 nm, simulation data of V_{th} accurately matches with V_{th3} model curves as x_{min} is in region 4, as discussed in detail with respect to Fig. 3-6.

Fig. 3-15 plots the DIBL along the channel length for GC-DMDG and GC-DG s-Si devices for different t_{ox} and t_{s-Si} values. The effective reduction in the DIBL is observed in GC-DMDG s-Si MOSFET when compared to GC-DG s-Si MOSFET because of the step-like profile in center potential of GC-DMDG s-Si MOSFET as shown in Fig. 3-4. Step-like profile in poten-

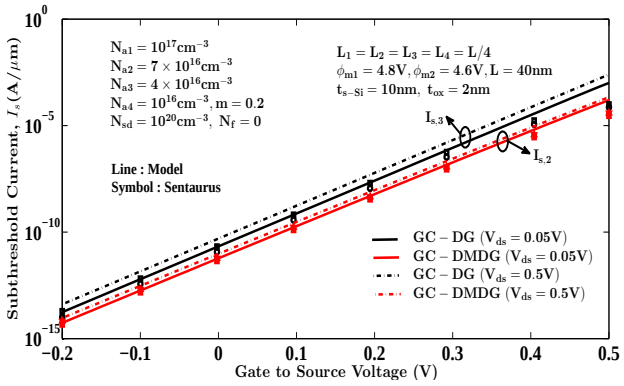

Figure 3.17: Variation of SC of GC-DG and GC-DMDG s-Si devices with L= 40 nm for different values of V_{ds}.

tial screens the variations in V_{ds} on position and minimum of the center potential of GC-DMDG s-Si MOSFET. In GC-DMDG s-Si MOSFET, among different values of t_{ox} and t_{s-Si}, t_{ox}= 1 nm and t_{s-Si}= 10 nm, shows reduced DIBL effect due to better gate control over the channel than drain control. In this case, minimum t_{ox} and t_{s-Si} values are considered to be no less than 1 nm and 10 nm.

Fig. 3-16 depicts the comparison of a subthreshold current of GC-DG and GC-DMDG s-Si MOSFETs for L= 40 nm. It is observed that the GC-DMDG s-Si device offers lower I_s than GC-DG s-Si device due to the larger V_{th} of GC-DMDG s-Si device over GC-DG s-Si MOSFET. Moreover, the effect of V_{ds} on I_s of GC-DMDG s-Si MOSFET is less compared to GC-DG s-Si MOSFET as the variations of V_{ds} are screened by the step-like center channel potential of GC-DMDG s-Si MOSFET. On the other hand, I_s of GC-DG s-Si device is increased by increasing the V_{ds} due to DIBL effect. Therefore, the proposed GC-DMDG s-Si MOSFET has improved subthreshold behavior over GC-DG s-Si MOSFET. Besides, since higher number of the electrons are diffused from the source end to drain end due to decreased source/channel interface barrier potential. I_s increases exponentially with respect to V_{gs} in the subthreshold region. The positions of minimum center channel potential are in region 3 and region 2 for GC-DMDG and GC-DG s-Si MOSFETs, respectively. From Fig. 3-16, it is observed that the simulation curves deviate from the proposed $I_{s,2}$ and $I_{s,3}$ model curves when V_{gs} is greater than V_{th} (i.e. threshold voltages of GC-DMDG and GC-DG s-Si MOSFETs are 0.397 and 0.351 V. Thus, the SC model is valid only in the subthreshold region of the device.

Fig. 3-17 demonstrates the effect of V_{ds} on I_s for different channel lengths of L= 30, 40 and 60 nm. I_s of GC-DMDG s-Si MOSFET increases as the channel length decreases due to SCEs. The V_{th} of GC-DMDG s-Si MOSFET decreases as channel length decreases, thereby an increment in the subthreshold current and decrement in the slope of $V_{gs} - I_s$ curve is observed.

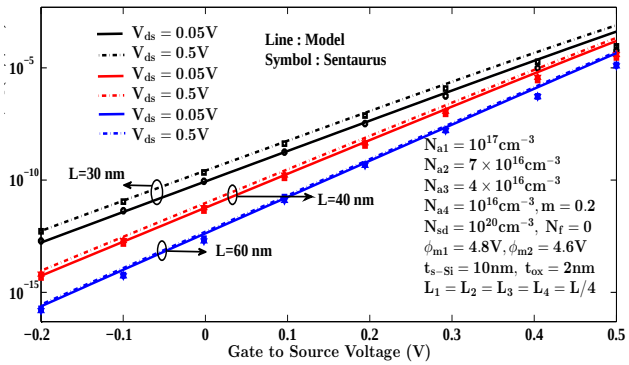

Figure 3.18: Variation of V_{ds} on subthreshold current of the GC-DMDG s-Si MOSFET for different channel lengths.

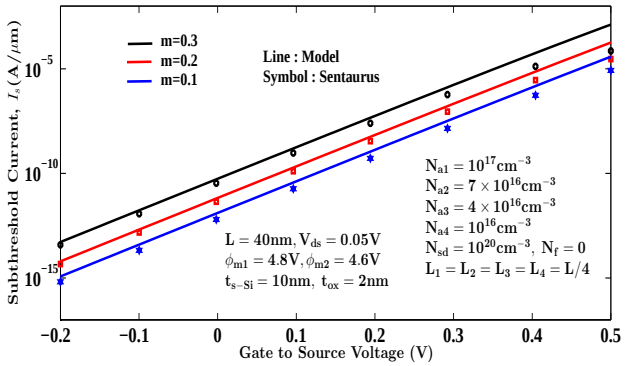

Figure 3.19: Variation of on SC of the GC-DMDG s-Si MOSFET with L= 40 nm for different Ge mole fractions.

Besides, it is clearly noticed from Fig. 3-17, the I_{OFF} increases as channel length reduces owing to SCEs. Moreover, the effect of V_{ds} on I_s is slightly more at short channel length compared to longer channel length due to the DIBL effect. The threshold voltages of the proposed device for channel lengths 30, 40, and 60 nm are 0.354, 0.397, and 0.432 V, respectively. It can be clearly observed in Fig. 3-17 that the SC ($I_{s,2}$) model is valid only in the subthreshold region because of deviation between $I_{s,2}$ model and simulated values of the same in saturation region. In this case, $I_{s,2}$ model is used as position of the minimum center channel potential in region 2.

Fig. 3-18 shows the effect of m on I_s of GC-DMDG s-Si MOSFET. Since the strain of the silicon channel increases, I_s of GC-DMDG s-Si MOSFET also increases owing to the reduced barrier potential of source/channel interface and flat-band voltage of the gate to channel of GC-DMDG s-Si device. The threshold voltages of proposed device for m values 0.1, 0.2, and 0.3 are 0.453, 0.397, and 0.337 V, respectively. It is noticed from Fig. 3-18 that the $I_{s,2}$ model is valid only below threshold region due to position of the minimum center channel potential in region 2. Hence, there is a deviation between $I_{s,2}$ model and simulated values of the same in saturation region.

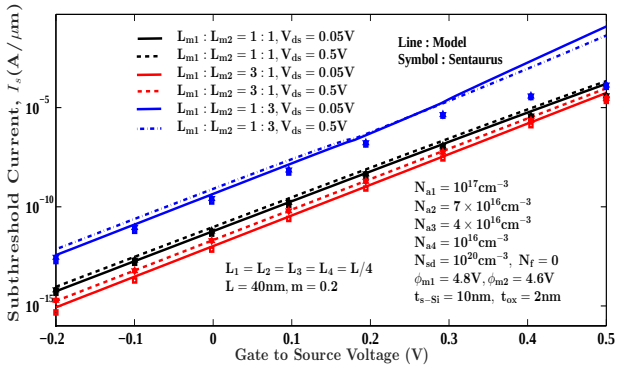

Figure 3.20: Variation of V_{ds} on subthreshold current of the GC-DMDG s-Si MOSFET with L= 40 nm for different gate length ratios of control/screen.

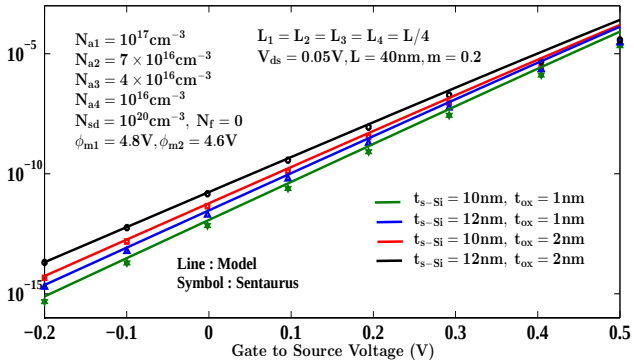

Figure 3.21: Variation of subthreshold current of GC-DMDG s-Si MOSFET with L= 40 nm for different t_{ox} and t_{si} values.

The variations in gate length ratios of control/screen on I_s of GC-DMDG s-Si MOSFET for different values of V_{ds} is demonstrated in Fig. 3-19. The subthreshold leakage current decreases as the length ratio of the control/screen gate increases owing to the higher source/channel interface potential barrier, as depicted in Fig. 3-7. Moreover, the effect of V_{ds} on I_s is more for higher gate length ratio of the control/screen due to $\psi_{r,min}$ that exists towards drain end, as shown in Fig. 3-7. In this case, $I_{s,2}$ model is used as position of the minimum center channel potential in region 2, as shown in Fig. 3-7.

In Fig. 3-20, the variations of t_{ox} and t_{s-Si} on I_s of GC-DMDG s-Si MOSFET are plotted. It is observed that the GC-DMDG s-Si device offers lower subthreshold leakage current when t_{s-Si}=10 nm and t_{ox}= 1 nm compared to different values of t_{ox} and t_{s-Si} due to higher source-channel built-in potential, as demonstrated in Fig. 3-8. Besides, I_{ON}/I_{OFF} ratio increases as reducing the values of t_{ox} and t_{s-Si}. Moreover, $I_{s,2}$ model is valid in subthreshold region for different values of t_{ox} and t_{s-Si} due to position of the minimum center channel potential in region 2, as shown in Fig. 3-8.

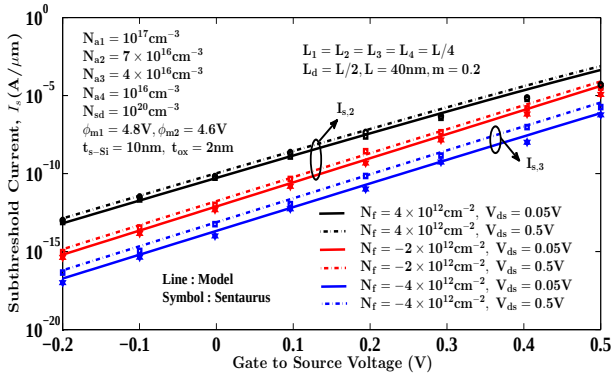

Figure 3.22: Variation of fixed charges on SC of the GC-DMDG s-Si device with L= 40 nm for V_{ds}= 0.05 and 0.5 V.

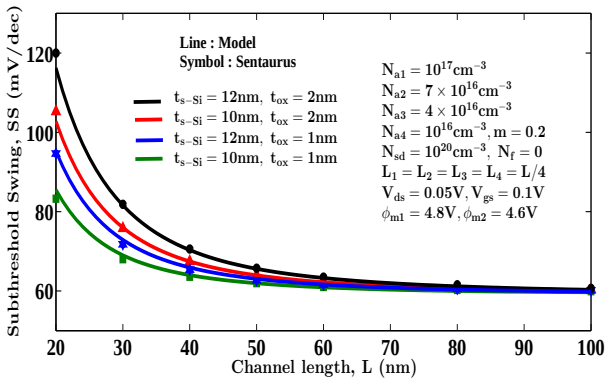

Figure 3.23: Variation of subthreshold swing of GC-DMDG s-Si MOSFET for different t_{ox} and t_{si} values.

Fig. 3-21 depicts the variation of fixed charge density on I_s of GC-DMDG s-Si MOSFET for different values of V_{ds}. I_s of GC-DMDG s-Si MOSFET decreases (increases) by increasing the negative (positive) interface charge density at s-Si/SiO_2 interface due to higher (lower) V_{th} of GC-DMDG s-Si MOSFET. It is clearly noticed that from Fig. 3-21, the effect of V_{ds} on I_s of GC-DMDG s-Si MOSFET is more for $N_f = -4 \times 10^{12}$ compared to positive N_f owing to the position of minimum center channel potential in region 3. $I_{s,2}$ model is valid in subthreshold region for $N_f = 4 \times 10^{12}$ and -2×10^{12} as position of the minimum center potential is in region 2. $I_{s,3}$ model is valid in subthreshold region for $N_f = -4 \times 10^{12}$ due to position of the minimum center channel potential in region 3.

Fig. 3-22 plots the influence of t_{ox} and t_{s-Si} on subthreshold swing for GC-DMDG s-Si MOSFET along the channel. It can be noted that among different values of t_{ox} and t_{s-Si}, when t_{ox} and t_{s-Si} = 1 nm and 10 nm, respectively, GC-DMDG s-Si MOSFET offers lower subthreshold swing due to better gate control over the channel. Moreover, subthreshold swing is deteriorated

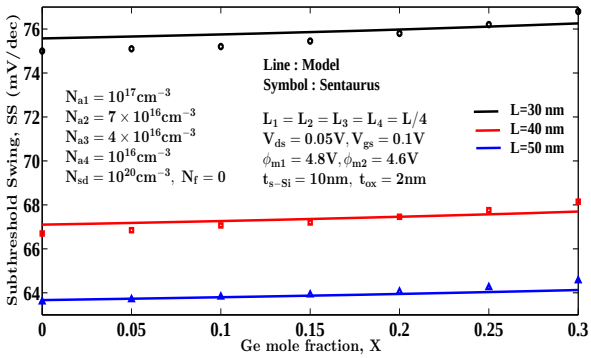

Figure 3.24: Variation of subthreshold swing of the GC-DMDG s-Si MOSFET for different Ge mole fractions.

by reducing the channel length due to increase in SCEs. However, the effect of t_{ox} and t_{s-Si} on subthreshold swing is more at short channel devices.

Fig. 3-23 depicts the variation of strain on subthreshold swing of GC-DMDG s-Si MOSFET for different channel lengths. Subthreshold swing slightly increases with strain due to reduced source/channel potential barrier as shown in Fig. 3-3. Fig. 3-24 depicts the effect of interface charge density with $L_d = L/2$ on subthreshold swing of GC-DMDG s-Si MOSFET along the channel length. Subthreshold swing of GC-DMDG s-Si MOSFET is increases/decreases by increasing the positive/negative charge density due to lower/ higher source-to-channel potential barrier as shown in Fig. 3-6.

Fig. 3-25 plots the effect of gate length ratios of control/screen on the SS of GC-DMDG s-Si device along the channel length for different values of V_{ds}. Subthreshold swing of the proposed GC-DMDG s-Si MOSFET decreases as length ratio of the control/screen gate increases owing to the increased slope of $V_{gs} - I_s$ curve, as shown in Fig. 3-19. It is noticed from Fig. 3-25 that the subthreshold swing degrades as V_{ds} increases owing to the DIBL effect. Moreover, the subthreshold swing of the proposed GC-DMDG s-Si device decreases as channel length of GC-DMDG s-Si device increases due to SCEs.

The performance of the proposed GC-DMDG s-Si MOSFET is compared with the previous works, as demonstrated in Table 3-2. It is observed from Table 3.2 that the proposed GC-DMDG s-Si device has lower I_{OFF}, higher I_{ON}/I_{OFF} ratio, and lower SS compared to GC-DG s-Si device and Guassian doped DMDG s-Si MOSFET with channel length 40 nm [78], [75]. Besides, the proposed GC-DMDG s-Si MOSFET has higher I_{ON}/I_{OFF} ratio than DMG junction less MOSFET with channel length of 80 nm [104]. Therefore, the proposed GC-DMDG s-Si

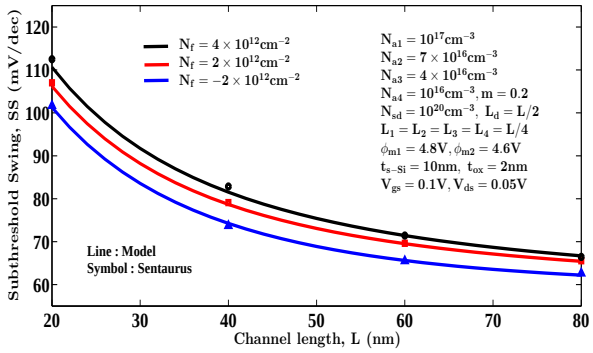

Figure 3.25: Variation of charge density on subthreshold swing of the GC-DMDG s-Si MOSFET with damaged length, $L_d = L/2$.

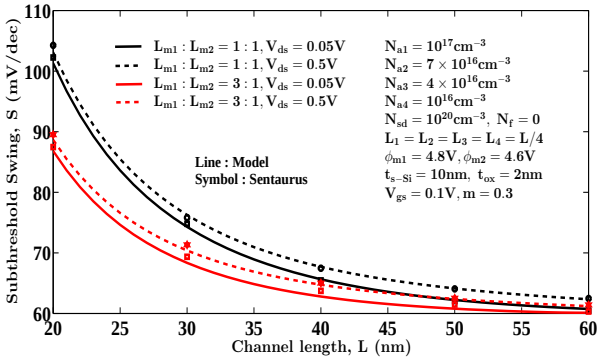

Figure 3.26: Variation of V_{ds} on SS of the GC-DMDG s-Si MOSFET for different gate length ratios of control/screen.

MOSEFT has attained improved subthreshold characteristics using DMG structure with graded channel engineering.

3.5 Conclusion

A center potential based threshold voltage, and SC models for symmetrical GC-DMDG s-Si MOSFET with localized charges has been analytically derived. Moreover, the analytical model of subthreshold swing has been developed by using an effective conductive path param-

Table 3.2: Performance comparison of the proposed GC s-Si MOSFET with the previous works

S.No.	Parameters	I_{ON}, A/μm	I_{OFF}, A/μm	I_{ON}/I_{OFF}	SS, mV/dec
1	GC-DMDG s-Si (L= 40 nm)	5×10^{-5}	2×10^{-15}	2.5×10^{10}	66
2	GC-DG s-Si (L= 40 nm)	8×10^{-5}	5×10^{-15}	1.6×10^{10}	68
3	DMDG s-Si (L= 40 nm) [78], [75]	4×10^{-5}	2×10^{-11}	2×10^{6}	70
4	DMG JLT (L= 80 nm) [104]	5×10^{-4}	10^{-14}	2×10^{9}	62

eter. In this work, the center potential based natural length for accurately estimating the SCEs. A detailed analysis has been performed on GC-DMDG s-Si MOSFET to explore the effects of various device parameters on the center potential, electric field, threshold voltage, DIBL, subthreshold current and swing. From the proposed model, the degradation of threshold voltage roll-off, subthreshold swing and DIBL is observed, due to increase in strain, decrease in channel length, and HCEs, that can be controlled by selecting optimum values of t_{ox} and t_{s-Si}, and using the DMG structure with GC engineering. It is observed that GC-DMDG MOSFET has better immunity against SCEs and HCEs than symmetrical GC-DG MOSFET. The model has been validated using TCAD and the results from the model are observed to be in good agreement with those from the simulator. As a continuation of this chapter, the analysis of analog/RF parameters of GC-DMDG s-Si MOSFET and GCGS-TMDG s-Si MOSFET with interface charges at s-Si/SiO_2 interface will be presented in the next chapter.

Chapter 4

Analog/RF performance of GC-DMDG and GCGS-TMDG s-Si MOSFETs with interface charges

4.1 Introduction

As discussed in Chapters 1 and 2, The DMG and GC engineering have been introduced by many researchers in DG MOSFET to reduce the HCEs and SCEs. However, in the literature, the analog/RF performance of GC-DMDG s-Si MOSFET with interface charges has not been presented. In this work, the analysis of analog/RF parameters of GC-DMDG s-Si MOSFET with interface charges at s-Si/SiO_2 interface is presented. The analog/RF performance of the proposed GC-DMDG s-Si MOSFET for different values of m, N_f, t_{s-Si}, and t_{ox} layer are thoroughly analyzed using Sentaurus TCAD simulator.

Further, the analog/RF performance of proposed MOSFET is enhanced triple gate material with gate stack (GS) structure. The TMG engineering with GC structure is incorporated in DG MOSFET to reduce the HCEs and SCEs. As a result, the analog/RF parameters of the proposed DG MOSFET are enhanced. Furthermore, high-k dielectric with SiO_2 used as gate stack is employed in DG MOSFET, so enhanced sub-threshold characteristics are attained due to the reduction in the gate leakage current of DG MOSFET [105]-[106]. Overall, analog/RF performances of the graded channel gate stack-triple material double gate (GCGS-TMDG) s-Si

MOSFET are enhanced by incorporating high-k dielectric material in gate stack, gate engineering and channel engineering.

4.2 Analog/RF performance of GC-DMDG s-Si MOSFET with interface charges

To assess the analog/RF performance of the proposed GC-DMDG s-Si MOSFET, the analog parameters of device such as transconductance (g_m), output conductance (g_d), transconductance generation factor $\left(TGF = \left(\frac{g_m}{I_{ds}}\right)\right)$, early voltage $\left(\frac{I_{ds}}{g_{ds}}\right)$, and intrinsic voltage gain $\left(\frac{g_m}{g_d}\right)$ are analyzed. TGF represents the efficiency of device to convert the DC power into AC gain at specific biased current. Higher TGF denotes that the lower DC drain current is required to get a particular value of g_m, which is desirable in low power analog applications. Besides, the RF parameters of the proposed device are unity current gain frequency (f_t), transconductance frequency product $\left(\text{TFP} = \left(\frac{g_m}{I_d}\right) f_t\right)$, gain frequency product $\left(\text{GFP} = \left(\frac{g_m}{g_d}\right) f_t\right)$, and Gain transconductance frequency product $\left(\text{GTFP} = \left(\frac{g_m}{g_d}\right)\left(\frac{g_m}{I_d}\right) f_t\right)$ are evaluated exhaustively. TFP gives the optimum performance of the proposed device in terms of power and bandwidth product in analog applications and GTFP denotes the optimum performance of the proposed device in terms of power efficiency and gain bandwidth product. The analog/RF figures of merit of GC-DMDG s-Si MOSFET are improved with an increase in the values of m, positive N_f, t_{ox}, and t_{s-Si} in the subthreshold region, and vice-versa in strong inversion region. The optimum analog/RF performance of the proposed GC-DMDG s-Si MOSFET is attained in strong inversion region compared to GC-DG s-Si MOSFET, i.e., the peak values of figures of merit of analog/RF performance for the proposed GC-DMDG s-Si MOSFET are obtained above the moderate inversion region. Also, the analog/RF performance of proposed GC-DMDG s-Si MOSFET is compared with the GC-DG s-Si MOSFET.

4.2.1 Results and discussion

This section presents the analysis of simulation results for analog/RF performance of GC-DG and GC-DMDG s-Si MOSFET. Fig. 4-1 shows the effect of strain on the transfer characteristics ($V_{gs} - I_{ds}$) and g_m of GC-DMDG s-Si MOSFET for V_{ds}=1 V. From Fig. 4-1, enhanced transfer characteristics of GC-DMDG s-Si MOSFET are observed as increasing the values of m due to reduction of the threshold voltage of GC-DMDG s-Si MOSFET. Besides, as m increases, g_m of GC-DMDG s-Si MOSFET increases in the subthreshold region, and vice-versa in strong

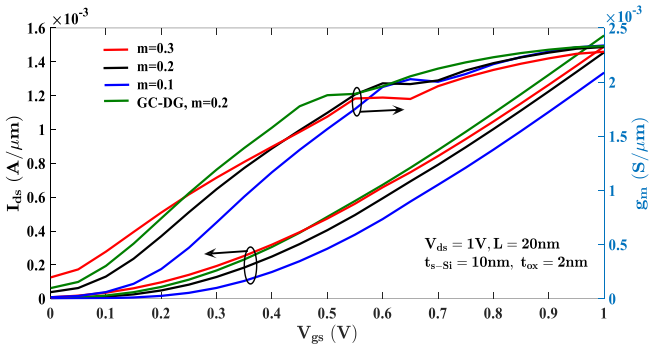

Figure 4.1: Effect of strain on transfer characteristics and g_m of GC-DMDG s-Si MOSFET when L= 20 nm.

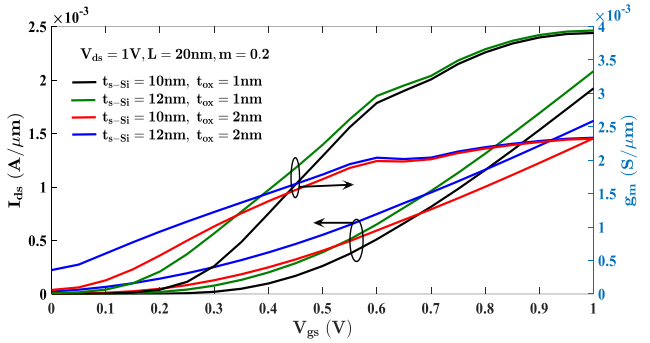

Figure 4.2: Effects of t_{ox} and t_{s-Si} on transfer characteristics and g_m of GC-DMDG s-Si MOSFET when L= 20 nm.

inversion region. Moreover, GC-DG s-Si MOSFET has improved transfer characteristics and better g_m are attained compared to GC-DMDG s-Si MOSFET due to the lower threshold voltage of GC-DG s-Si MOSFET than GC-DMDG s-Si MOSFET. Due to the existence of DMG structure, the proposed GC-DMDG s-Si MOSFET has higher threshold voltage, lower threshold voltage roll-off, and lower DIBL compared to GC-DG s-Si MOSFET.

The effects of t_{ox} and t_{s-Si} on transfer characteristics and g_m of GC-DMDG s-Si MOSFET are shown in Fig. 4-2. From Fig. 4-2, when t_{ox} and t_{s-Si} of GC-DMDG s-Si MOSFET increase, enhanced transfer characteristics and higher g_m are noticed in the subthreshold region due to decrement in the threshold voltage of GC-DMDG s-Si MOSFET. On the other hand, improved transfer characteristics and higher g_m are observed by decreasing t_{ox} and increasing t_{s-Si} of GC-DMDG s-Si MOSFET in strong inversion region due to the better gate control over the channel than drain. Moreover, improved SCEs are attained in the proposed device by decreasing t_{ox} and t_{s-Si}.

Fig. 4-3 depicts the effect of N_f at s-Si/SiO_2 interface with L_d on the transfer characteristics and g_m of proposed GC-DMDG s-Si MOSFET for V_{ds}=1 V. For a given L_d, it is observed from Fig. 4-3 that the improved values of transfer characteristics and g_m of GC-DMDG s-Si

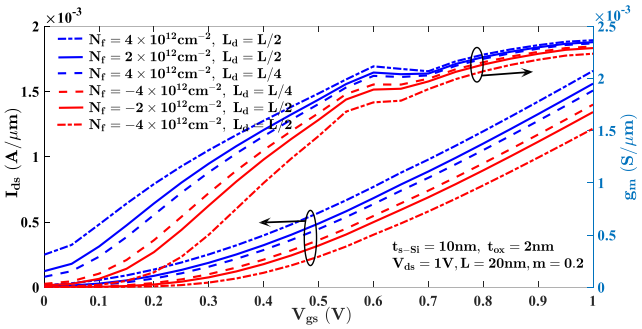

Figure 4.3: Effect of N_f with L_d on transfer characteristics and g_m of GC-DMDG s-Si MOSFET for L= 20 nm.

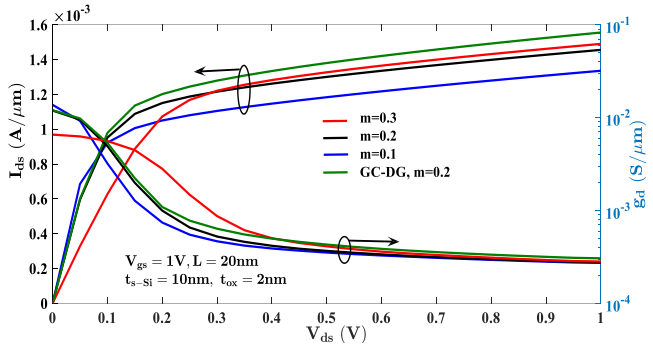

Figure 4.4: Effect of strain on drain characteristics and g_d of GC-DMDG s-Si MOSFET when L= 20 nm.

MOSFET by increasing positive N_f due to decrement in the threshold voltage of GC-DMDG s-Si MOSFET for positive N_f, and vice-versa for negative N_f. Moreover, as positive/negative N_f increases in the GC-DMDG s-Si MOSFET, the minimum of center channel potential increases/decreases, thereby threshold voltage of the proposed device decreases/increases. Also, the position of minimum center potential is shifted towards drain/source side, and hence DIBL of the proposed device is altered. As a result, analog/RF performance of the proposed GC-DMDG s-Si MOSFET is affected based on the interface charges at s-Si/SiO_2 interface with L_d.

Fig. 4-4 shows the effect of m on the drain characteristics ($V_{ds} - I_{ds}$) and g_d of GC-DMDG s-Si MOSFET for V_{gs}=1 V. From Fig. 4-4, by increasing m, it is noticed that the increment values of drain characteristics and g_d of GC-DMDG s-Si MOSFET are obtained because of reduction in the threshold voltage of device. Also, GC-DG s-Si MOSFET has better drain characteristics and higher g_d compared to GC-DMDG s-Si MOSFET due to lower gate control over the channel than drain of GC-DG s-Si MOSFET. Therefore, the proposed GC-DMDG s-Si device has lower g_d since the effect of drain voltage on the channel is lesser compared to GC-DG s-Si device.

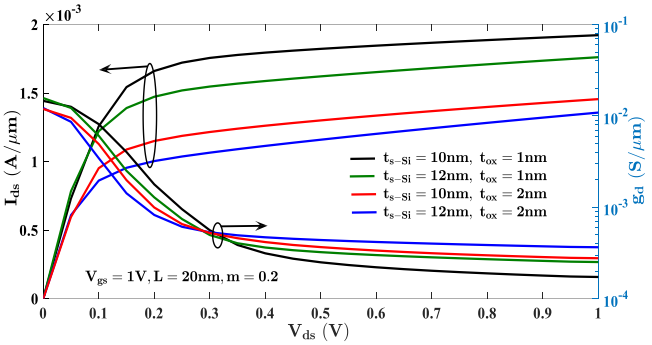

Figure 4.5: Effects of t_{ox} and t_{s-Si} on drain characteristics and g_d of GC-DMDG s-Si MOSFET when L= 20 nm.

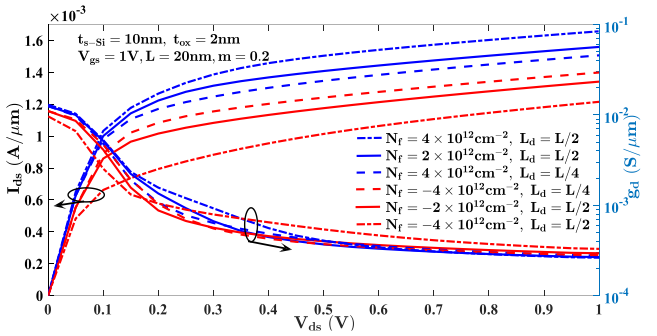

Figure 4.6: Effect of interface charge density with L_d on drain characteristics and g_d of GC-DMDG s-Si MOSFET when L= 20 nm.

Fig. 4-5 depicts the effects of t_{ox} and t_{s-Si} on drain characteristics and g_d of GC-DMDG s-Si MOSFET for V_{gs}=1 V. Among different values of t_{ox} and t_{s-Si}, when t_{ox} and t_{s-Si} are 1 nm and 10 nm, respectively, the proposed device shows enhanced drain characteristics and lower g_d due to higher gate control of the channel than drain. From Fig. 4-5, it is evident that the lower g_d is attained at higher values of V_{ds} by decreasing the values of t_{ox} and t_{s-Si} of GC-DMDG s-Si MOSFET due to reduced SCEs. Hence, the proposed s-Si GC-DMDG device has better analog performance, which is achieved by decreasing t_{ox} and t_{s-Si}.

Fig. 4-6 demonstrates the effect of N_f at s-Si/SiO_2 interface with L_d on the drain characteristics and g_d of GC-DMDG s-Si MOSFET for V_{gs}=1 V. For a given L_d, it is evident from Fig. 4-6 that the increment in drain characteristics are observed by increasing the positive N_f due to decreased threshold voltage of GC-DMDG s-Si MOSFET for positive N_f, and vice-versa for negative N_f. Moreover, for a given L_d, lower/higher g_d is observed at lower values of V_{ds} by increasing the negative/positive N_f, and vice-versa at higher values of V_{ds} due to DIBL effect.

Fig. 4-7 illustrates the effect of m on the TGF and $\frac{g_m}{g_d}$ of GC-DMDG s-Si MOSFET. As depicted in Fig. 4-7, by increasing the values of m and V_{gs} of GC-DMDG s-Si MOSFET, TGF decreases. In the subthreshold region, as I_{ds} varies exponentially with respect to V_{gs}, higher

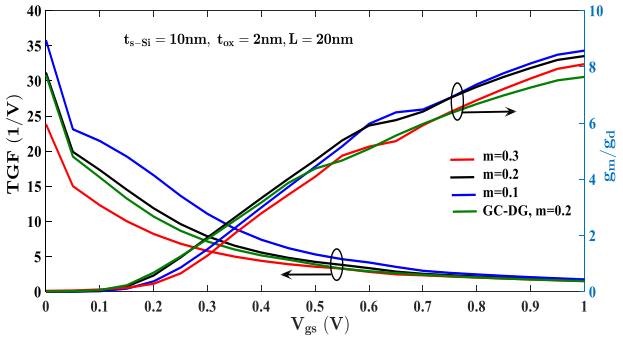

Figure 4.7: Effect of strain on TGF and g_m/g_d of GC-DMDG s-Si MOSFET when L= 20 nm.

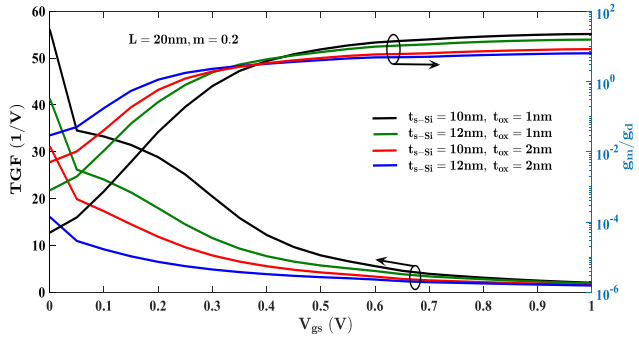

Figure 4.8: Effects of t_{ox} and t_{s-Si} on TGF and g_m/g_d of GC-DMDG s-Si MOSFET when L= 20 nm.

values of TGF are obtained. Therefore, the subthreshold region of operation of GC-DMDG s-Si MOSFET is highly preferred for low power analog applications. From Fig. 4-7, when m= 0.1, it is noticed that the peak value of TGF approaches closely to 38.6 V^{-1}, which is associated with the ideal subthreshold swing. Moreover, as m of s-Si GC-DMDG MOSFET increases, $\frac{g_m}{g_d}$ increases in subthreshold region owing to higher and lower values of g_m and g_d in subthreshold region, respectively, as shown in Fig. 4-1 and Fig. 4-4, and vice-versa in strong inversion region. Besides, as compared to GC-DG s-Si MOSFET, GC-DMDG s-Si MOSFET has higher TGF and better $\frac{g_m}{g_d}$ due to lower SCEs in GC-DMDG s-Si MOSFET. Therefore, the proposed GC-DMDG s-Si device has higher analog gain and better power conversion efficiency due to the existence of DMG structure compared to GC-DG s-Si MOSFET.

Fig. 4-8 depicts the effects of t_{ox} and t_{s-Si} on TGF and $\frac{g_m}{g_d}$ of GC-DMDG s-Si MOSFET. In Fig. 4-8, it is evident that the TGF increases as decreasing values of t_{ox} and t_{s-Si} as better gate control over the channel is attained than drain. As a result, the proposed GC-DMDG s-Si device has lower power consumption that is obtained by decreasing t_{ox} and t_{s-Si}. Besides, $\frac{g_m}{g_d}$ increases in a strong inversion region by reducing the values of t_{ox} and t_{s-Si} due to increment in g_m and decrement in g_d in strong inversion region, as depicted in Fig. 4-2 and Fig. 4-5, and vice-versa in weak inversion region.

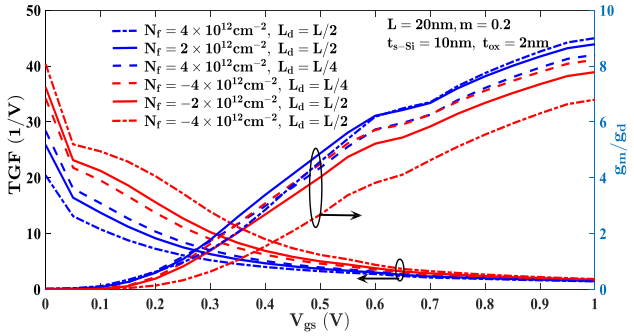

Figure 4.9: Effect of interface charge density with L_d on TGF and g_m/g_d of GC-DMDG s-Si MOSFET when L= 20 nm.

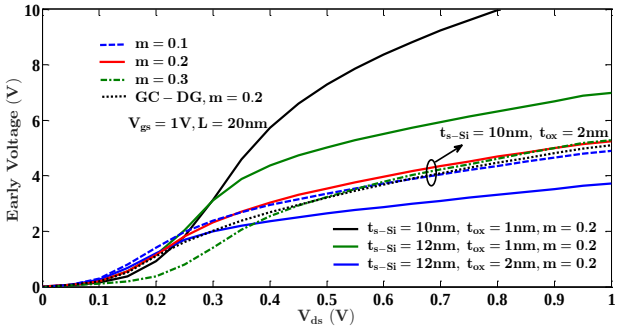

Figure 4.10: Effects of strain, t_{ox}, and t_{s-Si} on early voltage of GC-DMDG s-Si MOSFET when L= 20 nm.

Fig. 4-9 illustrates the variation of N_f at s-Si/SiO_2 interface on TGF and $\frac{g_m}{g_d}$ of GC-DMDG s-Si device for different values of L_d. For a particular L_d, by increasing negative N_f, TGF increases owing to the increment in the threshold voltage of GC-DMDG s-Si MOSFET, and vice-versa for positive N_f. Therefore, the proposed GC-DMDG s-Si MOSFET with negative N_f can be operated at lower operating voltages, and vice-versa for positive N_f. Moreover, for a given L_d, by increasing the positive N_f, the $\frac{g_m}{g_d}$ increases because of increment in g_m and decrement in g_d with respect to positive N_f, as shown in Fig. 4-3 and Fig. 4-6, and vice-versa for negative N_f. Besides, a slight improvement in the small signal gain of GC-DMDG s-Si device is obtained for positive N_f.

Fig. 4-10 depicts the variations of m, t_{ox}, and t_{s-Si} on early voltage of GC-DMDG s-Si MOSFET. At higher values of V_{ds}, early voltage of GC-DMDG s-Si MOSFET slightly increases as m increases. Also, it is increased by reducing the values of t_{ox} and t_{s-Si} because of higher gate control over the channel (higher early voltage represents the lower channel length modulation effect in the device). However, at lower values of V_{ds}, early voltage of GC-DMDG s-Si MOSFET decreases as m, t_{ox}, and t_{s-Si} increase. Moreover, the early voltage of the proposed GC-DMDG s-Si MOSFET is higher than GC-DG s-Si MOSFET owing to the lower g_d and DMG structure of GC-DMDG s-Si MOSFET. Thus, the channel length modulation effect

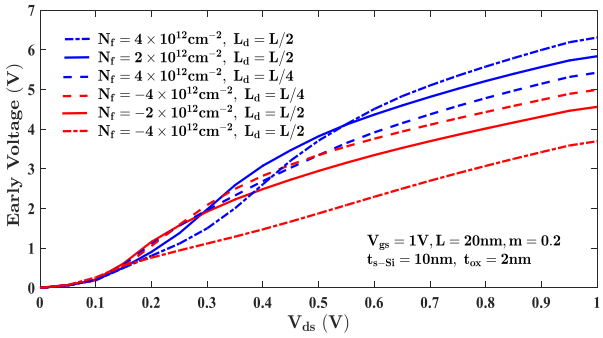

Figure 4.11: Effect of interface charge density with L_d on early voltage of GC-DMDG s-Si MOSFET when L= 20 nm.

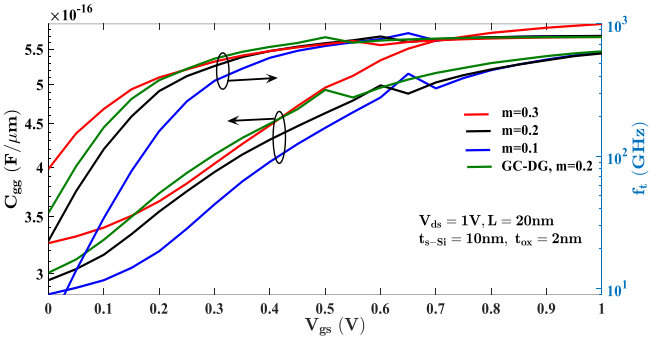

Figure 4.12: Effect of strain on C_{gg} and f_t of GC-DMDG s-Si MOSFET when L= 20 nm.

is reduced in proposed GC-DMDG s-Si MOSFET. Fig. 4-11 illustrates the variation of N_f at s-Si/SiO_2 interface on the early voltage of the GC-DMDG s-Si device for different values of L_d. For a given L_d, the early voltage of GC-DMDG s-Si MOSFET increases/decreases by increasing the positive/negative N_f due to a decrement/increment in g_d with respect to positive/negative N_f, as shown in Fig. 4-6. Thus, the effect of channel length modulation in GC-DMDG s-Si device is reduced due to positive N_f, and vice-versa for negative N_f.

Fig. 4-12 demonstrates the effect of m on total gate capacitance (C_{gg}) and f_t of GC-DMDG s-Si MOSFET. As m increases, C_{gg} of GC-DMDG s-Si MOSFET increases due to a reduction in flat-band voltage between the gate and channel of GC-DMDG s-Si MOSFET, and hence increment of inversion charges in the channel is obtained. Also, C_{gg} increases as increasing V_{gs} owing to increment of inversion charges in the channel. Moreover, by increasing the value of m, f_t of GC-DMDG s-Si MOSFET increases in weak inversion region due to an increment in g_m of GC-DMDG s-Si MOSFET in weak inversion region, as depicted in Fig. 4-1, and vice-versa in strong inversion region. From Fig. 4-12, as compared to GC-DMDG s-Si MOSFET, C_{gg} of GC-DG s-Si MOSFET is higher and f_t of GC-DG s-Si MOSFET is higher in weak inversion region due to the higher g_m of GC-DG s-Si MOSFET, and vice-versa in strong inversion region. As a result, the proposed GC-DMDG device has better unity current gain frequency in the strong inversion region compared to the GC-DG device.

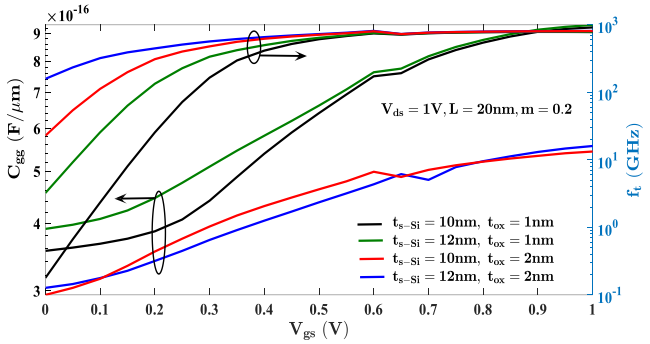

Figure 4.13: Effects of t_{ox} and t_{s-Si} on C_{gg} and f_t of GC-DMDG s-Si MOSFET when L= 20 nm.

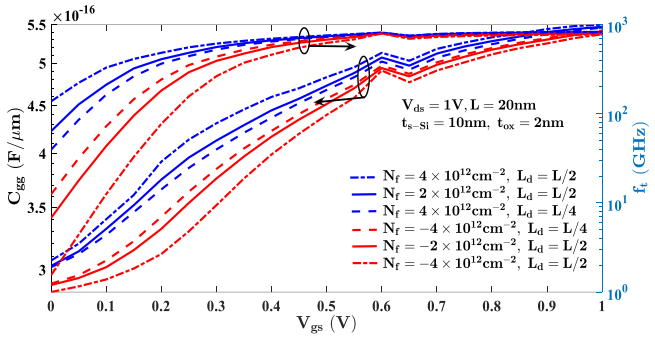

Figure 4.14: Effect of interface charge density with L_d on C_{gg} and f_t of GC-DMDG s-Si MOSFET when L= 20 nm.

Fig. 4-13 shows the variations of t_{ox} and t_{s-Si} on C_{gg} and f_t of GC-DMDG s-Si MOSFET. As t_{ox} decreases and t_{s-Si} increases, C_{gg} of GC-DMDG s-Si MOSFET increases owing to the improved gate control over the channel than drain and enhancement of inversion charges in the channel. In addition to this, f_t of GC-DMDG s-Si MOSFET increases as t_{ox} and t_{s-Si} increase because of increment in g_m with respect to thicknesses of oxide and substrate layer, as shown in Fig. 4-2.

The effect of N_f at s-Si/SiO_2 interface on C_{gg} and f_t of GC-DMDG s-Si MOSFET for different values of L_d is shown in Fig. 4-14. For a given L_d, C_{gg} of GC-DMDG s-Si MOSFET increases/decreases as positive/negative N_f increases due to increment/decrement of inversion charges in the channel of GC-DMDG s-Si MOSFET with respect to positive/negative N_f. And also, f_t of GC-DMDG s-Si MOSFET increases/decreases as positive/negative N_f increases due to enhancement/decrement in g_m of GC-DMDG s-Si MOSFET with respect to positive/negative N_f, as illustrated in Fig. 4-3.

Fig. 4-15 plots the effects of m, t_{ox}, and t_{s-Si} on voltage gain of GC-DMDG s-Si MOSFET with the operating frequency. It is observed from Fig. 4-15 that the voltage gain of GC-DMDG s-Si MOSFET decreases as m increases because of decrement in g_m in strong inversion region and increment in g_d, as shown in Fig. 4-1 and Fig. 4-4. Also, the voltage gain of GC-DMDG

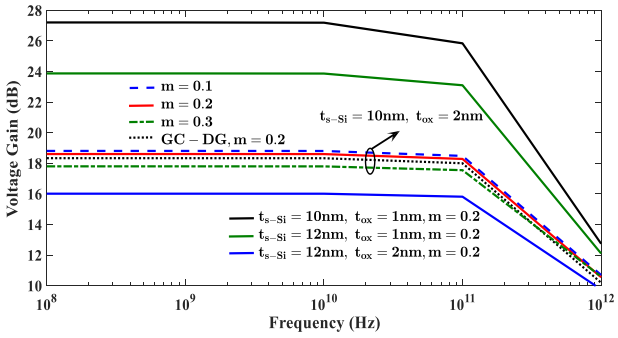

Figure 4.15: Effects of strain, t_{ox} and t_{s-Si} on voltage gain of GC-DMDG s-Si MOSFET when L= 20 nm.

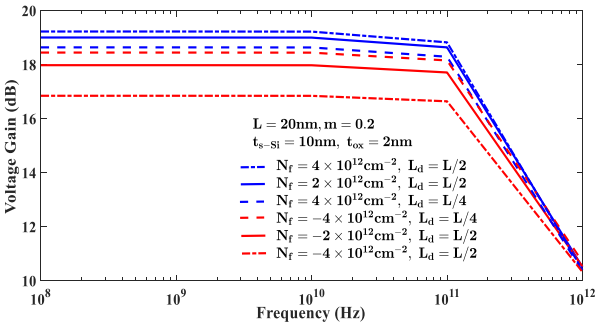

Figure 4.16: Effect of interface charge density with L_d on voltage gain of GC-DMDG s-Si MOSFET when L= 20 nm.

s-Si MOSFET decreases by increasing the values of t_{ox} and t_{s-Si} due to decrement in g_m in strong inversion region and increment in g_d, as shown in Fig. 4-2 and Fig. 4-5. Therefore, the voltage gain of GC-DMDG s-Si device is enhanced by decreasing the values of m, t_{ox}, and t_{s-Si}. Besides, the proposed GC-DMDG s-Si device has enhanced voltage gain compared to GC-DG device due to DMG structure.

Fig. 4-16 shows the variation of N_f at s-Si/SiO_2 interface with L_d on the voltage gain of the GC-DMDG s-Si device with the operating frequency. For a given L_d, the voltage gain of the GC-DMDG s-Si MOSFET decreases/increases as negative/positive N_f increases because of the decrement in g_m in strong inversion region and increment in g_d, as depicted in Fig. 4-3 and Fig. 4-6. Besides, the voltage gain of GC-DMDG s-Si MOSFET decreases as the operating frequency of the device increases due to the increased effect of the parasitic capacitances of the device.

Fig. 4-17 plots the effect of channel length on the current and power gains of GC-DMDG s-Si MOSFET with the operating frequency. Since the channel length of the device increases, current and power gains of GC-DMDG s-Si MOSFET decrease due to decrement in the drain current and g_m of GC-DMDG s-Si MOSFET. Moreover, as the operating frequency of a device

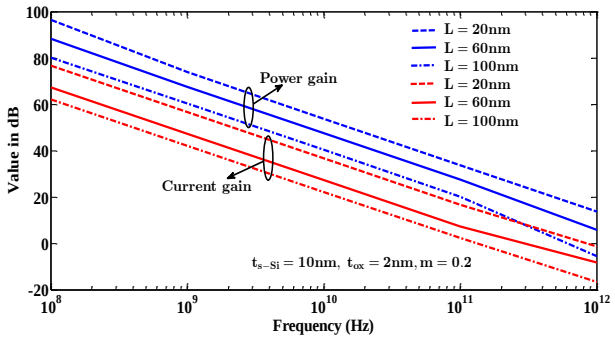

Figure 4.17: Current and Power gains of GC-DMDG s-Si MOSFET for different channel lengths.

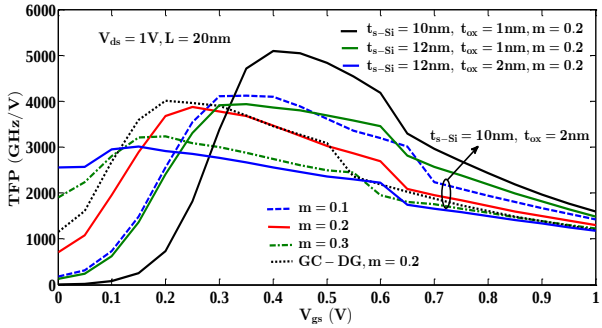

Figure 4.18: Effects of strain, t_{ox}, and t_{s-Si} on TFP of GC-DMDG s-Si MOSFET when L= 20 nm.

increases, current and power gains of GC-DMDG s-Si MOSFET decrease because of the increased effect of parasitic capacitances of the device. Besides, the effects of m, N_f, t_{ox}, and t_{s-Si} on the current and power gains of GC-DMDG s-Si MOSFET with the operating frequency is very small.

The effects of m, t_{ox} and t_{s-Si} on TFP of GC-DMDG s-Si MOSFET are shown in Fig. 4-18. From Fig. 4-18, it is noticed that TFP of GC-DG s-Si MOSFET is increased by reducing the values of m, t_{ox} and t_{s-Si} in moderate inversion region and the reverse trend is observed in weak inversion region. Moreover, the peak value of TFP is obtained in moderate inversion region. It is evident from Fig. 4-18 that the TFP of proposed GC-DMDG s-Si MOSFET is better than GC-DG s-Si MOSFET above the weak inversion region, and vice-versa in the weak inversion region. Therefore, for the proposed GC-DMDG s-Si MOSFET, optimized analog/RF performance is obtained in the moderate inversion region. The peak of TFP of GC-DG s-Si MOSFET is achieved at different values of V_{gs} with respect to m, t_{ox}, and t_{s-Si} in moderate inversion region owing to variation in threshold voltage of GC-DMDG s-Si MOSFET.

Fig. 4-19 depicts the effect of N_f at s-Si/SiO_2 interface on TFP of the GC-DMDG s-Si MOSFET for different values of L_d. For a given L_d, TFP of GC-DMDG s-Si device increas-

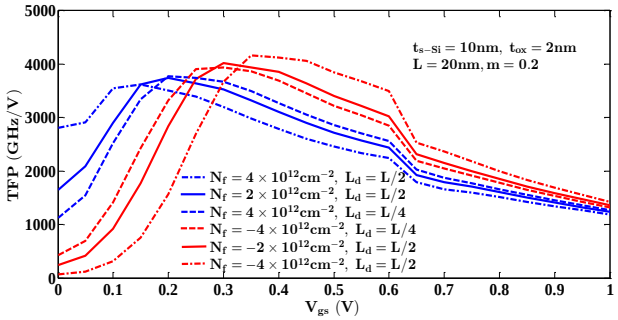

Figure 4.19: Effect of interface charge density with L_d on TFP of GC-DMDG s-Si MOSFET when L= 20 nm.

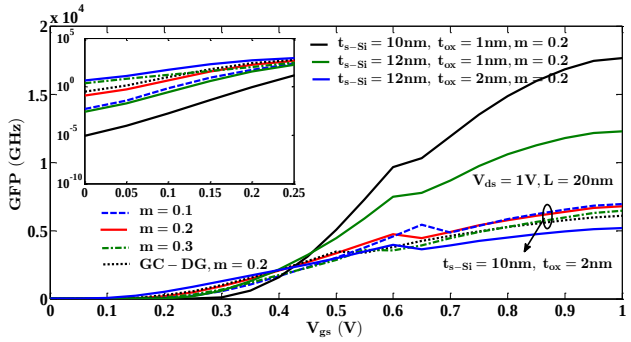

Figure 4.20: Effects of strain, t_{ox}, and t_{s-Si} on GFP of GC-DMDG s-Si MOSFET when L= 20 nm.

es/decreases as increasing negative/positive N_f at s-Si/SiO_2 interface in moderate and strong inversion regions and the reverse trend is observed in weak inversion region. Moreover, the maximum value of TFP of GC-DMDG s-Si MOSFET is attained at different V_{gs} values with respect to N_f in the moderate inversion region due to alteration in the threshold voltage of GC-DMDG s-Si MOSFET.

The variations of m, t_{ox}, and t_{s-Si} on GFP of GC-DMDG s-Si MOSFET are shown in Fig. 4-20. From Fig. 4-20, it is observed that GFP of GC-DMDG s-Si MOSFET is increased by reducing the values of m, t_{ox}, and t_{s-Si} in a strong inversion region and the reverse trend is observed in weak inversion region. Also, GFP of the proposed GC-DMDG s-Si MOSFET is higher than GC-DG s-Si MOSFET in strong inversion region, and vice-versa in the weak inversion region.

Fig. 4-21 shows the variation of N_f at s-Si/SiO_2 interface on GFP of the GC-DMDG s-Si MOSFET for different values of L_d. For a given L_d, GFP of GC-DMDG s-Si device increases/decreases as positive/negative N_f at s-Si/SiO_2 interface increases. It is observed from Fig. 4-20 and Fig. 4-21 that the higher peak values of GFP of GC-DMDG s-Si MOSFET are attained by decreasing the values of m, t_{ox}, and t_{s-Si}.

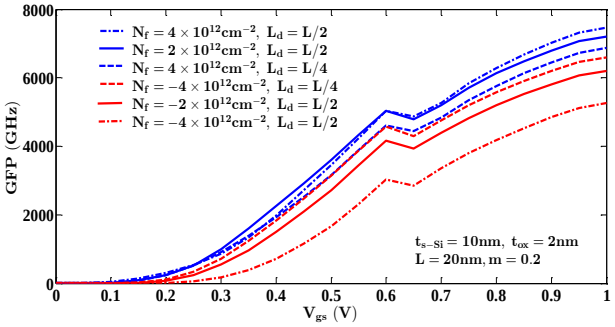

Figure 4.21: Effect of interface charge density with L_d on GFP of GC-DMDG s-Si MOSFET when L= 20 nm.

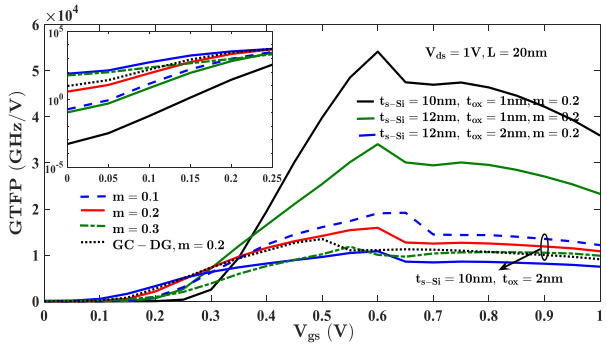

Figure 4.22: Effects of strain, t_{ox}, and t_{s-Si} on GTFP of GC-DMDG s-Si MOSFET when L= 20 nm.

The effects of m, t_{ox}, and t_{s-Si} on GTFP of GC-DMDG s-Si MOSFET are shown in Fig. 4-22. The GTFP of GC-DMDG s-Si MOSFET is increased by reducing the values of m, t_{ox}, and t_{s-Si} in a strong inversion region and the reverse trend is observed in the subthreshold region. Besides, the peak value of GTFP of the proposed device is observed in the strong inversion region. It is clear from Fig. 4-22 that the GTFP of proposed GC-DMDG s-Si MOSFET is higher than GC-DG s-Si MOSFET in a strong inversion region, and vice-versa in the subthreshold region. As shown in Fig. 4-22, the proposed GC-DMDG s-Si MOSFET shows improved analog/RF performance by decreasing the values of t_{ox} and t_{s-Si}.

Fig. 4-23 shows the variation of N_f at s-Si/SiO_2 interface on GTFP of the GC-DMDG s-Si MOSFET for different values of L_d. For a given L_d when $4\times10^{12} \leq N_f \leq -2\times10^{12}$, it is noticed that the GTFP of GC-DMDG s-Si device increases/decreases as positive/negative N_f increases at s-Si/SiO_2 interface in the weak inversion region, and vice-versa in strong inversion region. On the other hand, GTFP of GC-DMDG s-Si MOSFET decreases when $N_f > -2\times10^{12}$ due to the DIBL effect. From Fig. 4-23, it is noticed that the peak value of GTFP of GC-DMDG s-Si MOSFET is obtained at a V_{gs}, which is greater than the threshold voltage. Thus, it is noticed that the analog/RF figures of merit of the proposed GC-DMDG s-Si MOSFET is altered with respect to interface charges, as illustrated in Fig. 4-23.

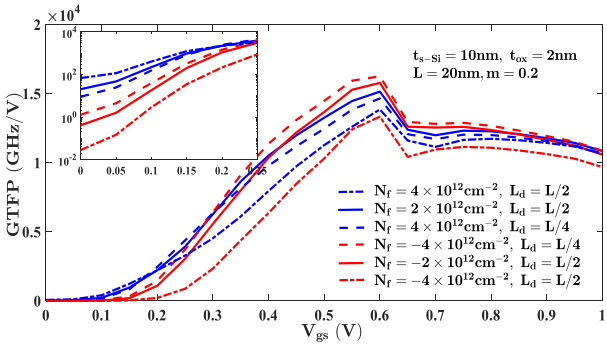

Figure 4.23: Effect of interface charge density with L_d on GTFP of GC-DMDG s-Si MOSFET when L= 20 nm.

Table 4.1: Performance evaluation of the proposed GC s-Si MOSFET with the literature.

Device	**g_m, mS**	**$\left(\frac{I_d}{g_d}\right)$, V**	**$\left(\frac{g_m}{I_d}\right)$, V^{-1}**	**$\left(\frac{g_m}{g_d}\right)$, dB**	**C_{gg}, fF**	**f_t, GHz**
GC-DG s-Si MOSFET	2.35	5.3	30.9	8.80	0.547	795
GC-DMDG s-Si MOSFET	4.00	11.1	33.3	13.54	0.924	783
high-k DG MOSFET [87]	3.35	3.3	26.5	23	–	–
GCDMDG MOSFET [42]	5.2	3.0	26	12.3	–	790
GCGS DG-MOSFET [52]	2.9	–	23	11.3	0.65	680

The performance of the proposed GC-DMDG s-Si MOSFET is compared with the previous works, as demonstrated in Table 4-1. It is observed from Table 4-1 that the proposed GC-DMDG s-Si device (m= 0.2 and t_{ox}= 1 nm) has higher values of g_m, TGF, early voltage, and f_t, compared to GC-DG s-Si device (m= 0.2 and t_{ox}= 2 nm), Nanoscale GCDMDG MOSFET with channel length 15 nm [42], graded channel and gate stack DG-MOSFET [52], and high-k dielectric DG MOSFET with channel length 20 nm [87]. However, the proposed GC-DMDG s-Si MOSFET has lower $\frac{g_m}{g_d}$ ratio than high-k dielectric DG MOSFET with channel length 20 nm [87]. Moreover, the proposed GC-DMDG s-Si MOSFET has lower g_m than Nanoscale GCDMDG MOSFET with channel length 15 nm [42]. Therefore, the overall analog/RF performance of the proposed GC-DMDG s-Si MOSEFT has attained improved characteristics using the DMG structure with GC engineering.

4.3 Analog/RF performance of GCGS-TMDG s-Si MOSFET with interface charges.

In this work, the performance evaluation of analog/RF of GCGS-TMDG s-Si MOSFET with fixed charges at s-Si/SiO_2 interface is demonstrated. The GC channel is obtained in s-Si substrate of GCGS-TMDG s-Si MOSFET by doping three different uniform concentrations.

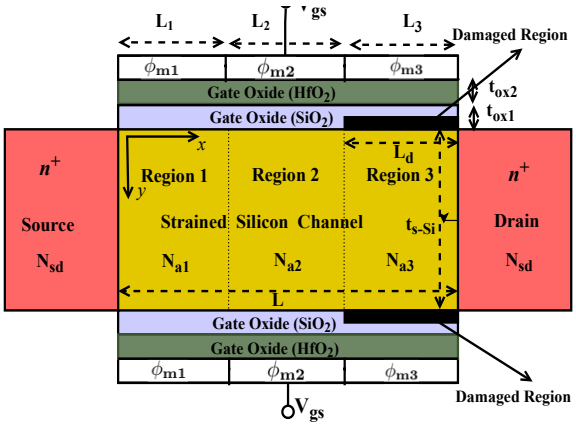

Figure 4.24: Structure of symmetrical GCGS-TMDG s-Si MOSFET with interface charges.

Table 4.2: Parameters and dimensions considered in simulation of GCGS-TMDG s-Si device

S. No.	Parameters	Variables	Dimensions
1	Length of s-Si channel	L	15 nm
2	doping of s-Si channel	N_{a1}, N_{a2}, N_{a3}	10^{17}, 5×10^{16}, 10^{16} cm^{-3}
3	Doping of Source/Drain regions	N_{sd}	10^{20} cm^{-3}
4	s-Si thickness	t_{s-Si}	6 nm
5	Oxide thickness	t_{ox1}, t_{ox2}	0.6, 1 nm
6	Work functions of control gate, and screen gate	$\phi_{m1}, \phi_{m2}, \phi_{m2}$	4.8, 4.6, 4.4 eV
7	Gate to source voltage	V_{gs}	0 - 1 V
8	Drain to source voltage	V_{ds}	0 - 1 V
9	Ge mole fraction	m	0.1 - 0.3
10	Interface charge density	N_f	-4×10^{12} - 4×10^{12} cm^{-2}
11	Applied frequency	f_0	0.1 - 1000 GHz

The analog/RF figure of merits of the proposed GCGS-TMDG s-Si MOSFET for various values of m, N_f with different damaged lengths, and the thicknesses of different high-k dielectric materials are exhaustively evaluated by using Sentaurus TCAD.

The analog/RF parameters of the GCGS-TMDG s-Si MOSFET are enhanced by increasing the values of m, positive N_f, and thickness of oxide layer in the sub-threshold region, and vice-versa in the above threshold region. Moreover, for the proposed GCGS-TMDG s-Si MOSFET, better performances of analog/RF parameters are obtained in moderate inversion region when compared to GCGS-DG s-Si MOSFET.

4.3.1 Proposed device structure

The 2-D diagram of GCGS-TMDG s-Si device with fixed charges is shown in Fig. 4-24. The graded s-Si channel region is split into three regions of lengths L_1, L_2, and L_3, which are

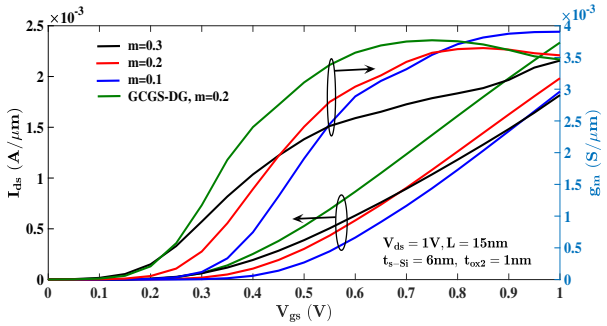

Figure 4.25: Variation of strain on transfer characteristics and g_m of GCGS-TMDG s-Si MOSFET when L= 15 nm.

doped with different uniform doping concentrations N_{a1}, N_{a2}, and N_{a3}, respectively. Control and screen gates, which have different work functions ϕ_{m1}, ϕ_{m2}, and ϕ_{m3}, are combined to attain the top and bottom gates of the GCGS-TMDG s-Si MOSFET. Control gate material is placed over graded channel region 1 and screen gate materials are placed over graded channel regions 2 and 3. In GCGS-DG s-Si MOSFET, a single gate material with an average work function of ϕ_{m1}, ϕ_{m2}, and ϕ_{m3} is used. Owing to HCEs, fixed charges are introduced at SiO_2/s-Si interface of GCGS-TMDG s-Si MOSFET and can be approximated as the damaged region of length L_d, as illustrated in Fig. 4-24. The values of different parameters of the proposed GCGS-TMDG s-Si MOSFET, which are used in TCAD simulation, are given in Table 4-2.

4.3.2 Results and discussion

For the proposed GCGS-TMDG s-Si MOSFET, Fig. 4-25 depicts the variation of strain in silicon channel on transfer characteristics and transconductance for V_{ds}=1 V. It is observed from Fig. 4-25 that the better transfer characteristics and higher g_m are attained in GCGS-DG s-Si MOSFET when compared to the proposed GCGS-TMDG s-Si MOSFET owing to lower threshold voltage of GCGS-DG s-Si MOSFET. In subthreshold region, as strain increases in the silicon channel, threshold voltage of GCGS-TMDG s-Si MOSFET decreases. Consequently, enhanced drain current and higher g_m are obtained.

The effect of t_{ox2} on $V_{gs} - I_{ds}$ and g_m with various gate stacks is illustrated in Fig. 4-26. It is observed from Fig. 4-26 that HfO_2/SiO_2 gate stack of GCGS-TMDG s-Si MOSFET has better transfer characteristics and higher value of g_m when compared to Si_3N_4/SiO_2 gate stack in strong inversion region owing to higher permittivity of HfO_2, and vice-versa in subthreshold region. Moreover, as t_{ox2} of GCGS-TMDG MOSFET decreases, drain current and g_m increase in strong inversion region owing to the greater gate control over the s-Si channel than the drain, and vice-versa in subthreshold region.

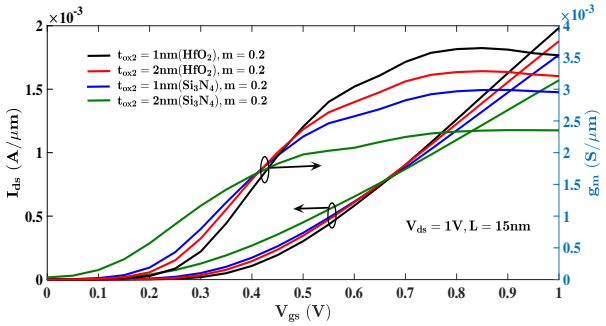

Figure 4.26: Effect of t_{ox2} on transfer characteristics and g_m of GCGS-TMDG s-Si MOSFET for different gate stacks.

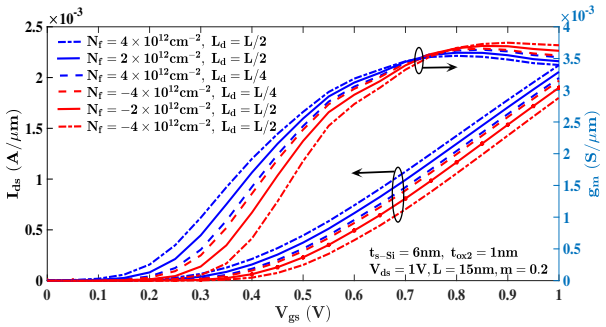

Figure 4.27: Effect of N_f with damaged length on transfer characteristics and g_m of GCGS-TMDG s-Si MOSFET for L= 15 nm.

At V_{ds}= 1V, the effect of fixed charge density at SiO_2/s-Si interface with damaged length on the $V_{gs} - I_{ds}$ and g_m is shown in Fig. 4-27. It is noticed from Fig. 4-27 that both the transfer characteristics and transconductance of GCGS-TMDG s-Si MOSFET increase in sub-threshold region as the positive N_f increases because of diminution in threshold voltage of GCGS-TMDG s-Si device for positive fixed charge density, and vice-versa for negative fixed charge density. Besides, as positive N_f increases in the GCGS-TMDG s-Si MOSFET, the minimum channel potential increases, thereby the threshold voltage of proposed MOSFET decreases, and vice-versa for negative N_f. Hence, the performance of analog/RF parameters of the proposed GCGS-TMDG s-Si device is affected with respect to the fixed charge density at SiO_2/s-Si interface with damaged length.

Fig. 4-28 depicts the effect of the strain in silicon channel on output characteristics and output conductance for V_{gs}= 1 V. It is observed from Fig. 4-28 that the GCGS-DG s-Si MOSFET has better output characteristics and higher value of g_d when compared to proposed GCGS-TMDG s-Si MOSFET because of lower threshold voltage of GCGS-DG s-Si MOSFET. Therefore, the effect of V_{ds} on s-Si channel of proposed GCGS-TMDG s-Si MOSFET is less than GCGS-DG s-Si MOSFET because of the TMG structure in proposed GCGS-TMDG s-Si MOSFET. Moreover, enhanced output characteristics and g_d of GCGS-TMDG s-Si MOSFET

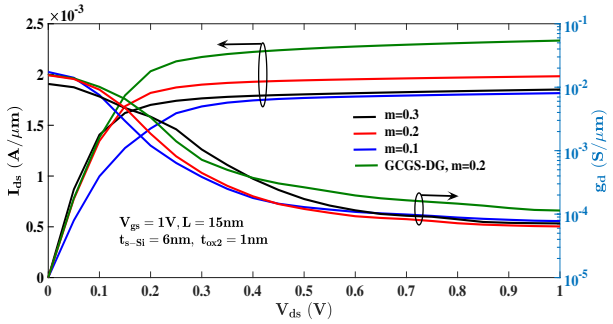

Figure 4.28: Variation of strain on output characteristics and g_d of GCGS-TMDG s-Si MOSFET when L= 15 nm.

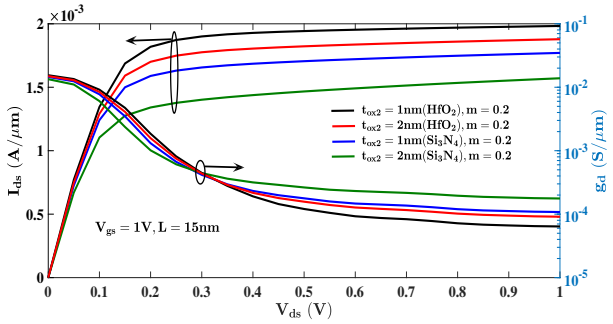

Figure 4.29: Effect of t_{ox2} on output characteristics and g_d of GCGS-TMDG s-Si MOSFET for different gate stacks.

are obtained by increasing the strain due to reduction in the threshold voltage of GCGS-TMDG s-Si MOSFET.

The effect of t_{ox2} on output characteristics and g_d of GCGS-TMDG s-Si MOSFET for various gate stacks is shown in Fig. 4-29. Among different high-k dielectric materials used in gate stack of proposed device, the proposed GCGS-TMDG s-Si MOSFET with HfO_2/SiO_2 gate stack exhibits improved output characteristics and low g_d than GCGS-TMDG s-Si device with Si_3N_4/SiO_2 gate stack due to higher permittivity of HfO_2. Also, in GCGS-TMDG s-Si MOSFET, as t_{ox2} decreases, SCEs are diminished, thereby enhanced output characteristics and low g_d are attained.

Fig. 4-30 illustrates the variation of N_f at SiO_2/s-Si interface with damaged length on the output characteristics and g_d of GCGS-TMDG s-Si MOSFET for V_{gs}= 1 V. It is noticed from Fig. 4-30 that the better (worse) output characteristics of GCGS-TMDG s-Si MOSFET are observed by increasing the positive (negative) N_f since threshold voltage of GCGS-TMDG s-Si MOSFET decreases (increases) for positive (negative) N_f. Moreover, low (high) value of output conductance is observed at low (high) drain voltages by increasing the negative N_f due to DIBL effect, and vice-versa for positive N_f.

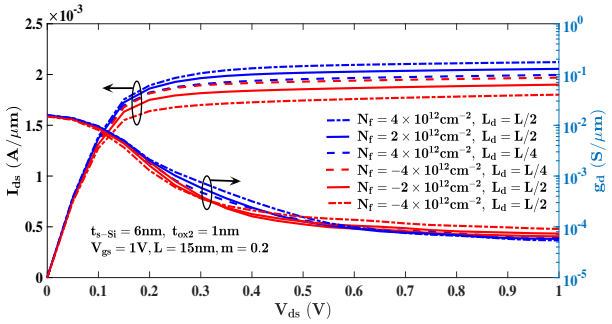

Figure 4.30: Effect of N_f with damaged length on output characteristics and g_d of GCGS-TMDG s-Si MOSFET for L= 15 nm.

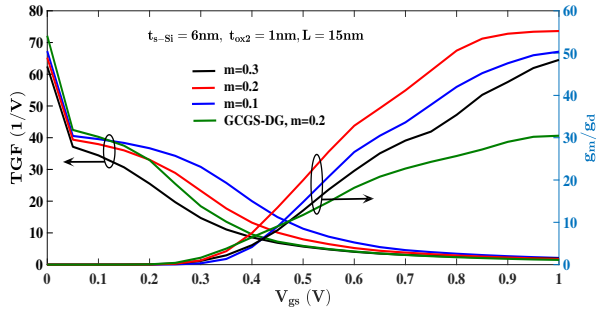

Figure 4.31: Variation of strain on TGF and intrinsic gain of GCGS-TMDG s-Si MOSFET with L= 15 nm.

The effect of strain on the TGF and intrinsic gain of GCGS-TMDG s-Si MOSFET is demonstrated in Fig. 4-31. As shown in Fig. 4-31, the proposed GCGS-TMDG s-Si MOSFET has higher TGF and higher intrinsic gain in comparison with GCGS-DG s-Si MOSFET because of the TMG structure of GCGS-TMDG s-Si MOSFET. Hence, the proposed device has higher power conversion efficiency than GCGS-DG s-Si MOSFET due to less SCEs. Also, as strain in silicon channel decreases, the transconductance generation factor and intrinsic gain of GCGS-TMDG s-Si MOSFET increase due to increase in the transconductance of GCGS-TMDG s-Si MOSFET, as depicted in Fig. 4-25. Moreover, as V_{gs} increases, $\frac{g_m}{g_d}$ of GCGS-TMDG s-Si MOSFET increases due to the increase in the inversion charge carriers of s-Si channel.

Fig. 4-32 depicts the variation of t_{ox2} on TGF and intrinsic gain of GCGS-TMDG s-Si MOSFET for various gate stacks. It is obvious from Fig. 4-32 that the increment in the values of TGF and intrinsic gain are observed by decreasing t_{ox2} of GCGS-TMDG s-Si device since g_m increases and g_d decreases, as illustrated in Fig. 4-26 and Fig. 4-29. Moreover, GCGS-TMDG s-Si MOSFET with HfO_2/SiO_2 gate stack has higher values of TGF and intrinsic gain in comparison with the Si_3N_4/SiO_2 gate stack. Thus, the proposed GCGS-TMDG s-Si MOSFET with HfO_2/SiO_2 gate stack has higher power conversion efficiency when compared to the proposed GCGS-TMDG s-Si MOSFET with Si_3N_4/SiO_2 gate stack.

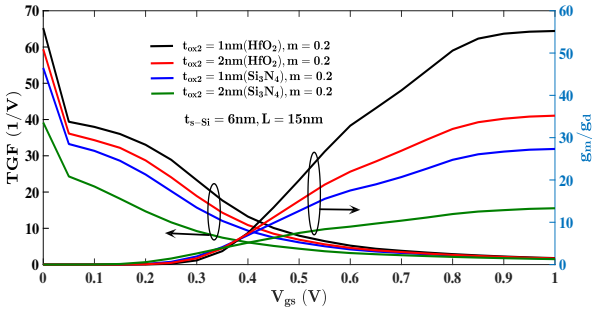

Figure 4.32: Effect of t_{ox2} on TGF and intrinsic gain of GCGS-TMDG s-Si MOSFET for different gate stacks.

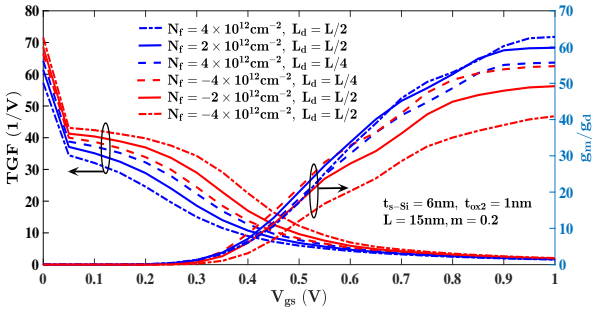

Figure 4.33: Effect of fixed charge density for different L_d on TGF and intrinsic gain of GCGS-TMDG s-Si MOSFET for L= 15 nm.

Fig. 4-33 depicts the variation of fixed charge density at SiO_2/s-Si interface on TGF and intrinsic gain of GCGS-TMDG s-Si device for various values of L_d. The increment in TGF of GCGS-TMDG s-Si MOSFET is attained due to the increment in V_{th} when negative fixed charge density with damaged length increases, and vice-versa for positive fixed charge density. Moreover, the intrinsic gain of the proposed device increases due to increment (decrement) in g_m (g_d) as positive N_f with L_d increases, as depicted in Fig. 4-27 and Fig. 4-30, and reverse trend is obtained when negative fixed charge density increases.

Fig. 4-34 illustrates the effects of strain in silicon channel and t_{ox2} on early voltage of GCGS-TMDG s-Si device. As shown in Fig. 4-34, it is observed that proposed GCGS-TMDG s-Si device has higher early voltage than GCGS-DG s-Si device owing to low g_d and TMG structure of GCGS-TMDG s-Si device. Besides, as strain increases and t_{ox2} decreases, the increment in early voltage of proposed GCGS-TMDG s-Si device is attained due to decrement in g_d, as depicted in Fig. 4-28 and Fig. 4-29. Also, higher early voltage is obtained for HfO_2/SiO_2 gate stack of GCGS-TMDG s-Si device when compared to Si_3N_4/SiO_2 gate stack of GCGS-TMDG s-Si device because of low g_d of HfO_2/SiO_2 gate stack, as shown in Fig. 4-28.

The effect of fixed charge density at SiO_2/s-Si interface on early voltage of proposed GCGS-TMDG s-Si device with damaged length is shown in Fig. 4-35. The early voltage

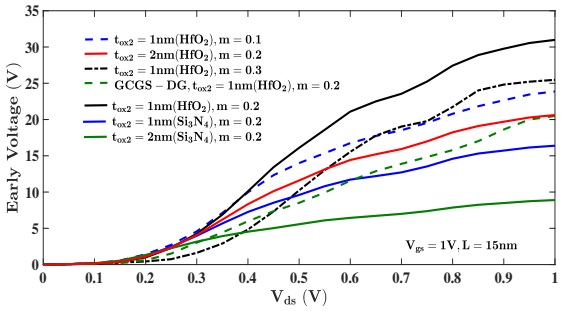

Figure 4.34: Effects of strain and t_{ox2} on early voltage of GCGS-TMDG s-Si MOSFET when L= 15 nm.

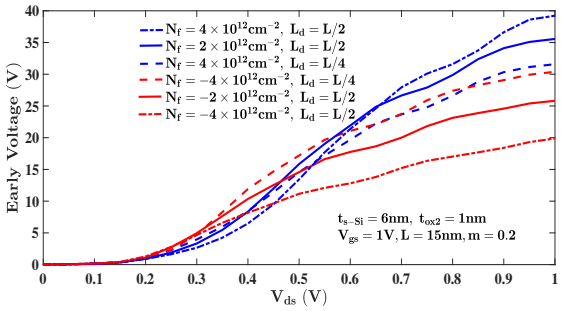

Figure 4.35: Effect of fixed charge density for different L_d on early voltage of GCGS-TMDG s-Si device when L= 15 nm.

of the GCGS-TMDG s-Si device increases (decreases) due to the decrement (increment) in output conductance as positive (negative) fixed charge density at SiO_2/s-Si interface increases, as depicted in Fig. 4-30. Thus, the channel length modulation of GCGS-TMDG s-Si device decreases (increases) as the positive (negative) fixed charge density increases. It is because of the fact that the effect of V_{ds} is less (more) on drain characteristics for positive (negative) fixed charge density.

Fig. 4-36 illustrates the variation of strain on total gate capacitance and f_t of GCGS-TMDG s-Si MOSFET. As strain increases, C_{gg} and f_t of GCGS-TMDG s-Si MOSFET increase owing to decrease in flat-band voltage of the GCGS-TMDG s-Si MOSFET. Moreover, by increasing the gate to source voltage, the increment in C_{gg} is obtained due to an enhancement

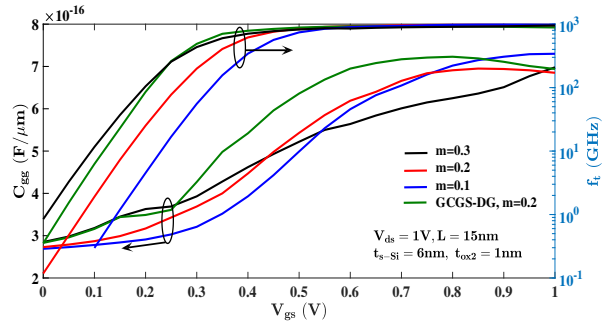

Figure 4.36: Variation of strain on C_{gg} and f_t of GCGS-TMDG s-Si device when L= 15 nm.

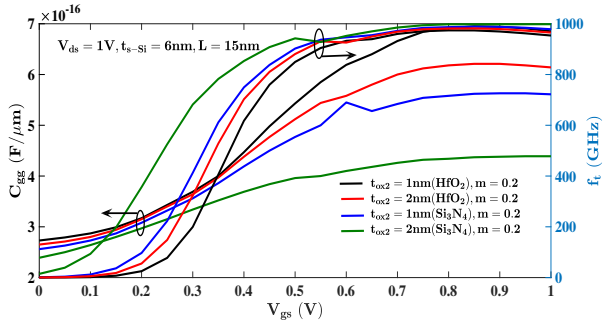

Figure 4.37: Effect of t_{ox2} on C_{gg} and f_t of GCGS-TMDG s-Si MOSFET for different gate stacks.

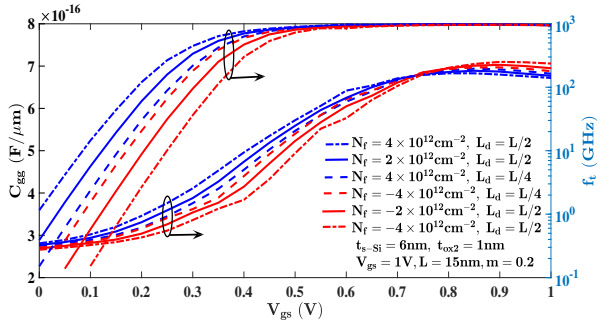

Figure 4.38: The effect of fixed charge density for various values of L_d on the C_{gg} and f_t of GCGS-TMDG s-Si MOSFET when L= 15 nm.

of the inversion carriers in the s-Si channel. Also, the proposed device has lower value of C_{gg} when compared to GCGS-DG s-Si device due to the high threshold voltage of GCGS-TMDG s-Si MOSFET. Besides, the proposed device has lower value of f_t when compared to GCGS-DG s-Si MOSFET due to low g_m of GCGS-TMDG s-Si MOSFET, as shown in Fig. 4-25.

The effect of t_{ox2} on C_{gg} and f_t of GCGS-TMDG s-Si MOSFET for different gate stacks is illustrated in Fig. 4-37. As t_{ox2} decreases, C_{gg} of GCGS-TMDG s-Si device increases since gate has more control than the drain in s-Si channel. In addition, higher C_{gg} is obtained for HfO_2/SiO_2 gate stack than Si_3N_4/SiO_2 gate stack in GCGS-TMDG s-Si device. Moreover, f_t of GCGS-TMDG s-Si MOSFET increases owing to increment in g_m when t_{ox2} increases, as depicted in Fig. 4-26. Also, higher f_t is attained for HfO_2/SiO_2 gate stack than Si_3N_4/SiO_2 gate stack in GCGS-TMDG s-Si device.

The effect of fixed charge density at SiO_2/s-Si interface on C_{gg} and f_t of GCGS-TMDG s-Si device for various values of damaged length is illustrated in Fig. 4-38. C_{gg} of GCGS-TMDG s-Si device increases due to increment of inversion carriers in s-Si channel as positive fixed charge density increases, and vice-versa for negative fixed charge density. And also, f_t of GCGS-TMDG s-Si device increases due to the increment in g_m as positive fixed charge density

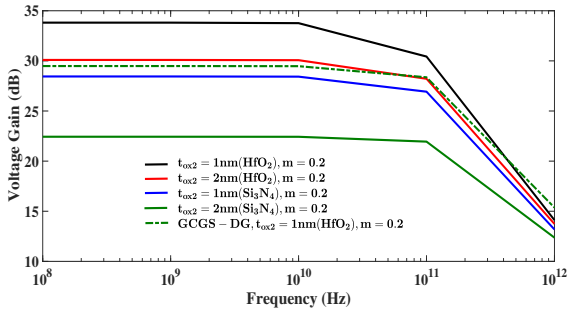

Figure 4.39: Effect of t_{ox2} on voltage gain of GCGS-TMDG s-Si MOSFET with L= 15 nm.

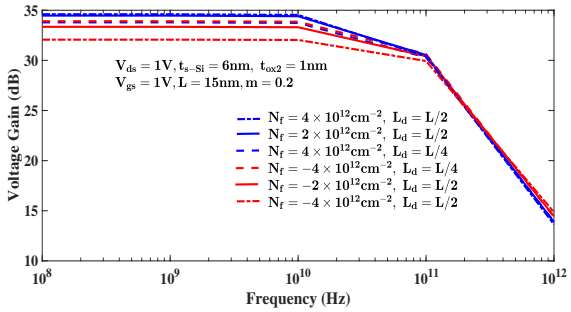

Figure 4.40: Effect of fixed charge density for different L_d on the voltage gain of GCGS-TMDG s-Si MOSFET with L= 15 nm.

increases at SiO_2/s-Si interface, and vice-versa for negative fixed charge density, as depicted in Fig. 4-27.

Fig. 4-39 depicts the effect of t_{ox2} on voltage gain of GCGS-TMDG s-Si MOSFET at various operating frequencies. As t_{ox2} decreases, the voltage gain of GCGS-TMDG s-Si MOSFET increases because of increment in transconductance and decrement in output conductance, as illustrated in Fig. 4-26 and Fig. 4-29. Furthermore, more increase in the voltage gain of GCGS-TMDG s-Si MOSFET is observed for HfO_2/SiO_2 gate stack than Si_3N_4/SiO_2 gate stack. Moreover, the voltage gain of the proposed GCGS-TMDG s-Si MOSFET is higher than GCGS-DG s-Si MOSFET due to the TMG structure of the proposed GCGS-TMDG s-Si MOSFET.

The effect of fixed charge density at SiO_2/s-Si interface on voltage gain of the GCGS-TMDG s-Si device at various operating frequencies is shown in Fig. 4-40. As positive fixed charge density with damaged length increases, the voltage gain of the proposed device increases due to the increment in g_m and decrement in g_d, as shown in Fig. 4-27 and Fig. 4-30. Also, voltage gain of proposed MOSFET decreases as the operating frequency increases. The reason behind the decrease in voltage gain is the increment in parasitic capacitances of the device.

Fig. 4-41 plots the effects of strain and t_{ox2} on unity power gain frequency of GCGS-TMDG s-Si MOSFET for different gate stacks. Since the strain in silicon channel increases

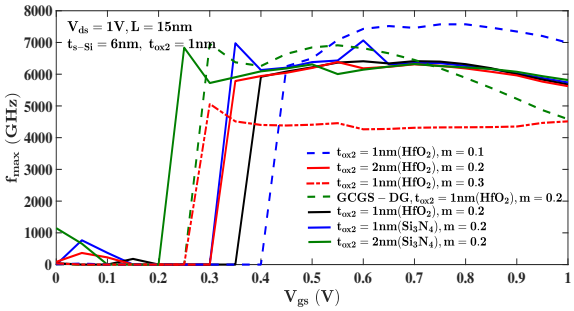

Figure 4.41: Effects of strain and t_{ox2} on f_{max} of GCGS-TMDG s-Si MOSFET for different gate stacks.

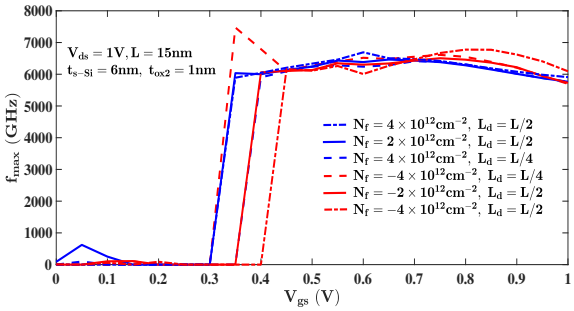

Figure 4.42: Effect of fixed charge density with damaged length on f_{max} of GCGS-TMDG s-Si MOSFET.

and t_{ox2} decreases, f_{max} of GCGS-TMDG s-Si MOSFET increases. Besides, higher f_{max} is obtained for Si_3N_4/SiO_2 gate stack when compared to HfO_2/SiO_2 gate stack in GCGS-TMDG s-Si MOSFET. Moreover, the proposed GCGS-TMDG s-Si MOSFET has lower unity power gain frequency when compared to GCGS-DG s-Si MOSFET. The variation of fixed charge density with damaged length on f_{max} of GCGS-TMDG s-Si MOSFET is demonstrated in Fig. 4-42. It is observed from Fig. 4-42 that the increment in f_{max} of GCGS-TMDG s-Si device is attained as negative fixed charge density increases with damaged length, and vice-versa for positive fixed charge density.

The effects of strain and t_{ox2} on TFP of GCGS-TMDG s-Si MOSFET are demonstrated in Fig. 4-43. It is identified from Fig. 4-43 that the TFP of the proposed GCGS-TMDG s-Si

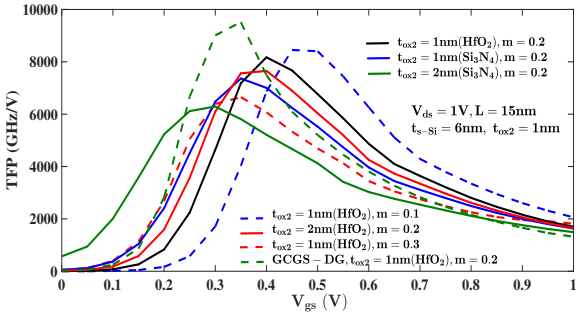

Figure 4.43: Effects of strain and t_{ox2} on TFP of GCGS-TMDG s-Si MOSFET with L= 15 nm.

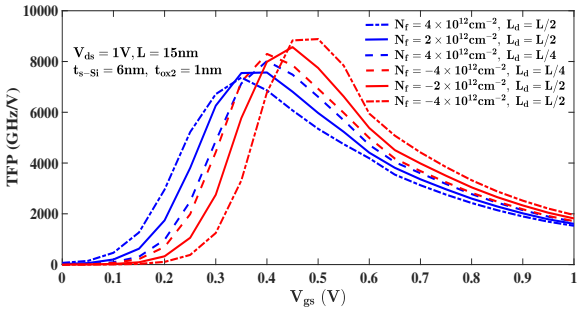

Figure 4.44: Effect of fixed charge density with damaged length on TFP of GCGS-TMDG s-Si MOSFET with L= 15 nm.

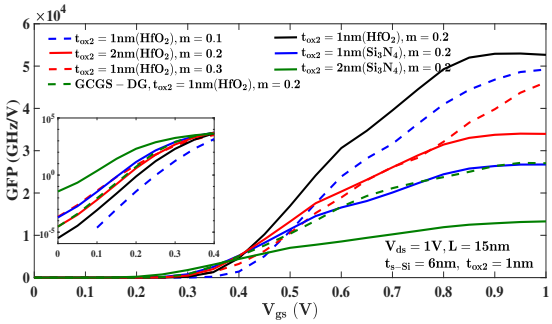

Figure 4.45: Effects of strain and t_{ox2} on GFP of GCGS-TMDG s-Si MOSFET with L= 15 nm.

MOSFET is lower than the TFP of the GCGS-DG s-Si MOSFET in above the sub-threshold region. Besides, it is seen that the TFP of GCGS-TMDG s-Si device increases in moderate inversion region as strain and t_{ox2} decrease, and reverse trend follows in sub-threshold region. Furthermore, higher TFP is obtained for HfO_2/SiO_2 gate stack than Si_3N_4/SiO_2 gate stack in GCGS-TMDG s-Si device.

The effect of fixed charge density with damaged length at SiO_2/s-Si interface on TFP of the GCGS-TMDG s-Si MOSFET is shown in Fig. 4-44. Enhancement/decrement in TFP of GCGS-TMDG s-Si MOSFET is observed by increasing the negative/positive fixed charge density at SiO_2/s-Si interface with damaged length in the moderate inversion region, and reverse trend follows in the sub-threshold region. Besides, the peak value of TFP of proposed GCGS-TMDG s-Si MOSFET is obtained at different gate to source voltages corresponding to fixed charge density due to change in threshold voltage of GCGS-TMDG s-Si device.

The effects of strain and t_{ox2} on GFP of GCGS-TMDG s-Si device are shown in Fig. 4-45. It is noticed from Fig. 4-45 that enhancement in GFP of GCGS-TMDG s-Si MOSFET is accomplished by decreasing the values of strain and t_{ox2} in above threshold region and the opposite trend is noticed in sub-threshold region. Also, GFP of proposed GCGS-TMDG s-Si MOSFET is more than GCGS-DG s-Si MOSFET in above threshold region, and reverse trend

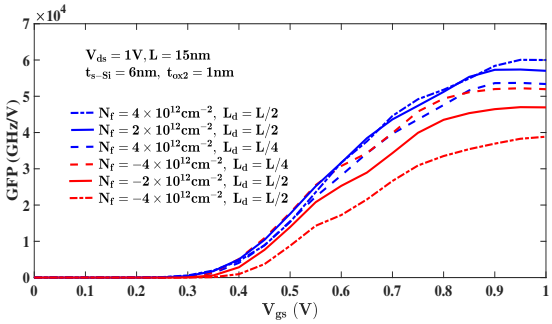

Figure 4.46: Effect of fixed charge density with damaged length on TFP of GCGS-TMDG s-Si MOSFET with L= 15 nm.

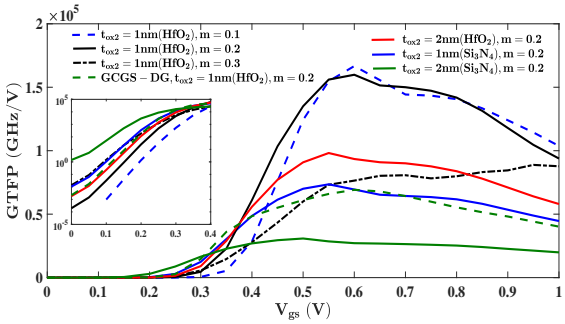

Figure 4.47: Effects of strain and t_{ox2} on GTFP of GCGS-TMDG s-Si MOSFET with L= 15 nm.

follows in below threshold region. Moreover, higher GFP is attained for HfO_2/SiO_2 gate stack than Si_3N_4/SiO_2 gate stack in GCGS-TMDG s-Si device.

Fig. 4-46 depicts the effect of fixed charge density at SiO_2/s-Si interface with damaged length on GFP of the GCGS-TMDG s-Si MOSFET. As positive/negative fixed charge density at SiO_2/s-Si interface with damaged length increases, increment/decrement in GFP of GCGS-TMDG s-Si MOSFET is attained owing to higher values of intrinsic gain and f_t with respect to positive N_f, as shown in Fig. 4-33 and Fig. 4-37.

Fig. 4-47 plots the effects of strain and t_{ox2} on GTFP of GCGS-TMDG s-Si device. The GTFP of GCGS-TMDG s-Si MOSFET increases by decreasing the values of strain and t_{ox2} in the above threshold voltage region and the opposite trend is noticed in the sub-threshold region. Furthermore, increase in GTFP for HfO_2/SiO_2 gate stack is more than the Si_3N_4/SiO_2 gate stack in GCGS-TMDG s-Si device. Besides, the maximum value of GTFP of proposed GCGS-TMDG s-Si MOSFET is obtained in the above threshold region. It is clearly observed from Fig. 4-47 that the GTFP of proposed GCGS-TMDG s-Si MOSFET is greater than the GCGS-DG s-Si MOSFET in above threshold voltage region, and reverse trend follows in below threshold region.

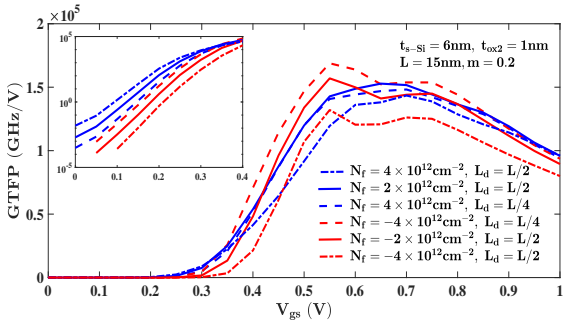

Figure 4.48: Effect of fixed charge density with damaged length on GTFP of GCGS-TMDG s-Si MOSFET with L= 15 nm.

Table 4.3: The performance evaluation of proposed GCGS-TMDG s-Si device with previous works.

Device	**g$_m$, S**	**$\left(\frac{I_d}{g_d}\right)$, V**	**$\left(\frac{g_m}{I_d}\right)$, V^{-1}**	**$\left(\frac{g_m}{g_d}\right)$**	**C$_{gg}$, fF**	**f$_t$, GHz**	**GTFP, (THz/V)**
GCGS-DG s-Si MOSFET	3.78	20.5	72.13	30.51	0.73	931	69.2
GCGS-TMDG s-Si MOSFET	3.65	31	65.2	54.95	0.69	947	160
GCDMDG MOSFET [42]	5.2	3.0	26	4.12	–	790	135
GCGS DG MOSFET [52]	2.9	–	23	3.67	0.65	680	–
High-k DG MOSFET [87]	3.35	3.3	26.5	14.12	–	–	132

Fig. 4-48 depicts the effect of fixed charge density with damaged length at SiO_2/s-Si interface on GTFP of the GCGS-TMDG s-Si MOSFET. The GTFP of GCGS-TMDG s-Si MOSFET increases/decreases by increasing the negative/positive fixed charge density with damaged length at SiO_2/s-Si interface in the above threshold voltage region, and vice-versa in sub-threshold region. However, when $N_f > -2 \times 10^{12}$, GTFP of GCGS-TMDG s-Si MOSFET decreases owing to the DIBL effect. Hence, it is observed from Fig. 4-48 that the Analog/RF parameters of the proposed GCGS-TMDG s-Si MOSFET vary according to fixed charge density at SiO_2/s-Si interface with damaged length.

The analog/radio frequency performance evaluation of the proposed GCGS-TMDG s-Si MOSFET is compared with the previous works in the literature, as illustrated in Table 4-3. It is noticed from the Table 4-3 that proposed GCGS-TMDG s-Si MOSFET (m= 0.2 and t_{ox2}= 1 nm) has higher values of TGF, early voltage, intrinsic gain, f_t, and GTFP when compared to GCGS-DG s-Si MOSFET (m= 0.2 and t_{ox2}= 1 nm), Nano-scale GCDMDG device having channel length 15 nm [42], GCGS DG device [52], and high-k oxide material DG MOSFET having channel length 20 nm [87]. Therefore, the proposed GCGS-DMDG s-Si MOSFET has better analog/RF figure of merit is attained by using the TMG with gate stack structure and graded channel engineering.

4.4 Summary and Conclusions

The analog/RF performance analysis of proposed GC-DMDG and GCGS-TMDG s-Si MOSFETs with interface charges has been evaluated using the TCAD simulator. From the result analysis, it has been concluded that the proposed GC-DMDG s-Si MOSFET has better analog/RF performance over GC-DG s-Si MOSFET in the strong inversion region. Moreover, the analog/RF performance of DG s-Si MOSFET is improved by using the DMG structure with the GC engineering technique. Improvements in TFP and GTFP of the proposed s-Si MOSFET have been observed by increasing the values of m, positive N_f, t_{ox}, and t_{s-Si} in the subthreshold region, and vice-versa in the strong inversion region.

Furthermore, the analog/RF figure of merit of DG s-Si MOSFET is enhanced by employing the high-k dielectric materials in GS, TMG structure, and GC engineering techniques. A rigorous analysis has been done to explore the various analog/RF figures of merit by varying different device parameters of proposed GCGS-TMDG s-Si MOSFETs. Moreover, the peak values of TFP, GFP, and GTFP of proposed s-Si MOSFET have been obtained at a V_{gs}, which is greater than the threshold voltage. Therefore, the proposed s-Si MOSFET has better analog/RF performance above the moderate inversion region. Also, the proposed GCGS-TMDG s-Si MOSFET has enhanced analog/RF performance when compared to GCGS-DG s-Si MOSFET in the above threshold region. The further part of this contribution, i.e., the variability analysis of GC-DMDG s-Si MOSFET with interface charges and CMOS inverter's performance will be presented in the next chapter.

Chapter 5

Variability analysis of GC-DMDG s-Si MOSFET with interface charges and CMOS inverter performance

5.1 Introduction

The simulation and modeling of subthreshold characteristics of symmetrical GC-DMDG s-Si MOSFET with fixed charges, the analog/RF performance of GC-DMDG and GCGS-TMDG s-Si MOSFET with fixed charges have been presented in Chapters 3 and 4, respectively. The variability analysis of GC-DMDG s-Si MOSFET with fixed charges has not been presented so far in the literature. In this present chapter, an attempt is made to analyze the variability of GC-DMDG s-Si MOSFET with fixed charges. By employing GC with gate engineering structure, reduced variability performance of DG s-Si MOSFET is achieved. Moreover, the performance evaluation of CMOS inverter using proposed GC-DMDG s-Si MOSFET is demonstrated.

This work illustrates the analysis of the effects of fluctuations in doping (RDF), oxide thickness (OTF), contact resistance (CRF), and line edge roughness (LER) on the performance of GCDM-DG s-Si device with fixed charges. The electrical characteristics of the device strongly depend on doping profiles and the physical dimensions, so the responsiveness of the device to the deviations of RDF and LER becomes more. Thus, we need to calculate the standard deviations of the threshold voltage and ON current of the device due to the perturbations

of RDF, LER, OTF, and CRF. Also, the variations in the characteristics of the MOSFET can be reduced by carefully choosing the device's dimensions. Besides, the proposed GCDM-DG s-Si p-MOSFET has less deviations when compared to proposed GCDM-DG s-Si n-MOSFET.

The variability analysis of the proposed device is simulated with the help of the statistical impedance field method (sIFM) approach available in Sentaurus device. The sIFM uses Green's function-based approach to create a huge number of randomized fluctuations of the parameters that are under investigation and evaluates the changes in the device performance in linear response. In statistical IFM method, the random device fluctuations are treated small perturbations of the reference device. The implementation of different variability sources in TCAD simulations is discussed in detail as given below.

a) Contact resistance fluctuations: The contact resistance variability is assessed at post processing by defining the parameter of standard deviation of the contact resistance.

b) Random dopant fluctuations (RDF): For RDF analysis, following Poisson distribution in the sIFM method, the dopants are considered independent and randomly distributed. The random variation parameter for RDFs in the physics section is doping, and RDFs are separated into contributions from the donor and acceptor species using the type keyword.

c) Oxide thickness fluctuations (OTF): The random variation parameter for gate oxide roughness in the physics section is geometric. Correlation function determines the way in which spatial correlations are modeled and is considered as grain in this case. Moreover, the amplitude of the roughness is chosen 10% of the oxide thickness approximately.

d) Line edge roughness (LER): The effects of LER can be considered in two ways. In the first way, the fluctuations due to changes in the gate length are accounted as geometric is used as a random variation parameter. In the second way, the changes in the doping profile are accounted as doping variation is used as a random variation parameter. To study the LER along the channel length direction, the amplitude of the gate edge shift is set to 1 nm and the parameter Îż determines the correlation length, which is set to 1 Âţm. Moreover, the spatial variations are considered uniformly. To find out the LER, variations of dielectric constant and space charge are considered in the Poisson equation and band energy profile variation is considered in the continuity equations.

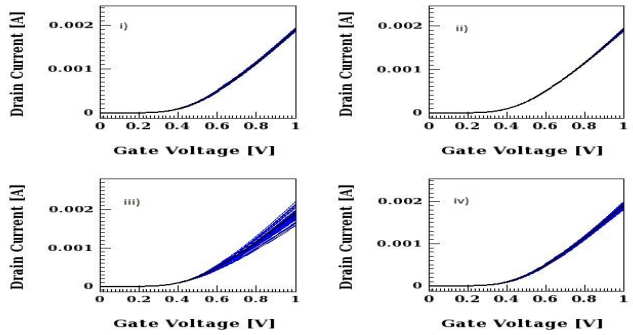

Figure 5.1: Variation of transfer characteristics of GCDM-DG s-Si n-MOSFET with L= 20 nm due to i) RDF, ii) OTF, iii) CRF, iv) LER.

5.2 Variability analysis of GC-DMDG s-Si MOSFET with interface charges

The variability analysis of the proposed GCDM-DG s-Si device with fixed charges is simulated with the help of the statistical impedance field method (sIFM) in Sentaurus TCAD [69]. The sIFM creates a huge number of randomized fluctuations of the parameters that are under investigation (dopant concentrations) and evaluates the changes in the device's performance in linear response.

5.2.1 Result analysis

This section illustrates the variability analysis of the GCDM-DG s-Si MOSFET with fixed charges. The effects of RDF, OTF, CRF, and LER are considered individually to perform variability analysis of the proposed device, and each case is simulated with an ensemble size of 150. Fig. 5-1 depicts the effects of RDF, OTF, CRF, and LER on the transfer characteristics of GCDM-DG s-Si n-MOSFET at L= 20 nm, t_{ox}= 1 nm, and m= 0.2. It is evident from Fig. 5-1 that the CRF has more effect on ON current and LER has moderate effect on threshold voltage of the device when compared to other fluctuations, as listed in Table 5-1. Moreover, the standard deviation of V_{th} (σV_{th}) of the proposed device is estimated for different values of V_{th} and extracted from the transfer characteristics at a V_{ds} of 0.05 V. Therefore, standard deviations of I_{ON} (σI_{ON}) and σV_{th} are calculated with respect to reference transfer characteristic curve (V_{th}= 0.327 V and I_{ON}= 7.3×10^{-4}), as seen in Table 5-1.

The effects of RDF, OTF, CRF, and LER on the transfer characteristics of GCDM-DG s-Si n-MOSFET at L= 40 nm, t_{ox}= 1 nm, and m= 0.2 are shown in Fig. 5-2. It is noticed from Fig.

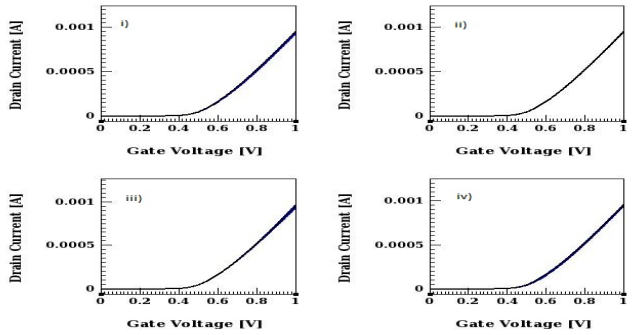

Figure 5.2: Variation of transfer characteristics of GCDM-DG s-Si n-MOSFET with L= 40 nm due to i) RDF, ii) OTF, iii) CRF, iv) LER.

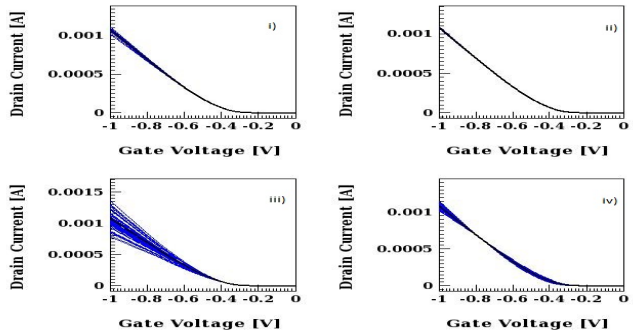

Figure 5.3: Variation of transfer characteristics of GCDM-DG s-Si p-MOSFET with L= 20 nm due to i) RDF, ii) OTF, iii) CRF, iv) LER.

5-1 and Fig. 5-2 that the effect of variations are less at a channel length of 40 nm as compared to a channel length of 20 nm due to reduced SCEs. However, CRF has considerable effect on I_{ON} of the device than other process variations, as listed in Table 5-1. Moreover, in this case, σI_{ON} and σV_{th} are calculated with respect to reference transfer characteristic curve (V_{th}= 0.399 V and I_{ON}= 4.21×10^{-4}), as illustrated in Table 5-1.

Fig. 5-3 depicts the effects of RDF, OTF, CRF, and LER on the transfer characteristics of GCDM-DG s-Si p-MOSFET at L= 20 nm, t_{ox}= 1 nm, and m= 0.2. It is evident from Fig. 5-3 that the CRF has more effect on I_{ON} and LER has moderate effect on threshold voltage of the device as compared to the other fluctuations, as listed in Table 5-2. Moreover, σI_{ON} and σV_{th} are calculated with respect to reference transfer characteristic curve (V_{th}= -0.415 V and I_{ON}= 3.19×10^{-4}), as demonstrated in Table 5-2. It is observed from Table 5-1 and Table 5-2 that the effects of RDF, OTF, CRF, and LER on the transfer characteristics of the proposed p-MOSFET are less than the proposed n-MOSFET because of the higher threshold voltage of proposed p-MOSFET.

The effects of RDF, OTF, CRF, and LER on the transfer characteristics of GCDM-DG s-Si p-MOSFET at L= 40 nm, t_{ox}= 1 nm, and m= 0.2 are shown in Fig. 5-4. It is observed from Fig.

Table 5.1: Variability analysis of proposed GCDM-DG s-Si n-MOSFET with V_{ds}= 0.05 V

	RDF		OTF		CRF		LER	
	σV_{th}, mV	σI_{ON}, A	σV_{th}, mV	σI_{ON}, A	σV_{th}, mV	σI_{ON}, A	σV_{th}, mV	σI_{ON}, A
L= 20 nm	2.5	1.82×10^{-5}	1.0	1.24×10^{-6}	0.5	4.66×10^{-3}	8.6	2.77×10^{-5}
L= 40 nm	1.1	6.35×10^{-6}	0.2	6.82×10^{-7}	0.1	1.47×10^{-3}	5.3	1.25×10^{-5}
m= 0.3	2.8	1.55×10^{-5}	1.0	1.1×10^{-6}	0.5	1.62×10^{-3}	8.7	4.5×10^{-5}
t_{ox}= 2 nm	2.8	9.75×10^{-6}	0.8	1.25×10^{-6}	0.9	2.93×10^{-3}	9.4	2.46×10^{-5}
N_f= 4×10^{-12}	2.4	1.74×10^{-5}	7.8	5.78×10^{-6}	0.6	4.6×10^{-3}	243.7	1.17×10^{-4}
N_f= -4×10^{-12}	1.6	1.26×10^{-5}	16.2	1.34×10^{-5}	0.9	2.71×10^{-3}	463.5	5.02×10^{-4}

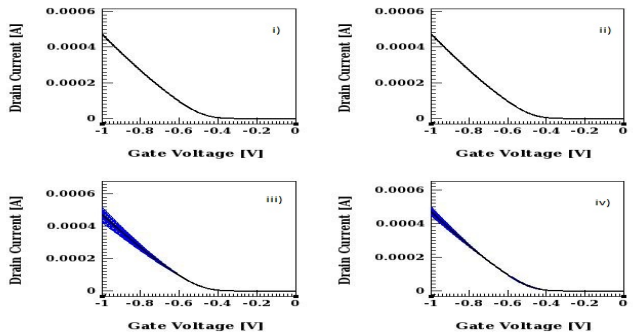

Figure 5.4: Variation of transfer characteristics of GCDM-DG s-Si p-MOSFET with L= 40 nm due to i) RDF, ii) OTF, iii) CRF, iv) LER.

5-3 and Fig. 5-4 that the effect of variations are less for channel length L= 40 nm as compared to L= 20 nm due to reduced SCEs. However, CRF has some effect on I_{ON} of the proposed device when compared to the other variations, as listed in Table 5-2. Moreover, in this case, σI_{ON} and σV_{th} are calculated with respect to reference transfer characteristic curve (V_{th}= -0.461 V and I_{ON}= 1.41×10^{-4}), as shown in Table 5-2.

The effects of RDF, OTF, CRF, and LER on the transfer characteristics of GCDM-DG s-Si n-MOSFET at L= 20 nm, t_{ox}= 1 nm, and m= 0.3 are illustrated in Fig. 5-5. It is evident from Fig. 5-5 that as strain increases in silicon channel, the impact of RDF, OTF, CRF, and LER on the transfer characteristics slightly decreases due to decrease in threshold voltage of proposed n-MOSFET. Moreover, σI_{ON} and σV_{th} are calculated with respect to reference transfer characteristic curve (V_{th}= 0.263 V and I_{ON}= 4.12×10^{-4}), as illustrated in Table 5-1.

Fig. 5-6 illustrates the effects of RDF, OTF, CRF, and LER on the transfer characteristics of GCDM-DG s-Si p-MOSFET at L= 20 nm, t_{ox}= 1 nm, and m= 0.3. The variations of RDF, OTF, CRF, and LER on the transfer characteristics slightly decreases due to the increase in the threshold voltage of the proposed MOSFET as strain increases in silicon channel. Moreover,

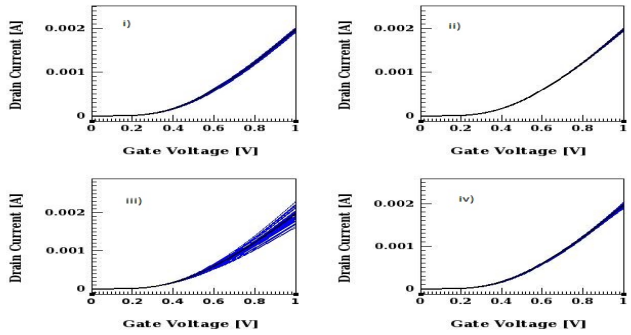

Figure 5.5: Variation of transfer characteristics of GCDM-DG s-Si n-MOSFET with m= 0.3 due to i) RDF, ii) OTF, iii) CRF, iv) LER.

Table 5.2: Variability analysis of proposed GCDM-DG s-Si p-MOSFET with V_{ds}= 0.05 V

	RDF		OTF		CRF		LER	
	σV_{th}, mV	σI_{ON}, A	σV_{th}, mV	σI_{ON}, A	σV_{th}, mV	σI_{ON}, A	σV_{th}, mV	σI_{ON}, A
L= 20 nm	1.2	5.48×10^{-6}	0.3	9.86×10^{-7}	1.1	7.52×10^{-4}	8.1	1.62×10^{-5}
L= 40 nm	0.9	1.13×10^{-6}	0.1	2.2×10^{-7}	0.3	1.53×10^{-4}	1.6	4.06×10^{-6}
m= 0.3	1.2	5.11×10^{-6}	0.3	8.84×10^{-7}	1.1	5.25×10^{-4}	7.6	1.59×10^{-5}
t_{ox}= 2 nm	1.1	1.7×10^{-6}	0.2	4.9×10^{-7}	1.5	3.9×10^{-4}	3.8	6.77×10^{-6}
N_f= 4×10^{-12}	1.2	5.41×10^{-6}	17.4	5.11×10^{-6}	1.0	7.78×10^{-4}	519.6	2.03×10^{-4}
N_f= -4×10^{-12}	1.4	7.04×10^{-6}	6.4	3.58×10^{-6}	0.5	1.2×10^{-3}	198.8	8.53×10^{-5}

σI_{ON} and σV_{th} are calculated with respect to reference transfer characteristic curve (V_{th}= -0.449 V and I_{ON}= 2.72×10^{-4}), as listed in Table 5-2.

The effects of RDF, OTF, CRF, and LER on the transfer characteristics of GCDM-DG s-Si n-MOSFET at L= 20 nm, t_{ox}= 2 nm, and m= 0.2 are depicted in Fig. 5-7. As t_{ox} increases in the GCDM-DG s-Si n-MOSFET, variations of ON current decrease due to less gate control over the channel than drain and variations of threshold voltage increase because of decrease in threshold voltage of proposed n-MOSFET. Besides, σI_{ON} and σV_{th} are calculated with respect

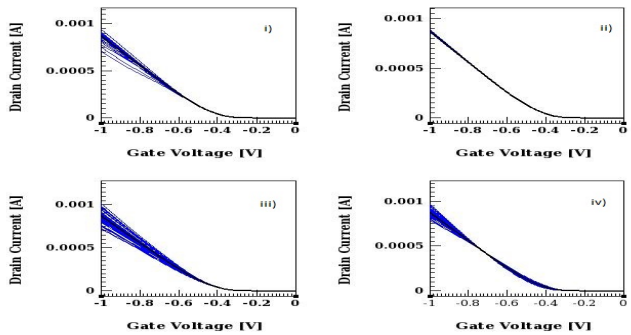

Figure 5.6: Variation of transfer characteristics of GCDM-DG s-Si p-MOSFET with m= 0.3 due to i) RDF, ii) OTF, iii) CRF, iv) LER.

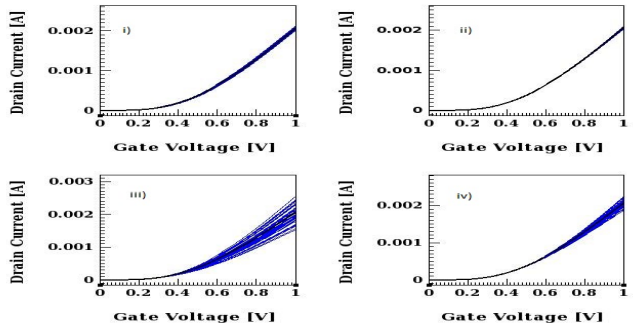

Figure 5.7: Variation of transfer characteristics of GCDM-DG s-Si n-MOSFET with t_{ox}= 2 nm due to i) RDF, ii) OTF, iii) CRF, iv) LER.

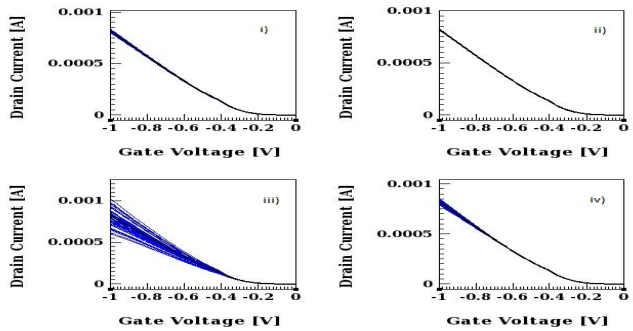

Figure 5.8: Variation of transfer characteristics of GCDM-DG s-Si p-MOSFET with t_{ox}= 2 nm due to i) RDF, ii) OTF, iii) CRF, iv) LER.

to reference transfer characteristic curve (V_{th}= 0.253 V and I_{ON}= 5.96×10^{-4}), as shown in Table 5-1.

Fig. 5-8 plots the effects of RDF, OTF, CRF, and LER on the transfer characteristics of GCDM-DG s-Si p-MOSFET at L= 20 nm, t_{ox}= 2 nm, and m= 0.2. As t_{ox} increases in the GCDM-DG s-Si p-MOSFET, variations of both ON current and threshold voltage decrease due to the less gate control over channel than drain. Besides, σI_{ON} and σV_{th} are calculated with respect to reference transfer characteristic curve (V_{th}= -0.372 V and I_{ON}= 2.354×10^{-4}), as illustrated in Table 5-2.

The effects of RDF, OTF, CRF, and LER on the transfer characteristics of GCDM-DG s-Si n-MOSFET along with negative fixed charge density (N_f) at L= 20 nm, t_{ox}= 1 nm, and m= 0.2 are shown in Fig. 5-9. As negative N_f is considered at oxide/channel interface, the effects of OTF and LER on both I_{ON} and V_{th} are more severe compared to the other effects. Due to the fixed charges at oxide/channel interface, the minimum channel potential and its position of the device are varied according to the polarity and magnitude of the fixed charges and length of damaged region. As negative N_f increases, threshold voltage of the device increases because of the decrement of minimum channel potential, and vice-versa for positive N_f. Besides, σI_{ON}

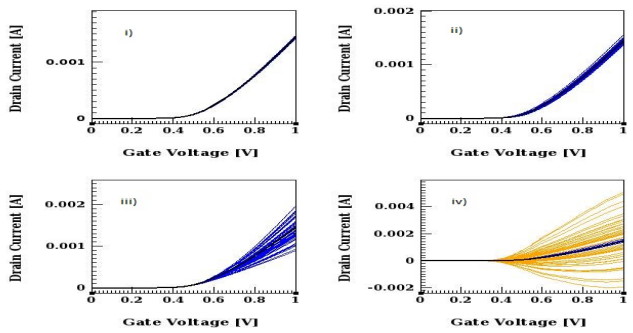

Figure 5.9: Variation of transfer characteristics of GCDM-DG s-Si n-MOSFET with N_f= -4×10^{12} due to i) RDF, ii) OTF, iii) CRF, iv) LER.

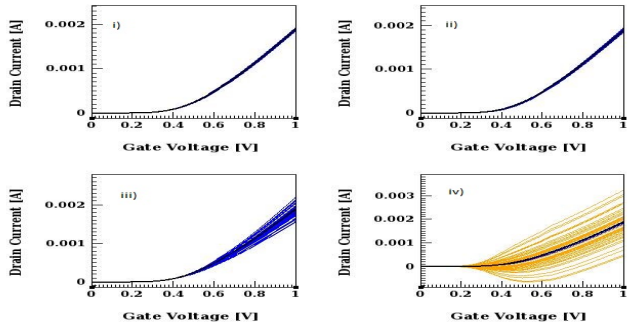

Figure 5.10: Variation of transfer characteristics of GCDM-DG s-Si n-MOSFET with N_f= 4×10^{12} due to i) RDF, ii) OTF, iii) CRF, iv) LER.

and σV_{th} are calculated with respect to reference transfer characteristic curve (V_{th}= 0.514 V and I_{ON}= 5.86×10^{-4}), as listed in Table 5-1.

Fig. 5-10 shows the effects of RDF, OTF, CRF, and LER on the transfer characteristics of GCDM-DG s-Si n-MOSFET along with positive N_f at L= 20 nm, t_{ox}= 1 nm, and m= 0.2 are shown in Fig. 5-10. As positive N_f is considered at oxide/channel interface, the effects of OTF and LER on both I_{ON} and V_{th} are more severe compared to the other effects. However, in case of the proposed device with positive N_f, the impacts of OTF and LER are less on both I_{ON} and V_{th} compared to the device that has negative N_f at oxide/channel interface. Moreover, σI_{ON} and σV_{th} are calculated with respect to reference transfer characteristic curve (V_{th}= 0.347 V and I_{ON}= 7.26×10^{-4}), as listed in Table 5-1.

Fig. 5-11 demonstrates the effects of RDF, OTF, CRF, and LER on the transfer characteristics of GCDM-DG s-Si p-MOSFET along with negative N_f at L= 20 nm, t_{ox}= 1 nm, and m= 0.2. As negative N_f is considered at oxide/channel interface, the effects of OTF and LER on both I_{ON} and V_{th} are more severe compared to the other effects. As positive N_f increases, threshold voltage of the device increases because of the decrement of minimum channel potential, and vice-versa for negative N_f. However, the impacts of OTF and LER on transfer characteristics

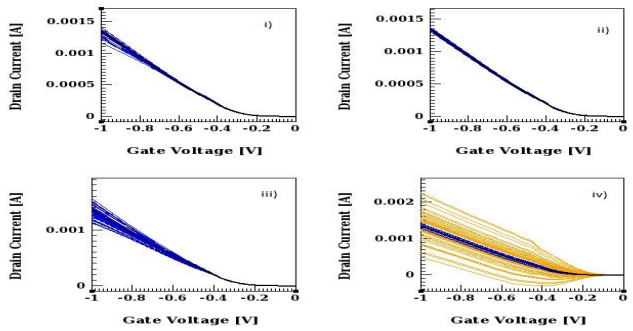

Figure 5.11: Variation of transfer characteristics of GCDM-DG s-Si p-MOSFET with N_f= -4×10^{12} due to i) RDF, ii) OTF, iii) CRF, iv) LER.

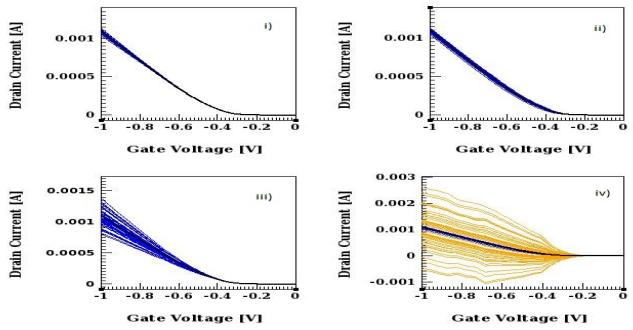

Figure 5.12: Variation of transfer characteristics of GCDM-DG s-Si p-MOSFET with N_f= 4×10^{12} due to i) RDF, ii) OTF, iii) CRF, iv) LER.

of the proposed p-MOSFET with negative N_f is less compared to the proposed n-MOSFET that has negative N_f. Besides, σI_{ON} and σV_{th} are calculated with respect to reference transfer characteristic curve (V_{th}= -0.225 V and I_{ON}= 3.92×10^{-4}), as shown in Table 5-2.

Fig. 5-12 illustrates the effects of RDF, OTF, CRF, and LER on the transfer characteristics of GCDM-DG s-Si p-MOSFET along with positive N_f at L= 20 nm, t_{ox}= 1 nm, and m= 0.2. As positive N_f is considered at oxide/channel interface, the effects of OTF and LER on both I_{ON} and V_{th} are more severe compared to other effects. However, in case of the proposed device

Table 5.3: Variability analysis of proposed GCDM-DG s-Si n-MOSFET with V$_{ds}$= 0.9 V

	RDF		OTF		CRF		LER	
	σV_{th}, mV	σI_{ON}, A	σV_{th}, mV	σI_{ON}, A	σV_{th}, mV	σI_{ON}, A	σV_{th}, mV	σI_{ON}, A
L= 20 nm	3.5	2.0×10^{-5}	1.5	1.31×10^{-5}	0.2	1.71×10^{-4}	5.7	4.09×10^{-5}
L= 40 nm	1.2	5.6×10^{-6}	0.3	3.4×10^{-6}	0.0	1.28×10^{-5}	5.2	6.6×10^{-6}
m= 0.3	4.0	2.29×10^{-5}	1.6	1.32×10^{-5}	0.2	1.81×10^{-4}	5.6	3.12×10^{-5}
t_{ox}= 2 nm	4.5	1.66×10^{-5}	1.6	4.98×10^{-6}	0.5	2.04×10^{-4}	11.0	2.6×10^{-5}
N$_f$= 4×10^{-12}	3.0	1.94×10^{-5}	6.5	2.53×10^{-5}	0.2	1.72×10^{-4}	236.0	5.93×10^{-4}
N$_f$= -4×10^{-12}	2.2	1.16×10^{-5}	10.7	4.53×10^{-5}	0.3	2.85×10^{-4}	281.1	1.48×10^{-3}

Table 5.4: Variability analysis of proposed GCDM-DG s-Si p-MOSFET with V_{ds}= 0.9 V

	RDF		OTF		CRF		LER	
	σV_{th}, mV	σI_{ON}, A	σV_{th}, mV	σI_{ON}, A	σV_{th}, mV	σI_{ON}, A	σV_{th}, mV	σI_{ON}, A
L= 20 nm	1.2	1.67×10^{-5}	0.5	5.75×10^{-6}	0.3	1.55×10^{-4}	10.4	2.81×10^{-5}
L= 40 nm	0.9	1.76×10^{-6}	0.2	1.0×10^{-6}	0.1	2.6×10^{-5}	4.9	1.15×10^{-5}
m= 0.3	1.2	5.07×10^{-5}	0.5	7.06×10^{-6}	0.3	7.97×10^{-5}	9.9	3.89×10^{-5}
t_{ox}= 2 nm	1.6	8.01×10^{-6}	0.7	2.89×10^{-6}	0.5	1.13×10^{-4}	1.4	1.43×10^{-5}
N_f= 4×10^{-12}	1.3	1.73×10^{-5}	9.3	2.07×10^{-5}	0.2	1.56×10^{-4}	250.0	6.67×10^{-4}
N_f= -4×10^{-12}	2.2	4.21×10^{-5}	5.5	1.56×10^{-5}	0.2	1.18×10^{-4}	192.9	3.76×10^{-4}

with negative N_f, the impacts of OTF and LER are less on both I_{ON} and V_{th} compared to the device that has positive N_f at oxide/channel interface. Also, the impacts of OTF and LER on transfer characteristics of the proposed n-MOSFET with positive N_f is less compared to the proposed p-MOSFET that has positive N_f. Moreover, σI_{ON} and σV_{th} are calculated with respect to reference transfer characteristic curve (V_{th}= -0.402 V and I_{ON}= 3.24×10^{-4}), as listed in Table 5-2.

The effects of RDF, OTF, CRF, and LER on the transfer characteristics of the GCDM-DG s-Si MOSFET at V_{ds}= 0.9 V are given in Table 5-3 and Table 5-4. As shown in Table 5-3 and Table 5-4, there is a slight increase in σI_{ON} and slight decrease in σV_{th} when V_{ds} changes from 0.05 V to 0.9V.

5.3 Performance evaluation of CMOS inverter using GC-DMDG s-Si MOSFET with interface charges

5.3.1 Proposed CMOS Inverter diagram

The circuit diagram of CMOS inverter using GC-DMDG s-Si MOSFET with interface charges is shown in Fig. 5-13. In the CMOS inverter, p-type and n-type GC-DMDG s-Si MOSFET have same dimensions except for the width of channel of p-type GC-DMDG s-Si MOSFET is twice the width of the channel of n-type GC-DMDG s-Si MOSFET and also the work function of control gate is considered to be less than the work function of screening gate in p-type GC-DMDG s-Si MOSFET. In CMOS inverter, V_{dd} is chosen as 1 V and external load capacitance (C_L) is taken as 3×10^{-14}F. For the transient response of CMOS inverter, the delay

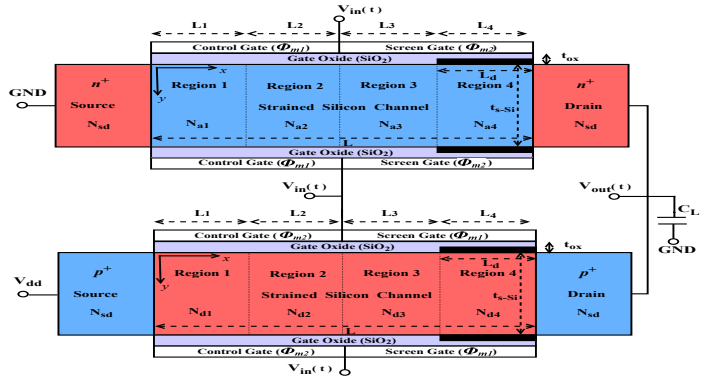

Figure 5.13: Circuit diagram of CMOS inverter using GC-DMDG s-Si MOSFET with interface charges.

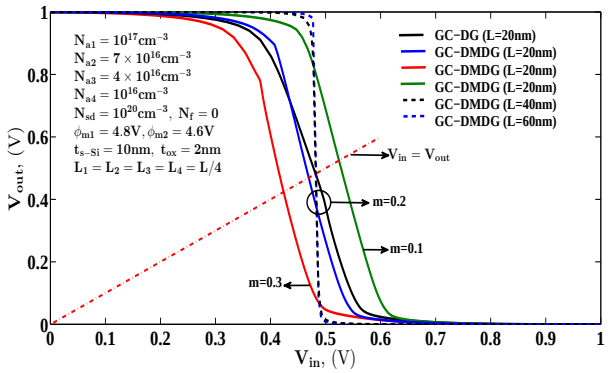

Figure 5.14: VTC of CMOS inverter using GC-DMDG s-Si MOSFET for different values of m and L

time (t_d), rise time (t_r) and fall time (t_f) are considered to be 10 pS. Pulse period and ON period (t_{on}) of input signal ($V_{in}(t)$) are chosen as 140 pS and 60 pS, respectively.

5.3.2 Result analysis

Fig. 5-14 depicts the voltage transfer characteristics (VTC) of CMOS inverter for different channel lengths and m values of GC-DMDG s-Si MOSFET. As shown in Table 5-5, due to an increase in threshold voltage of GC-DMDG s-Si MOSFET, noise margin low (NM_L) and noise margin high (NM_H) of inverter increase as channel length of proposed device increases. It is observed that the NM_L (NM_H) of CMOS inverter decreases (increases) by increasing m value due to decrease (increase) in the threshold voltage of n-type (p-type) GC-DMDG s-Si MOSFET. Moreover, VTC of CMOS inverter shift towards left (right) side by increasing (decreasing) m value due to the increment in driving capability of pull-down (pull-up) transistor of CMOS inverter. From Fig. 5-14, it is evident that the GC-DMDG s-Si MOSFET has better noise

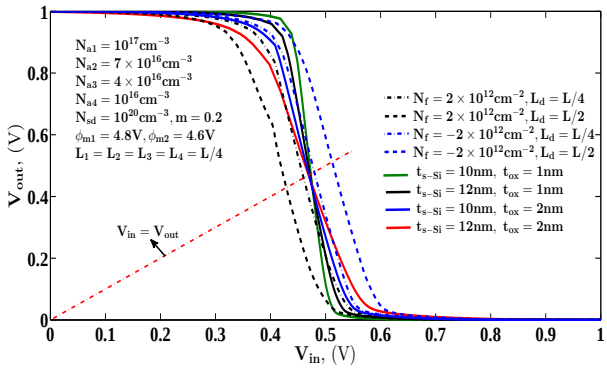

Figure 5.15: VTC of CMOS inverter using GC-DMDG s-Si MOSFET for different values of N_f, t_{ox} and t_{s-Si}

Table 5.5: Noise margin of CMOS inverter using GC-DMDG s-Si MOSFET

S.No.	**Parameters**	V_{IL} **(V)**	V_{IH} **(V)**	V_{OL} **(V)**	V_{OH} **(V)**	NM_L **(V)**	NM_H **(V)**
1	GC-DG s-Si (m= 0.2)	0.355	0.573	0.039	0.946	0.316	0.373
2	m= 0.1	0.439	0.621	0.027	0.953	0.412	0.332
3	m= 0.2	0.371	0.557	0.031	0.946	0.340	0.389
4	m= 0.3	0.312	0.500	0.047	0.945	0.265	0.445
5	t_{ox}= 1 nm, t_{s-Si}= 10 nm	0.410	0.521	0.021	0.979	0.389	0.458
6	t_{ox}= 1 nm, t_{s-Si}= 12 nm	0.393	0.539	0.025	0.965	0.368	0.426
7	t_{ox}= 2 nm, t_{s-Si}= 12 nm	0.339	0.582	0.039	0.932	0.300	0.350
8	N_d= 2×10^{12}, L_d= L/2	0.303	0.520	0.029	0.951	0.274	0.431
9	N_d= 2×10^{12}, L_d= L/4	0.358	0.550	0.030	0.944	0.328	0.394
10	N_d= −2×10^{12}, L_d= L/4	0.383	0.565	0.033	0.948	0.350	0.383
11	N_d= −2×10^{12}, L_d= L/2	0.411	0.609	0.032	0.961	0.379	0.352
12	L= 40 nm	0.451	0.501	0.014	0.987	0.437	0.486
13	L= 60 nm	0.467	0.498	0.011	0.991	0.456	0.493

margin than GC-DG s-Si MOSFET owing to higher threshold voltage and better SCEs of GC-DMDG s-Si MOSFET.

Fig. 5-15 shows the VTC of CMOS inverter for different N_f, t_{ox} and t_{s-Si} values of GC-DMDG s-Si MOSFET. Noise margin of CMOS inverter is improved by decreasing the t_{ox} and t_{s-Si} values of proposed device owing to increase in threshold voltage of GC-DMDG s-Si MOSFET, as shown in Table 5-5. Moreover, NM_L (NM_H) decreases (increases) by increasing the positive interface charge density with damaged length at s-Si/SiO_2 interface of GC-DMDG s-Si MOSFET due to the reduction (enhancement) in threshold voltage of n-type (p-type) GC-DMDG s-Si MOSFET, and vice-versa in the case of negative interface charge density at s-Si/SiO_2 interface. Moreover, VTC of CMOS inverter shift towards left (right) side by increasing positive (negative) interface charge density with damaged length due to the increment in the driving capability of pull-down (pull-up) transistor of CMOS inverter.

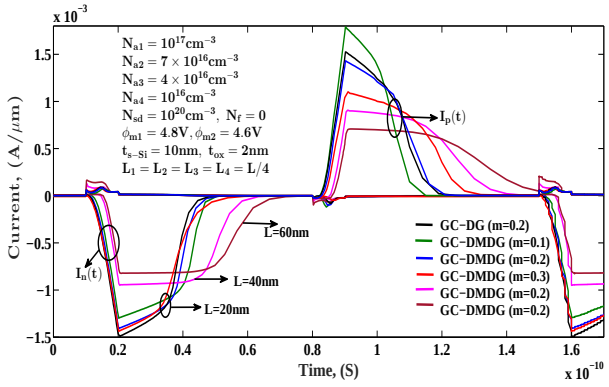

Figure 5.16: Transient response of currents ($I_n(t)$ and $I_p(t)$) in CMOS inverter for various values of m and L

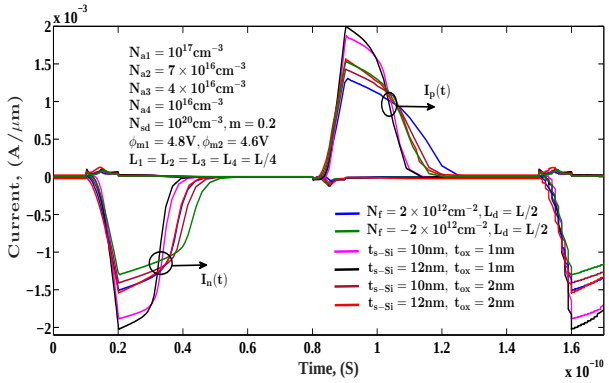

Figure 5.17: Transient response of currents ($I_n(t)$ and $I_p(t)$) in CMOS inverter for various values of N_f, t_{ox} and t_{s-Si}

Fig. 5-16 plots the transient response of currents ($I_n(t)$ and $I_p(t)$) in the CMOS inverter for different L and m values of GC-DMDG s-Si MOSFET. $I_n(t)$ and $I_p(t)$ are the currents flowing through the n-type and p-type GC-DMDG s-Si MOSFET of CMOS inverter, respectively. $I_n(t)$ and $I_p(t)$ of CMOS inverter decrease as channel length of proposed device increases because of the increasing threshold voltages of p-type and n-type GC-DMDG s-Si MOSFET. Besides, $I_n(t)$ ($I_p(t)$) increases (decreases) as m increases due to the reduction (enhancement) in threshold voltage of n-type (p-type) GC-DMDG s-Si MOSFET. From Fig. 5-16, higher $I_n(t)$ and $I_p(t)$ are observed in GC-DG s-Si MOSFET compared to GC-DMDG s-Si MOSFET due to the lower threshold voltage of GC-DG s-Si MOSFET.

Fig. 5-17 demonstrates the $I_n(t)$ and $I_p(t)$ of the CMOS inverter for various t_{ox} and t_{s-Si} values of s-Si GC-DMDG MOSFET. It is noticed that the $I_n(t)$ and $I_p(t)$ of CMOS inverter increase as t_{s-Si} (t_{ox}) of proposed device increases (decreases) because of the better gate control of the channel than drain. Moreover, $I_n(t)$ of CMOS inverter is increased (decreased) by positive (negative) interface charge density at s-Si/SiO_2 interface of proposed device and reverse trend is observed in $I_p(t)$ of CMOS inverter.

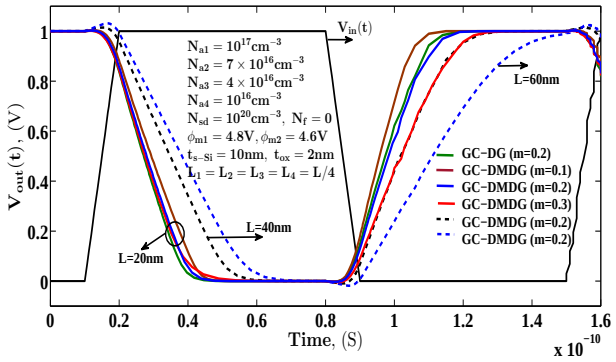

Figure 5.18: Transient response ($V_{out}(t)$) of CMOS inverter for various values of m and L

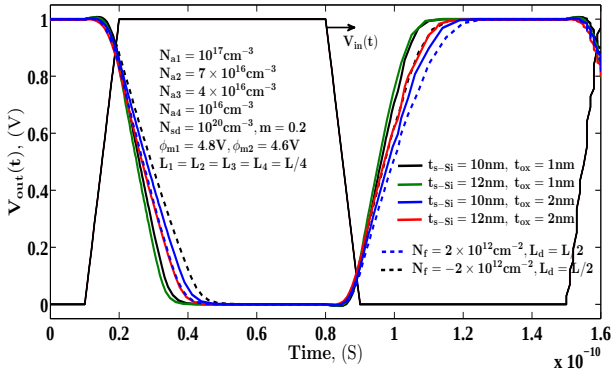

Figure 5.19: Transient response ($V_{out}(t)$) of CMOS inverter for various values of N_f, t_{ox} and t_{s-Si}

Fig. 5-18 shows the transient response of output voltage ($V_{out}(t)$) in the CMOS inverter for different L and m values of GC-DMDG s-Si MOSFET. It is observed that the rise time (t_r) and fall time (t_f) of $V_{out}(t)$ in CMOS inverter increase as the channel length of proposed device increases due to reduction of $I_n(t)$ and $I_p(t)$, as shown in Fig. 5-16. As m increases, t_r (t_f) of $V_{out}(t)$ is degraded (improved) due to lower (higher) $I_p(t)$ ($I_n(t)$) of CMOS inverter, as shown in Fig. 5-16. Moreover, minimum t_r and t_f of $V_{out}(t)$ are observed in CMOS inverter using GC-DG s-Si MOSFET than GC-DMDG s-Si MOSFET due to higher $I_n(t)$ and $I_p(t)$ of GC-DG s-Si MOSFET, as shown in Fig. 5-16.

Fig. 5-19 shows the $V_{out}(t)$ of CMOS inverter for different t_{ox} and t_{s-Si} values of GC-DMDG s-Si MOSFET. The t_r and t_f of $V_{out}(t)$ in CMOS inverter increase as t_{ox} (t_{s-Si}) of proposed device increases (decreases) owing to higher $I_n(t)$ and $I_p(t)$ of CMOS inverter, as shown in Fig. 5-17. Moreover, t_r of CMOS inverter is increased (decreased) by positive (negative) interface charge density at s-Si/SiO_2 interface of proposed device due to decrement (increment) of $I_p(t)$ in CMOS inverter and reverse trend is observed in t_f of CMOS inverter.

5.4 Summary and Conclusions

The variability analysis of proposed GCDM-DG s-Si MOSFET with fixed charge density has been evaluated using the TCAD tool. The variability of GCDM-DG s-Si MOSFET is reduced by employing the DMG structure and the GC engineering. A detailed variability analysis has been done to investigate the different effects, such as RDF, OTF, CRF, and LER by varying parameters of the GCDM-DG s-Si MOSFET. Decrements of σI_{ON} and σV_{th} of proposed GCDM-DG s-Si MOSFET have been obtained by increasing the channel length. Moreover, it is concluded from the results that the effects of OTF and LER on the device characteristics are severe when device has fixed charge density at oxide/channel interface. Besides, the impact of RDF, OTF, CRF, and LER on ON current and threshold voltage of proposed GCDM-DG s-Si p-MOSFET is less compared to the proposed GCDM-DG s-Si n-MOSFET.

Furthermore, a rigorous analysis has been done on noise margin and transient response of CMOS inverter using GC-DMDG s-Si MOSFET by varying different device parameters of s-Si GC-DMDG MOSFET. Finally, it has been concluded that the GC-DMDG s-Si MOSFET based CMOS inverter has a better noise margin and degraded transient response compared to GC-DG s-Si MOSFET.

Chapter 6

Conclusions and Future Scope

6.1 Conclusions

The thesis mainly reports on the analytical modeling and simulation of subthreshold characteristics of GC-DMDG s-Si MOSFET. Initially, a center potential based threshold voltage and SC models for symmetrical GC-DMDG s-Si MOSFET with localized charges have been analytically derived. Moreover, the analytical model of subthreshold swing has been developed by using an effective conductive path parameter. In this work, the center potential based natural length for accurately estimating the SCEs. A detailed analysis has been performed on GC-DMDG s-Si MOSFET to explore the effects of various device parameters on the center potential, electric field, threshold voltage, DIBL, subthreshold current and swing. From the proposed model, the degradation of threshold voltage roll-off, subthreshold swing and DIBL is observed, due to increase in strain, decrease in channel length, and HCEs, that can be controlled by selecting optimum values of t_{ox} and t_{s-Si}, and using the DMG structure with GC engineering. It is observed that GC-DMDG MOSFET has better immunity against SCEs and HCEs than symmetrical GC-DG MOSFET. The model has been validated using TCAD and the results from the model are observed to be in good agreement with those from the simulator.

The analog/RF performance analysis of proposed GC-DMDG and GC-DG s-Si MOSFETs with interface charges has been evaluated using the TCAD simulator. From the result analysis, it has been concluded that the proposed GC-DMDG s-Si MOSFET has better analog/RF performance over GC-DG s-Si MOSFET in the strong inversion region. Moreover, the analog/RF performance of DG s-Si MOSFET is improved by using the DMG structure with the GC engi-

neering technique. Improvements in TFP and GTFP of the proposed GC-DMDG s-Si MOSFET have been observed by increasing the values of m, positive N_f, t_{ox}, and t_{s-Si} in the subthreshold region, and vice-versa in the strong inversion region.

Furthermore, the analog/RF figure of merit of DG s-Si MOSFET is enhanced by employing the high-k dielectric materials in GS, TMG structure, and GC engineering techniques. A rigorous analysis has been done to explore the various analog/RF figures of merit by varying different device parameters of proposed GCGS-TMDG s-Si MOSFETs. Moreover, the peak values of TFP, GFP, and GTFP of proposed s-Si MOSFET have been obtained at a V_{gs}, which is greater than the threshold voltage. Therefore, the proposed s-Si MOSFET has better analog/RF performance above the moderate inversion region. Also, the proposed GCGS-TMDG s-Si MOSFET has enhanced analog/RF performance when compared to GCGS-DG s-Si MOSFET in the above threshold region.

Finally, the variability analysis of proposed GCDM-DG s-Si MOSFET with fixed charge density has been evaluated using the TCAD tool. The variability of GCDM-DG s-Si MOSFET is reduced by employing the DMG structure and the GC engineering. A detailed variability analysis has been done to investigate the different effects, such as RDF, OTF, CRF, and LER by varying parameters of the GCDM-DG s-Si MOSFET. Decrements of σI_{ON} and σV_{th} of proposed GCDM-DG s-Si MOSFET have been obtained by increasing the channel length. Moreover, it is concluded from the results that the effects of OTF and LER on the device characteristics are severe when device has fixed charge density at oxide/channel interface. Besides, the impact of RDF, OTF, CRF, and LER on ON current and threshold voltage of proposed GCDM-DG s-Si p-MOSFET is less compared to the proposed GCDM-DG s-Si n-MOSFET.

Furthermore, a rigorous analysis has been done on noise margin and transient response of CMOS inverter by varying different device parameters of GC-DMDG s-Si MOSFET. Finally, it has been concluded that the GC-DMDG s-Si MOSFET based CMOS inverter has a better noise margin and degraded transient response compared to GC-DG s-Si MOSFET based CMOS inverter.

6.2 Future Scope

In this thesis, the analytical modeling and simulation of subthreshold characteristics of GC-DMDG s-Si MOSFET with interface charges has been presented. This work can be further extended to other areas as follows.

- The analytical model of ON current could be developed for all regions of the GC-DMDG s-Si MOSFET.
- The analytical models for different device capacitors could be developed for the GC-DMDG s-Si MOSFET.
- Unified 2-D models could be derived for investigating the subthreshold performance of the GC-DMDG s-Si MOSFET for different high-k dielectric materials.

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List of Publications

List of Accepted/Published Journals

1. S. Subba Rao and N. Bheema Rao, "A Center Potential based Threshold Voltage Model for Graded-Channel Dual-Material Double Gate Strained-Si MOSFET with Interface Charges", **Journal of Computational Electronics**, Vol. 18, Issue 4, pp. 1173-1181, 2019. (SCIE-Springer)

2. S. Subba Rao and N. Bheema Rao, "Analytical modeling of subthreshold current and swing of strained-Si graded channel dual material double gate MOSFET with interface charges and analysis of circuit performance", **International Journal of Numerical Modelling: Electronic Networks, Devices and Fields**, Vol. 34, Issue 1, 2021. (SCI-Wiley)

3. S. Subba Rao and N. Bheema Rao, "Analog/RF performance of strained-Si Graded Channel Dual Material Double Gate MOSFET with interface charges", **Journal of Computational Electronics**, Vol. 20, Issue 1, pp. 492-502, 2021. (SCIE-Springer)

4. S. Subba Rao and N. Bheema Rao, "Analog/RF performance of Graded Channel Gate Stack Triple Material Double Gate strained-Si MOSFET with fixed charges", **Silicon**, 2021. (Accepted) (SCIE-Springer)

List of Journals under communication

1. S. Subba Rao and N. Bheema Rao, "Variability analysis of strained-Si Graded Channel Dual Material Double Gate MOSFET with interface charges", **Journal of Computational Electronics**(Revision Submitted) (SCI-Springer)