Design and Analysis of High-Performance Multilayer Differential Inductors for RFIC and MMIC Applications

Submitted in partial fulfillment of the requirements
for the award of the degree of
DOCTOR OF PHILOSOPHY

by

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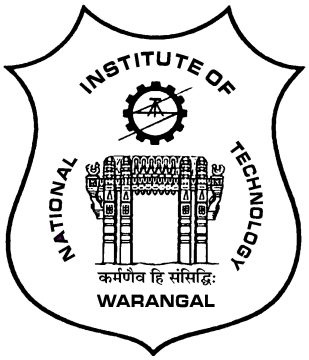

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NATIONAL INSTITUTE OF TECHNOLOGY WARANGAL
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2021

Dedicated to

My family & Teachers

Approval Sheet

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DECLARATION

This is to certify that the work presented in the thesis entitled "**Design and Analysis of High-Performance Multilayer Differential Inductors for RFIC and MMIC Applications**" is a bonafide work done by me under the supervision of **Prof. N. Bheema Rao**, Professor, Department of Electronics and Communication Engineering, National Institute of Technology Warangal, India and was not submitted elsewhere for the award of any degree.

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CERTIFICATE

This is to certify that the thesis entitled "**Design and Analysis of High-Performance Multi-layer Differential Inductors for RFIC and MMIC Applications**", which is being submitted by **Mr. Sunil Kumar Tumma (Roll No: 701622)**, in partial fulfillment for the award of the degree of Doctor of Philosophy to the Department of Electronics and Communication Engineering of National Institute of Technology Warangal, is a record of bonafide research work carried out by him under my supervision and has not been submitted elsewhere for any degree.

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ACKNOWLEDGEMENTS

Firstly, I would like to express my sincere gratitude to my supervisor Prof. N. Bheema Rao for the continuous support of my Ph.D study and related research, for his patience, motivation, and guidance. My sincere thanks to him for providing me an opportunity to join the institute as a Ph.D research scholar and giving me access to the research facilities. I find words inadequate to thank them for enabling me to complete this work in spite of all obstacles. The thesis would not have seen the light of the day without his insistent support and cooperation.

I am also grateful to Prof. L. Anjaneyulu, Head of the department, Department of Electronics and Communication Engineering, NIT Warangal for his valuable suggestions and support that he shared during my research tenure.

Besides my supervisor, I take this privilege to thank Doctoral Scrutiny Committee members, Dr. P. Sree Hari Rao, Associate professor, Department of Electronics and Communication Engineering, NIT Warangal, Dr. T.V.K. Hanumanth Rao, Associate professor, Department of Electronics and Communication Engineering, NIT Warangal, Prof. N. Vishwanathan, Department of Electrical Engineering, NIT Warangal for their continuous support, suggestions, and advices during my research period whenever required.

It is my pleasure to show my indebtedness to my co-scholars at NIT like Dr. P. Akhendra Kumar, Dr. R. Shashank, Dr. M.A. Mushahid Majid, S Subba Rao, Siva Rama Krishna, Jail Singh Bhookya, Santosh Kumar Veeramalla, Roshan Bodile, Prathap Soma, and Ravi Shankar Puppala for their help during the course of this work. I find no words inadequate to express any form of acknowledgement to my father, mother, wife, brothers for their love, support and patience for making my dream come true.

Finally, I thank God, for filling me every day with new hopes, strength, purpose and faith.

ABSTRACT

Integrated inductors are one of the most basic passive elements used in the design of Radio Frequency Integrated Circuits (RFICs) and Monolithic Microwave Integrated Circuits (MMICs) to implement the circuits like Voltage Controlled Oscillators (VCO), Low Noise Amplifiers (LNA), impedance matching networks, filters, and power amplifiers. In realization of these circuits, high performance, as well as miniaturized on-chip inductors, are desirable to increase the reliability and to reduce the fabrication cost. The spiral inductors are considered to be a good choice, however, it produces moderate-quality factor (Q). Differential excitation of the symmetric spiral inductor known as the differential inductor is used to obtain high-quality factors over a wide range of frequencies. Fractal curves are used in the realization of inductors to increases the inductance density compared to the spiral inductors for the equivalent on-chip area. The multilayer implementation of the symmetrical spiral inductor and fractal inductor with differential excitation improves the figure-of-merit such as inductance, quality factor, and self-resonance frequency (f_{SR}) over the conventional differential inductors.

Initially, in this thesis, several multilayer differential spiral inductors using variable width and multipath techniques have been proposed. Initially, the variable width series stacked differential spiral inductor has been proposed. The variable width of the metal decreases the series resistance and series stacking increases the metal trace length. Thus, it attains high Q and inductance over the conventional planar differential inductor. Furthermore, a variable multipath width multilayer differential inductor has been proposed. The variation in multipath width reduces the skin and proximity effects and up-down series stacking reduces the parasitic capacitance. Therefore, it attains high Q and self-resonance frequency over conventional planar differential inductor and planar multipath differential inductor. Later, series stacked non-parallel multipath differential inductor has been proposed that reduces the parasitic capacitance among the adjoining metal layers and also reduces the conductor's current crowding effects at high frequencies, leading to higher quality factor and self-resonance frequency over conventional series stacked multipath inductor occupying the equivalent on-chip area.

The conventional series stacked fractal inductor (CSSFI) achieves higher inductance due to longer trace lengths for the minimal on-chip area. However, it suffers from low Q and f_{SR} due to parasitic capacitance between the adjacent metal layers. To overcome this drawback a novel hybrid series stacked differential fractal inductor using Hilbert and Sierpinski fractal curves is proposed with two different layers connected in series using vias. The proposed inductor reduces the parasitic capacitance and negative mutual inductance between the adjacent layers

that attain significant improvement in overall inductance, quality factor, and self-resonance frequency when compared with CSSFI.

An Orthogonal Series Stacked Differential Fractal Inductor (OSSDFI) is proposed in which the consecutive metal layers have 90 degrees phase shift with one another. This kind of arrangement reduces the negative mutual inductance and parasitic capacitance between the adjacent metal layers to a larger extent. Thus, OSSDFI attains a 2-fold improvement in inductance and more than 50% improvement in Q when compared with CSSFI. A narrow band LNA using cascode topology with inductive source degeneration is designed and simulated for 5G band (27-30 GHz) applications in 90 nm CMOS technology using the tool Advanced Design System. The inductors in the LNA are replaced with the proposed high Q OSSDFI contributes to high gain, better input matching, and low noise figure compared to the state-of-the-art LNAs.

The conventional parallel stacked fractal inductor attains high Q but it suffers from low self-resonance frequency values owing to huge parasitic capacitance resultant from the adjacent metal layers. To overcome this, an orthogonal parallel stacked differential fractal inductor (OPSDFI) is proposed. Similar to OSSDFI, the OPSDFI also has the orthogonal arrangement of metal layers which reduces the adjacent layer parasitic capacitance. The metal layers in the OPSDFI are interconnected together on the four corners using vias from the top layer to the bottom layer. This kind of stacking increases the overall thickness of the inductor which in turn reduces the series resistance (R_s). The combined effect of the decrease in series resistance and parasitic capacitance improves the Q of the proposed OPSDFI compared with the conventional parallel stacked fractal inductor.

A multipath differential fractal inductor is proposed for wireless applications such as satellite, WLAN, Bluetooth, Microwave, Radar, and Cellular phone, etc. The multipath technique reduces the skin and proximity effects and improves the quality factor without any change in inductance and self-resonance frequency compared to the planar fractal inductor for the equal on-chip area.

Due to the unavailability of fabrication of inductors on Silicon substrate, most of the proposed inductors are scaled down to lower frequencies (scaled up to micrometer to millimeter scale) and are fabricated on FR-4 substrate. The proposed inductors are validated experimentally using Vector Network Analyzer (VNA-N9923A) of the frequency range from 0.01GHz to 1GHz. For all the fabricated inductors, the experimental results are in good agreement with the simulated results demonstrate the robustness of the design.

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List of Abbreviations

3D	Three Dimensional
AMS	Analog/mixed signal
ADS	Advanced Design System
BPF	Band Pass Filter
CMOS	Complemtary Metal Oxide Semiconductor
EM	Electro Magnetic
FOM	Figure of merit
IC	Integrated Circuit
LNA	Low Noise Amplifier
MIM	Metal Insulator Metal
MOM	Metal Oxide Metal
PCB	Printed Circuit Board
PGS	Patterned Ground Shield
PBG	Photonic Band Gap
RF	Radio Frequency
SoC	System On Chip
SDSSI	Symmetrical Trace Differential Stacked Spiral Inductor
VCO	Voltage Controlled Oscillator
VNA	Vector Network Analyzer
WLAN	Wireless Local Area Network

List of Symbols

μm	Micro Meter
nH	Nano Henry
pF	Pico Farad
Q	Quality Factor
ε	Epsilon
η	Eta

Chapter 1

Introduction

1.1 Overview

The rapid evolution of wireless and mobile communication demands a low cost, high integration level, small volume on-chip passive components in the implementation of the receiver and transmitter. The on-chip passive components were first proposed in the 1990s, a significant amount of research was published in the literature [1, 2]. These passive components are listed as capacitors, inductors, and resistors. Most of the wireless applications necessitate the integration of multiple functions like a personal digital assistant, video game, phone, web browser, email, digital camera, etc. This has motivated the researchers to integrate digital, analog/mixed-signal (AMS) modules on a single chip to realize the Radio Frequency (RF)/mixed-signal system-on-chip (SoC) [3, 4]. The main obstacle is the integration of passive components in the realization of an SoC. Applying Moore's law active components (CMOS transistors) are successfully scaled-down to increase the component density that reduce the die size. However, the passive components cannot be scaled down as fast as the active components due to specific capacitance, resistance, and impedance levels necessary to process the analog signal.

Passive components are chosen depending on the frequency of operation of the circuit and the type of connection. For low frequency of operation, passive devices can be connected externally. As frequency increases, the parasitic effect on devices will degrade the characteristics of passive components [5]. When the frequency of operation of an RF circuits increases, the values of inductances in it needs to be reduced and it's not possible to have such small inductance value by externally connected inductors [6]. For example, to design a voltage-controlled

oscillator (VCO) of 10 MHz an inductance of several μH, is needed. However, a 10 GHz VCO needs an inductance in the order of 1 nH. It is quite difficult to design such small inductance externally since the package pin and bond wire associated inductance can exceed 1nH. As a result, on-chip passive components that offer small inductance values are commonly used in RF and mm-wave applications.

In a typical PCB (Printed Circuit Board) of the RF front end, the passive components count is higher than the active components. For example, in an Ericson cell phone board active to passive component ratio is 1 : 21 [7]. The RF-front end WLAN (Wireless Local Area Network) transceiver developed by Maxim Integrated Products (MAX2820) for IEEE 802.11b applications has a passive component count of 33 capacitors, 4 resistors, and 4 inductors [8]. In a typical cell phone, RF front end as shown in Fig.1.1, the 85% of the passive component count occupies 70% of board area with 60% of board cost [9]. A single GPS (Global Positioning System) receiver developed by Maxim Integrated Products (MAX 2742) as shown in Fig.1.2 has more than 10 inductors which occupy about 25% of the board area [10]. Thus, the board area occupied by the passive components should be minimized to reduce the board cost and also to improve the frequency of operation. The passive component count will be reduced with the advancement in fabrication technology, time to market, and domain of the application. Thus, the realization of low cost and high-performance RF systems depends on the integration of passive components.

High-quality passive components are vital in the implementation of transceivers aimed for mm-wave communication as shown in Fig.1.3, for implementation of critical building blocks such as filters, transformers, low-noise amplifiers, power amplifiers, and oscillators. The on-chip inductor is the important passive component amongst the on-chip passive components [11]. The on-chip inductor's performance is determined based on quality factor (Q), self-resonance frequency (f_{SR}), inductance (L), and on-chip area. In the present scenario due to advancements in RF-VLSI technology, the demand for high-performance inductors in terms of high Q, high f_{SR}, and optimal inductance with a small on-chip area is increased.

Depending on the design technology on-chip inductors are mainly classified into three types which are active inductors, bond wire inductors, and spiral inductors. Bond wire inductors have an exceptionally high-quality factor (typically, 20–50), but they are not unsuitable for RF applications due to unwanted coupling with the other devices [12]. The active inductors are formed using transistors and other active components [13]. The advantages of active inductors are high-quality factor, high frequency of operation, better tuning capability, ease of fabrication,

Figure 1.1: Typical cellular phone RF front end circuit (Source-BOSCH)

and occupies the small on-chip area. The drawbacks of active inductors are limitations on coupling, high power consumption, and high noise interference.

Planar inductors are highly compatible with the IC interconnect scheme. Some of the planar inductors structures are loop [14], meander [15], and spiral [16]. The spiral inductor is considered to be the best choice due to its large positive mutual inductance, robustness, and ease of design. The performance of spiral inductors is degraded owing to substrate losses and metal losses. These losses limit the Q of the spiral inductor. Symmetrical spiral inductor with differential excitation known as differential inductor [17] improves the Q and f_{SR} as they are less affected by substrate parasitics. Differential inductors exhibit better noise rejection and robustness, which is vital in transceivers. Application of fractal curves in the implementation of inductor achieves higher inductance for the miniaturized on-chip area [18]. The thesis focuses on improving the performance of the multilayer differential spiral inductors as well as differentially excited multilayer fractal inductors which will be useful for RF and mm-wave applications.

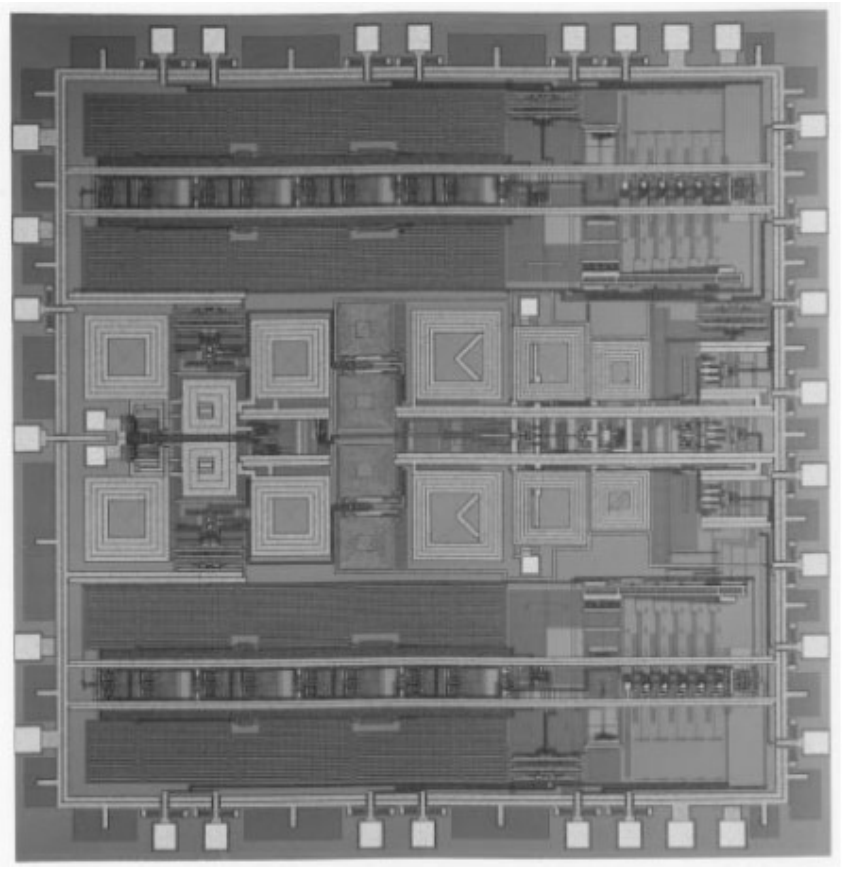


Figure 1.2: A single-chip GPS receiver (Maxim Inc.)

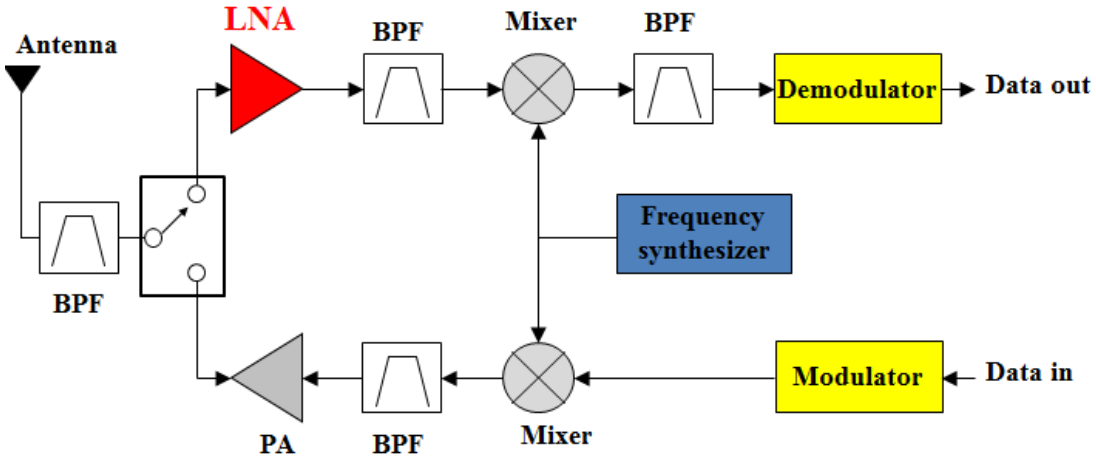


Figure 1.3: RF transceiver composed of different building blocks

1.2 On-chip inductors

1.2.1 Active inductor

Active inductors were designed using an operational amplifier (Op-Amp) and Gyrator-C based techniques. The Op-Amp based active inductor operates at low frequencies (up to 100 MHz), and it utilizes a large on-chip area and experiences non-linearity problems [19]. In contrast to this Gyrator-C based active inductor shown in Fig.1.4 operates at sub GHz to few GHz frequency range, and it occupies the small on-chip area, provides good linearity with high tunability [20]. The drawbacks of an active inductor are poor noise performance and high power consumption. The effective inductance (L_{eff}) of an active inductor is expressed using Eq.1.1

$$L_{eff} = \frac{C}{g_{m_1} g_{m_2}} \tag{1.1}$$

Where g_m is the transconductance of gain blocks and 'C' is the capacitance of the passive capacitor.

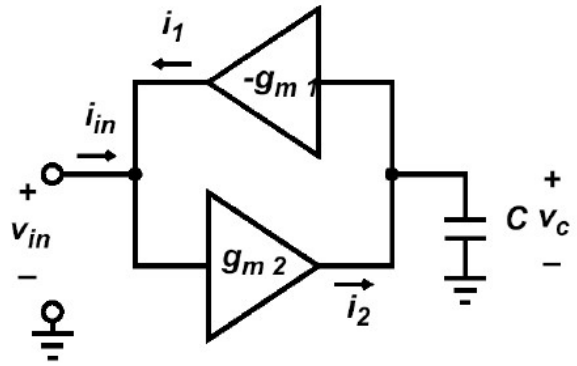


Figure 1.4: Gyrator-C based active inductor

1.2.2 Bondwire inductor

In 1995, Craninckx and Steyaert first explored on-chip bond wire inductors in RF integrated circuits [21]. Bond wires are used to make connections between a chip and an IC package has shown in Fig.1.5, and typically it offers an inductance of several nH and a resistance of several to several tens of mΩ. In general, bond wires are made of gold with a diameter of

about 25 to 250 μm and typical length of 2-5 mm. The series resistance of the bondwire inductors is very small, therefore it offers high quality factor typically 30 to 60. The performance of the bondwire inductor depends on length of the wire (l), diameter (d), height of the substrate (h), and frequency of operation. The physical dimensions and equivalent circuit of bondwire inductor has shown in Fig.1.6,

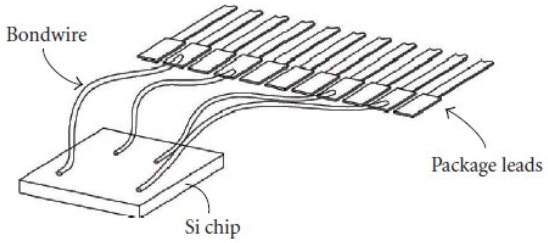


Figure 1.5: Interconnection of metal leads and packaged IC chip through bondwires

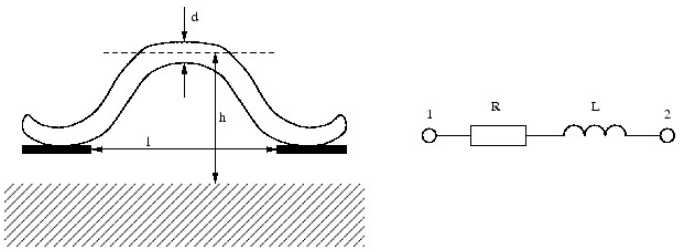


Figure 1.6: Bond wire and its equivalent circuit

The size of the bond wire is typically 100 μm $\times$ 100 μm, which introduce considerable parasitic capacitance and resistance due to underpass oxide layer and silicon. Due to these constraints bond wire inductors operation at higher-order frequencies is limited in terms of the quality factor, inductance, and self-resonance frequency.

1.2.3 Spiral inductor

The spiral inductor design shapes are circular, octagonal, hexagonal, and square. Among them, square, rectangle, and octagonal inductors are used most frequently in the circuits due to high Q and effective utilization of the on-chip area. The performance metrics such as inductance, quality factor, and self-resonance frequency are shown in Fig. 1.7. From Fig. 1.7, region I is considered as an inductive region. The frequency at which the Q value becomes '0' is known as self-resonance frequency (f_{SR}) of the inductor, after the (f_{SR}), the inductor behaves like a capacitor. The Q, L, and f_{SR} greatly affected by many parameters. Those parameters are classified into design-controlled parameters and process-controlled parameters. The design controlled parameters of the spiral inductor are also known as lateral parameters which are

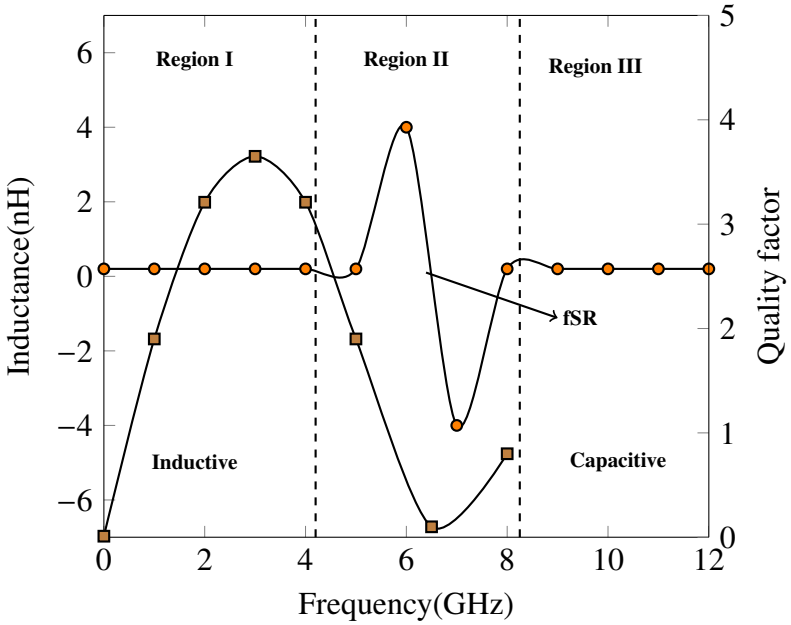


Figure 1.7: Performance metrics of on-chip inductor

known as inner diameter (d_{in}), outer diameter (d_{out}), the width of the conductor (w), the spacing between the adjacent conductors (s), and the number of turns (n). Different shapes of planar spiral inductors and the lateral parameters are shown in Fig.1.8.

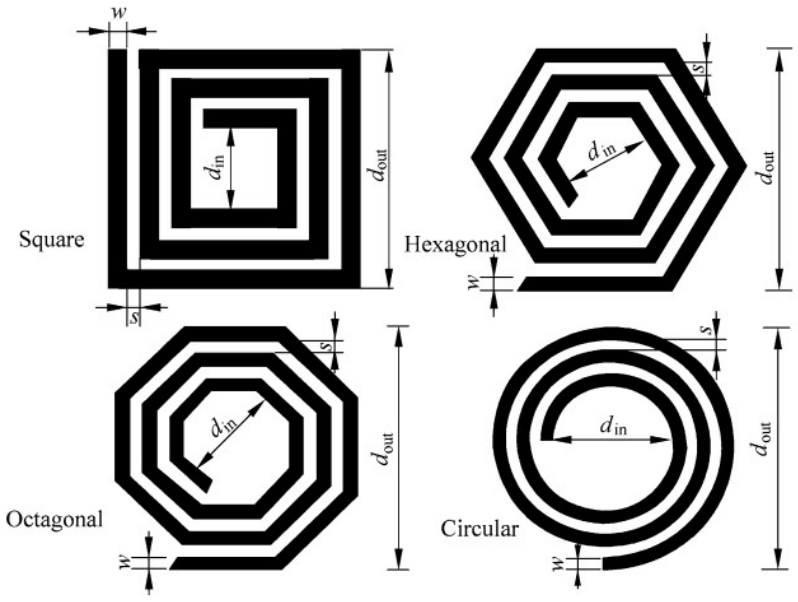
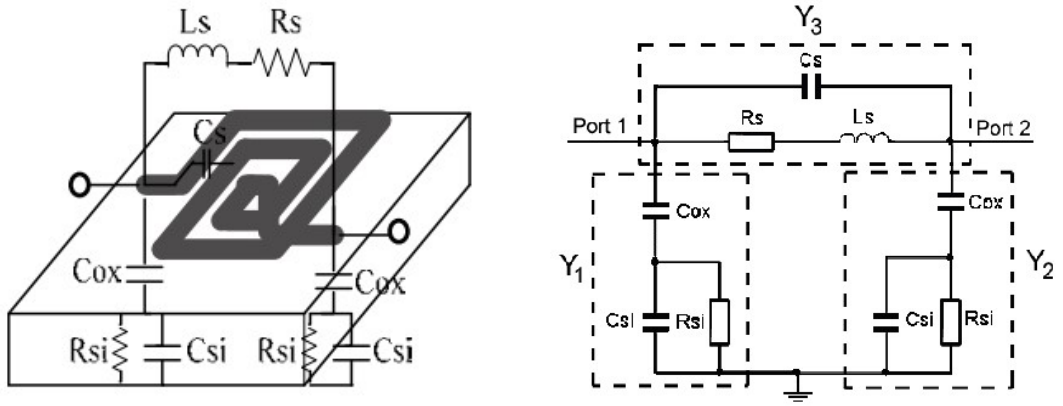


Figure 1.8: Different shapes and lateral parameters of planar spiral inductor

Process-controlled parameters are also known as 'vertical' parameters. They are metal resistivity, substrate resistivity, oxide thickness, metal thickness, and the number of metal layers. These parameters are used to define the inductance, capacitance, quality factor, and other parasitic elements of the inductor such as series resistance (R_s), oxide capacitance (C_{ox}), sub-

strate capacitance (C_{si}), substrate resistance (R_{si}), and spiral capacitance (C_s). Based on these parameters the physical model (π-model) of spiral inductor [22] is derived and it is shown in Fig.1.9.



(a) 3D view (b) Physical model of spiral inductor on Silicon

Figure 1.9: Typical π–equivalent model of spiral inductor

1.2.4 Impact of parasitics on the performance of on-chip inductor

The inductor is designed to store magnetic energy, but its inherent resistance and capacitance are counter-productive and are referred to as parasitic resistance and capacitance. The physical model shown in Fig.1.9, illustrates the parasitic resistance and capacitances associated with the on-chip inductor. This model is used to investigate the performance of the on-chip inductor at low frequencies of a few MHz and high frequencies of several gigahertz.

The Q of an inductor is the amount of energy stored to the amount of energy dissipated in one cycle of the excitation. The expression for the quality factor of on-chip inductor taking magnetic energy and electrical energy into consideration is given in Eq.1.2.

$$Q = 2\pi \left(\frac{\text{Peak Magnetic Energy - Peak Electrical Energy}}{\text{Energy loss in one oscillation cycle}} \right) \tag{1.2}$$

The Q of the on-chip inductor mounted on a silicon substrate, which is derived from the physical model is given in Eq.1.3 [22].

$$Q = \underbrace{\frac{\omega L}{R_s}}_{\text{ohmic loss}} \cdot \underbrace{\frac{R_p}{\left(R_p + \left[(\omega L/R_s)^2 + 1\right] R_s\right)}}_{\text{substrate loss}} \cdot \underbrace{\left[1 - \frac{R_s^2\left(C_s + C_p\right)}{L} - \omega^2 L\left(C_s + C_p\right)\right]}_{\text{self-resonance factor}} \tag{1.3}$$

$$R_p = \frac{1}{\omega^2 C_{ox} R_{Si}} + \frac{R_{Si}(C_{ox} + C_{Si})^2}{C_{ox}^2} \tag{1.4}$$

$$C_p = C_{ox}.\frac{1 + \omega^2(C_{ox} + C_{Si})C_{Si}R_{Si}^2}{1 + \omega^2(C_{ox} + C_{Si})^2 R_{Si}^2} \tag{1.5}$$

The inductor's self-resonance frequency (f_{SR}) is represented in Eq.1.6.

$$f_{SR} = \frac{1}{2\pi\sqrt{LC_{eq}}}. \tag{1.6}$$

In Eq.1.3, ω is known as the angular frequency at which stored energy is measured, R_s is the series resistance of the inductor, L is the total inductance, C_{ox} is the oxide capacitance between the spiral and substrate, C_s is the capacitance between metal traces, C_{Si} is the substrate capacitance, and R_{Si} is the substrate resistance. In Eq.1.4 and Eq.1.5, R_p and C_p are the total parasitic resistance and capacitances, respectively, which are the resultant of the oxide capacitance (C_{ox}), substrate capacitance (C_{Si}), and substrate resistance (R_{Si}) [22]. In Eq.1.6, C_{eq} is the parasitic capacitance resultant of C_s and C_p [23].

In Eq.1.3, the first term $\frac{\omega L}{R_s}$ accounts for the stored magnetic energy and the ohmic loss in the series resistance. At a low-frequency regime, the Q of the inductor is dependent on series resistance, and it is well described by $\frac{\omega L}{R_s}$.

The second term in Eq.1.3, represents the substrate loss factor. At high frequencies (Giga Hertz Range) the Q factor decreases and it is due to the combined effect of substrate loss and self-resonance. Physically, the substrate loss is due to penetration of electrically induced displacement current from metal-to-substrate and it is modeled by a substrate RC network comprised of C_{ox}, R_{Si}, and C_{Si} shown in Fig. 1.9. For typical on-chip inductors, the substrate loss factor causes 10 to 40% reduction in Q [22].

The last term in Eq.1.3, represents the self-resonance factor. The self-resonance factor describes the decrease in Q owing to the increase in the peak electric energy with frequency and the vanishing of Q at the self-resonance frequency.

In addition to Q, the total inductance (L) of the inductor is also affected at high frequencies. The substrate loss due to the magnetic field can be modeled as the mutual inductance between the metal and substrate [11]. The magnetically induced eddy currents will flow in a direction opposite to that of the current in the spiral. This mechanism increases the negative mutual inductance of the spiral and thus reduces the total inductance and hence Q. At gigahertz frequencies, the current crowding in the conductor reduces the skin depth and increases the resistance. The increase in series resistance causes a decrease in the Q [22]. The performance of the multilayer inductors and multilayer multipath inductrs at high frequencies is well decribed using the multilayer physical model which is derived from the single layer physical model [100, 103, 106]. The performance of the inductor is deteriorated after the peak Q frequency (f_{Qmax}) due to high substrate losses and current crowding effects.

The Y-parameters of the π-model for inductors can be directly determined from the π network series and shunt impedances [23]. The inductance, quality factor, and series resistance are determined from Y-parameters using Eq.1.7, Eq.1.8, and Eq.1.9 [24], respectively.

$$L = Im(\frac{-1}{2\pi f Y_{11}}) \tag{1.7}$$

$$Q = \frac{Im(Y_{11})}{Re(Y_{11})} \tag{1.8}$$

$$R_s = \frac{1}{Re(Y_{12})}. \tag{1.9}$$

1.2.5 Losses in spiral inductor

The spiral inductor's performance at high frequencies was degraded owing to substrate losses and ohmic losses [25]. The substrate losses are due to the penetration of Electric and Magnetic fields into the substrate, which is shown in Fig.1.10. The ohmic losses or metal losses are due to non-uniform current distribution within the metal arisen from skin effect and proximity effect [26].

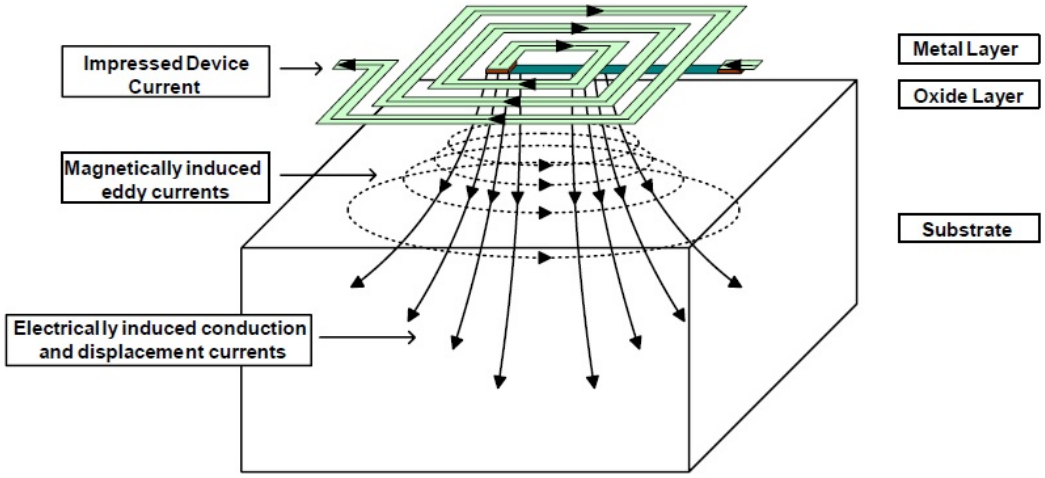


Figure 1.10: Substrate losses in spiral

Skin effect is defined as at any given frequency the magnetic field penetration through the metal line produces current flowing near the surface of the metal. Skin effect loss is dependent on skin depth (δ). The magnetic field generated from the adjacent metal lines induces the eddy currents and causes non-uniform current distribution in the metal. This phenomenon is called the proximity effect. The skin and proximity effects increase the effective resistance of the metal trace, which is shown in Fig.1.11. Thus, at a high frequency of operation increase in skin and proximity effects increases the series resistance of the inductor which in turn decreases the Q.

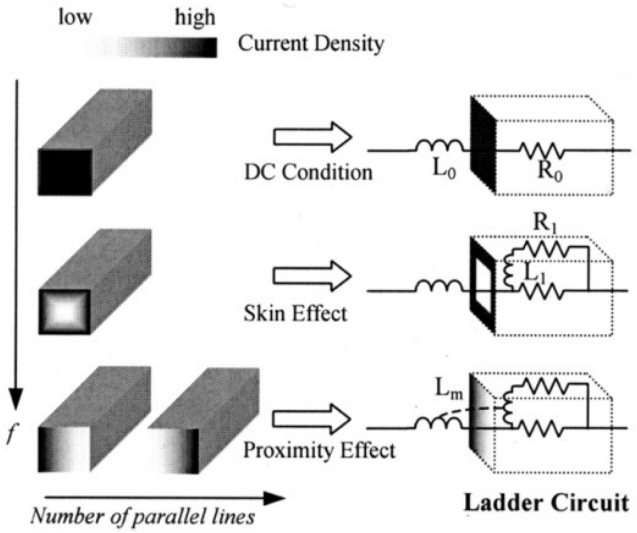


Figure 1.11: Variation of skin and proximity effects with frequency

To enhance the performance of spiral inductors in terms of figures-of merit (such as quality factor, inductance) different techniques were proposed. Substrate etching [27] as well as

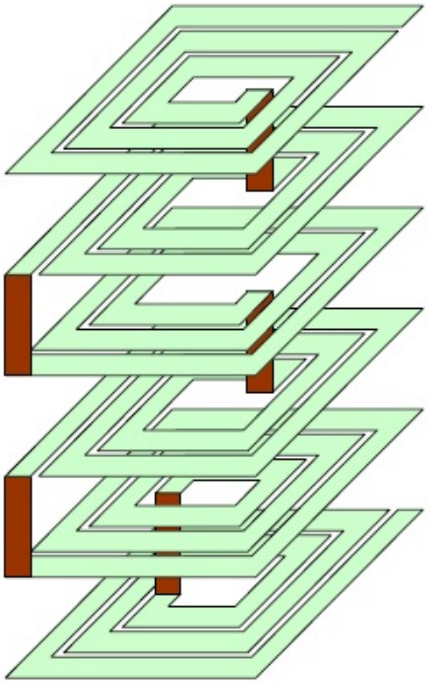
utilization of patterned ground shield [28] beneath the inductor and utilization of high resistivity substrate [29] had reduced the substrate losses and increased the Q at the expense of low f_{SR}. However, these techniques had an unusual and expensive fabrication process and not compatible with other active MOS devices. Differential inductors were proposed in the literature to increase the Q of the inductor without altering the fabrication process.

The performance of the spiral inductors was further improved by implementing them in multiple layers. In multilayer inductors, spirals are connected either connected in series or parallel in different metal layers. The spirals connected in series increases the total inductance and occupies the same on-chip area as compared with planar inductor [30]. The parallel connection of metal layers [31] increases the effective thickness of the metal which in turn decreases the series resistance and improves the Q. The series stacked and parallel stacked inductors are shown in Fig.1.12.

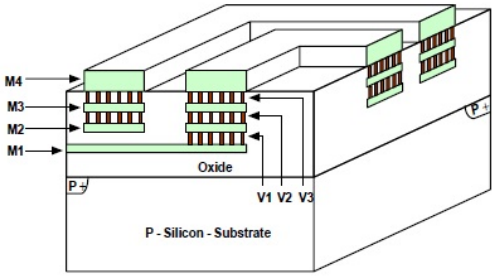
1.2.6 Differential inductor

The spiral inductors are classified into symmetrical and asymmetrical inductors based on the arrangement of ports. In the asymmetrical spiral inductor (conventional spiral inductor) as shown in Fig.1.13, the ports are on the opposite side of the structure, whereas in the symmetrical spiral inductor the ports are on the same side of the structure. The asymmetrical inductor is realized using a pair of asymmetrical spiral inductors shown in Fig.1.14 occupies a large on-chip area. A fully symmetrical inductor as shown in Fig.1.15 is realized by joining two separate spirals with a single spiral from one side of an axis of symmetry to the other using a number of cross-over and cross-under connections occupy a small on-chip area [17]. This winding style was first reported by Rabjohn [32] to connect both primary and secondary coils of the monolithic transformers.

The inductor can be excited in two possible ways, one is a single-ended (single port) mode and the other is differential (two/dual) mode. In single-ended excitation, one port is connected to the source and the other port is grounded. In differential excitation, the two ports are connected to the source (i.e. voltages and currents on the two ports are 180 degrees out of phase). The difference between single-ended and differential excitation is shown in Fig.1.16. The symmetrical inductor with differential excitation is referred to as the differential inductor. In differential excitation the two voltages V_1 and V_2 are in anti-phase, however, the currents I_1 and I_2 are in the same direction. This strengthens the magnetic field produced by the parallel conductor's groups and increases the overall inductance per unit area. The differential inductor



(a) Series stacked inductor



(b) Parallel stacked spiral using vias

Figure 1.12: Multiple metal stacking of the inductor

is best suited for the connection of the active devices as the input ports are on the same side of the structure.

The equivalent circuits derived from the π-model of the spiral inductor is shown in Fig.1.17 for the single-ended and differential excitation. The quality factor for both single-ended (Q_{se}) and differential excitations (Q_{diff}) are given in Eq.1.11 and Eq.1.12 [33]. Q_o is known as the quality factor corresponding to ohmic losses given in Eq.1.10. From Fig.1.17, it is evident that in differential excitation the substrate parasitic resistance R_P was doubled and C_p reduced to half [33]. This implies a huge reduction in substrate losses. Thus, the Q of the inductor had

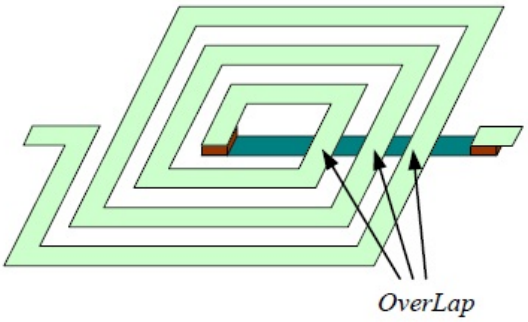


Figure 1.13: Asymmetrical spiral inductor

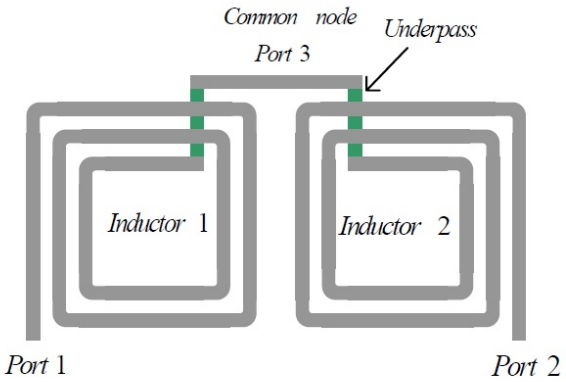


Figure 1.14: Symmetric spiral inductor using two asymmetrical spiral inductors

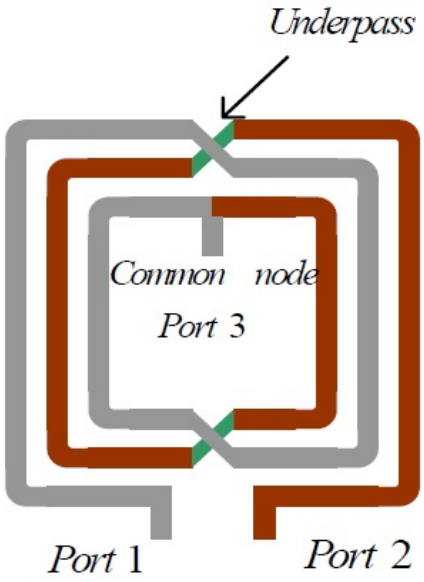
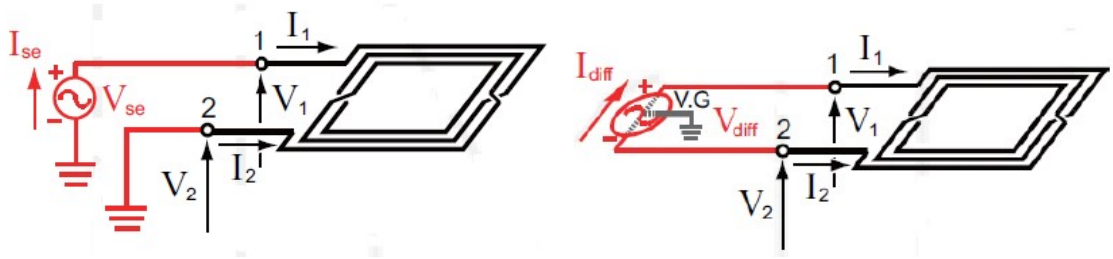
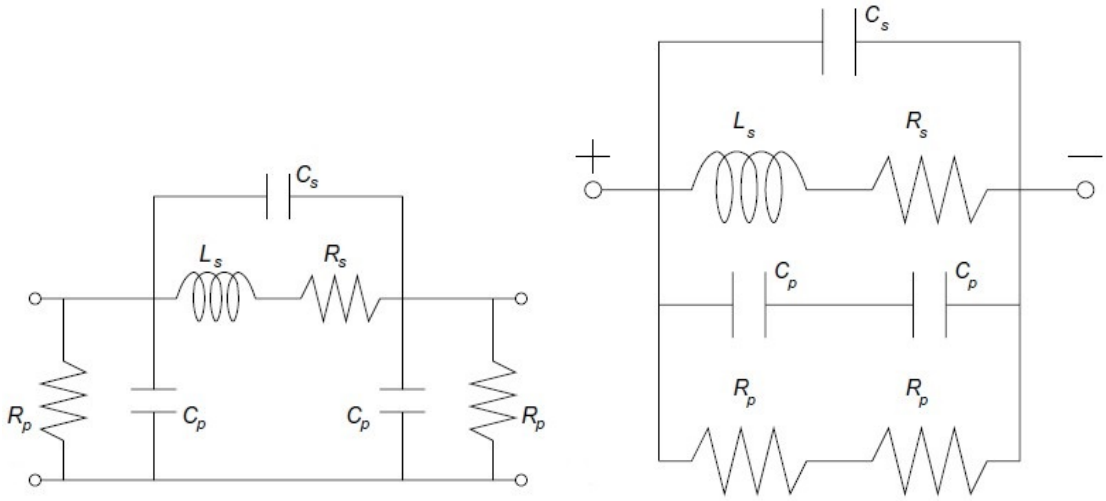


Figure 1.15: Symmetric spiral inductor



(a) Single-ended (b) Differential

Figure 1.16: Excitation of symmetric spiral inductor



(a) Single-ended (b) Differential

Figure 1.17: Lumped equivalent circuits for different excitations

greatly improved when driven differentially without altering the fabrication process. The f_{SR} had increased owing to decrease in effective parasitic capacitance from $C_p + C_O$ to $C_p/2 + C_O$.

$$Q_o = \frac{\omega L_s}{R_s} \tag{1.10}$$

$$Q_{se} = Q_o . \frac{1 - \left(\frac{R_s^2}{L_s} - \omega^2 L_s\right)(C_p + C_s)}{1 + \frac{R_s}{R_p}\left[1 + \left(\frac{\omega L_s}{R_s}\right)^2\right]} \tag{1.11}$$

$$Q_{diff} = Q_o . \frac{1 - \left(\frac{R_s^2}{L_s} - \omega^2 L_s\right)(\frac{C_p}{2} + C_s)}{1 + \frac{R_s}{2R_p}\left[1 + \left(\frac{\omega L_s}{R_s}\right)^2\right]} \tag{1.12}$$

The inductance, quality factor, and series resistance are calculated from the S-parameters obtained from the EM simulator or the vector network analyzer (VNA). Initially, S-parameters are converted into Y-parameters and the input impedance for the single-ended and differential excitation are calculated using Eq.1.13 and Eq.1.14 [33, 34]:

$$Z_{se} = 0.5 * (\frac{1}{Y_{11}} + \frac{1}{Y_{22}}) \tag{1.13}$$

$$Z_{diff} = \frac{(Y_{11} + Y_{12} + Y_{21} + Y_{22})}{(Y_{11}Y_{22} - Y_{12}Y_{21})} \tag{1.14}$$

Where, Y_{11} denotes the short circuit input admittance, Y_{22} denotes the short circuit output admittance, Y_{12} denotes the short circuit reverse transfer admittance, and Y_{21} denotes the short circuit forward transfer admittance.

The quality factor, inductance, and series resistance for single-ended and differential excitation are calculated using following equations [33, 34]:

$$Q_{se} = \frac{Imag(Z_{se})}{Real(Z_{se})} \tag{1.15}$$

$$Q_{diff} = \frac{Imag(Z_{diff})}{Real(Z_{diff})} \tag{1.16}$$

$$L_{se} = \frac{Imag(Z_{se})}{\omega} \tag{1.17}$$

$$L_{diff} = \frac{Imag(Z_{diff})}{\omega} \tag{1.18}$$

$$R_{se} = \frac{1}{Real(Y_{11})} \tag{1.19}$$

$$R_{diff} = Real(Z_{diff}) \tag{1.20}$$

1.3 On-chip capacitors

The capacitor is an important passive component in wireless RF applications. Types of on-chip capacitors available are MOS capacitors, MIM capacitors, MEMS capacitors, and passive capacitors. Capacitors are often used in impedance matching networks, RF oscillators, tuned resonators, and dc blocking circuits. In these circuits, area-efficient capacitors are highly desirable as capacitor occupies larger space in the die. The design of low leakage and high-performance capacitors is challenging in IC fabrication. The performance of the on-chip capacitor is measured in terms of capacitance per unit area, quality factor, and self-resonance frequency which are shown in Fig.1.18. The calculation of capacitance and quality factor values are given by Eq.1.21 and Eq.1.22 [24].

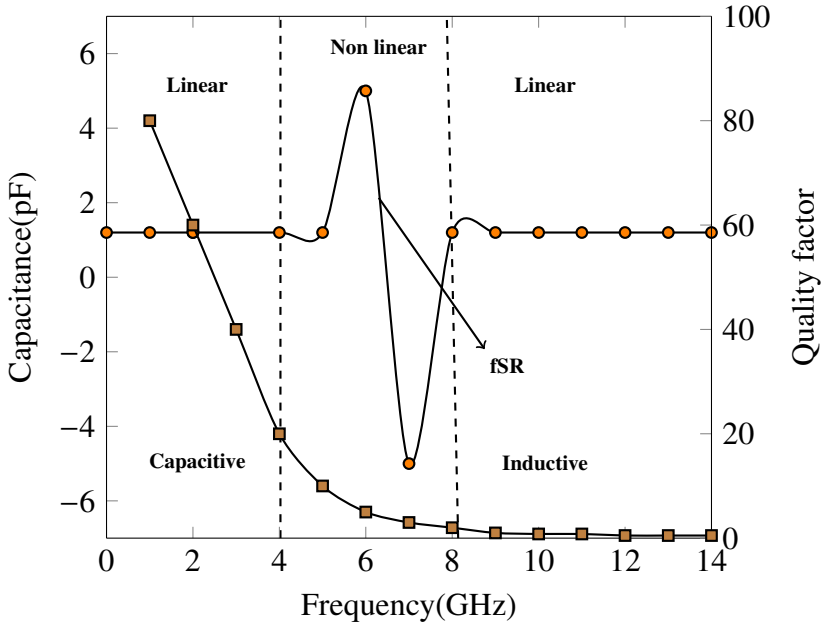


Figure 1.18: Performance metrics of on-chip capacitor

$$Capacitance = \frac{-Im[Y_{21}]}{2\pi f} \tag{1.21}$$

$$Q\ factor = \frac{Im[Y_{11}]}{Re[Y_{11}]} \tag{1.22}$$

MOS capacitors have been utilized for a long time because of the benefits of easy integration and native MOSFET fabrication [35, 36]. However, the MOS capacitor suffers from non-linear behavior, sensitivity, and poor quality factor that limits their application. Due to this, metal electrode parallel plate capacitors in nano-structure became popular, later it was termed

as Metal-Insulator-Metal (MIM) capacitors [37, 38]. These are constructed from a thin insulation film between two metal planes as shown in Fig. 1.19. The advantage of the MIM capacitor is insensitivity to a silicon substrate as the capacitor is formed by enclosing the electric field between the upper metal layers. However, as the capacitance is inversely proportional to the thickness of the insulator that does not scale with process technology, MIM capacitors do not follow technology scaling. Hence, the area of the capacitors relatively increases with progress in CMOS process technology. MEMS (Micro Electro Mechanical Systems) capacitor occupies a small on-chip area with high volume fabrication and it also attains high Q and f_{SR} with low power consumption [39, 40]. These are very much sensitive to the parasitic capacitive coupling between the substrate and metals and also suffer from inherent parasitic inductance. Fractal curves used in the implementation of capacitors increase the capacitance density and obtains high self-resonance frequency [41, 42]. The MEMS fractal capacitor is shown in Fig. 1.20.

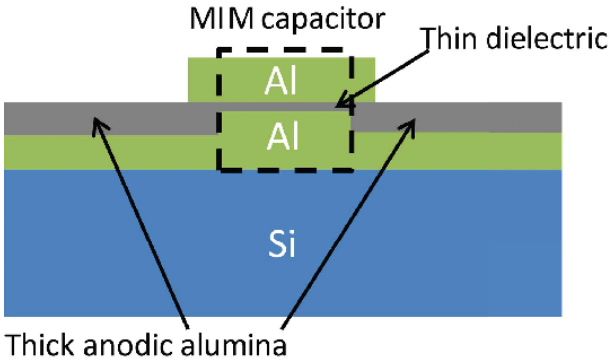


Figure 1.19: MIM capacitor

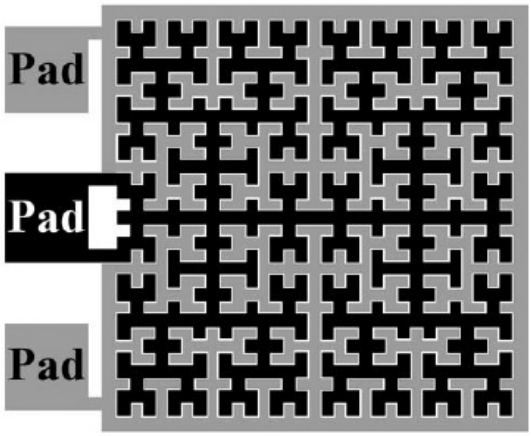


Figure 1.20: MEMS capacitor

1.4 Fractal curves

The French mathematician Mandelbrot discovered the term fractal which symbolizes broken or irregular fragments that fills every point in a bounded area [43]. Fractal has various properties like space-filling, recursive, infinite, and self-symmetry [44]. The fractal curves are typically defined by an iterative process. Some of the fractals are derived from mathematical formulas and some are derived from natural phenomena such as mountains, clouds, and trees. Generally, fractal curves are divided into two types, natural (random) and mathematical (deterministic). Nature fractals are all those that are available in nature-clouds, mountains, trees, leaves, valleys, and the human respiratory system. Fig. 1.21 shows examples of a few natural fractal curves. Mathematical fractals are developed using mathematical formulas and the concepts of iteration, recursion, etc. Widely known mathematical fractal curves are Hilbert, Sierpinski, Koch, Moore, Peano, etc [45, 46]. The mathematical space-filling curves are easily constructed using iterative algorithm [47]. Some of the well known mathematical space-filling curves are shown in Fig.1.22.

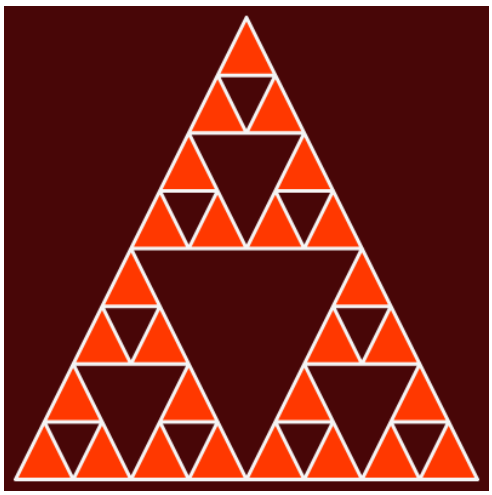
1.4.1 Applications of fractal geometry

The advancement in wireless communication systems has brought new challenges to the design and production of very good compact components. Such challenges encourage developers to find key solutions using different fractal geometries [48, 49]. Fractals are used in several branches of science and engineering disciplines such as image processing, microwave circuits, mechanics, forest and atmospheric sciences, and geology. One area of application that has impacted modern technology most is image compression using fractal image coding. Fractal image rendering and image compression schemes have led to a significant reduction in memory requirements and processing time. The self-similarity of the fractal geometry has been attributed to the dual-band nature of their frequency response.

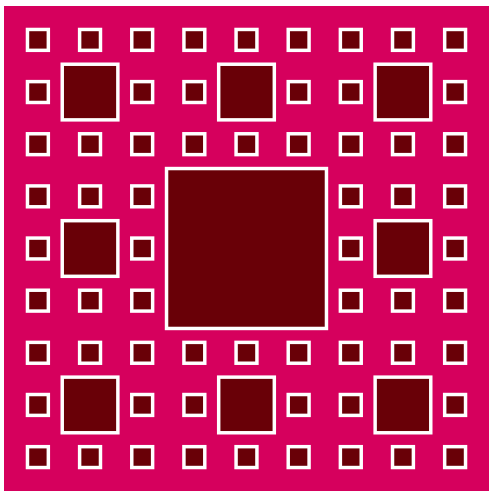
Integrated passive components such as capacitors, inductors, and resistors are the building blocks in MMICs to minimize the on-chip area. Fractal technology opens a new scope of opportunities in the miniaturization of passive RF and microwave components. Fractal-based electrical devices have been formerly demonstrated which includes fractal inductors, fractal capacitors, fractal sensors, fractal transformers, and fractal antennas. Fractal inductor attains large inductance value with miniaturized on-chip area compared to conventional planar spiral inductor [50, 51]. Fractal capacitors have high capacitance density in a single layer process

(a) Fern leaf-a natural fractal object

(b) Snow Flake



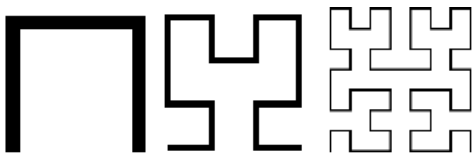
(c) Sierpinski Carpet



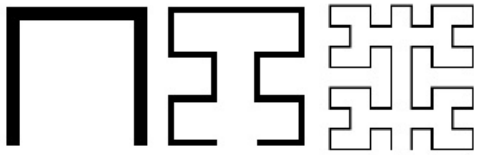
(d) Sierpinski Triangle

Figure 1.21: Natural fractal curves

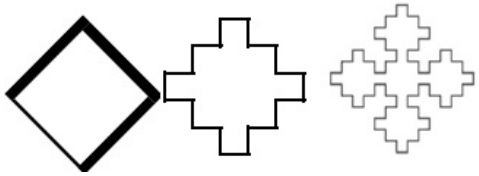
[52, 53], fractal sensors have smart sensing and compact size [54], fractal antennas have useful multiband frequency behavior [55, 56], and fractal transformers have higher inductance and reduced micro-fabrication complexity [57]. Wireless communication systems are getting benefited from the implementation of fractal passive components along with the filter and antennas. Fractal based inductor, capacitor, and transformer are shown in Fig.1.23, Fig.1.24, and Fig.1.25, respectively.



(a) Construction of Hilbert curve



(b) Construction of Moore curve



(c) Construction of Sierpinski curve

Figure 1.22: Mathematical fractal curves

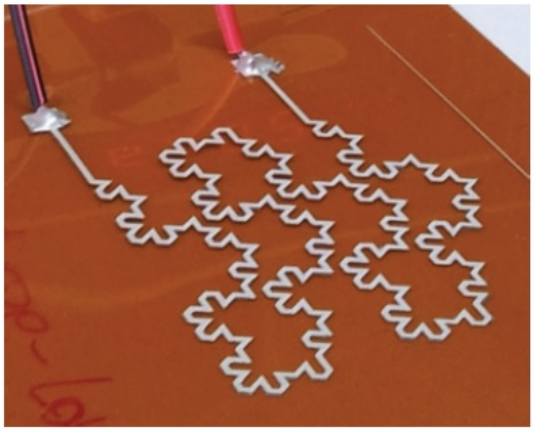


Figure 1.23: Fractal inductor

Figure 1.24: Fractal capacitor

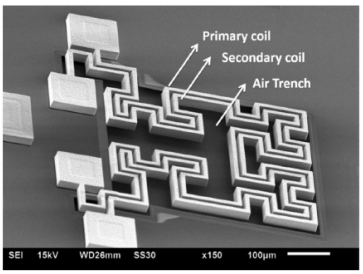


Figure 1.25: Fractal transformer

1.5 Low noise amplifier

Low noise amplifiers are key building blocks of the receiver in a wireless communication system. The input signal to the LNA is very weak and the main function of the LNA is to provide sufficient gain to suppress the noise of subsequent stages while adding as little noise as possible. The performance metrics of the LNA are gain, noise figure (NF), input matching, power dissipation, linearity, and stability factor.

The universal topology of an LNA circuit can be consists of three stages as shown in Fig. 1.26. It has the input matching network, transistor amplifier, and finally output matching network. Several LNA topologies were proposed in the literature have their own merits and demerits. The CG (common gate) and CS (common source) are mostly used configurations in the design of CMOS LNA circuits. The CS LNA provides high gain and good noise performance [58]. However, the bandwidth of the CS amplifier is low due to the miller effect. Placing an inductor in the source of a CS stage the well-known inductive source degeneration topology is obtained. The common source LNA with inductive degeneration improves the gain and noise performance of the LNA and it is used to design narrowband LNA circuits [59]. The CG LNA configuration provides better input matching, better reverse isolation, good linearity, and large bandwidth. However, it has poor noise performance. Few techniques, such as capacitive cross-coupling, has been presented to improve the CG stage noise performance [60, 61, 62]. Wide-band input matching is possible for CG configuration and hence this configuration is widely used in broadband LNA circuits [63, 64, 65].

Cascode LNA as shown in Fig. 1.29 provides superior noise performance, high power gain, low power consumption, and better reverse isolation [66, 67, 68]. Unfortunately, excellent noise and gain performance of cascode stage degrade at very high microwave frequencies. This is due to the increase in substrate parasitic admittance at the drain-source common node with the increase in frequency[69, 70]. Like a CS stage, the cascode stage is proper for narrowband applications, however using feedback techniques makes it possible using of cascode stage in multi-band and wideband applications [71, 72]. Another way to use cascode configuration in the wideband application is using complicated LC matching networks in the input [73].

The broadband input matching, high gain, and wide operation were obtained by distributed amplifiers (DA) [74] and multistage LNAs [75]. As the distributed amplifier and multistage LNAs are built from multiple cascading stages low power consumption and the minimal on-chip area would be difficult to obtain. The current-reuse LNA is exceptional for its ability to deliver high-performance in terms of low power dissipation, flat gain, low NF, good linearity,

and good input matching [76, 77]. Different noise cancellation techniques are proposed to improve the noise performance of the LNA [78, 79]. Multistage cascode LNAs have shown good performance in mm-wave frequency range [80, 81]. Likewise, various LNA topologies were proposed and still, research is going on optimize the performance of the LNA.

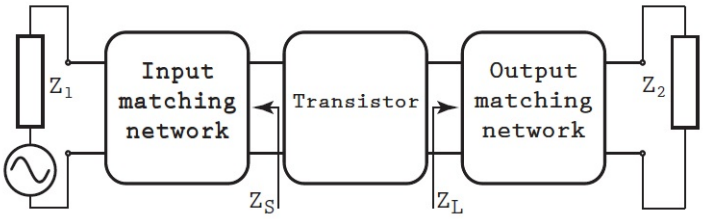


Figure 1.26: Block diagram of LNA

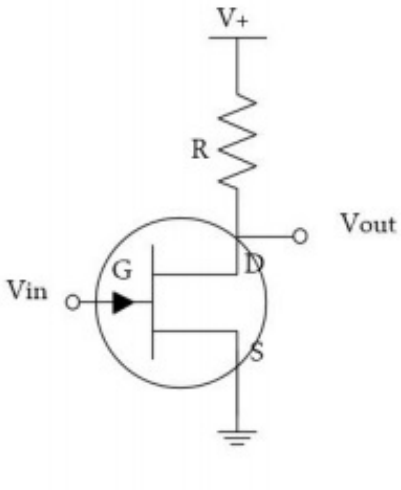


Figure 1.27: Common source

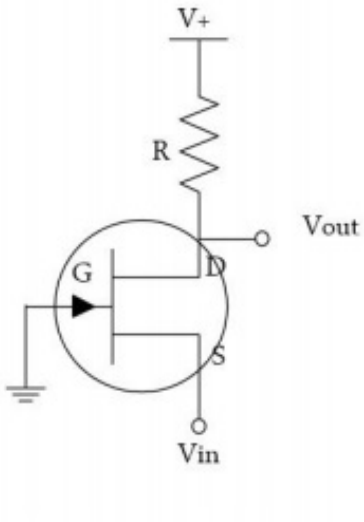


Figure 1.28: Common gate

1.6 Design tool and Measurement setup

Design, modeling, filed distribution, and scattering parameters of the proposed on-chip inductors are carried out by EM simulators. The EM simulators used in most of the works in this thesis are High-Frequency Structural Simulator (HFSS), Sonnet, and ADS (Advanced Design System) Momentum. To verify the characteristics of fabricated devices Vector Network Analyzer (VNA) is used. In addition to device characteristics, circuit simulations are performed using ADS (Advanced Design System) circuit simulator.

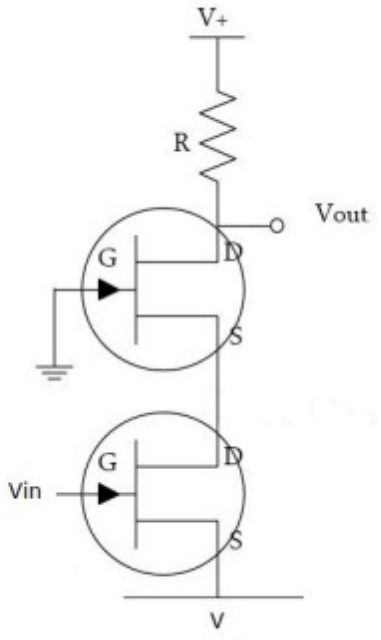


Figure 1.29: Cascode LNA

1.7 Motivation

Most of the circuits like LNA and VCO in analog and mixed-signal RFICs and MMICs are typically operated in a differential signal mode. Differential inductors are considered to be the best choice for implementing the differential circuits due to superior noise rejection properties and miniaturized on-chip area. High-quality factor on-chip differential inductors are essential to enhance the performance of a conventional integrated circuit.

1.8 Problem statement

To design a high-performance differential inductor that can be used for RF and mm-wave applications to enhance the performance of the system.

1.9 Objectives

- To design multilayer differential spiral inductor using multipath technique.

- To design and implement multilayer series stacked, parallel stacked, and planar multipath differential fractal inductors.
- To fabricate the proposed inductors and validate the simulation results with the measured results.
- To implement Low Noise Amplifier using proposed differential fractal inductors for high frequency applications.

1.10 Organization of Work

The thesis presents a performance analysis of on-chip multilayer differential spiral inductors and differential fractal inductors to improve performance metrics of the components for the equivalent on-chip area. It also deals with the implementation of LNA using proposed inductors.

Chapter 2 reviews the notable amount of most updated literature and a brief outline of the thesis is also presented.

Chapter 3 deals with the design and simulation of multilayer differential spiral inductor using multipath and variable width techniques.

Chapter 4 deals with the design and implementation of a novel hybrid series stacked differential fractal inductor for MMIC applications.

Chapter 5 deals with the design and implementation of multilayer stacked differential fractal inductors. It also deals with the design of narrowband LNA using the proposed OSSDFI. Furthermore, the performance of the proposed inductor and LNA circuit is compared with the existing state-of-the-art.

Chapter 6 deals with the design and implementation of multipath differential fractal inductor for wireless applications.

Chapter 7, conclusion of the thesis is summarized from the contributions and a brief discussion on the direction for future work is given.

Chapter 2

Literature Survey

2.1 Introduction

Development in wireless communication shows a keen interest in the design of radio transceivers. On-chip inductors integrated into RFIC's play a significant role in minimizing the size of radio transceivers. On-chip inductors play a fundamental role in RF circuits at a higher operating frequency, leading to different innovative structures over the years. In the subsequent sections, different on-chip inductors are reported and discussed according to the type of structure. These are not necessarily in the order of the year reported.

2.2 Review on On-Chip Inductor Design

The fabrication of inductor structures was investigated in the early 60s, but it was observed that inductors are the most difficult component to integrate because of their large on-chip area requirement and low-Q factor at GHz frequency practical applications. From conventional planar spiral inductors to several multilayer spiral inductors, the literature covers a wide range of on-chip inductors. The fractal curves were discovered to have symmetrical, space-filling, and recursive properties, which made them suitable for the development of on-chip inductors. We have included several types of fractal inductors in this literature, which offer few advantages over spiral inductors.

2.2.1 Conventional planar on-chip spiral inductors

This section describes several planar on-chip spiral inductors and their advantages and drawbacks.

In [82], E. Frlan, et al, designed and developed a lumped model for the first time to describe the characteristics of the square spiral inductor. The square spiral inductor was fabricated with 265 μm $\times$ 245 μm on-chip area on alumina substrate for the inner diameter of 160 μm. The width and spacing between the conductors are 20 μm and 10 μm, respectively. The inductor has obtained an inductance of 2 nH for low frequencies. The inductance value was reduced to 1.75 nH at self-resonance frequency of 20 GHz.

In [83], N.M. Nguyen, et al, designed and fabricated two square spiral inductors on standard Si substrate. The inductors have an outer diameter of 230 μm and 115 μm, respectively. The large and small inductors has obtained inductance values of 9.3 nH and 1.3 nH with the self-resonance frequency of 9.7 and 2.47 GHz, respectively. Both inductors have obtained Q values in the range of 3 to 8. A low pass LC filter is realized utilizing these inductors has shown better performance in terms of input matching, linearity, and power gain. The authors have realized an RF bandpass amplifier for L band (1-2 GHz) using monolithic inductor having an inductance of 4 nH in Silicon Bipolar technology [84]. The amplifier has obtained a peak gain of 8 dB, Noise Figure (NF) of 6.4 dB, and matched input impedance.

In [85], J. Burgahartz, et al, realized a square spiral inductor with 10 μm width 3.5 μm spacing for an on-chip area of 160 x 160 μm^2. The inductor has obtained a peak Q value of 9.7, inducatnce of 2.45 nH, and self-resonace frequency of 5.3 GHz. A bandpass filter (BPF), LNA, and VCO are implemented utilizing high Q square spiral inductor. Due to this, the insertion loss of BPF is improved by >5 dB, the LNA has obtained low Noise Figure (NF), low power consumption, and high gain, and the VCO has obtained power saving and improvement in phase noise by 7 dB. After this, there has been enormous progress in design, modeling, and optimization of inductors for various millimeter and microwave applications.

In [86], C.P.Yue et.al., developed a physical model for an on-chip inductor on a silicon substrate. The developed physical model is based on copper losses, substrate losses, and parasitic losses. This model helps to optimize the performance of the inductor. Several innovative inductor structures are proposed in the later years.

In [87], J.Y.C. Chang et al., designed a spiral inductor to obtain a large inductance value of 100 nH with an outer diameter of 440 μm. In this work, etching the substrate underneath the inductor reduces the substrate losses and improves the Q and self-resonance frequency of the inductor. The measurement results show that the removal of the substrate improves the self-resonance frequency to 3 GHz from 800 MHz. A balanced tuned amplifier has been implemented in a standard digital 2-μm CMOS IC process using 100 nH proposed inductor attains a power gain of 14 dB at a center frequency of 770 MHz, NF of 6 dB, the power dissipation of 7 mW from a 3-V supply.

In [88], A. Eroglu, has implemented a rectangular spiral inductor for high-frequency ISM (Industrial, Scientific, and Medical) applications. The author proposed an analytical model and algorithm to determine the physical dimensions and self-resonance frequency for the desired inductance value. After this five spiral inductors are built on 100 mil thick Alumina (Al_2O_3) substrate for different dimensions. The inductors have obtained inductance values ranging from 132 to 753 nH and self-resonance frequency values ranging from 38 to 81 MHz. The analytical results have shown better accuracy compared with simulated and measured results.

In [89], Jinglin Shi et.al, demonstrated the insertion of the patterned ground shield (PGS) beneath the inductor. The inductors and PGS were fabricated in 0.18 μm and 0.35 μm CMOS technology. The PGS provides good termination to the electric and magnetic field before it reaches the silicon substrate which reduces the substrate losses and improves the Q of the inductor to a greater extent. The authors have tested the performance of the inductor at different high temperatures and demonstrated that the use of PGS compensated for the decrease in Q. The authors have stated the effective way of separating PGS and top metal with an appropriate distance to enhance the Q for different high temperatures. The authors used metal PGS and poly strip PGS to analyze the performance of the inductor for the temperature range of 298 K to 358 K.

In [90], M.J. Chiang reported a complementary spiral-shaped electromagnetic bandgap (CSS-EBG) structure for spiral inductors and transmission line using 0.18 μm CMOS technology. The CSS-EBG structure enhances the Slow Wave factor (SWF) and characteristic impedance of the transmission line compared to conventional thin-film microstrip (TFMS) transmission line for the same line width and material properties. For spiral inductor, the CSS-EBG structure provides effective shielding to terminate the substrate coupling. This reduces the substrate losses and improves the quality factor of the inductor compared to conventional spiral inductors without shielding. The inductor attains a peak Q of 10.5 at 37.8 GHz for an outer diameter of 110 μm.

In [91], Hsien-Shun Wu et al, reported a spiral inductor incorporating a photonic bandgap (PBG) structure beneath the inductor as a ground plane substitute. The PBG ground plane is made of a thin, two-sided, printed-circuit board. The novel inductor configuration reduces the series resistance, increases the inductance, enhances the Q-factor and self-resonance frequency.

In [92], Hongrui Jaing et.al., reported silicon micromachining technique for fabrication of the spiral inductor. The spiral turns of the inductor were formed with two-layer polysilicon and suspended over 30 μm deep cavity beneath the silicon substrate. Copper (Cu) was coated onto the polysilicon spiral to achieve low resistance and Cu coated on the inner surfaces of the cavities, formed good RF ground, and electric and magnetic shielding. The electric and magnetic coupling, parasitic capacitances between the inductor and the silicon substrate are reduced by using a deep cavity. The high-quality factor of more than 30 and self-resonance frequency over 10 GHz was obtained by using a silicon micromachining technique. This process can be extended to other on-chip passive components.

In [93], C.Y Lee et.al, reported poly shielding and proton implantation techniques to optimize the quality factor of the inductor. The shielding effect and proton-bombarded substrate employed individually had improved the quality factor of the inductor by 37% and 54%, respectively compared to conventional spiral inductors without shielding. The combination of the poly shield and proton implant treatment method had improved the quality factor more than twice.

In [94], Min Park et.al, fabricated and investigated the performance of spiral inductor on three kinds of substrates having the resistivities 4-6 Ω-cm,30-50 Ω-cm, and 2K Ω-cm, respectively, using conventional CMOS technology. The utilization of high resistive substrate had reduced the substrate losses and increased the quality factor of the inductor. The detailed analysis had been done to show the effect of various layout parameters such as inner diameter, metal width and spacing, metal thickness, and the number of turns on the quality factor and inductance of the inductor for all three substrates.

In [95], Heng-Ming Hsu, proposed a spiral inductor with variation in metal width based on the arithmetic-progression step width. The metal width had decreased gradually from the outer turn to the inner turn. The decrease in metal width in the inner turns had a reduced concentration of magnetic field due to this the eddy current losses are reduced. The decrease in eddy current losses reduced the series resistance (R_s) of the inductor and increased the quality factor of the inductor compared to the standard conventional spiral inductor. The improvement in quality factor is directly proportional to the step width.

In [96], Shen Pei et.al, proposed a spiral inductor with variation in metal width according to the arithmetic progression and variation in spacing based on the geometric progression. The metal width and spacing had decreased gradually from the outer coil to the inner coil. The suppression of eddy current loss due to weak current crowding effects at the center of the inductor improves the quality factor of the inductor. The PGS is used to enhance the quality factor further.

In [97], Jing Liu, et.al, proposed a spiral inductor with variation in metal width and spacing. The metal width and spacing had decreased gradually from the outer side to the inner side of the inductor. The sum of metal width and space of each coil is fixed while the ratio of the metal width to space is gradually reduced from outside to inside. The variation in metal width and spacing had produced higher quality factor compared to variation in metal in metal width alone. However, both structures have a quality factor higher than conventional fixed width and spaced inductors.

In [98], Jing Liu, et.al, proposed a circular spiral inductor with multipath technique. In this technique, the width of the metal is divided into multiple paths based on the skin depth of the metal at the given frequency of operation. At high frequencies, the non-uniform current distribution owing to skin and proximity effects decreases the quality factor of the inductor. The multipath technique reduces the skin effect and the proximity effect by increasing the effective cross-section of the metal line, so the resistance of the inductor reduces and the quality factor increases compared to a conventional circular spiral inductor. The multipath technique produces a negligible decrease in inductance due to mutual coupling between the adjacent paths. The multipath inductor built with an on-chip area of 2300 μm $\times$ 2300 μm obtains an inductance of 240 nH.

2.2.2 Multilayer on-chip spiral inductors

Planar inductors occupy a larger on- chip area as it requires a minimum of two metal layers. Out of which one is in the top metal layer and another, the other one is an underpass. With advances in technology, the inductors can be realized by exploiting multiple metal layers.

In [99], Y Koutsoyannopoulos et.al, reported multilayer series stacked inductors for two and three layers. The metal layers are connected in series increases the overall length of the metal and increases the inductance value. In addition to this, the direction of the current in the top and bottom layers flows in the same direction which increases the positive mutual induc-

tance. The inductance increases up to 600% compared to conventional planar spiral inductors for the equivalent on-chip area. The multilayer series stacked inductors obtain large inductance values that can be obtained for the minimal on-chip area. However, the increase in parasitic capacitance between the consecutive metal layers decreases quality factor and self-resonance frequency.

In [100], Zolfaghari et al., reported a two-layer series stacked multilayer inductor using 0.25 μm technology consisting of five metal layers. The spirals are placed farther away from each other that reduces the parasitic capacitance to obtain high self-resonance frequency. The inductor implemented in the top and bottom layer (M5 and M2) has a 2-fold improvement in self-resonance frequency (1.79GHz) compared to the self-resonance frequency (0.96 GHz) of the inductor implemented in the top two consecutive layers (M5 and M4). There is not much variation in the inductance of both the inductors having the value 266 nH for an on-chip area of 240 μm $\times$ 240 μm. Stacked transformers were also implemented that obtain voltage gain of 3 (9.5 dB) at 1.5 GHz.

In [101], Chih-Chun Tang et al., proposed a miniature 3D inductor. The structure of the 3D inductor model is similar to the conventional stacked inductor but it is implemented in non-sequent metal layers. This structure reduces the metal to metal capacitance and increases the self-resonance frequency. The miniature 3D inductor consists of at least two or more stacked inductors by series connections and every stacked inductor has only one turn in every metal layer. The miniature 3D inductor is superior to the planar inductor in all aspects, especially saving about 80% area. The miniature 3D inductor has a higher self-resonance frequency than the conventional stacked inductor. The self-resonance frequency of the miniature 3D inductor is improved by 34% and the quality factor is reduced by 8% over the conventional stacked inductor for the same inductance value occupying the equivalent on-chip area. A 2.4-GHz CMOS low-noise amplifier (LNA) had implemented by utilizing the miniature 3-D inductors occupies the small on-chip area that reduced the size and cost of the RFIC. The proposed inductor is implemented in the 0.35μm one-poly-four-metal (1P4M) CMOS process.

In [102], Haobijam et.al., proposed a Multilayer Pyramidal inductor in six layers using 0.18μm technology. The metal can be traced spirally up and/or down in a pyramidal manner by connecting them in series. Pyramidal winding reduces the parasitic capacitance and increases the quality factor of the inductor. It achieves an inductance value of 23 nH with differential excitation with almost 19.5% improvement in Q factor and 30.6% improvement in self-resonance frequency over conventional planar inductors.

In [103], Xiangming Xu et.al., proposed multipath crossover interconnection octagon stacked spiral inductor which is fabricated with the 0.13 μm SiGe BiCMOS process. The metal wire of the spiral inductor is divided into multiple paths according to the process rule and the depth of the skin effects at the response frequency. The width of a single path is typically less than or equal to the skin depth. This multipath technique effectively depresses the proximity and skin effects, therefore contributing to the high Q-factor of the inductors and reducing the occupying area. The crossover-interconnection method can make the total path lengths approximately equal to each other and lowers the current-crowding effect, which also enhances the Q-factor. The proposed inductor attains 63.8% and 44% improvement in the peak Q (2.3 GHz) as compared to conventional stacked inductors (1.5 GHz) and conventional planar inductors. The proposed inductor had attained a Q value of 9.78 at 2.3 GHz with an inductance of 8.2 nH occupying an on-chip area of 0.0289 mm^2.

In [104], Venkata Narayana Rao Vanukuru et.al., proposed multipath multilayer up-down series stacking octagonal spiral inductor with equal path length. The up-down series winding reduces the interlayer capacitance which increases the peak Q and self-resonance frequency. The multipath technique lowers the skin and proximity effects and increases the slope of the quality factor characteristics. The proposed architecture simultaneously reduces both the ac resistance and capacitance while obtaining high inductance values. The proposed inductor is fabricated on a 0.18 μm high resistivity SOI (Silicon-on-Insulator) using a dual thick metal stack process. It achieves 10% improvement in peak-Q value, 50% improvement in peak Q frequency f_{Qmax}, and 100% improvement in self-resonance frequency over conventional series stacked multipath inductor.

In [105], J. N. Burghartz et.al., proposed multilevel spiral inductors using standard 0.8 *mu*m BiCMOS technology which consists of four metal layers. In the implementation of the inductor, the metal layers are shunted (connected in parallel) using dense via arrays to increase the effective thickness of the metal wire. The increase in thickness reduces the series resistance of the inductor which in turn improves the quality factor. The inductor with single metal layer (M3), shunting of three metal layers (M2/M3/M4) obtains quality factor of 6.5 and 8.6, respectively for on-chip area of 226 μm $\times$ 226 μm, 16 μm metal width, and 10 μm metal-metal space.

In [106], Venkata Narayana Rao Vanukuru et.al., proposed a multipath parallel stacked inductor. The metal layers are divided into multiple segments and cross overs are provided in the midway of each turn to make equal path lengths. The proposed inductor achieves more than 30% improvement in quality factor over conventional parallel stacked inductor owing to

reduced skin and proximity effect losses. The proposed inductor is fabricated in 0.18 μm CMOS technology on a high resistivity SOI using a dual thick metal stack process.

2.2.3 Symmetrical planar and multilayer on-chip spiral inductors

The symmetrical inductors reduce the substrate parasitics and enhance the inductor's performance to a greater extent for the same chip area. This section covers single-layer and multilayer symmetrical spiral inductors.

In [107], Mina Danesh et.al. presented a symmetric inductor structure that is excited differently that leads to improvement in quality factor and self-resonance frequency. Differently excited inductors have a higher quality factor compared with single-ended inductors since they are less affected by substrate parasitics. The proposed inductor achieves a high Q factor, self-resonance frequency for the less on-chip area.

In [108], Paul Findley et.al., presented a novel differential inductor structure to improve the self-resonance frequency. A novel differential inductor design avoids high voltage swing, high-phase-difference between the metal segments and reduces the effective shunt capacitance of each port to the ground by more than 50%. The proposed inductor attains more than 60% improvement in self-resonance frequency compared to conventional differential inductor without variation in quality factor and equivalent on-chip area.

In [109], J Chen et.al., modeled a differential inductor and transformer using an on-chip spiral inductor physical model. The equivalent circuit is drawn for each line segment considering the non-uniform current distribution and these segments are interconnected to form a differential inductor and transformer. The Q factor, inductance, and self-resonance frequency computed using the proposed model are in good agreement with the experimental data measured.

In [110], J.H. Gau et.al., presented a novel differential inductor (NDI) that is fully symmetrical in its layout compared to a conventional differential inductor (CDI). Its layout is fully symmetrical in geometry and electricity. And the center tap defined is no doubt to be the real center. The NDI and CDI are fabricated in 0.35 *mu*m BiCMOS process. The inductance of CDI and NDI are close to each other for a frequency lower than 4 GHz. However, the quality factor of NDI is a little worse than CDI due to the extra resistance from the metal trace at the center of NDI.

In [111], Wei-Zen Chen et. al., proposed a novel three-dimensional (3-D) symmetrical symmetric inductor, transformers, and balun. In the proposed multilayer 3-D symmetrical inductor each turn placed in individual layers reduces the parasitic capacitance and improves the self-resonance frequency over conventional planar inductor. However, the quality factor is degraded as the lower metal layers are placed near to the substrate. The inductance mismatch in the 3-D transformer is reduced and the coupling coefficient is increased and the 3-D balun achieves less gain mismatch and reduced phase error compared with the planar architecture. In the proposed architecture balun and transformer show wideband gain and phase matching.

In [112], Haobijam et. al., proposed a multilayer pyramidal symmetric inductor using four metal layers. The proposed inductor obtains identical inductance, quality factor, and self-resonance frequency compared to conventional differential inductor for the less on-chip area. The pyramidal structure of the symmetrical inductor reduces the parasitic capacitance and increases the self-resonance frequency compared to the conventional multilayer differential inductor. Two pyramidal inductor structures were fabricated with outer diameters 130 μm and 222 μm, respectively, in UMC 0.18 μm 1P6M RF CMOS process. The inductor with an outer diameter of 130 μm has obtained inductance value of 6.9 nH and 1 GHz with a maximum quality factor of 6 at 2.1 GHz. The other inductor with an outer diameter of 222 μm has an inductance of 27 nH with a maximum quality factor of 3 at 1.1 GHz. The proposed pyramidical inductor obtains higher inductance to area ratio (L/A) compared to planar symmetric and asymmetric inductors.

In [113], Joonchul Kim et. al., proposed a miniature symmetric trace differential stacked spiral inductor (SDSSI) using standard 0.18 μm CMOS technology. The SDSSI has a high self-resonance frequency and quality factor despite using the stacking technique because the parasitic capacitance between the layers is reduced by alternatively locating traces at different positions in each layer. A VCO is realized using SDSSI attains output power spectrum and phase noise of 0.79 dBm and 114 dBc/Hz, respectively, at 1-MHz offset frequency. The oscillation frequencies of the VCO cover from 1.84 GHz to 2.38 GHz with a tuning range of 26%. The on-chip area of the SDSSI and VCO is 80 μm^2 and 350 μm^2. The inductance and self-resonance frequencies are 5 nH and 11 GHz, respectively.

2.2.4 Planar and multilayer Fractal inductors

Fractal curves have larger conductive segments, resulting in a high inductance for the specific on-chip area. This section discusses planar and multilayer fractal inductors.

In [114], Nathan Lazarus, et.al., proposed several inductors based on space-filling curves. The space-filling property of the fractal inductor is the effective utilization of the on-chip area. The proposed inductors are replacements for serpentine inductors for the single-layer process. The developed inductors using fractal curves are suitable for stretchable electronics. The inductance density of the lower order fractal is more compared to serpentine inductors. As the number of iterations increases the inductance density decreases in fractal inductors. Fractal inductors are proven to be an efficient alternative at lower iteration to minimize the size.

In [115], Gang Wang, et.al., Presented a novel MEMS fractal inductor based on Hilbert space-filling curve. The fabricated inductor is comparable to the CMOS process. The MEMS fractal inductor achieves a 50 % improvement in inductance value compared to the planar inductor and winding form inductor.

In [116], G. Stojanovic et.al., Proposed a new lumped model for 2^{nd} order Hilbert fractal inductor based on the silicon substrate. The developed lumped model is based on the layout specifications and material properties. Frequency-dependent characteristics of fractal inductor such as quality factor and inductance with minimum tolerance are obtained. The maximum operating frequency of the device is 10GHz. It is noted that the proposed inductor has a maximum inductance value is 0.7nH and a Q factor of 15 with an area of 180μm x 235μm.

In [117], Akhendra Kumar et.al, proposed a fractal inductor based on Hilbert and Omega-shaped space-filling curves. The proposed Hilbert curve-based fractal loop inductor and omega curve-based fractal loop inductor had achieved improvements in the inductance value of 21% to 31% and 11% to 30.88%, respectively, over reported conventional planar fractal inductor. The proposed inductors are suitable for wireless applications in a frequency range of 3-500 MHz.

In [118], Kumar P et.al, proposed series stacked fractal inductor based on modified Hilbert space-filling curves. The inductor was implemented in three layers in which the bottom layers are stacked together using vias. The proposed inductor had achieved two times improvement in inductance over conventional planar fractal inductor due to mutual inductance between the plural metal layers. As the bottom layer composed of two metal layers, the thickness of the lower metal layers had greatly improved. The increase in the thickness of the lower metal layer decreases the series resistance and increases the quality factor compared to conventional series stacked fractal inductor. However, it has a moderate self-resonance frequency due to parasitic capacitance between the adjacent metal layers.

In[119], Kumar P et.al, proposed a parallel stacked fractal inductor based on modified Hilbert curves. The two metal layers of the inductor are connected by vias in parallel forms a cavity between the metal layers. The formed cavity improves the magnetic coupling between the metal layers which results in almost identical inductance value with single layer fractal inductor. The improvement in quality factor is observed due to the minimization of skin effect. The differential excitation of the inductor with parallel stacking had achieved a 50% improvement in quality factor over standard fractal inductors for the identical inductance value.

2.3 Summary

This chapter reviews the innovation and optimization of several on-chip inductors. The performance of the on-chip inductor is enhanced by implementing them in different shapes starting from a single layer to the multilayer fabrication process. Several techniques were reviewed to reduce the substrate losses to improve the Q factor. Design and optimization methods are also discussed for better performance. Several unsolved issues in the design of the fractal inductor have motivated me for this work.

Chapter 3

Multilayer spiral differential inductors

3.1 Introduction

The on-chip inductors play an important role in the design of RF circuits such as LNAs, VCOs, Bandpass filters, and other tuning circuits. Symmetrical inductor with differential excitation attains high-quality factor and high self-resonance frequency for the less on-chip area. The variable width and multipath techniques reduce the skin and proximity effects of the inductor that will improve the quality factor of the inductor. This chapter deals with the implementation of multilayer differential inductors using variable width and multipath techniques to enhance the performance of the inductor.

The design and simulation of the variable width series stacked differential inductor, variable multipath width multilayer differential inductor, series stacked non-parallel multipath differential inductor are discussed in section 3.2, section 3.3, and section 3.4, respectively.

3.2 Variable width series stacked differential spiral inductor

The proposed variable width series stacked differential spiral inductor is shown in Fig.3.1. The proposed inductor is implemented using three layers by gradually decreasing metal width from the top layer to the bottom layer. The proposed inductor is implemented for 3 turns (n) with an outer diameter (d_{out}) of 180 μm and width (w) of the metal varied from top layer to bottom layer as 14 μm, 12 μm, and 10 μm, respectively.

The series stacking helps to achieve a high inductance value for the miniaturized on-chip area [100]. The length of the conductor is made longer in the proposed inductor that increases the inductance value compared to planar standard differential inductor [104] shown in Fig.3.2.

The eddy current losses are directly proportional to the metal width of the inner turns. These Eddy current losses are reduced as the metal width decreases from the top metal layer to the bottom metal layer [95]. Thus, an increase in reduction of the metal width decreases the effective series resistance (R_s) and hence improves the quality factor. The hollow space (outer and inner diameters are equal) provided by the proposed inductor is very large compared to the standard differential inductor. The increase in hollow space reduces the magnetic field penetration into the substrate. This mechanism helps to reduce substrate losses. Thus, the decrease in substrate losses improves the Q of the inductor [120]. The novel variable width series stacked differential inductor has improvement in quality factor owing to a decrease in substrate losses and eddy current losses.

The proposed differential inductor has a high parasitic capacitance between the adjacent metal layers. The differential excitation of the inductor reduces the parasitic capacitance (C_P) to half ($C_P/2$) [95]. The decrease in parasitic capacitance due to differential excitation is compensated by an increase in parasitic capacitance when the individual turns are placed in different layers. Thus, the self-resonance frequency of the proposed differential inductor is maintained almost constant compared to the planar differential inductor.

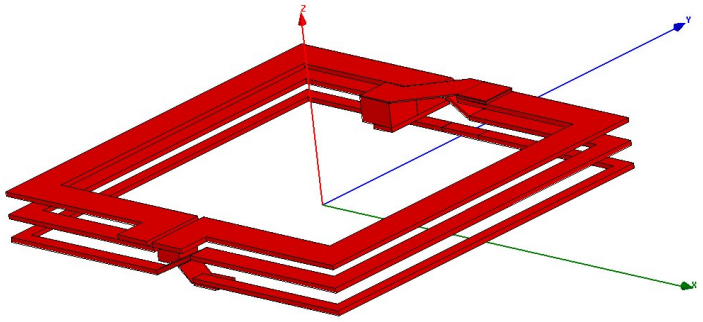


Figure 3.1: Proposed variable width series stacked differential inductor

3.2.1 Simulation results and discussion

The proposed inductor is simulated in single ended and differential excitation modes. The input impedance, quality factor, and inductance for both single ended and differential excitation

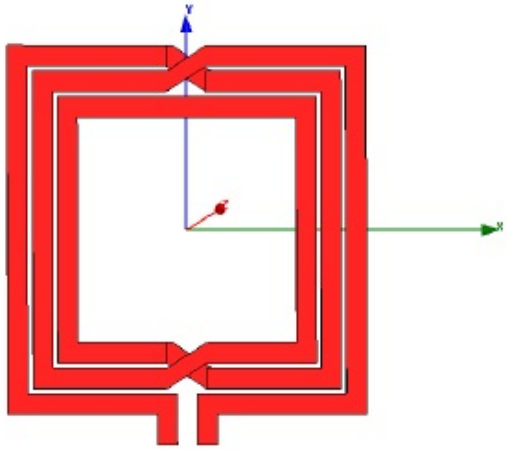


Figure 3.2: Standard planar differential inductor

are determined using Eqs.1.13, Eqs.1.14, Eqs.1.15, Eqs.1.16, Eqs.1.17, and Eqs.1.18, respectively.

The differential excitation of the inductor increases the parasitic resistance by twice ($2R_P$) and decreases the parasitic capacitance by half ($C_P/2$). This implies that the substrate losses of the inductor are reduced to a greater extent that improves the quality factor for the constant value of inductance. The variation in Q for both single-ended as well as differential excitation of the planar and proposed differential inductors is shown in Fig.3.3. The differential excitation has shown a 5% improvement in Q over single-ended excitation.

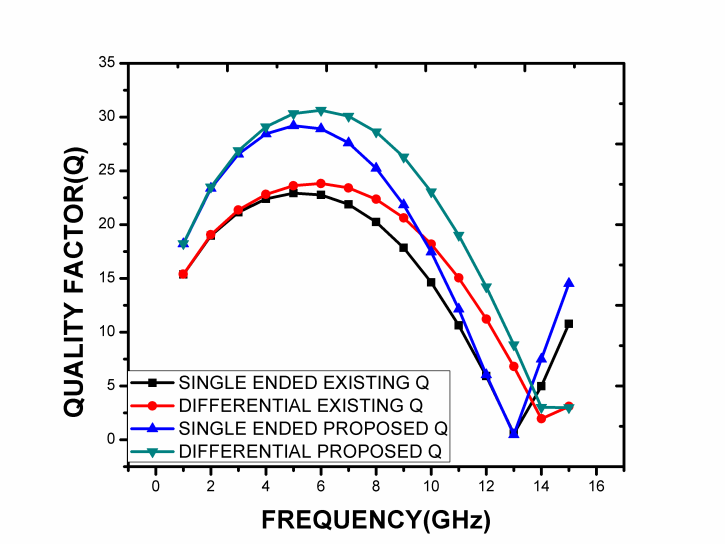


Figure 3.3: Comparison of Q for single-ended and differential excitation for the existing planar and proposed differential inductors

The comparison of quality factor and inductance is shown in Fig. 3.4 and Fig. 3.5, respectively. From Fig.3.4, it is evident that the Q is improved by 30% for the proposed differential inductor due to reduced substrate losses and eddy current losses compared to the standard differential inductor. From Fig.3.5, it is observed that the inductance of the proposed inductor has shown 35% improvement in inductance over planar standard differential inductor as the length of the conductor is made longer than the planar differential inductor. The comparison of simulation results for the proposed and standard differential inductors is shown in Table. 3.1.

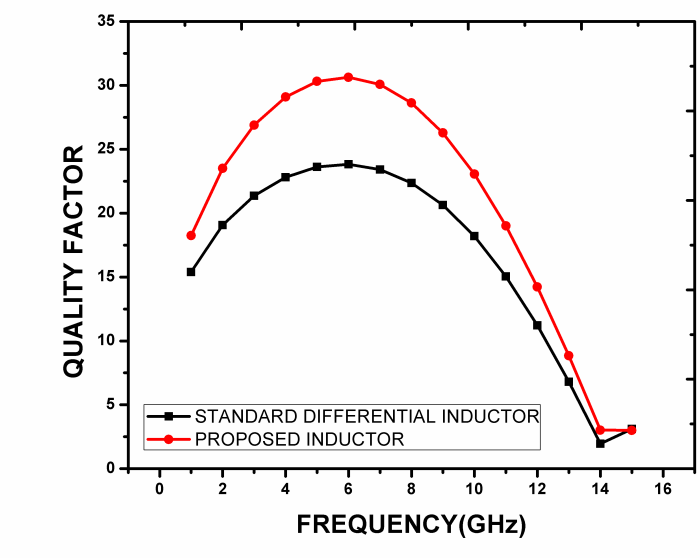


Figure 3.4: Comparison of Q for the planar and proposed differential inductors

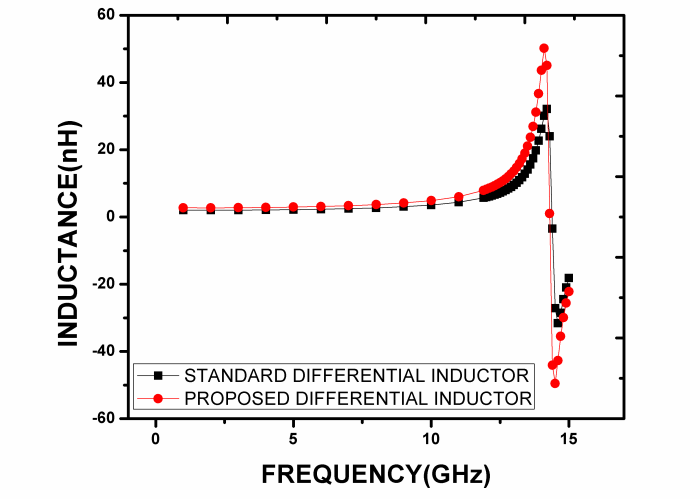


Figure 3.5: Comparison of inductance for the planar and proposed differential inductors

S.No	Type of inductor	d_{out} (μm)	w (μm)	n	Q	f_{SR} (GHz)	L (nH)
1.	Planar	180	10	3	23.53	14.6	2.2
2.	Proposed	180	10	3	30.86	14.4	3.1

Table 3.1: Comparison of simulated values for the proposed and planar differential inductors

3.3 Variable multipath width multilayer differential inductor

The skin and proximity effects are dominant at high frequencies which degrades the performance of the inductor. At high frequencies, the increase in magnetic field causes non-uniform current distribution in the conductor and makes the current flow near the skin of the conductor. This mechanism is known as the skin effect. The skin effect is dependent on the skin depth of the conductor (δ). The proximity effect is due to the penetration of magnetic fields from adjacent conductors. The skin and proximity effect together decreases the skin depth of the conductor and increases the series resistance (R_s).

The series resistance (R_s) of the inductor is expressed as a function of the skin depth (δ) of the conductor, and it is defined in Eq.3.1. The skin depth for a given frequency of operation can be found using Eq.3.2:

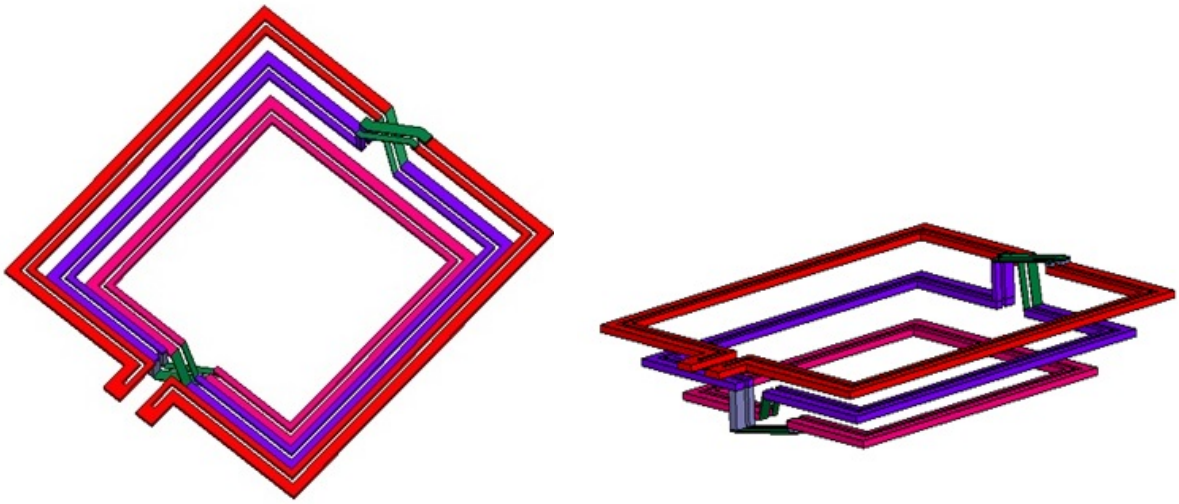
$$R_s = \frac{\rho l}{w\delta(1 - e^{\frac{-t}{\delta}})} \tag{3.1}$$

$$\delta = \sqrt{\frac{2\rho}{\omega\mu}} \tag{3.2}$$

In Eq.3.1 and Eq.3.2, ρ is known as the resistivity of the metal, l is the total length of the inductor, μ is known as the permeability of free space.

The multipath inductors [98] and variable width inductors [97] are proposed in the literature to suppress these losses. The proposed inductor utilizes both variable width and multipath techniques to enhance the performance of the inductor. The proposed variable multipath width multilayer differential inductor is shown in Fig. 3.6. The width of the conductor is partitioned into two multiple paths of unequal widths according to the skin depth of the inductor and it is

implemented in three layers. The inner path width is made less than the outer path width and greater than the skin depth to reduce the impact of the magnetic field in the inner turns.



(a) Top View (b) 3-D view

Figure 3.6: Proposed variable multipath width multilayer differential inductor

The multipath technique reduces the opposing eddy currents compared to single-path inductors and increases skin depth. Variation in multipath width in the proposed inductor has very few current crowding effects compared to equal width multipath inductor since adjacent paths have different opposing magnetic fields. The increase in skin depth reduces the series resistance and improves the Q.

In addition to variable width in multipath, the implementation of the proposed inductor in multilayers reduces the effective parasitic capacitance and substrate losses. This causes High Q and f_{SR} for the proposed inductor compared to the standard differential inductor and a planar multipath differential inductor for the equivalent on-chip area without affecting the inductance value.

3.3.1 Simulation results of the inductor

The proposed variable multipath width multilayer differential inductor as shown in Fig. 3.6 is implemented for three layers and these layers are interconnected using vias and crossovers with inner and outer diameters 180 μm and 90 μm, respectively. The spacing between the paths and the path width is decided based on the skin depth of the conductor. The skin depth for the

copper at 10 GHz is 0.7 μm which is calculated from equation (1). The pathwidth should be selected more than the skin depth of the conductor (copper). The overall width of the conductor is 10 μm and it is partitioned into two paths of different widths 5 μm and 3 μm, respectively.

The input impedance, quality factor, and inductance for the inductors are determined using Eqs.1.14, Eqs.1.16, and Eqs.1.17, respectively. From the simulation results as shown in Fig.3.7 the proposed inductor has 30% and 18% improvement in Q over planar and multipath differential inductors, respectively, as the proposed inductor has reduced current crowding effects and substate losses. The proposed inductor also has 50% and 15% improvement in Peak Q frequency (f_{Qmax}) over planar and multipath differential inductors, respectively due to reduced parasitic capacitance.

The simulation results for the self-resonance frequency and inductance are shown in Fig. 3.8. The proposed inductor has shown 50% and 25% improvement in self-resonance frequency over planar and multipath differential inductors, respectively, as it has less effective parasitic capacitance. The comparison of simulation results is shown in Table. 3.2 for the standard planar differential inductor, multipath differential inductor, and proposed inductor, respectively.

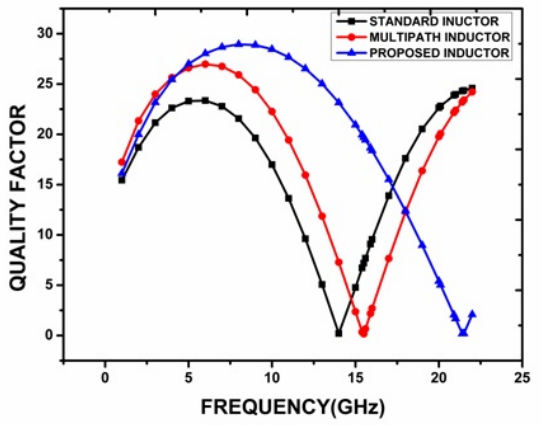


Figure 3.7: Comparison of Q

S.No	Type of inductor	Q	f_{SR} (GHz)	f_{Qmax} (GHz)	L (nH)
1.	Planar differential inductor [104]	23.2	14	5.5	2.3
2.	Planar multipath differential inductor [98]	26.8	15.5	6.4	2.4
3.	Proposed differential inductor	30.1	21.5	8.2	2.2

Table 3.2: Comparison of simulated values for the proposed and planar differential inductors

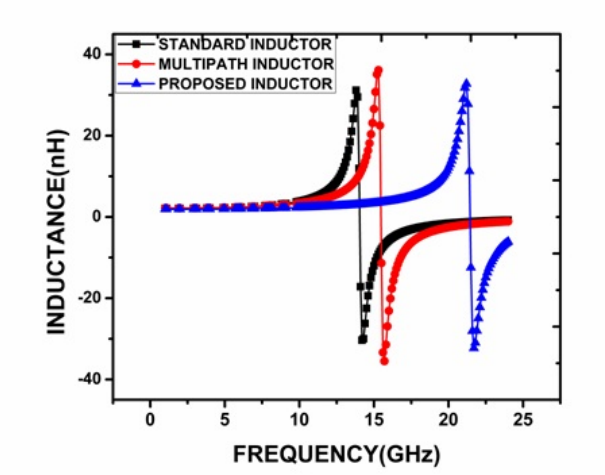


Figure 3.8: Comparison of self-resonance frequency

3.4 Series stacked non-parallel multipath differential inductor

In conventional series stacked multipath inductors the divided paths (segments) are in parallel with each other which forms the parasitic capacitance [103] and degrades the performance of the inductor. In the proposed inductors the segments have deviated from one another (not arranged in parallel) which decreases the parasitic capacitance and improves the Q and f_{SR} of the inductor to a significant extent. The proposed series stacked non-parallel multipath differential inductor is shown in Fig. 3.9. The top and bottom layers each consists of one differential inductor and these are connected in series using vias. As shown in Fig. 3.10a, the conductor width is 10 μm and it is partitioned into two segments with each segment has 2 μm width and spacing between the segments is 6 μm. The top layer consists of two segments denoted as S_1 and S_2 and the bottom layer consists of two segments denoted as S_3 and S_4 as shown in Fig. 3.10a. The segments in the top and bottom layers are not parallel to each other as shown in Fig. 3.10b.

The construction of non-parallel segments reduces the parasitic capacitance (reduces interlayer capacitance (C_s) and metal to the substrate (C_p)) and the multipath technique lowers the current crowding effects. Hence, the proposed inductor achieves high Q and f_{SR} for almost the same inductance value compared to the conventional series stacked multipath inductor.

3.4.1 Simulation results of the proposed inductor

The proposed inductor is designed for an outer diameter of 180 μm for 3 turns and simulated in HFSS using 0.18 μm CMOS technology. The differential impedance of the inductor is obtained by using Eq. 1.14. The simulated L and Q values for the proposed inductor are obtained by using Eq. 1.16 and Eq. 1.18.

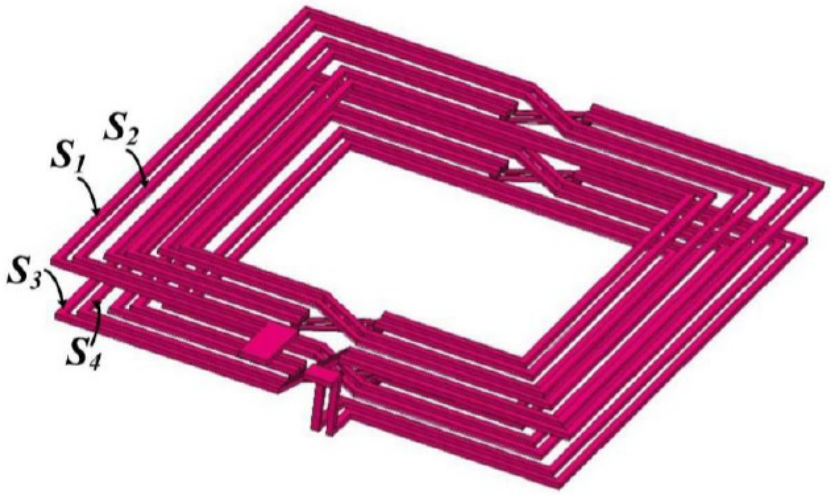
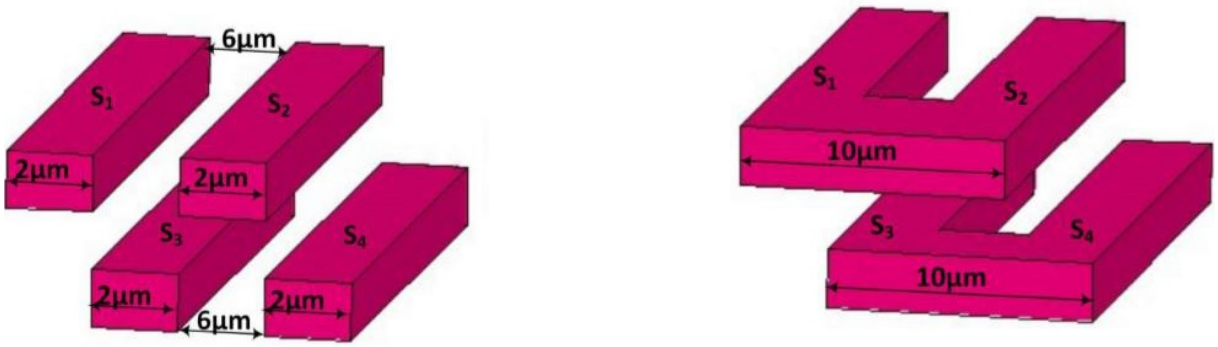
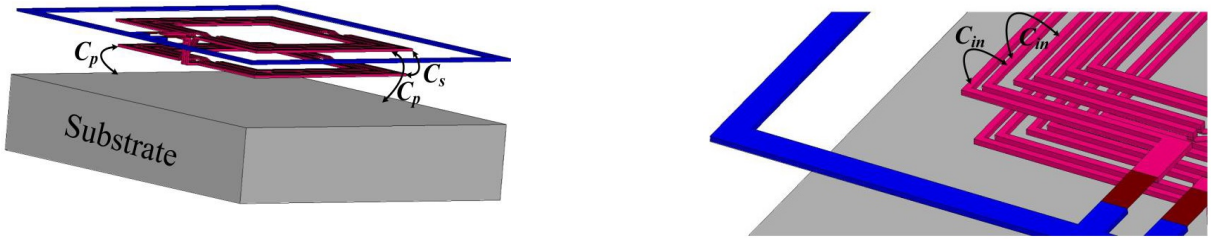


Figure 3.9: Proposed series stacked non parallel multipath differential inductor



(a) (b)

Figure 3.10: (a) Partition of conductor width (b) Non parallel metal layers



(a) (b)

Figure 3.11: (a) interlayer capacitance (C_s) and metal to substrate capacitance (C_p) (b) inter-winding capacitance (C_{in})

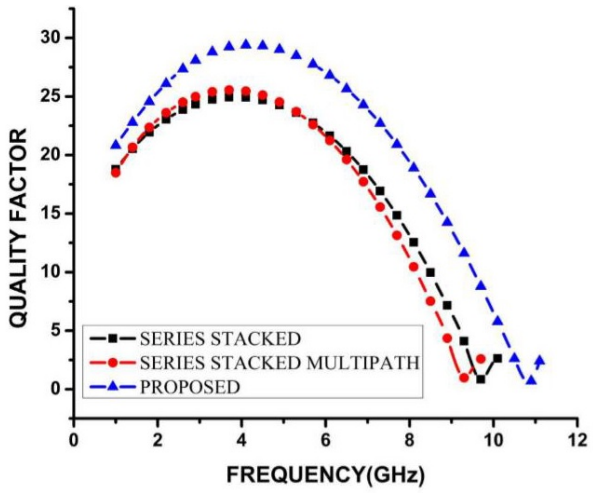


Figure 3.12: Comparison of Q

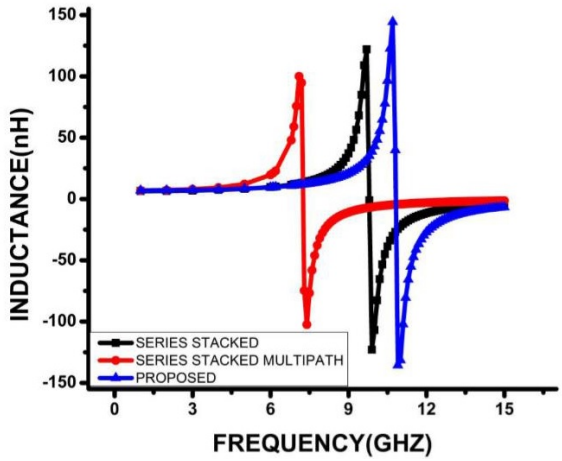


Figure 3.13: Comparison of inductance

The Q and inductance plots of the proposed inductor are shown in Fig. 3.12 and Fig. 3.13, respectively. From the results shown in Fig. 3.12, the proposed inductor with non-parallel segments achieves 25% improvement in f_{SR} for the same inductance value over conventional series stacked multipath inductor.

The interlayer capacitance between the adjacent layer decreases the Q and f_{SR} at higher frequencies. However, at higher frequencies, narrower metal width can have even higher Q because of the reduction in eddy-current losses in the metal and substrate due to smaller areas. The Q decrease from the peak Q frequency (f_{Qmax}) and reaches zero since the substrate parasitics and current crowding effects are very high.

From 3.13, it is noted that the Q of the proposed inductor is 33% greater than the conventional series stacked multipath inductor. The peak Q frequency (f_{Qmax}) is 4.7 GHz and f_{SR} is 11.5 GHz, are within the C-band. As the proposed inductor covers the entire C band (4-8 GHz), it is suitable for applications that include satellite communications, Wi-Fi, cordless phones, and surveillance and radar systems.

The simulation results for series stacked multipath inductor, conventional series stacked inductor, and the proposed inductor for an outer diameter of 180 μm are tabulated in Table 3.3.

S.No	Type of inductor	Q	f_{SR} (GHz)	f_{Qmax} (GHz)	L (nH)
1.	Conventional series stacked inductor [100]	22.52	9	3.6	7.09
2.	Series stacked multipath inductor [104]	25.07	9.2	4.1	7.8
3.	Proposed inductor	29.87	11.5	4.7	7.9

Table 3.3: Comparison of simulated values for the proposed and planar differential inductors

3.5 Summary

Multilayer differential inductors using variable width and multipath techniques are proposed in this chapter. The proposed inductors have obtained better performance in terms of the quality factor, inductance, and self-resonance frequency compared to conventional single layer and multilayer differential inductors. The proposed inductors are suitable for the CMOS fabrication process due to their square shape. The advantage of the proposed structure is that both ports are at the top metal layer, which makes them useful for differential input applications such as VCO and LNA, and it is also well suited for connecting active components.

Chapter 4

Hybrid series stacked differential fractal inductor

4.1 Introduction

On-chip inductors are the key circuit elements in monolithic microwave integrated circuits (MMICs) for the implementation of low noise amplifiers (LNA), voltage-controlled oscillators (VCO), filters, and single-chip transceivers. The conventional planar spiral inductors proposed in the literature are subjected to current crowding effects and substrate losses at high frequencies. The lack of a good inductor can be treated as a major barrier for better MMIC development. Fractal is a mathematical abstraction. Some fractal patterns have a finite area but an infinite perimeter [42], which makes it a good choice to build a novel structure of inductor in a limited area on MMIC chip. For obtaining high inductance values, the length of the conductor should be maintained high that increases the required on-chip area. Inductors making use of fractal geometry acts as the precise technique to resolve this problem. An exhaustive study of fractal inductors was carried out in the literature [18, 51, 112, 113, 121].

Series stacked fractal inductor improves the inductance value due to mutual coupling between the adjacent metal layers [118]. However, it suffers a low f_{SR} and low Q due to large parasitic capacitance formed between the adjacent metal layers. This chapter deals with the design and implementation of a novel series stacked fractal inductor with differential excitation using two different fractal curves. The overview of Hilbert and Sierpinski curves are discussed

in section 4.2. The design, analysis, and fabrication of a novel hybrid series stacked differential fractal inductor explained in section 4.3. The conclusions are given in section 4.4.

4.2 Hilbert and Sierpinski curves

A curve that bends and curls at every level of magnification is called a fractal curve. Different fractal curves were used to design fractal inductor which includes Hilbert, Sierpinski, Moore, Peano, and Luxburg [18]. The proposed inductor is designed by using Hilbert and Sierpinski curves. Hilbert curves were first described by David Hilbert in 1892. These are built through an iterative procedure that generates self-similar structures and space-filling curves. The construction and order of the Hilbert curves are shown in Fig. 4.1. Similarly, the Sierpinski curve, named after the Polish mathematician Waclaw Sierpinski demonstrates a more symmetrical structure than any other commonly used space-filling curves [122]. The Sierpinski curve is a form of mutual recursion resulting in a closed-loop when compared to the Hilbert space-filling curve. The identical length of the curves aids in the optimal utilization of the on-chip area. The construction and order of the Sierpinski curves are shown in Fig. 4.2. For a fractal curve the side length of each segment is defined as 'L', iteration order (IO) as 'n', and shortest segment length in each iteration as 'd_o' which are shown in Fig. 4.1 and Fig. 4.2. The d_o for each iteration is determined using Eq. 4.1: The overall conductor length is denoted as 'S' increases and it increases with increase in iteration order and it is given in Eq.4.2

$$d_0 = \frac{L}{2^n - 1} \tag{4.1}$$

$$S = (2^n + 1)L \tag{4.2}$$

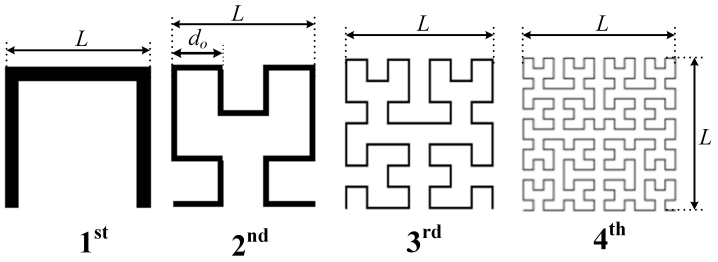


Figure 4.1: Order of the Hilbert curves

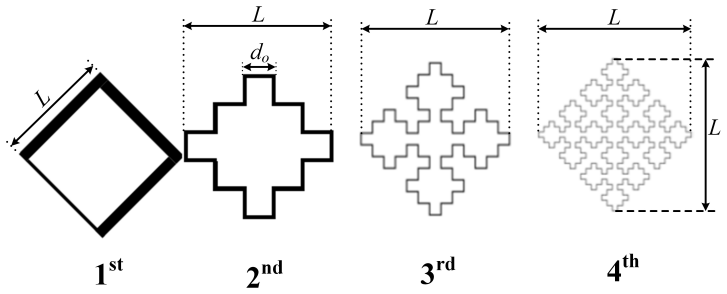


Figure 4.2: Order of the Sierpinski curves

The segment length (L) is equal to the outer diameter (OD) of the inductor which is directly proportional to the on-chip area. The overall conductor length for the two curves Hilbert and Sierpinski is almost the same in each iteration order for constant segment length (Lazarus et al., 2014; Wang et al., 2012) which is shown in Table 4.1. Therefore, these two curves are used to design the inductor.

Curve	1^{st} **order**	2^{nd} **order**	3^{rd} **order**	4^{th} **order**
Hilbert curve	$3L$	$5L$	$9L$	$17L$
Sierpinski Curve	$4L$	$5.66L$	$9.14L$	$16.30L$

Table 4.1: Illustration of length of the curve

4.3 Hybrid series stacked differential fractal inductor

In conventional series stacked fractal inductor [118] the top and bottom layers have the same fractal curves. The series stacked fractal inductor using Sierpinski and Hilbert curves are shown in Fig. 4.3 and Fig. 4.4, respectively. In contrast to this, the proposed hybrid series stacked differential fractal inductor as shown in Fig. 4.5 has the top layer built with Sierpinski curve and the bottom layer built with a Hilbert curve that is connected in series using vias. The proposed inductor attains high inductance due to a decrease in negative mutual inductance between the adjacent metal layers compared to the conventional series stacked fractal inductor. It also attains high Q and f_{SR} as it has fewer parasitics between the adjacent metal layers when compared to conventional series stacked fractal inductor.

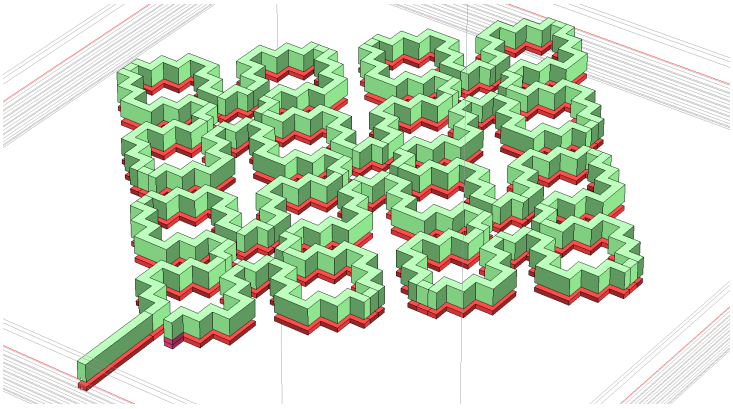


Figure 4.3: Series stacked fractal inductor using Sierpinski curve

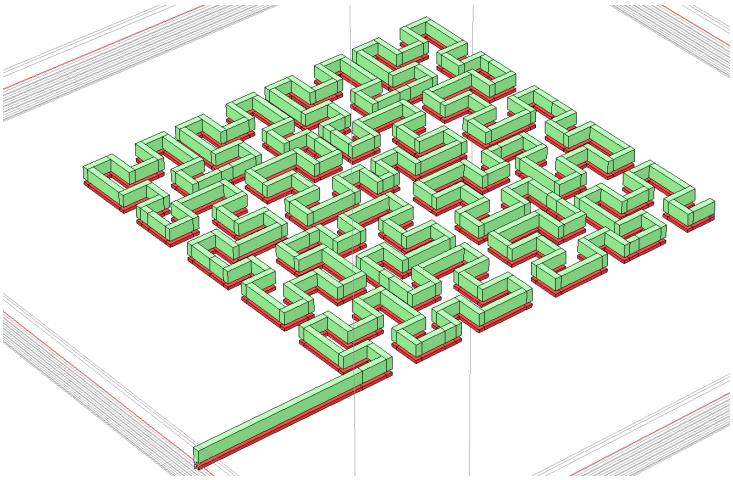


Figure 4.4: Series stacked fractal inductor using Hilbert curve

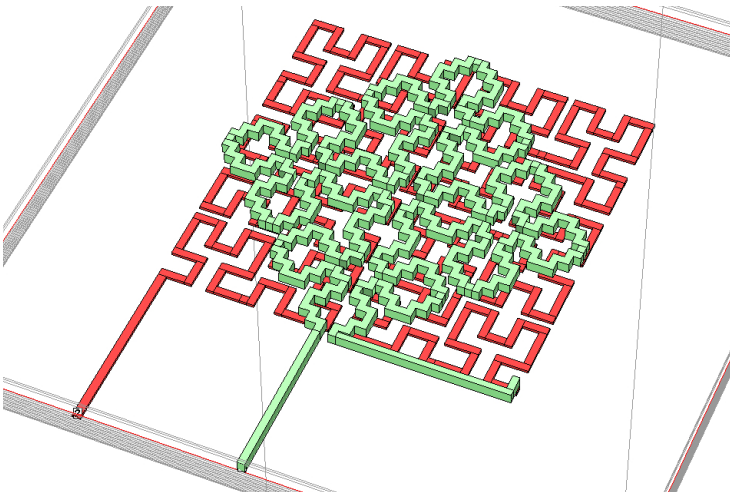


Figure 4.5: Proposed hybrid series stacked differential fractal inductor

4.3.1 Design and simulation of hybrid series stacked differential fractal inductor

The proposed inductor is implemented with an outer diameter (d_{out}) of 200 μm and the width of the conductor is 2 μm. The segment length and outer diameter both are equal for the proposed inductor. The Segment length (L) is considered as an indentation factor (IF). The proposed inductor is designed and simulated in Sonnet EM simulator using 180 nm standard CMOS process technology. The technology parameters and metal stacking for 180 nm CMOS process are shown in Fig. 4.6. The fabrication of the proposed inductor is compatible with TSMC 180 nm CMOS process.

The proposed inductor is excited differentially and the differential impedance of the proposed inductor is obtained by using Eq. 1.14. The simulated inductance, quality factor, and series resistance value for the proposed inductor are obtained by using Eq. 1.16, Eq. 1.18 and Eq. 1.20:

The segment length (L) is constant for all the iterations and can be considered as indentation factor (IF) and the shortest segment length (d_o) is variable for each iteration and considered as indentation depth (ID). The inductance, Q factor, dielectric constant, iteration order (IO), indentation factor, indentation depth, operating frequency, and self-resonance frequencies are tabulated in Table 4.2. Fig. 4.7 and Fig. 4.8 shows the implementation of the proposed inductor in 2^{nd} and 3^{rd} iteration orders. From Table 4.2, in all the three iterations, high inductance value is obtained using 4^{th} order fractal curves for the proposed inductor at the expense of moderate Q and f_{SR}. Hence, to achieve high inductance (L_{in}) the proposed inductor is designed based on 4^{th} order fractal curve.

IO	**IF(L)**	**ID (d_o)**	**Die.const**	**L_{in}(nH)**	**Q**	f_{SR}	f_{Qmax}	**Oper.Freq**
2^{nd}	200 μm	66 μm	4.2	1.5	20	32 GHz	16 GHz	1 GHz - 32 GHz
3^{rd}	200 μm	28 μm	4.2	2.8	18	28 GHz	14 GHz	1 GHz -28 GHz
4^{th}	200 μm	13 μm	4.2	3.9	16.34	22 GHz	11 GHz	1 GHz -22 GHz

Table 4.2: Performance metrics for proposed inductor with different iteration orders

The proposed inductor is implemented in the top two metal layers (metal 6 and metal 5) having a thickness of 3 μm and 0.75 μm to obtain high Q values as the thick metal layers have low ohmic losses. However, the advantage of obtaining high Q due to thick metal layers is limited to low frequencies as the current crowding effects and skin effects are severe at high frequencies.

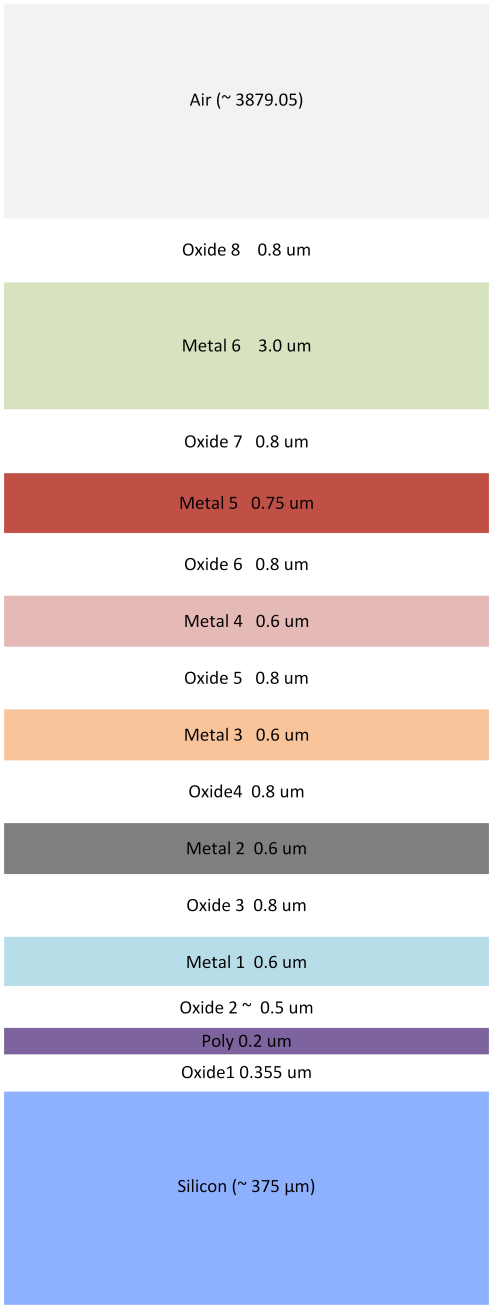


Figure 4.6: Technology parameters and metal stack for 180 nm process

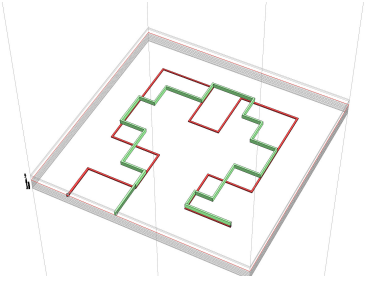


Figure 4.7: 2^{nd} IO (IF=200 μm, ID=66 μm).

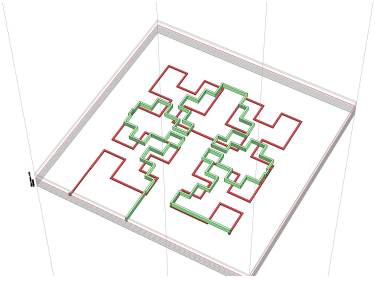


Figure 4.8: 3^{rd} IO (IF=200 μm, ID=28 μm).

The inductance plot for the proposed inductor is shown in Fig. 4.9 and the same is compared with other series stacked inductors. From Fig. 4.9, it is found that the proposed inductor has high inductance as compared to the series stacked Hilbert fractal inductor [118], series stacked Sierpinski fractal inductor [122] and series stacked spiral inductor [100]. In conventional series stacking the opposite currents in adjacent metal layers increase negative mutual inductance which leads to a reduction in total inductance value. When N inductors are connected in series, the total inductance (L_T) is the sum of self-inductance (L_i) and mutual inductances (M_{ij}) between the metal traces (adjacent or parallel), which is shown in Eq. 4.3. If the current directions in two metal traces are in same direction the mutual inductance ($\sum_{i=1}^{N}\sum_{j\neq i}^{N} M_{ij}$) is positive otherwise it is negative [123].

$$L_T = \sum_{i=1}^{N} L_i \pm \sum_{i=1}^{N}\sum_{j\neq i}^{N} M_{ij} \tag{4.3}$$

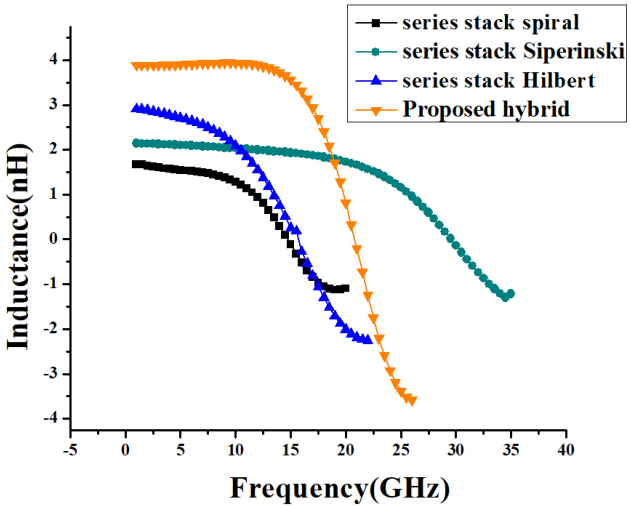


Figure 4.9: Comparison of inductance

In a proposed hybrid inductor, the opposite currents are reduced as the construction of the two curves are different from one another resulting in reduced negative mutual inductance and increased total inductance. The proposed inductor has shown 35%, 85%, and 200% improvement in inductance value over series stacked Hilbert fractal inductor, series stacked Sierpinski fractal inductor and series stacked spiral inductor, respectively.

The Quality factor plots for all the designed inductors are shown in Fig. 4.10. From Fig. 4.10, it is found that the proposed inductor has high Q compared to the series stacked Hilbert fractal inductor [118], series stacked Sierpinski fractal inductor [122] and series stacked spiral

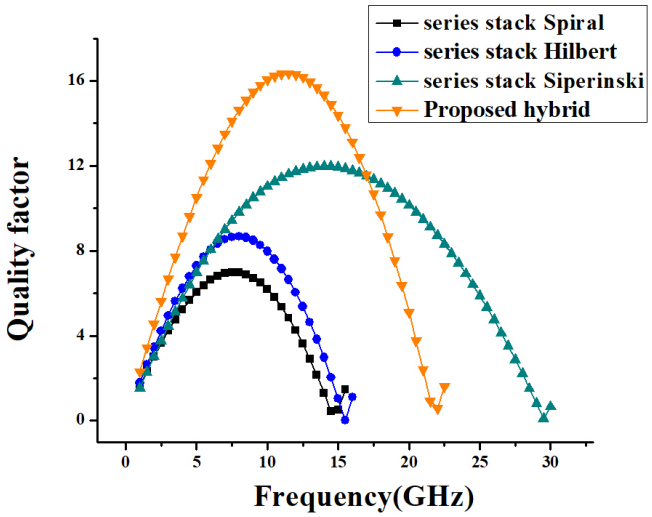


Figure 4.10: Comparison of Q

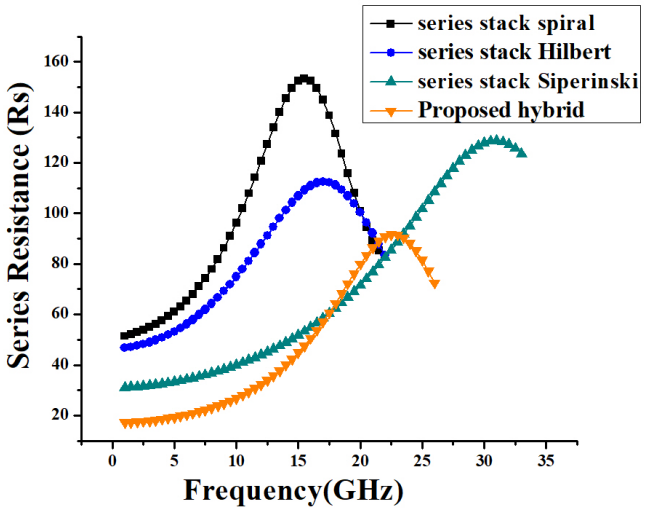


Figure 4.11: Comparison of series resistance

inductor [100]. In conventional series stacking, the adjacent metal layers form huge parasitic capacitance which reduces Q value. In a proposed hybrid inductor, the two different curves reduce the parasitic capacitance on the four corners of the inductor thus improving the value of Q. The proposed inductor has shown 50%, 58%, and 95% improvement in Q over series stacked Sierpinski fractal inductor, series stacked Hilbert fractal inductor, and series stacked spiral inductor, respectively. The series resistance (R_s) plot for all the inductors is shown in Fig. 4.11. The simulated series resistance (R_s) values at high Q for the proposed hybrid inductor, series stacked Hilbert fractal inductor, series stacked Sierpinski fractal inductor, and series stacked spiral inductor are 30 Ω, 84 Ω, 42 Ω and 114 Ω, respectively. The proposed inductor has a low series resistance value compared to conventional series stacked inductors.

At the high frequency of operation, the performance of the proposed inductor is degraded owing to skin effect, and current crowding effect. In the proposed inductor as the operating frequency increases beyond peak Q frequency (f_{Qmax}) of 11 GHz, the skin effect grows slowly and increases the series resistance (R_s) [26, 124]. The increase in series resistance decreases the Q. In addition to the skin effect, the inductor experiences the current crowding effects (proximity effect) generated from mutually induced eddy currents resulting in the non-uniform current distribution in the adjacent metal traces. As frequency increases beyond f_{Qmax} the current crowding effects are more dominant than skin effects. The increase in current crowding effects results in an exponential increase of the series resistance, which leads to a decrease in Q and L [125].

The series stacked Hilbert fractal inductor has higher inductance compared to series stacked Sierpinski fractal inductor as shown in Fig. 4.9 as the length of the Hilbert curve is higher than the Sierpinski curve in 4^{th} order as depicted in Table 4.1. The Q and f_{SR} of the series stacked Sierpinski fractal inductor is higher than series stacked Hilbert fractal inductor due to reduced parasitics as shown in Fig. 4.10. The hybrid fractal inductor combines the properties of both Hilbert curve and Sierpinski curve based series stacked inductors and yields a high Q, L, and moderate f_{SR} for the equivalent on-chip area.

The proposed hybrid series stacked fractal inductor reduces the interlayer parasitic capacitance. This capacitance is responsible for Q deterioration at higher operating frequencies. However, in the proposed inductor, the decrease in interlayer capacitance is also responsible for low negative mutual inductance and minimal substrate losses. Thus, higher Q and L values are obtained in comparison with conventional series stacked fractal inductors. However, from the peak Q frequency (f_{Qmax}) of operation, the current crowding effects and substrate parasitics are more dominant which are responsible for the decrease in Q.

The simulated L, Q, R_s, peak Q frequency (f_{Qmax}) and f_{SR} for the proposed inductor is tabulated in Table 4.3 and the same is compared with other competing inductor structures in literature. For the equivalent on-chip area the proposed inductor attains high Q, L, and moderate f_{SR} which is shown in Table 4.3. The proposed inductor offers high performance for MMIC frequency bands that range from 4 GHz to 15 GHz (C, X, Ku band) and 12 GHz to 20 GHz (Ku, K band). An MMIC contains active, passive, and interconnect components and is designed to operate at frequencies from hundreds of MHz to hundreds of GHz. Hence, the proposed inductor is well suited for MMIC applications.

Ref.	L(nH)	Q	OD (μm)	$R_s(\Omega)$	f_{SR}	f_{Qmax}
[100]	1.6	7.1	200	114	15 GHz	7.5 GHz
[126]	3.12	5	240	143	14 GHz	8 GHz
[116]	0.9	8.67	200	100	10 GHz	5 GHz
[103]	3.2	6.07	240	120	8 GHz	2.7 GHz
[115]	3.5	9.2	450	78	2 GHz	1 GHz
[127]	0.5	15	200	60	15 GHz	12 GHz
[118]	2.87	7.25	200	84	17 GHz	8 GHz
[122]	2.1	11.84	200	50	24 GHz	12 GHz
Proposed hybrid Inductor	**3.98**	**16.34**	**200**	**30**	**22 GHz**	**11 GHz**

Table 4.3: Performance comparison of the proposed inductor with existing state-of-the-art

4.3.2 Fabrication and Measurement results

Due to the unavailability of fabrication on the Silicon substrate, the proposed inductor is scaled down to lower frequencies and fabricated on the multilayer Printed Circuit Board (PCB) using FR-4 substrate with an area of 40 mm $\times$ 40 mm. The thickness of copper in the top layer is 0.6 mm and the bottom layer is 0.4 mm. The overall thickness of PCB is 1.60 mm and the spacing between the top and bottom layers is 0.197 mm. Fig. 4.12 and Fig. 4.13 shows the fabrication of the proposed inductor top and bottom views, respectively. Fig. 4.14 shows the experimentation of the fabricated inductor using Vector Network Analyzer (VNA-N9923A). The proposed inductor is validated experimentally using VNA of the frequency range from 0.01GHz to 1GHz. Owing to variation in technology from micrometer to mm scale the operating frequency is diminished to MHz from GHz. Consequently, the simulation results of the proposed inductor in mm scale are compared with the measurement results. From Fig. 4.15, it is evident that the simulated and measured inductances are really in better competition with each other, having the inductance value approximately equal to 202 nH. Furthermore, Fig. 4.16 displays that the simulated and measured quality factors are in good agreement with one another, with a peak Q equal to 42 at 152 MHz. The comparison of measured and simulated results is given in Table 4.4. The close alliance of the simulated and measured results recommends that the proposed inductor is considered to be a good candidate as an on-chip inductor in the CMOS process.

Parameter	Simulated results	Measured results
Inducatnce (nH)	202	195
Quality factor	42	40
Self-resonance frequency (MHz)	225	220

Table 4.4: Simulated results vs Measured results

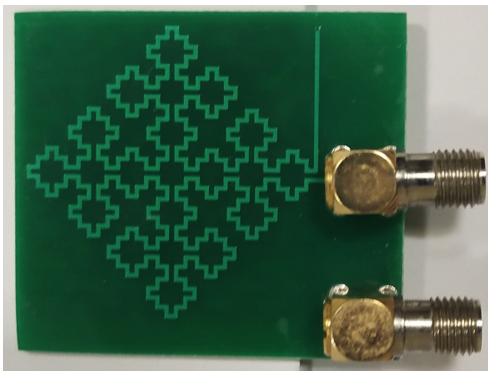


Figure 4.12: Fabricated inductor top view

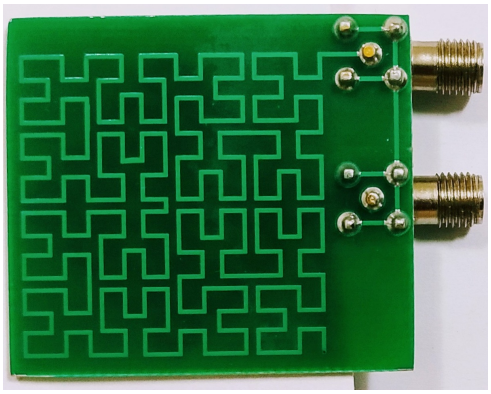


Figure 4.13: Fabricated inductor bottom view

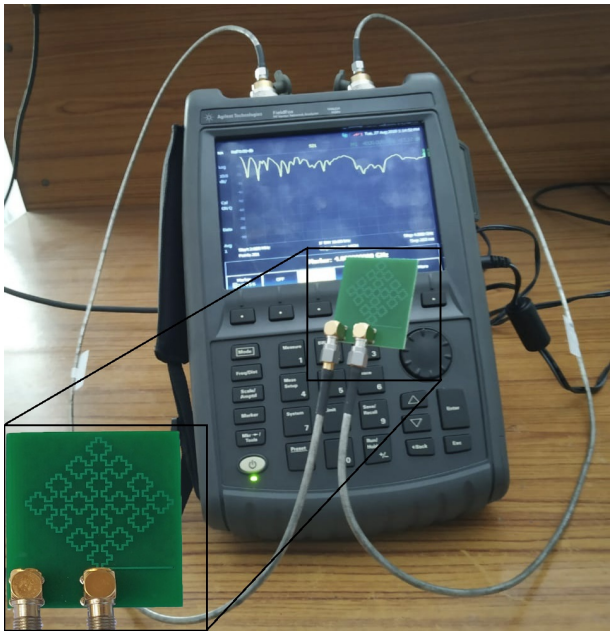


Figure 4.14: Measurement of results using network analyzer

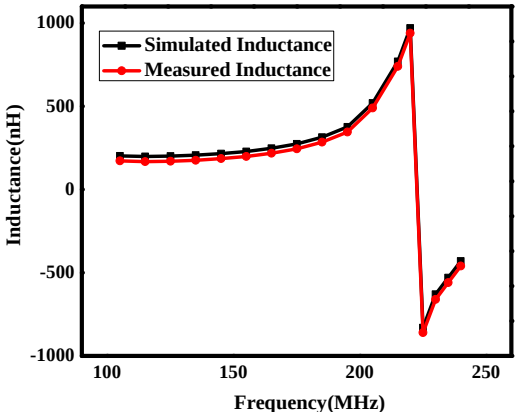


Figure 4.15: Simulated and measured L (nH)

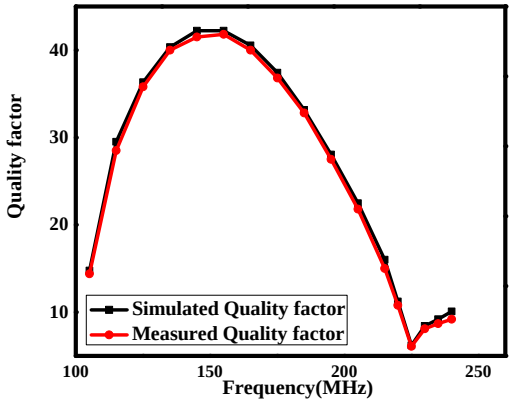


Figure 4.16: Simulated and measured Q

4.4 Summary

This chapter has presented the design, fabrication, and analysis of a novel hybrid series stacked differential fractal inductor using Hilbert and Sierpinski curves. The proposed inductor combines the properties of both the curves and yields good performance. The proposed inductor has a significant improvement in inductance, quality factor, and f_{SR} over conventional series stacked fractal inductors for the equivalent Outer diameter. The f_{SR} and f_{Qmax} of the proposed inductor are 22 GHz and 11 GHz, respectively which are in the MMIC band. The proposed hybrid inductor is fabricated on a multilayer PCB and the measurement results are in good concurrence with the simulated results demonstrating the robustness of the design. Therefore, the proposed inductor is found to be apt for usage as an on-chip inductor in the CMOS process. As the fabrication methods of the proposed hybrid inductor are well suited to the modern-day CMOS process, thus it's promising to be included in MMIC applications possibly in the near future.

Chapter 5

Multilayer stacked differential fractal inductors and its application in LNA

5.1 Introduction

Spiral inductors play a crucial role in the design of radio frequency integrated circuits (RFICs) and they typically consume a considerably large on-chip area. The employment of fractal structure in the implementation of on-chip inductors helps in improving the inductance for the miniaturized on-chip area. The LNA is an important building block of wireless communication systems. It is used to amplify the received signal to acceptable levels with minimum self-generated additional noise. The conventional series stacked fractal inductor improves the inductance and self-resonance frequency (f_{SR}) and reduces the quality factor owing to parasitic capacitance between the adjacent metal layers. The conventional parallel stacked inductors attains high Q at the cost of low inductance and f_{SR} values. This chapter aims to improve the performance of both series and parallel stacked inductors using orthogonal arrangement (90 degrees orientation) of metal layers.

LNA is the most important building block in the wireless receiver [128]. The purpose of the LNA is to amplify the input signal received from the antenna to an appropriate level with a minimum signal-to-noise ratio [129]. As the development of 5G wireless networks continues, the performance of the front end radio is an increasingly critical element in the RF receiver signal path, particularly concerning LNA. Millimeter-wave (mm-Wave) frequency bands for 5G mobile services include 26 GHz band (24.25–27.5 GHz) and 28 GHz band [130]. The

signal linearity, gain, input-output matching, stability, power consumption, and noise figure are key performance metrics of the LNA [131, 132].

This chapter deals with the design, analysis, and fabrication of orthogonal series and parallel stacked fractal inductors using differential excitation. In addition to this, the proposed OSSDFI is used in the implementation of narrowband LNA. Section.5.2 explains the design, simulation, and fabrication of Orthogonal series stacked differential fractal inductor (OSSDFI). Section.5.3 illustrates the design and simulation of narrow-band LNA using proposed OSSDFI for 27-30 GHz frequency range and also compared the performance of the LNA with state-of-the-art LNAs. Section.5.4 explains the design, simulation, and fabrication of Orthogonal parallel stacked differential fractal inductor (OPSDFI).

5.2 Orthogonal series stacked differential fractal inductor (OSSDFI)

The proposed orthogonal series stacked differential fractal inductor (OSSDFI) is implemented in three layers based on 3^{rd} order Hilbert space-filling curves as shown in Fig. 5.1. The 1^{st}, 2^{nd} and 3^{rd} order Hilbert curves are depicted in Fig. 4.3. The phase difference of the top layer with intermediate and bottom layers is 90° and 180°, respectively. The layers in the inductor are connected in a series stack using vias. In contrast, with conventional series stacked fractal inductor (CSSFI), the current directions in adjacent layers are not opposite for the proposed OSSDFI resulting in the reduction of the negative mutual inductance and a significant increase in total inductance value. The f_{SR} of the proposed inductor is reduced as the increase in inductance is more dominant than the decrease in the parasitic capacitance.

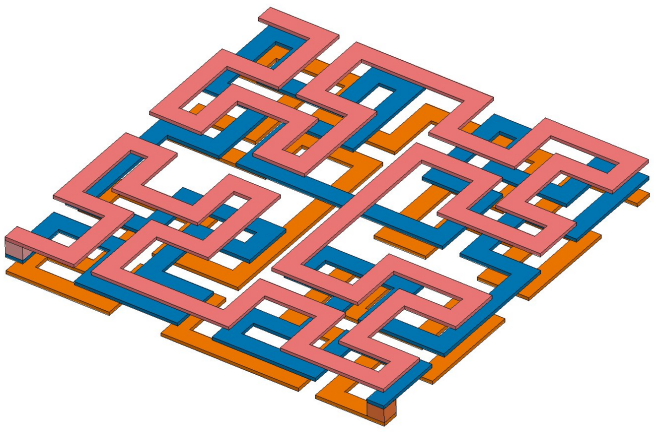


Figure 5.1: Proposed orthogonal series stacked differential fractal inductor

5.2.1 Simulation results of the proposed OSSDFI

The proposed inductor is designed and simulated using ADS (Advanced Design System) in 90 nm CMOS technology with an outer diameter of 200 μm and the width of the conductor is 10 μm. The on-chip area is directly proportional to the outer diameter. The input impedance (Z_{diff}), quality factor, total inductance and series resistance for differential excitation are evaluated using Eq. (1.14), Eq. (1.16), Eq. (1.18), and Eq. (1.20), respectively.

Fig. 5.2 and Fig. 5.3 show the inductance and quality factor plots for series stacked spiral inductor, CSSFI, and OSSDFI. The proposed OSSDFI has high inductance and high Q compared to the series stacked spiral inductor and CSSFI. The simulation results demonstrate that the OSSDFI shows twice the rise in inductance and 56% improvement in Q when compared to CSSFI.

The OSSDFI minimizes parasitic capacitance and negative mutual inductance between metal layers, resulting in an increase in Q and f_{SR} at higher frequencies. The impact of current crowding effects at higher frequencies is compensated by the decrease in parasitic capacitance. However, from the peak Q frequency (f_{Qmax}) of operation, the current crowding effects and substrate parasitics are more dominant which are responsible for the decrease in Q.

The performance summary of the proposed inductor and its comparison with existing inductors is demonstrated in Table 5.1. The self-resonance frequency of the proposed inductor is 40 GHz, which makes it suitable for the 5G applications as the service providers use 24.25-27.5 GHz band and 28 GHz band.

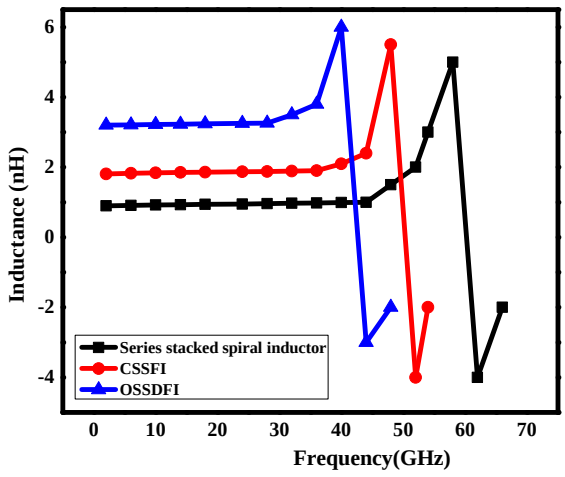


Figure 5.2: Comparison of inductance

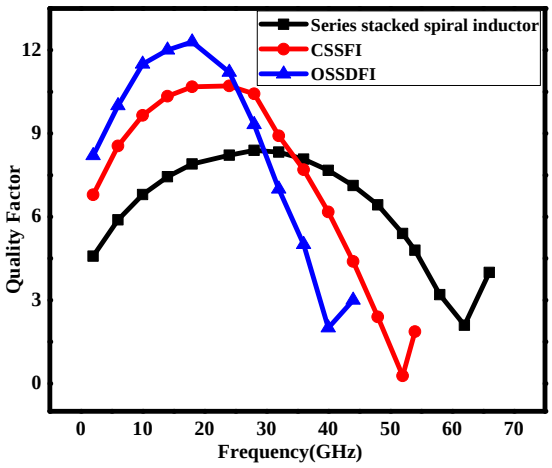


Figure 5.3: Comparison of quality factor

Parameter	[116]	[118]	[127]	[100]	OSSDFI
Inducatnce (nH)	0.9	2.45	0.5	1.61	**3.23**
Quality factor	8.67	7.25	15	7.63	**12.3**
Outer diameter (μm)	200	200	400	200	**200**
Series resistance (Ω)	250	180	160	150	**100**

Table 5.1: Performance comparison of the proposed inductor with existing state-of-the-art

5.2.2 Measurement results of the fabricated OSSDFI

The proposed inductor is fabricated on a multilayer printed circuit board (PCB) using FR4 material with a dielectric constant of 4.4. and area of 10 $\times$10 mm^2. The thickness of copper and the overall thickness of PCB are 0.035 mm and 1.60 mm with a spacing of 0.197 mm between metal layers. The fabricated inductor is shown in Fig. 5.4 and the experimental setup is shown in Fig. 5.5.

Due to technology scaling from micrometers to millimeters the frequency of operation is reduced from GHz to MHz. Therefore, the proposed inductor is simulated in the mm scale and the overall examination of measurement results is done by using a vector network analyzer. The comparison of simulated and measured inductances is illustrated in Fig. 5.6. It is vivid from the plots that the measured inductances are in good concurrence with simulated ones with inductance value equal to 225 nH. Similarly, Fig. 5.7 shows the comparison of simulated and measured results of the Q with the maximum quality factor approximately equal to 38 at 60 MHz. The pre-and post-measurement results for OSSDFI implemented on multilayer PCB are

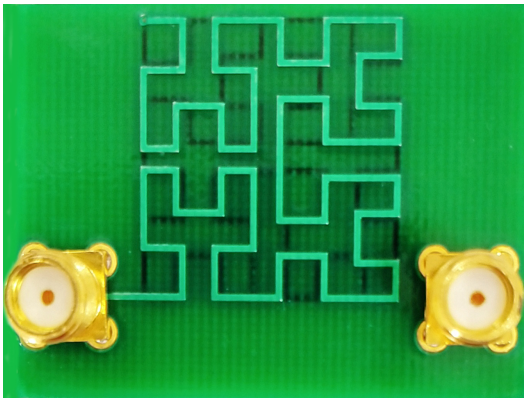


Figure 5.4: OSSDFI fabricated on Multi-layer PCB

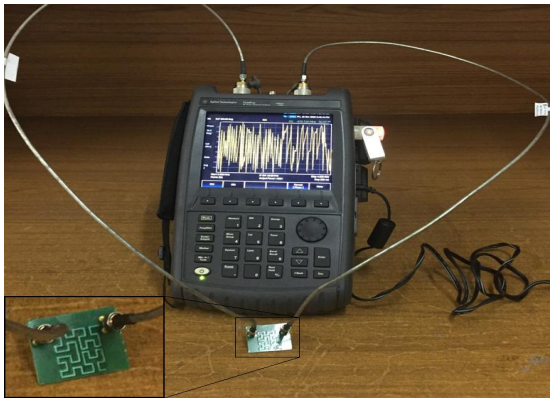


Figure 5.5: Experimentation using Network Analyzer

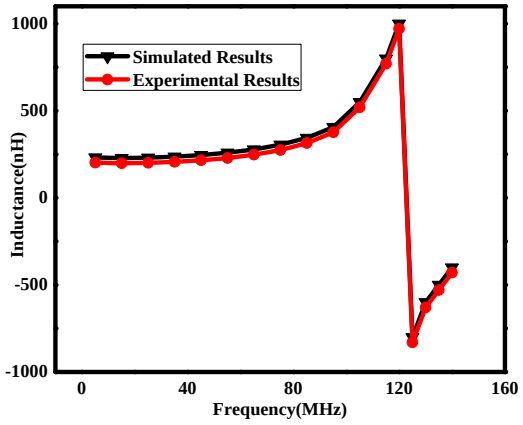


Figure 5.6: Simulated and measured inductance

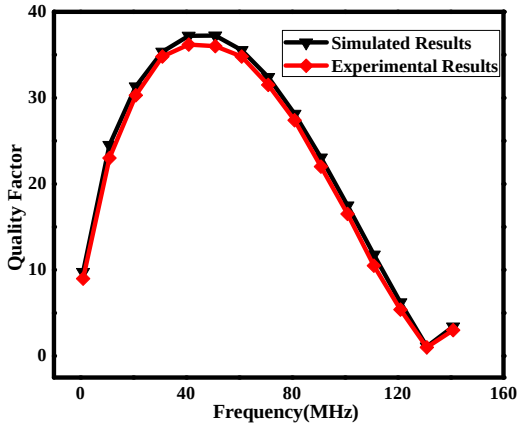


Figure 5.7: Simulated and measured Q

tabulated in Table 5.2. From Table 5.2, it is observed that the measured results are in good agreement with the simulated results. Therefore, the proposed inductor is observed to be well-suited for utilization as an on-chip inductor in the CMOS process.

Parameter	**Simulated results**	**Measured results**
Inducatnce (nH)	230	225
Quality factor	38	36
Self-resonance frequency (MHz)	125	124

Table 5.2: Simulated results vs Measured results

5.3 Design and simulation of the LNA

The cascode LNA with inductive source degeneration is the best topology used to obtain a high gain, low NF, and good input-output matching [133, 134] is shown in Fig. 5.8. The first stage of the LNA consists of the bandpass filter to tune the LNA for the required frequency of operation. The second stage is the cascode stage where the transistor M_1 is in common source mode and transistor M_2 is in common gate mode. Cascode architecture is used to increase forward gain while decreasing the reverse gain besides providing better isolation between input and output ports. The source inductor (L_s) provides negative feedback and stabilizes the gain. The gate inductor (L_g) provides input matching and a large value of gate inductance reduces the NF [30]. The drain inductance (L) is used to control the gain of the LNA. The third stage is the buffer stage used to provide better output matching at the output of the LNA [134]. The design specifications for the LNA are given in Table 5.3.

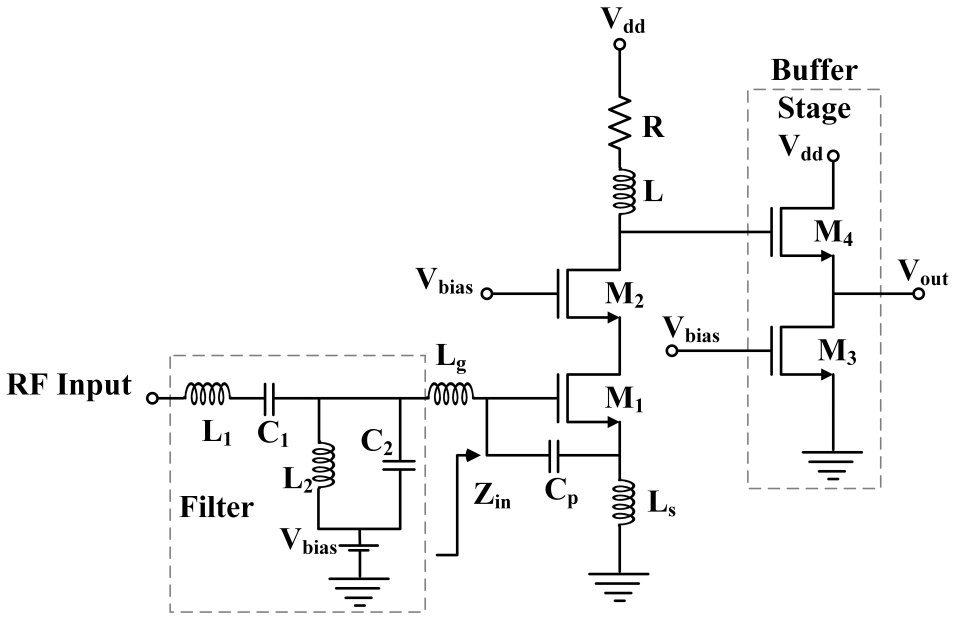


Figure 5.8: Cascode LNA with inductive source degeneration

5.3.1 Design of bandpass filter

The constant-k LC bandpass filter is used to tune the LNA for the required frequency of operation is shown in Fig. 5.9. The inductances L_1, L_2 are obtained by using (5.1) and (5.2) and the capacitances C_1, C_2 are obtained by using (5.3) and (5.4). In this design, upper cut-off frequency (f_2) is equal to 30 GHz and lower cut-off frequency (f_1) is equal to 27 GHz, where Z_0 is the characteristic impedance.

Parameter	Range
Operating frequency	27-30 GHz
Center frequency (f_o)	28 GHz
Noise figure	< 3 dB
Gain	33 dB
Input matching	< -10 dB
Technology	90 nm
Power supply (V_{DD})	2.2 V
Power dissipation (P_D)	< 10 mW

Table 5.3: Design specifications of LNA

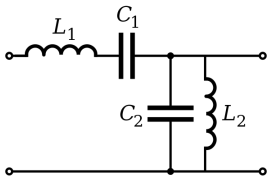


Figure 5.9: LC band pass filter

$$L_1 = \frac{Z_0}{2\pi(f_2 - f_1)}. \tag{5.1}$$

$$L_2 = Z_0 \frac{(f_2 - f_1)}{4\pi f_2 f_1}. \tag{5.2}$$

$$C_1 = \frac{2(f_2 - f_1)}{4\pi f_2 f_1 Z_0}. \tag{5.3}$$

$$C_2 = \frac{1}{Z_0 \pi (f_2 - f_1)}. \tag{5.4}$$

5.3.2 Design of L_s, L_g and C_{gs}

The input impedance (Z_{in}) is defined as the ratio of input voltage (V_{in}) to input current (I_{in}) given in Eq. (5.9). The input impedance of the common source inductive degenerated LNA is computed from the equivalent circuit as shown in Fig. 5.10.

$$V_{in} = I_{in} s L_g + I_{in} \frac{1}{sC_{gs}} + (I_{in} + g_m V_{gs}) s L_s. \tag{5.5}$$

$$V_{gs} = \frac{I_{in}}{sC_{gs}}. \tag{5.6}$$

$$V_{in} = I_{in} s L_g + I_{in} \frac{1}{sC_{gs}} + (I_{in} + \frac{g_m I_{in}}{sC_{gs}}) sL_s. \tag{5.7}$$

$$V_{in} = I_{in}[s(L_g + L_s] + \frac{1}{sC_{gs}} + \frac{g_m L_s}{C_{gs}}]. \tag{5.8}$$

Where, s, L_g, L_s, C_{gs} and g_m are complex frequency, gate inductance, source inductance, the gate to source capacitance, and transconductance, respectively.

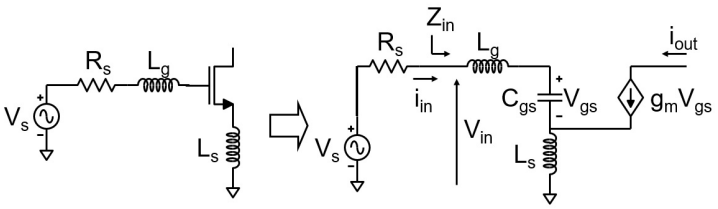


Figure 5.10: Input equivalent circuit of inductive degeneration architecture

$$Z_{in} = \frac{V_{in}}{I_{in}} = [s(L_g + L_s] + \frac{1}{sC_{gs}} + \frac{g_m L_s}{C_{gs}}]. \tag{5.9}$$

At resonance (ω=ω_o), $Im(Z_{in}) = 0$ and $Re(Z_{in}) = R_s$.

$$\omega_o(L_g + L_s) = \frac{1}{\omega_o C_{gs}} \implies \omega_o = \frac{1}{\sqrt{(L_g + L_s)C_{gs}}} \implies \omega_o^2(L_g + L_s)C_{gs} = 1. \tag{5.10}$$

$$R_s = \frac{g_m L_s}{C_{gs}}. \tag{5.11}$$

$$R_s = \omega_T L_s. \tag{5.12}$$

$$\omega_T = \frac{g_m}{C_{gs}}. \tag{5.13}$$

For better input matching choose the smallest possible value of L_s and compute unity gain angular frequency (ω_T) using Eq. (5.12). Consider g_m=5 mA/V and substitute in Eq. (5.13) to obtain C_{gs}. The gate inductance L_g is obtained by substituting center frequency f_o, C_{gs} and L_s in Eq. (5.10).

5.3.3 Gain of the LNA

The gain of the LNA is defined as the ratio of output voltage (V_{out}) to input voltage(V_{in}) is given in Eq. (5.14). It is computed from Fig. 5.10 as follows

$$\frac{V_{out}}{V_{in}} = \frac{-G_m sL}{1 - \omega^2 C_{gs}(L_g + L_s) + s.L_s.G_m}. \tag{5.14}$$

$$G_m = \frac{i_{out}}{V_{in}}. \tag{5.15}$$

Substitute Eq. (5.10) in Eq. (5.14), the simplified gain is equal to

$$Gain = \frac{V_{out}}{V_{in}} = \frac{-L}{L_s}. \tag{5.16}$$

$$Gain(dB) = 20\log(\frac{V_{out}}{V_{in}}). \tag{5.17}$$

The gain of the LNA is the ratio of load inductor (L) at the drain to the source inductor (L_s). To obtain high gain the value of L is chosen large but it depends upon the maximum inductance allowed by the technology. For 90 nm the maximum inductance is obtained as 10 nH. To obtain 33 dB gain compute the L value using Eq. (5.17).

5.3.4 Calculation of noise figure

The noise factor is defined as the ratio of signal to noise ratio at the input of the network $(S/N)_{in}$ divided by the signal to noise ratio at the output of the network $(S/N)_{out}$ as shown in (5.18). Noise factor expressed in decibels is called noise figure is computed as:

$$F = \frac{(S/N)_{in}}{(S/N)_{out}}. \tag{5.18}$$

$$NF(dB) = 10\log(F). \tag{5.19}$$

The noise figure of the common source inductive source degeneration [132] at the center frequency (f_o) is given as

$$NF = 1 + \frac{\gamma}{R_s g_m}\omega_o^2(R_s C_{gs} + g_m L_s)^2. \tag{5.20}$$

Substitute Eq. (5.10) and Eq. (5.11) in Eq. (5.20) to get the simplified expression for NF

$$NF = 1 + \gamma\frac{4(g_m L_s)^2}{R_s g_m}\frac{1}{C_{gs}(L_g + L_s)}. \tag{5.21}$$

$$NF = 1 + \frac{4\gamma L_s}{L_s + L_g}. \tag{5.22}$$

Where γ is known as the bias dependent coefficient of channel thermal noise and it varies between 2-3 [132]. The noise figure is dependent on L_s and L_g. The selection of small L_s and large L_g leads to low NF.

5.3.5 Stability

Stability is one of the important factors in the design of RF amplifiers. An LNA may become an oscillator if it is unstable in the circuit performance. After circuit design, its stability is examined using the stern stability factor [131] based characterization that is given as:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2}{2\,|S_{12}|\,|S_{21}|}. \tag{5.23}$$

$$\Delta = |S_{11}|\,|S_{22}| - |S_{12}|\,|S_{21}|\,. \tag{5.24}$$

Where S_{11},S_{12},S_{21} and S_{22} are known as S-parameters of the two-port network. S_{11} is the reflection coefficient at an input port, S_{12} is the reverse isolation, S_{21} is the forward voltage gain, and S_{22} is the reflection coefficient at an output port.

If K > 1 and | Δ | < 1, then the amplifier is considered to be stable. In recent years, K and Δ are replaced by the μ factor which is defined by Eq. (5.25). For an LNA to be stable the μ should be greater than 1 in the desired frequency of operation.

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - \Delta conj(S_{11})| + |S_{12} * S_{21}|}. \tag{5.25}$$

5.3.6 Calculation of optimal width of the transistors

The optimal width (W_{opt}) is also known as the maximum allowable width for each transistor in the circuit [131]. It is obtained by using Eq. (5.26), where C_{ox} is the gate capacitance per unit area [F/m^2] and L_{min} is the minimum channel length which is equal to 90 nm, ω_o ($2\pi f_o$) is the angular frequency at center frequency (f_o).

$$W_{opt} = \frac{1}{3\omega_o L_{min} C_{ox} R_s}. \tag{5.26}$$

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{K_{ox}\epsilon_o}{t_{ox}}. \tag{5.27}$$

where ϵ_{ox}=permittivity of gate oxide Sio_2[F/m], K_{ox}=relative permittivity of gate oxide Sio_2=3.9, ϵ_o=permittivity of Vaccum($8.85*10^{-12}$)[F/m], t_{ox}=thickness of gate oxide=$3.45*10^{-11}$[m]. Find C_{ox} using (5.27) and substitute in (5.26) to find W_{opt}.

5.3.7 Calculation of power dissipation

The effective voltage applied to MOSFET is computed from (5.28). The gate to source voltage V_{gs} is varied from 0.5 V to 1 V and the threshold voltage (V_{th}) is varied from 0.2 V to 0.3 V [135].

$$V_{eff} = V_{gs} - V_{th}. \tag{5.28}$$

The bias current I_D is calculated by substituting V_{eff} and g_m in Eq. (5.29),

$$I_D = 0.5 * g_m * V_{eff}. \tag{5.29}$$

The power dissipation (P_D) is calculated as Eq. (5.30),

$$P_D = V_{DD} I_D. \tag{5.30}$$

The width of the transistor (M_1) is chosen as 45 μm nearly equal to optimal width. The minimal length of every transistor is 90 nm. The width of the transistor (M_2) should be less than the width of the transistor (M_1) to reduce the parasitic capacitance. But, it has a lower limit to reduce the noise contribution of the device [134]. The width of the transistor M_2 is chosen as 30μm. The load inductor L and load resistance R_L is used to control the gain. The buffer stage (M_3 and M_4) is used to drive 50 Ω load. When both transistors M_3 and M_4 are in saturation the computed widths are 40 μm and 15 μm, respectively [131]. W_1, W_2, W_3, W_4 are widths of the transistors M_1, M_2, M_3, M_4, respectively. The values of the components for the LNA designed at a center frequency of 28 GHz are given in Table 5.4.

Component	**Value**
L_1, L_2, C_1, C_2	2.65 nH, 14.74 pH, 11.79 fF, 2.12 pF
L_s, L_g, L	0.1 nH, 3.13 nH, 4.46 nH
W_{opt}	50 μm
L_{min}	0.09 μm
W_1, W_2, W_3, W_4	45 μm, 30 μm, 40 μm, 15 μm
V_{bias} (Input Transistor)	816.5 mV
V_{bias}(Cascade Transistor),V_{bias}(Buffer Stage)	1.1 V, 545.23 mV
C_{ox}, C_{gs}	8.42 mF/m^2, 10 fF
V_{DD}	2.2 V
R	60 Ω

Table 5.4: Designed component values of LNA operating at center frequency

5.3.8 Simulation results of the LNA using OSSDFI

The LNA executed using designed components and proposed OSSDFI has shown in Fig. 5.11. The inductor L_g,L_s and L are simulated in layout level as shown in Fig. 5.12, Fig. 5.13, and Fig. 5.14, respectively, and the same is extracted to circuit-level simulation. The inductor L_s has lower inductance, hence it is implemented using single layer differential fractal inductor

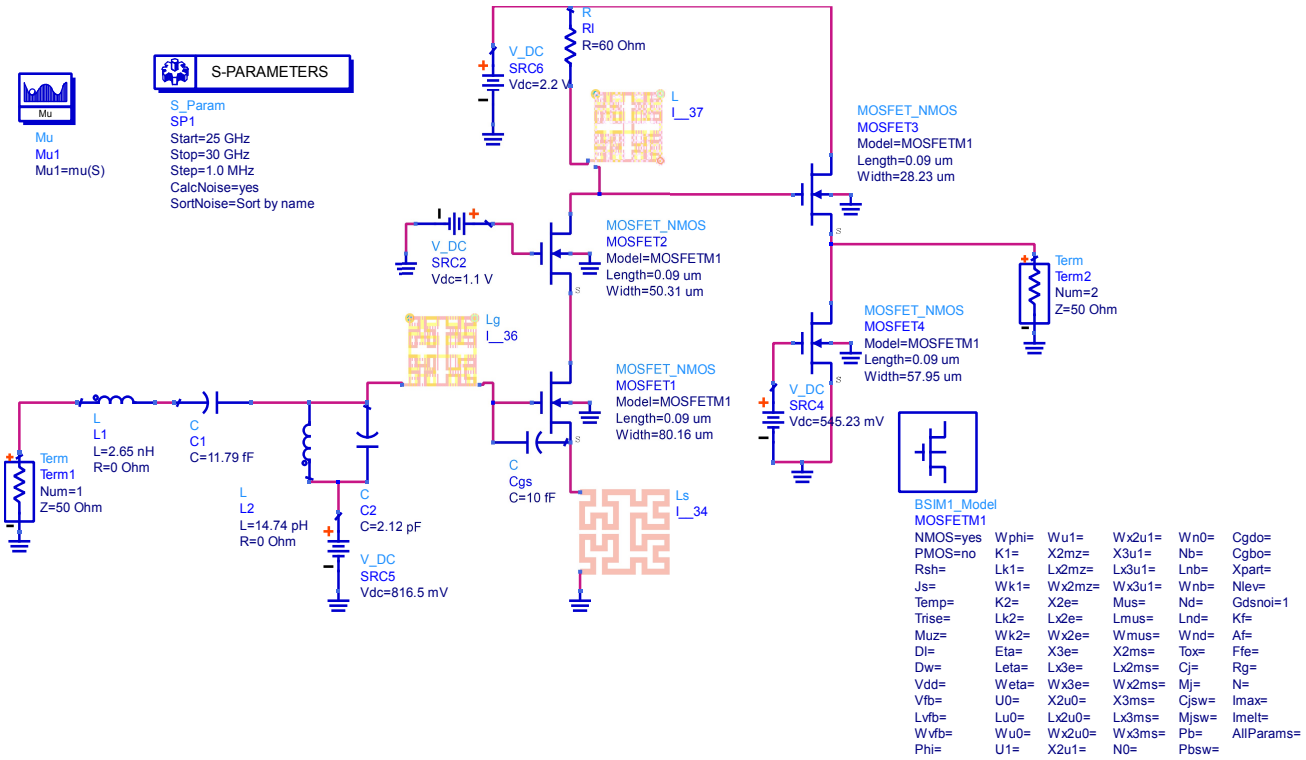


Figure 5.11: Inductive source degeneration LNA using proposed OSSDFI

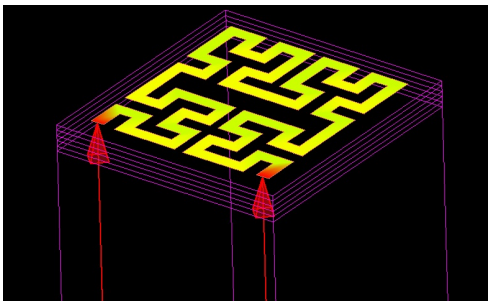


Figure 5.12: Single layer (L_s)

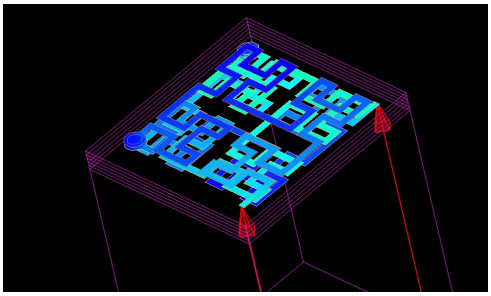


Figure 5.13: Three layer (L_g)

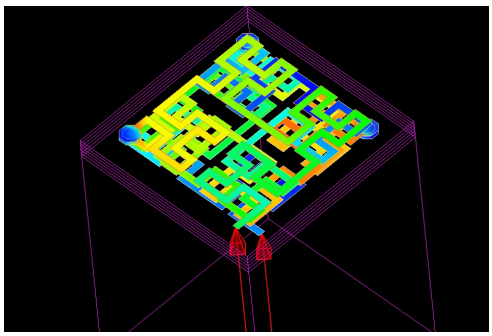


Figure 5.14: Four layer L

with an on-chip area of 25 μm $\times$ 25 μm. The inductor L_g and L shown in Fig. 5.8 are replaced by three layers and four layers OSSDFI, respectively, with an on-chip area of 100 μm $\times$ 100

μm. The simulated inductance plot for the proposed OSSDFI for the different layers is shown in Fig. 5.15. The simulated inductance values for L_s, L_g and L are 0.12 H, 3.2 nH and 4.98 nH, respectively. Comparison of designed and simulated inductances for different layers with an on-chip area is given in Table 5.5.

Inductance	**Designed inductance**	**Simulated inductance**	**No.of metal layers**	**On-chip area**
Gate inducatnce (L_g)	0.1 nH	0.12 nH	1	25 μm $\times$ 25 μm
Source inducatnce (L_s)	3.13 nH	3.2 nH	3	100 μm $\times$ 100 μm
Load inducatnce (L)	4.46 nH	4.98 nH	4	100 μm $\times$ 100 μm

Table 5.5: Comparison of designed and simulated inductances

The proposed OSSDFI achieves high inductance for a given on-chip area as the orthogonal arrangement of fractal metal layers reduces the negative mutual inductance. In order to accomplish similar inductance values as illustrated in Table 5.5 the series stacked spiral inductor and CSSFI require a large on-chip area. Consequently, the effective on-chip area to implement an LNA using the proposed OSSDFI is much less.

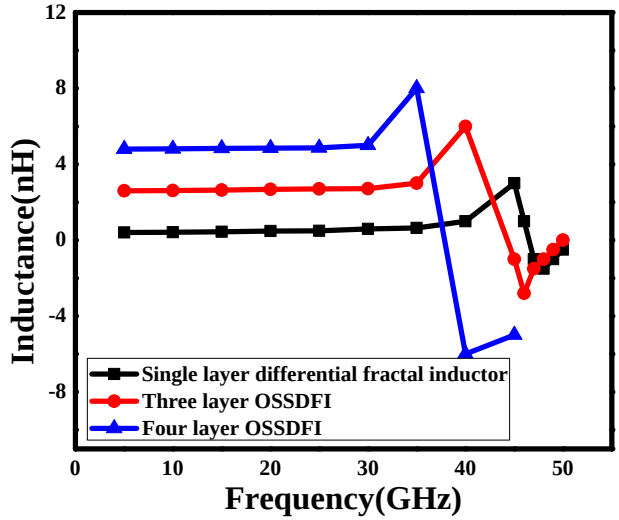


Figure 5.15: Simulated inductances for multilayer OSSDFI

The multilayer implementation reduces the series resistance of the inductor [30]. The proposed OSSDFI has very low series resistance which was shown in Table 5.2. Therefore, it has good input matching (S_{11}) of -10.438 dB at 28.46 GHz as shown in Fig. 5.16. The gate inductor (L_g) is far high compared to source inductance (L_s), hence it has a very low noise figure of 0.724-dB at 28.54 GHz as shown in Fig. 5.17. The designed gain of the LNA is 33 dB which is the ratio of load inductance to the gate inductance. The simulated gain (S_{21}) is 30.66 dB at

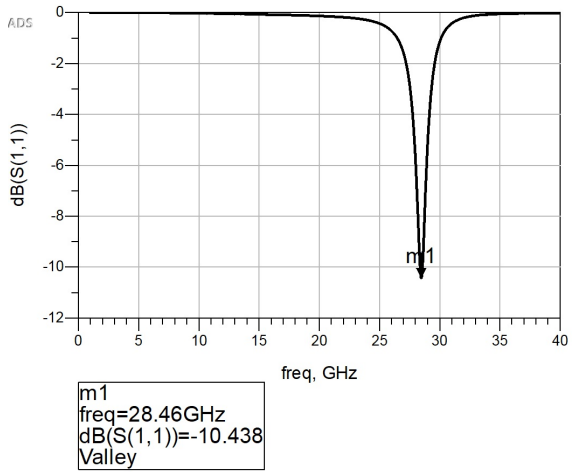


Figure 5.16: Input matching

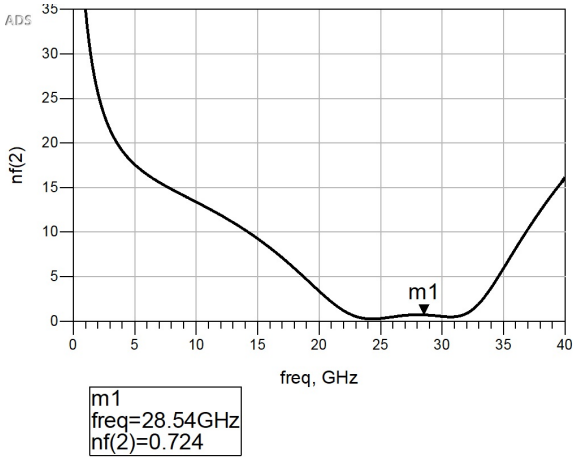


Figure 5.17: Noise figure

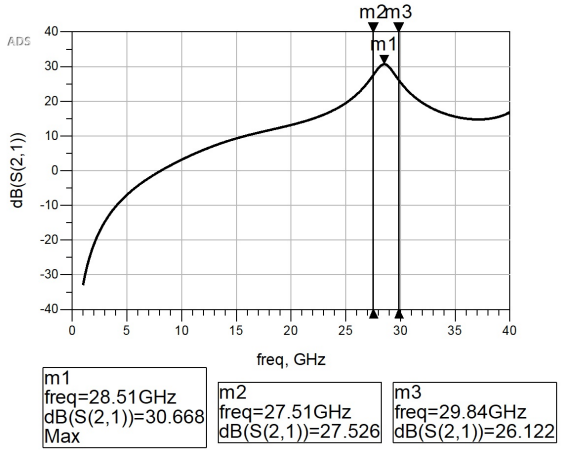


Figure 5.18: Gain

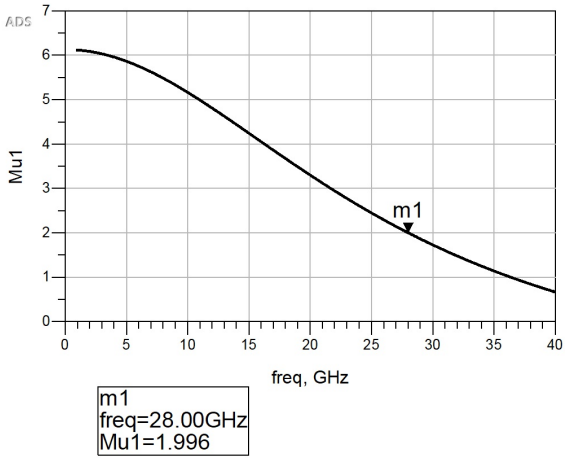


Figure 5.19: Stability factor

28.51 GHz is shown in Fig. 5.18. The 3 dB bandwidth is equal to 2.3 GHz as shown in Fig. 5.18. The stability factor plot is shown in Fig. 5.19 and the LNA is stable in the entire frequency range from 27 to 30 GHz as μ is greater than 1. The LNA has 5 mW power dissipation from the supply voltage of 2.2 V as the g_m is small. The comparison of the LNA with the existing state-of-the-art LNAs is presented in Table 5.6. The proposed LNA has high gain, low power dissipation, low noise figure, and good input matching compared to the LNAs existing in the literature. The fractional bandwidth is defined as the ratio of bandwidth to the center frequency. If the fractional bandwidth is less than 20%, the range of frequencies are known as narrowband [136]. The fractional bandwidth of the proposed LNA is 8%, hence it acts as a narrowband LNA.

Ref.	S_{11} [dB]	S_{21} [dB]	NF [dB]	Operating Freq.[GHz]	P_D [mW]	Supply Voltage	CMOS Tech.	Toplogy
[64]	-18	12.4	4.4-6.5	0.4-10	12	1.8 V	180 nm	WB, CG+CS
[137]	-9	12.5	3-7	2.6-10.2	7.2	1.2 V	90 nm	WB, Current reuse+Cascode
[138]	-9	11.9	3.6	26-42	40.8	2.4 V	90 nm	WB, Cascode
[133]	-18	14.8	3.8	29-44	18	1.2 V	90 nm	WB, Cascode
[139]	-10	21	4.67	30-50	20.4	1.2 V	90 nm	WB, Cascode
[134]	-10	11	2.6	3-10	15.4	1.8 V	180 nm	WB, Cascode
[140]	-18	11	2.6	15	15	1.3 V	130 nm	NB, Cascode
[141]	-20	13.1	3.9	24	14	1 V	180 nm	NB, Cascode
[142]	-11	12.86	5.6	24-26	30	1.8 V	180 nm	NB, Cascode
[143]	-21	15	6	24	30	1.5 V	180 nm	NB, CGRF
[144]	-18	12.5	5.4	60	4.4	1 V	90 nm	NB, Transformer Feedback
[145]	-26	21	7.6	52-56	15.1	1.5 V	130 nm	NB, Gate-inductive gain-peaking
[146]	-16	15.69	2.8	9.75-10.25	8.44	1.8 V	180 nm	NB, Cascode
This work	-10.438	30.668	0.724	27-30	5	2.2 V	90 nm	NB, Cascode

WB: Wideband, NB: Narrowband, CG: Common Gate, CS: Common Source, CGRF: Common-gate with resistive feedthrough

Table 5.6: Performance summary and comparison of the proposed LNA with state-of-the-art LNAs

5.4 Orthogonal parallel stacked differential fractal inductor (OPSDFI)

The proposed orthogonal parallel stacked differential fractal inductor has shown in Fig. 5.20 is implemented using Hilbert curves for three layers. In traditional parallel stacked fractal inductor [119] the parallel metal traces results in huge parasitic capacitance. In contrast to this, the top layer of the proposed OPSDFI has the phase differences of 90° and 180°, respectively with next consecutive two layers. This kind of orthogonal arrangement decreases the interlayer capacitance (C_s) and increases the f_{SR} of the proposed OPSDFI to a significant extent when compared with traditional parallel stacked fractal inductor. In addition to this, the three layers are stacked together by connecting vias from the top layer to the bottom layer on the four corners. This kind of stacking helps to increase the overall thickness of the inductor. The thickness of the metal and the series resistance (R_s) are in inverse relation with each other [31]. Therefore, an increase in thickness decreases the series resistance. The decrease in R_s and C_s together greatly improves the Q of the proposed OPSDFI compared with traditional parallel stacked fractal inductor.

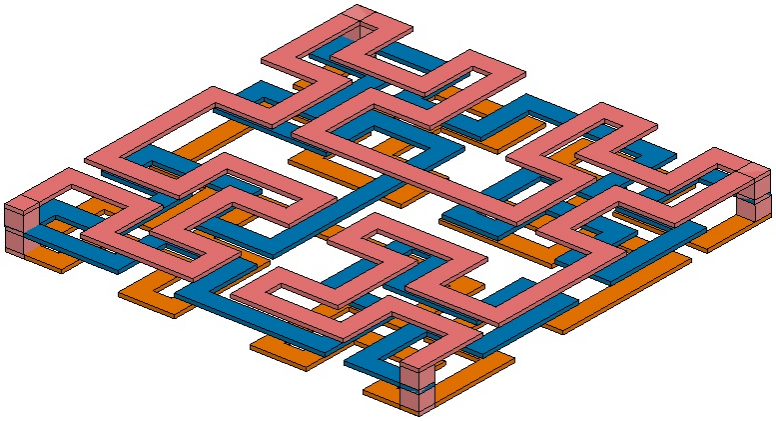


Figure 5.20: Orthogonal parallel stacked differential fractal inductor

5.4.1 Simulation results and performance analysis of the proposed OPSDFI

The proposed OPSDFI as shown in Fig. 5.21 is built with an on-chip area of 200 μm $\times$ 200 μm and conductor width of 10 μm, respectively. The simulations were performed in 180 nm CMOS technology using ADS. The input impedance (Z), inductance, quality factor, and series resistance for differential excitation of the proposed inductor were found using Eq. (1.14), Eq. (1.16), Eq. (1.18), and Eq. (1.20), respectively.

Fig. 5.22, Fig. 5.23, and Fig. 5.24, shows the plots of Q, L, and R_s, respectively. Fig. 5.21 demonstrates that the proposed OPSDFI has a very high Q value, which is two times higher than the parallel stacked fractal inductor [119] and parallel stacked symmetrical inductor [147]. From Fig. 5.22, it is also evident that the f_{SR} value is 2 times higher than the parallel stacked symmetrical inductor and nearly equal to the parallel stacked fractal inductor. Fig. 5.23 shows that the proposed OPSDFI seems to have a negotiable decrease in inductance compared to the traditional parallel stacked fractal inductor. Fig. 5.24 shows that the proposed OPSDFI has very less series resistance in the order of 10 Ω compared to the traditional parallel stacked fractal inductor and symmetrical parallel stacked inductor.

In OPSDFI, increasing the thickness of the metal reduces the series resistance even at higher frequencies, resulting in high Q values. The current crowding effects and substrate parasitics are significantly increased from the peak Q frequency (f_{Qmax}) of operation, which accounts for the drop in Q, although the thickness is very high.

The performance of the proposed OPSDFI is compared with a few parallel stacked inductors. A specific metric known as a figure of merit (FOM) is specified in (5.31) to compare the

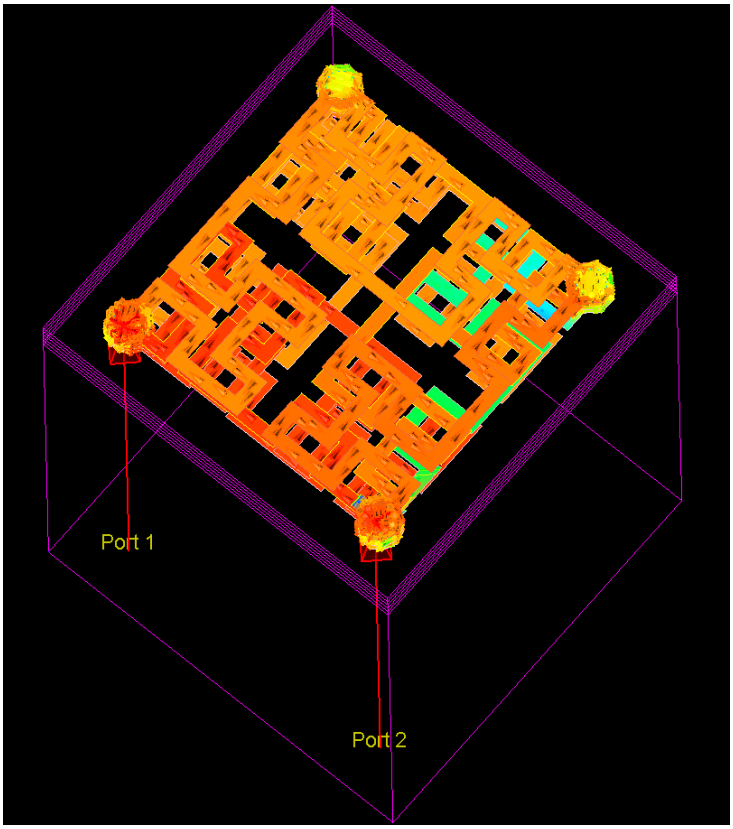


Figure 5.21: Simulation of the proposed OPSDFI (On-chip area= 200 μm × 200 μm)

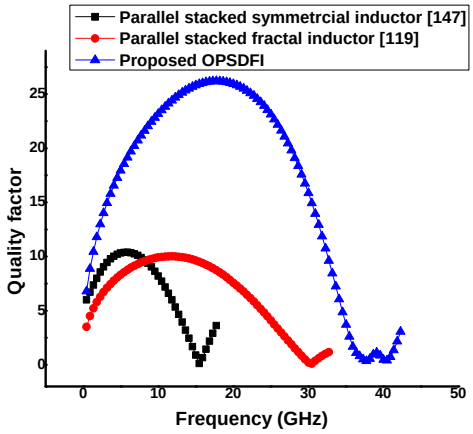


Figure 5.22: Q plots

performance of the on-chip inductor [148]. The performance comparison of the proposed OPSDFI with existing state-of-the-art is shown in Table 5.7. The FOM of the proposed OPSDFI is 5.89, and it is very large, presenting it better than the parallel stacked inductors reported in the literature.

$$FOM = \left(\frac{L \times Q \times f_{SR}}{\sqrt{Area}} \right) \tag{5.31}$$

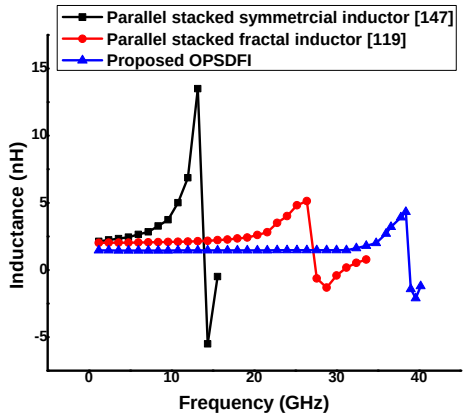


Figure 5.23: Inductance plots

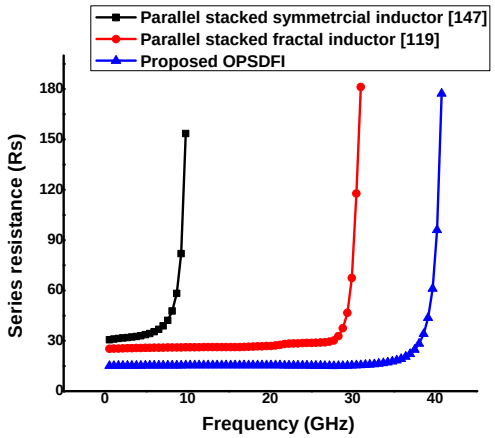


Figure 5.24: Series resistance plots

Ref..	Q	L (nH)	f_{SR} (GHz)	On-chip Area	FOM
[149]	7.06	0.5	5	117 μm × 117 μm	0.15
[104]	15.9	6.5	3	380 μm × 500 μm	0.71
[147]	14.1	2.9	17	200 μm × 200 μm	3.47
[119]	16	1.5	40	200 μm × 200 μm	4.8
This Work	**25**	**1.24**	**38**	**200 μm × 200 μm**	**5.89**

Table 5.7: State-of-the-art comparison of the proposed inductor

5.4.2 Measurement results of the fabricated OPSDFI

The proposed OPSDFI is constructed on a multi-layered printed circuit board (PCB) with a 10×10 mm^2 area mounted FR4 substrate. The thickness of copper is 0.035 mm, the separation between the layers is 0.197 mm, and the total thickness of the PCB is 1.60 mm. Fig. 5.25 displays the fabricated inductor, and the experimentation is shown in Fig. 5.26.

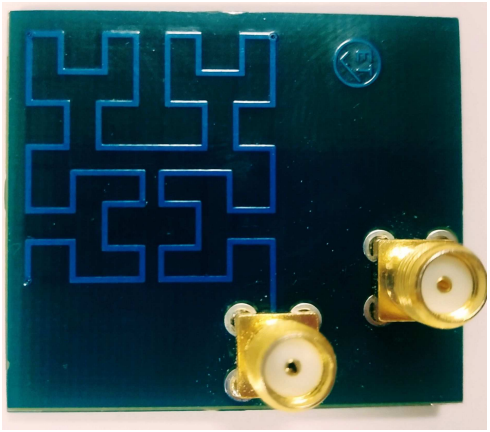


Figure 5.25: Fabricated OPSDFI on multilayer PCB

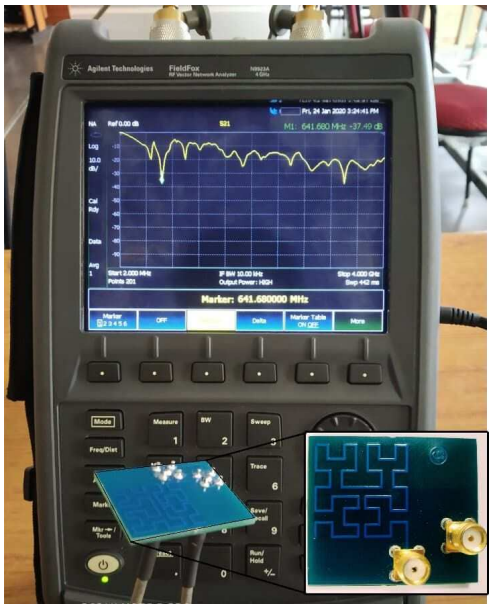


Figure 5.26: Measurement of results using VNA

Owing to variation in technology from micrometer to millimeter scale the operating frequency is diminished to MHz from GHz. Consequently, the proposed OPSDFI is simulated in the mm scale and the assessment of the measured results is carried out with the aid of a network analyzer N9923A. The similarity between measured and simulated inductances is shown in Fig. 5.27. From the graph it is apparent that the simulated and measured inductances are truly in better competition with each other, having an inductance value of approximately 33 nH. Fig. 5.27 also displays the similarities of the simulated and measured quality factors, with a peak quality factor nearly equal to 62 at 400 MHz. Table 5.8 ensures that the simulated results are in close alliance with the measured results. These findings suggest that the proposed OPSDFI is considered to be very well suited for use in the CMOS process as an on-chip inductor.

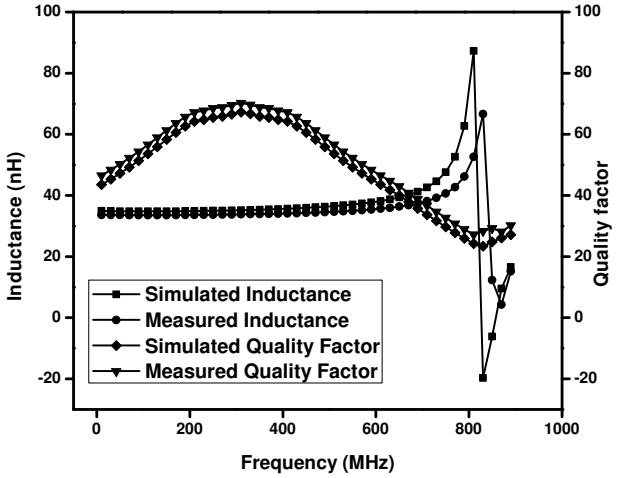


Figure 5.27: Comparison of measured and simulated results

Parameter	Simulated results	Measured results
L (nH)	36	33
Q	65	62
f_{SR} (MHz)	850	830

Table 5.8: Measured results vs Simulated results

5.5 Summary

A novel OSSDFI is designed to demonstrate the improvement in inductance and quality factor of 200% and 56%, respectively over CSSFI. The proposed OPSDFI has shown the enhancement in self-resonance frequency and quality factor over the traditional parallel stacked fractal inductor. The proposed OSSDFI and OPSDFI have been fabricated on a multilayer PCB and the measurement results are in good concurrence with the simulated results demonstrating the robustness of the design. Therefore, the proposed inductors are found to be apt for usage as an on-chip inductor in the CMOS process. A narrow band LNA is designed for 27-30 GHz using the proposed OSSDFI and the circuit simulations were done using ADS in 90 nm CMOS technology. The LNA has achieved high gain, low noise figure, low power consumption, and better input matching. These results exhibit that LNA realized using the proposed OSSDFI is appropriate for 5G communication standards.

Chapter 6

Multipath differential fractal inductor for wireless applications

6.1 Introduction

High performance on-chip inductors are essential to improve the performance of RFICs (Radio frequency integrated circuits) and MMICs (Monolithic microwave integrated circuits). Despite high Q values, the spiral inductors are unable to achieve higher inductance for the miniaturized on-chip area. This problem is solved using fractal curves in the implementation of the inductor. The space-filling property of the fractal curves results in longer conductive segments leads to high inductance density while occupying the equal on-chip area. Even though obtaining high inductance for the minimum on-chip area, single layer fractal inductors suffer from low-quality factor values. This chapter focusses on improving the quality factor of the planar fractal inductor using the multipath technique [103, 127].

This chapter is outlined as follows: Section 6.2 deals with the design and simulation of the proposed multipath differential fractal inductor and also analyzes the performance of the proposed differential fractal inductor with state-of-the-art inductors in the literature, section 6.3 illustrates the manufacturing of the proposed inductor on PCB (Printed Circuit Board) and experimental validation using Vector Network Analyzer (VNA-N9923A). Final section 6.4 presents the conclusions.

6.2 Design and simulation of the proposed multipath differential fractal inductor

The conventional fractal inductor as shown in Fig. 6.1 is built for an on-chip area of 200 μm $\times$ 200 μm with a conductor width of 10 μm. In the proposed multipath differential fractal inductor the width of the conductor is divided into multiple paths and it also occupies an on-chip area of 200 μm $\times$ 200 μm. From Eq. 3.2, the skin depth of the copper at 1 GHz and 20 GHz is obtained as 2 μm and 0.46 μm, respectively. The width of the path has chosen greater than or equal to the skin depth (δ) of the conductor [103] for the given frequency of operation. Implementation of the proposed multipath differential fractal inductor for 2-paths, 3-paths, and 4-paths is shown in Fig. 6.2, Fig. 6.3, and Fig. 6.4, respectively. In a 2-path inductor, the width of each path is 4 μm, and spacing between the paths is 2 μm. In a 3-path inductor, the width of each path is 3 μm, and spacing between the paths is 0.5 μm. In a 4-path inductor, the width of each path is 2.25 μm, and spacing between the paths is 0.4 μm.

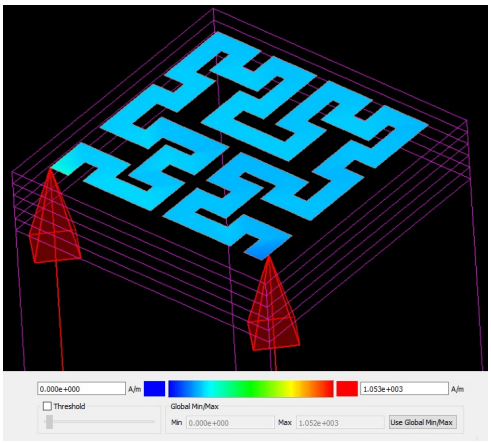


Figure 6.1: Conventional fractal

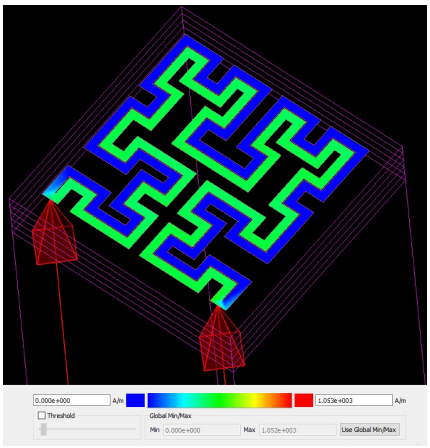


Figure 6.2: 2-path inductor

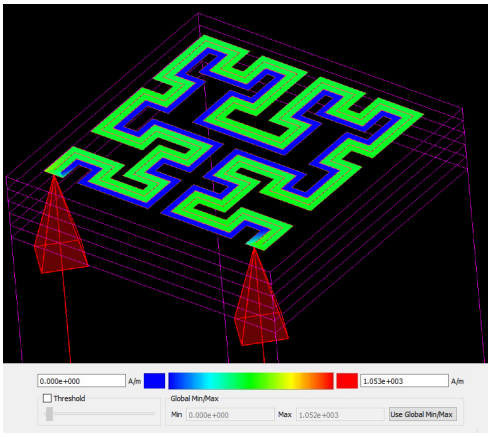


Figure 6.3: 3-path inductor

Figure 6.4: 4-path inductor

The simulations of the proposed inductor are performed in 180 nm CMOS technology using the ADS tool. The manufacturing of the proposed inductor is adaptable with the TSMC 180nm CMOS process. Fig. 4.6, shows the metal and oxide layers thickness of the TSMC 180 nm CMOS process. The proposed inductor is implemented on the top metal layer having a thickness of 3 μm. The fractal inductors are symmetrical [44], thus differential excitation is used to enhance the quality factor of the inductor [107]. The input impedance (Z_{diff}), quality factor, total inductance and series resistance for differential excitation are evaluated using Eq. (1.14), Eq. (1.16), Eq. (1.18), and Eq. (1.20), respectively.

In a conventional fractal inductor, the adjacent magnetic fields produce the eddy currents and results in non-uniform current density in the conductor. Lenz's law states that the magnetic field generated from the eddy currents oppose the original magnetic field. Thus, the induced eddy currents reduce the skin depth of the conductor and increase the series resistance (R_s). From Eq.1.3, it is apparent that the Q and R_s are inversely proportional to one another. Thus, the increase in R_s decreases the Q.

In the proposed multipath differential fractal inductor the width of the path and the spacing between each path is chosen according to the skin depth and minimum design rule [103]. Thus, the multipath technique with smaller path widths reduces the opposing magnetic fields and increases the skin depth of the metal [103]. The increase in skin depth improves the current density of the metal, which leads to an increase in Q. Thus, the multipath technique reduces skin effects and improves Q. The magnetic field generated from the adjacent metal lines induces the eddy currents and causes non-uniform current distribution in the metal. This phenomenon is called the proximity effect. The multipath technique produces the uniform current in each path and reduces the ohmic losses caused by adjacent metal lines. Thus, the proximity effect can be depressed using a multipath technique. The decrease in skin effects and proximity effects collectively reduces the series resistance of the inductor. Therefore, the proposed multipath differential fractal inductor attains a high-quality factor over a conventional fractal inductor. The current density scale is indicated at the bottom of Fig. 6.1, Fig. 6.2, Fig. 6.3, and Fig. 6.4, respectively. As the number of paths increases current density becomes more uniform owing to reduced skin and proximity effects. However, the multipath technique produces a small decrease in the inductance owing to the coupling between the adjacent paths.

Fig. 6.5 shows the comparison of the quality factor of the proposed inductor built for multiple paths and conventional planar fractal inductor. From Fig. 6.5, it is observed that at 5 GHz, the peak quality factor values for the conventional, 2-path, 3-path, and 4-path fractal inductors are 18, 24, 26, and 28, respectively, which shows the increase in the quality factor with

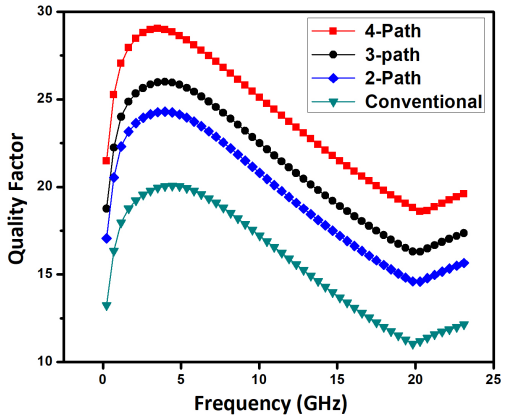


Figure 6.5: Relation between quality factor and multiple paths

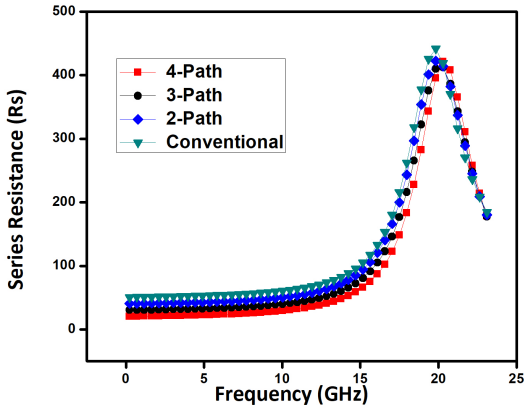


Figure 6.6: Relation between series resistance and multiple paths

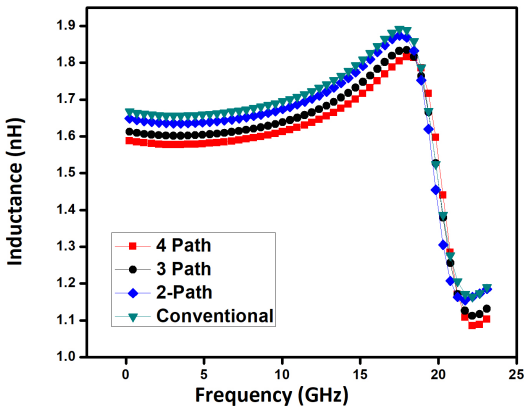


Figure 6.7: Relation between inductance and multiple paths

the increase in the number of paths. The proposed inductor implemented for 4-paths attains a very high-quality factor which is 55% higher than the conventional planar fractal inductor. The

series resistance plot as shown in Fig. 6.6 illustrates the decrease in series resistance with an increase in the number of paths. From Fig. 6.6, it is evident that the series resistance values for the conventional, 2-path, 3-path, and 4-path fractal inductors are 45 Ω, 35 Ω, 25 Ω, and 20 Ω, respectively, which shows the decrease in series resistance with the increase in the number of paths. From Fig. 6.7, it is evident that the inductance values for the conventional, 2-path, 3-path, and 4-path fractal inductors are 1.68 nH, 1.65 nH, 1.61 nH, and 1.58 nH, respectively, which shows a small decrease in inductance between the adjoining paths owing to negative mutual coupling.

The adoption of the multipath width technique for the fractal inductor decreases the proximity and skin effect since the narrower metal width can have a higher Q due to lower eddy-current losses in the metal and substrate at higher frequencies. However, after peak Q frequency (f_{Qmax}) of operation, the current crowding effects, and substrate parasitics are more dominant which are responsible for the decrease in Q.

The proposed fractal inductor attains high-quality factor values (>25) between 2-12 GHz that covers wireless application-oriented bands such as S-band (2-4 GHz) which is used for Wifi, Bluetooth, and cellular phones applications, C-band (4-8 GHz) which is used for Satelite and microwave relay applications, and X-Band (8-12 GHz) which is used for Radar applications. Hence, it is recommended to utilize the proposed multipath differential fractal inductor for these wireless applications. A unique parameter known as a Figure of Merit (FOM) specified in Eq. 5.31 is used to compare the performance of the proposed inductor with different inductors in the literature. Table 6.1 demonstrates that the proposed inductor has a higher FOM of 4.59 compared to state-of-the-art inductors.

Ref...	**Q**	**L (nH)**	$f_{SR}(GHz)$	**On-chip area** (μm^2)	**FOM**
[116]	12	0.9	10	180×235	0.52
[127]	15	0.5	15	200×200	0.56
[103]	6.07	3.2	8	240×240	0.64
[107]	6.6	7.8	6	250×250	1.23
[150]	20	9.2	3.2	350×350	1.68
[151]	22	3.42	12	340×340	2.65
[147]	14	2.9	17	200×200	3.47
This Work	**28**	**1.64**	**20**	$\mathbf{200 \times 200}$	**4.59**

Table 6.1: Comparison of the proposed multipath fractal inductor with state-of-the-art inductors

6.3 Fabrication and measurement of results on PCB

Due to the unavailability of fabrication on the Silicon substrate, the proposed inductor is scaled down to lower frequencies and fabricated on the Printed Circuit Board (PCB) using FR-4 substrate with an area of 20 mm × 20 mm. The thickness of copper is 0.035 mm and the overall PCB thickness is 1.60 mm. Fig. 6.8 shows the fabrication of the proposed inductor constructed for 4-paths and Fig. 6.9 shows the experimentation of the fabricated inductor using Vector Network Analyzer (VNA-N9923A). The proposed inductor is validated experimentally using VNA of the frequency range from 0.01GHz to 1GHz. Owing to variation in technology from micrometer to mm scale the operating frequency is diminished to MHz from GHz. Consequently, the simulation results of the proposed inductor in mm scale are compared with the measurement results. From Fig. 6.10, it is evident that the simulated and measured inductances are really in better competition with each other, having the inductance value approximately equal to 25 nH. Furthermore, Fig. 6.10 also displays that the simulated and measured quality factors are in good agreement with one another, with a peak Q equal to 73 at 125 MHz. The comparison of measured and simulated results is given in Table 6.2. The close alliance of the simulated and measured results recommends that the proposed inductor is considered to be a good candidate as an on-chip inductor in the CMOS process.

Parameter	Simulated	Measured
Quality factor	73	70
Self-resonance frequency (MHz)	284	280
Inducatnce (nH)	25	22

Table 6.2: Measured results vs Simulated results

6.4 Summary

In this chapter, a multipath differential fractal inductor is proposed to demonstrate the increase in quality factor over the conventional planar fractal inductor. The proposed inductor has shown a 55% enhancement in Q over conventional fractal inductor for the equal on-chip area owing to reduced skin and proximity effects. The measured results of the proposed inductor manufactured on the PCB are in close competition with the simulated results exhibit the efficiency of the design. Thus, it is recommended to utilize the proposed inductor as an on-chip inductor in the CMOS process. The proposed multipath differential fractal inductor at-

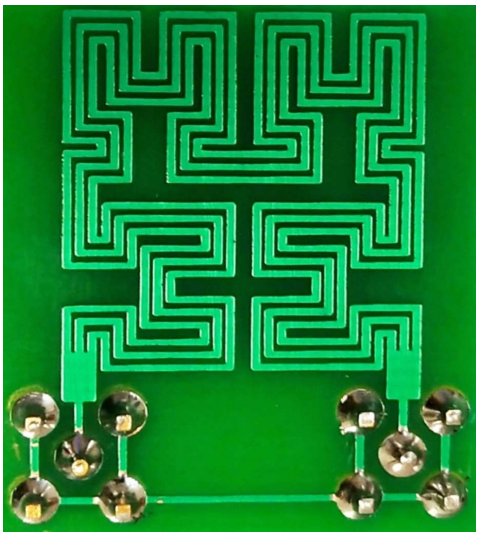


Figure 6.8: Fabricated inductor

Figure 6.9: Measurement of results

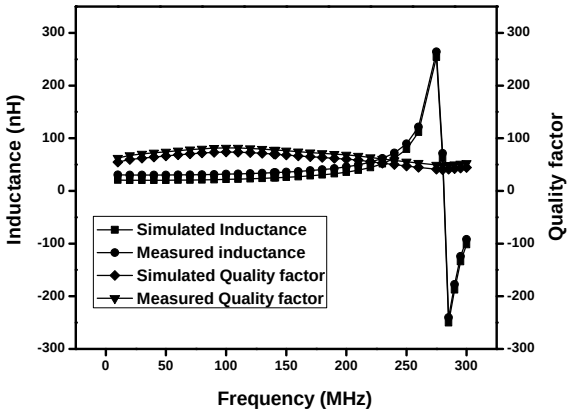


Figure 6.10: Comparison of simulated and measured results

tains a high-quality factor (>25) makes it suitable for the implementation of the critical building blocks of the wireless transceivers such as LNA, VCO, and filters.

Chapter 7

Conclusions And Future Scope

7.1 Conclusions

The thesis focusses on the design, analysis, and fabrication of multilayer on-chip differential spiral and fractal inductotrs along with implementation of LNAs which are essential in implementation of high frequency RFICs and MMICs.

Initially, variable width series stacked differential spiral inductor is proposed which attains 30% improvement in Q and 35% improvement in inductance over planar standard differential inductor for the equivalent on-chip area. Furthermore, variable multipath width multilayer differential inductor is proposed that attains 30% and 18% improvement in Q, 50% and 15% improvement in Peak Q frequency (f_{Qmax}), and 50% and 25% improvement in self-resonance frequency over planar and multipath differential inductors, respectively. Later, series stacked non-parallel multipath differential inductor is proposed that achieves 25% improvement in f_{SR} and 33% improvement in Q over conventional series stacked multipath inductor for the equivalent inductance and on-chip area. Thus, multilayer differential spiral inductors with variable width and multipath techniques have achieved high inductance, high-quality factor, and high self-resonance frequency compared to the planar and multilayer differential spiral inductor.

Fractal curves were used in the implementation of on-chip inductors to improve the performance. As a part of this, a novel hybrid series stacked differential fractal inductor has been proposed. The hybrid inductor combines the properties of both Hilbert and Sierpinski curves and yields good performance. The proposed inductor has shown 35%, 50%, and, 30% improvement in inductance, quality factor, and f_{SR}, respectively over conventional series stacked

fractal inductors for the equivalent outer diameter. Due to the unavailability of fabrication on the Silicon substrate, the proposed inductor is scaled down to lower frequencies and fabricated on the multilayer Printed Circuit Board (PCB). The close alliance of the simulated and measured results recommends that the proposed inductor is considered to be a good candidate as an on-chip inductor in the CMOS process. The hybrid inductor has high Q values between 5-20 GHz frequency which are well within the MMIC band, thus it's promising to be included in MMIC applications possibly in the near future.

Orthogonal series stacked differential fractal inductor has proposed that achieves 200% and 56% improvement in inductance and quality factor, respectively. Orthogonal parallel stacked differential fractal inductor proposed has attained a 2-fold improvement in quality factor and more than 50% enhancement in self-resonance frequency compared to the traditional parallel stacked fractal inductor with a relatively minimal decrease in inductance. The proposed OSSDFI and OPSDFI have been fabricated on a multilayer PCB and the measurement results are in good concurrence with the simulated results demonstrating the robustness of the design. Therefore, the proposed inductors are found to be apt for usage as an on-chip inductor in the CMOS process. A narrow band LNA is designed for a 27-30 GHz frequency range using the proposed high Q OSSDFI. The LNA has achieved a high gain of 30.668 dB, a low noise figure of 0.724 dB, and good input matching of <-11 dB. The LNA has a power dissipation of 5 mW from a 2.2-V power supply and it has 3-dB bandwidth equal to 2.3 GHz.

Finally, a multipath differential fractal inductor has been proposed that attains 65% improvement in Q over conventional planar fractal inductor for equivalent inductance, self-resonance frequency, and on-chip area. The measured results of the proposed inductor manufactured on the PCB are in close competition with the simulated results that exhibit the efficiency of the design. Therefore, it is recommended to utilize the proposed inductor as an on-chip inductor.

7.2 Future Scope

Performance of RF Circuits and mm wave circuits could be enhanced by replacing the existing inductors with the proposed ones. Using patterned ground shield, EBG (Electromagnetic band gap) structures, magnetic materials as substrate, Figure-of-merits of the proposed on-chip inductors could be improved.

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List of Publications

List of Accepted/Published Journals

1. Sunil Kumar Tumma and N. Bheema Rao, “Design of high performance narrowband low noise amplifier using an on-chip orthogonal series stacked differential fractal inductor for 5G applications", *Turkish Journal of Electrical Engineering & Computer Sciences*, Vol 28, No, 1, 45-60, 2016, doi:10.3906/elk-elk-1903-185. (SCIE indexed).

2. Sunil Kumar Tumma and N. Bheema Rao, “A novel hybrid series stacked differential fractal inductor for MMIC applications", *Circuit World (Emerald Publishing)*, Vol 46, No,2, pp.137–145, 2019, doi: 10.1108/CW-06-2019-0058. (SCIE indexed).

3. Sunil Kumar Tumma and N. Bheema Rao, “High-quality factor multipath differential fractal inductor for wireless applications", *Circuit World (Emerald Publishing)*. (SCIE indexed).

4. Sunil Kumar Tumma and N. Bheema Rao, “High Q orthogonal parallel stacked differential fractal inductor for MMIC applications", *The IET Microwaves, Antennas & Propagation*. (SCIE indexed- Under Revision).

5. Sunil Kumar Tumma and N. Bheema Rao, “Series stacked non-parallel multipath differential inductor for C band Applications", *Springer Lecture Notes in Electrical Engineering-Book Chapter*, Published. (Scopus Indexed).

List of published conferences

1. Sunil Kumar Tumma and N. Bheema Rao, “A novel High Q variable width differential series stacked spiral inductor", *IEEE international conference on Computing communication and Networking Technologies (ICCCNT)*, 3^{rd} – 5^{th} July, 2017, IIT Delhi, Delhi, India. (IEEE Xplore).

2. Sunil Kumar Tumma and N. Bheema Rao, “High performance Variable width multipath multilayer differential inductor", *IEEE India Council International Conference (INDICON-2017)*,15^{th} – 17^{th}, December, 2017, IIT-Roorke, Roorke, India. (IEEE Xplore).