INVESTIGATION ON SINGLE-PHASE VOLTAGE SOURCE BASED INVERTER TOPOLOGIES FOR GRID-CONNECTED PHOTOVOLTAIC POWER GENERATION SYSTEMS

Submitted in partial fulfilment of the requirements

for the award of the degree of

DOCTOR OF PHILOSOPHY
in
Electrical Engineering

By

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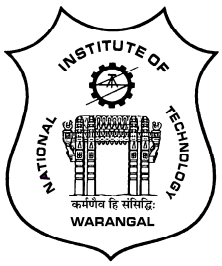

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AUGUST-2020

APPROVAL SHEET

This Thesis entitled "**Investigation on Single-Phase Voltage Source based Inverter Topologies for Grid-Connected Photovoltaic Power Generation systems**" by **Kuncham. Sateesh Kumar** is approved for the degree of Doctor of Philosophy.

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CERTIFICATE

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DECLARATION

This is to certify that the work presented in the thesis entitled **"Investigation on Single-Phase Voltage Source based Inverter Topologies for Grid-Connected Photovoltaic Power Generation systems"** is a bonafide work done by me under the supervision of **Dr. A. Kirubakaran, Assistant Professor, & Dr. N. Subrahmanyam, Professor,** Department of Electrical Engineering, National Institute of Technology Warangal, Warangal, India and was not submitted elsewhere for the award of any degree.

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ACKNOWLEDGEMENTS

It gives me immense pleasure to express my deep sense of gratitude and thanks to my supervisor **Dr. A. Kirubakaran,** Assistant Professor, and **Dr. N. Subrahmanyam**, Professor, Department of Electrical Engineering, National Institute of Technology Warangal, for their invaluable guidance, support, and suggestions. Their knowledge, suggestions, and discussions helped me to become a capable researcher. They showed me the interesting side of this wonderful and potential research area. Their encouragement helped me to overcome the difficulties encountered in my research as well in my life.

I am very much thankful to **Prof. M. Sailaja Kumari** Head, Department of Electrical Engineering for his constant encouragement, support and cooperation.

I take this privilege to thank all my Doctoral Scrutiny Committee members, **Dr. V. T. Somasekhar**, Professor, Department of Electrical Engineering, **Dr. B. L. Narasimharaju,** Associate Professor, Department of Electrical Engineering and **Dr. P. Srihari Rao,** Associate Professor, Department of Electronics and communication Engineering for their detailed review, constructive suggestions and excellent advice during the progress of this research work.

I also appreciate the encouragement from teaching, non-teaching members, and fraternity of Department of Electrical Engineering of NIT Warangal. They have always been encouraging and supportive.

I wish to express my sincere thanks to **Prof. N.V. Ramana Rao**, Director, NIT Warangal for his official support and encouragement.

I convey my special thanks to my contemporary Research Scholars Mr. Jammy Ramesh Rahul, Mr. Abhilash T, Mr. Chinmay Kumar Das, Mr. Venu Sonti, Mr. Hema Sundhar K, Mr. Sathyakar VVK, Mr. Bhaskar, Mr. Ram Kumar, Mr. Gurappa, Mr. Anil Kumar B, Mr. Kalyan, Mr. Sachidananda Prasad, Mr. Eswar Gowd, Mr. Vishnu Prasad, Mr. Hareesh M, Mr. Suresh L, Mr. Ratna Rahul and also M Tech (Power Electronics) students Suneel B (2019), Punam (2020).

I acknowledge my gratitude to all my teachers and colleagues at various places for supporting me to complete the work.

I wish to express my gratitude to SERB for utilizing facilitates to carry out a part of the research work under EMR project grant 2016/007811.

My special, sincere acknowledgement, heartfelt gratitude and indebtedness are due to my parents **Shri. K. Srirama Murthy** & **Smt. Bharati**, my wife **K. Rama Devi**, my grandmother **K. Anasuryamma,** my sister **Ch. Sandhya**, my brother **K. Ashok Kumar,** my uncle **V. Srinivas**, my Aunt **V. Dhanalakshmi**, and other family members for their sincere prayers, blessings, constant encouragement, shouldering the responsibilities and moral support rendered to me throughout my life, without which my research work would not have been possible. I heartily acknowledge all my relatives for their love and affection towards me.

Above all, I express my deepest regards and gratitude to "**ALMIGHTY**" whose divine light and warmth showered upon me the perseverance, inspiration, faith and enough strength to keep the momentum of work high even at tough moments of research work.

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ABSTRACT

Emerging renewable power generations such as photovoltaic, wind, and fuel cells are getting much attention of the researchers in the present scenario due to dwindling conventional energy sources. As per the renewable global status report, the photovoltaic power generation systems (PVPGS) during the last decade has an exponential growth due to low price and deserves a prominent place with an overall global installation of 583.5 GW capacity by the end of 2019. Among those, the grid-connected PVPGS occupied 90% of the market share due to its simple structure, low cost, and longer life-time. Depends on the voltage and power rating of the PV source, each grid-connected PVPGS comprises a series, parallel, and both the combinations of PV modules, followed by inverter and filter circuit to feed the generated power into the AC grid.

Based on the number of power processing stages, the inverters are classified into single-stage and two-stage systems. The applications such as central (100 kW to 850 kW) and string PVPGS (1 kW to 10 kW) require a single central inverter to interface with a whole PV array to the grid, known as single-stage inverter. Conversely, applications like module (<1 kW) and multi-string (10 kW to 100 kW) PVPGS utilize a front end DC-DC converter followed by an inverter for injecting PV power into the grid, known as two-stage inverter. Moreover, an additional DC-DC converter is used prior to the inverter for extracting maximum power from the PV source and for boosting the low PV voltage to higher DC voltage. The number of PV modules which are connected in series are less in two-stage inverter in comparison with the single-stage inverter to overcome the effects due to partial shading and module mismatch. Whereas, the two-stage inverter requires more number of passive components and power electronic devices for boosting and inversion operations, which results in increased component count and reduced efficiency. Since, both of the single-stage and two-stage inverters have their own merits and demerits; hence they will optimally selected based on the power generating capacity.

In both of the inverter configurations, galvanic isolation from the leakage current is a major challenge to solve the safety and reliability issues of grid-

connected PVPGS. To address this issue, both the single-stage and two-stage inverters are further categorized into isolated type and non-isolated type based on the placement of transformer in the power conversion stage. A bulky line frequency transformer (LFT) in the AC grid side or a compact high frequency transformer (HFT) in the DC source side is normally employed to provide the galvanic isolation between the PV source and the grid. Besides the galvanic isolation, it also steps up the low PV output voltage. However, the use of transformer make the system become heavy, expensive and reduces its overall efficiency.

To alleviate the above drawbacks transformerless or non-isolated inverters becomes popular in the PVPGS. However, the removal of the transformer yields a direct connection between the inverter and PV module. In consequence, a resonant circuit is formed with the parasitic capacitances among PV module and ground, filter inductors and grid impedances. The common mode voltage (CMV) fluctuations produced by the inverter can excite this resonant circuit and causes the flow of leakage current from grid to PV module through PV parasitic capacitance (C_{PV}). This increases electro-magnetic interference (EMI), total harmonic distortion (THD) and power losses, and also decreases the reliability and operational safety. Therefore, various topologies and different pulse width modulation (PWM) schemes have been proposed to reduce the leakage current and to enhance the overall system efficiency.

In contemporary, multilevel inverters (MLIs) are emerging in the area of grid-connected PVPGS because of its significant advantages like high quality of power output by lowering the THD, reduced losses with the reduction in voltage stress of the switches, reduced filter size with increased modularity. It is much more advantageous to have such benefits in non-isolated PV inverter topologies along with a reduction in leakage current. The popular MLI configurations are neutral point clamped (NPC), flying capacitor (FC) and cascaded H-bridge (CHB) inverters. The limitations of these MLIs are more component count, voltage balancing issues and control complexity for an increased number of output voltage levels. To overcome these drawbacks various other topologies are also developed in recent years. Most of these topologies utilizes the classical structures such as NPC, FC, CHB, and their variants. However, some of the

common limitations are stopping the usage of MLIs directly into grid-connected PVPGS such as higher leakage current, requirement of isolated DC sources, and increased component count.

Hence, there is a wide scope for further research in the area of single-phase inverter topologies for grid-connected PVPGS. Moreover, to address the aforesaid issues, namely, (i) operability with a single source, (ii) reduced switch count, (iii) leakage current reduction without the use of isolation transformer, (iv) reactive power capability, and (v) high efficiency, this research focuses on the development of different single-stage and two-stage inverter topologies for grid-connected PVPGS. In this context, four single-stage configurations and three two-stage configurations have been proposed in this thesis.

In the first proposal, a bi-directional clamping (BDC) based H5, Highly efficient reliable inverter concept (HERIC), and H6 TLI topologies are proposed with improved PWM schemes. BDC branch reduces the leakage current by clamping the inverter terminal voltages to half of the DC-link voltage during the freewheeling period and the improved PWM schemes ensure bi-directional current path while operating in negative power region. The common mode and differential characteristics of all the topologies are tested with MATLAB simulations and further justified with experimental results. Moreover, the performance characteristic comparisons of the proposed and traditional topologies are presented to highlight the merits of the proposed solution over the conventional.

In the second proposal, a novel two-stage power conditioner with the inherent benefits of boosting, generation of seven-level output voltage with minimum leakage current in a grid-connected PVPGS is proposed. The proposed power conditioner is an upgrade of a front-end multi output dc–dc boost converter and an asymmetrical seven-level inverter. A HFT employed in front-end converter produces balanced dc-link voltages to generate the seven-level output voltage. The leakage current caused by the parasitic capacitance of the PV panel is minimized by providing a common-mode conducting path to the inverter. This results in a reduction of the leakage current well below the grid standards. Furthermore, the proposed configuration utilizes a minimum number of devices

for every level generation, which reduces the control complexity and also improves the system efficiency.

In the third proposal, a two-stage hybrid transformerless multilevel inverter for single-phase grid-connected PVPGS is presented. The proposed topology comprises a multilevel boost converter (MLBC) and a symmetrical hybrid MLI. MLBC combines the boosting and switched capacitor voltage functions to produce self-balanced multiple voltage levels. The proposed MLI is derived from a combination of bidirectional switches, a half bridge, and a diode-clamped branch, which can produce only two variations in the total common mode voltage and is capable of suppressing leakage current as per VDE 0126-1-1 grid standards. It offers the advantages of scalability, reactive power capability, reduced total harmonic distortion, and filter size.

In the fourth proposal, a T-type hybrid five-level inverter and its level-shifted pulse width modulation scheme offers: (i) Reduced leakage current by eliminating the high frequency variations and sudden transitions in the voltage across PV parasitic capacitance, (ii) A path for the negative current in all the modes of operation under unity and non-unity power factor conditions of the grid without degrading the waveform quality. Moreover, the proposed inverter is integrated with a traditional three-level boost converter (3LBC) for boosting the PV output voltage and also to extract maximum power from the PV source. The 3LBC provides high efficiency and reduced input inductor size for the same power rating over the conventional boost converter.

In order to evolve steady state and dynamic performance of all the proposed topologies reported in the thesis, a thorough investigation of all the topologies has been achieved through both simulations and experiments. The simulations are performed in MATLAB/Simulink software and the proto type models are built using IRFP460 MOSFET modules and TLP250 opto coupler driver ICs. The control schemes are implemented in MATLAB Platform using Xilinx System Generator Blocks, Spartan 6 FPGA processor, and DSP TMS320F2812/28335 processor for real time operation. The grid-connected operation of the proposed topologies is verified using OPAL-RT OP4500 real-time modules. Moreover, in this study, an exhaustive comparison of various

topologies is shown based on component count, voltage stress across the semiconductor devices, common mode voltage behavior, and leakage current magnitude to demonstrate the merits of the proposed topologies. Finally, the performance of the proposed topologies is evaluated through Power Simulation (PSIM) thermal module and records maximum efficiency of 90-98%. This ensures that the proposed topologies are most opted for grid-connected PVPGS.

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ABBREVIATIONS

3LBC	Three-level boost converter
AC	Alternating Current
ADC	Analog to digital conversion
AH6	Active H6
ANPC	Active Neutral-Point Clamped
BDC	Bi-Directional clamping branch
BPWM	Bipolar PWM
BIS	Bureau of Indian Standards
CCM	Continuous Conduction Mode
CHB	Cascaded H-Bridge
CMF	Common-mode Filter
CMLI	Cascaded Multitlevel Inverter
CMV	Common-mode Voltage
CSI	Current Source Inverter
CSV	Comma separated values
DBSMI	Double Bidirectional Switch Multilevel inverter
DC	Direct Current
EMI	Electro-magnetic Interference
FBNPC	Full-Bridge NPC
FC	Flying Capacitor
FPGA	Field programmable gate array
H-B	Hybrid-Bridge
H-B	Hybrid-Bridge
HBZVR-D	H-Bridge Zero Voltage State Rectifier–Diode
HERIC	Highly Efficient and Reliable Inverter Concept
HFT	High Frequency Transformer
HIL	Hard ware in Loop
HNPC	Hybrid NPC
HRE	Highly Reliable and Efficient
IEA	International Energy Agency
IEC	International Electro-technical Commission

IEEE	Institute of Electrical and Electronics Engineers
LFT	Line Frequency Transformer
MDO	Mixed Domain Oscilloscope
MLBC	Multi-level boost converter
MLI	Multilevel Inverter
M-NPC	MOSFET-neutral point clamped converter
MPPT	Maximum power point tracking
NPC	Neutral-point Clamped
P and O	Perturb and Observation
PCB	Printed circuit board
PI	Proportional-Integral
PN-NPC	Positive And Negative Neutral Point Clamped Converter
PR	Proportional-Resonant
PSIM	Power Simulation
PV	Photovoltaic
PVPGS	PV Power Generation Systems
PWM	Pulse-width Modulation
RMS	Root-Mean Square
SLS-PWM	Sinusoidal level-shifted pulse width modulation
THD	Total Harmonic
TLI	Transformerless Inverter
UPF	Unity Power Factor
UPWM	Unipolar PWM

LIST OF SYMBOLS

C_{dc}	DC-link capacitor
C_{PV}	PV parasitic capacitance
C_{1g}, C_{2g}	Parasitic capacitance between the heat-sink and ground
C_f	Filter capacitor
$C_{DM\text{-}S}$	Split DC-link capacitor
C_{oss}	Output capacitance
D	Duty ratio
f_s	Switching frequency
f_r	Resonance frequency
g	ground
i_{max}	Maximum load current
I_{rr}	Reverse- recovery time
i_c	Circulating current
$Iref$	Reference grid current
i_g	Grid current
$i_{leakage}$	Leakage current
K_P	Integral constant
K_I	Integral constant
$L1$	Filter inductor 1
$L2$	Filter inductor 2
M_a	Modulation index
N	Negative terminal of the DC source
P	Positive terminal of the DC source
PLL	Phase locked loop
$Prated$	Output power rating
$P_{SW\text{-}I}$	Switching loss of the inverter
$P_{SW\text{-}B}$	Switching loss of the boost converter
Pc	Conduction loss of the inverter
$P_{C\text{-}D}$	Conduction loss of the diode
$P_{SW\text{-}D}$	Switching loss of the diode
R_f	Damping resistor

t_b	Turn-off time of the diode
t_{off}	Turn-off time
t_{on}	Turn-on time
Tc	Total time of conduction
V_{AN}	Voltage across inverter terminal A to negative terminal of DC source
V_{BN}	Voltage across inverter terminal B to negative terminal of DC source
V_{DM}	Differential-mode voltage
V_{CM}	Common-mode voltage
$V_{CM\text{-}DM}$	Additional Common-mode voltage
V_{TCMV}	Total common-mode voltage
V_{dc}	DC input voltage
v_g	Grid voltage
$V_{N\text{-}g}$	Voltage between the source negative terminal to ground
V_b	Blocking voltage
V_{db}	Blocking voltage of the diode
θ_{S1}	Starting angle
θ_{S2}	Ending angle
Θ	Phase angle between grid voltage and current

Chapter

1

INTRODUCTION

Chapter 1

Introduction

1.1. Background

In the present scenario, renewable power generation is emerging to meet the increased energy demands due to dwindling conventional energy sources. On the other hand, an extensive scale of burning fossil fuels has a huge impact on environmental pollution, global warming, and climate change. In such conditions, the people are showing much interest in renewable power generation. There are wide varieties of renewable energy sources like solar, wind, fuel cell, hydro, and biomass, etc. In recent years, photovoltaic (PV) power generation is growing at a rapid rate as per the study carried by International Energy Agencies (IEA). The growth of PV power generation is exponential as depicted in Fig. 1.1 [1]. This is mainly due to the falling prices of PV materials, technology development in the production of large scale manufacturing of PV modules, deployable at any location with suitable placement of PV arrays, improvement of semiconductor technology, and associate inverter or converter topologies [2]. Thus, the investment in the solar PV industry has a significant share in the market over the other sources of renewable energy.

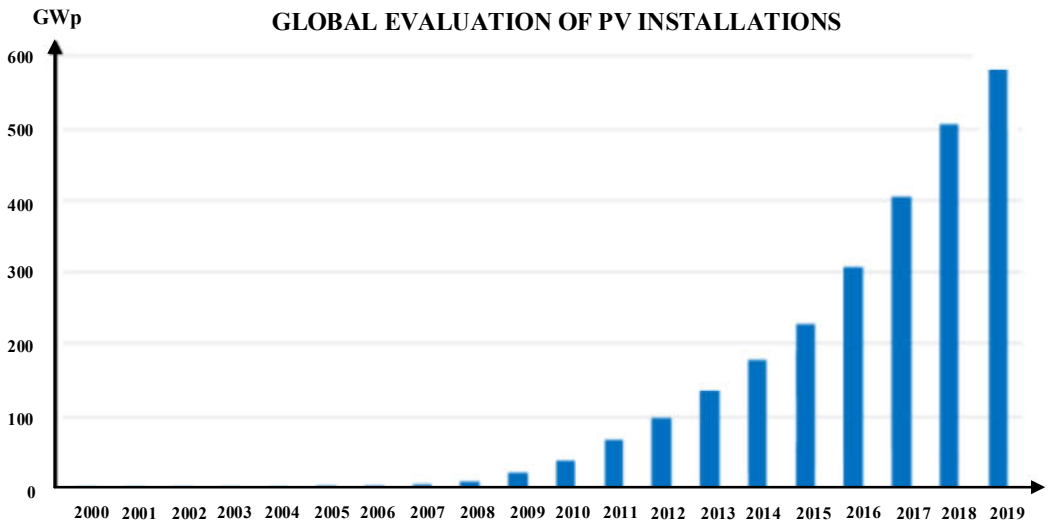


Fig. 1.1. Global evaluation of PV installations.

Moreover, grid-connected PV power generation is more popular because they do not need energy storage devices. Also, it can inject power into the grid when there is no local demand. Lithium-ion and lead-acid batteries are generally used as storage devices in standalone PV systems which reduce the reliability of PV systems, increase the overall operation and maintenance cost and also require additional controllers for charging and discharging.

Therefore, grid-connected PV power generation occupies 90% of the total share in the PV market in comparison with the standalone systems [3]. In this context, various grid-connected PV power generation systems (PVPGS) are developed to convert the direct current (DC) generated from the PV source to alternating current (AC) as per the standards and specifications of the grid. However, the need for reduced device count, lower leakage current and better quality of output waveforms motivate further research on this arena. Different technologies employed for the PVPGS, PV inverter topologies, leakage current issue in non-isolated inverters, and standards of grid-connected PV inverters are described in the forthcoming sections.

1.2. PV Power Generation Systems

In general, the grid-connected PVPGS are classified into four important categories named as a module, string, multi-string, and central inverters based on the maximum power point tracking (MPPT) and power generating capacity as shown in Fig. 1.2 and the same is compared in Table. 1.1. The brief description of all the PVPGS are as follows [4]-[5];

1.2.1. Module Inverters

Module inverters are developed to mitigate problems like partial shading, voltage mismatch, and uneven aging. Generally, they are arranged at the backside of each PV panel due to its smaller size and compact design known as micro-inverter. The micro-inverters provide the highest flexibility for the extension of PV power generation with the simplest modular structure. Further, these inverters are subdivided into two categories such as AC module and DC-optimizer as shown in Fig. 1.2(a) and (b) respectively. In the AC module application, a single

PV panel is integrated with the grid by the use of a high voltage gain inverter or with an additional DC-DC converter as shown in Fig.1.2(a).

Conversely, in the DC optimizers, each PV module consists of a separate DC-DC converter for boosting the low PV voltage to higher DC-link voltage and to enable the module-level MPPT. Further, outputs of all the DC-DC converters form a high voltage DC bus that is connected to a central grid-connected inverter. In all the micro-inverters, the number of power converters in a fully distributed system increases due to their per module architecture. Since the possibility of module-level MPPT, low PV system installation effort, easy monitoring, and failure detection, module inverters are useful for complex roof structures, small systems, or a combination of different roof orientations.

1.2.2. String Inverters

The string inverter is depicted in Fig. 1.2(c), where a single string of PV modules is connected to the inverter for interfacing the PV power into the grid. They can be subdivided into single-stage and two-stage topologies based on the addition (or not) of DC-DC converter for voltage boosting. String inverter registers less MPPT efficiency in comparison with the AC module inverter under partial shading condition. Conversely, for the PVPGS of the same power rating, the string inverter has more efficiency and lower cost per watt. The string inverter is popular for small and medium scale PVPGS, especially for rooftop PV plants.

1.2.3. Multi-String Inverters

To improve the flexibility and MPPT performance of the string inverter, the multi-string inverter is developed and is shown in Fig. 1.2(d). In this system, the strings are divided into smaller groups and connected through an independent DC-DC converter, all such groups are then connected to the single central inverter. The additional DC-DC converter is used to attain better MPPT performance and to boost the output PV voltage to high DC-link voltage. Thus, the overall energy extraction from the PV source is improved and the control complexity is reduced in comparison with the string inverters. The multi-string inverters are suitable for both medium and large-scale PV power plants due to the reduced effect of partial shading and voltage mismatching.

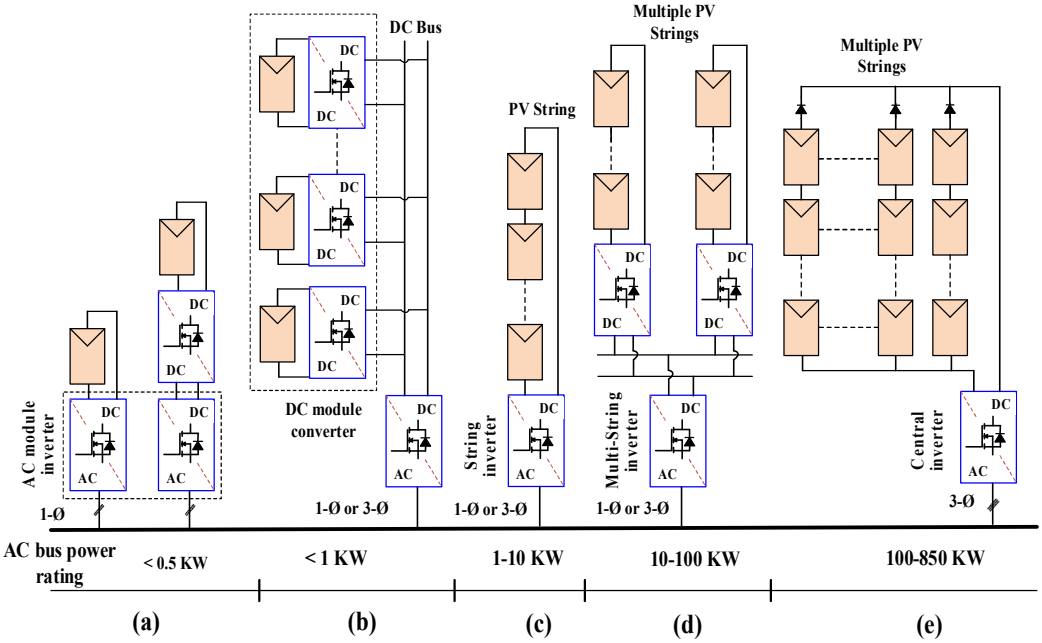


Fig. 1.2. Grid-connected PVPGS technologies: (a) AC module, (b) DC Optimizer, (c) String inverter, (d) Multi-String inverter, and (e) Central inverter.

Table 1.1 Overview of grid-connected PVPGS

Inverter type	Module	String	Multi-String	Central
Power range	< 1 KW	< 10 KW	< 500 KW	< 850 KW
Devices	Mosfet	Mosfet, IGBT	Mosfet, IGBT	IGBT
MPPT Type	Module	Large string	Small string	Array
Converter efficiency	Lowest (up to 96.5%)	High (up to 97.8%)	High (up to 98%)	Highest (up to 98.6%)
Positive features	* Flexible/Modular * Easy installation * Plug-play type * Highest MPPT efficiency	* Reduced DC wiring * Transformerless (very common) * Good MPPT efficiency	* Flexible/ Modular * Low cost for multiple string systems * High MPPT efficiency	* Simple structure * Highest converter efficiency * Reliable
Negative features	* High cost per watt * Two-stage system is mandatory * High losses	* High component count * One string, one inverter	* Two-stage is mandatory	* Needs blocking diodes * Poor MPPT performance * Not flexible
Examples	Siemens SMIINV215R60 and Power One aurora MICRO - 0.3-I	Danfoss DLX 4.6 and ABB PVS 300	SMA SB5000TL and SATCON Solstic	SMA MV Power Platform and 1.6 Siemens SINVERT PVS630

1.2.4. Central Inverters

The central inverter is depicted in Fig. 1.2(e), where a single inverter is interfaced with a whole PV array to the grid. The PV array is composed of series-connected PV modules (called a string) to produce a sufficiently higher voltage. These series connections are then connected in parallel based on the current requirement. A blocking diode is connected in series to each PV string to avoid the reverse flow of current under partial shading or voltage mismatch occurs. Also, only a global MPPT is possible in this configuration due to a single inverter connected to the whole PV array, which leads to the lowest MPPT efficiency of all PVPGS. But, it provides a simple structure, reliable, and efficient converter, making it one of the most common solutions for large scale PVPGS.

1.3. Classification of PV Inverter Configurations

From the above discussion, it is observed that either a single central inverter (i.e., single-stage) or an inverter with front-end DC-DC converter (i.e., two-stage) are being used with the grid-connected PVPGS. Generally, an additional DC-DC converter is used prior to the inverter for extracting maximum power from the PV source and for boosting the low PV voltage to higher DC voltage. The number of PV modules which are connected in series are less in two-stage inverter in comparison with the single-stage inverter to overcome the effects due to partial shading and module mismatch. Whereas, the two-stage inverter requires more number of passive components and power electronic devices for boosting and inversion operations, which results in increased component count and reduced efficiency. Since, both of the single-stage and two-stage inverters have their own merits and demerits; hence they will optimally selected based on the power generating capacity. In both cases, galvanic isolation from the leakage current is a major challenge to solve the safety and reliability issues of grid-connected PVPGS. To address this issue, PV inverters are further sub-classified into four groups based on the placement of isolation transformer in the power conversion circuit and they are explained as follows [6]-[7]:

1.3.1. Single-Stage Isolated Inverter Configuration

This topology comprises a DC-AC inverter and a line frequency transformer (LFT) as shown in Fig. 1.3. The LFT step-up the low voltage to medium voltage and also provides the galvanic isolation from the PV source to the grid. It is the earliest and popular topology in almost all central inverter based PVPGS. Nevertheless, the bulky LFT has several disadvantages such as low power density, low efficiency, higher power losses, and increased cost of the overall system.

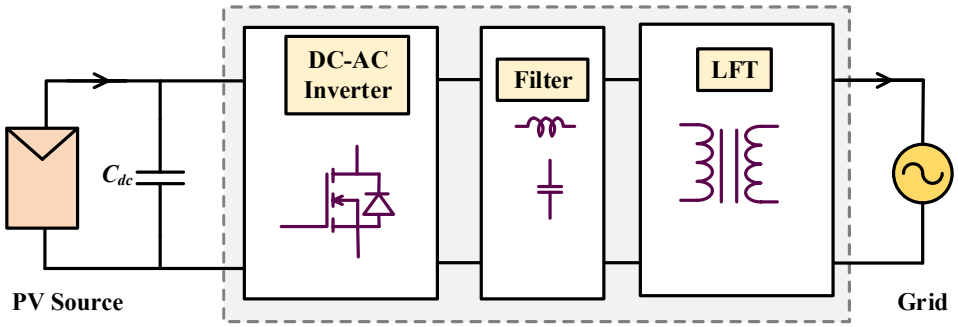


Fig. 1.3. Single-stage isolated inverter configuration.

1.3.2. Single-Stage Non-Isolated Inverter Configuration

The single-stage non-isolated inverter configuration is commonly known as transformerless inverter (TLI) configuration. To overcome the drawbacks associated with bulky LFT, it is eliminated from the power circuit as shown in Fig. 1.4. However, removal of the transformer yields a direct connection between PV inverter and the grid. Consequently, the common-mode voltage (CMV) fluctuations produced by the inverter can excite the PV parasitic capacitance and causes the flow of leakage current from the grid to PV module. This increases electro-magnetic interference (EMI), total harmonic distortion (THD), and also decreases the reliability and operational safety. To overcome these drawbacks several types of transformerless inverter topologies and different pulse width modulation (PWM) schemes were proposed in the literature. Thus, a negligible amount of leakage current is attained without the use of a transformer in the power circuit and also achieving the highest power density and efficiency. Therefore, these inverter topologies draw more attention from the researchers, industries, and policy makers to design and develop for grid-connected string and multi-string PVPGS.

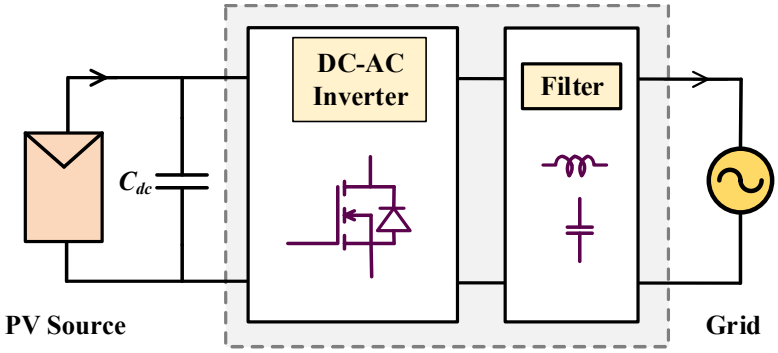
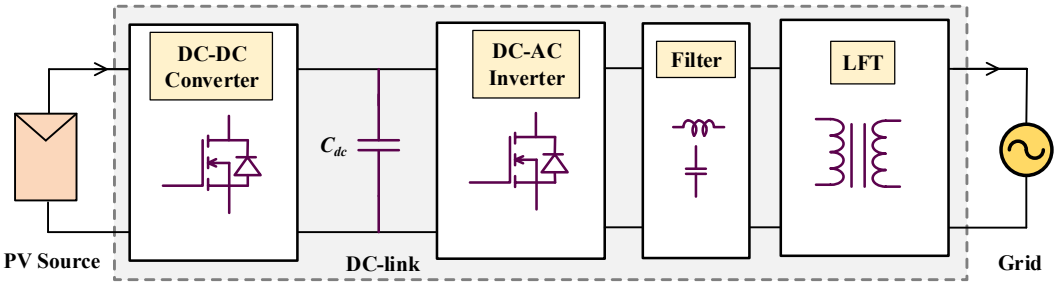


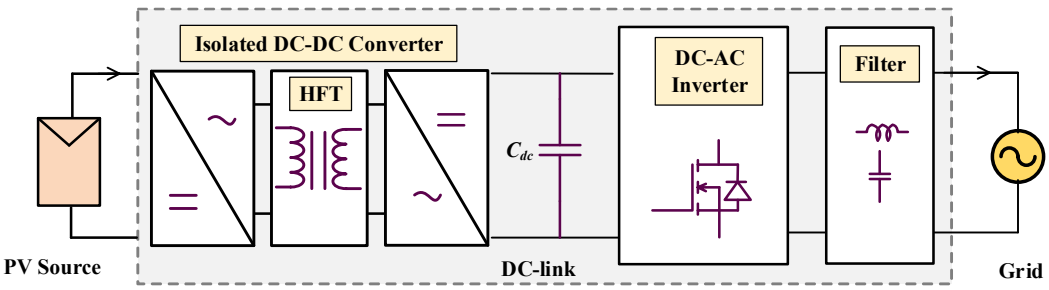
Fig. 1.4. Single-stage non-isolated inverter configuration.

1.3.3. Two-Stage Isolated Inverter Configuration

In this category, an LFT or a high-frequency transformer (HFT) is placed between the PV panel and the utility grid for providing isolation from the leakage current as shown in Fig. 1.5. Generally, an LFT is placed at the grid side and HFT is placed in the DC side as shown in Figs. 1.5(a) and (b) respectively. The use of a transformer in either way for realizing the galvanic isolation has a great effect on power conversion efficiency and power density of the grid-connected PV system.



(a)



(b)

Fig. 1.5. Two-stage isolated inverter configuration with: (a) LFT and (b) HFT.

Moreover, the cost, size, and weight of the transformer will increase in proportion with the power rating of the system. In comparison with the LFT based isolation, HFT based isolation offers reduced size, weight, and cost of the overall power conversion system. However, the incorporation of HFT in the DC-DC converter stage increases the number of power processing stages which further results in reduced efficiency. Typically, the inverter topologies with HFT in the power conversion stage are used in module inverters.

1.3.4. Two-Stage Non-Isolated Inverter Configuration

In this topology, both LFT and HFT are eliminated to reduce the power losses, size, weight, and cost of the overall PV power conversion system as depicted in Fig. 1.6. Moreover, the removal of the transformer from the power conversion system improves efficiency and power density. Hence, these inverter configurations are more popular for multi-string and AC module applications. However, the elimination of the transformer causes a flow of leakage current from the grid to PV source. Addressing the issue of leakage current and voltage amplification in the grid-connected PVPGS, without the use of a transformer is a new challenge for the researchers and industries to obtain the benefits of high efficiency and high power density.

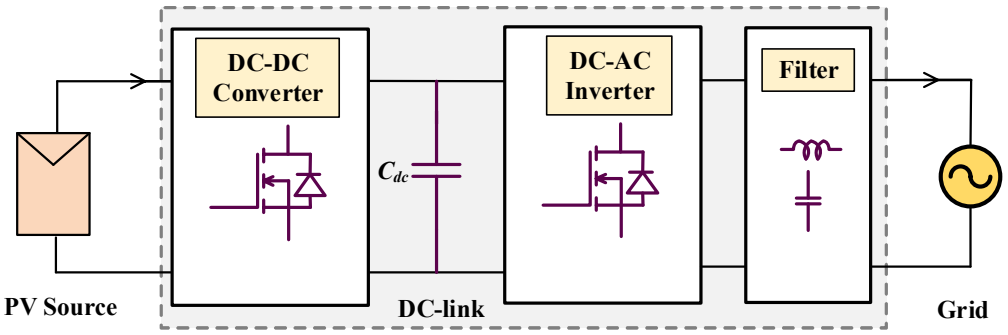


Fig. 1.6. Two-stage non-isolated inverter topology.

1.4. Analysis of Leakage Current in Non-Isolated Inverter Topologies

As per the above survey, the advantages derived by the elimination of transformer from the power conversion stage has drawn more attention of the researchers. However, removal of the transformer yields a direct connection between PV inverter and grid. In this context, a resonant circuit is formed with the

parasitic capacitances among PV module and ground, filter inductors and grid impedances. This results in the flow of leakage current between the PV module and stand-alone load/grid through the PV parasitic capacitance (C_{PV}). The flow of leakage current increases EMI, THD, and power losses, and also decreases the reliability and operational safety.

Generally, the leakage current path is created among PV modules and ground due to the existence of parasitic capacitance (C_{PV}) between the aluminium frame and solar cell, glass and solar cell of the PV module as shown in Fig. 1.7 [8]. The value of C_{PV} is mainly dependent on the surface area of the PV cell, the distance between the PV cell and frame, atmospheric conditions, dust, humidity, etc. Thus, the value of C_{PV} is not constant and it varies with respect to the environmental conditions. The typical value of C_{PV} varies between several picofarads to few microfarads. The current flowing through the C_{PV} is called leakage current. Moreover, the magnitude of leakage current flowing mainly depends on the value of C_{PV} and variations in the total common-mode voltage (V_{TCMV}) as shown in (1.1).

$$i_{leakage} = C_{PV} \frac{dV_{TCMV}}{dt} \tag{1.1}$$

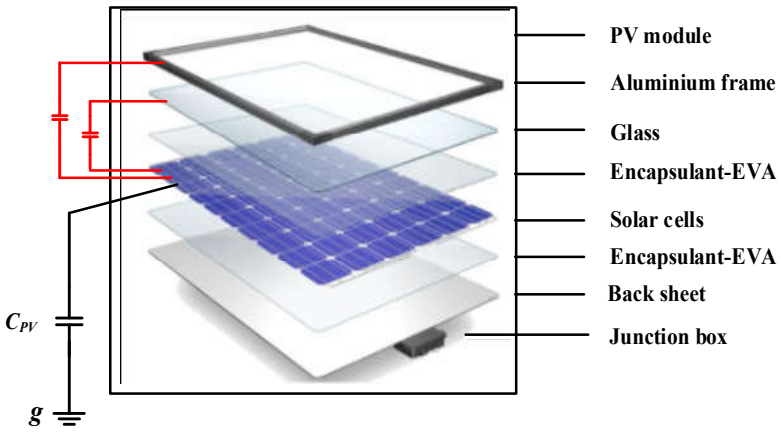


Fig. 1.7. Parasitic capacitance of the PV module.

The analysis for finding the total voltage variations in CMV is explained as follows; the typical structure of non-isolated inverter configuration with most significant stray elements is illustrated in Fig. 1.8, where positive and negative terminals of the input PV source are denoted with *P* and *N, A* and *B* are the output terminals of the inverter respectively. As per the definitions, the common-mode

voltage 'V_{CM}' and differential-mode voltage 'V_{DM}' are expressed in terms of inverter terminal voltages V_{AN} and V_{BN} as follows;

$$V_{DM} = V_{AN} - V_{BN} \tag{1.2}$$

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2} \tag{1.3}$$

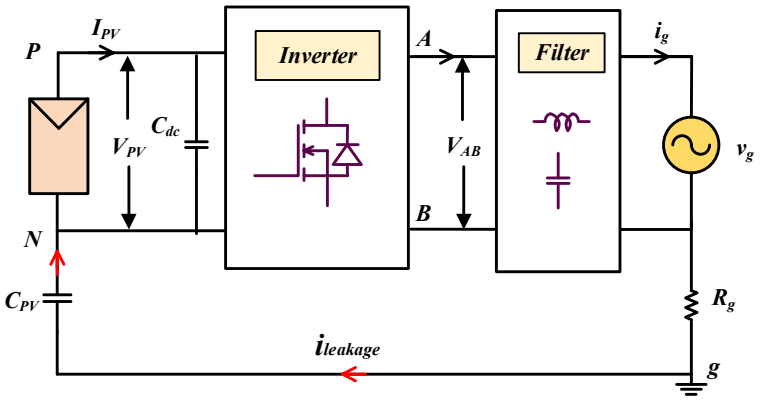


Fig. 1.8. Typical structure of non-isolated inverter configuration with most significant stray elements.

From the analysis given in ref [9], it is concluded that the V_{CM} may have a clear influence on the leakage current generation. The additional CMV ($V_{CM\text{-}DM}$), which is transformed from the V_{DM}, is derived by

$$V_{CM-DM} = V_{DM} * \frac{L2 - L1}{2 * (L2 + L1)} \tag{1.4}$$

From (1.4), the V_{DM} with asymmetrical filter inductors ($L1 \neq L2$) may have some contributions to the CMV, resulting in additional leakage current. The total high-frequency common-mode voltage V_{TCMV} can be evaluated by

$$V_{TCMV} = V_{CM} + V_{CM-DM} = \frac{V_{AN} + V_{BN}}{2} + \frac{V_{AN} - V_{BN}}{2} \frac{L2 - L1}{(L2 + L1)} \tag{1.5}$$

If, $L1$=0, V_{TCMV} is simplified by

$$V_{TCMV} = \frac{V_{AN} + V_{BN}}{2} + \frac{V_{AN} - V_{BN}}{2} = V_{AN} \tag{1.6}$$

If, $L2=0$, V_{TCMV} is simplified by

$$V_{TCMV} = \frac{V_{AN} + V_{BN}}{2} + \frac{V_{AN} - V_{BN}}{2} = V_{BN} \tag{1.7}$$

Where, the inverters are asymmetrical inductor configuration (i.e., $L1$=0 or $L2$=0), the necessary and sufficient condition to eliminate the leakage current is that the inverter terminal voltage V_{AN} or V_{BN} keeps constant.

If, $L1=L2=L/2$, V_{TCMV} is simplified by

$$V_{TCMV} = \frac{V_{AN} + V_{BN}}{2} = V_{CM} \tag{1.8}$$

Once the inverters are with symmetrical inductor configuration ($L1=L2$), the necessary and sufficient condition to eliminate the leakage current is that the V_{TCMV} has no high-frequency variation. Usually, these high-frequency oscillations depend on the topology structure and modulation scheme employed for the switching of the inverter. In this context, several solutions were given in the literature either by improving the structure of the topology or by the PWM scheme.

1.5. Multilevel Inverter Technology

In recent days, multilevel inverters (MLIs) are emerging in the area of grid-connected PVPGS because of their significant advantages like high quality of power output by lowering the THD, reduced losses with the reduction in voltage stress of the switches, reduced filter size with increased modularity. It is much more advantageous to have such benefits in non-isolated PV inverter topologies along with a reduction in leakage current. The popular MLI configurations are neutral-point clamped (NPC), flying capacitor (FC) and cascaded H-bridge (CHB) inverters as depicted in Fig. 1.9 [10]. The limitations of these MLIs are more device count, DC voltage balancing issues and control complexity for an increased number of levels. A detailed review, classification, and description of different MLI topologies are presented in the references [11]-[12]. Most of the topologies presented in the literature use classical structures such as NPC, FC, CHB, and their variants.

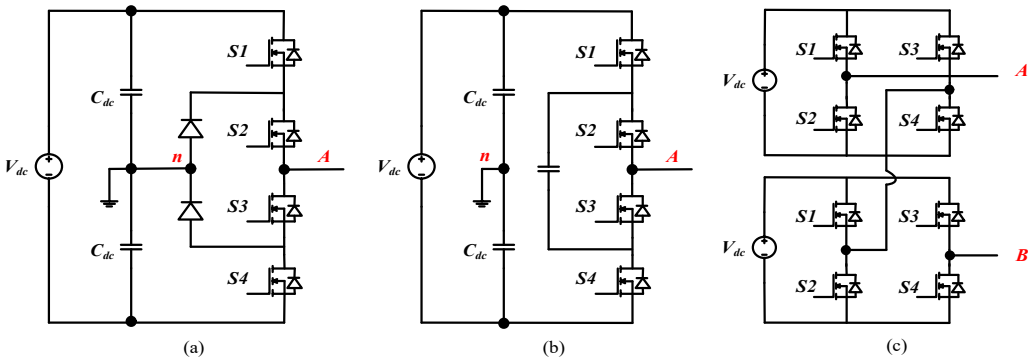


Fig. 1.9. Classical multilevel inverter topologies: (a) Neutral-point clamped, (b) Flying capacitor and (c) Cascaded H-bridge.

However, some common limitations are stopping the usage of aforesaid MLIs directly into the grid-connected PVPGS as follows:

- Requirement of isolated DC sources and complex control schemes to obtain the DC-link capacitor voltage balancing for realizing the multilevel output voltage.
- Uni-directional current flow from source to the grid will deteriorate the waveform quality during reactive power region which results in increased THD.
- Increased high-frequency oscillations in V_{TCMV} causes the higher magnitude of leakage current.
- Increased power losses due to more number of switching devices.

Therefore, to address the aforesaid limitations, the present research is focusing on the development of new MLI topologies with improved modulation schemes. Moreover, the design and development of any new inverter for grid-connected PVPGS should meet the standards specified by the national and international agencies as explained below.

1.6. Important Standards Dealing with the Grid-Connected PVPGS

The main objective of the PV inverter is to extract maximum power from the PV module and inject sinusoidal current in the grid/stand-alone load. To ensure better system performance and reliable operation, the newly developed

interfacing inverter should fulfil the standards of PV systems. The standards are normally imposed by different international regulation authorities like the Institute of Electrical and Electronics Engineers (IEEE), the International Electro-technical Commission (IEC) and the Association for Electrical, Electronic, and Information Technologies (VDE). In the case of grid-connected operation of PV inverters, these standards deal with some important aspects, such as isolation from the flow of leakage current due to PV parasitic capacitances, THD, reactive power capability [13]-[15].

1.6.1. Leakage Current

Isolation from the flow of leakage current is one of the most important requisites for PV inverters. The parasitic capacitance formed between the PV module and ground creates a path to leakage current and it will increase EMI, THD and power losses, and also decreases the reliability and operational safety. Because of all these effects, various standards were imposed on the PV inverters, which deals with the magnitude of leakage current flowing through the PV module. One of the standards among them is VDE 01260-1-1. As per this standard, the magnitude of leakage current should not exceed 300 mA (peak). Therefore, all the commercially available PV inverters should meet VDE 01260-1-1 standard.

1.6.2. Total Harmonic Distortion

To regulate the undesirable effects due to THD of PV inverters, the international regulations such as IEEE 1547, IEC 61727 and IEC61000-3-2 standards imposed a limit on THD. According to these limits, the harmonic content in the injected current should be less than 5%. Moreover, these standards also provide a maximum limit of 1% of DC injection; whereas VDE 01260-1-1 allows a maximum DC of 1 A. The THD of the injected current can be minimized by designing suitable filters circuit, improving the modulation techniques applied to the inverter and also by employing multilevel inverter concept. Some of the most significant harmonic contents specified by the IEEE 1547 standard are listed in Table. 1.2.

Table 1.2 IEEE 1547 THD standard for grid-connected PVPGS

Harmonic order, h	5	7	11	13	17	19	23	25	Overall THD (%)
IEEE 1547 Harmonic Voltage THD (%)	4	4	2	2	1.5	1.5	0.6	0.3	<5

1.6.3. Reactive Power Capability

To allow the high penetration of PV power into the grid, the next generation of PV inverters should provide enough reactive power support similar to the conventional power plants. In recent days, almost every international standard has imposed that a definite amount of reactive power should be handled by the grid-connected PV inverter. According to VDE-AR-N-4105, grid-connected PV inverter of power rating below 3.68 KVA, should attain power from 0.95 lagging to 0.95 leading. Therefore, a newly designed inverter should give reactive power support without affecting the waveform quality.

Table 1.3 BIS / IEC standards for grid-connected PV inverters in India

S.No	Parameter		Range	
1	**DC current injection**		< 0.5% of rated current	
2	**Harmonics** (IEC 61000-3-2)		< 5% at rated inverter output	
3	**Voltage deviations**	Voltage (% Un)	Ride trough until	Maximum response time
		V < 50%Un	1.7s	1.8s
		50% Un ≤ V < 85%	3s	3.1s
		110% Un < V < 120%	2s	2.1s
		120% Un < V < 130%	0.2s	0.3s
		V > 130% Un	-	0.05s
4	**Power factor**		± 0.8 (for inductive and capacitive with an accuracy of ± 0.01)	
5	**Leakage current** IEC62109-2		Power rating up to 30KVA must disconnect within 0.3sec when the measure rms leakage current greater than 300mA	

*Un – Nominal voltage

1.6.4. Standards and recommended practices for grid-connected inverters in India

The Ministry of New and Renewable Energy (MNRE) is monitoring the quality control of PVPGS under the Bureau of Indian Standards (BIS). The main theme of these standards is to give the performance benchmark for the PV modules, PV inverters and batteries used in the PVPGS. In the case of grid-connected inverters IS 16221 – Part II and IS 16169 are specified to cover safety requirements and islanding prevention measures respectively. Both the standards are adopted from International Electro-technical Commission (IEC). Some of the important regulations imposed on DC current injection, THD, voltage deviation and operating power factor are given in Table. 1.3.

1.7. Summary

From all the above discussions; it is observed that the design of inverters with the reduced component count and without the isolation transformer is a new trend in both single-stage and two-stage inverter topologies for grid-connected PVPGS. Moreover, the integration of MLIs will enhance the performance of the power converter and improves waveform quality. Hence, the researchers, industries, and research & development sectors are focusing very much in this area to explore different possible solutions by designing novel inverter configurations with improved PWM techniques.

To align with this trend and to made significant contributions in this field, the following research work is carried out based on the investigation on single-phase voltage source based inverter topologies for grid-connected PVPGS with the objectives of increased efficiency by reducing device count and by the elimination of isolation transformer, and improved output waveform quality by adopting multilevel inverter technology. In this context, seven interesting solutions are proposed for both single-stage (four topologies) and two-stage (three topologies) operations in grid-connected PVPGS.

Chapter 2

LITERATURE SURVEY

Chapter 2

Literature Survey

2.1. Introduction

Photovoltaic power generation systems (PVPGS) is the most promising solution to meet world energy requirements. As per the renewable energy status report [16], the total capacity of 583.5 GW solar power generating units were installed by the end of 2019, out of which the majority (90%) is the grid-connected system. This significant diffusion of PVPGS into the electric grid effectively mitigates the poisonous gas emission and global warming issues due to the reduction in the utilization of conventional fossil fuels. Nevertheless, existing PV technologies such as poly-crystalline or mono-crystalline semiconductor based PV modules can only achieve maximum efficiency of 15% and 18%, respectively. Therefore, transferring power effectively for various applications in agricultural, residential and grid-connected systems becomes challenging due to changes in solar irradiation, changes in operating temperatures, partial shading and grounding issues. A lot of investigation is going in terms of PV material design, power electronic interfacing circuits and control schemes. Finding solutions to achieve minimum device counts, minimum leakage current and reduced control complexity will enhance the overall reliability and efficiency of the PVPGS. In general, the grid-connected PVPGS consists of a PV source, an inverter and a passive filter circuit to feed the generated AC power into the utility grid.

Inverter plays a crucial role in the grid-connected PVPGS, which are further categorized into voltage source inverters (VSIs) and current source inverters (CSIs). In the present work, VSI based power converters have been considered as they have much higher employment due to their merits of low cost, simple control and mature technology [17]. The VSIs are normally categorized into isolated type and non-isolated type based on the placement of the transformer in the power processing stage. A bulky line frequency transformer (LFT) in the AC grid side or a compact high frequency transformer (HFT) in the DC source side is usually employed to provide the galvanic isolation between the PV source

and grid. Besides the galvanic isolation, it also step-up the low PV output voltage. Eventually, the use of a transformer in either way declines the efficiency, power density and enhances the size, cost of the system [18].

To alleviate the above-said problems, both LFT and HFT are eliminated from the power processing stage in non-isolated inverters. However, removal of the transformer yields a direct connection between inverter and PV module. In consequence, a resonant circuit is formed with the parasitic capacitances among PV module and ground, filter inductors and grid impedances. The total common mode voltage (V_{TCMV}) fluctuations produced by the inverter can excite this resonant circuit and causes the flow of leakage current from the grid to the PV module through PV parasitic capacitance. Also, it will increase EMI, THD and power losses and also decreases the reliability and operational safety. Therefore, various topologies and PWM schemes have been proposed to reduce the leakage current to meet the grid regulatory standards and also enhance the overall efficiency [19].

This chapter presents a detailed review of existing single-phase inverter topologies for grid-connected PVPGS. Further, a comprehensive study of both single-stage and two-stage topologies are carried out based on the reduction of leakage current. Also, a thorough comparison has been formulated in terms of active and passive component count, leakage current magnitude, common mode voltage (CMV) behavior, reactive power control capability and output levels, to identify the suitable configurations. For simplicity of drawings, the PV module is modeled as an equivalent DC source throughout this chapter.

2.2. Classification of the Single-Stage Transformerless Inverter Topologies

All the topologies proposed in the literature employed two different approaches for the reduction of leakage current. One such method is to accomplish a solid connection between the AC circuit to the DC circuit (i.e., bypassing the PV parasitic capacitance). While the other method is to eliminate the high-frequency oscillations in V_{TCMV} (i.e., with additional power electronic circuitry). Fig. 2.1 depicts a classification of some important single-stage transformerless inverter (TLI) topologies in two major groups based on the

placement of filter inductor and they are named as asymmetrical ($L1=L_f$, $L2=0$) and symmetrical ($L1=L2=L_f/2$) type TLIs. Moreover, the symmetrical type TLIs are further categorized into four sub-groups based on the selection of additional decoupling and clamping circuits to reduce the leakage current. Those are, DC decoupling without clamping, DC decoupling with clamping, AC decoupling without clamping and AC decoupling with clamping [20]-[21].

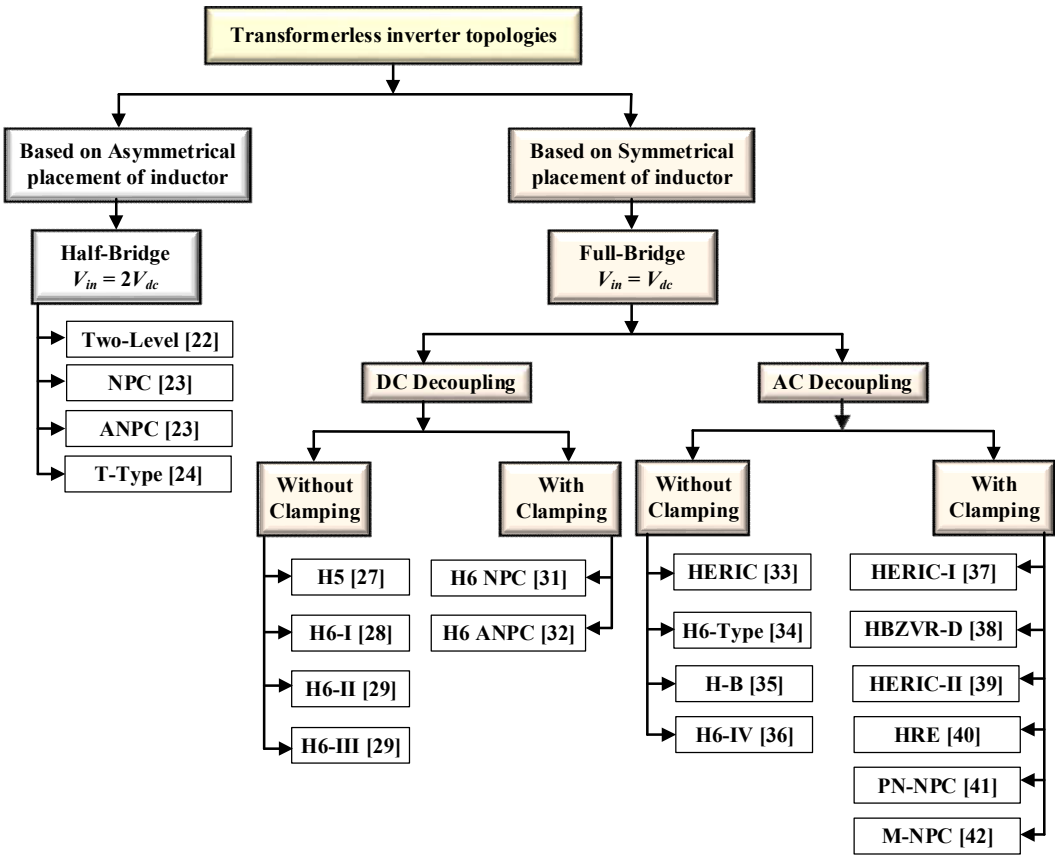


Fig. 2.1 Classification of single-stage TLI topologies based on inductor placement.

In asymmetrical type TLI topologies, a solid connection is established between the grid neutral to the terminal *O* (mid-point of two capacitors). Hence the V_{TCMV} is kept constant. Consequently, the magnitude of leakage current is completely negligible. Based on the half-bridge concept, a simple two-level inverter with two power semiconductor switches is developed in [22], to eliminate the leakage current as shown in Fig. 2.2(a). However, the total DC-link voltage and the voltage stress of the semiconductor switches should be twice the grid peak voltage. Also, the bipolar output voltage of the inverter increases the filter size and cost. To overcome these drawbacks, the three-level neutral point clamped (NPC) inverter can be employed as shown in Fig. 2.2(b), where the dynamic voltage

balance of the switches is achieved by the clamping diodes. One of the major problems of NPC topology is the unbalanced conduction losses among the semiconductor switches. By replacing the passive diodes with two semiconductor switches, the active NPC (ANPC) is derived and it is shown in Fig. 2.2(c) [23].

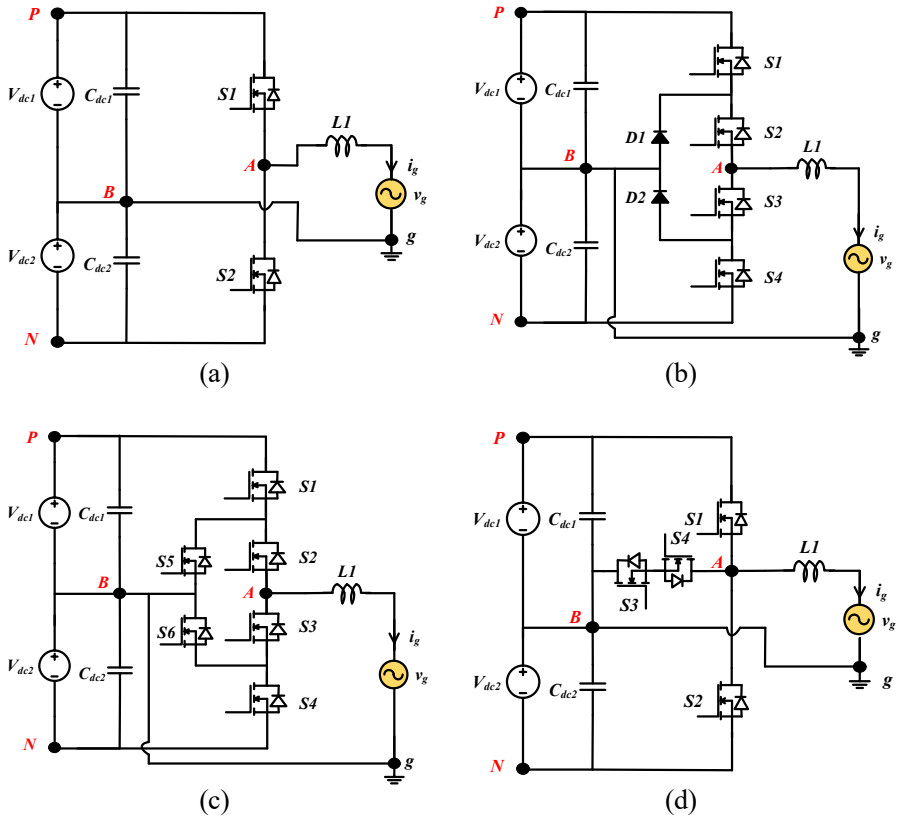
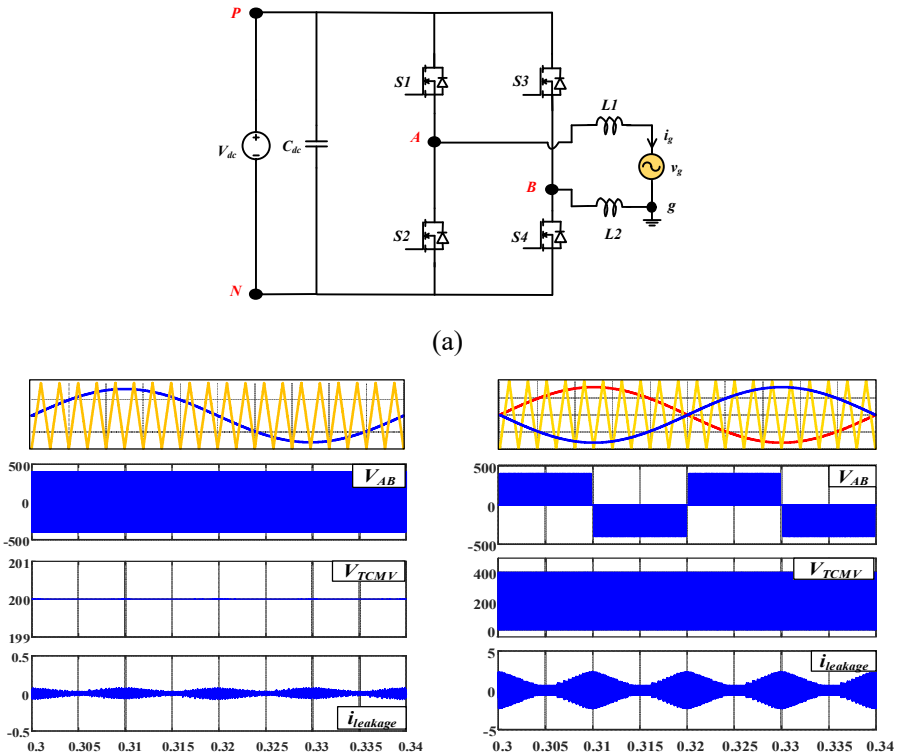


Fig. 2.2. Asymmetrical inductor based TLI topologies: (a) Two-level inverter, (b) Three-level NPC inverter, (c) Three-level ANPC inverter and (d) Three-level T-Type inverter.

Because of the controllable clamping branch, abundant switching patterns and freewheeling current paths are available for the ANPC inverter. Consequently, conduction losses are distributed uniformly and the reactive power control capability can easily be provided. Nevertheless, due to the conduction of two switches at any switching operation for NPC or ANPC topologies results in considerable losses in the low-voltage applications. To get more advantages from asymmetrical three-level inverter topologies and to reduce the power losses in low-voltage applications, the T-type inverters are proposed by Kolar et al., as shown in Fig. 2.2(d) [24]. Where a common-drain connected bi-directional switches are placed between the mid-point of the half-bridge inverter and split DC-link capacitors to attain a similar three-level output voltage generation in the NPC or ANPC inverters.

One of the major drawbacks in all the half-bridge topologies is the requirement of high input DC voltage to meet the grid peak voltage. But, the output voltage of the PV module is relatively low. Hence it is necessary to connect more PV modules in series to meet the high input DC voltage. It can decrease the power output generated by the PV modules due to the partial shading and module mismatch, especially in the urban areas.

Further, to reduce the requirement of high input DC voltage, a full-bridge (F-B) inverter with bipolar PWM (BPWM) and unipolar PWM (UPWM) schemes are introduced in the early stage of symmetrical filter inductor based topologies [25]. In the case of BPWM, two-level voltage ($+V_{DC}$, $-V_{DC}$) is generated by switches *S1* and *S4* during positive half-cycle, *S2* and *S3* during negative half-cycle. Also, it generates constant V_{TCMV} and less leakage current as shown in Fig. 2.3(b). However, the terminal voltage (V_{AB}) step is twice the input DC voltage, which results in increased THD, EMI noise and switching losses. On the other hand, in the case of F-B inverter with UPWM, the V_{AB} step is halved to reduce the EMI noise, THD and inductor size as shown in Fig. 2.3(c). But, it fails to limit the leakage current due to high-frequency oscillations in V_{TCMV}.



(a)

(b) (c)

Fig. 2.3. (a) Full-bridge inverter, (b) Bipolar PWM, (c) Unipolar PWM.

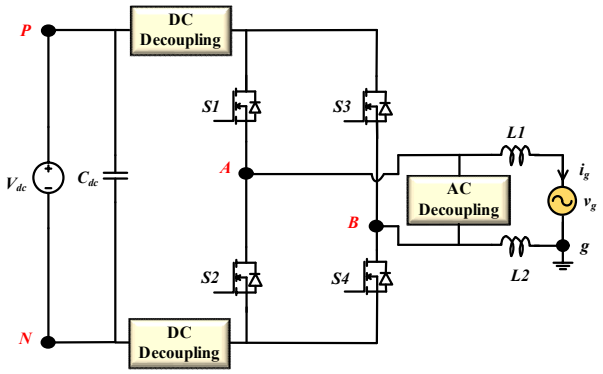


Fig. 2.4. Full-bridge inverter with decoupling network.

Therefore, both of the PWM schemes with conventional F-B inverter are not satisfying the grid codes and standards. One of the critical reasons for high-frequency oscillations in V_{TCMV} with the UPWM scheme is due to the fact that either positive or negative terminal of the DC source is connected to the freewheeling path during zero voltage state. This can be avoided by providing a decoupling network to the F-B inverter using additional circuitry as shown in Fig. 2.4. Based on this concept, many topologies and patented solutions are proposed in the literature to achieve the advantages of both BPWM and UPWM schemes (*i.e.,* higher efficiency and the lower leakage current).

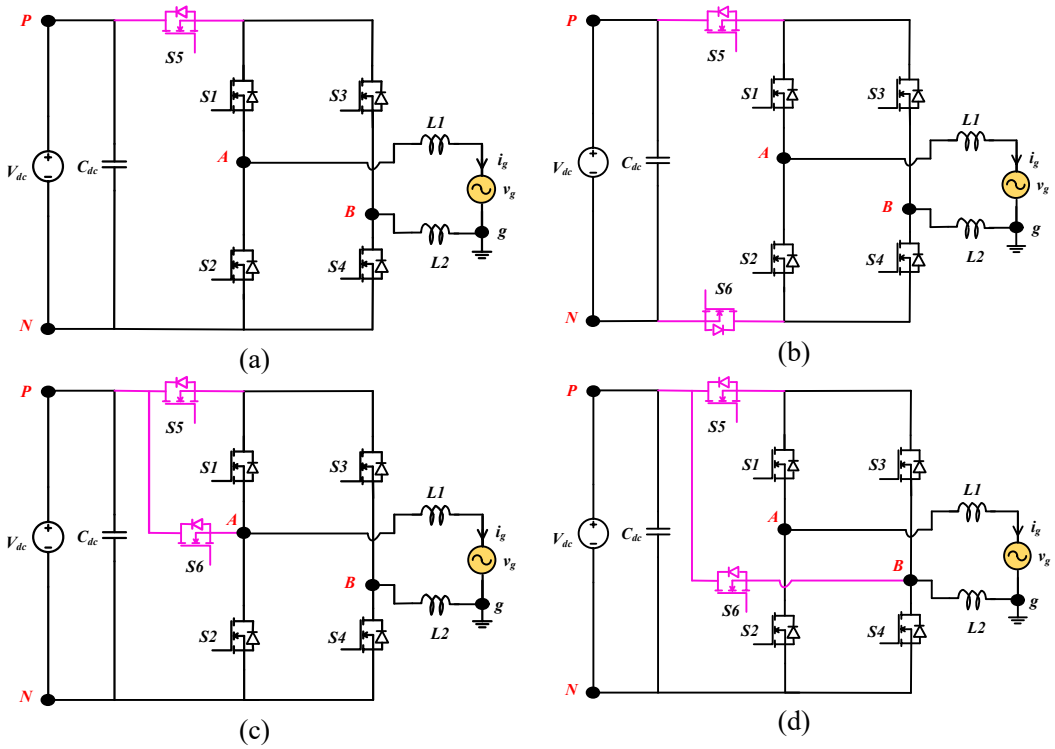


Fig. 2.5. DC decoupling based: (a) H5 inverter, (b) H6-I inverter, (c) H6-II inverter and (d) H6-III inverter.

In DC decoupling based inverter topologies, an additional decoupling network is placed between the DC source and F-B module to provide isolation during the freewheeling state [26]. One such solution proposed by Victor *et al.* and patented by SMA solar technology. Switch *S5* is inserted between the positive terminal and F-B module to act as a decoupling network, which is the well-known H5 TLI as depicted in Fig. 2.5(a) [27]. The operation is almost similar to the F-B inverter except for zero level, where switch *S5* is turned-OFF to provide isolation from the grid. However, switch *S5* operates at a double frequency in comparison with other switches, which results in unbalanced power losses. Also, it increases the burden of heat-sink design and reduces the power density.

To balance the power losses occurring due to decoupling switch, one more switch *S6* is inserted between the negative terminal and F-B module known as H6 TLI and it is depicted in Fig. 2.5(b) [28]. However, the power losses are increased due to the conduction of four switches during power transferring modes. To reduce the conduction losses, position of the *S6* can be changed, as shown in Figs. 2.5(c) and (d) and it is known as improved H6 TLI topologies [29]. The operations of all these topologies are quite similar except for the freewheeling period. Moreover, the loss distribution of the decoupling switches also balanced by improving the topology structure. However, in practice, the junction capacitance of the switches alters from 100 pF-10 nF [30], which cannot be ignored. Also, it causes more oscillations in the CMV and results in the flow of excess leakage current. Therefore, the decoupling circuit alone cannot preserve constant V_{TCMV} in all the operating modes of the inverter.

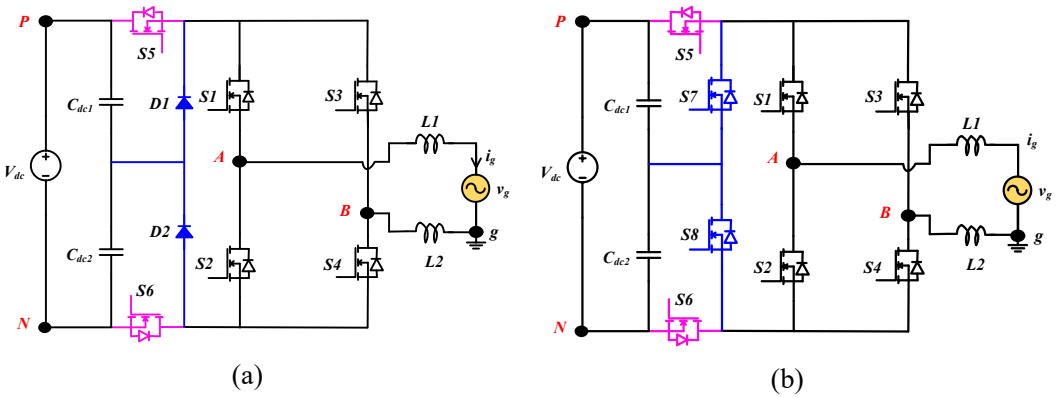


Fig. 2.6. DC decoupling based (a) Passive clamped NPC H6 inverter and (b) ANPC H6 inverter.

To alleviate the leakage current problems and to improve the waveform quality in an optimized way, passive or active clamping branches with split DC-link capacitors should be inserted between the DC source and F-B module. Which can preserve a defined and constant CMV also diminishes the effect of switch junction capacitors during the freewheeling period. In this circumstance, Azary *et al*., proposed a modified H6 TLI topology [31] by inserting two passive diodes between the split DC-link capacitors and the F-B module as shown in Fig. 2.6(a). During the freewheeling period the switch *S5* and *S6* are turned-OFF and diodes *D1*, *D2* clamps the terminal voltage to half of the DC-link voltage. Further, the clamping of CMV can also be provided by inserting the two active switches between the mid-point of DC capacitors and the F-B module, known as ANPC H6 or as shown in Fig. 2.6(b) [32]. However, the DC decoupling and clamping operations require more number of devices in the conduction, which results in increased component count, power losses and reduced efficiency.

Conversely, the same functions can also be achieved with AC based decoupling inverter topologies, where the decoupling network is inserted between the F-B module and filter inductors to provide isolation during the freewheeling period. A highly efficient and reliable inverter concept (HERIC) was first invented in the year 2003 [33], which is formed by inserting two active switches (*S5* and *S6*) between the F-B module and the symmetrical filter inductors, as shown in Fig. 2.7(a). Conduction of the switches *S5* and *S6* depends on the grid voltage polarity during the freewheeling period. If grid voltage polarity is positive, the switch *S5* and the body diode of *S6* will conduct, else the switch *S6* and body diode of *S5* will conduct to decouple the source from the grid. Conduction losses of the HERIC inverter is less in comparison with the DC decoupled topologies because only two devices are in conduction at any operating state.

Based on the similar principle, some of the other AC decoupled based topologies are derived as illustrated in Figs. 2.7(b) and (c). An H6 TLI topology is proposed in [34], where AC side decoupling is achieved by conducting switch *S4* and diode *D1* or switch *S3* and *D2* during the freewheeling period based on the grid voltage polarity. Further, a hybrid-bridge [35] (H-B) TLI is derived based on H6 TLI. The placement of bi-directional switch is the only difference between the H6 and H-B topologies.

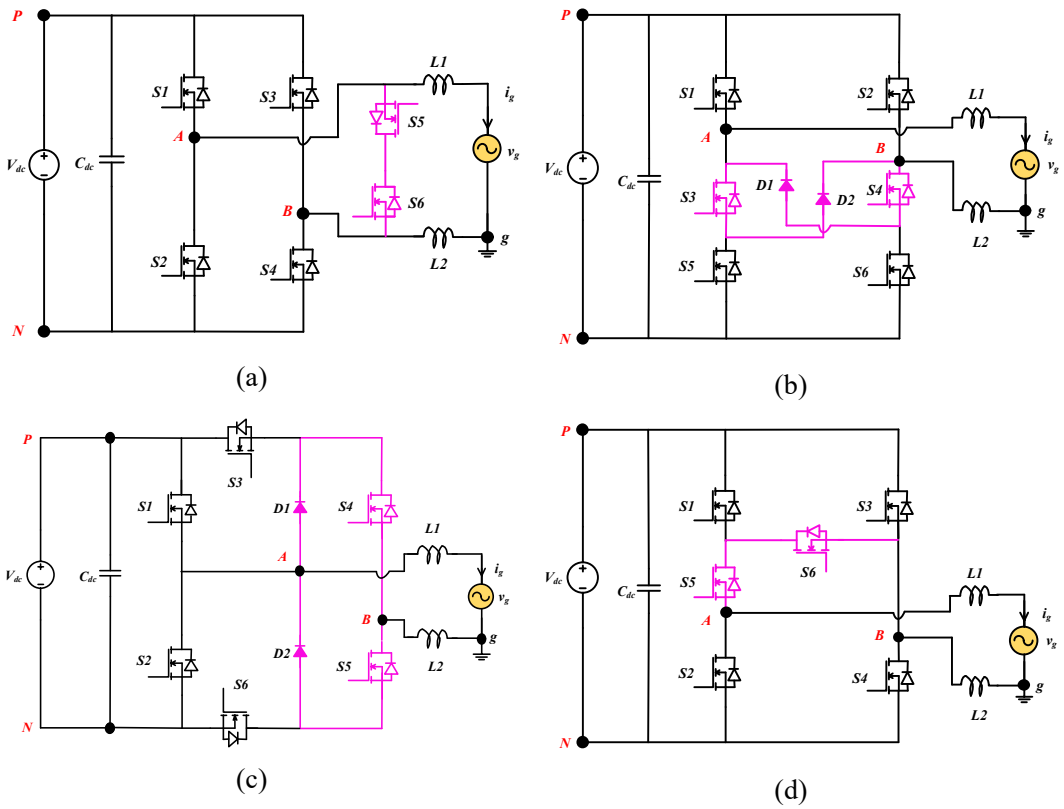


Fig. 2.7. AC decoupling based: (a) HERIC, (b) H6, (c) Hybrid-bridge and (d) H6-IV.

Hence, the PWM schemes, operating modes, power losses and leakage current analysis are quite similar. Another AC decoupled TLI topology is proposed in [36], by changing the position of a bidirectional switches as illustrated in Fig. 2.7(d). But, the switching and conduction losses of all three derived topologies are high in comparison with the HERIC inverter due to more number of switches are in conduction during the power transferring modes. However, the effect of switch junction capacitors is not considered in all the AC decoupling based topologies as above-mentioned, which results in high-frequency oscillations in V_{TCMV}. Consequently, excess leakage current can flow in the resonant circuit formed due to the PV parasitic capacitance.

In this circumstance, different HERIC based TLI topologies were proposed to clamp the terminal voltages to half of the DC-link voltage during the freewheeling period. Senjun *et al*., proposed a passive clamping based derived HERIC topology by inserting two diodes between the mid-point of DC-link capacitors and the drain of the active switch *S5* and *S6* respectively, as illustrated in Fig. 2.8(a) [37]. By providing the gate pulses to active switches *S5* and *S6* simultaneously, the CMV is clamped to half of the DC-link voltage. An H-bridge

zero voltage state rectifier–diode (HBZVR-D) topology [38] is shown in Fig. 2.8(b) is another solution, where one switch and six diodes are used for both AC decoupling and passive clamping respectively. An active switch *S5* is tuned-ON during the freewheeling period to decouple the inverter, at the same time the diodes clamps the terminal voltages of the inverter to half of the DC-link voltage based on the current direction.

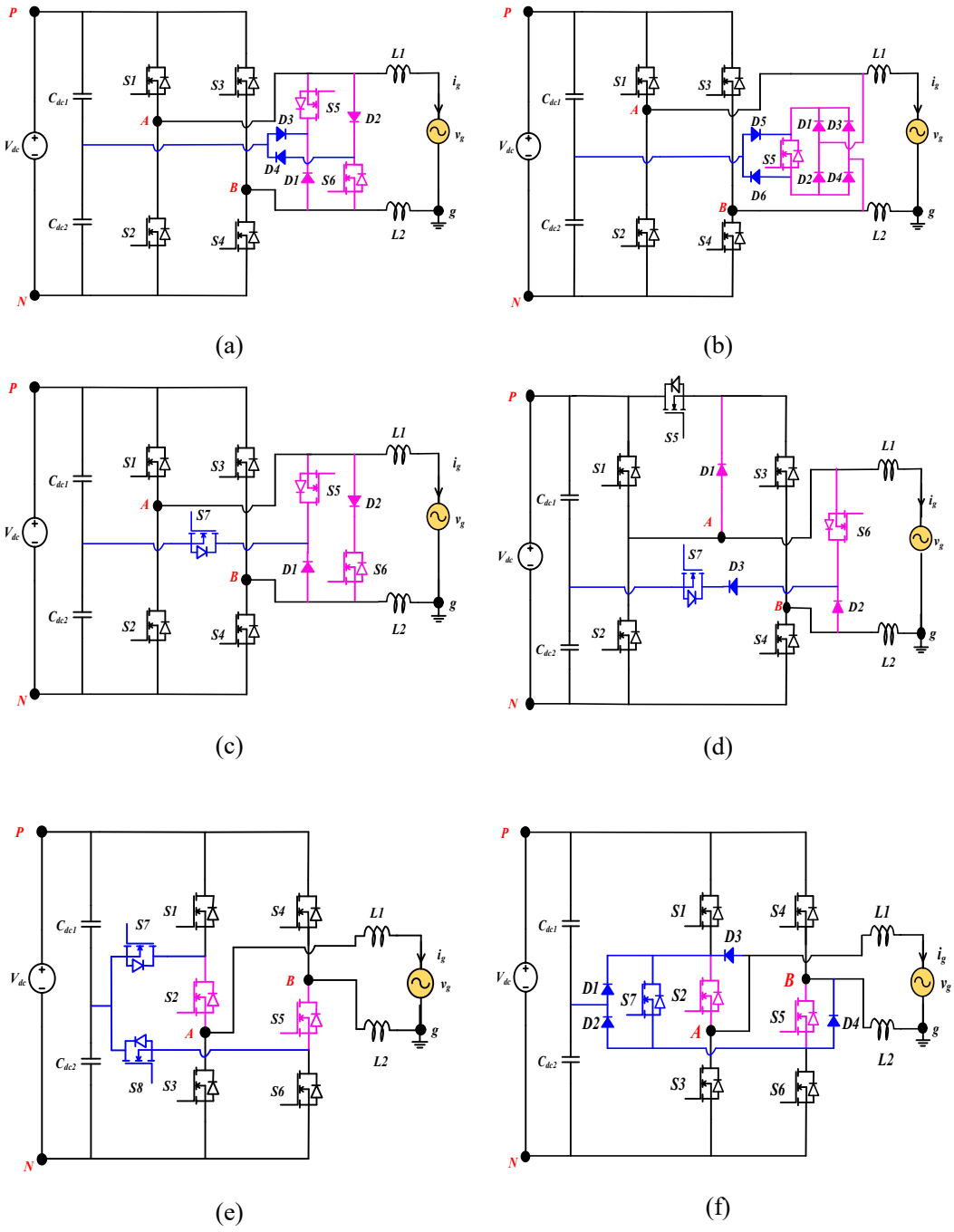


Fig. 2.8. AC decoupling based: (a) Passive clamped HERIC-I, (b) HBZVR-D, (c) Active clamped HERIC-II, (d) HRE, (e) PN-NPC and (f) M-NPC.

A similar operation can also be achieved by active clamping as shown in Fig. 2.8(c) [39], where one active switch is inserted between the DC-link capacitors and the bi-directional branch (formed by connecting a MOSFET in series with diode). By turning-ON both clamping and bi-directional switches, the CMV is clamped to half of the DC-link voltage. Similarly, a family of modified F-B TLI topologies are proposed to obtain AC decoupling and active clamping, by adding extra switches and diodes, named as highly reliable and efficient (HRE) inverter [40], positive and negative neutral point clamped converter (PN-NPC) [41] and Mosfet-neutral point clamped converter [42] (M-NPC) as depicted in Figs. 2.8(d)-(f) respectively. The primary object of all the aforementioned topologies is to achieve both AC decoupling and CMV clamping with highest possible efficiency.

Table 2.1 Comparative assessment of single-stage TLI topologies.

Topology	Input Voltage	Component Count						Advantages	Disadvantages
		C_{dc}	M	D	L_f	C_f	TDC		
Two-level [22]	$2*V_{dc}$	2	2	0	1	1	2	• Constant CMV • Negligible leakage current • Reactive power capability	▪ Input voltage is double the grid-peak voltage ▪ Two-level output ▪ More switching losses
NPC [23]	$2*V_{dc}$	2	4	2	1	1	8	• Constant CMV • Negligible leakage current • Reactive power capability	▪ Input voltage is double the grid-peak voltage ▪ Uneven distribution of conduction losses
ANPC [23]	$2*V_{dc}$	2	6	0	1	1	8	• Constant CMV • Negligible leakage current • Reactive power capability • Uniform distribution of conduction losses	▪ Input voltage is double the grid-peak voltage
TNPC [24]	$2*V_{dc}$	2	4	0	1	1	6	• Constant CMV • Negligible leakage current • Reactive power capability • Higher efficiency in comparison with NPC, ANPC	▪ Input voltage is double the grid-peak voltage
F-B BPWM [25]	V_{dc}	1	4	0	2	1	4	• Constant CMV • Negligible leakage current • Reactive power capability	▪ Two-level output ▪ More switching losses ▪ Higher THD
F-B UPWM [25]	V_{dc}	1	4	0	2	1	8	• Lower THD in comparison with BPWM	▪ Oscillatory CMV ▪ Higher leakage current
H5 [27]	V_{dc}	1	5	0	2	1	10	• Lower component count	▪ Oscillatory CMV due to switch junction capacitances ▪ Medium leakage current ▪ Unity power factor only

H6-I [28]	V_{dc}	1	6	0	2	1	12	• Even distribution of the power losses in comparison with the H5	▪ Oscillatory CMV due to switch junction capacitances ▪ Medium leakage current ▪ Unity power factor only
H6-II [29]	V_{dc}	1	6	0	2	1	10	• Lower and evenly distributed power losses in comparison with the H6-I	▪ Oscillatory CMV due to switch junction capacitances ▪ Medium leakage current ▪ Unity power factor only
H6-III [29]	V_{dc}	1	6	0	2	1	10	• Lower and evenly distributed power losses in comparison with the H6-I	▪ Oscillatory CMV due to switch junction capacitances ▪ Medium leakage current ▪ Unity power factor only
NPC-H6 [31]	V_{dc}	2	6	2	2	1	16	• Constant CMV • Negligible leakage current	▪ More component count and Higher power losses ▪ Unity power factor only
ANPC-H6 [32]	V_{dc}	2	8	0	2	1	16	• Constant CMV • Negligible leakage current	▪ More component count and Higher power losses ▪ Unity power factor only
HERIC [33]	V_{dc}	1	6	0	2	1	8	• Highly efficient	▪ Oscillatory CMV due to switch junction capacitances ▪ Medium leakage current ▪ Unity power factor only
H6 [34]	V_{dc}	1	6	2	2	1	10	-----	▪ Oscillatory CMV due to switch junction capacitances ▪ Medium leakage current ▪ Unity power factor only
H-B [35]	V_{dc}	1	6	2	2	1	10	------	▪ Oscillatory CMV due to switch junction capacitances ▪ Medium leakage current ▪ Unity power factor only

H6-IV [36]	V_{dc}	1	6	0	2	1	9	------	▪ Oscillatory CMV due to switch junction capacitances ▪ Medium leakage current ▪ Unity power factor only
HERIC-I [37]	V_{dc}	2	6	4	2	1	10	• Constant CMV • Negligible leakage current	▪ More component count and higher power losses ▪ Unity power factor only
HBZVR-D [38]	V_{dc}	2	5	6	2	1	12	• Constant CMV • Negligible leakage current • Operability in all the power factors	▪ More component count and higher power losses
HERIC-II [39]	V_{dc}	2	7	2	2	1	11	• Constant CMV • Negligible leakage current	▪ More component count and higher power losses ▪ Unity power factor only
HRE [40]	V_{dc}	2	7	3	2	1	14	• Constant CMV • Negligible leakage current	▪ More component count and higher power losses ▪ Unity power factor only
PN-NPC [41]	V_{dc}	2	8	0	2	1	14	• Constant CMV • Negligible leakage current	▪ More component count and higher power losses ▪ Unity power factor only
M-NPC [42]	V_{dc}	2	7	4	2	1	14	• Constant CMV • Negligible leakage current	▪ More component count and higher power losses ▪ Unity power factor only

C_{dc} –DC capacitor, M –Mosfet, D –Diodes, L_f –Filter inductor, C_f - Filter capacitor, TDC - Total devices are in conduction during one complete cycle.

A brief comparative assessment of all the aforesaid single-stage TLI topologies is given in Table 2.1. In the half-bridge based topologies, both leakage current elimination and reactive power control capability is achieved by solid connection and bidirectional current paths provided by the body diodes of MOSFETs respectively. However, the requirement of high input DC voltage limits the application of Half-bridge topologies in PVPGS. In the F-B based TLI topologies, both decoupling and clamping branches are essential to eliminate the high-frequency oscillations from the V_{TCMV}, which results in the significant reduction of leakage current. However, all the F-B topologies and their PWM schemes are only reported to operate at unity power factor (UPF) condition of the grid. But, in modern days, reactive power capability of the TLI is much important to penetrate a large amount of PV power into the grid as per the VDE-AR-N4105 standard.

To fill the gap, Freddy *et al.,* [43] proposed an improved modulation technique for the basic H5 and HERIC inverter topologies. In addition to that, two different inverter topologies are also recommended in refs [44]-[45] to serve the functions of high efficiency and reactive power support with the increased component count. Nevertheless, clamping of the inverter terminal voltages during the freewheeling period is not considered in refs. [44]-[45], which results in more oscillations in V_{TCMV}. Consequently, excess leakage current will flow in the resonant circuit and it further increases the size of common mode filter (CMF). Further, increased component count and passive filters to realize the reactive power control will hike the overall cost and also enlarge the size of the system. Eventually, the three-level operation of all the topologies described above requires the larger filter size to lower the THD.

2.3. Classification of the Single-Stage Transformerless MLI Topologies

In contemporary, MLIs were introduced in both the medium and high power applications due to their advantages like the high quality of output power by lowering the THD, improved efficiency by reducing the voltage stress of the switches, reduced filter size and increased modularity. Therefore, it attracts the attention of both academia and industry now a days to have such benefits in PVPGS along with an ability of reduction in leakage current. Various inverter topologies were proposed in the literature to achieve both multilevel operation and leakage current elimination. The basic classification of all these topologies has been made based on the placement of filter inductors, as illustrated in Fig. 2.9. The asymmetrical filter inductor based topologies are further sub-classified into two

groups depends on the magnitude of input DC voltage to achieve 230V, 50 Hz grid frequency. The following section demonstrates the classification of various five-level TLI topologies based on the leakage current elimination and CMV analysis [46]-[48].

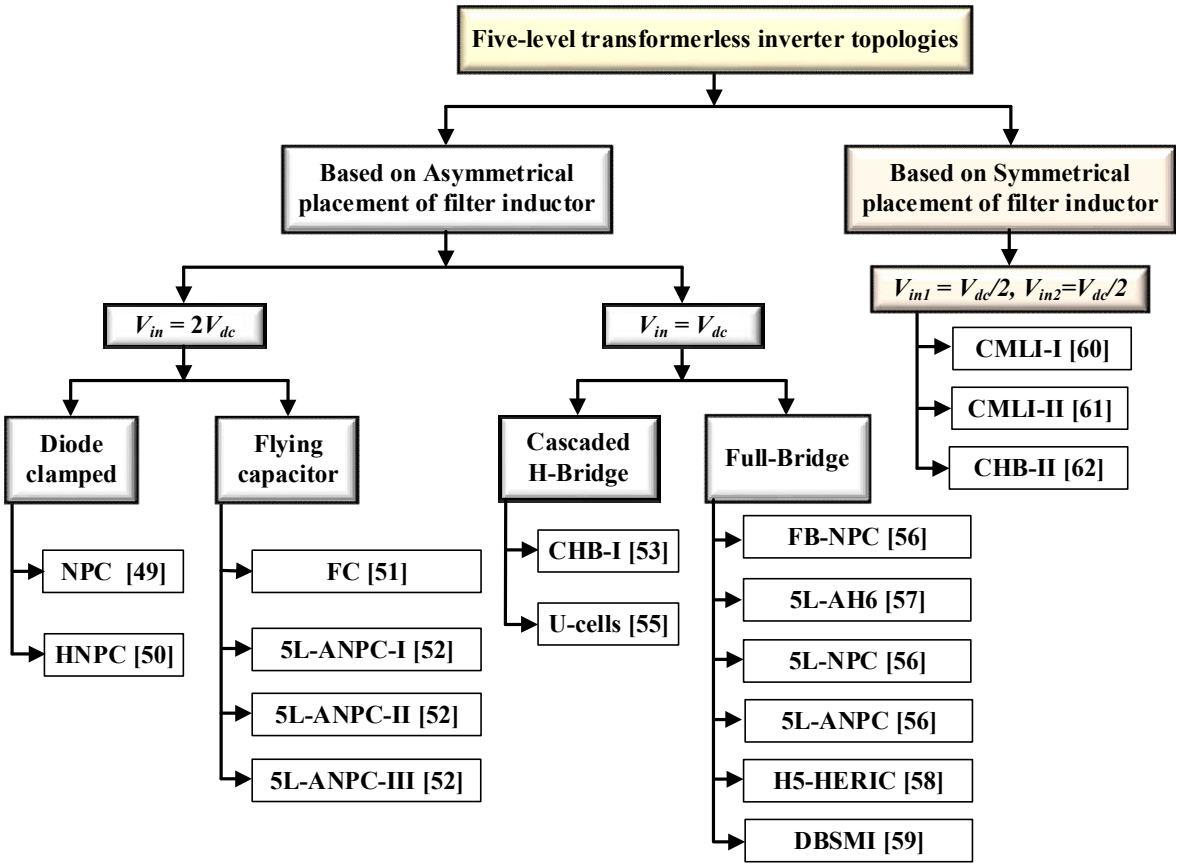


Fig. 2.9. Classification of the single-stage five-level TLI topologies based on inductor placement.

Fig. 2.10(a) illustrates one of the traditional diode clamped MLI, also known as NPC MLI, where the blocking diodes are used to generate the voltage levels from neutral point voltage [49]. The total number of blocking diodes, semiconductor switches and DC-link capacitors are increased in proportion with the number of voltage levels, which results in more power losses and DC-link capacitor voltage balancing issues. A hybrid NPC (HNPC) MLI is proposed in [50] and it is illustrated in Fig. 2.10(b). This topology achieves multilevel output with reduced number of diodes and also registers higher efficiency in comparison with the classical NPC MLI. Fig. 2.11(a) depicts another traditional FC based MLI topology, where the required output voltage levels are produced by summing the FC voltage and DC-link capacitor voltages. However, the FC MLI prerequisite a sophisticated control strategies to balance the capacitor voltages, lower

lifetime and higher maintenance cost due to the presence of an increased number of FCs and DC-link capacitors to generate higher voltage levels [51].

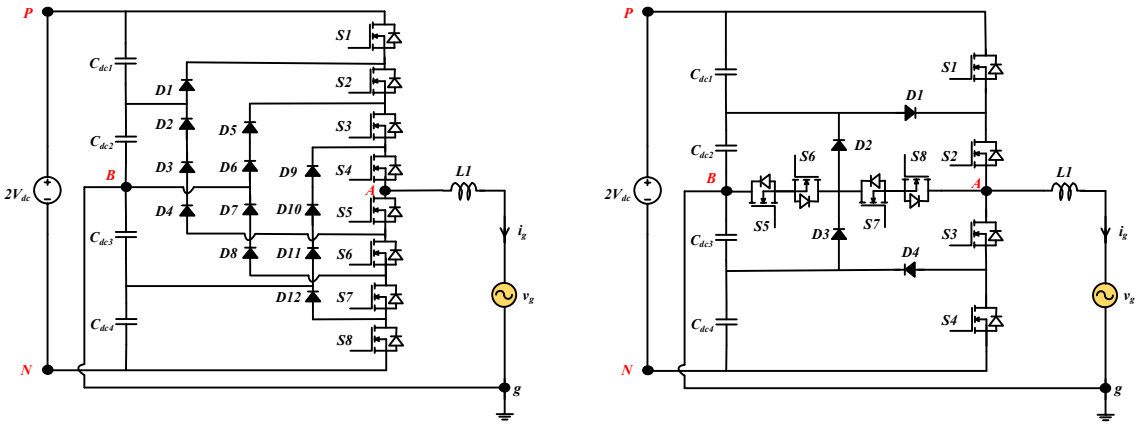


Fig. 2.10. (a) Diode clamped MLI, (b) HNPC MLI.

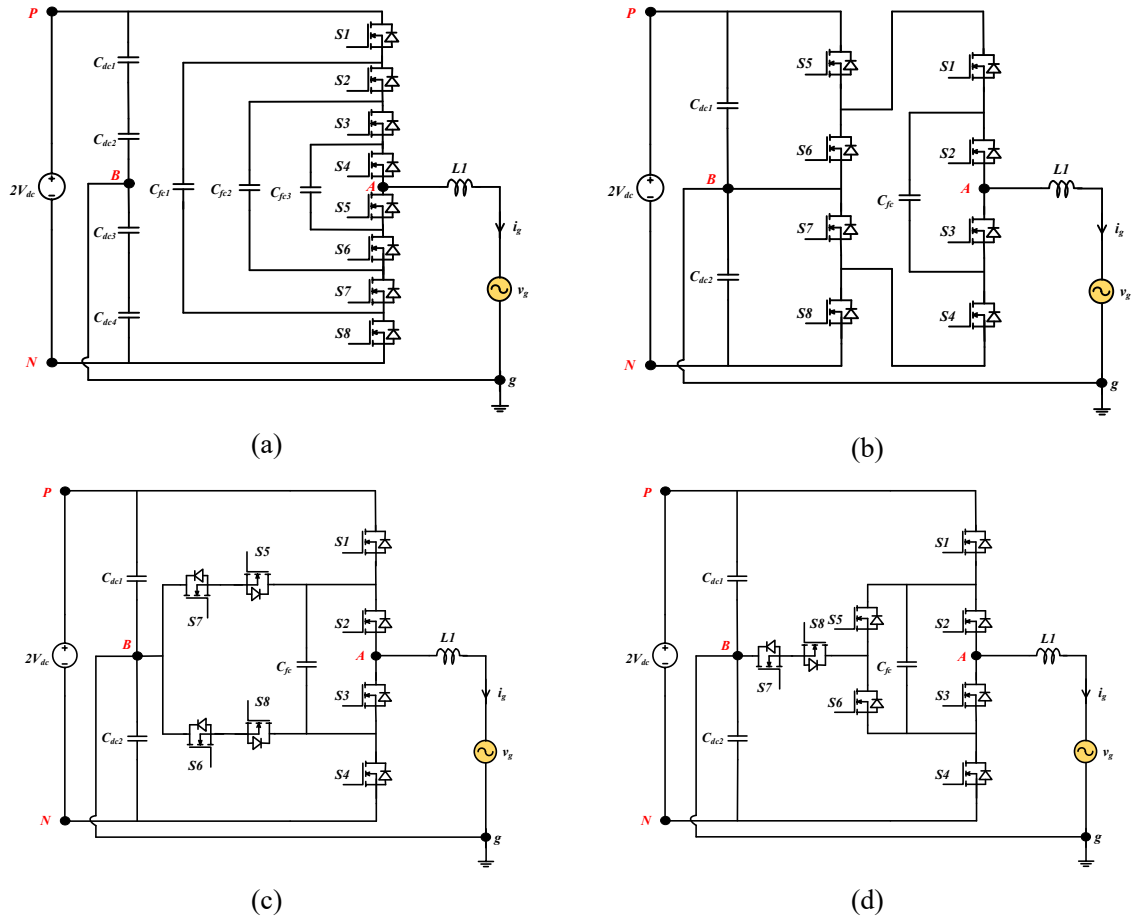


Fig. 2.11. (a) Flying capacitor MLI, (b) 5L-ANPC-I, (c) 5L-ANPC-II and (d) 5L-ANPC-III.

Therefore, to overcome the issues of both NPC and FC type MLIs, a hybrid structure of MLI is derived by combining the 3L-ANPC leg and a 3L-FC power cell, as

shown in Fig. 2.11(b), named as 5L-ANPC [52]. The number of voltage levels are increased with the levels produced by the FC. Moreover, the circuit structure offers a reduced number of capacitors and no series-connected diodes for generating the higher voltage levels, which results in higher efficiency and reduces control complexity to balance DC-link capacitor voltages. Figs. 2.11(c) and (d) are the additional 5L-ANPC topologies derived by replacing the position of 3L-ANPC. The leakage current magnitude is almost negligible in all the above-mentioned topologies, due to the establishment of a solid connection between the AC circuit and DC circuit (bypassing the PV parasitic capacitance). However, all these topologies require more number of PV modules in series to meet the grid peak voltage, which results in the reduction of the PV power output due to partial shading and module mismatch.

Further, to reduce the requirement of high input DC voltage, a traditional CHB MLI is derived by using H-bridge modules, as illustrated in Fig. 2.12(a) [53]. Where each module utilizes a separate DC source and they further connected in cascaded passion for realizing the multilevel output. However, the conventional sinusoidal level-shifted PWM (SLSPWM) for generating multilevel output introduces high-frequency oscillations in V_{TCMV} and which results in a higher magnitude of leakage current. Thus, a modified PWM strategy for traditional CHB MLI is proposed in [54], to eliminate the high-frequency oscillations in V_{TCMV} and also to reduce the corresponding leakage current. Nevertheless, the CHB MLI topology requires more number of semiconductor switches to realize the multilevel operation, which reduces the efficiency and increases the cost. Therefore, a reduced switch count packed U-cells based MLI topology is proposed in [55], as shown in Fig. 2.12(b). However, the employed PWM scheme unable to eliminate the high-frequency oscillations in V_{TCMV} and which results in a higher magnitude of leakage current. Besides, both the CHB and packed U-cells based topologies require isolated DC sources for generating the multilevel output and also demands a sophisticated control strategy to match the power balance between each PV source.

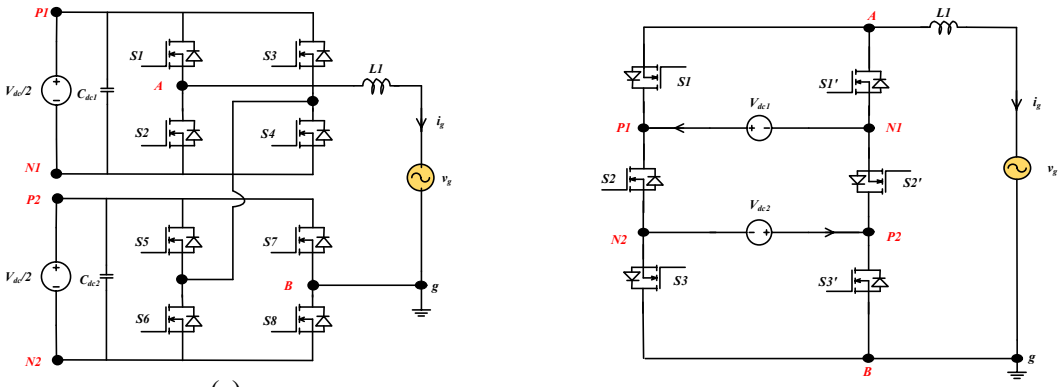


Fig. 2.12. Five-level (a) CHB-I inverter topology, (b) Packed U-cells inverter topology.

Therefore, in the recent works of literature, different F-B based five-level TLI topologies are proposed with a single DC source, as illustrated in Fig. 2.13. In all the F-B based five-level TLI topologies, the SLSPWM scheme is employed to balance DC-link capacitor voltages and thereby realizing the five-level output voltage. Also, the SLSPWM scheme provides a solid connection between the grid and positive or negative terminal of the source during the freewheeling period to limit the switching frequency oscillations in the terminal voltages (V_{AN}, V_{BN}) of the inverter. Further, the $V_{CM\text{-}DM}$ produced by the asymmetrical placement of filter inductor is utilized to nullify the high-frequency oscillation from V_{TCMV} (=V_{BN}) completely. Figs. 2.13(a) and (b) illustrate the FBNPC and active H6 (AH6) topologies proposed in [56]-[57] respectively. Both of these topologies can produce five-level output with a single DC source and also achieves the natural balancing of DC-link capacitor voltages with their PWM schemes.

However, these topologies suffer from the disadvantages of more component count and increased power losses due to the conduction of at least four devices in each mode of operation. Therefore, to reduce the power losses, a 3L-NPC leg is connected with a half-bridge leg to form a five-level NPC inverter, as shown in Fig. 2.13(c). Similarly, a 3L-ANPC leg is connected with a half-bridge leg to realize five-level ANPC inverter, as shown in Fig. 2.13(d). In both of these topologies [56], the number of conducting switches in a complete cycle is reduced in comparison with the FBNPC and AH6 type inverters. However, one of the main drawbacks of the 5L-NPC and 5L-ANPC topologies is the conduction of at least three devices during the freewheeling period. Thus, to further reduce the conduction of devices during the freewheeling period, two more F-B based asymmetrical TLI topologies are derived in [58]-[59], named as H5-HERIC and double bi-directional switch MLI (DBSMI) as shown in Figs. 2.13(e) and (f) respectively. In both of

these topologies, only two semiconductor switches are in conduction during the freewheeling period. Therefore, the overall efficiency of both H5-HERIC and DBSMI topologies are improved as compared with the other F-B based five-level TLI topologies. Eventually, in all the aforesaid F-B based five-level TLI topologies, there exist sudden transitions in V_{TCMV} from 'V_{PV}' to '*0*' and vice-versa with grid frequency variations, which results in a more significant spike in the leakage current. Sometimes, the peak value of the leakage current may exceed DIN VDE0126-1-1 grid standard because of the uncontrolled value of C_{PV} due to environmental conditions. Moreover, a bulky and expensive filter inductor is required to limit the high-frequency switching ripple in the grid current.

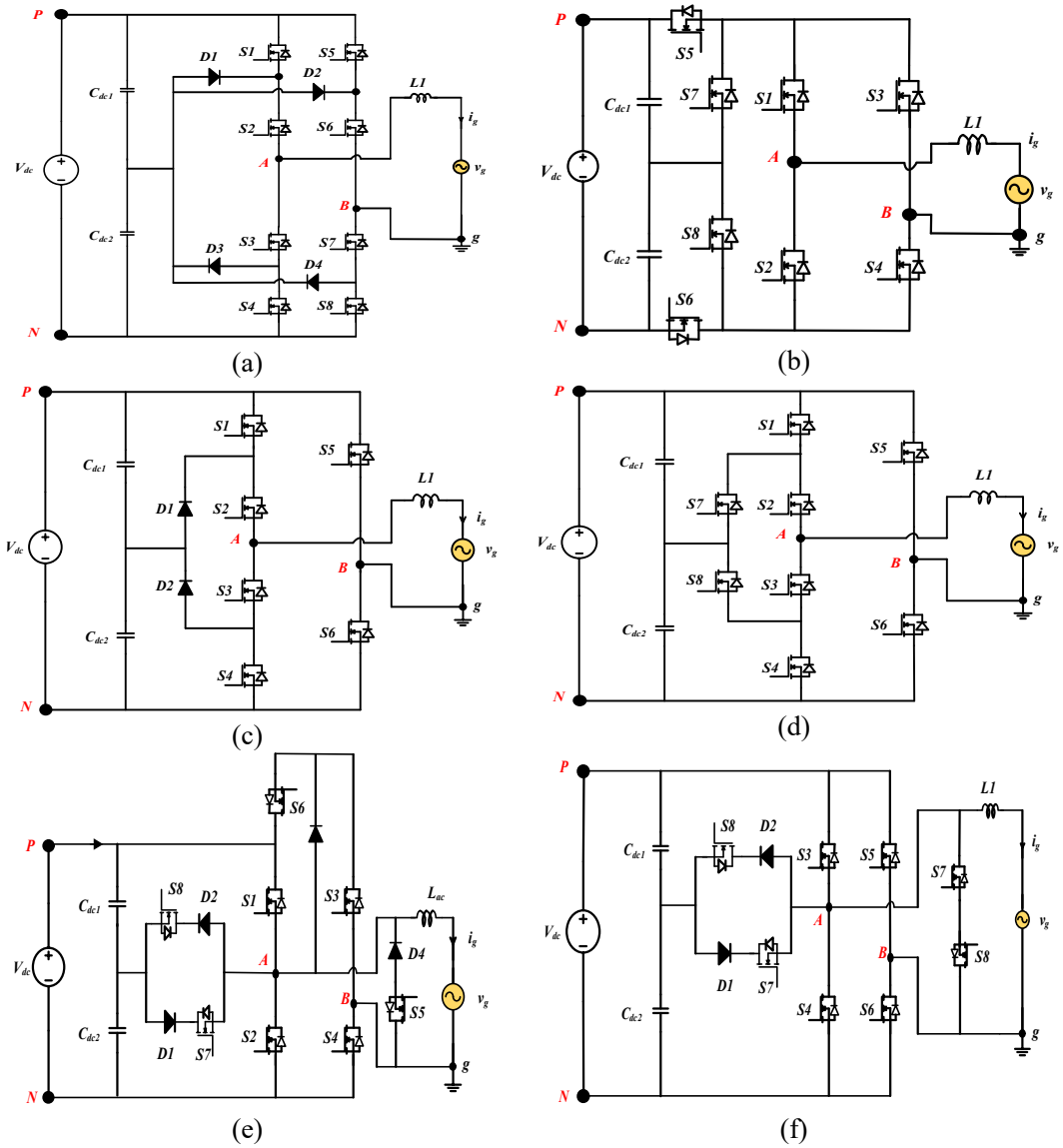
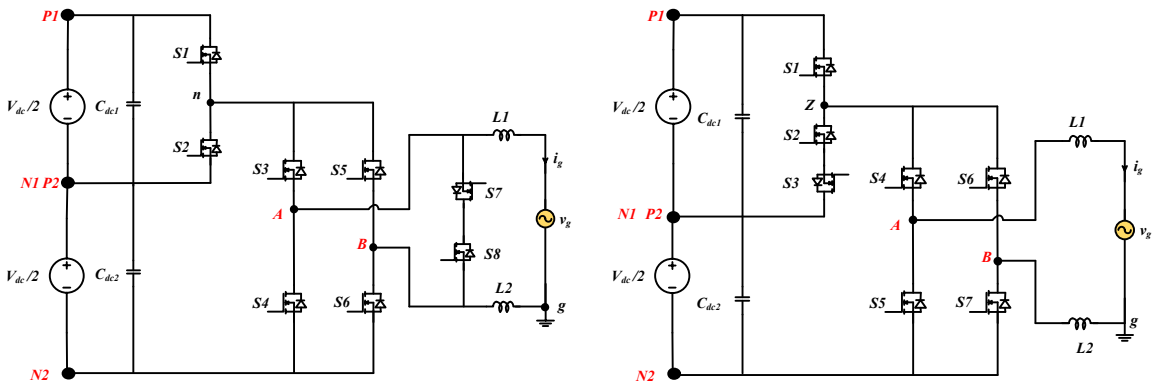
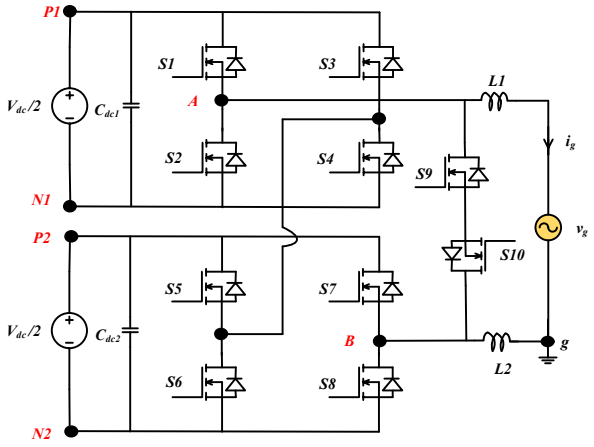


Fig. 2.13. F-B based five-level topologies: (a) FBNPC, (b) 5L-AH6, (c) 5L-NPC, (d) 5L-ANPC, (e) H5-HERIC and (f) DBSMI.

Further classification of five-level TLIs is made by the F-B based symmetrical placement of filter inductors. Two such interesting cascaded MLI topologies (CMLI) are proposed by Venu *et al.,* in refs [60], [61] as shown in Figs. 2.14(a) and (b), respectively. In these two topologies, a novel PWM strategy is proposed to eliminate the high-frequency oscillations in V_{TCMV} for minimizing the leakage current. Also, these MLIs are reliable candidates for high efficiency and reduced component count. However, due to the presence of sudden transitions in the V_{TCMV} while transferring from $\pm 0.5V_{dc}$ level to $\pm V_{dc}$ level and vice-versa results in unwanted spikes in the leakage current. In addition to that, the proposed PWM switching scheme results in higher THD and output filter size. Based on a similar concept, another elegant solution is proposed by Farhad *et al.,* in [62], as shown in Fig. 2.14.(c). In this topology, two additional switches are added to the conventional CHB inverter for obtaining constant V_{TCMV} (i.e., by eliminating both high-frequency oscillations and sudden transitions) by using redundant states during the freewheeling period. But, this configuration has the disadvantage of increased component count and power losses. However, all the F-B based symmetrical five-level TLI topologies require two isolated PV sources for realizing the multi-level output, which increases the cost and complexity of the control system for tracking maximum PV power.



(a) (b)



(c)

Fig. 2.14. Symmetrical Five-Level TLI topologies: (a) Cascaded MLI (CMLI)-I, (b) CMLI-II and (c) CHB-II.

A brief comparative assessment of all the single-stage five-level TLI topologies are given in Table 2.2, from this comparative assessment one can quickly formulate the merits and demerits of each topology, in terms of component count, cost, efficiency and leakage current. In the diode clamed, FC type and hybrid five-level TLI topologies, both the leakage current elimination and reactive power control capability is achieved by solid connection and bidirectional current paths provided by the body diodes of MOSFETs respectively. However, the requirement of high input DC voltage limits the application of these topologies in PVPGS.

The asymmetrical inductor based CHB-I MLI and packed U-cells based topologies generates five-level output with reduced voltage (i.e., $V_{in1}=V_{dc}/2$ and $V_{in2}=V_{dc}/2$). Nevertheless, the high-frequency oscillations present in the CMV causes a higher magnitude of leakage current. Further, the F-B based asymmetrical TLI topologies and symmetrical CMLI topologies are derived to improve the efficiency and also to eliminate the high-frequency oscillations in V_{TCMV}. However, the applied PWM schemes and their topology structures are unable to cancel the sudden transitions (with grid frequency) in $V_{TCMV,}$ which causes a more significant spike in the leakage current. Thus, a novel CHB-II MLI is developed to obtain constant CMV and thereby, it registers very less leakage current in comparison with all other topologies. Further, most of the topologies are reported to operate under UPF conditions only. Whereas the reactive power capability of the inverter is essential for the grid-connected PV system as per the VDE-AR-N4105 standard.

Table 2.2 Comparative assessment of single-stage five-level TLI topologies.

Topology	DC Sources	Input Voltage	Component Count						Advantages	Disadvantages
			C_{dc}	M	D	L_f	C_f	TDC		
5L-DC [49]	1	$2*V_{dc}$	4	8	8	1	1	24	• Constant CMV • Negligible leakage current • Reactive power capability	▪ Requirement of more no.of diodes ▪ DC-link voltage balancing issue ▪ Poor efficiency ▪ Input voltage is double the grid-peak voltage
HNPC [50]	1	$2*V_{dc}$	4	8	4	1	1	16	• Constant CMV • Negligible leakage current • Reactive power capability • Higher efficiency compared to 5L-DC	▪ Complex DC-link voltage balancing ▪ Input voltage is double the grid-peak voltage
5L-FC [51]	1	$2*V_{dc}$	7	8	0	1	1	24	• Constant CMV • Negligible leakage current • Reactive power capability	▪ Requirement of more no.of DC capacitors ▪ DC-link voltage balancing issue ▪ Poor efficiency ▪ Input voltage is double the grid-peak voltage
ANPC-I [52]	1	$2*V_{dc}$	3	8	0	1	1	18	• Constant CMV • Negligible leakage current • Reactive power capability • Higher efficiency compared to 5L-FC	▪ Complex DC-link voltage balancing ▪ Input voltage is double the grid-peak voltage
ANPC-II [52]	1	$2*V_{dc}$	3	8	0	1	1	16	• Constant CMV • Negligible leakage current • Reactive power capability • Higher efficiency compared to ANPC-I	▪ Complex DC-link voltage balancing ▪ Input voltage is double the grid-peak voltage

ANPC-III [53]	1	$2*V_{dc}$	3	8	0	1	1	20	• Constant CMV • Negligible leakage current • Reactive power capability • Abundant switching states to balance the DC-link voltage	▪ Input voltage is double the grid-peak voltage
CHB-I [53]	2	V_{dc}	2	8	0	1	1	24	• Modularity feature • Reduced input DC voltage in comparison with DC and FC based topologies	▪ Requirement of isolated DC sources ▪ Oscillatory CMV ▪ More leakage current ▪ Unity power factor only
U-cell [55]	2	V_{dc}	2	6	0	1	1	18	• Lower switch count compared to CHB • Higher efficiency	▪ Requirement of isolated DC sources ▪ Oscillatory CMV ▪ More leakage current ▪ Unity power factor only
FBNPC [56]	1	V_{dc}	2	8	4	1	1	26	• Requirement of single DC source • Self-balanced DC-link capacitors	▪ Square shape CMV ▪ Medium leakage current ▪ Unity power factor only ▪ Higher power losses
5L-AH6 [57]	1	V_{dc}	2	8	0	1	1	24	• Requirement single DC source • Self-balanced DC-link capacitors	▪ Square shape CMV ▪ Medium leakage current ▪ Unity power factor only ▪ Higher power losses
5L-NPC [56]	1	V_{dc}	2	6	2	1	1	18	• Requirement single DC source • Self-balanced DC-link capacitors	▪ Square shape CMV ▪ Medium leakage current ▪ Unity power factor only ▪ Higher power losses
5L-ANPC [56]	1	V_{dc}	2	8	0	1	1	19	• Requirement single DC source • Self-balanced of DC-link capacitors	▪ Square shape CMV ▪ Medium leakage current ▪ Unity power factor only ▪ Higher power losses
H5-HERIC [58]	1	V_{dc}	2	8	4	1	1	16	• Requirement single DC source • Self-balanced DC-link capacitors	▪ Square shape CMV ▪ Medium leakage current ▪ Unity power factor only

DBSMI [59]	1	V_{dc}	2	8	2	1	1	14	• Requirement single DC source • Self-balanced DC-link capacitors	▪ Square shape CMV ▪ Medium leakage current ▪ Unity power factor only
CMLI-I [60]	2	V_{dc}	2	8	0	2	1	14	• Higher efficiency • Low component count	▪ Requirement of isolated DC sources ▪ Low amplitude square shape CMV ▪ Medium leakage current ▪ Unity power factor only
CMLI-II [61]	2	V_{dc}	2	7	0	2	1	16	• Higher efficiency • Low component count	▪ Requirement of isolated DC sources ▪ Low amplitude square shape CMV ▪ Medium leakage current ▪ Unity power factor only
CHB-II [62]	2	V_{dc}	2	10	0	2	1	18	• Constant CMV • Lower leakage current	▪ Requirement of isolated DC sources ▪ Unity power factor only

C_{dc} –DC capacitor, M –Mosfet, D –Diodes, L_f –Filter inductor, C_f - Filter capacitor, TDC - Total devices are in conduction during one complete cycle.

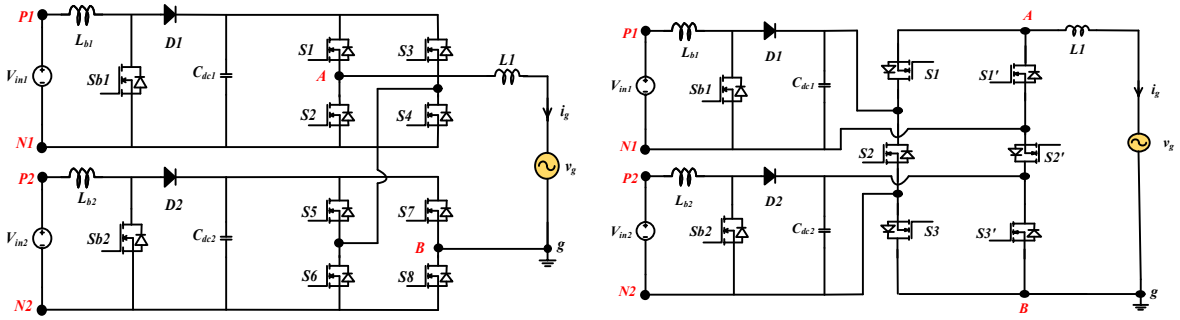
2.4. Various types of Two-Stage Multilevel Inverter Topologies

Recently, module and multi-string type PVPGS became popular and fast-growing segments throughout the world due to its higher PV power extraction, low PV system installation effort, easy monitoring and failure detection. However, the PV module output (i.e., 30V-50V) is relatively small to meet the grid voltage requirement (315V – 480V). The conventional solution to achieve this voltage requirement is to connect more number of PV modules are in series. But, the power generated by the PV modules is reduced significantly due to partial shading and module mismatch, especially in the residential and urban areas. In this context, the parallel-connected PV module arrangement is more efficient than series-connected PV module arrangements [63]-[64]. On the other hand, the parallel-connected PV modules do not give higher DC-link voltages to meet the grid standards. Consequently, to match the voltage profile, the grid-connected inverter requires an additional DC-DC converter, named as two-stage inverters.

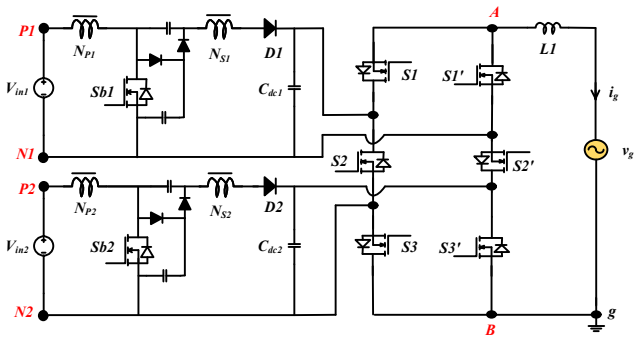
Generally, a front-end DC-DC power converter is used for boosting the low PV output voltage, which can improve the maximum power extraction from the PV source and also reduces the control complexity of the inverter. The main design challenges of the two-stage inverters are the high efficiency, lower cost and effective decoupling of the pulsating power delivered to the grid from the PV module to minimize the leakage current. In these circumstances, several two-stage three-level topologies have been reviewed in refs. [65]-[66]. Most of these topologies comprise either a non-isolated type or an isolated type boost converter (with HFT) followed by half-bridge or full-bridge inverter. However, the three-level output of the topologies described above requires the larger filter size to lower the THD. Consequently, the cost and size of the overall system is increased [67]-[68].

To overcome the above issues, some authors have proposed two-stage MLIs with minimum leakage current. Haimanti et al [69] proposed a two-stage five-level inverter topology by integrating two CHB modules with isolated conventional boost converter, as shown in Fig. 2.15(a). However, the topology requires more number of semiconductor switches to realize the multilevel operation, which reduces the efficiency and increases the cost. Similarly, Fig. 2.15(b), shows the two-stage packed U-cells based five-level inverter for distributed energy resources [70]. It requires a reduced switch count in comparison with the CHB module based two-stage inverter. Another packed U-cell based two-stage five-level inverter is proposed in [71], where the conventional boost converter is introduced

with coupled inductor circuit to obtain higher boost capability and higher efficiency, as shown in Fig. 2.15(c). Further, the above-said three topologies are modular and can extend for an increased number of output levels. In addition to modularity, it also facilitates independent DC-link voltage balancing by incorporating distributed MPPT, which is feasible for grid-connected PV applications.



(a) (b)



(c)

Fig. 2.15. Two-stage dual DC source based five-level inverter (a) Topology 1, (b) Topology 2 and (c) Topology 3.

Further, a single DC source based two-stage five-level topologies are reviewed as follows, Selvaraj *et al.,* [72] presents a bidirectional T-type five-level inverter with conventional boost converter, as shown in Fig. 2.16(a). It requires a single DC source, a reduced number of switches in comparison with the CHB and packed U-cells based two-stage inverters. Moreover, a balanced DC-link capacitor voltage is attained with the modified sinusoidal PWM scheme. Similarly, one more elegant topology is proposed by Kim et al., [73] as shown in Fig. 2.16(b). Where the conventional boost converter is replaced with a modified three-level boost converter (3LBC) and it is further fed to a five-level NPC inverter to achieve higher efficiency and reduced boost inductor size.

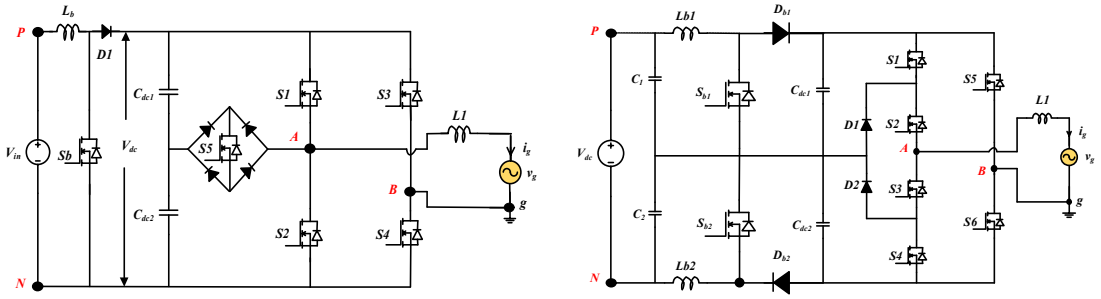


Fig. 2.16. Two-stage single DC source based five-level inverter (a) Topology 1, (b) Topology 2.

Owing to the advantages of multilevel operation, self-balancing of DC-link capacitor voltages and reduced component count, some of the other two-stage seven-level inverter topologies are proposed in the recent work of literature. In refs [74]-[75], two different two-stage seven-level configurations are proposed with a conventional boost converter as shown in Fig. 2.17(a) and (b), respectively. Both of these topologies utilize the advantage of unequal voltages (V_{in2}=2*V_{in1}) to realize the more number of levels in the output with reduced switch count in comparison with conventional NPC, FC and CHB topologies.

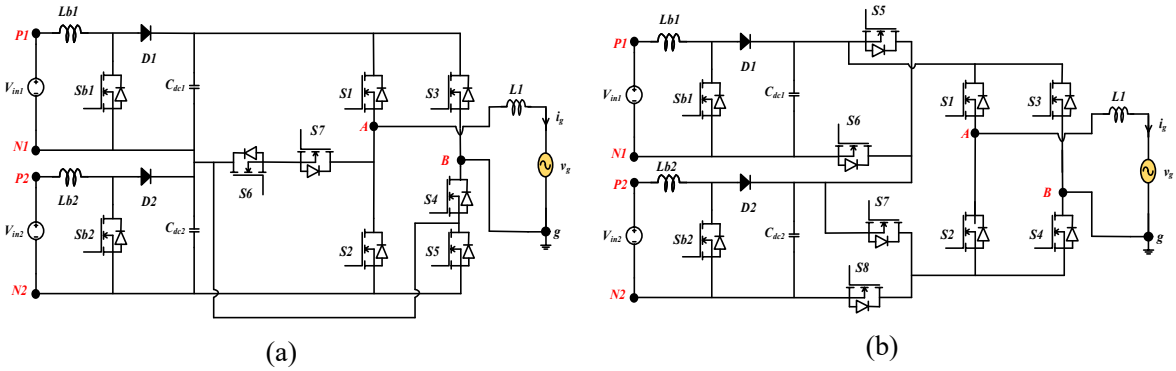


Fig. 2.17. Two-stage dual DC source based seven-level inverter (a) Topology 1, (b) Topology 2.

Another classification is based on the symmetrical (equal voltages) single-source based seven-level inverter topology with a simple boost converter for grid-connected PVPGS is proposed in ref [76] and it is shown in Fig. 2.18(a). However, the main disadvantage of the topology is the complexity in capacitor voltage balancing for the generation of a higher number of voltage levels. Also, the conventional boost converter has the lowest efficiency at higher voltage gains. Because of the above drawbacks, some of the other asymmetrical (unequal voltages) two-stage seven-level inverter topologies are proposed in refs [77]-[79] and they are shown in Figs. 2.18(b), (c) and (d) respectively.

These topologies take advantage of balanced asymmetrical voltage produced by the HFT to generate the seven-level output. Moreover, the power sharing by the HFT is up to 33% of the total power capacity of the converter, hence the power density and losses of the overall system have less impact due to the introduction of HFT. However, these configurations have a disadvantage of increased component count and higher power losses to realize the two-stage multilevel operation.

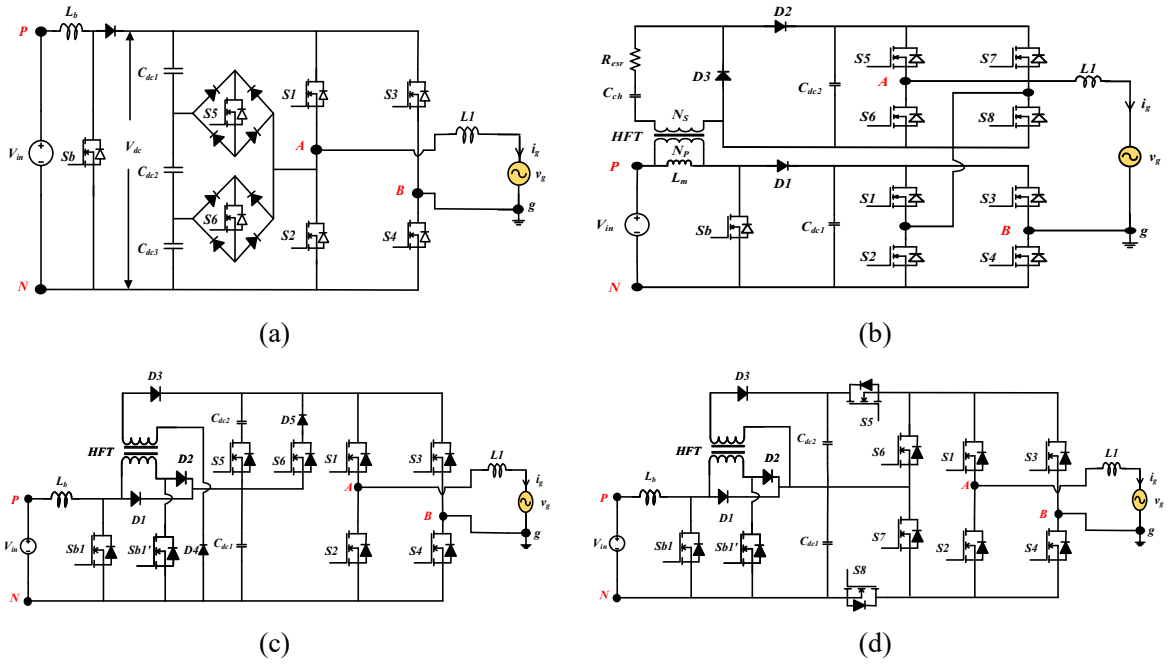


Fig. 2.18. Two-stage single DC source based seven-level inverter (a) Topology 1, (b) Topology 2, (c) Topology 3, (d) Topology 4.

A brief comparative assessment of all the two-stage MLI topologies is presented in Table. 2.3, for easy estimation of the merits and demerits. From Table. 2.3, it is identified all the aforesaid two-stage five-level and seven-level inverter topologies are not considering the high-frequency voltage variations in V_{TCMV} (except topology [73]), which leads to the use of an additional isolation transformer near to the grid side for eliminating the leakage current in PV power generation applications. Consequently, the size, cost and power losses of the overall power conversion system will increase. Further, all they are reported to operate under UPF conditions only. Whereas the reactive power capability is also an important feature for the grid-tied PV inverter as per theVDE-AR-N4105 standard [80].

Table 2.3 Comparative assessment of two-stage MLI topologies

Topology	DC Sources	No. of Levels	Component count						Voltage gain	Advantages	Disadvantages
			C_{dc}	M	D	L_f	C_f	HFT			
Ref [69]	2	5	2	10	2	3	1	0	$V_{in}/(1-D)$	------	▪ Requirement of two isolated DC sources ▪ Oscillatory CMV ▪ More leakage current ▪ Unity power factor only
Ref [70]	2	5	2	8	2	3	1	0	$V_{in}/(1-D)$	------	▪ Requirement of two isolated DC sources ▪ Oscillatory CMV ▪ More leakage current ▪ Unity power factor only
Ref [71]	2	5	2	8	6	1	1	2	$(V_{in}(2+(N_s/N_p)D))/(1-D)$	• Higher voltage gain	▪ Requirement of two isolated DC sources and two HFTs ▪ Oscillatory CMV ▪ More leakage current ▪ Unity power factor only
Ref [72]	1	5	2	6	5	2	1	0	$V_{in}/(1-D)$	• Lower component count	▪ Oscillatory CMV ▪ More leakage current ▪ Unity power factor only
Ref [73]	1	5	2	8	4	3	3	0	$V_{in}/(1-D)$	• Absence of high-frequency variations in CMV • Medium leakage current	▪ Unity power factor only
Ref [74]	2	7	2	10	2	3	1	0	$V_{in}/(1-D)$	-----	▪ Requirement of two isolated DC sources ▪ Oscillatory CMV ▪ More leakage current ▪ Unity power factor only

Ref [75]	2	7	2	10	2	3	1	0	$V_{in}/(1-D)$	-----	▪ Requirement of two isolated DC sources ▪ Oscillatory CMV ▪ More leakage current ▪ Unity power factor only UPF
Ref [76]	1	7	3	7	9	3	1	0	$V_{in}/(1-D)$	-----	▪ Oscillatory CMV ▪ More leakage current ▪ Unity power factor only
Ref [77]	1	7	2	9	3	2	2	1	$(V_{in}/(1-D))$ $*(1+(N_s/N_p))$	• Absence of high-frequency variations in CMV • Medium leakage current • Higher voltage gain	▪ Requirement of the HFT ▪ Oscillatory CMV ▪ More leakage current ▪ Unity power factor only ▪ More power losses due to parasitic elements
Ref [78]	1	7	2	8	5	2	1	1	$(V_{in}/(1-D))$ $*(1+(N_s/N_p))$	• Higher voltage gain	▪ Requirement of the HFT ▪ Oscillatory CMV ▪ More leakage current ▪ Unity power factor only
Ref [79]	1	7	2	10	3	2	1	1	$(V_{in}/(1-D))$ $*(1+(N_s/N_p))$	• Higher voltage gain	▪ Requirement of the HFT ▪ Oscillatory CMV ▪ More leakage current ▪ Unity power factor only

C_{dc} –DC capacitor, M –Mosfet, D –Diodes, L_f –Filter inductor, C_f - Filter capacitor, HFT – High-frequency Transformer, LFT – Line-frequency transformer.

2.5. Problem Formulation

After reviewing various single-phase single-stage and two-stage inverter topologies presented in the literature, the following observations have been made,

a) Recent research is focused on synthesizing novel topologies for grid-connected PVPGS due to the requirement of fewer power devices and higher efficiency.
b) Elimination of the high-frequency oscillations and achieving reactive power control capability simultaneously in the non-isolated inverter topologies could be an advantageous proposition for grid-connected PVPGS.
c) On the other hand, integration of the multilevel technology in the inverter topologies lower the THD and lower the dv/dt stress.
d) Self-balancing of the DC-link capacitor voltages for an increased number of voltage levels reduces the control complexity.
e) The use of more passive components and isolated DC sources for an increased number of voltage levels leads to an increase in the cost, size and weight of the system.

Hence, there is adequate scope for further enhancement in the area of single-phase inverter topologies for grid-connected PVPGS. Moreover, the issues described above, namely, (i) operability with a single source, (ii) reduced switch count, (iii) leakage current reduction without the use of isolation transformer, (iv) reactive power capability and (v) high efficiency, this research focuses on the development of different single-stage and two-inverter topologies for grid-connected PVPGS. Therefore, in this investigation, Four single-phase single-stage configurations and three single-phase two-stage configurations have been proposed.

2.6. Organization of the Thesis

The thesis is organized into seven chapters and the work included in each chapter is briefly outlined as follows:

The **first chapter,** describes an overview of the present problem in the electric power system and pertinent background to the development of grid-

connected PVPGS. An introduction to different types of inverter topologies based on the number of power conversion stages and their issues, standards are discussed.

In the **second chapter,** a comprehensive literature review on both single-stage and two-stage inverter topologies have been presented. This literature gives an overview of the development of single-phase VSI based inverter topologies to eliminate the leakage current. Brief comparison tables of different single-stage and two-stage inverters are presented in this chapter based on the active and passive component count, leakage current, nature of V_{TCMV} and operability of power factor. Further, this chapter sets the path for the development of new single-phase VSI based single-stage and two-stage inverter topologies for grid-connected PVPGS.

In the **third chapter,** a bi-directional clamping based H5, HERIC, H6 and Hybrid-bridge topologies are proposed with improved PWM schemes. Effect of switch junction capacitances on CMV and reactive power flow in both traditional and proposed topologies were analyzed. The common-mode and differential characteristics of all the topologies are tested with MATLAB simulations and further justified with experimental results. Moreover, the characteristic performance comparisons of the proposed and traditional topologies are presented to highlight the merits of the proposed solution over the conventional.

In the **fourth chapter,** a new power conditioner with the inherent benefits of boosting, generation of seven-level output voltage with minimum leakage current in a grid-connected PVPGS is proposed. The system description, different modes of operation, closed-loop control system and the leakage current analysis are extensively described. Simulation work is carried out for the validation of a grid-connected mode of operation for the proposed power conditioner. Moreover, the experimental test setup is built to validate the proposed inverter under steady-state and dynamic conditions. Finally, the power conditioner is critically evaluated through a detailed comparison with respect to the other two-stage inverters for grid-connected PVPGS.

In the **fifth chapter,** a two-stage hybrid transformerless MLI for single-phase grid-connected PVPGS is presented. The system description, different

modes of operation, modulation technique, and the common-mode voltage analysis are extensively described. Simulation work is carried out and a prototype model is developed for the validation of results under steady-state and dynamic conditions. A detailed comparison is also made to show the advantages of the proposed topology with various other MLIs.

In the **sixth Chapter**, a two-stage T-type hybrid five-level TLI for grid-connected PVPGS is presented with the merits of reduced leakage current and reactive power control capability. The system description, different modes of operation, modulation technique and common mode voltage analysis are described. Simulation work is carried and a prototype model is developed for the validation of results under steady-state and dynamic conditions. Further, the advantages of the proposed topology are highlighted through a detailed comparison with other MLIs.

The **seventh chapter**, concludes the thesis by summarizing the contributions and indicates the directions for further research in the area of grid-connected PVPGS.

Chapter 3

BI-DIRECTIONAL TRANSFORMERLESS INVERTER TOPOLOGIES

Chapter 3

Bi-directional Transformerless Inverter Topologies

3.1. Introduction

In the present scenario, grid-connected PVPGS are getting popular to meet the increasing energy demands in terms of commercial and industrial applications. However, integration of PVPGS into the grid is becoming challenging in modern days due to more device counts, lower efficiency, larger size and higher cost as clearly reported in Chapter 2. To meet these challenges, transformerless inverters (TLIs) are widely accepted and more suitable for PV power applications. But, in the absence of a transformer, there exist a galvanic connection between PV array to the ground and it results in the flow of hazardous leakage current. Several TLI topologies have been proposed in the literature with decoupling circuits to reduce the leakage current. Among those H5, HERIC, H6 and Hybrid-bridge (H-B) topologies are the most popular and widely accepted TLIs. Nevertheless, the effect of switch junction capacitances was not considered in the common-mode voltage (CMV) analysis, which inevitably causes excess leakage current. Moreover, in the recent days, reactive power capability is one of the prerequisite issue for TLIs to penetrate more amount of PV power into the grid. However, with the traditional PWM schemes it cannot be accomplished due to the absence of a bi-directional current path during the freewheeling period .

Therefore, in this chapter, a bi-directional clamping (BDC) based H5, HERIC, H6 and H-B TLI topologies is proposed with improved PWM schemes. BDC branch reduces the leakage current by clamping the inverter terminal voltages to half of the DC-link voltage during the freewheeling period and the improved PWM schemes ensure bi-directional current path while operating in negative power region. The reasons for fluctuating CMV and non-reactive power capability of the conventional topologies are discussed in detail. The performance of both traditional and proposed topologies are tested with MATLAB simulations and further justified with experimental results. Moreover, the dynamic performance of the proposed inverters under grid-connected mode of operation is

tested by using OPAL-RT OP4500 modules under different operating power factor conditions of the grid. In addition to the above, the efficiency evaluation of both the traditional and proposed topologies is carried out by using a thermal module toolbox in power simulation (PSIM) software.

3.2 Analysis of the Conventional H5, HERIC, H6 and Hybrid-Bridge TLI Topologies

The topological structures and gate pulses of the traditional H5, HERIC, H6 and H-B TLIs are shown in Figs. 3.1 to 3.4, respectively [33]-[36]. Where, V_{dc} is the equivalent PV voltage, namely, input DC voltage of the inverter, C_{PV} is the parasitic capacitance of the PV module. Positive and negative terminals of the input DC source are denoted as *P* and *N*. Similarly, phase and neutral terminals of the inverter are denoted as *A* and *B*, respectively.

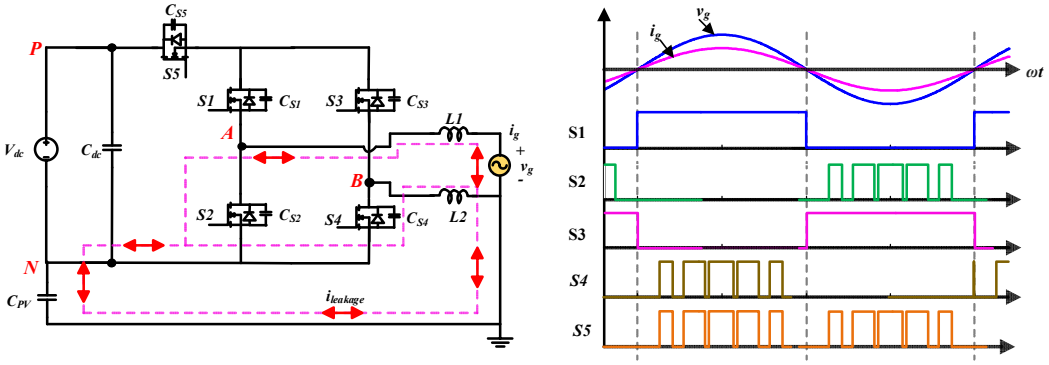


Fig. 3.1. H5 TLI: (a) circuit structure (b) gate pulses.

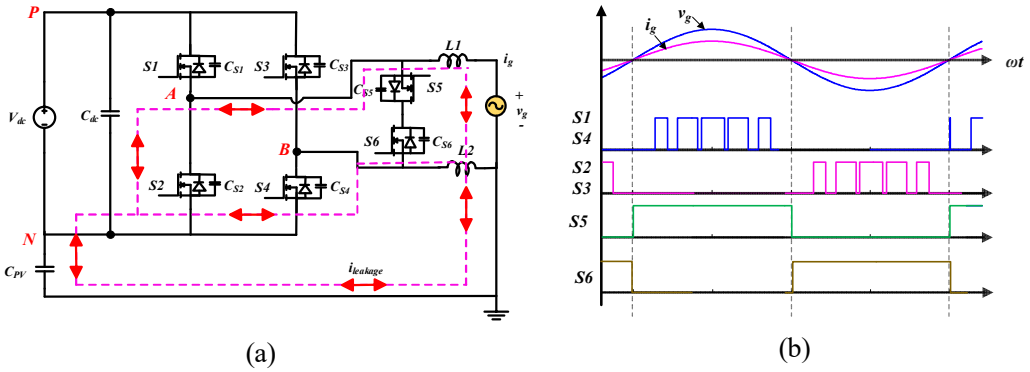
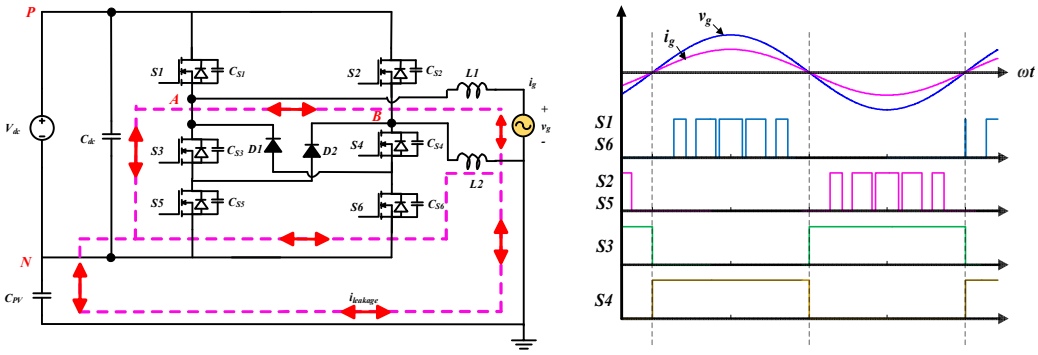
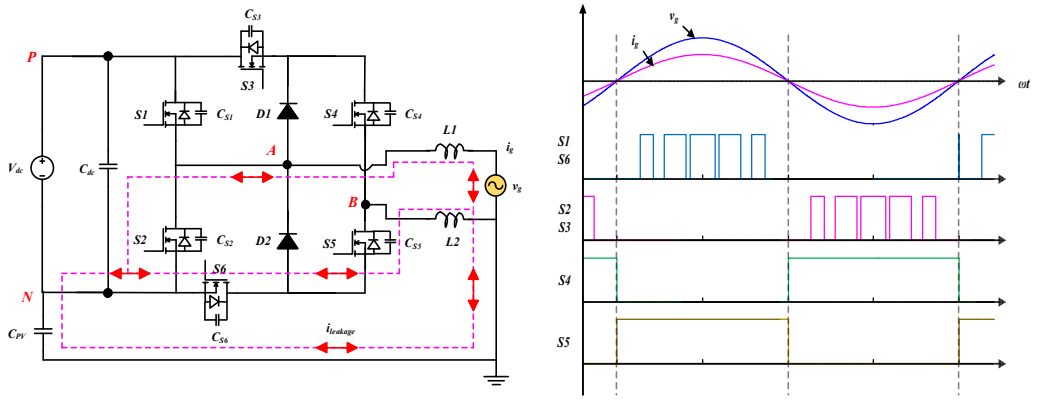


Fig. 3.2. HERIC TLI: (a) circuit structure (b) gate pulses.



(a) (b)

Fig. 3.3. H6 TLI: (a) circuit structure (b) gate pulses.



(a) (b)

Fig. 3.4. H-B TLI: (a) circuit structure (b) gate pulses.

General expressions used for the computation of CMV 'V_{CM}' and differential-mode voltage 'V_{DM}' are indicated in terms of inverter terminal voltages V_{AN} and V_{BN} are as follows;

$$V_{DM} = V_{AB} = V_{AN} - V_{BN} \tag{3.1}$$

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2} \tag{3.2}$$

Asymmetry in the filter inductors ($L1$ and $L2$) produces an additional CMV ($V_{CM\text{-}DM}$) as given in (3.3). Thus, the total CMV (V_{TCMV}) and leakage current ($i_{leakage}$) can be expressed in (3.4) and (3.5) respectively.

$$V_{CM-DM} = V_{DM} \cdot \frac{L2 - L1}{2(L2 + L1)} \tag{3.3}$$

$$V_{TCMV} = V_{CM} + V_{CM-DM} \tag{3.4}$$

$$i_{leakage} = C_{PV} \frac{dV_{TCMV}}{dt} \tag{3.5}$$

It is apparent that the leakage current depends on V_{TCMV} and the equivalent parasitic capacitance (C_{PV}). If *L1=L2* (for a well-designed circuit with symmetrically structured magnetic), additional CMV is zero (i.e., $V_{CM\text{-}DM} = 0$) and $V_{TCMV} = V_{CM}$. From (3.5), if V_{TCMV} is constant $i_{leakage} = 0$. In opposite, if high-frequency oscillations are present in CMV, leakage current will flow through the C_{PV}, which is inevitable in all the TLI topologies. Usually, these oscillations depend on the topology and PWM scheme employed for the switching of an inverter. Further, the effect of low-frequency components such as C_{1g}, C_{2g} (parasitic capacitance between the heat-sink and ground, which is in range of tens to hundreds of picofarads) on leakage current is very less [9], [45]. Hence they are ignored in the analysis of leakage current for simplicity.

3.2.1. Analysis of Oscillations in the CMV due to Junction Capacitance of the Switches

In real-time, the analysis of leakage current due to junction capacitances of the MOSFETs cannot be ignored. Traditional H5 inverter is considered as an example for analyzing the effect of switch junction capacitance on CMV and it is explained as follows [20], [81]; From Fig. 3.5(a), $V_{AN} = V_{dc}$, $V_{BN} = 0$ and $V_{CM} = V_{dc}/2$ for positive half cycle. Similarly, from Fig. 3.5(c), $V_{AN} = 0$, $V_{BN} = V_{dc}$ and $V_{CM} = V_{dc}/2$ for a negative half cycle. It is observed that the CMV is constant (i.e., $V_{dc}/2$) in both the half cycles. Whereas in the freewheeling mode, filter inductor currents continuously freewheel through the grid and power cannot be transferred from the input DC source as shown in Figs. 3.5(b) and (d). While transferring from positive half cycle to freewheeling period, switches *S4* and *S5* are switched off synchronously.

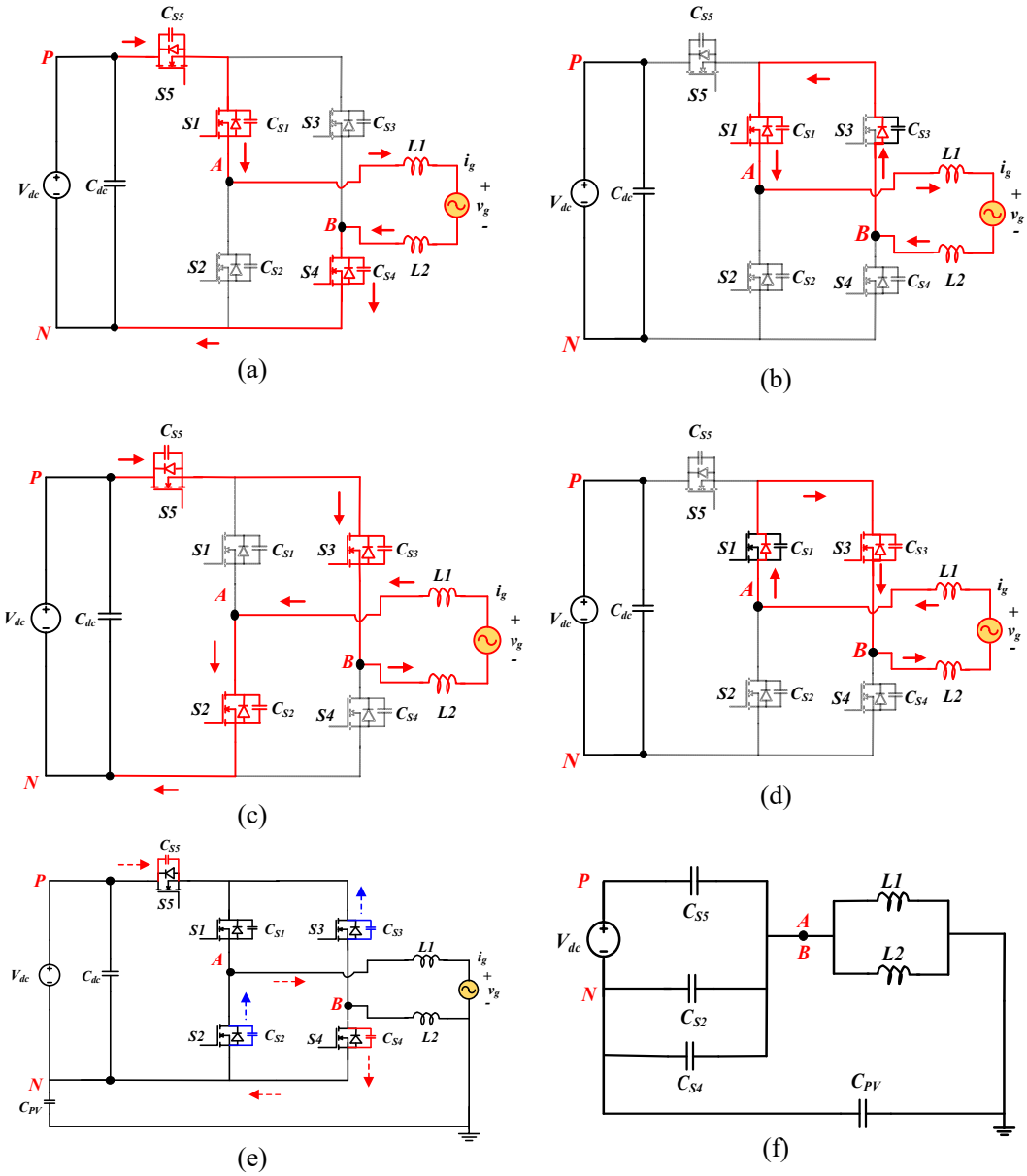


Fig. 3.5. Operating states, charging and discharging of switch junction capacitances of H5 topology in positive power transferring mode: (a) Positive half cycle, (b) Freewheeling period during positive half cycle, (c) Negative half cycle, (d) Freewheeling period during negative half cycle, (e) Charging and discharging of switch junction capacitances during positive half cycle and (f) Simplified circuit.

During the transient period junction capacitances of the switches *S4, S5* are charging and the switches *S2, S3* are discharging as depicted in Fig. 3.5(e). After completion of the transition, the body diode of *S3* will conduct to provide the freewheeling path. Also, the terminal voltage V_{AN} increases and V_{BN} decreases due to charging and discharging of junction capacitances [20]. From the simplified circuit depicted in Fig. 3.5(f), the terminal voltages can be evaluated by (3.6) using Kirchhoff's current law. The steady-state terminal voltages during

the freewheeling period are regulated by the junction capacitances of the MOSFETs as shown in Eq. (3.6). Therefore, the V_{CM} of the H5 inverter is not constant throughout the whole period, which results in abrupt leakage current. Similarly, the terminal voltages of the HERIC, H6 and H-B inverter topologies are given in Eq. (3.7), (3.8) and (3.9) respectively. [82], [83].

$$V_{AN} = V_{BN} = \frac{C_{S2} + C_{S5}}{C_{S2} + C_{S5} + C_{S4}} V_{dc} \tag{3.6}$$

$$V_{AN} = V_{BN} = \frac{C_{S1} + C_{S3}}{C_{S1} + C_{S2} + C_{S3} + C_{S4}} V_{dc} \tag{3.7}$$

$$V_{AN} = V_{BN} = \frac{C_{S1} + C_{S2}}{C_{S1} + C_{S2} + \frac{C_{S3}.C_{S5}}{C_{S3} + C_{S5}} + C_{S4}} V_{dc} \tag{3.8}$$

$$V_{AN} = V_{BN} = V_{dc}. \frac{C_{S1} + \frac{C_{S3}.C_{S4}}{C_{S3} + C_{S4}}}{C_{S1} + C_{S2} + \frac{C_{S3}.C_{S4}}{C_{S3} + C_{S4}} + C_{S6}} \tag{3.9}$$

From the above expressions, it is evident that V_{AN} and V_{BN} are not equal to $V_{dc}/2$ during the freewheeling period for all four traditional topologies. Therefore, CMV cannot be kept constant in all the operating modes of the inverters and it will further increase the magnitude of leakage current.

3.2.2. Analysis of the Bi-Directional Current Path in Traditional TLI Topologies

The reactive power control capability of the inverter is determined based on the bi-directional current path provided by the topology and its PWM technique. From Figs. 3.6 to 3.9; it is observed that the conventional PWM technique applied for all the four topologies is not providing a bi-directional current path during the freewheeling period under the negative power region. For example, in H5 topology switch *S3* is turn-off during positive v_g and negative i_g as shown in Fig. 3.6(a). Similarly, switch *S1* is turn-off during negative v_g and positive i_g as shown in Fig. 3.6(b). Thus, reactive power control capability cannot be realized with the traditional PWM scheme applied to the H5 topology. In the

same way, switch *S6 ($+v_g$ and $-i_g$)*, *S5 ($-v_g$ and $+i_g$)* in Heric, switches *S3 ($+v_g$ and $-i_g$)*, *S4 ($-v_g$ and $+i_g$)* in H6 and switch *S4 ($+v_g$ and $-i_g$)*, *S5 ($-v_g$ and $+i_g$)* in H-B inverter are turn-off under negative power region as shown in Figs. 3.7, 3.8 and 3.9, respectively. Therefore, PWM schemes applied to the traditional TLI topologies should be improved to support the bi-directional current path during the freewheeling period.

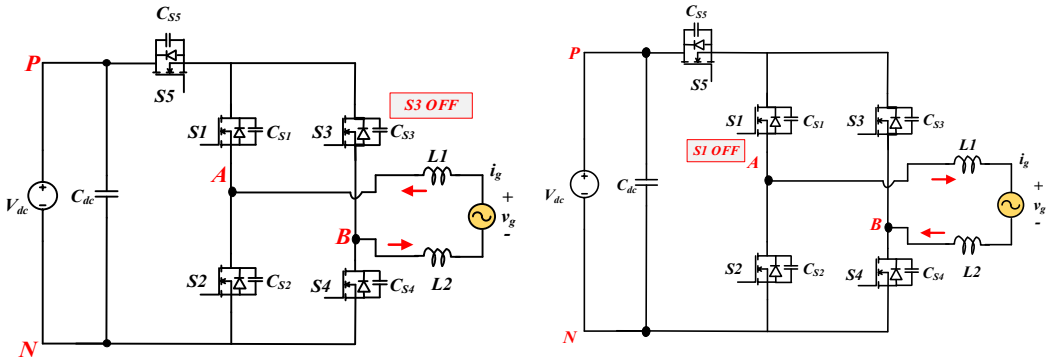


Fig. 3.6. H5 topology during negative power region; (a) positive v_g and negative i_g, (b) negative v_g and positive i_g.

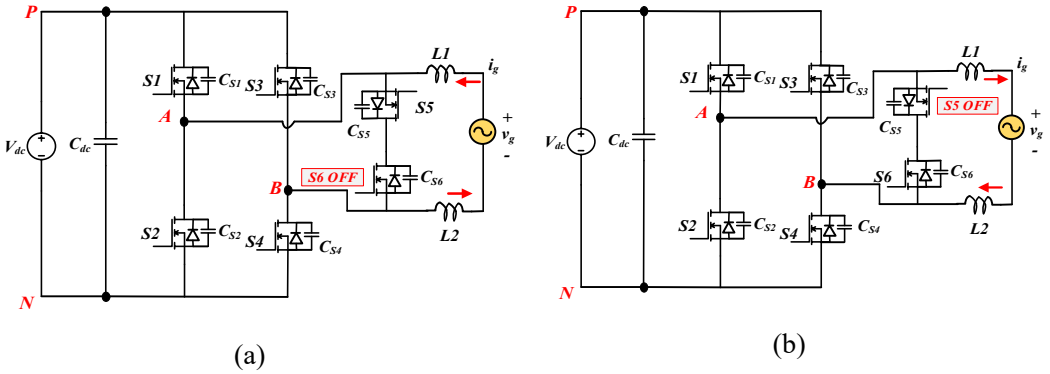


Fig. 3.7. HERIC topology during negative power region; (a) positive v_g and negative i_g, (b) negative v_g and positive i_g.

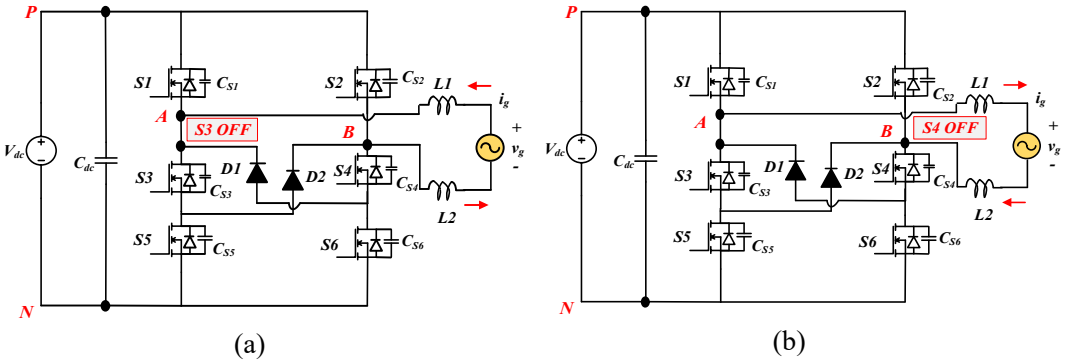
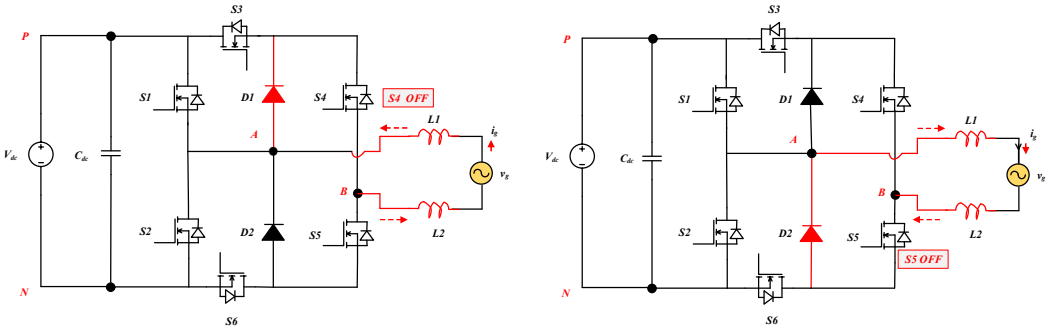


Fig. 3.8. H6 topology during negative power region; (a) positive v_g and negative i_g, (b) negative v_g and positive i_g.



(a) (b)

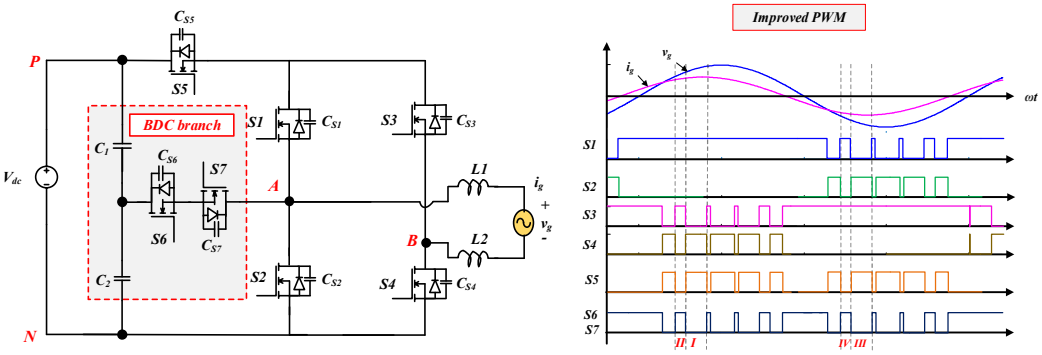
Fig. 3.9. H-B topology during negative power region; (a) positive v_g and negative i_g, (b) negative v_g and positive i_g.

3.3. Proposed BDC based H5, HERIC, H6 and H-B TLI Topologies

To solve the above-mentioned issues, a BDC branch is integrated along with improved PWM schemes for the traditional H5, Heric, H6 and H-B topologies, as shown in Figs. 3.10, 3.11, 3.12 and 3.13 respectively. The BDC branch is obtained by connecting two source connected MOSFETs with split DC-link capacitors to clamp the terminal voltages of the inverter to $V_{dc}/2$ during the freewheeling period. Moreover, improved PWM schemes are allowing the current in both directions to support the reactive power control during the freewheeling period.

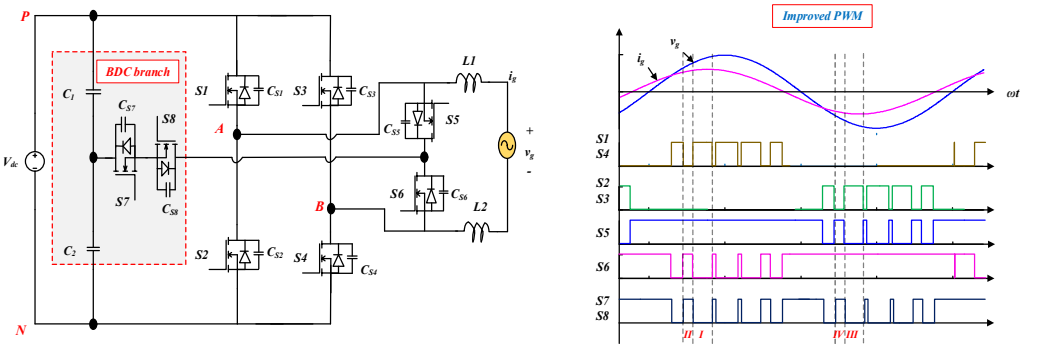
3.3.1. Operating States

Operating states of the inverters in both unity and non-unity power factor operations of the grid are explained in this section. Based on the voltage polarity, the operation of the inverters is classified into three states (i.e., $V_{AB}=V_{dc}$, $V_{AB}=$ Zero and $V_{AB}=-V_{dc}$) and each state allows the current from source to grid and vice-versa. Operation of both traditional and BDC based topologies are the same during the positive power region. Further, switching logic, terminal voltages and CMV calculations for BDC based topologies are listed in Table 3.1.



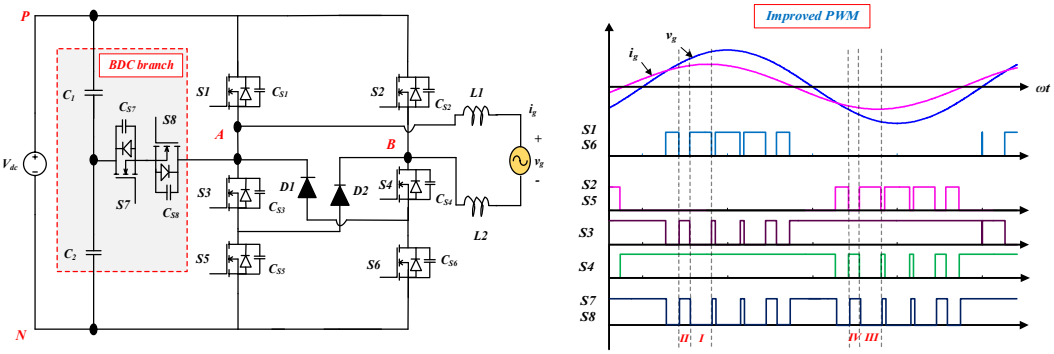
(a) (b)

Fig. 3.10. BDC-H5 TLI: (a) Circuit diagram, (b) improved PWM.



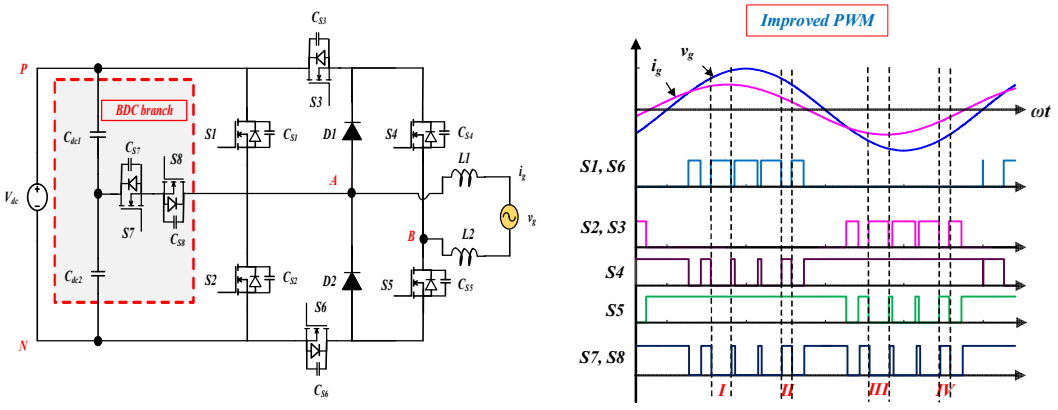
(a) (b)

Fig. 3.11. BDC-HERIC TLI: (a) Circuit diagram, (b) improved PWM.



(a) (b)

Fig. 3.12. BDC-H6 TLI: (a) Circuit diagram, (b) improved PWM.



(a) (b)

Fig. 3.13. BDC-H-B TLI: (a) Circuit diagram, (b) improved PWM.

State 1: In this state, $V_{AB} = V_{dc}$ and the current flows either from source to grid or vice-versa, as shown in Figs. 3.14(a), 3.15(a), 3.16(a) and 3.17(a) respectively. During this state, in positive power region, current flows through MOSFETs and in the negative power region current flows through body diodes of MOSFETs. The inverter terminal voltages $V_{AN}=V_{dc}$, $V_{BN}=0$. Hence V_{DM} and V_{CM} become,

$$V_{DM} = V_{AN} - V_{BN} = V_{dc} \tag{3.9}$$

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2} = \frac{V_{dc}}{2} \tag{3.10}$$

State 2: In this state, $V_{AB} = 0$ and the current freewheels through the inductors and grid or vice-versa via MOSFETs or body diodes of MOSFETs, as shown in Figs. 3.14(b), 3.15(b), 3.16(b) and 3.17(b) respectively. During this state, DC source is isolated from the grid and also the inverter terminal voltages are clamped to half of the DC-link voltage, such as $V_{AN}=V_{dc}/2$, $V_{BN}= V_{dc}/2$. Hence V_{DM} and V_{CM} become,

$$V_{DM} = V_{AN} - V_{BN} = 0 \tag{3.11}$$

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2} = \frac{V_{dc}}{2} \tag{3.12}$$

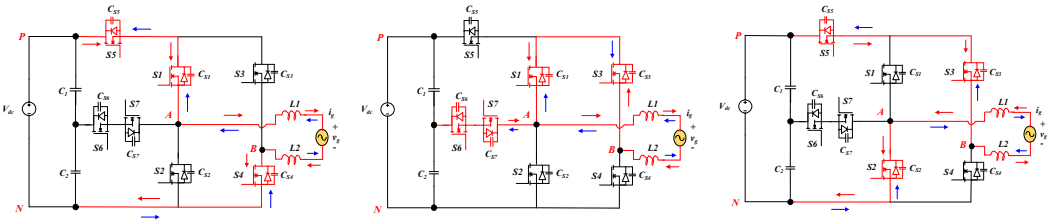
State 3: In this state, $V_{AB} = -V_{dc}$ and the current flows either from source to grid or vice-versa as shown in Figs. 3.14(c), 3.15(c), 3.16(c) and 3.17(c), respectively. During this state, in positive power region, current flows through MOSFETs and in the negative power region current flows through body diodes of MOSFETs. The inverter terminal voltages $V_{AN}=0$, $V_{BN}=V_{dc}$. Hence V_{DM} and V_{CM} become,

$$V_{DM} = V_{AN} - V_{BN} = -V_{dc} \tag{3.13}$$

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2} = \frac{V_{dc}}{2} \tag{3.14}$$

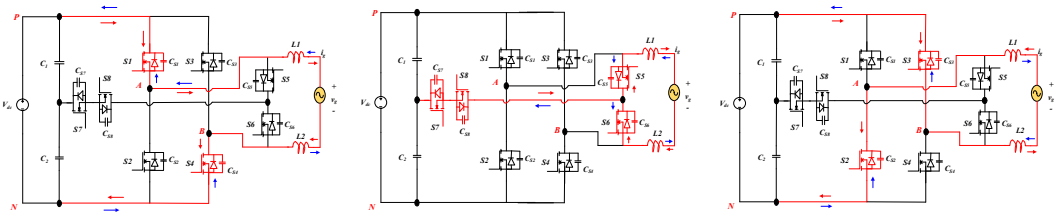
From equations (3.9)-(3.14), it is observed that the V_{CM} is maintained constant in all the operating modes of BDC based TLI topologies. Therefore, the effect of switch junction capacitance is eliminated by clamping the terminal

voltages to $V_{dc}/2$. Consequently, the magnitude of leakage current and size of the CMF is reduced in the proposed TLI topologies [20].



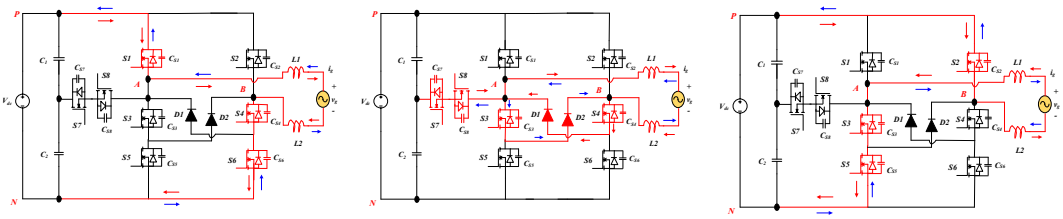
(a) (b) (c)

Fig. 3.14. Operating modes of the BDC-H5 inverter (a) $V_{AB}= V_{dc}$, (b) $V_{AB}= 0$, (c) $V_{AB}=-V_{dc}$.



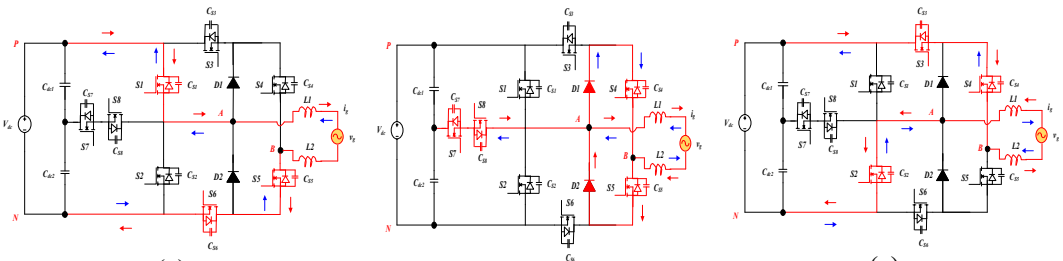
(a) (b) (c)

Fig. 3.15. Operating modes of the BDC-HERIC inverter (a) $V_{AB}= V_{dc}$, (b) $V_{AB}= 0$, (c) $V_{AB}=-V_{dc}$.



(a) (b) (c)

Fig. 3.16. Operating modes of the BDC-H6 inverter (a) $V_{AB}= V_{dc}$, (b) $V_{AB}= 0$, (c) $V_{AB}=-V_{dc}$.



(a) (b) (c)

Fig.3. 17. Operating modes of the BDC-H-B inverter (a) $V_{AB}= V_{dc}$, (b) $V_{AB}= 0$, (c) $V_{AB}=-V_{dc}$.

3.3.2. Improved PWM Strategy

Figs. 3.10(b), 3.11(b), 3.12(b) and 3.13(b) illustrate the improved UPWM schemes for BDC based H5, HERIC, H6 and H-B topologies, respectively. Here, a bi-directional current path is provided for the inverters by turning on the

switches *S1* and *S3* in H5, *S5* and *S6* in HERIC, *S3* and *S4* in H6 and *S4* and *S5* in H-B topologies during the freewheeling period. Moreover, in zero states, only two switches and two diodes are conducting with respect to the current direction. Further, the proposed BDC branch clamps the V_{AN}, V_{BN} to $V_{dc}/2$, which ensures constant CMV during the freewheeling period in both unity power factor and non-unity power factor operations of the grid.

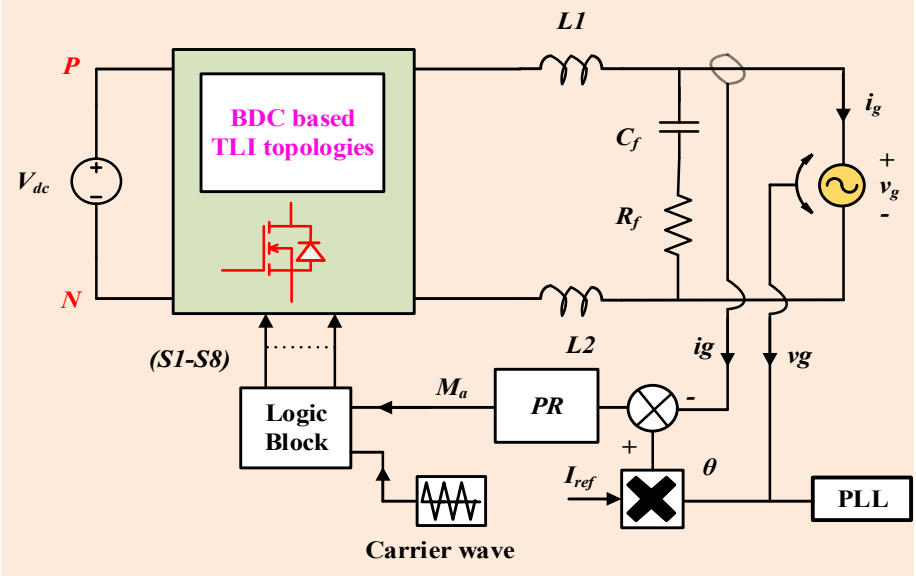


Fig. 3.18. Closed loop control of BDC based topologies.

The closed-loop operation of the proposed TLI topologies is verified by using current control strategy proposed in [84]. The closed-loop controller comprises a proportional-resonant (PR) controller and switching logic block to generate the reference sine wave based on the availability of input power, as shown in Fig. 3.18. A damping resistance (R_f) is connected in series with the filter capacitor (C_f), which attenuates part of the ripple on the switching frequency in order to alleviate the issues of resonance [85].

Table 3.1. Switching logic and CMV calculations of BDC based H5, HERIC, H6 and H-B TLI topologies

BDC based TLIs		*S1*	D_{S1}	*S2*	D_{S2}	*S3*	D_{S3}	*S4*	D_{S4}	*S5*	D_{S5}	*S6*	D_{S6}	*S7*	D_{S7}	*S8*	D_{S8}	*D1*	*D2*	V_{AN}	V_{BN}	$V_{TCMV}=V_{CM}$
H5	$i_g>0$	1	0	0	0	0	0	1	0	1	0	0	0	0	0	-	-	-	-	V_{dc}	0	$V_{dc}/2$
$V_{AB}=V_{dc}$	$i_g<0$	0	1	0	0	0	0	0	1	0	1	0	0	0	0	-	-	-	-	V_{dc}	0	$V_{dc}/2$
H5	$i_g>0$	1	0	0	0	0	1	0	0	0	0	1	0	0	1	-	-	-	-	$V_{dc}/2$	$V_{dc}/2$	$V_{dc}/2$
$V_{AB}=0$	$i_g<0$	0	1	0	0	1	0	0	0	0	0	0	1	1	0	-	-	-	-	$V_{dc}/2$	$V_{dc}/2$	$V_{dc}/2$
H5	$i_g>0$	0	0	1	0	1	0	0	0	1	0	0	0	0	0	-	-	-	-	0	V_{dc}	$V_{dc}/2$
$V_{AB}=-V_{dc}$	$i_g<0$	0	0	0	1	0	1	0	0	0	1	0	0	0	0	-	-	-	-	0	V_{dc}	$V_{dc}/2$
HERIC	$i_g>0$	1	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	-	-	V_{dc}	0	$V_{dc}/2$
$V_{AB}=V_{dc}$	$i_g<0$	0	1	0	0	0	0	0	1	1	0	0	0	0	0	0	0	-	-	V_{dc}	0	$V_{dc}/2$
HERIC	$i_g>0$	0	0	0	0	0	0	0	0	1	0	0	1	1	0	0	1	-	-	$V_{dc}/2$	$V_{dc}/2$	$V_{dc}/2$
$V_{AB}=0$	$i_g<0$	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	0	-	-	$V_{dc}/2$	$V_{dc}/2$	$V_{dc}/2$
HERIC	$i_g>0$	0	0	1	0	1	0	0	0	0	0	1	0	0	0	0	0	-	-	0	V_{dc}	$V_{dc}/2$
$V_{AB}=-V_{dc}$	$i_g<0$	0	0	0	1	0	1	0	0	0	0	1	0	0	0	0	0	-	-	0	V_{dc}	$V_{dc}/2$
H6	$i_g>0$	1	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	V_{dc}	0	$V_{dc}/2$
$V_{AB}=V_{dc}$	$i_g<0$	0	1	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	V_{dc}	0	$V_{dc}/2$
H6	$i_g>0$	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	1	1	0	$V_{dc}/2$	$V_{dc}/2$	$V_{dc}/2$
$V_{AB}=0$	$i_g<0$	0	0	0	0	1	0	0	0	0	0	0	0	0	1	1	0	0	1	$V_{dc}/2$	$V_{dc}/2$	$V_{dc}/2$
H6	$i_g>0$	0	0	1	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	V_{dc}	$V_{dc}/2$
$V_{AB}=-V_{dc}$	$i_g<0$	0	0	0	1	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	V_{dc}	$V_{dc}/2$
H-B	$i_g>0$	1	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	V_{dc}	0	$V_{dc}/2$
$V_{AB}=V_{dc}$	$i_g<0$	0	1	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	V_{dc}	0	$V_{dc}/2$
H-B	$i_g>0$	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	1	0	1	$V_{dc}/2$	$V_{dc}/2$	$V_{dc}/2$
$V_{AB}=0$	$i_g<0$	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	0	1	0	$V_{dc}/2$	$V_{dc}/2$	$V_{dc}/2$
H-B	$i_g>0$	0	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	V_{dc}	$V_{dc}/2$
$V_{AB}=-V_{dc}$	$i_g<0$	0	0	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	V_{dc}	$V_{dc}/2$

*D_{S1} to D_{S8} are the body diodes of switches *S1* to *S8* respectively.

3.4. Selection of Passive Components

The size of the DC-link capacitors [7], [86] is determined by using Equation 3.15, which is derived based on the amplitude of ripple in DC-link voltage (ΔV_{dc}). Where P_{rated} is the rated power, ω is the grid frequency in rad/sec. A passive filter is employed to limit the harmonic content by DC-AC inverter at point of common coupling and its detailed design procedure is given in reference [87]. The IEEE 1547 grid interconnection standards are considered to limit the harmonic content. The design of the filter inductor ($L1=L2=L_f/2$) depends on the desired peak-peak current ripple ($\Delta i_{LP\text{-}P}$) and it is given in equation 3.16. The design of the filter capacitor is based on the maximum power factor seen by the grid. The value of the filter capacitor (C_f) is calculated as per equation 3.17 for a 5% ripple. Where P_{rated} is the rated power, v_g is the RMS value of the grid voltage, V_{dc} is the total DC-link voltage; f and f_s are the grid frequency and switching frequency of inverter, respectively.

$$C1 = C2 = \frac{P_{rated}}{2\omega V_{dc}\Delta V_{dc}} \tag{3.15}$$

$$\frac{V_{dc}}{24 f_s L_f} = \Delta i_{LP-P} < 25\% \frac{P_{rated}}{v_g} \tag{3.16}$$

$$C_f = 5\% \frac{P_{rated}}{2\pi . f . v_g^2} \tag{3.17}$$

3.5. Simulation Results

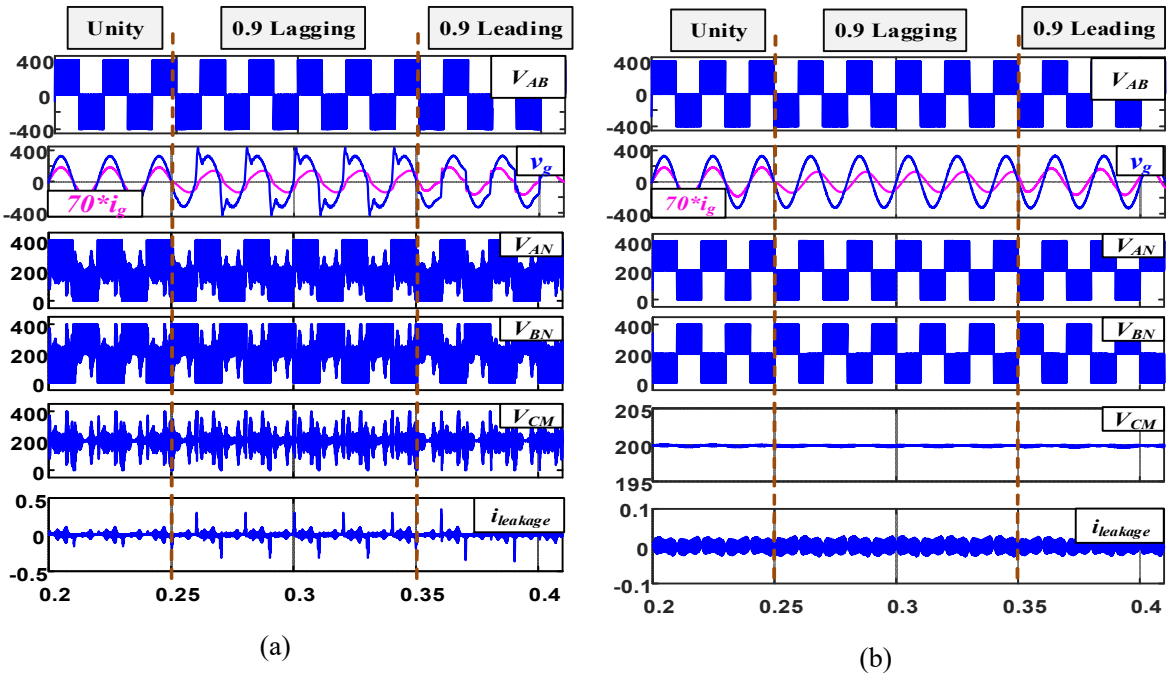
To test the proposed concept, simulation studies were carried out as per the specifications listed in Table 3.2 by using MATLAB software. An equivalent capacitance of 42 nF is placed between the terminals of DC power source to the ground for the evolution of leakage current caused due to oscillations in CMV. Further, the reactive power control capability of the proposed grid-connected inverters is tested for 0.9 lagging and 0.9 leading conditions. Fig. 3.19 shows the differential mode (V_{AB}, v_g *and* i_g) and common mode (V_{AN}, V_{BN}, V_{CM} and $i_{leakage}$) characteristics of both traditional and BDC based H5 topologies. Similarly, Figs. 3.20, 3.21 and 3.22 illustrate the waveforms of both traditional and BDC based HERIC, H6 and H-B inverter topologies.

From the simulation results, it can be observed that the improved PWM schemes provide the reactive power support to enhance the inverter operation in all the operating

modes without losing the waveform quality. Moreover, the additional BDC branch effectively clamps the CMV to $V_{dc}/2$ in all the operating modes of the proposed inverter topologies. Therefore, high-frequency oscillations due to switch junction capacitances are eliminated in V_{CM} during the freewheeling states, which result in the reduction of leakage current [88].

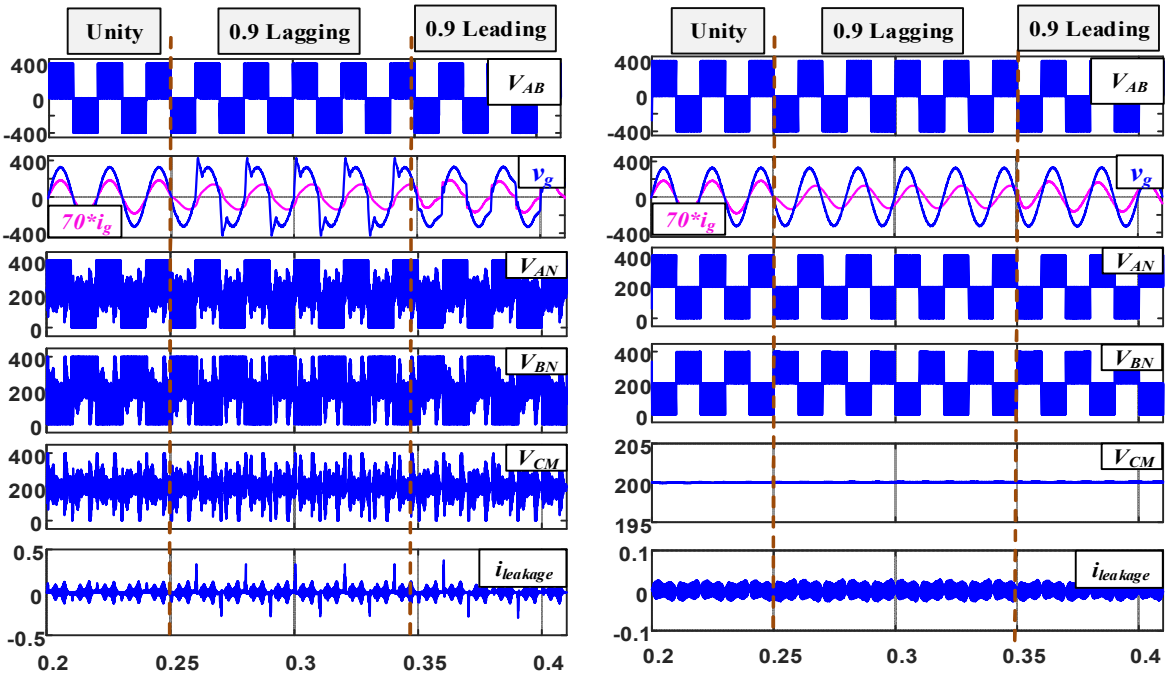
Table 3.2. System parameters

S. No	Parameters	Values
1	Input voltage	400 V
2	Inductor L_1, L_2	4 mH
3	Capacitors C_{dc1}, C_{dc2}, C_f, C_{PV}	1 mF, 1 mF, 2 µF, 42 nF
4	AC output voltage	230 V, 50 Hz
5	Switching frequency f_s	10 kHz
6	Output power	500 W
7	Resistances R_g, R_f	10 Ω, 5 Ω
8	Mosfet	IRFP460N
9	Diode	MUR1560



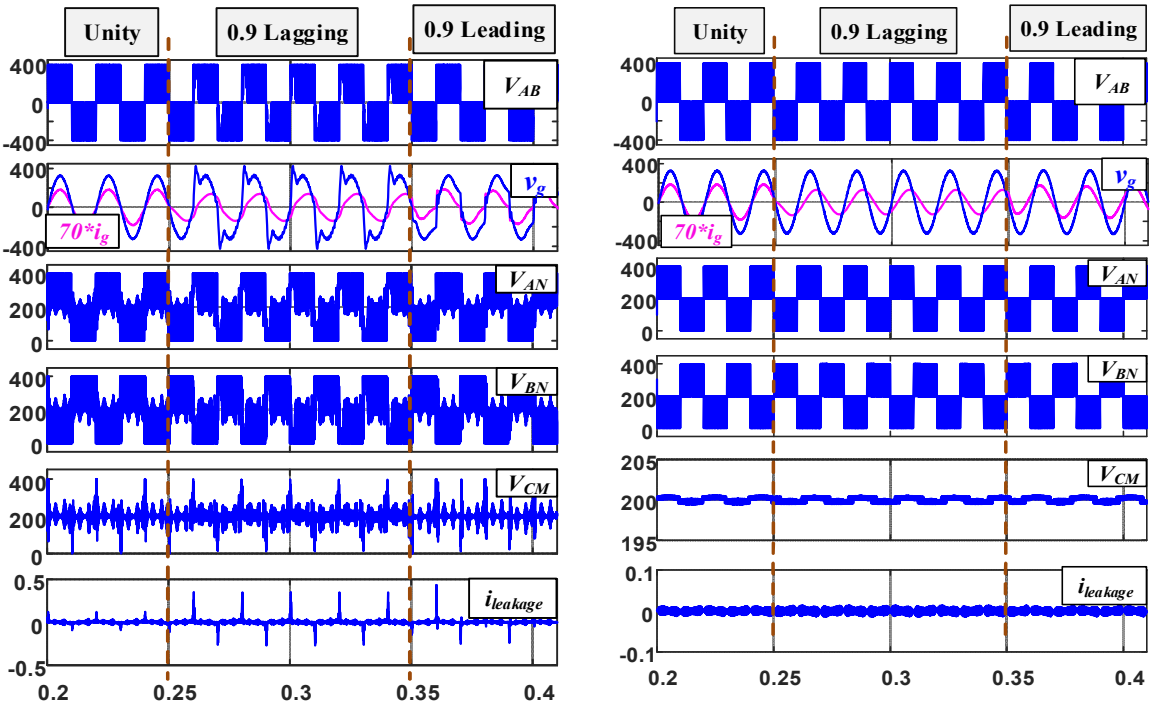
(a) (b)

Fig. 3.19. Differential mode and common mode results; (a) H5, (b) BDC-H5 inverter.



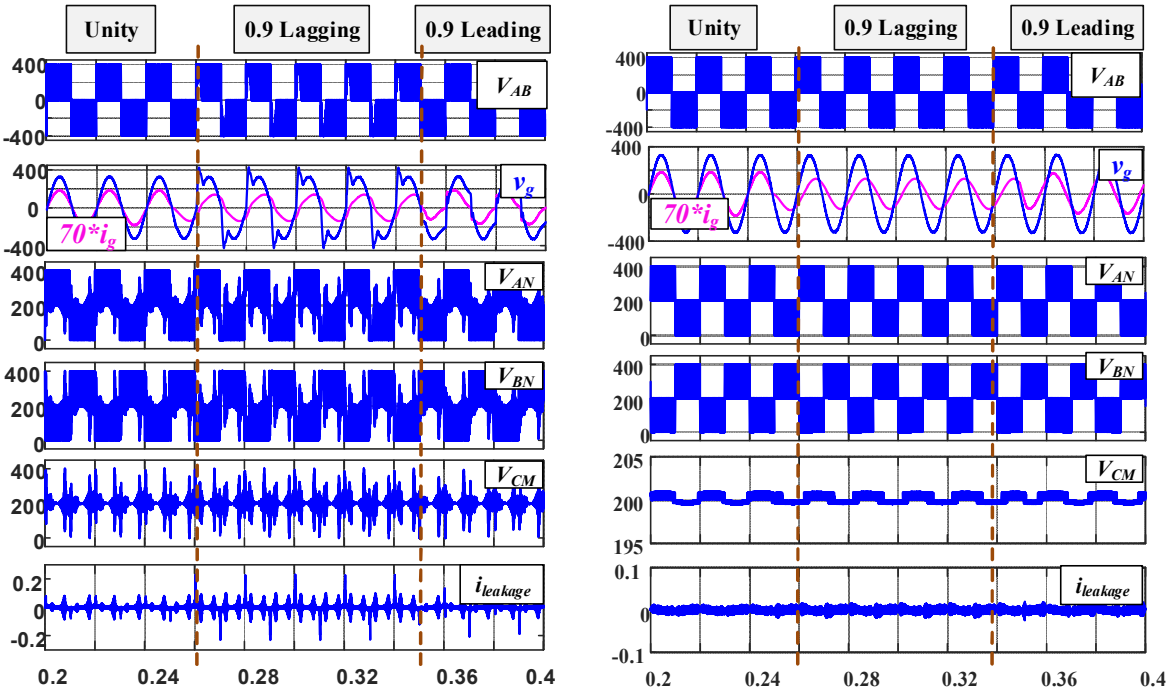
(a) (b)

Fig. 3.20. Differential mode and common mode results; (a) HERIC, (b) BDC-HERIC inverter.



(a) (b)

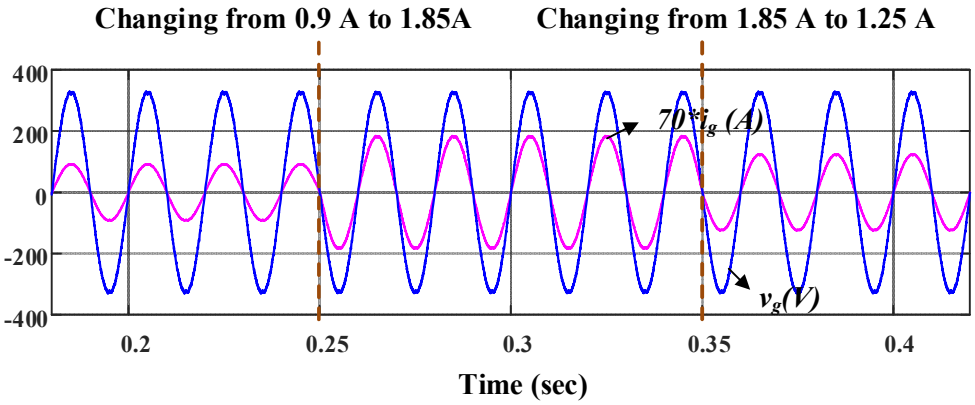
Fig. 3.21. Differential mode and common mode results; (a) H6, (b) BDC-H6 inverter.



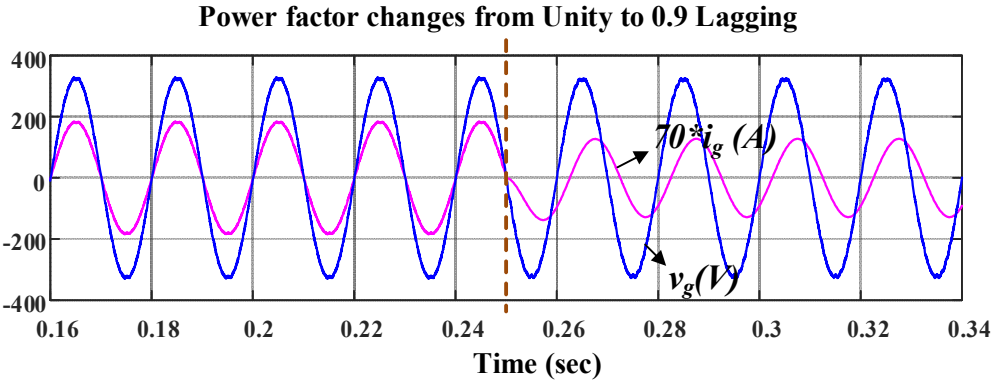
(a) (b)

Fig. 3.22. Differential mode and common mode results; (a) H-B, (b) BDC-H-B inverter.

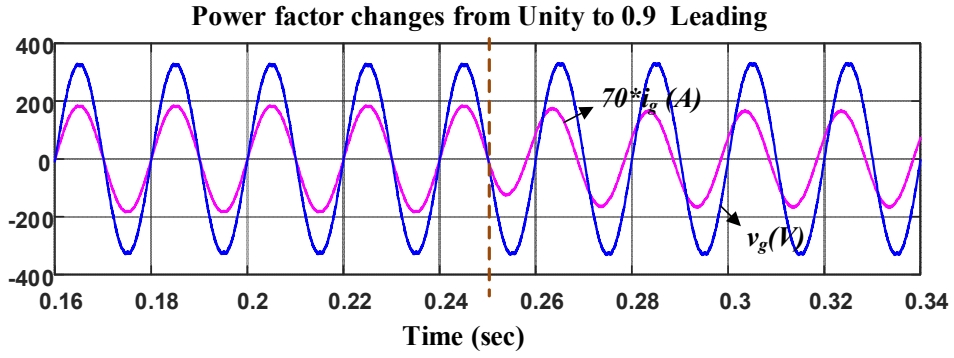
Further, the dynamic response of the BDC-H5 topology is tested and the results are given in Fig. 3.23. It is demonstrated that the improved modulation strategy and topology is working properly during sudden changes in grid conditions; Fig. 3.23 (a) show the step changes in grid current, Fig. 3.23 (b) and (c) shows the sudden change in grid power factor from unity to 0.9 lagging and unity to 0.9 leading, respectively.



(a)



(b)



(c)

Fig. 3.23. Dynamic response of BDC-H5 topology: (a) step changes in grid current; power factor changes from: (b) unity to lagging and (c) unity to leading.

3.6. Experimental Results

To prove the effectiveness of the proposed TLI topologies, a 500 W generalized inverter circuits were built and tested utilizing the available resources in the laboratory, as shown in Fig. 3.24. The system parameters used for the testing of both traditional and BDC based topologies, are listed in Table 3.2. Performance of all the topologies is tested under unity, 0.9 lagging (125 Ω, 400 mH) and 0.9 leading (125 Ω, 50 µF) conditions to validate the reactive power control capability. Also, an equivalent capacitance of 42 nF is placed between the terminals of DC power source to the ground for measuring the magnitude of leakage current caused due to oscillations in CMV. Differential voltage (V_{AB}), load voltage (v_l), load current (i_l), and leakage current ($i_{leakage}$) are shown in a single window to affirm the identical CMV behaviour in all the operating modes of proposed TLI topologies. MDO3024 and UT283A power quality meter was used to measure the leakage current magnitude and THD, respectively.

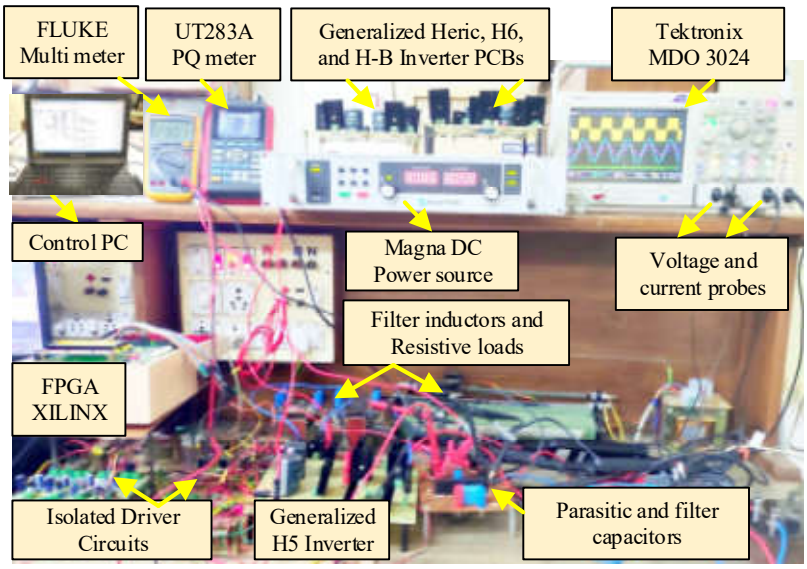


Fig. 3.24. Experimental test setup.

Figs. 3.25, 3.26, 3.27 and 3.28 illustrate differential mode (V_{AB}, v_l *and* i_l) and common mode (V_{AN}, V_{BN}, V_{TCMV} *and* $i_{leakage}$) characteristics of both traditional and BDC based H5, HERIC, H6 and H-B topologies, respectively. Moreover, the performance evaluation of all the topologies are listed in the Table. 3.3. Differential mode characteristics of both traditional and BDC-H5 topology are similar while operating under the unity power factor condition, as shown in Figs. 3.25(a) and (f). From Figs. 3.25(b) and (c); it is observed that the output waveforms of traditional H5 topology are distorted while operating in non-unity power factor conditions due to the absence of bi-directional current path during the freewheeling period. Whereas, in BDC-H5 topology, reliable output waveforms can be observed as shown in Figs. 3.25(g) and (h) due to the presence of bi-directional current path provided by the improved PWM scheme (as per the analysis given in Section. 3.3).

Further, common mode characteristics of the traditional H5 topology are illustrated in Figs. 3.25(d) and (e). Due to the effect of junction capacitance of the switches during the freewheeling period there exist oscillations in the total CMV. Moreover, these oscillations can excite the resonant circuit formed by the parasitic capacitance connected to the DC source and results in excess leakage current (as per the analysis given in Section. 3.2). Whereas, in BDC-H5 topology, an additional BDC branch is connected to clamp the V_{TCMV} to $V_{dc}/2$ and results in complete abolishment of such oscillations as shown in Fig. 3.25(i). Also, it further reduces the leakage current magnitude as shown in Fig. 3.25(j).

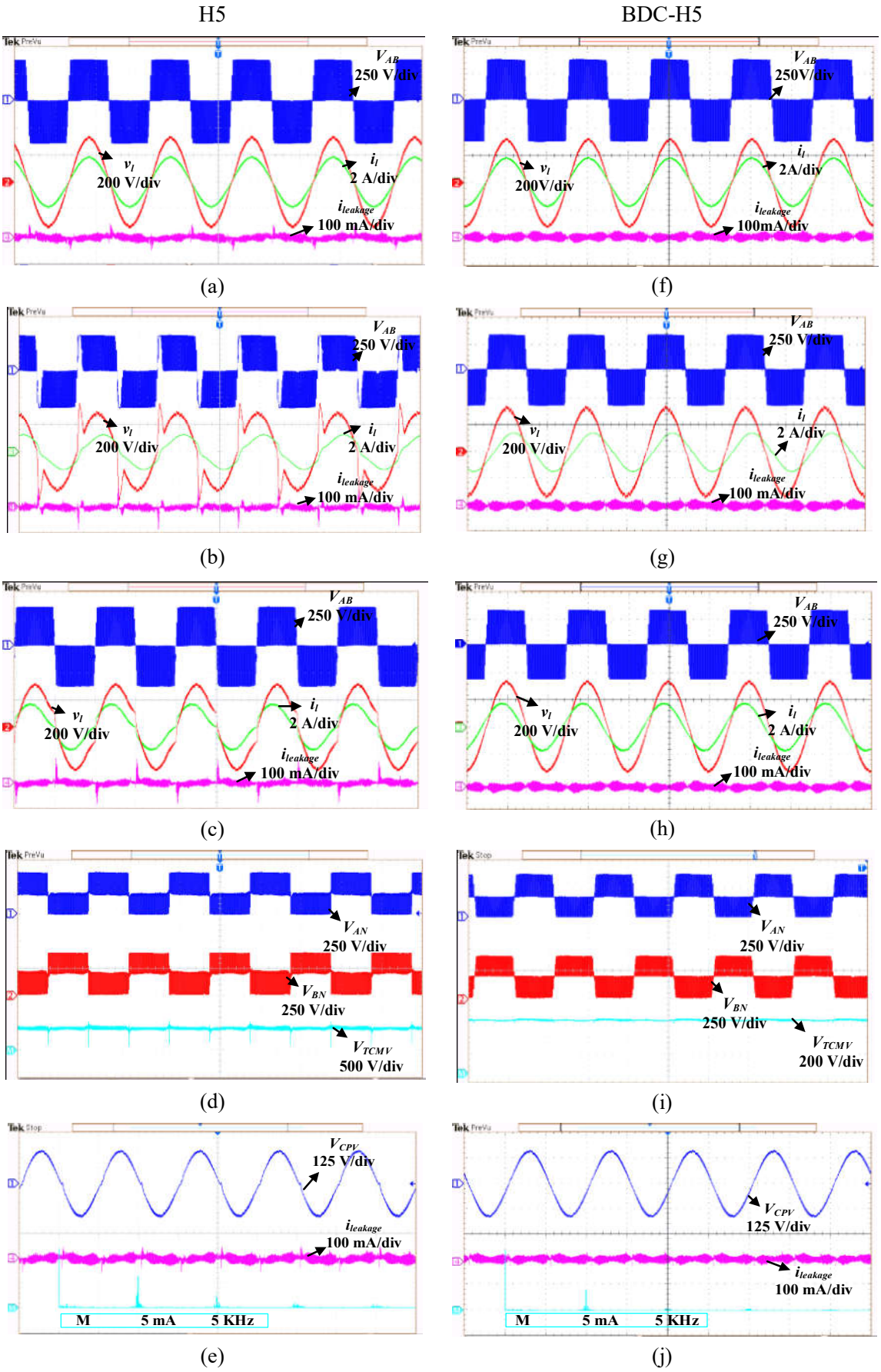
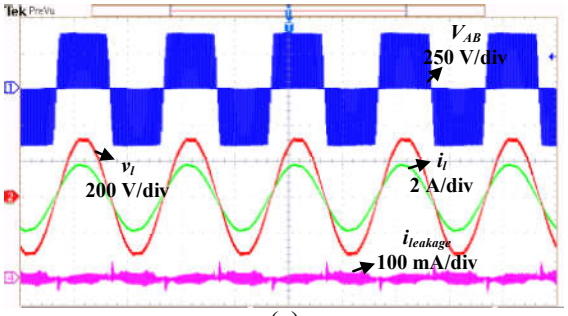


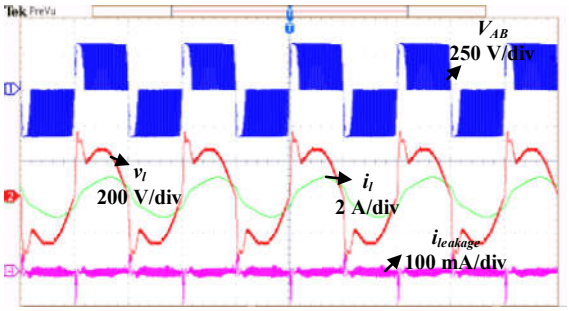
Fig. 3.25. Differential mode and common mode characteristics of H5 and BDC-H5 topologies.

Similarly, the experimental results of both traditional and BDC-based HERIC, H6 and H-B topologies are shown in Figs. 3.26 - 3.28 respectively. Where H-B and BDC H-B topologies are tested for unity, 0.6 lagging and 0.6 leading power factors to test the suitability of proposed topology and PWM strategy, especially for deplorable operating conditions of the standalone load.

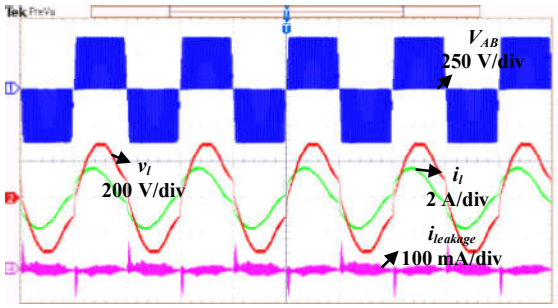
HERIC



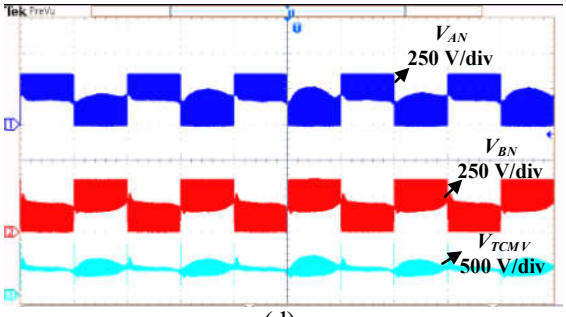
(a)



(b)

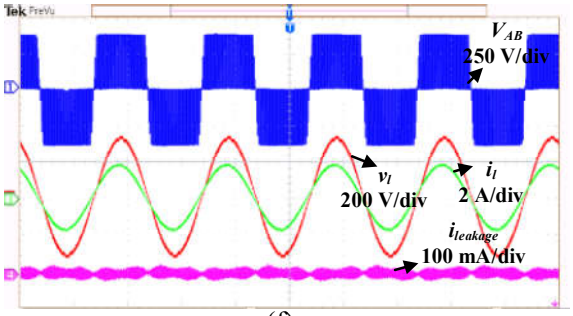


(c)

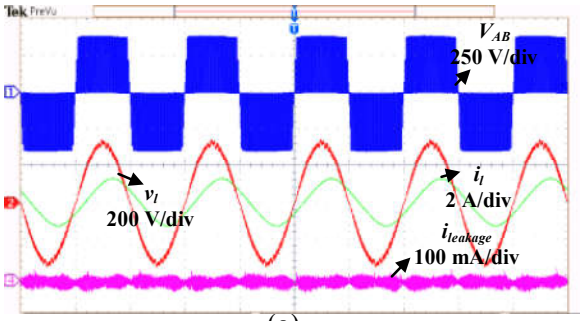


(d)

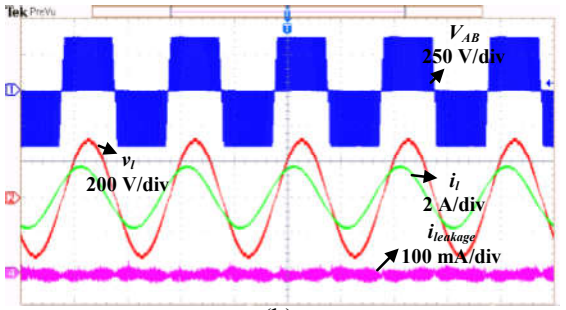
BDC-HERIC



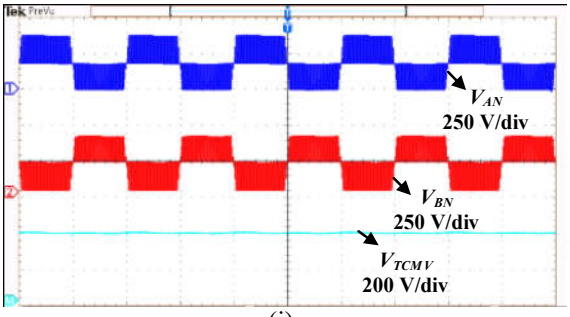
(f)



(g)



(h)



(i)

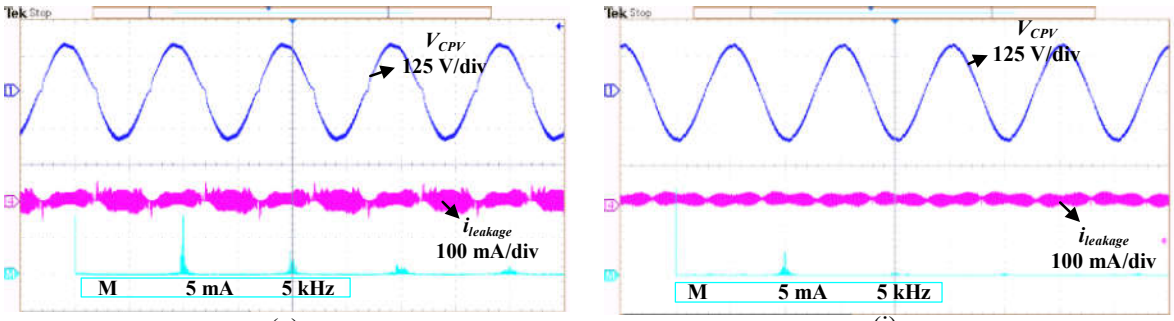
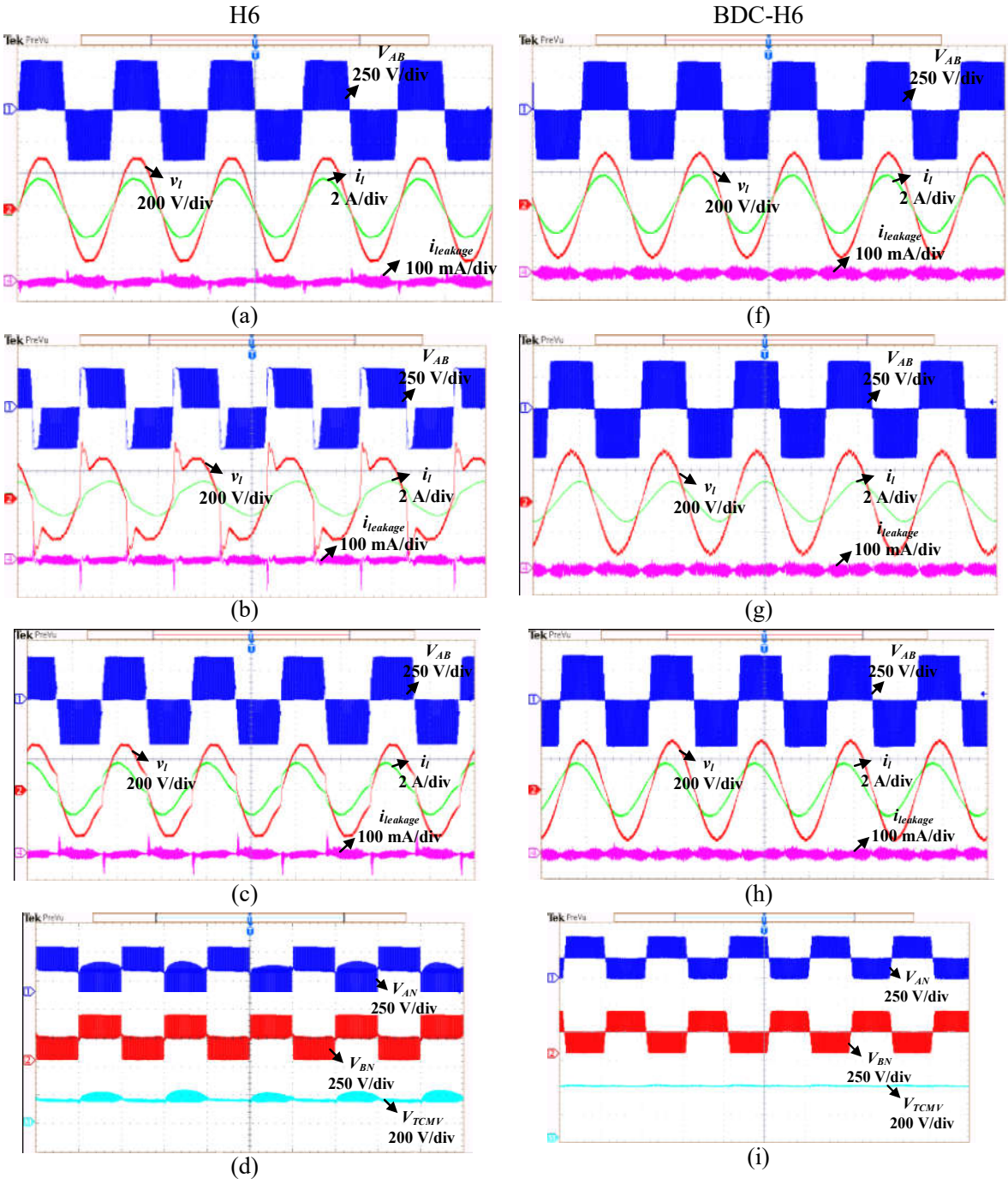
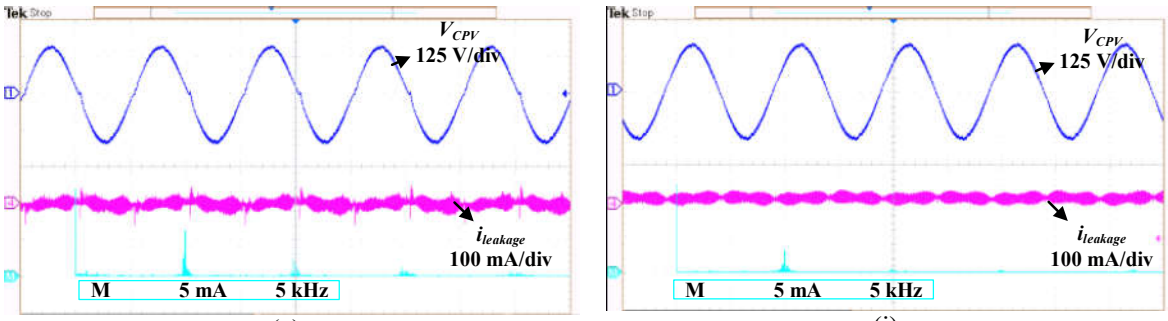


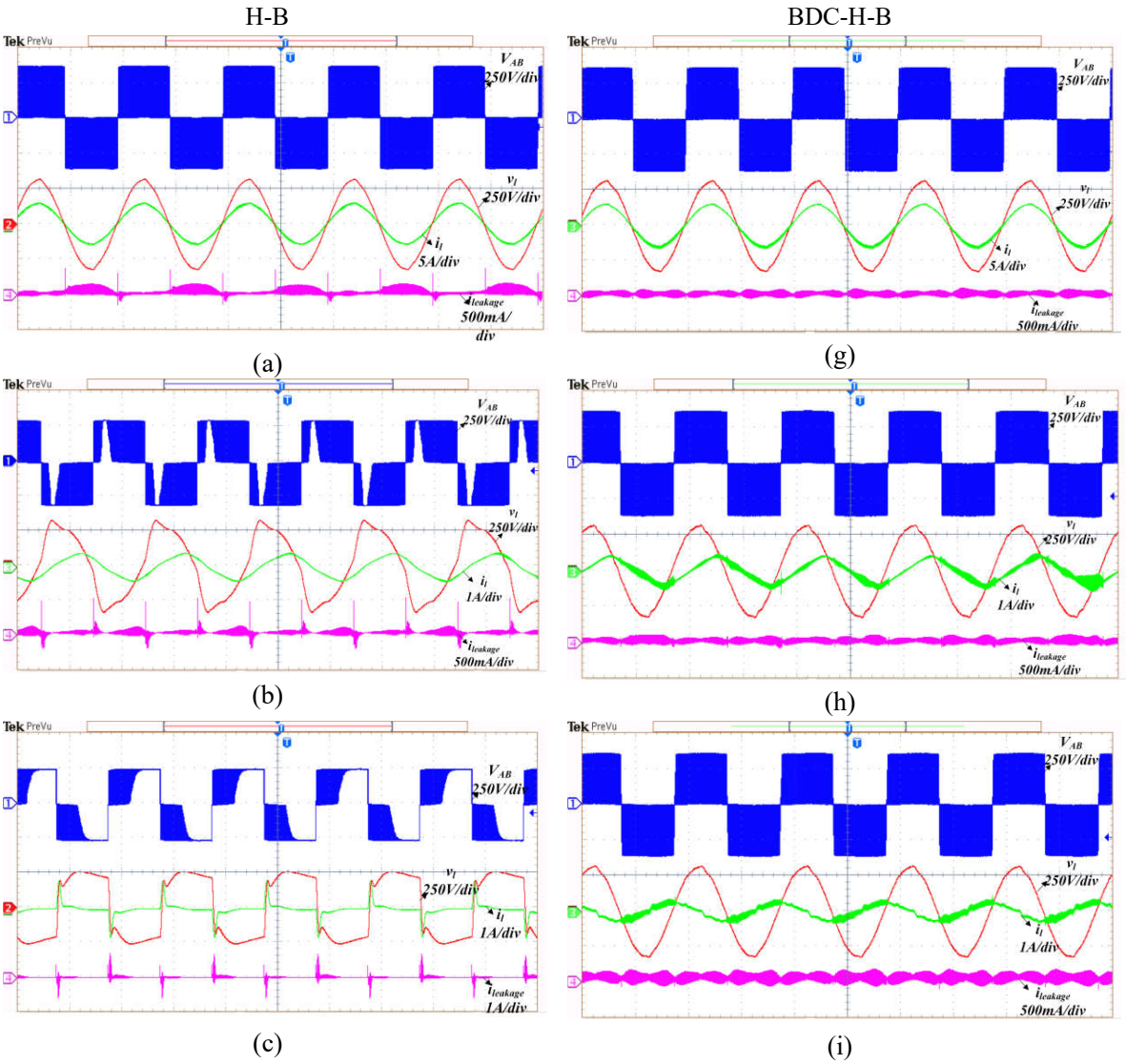
Fig. 3.26. Differential mode and common mode characteristics of HERIC and BDC-HERIC topologies.





(e) (j)

Fig. 3.27. Differential mode and common mode characteristics of H6 and BDC-H6 topologies.



(a) (g)

(b) (h)

(c) (i)

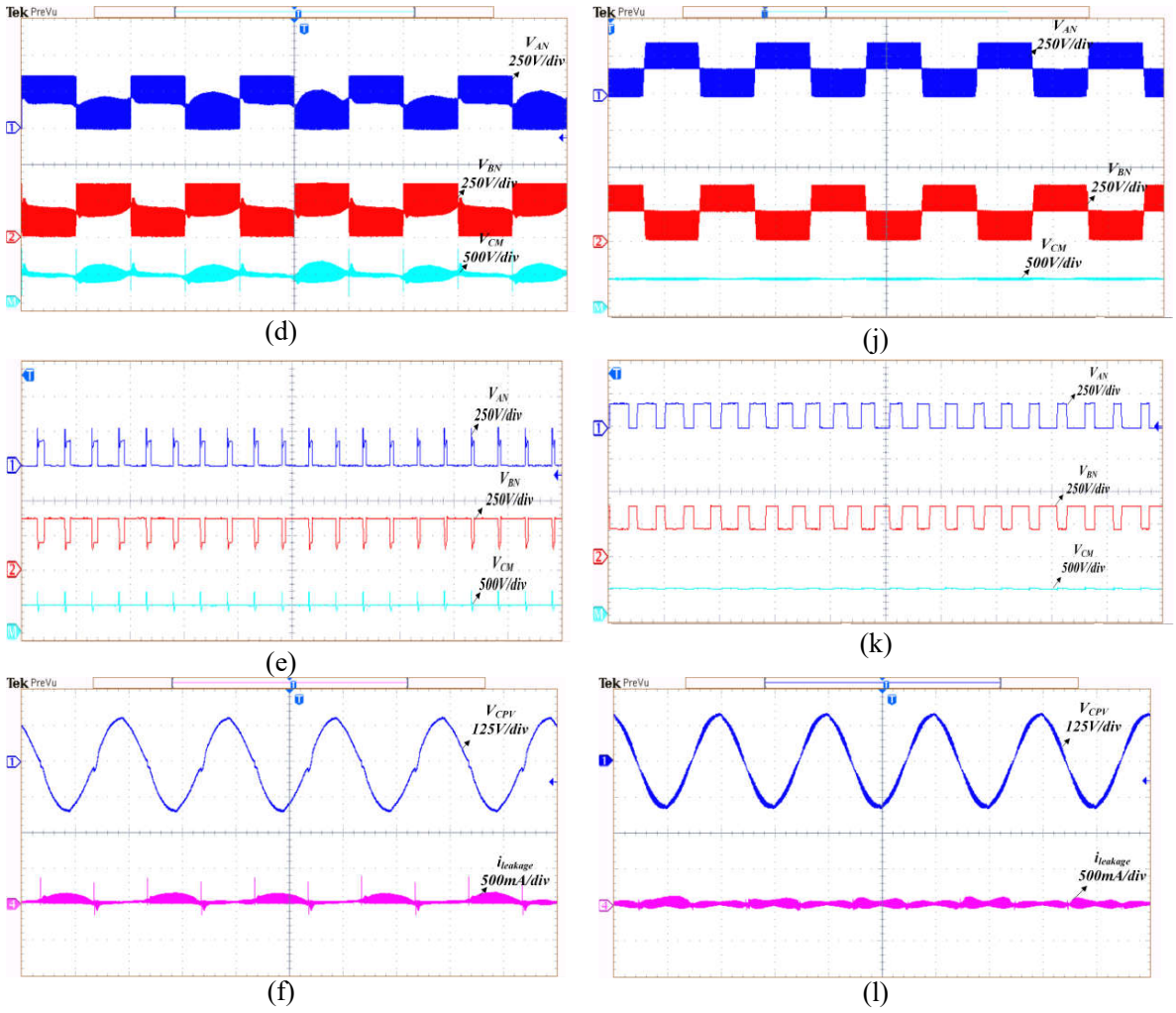
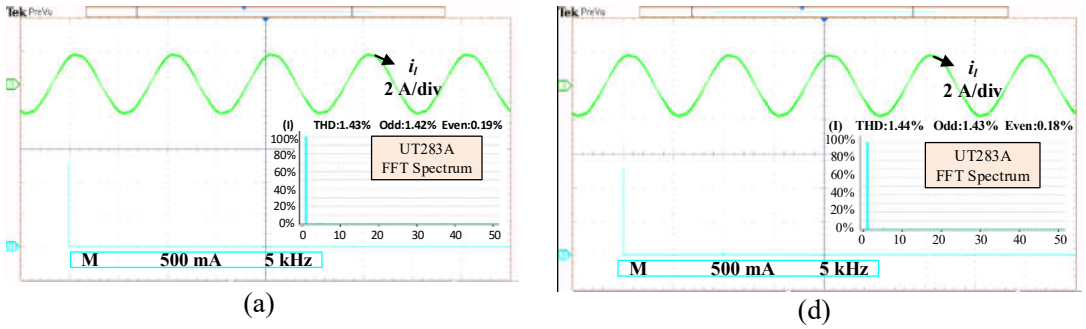


Fig. 3.28. Differential mode and common mode characteristics of H-B and BDC-H-B topologies.

Moreover, the performance evaluation of both traditional and BDC based topologies are listed in the Table. 3.3 for easy comparison. Further, Fig. 3.29 shows the THD measurement of output current waveforms (measured using MDO 3024 and UT283A 1-Ø power quality meter) at unity, 0.9 lagging and, 0.9 leading power factors of both traditional and BDC-H5 topology respectively. From the data given in the Table. 3.3; it is noticed that the measured %THD of the proposed topologies is less than the IEC61000-3-2 standard for all the operating conditions [45]. The RMS value of the leakage current is also less for BDC based topologies under different power factor conditions in comparison with traditional topologies. Therefore, both leakage current reduction and reactive power control capability are achieved by upgrading the traditional topologies with the BDC branch and improved modulation schemes, respectively.

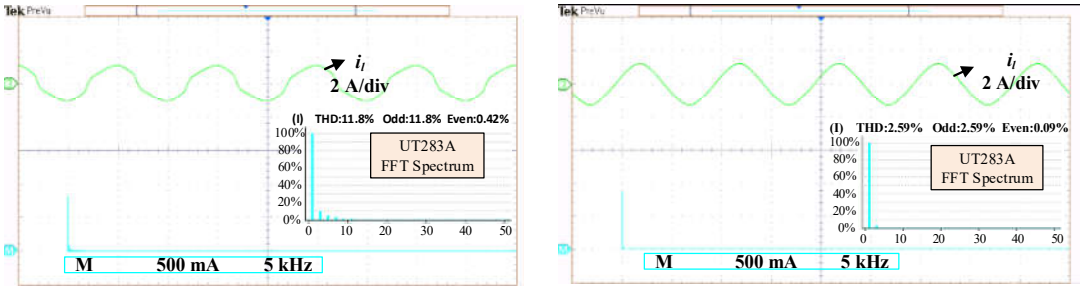
H5 BDC-H5

Unity power factor



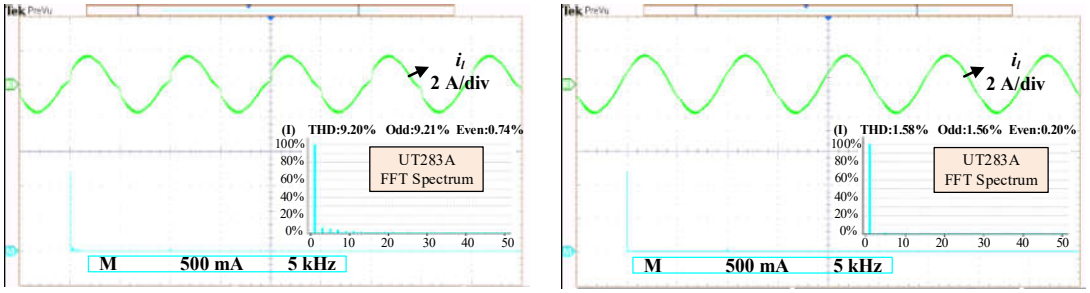
(a) (d)

Lagging power factor



(b) (e)

Leading power factor



(c) (f)

Fig. 3.29. THD Measurement of current waveforms for H5 and BDC-H5.

Table 3.3. Performance evaluation of the traditional and BDC based topologies

Features		H5	BDC-H5	HERIC	BDC-HERIC	H6	BDC-H6	H-B	BDC-H-B
PWM		Unipolar	Unipolar	Unipolar	Unipolar	Unipolar	Unipolar	Unipolar	Unipolar
Total No.of MOSFETs		5	7	6	8	6	8	6	8
Total No.of Diodes		0	0	0	0	2	2	2	2
Total No.of components conducting in one cycle		10	14	8	12	10	14	10	14
Total blocking voltage		$4.5*V_{dc}$	$5.5*V_{dc}$	$6*V_{dc}$	$7*V_{dc}$	$7*V_{dc}$	$8*V_{dc}$	$7*V_{dc}$	$8*V_{dc}$
Unity power factor	$i_{leakage\_RMS}$	16.4 mA	8.52 mA	21.9 mA	8.67 mA	12.4 mA	8.36 mA	13.5 mA	9.13 mA
	% THD	1.43 %	1.44 %	1.45 %	1.53 %	1.47 %	1.54 %	2.07 %	1.54 %
Lagging power factor	$i_{leakage\_RMS}$	22.5 mA	9.28 mA	27.6 mA	9.38 mA	18.05 mA	9.13 mA	36.2 mA	10.5 mA
	% THD	11.8 %	2.59 %	11.38 %	2.59 %	11.50 %	2.07 %	9.45 %	2.80 %
Leading power factor	$i_{leakage\_RMS}$	17.95 mA	8.55 mA	22.6 mA	8.7 mA	15.48 mA	8.06 mA	29.8 mA	9.56 mA
	% THD	9.20 %	1.58 %	10.76 %	1.68 %	11.28 %	1.71 %	8.67 %	1.86 %
Size of the CMF		Large	Small	Large	Small	Large	Small	Large	Small
Reactive power capability		No	Yes	No	Yes	No	Yes	No	Yes
CMV		Oscillating	Constant	Oscillating	Constant	Oscillating	Constant	Oscillating	Constant
Bi-directional current path during negative power region		Not present	Present	Not present	Present	Not present	Present	Not present	Present

3.6.1. Dynamic Performance

The dynamic performance of the BDC based topology under the grid-connected mode of operation is tested in real-time validation with OPAL-RT by using OP4500 modules [89]. Where two OP4500 modules of OPAL-RT are integrated, as illustrated in Fig. 3.30. To analyze the performance under various power factor conditions of the grid, one of the modules considered as a plant, that is BDC-based topology. Conversely, other module act as a controller, that is the PR controller given in Fig. 3.18. The plant module along with its interface, produces actual signals as per the operating conditions and sudden disturbances, which will be captured by a controller through the communication channel. The controller module generates the necessary modulation index (M_a) by the use of PR controller as explained in section 3.3.2, to validate the closed-loop operation of the proposed BDC based topology. The sampling time is selected as 100 µs, which produces the switching frequency of 10 kHZ. The overrun errors are eliminated with this selection of switching frequency. Hence the real-time validation will be more accurate. The front-view of the OPAL-RT module is illustrated in Fig. 3.31 with the access points for port A (digital input/output pins), port B (differential input/output pins), port C (analog input/output port) and port D (computer connection port).

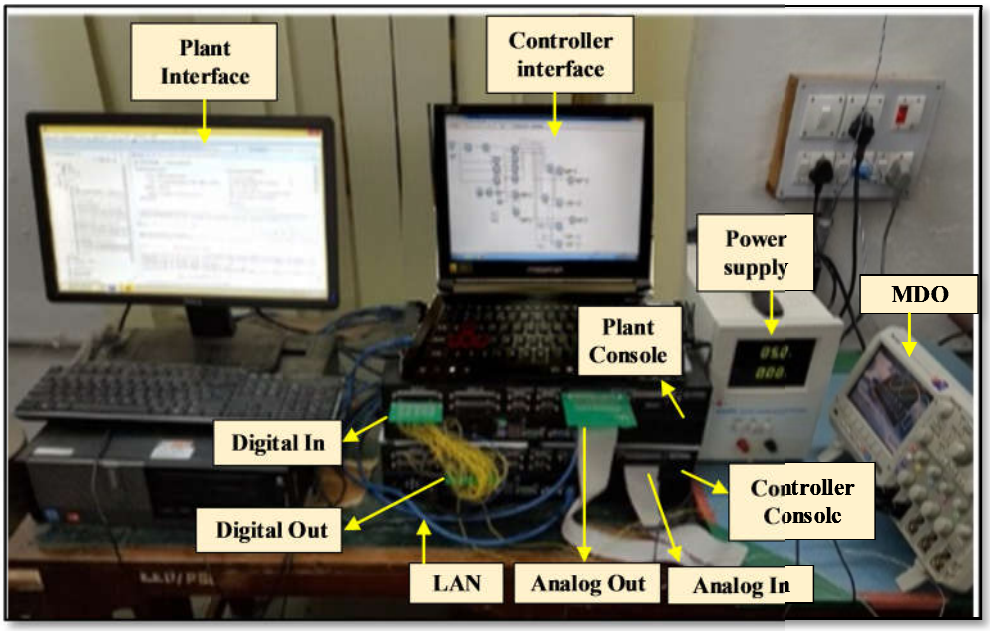


Fig. 3.30. OPAL-RT real-time environmental setup.

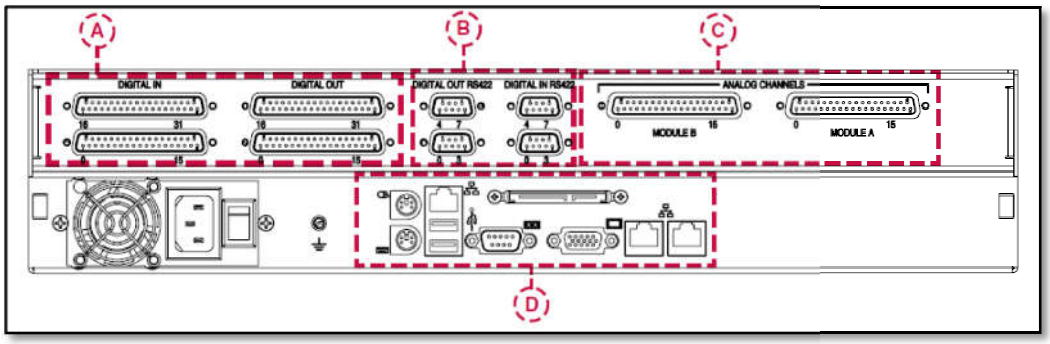
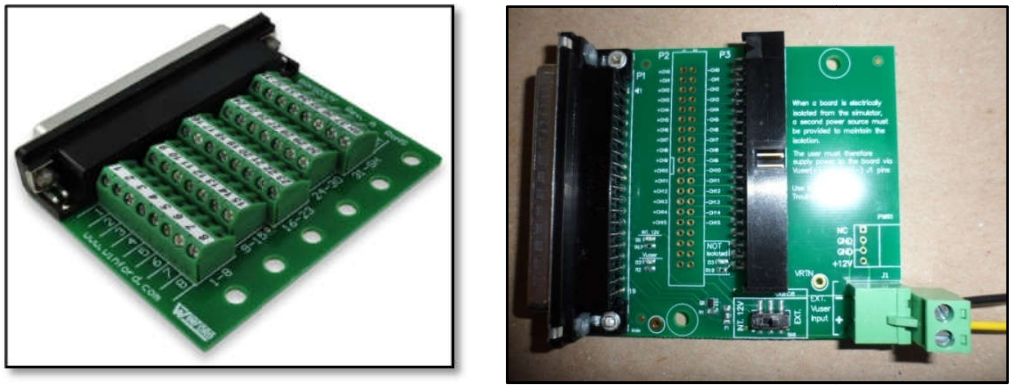


Fig. 3.31. Front view of OP4500 module.

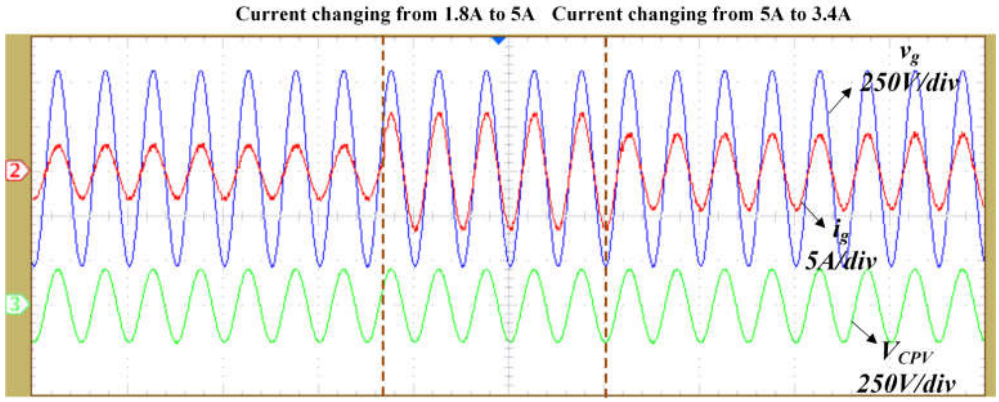


(a) (b)

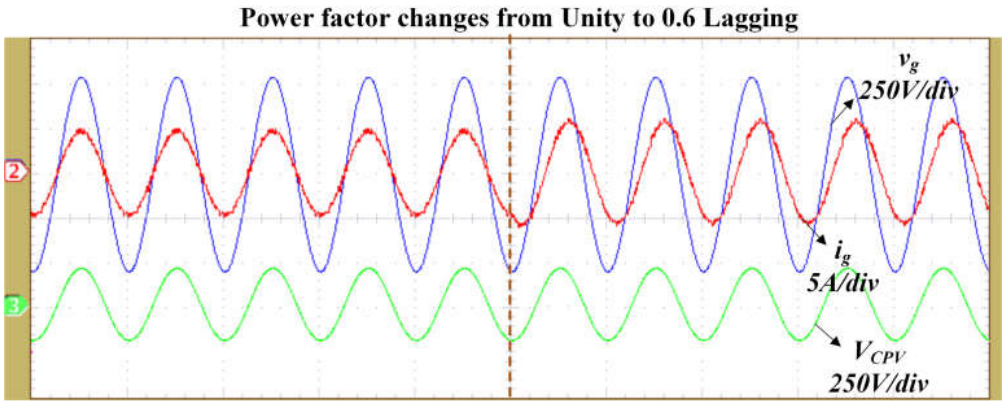
Fig. 3.32. DB 37; (a) Digital port, (b) Analog port.

Fig. 3.32 shows the connector DB 37, useful for connecting the ports A and C, respectively. Each DB 37 can access 16 pins associated I/Os (i.e., either analog or digital). With these interactions and involved interfacings between two OP4500 modules, a hardware-in-loop (HIL) system of the proposed BDC based topology along with a closed-loop control system can be realized.

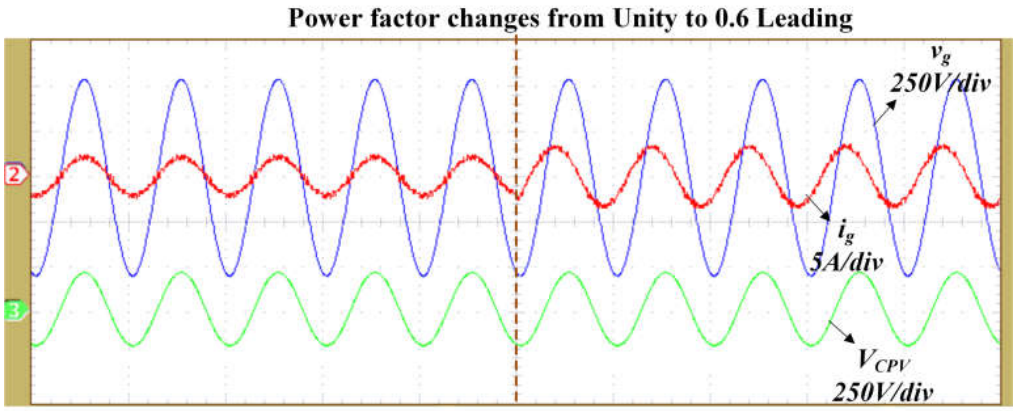
The responses under step-change in real and reactive powers are captured by MDO 3024. Fig. 3.33 (a) shows the step-change in grid current from 1.8 A to 5 A and then 3.4 A (i.e., by changing reference active power). Figs. 3.33 (b) and (c) shows the grid voltage and current waveforms when power factor changes from unity to 0.6 lagging and unity to 0.6 leading respectively (i.e., by changing reference reactive power by keeping real power is constant). In all these figures, voltage across C_{PV} is also captured for the validation similar common-mode characteristics under different power conditions of grid. From Fig. 3.33, it can be observed that the BDC based topologies are capable of support the reactive power control with superior quality of waveforms in comparison with the traditional topologies. Moreover, the controller implementation is the same for the other proposed topologies.



(a)



(b)



(c)

Fig. 3.33. Dynamic response of the BDC-H-B topology: (a) step change in the grid current, transient change in power factor from (b) unity to lagging and (c) unity to leading.

3.7. Evaluation of Efficiency using PSIM Themal Module

The PSIM thermal module enables the quick way of estimating the losses of power semiconductor devices based on real device characteristics provided by the manufacturer datasheet. The characteristics of various devices can be added by using a device database

editor in PSIM. Then, the devices can be selected for PSIM model and their switching and conduction losses can be calculated in the simulation. Both static (conduction voltage drop, on-state resistance, etc.,) and dynamic (turn-on, turn-off transients) characteristics are taken in to account in the simulation. Using the device voltage and current calculations during the simulation period, PSIM accesses the device database and then evaluated the conduction and switching losses. The detailed procedure for evaluating the losses of power semiconductor devices using the PSIM thermal module is given in refs [90]-[92]. In this context, the efficiency of both traditional and proposed topologies are evaluated using the thermal module toolbox in PSIM software. For example, a snapshot of the traditional H5 inverter, which is implemented using the PSIM thermal module, is given in Fig. 3.34.

Where each MOSFET consists of four nodes for power losses and they are: MOSFET conduction loss P_{C_Q}, MOSFET switching loss P_{S_Q}, body diode conduction loss P_{C_D} and body diode switching loss P_{S_D}. Generally, these losses are in the form of currents flowing out of these nodes measured by ammeters. To model the thermal behavior of each switch with respect to ambient temperature of 40°C ($T_{\_ambient}$), an equivalent resistance R_{eq} of 0.79Ω (R_{th_jc} + R_{th_cs} +$R_{\_heatsink}$) in series with the DC source is connected. Where R_{th_jc} is thermal resistance between junction to the casing, R_{th_cs} is thermal resistance between casing to a heat sink, R_{th_sa} is the thermal resistance between heat sink to ambient.

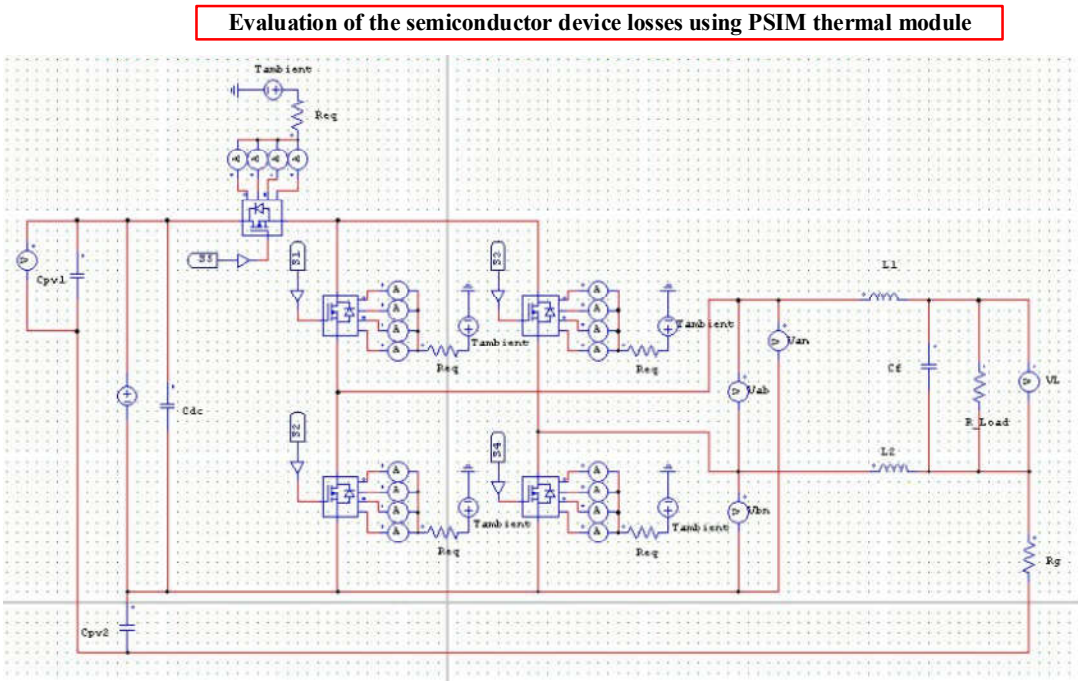


Fig. 3.34. PSIM thermal model for the traditional H5 inverter.

Finally, efficiency curves of both traditional and BDC based H5, HERIC and H6 topologies are drawn in Fig. 3.35 under the same test conditions as given in the Table. 3.2. The number of conducting devices and total blocking voltage are the same for the both BDC based H6 and H-B topologies. Hence the efficiency curves are superimposed on one another. Moreover, the proposed topologies registers slightly lower efficiency due to increased power losses in the additional BDC branch in comparison with the traditional topologies. However, the leakage current reduction and reactive power control capability of the proposed topologies attracts the attention of researchers in the future PV power generation systems.

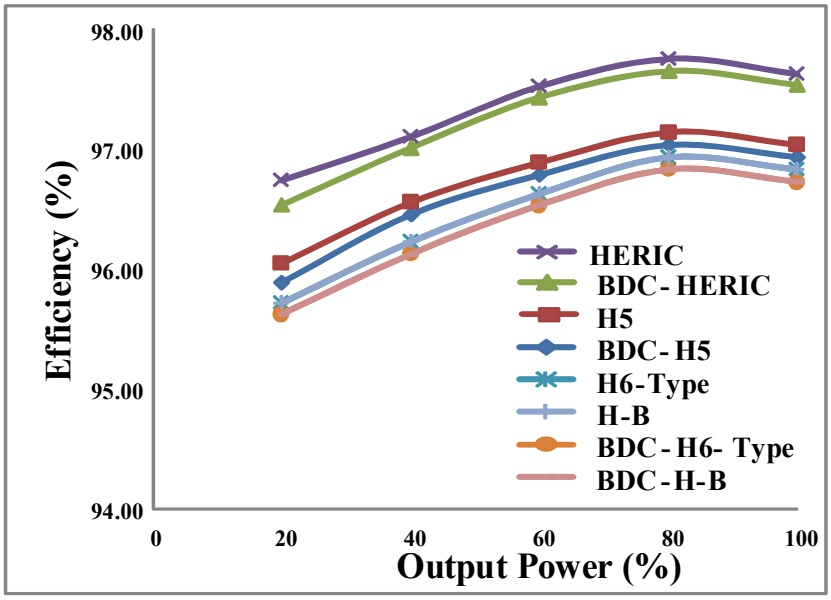


Fig. 3.35. Efficiency curves of the both traditional and BDC topologies.

3.8. Summary

In this chapter, BDC based H5, HERIC, H6 and H-B TLIs are proposed with the features of reactive power control capability and reduced leakage current. Improved modulation schemes enable the inverters to operate in both unity and non-unity power factor condition without losing waveform quality. Moreover, the additional BDC branch maintains constant CMV (half of the input DC voltage) in all the operating modes of the inverter. Thus, the magnitude of leakage current is reduced in the proposed topologies. Finally, the performance of both traditional and BDC based topologies is validated through simulation and experimentation and also their results are compared to highlight the novelty of proposed configurations.

3.9. Contributions

Bi-directional clamping based H5, HERIC, H6, and Hybrid TLI topologies for PVPGS are proposed to achieve;

a) Reduced leakage current by abolishing the fluctuations in V_{TCMV} due to switch junctions capacitances.

b) Reactive power capability with a modified SPWM technique.

c) Reduction of the number of components compared to the classical decoupling and clamping based single-stage three-level inverters.

3.10. Papers Published

1) Sateesh Kumar Kuncham, Kirubakaran Annamalai, and Subrahmanyam Nallamothu, **"An Improved Hybrid-Bridge Transformerless Inverter Topology with Bi-Directional Clamping and Reactive Power Capability,"** *IEEE Transactions on Industry Applications*, vol. 55 (6), pp. 7400-7409, May. 2019.

2) Sateesh Kumar Kuncham, Kirubakaran Annamalai, and Subrahmanyam Nallamothu, **"Bi-Directional Clamping Based H5, HERIC and H6 Transformerless Inverter Topologies with Reactive Power Capability,"** *IEEE Transactions on Industry applications* (DOI: 10.1109/TIA.2020.2999552).

3) K. Sateesh Kumar, A. Kirubakaran, N. Subrahmanyam **"Bi-Directional Clamping Based H5, HERIC and H6-Type Transformerless Inverter Topologies with Improved Modulation Technique,"** *IEEE PESGRE Conference, pp.1-6, 2020.*

Chapter 4

A Two-Stage Seven-Level Power Conditioner for Photovoltaic Applications

Chapter 4

A Two-Stage Seven-Level Power Conditioner for Photovoltaic Applications

4.1. Introduction

The single-stage topologies proposed in the previous chapter are mostly suitable for string inverters and have the advantages of reduced switch count, lower leakage current and reactive power control capability for the grid-connected PVPGS. This chapter proposes a two-stage power conditioner with inherent benefits of boosting, generation of seven-level output voltage with minimum leakage current in a grid-connected PVPGS, which is especially suitable for multi-string applications.

The proposed power conditioner is an upgrade of a front-end multi-output DC-DC boost converter and an asymmetrical seven-level inverter. An *HFT* employed in front-end converter produces balanced DC-link voltages to generate the seven-level output voltage. The leakage current caused by the parasitic capacitance of the PV panel is minimized by providing a common-mode conducting path to the inverter. This results in a reduction of the leakage current well below the VDE0126-1-1 grid standards. Further, the proposed configuration utilizes a minimum number of devices for every level generation, which reduces the control complexity and also improves the system efficiency. The dynamic performance of the system is tested for intermittent changes in the PV characteristics for grid-connected operation. The proposed power conditioner is simulated using MATLAB software and a laboratory prototype of 750 W was developed to validate its feasibility. Finally, a comparison is made with other recently proposed seven-level inverters to highlight the benefits of this power conditioner over others.

4.2. System Configuration

Fig. 4.1 depicts the proposed power conditioner, which comprises a front-end DC-DC converter and an asymmetrical MLI. The front-end DC-DC converter boosts the output voltage of the PV source to the grid voltage level and also produces two isolated voltages of $(2/3)V_{dc}$ and $(1/3)V_{dc}$. The switching operation of the complementary switches in the boost converter and *HFT* ensures proper voltage balancing of the DC-link capacitors. Further, the inverter generates a seven-level output voltage with six semiconductor switches. The *LC* and common-mode filters (CMF) are connected across the output of the inverter to limit the high-frequency oscillations in the CMV and it will be explained in section 4.3. The detailed operation of the proposed configuration is as follows;

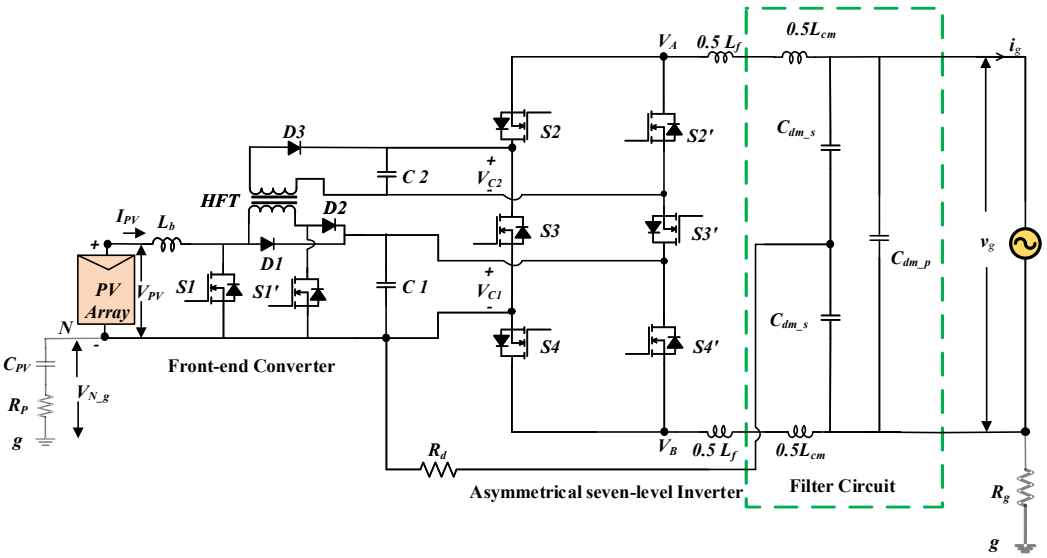


Fig. 4.1 Proposed single-phase two-stage power conditioner.

4.2.1. Front-end DC-DC Boost Converter

The front-end DC-DC boost converter is derived from the conventional boost converter in combination with a (2:1 turns ratio) *HFT* to produce two different DC voltages. The front-end converter is operated in two distinct modes such as boosting mode and current fed forward converter mode to produce $(2/3)V_{dc}$ and $(1/3)V_{dc}$ voltages, as shown in Figs. 4.2(a) and (b). In boost mode inductor L_b, diode *D1* and switch *S1′* are operated to produce a voltage across capacitor *C1*. Similarly, in current fed forward converter mode inductor L_b, *HFT*, diodes *D2*, *D3* and switches *S1*, *S1′* are operated to charge the capacitor *C2*. Switches *S1* and *S1′* are complementary to each other. When switch *S1* is OFF

and the complementary switch *S1'* is ON, capacitor *C1* is connected across the primary of the *HFT* through diode *D1* and switch *S1'* as shown in Fig. 4.2(b). The stored energy in the inductor and the input PV source charges capacitor *C1*. Since capacitor *C2* is connected to the secondary of the *HFT* through diode *D3*, half of the primary voltage is applied to charge capacitor *C2*. Hence, the voltages across the two DC-link capacitors are maintained at V_{C1} and V_{C2}. From Fig. 4.2(a), when switch *S1* is conducting, inductor 'L_b' stores the energy from the source and magnetizing current in the transformer winding discharges through the capacitor *C1* and diode *D2*.

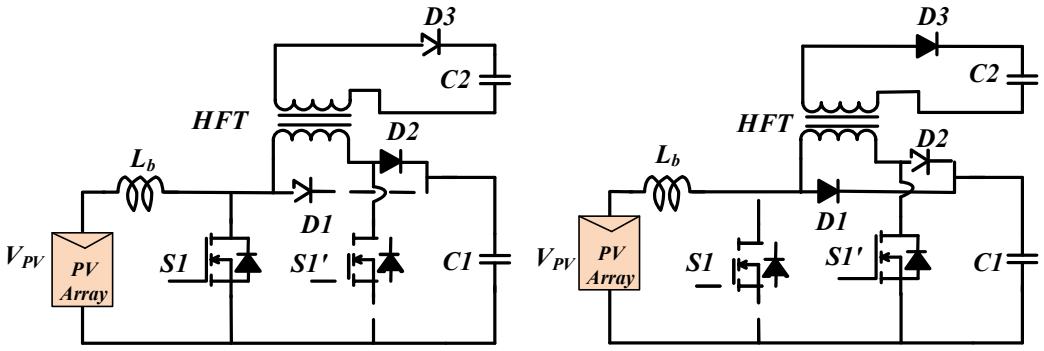


Fig. 4.2 Operation forward boost converter (a) S1 is ON, (b) S1 is OFF.

Since, stored energy in the magnetizing inductance is transferred to the output capacitors *C1* and not back to the source, the output power efficiency improves. Moreover, capacitor *C1* and *C2* are charged in parallel by using the *HFT* of the converter, which ensures the voltages to be in asymmetric (2:1) in nature [78]. Moreover, power transferred to the *HFT* is only 33% of rated power; this reduces the power rating and losses of the *HFT*. Assuming the converter is operating in continuous conduction mode (CCM), the voltage across the capacitors can be expressed as follows:

$$V_{C1} = \frac{1}{1-D} V_{PV} \tag{4.1}$$

$$V_{C2} = \frac{1}{2*(1-D)} V_{PV} \tag{4.2}$$

4.2.2. Asymmetrical Seven-Level Inverter

In this work, a popular asymmetrical MLI reported in [55], [93], is considered to realize the seven-level output. It consists of six active switches *S2, S2′, S3, S3′, S4, S4′*. Switches *S2′, S3′* and *S4′* that are complementary to switches *S2*, *S3 and S4,* respectively. Therefore three independent states would give (2^3=8) eight active states. The asymmetrical seven-level inverter is fed with voltages V_{C1} and V_{C2}, which are generated from the multi-output DC-DC boost converter. In any of the switching state, three switches are in conduction to realize the output AC voltage. Table 4.1 shows the different switching states corresponding to each level generation. The voltage blocking capability of the switch pairs (*S2, S2′*), (*S3, S3′*) and (*S4, S4′*) are V_{C2}, (V_{C1}+V_{C2}), V_{C1} respectively. The control pulses to the inverter switches are produced using the sinusoidal level-shifted pulse width modulation (SLSPWM) technique.

Table 4.1 Switching state of the asymmetrical seven-level inverter

Modes	Switching Scheme						Source Combination
	S2	*S3*	*S4*	*S2′*	*S3′*	*S4′*	
Positive	1	0	0	0	1	1	V_{C2}
	0	0	1	1	1	0	V_{C1}
	1	0	1	0	1	0	V_{C1}+V_{C2}
Zero	0	0	0	1	1	1	*0*
	1	1	1	0	0	0	
Negative	0	1	0	1	0	1	-(V_{C1}+V_{C2})
	1	1	0	0	0	1	-V_{C1}
	0	1	1	1	0	0	-V_{C2}

4.2.3. Closed-loop Control System

The development of a suitable controller plays a major role in extracting maximum power from the PV source into the grid. The basic functions of the controller are MPPT from PV, DC-link voltage balancing, generation of seven-level output voltage and injecting current into the grid. Hence, two control loops are developed with proportional-integral (*PI*) and proportional-resonant (*PR*) controllers [94], [95]. The outer loop *PI* controller performs the voltage control, while the inner loop *PR* controller achieves the current control loop. Thus the

overall controller facilitates the regulation of intermittent variations in PV characteristics. A simple perturb and observation (*P* and *O*) algorithm is used to extract the maximum power from the PV panels [96]. An inner loop current control and outer loop voltage control are developed to limit the effect of inductor current ripple and capacitor voltage ripple on the performance of MPPT by decoupling the PV panel operating conditions from perturbations at load/grid as shown in Fig. 4.3.

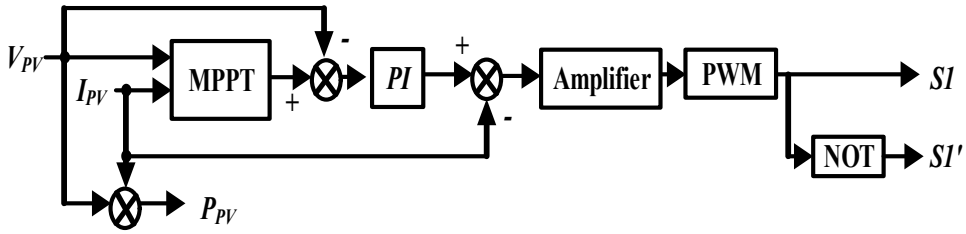


Fig. 4.3. MPPT control block.

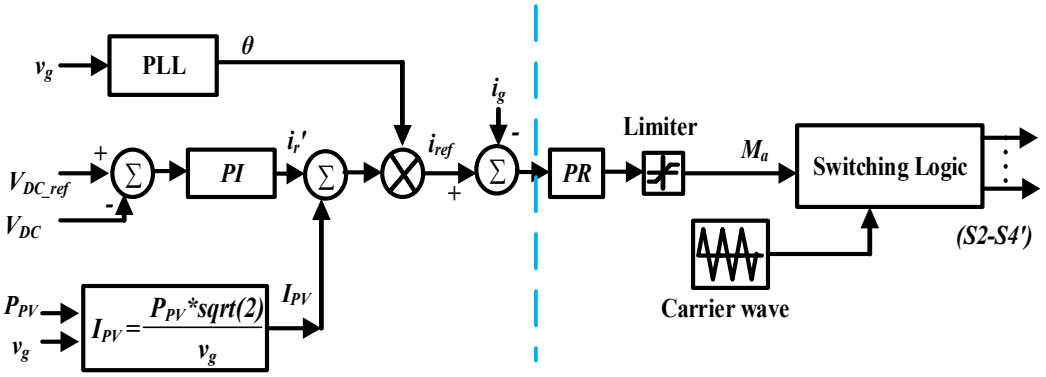


Fig. 4.4. Closed-loop control of inverter.

Further, to inject generated PV current into the grid by preserving constant DC-link voltage, a two-loop controller is developed and is shown in Fig. 4.4. The DC-link voltage control gives the reference grid current and then the improved *PR* controller generates the modulation index M_a, which is further fed to the SLSPWM logic block to produce the switching pulses for inverter switches as shown in Table 4.1. An improved *PR* controller [95] is used for injecting current into the grid. It has the advantage of limiting the steady-state error and is also robust in the control of inverter voltage due to parameter variations. Thus, improved *PR* controller performance is far better when compared with the *PI* controller. Phase locked loop (PLL) circuit is used to generate in-phase current to

grid voltage. The transfer function of *PI* and improved *PR* controller are given as follows;

$$G_{PI}(s) = K_P + \frac{K_I}{S} \tag{4.3}$$

$$I_{PV} = \frac{P_{PV} * \sqrt{2}}{v_g} \tag{4.4}$$

$$G_{PR}(s) = K_P + \frac{2K_r\omega_{PR}s}{s^2 + 2\omega_{PRc}s + \omega_1^2} \tag{4.5}$$

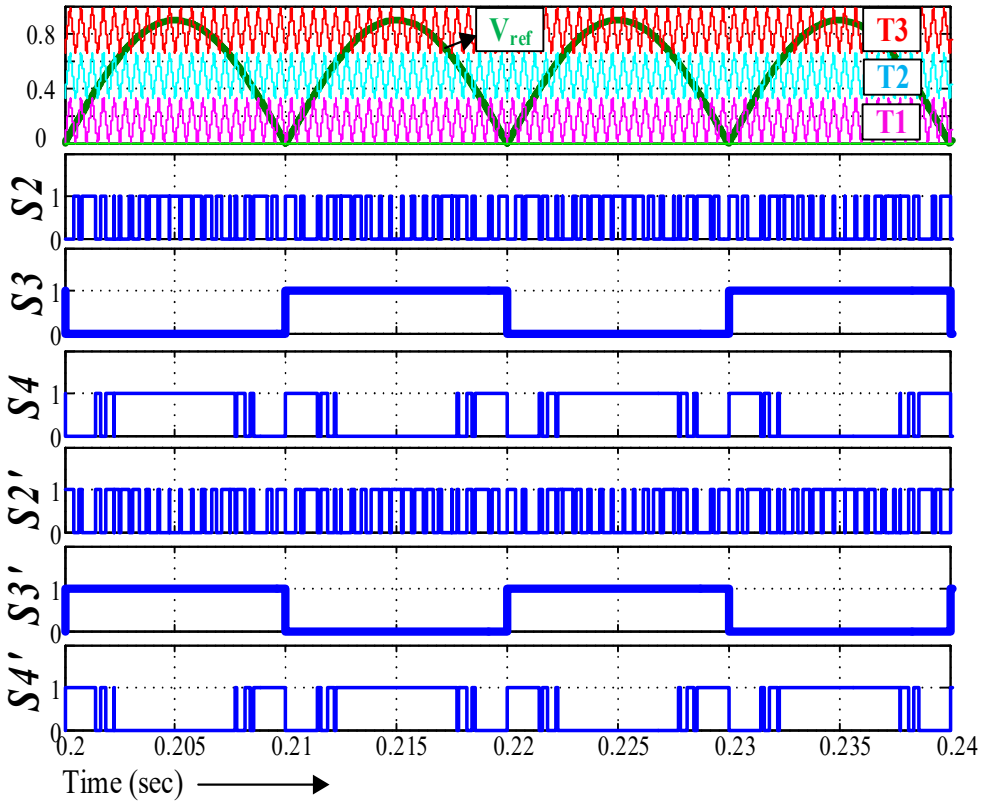


Fig. 4.5. Simulation waveforms of SLSPWM and corresponding gate pulses to the inverter switches.

Further, to show the closed-loop controller performance, the proposed power conditioner and its controller are developed in MATLAB environment for a maximum PV power capacity of 1.26 kW and a simple *P* and *O* MPPT algorithm is used to track the maximum power from the PV source. The specifications considered for the PV source are as follows: voltage, current and power at maximum power V_{MP} = 19.2 V, I_{MP} = 3.64 A and P_{MP} = 70 W,

respectively. A total of three parallel rows of six panels are connected in series (N_S = 6, N_P = 3) to generate the power of 1.26 kW at a standard temperature of 25^{o}C and insolation of 1000 W/m^2. Various details of the parameters considered for simulations are given in Table 4.2. Fig. 4.5 shows the gate pulses generated by the SLSPWM technique for driving the inverter switches. To inject active power (P) into the grid, the inverter produces a voltage V_r having a phase and the same is given in equations (4.6) and (4.7). In the case of P = 1.26 kW, V_{ac} = 230 V, (L_f+L_{CM}) = 5.25 mH, R = 0.1 Ω, V_r = 230.54 V, δ = 0.039 in radians [12].

$$\delta = arctan\left(\frac{2\pi f\left(L_f + L\right)P}{V_{ac}^2 + RP}\right) \tag{4.6}$$

$$V_r = \left(V_{ac} + \frac{RP}{V_{ac}}\right)\frac{1}{cos\,\delta} \tag{4.7}$$

Fig. 4.6 shows the simulation results of the proposed seven-level power conditioner with closed-loop control. Figs. 4.6(a) to (e) and 4.6(f) to (j) show the waveforms corresponding to insolation changes from 1000 W/m^2 to 800 W/m^2 and vice-versa. Figs. 4.6(a) and (f) show the PV power versus voltage characteristics for various insolation changes. The variations in output PV power and the corresponding DC-link voltages are depicted in Figs. 4.6(b) and (g), Figs. 4.6(c) and (h), respectively. It can be noted that the capacitor voltages of front-end DC-DC converter are maintained constant despite changes in the PV curve due to insolation variations. The seven-level inverter output voltage, filtered output voltage and phase current waveforms for unity power factor (UPF) operation of the grid are given in Figs. 4.6(d) and (i) and Figs. 4.6(e) and (j) respectively. The variation of grid current at the constant voltage for insolation changes can be observed clearly in Figs. 4.6(e) and (j) which shows that the developed power conditioner and the closed-loop controller effectively inject power into the grid for intermittent changes in PV characteristics. For better visibility of the grid current waveforms shown in Figs. 4.6(e) and (j) are scaled to 20 times. In addition, Fig. 4.7 depicts the %THD of grid current as 2.39% at 800 W/m^2 PV insolation and it is within the limits of the IEEE 1547 grid standard.

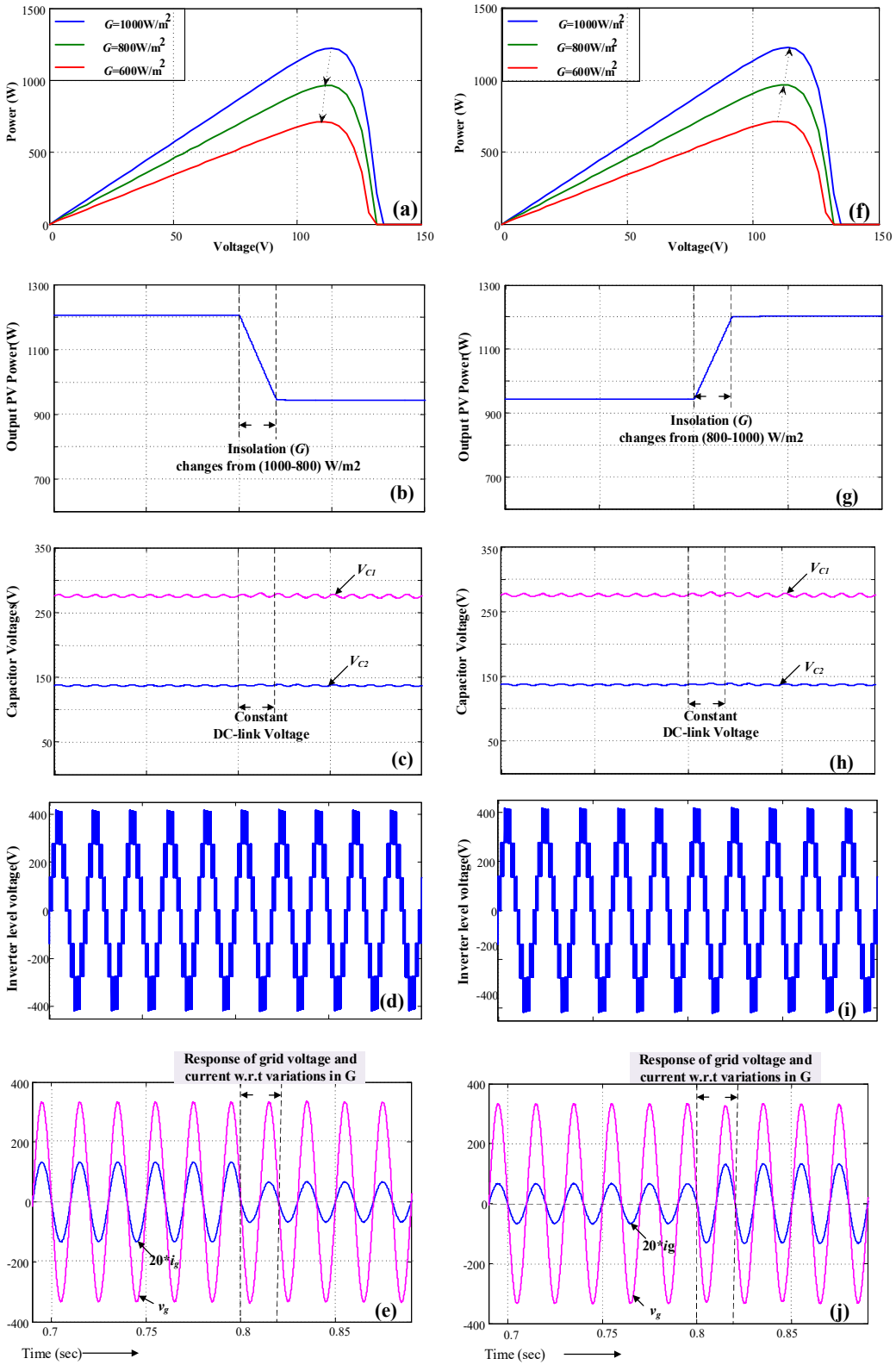


Fig. 4.6. Simulation results of the proposed power conditioner integrated with closed loop control when input insolation varies from 1000 W/m^2 to 800 W/m^2 and vice versa. The subplot gives the waveforms of (a) and (f) PV characteristics; (b) and (g) Output PV power; (c) and (h) Balanced DC capacitor voltages; (d) and (i) seven-level output voltage of asymmetrical MLI; (e) and (j) grid voltage and injected current.

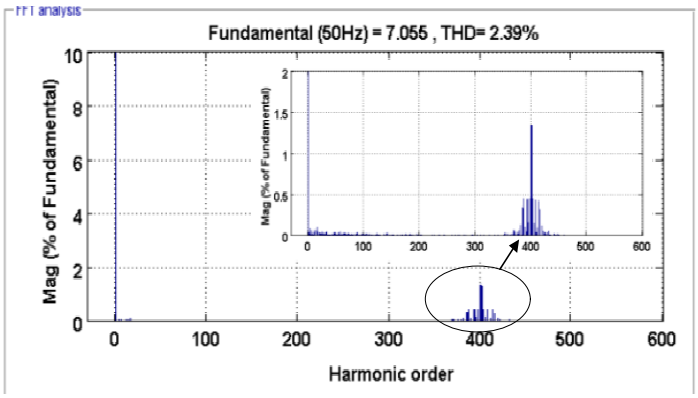


Fig. 4.7. FFT spectrum of grid current.

4.3. Leakage Current Analysis

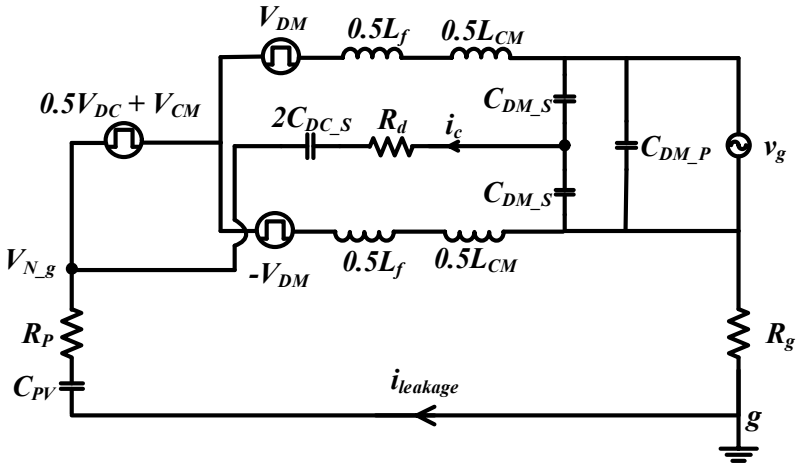
One of the major issues in grid-connected PV inverter is the leakage current generated by the PV parasitic capacitors due to variations in CMV. To address the leakage current in the proposed converter, a passive *LC* filter and an additional CMF is employed at the inverter side. The effect of variations in the CMV can be evaluated by generated common-mode (CM) and differential-mode (DM) terminal voltages, which are defined in Eq. (4.8) and Eq. (4.9). V_{AN} and V_{BN} are the terminal voltages of the inverter with respect to the negative terminal of the PV source, as shown in Fig. 4.1;

$$V_{DM}(\omega) = \left[V_{AN}(\omega) + V_{BN}(\omega)\right] \tag{4.8}$$

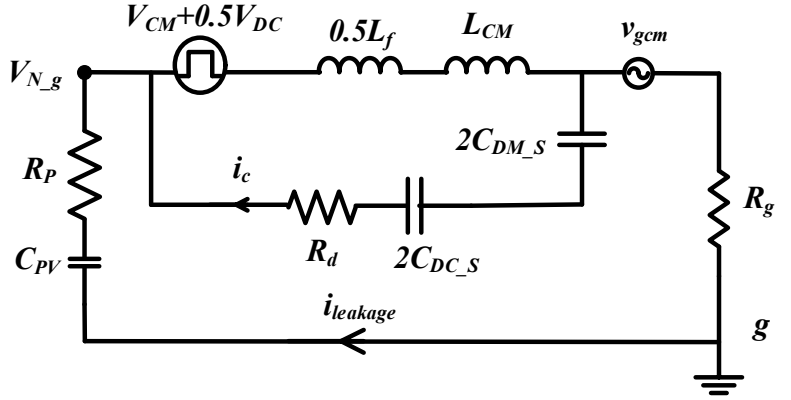
$$V_{CM}(\omega) = 0.5\left[V_{AN}(\omega) + V_{BN}(\omega)\right] \tag{4.9}$$

Where V_{CM} and V_{DM} are common-mode and differential mode voltages, respectively. Generally, the variations in CMV are determined based on the topology and the control strategy. In this system, the CMV is associated with switching frequency as well as grid frequency variations. The switching frequency variations in CMV occur when there is a transition from one voltage level to another voltage level. The grid frequency variations in CMV occur during the transition between the positive half cycle to the negative half cycle. The midpoint of the split capacitors is connected to the negative terminal of the DC bus through a damping resistor R_d to provide a conducting path to CM current, as shown in Fig. 4.1 [97]. Due to the symmetrical nature of the filter inductor, there is no effect on active and reactive power flow.

Further, to analyze common-mode characteristics of the asymmetrical MLI, an equivalent circuit is illustrated in Fig. 4.8(a); L_{CM} is the common-mode choke, C_{DM_P} and two split capacitors C_{DM_S} are used in the differential mode capacitor stage, C_{DC_S} split DC-link capacitors, R_P and C_{PV} are the parasitic elements of the PV source to ground and R_g is the ground resistance. Fig. 4.8(b) depicts the simplified common-mode equivalent circuit for easy analysis of CMV and leakage current behavior.



(a)



(b)

Fig. 4.8 (a) CM Equivalent circuit (b) Simplified CM equivalent circuit.

In the simplified model, the passive components C_{DC_S}, C_{DM_S} and a small damping resistor R_d are added in series to the common-mode path. From Fig. 4.8(b) the effect of common-mode voltages on PV source negative terminal V_{N_g} can be determined by Eq. (4.10). The resonant frequency ω_r of LC components are ($0.5L_f + L_{CM}$) and ($2C_{DM\_S}$ // $2C_{DC\_S}$). Usually, the value of ω_r is higher than the ripple frequency (100 Hz) and much lower than switching frequency; thus, Eq. (4.10) can be simplified as Eq. (4.11). Smaller ω_r leads to higher attenuation to the common-mode voltage V_{CM}. The common-mode path provided by the filter

circuit attenuates variations in the CMV as per Eq. (4.12). The grid frequency variation in CMV causes a small spike in the leakage current. Hence the RMS value of the leakage current corresponding to switching frequency variations is more in comparison with the grid frequency variations. Voltages V_{dc}, V_{ripple} and V_{gcm} have a low effect on the PV terminal voltage due to lower operating frequencies. Moreover, additional CM noise current i_c, which is generated and circulated in the CM path provided by the AC filter is shown in Fig. 4.8(a). From Fig. 4.8(b), this CM noise current can be calculated as per Eq. (4.13).

$$V_{N\_g} = \frac{-\left(V_{CM} + 0.5V_{dc}\right)}{1-\omega^2\left(0.5L_f + L_{CM}\right)\left(2C_{DM\_S} \,//\, 2C_{DC\_S}\right)} + V_{gcm}$$

$$V_{N\_g} = \frac{-\left(V_{CM} + 0.5V_{dc}\right)}{1-\frac{\omega^2}{\omega_r^2}} + V_{gcm} \tag{4.10}$$

$$V_{N\_g} = \frac{-V_{CM}(\omega)}{1-\frac{\omega}{\omega_r^2}} - 0.5V_{dc} - 0.5V_{ripple} + V_{gcm} \tag{4.11}$$

$$Atten(\omega) = 20\,log_{10}\left(\left|1-\frac{\omega^2}{\omega_r^2}\right|\right) \tag{4.12}$$

$$i_c = V_{CM}(\omega) * k(\omega) + 0.5V_{ripple} * k(2\pi * 100) \tag{4.13}$$

$$k(\omega) = \frac{\omega}{1-\frac{\omega^2}{\omega_r^2}}\left(2C_{DM\_S} \,//\, C_{DC\_S}\right) \tag{4.14}$$

$$i_{leakage} = C_{PV}\frac{dV_{N\_g}}{dt} \tag{4.15}$$

It shows that i_c is mainly decided by (i) switching frequency components (ω) and grid frequency component (ii) resonant frequency component (ω_r) and (iii) twice the grid frequency (100 Hz) component. Since ω_r is much smaller than ω, almost all the high-frequency noise is applied to L_{CM}. Therefore a factor $k(\omega)$ as given in Eq. (4.14) is applied to V_{CM}, so that the total variations in V_{N_g} are minimized. Further, Eq. (4.15) shows that the leakage current flows in the parasitic elements of the PV source. Finally, the magnitude of leakage current can

be effectively limited by an additional CMF. The filter circuit does not introduce extra components, but it restructures passive components of AC filter. Thus, inverter operation and reliability are guaranteed.

4.4. Selection of Passive Filter Components

The design of boost inductor (L_b) is based on the ripple content in the input current (ΔI_{in}) and the switching frequency (f_s) is shown in equation (4.16) [98]. Where V_{in} is the input voltage, D is the duty cycle of the boost converter. Moreover, the sizing of the DC-link capacitors (*C1* and *C2*) and filter inductor (L_f) is same as explained in the previous chapter.

$$L_b = \frac{V_{in}.D}{\Delta I_{in}.f_s} \tag{4.16}$$

The values of differential-mode capacitor C_{DM} is limited by reactive power level. For this 750 W system, 25% reactive power is chosen in the equation (4.17) [98]. The value of split capacitors $C_{DM\text{-}S}$ and $C_{DM\text{-}P}$ is determined as the equation (4.18) ($C_{DM\text{-}S} < C_{DM\text{-}P}$). Further, the value of $C_{DM\text{-}S}$ and L_{CM} can be chosen by tuning the value of resonance frequency (ω_r). Typically, ω_r can be chosen to be smaller than on tenth of switching frequency [85].

$$C_{DM} < 25\% \frac{P_{rate}}{2\pi.f.v_{ac}^2} \tag{4.17}$$

$$0.5C_{DM-S} + C_{DM-P} = C_{DM} \tag{4.18}$$

$$\omega_r = \frac{1}{\sqrt{L_{CM}C_{DM-S}}} \tag{4.19}$$

4.5. Simulation and Experimental Results

In this section, simulation and experimental results are presented and they are given side by side to validate the feasibility of the proposed topology. The fabricated experimental setup with various components is shown in Fig. 4.9. Various parameters considered for the simulations and the experimental setup is given in Table 4.2. The experimental setup is developed using IRFP460 MOSFETs, MUR1560 diodes, copper-based printed circuit board (PCB) and

connecting wires as per the availability in the lab. The PWM pulses required for the boost converter and asymmetrical inverter are generated with the use of the DSP2812 processor and DIGILENT ATLYS Spartan-6 FPGA board, respectively. TLP250 based driver circuit is used for driving the MOSFETs. A regulated DC power supply is used as an input source to the front-end boost converter. The output of the asymmetrical MLI is connected to load resistance through *LC* and CMF. To measure the leakage current, parasitic capacitance C_{PV} in series with R_P is connected at node *N* as shown in Fig. 4.1. The waveforms are captured using DPO 3034 with the help of the current probe TCP 0030 and differential voltage probe TMDP0200.

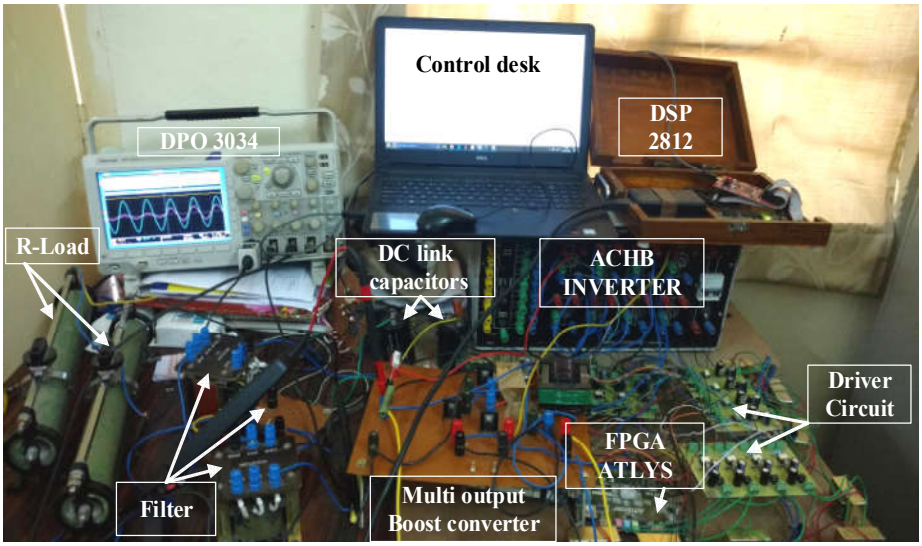


Fig. 4.9. Experimental prototype for the proposed power conditioner.

From Fig. 4.10, it is observed that the input voltage is 96 V and input current of the multi-output boost converter is continuous in nature; which confirms that conduction mode of operation is continuous and also the voltages across capacitor *C1* and *C2* are balanced and preserved corresponding to the turns ratio (2:1) of *HFT*. It is essential to deal with high penetration of power into the grid and reactive power capability in the future PV inverters [43]. Therefore a newly designed inverter should allow the reactive power flow without affecting the levels in the output. From Fig. 4.11, it is noticed that the waveforms of seven-level voltage, load voltage and current for unity, 0.9 lagging power factor (200 Ω, 300 mH,) and 0.9 leading power factor (135 Ω, 50 μF) loads respectively; it is evident that the proposed power conditioner and its modulation scheme suitable for both real and reactive power flow.

The experimental THD of load voltage and currents are measured using MDO3024 and YOKOGOWA WT310E digital power analyzer, as given in Fig. 4.12. The measured %THD of the filtered output voltage and current is 1.10%, which is well below the IEC61000-3-2 standard [99]. Figs. 4.13(a) and (b) illustrate the simulation and experimental results of the inverter terminal voltages (V_{AN}, V_{BN}) and V_{CM}. It is observed that the CMV has both switching and grid frequency variations. To eliminate the switching frequency components and to reduce the leakage current magnitude below the grid standards, a CMF is connected across the terminal of the inverter, which forms a low-pass filter circuit as explained in section 4.3.

Table 4.2 System parameters

Parameters	Specification
Power (P)	750 W
DC-link voltage (V_{dc})	380 V
AC output voltage (V_{load})	230 V
Fundamental frequency (f)	50 Hz
Switching frequency (f_s)	20 kHz
Inductors (L_f, L_{cm}, L_b)	2 mH, 2 mH, 3 mH
Capacitors (C_{dm_s}, C_{dm_p}, C_{DC_s}, C_{PV})	1 µF, 2 µF,1000 µF, 21 nF
Resistors (R_d, R_g, R_p)	2.2 Ω, 10 Ω, 2.2 Ω
High frequency transformer	Core type: ETD 42/21/15 Magnetizing inductance (L_m): 8.2 mH Leakage inductance referred to primary: 66 µH Turns ratio: 2:1

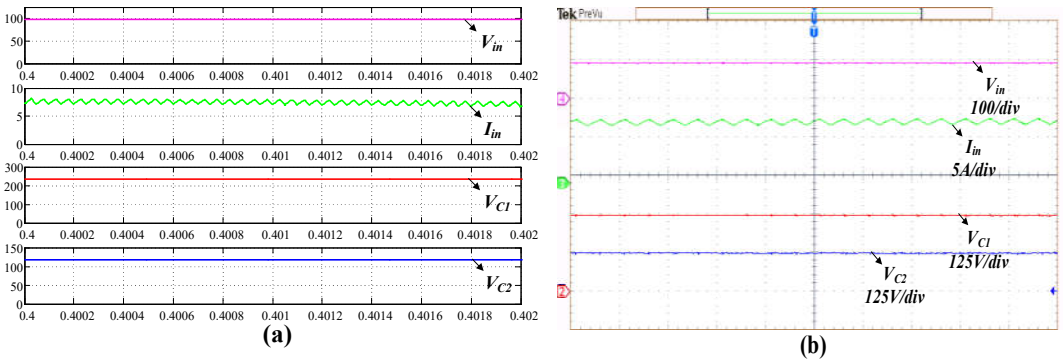


Fig. 4.10. Input voltage, current and DC-link voltage waveforms of (a) simulation and (b) experiment.

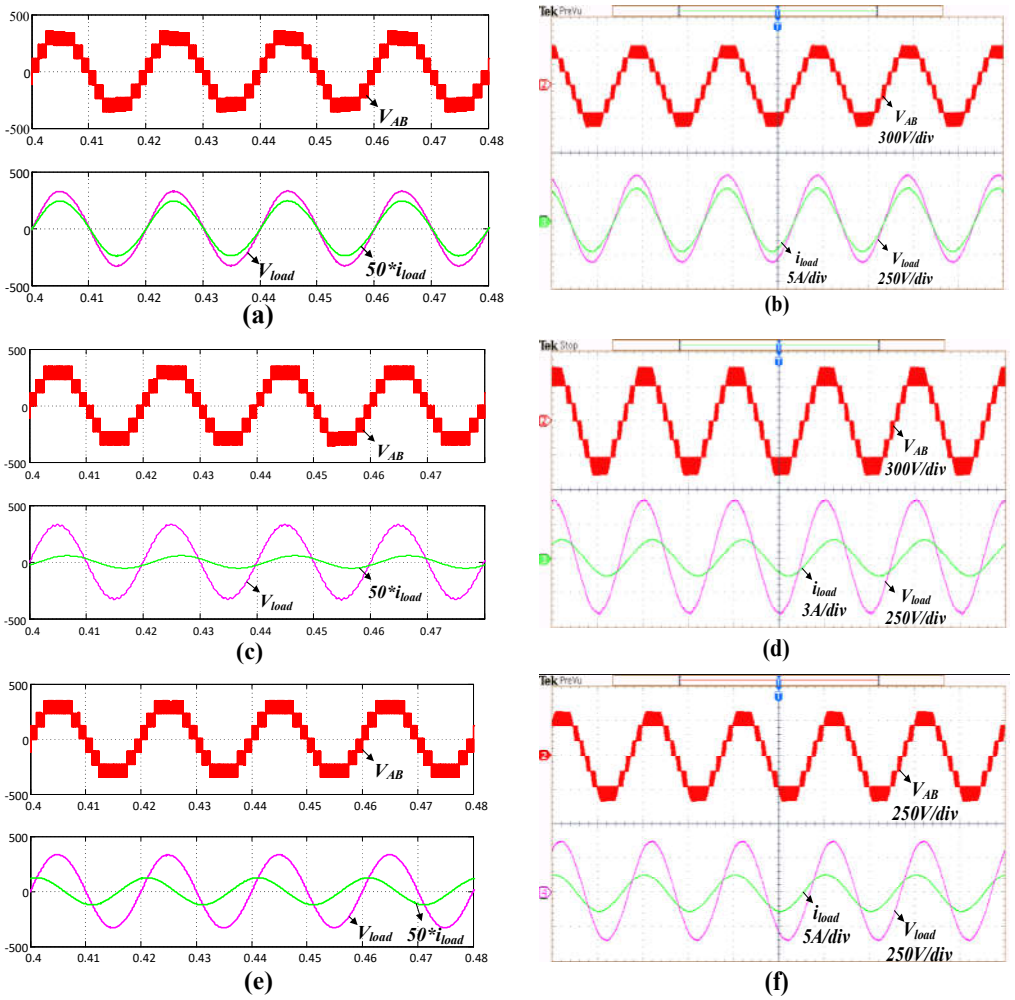


Fig. 4.11. Simulation and experimental results of seven-level voltage, load voltage and current (a) and (b) unity power factor; (c) and (d) (0.9) lagging power factor; (e) and (f) (0.9) leading power factor.

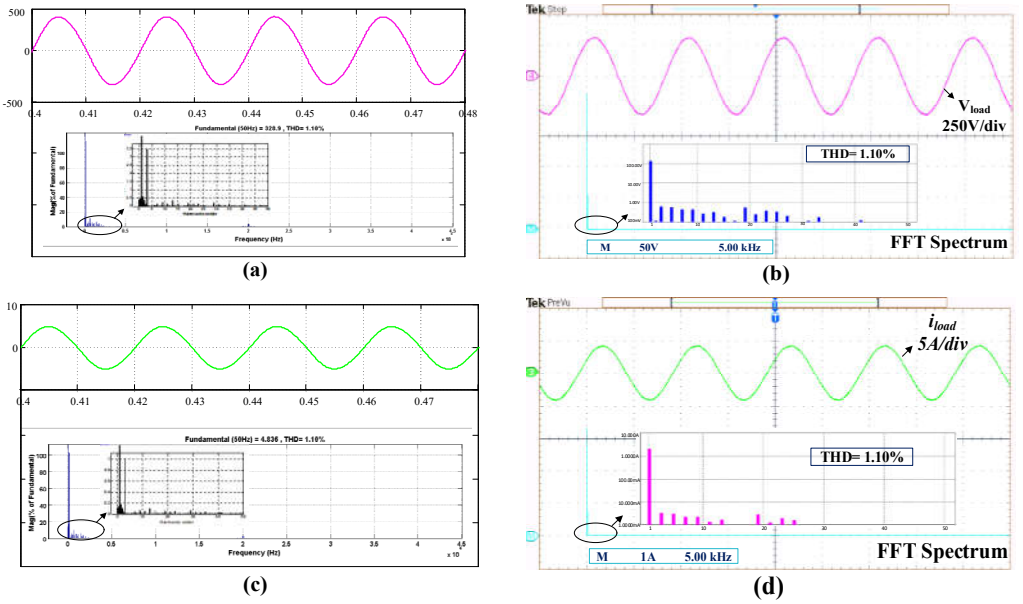


Fig. 4.12. Simulation and experimental FFT spectra for unity power factor operation (a) and (b) load voltage; (c) and (d) load current.

Figs. 4.13(c) and (d) depict the measured waveforms of PV terminal voltage and leakage current in both simulation and experimentation; it is observed that high-frequency voltage transitions in V_{N_g} are attenuated and the RMS magnitude of leakage current is limited to 14 mA, which indicates the effectiveness of the proposed power conditioner along with CM filter.

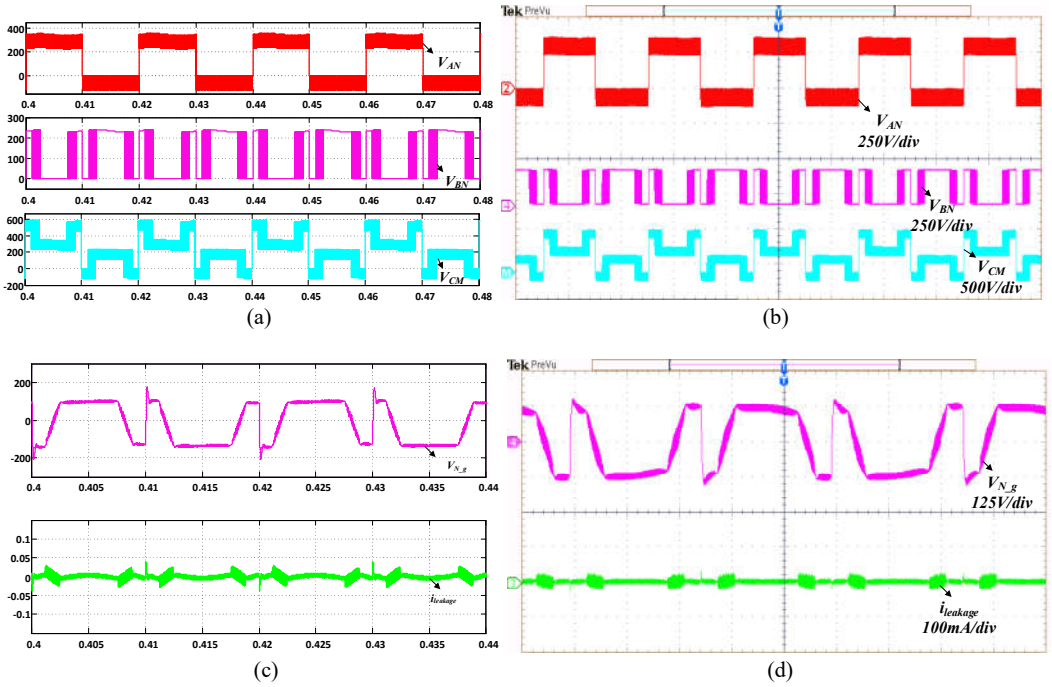


Fig. 4.13. Simulation and experimental waveforms of the (a) and (b) Terminal voltages V_{AN}, V_{BN} and V_{CM}; (c) and (d) $V_{N\text{-}g}$ and leakage current.

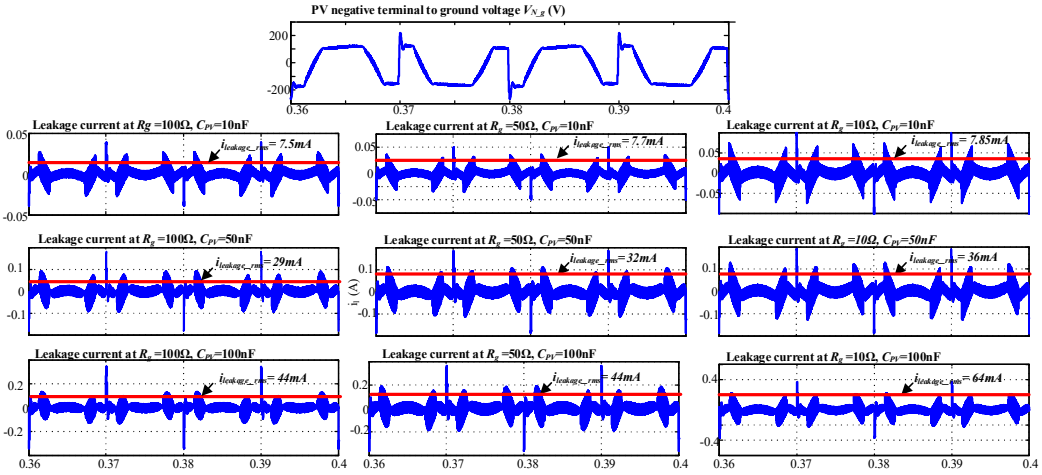


Fig. 4.14. Simulation results of $V_{N\text{-}g}$ and leakage current.

Further, to demonstrate the practical limitation of the leakage current, three different grounding resistances and parasitic capacitances are considered as per the reference to evolve the leakage current magnitude [12]. From Fig. 4.14, it is

noticed that in all nine cases, the RMS leakage current magnitude does not exceed VDE 126-1-1 grid standards. Therefore the proposed topology, along with CMF is effective in limiting the leakage current.

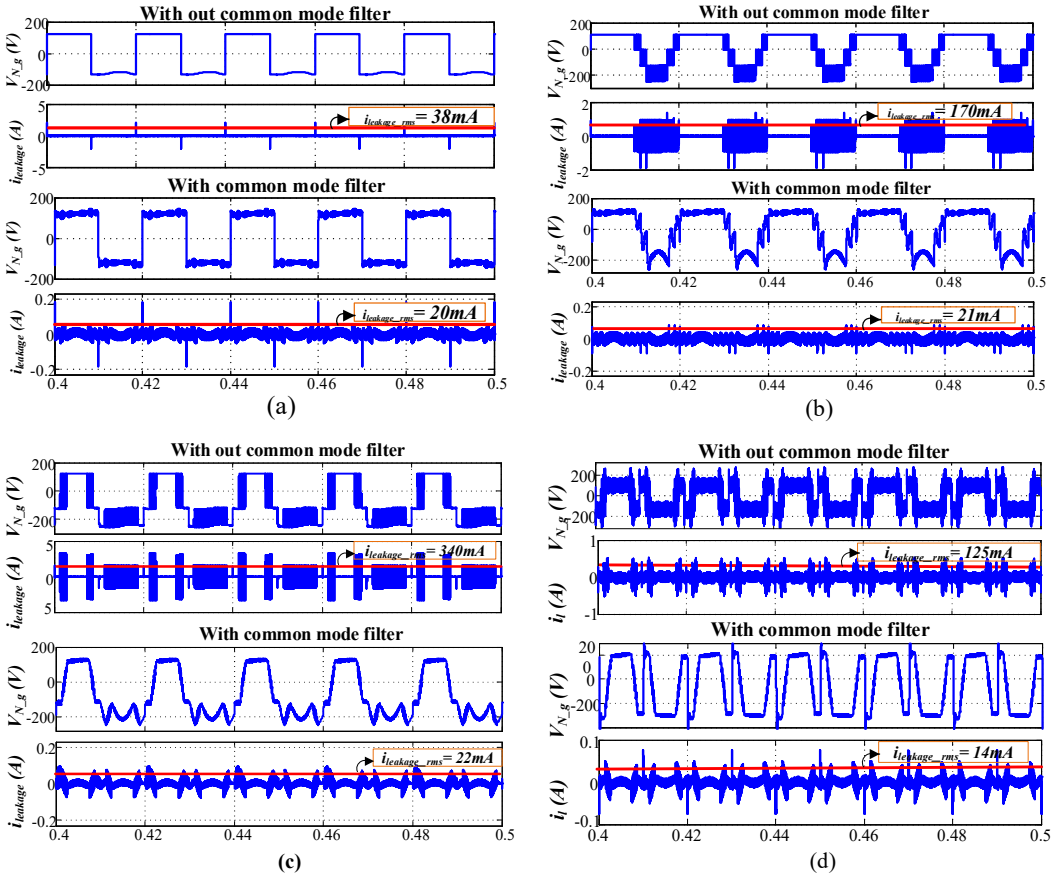


Fig. 4.15 Comparison of V_{N_g}, leakage current $i_{leakage}$ and its RMS value without and with CM filter. (a) Ref [77]; (b) Ref [78]; (c) Ref [79]; (d) proposed topology.

Fig. 4.15 illustrates the comparison of leakage currents and the corresponding PV terminal voltages for different configurations presented in references [77], [78], [79]. The simulation study for all the configurations is carried out for the same conditions as given in Table 4.2. Based on the configuration and PWM control strategy, the PV terminal to ground voltage V_{N_g} contains switching frequency or grid frequency or both of different amplitudes. From Fig. 4.15(a), it is noticed that $V_{N\text{-}g}$ of the configuration reported in [77] contains only grid frequency variations of two different amplitudes; hence the resultant value of RMS leakage current is 38 mA. Figs. 4.15(b) and (c) depict $V_{N\text{-}g}$ and $i_{leakage}$ of the configurations reported in [78]-[79]. It is noticed that both switching frequency and grid frequency variations of four different amplitudes are present in $V_{N\text{-}g}$, which results in the leakage current of 170 mA and 340 mA

respectively. From Fig. 4.15(d), it is observed that $V_{N\text{-}g}$ of the proposed power conditioner consists of both switching and grid frequency variations of three different amplitudes; hence the resultant value of RMS leakage current is 125 mA.

All these inverters with such leakage currents are not feasible for PV applications directly without providing isolation. Therefore, a common-mode filter is connected across terminals of the inverter by employing common-mode path from split capacitor to the negative terminal of PV source for attenuating high-frequency variations in the common-mode voltage, as explained in section 4. Hence, the leakage current is reduced to 20 mA, 21 mA and 22 mA for the topologies reported in [77]-[79] respectively, as shown in Fig. 4.15. However, the proposed power conditioner has a leakage current of 14 mA. In addition to that, the overall component count and cost of the proposed power conditioner is low and the efficiency is more as compared with other topologies. Therefore, from the above discussion, it can be emphasized that the proposed power conditioner along with CMF limits the leakage current well below the grid standards with lower component count and higher efficiency for unity and non-unity power factor conditions.

4.5.1. Dynamic Performance

A simple PI controller is realized in a digital signal processor (DSP) using an embedded code generator toolbox in MATLAB. The capacitor voltages are in the ratio of 2:1 with the *HFT* and hence the control of *C1* voltage automatically regulates the total DC-link voltage. Thus, the measurement of DC capacitor voltage *C1* requires a voltage sensor for computing the total DC-link voltage. The sensed *C1* voltage scaled down to the required level and then fed into the DSP through analog to conversion (ADC). To maintain the DC-link voltage of 350 V, capacitor voltage *C1* is sensed and compared with a set reference value of 230 V; then, the error is fed to the *PI* controller, which produces the required duty ratio. For generating the driving pulses to switches *S1* and *S1'*, the duty ratio is compared with a triangular wave of frequency 20 kHz.

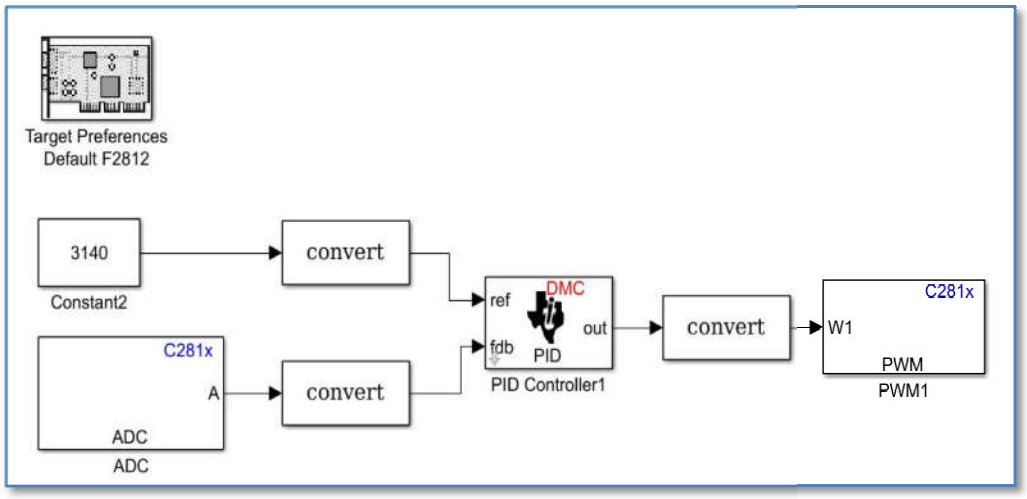


Fig. 4.16. Generation of the control pulses using DSP.

Fig. 4.16 shows the implementation of the PI controller using an embedded code generator toolbox using MATLAB, where the DSP TMS320F2812 board is selected for the pulse generation. The sensed analog signal is converted into an equivalent digital value by using Eq. (4.19) and then given to the PI controller as an actual signal. The set reference value is calculated as per the requirement, i.e. 4095*(2.3-0)*0.33=3139.5=3140. Finally, both are compared and the error fed PI controller to generate the desired duty ratio for regulating the DC-link voltage as 350 V irrespective of the disturbances. The detailed explanation of the use of each and every block of the controller is clearly described in the ref [100].

$$Digital\ value = 4095 * \frac{(Input\ analog\ value - ADCLO)}{3} \tag{4.19}$$

Where, *ADCLO* is the lowest operating voltage (ideally zero).

To test the dynamic performance of the proposed power conditioner, the system is tested in two different conditions, i.e. (i) changes in input voltage and (ii) step change in load. Fig. 4.17(a) shows the constant capacitor voltage *C1* despite changes to the input voltage from 80 V to 90 V and then to 85 V. It can be noticed that the capacitor voltage *C1* reaches steady state immediately after a slight deviation during the transitions in input voltage. Further, the inverter is tested for step-change in load current by 40% and the their corresponding experimental results are given in Figs. 4.17(b) and (c) respectively. In both cases, the filtered output voltage and dc bus voltage V_{C1} are maintained almost constant for step changes in load. It is clearly evident that the model exhibits fast dynamic

response in one fundamental cycle of operation for the wide variation in input voltage as well as a load, which validates the effectiveness of the controller. Therefore, from the above discussion, it can be concluded that the dynamic performance of the proposed power conditioner is capable of feeding the power into the grid under intermittent changes of PV characteristics.

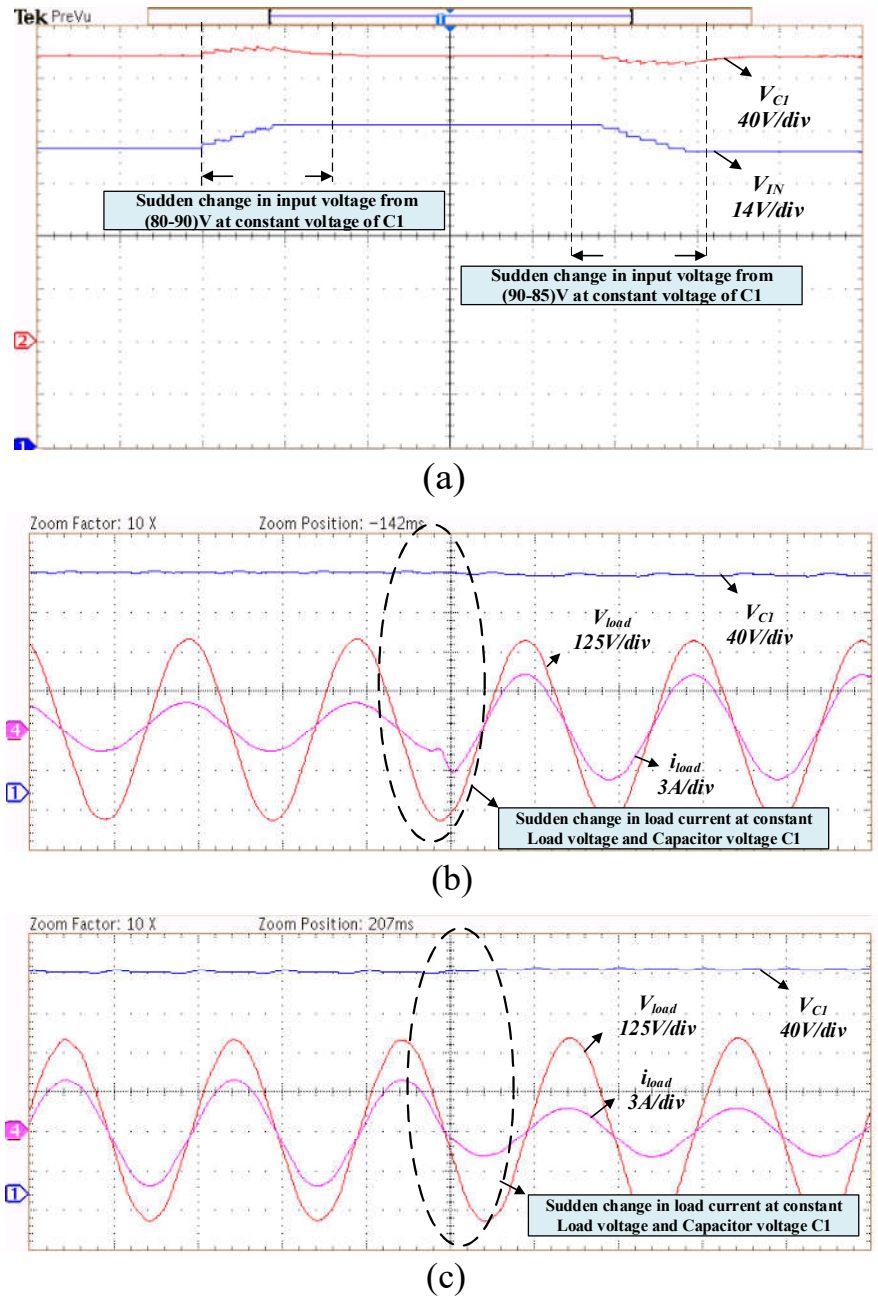


Fig. 4.17. Experimental waveforms of (a) capacitor voltage (V_{C1}) with respect to changes in input voltage; (b) and (c) load voltage, capacitor voltage (V_{C1}) response with respect to step change in load.

4.6. Evaluation of Losses

This section deals with the evaluation of losses of different two-stage seven-level PV inverters to highlight the merits of the proposed system. The losses are calculated using steady-state equations referred in [34], [101]-[103] and PSIM thermal module simulations have also been performed to validate the losses obtained. Based on the on-state resistance and blocking voltage, various switches and diodes selected for the evaluation of losses and they are given in Table 4.3. The expressions used for the calculation of switching and conduction losses of the MOSFET are as follows:

$$P_{SW\_I} = \frac{1}{2\pi}\frac{V_b\left(t_{on}+t_{off}\right)}{2T_c}\int_{\theta_{S2}}^{\theta_{S1}}\left|i_L\right|d\theta \tag{4.20}$$

$$P_{SW\_B} = \frac{1}{2}IV_b\left(t_{on}+t_{off}\right)f_S + \frac{1}{2}C_{oss}V_b^2 f_{SW} \tag{4.21}$$

$$P_C = \frac{1}{2\pi}\int_0^{\pi} i(t)V_{SW}(t)d_{SW}(t)d(\omega t) \tag{4.22}$$

Where, P_{SW_I}, P_{SW_B} are the switching losses of MOSFET for inverter and front-end boost converter respectively. V_b denotes the blocking voltage of the switch, T_c, t_{on} and t_{off} denote inverter switching period and operating times of the switches, θ_{S1} and θ_{S2} are angles of the starting and the ending of an interval with switching losses, $\left|i_L\right| = i_{max}M_a \sin\theta$, M_a is modulation index, i_{max} is maximum load current. I, C_{oss} are average current and output capacitance. Where P_C is conduction loss of the MOSFET, $i(t) = I_M \sin\omega t$, $v_{SW}(t) = i(t)R_{ds}$, $d_{SW}(t) = M_a \sin\omega t$. The expressions used for the calculation of conduction and reverse-recovery losses of the diodes are as follows;

$$P_{C\_D} = \frac{1}{2\pi}\int_0^{\pi} i(t)V_d(t)D_{diode}(t)d(\omega t) \tag{4.23}$$

$$P_{d\_SW} = \frac{1}{2\pi}\int_0^{\pi}(0.5V_{bd})(0.5I_{rr})f_s t_b d(\omega t) \tag{4.24}$$

P_{C_D}, P_{d_sw} denotes conduction and reverse-recovery loss in diode respectively. Where, $i(t) = I_M sin(\omega t)$, $V_d(t) = V_f + i(t)R_{ak}$, $D_{diode}(t) = 1\text{-}M_a sin(\omega t)$, V_f is the voltage drop in diode under off condition, R_{ak} is the on-drop resistance, V_{db} is the blocking voltage of the diode, I_{rr} is the reverse-recovery current and t_b is turn-off time of the diode. Table 4.4 elaborates on the operation of switches in various seven-level inverter topologies for grid-connected PV systems. It has been observed that the proposed topology has the least component count and the number of switching devices at each output level generation is low, which results in high efficiency of the proposed topology compared to other topologies. Fig. 4.18 depicts a comparison of the blocking voltage of each switching device used in various inverters. Fig. 4.19 illustrates the comparison of loss distribution among various components for different MLI configurations.

Table 4.3. Selection of switches and diodes

Device	Part number	Rating
MOSFET	FCA76N60N	400V/76A
	IRF300P227	300V/50A
	IRFP4127PbF	250V/75A
Diode	RUR1S1560S	600V/15A

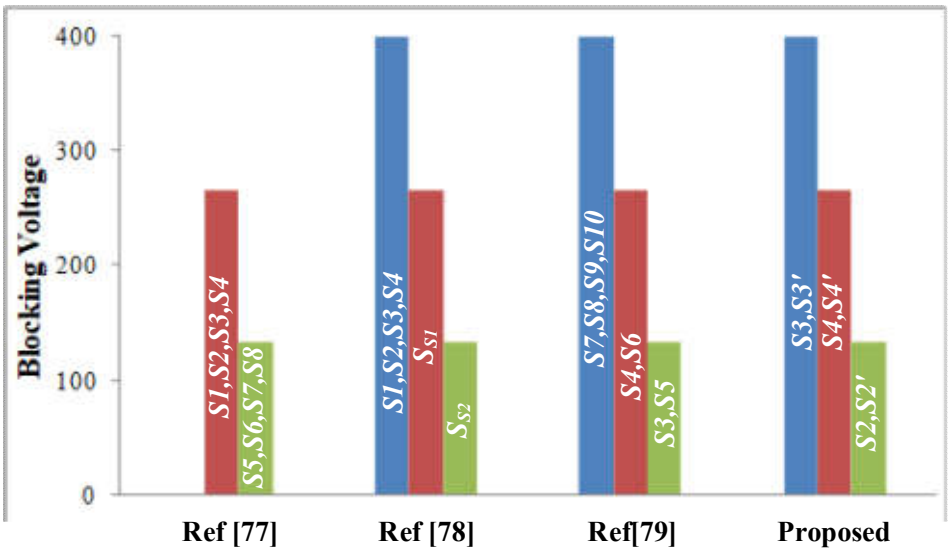


Fig. 4.18. Blocking voltages of the switches used in various MLI topologies.

Table 4.4. Operation of various switches in different topologies

S.No	Reference number	I	II		III		IV		V		VI	
			S	D	P	N	P	N	P	N	P	N
1	Ref [77]	4	9	3	14	14	3	3	2	2	4	4
2	Ref [78]	3	8	5	15	15	6	6	0	0	2	2
3	Ref [79]	4	10	3	15	15	6	6	0	0	2	2
4	Proposed Topology	3	8	3	13	13	4	4	2	2	2	2

I – Number of switches and diodes in conduction during freewheeling period;

II – Total number of devices used in the given topology S -switches; D –Diodes;

III –Number of diodes and switches in conduction during one cycle of two-stage system P- Positive cycle; N- Negative cycle;

IV – Number of switches operating at higher switching frequency loss of the two-stage system;

V – Number of switches operating at medium switching frequency loss of the two-stage system;

VI – Number of switches operating at lower switching frequency loss of the two-stage system.

From Fig. 4.19, it is evident that the efficiency of the proposed two-stage configuration is higher in comparison with other recently proposed topologies presented in [77]-[79]. The power transferred by *HFT* is less than the one-third of the total output of the PV source in all the above-mentioned topologies. Hence the degradation of power efficiency with the use of *HFT* is not a severe problem. To validate the theoretical losses, a PSIM thermal module is developed and simulated at various loading conditions. The PSIM thermal module enables a quick way of estimating the switching and conduction losses of semiconductor switches based on real device characteristics. Finally, Fig. 4.20 (a) & (b) depicts the efficiency curve of the proposed power conditioner based on theoretical and PSIM thermal module analysis. Both the results are very close to each other and also it is noticed that a slight increase in efficiency of the configuration for the input voltage changes from 80V to 100V. This ensures that the efficiency of the proposed configuration is more than 90% at different input voltages.

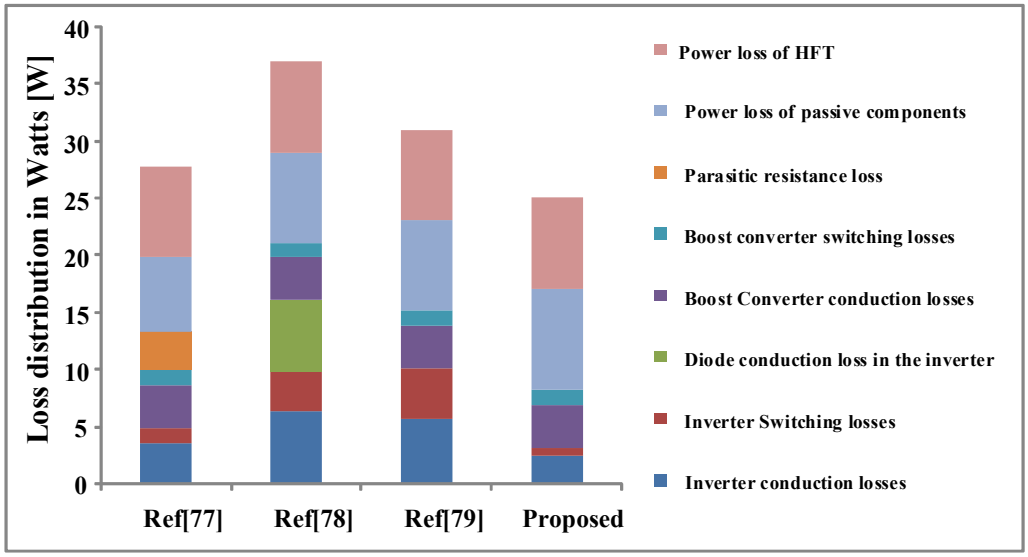
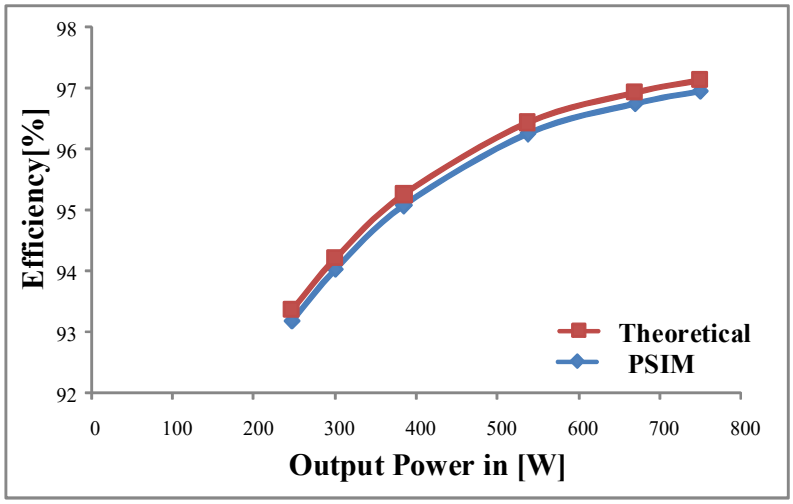
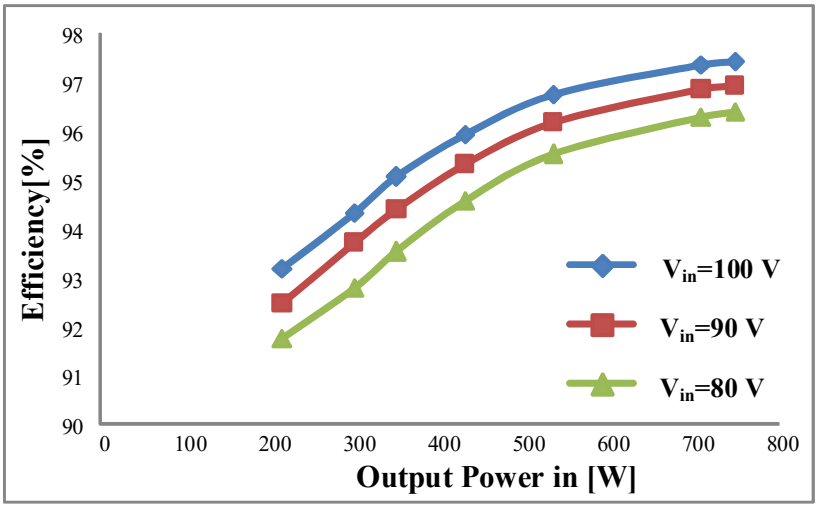


Fig. 4.19. Loss distribution in various topologies at 750 W of output power.



(a)



(b)

Fig. 4.20. Efficiency curves (a) Theoretical and PSIM and (b) Different input voltages.

4.7. Comparison of the Proposed Inverter with Existing Two-Stage PV Inverter Topologies

The detailed comparisons with the existing two-stage seven-level inverters are given in Table 4.5 to highlight the merits of the proposed power conditioner; it is observed that the total component count, leakage current and blocking voltages are less compared with the topologies in [76, 78 & 79]. Whereas, the leakage current and blocking voltages of Ref. [77] are close to the proposed topology, but it is augmented with an extra semiconductor device and parasitic resistance losses as shown in Fig. 4.19. Moreover, the use of bulky and low-frequency transformer at AC side is eliminated. Furthermore, the proposed common-mode filter solution can be employed for the topologies reported in Refs [77]-[79] to minimize the leakage current.

Table 4.5. Comparison of different seven-level inverter topologies

Parameter		**Ref [76]**	**Ref [77]**	**Ref [78]**	**Ref [79]**	**Proposed**
MOSFETS	LF	2	4	2	2	2
	OLF	5	5	6	8	6
Diodes		9	3	5	3	3
DC capacitors		3	2	2	2	2
HFT		-	1	1	1	1
Reactive power capability		Yes*	Yes	No	Yes	Yes
Leakage current	Without CMF	165mA	38mA	170mA	340mA	125mA
	With CMF	18mA	20mA	21mA	22mA	14mA
Blocking Voltage	MOSFET	$6.5V_{dc}$	$4V_{dc}$	$5V_{dc}$	$6V_{dc}$	$4V_{dc}$
	Diode	$5V_{dc}$	$1.35V_{dc}$	$1.65V_{dc}$	$1.65V_{dc}$	$1.65V_{dc}$

LF=line-frequency, OLF= other than line-frequency, Yes*=possible with modified modulation technique, CMF=common-mode filter, V_{dc}=Total DC-link voltage.

4.8. Summary

In this chapter, a new single-phase two-stage seven-level power conditioner suitable for the PVPGS is presented. The proposed single-phase seven-level power conditioner employs a front-end DC-DC boost converter and an asymmetrical seven-level inverter. This topology uses only eight power semiconductor switches in comparison with other topologies for the realization of seven-level output, which leads to improved efficiency. The proposed power conditioner ensures guaranteed balancing of DC-link capacitor voltages with simple control. Besides, the leakage current is limited effectively within the VDE0126-1-1 grid standards. The developed controller shows better performance by regulating the output voltage and injecting current into the grid for intermittent changes in PV. The experimental results are in good correlation with the simulation results, which proves the capability of the proposed topology.

4.9. Contributions

a) Registers high efficiency and lower component count for the realization of seven-level output voltage as compared to the conventional topologies.
b) High-frequency oscillations in the voltage across PV parasitic capacitance are eliminated, and thereby the leakage current is reduced below the VDE-01260-1-1 grid standards.
c) It provides the reactive power support for the grid-connected PVPGS.

4.10. Papers Published

1) Sateesh Kumar Kuncham, Kirubakaran Annamalai, and Subrahmanyam Nallamothu. "**Single-Phase Two-Stage Seven-Level Power Conditioner for Photovoltaic Power Generation System**" *IEEE Journal of Emerging and Selected Topics in Power Electronics,* vol.8 (1), pp. 794-804, Apr. 2019.

Chapter 5

A Two-Stage Hybrid Transformerless Multilevel Inverter

Chapter 5

A Two-Stage Hybrid Transformerless Multilevel Inverter

5.1. Introduction

The two-stage inverter which was introduced in the previous chapter, requires an HFT and a common-mode filter for boosting the low PV voltage and for the elimination of high-frequency oscillations in CMV respectively. To overcome these drawbacks, a new structure of single-phase two-stage hybrid transformerless MLI for PVPGS is presented in this chapter. The proposed topology comprises a multilevel boost converter (MLBC) and a symmetrical hybrid MLI. The MLBC combines the boosting and switched capacitor voltage functions to produce self-balanced multiple voltage levels. The proposed MLI is derived from the combination of bi-directional switches, a half-bridge and a diode clamped branch, which can eliminate high-frequency oscillations in the total common-mode voltage and is capable of suppressing leakage current as per DIN-VDE 01261-1 grid standards. It offers the advantages of scalability, reactive power capability, reduced THD and filter size.

This chapter presents the modes of operation of the proposed inverter to generate seven-level output under both positive and negative power regions. Comparative studies are also undertaken to show the merits of the proposed configurations with other classical MLIs and recently proposed two-stage inverter topologies. The proposed inverter is simulated in MATLAB/SIMULINK environment and an experimental setup has been built in the laboratory to validate the effectiveness of the recommended configuration.

5.2. System Description

The schematic arrangement of the proposed two-stage transformerless grid-connected PV inverter is shown in Fig. 5.1. This two-stage configuration comprises MLBC and a symmetrical hybrid MLI. The MLBC produces N number of boosted voltage levels from the input PV source to meet the DC-link

voltage requirement without using an HFT and extreme duty cycle ratio; also each device blocks only (1/N) times DC-link voltage. It has significant advantages of (i) higher efficiency with reduced voltage stress across the devices and (ii) guaranteed balancing of the DC-link capacitors by clamping the diodes based on the capacitor voltages.

The proposed hybrid MLI converts multilevel DC to AC. The gate pulses to the inverter switches are generated through a modified sinusoidal level-shifted pulse width modulation (SLS-PWM). It enables the inverter to operate under all types of loading conditions such as unity, lagging and leading power factors without changing the CMV behavior. Moreover, the magnitude of RMS leakage current is well below the grid standards with the simple asymmetrical filter inductor. Furthermore, the number of levels in the output voltage of MLBC and hybrid MLI can be increased by adding a basic unit. The complete closed-loop control diagram for MPPT and grid current injection of the two-stage system [76], [104] is shown in Fig. 5.1. The detailed operation of MLBC, hybrid MLI, control strategy and CMV analysis are explained in the following sections.

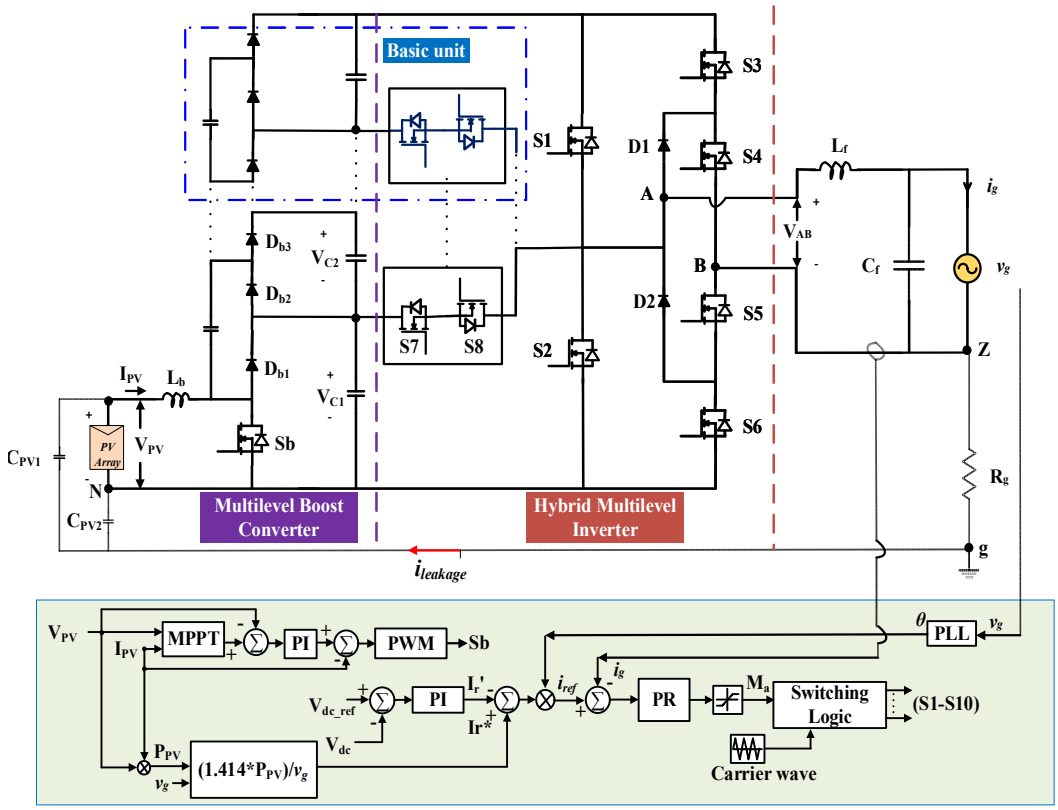


Fig. 5.1. Proposed two-stage grid-connected PV inverter.

5.3. Operation of the Multilevel boost Converter

Fig. 5.2 shows the three-level DC-DC converter, which is derived from conventional boost converter using diodes and capacitors [105]. One of the main advantages of MLBC is its capability of balancing DC capacitors without adding additional circuitry. The three-level boost converter act as a front-end converter to boost the input DC voltage. The working of the MLBC circuit is depicted in Figs. 5.2(a) and (b). Where different switching states of the power devices are described below. In Fig. 5.2(a), when the switch Sb is in ON state, inductor L_b is connected to the input DC source (V_{in}). Under this condition, if the capacitor C4's voltage is less than C1's voltage, then C1 clamps C4's voltage through a diode D_{b2} and switch Sb. Simultaneously, if the voltage across C4+C5 is less than the voltage across C1+C2, then C1 and C2 clamp the voltage across C4 and C5 through a D_{b4} and Sb.

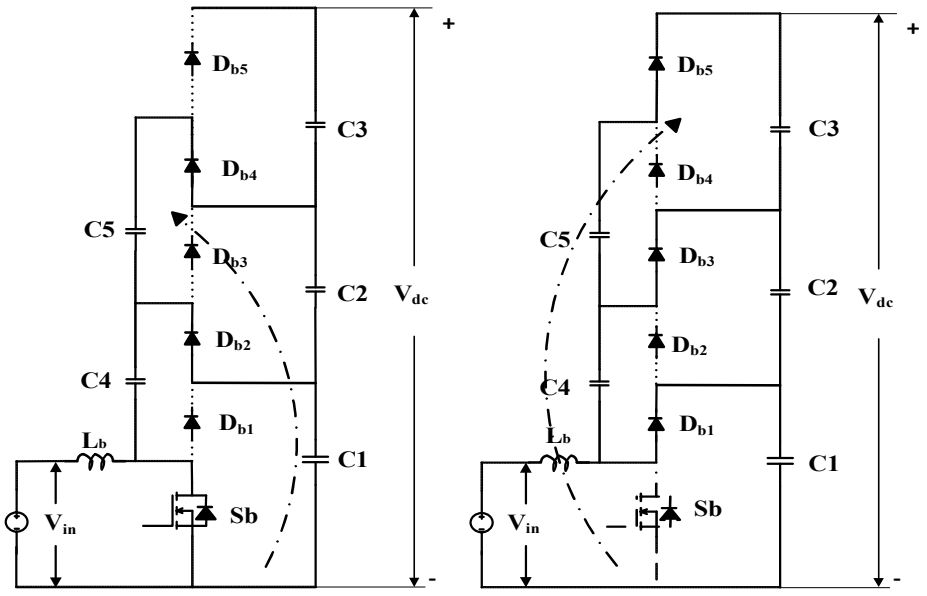


Fig. 5.2. Operating condition of the switch (a) on-state (b) off state.

Similarly, in Fig. 5.2(b), when Sb is in OFF state, inductor current conducts D_{b1} and charges the capacitor C1. When D_{b1} conducts, C4 and the voltage V_{in} plus the inductor's voltage clamp the voltage across C1 and C2 through D_{b3}. Similarly, the voltage across the inductor plus V_{in}, C4 and C5 clamp the voltage across C1, C2 and C3 through D_{b5}. It is important to note that diodes D_{b1}, D_{b3} and D_{b5} conduct synchronously in the circuit and they are complemented

with the diodes D_{b4}, D_{b2} and Sb. The total DC-link voltage (V_{dc}) and input inductor current (I_L) can be expressed in terms of the input voltage (V_{in}) and duty ratio as per Eqs. 5.1 and 5.2 respectively. R_0 is the output resistance and D is the duty ratio of the MLBC. The total number of capacitors and diodes required for 'N' level DC output are (2N-1). The voltage across the capacitors 'V_c' and the blocking voltage 'V_b' of switch and diode are expressed by Eq. 5.3.

$$V_{dc} = \frac{N * V_{in}}{(1-D)} \tag{5.1}$$

$$I_L = \frac{N^2 V_c}{(1-D)\ R_o} \tag{5.2}$$

$$V_b = V_c = \frac{V_o}{N} \tag{5.3}$$

5.4. Proposed Hybrid Transformerless Multilevel Inverter

The proposed MLI is derived by combining the common emitter bi-directional MOSFET branches and a hybrid-bridge three-level inverter. The hybrid-bridge inverter consists of a half-bridge leg with S1, S2 and an NPC leg with S3, S4, S5, S6, D1 and D2; this enables the polarity generation for the three-level DC voltages. The common emitter bi-directional branch can select capacitor voltages such as V_{C1}, (V_{C1}+V_{C2}), (V_{C1}+V_{C2}+V_{C3}) and so on based on the selected number of output voltage levels (N).

5.4.1. Operating States of the Inverter in Different Modes

In this section, the detailed switching configurations adopted for unity power factor of the grid (v_g and i_g positive, v_g and i_g negative) and non-unity power factor conditions of the grid (v_g positive, i_g negative and v_g negative, i_g positive) of seven-level inverter and the modified SLS-PWM are presented. Fig. 5.3 shows the proposed seven-level inverter topology. Moreover, it is assumed that the voltage across each DC-link capacitor is equal throughout the analysis (i.e., V_{C1}=V_{C2}=V_{C3}=V).

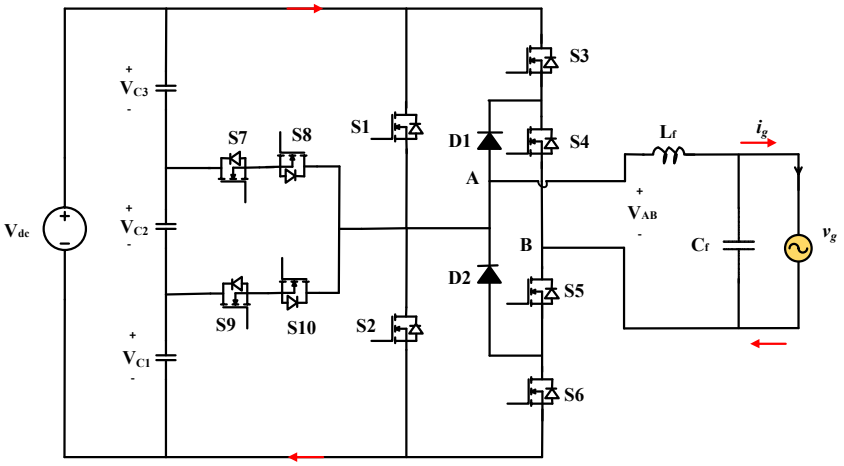


Fig. 5.3. Proposed hybrid seven-level inverter topology.

Case. I: Positive grid voltage and grid current

Assume both the grid voltage (v_g) and current (i_g) are positive, the voltage levels can be expressed as $(V_{C1}+V_{C2}+V_{C3})=V_{dc}$, $(V_{C1}+V_{C2})= (2/3)V_{dc}$ and $V_{C1}= (1/3)V_{dc}$. Fig. 5.4(a) corresponds to state 1 in Table. 5.1, switches S1, S5, S6 and S7 are turned ON while switches S2, S3, S4, S8, S9 and S10 are turned OFF, which corresponds to the normal operation of a hybrid-bridge inverter. In this case, $V_{AB}= (V_{C1}+V_{C2}+V_{C3})$ and the output current flows from MLBC to load through S1 and returns through S5 and S6. Fig. 5.4(b) corresponds to state 2 in Table. 5.1, switch S1 is OFF, while S7 and the body diode of S8 are turned ON (S5 and S6 remain ON) and the switches S2, S3, S4, S9 and S10 are turned OFF. In this case, $V_{AB}= (V_{C1}+V_{C2})$ and the output current flows from the lower two capacitors to the load through switches S7 and the body diode of S8, S5 and S6. Fig. 5.4(c) corresponds to state 3 in Table. 5.1, switches S9 and the body diode of S10 are turned ON (S5 and S6 remain ON) and the switches S2, S3, S4, S7 and S8 are turned OFF. In this case, $V_{AB}=V_{C1}$ and the output current flows from the lower capacitor to the load through switches S9, the body diode of S10, S5 and S6.

Case. II: Negative grid voltage and grid current

When both the grid voltage (v_g) and currents (i_g) are negative, voltage levels $(V_{C1}+V_{C2}+V_{C3}) = -V_{dc}$, $(V_{C2}+V_{C3}) = -(2/3)V_{dc}$ and $V_{C3} = -(1/3)V_{dc}$ are produced as shown in Fig 5.4. Fig. 5.4(d) corresponds to state 6 in Table. 5.1, switches S2, S3, S4 and S10 are turned ON while the switches S1, S5, S6, S7, S8

and S9 are turned OFF, which corresponds to the normal operation of a hybrid-bridge inverter. In this case, $V_{AB} = -(V_{C1}+V_{C2}+V_{C3})$ and the output current flows from load to MLBC through S3, S4 and returns through S2. Fig. 5.4(e) corresponds to state 7 in Table. 5.1, the body diode of S9 and S10 are turned ON (S3 and S4 remain ON) and the switches S1, S2, S5, S6, S7 and S8 are turned OFF. In this case, $V_{AB} = -(V_{C2}+V_{C3})$ and the output current flows from the load to the upper two capacitors through switches S10, body diode of S9, S3 and S4. Fig. 5.4(f) corresponds to state 8 in Table. 5.1, switches S8 and the body diode of S7, are turned ON (S3 and S4 remain ON) and the switches S1, S2, S5, S6, S9 and S10 are turned OFF. In this case, $V_{AB} = -V_{C3}$ and the output current flows from the load to top capacitor through switch S8, the body diode of S7, S3 and S4.

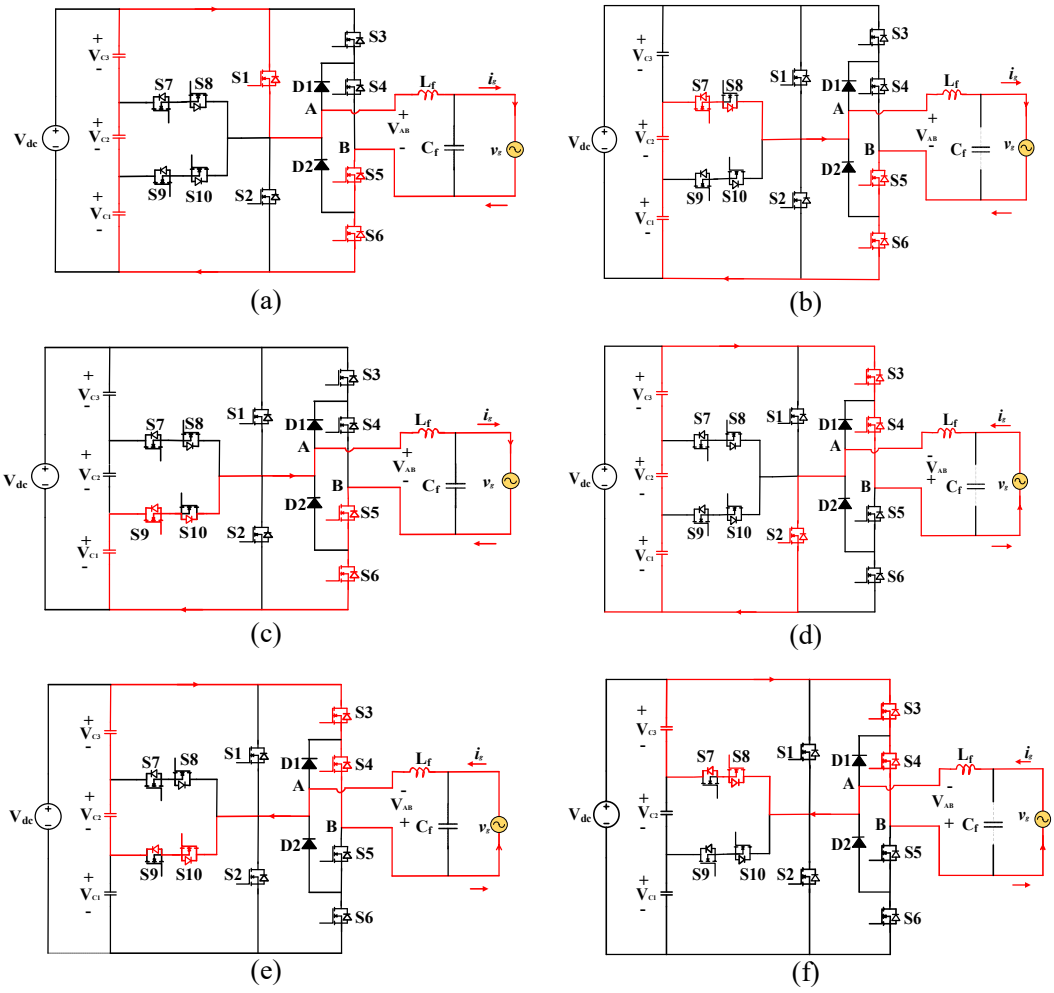


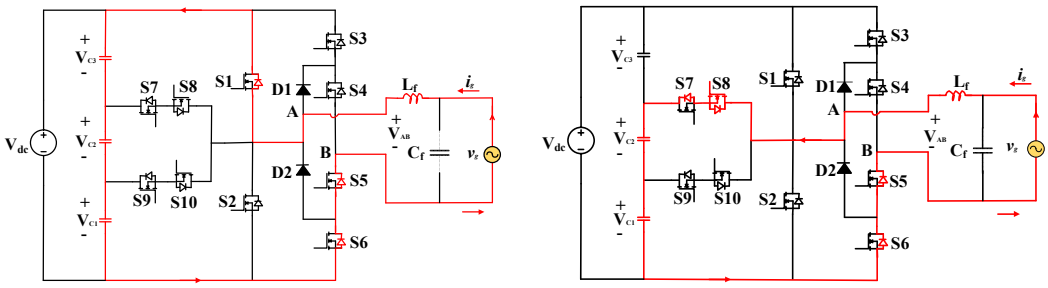
Fig. 5.4. Operating modes of the proposed topology when v_g, i_g are positive and v_g, i_g are negative respectively (a) $V_{AB}= (V_{C1}+V_{C2}+V_{C3})$, (state 1 in Table. 5.1), (b) $V_{AB}= (V_{C1}+V_{C2})$ (state 2 in Table. 5.1), (c) $V_{AB}= V_{C1}$ (state 3 in Table. 5.1), (d) $V_{AB}= -(V_{C1}+V_{C2}+V_{C3})$ (state 6 in Table. 5.1), (e) $V_{AB}= -(V_{C2}+V_{C3})$ (state 7 in Table. 5.1), (f) $V_{AB}= -V_{C3}$(state 8 in Table. 1).

Case. III: Positive grid voltage and negative grid current

When the grid voltage (v_g) is positive and gird current (i_g) is negative, voltage levels ($V_{C1}+V_{C2}+V_{C3}$) = V_{dc}, ($V_{C1}+V_{C2}$) = (2/3)V_{dc} and V_{C1}= (1/3)V_{dc} are produced as shown in Fig. 5.5 and the related states are given in Table. 5.1. For all the states in this mode, current flows from the grid to MLBC; return path for currents are provided by the body diodes of S5 and S6. From Fig 5.5(a), the output voltage V_{AB}= ($V_{C1}+V_{C2}+V_{C3}$) is produced and the current flows through the body diode of S1. In Fig. 5.5(b), S8 and body diode of S7 are conducting to complete the path for the current and the output voltage V_{AB}= ($V_{C1}+V_{C2}$). In state 3, Fig. 5.5(c), S10 and body diode of S9 are conducting to complete the current path and the output voltage V_{AB}= V_{C1}.

Case. IV: Negative grid voltage and positive grid current

When the grid voltage (v_g) is negative and current is positive (i_g), voltage levels ($V_{C1}+V_{C2}+V_{C3}$) = -V_{dc}, ($V_{C2}+V_{C3}$) = -(2/3)V_{dc} and V_{C3} = -(1/3)V_{dc} are produced as shown in Fig. 5.5 and the related states are given Table. 5.1. All the states in this mode, current flows from the MLBC to grid, return path for current is provided by the body diodes of S3 and S4. From Fig. 5.5(d), the body diode of S2 conducts to complete the current path and output voltage V_{AB} = -($V_{C1}+V_{C2}+V_{C3}$). From Fig. 5.5(e), S9 and body diode of S10 are conducting to complete the current path and the output voltage V_{AB} = -($V_{C2}+V_{C3}$). From Fig. 5.5(f), S7 and body diode of S8 are conducting to complete the current path and output voltage V_{AB} = -V_{C3}.



(a) (b)

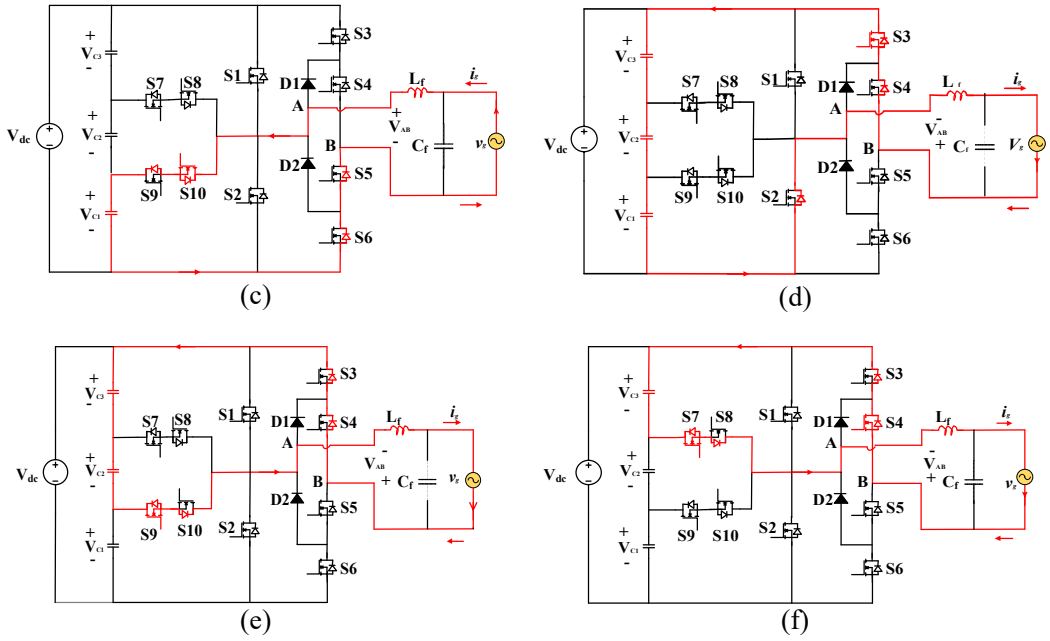


Fig. 5.5. Operating modes of the proposed topology when v_g positive and i_g negative, v_g negative and i_g positive respectively. (a) $V_{AB} = (V_{C1}+V_{C2}+V_{C3})$ (state 1 in Table. 5.1), (b) $V_{AB}= (V_{C1}+V_{C2})$ (state 2 in Table. 5.1), (c) $V_{AB}=V_{C1}$ (state 3 in Table. 5.1), (d) $V_{AB} = -(V_{C1}+V_{C2}+V_{C3})$ (state 6 in Table. 5.1), (e) $V_{AB} =-(V_{C2}+V_{C3})$ (state 7 in Table. 5.1), (f) $V_{AB}= -(V_{C3})$ (state 8 in Table. 5.1).

Table 5.1. Common-mode voltage calculation.

State	V_{AN}	V_{BN}	V_{CM}	V_{DM}	V_{S1}	$V_{TCMV}=V_{BN}$
1	3V	0	1.5V	3V	-1.5V	0
2	2V	0	V	2V	-V	0
3	V	0	0.5V	V	-0.5V	0
4	0	0	0	0	0	0
5	3V	3V	3V	0	0	3V
6	0	3V	1.5V	-3V	1.5V	3V
7	V	3V	2V	-2V	V	3V
8	2V	3V	2.5V	-V	0.5V	3V

* Where V= (1/3)V_{dc}

Case. V: Freewheeling Period

Finally, freewheeling states can be produced in two different forms, as shown in Fig. 5.6. In positive half cycle, switches S4, S5 and S6 are turned ON as shown in Fig. 5.6(a) and state 4 in Table. 5.1. In the negative half cycle switches

S3, S4 and S5 are turned ON as shown in Fig 5.6(b), which corresponds to state 5 in Table. 5.1. To clamp the voltages V_{AN} and V_{BN} to either zero or V_{dc} in the freewheeling period, switches S6 and S3 are turned ON respectively. Therefore, the total common-mode voltage (V_{TCMV}) has only two voltage variations as shown in Table. 5.1. It is evident that in both the cases, the current can flow in any direction through the diodes D1 and D2.

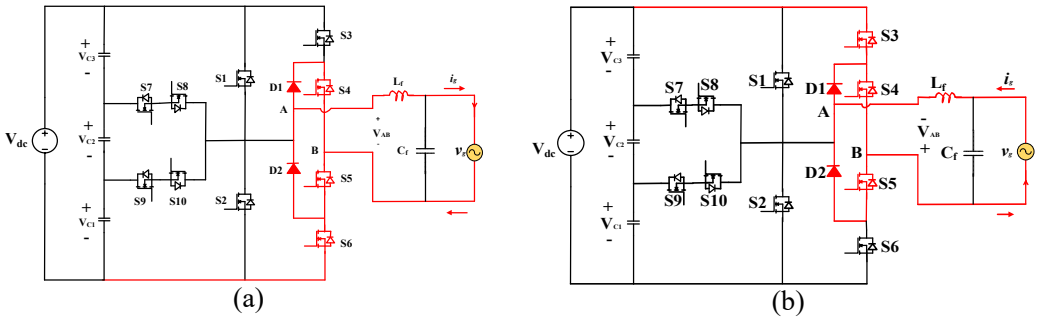


Fig. 5.6. Operating modes of the proposed topology in zero states (V_{AB}=0); (a) state 4 in Table. 5.1, (b) state 5 in Table. 5.1.

5.5. Modified SLS-PWM Technique with Reactive Power Capability

The sinusoidal level-shifted pulse width modulation (SLS-PWM) technique is adapted for the output voltage generation. In this section, a detailed implementation of the modified SLS-PWM is discussed. The seven-level output voltage waveform is synthesized using the states explained in the above section and they are split into four modes of operation. Fig. 5.7 shows various operating modes of the grid and detailed switching patterns for the proposed inverter topology.

For better visualization of the switching pattern, switching frequency (f_s) is selected as 2 kHz and demonstrated for one cycle of operation. It can be noticed that switches S1and S2 are conducting at the top level, which corresponds to positive v_g and negative v_g respectively. S3 and S6 operate at the fundamental frequency of the grid and are complementary. Switch S4 conducts in the positive half cycle and S5 conducts in the negative half cycle. Moreover, switches S4 and S5 also conduct in the freewheeling states to provide the current path under any current direction.

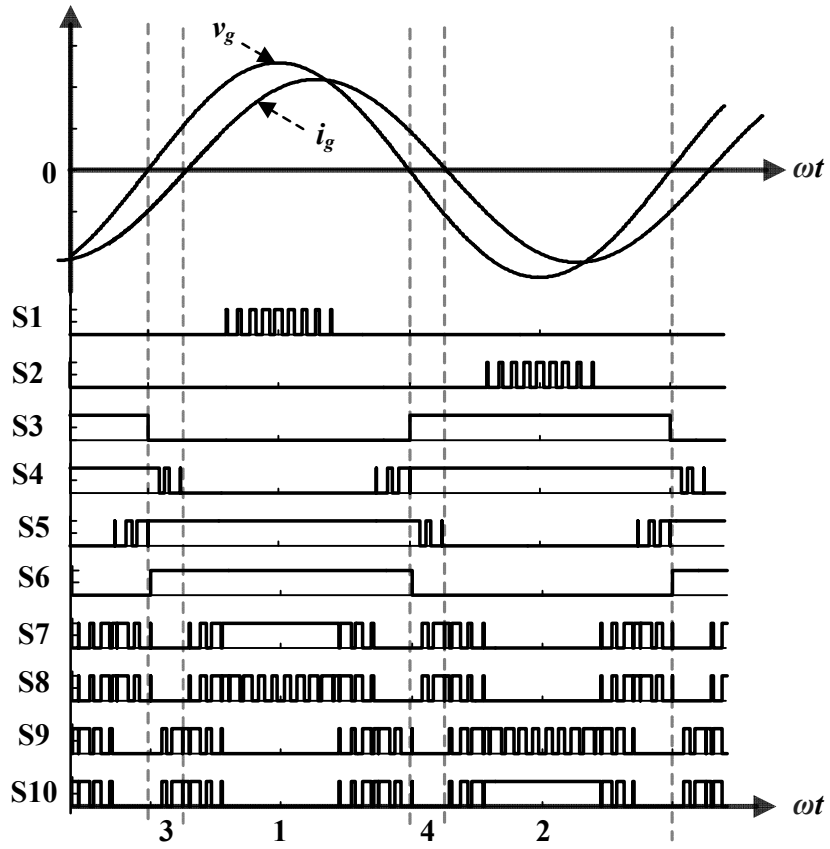


Fig. 5.7. Switching patterns for the inverter switches with reactive power capability.

Mode 1: The grid voltage and currents are positive.

Mode 2: The grid voltage and currents are negative.

Mode 3: The grid voltage is positive and current is negative.

Mode 4: The grid voltage is negative and current is positive.

Switches S7, S8, S9 and S10 along with their body diodes conduct in $(2/3)V_{dc}$ and $(1/3)V_{dc}$ levels in any mode of operation, as shown in Fig. 5.4 and 5.5. To avoid the current dependent the commutation of bi-directional MOSFET branch, gate pulses given to switches (S7, S8) and (S9, S10) are different. A detailed analysis is given in reference [24]. The modulation index (M_a) and the output voltage of the inverter are as follows.

$$M_a = \frac{V_{ref}}{3Vc} \tag{5.4}$$

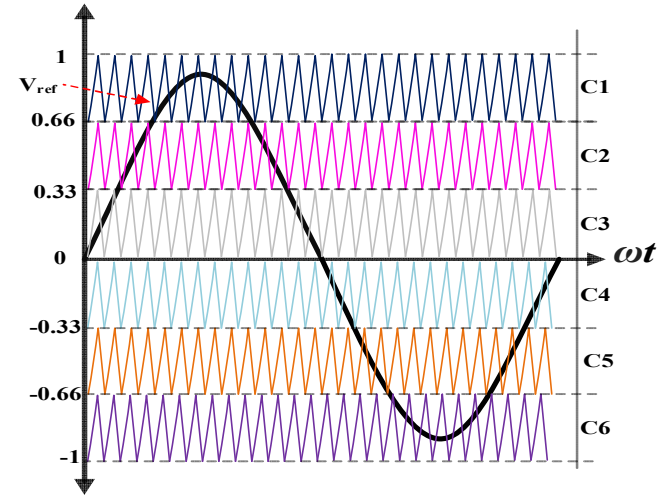
$$v_g = \frac{M_a * V_{dc}}{\sqrt{2}} \tag{5.5}$$

Where V_{ref} is the peak value of reference sine wave and V_c is amplitude of the carrier waveforms. Fig. 5.8(a) illustrates SLS-PWM technique for the seven-level inverter with one sinusoidal reference wave and six triangular carrier waves (C1, C2, C3, C4, C5 and C6). Fig. 5.8(b) shows the detailed implementation of the SLS-PWM technique. The Boolean logic functions derived for the control of switching devices are given in Eq. 5.6.

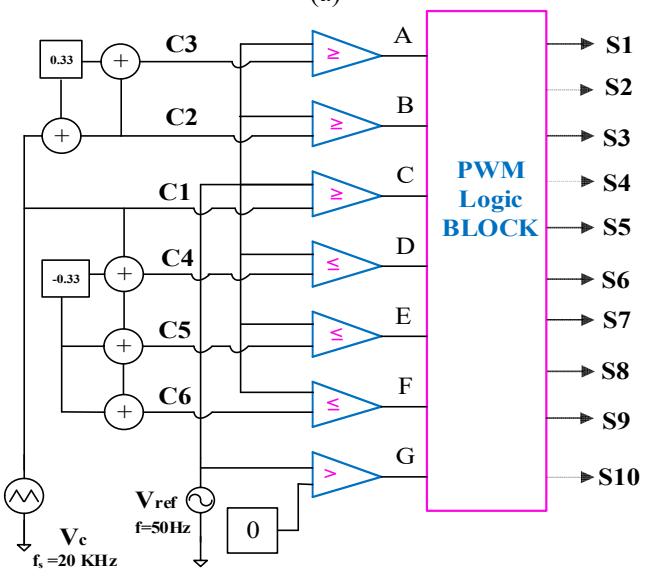
$$S1 = C,\ S2 = F,\ S3 = \overline{G},\ S4 = \overline{G} + \overline{A}$$

$$S5 = G + \overline{D},\ S6 = G,\ S7 = B + E \oplus D,\ S8 = (E \oplus D) + (B \oplus C)$$

$$S9 = (A \oplus B) + (E \oplus F),\ S10 = (A \oplus B) + E \tag{5.6}$$



(a)



(b)

Fig. 5.8. (a) Seven-level SLS-PWM technique, (b) Implementation of SLS-PWM.

5.6. Common-mode voltage Analysis

The CMV analysis of the proposed inverter is carried out regarding the guidelines addressed in Ref [9]. The differential-mode voltage (V_{DM}) and common-mode voltage (V_{CM}) of the inverter are used to analyze the total common-mode voltage (V_{TCMV}) in each state of the inverter. In the proposed transformerless seven-level configuration, the filter inductor is placed between the inverter phase and grid (L_1=L_f and L_2=0). Therefore, the voltage source (V_{S1}) is produced due to asymmetries in line impedances and also asymmetries in the parasitic capacitances between the switches and ground as expressed in Eq. (5.9).

$$V_{DM} = V_{AB} = V_{AN} - V_{BN} \tag{5.7}$$

$$V_{DM} = \left(V_{AN} + V_{BN}\right) * 0.5 \tag{5.8}$$

$$V_{S1} = V_{DM}\left(L_2 - L_1\right) / \left(2*\left(L_1 + L_2\right)\right) = -0.5V_{DM} \tag{5.9}$$

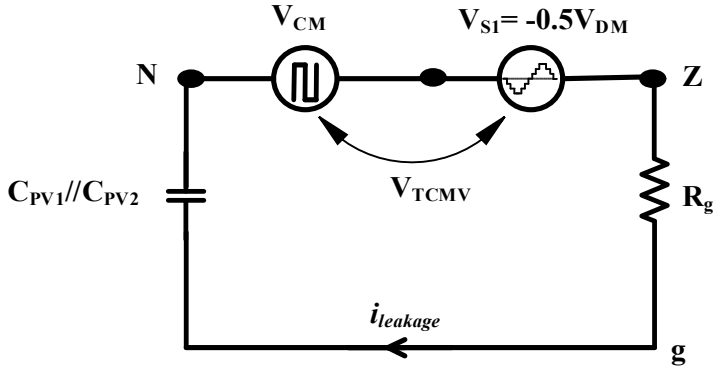


Fig. 5.9. Equivalent common-mode model for the proposed topology.

Fig. 5.9 illustrates the equivalent common-mode model of the proposed configuration. From Fig. 5.1; it can be noticed that the equivalent voltage between terminals N and Z are referred to V_{TCMV}, which directly feeds two impedances in the circuit path, such as equivalent parasitic capacitance C_{PV} (C_{PV1}//C_{PV2}=C_{PV1}+C_{PV2}) of the PV source and the ground resistance R_g. From the Eq. (5.11), the magnitude of leakage current mainly depends on C_{PV} and variations in the total CMV. From Table. 5.1, it is observed that V_{TCMV} has '0' during the positive half cycle i.e. state 1 to 4 and 'V_{dc}' during the negative half cycle i.e., states 5 to 8. The transition between the two values is observed at zero

states; hence V_{TCMV} commutates at the line frequency. Therefore $i_{leakage}$ is maintained almost close to zero most of the time, except at zero crossings, where it exhibits a large spike due to sudden variation in dV_{tcmv}/dt during the transition. Table. 5.1 shows the total common-mode voltage calculation in different states, where it is assumed that all the DC link capacitors are of equal magnitude i.e., $V_{C1}=V_{C2}=V_{C3}= (1/3)V_{dc}$.

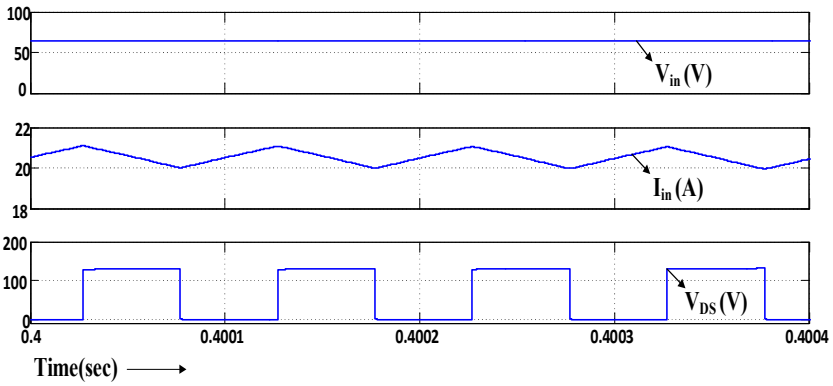
$$V_{TCMV}=V_{CM}+V_{S1}=V_{BN} \tag{5.10}$$

$$i_{leakage}=C_{PV}\frac{dV_{TCMV}}{dt} \tag{5.11}$$

5.7. Simulation Results

In order to verify the theoretical concept as aforementioned, the simulation work is carried out in MATLAB/SIMULINK software. The SLS-PWM technique is implemented to generate the control pulses for hybrid inverter using the switching logic given in section 5.5. Various parameters selected for the simulation work are as follows: input DC voltage V_{in} = 65V, D=0.5, P_{rated} = 1.2 kW, for unity power factor operation, Switching frequency f_s = 20 kHz, M_a= 0.84, passive elements L_b = 0.5 mH (20% of ΔI_{in}), C1=C2=C3=C4=C5=1300 µF (1% of ΔV_{dc}), L_f = 1 mH (20% of Δi_{LP_P}), C_f = 4 µF, C_{PV} = 20 nF and R_g = 100 Ω.

Fig. 5.10(a) shows simulation results of input voltage, current and drain-source voltage (V_{DS}) of Sb. The voltages across the DC-link capacitors V_{C1}, V_{C2}, V_{C3} and also total DC-link voltage are shown in Fig. 5.10(b) and (c) respectively. From Fig. 5.10, it is noticed that the front end MLBC is operating in continuous conduction mode (CCM) and generating a three-level balanced DC-link voltage.



(a)

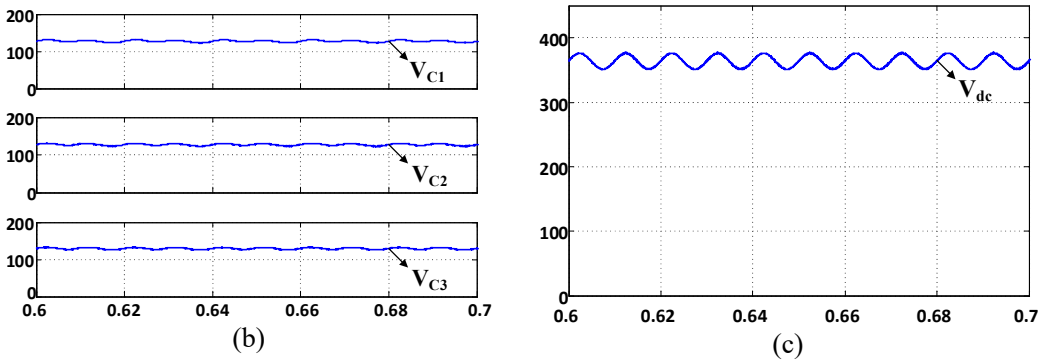


Fig. 5.10. Simulation results of MLBC; (a) input voltage, current and drain-source voltage of Sb, (b) balanced capacitor voltages (c) total DC-link voltage.

The total DC output voltage of the MLBC is further fed to the inverter stage to produce seven-level output voltage, as shown in Fig. 5.11(a). The filtered output voltage and load current waveforms for unity, (0.58) lagging and (0.58) leading power factors of the load are given in Fig. 5.11(b), (c) and (d) respectively. It can be noticed that the proposed topology is capable of supplying reactive power, as explained in Section. 5.4.

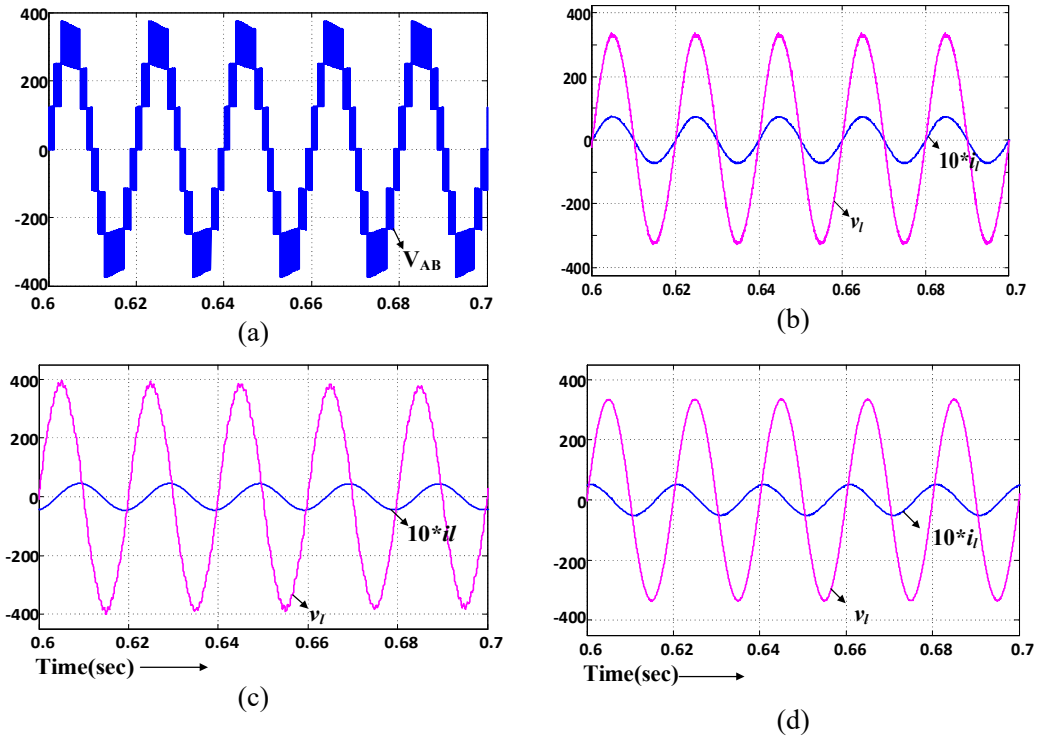


Fig. 5.11. Simulation results for the proposed seven-level inverter: (a) seven-level output voltage (b), (c) and (d) v_l and i_l at unity, lagging (0.58) and leading (0.58) power factor operations respectively.

The measured FFT spectrums for the seven-level MLI output waveforms are given in Fig 5.12. Fig 5.12(a) depicts the total harmonic distortion (THD) of seven-level voltage and Fig 5.12(b) and (c) depict the load voltage and current after the LC filter respectively. It can be noticed that the measured THD of voltage reduced from 23.71% to 1.45% after filtering and the current THD is 1.45%. This confirms that the designed LC filter effectively attenuates the harmonic content and it is within the limits of IEEE1547 grid standards.

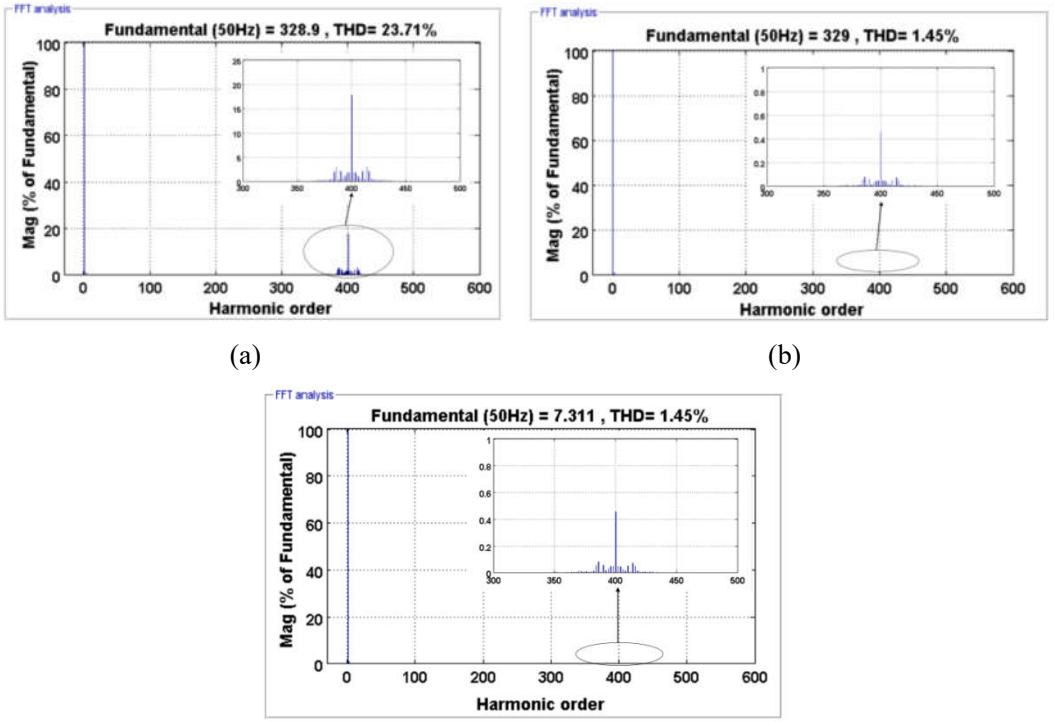


Fig. 5.12. THD spectrums of the seven-level MLI: (a) terminal voltage V_{AB} and, (b) load voltage and, (c) load current with R load.

Figs. 5.13.(a)-(d) illustrate the measured waveforms of terminal voltages V_{AN}, V_{BN}, V_{CM} and $i_{leakage}$ respectively. It is to be noted that uncontrolled spikes in the leakage current appear with grid frequency variation due to changes in V_{TCMV}. Moreover, the magnitude of the spikes depends on the V_{TCMV} and parasitic capacitance (C_{PV}) formed by the PV source. The transitions in V_{TCMV}, at every zero crossing generates a spike, as shown in Fig. 5.13.(d). Here, the root mean square (RMS) value of leakage current is 40mA, which is much below the DIN VDE 0126-1-1 grid standards. The ground resistance may help to suppress these peaks of the leakage current [88].

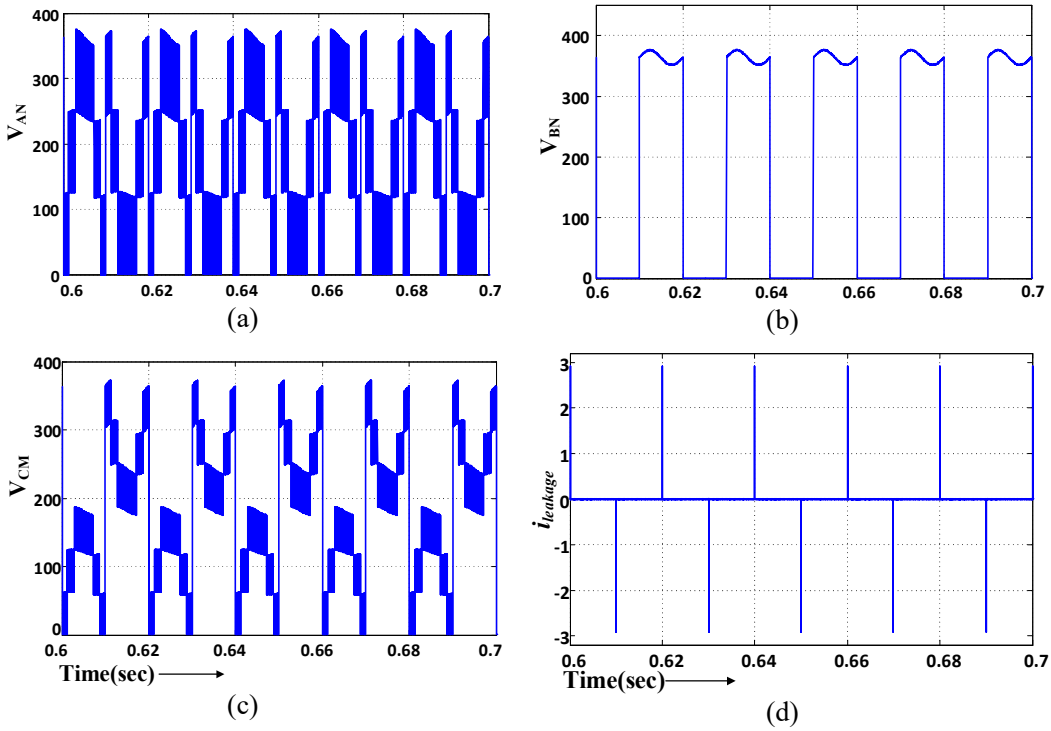


Fig. 5.13. Simulation results of seven-level inverter; (a) voltage V_{AN}, (b) voltage V_{TCMV} (=V_{BN}), (c) CMV and (d) Leakage current $i_{leakage}$.

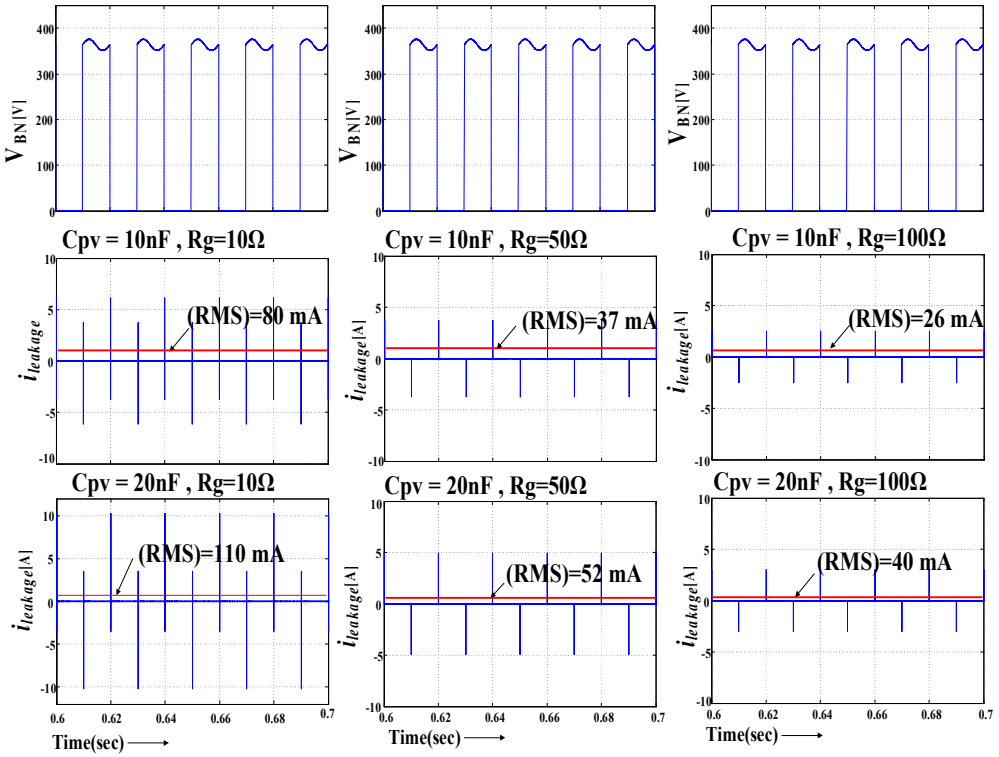


Fig. 5.14. Total common-mode voltage V_{TCMV} (=V_{BN}) and leakage current ($i_{leakage}$) at three different parasitic capacitance and ground resistance conditions.

To prove the effectiveness of the proposed topology in limiting RMS leakage current, three different combinations of ground resistances and parasitic capacitances are considered to evolve at the leakage current magnitude. From Fig. 5.14, it can be noticed that in all three cases, the RMS leakage current does not exceed German DIN VDE 126-1-1 grid standards. Hence, the proposed circuit configuration is effective in limiting the leakage current.

Fig. 5.15 illustrates the performance of the proposed system with MPPT and grid-connected mode for changes in PV insolation from 1000 W/m^2 to 600 W/m^2. Two series (N_S) and three parallel (N_P) combinations of PV-MLU255HC panels were used as PV sources. Specifications of the PV panel at standard test conditions are; Voltage at maximum power V_{MPP}=31.2 V, Current at maximum power I_{MPP}=8.18A and Maximum power P_{MPP}=255W. Simple Perturb and Observation algorithm is used for MPPT operation. It can be noticed that the dc-link voltage and grid voltage is well regulated and corresponding changes in the power levels were also observed at 0.6 sec.

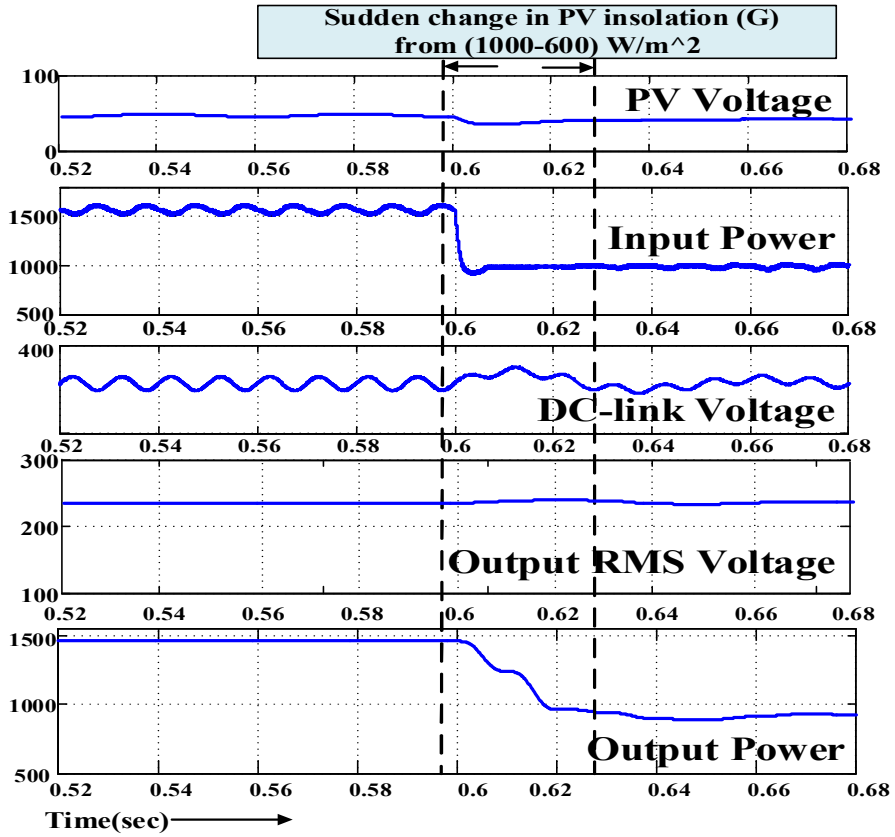


Fig. 5.15. Voltage and power results of grid-connected two-stage inverter when insolation changes from 1000 W/m^2 to 600 W/m^2

To show the modularity of the proposed two-stage system, five-level generation is presented through Fig. 5.16 with a reduction in one basic unit as compared to seven-level operation. Figs 5.17(a) and (b) show the balanced DC-link voltages and the total DC output voltage of the two-stage MLBC, which is fed to the inverter stage to produce five-level output voltage as shown in Fig. 5.17(c). The filtered output voltage and their corresponding load current for unity power factor (UPF) operation are given in Fig. 5.17(d).

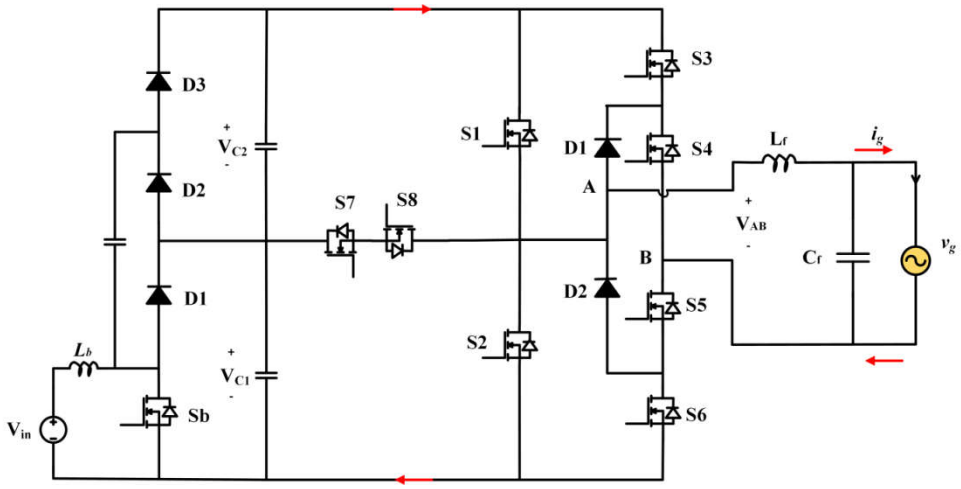


Fig. 5.16. Proposed two-stage five-level inverter.

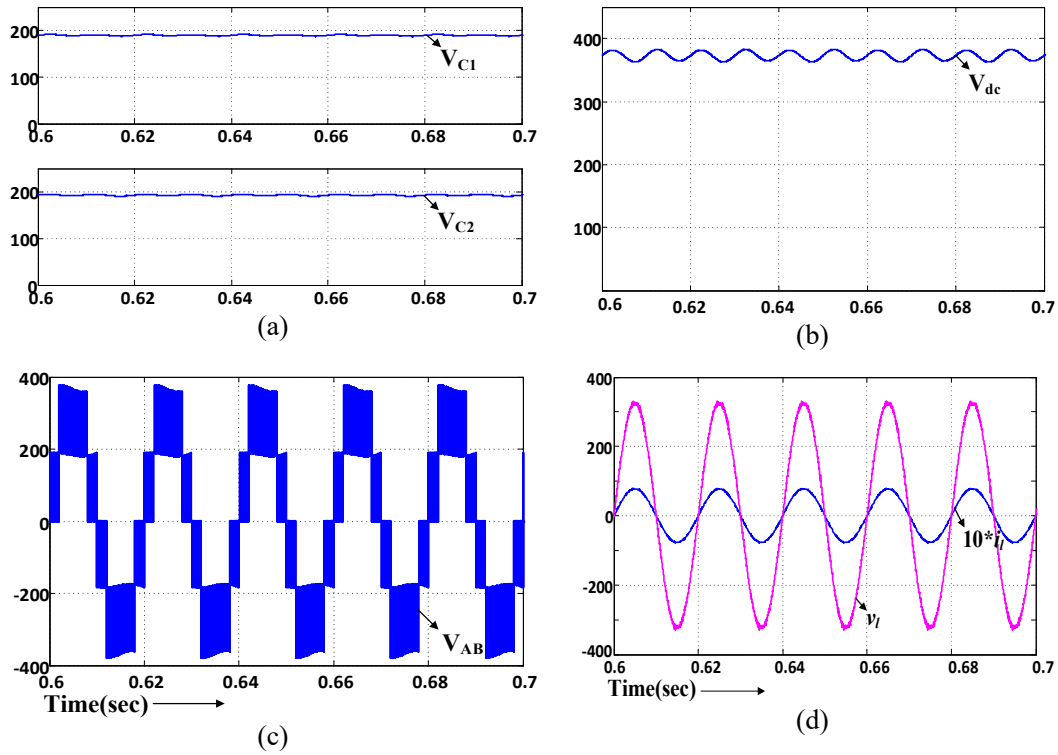


Fig. 5.17. Simulation results of the proposed five-level inverter; (a) DC capacitor voltages, (b) DC-link voltage, (c) five-level inverter voltage and, (d) output load voltage and current after the LC filter.

5.8. Experimental Results

To verify the effectiveness of the proposed two-stage system, a 200 W experimental prototype was built with available lab components as a proof of concept. Fig. 5.18 shows the experimental prototype, which consists of power circuits with switches IRF460, diodes MUR1520, TLP250 based driver circuits, controllers and loads. The PWM pulses to the MOSFET switches in the inverter are produced by DIGILENT ATLYS Spartan-6 FPGA board with Ma = 0.84. DSP TMS320F28335 is used for the generation of control pulse to the MOSFET used in MLBC.

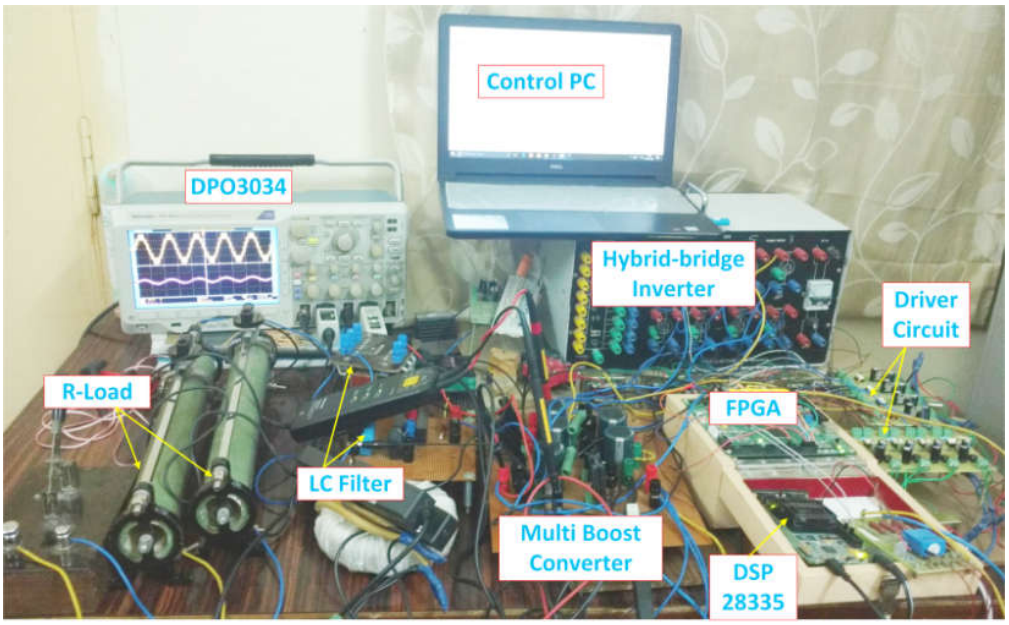
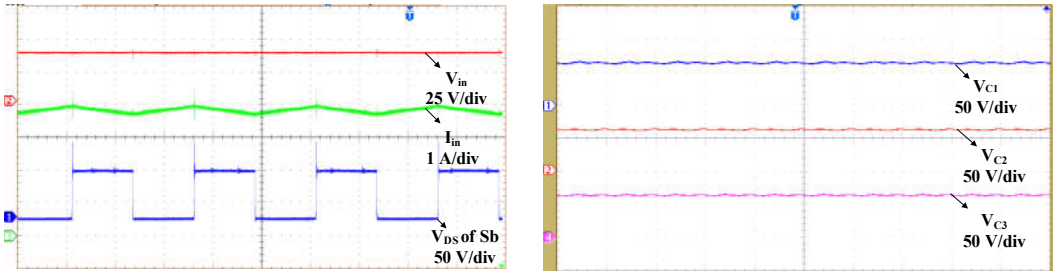


Fig. 5.18. Experimental setup.

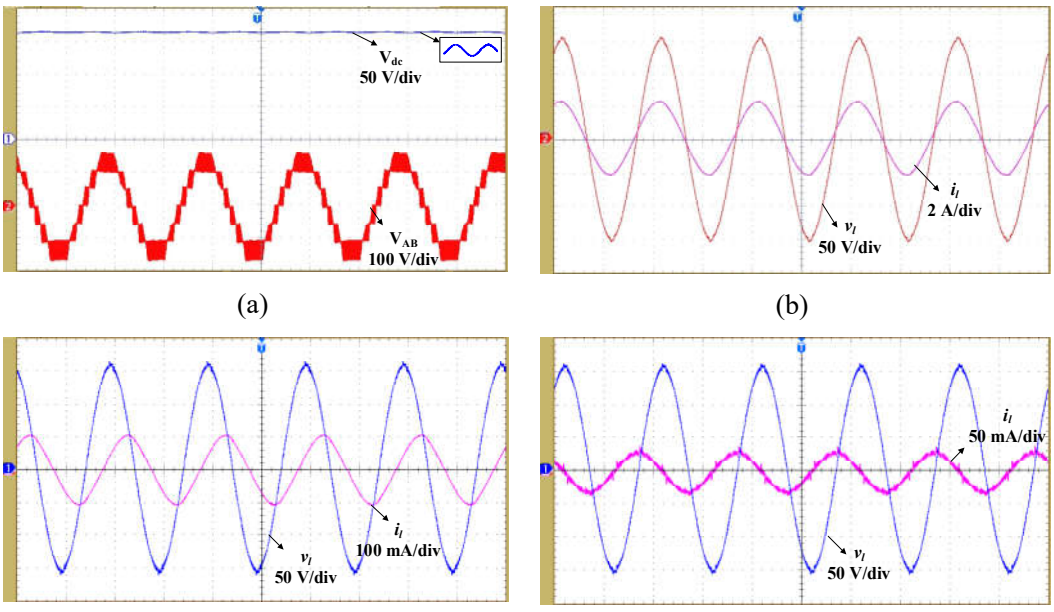
The specifications of various components for the experiment are as follows: Input DC voltage $V_{in} \approx 31$ V, switching frequency (f_s) as 20 kHz, duty ratio D = 0.5, boost inductor L_b = 0.6 mH (20% of ΔI_{in}), DC-link capacitors C1=C2=C3=C4=C5 ≈ 1000 µF (1% of ΔV_{dc}), L_f = 1mH (20% of Δi_{LP_P}), C_f = 3 µF, C_p = 20 nF and R_g = 100 Ω. The waveforms are captured using DPO 3034 with the help of differential voltage probe TMDP0200 and current probe TCP 0030. The experimental results for the proposed two-stage seven-level inverter are given in Figs 5.19 to 5.23. Fig. 5.19(a) depicts the input voltage, current and drain-source voltage. It is observed that the input current is continuous in nature, which confirms that the MLBC is operating in CCM. The balanced DC-link voltages of the MLBC are depicted in Fig. 5.19(b).



(a) (b)

Fig. 5.19. Experimental results of the MLBC; (a) input voltage, current and drain-source voltage of Sb, (b) balanced DC-link voltages.

The measured total DC-link voltage across the output of MLBC, seven-level output voltage, filtered output voltage and load current are shown in Fig 5.20(a) and (b) respectively. Figs. 5.20(c) and (d) show the waveforms of seven-level inverter under 0.58 lagging load and 0.58 leading load conditions. This shows that the proposed configuration is capable of controlling the reactive power without affecting the common-mode voltage behavior and multilevel output quality.



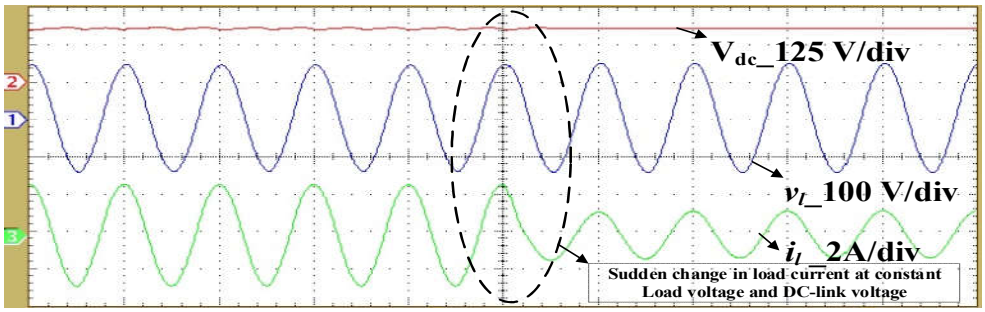
(a) (b)

(c) (d)

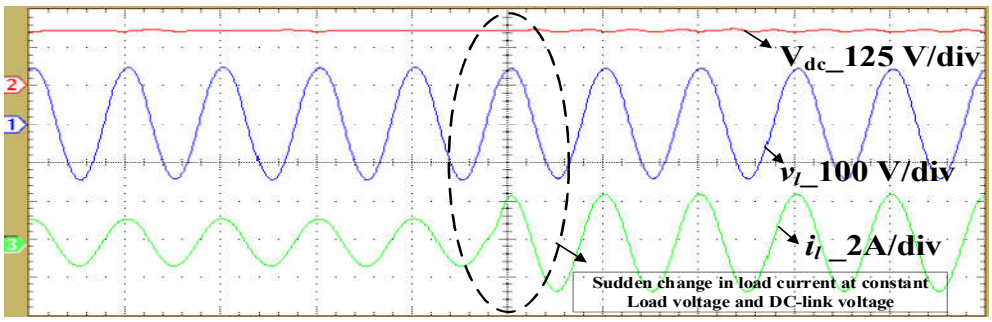
Fig. 5.20. Experimental results of the proposed topology (a) total DC-link voltage and seven-level voltage; load voltage and current under (b) UPF, (c) 0.58 lagging and, (d) 0.58 leading conditions respectively.

Further, the dynamic response of the proposed multilevel inverter is obtained by implementing a simple PI controller in DSP TMS320F2812 controller, as explained in the previous chapter. Figs 5.21(a) and (b) show the

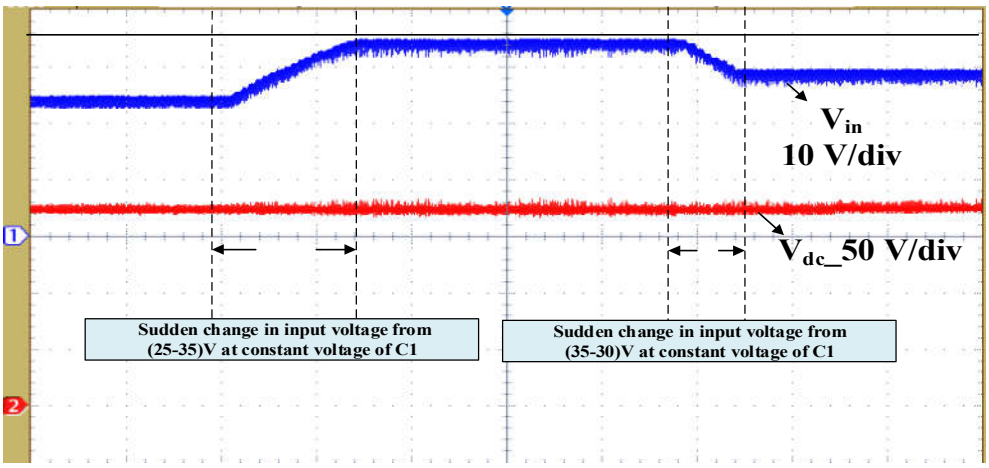
dynamic response of the proposed system under step change in load from 350 Ω to 150 Ω and vice-versa. Similarly, it can be noticed that, from Fig. 5.21(c) the DC-link voltage is kept constant as the input DC voltage changes from 25V to 35V and then to 30V. It shows that the proposed two-stage system and its modulation scheme can effectively feed power into the grid under temperature and insolation changes of the PV source. Here the currents in Figs. 5.21(a) and (b) are multiplied by a factor of three to better visualize the response.



(a)



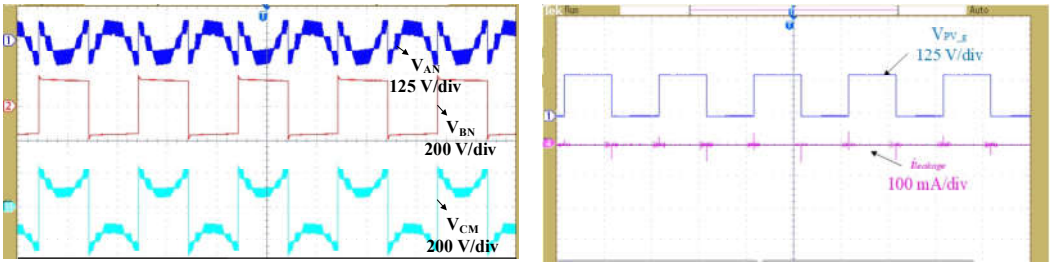
(b)



(c)

Fig. 5.21. Experimental results of the proposed topology (a) and (b) step change in load current from high to low and low to high at constant output voltage and (c) transient voltage variations in input voltage and their corresponding DC-link voltage.

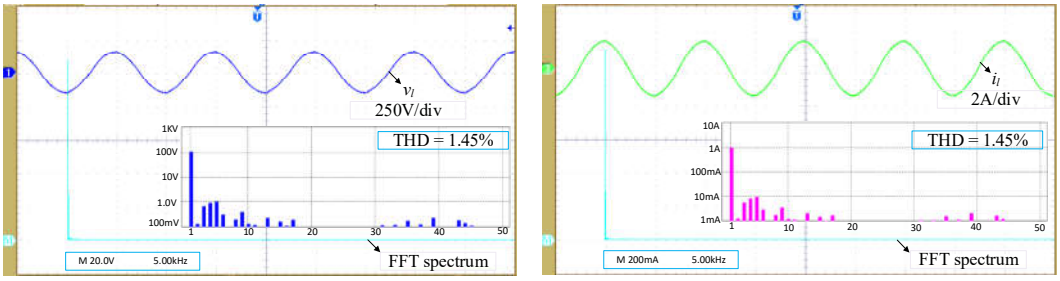
Fig. 5.22(a) shows the waveforms of the inverter terminal voltage V_{AN}, V_{BN} and V_{CM}. Fig. 5.22(b) shows the voltage waveform across the input DC source positive terminal to ground and corresponding leakage current flowing through the parasitic capacitor. It can be observed that the voltage across C_{PV} varies at grid frequency. Consequently, the leakage current consists of sudden spikes when there is a transition of voltage $V_{N\text{-}g}$ from zero to V_{dc} as explained in section 5.5. The RMS value of $i_{leakage}$ reaches 7.146 mA, which is well below 300 mA limit imposed by German DINVDE0126-1-1 grid standards. The experimental performance of the proposed system shows that the absence of high-frequency transitions in the CMV. Therefore, the leakage current $i_{leakage}$ is significantly reduced.



(a) (b)

Fig. 5.22. Experimental results of the proposed topology (a) terminal voltages of V_{AN}, V_{BN} and V_{CM} and (b) terminal voltage across DC source to ground V_{Ng} and corresponding leakage current.

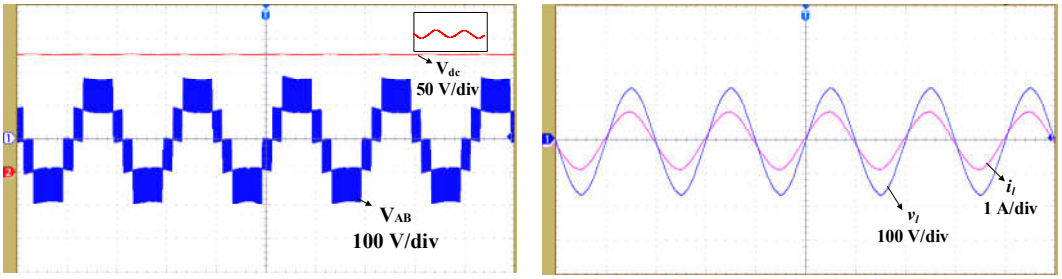
In addition, the experimental THD of the proposed configuration is measured using DPO 3034 and YOKOGAWT310E digital power meter, shown in Figures 5.23(a) and (b). It is observed that the filtered output voltage and their corresponding load current THD of 1.45% show good agreement with the simulation results and also meet IEEE1547 grid standards.



(a) (b)

Fig. 5.23. Experimental FFT spectrums for the proposed seven-level MLI
(a) load voltage, (b) load current.

Further, to verify the modularity feature of the proposed configuration, the experimental prototype is restructured for the generation of five-level operation. Fig. 5.24 shows the experimental results of the five-level inverter under UPF operation. The measured DC-link voltage across the output of MLBC, five-level inverter output voltage and filtered output voltage and their corresponding load current respectively are shown in Figs. 5.24(a) and (b). From there, the experimental results are found to be in good agreement with the simulation results. The CMV and leakage current justifies that the proposed transformerless hybrid PV inverter is well suited for grid-connected PV applications.



(a) (b)

Fig. 5.24. Experimental results of the proposed two-stage five-level inverter (a) DC-link and level voltage, (b) filtered output voltage and current waveforms under UPF.

5.9. Comparison with the Existing Topologies

In this section, a comparison of the two-stage topologies with the proposed system is given to highlight its merits. From Table 5.2, it can be noticed that the boosting factor of the proposed two-stage system is double without using HFT and extreme duty ratio. Hence, it requires fewer number PV panels connected in series to maintain required DC-link voltage, which improves the performance of MPPT and also efficiency. Moreover, the modular structure of the topology enables an increase in the number of levels in output voltage, which leads to an enhancement in the quality of output power with reduced filter size. Furthermore, the magnitude of leakage current is limited below the DIN VDE0126-1-1 grid standard without employing LFT or EMC filter, which increases the efficiency and reduces the size of the overall two-stage system. Finally, reactive power capability is achieved with a circuit structure and with modified SLS-PWM. But, the limitation of the proposed method is that an

increase in the number of components used. However, the overall performance of the proposed two-stage system is better than the existing topologies in refs [77]-[79].

Table 5.2 Comparison various two-stage configurations.

Part Name	**Ref[77]**	**Ref[78]**	**Ref[79]**	**Proposed**
MOSFET	9	8	10	11
Diode	3	5	3	7
HFT	1	1	1	-
Capacitor	2	2	2	5
Boosting factor	$1.5kV_{in}$	$1.5kV_{in}$	$1.5kV_{in}$	$3kV_{in}$
Modularity	-	-	-	Yes
Leakage current	-	-	-	< 300mA
LFT or EMC filter	Yes	Yes	Yes	-
Voltage stress of MOSFET	$4.58V_{dc}$	$6V_{dc}$	$7V_{dc}$	$8.33V_{dc}$
Blocking voltage of Diode	$1.08V_{dc}$	$2.33V_{dc}$	$2.33V_{dc}$	$3.33V_{dc}$
Reactive power possibility	Yes*	No	Yes*	Yes

Table 5.3. Comparison of the proposed topology with conventional MLI topologies

Part Name		**DC**	**FC**	**CHB**	**Proposed**
MOSFET		12	12	12	10
Diodes		30	0	0	2
Capacitors	DC-link	6	6	3	3
	Auxiliary	0	15	0	0
DC Sources		1	1	3	1

In Table 5.3, a comparison of conventional seven-level inverters with the proposed hybrid inverter is given in Refs [10], [51]. The total number of active and passive components and DC sources required for the realization of seven-level output are fewer in comparison with conventional multilevel inverters. Hence the cost and size of the proposed inverter is lower.

Table 5.4. Parameters and devices used for the calculation of efficiency

Parameter	**v_O**	**F**	**f_s**	**L_b**	**D**	**M_a**	**L_f**	**C_f**	**C1-C5**	**C_{PV}**
Value	230V	50Hz	20kHz	0.5mH	0.5	0.84	1mH	4µF	1300µF	20nF
Device	**S1 to S6**		**S8 and S9**		**S7, S10 and Sb**			**Diodes**		-
Part number	FCA76N60N		IRF300P227		IRFP4127PbF			RUR1S1560S		-
Rating	400V/76A		300V/50A		250V/75A			600V/15A		-

5.10. Efficiency Calculation

Generally, losses in the semiconductor devices depend on the conduction period and the corresponding blocking voltage. The selection of switches is based on the blocking voltage with lower on-state resistance enhances the overall efficiency of the system. Table 5.4 lists the various parameters, switches and diodes and their corresponding part number used for the calculation of efficiency in both theoretical and PSIM studies. The theoretical evaluation of losses is carried out using the standard equations were discussed in the previous chapter (section 4.6). To validate the losses, PSIM thermal module is implemented for the proposed configuration with the real parts as datasheets.

Fig. 5.25 illustrates the developed two-stage configuration of the PSIM thermal module (where thermal resistances and parasitic resistances are not shown for simplicity of the drawing). Distribution of losses due to various switches and diodes using PSIM are drawn in Fig. 5.26. It is observed that the switching losses are reduced considerably in comparison with conduction losses. Switches S3, S4, S5 and S6 operate almost close to grid frequency and the blocking voltage is V_{dc}, thereby the losses are equal. The clamping diodes used in the NPC leg conduct only in the freewheeling period; hence the losses are very

low. Losses across switches S1 and S2 are equal because the blocking voltage and operating frequency are the same. The bi-directional switches S7 and S8 are operating at different frequencies and blocking voltages. For example, switch S7 blocks voltage of $(2/3)V_{dc}$ and switch S8 blocks voltage of $(1/3)V_{dc}$ and also they are operating at different frequencies. Therefore, the losses in the bi-directional branch switches are different in the proposed inverter. The power loss in the boost converter switch Sb and diodes (D_{b1}-D_{b5}) are shown in Fig. 5.26(b). Finally, from Fig. 5.27, it can be concluded that the efficiency of both the theoretical and PSIM simulation match so well that it validates the performance of the developed system.

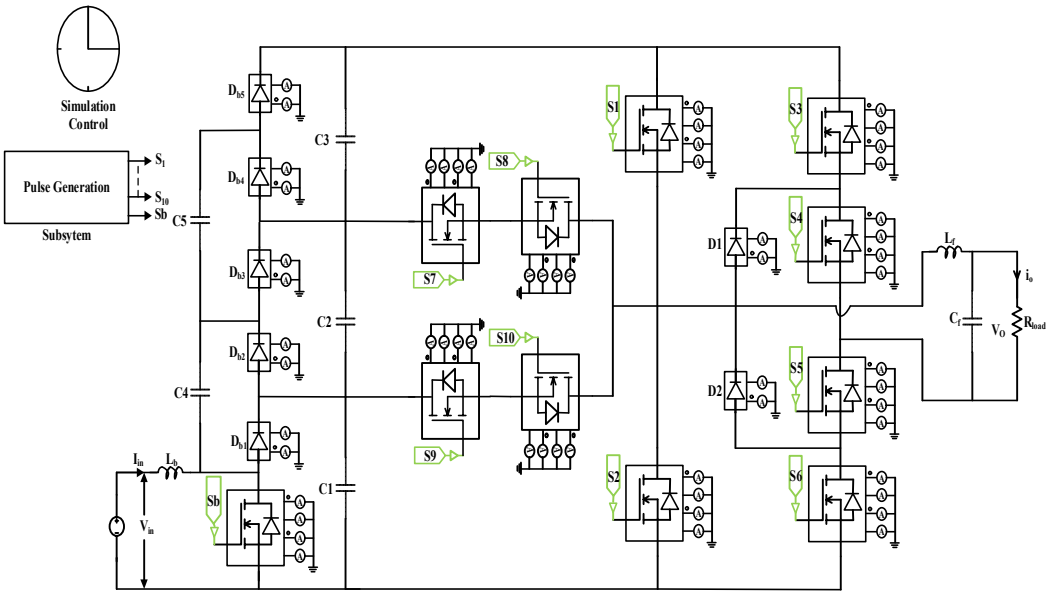
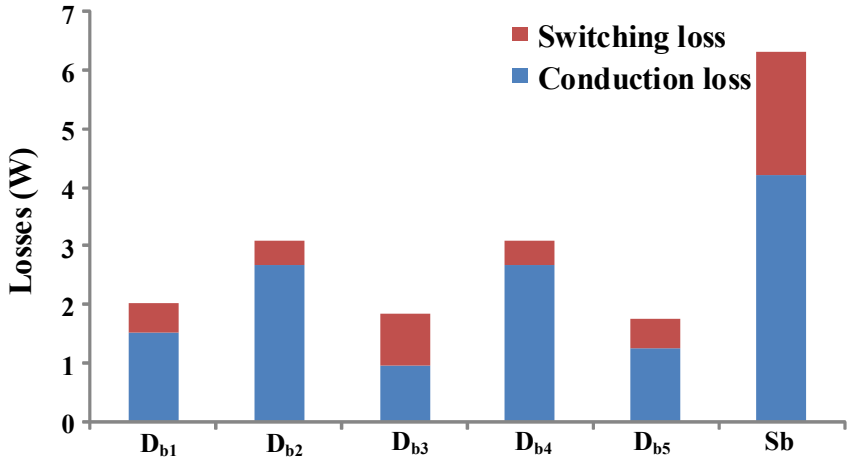


Fig. 5.25. PSIM thermal module model for the proposed two-stage seven-level MLI.

(a)



(b)

Fig. 5.26. Distribution of power losses in the semiconductor switches of (a) hybrid seven-level inverter (b) multilevel boost converter.

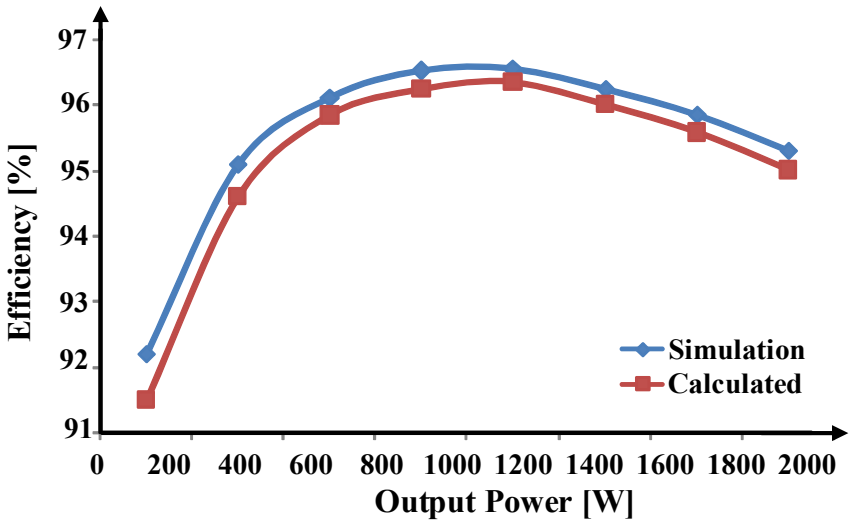


Fig. 5.27. Efficiency curve.

5.11. Summary

A single-phase two-stage hybrid multilevel inverter for grid-connected PV applications is presented. The self-balanced capacitor voltage capability of the MLBC enables low control complexity and modularity for any level output of DC and also provides high boosting gain. The proposed multilevel inverter structure and its modulation technique provide the bi-directional path to the current in all modes of operation. Besides, reactive power control is also possible without affecting common-mode voltage behavior and the output levels in the

multilevel inverter. The leakage current is within the limits of German DIN VDE0126-1-1 grid standards due to grid frequency variations in total CMV. Thus, the proposed two-stage system provides high-quality output power and efficiency for the grid-connected PVPGS.

5.12. Contributions

a) Requires lower switch count for the realization of seven-level output voltage in comparison with traditional NPC, FC, and CHB topologies.
b) Functions like boosting of the PV voltage, balancing the DC-link capacitor voltages, and the reduction of leakage current can be achieved without the use of high-frequency transformer.
c) The modified SPWM scheme provides the bi-directional current path to the inverter for supporting the reactive power flow without disturbing the waveform quality.
d) Moreover, both converter and the inverter are modular to obtain the more number of output voltage levels.

5.13. Papers Published

1) Sateesh Kumar Kuncham, Kirubakaran Annamalai, and Subrahmanyam Nallamothu. "**A new structure of single-phase two-stage hybrid transformerless multilevel PV inverter**" *International Journal of Circuit Theory and Applications,* vol. 47 (1), pp. 152-174, Jan-2019.
2) K. Sateesh Kumar, A. Kirubakaran, N. Subrahmanyam **"A Hybrid-Bridge Asymmetrical Transformerless Five-Level Photovoltaic Inverter",** *14th IEEE INDIA council (INDICON) Conference,* pp.1-6, 2017.

Chapter 6

A Two-Stage T-type Hybrid Five-Level Transformerless Inverter

Chapter 6

A Two-Stage T-type Hybrid Five-Level Transformerless Inverter

6.1. Introduction

The two-stage hybrid MLI proposed in chapter 5 has the advantage of high voltage gain, self-balancing of the DC-link capacitor voltages, reactive power capability and the reduction of leakage current without the use of the isolation transformer. However, due to the sudden transition in V_{TCMV} from 'V_{dc}' to '*0*' induces a sudden spike in the leakage current. Sometimes, it can cross the grid standards due to the intermittent nature of the PV parasitic capacitance. In addition to that, the front-end boost converter requires more number of capacitors and diodes to realize the boosting and multilevel operation. Therefore, to address the above-said problems, this chapter presents a two-stage T-type hybrid five-level TLI for grid-connected PV applications. The proposed T-type hybrid five-level inverter and its SLS-PWM scheme offers, (i) Reduced leakage current by eliminating the high-frequency variations and sudden transitions in the voltage across PV parasitic capacitance (C_{PV}), (ii) A path for the negative current in all the modes of operation under unity and non-unity power factor conditions of the grid without degrading the waveform quality.

Moreover, in this chapter, the proposed inverter is integrated with a traditional three-level boost converter (3LBC) for boosting the lower PV voltage to higher DC-link voltage and also to extract maximum power from the PV source. The 3LBC will provide high efficiency and reduced input inductor size for the same power rating over the conventional boost converter. Simulation results of the proposed system are presented using MATLAB software and a 500 W experimental prototype is constructed and tested in the laboratory to validate the feasibility of the recommended configuration. Finally, a comparison of the proposed inverter with other five-level TLI topologies is presented to highlight its merits.

6.2. System Description

Fig. 6.1 depicts the schematic arrangement of the proposed two-stage inverter configuration. It comprises a 3LBC followed by a proposed T-type hybrid five-level TLI with the symmetrical placement of the filter circuit. 3LBC serves the functions of both voltage boosting and MPPT by employing a simple closed-loop control system. Further, the proposed inverter produces output AC voltage by switching MOSFETs using the SLS-PWM scheme, which enhances the inverter operation at all power factors without affecting the CMV. Moreover, symmetrical placement of the *LCL* filter circuit provides a common-mode conducting path to the inverter for limiting the magnitude of leakage current below the grid standards. Operation and control of 3LBC is explained as follows,

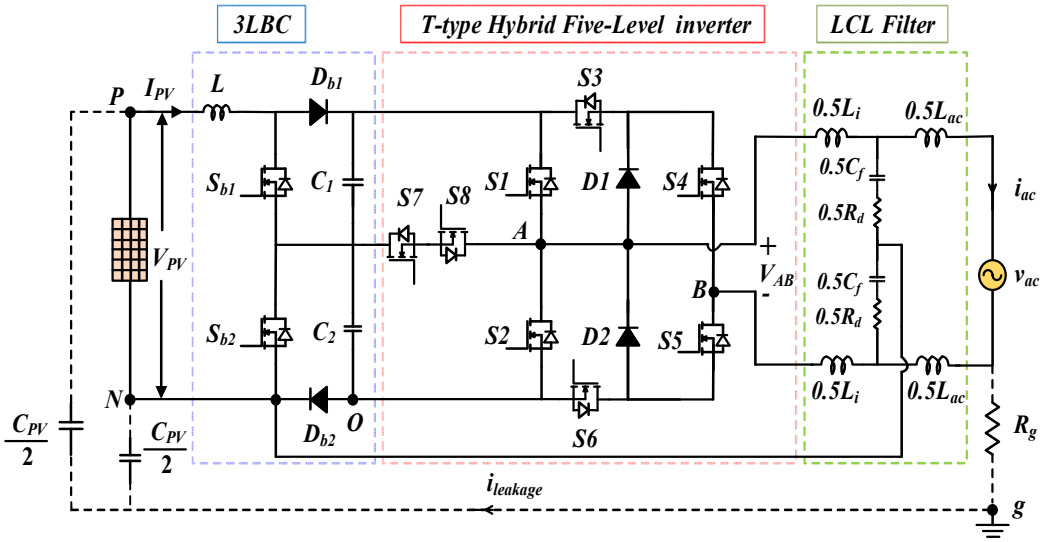


Fig. 6.1.Proposed two-stage T-type hybrid five-level TLI.

6.2.1. Front-end 3LBC

Fig. 6.2 depicts the front end 3LBC given in [106], which comprises of boost inductor L, two DC-link capacitors C_1 and C_2 and two switches S_{b1} and S_{b2}. Depending on switching states, the 3LBC has four modes of operation, as shown in Fig. 6.3. Mode 2 and Mode 3 occur when either S_{b1} or S_{b2} is turned ON. Mode 1 and Mode 4 occur when S_{b1} and S_{b2} are turned ON or OFF respectively. It is noticed that there are two operating regions based on the value of duty ratio D. In region1, R1 ($0<D<0.5$) allows the converter to operate in Modes 2, 3 and 4. In region2, R2 ($0.5<D<1$) enable the converter to operate in Modes1, 2 and 3.

The control pulses for the switches S_{b1} and S_{b2} are generated with a simple control circuit, as depicted in Fig. 6.2, where the reference duty cycle (D_{ref}) is generated from the MPPT controller to track maximum PV power. Further, to balance the DC-link capacitor voltages duty ratio ΔD is produced with a simple PI controller and then it is passed through the PWM circuit to generate the control pulses S_{b1} and S_{b2}. Eq. (6.1) gives the relation between input PV voltage and DC-link voltage. Where, V_{PV} and V_{dc} indicate the PV source voltage and total DC-link voltage respectively.

$$V_{dc} = \frac{V_{PV}}{(1-D)} \tag{6.1}$$

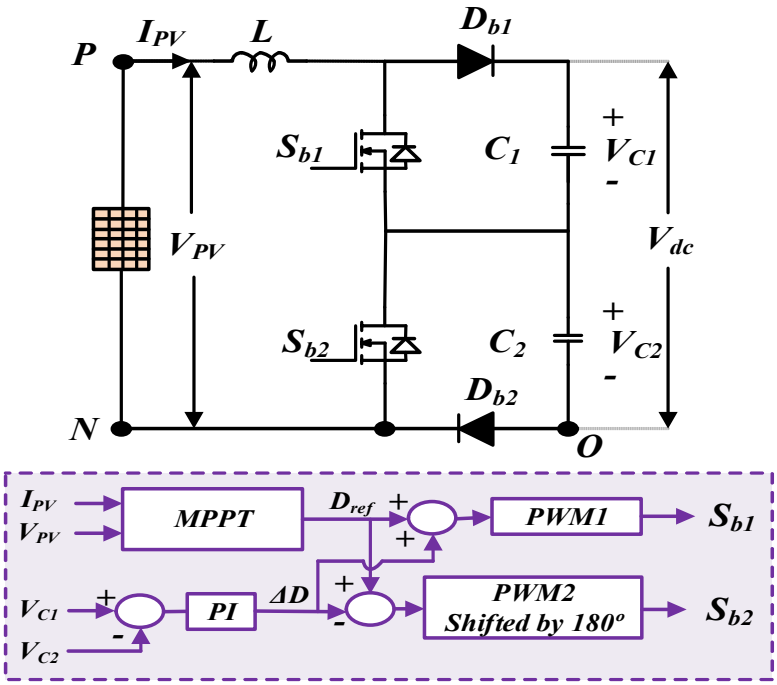
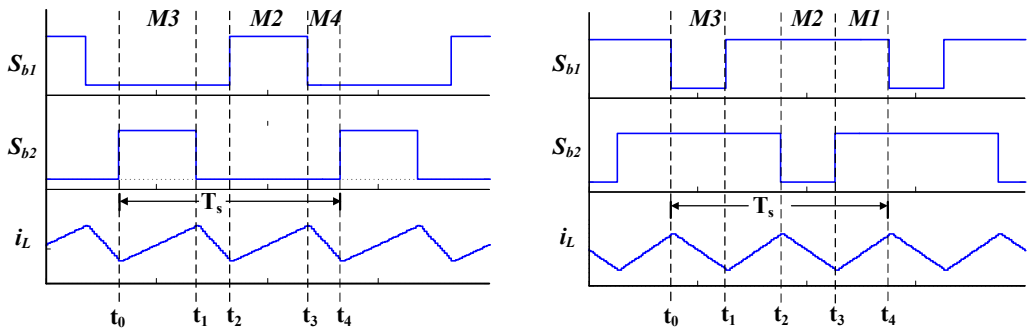


Fig. 6.2. Block diagram of 3LBC with PI control.



(a) (b)

Fig. 6.3. Gate pulses and inductor current of *3LBC*: (a) region 1, (b) region 2.

6.3. Proposed T-Type Hybrid TLI

6.3.1. Circuit Structure

The proposed five-level TLI, as depicted in Fig. 6.4 comprises a half-bridge leg *(S1*, *S2),* a neutral point clamping (*NPC*) branch *(D1*, *D2*, *S3*, *S4*, *S5 and S6)* and a T-type bi-directional clamping branch *(S7, S8)*. The combination of half-bridge leg and *NPC* branch forms a hybrid structure and it is further enhanced with T-type bi-directional clamping branch to build a T-type hybrid five-level inverter. Hybrid structure generates the polarity and the bi-directional MOSFET branch enables the capacitor selection for five-level output and also clamps the inverter terminal voltages to $V_{dc}/2$ during the freewheeling period.

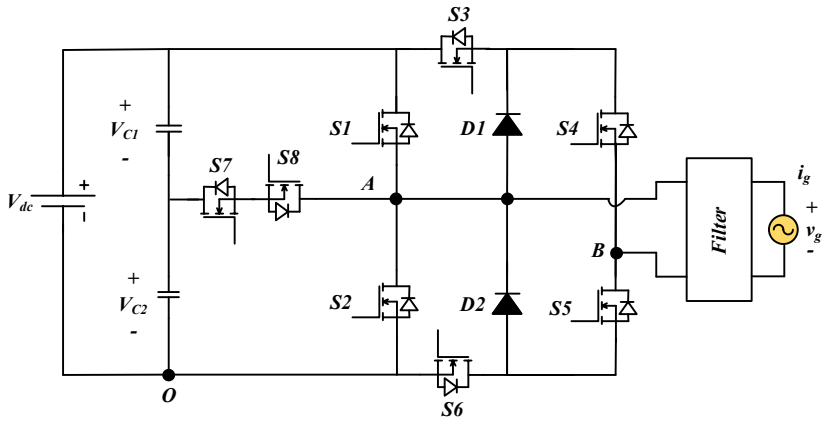


Fig. 6.4. Proposed T-Type Hybrid Five-level TLI.

6.3.2. Operating States

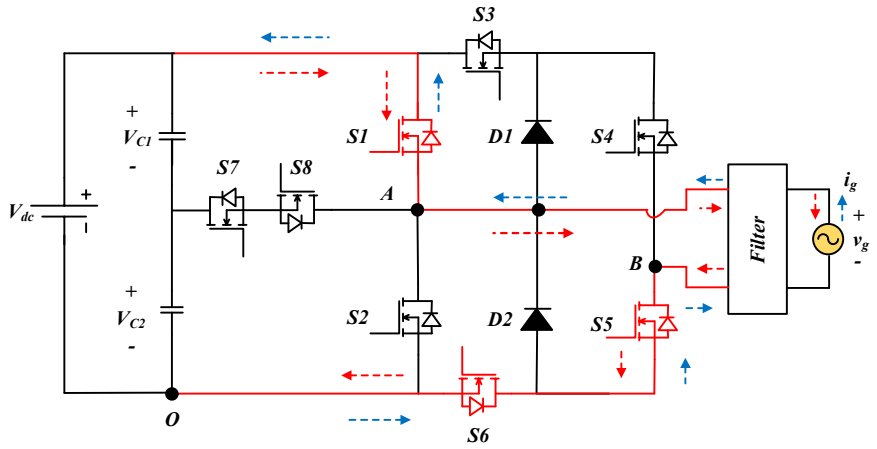
Table. 6.1 shows the operating states of the proposed inverter topology. State 1 and State 2 correspond to (V_{C1}+V_{C2}) and V_{C2}, State 3 corresponds to zero voltage level of the inverter, State 4 and State 5 correspond to -V_{C1} and -(V_{C1}+V_{C2}) respectively.

State 1: In this state, V_{AB}= (V_{C1}+V_{C2}) and the current flows either from 3LBC to grid or vice-versa as shown in Fig. 6.5(a). When the current flows from 3LBC to the grid, switches *S1*, *S5* and *S6* are in conduction. If the current flows from the grid to 3LBC, body diodes of the switches *S1*, *S5* and *S6* are in conduction. Throughout this state, DC-link capacitors are in series and they are connected in parallel to the grid.

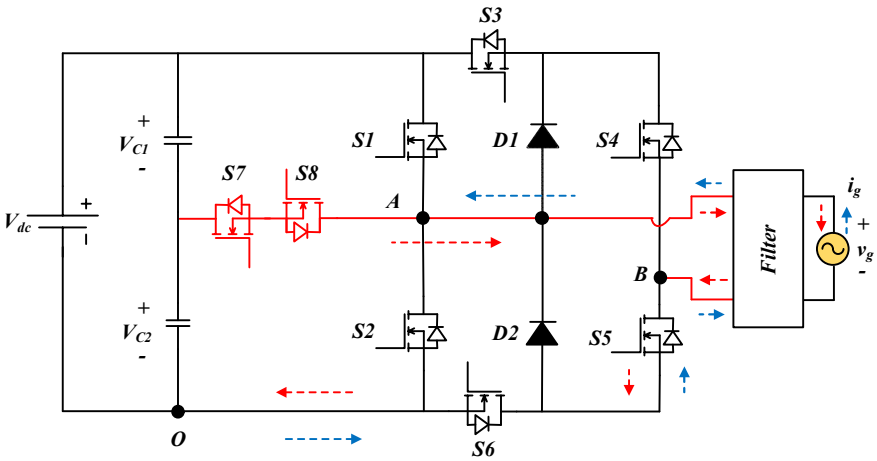
Table 6.1. Switching logic of the inverter

State	*Voltage (V_{AB})*	*S1*	*S2*	*S3*	*S4*	*S5*	*S6*	*S7*	*S8*
State 1	**(V_{C1}+V_{C2})**	1	0	0	0	1	1	1	0
State 2	**V_{C2}**	0	0	0	0	1	1	1	1
State 3	**0**	0	0	0	1	1	0	1	1
State 4	**-V_{C1}**	0	0	1	1	0	0	1	1
State 5	**-(V_{C1}+V_{C2})**	0	1	1	1	0	0	0	1

State 2: In this state, V_{AB}=V_{C2} and the current flows either from *3LBC* to grid or vice-versa, as shown in Fig. 6.5(b). When current flows from 3LBC to the grid, switches *S5*, *S6*, *S7 and* body diode of *S8* are in conduction. If the current flows from the grid to 3LBC, switch *S8* and body diodes of the switches *S5*, *S6* and *S7* are in conduction. Throughout this state DC-link capacitor *C2* is connected parallel to the grid.



(a)



(b)

Fig. 6.5. Operating states of the inverter: (a) State 1 (V_{AB}= (V_{C1} + V_{C2})), (b) State 2 (V_{AB}= V_{C2}).

State 3: In this state, V_{AB}= 0, which provides a freewheeling path in the positive as well as negative half cycles of the grid. Switches *S4*, *S5*, *S7*, *S8*, *D1 and D2* are turned-ON, as shown in Fig. 6.6. During this state, any of the two above said switches and two diodes would conduct based on the direction of the current. Moreover, throughout this state PV source is isolated from the grid and also the potentials of V_{AO} and V_{BO} are clamped to mid-point of DC-link capacitors. Therefore, the effect of switch junction capacitance and the amplitude variations in CMV are reduced [107]. The detailed explanation on CMV behaviour for the proposed system will be given in Section 6.4.

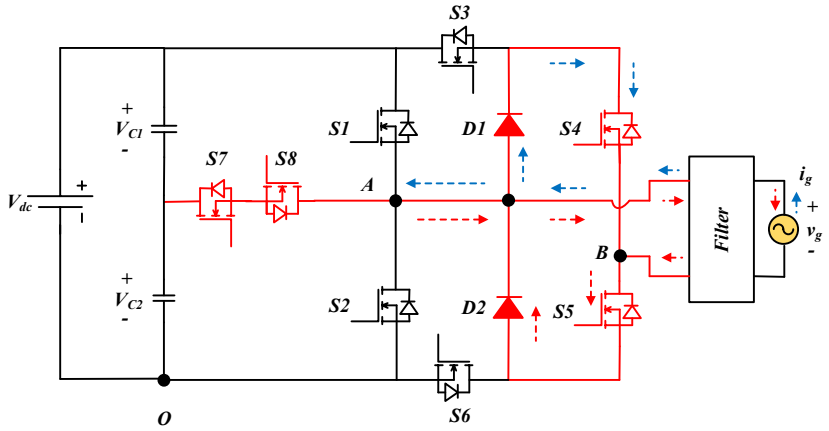


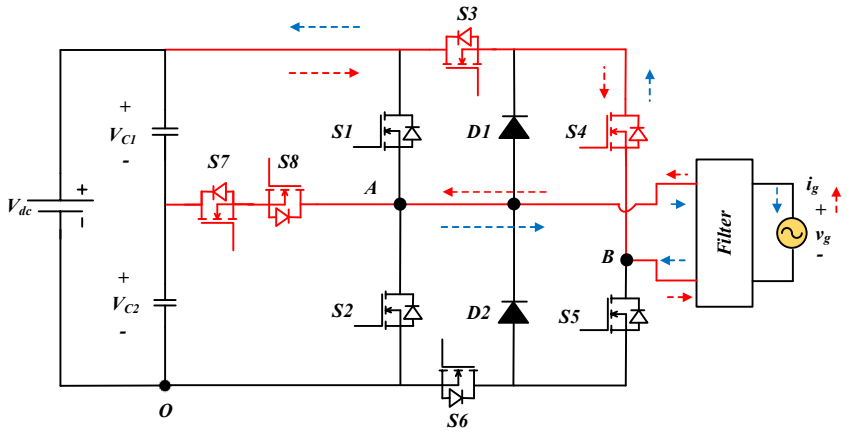
Fig. 6.6. Operation of the inverter during state 3 (V_{AB}=0).

State 4: In this state, V_{AB}= -V_{C1} and the current flows either from the grid to 3LBC or vice-versa, as shown in Fig. 6.7(a). When current flows from the grid to 3LBC, switches *S3*, *S4*, *S8* and body diode of *S7* are in conduction. If the current flows from 3LBC to grid, switch *S7* and body diodes of the switches *S3*, *S4* and *S8* are in conduction. Throughout this state, DC-link capacitor *C1* is connected parallel to the grid.

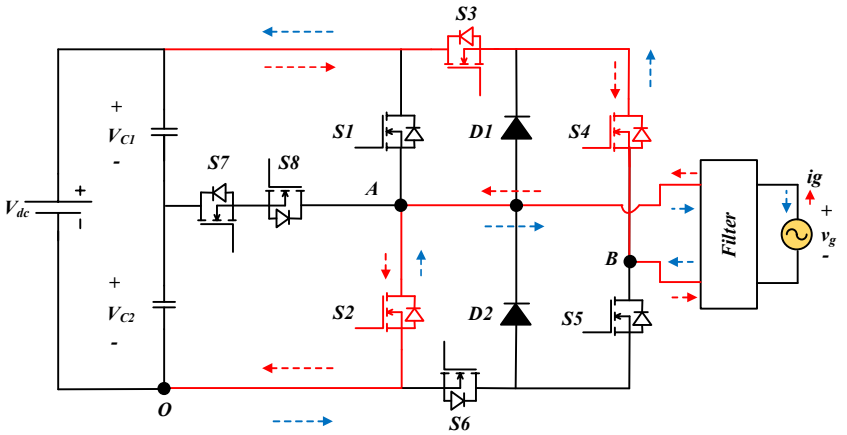
State 5: In this state, V_{AB} = -(V_{C1}+V_{C2}) and the current flows either from the grid to 3LBC or vice-versa, as shown in Fig. 6.7(b). When, the current flows from the grid to 3LBC, switches *S2*, *S3* and *S4* are in conduction. If the current flows from 3LBC to grid, body diodes of the switches *S2*, *S3 and S4* are in conduction. Throughout this state, DC-link capacitors are in series and they are connected parallel to the grid.

From all operating states of the inverter, it is observed that switches *S1* and *S2* are conducting only in the top levels of the output voltage. *S3* and *S6* are

conducting in the negative and positive cycles except for zero level, respectively. *S4* and *S5* are conducting in the negative and positive half cycles of the grid respectively. *S7* and *S8* are conducting according to the selection of voltage levels. Usually, switches *S4*, *S5* and *D1*, *D2* are enough to provide zero state, but it will float the terminal voltages of the inverter, which causes an imbalance in the CMV due to junction capacitances of the switches. Therefore, to clamp the CMV at $V_{dc}/2$ switches *S7* and *S8* are also in conduction during zero states. Moreover, this provides a path for current in any direction to realize the reactive power control capability of the inverter with similar CMV behavior. Therefore, the proposed T-type hybrid five-level inverter is capable of producing voltage levels in the output under different power factor conditions of the grid without affecting the waveform quality.



(a)



(b)

Fig. 6.7. Operating states of the inverter (a) State 4 (V_{AB}= - V_{C1}), (b) State 5 (V_{AB}= -(V_{C1}+V_{C2}).

6.3.3. Closed-loop Control

The reactive power capability of the proposed two-stage system is tested by using closed-loop control technique referred to [45] and it is depicted in Fig. 6.8. It comprises of an orthogonal signal generator (OSG) based power calculator, improved Proportional-Resonant (PR) controller [95] and LSPWM logic block for generating control pulses (*G1* to *G8*) to the inverter switches as shown in Fig. 6.9.

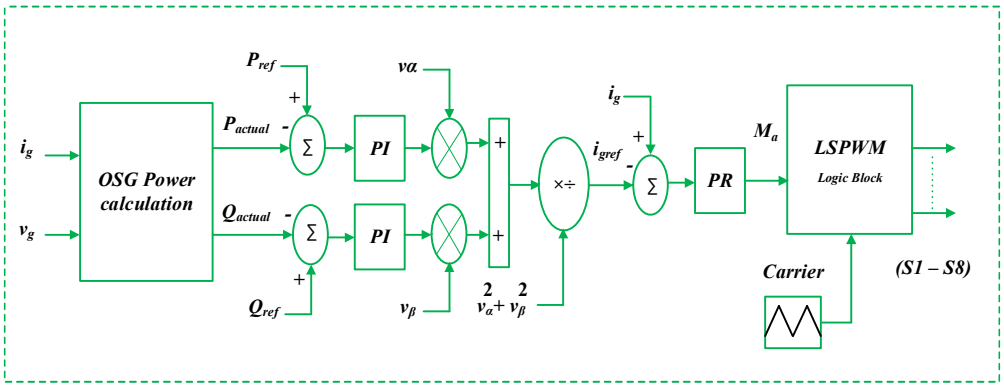


Fig. 6.8. Closed-loop control of the proposed inverter topology.

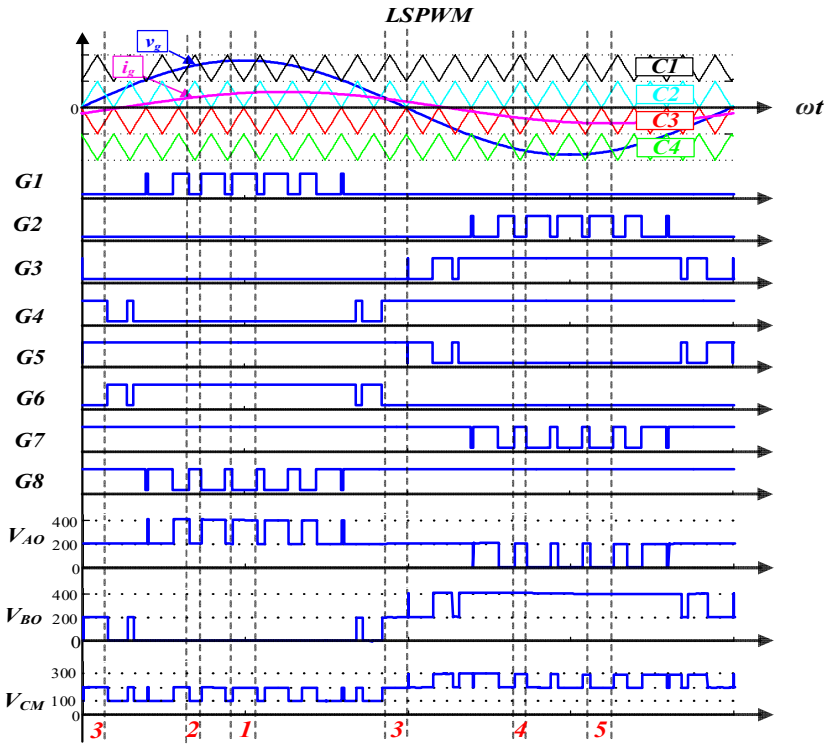


Fig. 6.9. Switching pulse generation corresponding to its operating states of the proposed inverter.

6.4. Common-mode Voltage Analysis

Leakage current flow is one of the major problems in grid-connected TLI for PV power generation systems. High-frequency oscillations present in the CMV will electrify the resonant circuit and leads to flow of leakage current ($i_{leakage}$) from the grid to PV source. To analyze the CMV behaviour, an equivalent circuit of the proposed inverter is drawn in Fig. 6.10(a). Where V_{AO} and V_{BO} are the inverter terminal voltages with respect to '*O*' as shown in Fig. 6.4. From the definitions [45], the CMV and differential-mode voltage (DMV) are expressed as follow,

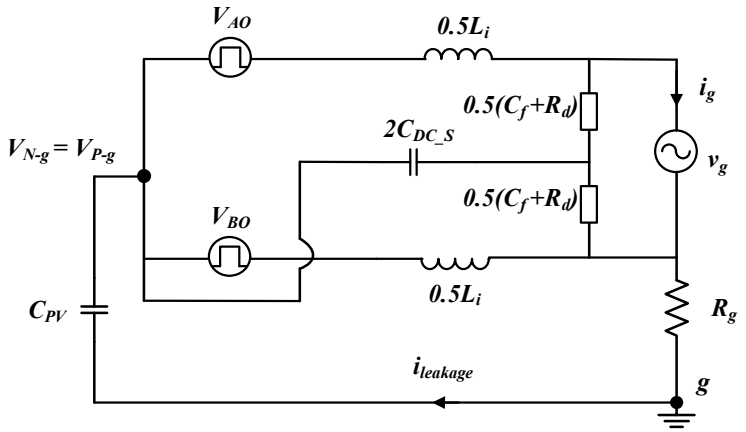
$$V_{CM} = \frac{V_{AO} + V_{BO}}{2} \tag{6.2}$$

$$V_{DM} = V_{AB} = V_{AO} - V_{BO} \tag{6.3}$$

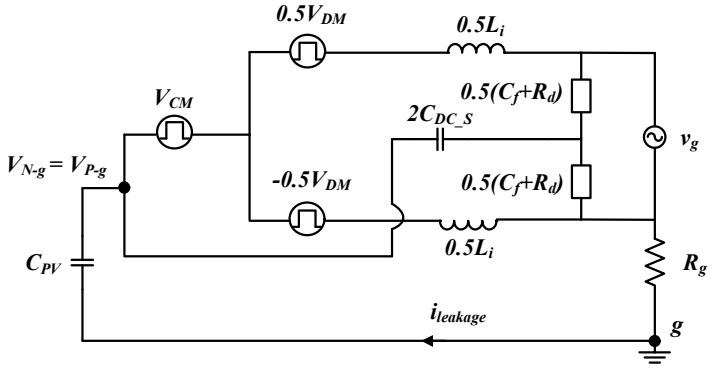
$$V_{CM-DM} = V_{DM} \cdot \frac{L2 - L1}{2(L2 + L1)} \tag{6.4}$$

$$V_{TCMV} = V_{CM} + V_{CM-DM} \tag{6.5}$$

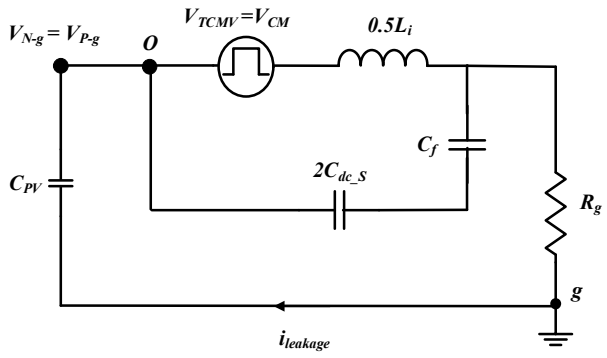
Where V_{CM} and V_{DM} are the CMV and DMV respectively. Usually, the variations in the CMV depends on the structure and control scheme employed for the switching of the inverter. Moreover, depending on the placement of filter inductors, an additional CMV ($V_{CM\text{-}DM}$) exists and it is given in Eq. (6.4). Thus, total common-mode voltage (V_{TCMV}) consists of both V_{CM} and $V_{CM\text{-}DM}$ as expressed in Eq. (6.5). If the filter inductor is placed asymmetrically such as $L1=L_f$ and $L2= 0$, $V_{CM\text{-}DM} = -0.5V_{DM}$ and $V_{TCMV}= V_{BO}$. In opposite to that, if $L1=L2=0.5L_f$ (for well-designed inductors with symmetrically structured magnetic), $V_{CM\text{-}DM} = 0$ and $V_{TCMV} = V_{CM}$. Equivalent circuit of the inverter in terms of CMV and DMV as depicted in Fig. 6.10(b). According to operating states of the proposed inverter and on-off positions of the switches presented in Section 6.3.2, the variations in V_{TCMV} (=V_{CM}) can be evaluated in each state of operation as follows:



(a)



(b)



(c)

Fig. 6.10. (a). Common-mode equivalent circuit of the proposed TLI, (b) Equivalent circuit in terms of CMV and DMV and (c) Simplified circuit.

$$\text{State 1: } V_{TCMV} = \frac{1}{2}\left(V_{AO} + V_{BO}\right) = \frac{1}{2}\left(V_{dc} + 0\right) = \frac{1}{2}V_{dc} \tag{6.6}$$

$$\text{State 2: } V_{TCMV} = \frac{1}{2}\left(V_{AO} + V_{BO}\right) = \frac{1}{2}\left(\frac{V_{dc}}{2} + 0\right) = \frac{1}{4}V_{dc} \tag{6.7}$$

$$\text{State 3: } V_{TCMV} = \frac{1}{2}\left(V_{AO} + V_{BO}\right) = \frac{1}{2}\left(\frac{V_{dc}}{2} + \frac{V_{dc}}{2}\right) = \frac{1}{2}V_{dc} \tag{6.8}$$

$$\text{State 4: } V_{TCMV} = \frac{1}{2}\left(V_{AO} + V_{BO}\right) = \frac{1}{2}\left(\frac{V_{dc}}{2} + V_{dc}\right) = \frac{3}{4}V_{dc} \tag{6.9}$$

$$\text{State 5: } V_{TCMV} = \frac{1}{2}\left(V_{AO} + V_{BO}\right) = \frac{1}{2}\left(0 + V_{dc}\right) = \frac{1}{2}V_{dc} \tag{6.10}$$

From Eqs. (6.6)-(6.10), it is noted that the variations in V_{TCMV} for the proposed topology are restricted to *(1/4)*V_{dc}* to *(3/4)*V_{dc},* due to clamping of inverter terminal voltages to half of the DC-link voltage during zero state. Moreover, the difference in amplitude of V_{TCMV} is only *(1/4)*V_{dc}* while transferring from one state to another state vice-versa, as shown in Fig. 6.9. But the high-frequency variations in V_{TCMV} will directly affect the voltage across C_{PV} (i.e., $V_{N\text{-}g}$) and also results in higher leakage current as shown in Eq. (6.11). To reduce the effect of V_{TCMV} on $V_{N\text{-}g}$, in the proposed topology, a common-mode conducting path is provided for the inverter from split filter capacitors to the negative terminal of DC source as shown in Fig. 6.1. The low-frequency components such as grid voltage (50 Hz), ripple voltage (100 Hz) and DMV do not affect leakage current. Hence, they are neglected in the simplified circuit of the proposed TLI, as shown in Fig. 6.10(c) [9]. A small value of damping resistor (R_d) is also ignored for easy analysis.

$$i_{leakage} = C_{PV}\frac{dV_{N-g}}{dt} \tag{6.11}$$

$$V_{N-g} = \frac{-V_{TCMV}(\omega)}{1-\omega^2(0.5L_i)\left(2C_{dc\_S} \,//\, C_f\right)}$$

$$V_{N-g} = \frac{-V_{TCMV}(\omega)}{1-\frac{\omega^2}{\omega_r^2}} \tag{6.12}$$

$$A(\omega) = 20\,log\left(\left|1-\frac{\omega^2}{\omega_r^2}\right|\right) \tag{6.13}$$

From the simplified circuit as shown in Fig. 6.10(c), the total voltage variations in $V_{N\text{-}g}$ is determined by Eq. (6.12). Where 'ω' and 'ω_r' are the switching and resonant frequencies in rad/sec respectively. The attenuation factor $A(\omega)$ is applied to the V_{TCMV} is shown in Eq. (6.13). Smaller ω_r leads to higher attenuation on V_{TCMV}. Thus, the major contributor for voltage variations in $V_{N\text{-}g}$ is attenuated with a factor $A(\omega)$. Also, the LC circuit formed by the common-mode conducting path of the inverter results in the trapezoidal waveform of $V_{N\text{-}g}$ with the fundamental frequency. Hence, the magnitude of leakage current is limited below the grid standards for the proposed topology. Further, the proposed solution does not affect the active and reactive power injection into the grid due to the symmetrical placement of the filter inductors.

6.5. Simulation Results

MATLAB/Simulink results are presented to validate the performance of the proposed two-stage system integrated with closed-loop control under dynamic changes in both active and reactive powers. Various system parameters used for the proposed configuration in both simulation and experimentation are given in the Table 6.2. The PV panel is modeled with a 200 V DC source and the capacitance of 60 nF is connected between the terminals of DC source to the ground for emulating the PV parasitic capacitance.

Table 6.2. System Parameters

S. No	Parameters	Value
1	Power rating	500 W
2	Input voltage	200 V
3	AC output voltage	230V, 50 Hz
4	Switching frequency f_s	10 kHz
5	Inductor L, L_i, L_{ac}	3 mH, 6 mH, 1.2 mH
6	Capacitors $C1$, $C2$, C_f, C_{PV}	1 mF, 1mF, 2 μF, 60 nF
7	R_d and R_g	5Ω and 10 Ω
8	MOSFET	IRFP460N
9	Diode	RURP1560

In Fig. 6.11, active power (P) is changing by maintaining reactive power (Q) as constant and in Fig. 6.12 it is vice-versa. Subplots of Figs. 6.11 and 6.12 consists of reference and actual active, reactive powers, DC-link voltage and individual capacitor voltages, V_{AB}, v_g and i_g and also common-mode voltage (V_{CM}) of the inverter repectively. Grid current (i_g) is scaled by a factor of 70 for better visibility during reference power changes. From Figs. 6.11 and 6.12, it is observed that active and reactive powers are effectively tracked the reference powers by maintaining constant and balanced DC-link voltage. Moreover, the bi-directional current path provided by the LSPWM scheme enables the inverter to operate in a reactive power region without having any spikes in grid voltage and current.

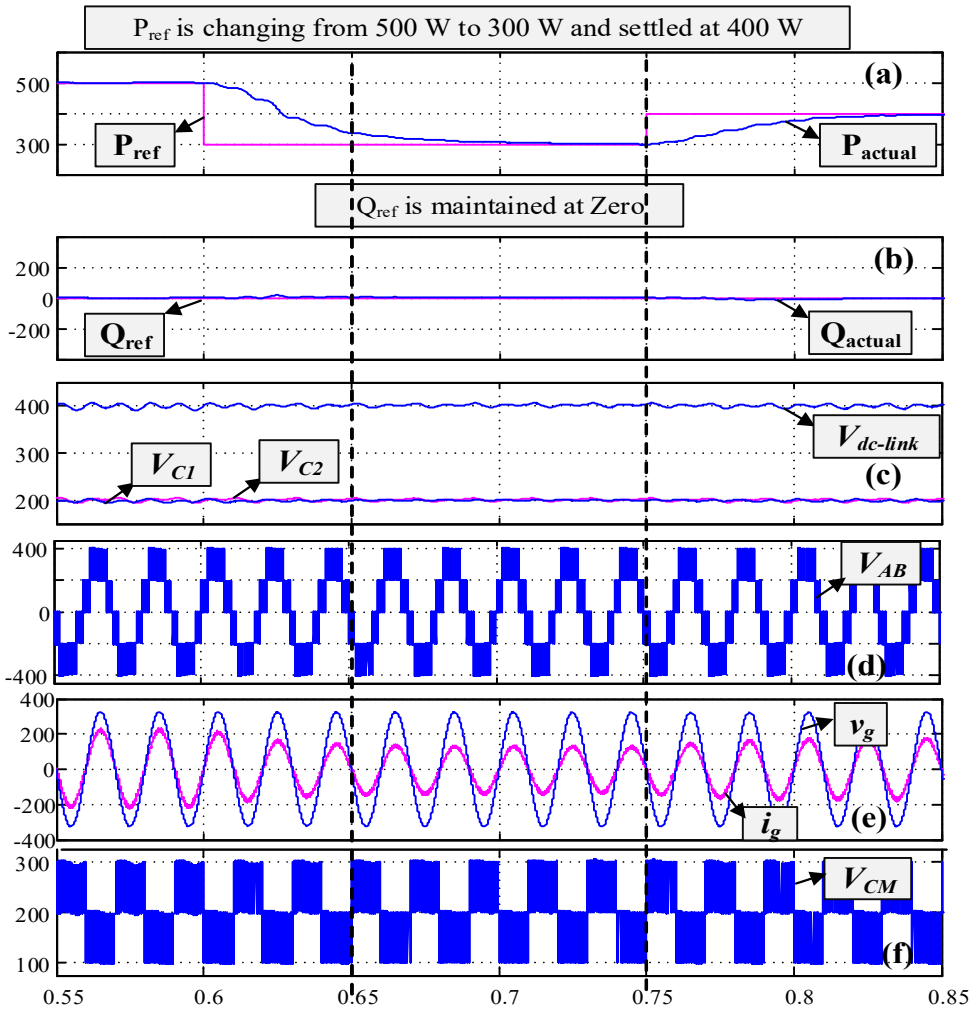


Fig. 6.11. Simulation results of the proposed two-stage system when P_{ref} is changing from 500 W to 300 W and setteled at 400 W, (a) sudden changes in P_{ref}, (b) constant Q_{ref}, (c) total DC-link voltage and capacitor voltages *C1* and *C2*, (d)V_{AB}, (e) v_g and 70*i_g, (f) V_{CM}.

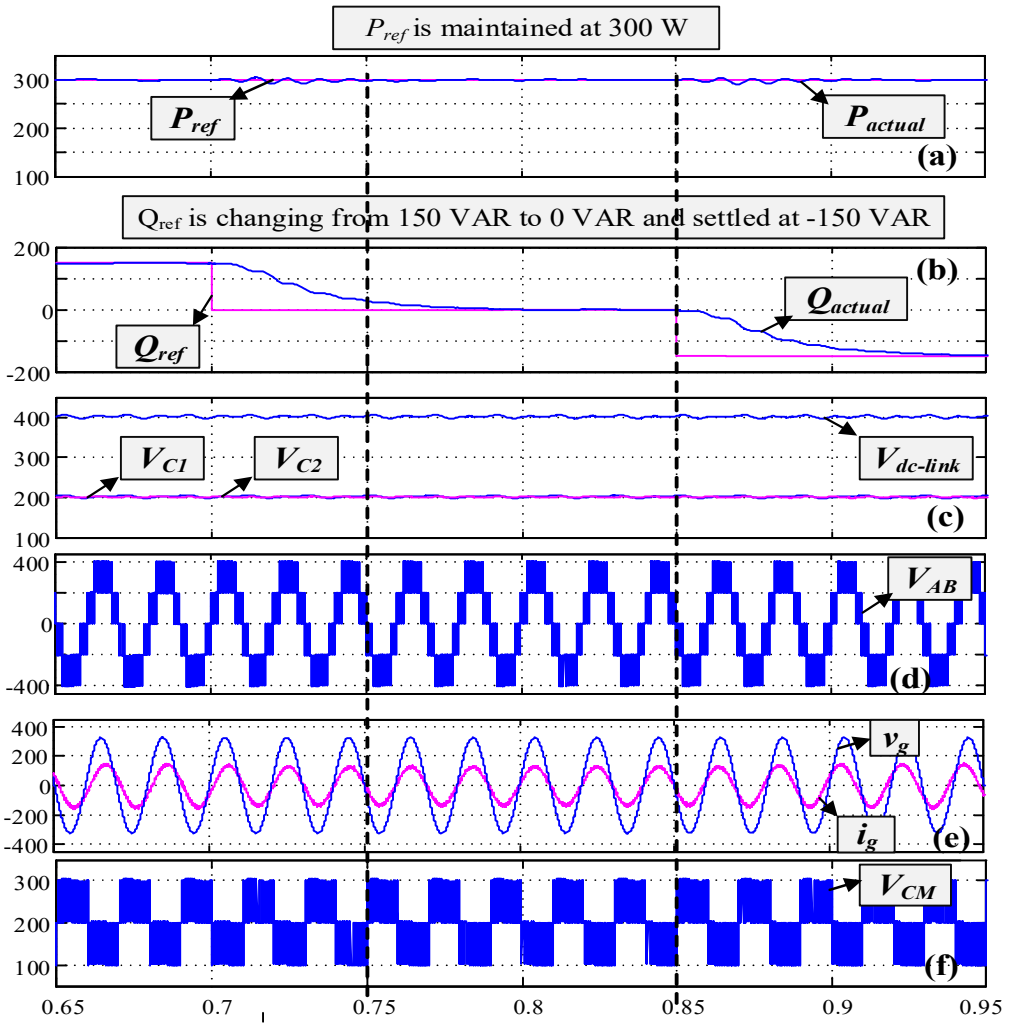


Fig. 6.12. Simulation results of the proposed two-stage system when Q_{ref} is changing from 150 VAR to 0 VAR and setteled at -150 VAR, (a) constant P_{ref}, (b) sudden changes in Q_{ref}, (c) total DC-link voltage and capacitor voltages *C1* and *C2*, (d)V_{AB}, (e) v_g and 70*i_g, (f) V_{CM}.

Further, the common-mode characteristic curves of the proposed topology are depicted in Fig. 6.13. Subplots of Fig. 6.13 consists of V_{AO}, V_{BO}, V_{CM}, $V_{N\text{-}g}$ *and* $i_{leakage}$ respectively. Due to clamping of the inverter terminal voltages during the freewheeling period, the difference in amplitude variations of V_{TCMV} is restricted to (1/4)*V_{dc} while transferring from one state to another state vice-versa. Moreover, to attenuate such high frequency and low amplitude variations in V_{TCMV}, a common-mode conducting path is provided for the inverter. Therefore, the total high-frequency variations and sudden transitions are absent in $V_{N\text{-}g}$, which results in the reduction of leakage current as shown in subplot of Fig. 6.13. The rms value of the leakage current 16.6 mA is measured from the simulations of proposed symmetrical TLI for the specifications given in Table 6.2 and also it is well below the grid standards.

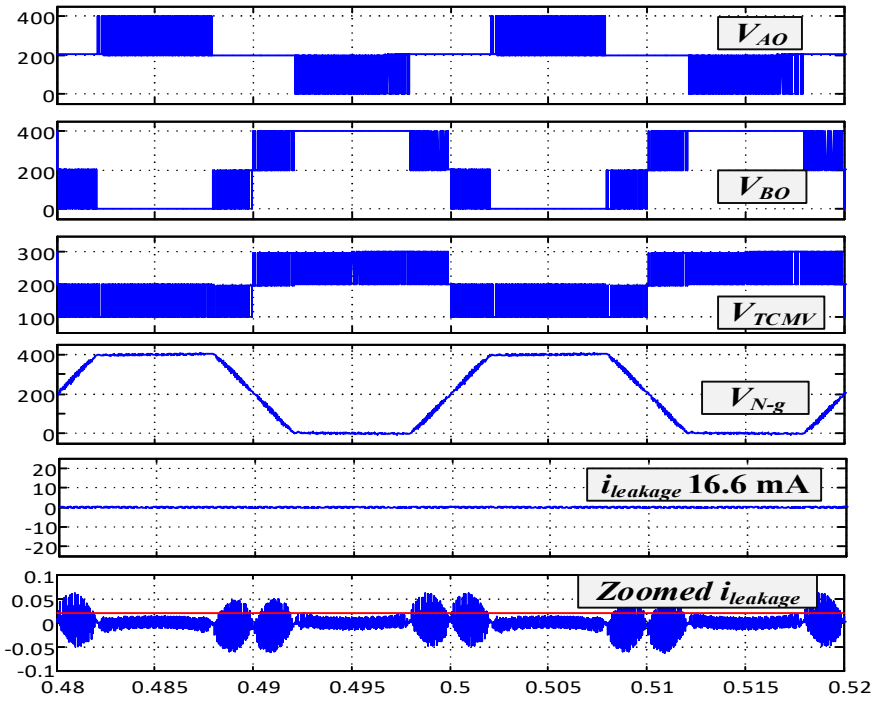


Fig. 6.13 Common-mode characteristics of the proposed TLI topology.

6.6. Experimental Results

To validate the simulation studies of the proposed two-stage system, a 500 W experimental test setup is built based on the available lab facility and it is shown in Fig. 6.14. Various passive components employed for the development of proto-type are designed based on the analysis given in chapter 3. The parameters and components used for the experimental setup are given in Table 6.2. To show the leakage current flow with C_{PV} due to oscillations in CMV, an equivalent capacitor is modelled and connected across the DC terminal and ground.

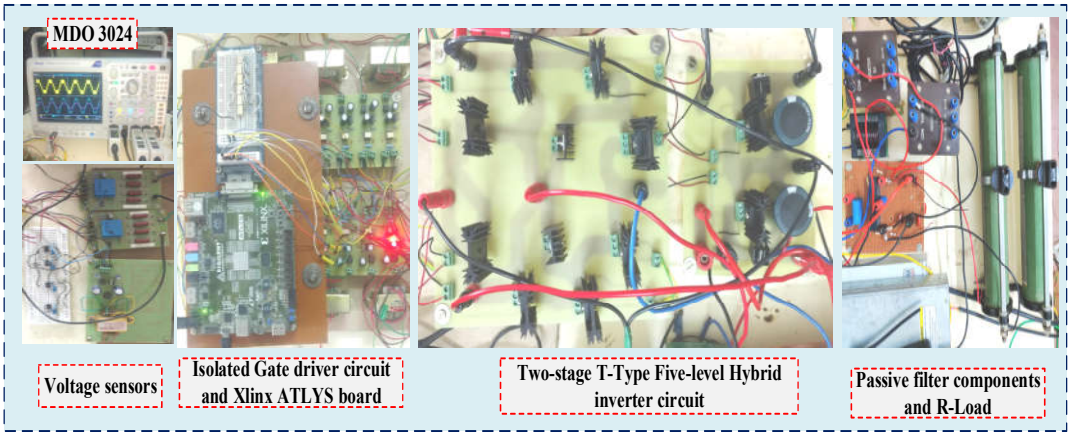


Fig. 6.14. Experimental prototype.

Fig. 6.15(a) shows the balanced voltages across the DC-link capacitors obtained from the simple control (as shown in Fig. 6.2) implemented using ATLYS Spartan-6 FPGA board [65]. Figs. 6.15(b), (c) and (d) shows the output waveforms of the inverter under unity, 0.9 lagging (200 Ω, 300 mH) and 0.9 leading (135 Ω, 50μF) power factor conditions respectively, which confirms the effectiveness of the proposed modulation scheme and topology for controlling the reactive power without affecting the waveform quality and multilevel operation. Moreover, %THD of the load current represented in Fig. 6.16(a), (b) and (c) are measured using CSV (comma separated values) data obtained from MDO 3024 and which is less than IEC61000-3-2 standard.

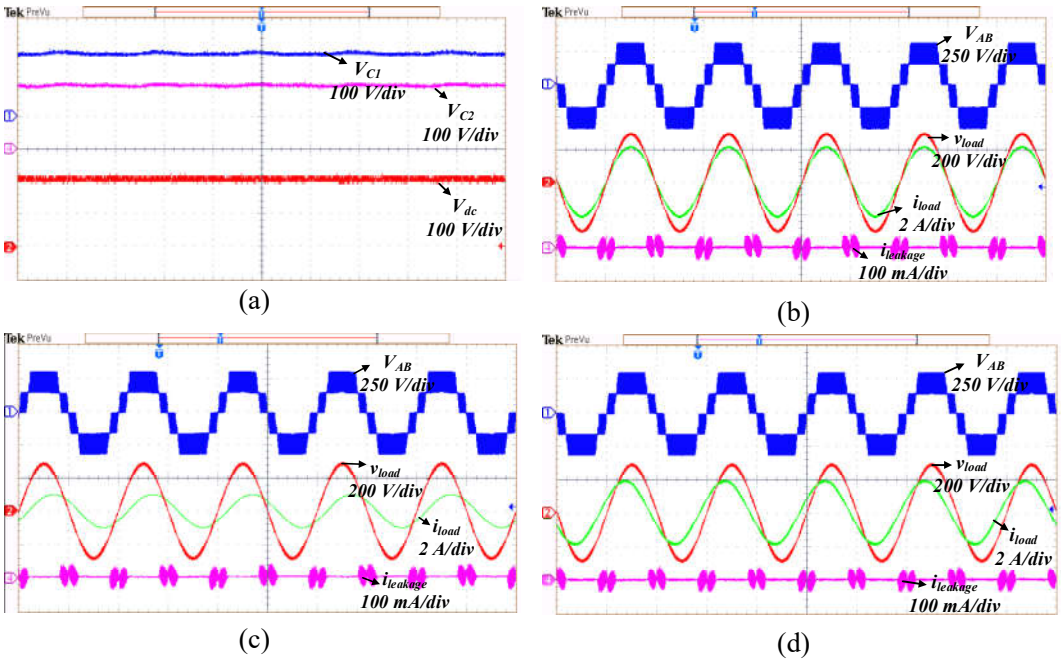
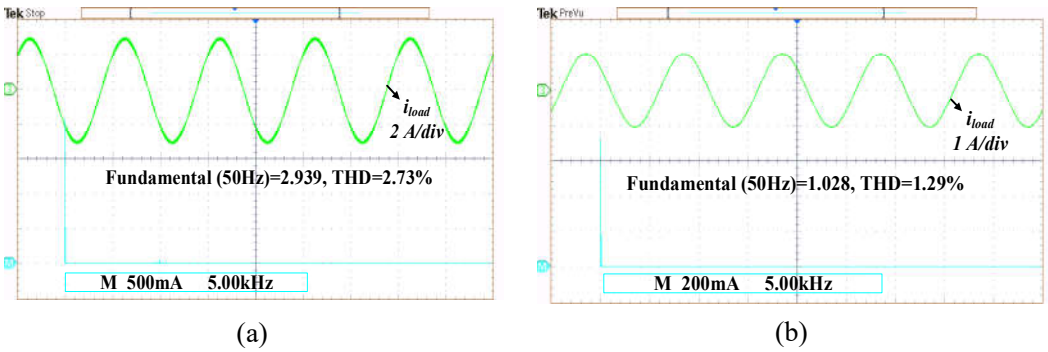
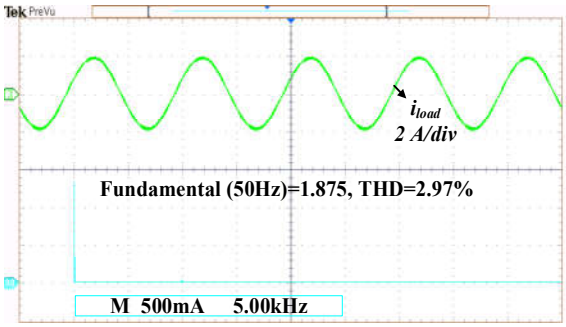


Fig. 6.15. (a) Input voltage, DC voltages waveforms of 3LBC, Five-level voltage (V_{AB}), load voltage (V_{load}), load current (i_{load}) and leakage current ($i_{leakage}$) under (b) Unity power factor, (c) Lagging power factor, (d) Leading power factor.

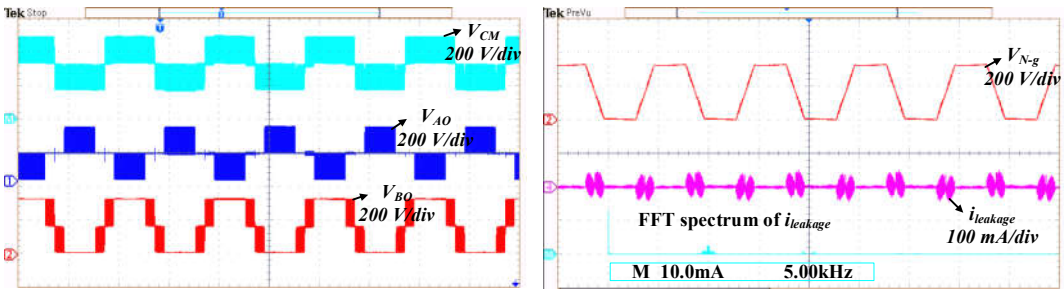




(c)

Fig. 6.16. FFT spectrums of load current under (a) Unity power factor, (b) Lagging power factor, (c) Leading power factor.

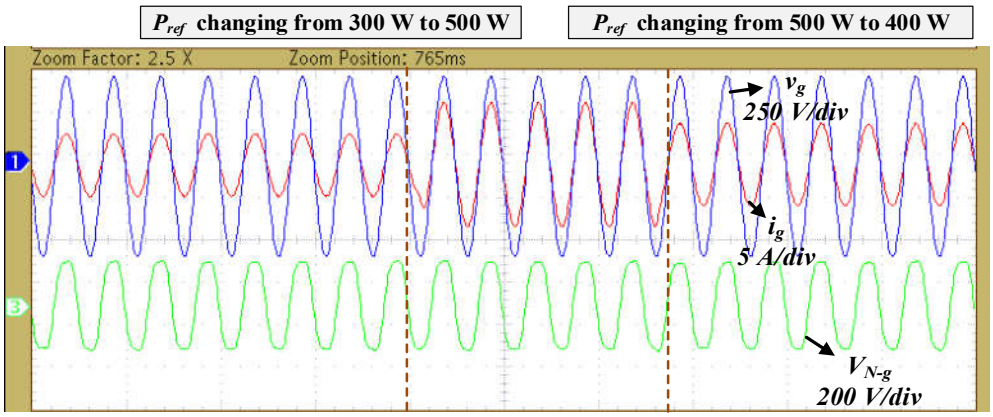
Fig. 6.17 shows the *CMV* behavior of the proposed configuration. The terminal voltage V_{AO}, V_{BO} and V_{CM} waveforms are given in Fig. 6.17(a). By observing the PV terminal voltage V_{N_g} in Fig. 6.17(b), it is confirmed that the common-mode path introduced by the *LCL* filter effectively limits the high-frequency variations and sudden transitions in the voltage across C_{PV}. The measured value of the RMS leakage current is 17.42 mA, which is very close to the simulation value and also well below than 200 mA as per German DINVDE0126-1-1 standard. Moreover, the leakage current reduction is guaranteed irrespective of the operating power factor because of the similar CMV characteristics at all three power factor conditions.



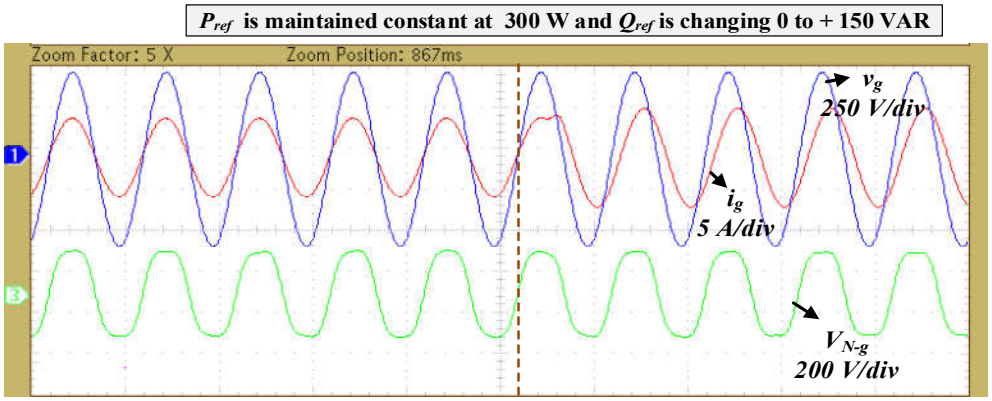
(a) (b)

Fig. 6.17. (a) Inverter terminal voltages V_{AO}, V_{BO}, V_{CM}, (b) PV negative terminal to ground voltage (V_{N_g}) and leakage current ($i_{leakage}$).

Further, the dynamic performance of the proposed two-stage system under different power factor conditions of the grid is verified using real-time validation with OPAL-RT OP4500 modules, as explained in Chapter 3. Fig. 6.18(a) shows the step-change in reference power from 300 W to 500 W and then settled at 400 W. Figs. 6.18(b) and (c) show the step-change reactive power from 0 to ±150 VAR respectively for grid-connected operation.



(a)



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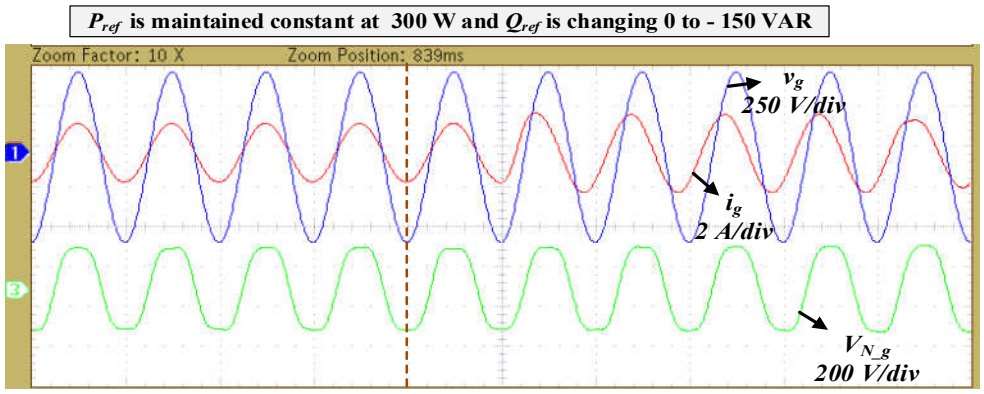


(c)

Fig. 6.18. (a) Dynamic performance of the proposed two-stage system (a) Step change in real power, Step change in reactive power (b) Lagging (c) Leading.

It can be noticed that the inverter is capable of providing reactive power support at all power factors without degrading the quality of output waveforms. Further, the efficiency versus output power curve of the proposed two-stage system is evaluated using steady-state formulas referred to chapter 4. The maximum efficiency of 97.24% is attained for the proposed two-stage system as shown in Fig. 6.19.

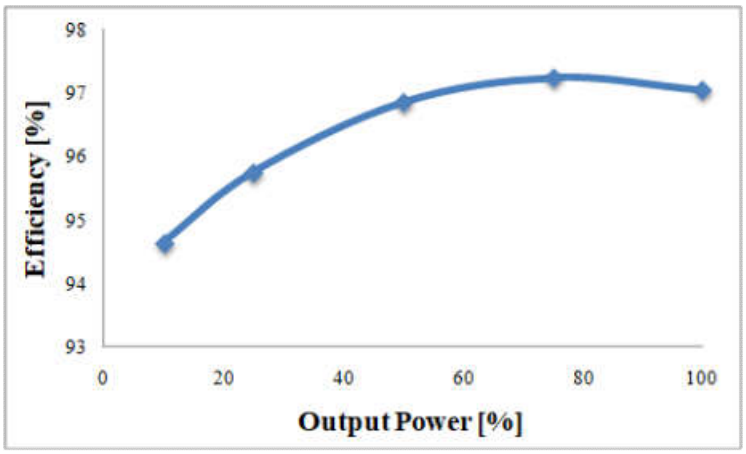


Fig. 6.19. Efficiency curve.

6.7. Comparison of the Proposed TLI with other Five-Level TLI Topologies

In this section, a comparison of the proposed topology with other recently reported five-level TLI topologies is presented. Simulations are performed using PSIM thermal module real-time devices (MOSFET-FCA76N60N and Diode-MUR1560) for obtaining the common-mode characteristics, Fast Fourier transform (FFT) of leakage current and loss distribution among various devices. Fig. 6.20 illustrates the comparison of PV terminal voltage ($V_{N\text{-}g}$) and leakage current for different topologies reported in Refs [56]-[59] with the proposed topology respectively. All the topologies are simulated under the same test conditions as given in Table 6.2. Generally, the variations in $V_{N\text{-}g}$ depends on the topology structure and the modulation scheme employed for the switching of an inverter.

From Eq. (6.11), it is evident that the magnitude of leakage current is directly proportional to the total variations in $V_{N\text{-}g}$ and size of the C_{PV}. Fig. 6.20(a) shows the waveforms of $V_{N\text{-}g}$ and $i_{leakage}$ for topologies presented in [56]-[59], it is observed that $V_{N\text{-}g}$ is varying suddenly from V_{dc} to 0 while transferring from positive half-cycle to negative half-cycle. Fig. 6.20(b) shows the waveforms of $V_{N\text{-}g}$ and $i_{leakage}$ for the topologies presented in [60]-[61], where $V_{N\text{-}g}$ has sudden variations while transferring from $\pm 0.5V_{dc}$ level to $\pm V_{dc}$ level and vice-versa. These sudden variations of $V_{N\text{-}g}$ results in more spikes in the leakage current. Fig. 6.20(c) depicts the waveforms of $V_{N\text{-}g}$ and $i_{leakage}$ for the topology presented in ref

[62], where the redundant states formed by the derived CHB inverter eliminates both high frequency and sudden transitions in $V_{N\text{-}g}$. Similarly, $V_{N\text{-}g}$ and $i_{leakage}$ of the proposed inverter topology are depicted in Fig. 6.20(d), where clamping of the inverter terminal voltages to half of the DC-link voltage and common-mode conducting path of the inverter eliminates both high frequency and sudden transitions in $V_{N\text{-}g}$.

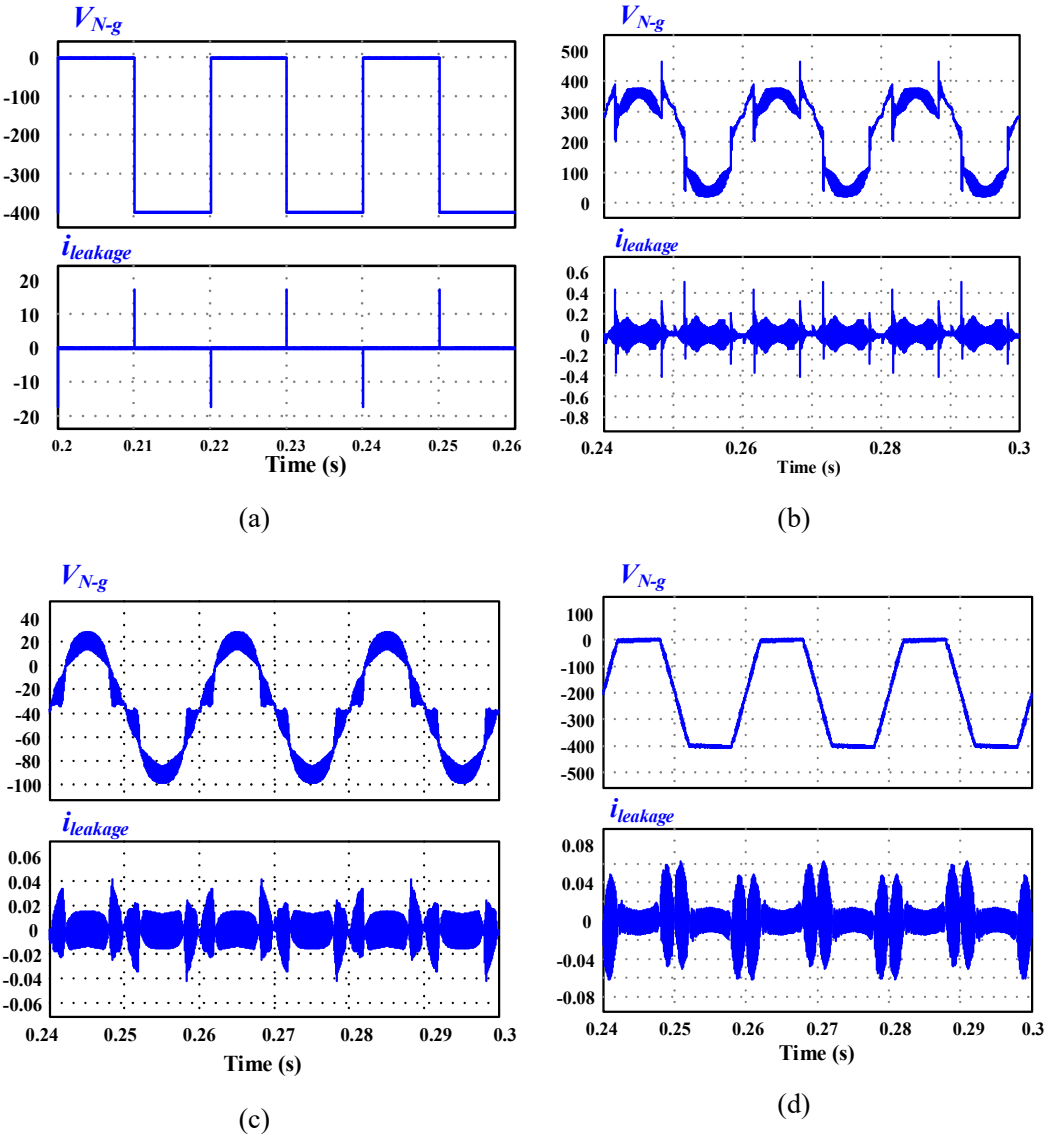


Fig. 6.20 Voltage across C_{PV} and leakage current of the, (a) Topologies [56]-[59], (b) Topologies [60]-[61], (c) Topology [62] and (d) Proposed topology.

Moreover, the measured RMS values of the leakage current for the topologies reported in [56]-[59] is 180 mA, topologies reported in [60]-[61] is 57 mA, topology published in [62] is 13 mA and for the proposed topology is 16 mA respectively. Thus, the size of the additional common-mode filter is significantly

reduced for the proposed topology and derived CHB topology in comparison with the others. Usually, the low impedance path offered by C_{PV} at resonant frequency causes higher leakage current and the same is noticed in FFT spectrum as illustrated in Fig. 6.21.

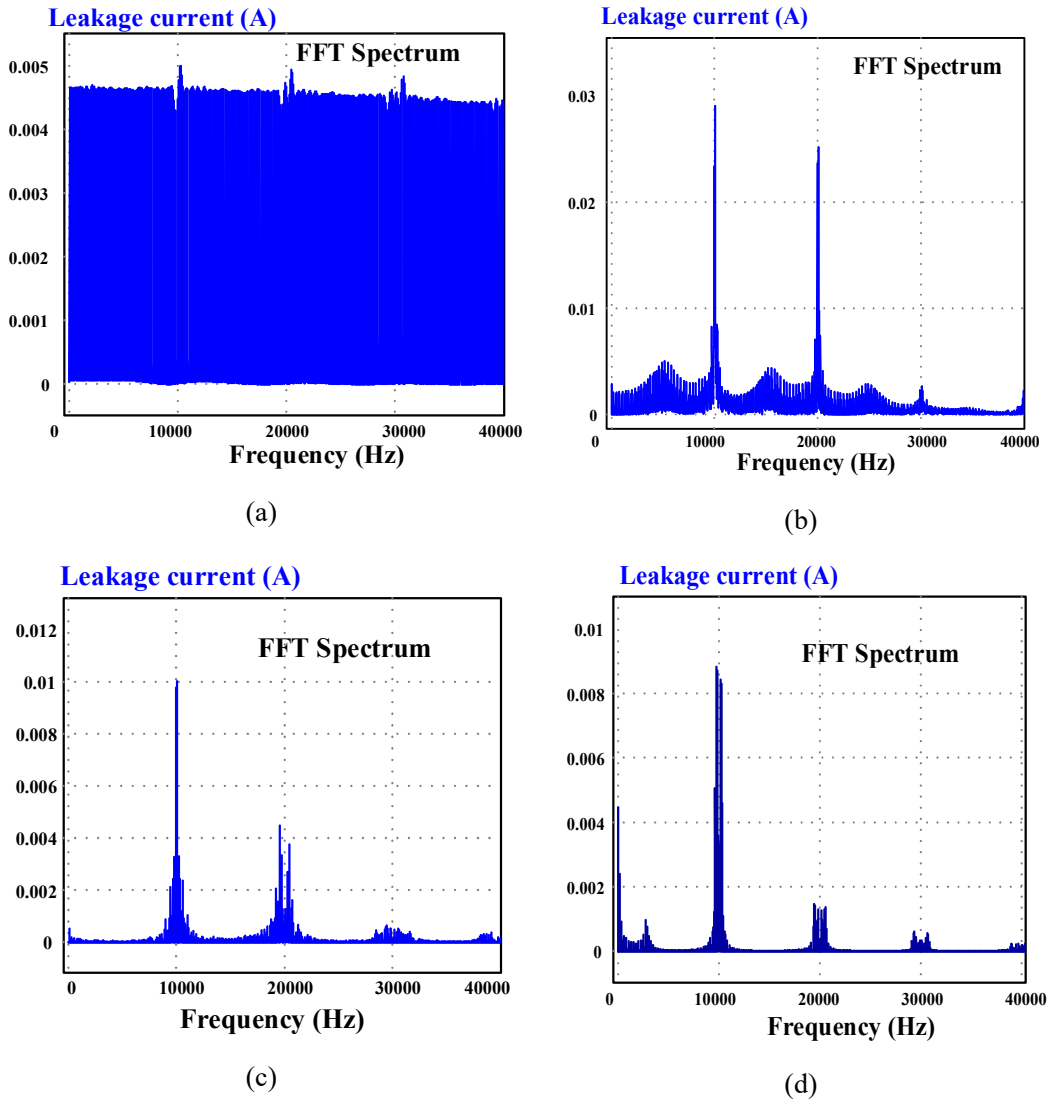
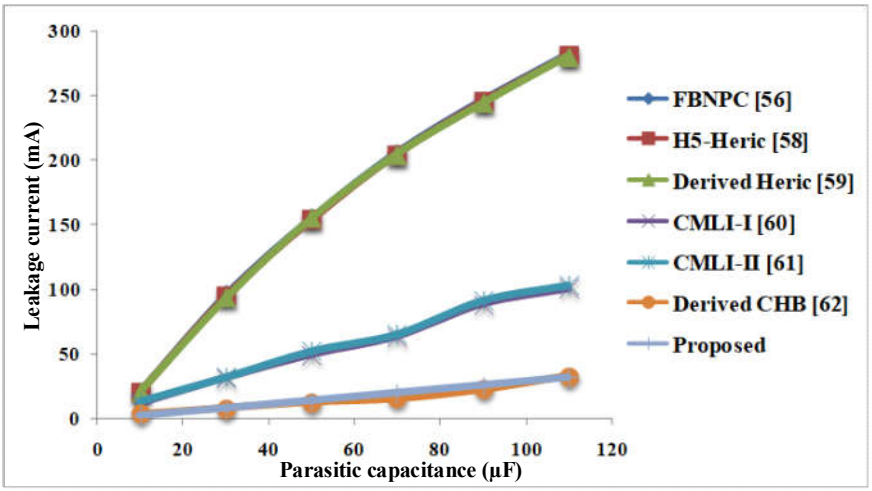
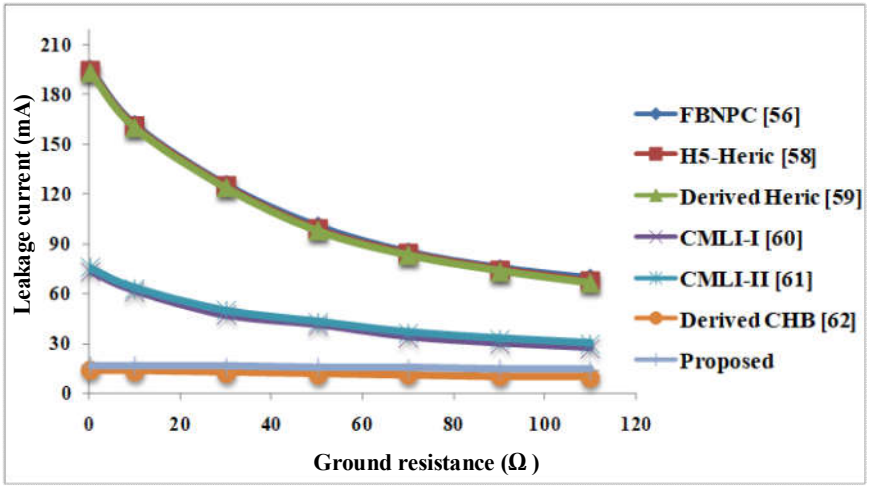


Fig. 6.21. FFT spectrum of the, (a) Topologies [56]-[59], (b) Topologies [60]-[61], (c) Topology [62] and (d) Proposed topology.

Further, to realize the practical limitation of leakage current under various environmental conditions, the topologies were simulated at different parasitic capacitances and grounding resistances as shown in Figs. 6.22(a) and (b) respectively. From the above discussion and simulation Figs. 6.20 to 6.22, it is concluded that the derived CHB and the proposed inverter topology offers very less leakage current in comparison with other five-level topologies proposed in [56]-[61].



(a)



(b)

Fig. 6.22. (a) Parasitic capacitances versus leakage current curve,
(b) Ground resistance versus leakage current.

Further, detailed comparisons of the proposed topology with other five-level topologies are given in Table 6.3, Table 6.4 and Table. 6.5 in terms of device count, leakage current magnitude, reactive power capability, etc. It is noticed that the total number of PV sources required for the proposed topology is less than the CMLI-I [60], CMLI-II [61] and derived CHB topologies. Also, the total number of components is less in comparison with the FBNPC [56], H5-Heric [58] and derived CHB [62] topologies. Moreover, the proposed inverter structure and its modulation scheme effectively minimizes the leakage current and also supports the reactive power control. From Table 6.4, it is observed that the proposed topology requires fewer conducting devices in comparison with the FB-NPC and derived CHB. Thus, the proposed T-type hybrid five-level TLI is expected to show lower losses and high efficiency.

Table 6.3. Comparison of various multilevel topologies with proposed configuration

Topology	FBNPC [56]	H5-Heric [58]	Derived Heric [59]	CMLI-1 [60]	CMLI-II [61]	Derived CHB [62]	Proposed
No.of PV Sources	1	1	1	2	2	2	1
MOSFETs	8	8	8	8	7	10	8
Diodes	4	4	2	0	0	0	2
Filter inductor placement	Asymmetrical	Asymmetrical	Asymmetrical	Symmetrical	Symmetrical	Symmetrical	Symmetrical
Voltage across C_{PV}	Square	Square	Square	Close to sine	Close to sine	Sine	Trapezoidal
Leakage current (RMS)	181.4 mA	181 mA	180.3 mA	56.5 mA	57.1 mA	13.7 mA	16.7 mA
Size of the CMF	Large	Large	Large	Medium	Medium	Small	Small
Reactive power capability	Yes	No	No	No	No	No	Yes
Freewheeling states during negative power transfer	Realized	Not Realized	Not Realized	Not Realized	Not Realized	Not Realized	Realized

Table 6.4. Comparison of conducting devices and blocking voltages for various MLI topologies with proposed configuration

Topology			FBNPC [56]	H5-Heric [58]	Derived Heric [59]	CMLI-1 [60]	CMLI-II [61]	Derived CHB [62]	Proposed
No.of MOSFETs conducting	PP	V_{dc}	4	2	2	3	3	4	3
		$0.5*V_{dc}$	4	2	2	2	3	3	3
	FP	*0*	4	1	1	1	1	1	1
	NP	$-0.5*V_{dc}$	4	3	2	2	3	3	3
		$-V_{dc}$	4	3	2	3	3	4	3
No.of diodes conducting	PP	V_{dc}	0	0	0	0	0	0	0
		$0.5*V_{dc}$	1	1	1	1	1	1	1
	FP	*0*	0	1	1	1	1	1	1
	NP	$-0.5*V_{dc}$	1	1	1	1	1	1	1
		$-V_{dc}$	0	0	0	0	0	0	0
Total devices conducting in one cycle			22	14	12	14	16	18	16
Total blocking voltage	MOSFET		$4*V_{dc}$	$7*V_{dc}$	$7*V_{dc}$	$7*V_{dc}$	$6*V_{dc}$	$6*V_{dc}$	$6*V_{dc}$
	Diode		$2*V_{dc}$	$3*V_{dc}$	V_{dc}	0	0	0	$2*V_{dc}$

*PP=Positive period, **FP=Freewheeling period, ***NP=Negative period.

Evaluation of the switching and conduction losses of each power device is carried out by using the PSIM thermal module under the same operating conditions as given in Table. 6.2. Also, the loss distribution of various power switches and diodes for different topologies are illustrated in Fig. 6.23. It can be visualized that total losses for the proposed topology is lower than FB-NPC and derived CHB and higher than H5-Heric, derived Heric, CMLI-1 and CMLI-II. However, it offers minimum leakage current, reactive power capability and reduced number of PV sources in comparison with the other inverter topologies. Therefore, the proposed inverter topology is an optimal trade-off in comparison with other topologies and also a reliable candidate for future PV power generation systems.

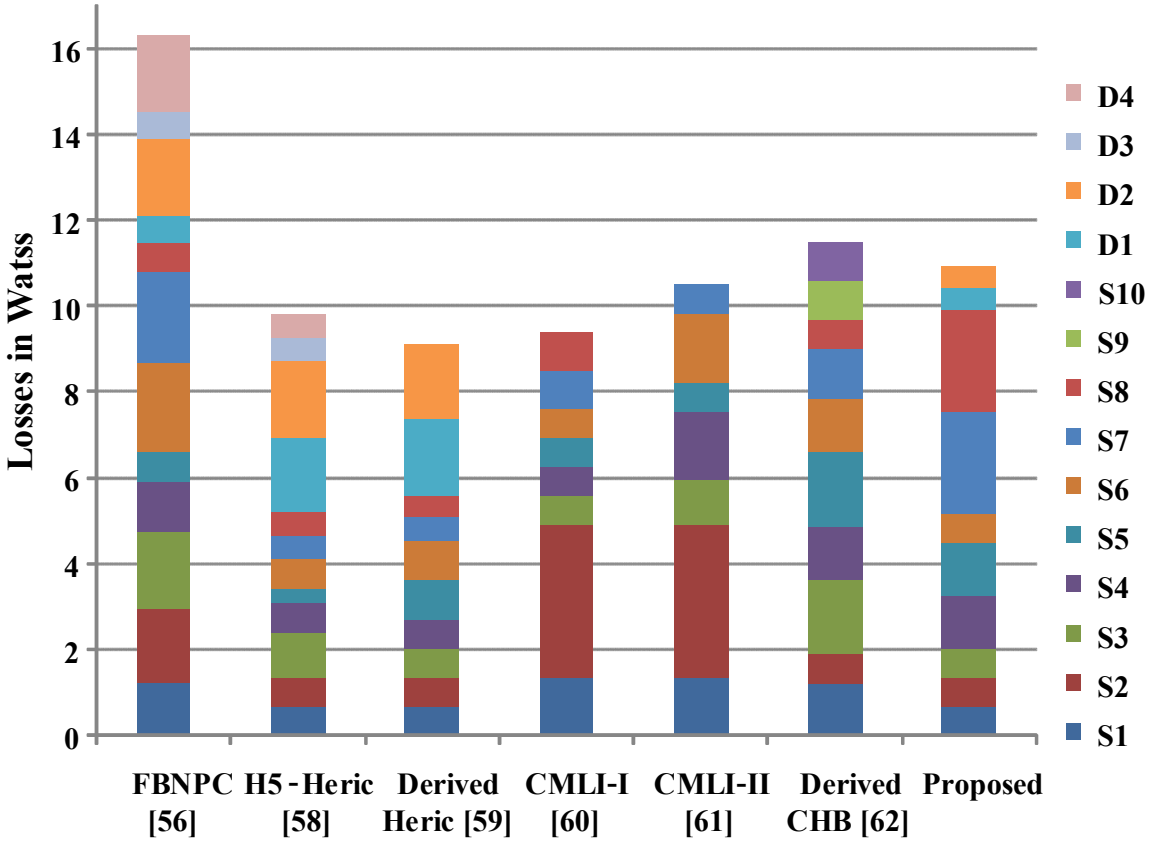


Fig. 6.23. Loss distribution of the various TLIs with proposed topology.

6.8. Summary

In this chapter, a single-phase two-stage T-type hybrid five-level inverter is presented, which provides boosting, multilevel operation, reactive power control and also offers minimum leakage current for transformerless *PV* applications. The 3LBC balances the DC-link capacitors by using a simple control algorithm, which reduces the control complexity of the inverter. The proposed inverter topology and its LSPWM technique

provide a path to the current at different power factor conditions without affecting the CMV behavior. Moreover, the leakage current flowing through C_{PV} is limited by clamping the terminal voltages of the inverter to half of the DC voltage during zero states and also by introducing common-mode path to the inverter using *LCL* filter. Both simulation and experimental results are presented to justify claims of the proposed configuration. Finally, a detailed comparison with the existing topologies is given to focus on the merits of the proposed configuration.

6.9. Contributions

a) The front-end power converter provides high efficiency and reduced inductor size for the same power rating over the conventional boost converter.

b) Eliminates both the high-frequency oscillations and sudden transitions in the total CMV, which results in a reduction of leakage current below the grid standard.

c) Modified PWM scheme enables the bi-directional current path of the inverter to improve the waveform quality in both unity and non-unity power factor conditions.

d) The efficiency and power density of the two-stage system is improved due to the absence of the transformer and additional CMF in the power conversion stage.

6.10. Papers Published

1) K. Sateesh Kumar, A. Kirubakaran, N. Subrahmanyam **"A Novel Two-Stage Hybrid T-type Five-Level Transformerless Inverter"** *IEEE i-PACT Conference, pp.1-6, 2019.*

2) Sateesh Kumar Kuncham, Kirubakaran Annamalai and Subrahmanyam Nallamothu, **"A Two-Stage T-type Hybrid Five-Level Transformerless Inverter for PV Applications"** *IEEE Transactions on Power Electronics,* vol. 35 (9), pp. 9512-9523, Sep. 2020.

Chapter 7

CONCLUSION AND FUTURE SCOPE

Chapter 7

Conclusion and Future Scope

7.1. Conclusion

Photovoltaic power generation systems (PVPGS) has acquired more importance than other renewable sources of energy due to its rooftop implementation ability in small and medium power scales connected to the 1-φ grid. To make the system more simple and reliable a line frequency transformer is eliminated from the power conversion stage. But, the removal of the transformer yields a direct connection between the inverter and PV module and it further results in the flow of leakage current due to PV parasitic capacitance. Generally, the high-frequency oscillations present in the common-mode voltage causes the flow of leakage current. Moreover, the flow of leakage current in the power circuit increases the electromagnetic interference, total harmonic distortion (THD) and power losses and also decreases the reliability and operational safety. To overcome the aforesaid drawbacks and make the system highly reliable for grid-connected PV applications, several topologies were proposed in the literature by eliminating the high-frequency oscillations in common-mode voltage (CMV). In contemporary, multilevel inverters are gaining much popularity in the PV power applications due to their high quality of output power, reduced filter size and THD.

In this thesis, a detailed literature has been reported based on various single-phase non-isolated voltage source based inverter topologies for both single-stage and two-stage PV applications. After reviewing various topologies the following objectives have been identified for investigation,

- Pertinent and comprehensive literature review on both single-stage and two-stage inverter topologies for grid-connected PVPGS.
- Development of the new single-stage and two-stage inverter topologies for PVPGS with the features of lower switch count, lower leakage current, lower THD, high efficiency, and operability in negative power region.

- Operation, Design and Simulation of proposed topologies under steady state and dynamic conditions.
- Development of a proto-type model for experimental verification under standalone operation with equivalent DC source.

To address the above problems, this thesis proposes four single-stage three-level and three two-stage multilevel inverter topologies with the aim of, namely, (i) operability with a single source, (ii) reduced switch count, (iii) leakage current reduction without the use of isolation transformer, (iv) reactive power capability and (v) high efficiency.

Mindful of these objectives, in the first proposal a bi-directional clamping (BDC) based H5, Heric, H6 and Hybrid-bridge transformerless inverter topologies have been presented with improved PWM schemes. BDC branch reduces the leakage current by clamping the inverter terminal voltages to half of the DC-link voltage during the freewheeling period and the improved PWM schemes ensure bi-directional current path while operating in the non-unity power factor conditions. Thus, the magnitude of leakage current is reduced in the proposed topologies. Moreover, the proposed topologies are mostly suitable for string inverters.

In the second proposal, a single-phase two-stage seven-level power conditioner for grid-connected PVPGS is presented in this thesis, which can be most suitable for multi-string and module type applications. The proposed single-phase seven-level power conditioner employs a front end DC-DC boost converter and an asymmetrical seven-level inverter. This topology uses very few power semiconductor switches in comparison with other topologies for the realization of seven-level output, which leads to improved efficiency. Moreover, it ensures guaranteed balancing of DC-link capacitor voltages with the use of high-frequency transformer in the front-end converter. Besides, the leakage current is limited effectively within the VDE0126-1-1 grid standards by employing an additional common mode filter. However, the use of high-frequency transformer and common mode filter reduces the power density and increases the size of the overall two-stage system.

Owing to the above problems, a single-phase hybrid transformerless multilevel inverter is proposed for PV power applications. The self-balanced capacitor voltage capability of the MLBC enables low control complexity and modularity for any level of output DC and also provides high boosting gain. The proposed multilevel inverter structure and its modulation technique provide the bi-directional path to the current in all modes of operation. Also, reactive power control is also possible without affecting common-mode voltage behavior and the output levels in the multilevel inverter. The leakage current is within the limits of grid standards due to the elimination of the high-frequency oscillations in total CMV. However, due to the sudden transition in V_{tcmv} from V_{dc} to 0 induces a sudden spike in the leakage current. Sometimes, it can cross the grid standards due to the intermittent nature of the PV parasitic capacitance. Also, the front-end boost converter requires more number of capacitors and diodes to realize the boosting operation.

In order to overcome this shortcoming, a two-stage T-type hybrid five-level transformerless inverter (TLI) for grid-connected photovoltaic (PV) applications has been presented. The proposed T-type hybrid five-level inverter and its level-shifted pulse width modulation scheme offers, reduced leakage current by eliminating the high frequency variations and sudden transitions in the voltage across PV parasitic capacitance (C_{PV}) and provides a path for the negative current in all the modes of operation under unity and non-unity power factor conditions of the grid without degrading the waveform quality. Moreover, in this chapter, the proposed inverter is integrated with a traditional three-level boost converter (3LBC) for boosting the lower PV voltage to higher DC-link voltage and also to extract maximum power from the PV source. The 3LBC provides high efficiency and reduced input inductor size for the same power rating over the conventional boost converter.

In order to evaluate steady-state and dynamic performance of all the proposed topologies reported in the thesis, a thorough investigation of all the topologies has been achieved through simulation studies and experiments. The simulations are performed in MATLAB/Simulink software and the prototype models are built using IRFP460 MOSFET modules and TLP250 opto-coupler driver ICs. The control schemes are implemented in MATLAB Platform using

Xilinx System Generator Blocks, Spartan 6 FPGA processor and DSP TMS320F2812/28335 processor for real-time operation. The grid-connected operation of the proposed topologies is verified using OPAL-RT OP4500 real-time modules. Moreover, in this study, an exhaustive comparison of various topologies have been done with the proposed topologies to demonstrate the merits in terms of component count and voltage stress across the semiconductor devices, common-mode voltage behavior and leakage current magnitude. Finally, the performance of the proposed topologies is evaluated through the PSIM thermal modules, which indicate a maximum efficiency of 90-98%. It ensures that the proposed topologies are most opted for PVPGS.

7.2. Author's contribution

I. Bi-directional Clamping Based H5, Heric, H6 and Hybrid-Bridge Transformerless Inverter Topologies with Reactive Power Capability

Bi-directional clamping based H5, Heric, H6 and Hybrid TLI topologies for PVPGS are proposed to achieve,

a) Reduced leakage current by abolishing the fluctuations in V_{TCMV} due to switch junctions capacitances.

b) Reactive power capability with a modified SPWM technique.

c) Reduction of the number of components compared to the classical decoupling and clamping based single-stage three-level inverters.

II. Single-Phase Two-Stage Seven-Level Power Conditioner for Photovoltaic Power Generation System

a) Registers high efficiency and lower component count for the realization of seven-level output voltage as compared to the conventional topologies.

b) High-frequency oscillations in the voltage across PV parasitic capacitance are eliminated and thereby the leakage current is reduced below the VDE-01260-1-1 grid standards.

c) It provides the reactive power support for the grid-connected PVPGS.

III. A Single-Phase Two-Stage Hybrid Transformerless Multilevel PV Inverter

a) Requires lower switch count for the realization of seven-level output voltage in comparison with traditional NPC, FC and CHB topologies.
b) Functions like boosting of the PV voltage, balancing the DC-link capacitor voltages and the reduction of leakage current can be achieved without the use of high-frequency transformer.
c) The modified SPWM scheme provides the bi-directional current path to the inverter for supporting the reactive power flow without disturbing the waveform quality.
d) Both converter and the inverter are modular to obtain the more number of output voltage levels.

IV. A Two-Stage T-Type Hybrid Five-Level Transformerless Inverter for PV Applications

a) The front end power converter provides high efficiency and reduced inductor size for the same power rating over the conventional boost converter.
b) Eliminates both the high-frequency oscillations and sudden transitions in the total CMV, which results in a reduction of leakage current below the grid standard.
c) Modified PWM scheme enables the bi-directional current path of the inverter to improve the waveform quality in both unity and non-unity power factor conditions.
d) The efficiency and power density of the two-stage system is improved due to the absence of the transformer and additional CMF in the power conversion stage.

7.2. Future Scope

The proposed research can be extended further in the following areas:

- Investigation of the proposed configurations for three-phase systems.

- Investigation of the proposed configurations with PV and grid-connected systems in order to further evaluate the performance of the system in real-time.
- Investigation of other single-stage and two-stage multilevel inverter topologies with reduced switch count, lower leakage current and reactive power control capability.
- Addressing different control techniques and advanced control algorithms for grid-connected PVPGS to feed both the real and reactive power into the grid with reduced control complexity.

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LIST OF PUBLICATIONS

International Journals

1) Sateesh Kumar Kuncham, Kirubakaran Annamalai, and Subrahmanyam Nallamothu. "**A new structure of single-phase two-stage hybrid transformerless multilevel PV inverter**" *International Journal of Circuit Theory and Applications,* vol. 47 (1), pp. 152-174, Jan-2019.
2) Sateesh Kumar Kuncham, Kirubakaran Annamalai, and Subrahmanyam Nallamothu. "**Single-Phase Two-Stage Seven-Level Power Conditioner for Photovoltaic Power Generation System**" *IEEE Journal of Emerging and Selected Topics in Power Electronics,* vol.8 (1), pp. 794-804, Apr. 2019.
3) Sateesh Kumar Kuncham, Kirubakaran Annamalai, and Subrahmanyam Nallamothu, "**An Improved Hybrid-Bridge Transformerless Inverter Topology with Bi-Directional Clamping and Reactive Power Capability**" *IEEE Transactions on Industry Applications*, vol. 55 (6), pp. 7400-7409, May. 2019.
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5) Sateesh Kumar Kuncham, Kirubakaran Annamalai, and Subrahmanyam Nallamothu, "**Bi-Directional Clamping Based H5, HERIC and H6 Transformerless Inverter Topologies with Reactive Power Capability**" *IEEE Transactions on Industry applications,* (DOI: 10.1109/TIA.2020.2999552).

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1) K. Sateesh Kumar, A. Kirubakaran, N. Subrahmanyam **"A Hybrid-Bridge Asymmetrical Transformerless Five-Level Photovoltaic Inverter",** 2017 *14th IEEE INDIA councilI INDICON-2017 Conference, pp.1-6, 2017.*
2) K. Sateesh Kumar, A. Kirubakaran, N. Subrahmanyam **"A Novel Two-Stage Hybrid T-type Five-Level Transformerless Inverter"** *IEEE i-PACT Conference, pp.1-6, 2019.*
3) K. Sateesh Kumar, A. Kirubakaran, N. Subrahmanyam **"Bi-Directional Clamping Based H5, HERIC and H6-Type Transformerless Inverter Topologies with Improved Modulation Technique"** *IEEE PESGRE Conference, pp.1-6, 2020.*

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