INVESTIGATIONS ON TOPOLOGIES AND CONTROL ALGORITHMS OF DSTATCOM TO COMPENSATE CURRENT RELATED POWER QUALITY ISSUES

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requirements for the award of the

degree of

DOCTOR OF PHILOSOPHY

in

ELECTRICAL ENGINEERING

by

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CERTIFICATE

This is to certify that the thesis entitled **"Investigations on topologies and control algorithms of DSTATCOM to compensate current related power quality issues"**, which is being submitted by **Mr. Alladi Pranay Kumar (Roll No. 716011)**, is a bona fide work submitted to National Institute of Technology Warangal in partial fulfilment of the requirement for the award of the degree of **Doctor of Philosophy** in Department of Electrical Engineering. To the best of my knowledge, the work incorporated in this thesis has not been submitted elsewhere for the award of any degree.

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DECLARATION

This is to certify that the work presented in the thesis entitled **"Investigations on topologies and control algorithms of DSTATCOM to compensate current related power quality issues "** is a bona fide work done by me under the supervision of **Dr. G. Siva Kumar, and Dr. D. Sreenivasarao,** Assistant Professors, Department of Electrical Engineering, National Institute of Technology Warangal, India and was not submitted elsewhere for the award of any degree.

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ABSTRACT

In modern distribution systems, the major power consumption has been in reactive and non-linear loads, such as motor drives, fans, pumps, and power electronic equipment. The consumption of excessive reactive power results into poor power factor at supply mains, poor voltage regulation, increased feeder losses and reduced the active power flow capability of the distribution system. Moreover, situation worsens in the presence of non-linear loads and raises power quality issues in distribution system. The operation of non-linear loads in distribution systems results into harmonic current burden and interrupts the normal operation of electrical and electronic equipment that are connected to the distribution system. At the same time, the power electronic equipment are typically designed with sophisticated microprocessor-based controllers which are quite sensitive to deviations in the voltage waveform. In recent years, with the advent of sophisticated electronic equipment, the electric power quality (PQ) has become an issue of concern and extensive research is being held to improve the power quality.

In the early days, synchronous condenser, mechanically switched capacitors and inductors have been used for reactive power compensation. However, due to their slow response and mechanical wear and tear, use of these devices is limited for the applications where fast compensation is not desirable. With the advent of first generation flexible alternating current transmission system (FACTS) devices, thyristor-controlled static var compensators (SVCs) made a significant advances in reactive power compensation. These devices are fast in operation and smooth control of reactive power compensation can be obtained. These SVC schemes are attractive due to their theoretical simplicity, however, practical disadvantages such as requirement of large inductor and capacitor banks, dependency of the reactive power compensation on operating voltage, hindered their popularity. With the significant progress of self-commutated semiconductor devices, attention has been focused on second generation FACTS devices which are based on voltage source and current source inverters. Among them, static synchronous compensator (STATCOM) has attracted the attention of researchers and power industries

for reactive power compensation and voltage regulation in transmission systems.

On the other hand, in the distribution system, harmonic regulation guidelines such as IEEE 519-1992 and IEC 61000 are applied to limit the current and voltage harmonics levels. To meet these requirements, the harmonics must be mitigated. Therefore, to eliminate harmonics and compensate reactive power, the FACTS technology can be extended further to distribution system. These devices solve power quality problems in the distribution system and they are popularly known as custom power devices (CPDs). The family of CPDs includes distribution static compensator (DSTATCOM), dynamic voltage restorer (DVR) and unified power quality conditioner (UPQC). Among them, DSTATCOM is a shunt connected device, which mitigates current related power quality problems, such as reactive power compensation, harmonic elimination, load balancing and neutral current elimination. In this thesis, an attempt has been made to develop and control various DSTATCOM topologies for power quality improvement in three-phase four-wire (3P4W) distribution system.

A cost-effective and high performance inverter is a prerequisite for the realization of a DSTATCOM. These inverters can be broadly categorized into two classes, namely, voltage source inverter (VSI) and current source inverter (CSI). In the present work, VSI has been considered as a power circuit for DSTATCOM, due to its higher market penetration and more noticeable development as compared to CSI topologies. The performance of any DSTATCOM topology depends on topology of VSI, reference current extraction technique and controller used to generate the switching pulses.

Among the available DSTATCOM topologies, three H-bridge (HB), three leg DSTATCOM, three-phase split-capacitor (TPSC) DSTATCOM and four leg DSTATCOM (FL-DSTATCOM) topologies are treated as traditional topologies. Three single phase H-bridge inverters are used to implement a three HB DSTATCOM, which can be applicable to both three-phase three-wire (3P3W) and 3P4W systems. However, the limitations of this topology are requirement of higher number of switching devices and coupling transformers, which will increase the size and cost of the DSTATCOM. A three leg VSI based DSTATCOM is having lesser number of switching devices and do not require any coupling transformers. However, this topology is not suitable for 3P4W systems. The structure of TPSC topology is same as three leg topology except the number of capacitors in its dc link. The dc link of three leg DSTATCOM consists of only one capacitor

whereas, the dc link of TPSC topology consists of two capacitors. The mid-point of the dc link is connected to the neutral conductor so that it is suitable for both 3P3W and 3P4W systems. The limitation of TPSC topology is, unequal voltage sharing of dc link capacitors during the transient operation of unbalanced and non-linear loads. FL-DSTATCOM require two additional switches compared to three leg and TPSC and it is suitable for both 3P3W and 3P4W systems. The advantages of this topology are better controllability, simple structure, easy control and the absence of capacitor voltage balancing problem unlike TPSC topology.

The conventional reference current extraction techniques are, unit template theory (UTT), instantaneous reactive power theory (IRPT), synchronous reference frame theory and instantaneous symmetrical component theory (ISCT). In recent years, model predictive control (MPC) has attracted researchers to replace, conventional pulse width modulation (PWM) and hysteresis controllers due to its versatile nature. The advantages of MPC are, simple addition and treatment of constraints, multi-variable case can be easily addressed, simple structure and good transient and steady state response. In MPC, the difference between the reference and actual value of a variable is considered as a cost function and evaluate the cost function for the available switching states. Among all the states, select a switching state, which minimizes the cost function and apply it for the upcoming instant. The additional constraints are included in the cost function using weighting factor and the weighting factor values are ranging from 0 to ∞. one of the considerable limitation of MPC is higher switching frequency.

In this thesis, an attempt has been made to overcome the capacitor voltage balancing problem in TPSC topology, by including an additional constraint in the cost function along with current control. Similarly, The higher switching frequency limitation of MPC is also reduced by including an additional constraint in the cost function. These two additional constraints are included using weighting factors and selection of weighting factor values has done using VlseKriterijumska Optimizacija I Kompromisno Resenje (VIKOR) method.

To reduce the higher neutral leg switching frequency of FL-DSTATCOM, an additional constraint is included in the cost function using weighting factor and the Technique for Order Preference by Similarity to the Ideal Solution (TOPSIS) is applied to simplify the weighting factor tuning process. The reduction in neutral leg switching frequency will

reduce the phase leg switching frequency as they are dependent on each other.

Conventional MPC do not use any modulating signal, therefore it is a variable switching frequency control technique. This variable switching frequency further leads to uneven switching stress and also makes the filter design little complex. An attempt has been made in this thesis, to overcome the limitation and operate the VSI at constant switching frequency by using the concept of three dimensional space vector modulation (3DSVM).

Four switch VSI based DSTATCOM topologies are cost effective solution compared to TPSC and FL-DSTATCOM topologies. However, the absence of fourth leg in these two topologies, restrict them for 3P4W systems. Therefore, in the presesnt work, four different DSTATCOM topologies are formed by combining, two four switch VSI topologies with different transformer arrangements such as zigzag and T-connected transformer. This combination will reduce the cost of the DSTATCOM as well as compensate the current related power quality issues along with neutral current compensation.

The control algorithms have been implemented on dSPACE MicroLabBox 1202 R&D controller, the topologies are implemented using an IGBT based inverter and LEM made voltage and current transducers are used to sense the voltage and current signals. The developed prototypes have been studied for reactive power compensation, harmonic elimination and neutral current compensation with different loading and utility conditions.

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ABBREVIATIONS

3DSVM	Three dimensional SVM
3HB	Three H-Bridge
3P3W	Three-Phase Three-Wire
3P4W	Three-Phase Four-Wire
AC	Alternating Current
APF	Active Power Filter
CCM	Current Control Mode
CPD	Custom Power Device
CSI	Current Source Inverter
DC	Direct Current
DSTATCOM	Distribution Static Compensator
FACTS	Flexible AC Transmission Devices
FL-DSTATCOM	Four Leg DSTATCOM
FSOC	Four-Switch One-Capacitor
FSSC	Four-Switch Split-Capacitor
HC	Hysteresis Controller
HVDC	High Voltage Direct Current
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronics Engineers
IGBT	Insulated Gate Bipolar Transistor
IRPT	Instantaneous Reactive Power Theory
ISCT	Instantaneous Symmetrical Component Theory
MCDM	Multi-Criteria Decision Making
MPC	Model Predictive Control
PCC	Point of Common Coupling
PI	Proportional Integral
PLL	Phase Locked Loop
PQ	Power Quality

PWM	Pulse Width Modulation
RMS	Root Mean Square
SRF	Synchronous Reference Frame
SSB	Solid State Breaker
SSCL	Solid State Current Limiter
SSTS	Solid State Transfer Switch
SVM	Space Vector Modulation
THD	Total Harmonic Distortion
TPFL	Three-Phase Four Leg
TPFS	Three-Phase Four-Switch
TPSC	Three-Phase Split-Capacitor
UCC	Unit Capacitor Constant
UTT	Unit Template Technique
VA	Volt-Ampere
VAR	Volt Ampere Reactive
VCM	Voltage Control Mode
VSI	Voltage Source Inverter

NOTATIONS

λ	Weighting factor
ΔI	Acceptable current limit
ω	Fundamental frequency of the supply voltage in rad/s
θ	Angle between voltage and current
C	Cost function
C_{dc}	DC-link capacitance
f	Fundamental supply frequency
$f_{sw,max}$	Maximum switching frequency
f_{sw}	Switching frequency
G	Conductance factor
h	Hysteresis band
i_c^*	Reference rms filter current
i_c	Instantaneous filter or DSTATCOM current
I_c	rms filter current
i_{cn}	Instantaneous compensator side neutral current
I_{dc}	DC-link current for CSI
i_l	Instantaneous load current
i_{ln}	Instantaneous load neutral current
i_p	Active current component of load
i_q	Reactive current component of load
i_s	Instantaneous source current
I_s	rms source current
i_{sn}	Instantaneous source side neutral current
I_{spm}^*	Peak value of reference source current
I_l	rms load current
L_{dc}	DC-link inductance for CSI
L_s	Equivalent inductance of feeder
L_f	Interfacing inductance

m	Amplitude modulation index
n	Number of cycles with transient operation
P_{lavg}	Average real or active power of load
$Q_{f,max}$	Maximum DSTATCOM reactive power
R	Regret measure
R_s	Equivalent resistance of feeder
R_f	Internal resistance of Interfacing inductance
S	Utility measure
S_1	Upper switch of inverter leg connected to phase-a
S_2	Lower switch of inverter leg connected to phase-a
S_3	Upper switch of inverter leg connected to phase-b
S_4	Lower switch of inverter leg connected to phase-b
S_5	Upper switch of inverter leg connected to phase-c
S_6	Lowerr switch of inverter leg connected to phase-c
S_7	Upper switch of inverter leg connected to neutral
S_8	Upper switch of inverter leg connected to neutral
T	Fundamental time period
u_p	In-phase unit vector
u_q	Quadrature unit vector
V_{dc}^*, $V_{dc,ref}$	Reference dc-link voltage
v_c	Inverter output voltage
V_{dc}	DC-link voltage
v_{inv}	Instantaneous inverter or converter ac side voltage
v_s	Instantaneous source voltage
X	kVA rating of inverter

CHAPTER 1

Introduction

The role of the alternating current (ac) distribution system is to deliver the generated electric power to industrial, commercial and residential load centers. Distribution system has always been susceptible to problems regarding reactive power and unbalance from the very beginning. Continuous research in the area of power semiconductor devices has motivated researchers, to use them in applications such as adjustable speed drives, battery chargers, home appliances and electric vehicles [1], [2]. However, these power electronic equipment draw, non-linear currents which affect the distribution system as well as other loads connected to the system. In olden days, power outage is the only power quality issue known to most of the consumers. However, increased awareness among customers, has led them demanding manufacturers to develop electric equipment, which are susceptible to override power quality disturbances. Similarly, utilities must supply good quality of power to consumers for satisfactory operation of equipment. In general, power quality is the set of boundaries that allows a system to work in its intended manner without any significant loss in its performance [3]. It is necessary to maintain quality of power at various stages in power sector such as generation, transmission and distribution. Especially, it is very important at the utilization level, because the end user gets effected, if there are any issues in the quality of power.

1.1 Classification of power quality problems and their causes

The primary reasons for power quality issues are equipment failure, lightning, faults, notches, voltage distortions, operation of non-linear and unbalanced loads [4]. In general, power quality is quantified as current, voltage and frequency variations in the supply, which results in either mal-operation or failure of customer equipment. Voltage sags, swells, surge, notches, flicker, fluctuations, unbalance and harmonics are voltage related power quality issues that occur in the distribution system. Similarly, current

related issues are poor power factor, harmonic currents, unbalanced currents and large neutral current because of the presence of non-linear and unbalanced loads. The important reasons for power quality issues are mentioned below:

- The presence of arc furnaces, adjustable speed drives, uninterrupted power supplies and switch mode power supplies in the vicinity of consumers.
- Natural reasons such as lightning phenomena, flash-over and failure of electrical equipment.
- Operation of large capacitor banks and transformers.
- Distribution of single-phase loads with unequal rating.
- Frequent turn on and off of large motors and fluctuating loads.
- Operation of non-linear, unbalanced and reactive loads.

A brief explanation of major power quality issues are explained here.

Transients

Transient is defined as the part of change in a variable that disappears during transition from one operating condition to other operating condition. Transients can be further classified as impulsive and oscillatory. Impulsive transient is a sudden non-power frequency change in the steady-state condition of voltage, current or both in either positive or negative direction. However, oscillatory transient is change in both positive and negative directions.

Long-duration voltage variations

It is defined as the root mean square (rms) deviations at power frequencies for more that 1 minute. Long-duration voltage variations are further classified as over voltages, under voltages, and sustained interruptions. An increase in ac rms voltage to greater than 110 percent at power frequency for longer than 1 minute is defined as an over voltage. Energization of capacitor banks or switching off a large loads will create over voltages. At the same time, under voltage is defined as decrease in rms voltage to

90 percent at power frequency for more than 1 minute. The reason behind the under voltage is exactly opposite to over voltage. When the supply voltage is zero for a period of more than 1 minute it is named as sustained interruption.

Short-duration voltage variations

Fault conditions, higher starting currents due to turning and on of heavier loads and loose connections in power wiring are leading to short-duration voltage variations. They are further classified as sags, swells and interruptions. A sag is defined as the decrease in rms voltage or current to 0.1 to 0.9 per unit (pu) for a duration of 0.5 cycles to 1 minute. Similarly, swell is defined as an increase in rms voltage or current to 1.1 pu to 1.8 pu for a duration of 0.5 cycle to 1 minute. Finally, an interruption occurs when the load current or supply voltage decreases to less than 0.1 pu for a period of less than 1 minute.

Voltage imbalance

It is also named as voltage unbalance and it is defined as the ratio of maximum deviation from the average of three-phase voltages or currents to the average of three-phase voltages or currents. Voltage imbalance is always expressed in percent. It is also defined as, the ratio of either negative or positive sequence component to the positive sequence component. Presence of single-phase loads in three-phase system are the primary reason for voltage imbalance.

Waveform distortion

At power frequency, a steady state deviation from an ideal sine wave is defined as waveform distortion. There are five different types of waveform distortions and they are dc offset, harmonics, inter harmonics, notching and noise.

1.2 Effects of power quality problems on end users

The problems in power quality affect consumers, manufacturers and utilities, which can lead to production damage, wastage of raw material, missing data and equipment failure. Out of all the causes of power quality problems, operation of non-linear, unbalanced and reactive loads are considered to be one of the most significant reasons for power quality problems in modern distribution systems [4], [5]. Therefore, the scope of this thesis is limited to compensation of current related power quality issues only. These power quality issues lead to several problems in the distribution system such as:

- Increased losses in the system due to the requirement of large amount of reactive power.
- Excessive neutral current which require large size of conductor.
- Harmonic currents leading to harmonic torques in electric machines.
- Occurrence of resonance in inductor and capacitor banks due to the presence of harmonics.
- Negative and zero sequence currents in the distribution system.
- Vibrations, noise, over heating, derating of electric cables and causes dielectric breakdown.
- Mal-function of circuit breakers and relays.

A brief description of current related power quality issues are discussed below.

1.2.1 Reactive power burden

Reactive power burden on distribution systems is due to the operation of loads that draw high reactive power. Reactive power is a concept used by engineers to describe the background energy movement in an ac system arising from the production of electric and magnetic fields. These fields store energy which is exchanged in each ac cycle. Devices which store energy by virtue of a magnetic field produced by flow of current

are said to absorb reactive power; while those which store energy by virtue of electric fields are said to generate reactive power [6]. Volt-ampere reactive (VAR) is a unit used to measure reactive power in an ac electric power system. Reactive power is required to maintain the voltage to deliver active power through transmission lines and distribution feeders. Electric machines require reactive power for successful operation. When enough reactive power is not available, it is not possible to push the real power demanded by the loads through the lines. The satisfactory operation of customer appliances and industries require reactive power and it has to be supplied by the source. Motors, tap changing transformers, choke coils, inductive loads, phase controlled rectifiers are some of the examples of reactive loads in the distribution system [6]. This reactive power requirement will further reduce the power factor of the system. The increasing demand for reactive power or poor power factor causes,

- Increase in current rating of the system to supply the same amount of active power.
- Large copper losses which further reduce the efficiency of the system.
- Poor Voltage regulation.
- Necessity to increase conductor size which increases the cost.
- Requirement of large kilo-volt-ampere (kVA) rating equipment such as alternators and transformers.

1.2.2 Influence of harmonic currents

Harmonic currents are the unwanted frequency components superimposed on the fundamental current waveform. The main sources of harmonic currents, before the deployment of power electronic devices in the equipment are fluorescent lamps and electric arc furnaces. Similarly transformers and electric machines produce harmonic currents in low proportion [7]. In recent times, the rapid growth in the area of power electronic devices increased the amount of harmonic currents. The important sources of harmonic currents are adjustable speed drives using converters, ac voltage controllers, cyclo-converters, switched mode power supplies, high voltage direct current (HVDC) transmission, static VAR compensators and phase controlled rectifiers. The effects of harmonic currents are:

- Voltage waveform distortion.
- Series and parallel resonance problem.
- Requirement of capacitor banks for power factor correction.
- Over heating of electrical machines because of harmonic losses.
- Development of harmonic torques in electrical motors.
- The increment in the root mean square (rms) currents, causes additional power loss in the distribution network.

1.2.3 Influence of excess neutral current

In electrical power system, electricity is generated, transmitted and distributed mostly as a three-phase three-wire system (3P3W) or some times as three-phase four-wire (3P4W) system. In the distribution system, most of the consumer loads are single-phase with unequal rating [8]. The unequal distribution of single-phase loads on three phase distribution system will leads to unbalanced source currents, which further increase the amount of neutral current. Sometimes, the amount of neutral current flowing through the neutral conductor will be more than the line current [9]. In a balanced system, the use of non-linear loads will allow the flow of zero sequence currents which further increase the amount of neutral current [9]. Some of the sources of neutral currents are personal computers, printers and single-phase power supplies. The effects of higher neutral current are excessive power loss in neutral conductor, common mode noise, over loading of transformers and distribution feeders, wiring failure and flat topping of voltage waveform.

1.3 Power quality standards

There are several organizations on the national and international stages working closely with equipment manufacturers, research organizations and engineers to come up with standards governing guidelines, recommended practices, and harmonic limits [7]. The primary objective of the standards is to decide whether the amount of distortion will

affect the performance or not and they will provide a common ground for all involved parties to work together to ensure compatibility between the end-user equipment and the system. Therefore, to quantify these problems some standards have been developed by various institutes and organizations, so that, consumers, manufacturers and industries are required to follow standards to maintain acceptable level of power quality. Along with these standards, some measuring devices and measurement methodologies have been developed to quantify the level of power quality and its causes. The available standards are, IEEE Standard 519-1992, IEEE standard 1159-1995, IEC 61000-2-2, IEC 61000-2-4, and IEC 61000-3-2 and so on [10], [11]. IEEE 5191992 standard, limits the amount of current harmonics injected by a user at the point of common coupling (PCC). For example, the IEEE 5191992 standard recommends a limit of 5% total harmonic distortion (THD) in the current at the PCC in a weak system.

1.4 Solutions to power quality issues

Low quality power affects the customers in many ways. The lack of quality power will cause loss of production, damage of equipment or appliances or can even be detrimental to human health. Therefore, it is very important to maintain a high standard of power quality. There are sets of conventional solutions to the power quality problems, which have existed for a long time. However these conventional solutions use passive elements and do not always respond correctly with ever changing power systems. The increased power capabilities, ease of control, and reduced costs of modern semiconductor devices have made power electronic converters affordable in a large number of applications. New flexible solutions to many power quality problems have become possible with the aid of these power electronic converters. Therefore, from past few decades, several mitigation techniques have been evolved to improve power quality, which includes,

- Passive power filters.
- Active power filters such as custom power devices.
- Hybrid power filters.

1.4.1 Passive power filters

As non-linear loads draw harmonic and reactive currents from the ac source for their satisfactory operation, these current components will reduce power factor of the system thereby reducing efficiency. These are also disturbing the other customers, protecting devices connected to the same system. Normally, harmonic currents are reduced by passive power filters and especially, when capacitors are connected to supply the required reactive power, which further improves the power factor [7]. These passive power filters are a combination of passive elements such as inductors, capacitors and resistors. Passive power filters are classified as series, shunt and hybrid power filters [12], [13]. Series filters are connected in series with non-linear loads which provides high impedance for harmonic currents, which does not allow them to enter into the supply system. Shunt filters are connected in shunt with harmonic loads, and provide low impedance path for the harmonic currents so that it will not enter into supply. Finally, hybrid filters are a combination of series and shunt filters.

These passive power filters can be sub classified as tuned and damped filters. Tuned filter act like a high pass filter in shunt connection and high block filter in series connection. Similarly, damped filters behave like a low pass filter in shunt connection and low block filter in series connection [7]. Some of the examples of tuned and damped filters are shown in Fig. 1.1 and Fig. 1.2. In these two figures, resistance, inductance and capacitance of the filter are represented as R, L, and C.

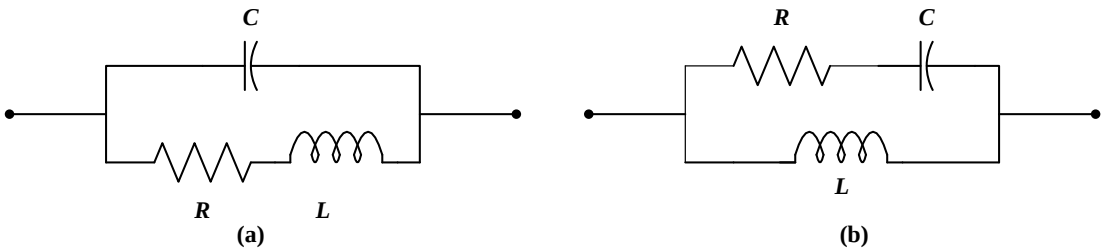


Fig. 1.1 Series passive power filters (a) Tuned filter, and (b) Damped filter.

The advantages of passive power filters are

- Implementation is simple.
- There are no switching and conduction losses which actually improve the efficiency.

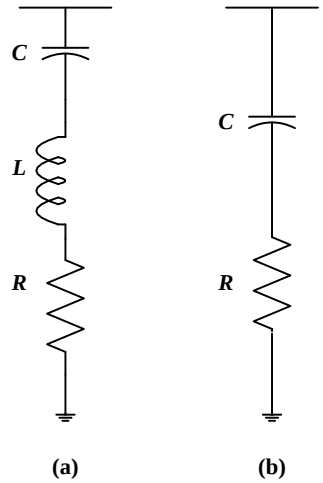


Fig. 1.2 Shunt passive power filters (a) Tuned filter, and (b) Damped filter.

- Improving voltage profile by supplying reactive power.

However, these passive filters have several limitations such as

- These filters are fixed once installed.
- Large size which further increases the cost.
- The changes in operating and weather conditions will lead to detuning of filter and also increases the level of distortion.
- Loss of missing or damaged elements leads to change in resonant frequency.
- The presence of dc components will saturate filter reactors.

The rapid growth in the power electronic devices encouraging the researchers to develop power electronic based compensating devices to overcome the limitations of passive power filters and they are named as active power filters.

1.4.2 Active power filters

The continuous increase in problems due to harmonic, reactive currents and the disadvantages of passive power filters, have attracted the attention of researchers to develop adjustable and dynamic solutions to mitigate power quality problems using power electronic devices and they are named as active power filters [14]–[16]. These active power

filters are classified as series, shunt and combination of series-shunt active power filters, depending on the type of connection. Series active power filters are designed to compensate the voltage related power quality issues. Shunt active power filters are used to compensate the current related power quality issues such as reactive power burden, harmonic elimination, load balancing, and elimination of excessive neutral current. After the evolution of insulated gate bipolar transistors (IGBT), these active power filters gain much more attention because of their easy implementation and control. With the continuous evolution of active power filters, the researchers are widened their compensation capabilities and formed a new group of compensating devices. These devices are named as custom power devices (CPD). The available CPDs are, distribution static compensator (DSTATCOM), dynamic voltage restorer (DVR) and unified power quality conditioner (UPQC). Among them, DSTATCOM is used to compensate current and voltage related power quality issues. The schematic diagram of a DSTATCOM connected distribution system is shown in Fig. 1.3. In this figure, i_{sa}, i_{sb}, and i_{sc} represents the source currents. i_{la}, i_{lb}, and i_{lc} represents the load currents. i_{ca}, i_{cb}, and i_{cc} represents the filter or compensator or DSTATCOM currents. v_{sa}, v_{sb}, and v_{sc} represents the voltages at PCC. L_f is interfacing inductance, R_f is internal resistance of L_f, source inductance and resistance are represented with L_s and R_s. $S_1 - S_6$ are the inverter switches. The operation of DSTATCOM and active power filter are identical to each other.

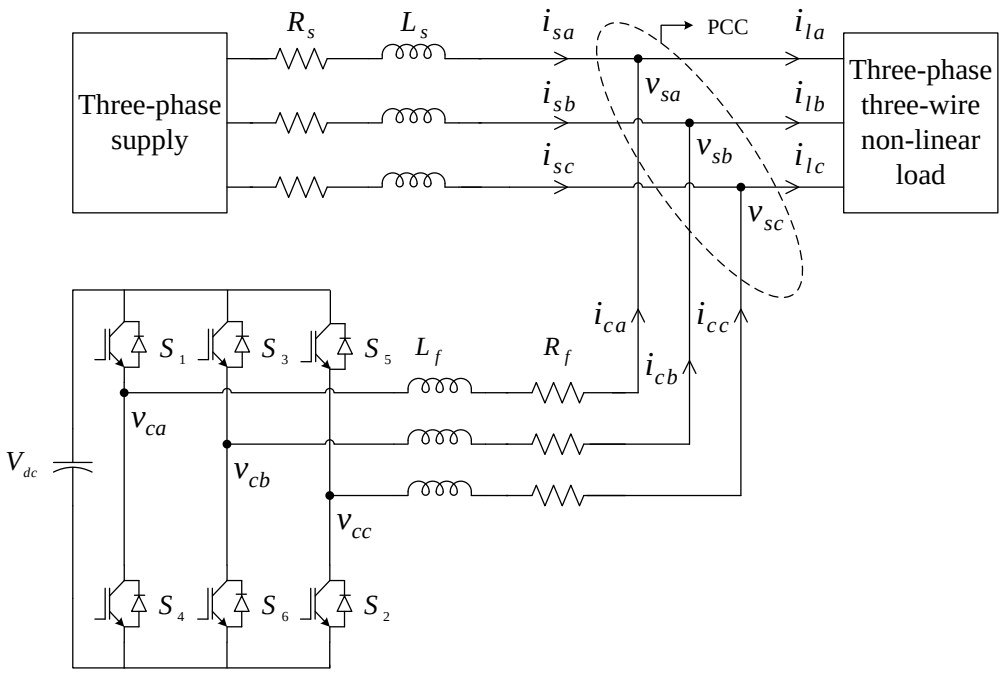


Fig. 1.3 Schematic diagram of DSTATCOM connected distribution system.

1.4.3 Hybrid power filters

Hybrid power filter is a combination of passive and active power filters. The ratings of the active filters are reduced by adding passive components to them and converting them as hybrid power filters [17]–[19]. These filters are cost effective solutions for some of the non-linear loads. The schematic diagram of the hybrid filter is shown in Fig. 1.4. The control and design complexity of hybrid power filters have limited its applications.

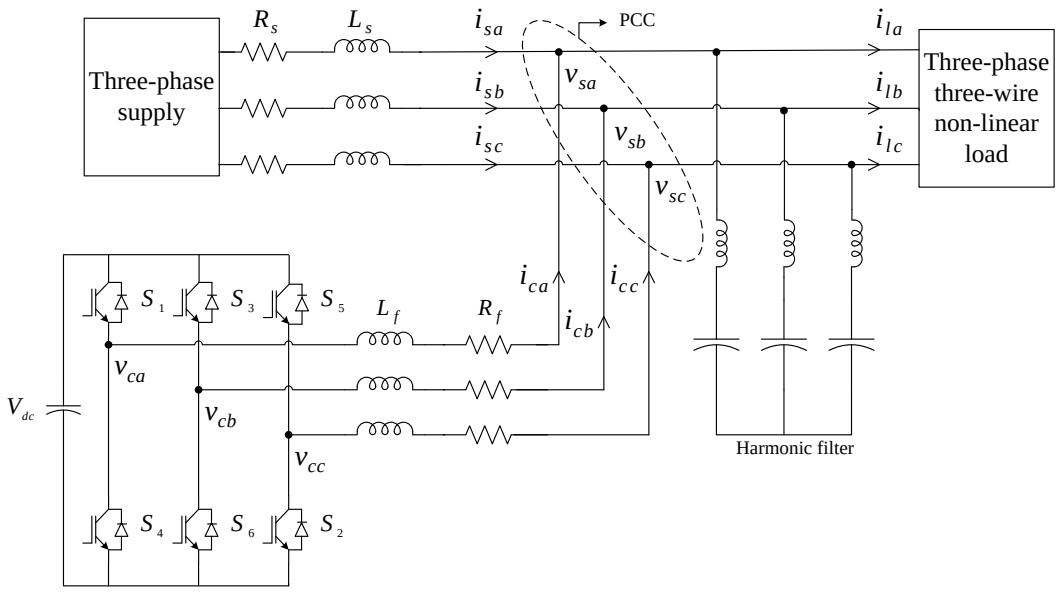


Fig. 1.4 Schematic diagram of hybrid filter connected distribution system.

1.5 Objectives

DSTATCOM is a shunt connected custom power device (CPD) which is used to compensate current and voltage related power quality issues in the distribution system. The performance of any DSTATCOM depends on its topology, reference current generation technique and control algorithm to generate switching pulses for the inverter. Based on literature of active power filters and their control algorithms [21]–[59], the following limitations are observed and motivated to considered them as objectives of this research work.

1. Conventional three-phase split-capacitor (TPSC) DSTATCOM has the limitation of voltage divergence of dc link capacitors during the compensation of unbal-

anced load currents [34], [35]. In literature, switching of inverter is adjusted to overcome this limitation; however, it further increases the control complexity. In recent years, model predictive control (MPC) methods have been used in many research areas because of its easy implementation, providing good dynamic and steady-state response, and constraints can be easily added to the cost function [54]–[57]. However, it has the limitation of higher switching frequency. To alleviate these problems, one constraint is to suppress voltage divergence and the other is to reduce the switching frequency is included in the cost function using weighting factors. Optimal selection of switching state for minimization of a multi-constraint cost function depends on the weighting factor; however, its tuning is a challenging task. Therefore, in this objective, the simplification of weighting factor tuning is achieved using VlseKriterijumska Optimizacija I Kompromisno Resenje (VIKOR) method and it further selects the optimal switching to improve power quality, reduce voltage divergence, reduce switching frequency and simplification of weighting factor tuning.

2. Even though four leg DSTATCOM (FL-DSTATCOM) has more switches compared to TPSC, the other advantages such as better controllability, low dc link voltage and absence of capacitor voltage balancing problem gives superiority to FL-DSTATCOM over other topologies [37], [38]. However, it has the limitation of higher neutral leg switching frequency. This higher neutral leg switching frequency can be reduced by including an additional constraint in the cost function using weighting factor, which is one of the advantage of MPC. But, the selection of weighting factor during multi constraint case is a cumbersome task. Therefore, in this objective, to simplify the weighting factor selection process, an optimization technique, namely, Technique for Order Preference by Similarity to the Ideal Solution (TOPSIS) is used, which further selects the optimal switching state to improve power quality, reduce the neutral leg switching frequency as well as simplify the weighting factor selection process.

3. MPC techniques have convenience of including additional control parameters in the cost function smoothly, and added constraints are treated according to their importance. However, using MPC, the switches of voltage source inverter (VSI) of DSTATCOM, have to operate at higher switching frequency which is also a variable value. Further, it lead to unequal stress and higher switching losses

across inverter switches. Therefore, a constant and user defined switching frequency MPC technique is developed using, three dimensional space vector modulation (3DSVM), which is applied to FL-DSTATCOM to conquer the limitations of MPC along with the compensation of power quality issues.

4. Among the available DSTATCOM topologies, three-phase four leg (TPFL) and three-phase split-capacitor (TPSC) topologies occupy a dominant position because of their simple structure. In the literature, to reduce the cost and size, TPFL and TPSC inverters are replaced with three-phase four-switch (TPFS) inverters [31], [32]. The performance of TPFS inverter is identical to three-phase four leg, three-phase split capacitor inverter topologies during balanced load conditions. During unbalanced load conditions, the absence of the neutral wire in TPFS topologies does not allow DSTATCOM to compensate the unbalance in load currents. To overcome this limitation, a special purpose transformer is connected across the load along with the DSTATCOM. Therefore, in this objective, two different TPFS topologies, namely, four-switch one-capacitor (FSOC) and four-switch split-capacitor (FSSC) are combined with two special purpose transformers which include zigzag and T-connected for 3P4W distribution systems to compensate the neutral current along with harmonic and reactive power.

1.6 Organization of the thesis

The complete thesis is divided into seven chapters. In this chapter, a brief introduction of power quality, causes along with effects of them on end users is discussed. Then solutions to power quality issues such as passive, active and hybrid power filters are explained. Finally, motivations and objectives of the thesis are discussed.

In **Chapter 2**, various topologies of DSTATCOM, reference current extraction techniques and controllers to generate the switching pulses are discussed.

In **Chapter 3**, reference current extraction using conductance factor method followed by predictive model of TPSC DSTATCOM and application of VIKOR method for optimal switching state selection is explained. Finally, simulation and experimental results are discussed which prove the efficiency of the proposed control algorithm.

In **Chapter 4**, reference current extraction under unbalanced and distorted supply conditions, predictive model of FL-DSTATCOM and application of TOPSIS method for optimal selection of switching state are explained. Then, simulation and experimental results are provided which show the efficacy of the proposed control algorithm.

In **Chapter 5**, initially MPC with three dimensional space vector modulation (3DSVM) to generate constant frequency switching pulses are discussed. Then simulation and experimental results are provided to prove the efficiency of the proposed control algorithm.

In **Chapter 6**, configuration of TPFS topologies with special transformers is discussed followed by neutral current compensation using special transformers connected TPFS DSTATCOM. Finally simulation and experimental results are explained, which shows superior performance of the proposed work. The main conclusions of the proposed work and possible future research scope have been summarized in **Chapter 7**.

CHAPTER 2

Configurations and Control Algorithms of DSTATCOM

Flexible ac transmission systems (FACTS) were developed to improve the power carrying capability and stability of the transmission system. Similarly, custom power is related to the application of power electronic controllers in the distribution system [3]. N. G. Hingorani has first introduced the concept of custom power and the custom power devices (CPD) are classified as network reconfiguring type and compensating type [20]. The available network reconfiguring type devices are solid state breaker (SSB), solid state current limiter (SSCL) and solid state transfer switch (SSTS). The applications of these devices are current breaking, current limiting and current transferring. Similarly, the compensating type devices such as CPDs are used either to improve the voltage quality or to compensate the current related quality issues. Among the available CPDs, distribution static compensator (DSTATCOM) is a shunt connected device which is used to improve power factor, current harmonics elimination and neutral current reduction [4]. The performance of any DSTATCOM mainly depends on its configuration, control algorithm to extract reference currents and controller to generate switching pulses for inverter.

2.1 Classification of DSTATCOM configurations

DSTATCOMs are mainly classified based on the type of converter used and number of phases [21]–[32]. The converter can be either voltage source inverter (VSI) or current source inverter (CSI). Supply based classifications are emerged on the number of phases and they are, two-wire (single-phase), three-phase three-wire (3P3W) and three-phase four-wire (3P4W) DSTATCOM [4].

2.1.1 Converter based classification

The connection diagram of CSI and VSI is shown in Fig. 2.1. In this figure, L_{dc} and I_{dc} represents dc link inductor and current flowing through the dc link inductor. Similarly,

C_{dc} and V_{dc} represents dc link capacitance and voltage across the dc link capacitor. CSI consists of IGBT switches and a diode connected in series with each switch to block the reverse voltage. CSI is always supported by a large inductor which acts as a current source. Similarly, VSI consists of IGBT with anti-parallel diode and they are supported by a capacitor which acts as a voltage source. The advantages of CSI is its robustness and the advantages of VSI are low initial cost, small size and high efficiency [21]. The advantages of VSI and its wide range of applications motivated to consider VSI as a power circuit in this thesis.

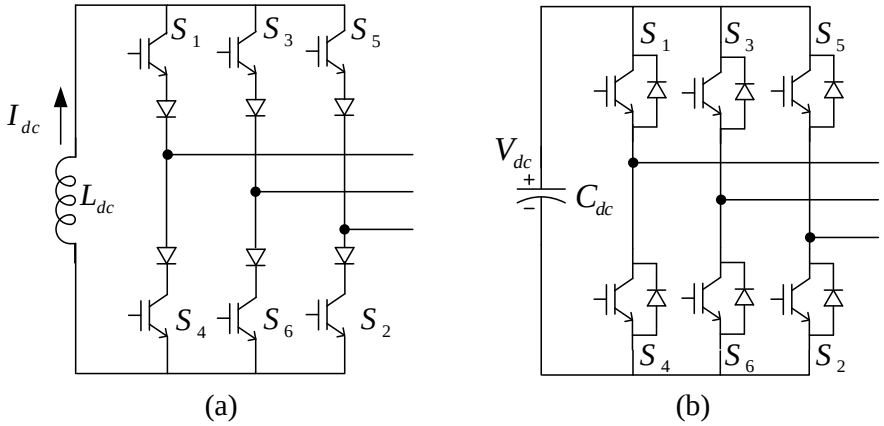


Fig. 2.1 Connection diagram of (a) Current source inverter (b) Voltage source inverter.

2.1.2 Supply based classification

Depending on the type of distribution supply system, DSTATCOMs are classified as single-phase or two-wire, 3P3W and 3P4W system .

Single-phase DSTATCOMs

Single-phase DSTATCOMs are dedicated to compensate power quality issues in the single-phase system. It will compensate the harmonic currents generated by non-linear loads and it can also improve power factor of the system [22]–[24]. Fig. 2.2 and Fig. 2.3 shows, two different single-phase DSTATCOM configurations such as single-phase H-bridge DSTATCOM and single-phase split-capacitor DSTATCOM. Single-phase H-bridge DSTATCOM shown in Fig. 2.2 has, four switches and one dc link capacitor. The mid-point of one leg is connected to phase conductor at point of common coupling (PCC) through an interfacing inductor while the mid-point of other leg is connected

to neutral conductor. Single-phase split-capacitor DSTATCOM shown in Fig. 2.3 has, two switches and two capacitors (C_{dc1} and C_{dc2}) in dc link. In this, the mid-point of the leg which is having two switches is connected to the phase conductor and the neutral conductor is connected to mid-point of capacitors. Even though this topology require only two switches, the voltage balancing of split-capacitors is a challenging task.

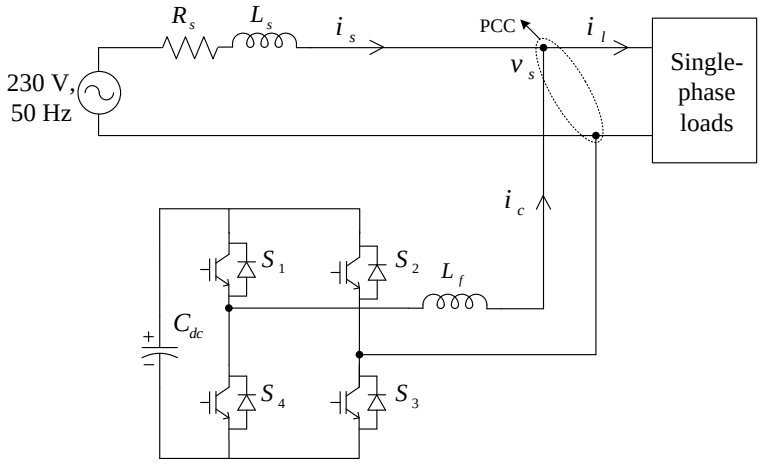


Fig. 2.2 Single-phase H-bridge DSTATCOM topology.

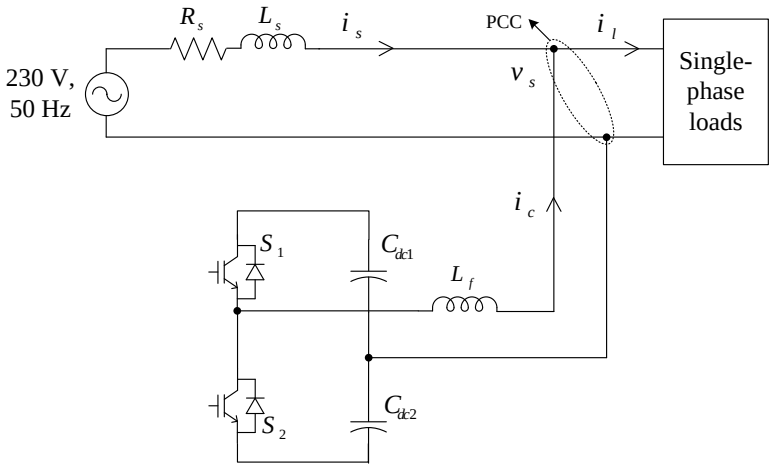


Fig. 2.3 Single-phase split-capacitor DSTATCOM topology.

Three-phase three-wire DSTATCOMs

Three-phase three-wire (3P3W) DSTATCOMs are mainly used in industrial applications, adjustable speed drives, arc furnaces and traction applications. In this kind of configurations, the absence of neutral wire has limited its applications to compensate balanced non-linear loads only. There are three different types of 3P3W DSTATCOM configurations available and they are shown in Fig. 2.4. In this figure, i_{sa}, i_{sb}, and i_{sc}

represents the source currents. i_{la}, i_{lb}, and i_{lc} represents the load currents. i_{ca}, i_{cb}, and i_{cc} represents the filter or compensator or DSTATCOM currents. v_{sa}, v_{sb}, and v_{sc} represents the voltages at PCC. Among them, conventional three leg DSTATCOM is shown in Fig. 2.4 (b). In this configuration, the output of each leg is connected to one phase at PCC through an interfacing inductor and the dc link has only one capacitor [25]–[28]. The second configuration is four-switch split-capacitor (FSSC) DSTATCOM and it is shown as Fig. 2.4 (c). In this configuration two legs are connected to two phases and the mid-point of split-capacitor is connected to third phase [31]. Four-switch one-capacitor (FSOC) DSTATCOM is the third configuration and is shown in Fig. 2.4 (d). In this configuration, two phases are connected to two legs and the third phase is connected to either negative or positive dc rail through a passive filter [32].

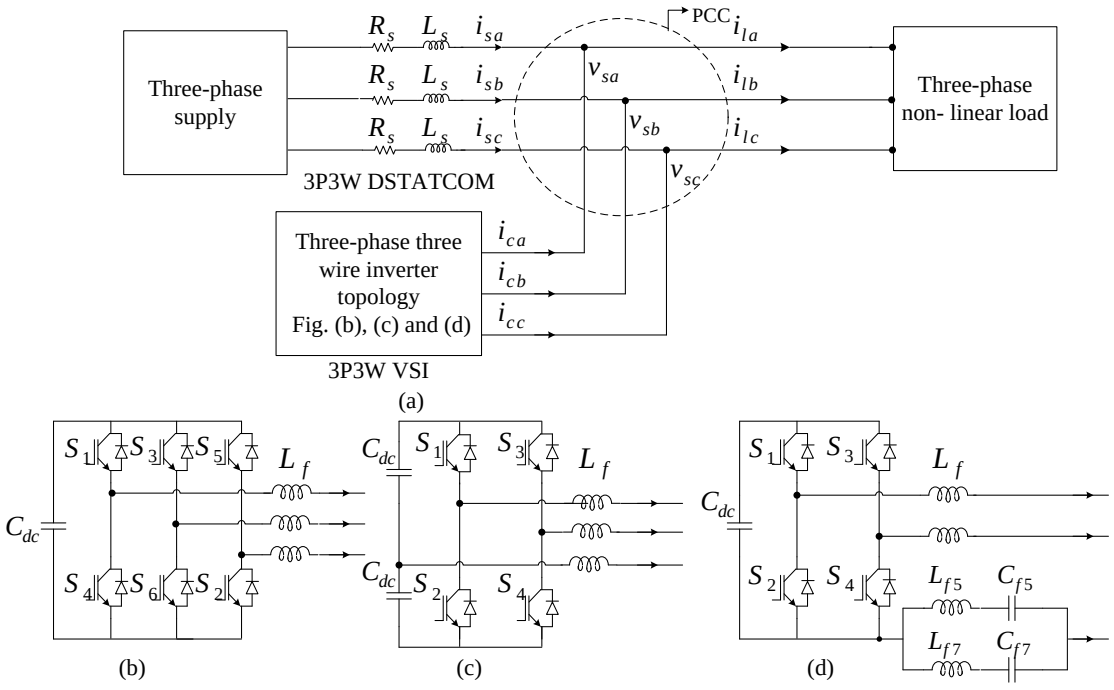


Fig. 2.4 (a) Schematic diagram of three-phase three-wire DSTATCOM topologies (b) Three leg DSTATCOM (c) FSSC, and (d) FSOC.

Three-phase four-wire DSTATCOMs

As mentioned, the absence of neutral wire in 3P3W DSTATCOM cannot compensate the unbalance in load currents. Therefore, to overcome this limitation three-phase four-wire (3P4W) DSTATCOM topologies are evolved in the distribution system [33]–[38]. This DSTATCOM configuration can improve power factor, reduce harmonic currents

and also compensate the neutral current. The available 3P4W topologies are three H-bridge (HB) DSTATCOM topology, three-phase split-capacitor topology (TPSC) and four leg DSTATCOM (FL-DSTATCOM). The schematic diagram of three HB DSTATCOM is shown in Fig. 2.5. In this topology, the outputs of three single-phase H-bridge inverters are connected to three isolation transformers [33]. One end of the secondary winding of each isolation transformer is connected to phase conductor and the other ends are connected to neutral conductor. This topology require twelve switches and also three isolation transformers for coupling.

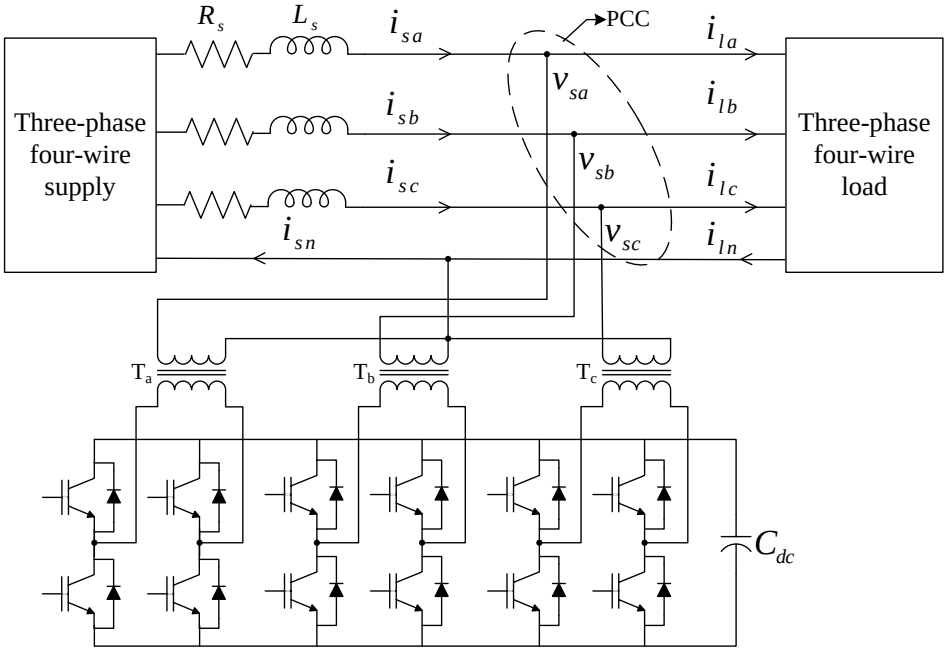


Fig. 2.5 Three H-bridge DSTATCOM topology in 3P4W distribution system.

The schematic diagram of TPSC DSTATCOM is shown in Fig. 2.6. In this topology, three legs are connected to PCC through interfacing inductors [34], [35]. The dc link of this topology is having two capacitors and the mid-point of these capacitors is connected to neutral conductor to compensate unbalanced load currents.

The higher unbalance or dc offset present in load currents leads to deviation of dc link capacitor voltages, which affects the performance of TPSC DSTATCOM. To overcome this limitation, a balancing circuit is required to connect across the dc link [36]. This additional control circuit consists of two switches and inductor with series resistance. The connection diagram is shown in Fig. 2.7. If the voltage across C_{dc1} is high compared to C_{dc2}, switch S_7 will turn on and C_{dc1} will deliver the additional energy to C_{dc2} through this inductor. This process will continue until the voltage across two capacitors

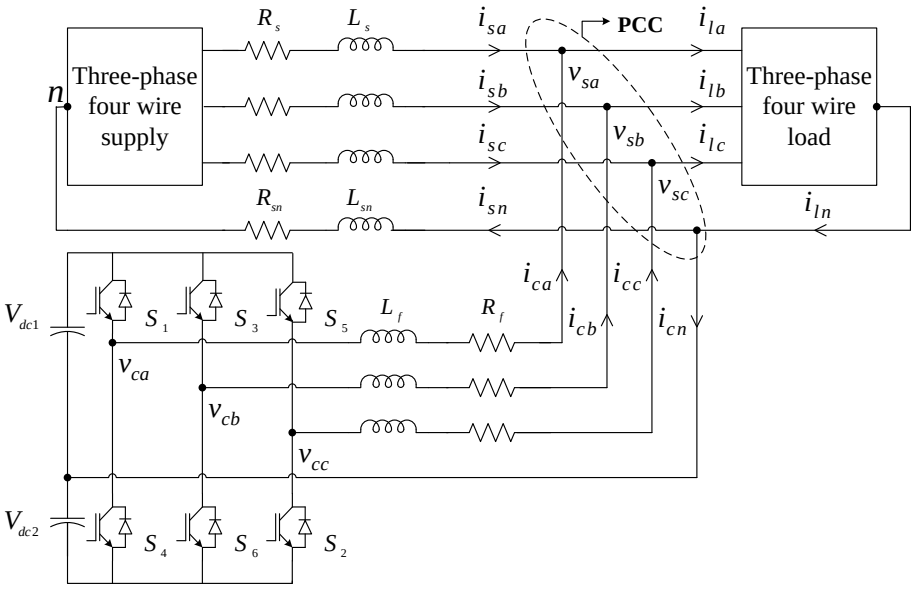


Fig. 2.6 Three-phase split-capacitor DSTATCOM topology in 3P4W distribution system.

is equal. The process is exactly opposite if the voltage across C_{dc2} is higher than C_{dc1}.

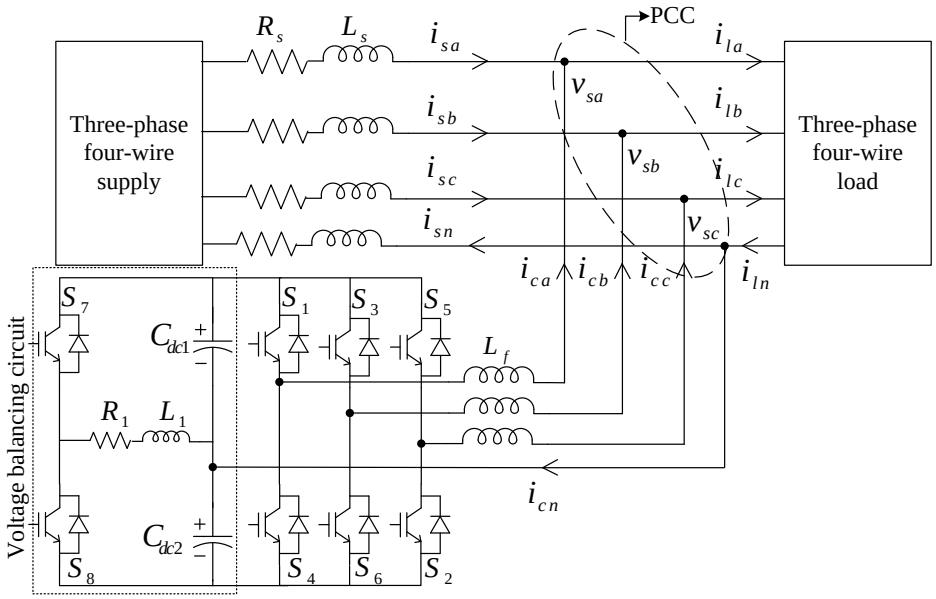


Fig. 2.7 Three-leg split-capacitor DSTATCOM topology with voltage balancing circuit in 3P4W distribution system.

The last configuration is four leg DSTATCOM (FL-DSTATCOM) and is shown in Fig. 2.8. This configuration is formed by adding an extra leg to 3P3W DSTATCOM shown in Fig. 2.4 (b). The number of switches in this configuration is fewer compared to three HB and high compared to TPSC. There is no capacitor voltage unbalance problem in this topology because, it is having only one capacitor in its dc link. Further the required dc link voltage is half of TPSC DSTATCOM [37], [38]. The comparison between all

these topologies is presented in Table. 2.1. From the table the following observations are made.

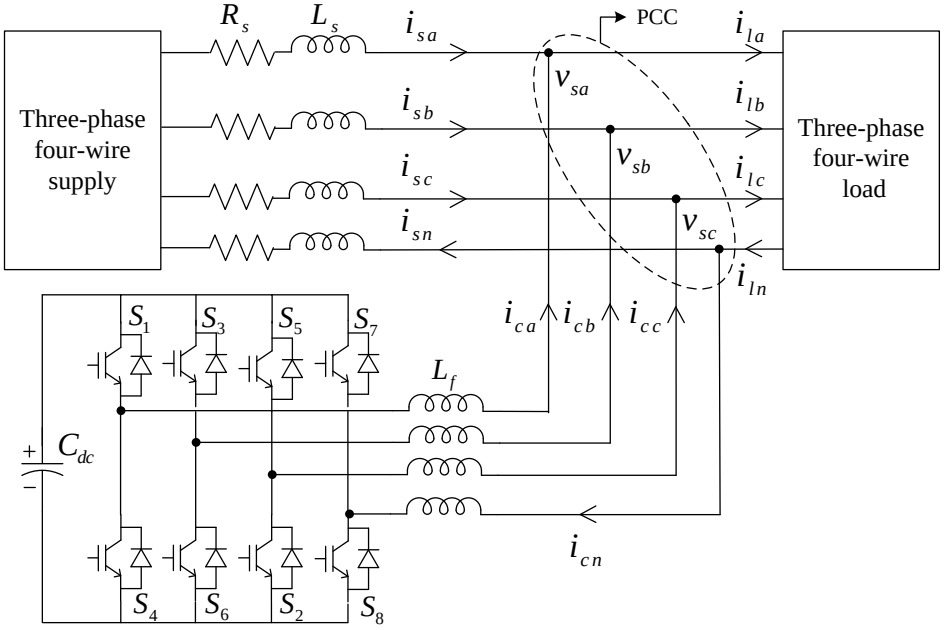


Fig. 2.8 Four leg DSTATCOM topology for 3P4W distribution system.

Table. 2.1 Comparison between three-phase DSTATCOM topologies

Topology features	Three H-bridge DSTATCOM [33]	Three leg DSTATCOM [25]–[28]	Three-phase split-capacitor DSTATCOM [34], [35]	Four leg DSTATCOM [37], [38]
Number of switches	12	6	6	8
Number of DC capacitors	1	1	2	1
Network suitability	3P3W, 3P4W	3P3W	3P3W, 3P4W	3P3W, 3P4W
Voltage stress across each switch	2 V_{sm}	$\frac{2}{\sqrt{3}}$ $(V_{sm})_{L-L}$	$\frac{3.2}{\sqrt{3}}$ $(V_{sm})_{L-L}$	$\frac{2}{\sqrt{3}}$ $(V_{sm})_{L-L}$
Switching loss	Comparatively low	Low	High	Moderate
Unbalance compensation	Yes	No	Yes	Yes
Total cost	Rs 98,587/-	Rs 54,643/-	Rs 55,631/-	Rs 69,939/-

where $(V_{sm})_{L-L}$ is peak of line to line PCC voltage.

- Three HB topology is suitable for both 3P3W and 3P4W applications. But the number of switches required to implement this topology is very high and it also requires three isolation transformers which increases the overall cost.

- Three leg DSTATCOM topology has fewer switches, low switching losses and is inexpensive to implement. However, this topology cannot compensate the unbalance in load currents, which implies that it is not suitable for 3P4W applications.

- TPSC topology is applicable to both 3P3W and 3P4W applications, having lesser number of switches and moderate cost. But, the required dc link voltage is high and it has capacitor voltage unbalance problem can occur during compensation of stringent unbalance loads.

- FL-DSTATCOM is also applicable to both 3P3W and 3P4W systems, have moderate switching losses, low dc link voltage and no capacitor voltage balancing problem. However, the limitation of this topology is that two extra switches and their control. Sometimes, the extra switches may operate at higher switching frequency.

2.2 Control algorithms to extract reference currents

Control algorithm of any DSTATCOM topology depends mainly on reference current extraction technique. There are two different control techniques available in literature. Between them one is direct control and the other is in-direct control. Direct control involves the estimation of reference DSTATCOM currents, where as, in-direct control deals with the estimation of reference source currents. Various reference current extraction methods are proposed in the literature and these methods are briefly classified as frequency domain and time domain methods [39]–[49]. Among the available frequency domain methods, Fourier series theory, fast Fourier transform theory, discrete Fourier transform theory and wavelet transform theory are commonly used [40]–[43]. However, these frequency domain methods have several limitations such as large memory requirements, proper design of anti-aliasing filter, proper synchronization between sampling time and fundamental frequency, high computational burden, sluggish nature and also performance is not satisfactory during transient conditions [40]. The time domain methods are having more advantages when compared to frequency domain methods such as simple implementation, increased speed and less number of calculations compared to frequency domain methods. The advantages and limitations of some of the available

time domain methods such as unit template technique, instantaneous reactive power theory (IRPT), synchronous reference frame theory (SRFT) and instantaneous symmetrical component theory (ISCT) are discussed in the following section [44]–[48]. The main purpose of using DSTATCOM is injection of suitable compensating currents, so that, supply has to deliver only average fundamental active component of load current, to make source currents balanced, sinusoidal and in-phase with the voltages at PCC. Therefore, the evolution of any reference current extraction technique mainly leads to extraction of average fundamental active component of load current.

2.2.1 Unit template technique (UTT)

The block diagram of reference current extraction using unit template technique is shown in Fig. 2.9 [4]. To implement this method, dc link voltage and PCC voltages are required to be sensed. The amplitude of PCC voltage (V_{sm}) is calculated using sensed PCC voltages as given in (2.1),

$$V_{sm} = \sqrt{\frac{2}{3}(v_{sa}^2 + v_{sb}^2 + v_{sc}^2)}. \tag{2.1}$$

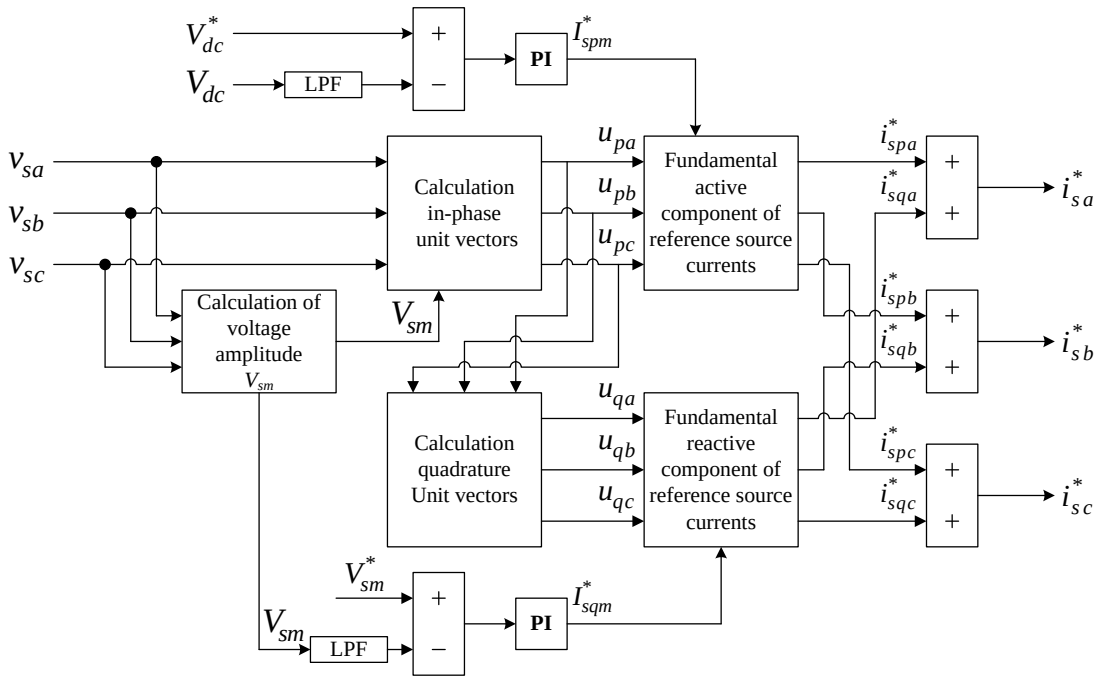


Fig. 2.9 Unit template technique (UTT).

The estimation of in-phase and quadrature unit vectors plays a vital role in this method.

In-phase unit vectors (u_{pa}, u_{pb}, and u_{pc}) are obtained by dividing sensed voltages with their amplitudes.

$$u_{pa} = \frac{v_{sa}}{V_{sm}}; \quad u_{pb} = \frac{v_{sb}}{V_{sm}}; \quad u_{pc} = \frac{v_{sc}}{V_{sm}}. \tag{2.2}$$

Where, v_{sa}, v_{sb}, and v_{sc} are the voltages at PCC. Apply vector alzebra, to calculate quadrature unit vectors (u_{qa}, u_{qb}, and u_{qc}) using in-phase unit vectors and they are given as,

$$u_{qa} = \frac{-u_{pb} + u_{pc}}{\sqrt{3}}; \quad u_{qb} = \frac{3u_{pa} + u_{pb} - u_{pc}}{2\sqrt{3}}; \quad u_{qc} = \frac{-3u_{pa} + u_{pb} - u_{pc}}{2\sqrt{3}}. \tag{2.3}$$

The derivation of unit vector extraction is explained in Appendix A. In self-supported DSTATCOM topologies, it is always required to maintain dc link voltage as a constant value. To achieve this, the difference between the reference and actual dc link voltage is processed through a PI controller, which gives the amplitude of active component of reference source current (I^*_{spm}). For power factor correction and load balancing, reference source currents are obtained by multiplying I^*_{spm} with in-phase unit vectors.

$$i^*_{spa} = I^*_{spm} \times u_{pa}, \quad i^*_{spb} = I^*_{spm} \times u_{pb}, \quad i^*_{spc} = I^*_{spm} \times u_{pc}. \tag{2.4}$$

Difference between the amplitude of reference PCC voltage (V^*_{sm}) and calculated PCC voltage is passed through a PI controller. The output of the PI controller is considered as the amplitude of reactive component of reference source (I^*_{sqm}) and it is multiplied with the quadrature unit vectors to obtain reactive component of reference source current (i^*_{sqa},i^*_{sqb}, and i^*_{sqc}).

$$i^*_{sqa} = I^*_{sqm} \times u_{qa}, \quad i^*_{sqb} = I^*_{sqm} \times u_{qb}, \quad i^*_{sqc} = I^*_{sqm} \times u_{qc}. \tag{2.5}$$

In voltage control using DSTATCOM, reference currents are obtained by adding reference fundamental active and reactive components and they are given as,

$$i^*_{sa} = i^*_{spa} + i^*_{sqa}, \quad i^*_{sb} = i^*_{spb} + i^*_{sqb}, \quad i^*_{sc} = i^*_{spc} + i^*_{sqc}. \tag{2.6}$$

The advantages of this method are simple in implementation and required fewer calculations. However, this method is generating reference currents from dc link voltage balancing circuit but not from the load currents, which leads to high amount of initial

currents and some times it does not give satisfactory performance [4]. The performance of this method completely depends on PI controller output, therefore small errors in the output of PI controllers leads to large deviations.

2.2.2 Instantaneous reactive power theory (IRPT)

Akagi H. et. al. proposed instantaneous reactive power theory and it is also called $p-q$ theory [44]. The name itself indicates that, this theory is dependent on the estimation of instantaneous reactive power so that DSTATCOM can compensate the reactive power required by the load, therefore it is valid not only in steady state but also in transient conditions. The block diagram of IRPT is shown in Fig. 2.10. In this theory, initially PCC voltages (v_{sabc}), load currents (i_{labc}) and dc link voltage (V_{dc}) are sensed. Then, the sensed voltages and currents are converted from abc frame to $\alpha\beta$ frame using Clarke's transformation. The instantaneous voltages and currents in $\alpha\beta$ frame are given as,

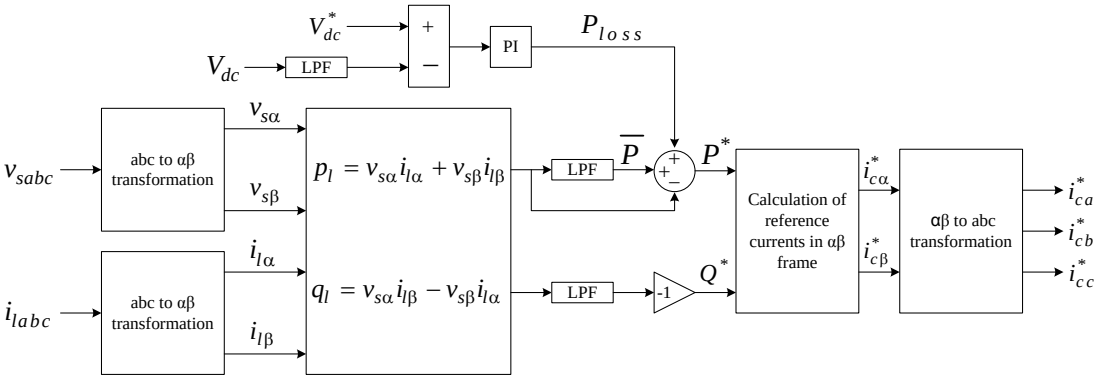


Fig. 2.10 Instantaneous reactive power theory (IRPT).

$$\begin{bmatrix} v_{s\alpha} \\ v_{s\beta} \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} v_{sa} \\ v_{sb} \\ v_{sc} \end{bmatrix} \tag{2.7}$$

$$\begin{bmatrix} i_{l\alpha} \\ i_{l\beta} \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} i_{la} \\ i_{lb} \\ i_{lc} \end{bmatrix}. \tag{2.8}$$

The instantaneous active and reactive powers are calculated using voltages and currents obtained from (2.7) and (2.8) and they are given as

$$\begin{bmatrix} p_l \\ q_l \end{bmatrix} = \begin{bmatrix} v_{s\alpha} & v_{s\beta} \\ -v_{s\beta} & v_{s\alpha} \end{bmatrix} \begin{bmatrix} i_{l\alpha} \\ i_{l\beta} \end{bmatrix}. \tag{2.9}$$

These active and reactive powers consists of average and oscillatory components, therefore p_l and q_l can also be represented as

$$p_l = \overline{p} + \tilde{p}, \qquad q_l = \overline{q} + \tilde{q}. \tag{2.10}$$

In the above equation $\overline{p}$ and $\overline{q}$ represent the average components and $\tilde{p}$ and $\tilde{q}$ represent the oscillating components. To get balanced and sinusoidal source currents with unity power factor, DSTATCOM has to supply complete reactive and harmonic power required by the load. Therefore, it is necessary to separate average and oscillating power components from total active and reactive powers and it is accomplished by a low pass filter. After separating the powers, $-\tilde{p}$, $-\overline{q}$ are considered as the reference powers for DSTATCOM to achieve its objective. However, in self-supporting DSTATCOM applications, the dc link require active power support to maintain constant voltage across the dc link. This active power component is obtained by, passing the difference between the reference and actual dc link voltages through a PI controller which is shown in Fig. 2.10. The output of the PI controller is represented as P_{loss} and it is added to $-\tilde{p}$. After getting the reference powers ($P^* = -\tilde{p} + P_{loss}$ and $Q^* = -q$), reference compensator currents are obtained using 2.11.

$$\begin{bmatrix} i^*_{c\alpha} \\ i^*_{c\beta} \end{bmatrix} = \frac{1}{v_\alpha^2 + v_\beta^2} \begin{bmatrix} v_\alpha & v_\beta \\ v_\beta & -v_\alpha \end{bmatrix} \begin{bmatrix} P^* \\ Q^* \end{bmatrix}. \tag{2.11}$$

The obtained reference currents are in $\alpha\beta$ frame. Therefore, using inverse Clarke's transformation, reference currents are converted into *abc* frame and they are given as,

$$\begin{bmatrix} i^*_{ca} \\ i^*_{cb} \\ i^*_{cc} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i^*_{c\alpha} \\ i^*_{c\beta} \end{bmatrix}. \tag{2.12}$$

The advantages of IRPT are simple implementation and PLL is not required to get the synchronization angle. The limitation of IRPT is, the performance of system is not satisfactory during distortions in supply voltage.

2.2.3 Synchronous reference frame (SRF) theory

Synchronous reference frame theory is also called as *dq* theory [26], [34]. The implementation of SRF theory requires various quantities such as load currents (i_{labc}), voltages at PCC (v_{sabc}), DSTATCOM output currents (i_{cabc}) and dc link voltage (V_{dc}). The pictorial representation of SRF theory is shown in Fig. 2.11.

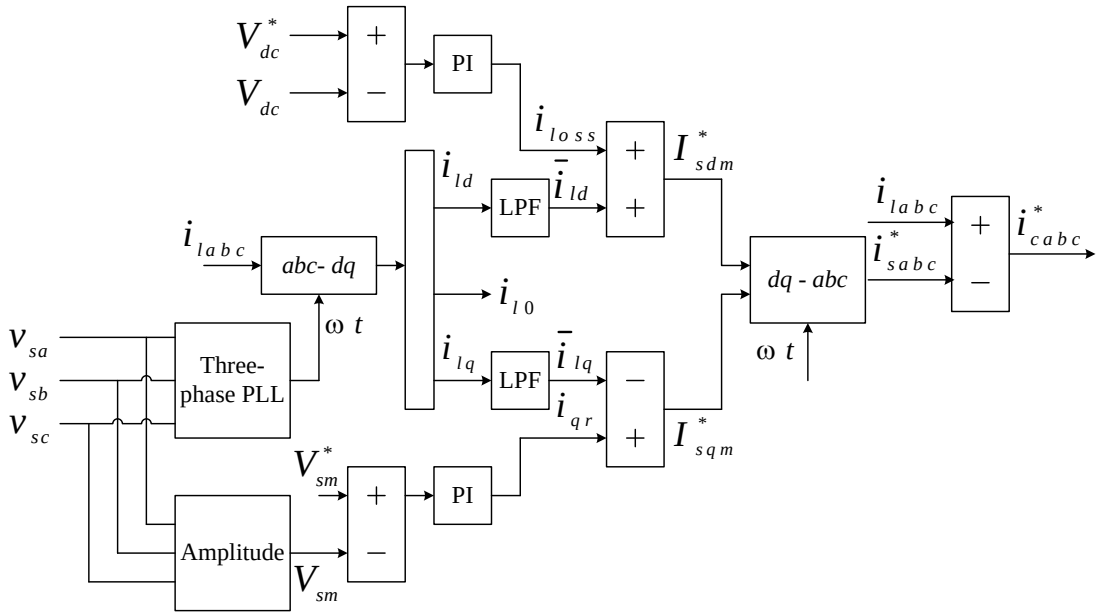


Fig. 2.11 Synchronous reference frame (SRF) theory.

Initially, sensed load currents are converted from *abc* frame to *dq* frame using *abc-dq* transformation. The load currents in *dq* frame are given as,

$$\begin{bmatrix} i_{ld} \\ i_{lq} \\ i_{l0} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos\omega t & \cos(\omega t - 120) & \cos(\omega t + 120) \\ -\sin\omega t & -\sin(\omega t - 120) & -\sin(\omega t + 120) \\ 1/2 & 1/2 & 1/2 \end{bmatrix} \begin{bmatrix} i_{la} \\ i_{lb} \\ i_{lc} \end{bmatrix}. \tag{2.13}$$

In the above equation, the information about synchronization angle (ωt) is obtained by passing v_{sa}, v_{sb}, and v_{sc} through a phase locked loop (PLL). The extracted *dq* currents

are the combination of average and oscillating components, which can be expressed as

$$i_{ld} = \bar{i}_{ld} + \tilde{i}_{ld}, \qquad i_{lq} = \bar{i}_{lq} + \tilde{i}_{lq} \tag{2.14}$$

In the above equation, i_{ld}, i_{lq} represents the total active and reactive components, $\bar{i}_{ld}$, $\bar{i}_{lq}$ represent average active and reactive powers, similarly $\tilde{i}_{ld}$, $\tilde{i}_{lq}$ represents the oscillating components. To achieve balanced and sinusoidal source currents with unity power factor, supply has to deliver only fundamental active component of load current. Therefore, a LPF is used to eliminate $\tilde{i}_{ld}$ from i_{ld}. In general, DSATCOM requires active current component to maintain constant voltage across its dc link, otherwise the dc link will collapse after a certain duration. As shown in Fig. 2.11, the difference between the reference and measured dc link voltage is passed through a PI controller and output of it is added to $\bar{i}_{ld}$ to achieve the amplitude of total reference source current.

$$I^*_{sdm} = \bar{i}_{ld} + i_{loss}. \tag{2.15}$$

To achieve unity power factor and load balancing, consider I^*_{sdm} as the reference source current. However, the obtained reference current is in *dq* frame. Therefore, *dq-abc* transformation is used to convert reference currents from *dq* to *abc* frame. The instantaneous currents in *abc*-frame are calculated as,

$$\begin{bmatrix} i^*_{sa} \\ i^*_{sb} \\ i^*_{sc} \end{bmatrix} = \begin{bmatrix} \cos\omega t & -\sin\omega t & 1 \\ \cos(\omega t - 120) & -\sin(\omega t - 120) & 1 \\ \cos(\omega t + 120) & -\sin(\omega t + 120) & 1 \end{bmatrix} \begin{bmatrix} I^*_{sdm} \\ 0 \\ 0 \end{bmatrix}. \tag{2.16}$$

The amplitude of PCC voltage (V_{sm}) is given in (2.1). In voltage control mode, it is required to maintain rated voltage at PCC (V^*_{sm}). To achieve this, difference between the V^*_{sm} and V_{sm} is passed through a PI controller and the output of PI controller (i_{qr}) is used to regulate the PCC voltage. Subtract $\bar{i}_{lq}$ from i_{qr}, which gives us the amplitude of reference reactive component (I^*_{sqm}). The obtained active (I^*_{sdm}) and reactive (I^*_{sqm}) components are converted to *abc* frame using *dq-abc* transformation and they are considered as reference source currents i^*_{sabc} to maintain rated voltage at PCC. Finally, the required reference DSTATCOM currents i^*_{cabc} are obtained by subtracting source currents from load currents.

$$i^*_{cabc} = i_{labc} - i^*_{sabc}. \tag{2.17}$$

Because of its simple structure and fewer calculations, SRF theory has become one of the frequently used reference current extraction method. However, the limitations are requirement of PLL to measure synchronization angle and reduced performance during distortions in supply voltage.

2.2.4 Instantaneous symmetrical component theory (ISCT)

The block diagram representation of reference current generation using instantaneous symmetrical component theory [35] is shown in Fig. 2.12.

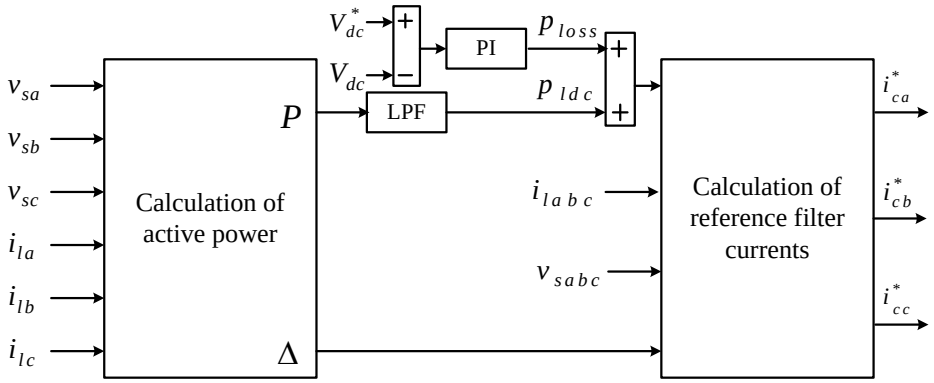


Fig. 2.12 Instantaneous symmetrical component theory (ISCT).

One of the objectives of using DSTATCOM is achieving balanced source currents, which implies that the sum of source currents should always be zero.

$$i_{sa} + i_{sb} + i_{sc} = 0. \tag{2.18}$$

The other objective is, maintaining required power factor angle between voltages and currents at PCC, which implies that,

$$\begin{aligned} \angle v_s &= \angle i_s + \theta \\ \frac{1}{3}\angle(v_{sa} + a v_{sb} + a^2 v_{sc}) &= \frac{1}{3}\angle(i_{sa} + a i_{sb} + a^2 i_{sc}) + \theta \end{aligned} \tag{2.19}$$

where, θ is power factor angle. L.H.S of (2.19) is expressed as,

$$\begin{aligned}
\text{L.H.S} &= \angle\left[\frac{1}{3}\left(v_{sa} + \left(\frac{-1}{2} + j\frac{\sqrt{3}}{2}\right)v_{sb} + \left(\frac{-1}{2} - j\frac{\sqrt{3}}{2}\right)v_{sc}\right)\right] \\
&= \angle\left[\frac{1}{3}\left(\left(v_{sa} - \frac{v_{sb}}{2} - \frac{v_{sc}}{2}\right) + j\frac{\sqrt{3}}{2}\left(v_{sb} - v_{sc}\right)\right)\right] \\
&= \tan^{-1}\frac{(\frac{\sqrt{3}}{2})(v_{sb} - v_{sc})}{\left(v_{sa} - \frac{v_{sb}}{2} - \frac{v_{sc}}{2}\right)} \\
&= \tan^{-1}\frac{K_1}{K_2}
\end{aligned} \tag{2.20}$$

. where, $K_1 = (\frac{\sqrt{3}}{2})(v_{sb} - v_{sc})$, $K_2 = \left(v_{sa} - \frac{v_{sb}}{2} - \frac{v_{sc}}{2}\right)$. Similarly, R.H.S of the equation is expanded as below.

$$\begin{aligned}
\text{R.H.S} &= \angle\left[\frac{1}{3}\left(i_{sa} + \left(\frac{-1}{2} + j\frac{\sqrt{3}}{2}\right)i_{sb} + \left(\frac{-1}{2} - j\frac{\sqrt{3}}{2}\right)i_{sc}\right)\right] + \theta \\
&= \angle\left[\frac{1}{3}\left(\left(i_{sa} - \frac{i_{sb}}{2} - \frac{i_{sc}}{2}\right) + j\frac{\sqrt{3}}{2}\left(i_{sb} - i_{sc}\right)\right)\right] + \theta \\
&= \tan^{-1}\frac{(\frac{\sqrt{3}}{2})(i_{sb} - i_{sc})}{\left(i_{sa} - \frac{i_{sb}}{2} - \frac{i_{sc}}{2}\right)} + \theta \\
&= \tan^{-1}\frac{K_3}{K_4} + \theta
\end{aligned} \tag{2.21}$$

. where, $K_3 = (\frac{\sqrt{3}}{2})(i_{sb} - i_{sc})$, $K_4 = \left(i_{sa} - \frac{i_{sb}}{2} - \frac{i_{sc}}{2}\right)$. Equating (2.20) and (2.21) leading to the following.

$$\tan^{-1}\frac{K_1}{K_2} = \tan^{-1}\frac{K_3}{K_4} + \theta. \tag{2.22}$$

Apply tangent on both sides of (2.22) and the simplified form is,

$$\frac{K_1}{K_2} = \frac{K_3 + K_4\tan\theta}{K_4 - K_3\theta} \tag{2.23}$$

The above equation implies that,

$$K_1K_4 - K_1K_3\tan\theta - K_2K_3 - K_2K_4\tan\theta = 0 \tag{2.24}$$

Substitute the values of K_1, K_2, K_3, and K_4 and simplify (2.24) will give us,

$$\begin{aligned}\{(v_{sb}-v_{sc})+\beta\,(v_{sb}+v_{sc}-2v_{sa})\}\,i_{sa}+\{(v_{sc}-v_{sa})+\beta\,(v_{sc}+v_{sa}-2v_{sb})\}\,i_{sb}\\ +\{(v_{sa}-v_{sb})+\beta\,(v_{sa}+v_{sb}-2v_{sc})\}\,i_{sc}=0\end{aligned} \tag{2.25}$$

where, $\beta = \tan^{-1}(\frac{\theta}{\sqrt{3}})$. (2.25) is modified as,

$$\{(v_{sb}-v_{sc})+\beta A\}\,i_{sa}+\{(v_{sc}-v_{sa})+\beta B\}\,i_{sb}+\{(v_{sa}-v_{sb})+\beta C\}\,i_{sc}=0 \tag{2.26}$$

where, $A = v_{sb}+v_{sc}-2v_{sa}$, $B = v_{sc}+v_{sa}-2v_{sb}$ and $C = v_{sa}+v_{sb}-2v_{sc}$.

Supply has to deliver only average component of load power in order to maintain sinusoidal source currents, which is the third objective of DSTATCOM.

$$v_{sa}i_{sa}+v_{sb}i_{sb}+v_{sc}i_{sc}=P_{lavg}. \tag{2.27}$$

The matrix form of representing equations (2.18), (2.25) and (2.27) is

$$\begin{bmatrix}1 & 1 & 1\\ (v_{sb}-v_{sc})+\beta A & (v_{sc}-v_{sa})+\beta B & (v_{sa}-v_{sb})+\beta C\\ v_{sa} & v_{sb} & v_{sc}\end{bmatrix}\begin{bmatrix}i_{sa}\\ i_{sb}\\ i_{sc}\end{bmatrix}=\begin{bmatrix}0\\ 0\\ P_{lavg}\end{bmatrix}. \tag{2.28}$$

The above equation is of the form, $[A][i] = [P]$. Then, the source current can be calculated using $[i] = [A]^{-1}[P]$.

$$\begin{bmatrix}i_{sa}\\ i_{sb}\\ i_{sc}\end{bmatrix}=\frac{1}{\left(\sum\limits_{j=a,b,c}v_{sj}^2-3v_{s0}^2\right)}\begin{bmatrix}(v_{sa}-v_{s0})+\beta(v_{sb}-v_{sc})\\ (v_{sb}-v_{s0})+\beta(v_{sc}-v_{sa})\\ (v_{sc}-v_{s0})+\beta(v_{sa}-v_{sb})\end{bmatrix}\begin{bmatrix}P_{lavg}\end{bmatrix} \tag{2.29}$$

where, $v_{s0} = \frac{1}{3}(v_{sa}+v_{sb}+v_{sc})$. Finally, the reference filter currents are the difference between load currents and reference source currents, and they are given as,

$$i_{ca}^{*}=i_{la}-i_{sa};\qquad i_{cb}^{*}=i_{lb}-i_{sb};\qquad i_{cc}^{*}=i_{lc}-i_{sc}. \tag{2.30}$$

The unity power factor operation is achieved by assuming $\theta = 0$, which implies β is also

equal to zero. After substituting $\beta = 0$ in (2.29), the new reference currents are given as,

$$\left.\begin{aligned} i^*_{ca} &= i_{la} - \left(\frac{v_{sa} - v_{s0}}{\triangle}\right) P_{lavg} \\ i^*_{cb} &= i_{lb} - \left(\frac{v_{sb} - v_{s0}}{\triangle}\right) P_{lavg} \\ i^*_{cc} &= i_{lc} - \left(\frac{v_{sc} - v_{s0}}{\triangle}\right) P_{lavg} \end{aligned}\right\} \tag{2.31}$$

where, $\triangle = (\Sigma_{j=a,b,c}\ v^2_{sj} - 3v^2_{s0})$. After including the power loss term (P_{loss}), then (2.31) becomes,

$$\left.\begin{aligned} i^*_{ca} &= i_{la} - \left(\frac{v_{sa} - v_{s0}}{\triangle}\right)\left(P_{lavg} + P_{loss}\right) \\ i^*_{cb} &= i_{lb} - \left(\frac{v_{sb} - v_{s0}}{\triangle}\right)\left(P_{lavg} + P_{loss}\right) \\ i^*_{cc} &= i_{lc} - \left(\frac{v_{sc} - v_{s0}}{\triangle}\right)\left(P_{lavg} + P_{loss}\right) \end{aligned}\right\} \tag{2.32}$$

The advantages of this method are elimination of PLL and there is no requirement of complex transformations. However, this control algorithm is not directly applicable under unbalance and distortions in supply voltages.

2.3 Controllers to generate switching pulses

The extracted reference compensator currents using reference current extraction techniques are compared with actual compensator currents to generate switching pulses for DSTATCOM. The performance of any DSTATCOM topology depends on the switching control strategy applied to generate the switching pulses. The important controllers are, hysteresis controllers, linear controllers, sliding mode controllers, predictive controllers and artificial intelligence based controllers [50]–[53]. Among the available controllers pulse width modulation (PWM) based linear controllers, hysteresis controllers are adopted by most of the researchers because of their simple structure and easy implementation.

2.3.1 Pulse width modulation (PWM) controller

In PWM techniques, the reference signal is compared with a carrier signal to generate switching pulses to drive the switches of VSI. In open loop, the output of a single-phase

inverter is controlled by comparing a reference sinusoidal signal with a triangular carrier signal. Similarly, in three-phase VSI applications, three sinusoidal signals with a phase displacement of 120° is considered as reference signals and they are compared with the carrier signal to generate the switching pulses. In current control using DSTATCOM the difference between the reference and actual DSTATCOM currents, is passed through a PI controller and the output of PI is compared with a carrier signal, which gives gating pulses to drive switches of VSI. PWM current controller based switching pulse generation is shown in Fig. 2.13

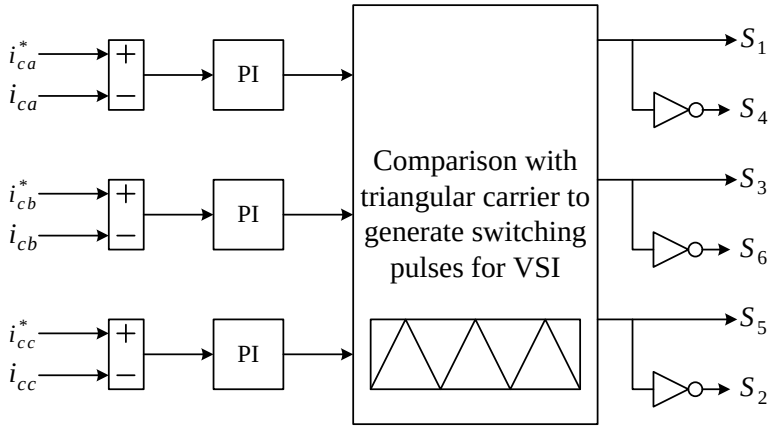


Fig. 2.13 Pulse generation using PWM current controller.

2.3.2 Hysteresis controller

In hysteresis current control, hysteresis band is used to limit the current error within this band, by continuously switching on and off the inverter switches. The pulse generation using hysteresis current controller is explained for a three-phase inverter. If the current error crosses $+h$, upper switch of the leg is turned on to limit the current error below $+h$. Similarly, if the current crosses $-h$, upper switch of the leg is turned off to limit the current between the boundaries. The gate pulses for the lower switches of each leg are obtained by applying complement to gate pulses of upper switch of the same leg. The pictorial representation of hysteresis current controller based switching pulse generation is shown in Fig. 2.14.

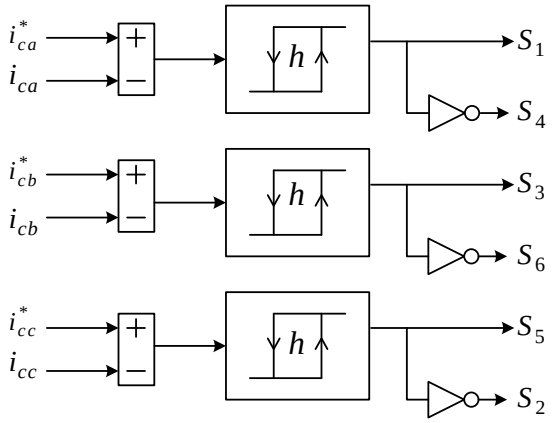


Fig. 2.14 Pulse generation using hysteresis current controller.

2.4 Model predictive control (MPC)

In recent years, model predictive control (MPC) methods have evolved as an alternative to conventional control methods because of its easy implementation, providing good dynamic and steady-state response, and constraints can be easily added to the cost function [54]–[57]. Process control industry is the first field, where MPC is applied. However, the extended development in the area of microprocessors and digital controllers improves the use of MPC techniques in several other areas such as grid-connected inverters, active power filters and motor control. In any control system, the main objective is minimizing the error between reference and actual variable. Similarly, the important objectives in power converters is to minimize the current or voltage errors, reduction in switching frequency and switching losses. The block diagram of MPC is shown in Fig. 2.15. In MPC, initially, one needs to predict the behavior of required control variables for the possible switching states. Calculate the cost function value for each possible prediction. Finally, select a switching state, which minimizes the cost function value. Utilization of MPC methods to the DSTATCOM for power quality improvement mainly depends on minimization of a single constraint cost function, which consists of the difference between the reference and actual filter currents as a control parameter. As mentioned, the advantage of MPC is simple inclusion of additional constraints, which is very helpful to overcome the limitations of DSTATCOMs such as capacitor voltage balancing and switching frequency reduction. These constraints can be easily included in the cost function using weighting factor. A detailed explanation of application of MPC to TPSC and FL-DSTATCOM topologies is explained in Chapters 3 and 4.

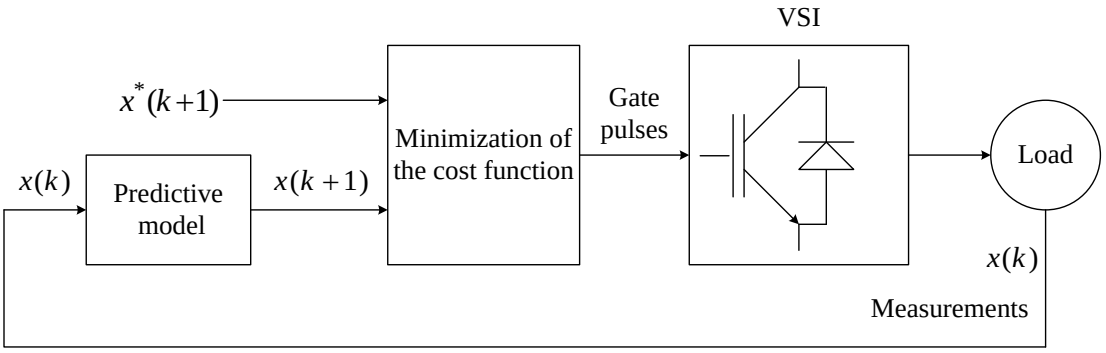


Fig. 2.15 Pulse generation using model predictive control.

2.5 Design of DSTATCOM parameters

The performance of DSTATCOM is depending on various parameters, which includes the dc link voltage, dc link capacitance, interfacing inductance, rating of VSI [25]–[27], [37], [58], [59]. These parameters of the VSI are need to be designed appropriately for satisfactory performance of DSTATCOM.

2.5.1 DC-link voltage (V_{dc})

The selection of dc link voltage have a vital role in any DSTATCOM topology. The value of dc link voltage varies between 1.6 to 2 times of the amplitude of phase voltage to get optimal performance of DSTATCOM [25], [26], [37]. In three leg topology and four leg topology, the dc link voltage is considered as 2 times of the amplitude of phase voltage and it is given as,

$$V_{dc} = \frac{2\sqrt{2}V_{LL}}{\sqrt{3}m_a} \tag{2.33}$$

where, V_{LL} represents the line-line voltage and m_a represents the modulation index. Similarly, in split capacitor topology, each capacitor voltage is considered as 1.6 times of amplitude of phase voltage and it given as

$$V_{dc1} = V_{dc2} = \frac{1.6\sqrt{2}V_{LL}}{\sqrt{3}m_a} \tag{2.34}$$

2.5.2 DC-link capacitor (C_{dc})

The value of dc link capacitance is designed using unit capacitor constant (UCC) [60]. It can be expressed as the ratio of energy stored by the capacitor to the maximum reactive power demanded by the load.

$$UCC = \frac{\frac{1}{2}C_{dc}V_{dc}^2}{Q} \tag{2.35}$$

In the above equation, Q represents the maximum reactive power required by the load. The other way of calculating C_{dc} is using variation of VSI rating during transient conditions. Assume that the rating of the VSI varies from 50% to 200% under transient conditions and the rating is considered as x. Then, the change in energy can be expressed as,

$$\Delta E = \left(2x - \frac{x}{2}\right)nT \tag{2.36}$$

where, n represents the number of cycles under system is in transient condition and T represents the time period. As mentioned in a split capacitor topology, dc link voltage is considered as 1.6 times the amplitude of phase voltage (V_m), therefore under transient condition dc link voltage varies from 1.4 to 1.8 times V_m [25]–[27]. Then, the following relation is obtained.

$$\frac{1}{2}C_{dc}[(1.8V_m)^2 - (1.4V_m)^2] = (2x - \frac{x}{2})nT \tag{2.37}$$

Simplify (2.37),

$$C_{dc} = \frac{2(2x - \frac{x}{2})nT}{(1.8V_m)^2 - (1.4V_m)^2} \tag{2.38}$$

2.5.3 Interfacing inductor (L_f)

In DSTATCOM topology, interfacing inductor is used to eliminate the switching frequency harmonic from the VSI injected current. The switching dynamics of the hysteresis controller is used to find the interfacing inductance (L_f) value [61]. Fig. 2.16 shows the switching dynamics of hysteresis current controller. In this figure, solid line represents the actual filter current, and the difference between the upper and lower limits is considered as hysteresis band ($\pm h$), and the dotted line represents the reference filter current.

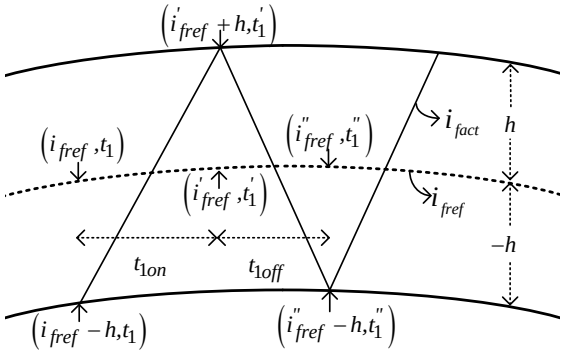


Fig. 2.16 Switching dynamics of hysteresis controller for *L*-filter design.

From Fig. 2.16, the rate of change of currents during increasing and decreasing slopes are given as,

$$\left.\begin{aligned}\frac{\mathrm{d}i_{fact}}{\mathrm{d}t_{on}} &= \frac{(i'_{fref}-i_{fref})+2h}{t_{on}}\\ \frac{\mathrm{d}i_{fact}}{\mathrm{d}t_{off}} &= \frac{(i''_{fref}-i'_{fref})-2h}{t_{off}}\end{aligned}\right\} \tag{2.39}$$

During increasing slope the dc link voltage is considered as positive and during decreasing slope it is considered as negative. Apply KVL from the output of VSI to PCC will give us the following equation,

$$\left.\begin{aligned}m_a V_{dc}-V_m\sin\omega t &= L_f\frac{\mathrm{d}i_{fact}}{\mathrm{d}t_{on}}+R_f i_{fact}\\ -m_a V_{dc}-V_m\sin\omega t &= L_f\frac{\mathrm{d}i_{fact}}{\mathrm{d}t_{off}}+R_f i_{fact}\end{aligned}\right\} \tag{2.40}$$

where, m_a represents the modulation index, R_f is internal resistance of inductor L_f. The low value of R_f is leading to the elimination of voltage drop across it in the (2.40). Calculate t_{on} and t_{off}, by simplifying (2.39) and (2.40).

$$\begin{aligned}t_{on} &= \frac{2hL_f}{m_a V_{dc}-V_m\sin\omega t-i_{fact}R_f}\\ t_{off} &= \frac{2hL_f}{m_a V_{dc}+V_m\sin\omega t+i_{fact}R_f}\end{aligned} \tag{2.41}$$

From (2.41), the switching frequency (f_{sw}) is derived as,

$$f_{sw}=\frac{1}{t_{on}+t_{off}}=\frac{1}{4hL_f}\Big(m_a V_{dc}-\frac{V_m^2}{m_a V_{dc}}\sin^2\theta\Big). \tag{2.42}$$

It is observed from (2.42) that, the switching frequency becomes maximum when θ value is zero. Therefore, the inductance value for maximum switching frequency is

given as,

$$L_f = \frac{m_a V_{dc}}{4h f_{sw,max}}, \tag{2.43}$$

where, $f_{sw,max}$ is maximum switching frequency. From the above equation it is observed that the value of L_f depends on dc link voltage, maximum switching frequency and hysteresis band width. In general, h value is considered as (5)% of rated filter current.

2.6 Summary

In this chapter, the advantages and limitations of various DSTATCOM topologies such as three HB, three leg DSTATCOM, TPSC and FL-DSTATCOM are discussed. Then reference current extractions namely, UTT, IRPT, SRF and ISCT are explained. Conventional controllers such as PWM and hysteresis are discussed followed by modern control technique, namely MPC. Finally, the design procedure of various parameters of the DSTATCOM are discussed.

CHAPTER 3

Model Predictive Control of TPSC DSTATCOM with Simplified Weighting Factor Selection Using VIKOR Method for Power Quality Improvement

Power quality improvement using model predictive control (MPC) involves, the selection of a inverter switching state which minimizes the difference between reference and actual DSTATCOM currents. However, higher switching frequency is the limitation of MPC and voltage divergence of dc link capacitors in case of three-phase split-capacitor (TPSC) DSTATCOM. To address these problems, two additional constraints are included in the cost function using weighting factors. Between them, one is to suppress the voltage divergence and other is to reduce the switching frequency. Optimal selection of switching state for minimization of a multi-constraint cost function depends on the weighting factor, however, its tuning is a challenging task. In this chapter, the tuning of weighting factor is achieved using VlseKriterijumska Optimizacija I Kompromisno Resenje (VIKOR) method and it further selects the optimal switching state based on a specific measure of closeness to the ideal solution and multi-criteria ranking index. The advantages of the proposed control algorithm are compensation of power quality issues, balancing the dc link voltages, switching frequency reduction of inverter and simplification of weighting factor tuning.

3.1 Introduction

In recent years, MPC methods have been used in many research areas, due to its ease in implementation, providing good dynamic and steady-state response, and easy addition of constraints to the cost function [54], [55]. Extended development in the area of microprocessors and digital controllers has improved the use of MPC techniques in several areas such as grid connected inverters, active power filters and motor control [56], [57]. Application of MPC methods to DSTATCOM for power quality improvement mainly

depends on, minimization of a single constraint cost function which consists of the difference between reference and actual DSTATCOM current as a control parameter [26], [62]. In this chapter, the required reference DSTATCOM currents are extracted using conductance factor based method [63].

Distinct leakage currents or asymmetrical charging of dc link capacitors during compensation of loads with higher unbalance factor initiate, voltage unbalance across the capacitors of TPSC topology, which deteriorate the DSTATCOM performance [64], [65]. In the literature, switching of the inverter is adjusted to overcome this limitation, however, it increases control complexity [65]–[67]. As mentioned earlier, the advantage of MPC is, easy inclusion of control parameters; therefore voltage unbalance problem can be eliminated by considering the difference between capacitor voltages as an additional control parameter. This additional control parameter is included in the cost function using a weighting factor. Similarly, switching frequency related to control effort is high using MPC, and it increases the switching losses. This higher switching frequency limitation of MPC is controlled by considering the difference between the present and previous switching state as a control parameter and it is added to the cost function using another weighting factor. The selection of suitable switching state during multi-constraint case is a challenging task and it completely depends on the weighting factor [68]. Therefore, the simplification of weighting factor tuning is necessary and in this work, it is achieved using a multi-criteria decision making (MCDM) method, namely, VIKOR [69]. In this method, initially ranking is given to all the cost fucntion values and selection from the available set of alternatives is done in the presence of multi-criteria. Then, based on the specific measure of closeness to the ideal solution and multi-criteria ranking index, it selects the optimal solution from the available alternatives.

3.2 Proposed MPC with VIKOR method

The schematic diagram of TPSC DSTATCOM connected distribution system is shown in Fig. 3.1. Here, DSTATCOM is connected through an interfacing inductor (L_f) at the point of common coupling (PCC). Interfacing inductor is used to eliminate ripples from the DSTATCOM currents and the internal resistance of L_f is represented as

R_f. The source and load neutral conductors are connected to the mid-point of dc link which eliminates the requirement of additional switches like four leg DSTATCOM (FL-DSTATCOM) topology to compensate the unbalanced load currents. In Fig. 3.1, i_{sa}, i_{sb} and i_{sc} represent source currents. i_{la}, i_{lb} and i_{lc} represent load currents and i_{ca}, i_{cb} and i_{cc} represent DSTATCOM currents. PCC voltages are represented by v_{sa}, v_{sb} and v_{sc}. Inverter phase voltages are represented by v_{ca}, v_{cb} and v_{cc}. Source, load and DSTATCOM neutral currents are represented by i_{sn}, i_{ln} and i_{cn} respectively.

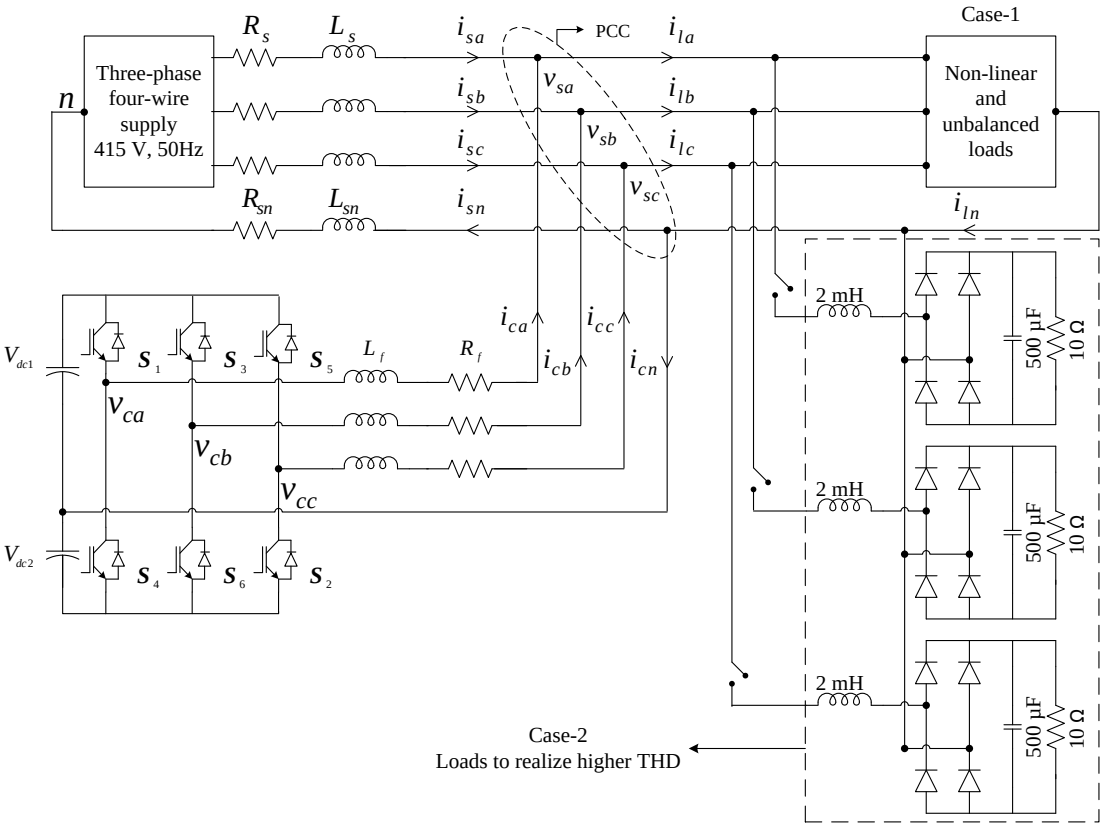


Fig. 3.1 Schematic diagram of DSTATCOM connected distribution system.

The design of various parameters of DSTATCOM such as dc link voltage, dc link capacitance and interfacing inductor are explained below.

DC link voltage (V_{dc1}, V_{dc2}):

The voltage across each individual dc link capacitor is considered as 1.6 times of peak value of phase voltage [25]. The dc bus voltage is calculated as

$$V_{dc1} = V_{dc2} = \frac{1.6\sqrt{2}V_{LL}}{\sqrt{3}m} \tag{3.1}$$

where, V_{LL} is the line to line voltage and m is the amplitude modulation index, usually

it is considered as unity.

DC link capacitance (C_{dc1}, C_{dc2}):

The capacitance value of each dc link capacitor depends on, kVA (X) of the inverter, allowed voltage change (1.4 to 1.8 times of peak voltage), fundamental time period (T) and the number of cycles with transient operation (n) [25]. Therefore, the dc link capacitance is given as:

$$C_{dc1} = C_{dc2} = \frac{2(2X - \frac{X}{2})nT}{(1.8V_m)^2 - (1.4V_m)^2}. \tag{3.2}$$

Interfacing Inductor (L_f):

The value of interfacing inductance mainly depends on acceptable ripple current (ΔI), maximum switching frequency (f_{smax}) and peak value of phase voltage (V_m) [25].

$$L_f = \frac{1.6V_m}{4\Delta I f_{smax}}. \tag{3.3}$$

During simulation studies, supply voltage is considered as 415 V, X = 25 kVA, n = 0.5, T = 0.02 s, ΔI = 1.6 A, and f_{smax} = 20 kHz. Therefore, using (3.1), (3.2) and (3.3) the obtained value of dc link voltage $V_{dc1} = V_{dc2}$ = 540 V, the dc link capacitance $C_{dc1} = C_{dc2}$ = 5100 μF. The calculated value of L_f is 4.33 mH and in this chapter it is considered as 5 mH.

Similarly, for experimental studies, V_{LL} is considered as 50 V, X = 300 VA, n = 0.5, T = 0.02 s, ΔI = 0.4 A, and f_{smax} = 5 kHz . Because of the rating constraints, the experimental setup is developed at lower voltage and power ratings. Using (3.1), the obtained value of dc link voltage $V_{dc1} = V_{dc2}$ = 70 V. Using (3.2), the calculated value of dc link capacitance is 4220 μF. Therefore, the nearest available rating 4700 μF is selected for both capacitors ($C_{dc1} = C_{dc2}$ = 4700 μF). Using (3.3), the value of L_f is obtained as 8.164 mH and in this chapter it is considered as 9 mH.

The block diagram of the complete control algorithm is shown in Fig. 3.2. There are mainly four steps involved in the implementation of MPC with VIKOR method for DSTATCOM control.

1. Reference current extraction using conductance factors. In this, sensed PCC volt-

ages, load currents and dc link voltage are used to extract reference compensator currents (i_c^*) using conductance factor method [63].

2. Predictive model of TPSC DSTATCOM is used to estimate the compensator currents at $(k+1)^{th}$ instant (i.e., $i_c(k+1)$).

3. Applying Lagrange's extrapolation, to calculate reference DSTATCOM currents at $(k+1)^{th}$ instant (i.e., $i_c^*(k+1)$) and cost function formation.

4. Selection of optimal switching state from available switching states using VIKOR method.

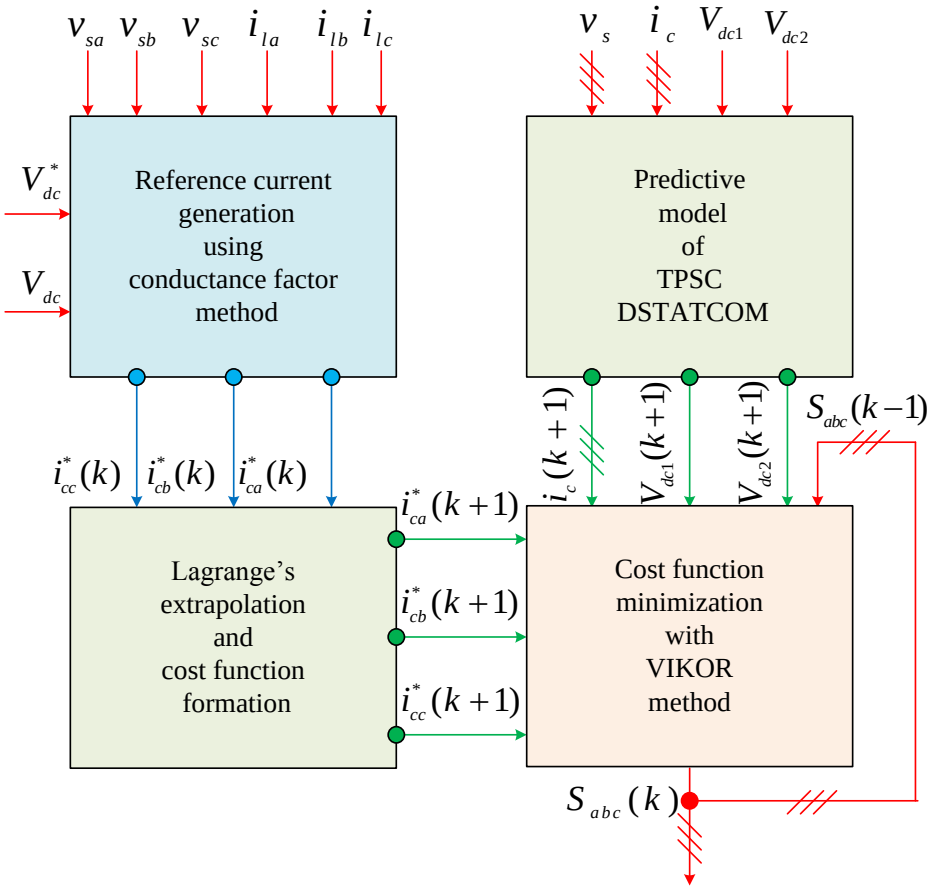


Fig. 3.2 Proposed MPC algorithm with VIKOR method.

3.2.1 Reference current extraction using conductance factor method

The main objective of using TPSC DSTATCOM is to achieve, balanced and sinusoidal source currents which are also in-phase with the voltages at PCC. Fig. 3.3 shows, conductance factor based reference current extraction method which is used in the proposed

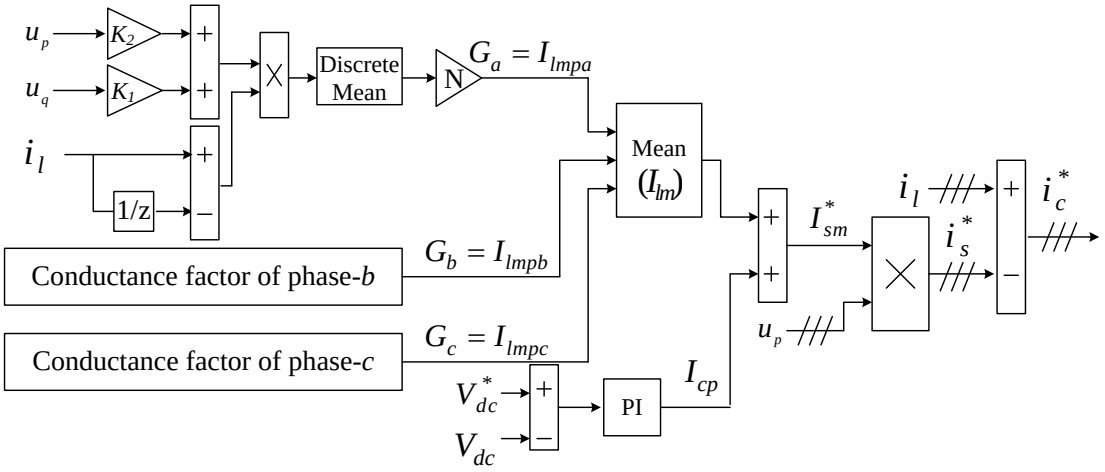


Fig. 3.3 Reference current extraction using conductance factor method.

work, to extract the fundamental in-phase component of load currents [63]. To implement this control algorithm, it is required to sense load currents, DSTATCOM currents, PCC voltages, individual voltages of the dc link capacitors and complete dc link voltage. In-phase and quadrature unit vectors, which are essential to implement the control algorithm are calculated from sensed PCC voltages. In-phase unit vectors are expressed as,

$$u_{pa} = \frac{v_{sa}}{V_{sm}}; \quad u_{pb} = \frac{v_{sb}}{V_{sm}}; \quad u_{pc} = \frac{v_{sc}}{V_{sm}} \tag{3.4}$$

where, V_{sm} represents the amplitude of phase voltage at PCC and is given as [63],

$$V_{sm} = \sqrt{\frac{2}{3}(v_{sa}^2 + v_{sb}^2 + v_{sc}^2)}. \tag{3.5}$$

Similarly, quadrature unit vectors are calculated as,

$$u_{qa} = \frac{-u_{pb} + u_{pc}}{\sqrt{3}}; \quad u_{qb} = \frac{3u_{pa} + u_{pb} - u_{pc}}{2\sqrt{3}}; \quad u_{qc} = \frac{-3u_{pa} + u_{pb} - u_{pc}}{2\sqrt{3}}. \tag{3.6}$$

Load current is a combination of active, reactive, harmonic and dc component and is given by,

$$i_l(t) = i_{lp}(t) + i_{lq}(t) + i_h(t) + I_{dc}. \tag{3.7}$$

(3.7) can also be written as,

$$i_l(t) = Gv_t(t) + B\int v_s(t)\mathrm{d}t + i_h(t) + I_{dc} \tag{3.8}$$

where, G is conductance and B is susceptance. The value of G is obtained by taking the derivative of (3.8) using trapezoidal rule [63].

$$i_{l(j)} - i_{l(j-1)} = G(v_{t(j)} - v_{s(j-1)}) + \frac{T_s}{2}(v_{s(j)} - v_{s(j-1)})B + (i_{h(j)} - i_{h(j-1)}). \tag{3.9}$$

The matrix form representation of (3.9) is

$$\begin{bmatrix} v_{s1} - v_{s0} & \frac{T_s}{2}(v_{s1} + v_{s0}) & i_{h1} - i_{h0} \\ \vdots & \vdots & \vdots \\ v_{sN} - v_{s(N-1)} & \frac{T_s}{2}(v_{sN} + v_{s(N-1)}) & i_{hN} - i_{h(N-1)} \end{bmatrix}_{N\times 3} \begin{bmatrix} G \\ B \\ 1 \end{bmatrix}_{3\times 1} = \begin{bmatrix} i_{l1} - i_{l0} \\ \vdots \\ i_{lN} - i_{l(N-1)} \end{bmatrix}_{N\times 1} \tag{3.10}$$

where, T_s is the sampling time and N is the ratio of fundamental time period to sampling time. (3.10) is of the form PX=Q. Then the value of G is obtained by computing $X = (P^T P)^{-1} P^T Q$ and is given as [63],

$$G(t) = \frac{\sum_{j=1}^{N} (i_{l(j)} - i_{l(j-1)})(v_{s(j)} - v_{s(j-1)})}{\sum_{j=1}^{N} (v_{s(j)} - v_{s(j-1)})^2}. \tag{3.11}$$

After finding $G(t)$, fundamental active component of load current can be written as,

$$i_{lp}(t) = G(t)v_s(t). \tag{3.12}$$

In general, fundamental active component of load current is the product of its peak amplitude (I_{lmp}) and unit vector (u_p) which is in-phase with the voltage at PCC.

$$i_{lp}(t) = I_{lmp}u_p. \tag{3.13}$$

After comparing (3.13) with (3.12), it is found that, the peak amplitude of fundamental active component of load current (I_{lmp}) is same as the conductance factor (G), by replacing voltage (v_s) in (3.11) and (3.12) with in-phase unit vector (u_p). Therefore,

$$I_{lmp}(t) = G(t) = \frac{\sum_{j=1}^{N} (i_{l(j)} - i_{l(j-1)})(u_{p(j)} - u_{p(j-1)})}{\sum_{j=1}^{N} (u_{p(j)} - u_{p(j-1)})^2}. \tag{3.14}$$

Riemann integral is used to simplify (3.14) and the simplified equation is given as [63],

$$I_{lmp}(t) = \sum_{j=1}^{N}(i_{l(j)} - i_{l(j-1)})(u_{q(j)} * K_1 + u_{p(j)} * K_2), \tag{3.15}$$

where, $K_1 = \dfrac{\cos(\omega T_s/2)}{N \sin(\omega T_s/2)}$, $K_2 = \dfrac{1}{N}$.

After computing the conductance factors for each phase, the average (I_{lm}) of these three values will give fundamental active component of load current which is used to achieve balanced source currents even though the load currents are unbalanced. VSI draw active power, to maintain constant voltage across its dc link and the dc link voltage of the self supported dc bus is regulated using a PI controller. The input for PI controller is the difference between the reference dc link voltage and the measured dc link voltage. The output of PI (I_{cp}) is added to the fundamental active component of load current to obtain the peak amplitude of reference source current ($I^*_{sm} = I_{lm} + I_{cp}$). The reference source current is obtained by multiplying the amplitude of source current with in-phase unit vector ($i^*_s = I^*_{sm} u_p$). Then, the reference DSTATCOM current is the difference between measured load current and the reference source current.

$$i^*_c = i_l - i^*_s. \tag{3.16}$$

After finding the reference currents, model of the DSTATCOM is used to predict the future values of DSTATCOM currents and these two currents are used to form the required cost fucntion.

3.2.2 Predictive model of TPSC DSTATCOM

In this chapter, TPSC based VSI is used to implement DSTATCOM and there are only 8 switching states available for this topology. The dynamic model of DSTATCOM is used to predict the future value of DSTATCOM currents for every available switching state, which mainly depends on PCC voltages, currents and voltages of DSTATCOM. Then, compare the predicted current of every switching state with reference current and select a state which gives the minimum error. From Fig. 3.1, the voltage at the inverter terminal is equal to sum of voltage drop across the inductor along with its internal

resistance and voltage at PCC i.e.,

$$v_c = i_c R_f + L_f \frac{\mathrm{d}i_c}{\mathrm{d}t} + v_s. \tag{3.17}$$

Solving (3.17) for $\frac{\mathrm{d}i_c}{\mathrm{d}t}$,

$$\frac{\mathrm{d}i_c}{\mathrm{d}t} = \left(\frac{v_c - v_s}{L_f}\right) - i_c \frac{R_f}{L_f}. \tag{3.18}$$

The forward Euler approximation method is used to replace $\frac{\mathrm{d}i_c}{\mathrm{d}t}$ in (3.18), and it is represented as,

$$\frac{\mathrm{d}i_c}{\mathrm{d}t} = \frac{i_c(k+1) - i_c(k)}{T_s}. \tag{3.19}$$

The discrete time representation of (3.18) is given as follows:

$$\frac{i_c(k+1) - i_c(k)}{T_s} = \left(\frac{v_c(k) - v_s(k)}{L_f}\right) - i_c(k)\frac{R_f}{L_f}. \tag{3.20}$$

From (3.20), DSTATCOM current at $(k+1)^{th}$ instant is,

$$i_c(k+1) = (v_c(k) - v_s(k))\frac{T_s}{L_f} + i_c(k)\left(1 - \frac{R_f T_s}{L_f}\right). \tag{3.21}$$

In (3.21), $v_c(k)$ represents the voltage at the inverter terminals, which mainly depends on the switching states of VSI, $v_s(k)$ represents the voltage at PCC and $i_c(k)$ represents the measured DSTATCOM current. The various switching combinations and the voltages available at the terminals of the VSI are given in Table. 3.1. The DSTATCOM currents at $(k+1)^{th}$ instant are calculated by substituting the voltages and currents in (3.21) with respective values. As discussed, the limitation of TPSC DSTATCOM is voltage divergence across the two capacitors of dc link. To overcome this limitation, it is required to

Table. 3.1 Switching states with respective voltages of TPSC DSTATCOM

State	S_1	S_3	S_5	v_{ca}	v_{cb}	v_{cc}
1	0	0	0	$-V_{dc2}$	$-V_{dc2}$	$-V_{dc2}$
2	1	0	1	V_{dc1}	$-V_{dc2}$	V_{dc1}
3	1	1	0	V_{dc1}	V_{dc1}	$-V_{dc2}$
4	0	1	0	$-V_{dc2}$	V_{dc1}	$-V_{dc2}$
5	0	1	1	$-V_{dc2}$	V_{dc1}	V_{dc1}
6	0	0	1	$-V_{dc2}$	$-V_{dc2}$	V_{dc1}
7	1	0	0	V_{dc1}	$-V_{dc2}$	$-V_{dc2}$
8	1	1	1	V_{dc1}	V_{dc1}	V_{dc1}

find the voltage across the capacitors and include the difference between them as a control parameter in the cost function. Current flowing through each capacitor is a function of dc link voltage and is given as:

$$i_{dc} = C_{dc}\frac{\mathrm{d}V_{dc}}{\mathrm{d}t}. \tag{3.22}$$

The dc link voltages in discrete form is obtained by applying forward Euler approximation to (3.22) and it is given as follows:

$$\frac{V_{dc}(k+1) - V_{dc}(k)}{T_s} = \frac{i_{dc}(k)}{C_{dc}}. \tag{3.23}$$

Voltage across each capacitor is given by:

$$\begin{aligned} V_{dc1}(k+1) &= V_{dc1}(k) + i_{dc1}(k)\frac{T_s}{C_{dc}}, \\ V_{dc2}(k+1) &= V_{dc2}(k) + i_{dc2}(k)\frac{T_s}{C_{dc}}. \end{aligned} \tag{3.24}$$

Therefore, it is necessary to calculate current flowing through the capacitor to find the voltage across each capacitor. The values of i_{dc1} and i_{dc2} depends on the state of the switch and current flowing through each phase and it is given by:

$$\begin{aligned} i_{dc1}(k) &= -(S_a i_{ca} + S_b i_{cb} + S_c i_{cc}), \\ i_{dc2}(k) &= (\overline{S_a} i_{ca} + \overline{S_b} i_{cb} + \overline{S_c} i_{cc}). \end{aligned} \tag{3.25}$$

In (3.25), S_a, S_b and S_c represents the switching states of the upper switches. Similarly, $\overline{S_a}$, $\overline{S_b}$ and $\overline{S_c}$ represents the switching states of the lower switches of three-phase VSI of TPSC DSTATCOM.

3.2.3 Lagrange's extrapolation and cost function formation

The cost function of the proposed control algorithm consists of three terms. The first term in the cost function is the difference between the reference and actual DSTATCOM currents at $(k+1)^{th}$ state. The value of $i_c(k+1)$ is given in (3.21) and $i_c^*(k+1)$ is calculated from $i_c^*(k)$ using second order Lagrange's extrapolation [26]. The derivation (3.26) using

second order Lagrange's extrapolation is explained in Appendix A.

$$i_c^*(k+1) = 3i_c^*(k) - 3i_c^*(k-1) + i_c^*(k-2). \tag{3.26}$$

Therefore, the first term in the cost function is considered as,

$$C_1 = \sum_{j=a,b,c} |\, i_{cj}^*(k+1) - i_{cj}(k+1)|. \tag{3.27}$$

The second term in the cost function is the difference between the voltages across two capacitors of the dc link, which is used to decrease the deviation in voltage.

$$C_2 = |\, V_{dc1}(k+1) - V_{dc2}(k+1)|. \tag{3.28}$$

The main limitation of using MPC is higher switching frequency and it is reduced by adding the difference between present and previous switching state as an additional control parameter to the cost function.

$$C_3 = \sum_{j=a,b,c} |\, (S_j(k) - S_j(k-1))|. \tag{3.29}$$

In (3.29), the value of $S_j(k-1)$ is obtained by considering as a feedback variable. Therefore, using conventional predictive control method, the complete cost function is formed by adding three individual cost functions using weighting factors:

$$C = C_1 + \lambda_1 C_2 + \lambda_2 C_3 \tag{3.30}$$

where, λ_1 and λ_2 are the weighting factors.

However, tuning of weighting factors is a challenging task and also the number of weighting factors will increase by increasing the number of constraints in the cost function. Therefore, the complexity in the tuning is reduced by choosing a MCDM method namely VIKOR. This method initially gives ranking and select the optimal switching state from the available switching states and the selected state is applied to the DSTATCOM.

3.2.4 Application of VIKOR method for selecting optimal switching state

Step 1: In (3.30), C_1 represents the cost function belongs to current control, C_2 represents the cost function belongs to voltage balancing and C_3 is for switching frequency reduction. In this method, initially cost functions C_1, C_2 and C_3 are individually evaluated for each available switching state and those values are represented as follows:

$$C_{IJ} = \begin{bmatrix} C_{11} & C_{12} & C_{13} \\ C_{21} & C_{22} & C_{23} \\ C_{31} & C_{32} & C_{33} \\ C_{41} & C_{42} & C_{43} \\ C_{51} & C_{52} & C_{53} \\ C_{61} & C_{62} & C_{63} \\ C_{71} & C_{72} & C_{73} \\ C_{81} & C_{82} & C_{83} \end{bmatrix}_{8\times 3} \tag{3.31}$$

The order of matrix C_{IJ} depends on the number of available switching states and the number of control parameters.

Step 2: After evaluating the cost functions for each switching state, select the positive and negative best value for each cost function. Positive best value represents the maximum and negative best value represents the minimum value in each column of C_{IJ}. The objective of this method is to minimize the error, therefore the negative best value is considered as the ideal solution.

$$\begin{aligned} C_1^- &= \min(C_{i1}); \quad C_2^- = \min(C_{i2}); \quad C_3^- = \min(C_{i3}), \\ C_1^+ &= \max(C_{i1}); \quad C_2^+ = \max(C_{i2}); \quad C_3^+ = \max(C_{i3}). \end{aligned} \tag{3.32}$$

Step 3: Utility measure S_i represents the average scores and regret measure R_i represents the worst group scores and they are represented as follows.

$$S_i = \sum_{j=1}^{3} w_j \frac{C_j^- - C_{ij}}{C_j^- - C_j^+} \tag{3.33}$$

$$R_i = \max_j \left[w_j \frac{(C_j^- - C_{ij})}{(C_j^- - C_j^+)} \right] \tag{3.34}$$

In (3.33) and (3.34), w_j represents the weight assigned to the j^{th} cost function. According to VIKOR method the sum of all weights must be equal to one i.e.,

$$\sum_{j=1}^{3} w_j = 1 \tag{3.35}$$

Step 4: The last step in this method is the selection of optimal switching state from available switching states using VIKOR index (Q). The value of Q is calculated using,

$$Q_i = m\left[\frac{(S_i - S^-)}{(S^+ - S^-)}\right] + (1-m)\left[\frac{(R_i - R^-)}{(R^+ - R^-)}\right] \tag{3.36}$$

where, the superscripts '$-$' represents the minimum value and '$+$' represents the maximum value and usually the group utility factor 'm' is set to be 0.5. Q is estimated for each switching state and the state which is giving the minimum Q will be the optimal switching state that has to be applied at next instant for DSTATCOM control. For example, Table. 3.2 shows the values of VIKOR index (Q) for all the switching states during one sample time. Among all the states, the switching state '7' is giving the minimum Q, therefore it will be applied in the next instant (row is shown in bold letters).

Table. 3.2 Selection of optimal switching state using Q

State	C_1	C_2	C_3	S	R	Q
1	6.2399	0.3178	2	0.6019	0.2667	0.5546
2	3.4657	0.3133	1	0.246	0.1333	0.2211
3	7.3465	0.3089	2	0.6107	0.3107	0.6066
4	10.1207	0.3133	3	0.9667	0.5	1
5	9.4463	0.3089	2	0.754	0.454	0.8368
6	5.5656	0.3133	1	0.3893	0.1893	0.3577
7	**2.7913**	**0.3089**	**0**	**0.0333**	**0.0333**	**0**
8	6.6721	0.3044	1	0.3981	0.2647	0.4433

3.3 Simulation studies

Various parameters of the distribution system and DTSTACOM which are required to implement the proposed control algorithm are given in Table. 3.3. Three different loads are considered for simulation studies. Load-1 is a combination of three single-phase diode bridge rectifiers with different RL values at its dc side; load-2 is a three-phase balanced RL load and load-3 is a combination of three single-phase diode bridge

rectifiers with equal *RC* values at its dc side. Using these three loads, two different case studies are formed to analyze the performance of the proposed control algorithm. In case-1, during 1 to 1.75 s load-1 and load-2 are connected to the distribution system, which draw non-linear and unbalanced load currents. During 1.75 to 3 s load-2 is removed and it is again connected at 3 s to analyze the dynamic performance. In case-2, load-3 is connected to analyze the performance during compensation of loads with higher THD values. As mentioned, the cost function of the proposed control algorithm consists of three individual control parameters. However, to understand the efficacy of the proposed control algorithm, dc link voltages and switching frequencies are shown without and with considering their control parameters in cost function.

Table. 3.3 Simulation parameters

Parameter	Value
System voltage	415 V
Feeder impedance (Z_s)	0.07 Ω, 0.2 mH
Interfacing inductor (L_f)	5 mH (R_f = 0 Ω)
DC link voltage (V_{dc})	1080 V
DC capacitor (C_{dc1}, C_{dc2})	5100 μF
w_1, w_2 and w_3	0.5, 0.1 and 0.4
PI controller	k_p = 0.45, k_i = 4.5
Non-linear and unbalanced load (Three single-phase diode bridge rectifiers) (Load-1)	6 Ω, 150 mH (phase-*a*) 5 Ω, 150 mH (phase-*b*) 4 Ω, 150 mH (phase-*c*)
Three-phase balanced linear load (Load-2)	15 Ω, 30 mH (on each phase)
Loads with higher THD (Load-3)	Three single-phase diode bridge rectifiers feeding parallel connection of 10 Ω, 500 μF (on each phase)
Sampling time (T_s)	10 μs

3.3.1 Performance during compensation of non-linear and unbalanced loads

As mentioned earlier, compensation of loads with higher unbalance factor are leading to unequal flow of currents in the dc link which results in voltage across one capacitor continuously rising, and the other to fall. Fig. 3.4 shows the complete dc link voltage (V_{dc}) and the voltage across two capacitors (V_{dc1} and V_{dc2}). It is observed that the complete dc link voltage is maintained constant with respect to the reference value, however, the individual voltages diverge during load changes due to unequal charging

and discharging currents.

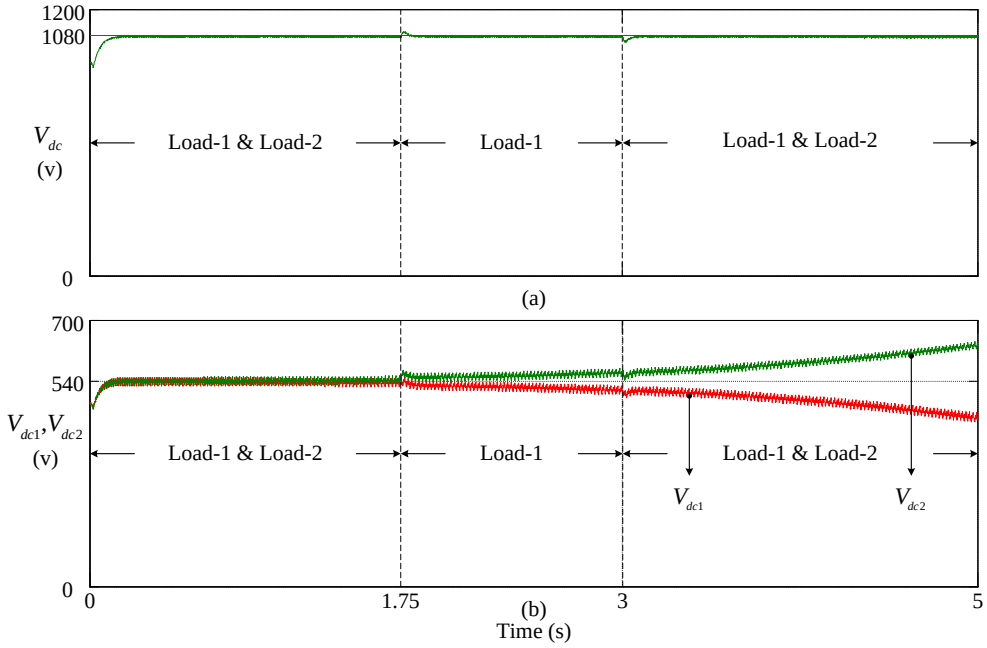
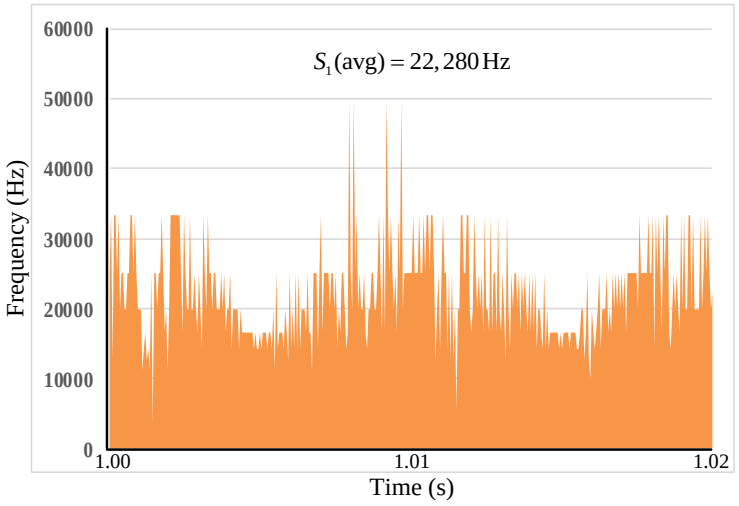


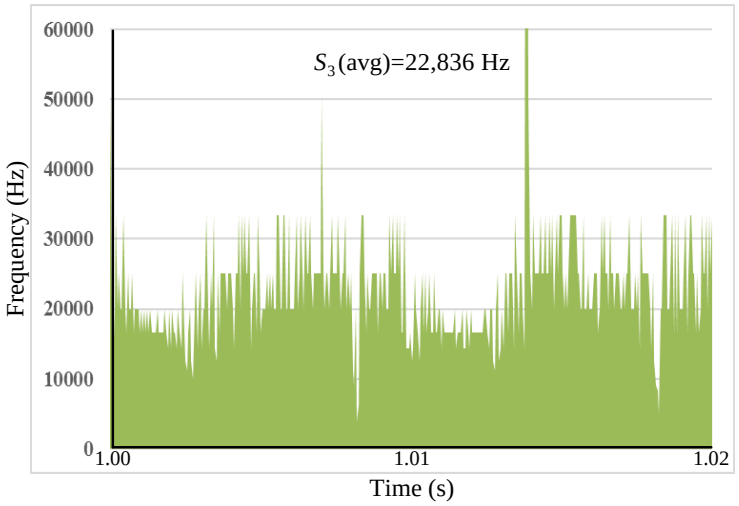
Fig. 3.4 Without adding additional constraints (a) Voltage across complete dc link, and (b) Voltage across individual capacitors.

The average switching frequency is estimated from instantaneous switching frequencies which are calculated by measuring the time period of every switching cycle in one fundamental time period. The calculated switching frequency of MPC method without adding switching frequency constraint in the cost function are 22,280 Hz, 22,836 Hz, and 22,100 Hz for each leg and they are illustrated in Fig. 3.5. These capacitor voltage divergence and higher switching frequency limitations are tackled by adding them as additional control parameters to the cost function along with DSTATCOM currents. Fig. 3.6 shows PCC voltage, source current, load current, DSTATCOM current, load and source neutral currents, after adding all control parameters to the cost function. As mentioned, at 1.75 s three-phase balanced linear load is removed and it is observed from Fig. 3.6 that, the transient performance using the proposed method is satisfactory. It is also observed that the source currents are balanced and sinusoidal even though the load currents are non-linear and unbalanced. Unbalanced loads cause the flow of neutral current, but the compensator is not allowing it through the source neutral conductor which is shown in Fig. 3.6.

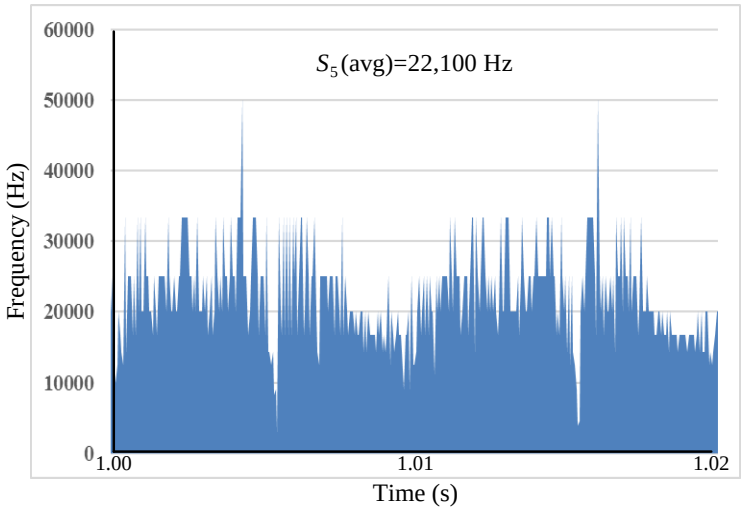
The rms values of unbalanced and non-linear load currents are 41.94 A, 47.23 A and 54.92 A with THDs 21.4%, 24.87% and 25.5% for phase-*a*, phase-*b* and phase-*c* respectively. However, the rms values of source currents are 42.5 A, 42.67 A and 42.45



(a)



(b)



(c)

Fig. 3.5 Average switching frequency without adding additional constraints (a) S_1 (b) S_3, and (c) S_5.

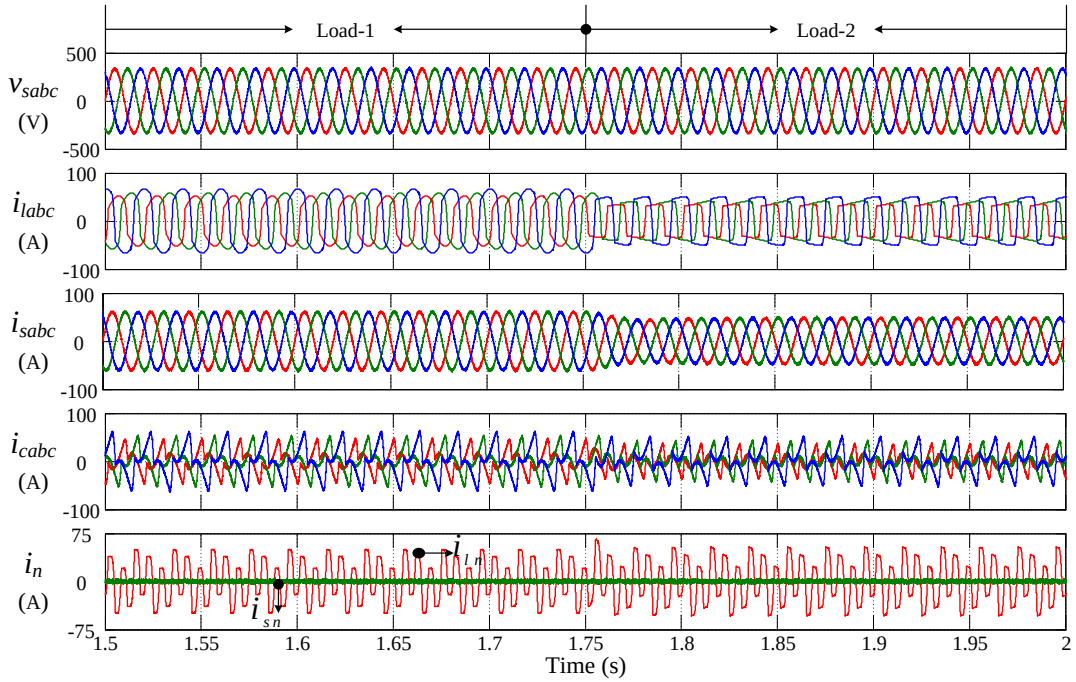


Fig. 3.6 Simulation results using proposed control algorithm.

A, which indicate they are balanced and THD values 2.42%, 2.41% and 2.46% indicate they are sinusoidal. Fig. 3.7 shows the complete dc link voltage and individual capacitor voltages and it is observed that, after adding voltage difference between two capacitors as a cost function, the complete dc link voltage is maintained with respect to its reference value and individual capacitor voltages are also balanced.

Fig. 3.8 shows the average switching frequencies after including additional constraints in the cost function. From this figure it is observed that the average switching frequency is reduced using proposed method and the reduced switching frequencies are 12,875 Hz, 12,652 Hz and 12,929 Hz for S_1, S_3 and S_5 respectively. Fig. 3.9 shows the tracking of compensator current and switching pulses for one fundamental time period. It is observed that, after adding switching frequency reduction constraint in the cost function, the switching frequency is reduced. The reduction in switching frequency causes slight increase in tracking error which is also shown in Fig. 3.9. Table. 3.4 shows the comparison of THD and switching frequency without and with including additional constraints in the cost fucntion. From this table, it is observed that, due to the reduction in switching frequency a slight increase in THD performance of source current is observed. However, the increase in THD is insignificant and still under the limits of IEEE std 519-1992 standard (less than 5%), which emphasize that the proposed control algorithm is efficient.

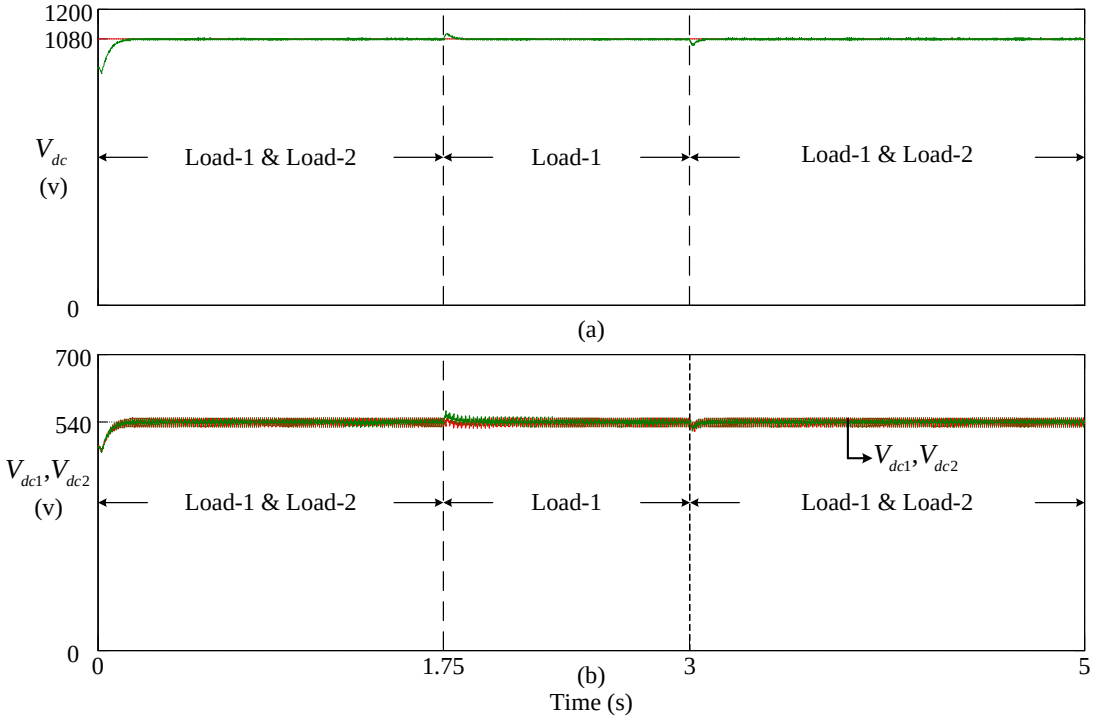


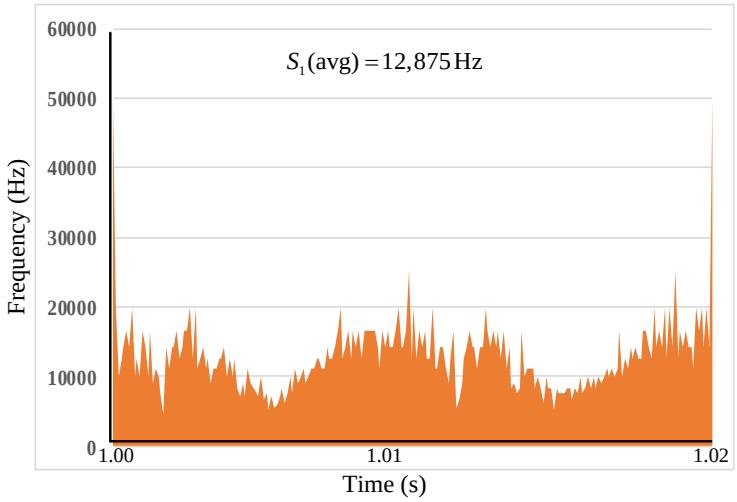
Fig. 3.7 After including additional constraints (a) Voltage across complete dc link, and (b) Voltage across individual capacitors.

Table. 3.4 Comparison of THD and switching frequency

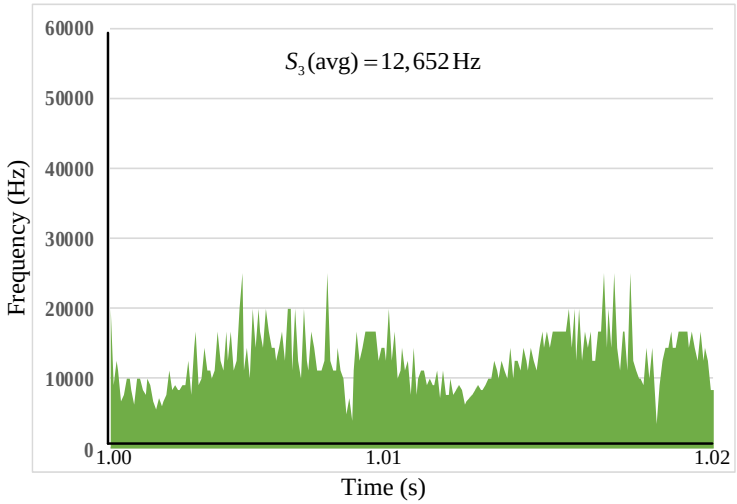
Parameter	THD			Switching frequency (Hz)		
	i_{sa}	i_{sb}	i_{sc}	S_1	S_3	S_5
Without additional constraints	1.57%	1.46%	1.69%	22,280	22,836	22,100
With additional constraints	2.42%	2.41%	2.46%	12,875	12,652	12,929

3.3.2 Performance with higher THD loads

In this case, three single-phase diode bridge rectifiers with capacitor filter on dc side are connected as shown in Fig. 3.1. The parallel connection of capacior on load side results in stringent distortion of source currents and results in high THD. During 0 to 0.5 s, DSTATCOM is operated with only current control and at 0.5 s, additional constraints are added to the cost function. Fig. 3.10 shows the source currents, load currents, DSTATCOM currents and PCC voltages and the THD of load currents is 70% for each phase. Table. 3.5 shows the THDs of source currents, switching frequencies without and with including additional constraints. From this table, it is observed that the THD of source currents without adding additional constraints is 1.75%, 1.72%, 1.72% and the average switching frequencies are 28,506 Hz, 28,426 Hz and 28,891 Hz for phase-*a*, phase-*b* and phase-*c* respectively. After adding the switching frequency constraint, the frequency values are reduced to 17,723 Hz, 18,192 Hz and 17,799 Hz. Similarly, the



(a)



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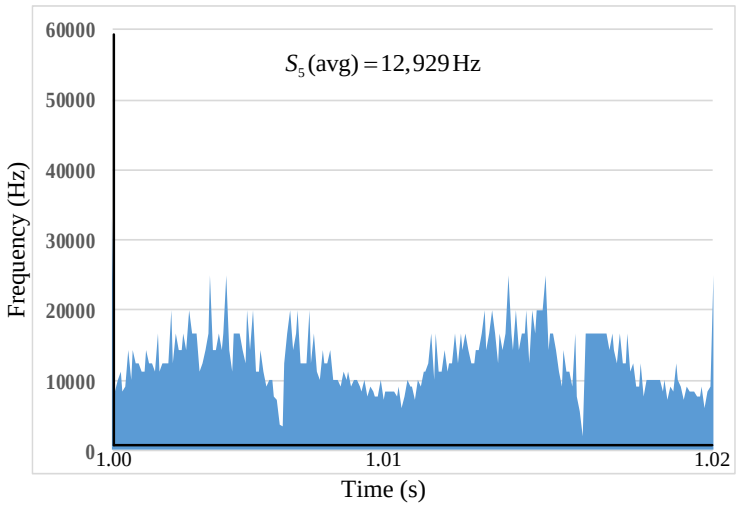


(c)

Fig. 3.8 Average switching frequency after adding additional constraints (a) S_1 (b) S_3, and (c) S_5.

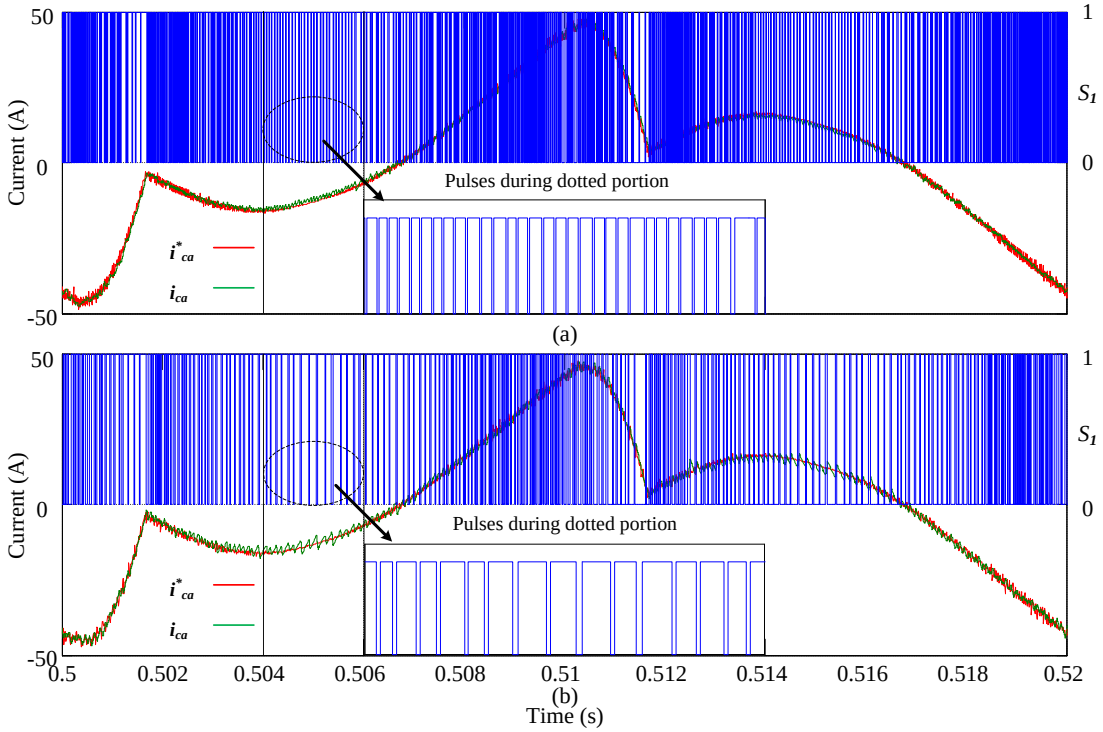


Fig. 3.9 Current tracking and switching pulses comparison (a) Without adding switching frequency constraint, and (b) After including switching frequency constraint in the cost function.

THD values are 2.62%, 2.65% and 2.62% showing that they are well within the limits of IEEE recommendations. Therefore, the proposed method will be applicable to higher THD loads as well.

Table. 3.5 THD and switching frequency comparison for loads with higher THD

Parameter	THD			Switching frequency (Hz)		
	i_{sa}	i_{sb}	i_{sc}	S_1	S_3	S_5
Without adding additional constraints	1.75%	1.72%	1.72%	28,506	28,426	28,891
After adding additional constraints	2.62%	2.65%	2.62%	17,723	18,192	17,799

3.4 Experimental studies

In this chapter, performance of the proposed control algorithm is further validated using experimental studies. Due to the laboratory constraints the experimental setup is built for low voltage and low power rating. The design procedure of the parameters such as

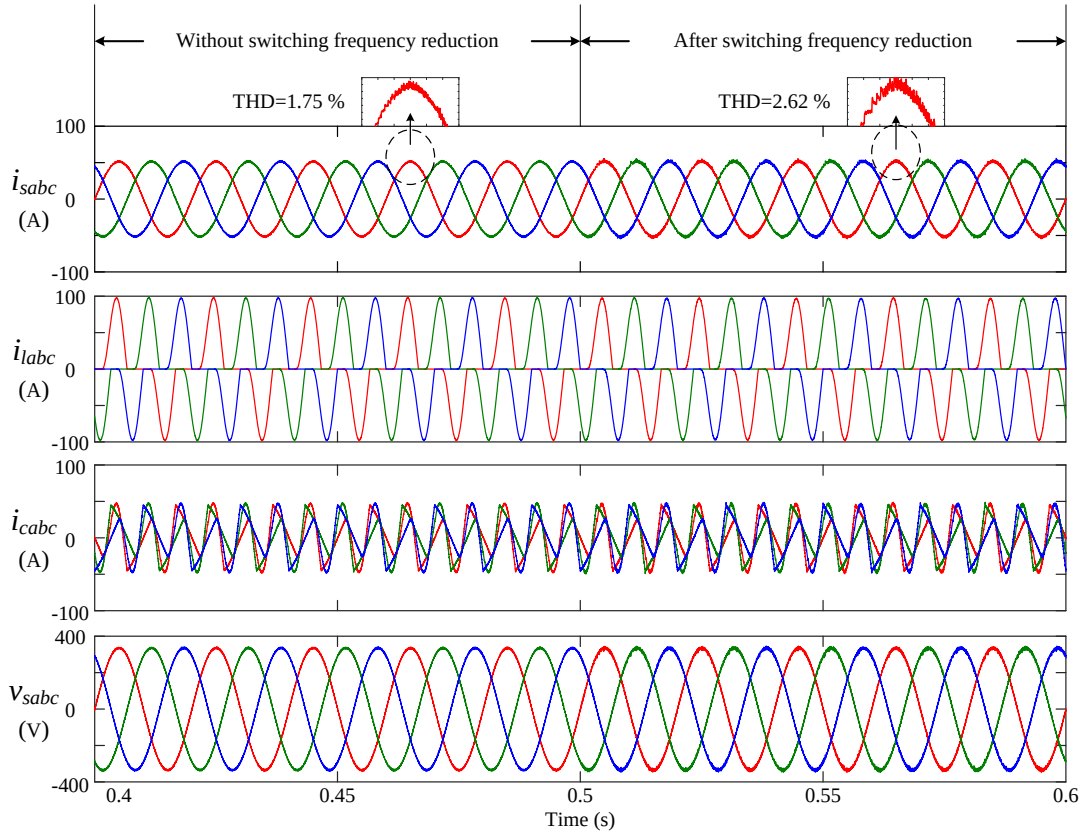


Fig. 3.10 Voltages and currents without and with additional constraints during higher THD loads.

dc link voltage, dc link capacitance and interfacing inductor are already explained. The photograph of the experimental setup is shown in Fig. 3.11. Two different loads are considered for experiment. Load-1 is a three-phase diode bridge rectifier and load-2 is a combination of load-1 and three-phase unbalanced linear load. dSPACE MicroLab-Box 1202 is used as an interface between the personnel computer (PC) and real time environment.

Table. 3.6 Experimental parameters

Parameter	Value
System voltage	50 V
Interfacing Inductor (L_f)	9 mH (with R_f = 0.02 Ω)
DC link voltage (V_{dc})	140 V
DC capacitor (C_{dc1}, C_{dc2})	4700 μF
w_1, w_2 and w_3	0.5, 0.1 and 0.4
Non-linear load	Three-phase diode bride rectifier with load 20 Ω, 150 mH
Unbalanced linear load	5 Ω, 10 mH (phase-a) 34 Ω (phase-b) 17 Ω (phase-c)
Sampling time (T_s)	50 μs

Fig. 3.12 shows, various parameters such as PCC voltages, load currents, DSTATCOM currents and source currents during load variation. From this figure, it is observed that

during load-1, DSTATCOM inject currents such that the source currents are balanced and sinusoidal. Similarly, during load-2 source currents are balanced and sinusoidal regardless of the unbalanced and non-linear load currents. Fig. 3.13 shows, voltage across two capacitors of the dc link. From the figure, it is observed that the complete dc link voltage of 140 V is equally shared between the capacitors and further this voltage is maintained constant during load variations.

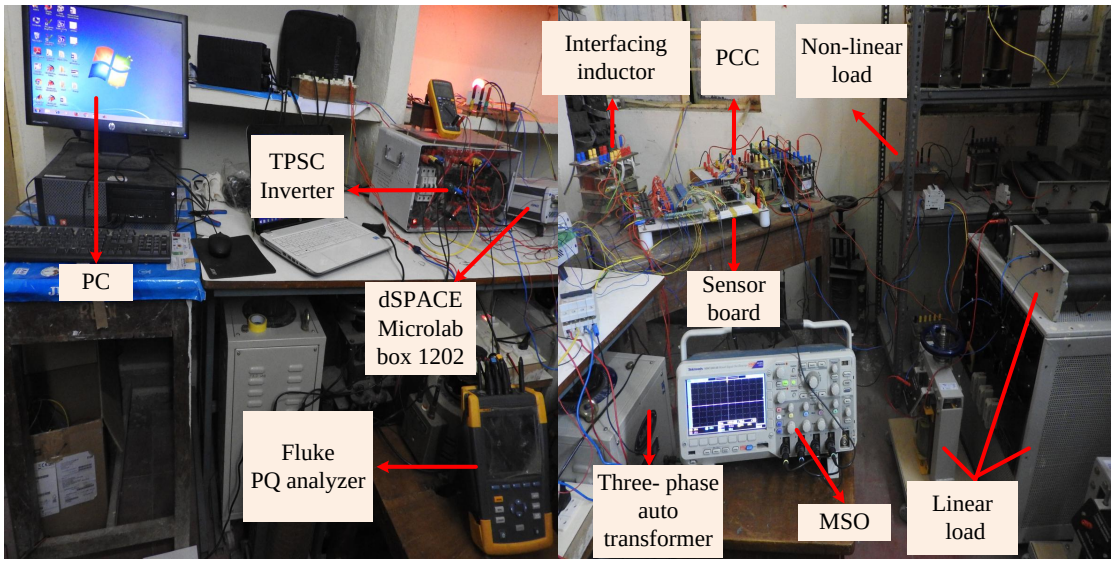
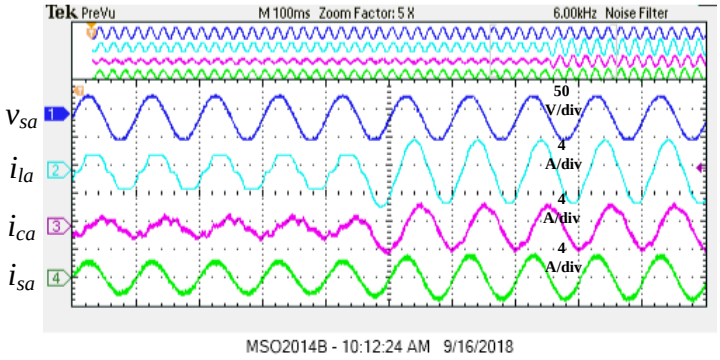
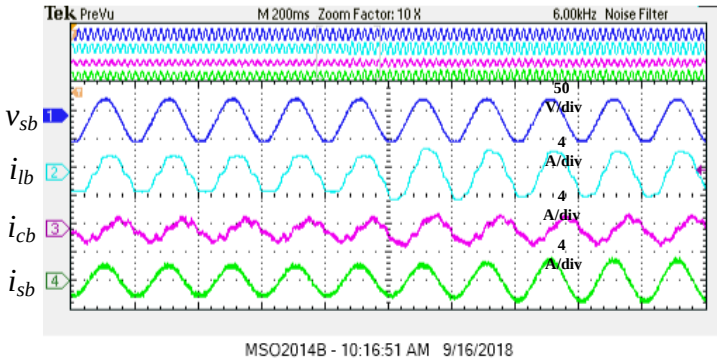


Fig. 3.11 Photograph of the experimental setup.

Table. 3.7 shows THD of source currents, switching frequencies with only current control and after including additional constraint. Initially, the THD of source currents are 3.4%, 2.7% and 1.8% and after adding additional constraints the THDs are 3.9%, 3.6% and 2.8% for phase-*a*, phase-*b* and phase-*c*, respectively. Fig. 3.14 shows the THD results measured by power quality analyzer (Fluke 435 series II). The average switching frequency of IGBT switches, without and with additional constraint in the cost functions are 4,748 Hz, 4,720 Hz and 4,803 Hz and they are shown in Fig. 3.15. As mentioned earlier, with the proposed method, the average switching frequencies are reduced after adding the switching state as a control parameter which is shown in Fig. 3.16 and they are given as 2,807 Hz, 2,823 Hz and 2,810 Hz. Therefore, from Fig. 3.12, Fig. 3.13 and Fig. 3.16 it is observed that, the proposed VIKOR based MPC technique is selecting an optimal switching state from the available switching states, which achieves balanced and sinusoidal source currents, eliminated the voltage divergence, reduced the switching frequency and also simplified the weighting factor selection.



(a)



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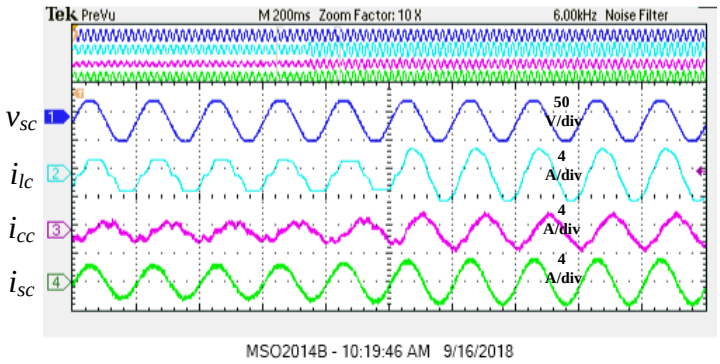


(c)

Fig. 3.12 Parameters during load variation (a) Phase-*a* (b) Phase-*b*, and (c) Phase-*c*.

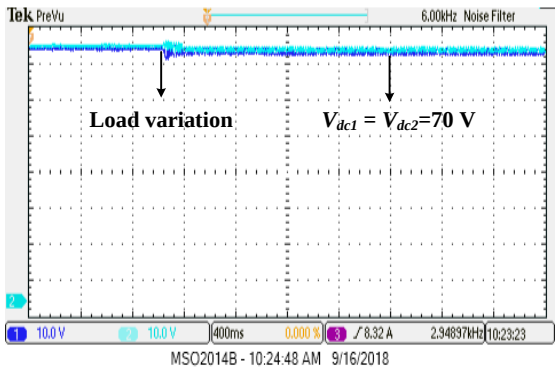


Fig. 3.13 DC link voltage during load variation.

Table. 3.7 THD and switching frequency during experimental studies

Parameter	THD			Switching frequency (Hz)		
	i_{sa}	i_{sb}	i_{sc}	S_1	S_3	S_5
Without adding additional constraints	3.4%	2.7%	1.8%	4,748	4,720	4,803
After adding additional constraints	3.9%	3.6%	2.8%	2,807	2,823	2,810

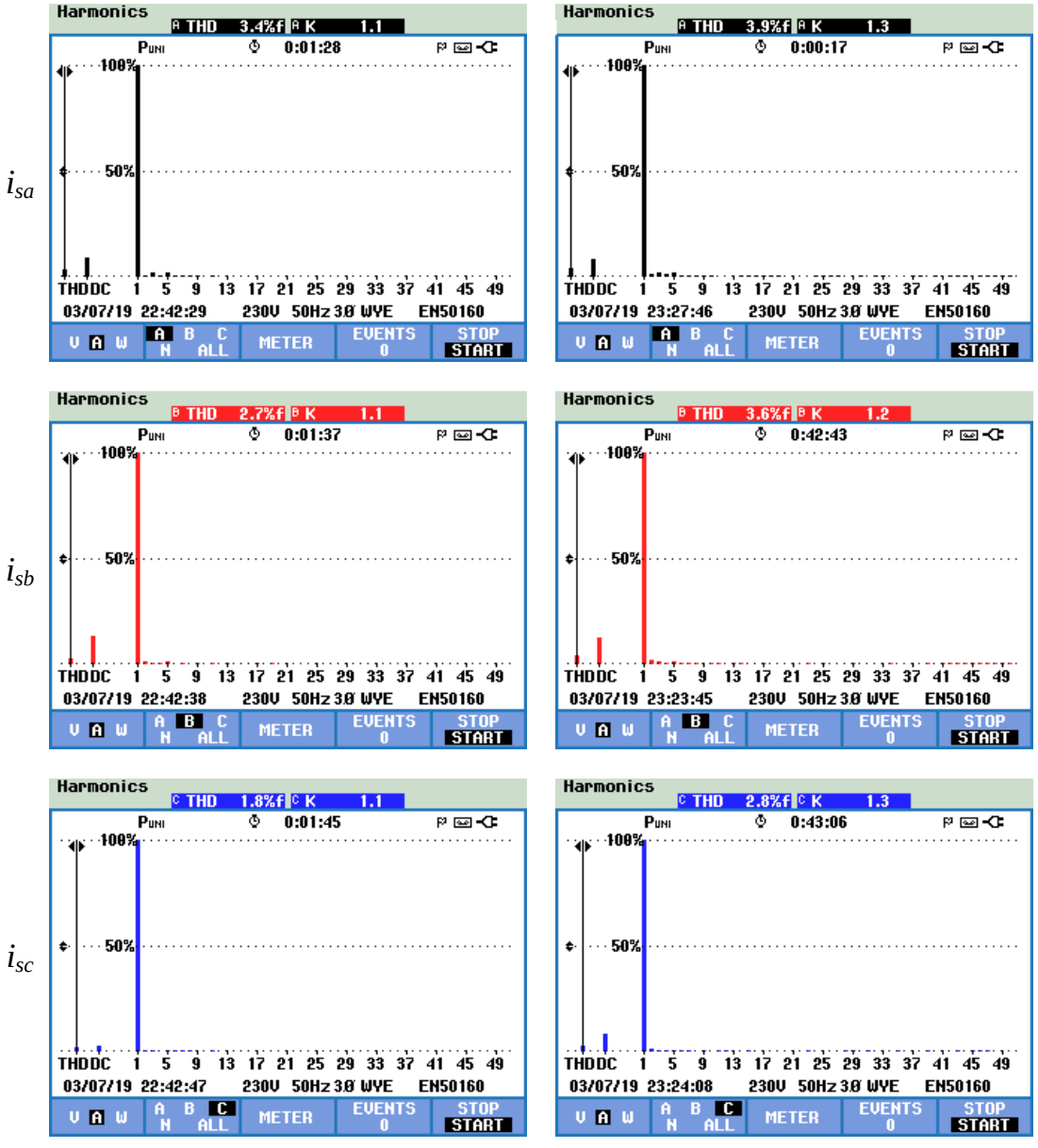
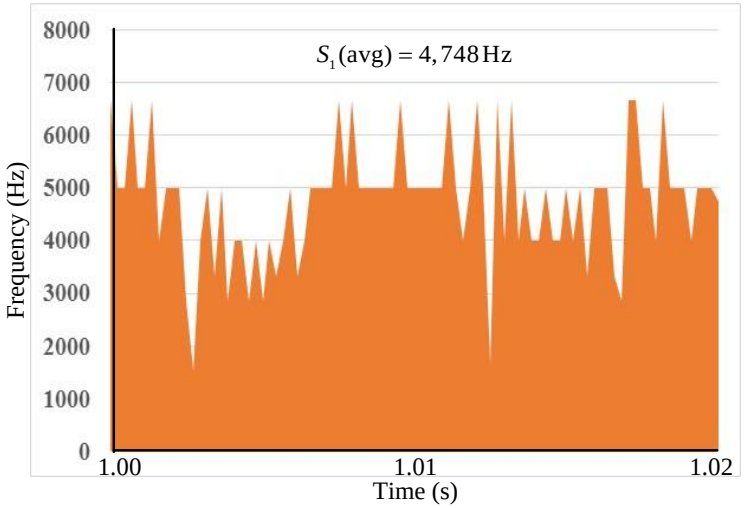
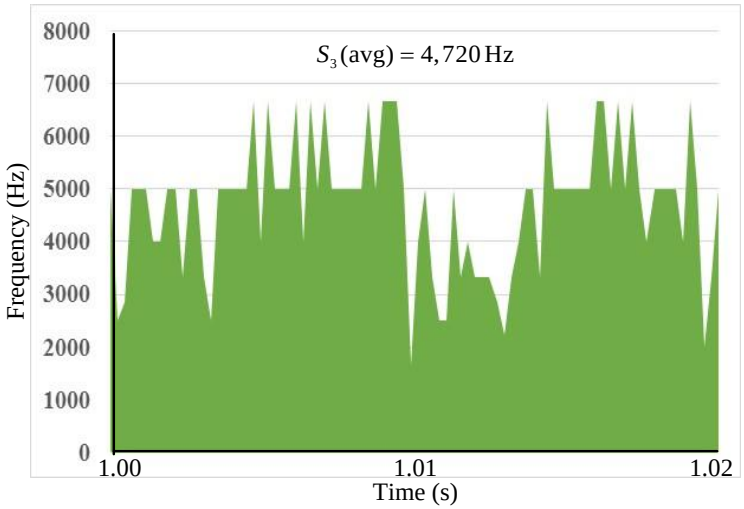


Fig. 3.14 THDs of source currents (a) Without additional constraints, and (b) With additional constraints.



(a)



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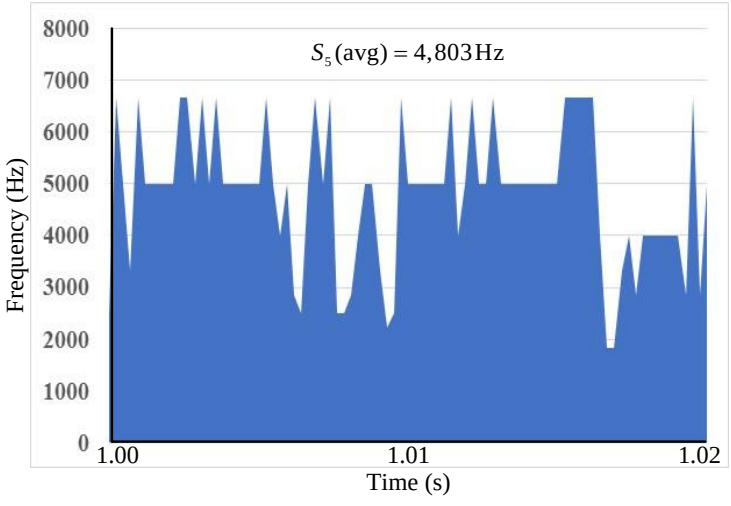
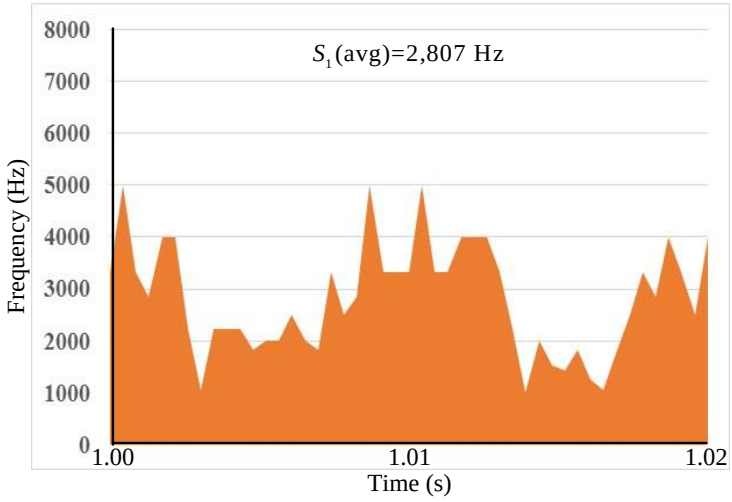
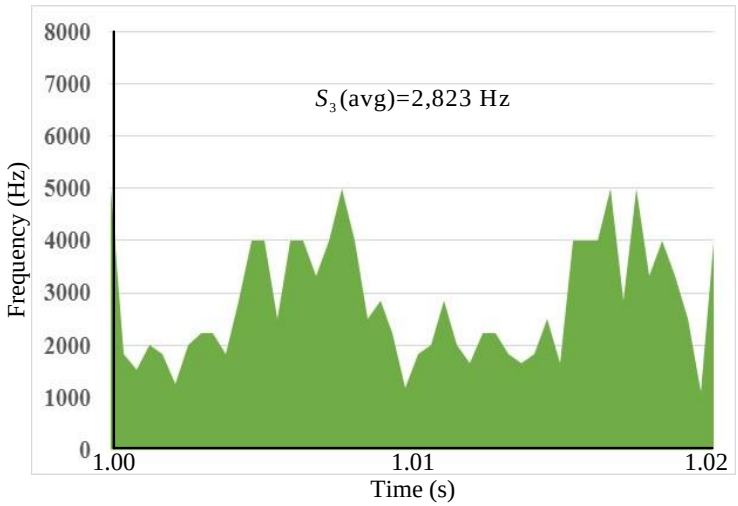


(c)

Fig. 3.15 Average switching frequency without adding additional constraints during experimental studies (a) S_1 (b) S_3, and (c) S_5.



(a)



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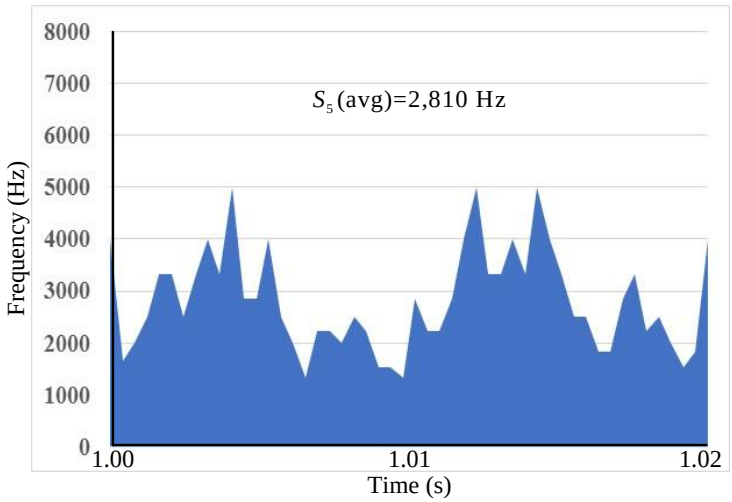


(c)

Fig. 3.16 Average switching frequency after adding additional constraints during experimental studies (a) S_1 (b) S_3, and (c) S_5.

3.4.1 Simulation results for experimental parameters

As the experimental studies are performed on low scale, to corroborate experimental and simulation results, simulation studies are carried out using experimental parameters. PCC voltages, load currents, source currents, DSTATCOM currents and neutral currents are shown in Fig. 3.17. Complete dc link voltage and individual capacitor voltages are shown in Fig. 3.18. Form these figures, it is observed that, DSTATCOM is achieved balanced, sinusoidal source currents and the dc link voltages are also equally utilized.

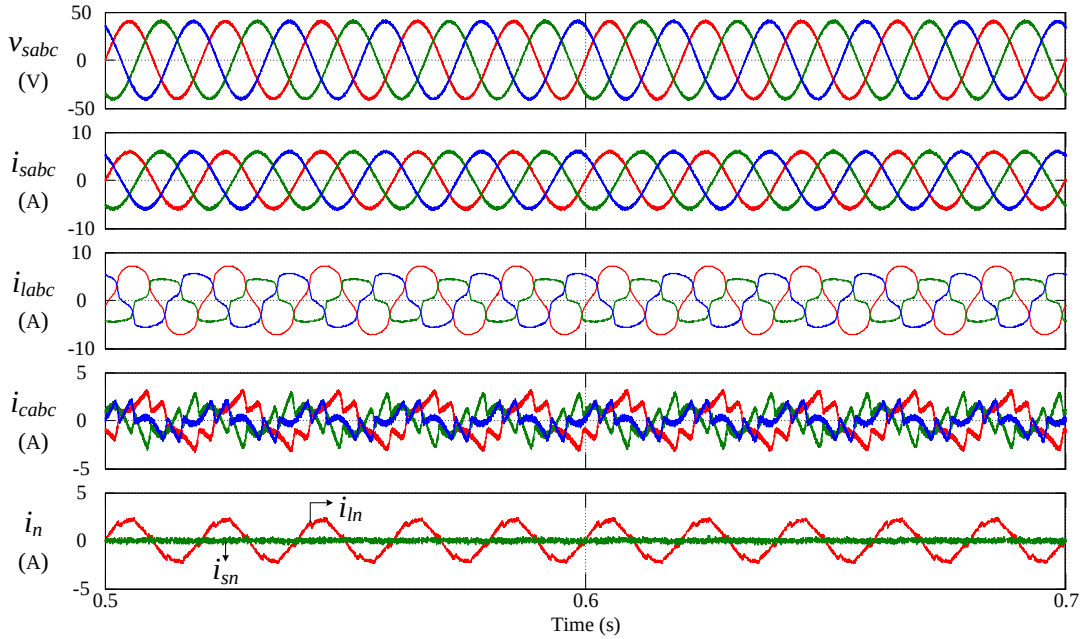


Fig. 3.17 Simulation results of voltages and currents with experimental parameters.

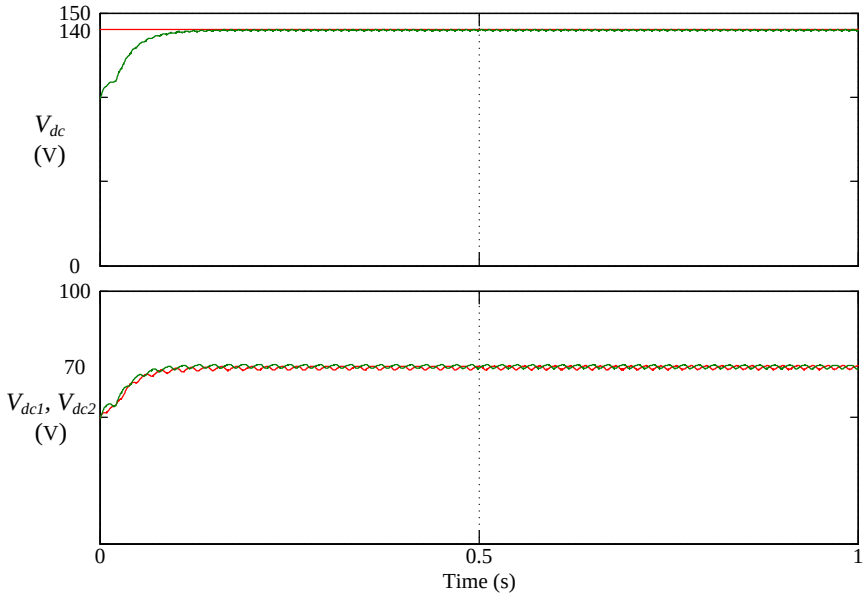


Fig. 3.18 Complete dc link and individual capacitor voltages.

3.5 Summary

In this chapter, MPC of TPSC DTSTACOM with VIKOR method is presented. The summary of the proposed work is as follows:

1. Capacitor voltage divergence limitation of TPSC DSTATCOM topology and higher switching frequency limitation of MPC are conquered by adding them in the cost function as two additional control parameters along with the DSTATCOM currents.

2. Weighting factor selection process is simplified using VIKOR method, therefore the proper balance among the control parameters of the cost function is maintained.

3. The simulation and experimental studies are proved that the proposed method is efficiently compensating the current related power quality issues, maintained equal voltage across two capacitors of dc link, reduced the switching frequency and also simplified the weighting factor selection.

CHAPTER 4

Model Predictive Control with TOPSIS Method for Four Leg DSTATCOM to Improve Power Quality and Reduce Switching Frequency

In this chapter, model predictive control (MPC) of four leg distribution static compensator (FL-DSTATCOM) is proposed to compensate the current related power quality issues under unbalanced and distorted supply voltages. FL-DSTATCOM has a limitation of higher neutral leg switching frequency and it can be reduced by adding an additional constraint to the cost function using a weighting factor. The reduction in neutral leg switching frequency will further reduces the switching frequency of phase legs. But, the selection of weighting factor during multi-constraint case is a cumbersome task. Therefore, to simplify the weighting factor selection process, an optimization technique, namely, the Technique for Order of Preference by Similarity to Ideal Solution (TOPSIS) is used, which further selects the optimal switching state.

4.1 Introduction

Among the available DSTATCOM topologies, three H-bridge (HB), three-phase split -capacitor (TPSC) and four leg DSTATCOM (FL-DSTATCOM) are mostly used for 3P4W applications [70]. However, three HB topology has the limitation of more switches and also requires isolation transformer for coupling [65]. TPSC topology, on the other hand, reduces the requirement of more number of switches, but the capacitor voltage balancing is a considerable issue and also this topology requires higher dc link voltage [25]. Though, FL-DSTATCOM has more switches compared to TPSC, other advantages such as better controllability, low dc link voltage and absence of capacitor voltage balancing problem make FL-DSTATCOM superior to other topologies [65]. Therefore, in this chapter, a FL-DSTATCOM is used to compensate the current related power quality issues.

Conventional operation of DSTATCOM mostly involves two different modes. Between them, one is harmonic free (HF) mode and the other is power factor correction (PFC) mode. During balanced and sinusoidal supply voltages, both HF and PFC mode achieve the similar performance. However, during unbalance and distortions in supply voltage, it is not possible to operate DSTATCOM in HF and PFC mode simultaneously [71], [72]. This is because, perfect compensation of harmonics may not provide unity power factor; similarly, unity power factor operation does not guarantee perfect harmonic compensation [47], [73]. Therefore, in this chapter, only HF operation of DSTATCOM is considered, which will make the source currents balanced and sinusoidal.

The performance of DSTATCOM mainly depends on reference current extraction and control algorithm used to generate gate pulses. A considerable amount of investigations has already been accomplished in the area of reference current extraction techniques and control algorithms [40], [48], [74]. Extraction of reference currents is a challenging task when the loads are supplied by unbalanced and distorted voltages, because they depend on upstream loads and voltage unit vectors [75]. In general, the unit vectors of a three-phase balanced system are sinusoidal in nature, and also have unit amplitude. In most of the control algorithms, the direct estimation of unit vectors from the PCC voltages leads to deviation of unit vectors, during unbalance and distortions in supply voltage. Therefore, in this thesis, a combination of state observer and theory of symmetrical components is used to estimate unit vectors, which have the same nature as ideal unit vectors [76]. After extracting unit vectors, conductance factor based method is implemented in which, the extracted unit vectors and sensed load currents are used to estimate the reference source currents [63]. Finally, the difference between load currents and reference source currents will give us reference DSTATCOM currents.

In recent years, MPC methods are attracting most of the researchers over traditional pulse width modulation (PWM) and hysteresis based controllers due to its simple concept, model based implementation, elimination of modulating signal, easy addition of control parameters and better attention given to added constraints [56], [57]. A three leg DSTATCOM is controlled using MPC to compensate the voltage sags in the distribution system [77]. A hysteresis controller based MPC is proposed for DSTATCOM [78]; in this control technique, model of DSTATCOM is used to predict the reference current at $(k+1)^{th}$ state. Then the difference between the reference and actual value is given to hysteresis controller which further generates the switching signals. Predictive current

control of a three leg DSTATCOM is proposed in [62], [79], and it is proved that the performance of the control technique is better than the conventional PI, hysteresis, ramp based and sliding mode controllers. Model predictive control of three leg DSTATCOM is proposed [80] to compensate harmonic and reactive components in load currents. However, all the above mentioned topologies are not suitable for 3P4W systems, because of the absence of fourth leg. In [26], MPC is proposed for TPSC DSTATCOM which can compensate the reactive, harmonic and neutral currents. However, this topology suffers with the problem of capacitor voltage unbalance, requires higher dc link voltage and operates at higher switching frequencies. In FL-DSTATCOM topologies, the dependency of phase voltage on neutral voltage will further increase the neutral leg switching frequency [81]. As mentioned earlier, that the advantage of MPC is easy addition and better attention to control parameters; the limitation of higher switching frequency will be reduced by adding the difference between the present and previous switching state as an additional control parameter using a weighting factor. The reduction in neutral leg frequency will also reduce the phase leg frequency because each is dependent on the other. However, there is no particular method in the literature to tune the weighting factor value [82]. To simplify the weighting factors selection, the traditional multi criteria decision making (MCDM) methods are attractive [69]. Therefore, in this chapter a MCDM method, namely, TOPSIS is used. With this method, a better alternative among the available switching states is selected based on the concept of compromise solution.

4.2 Proposed MPC with TOPSIS for FL-DSTATCOM

The schematic diagram of FL-DSTATCOM connected distribution system is shown in Fig. 4.1. FL-DSTATCOM is connected at the PCC through an interfacing inductor which eliminates switching harmonics in compensating current. PCC voltages, load currents and DSTATCOM currents are sensed for the extraction of unit vectors and reference currents. The procedure of the proposed control algorithm is explained as follows.

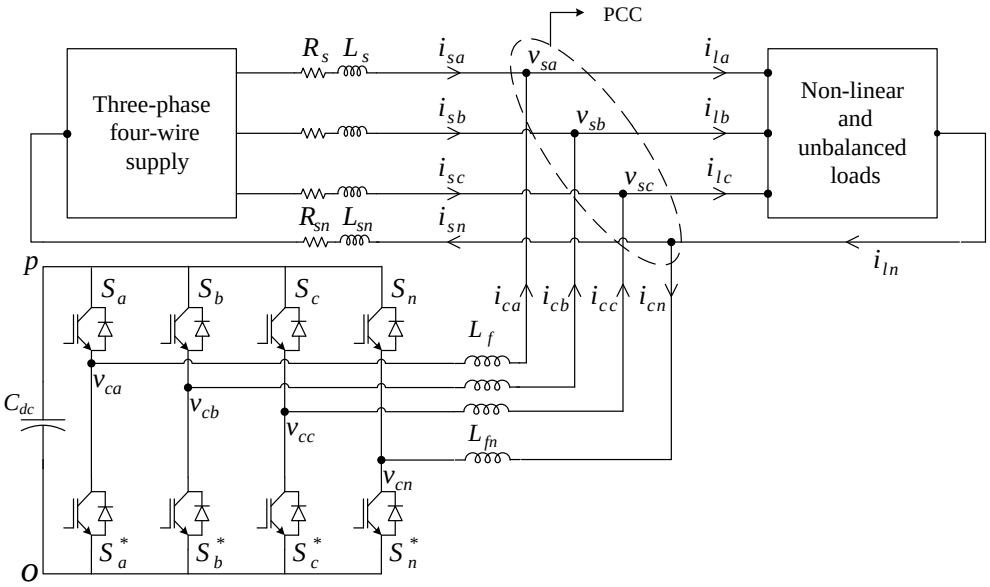


Fig. 4.1 Schematic diagram of a FL-DSTATCOM connected distribution system.

4.2.1 Unit vector estimation using state observers from unbalanced and distorted supply voltages

The estimation of conductance factors and reference currents depends mainly on load currents and unit vectors extracted from PCC voltages. During balanced and sinusoidal supply voltages, in-phase unit vectors are expressed as,

$$u_{pa} = \frac{v_{sa}}{V_{sm}}, \quad u_{pb} = \frac{v_{sb}}{V_{sm}}, \quad u_{pc} = \frac{v_{sc}}{V_{sm}} \tag{4.1}$$

where, v_{sa}, v_{sb} and v_{sc} represents the phase voltages at PCC and V_{sm} represents the peak amplitude of phase voltage at PCC and is given as,

$$V_{sm} = \sqrt{\frac{2}{3}(v_{sa}^2 + v_{sb}^2 + v_{sc}^2)}. \tag{4.2}$$

Similarly, quadrature unit vectors are expressed as:

$$u_{qa} = \frac{-u_{pb} + u_{pc}}{\sqrt{3}}, \; u_{qb} = \frac{3u_{pa} + u_{pb} - u_{pc}}{2\sqrt{3}}, \; u_{qc} = \frac{-3u_{pa} + u_{pb} - u_{pc}}{2\sqrt{3}}. \tag{4.3}$$

In general, the magnitude of unit vector is 1 and the unit vectors should be harmonic free. However, during unbalance and distortion in supply voltage, the unequal amplitude values and the presence of distortion, makes it difficult to estimate the unit vectors using (4.1) and (4.3). The extraction of unit vectors from the fundamental positive

sequence voltages eliminates this difficulty, because they are equal in amplitude and distortion free. The extraction of fundamental in-phase and quadrature voltages from a voltage signal using state observer is shown in Fig. 4.2 and it mainly depends on its state space model [76]. Required fundamental in-phase and quadrature components are represented as,

$$v_s(t) = \begin{bmatrix} v_{sp}(t) \\ v_{sq}(t) \end{bmatrix} = \begin{bmatrix} V_{sm}\sin\omega_1 t \\ V_{sm}\cos\omega_1 t \end{bmatrix}. \tag{4.4}$$

Where, $v_{sp}(t)$ and $v_{sq}(t)$ are the fundamental in-phase and quadrature voltages. V_{sm} is the amplitude of the fundamental component and ω_1 is the fundamental frequency. Differentiating (4.4) with respect to ω_1 will give us,

$$\dot{v}_s(t) = \begin{bmatrix} \omega_1 V_{sm}\cos\omega_1 t \\ -\omega_1 V_{sm}\sin\omega_1 t \end{bmatrix} = \begin{bmatrix} 0 & \omega_1 \\ -\omega_1 & 0 \end{bmatrix} \begin{bmatrix} V_{sm}\sin\omega_1 t \\ V_{sm}\cos\omega_1 t \end{bmatrix} = A v_s(t) \tag{4.5}$$

At the same time, output of the state observer will be fundamental in-phase component and it is represented as,

$$v(t) = V_{sm}\sin\omega_1 t = \begin{bmatrix} 1 & 0 \end{bmatrix} \begin{bmatrix} V_{sm}\sin\omega_1 t \\ V_{sm}\cos\omega_1 t \end{bmatrix} = C^T v_s(t), \tag{4.6}$$

A linear second order continuous time oscillating system (in terms of state equation and output equation) at ω_1 can be described as [76]

$$\begin{aligned} \dot{v}_s(t) &= A v_s(t), \\ v(t) &= C^T v_s(t), \end{aligned} \tag{4.7}$$

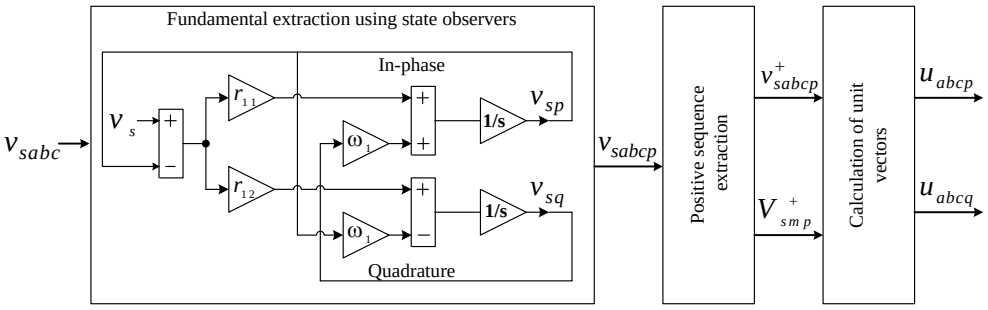


Fig. 4.2 Extraction of unit vectors using state observer and theory of symmetrical components [76].

In closed loop system, the observation error is given as,

$$e(t) = v_s(t) - \widehat{v_s}(t). \tag{4.8}$$

where, $\widehat{v_s}(t)$ is the estimate of the actual voltage. Then the model of the observer will be [76],

$$\begin{aligned} \widehat{\dot{v}_s}(t) &= A\widehat{v_s}(t) + Re(t), \\ \widehat{v}(t) &= C^T\widehat{v_s}(t), \end{aligned} \tag{4.9}$$

where, $R = \begin{bmatrix} r_{11} & r_{12} \end{bmatrix}^T$. The state error vector can be written as,

$$\dot{v}_s(t) - \widehat{\dot{v}_s}(t) = Av_s(t) - A\widehat{v_s}(t) - Re(t) = (A - RC^T)(v_s(t) - \widehat{v_s}(t)). \tag{4.10}$$

The above equation can also be written as,

$$\dot{e}(t) = (A - RC^T)e(t). \tag{4.11}$$

The characteristic equation of error will be [76],

$$|\mathrm{S}I - (A - RC^T)| = 0. \tag{4.12}$$

The roots of the error characteristic equation are the closed loop poles. The value of R can be chosen such that $(A - RC^T)$ has reasonably fast and stable roots. The assumed closed loop poles are $S = (-a\omega \pm j\omega)$. The relation between R and a is,

$$R = \begin{bmatrix} r_{11} & r_{12} \end{bmatrix}^T = \begin{bmatrix} 2a\omega & a^2\omega \end{bmatrix}^T. \tag{4.13}$$

The transient response of the observer will be decided by the real part of the pole. If the location of the pole is closer to the origin, time constant will be high and output is purely sinusoidal. If it is away from the origin, the time constant is reduced and harmonics will be added to the output signal. Therefore in this chapter, the value of a is assumed to be 0.1, so that the obtained values of r_{11} and r_{12} are 62.8 and 3.14, which will provide in-phase and quadrature voltages (v_{sp}, v_{sq}) with better quality. Three state observers are required for the extraction of fundamental voltages from three phases and

the same values of r_{11} and r_{12} are applied for all the state observers. During balanced and distorted supply conditions, a state observer is sufficient to extract unit vectors. But during unbalance in the supply voltage, amplitudes of each state observer output is different; therefore it is not possible to get unit vectors. To overcome this limitation, fundamental positive sequence voltages (v^+_{sabcp}) are required, which have equal amplitude without any distortion. The theory of symmetrical components is applied to obtain the fundamental positive sequence voltages (v^+_{sabcp}) and they are given as:

$$\begin{bmatrix} v^+_{sap} \\ v^+_{sbp} \\ v^+_{scp} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 1 & a & a^2 \\ a^2 & 1 & a \\ a & a^2 & 1 \end{bmatrix}\begin{bmatrix} v_{sap} \\ v_{sbp} \\ v_{scp} \end{bmatrix} \tag{4.14}$$

where, v_{sap}, v_{sbp} and v_{scp} are fundamental in-phase voltages and $a = 1\angle 120^\circ$. After extracting fundamental positive sequence voltages, they are divided by their amplitudes to find the required in-phase unit vectors and they are given as

$$u_{pa} = \frac{v^+_{sap}}{V^+_{smp}}; \quad u_{pb} = \frac{v^+_{sbp}}{V^+_{smp}}; \quad u_{pc} = \frac{v^+_{scp}}{V^+_{smp}} \tag{4.15}$$

where, the amplitude is given as, $V^+_{smp} = \sqrt{\frac{2}{3}\left((v^+_{sap})^2 + (v^+_{sbp})^2 + (v^+_{scp})^2\right)}$. Quadrature unit vectors are calculated from in-phase unit vectors and they are given as,

$$u_{qa} = \frac{-u_{pb} + u_{pc}}{\sqrt{3}}; \quad u_{qb} = \frac{3u_{pa} + u_{pb} - u_{pc}}{2\sqrt{3}}; \quad u_{qc} = \frac{-3u_{pa} + u_{pb} - u_{pc}}{2\sqrt{3}}. \tag{4.16}$$

The block diagram of reference current extraction using conductance factors and switching pulse generation using MPC is shown in Fig. 4.3. The complete procedure for reference current extraction and switching pulse generation is explained in the following subsections.

4.2.2 Reference current extraction using conductance factor

In general, non-linear load currents are a combination of active, reactive, harmonic and dc components, which can be expressed as [63],

$$i_l(t) = i_{lp}(t) + i_{lq}(t) + i_{lh}(t) + I_{dc} \tag{4.17}$$

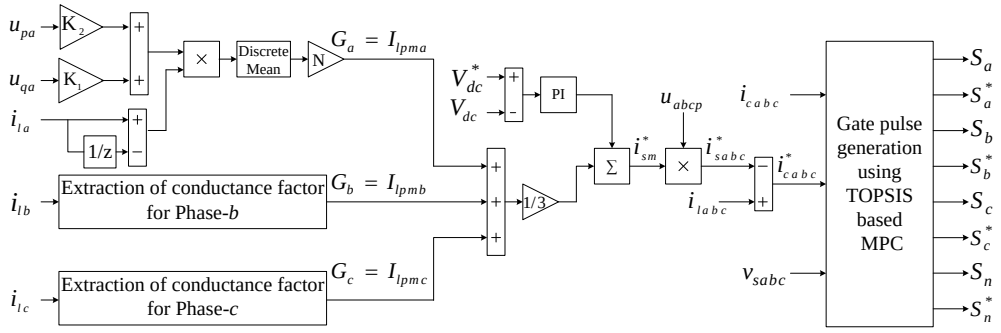


Fig. 4.3 Proposed conductance factor based control algorithm for FL-DSTATCOM.

where, $i_{lp}(t) = I_{mp}\sin\omega t$, $i_{lq}(t) = I_{mq}\sin(\omega t - \frac{\pi}{2})$ and $i_h(t) = \sum_{h=2}^{\infty} I_{mh}\sin(h\omega t + \phi_h)$. (4.17) is expressed in terms of instantaneous PCC voltages,

$$i_l(t) = Gv_s(t) + B\int v_s(t)\mathrm{d}t + i_{lh}(t) + I_{dc} \tag{4.18}$$

where, G is the conductance factor and is equal to $1/R$ and $B = 1/L$. To achieve harmonic free, balanced source currents, supply has to deliver fundamental active component of load current irrespective of the load. From (4.18), it is observed that, fundamental active component of load current is obtained by multiplying conductance factor with voltage at PCC and it is evaluated by taking the derivative of (4.18) using trapezoidal rule over N consecutive intervals [63]. Here, N represents the number of samples and is the ratio of fundamental time period and sampling time (T_s).

$$i_{l(j)} - i_{l(j-1)} = G(v_{s(j)} - v_{s(j-1)}) + \frac{T_s}{2}(v_{s(j)} + v_{s(j-1)})B + (i_{lh(j)} - i_{lh(j-1)}) \tag{4.19}$$

where, $j = 1, 2, 3, ..., N-1, N$, $i_{lj} = i_l(t_j)$, $i_{lh(j)} = i_{lh}(t_j)$, $v_{s(j)} = v_s(t_j)$. Expressing (4.19) in matrix form [63],

$$\begin{bmatrix} v_{s1} - v_{s0} & \frac{T_s}{2}(v_{s1} + v_{s0}) & i_{lh1} - i_{lh0} \\ \vdots & \vdots & \vdots \\ v_{sN} - v_{s(N-1)} & \frac{T_s}{2}(v_{sN} + v_{s(N-1)}) & i_{lhN} - i_{lh(N-1)} \end{bmatrix} \begin{bmatrix} G \\ B \\ 1 \end{bmatrix} = \begin{bmatrix} i_{l1} - i_{l0} \\ \vdots \\ i_{lN} - i_{l(N-1)} \end{bmatrix}. \tag{4.20}$$

The above equation is in the form of $PX = Q$, so that conductance factor, G can be calculated using [63]:

$$X = (P^T P)^{-1} P^T Q. \tag{4.21}$$

Individual terms of (4.21) are given in (4.22), (4.23) and (4.24). Initially, $P^T P$ is expressed in (4.22). Assuming the voltages in (4.22) as pure sinusoidal, use Riemann integral [63] to simplify the individual elements of the matrix. After simplification, all the non-diagonal elements become zero and the inverse of (4.22) is given in (4.23) and the matrix $P^T Q$ is given in (4.24).

$$P^T P = \begin{bmatrix} \sum_{j=1}^{N}(v_{sj} - v_{s(j-1)})^2 & \left(\frac{T_s}{2}\right)\sum_{j=1}^{N}(v_{sj}^2 - v_{s(j-1)}^2) & \sum_{j=1}^{N}(v_{sj} - v_{s(j-1)})(i_{lhj} - i_{lh(j-1)}) \\ \left(\frac{T_s}{2}\right)\sum_{j=1}^{N}(v_{sj}^2 - v_{s(j-1)}^2) & \left(\frac{T_s}{2}\right)\sum_{j=1}^{N}(v_{sj} + v_{s(j+1)})^2 & \left(\frac{T_s}{2}\right)\sum_{j=1}^{N}(v_{sj} + v_{s(j+1)})(i_{lhj} - i_{lh(j-1)}) \\ \sum_{j=1}^{N}(v_{sj} - v_{s(j-1)})(i_{lhj} - i_{lh(j-1)}) & \left(\frac{T_s}{2}\right)\sum_{j=1}^{N}(v_{sj} + v_{s(j+1)})(i_{lhj} - i_{lh(j-1)}) & \sum_{j=1}^{N}(i_{lhj} - i_{lh(j-1)})^2 \end{bmatrix} \tag{4.22}$$

$$(P^T P)^{-1} = \begin{bmatrix} \frac{1}{\sum_{j=1}^{N}(v_{sj} - v_{s(j-1)})^2} & 0 & 0 \\ 0 & \frac{4}{T_s^2 \sum_{j=1}^{N}(v_{sj} + v_{s(j-1)})^2} & 0 \\ 0 & 0 & \frac{1}{\sum_{j=1}^{N}(i_{lhj} - i_{lh(j-1)})^2} \end{bmatrix} \tag{4.23}$$

$$P^T Q = \begin{bmatrix} \sum_{j=1}^{N}(i_{lj} - i_{l(j-1)})(v_{sj} - v_{s(j-1)}) \\ \left(\frac{T_s}{2}\right)\sum_{j=1}^{N}(i_{lhj} - i_{lh(j-1)})(v_{sj} + v_{s(j-1)}) \\ \sum_{j=1}^{N}(i_{lj} - i_{l(j-1)})(v_{sj} + v_{s(j-1)}). \end{bmatrix} \tag{4.24}$$

After finding $(P^T P)^{-1}$ and $P^T Q$, conductance factor G is obtained by multiplying first row of matrix $(P^T P)^{-1}$ with $P^T Q$ and it is given in (4.25).

$$G(t_N) = \frac{\sum_{j=1}^{N}(i_{lj} - i_{l(j-1)})(v_{sj} - v_{s(j-1)})}{\sum_{j=1}^{N}(v_{sj} - v_{s(j-1)})^2}. \tag{4.25}$$

After calculating the conductance factor, active component of load current is obtained by multiplying instantaneous voltage with conductance factor.

$$i_{lp} = G(t_N) \times v_s(t_N). \tag{4.26}$$

In general, fundamental active component of load current is expressed as a product of maximum value of load current and in-phase unit vector i.e.,

$$i_{lp} = I_{lpm} \times u_p. \tag{4.27}$$

It is observed from (4.26) and (4.27) that, by replacing voltages in (4.25) and (4.26) with respective unit vectors, conductance factor will be the same as peak value of fundamental active component of load current i.e., $G(t_N) = I_{lpm}$. After replacing the voltage in (4.25) with respective unit vector, the conductance factor is given as,

$$G(t_N) = \frac{\sum_{j=1}^{N} (i_{lj} - i_{l(j-1)})(u_{pj} - u_{p(j-1)})}{\left(u_{pj} - u_{p(j-1)}\right)^2}. \tag{4.28}$$

Simplifying (4.28) using Riemann integral [63],

$$G_p(t_N) = \sum_{j=1}^{N} (i_j - i_{j-1})(u_{qj} \times K_1 + u_{pj} \times K_2) \tag{4.29}$$

where, $K_1 = \dfrac{\cos(\omega T_s/2)}{N \sin(\omega T_s/2)}$, $K_2 = \dfrac{1}{N}$ [63]. To find the conductance factors for phase-a, phase-b and phase-c, substitute respective unit vectors in (4.29) and they are given in (4.30)

$$\begin{aligned}
G_a(t_N) = I_{lpma} &= \sum_{j=1}^{N} (i_{laj} - i_{la(j-1)})(u_{qaj} \times K_1 + u_{paj} \times K_2); \\
G_b(t_N) = I_{lpmb} &= \sum_{j=1}^{N} (i_{lbj} - i_{lb(j-1)})(u_{qbj} \times K_1 + u_{pbj} \times K_2); \\
G_c(t_N) = I_{lpmc} &= \sum_{j=1}^{N} (i_{lcj} - i_{lc(j-1)})(u_{qcj} \times K_1 + u_{pcj} \times K_2)\ .
\end{aligned} \tag{4.30}$$

To achieve balanced and sinusoidal source currents, reference source current will be considered as average of fundamental active component of three load currents.

$$I_{lpm} = \frac{I_{lpma} + I_{lpmb} + I_{lpmc}}{3}. \tag{4.31}$$

DSTATCOM requires active power to support the switching losses of the voltage source inverter. In general, this active power has to be supplied by the utility. The difference

between actual and measured dc link voltage values ($V^*_{dc} - V_{dc}$) are passed through a PI controller which generates the required active component of current (I^*_{dc}) and it is responsible for inverter switching losses.

$$I^*_{dc} = K_p(V^*_{dc} - V_{dc}) + K_i \int (V^*_{dc} - V_{dc})\mathrm{d}t. \tag{4.32}$$

ZieglerNichols method [83] is used to select the values of K_p and K_i. In the above equation the value of K_p is considered as 0.45 and the value of K_i is considered as 4.5. Finally, reference source current is a combination of average value of fundamental active component of load current and the current required to maintain constant voltage across the dc link of the VSI and is given as,

$$i^*_{sa} = (I_{lpm} + I^*_{dc}) \times u_{pa};\ i^*_{sb} = (I_{lpm} + I^*_{dc}) \times u_{pb};\ i^*_{sc} = (I_{lpm} + I^*_{dc}) \times u_{pc}. \tag{4.33}$$

After calculating the reference source currents, the reference DSTATCOM currents will be the difference between the actual load currents and the reference source currents.

$$i^*_{ca} = i_{la} - i^*_{sa};\ i^*_{cb} = i_{lb} - i^*_{sb};\ i^*_{cc} = i_{lc} - i^*_{sc}. \tag{4.34}$$

4.2.3 Predictive model of FL-DSTATCOM and cost function formation

FL-DSTATCOM has 16 possible switching states. The voltages of all the phases with respect to negative dc rail and to the mid point of the neutral leg are given in Table. 4.1, for all the available switching states.

Predictive model of the FL-DSTATCOM is used to estimate the compensator currents at $(k+1)^{th}$ state. From Fig. 4.1, the output voltage of the inverter is the sum of voltage drop across the interfacing inductor and voltage at the PCC, which can be written as,

$$v_c = L_f \frac{\mathrm{d}i_c}{\mathrm{d}t} + R_f i_c + v_s \tag{4.35}$$

Table. 4.1 Pole voltages and phase voltages of FL-DSTATCOM

S_a	S_b	S_c	S_n	v_{cao}	v_{cbo}	v_{cco}	v_{cno}	v_{can}	v_{cbn}	v_{ccn}
0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	V_{dc}	$-V_{dc}$	$-V_{dc}$	$-V_{dc}$
0	0	1	0	0	0	V_{dc}	0	0	0	V_{dc}
0	0	1	1	0	0	V_{dc}	V_{dc}	$-V_{dc}$	$-V_{dc}$	0
0	1	0	0	0	V_{dc}	0	0	0	V_{dc}	0
0	1	0	1	0	V_{dc}	0	V_{dc}	$-V_{dc}$	0	$-V_{dc}$
0	1	1	0	0	V_{dc}	V_{dc}	0	0	V_{dc}	V_{dc}
0	1	1	1	0	V_{dc}	V_{dc}	V_{dc}	$-V_{dc}$	0	0
1	0	0	0	V_{dc}	0	0	0	V_{dc}	0	0
1	0	0	1	V_{dc}	0	0	V_{dc}	0	$-V_{dc}$	$-V_{dc}$
1	0	1	0	V_{dc}	0	V_{dc}	0	V_{dc}	0	V_{dc}
1	0	1	1	V_{dc}	0	V_{dc}	V_{dc}	0	$-V_{dc}$	0
1	1	0	0	V_{dc}	V_{dc}	0	0	V_{dc}	V_{dc}	0
1	1	0	1	V_{dc}	V_{dc}	0	V_{dc}	0	0	$-V_{dc}$
1	1	1	0	V_{dc}	V_{dc}	V_{dc}	0	V_{dc}	V_{dc}	V_{dc}
1	1	1	1	V_{dc}	V_{dc}	V_{dc}	V_{dc}	0	0	0

solving, (4.35) for $\frac{\mathrm{d}i_c}{\mathrm{d}t}$ will give us,

$$\frac{\mathrm{d}i_c}{\mathrm{d}t} = \frac{(v_c - v_s)}{L_f} - \frac{i_c R_f}{L_f}. \tag{4.36}$$

The above equation can be simplified using Forward Euler approximation, and according to this method,

$$\frac{\mathrm{d}i_c}{\mathrm{d}t} = \frac{i_c(k+1) - i_c(k)}{T_s}. \tag{4.37}$$

Substitute, (4.37) in (4.36) and simplify (4.36) for $i_c(k+1)$,

$$i_c(k+1) = \frac{(v_c(k) - v_s(k))T_s}{L_f} + i_c(k)\left(1 - \frac{R_f T_s}{L_f}\right). \tag{4.38}$$

From (4.38), it is observed that DSTATCOM current at $(k+1)^{th}$ state depends on filter current, inverter output voltage and PCC voltage at k^{th} state. After calculating the filter currents, the cost function for current control is the difference between the reference and actual filter currents at $(k+1)^{th}$ state.

$$C_1 = \mid i_c^*(k+1) - i_c(k+1) \mid . \tag{4.39}$$

In the above equation, reference filter current at $(k+1)^{th}$ state is obtained from filter

currents at previous states using second order Lagrange extrapolation:

$$i_c^*(k+1) = 3i_c^*(k) - 3i_c^*(k-1) + i_c^*(k-2). \tag{4.40}$$

To limit the higher neutral leg switching frequency of FL-DSTATCOM, it is required to consider the difference between the present and previous switching state of the neutral leg as an additional constraint, which is,

$$C_2 = \mid S_n(k) - S_n(k-1) \mid . \tag{4.41}$$

A single cost function for current control and switching frequency reduction is formed by adding two individual cost functions (C_1, C_2) using a weighting factor (λ).

$$C = C_1 + \lambda C_2. \tag{4.42}$$

The compensation using MPC depends on λ and there is no particular method present to find the value of λ. However, traditional MCDM methods, simplify the weighting factor tuning by reducing the range from $(0 - \infty)$ to $(0 - 1)$. Therefore, in the proposed work, simplification of weighting factor selection is done using an MCDM method, namely TOPSIS. In this method, the best alternative from the available options should be closer to the negative ideal solution and far away from positive ideal solution. The step by step procedure of TOPSIS method is explained as follows.

4.2.4 Weighting factor simplification and cost function minimization using TOPSIS based MPC

The detailed procedure of simplification of weighting factor tuning and selection of optimal switching state using TOPSIS method is explained as follows.

Step 1: Initially both control parameters are evaluated for all switching states and they are represented as:

$$C_{PQ} = \begin{bmatrix} C_{11} & C_{12} \\ C_{21} & C_{22} \\ \vdots & \vdots \\ C_{p1} & C_{p2} \end{bmatrix}_{pq} \tag{4.43}$$

where 'p' represents the number of switching states which is equal to 16 and 'q' represents the number of individual cost functions which is equal to 2.

Step 2: Select the switching states which give minimum and maximum values among all available values for both the cost functions.

$$\begin{aligned} C_{m1} &= \min(C_{i1}); \quad C_{M1} = \max(C_{i1}), \\ C_{m2} &= \min(C_{i2}); \quad C_{M2} = \max(C_{i2}) \end{aligned} \tag{4.44}$$

where 'i' varies from 1 to 'p'.

Step 3: In this step normalized data is calculated from values obtained from step 1 and step 2, using the following formula.

$$X_{i1} = \sigma_1\left(\frac{C_{m1} - C_{i1}}{C_{m1} - C_{M1}}\right); \quad X_{i2} = \sigma_2\left(\frac{C_{m2} - C_{i2}}{C_{m2} - C_{M2}}\right). \tag{4.45}$$

The values σ_1 and σ_2 are depend on the relative importance of two individual cost functions and the sum of σ_1 and σ_2 should be always equal to one. Therefore, in the proposed work, the value of σ_1 is chosen as 0.9 and the value of σ_2 is chosen as 0.1.

Step 4: Select the positive and negative best values from the normalized data which is obtained from step 3.

$$\begin{aligned} X_{m1} &= \min(X_{i1}); \quad X_{M1} = \max(X_{i1}), \\ X_{m2} &= \min(X_{i2}); \quad X_{M2} = \max(X_{i2}) \end{aligned} \tag{4.46}$$

where, X_{m1}, X_{m2} are the negative best solutions and X_{M1}, X_{M2} are the positive best solutions.

Step 5: After obtaining the positive and negative best solutions from the normalized data, calculate the distance of each value from positive and negative best solutions.

$$D_i^+ = \sqrt{(X_{i1} - X_{M1})^2 + (X_{i2} - X_{M2})^2}, \quad D_i^- = \sqrt{(X_{i1} - X_{m1})^2 + (X_{i2} - X_{m2})^2}. \tag{4.47}$$

Step 6: In this step closeness coefficient (Q) to the negative ideal solution is calculated. Because, the switching state which is giving minimum current error and switching state error should be applied at the next instant.

$$Q = \frac{D_i^-}{D_i^+ + D_i^-}. \tag{4.48}$$

Step 7: In the last step, select a state which will give the minimum value of Q and it is applied to VSI of FL-DSTATCOM to compensate the current related power quality issues along with switching frequency reduction.

4.3 Simulation studies

The assessment of the proposed control algorithm is carried out using both simulation studies. Various parameters considered for the simulation studies are tabulated in Table. 4.2. Two different case studies are considered to evaluate the efficiency of the proposed control algorithm. In case-1, a three-phase diode bridge rectifier and a three-phase unbalanced *RL* load is connected. Similarly, in case-2, three single-phase diode bridge rectifiers and a balanced *RL* load is considered to achieve higher THD load currents.

4.3.1 Performance during case-1

Loads considered for case-1 are mentioned in Table. 4.2. In this case, simulation results are shown for 2 s. From (0 - 0.2) s, FL-DSTATCOM is not connected to the distribution system and is connected at 0.2 s. Fig. 4.4 shows the performance of FL-DSTATCOM before and after connecting it to the distribution system. From the figure, it is observed that, during (0 - 0.2) s, load currents and source currents are same and there are no compensating currents. At 0.2 s, FL-DSTATCOM is connected to PCC, so that source currents become balanced and sinusoidal. During (0 - 1) s, the cost function consists of only current control term as expressed in (4.39). At 1 s, the switching frequency reduction constraint is included in the cost function.

Fig. 4.5 shows the voltages and currents of DSTATCOM and distribution system after

Table. 4.2 Simulation parameters

Parameters	**Values**
Unbalanced and distorted supply voltage	V_{sa1} = 240 V, V_{sb1} = 0.8 × 240 V, V_{sc1} = 1.2 × 240 V. V_{sa5} = 0.2 × 240 V V_{sb5} = 0.24 × 240 V, V_{sc5} = 0.16 × 240 V.
Feeder impedance (Z_S)	0.07 Ω, 0.2 mH
Interfacing inductor (L_f)	5 mH
Neutral impedance (Z_{Sn})	(0.07+j0.0628) Ω
DC link (V_{dc}, C_{dc})	700 V, 5000 μF
Sampling time	10 μs
Load	Case-1 (a) Three-phase diode bridge rectifier feeding an *RL* load with *R*=12 Ω, *L*=50 mH on phase (b) Unbalanced linear load with R_a=5 Ω, L_a=50 mH (on phase-*a*) and R_b=10 Ω, L_b=50 mH (on phase-*b*) Case-2 (a) Three single-phase diode bridge rectifiers feeding *R*=5 Ω, *L*=150 mH (on phase-*a*), *R*=7 Ω, *L*=150 mH (on phase-*b*) and *R*=6 Ω, *L*=150 mH (on phase-*c*). (b) Balanced linear load with *R* =15 Ω, *L* = 30 mH.

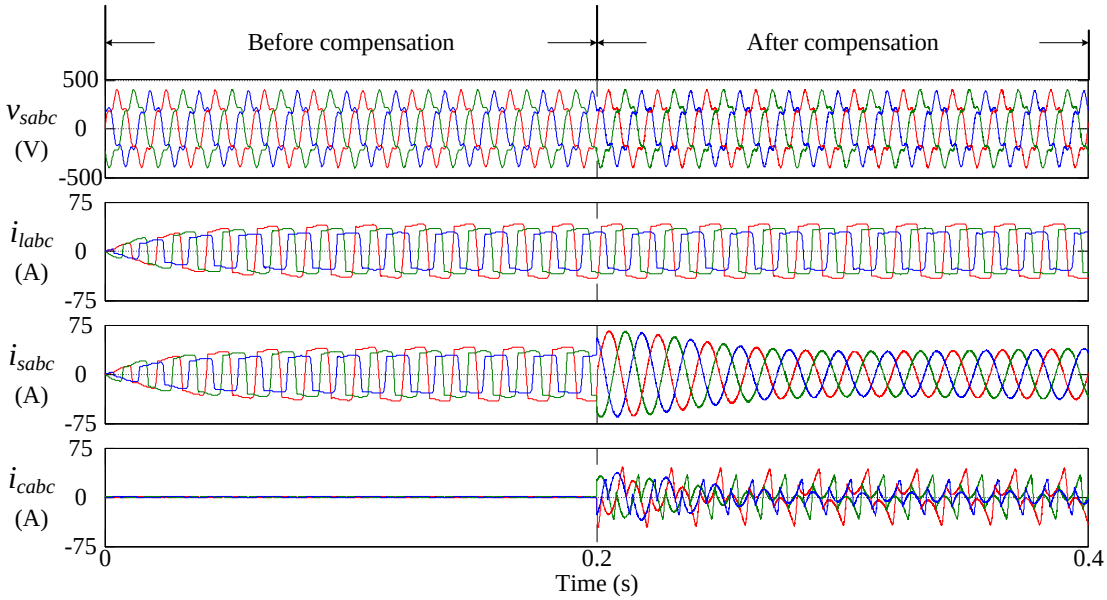


Fig. 4.4 Voltages and currents before and after connecting the FL-DSTATCOM.

including the switching frequency reduction constraint in the cost function. The rms values of PCC voltages are 239.3 V, 213.8 V and 261.7 V; similarly, the % distortions are 20.29, 24.84 and 16.62, indicating that the PCC voltages are unbalanced and distorted. The rms values of load currents are 43.16 A, 34.66 A and 35.38 A, with THDs 16.11%, 22.81% and 17.34%, respectively. It is observed that the load currents are non-linear and unbalanced. After compensation, the rms values of source currents are

31.65 A, 31.64 A and 31.64 A, with THDs 1.68%, 1.54% and 1.57% indicate that the source currents become balanced and sinusoidal, which can be observed from Fig. 4.5. The average switching frequencies of upper switches in each leg are measured and the values are given in Table. 4.3. In the same table, rms values and THDs of PCC voltages, load currents and source currents are also given. From the table it is evident that the switching frequency of the neutral leg switch is very high compared to phase leg switch. After including switching frequency reduction constraint at 1s, the switching frequency of the neutral leg is reduced from 29,690 Hz to 11,039 Hz. As mentioned the reduction in neutral leg switching frequency will also reduce the frequencies of phase legs and the reduced values are given in Table. 4.3.

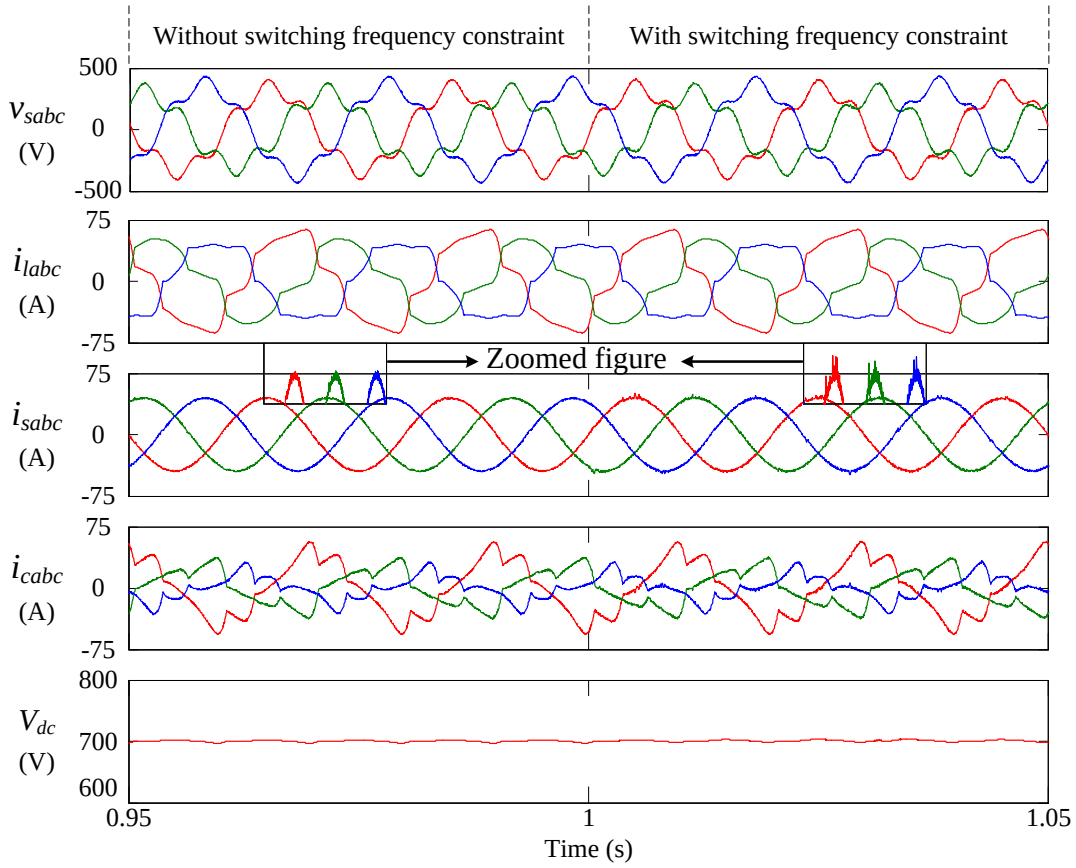


Fig. 4.5 Voltages and currents without and with additional constraint during case-1.

Fig. 4.6 shows neutral currents of load, DSTATCOM and source. From this figure it is observed that, source neutral current is almost zero during both single and multiple constraint cost functions. From the zoomed figure it is observed that, even though the tracking accuracy is reduced, there is no considerable variation in the neutral current. During the entire operation, the dc link voltage is maintained constant (equal to 700 V) and it is shown in Fig. 4.5.

Table. 4.3 Parameters without and with additional constraint during case-1

Parameters	With single constraint (0-1) s	with two constraints (1-2) s
v_{sa} (V, THD)	239.3 (20.29%)	239.2 (20.31%)
v_{sb} (V, THD)	213.8 (24.84%)	213.8 (24.87%)
v_{sc} (V, THD)	261.7 (16.62%)	261.6 (16.63%)
i_{la} (A, THD)	43.16 (16.11%)	43.16 (16.11%)
i_{lb} (A, THD)	34.66 (22.81%)	34.66 (22.81%)
i_{lc} (A, THD)	35.38 (17.34%)	35.38 (17.34%)
i_{sa} (A, THD)	31.65 (1.68%)	31.74 (2.68%)
i_{sb} (A, THD)	31.64 (1.54%)	31.53 (2.08%)
i_{sc} (A, THD)	31.63 (1.57%)	31.7 (2.25%)
S_a (Hz)	20,765	14,841
S_b (Hz)	22,695	14,561
S_c (Hz)	19,317	13,333
S_n (Hz)	29,690	11,039

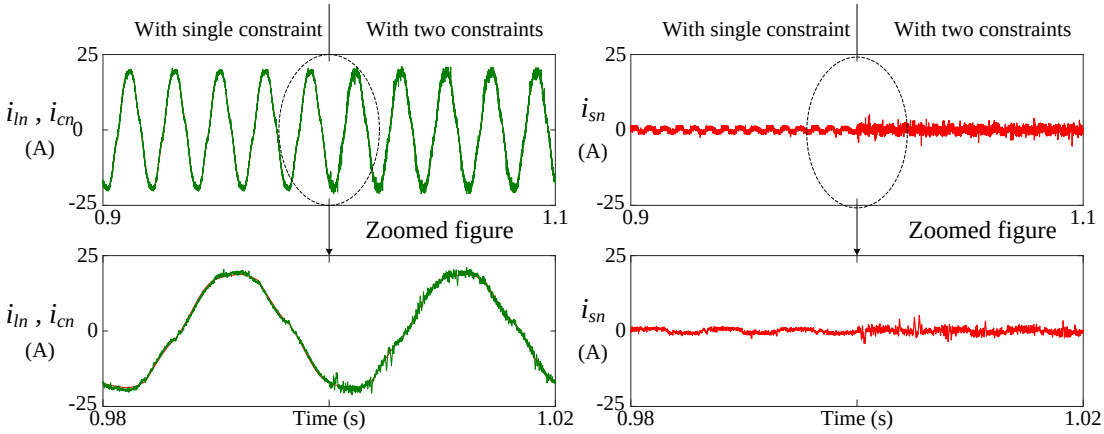


Fig. 4.6 Neutral currents without and with additional constraint during case-1.

4.3.2 Performance during case-2

The performance of the proposed control algorithm is further evaluated for load currents with higher unbalance and higher THDs. Loads considered in case-2 are mentioned in Table. 4.2. RMS values as well as THDs of PCC voltages, load currents, source currents and switching frequencies of each leg are given in Table. 4.4 for both single and multiple constraint cost functions. It is observed that the source currents are balanced and sinusoidal even though the supply voltages and load currents are unbalanced and distorted. It is also observed that the switching frequency of neutral leg is 27,752 Hz which is high. After adding additional constraint switching frequency is reduced to 10,108 Hz. The switching losses for each phase without and after including the switching frequency reduction constraint are also shown in Table. 4.4. It is observed that, the reduction in switching frequency leads to reduction in switching losses. Neutral

currents of load, DSTATCOM and source are shown in Fig. 4.7 and it is observed that the number of switching pulses are reduced after adding switching frequency reduction constraint. Similarly, source neutral current is almost zero during both single and multiple constraints.

Table. 4.4 Parameters without and with additional constraint during case-2

Parameters	With single constraint (0-1) s	With two constraints (1-2) s
v_{sa} (V, THD)	239.3 (20.79%)	239.2 (20.31%)
v_{sb} (V, THD)	213.8 (24.84%)	213.8 (24.87%)
v_{sc}(V, THD)	261.7 (16.62%)	261.6 (16.63%)
i_{la} (A, THD)	35.96 (34.86%)	35.96 (34.86%)
i_{lb} (A, THD)	30.5 (37.33%)	30.5 (37.33%)
i_{lc}(A, THD)	25.1 (38.70%)	25.1 (38.70%)
i_{sa} (A, THD)	29.61 (1.75%)	29.64 (2.15%)
i_{sb} (A, THD)	29.63 (1.80%)	29.69 (2.14%)
i_{sc}(A, THD)	29.5 (1.78%)	29.49 (2.14%)
S_a (Hz)	21,992	17,908
S_b (Hz)	21,561	17,378
S_c (Hz)	21,963	15,380
S_n (Hz)	27,752	10,108
SL_a (W)	253	193
SL_b (W)	174	124
SL_c (W)	133	97
SL_n (W)	745	245
Total (W)	1305	660

*where SL is the switching loss.

The simulation results of case-1 and case-2 indicate that the proposed control algorithm achieves balanced and sinusoidal source currents, irrespective of the distortion in either source or load. It is also reduced the switching frequency of the neutral leg which further reduces the switching frequencies of the phase legs without increasing the source neutral current.

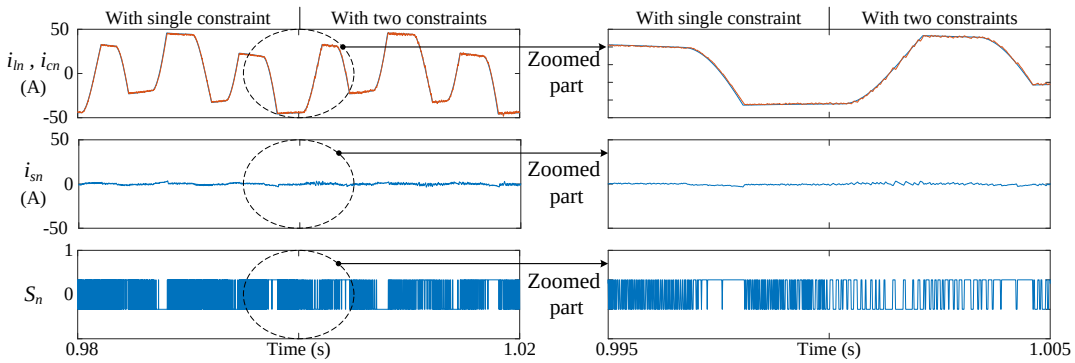


Fig. 4.7 Neutral currents without and with additional constraint during case-2

4.4 Experimental studies

The effectiveness of the proposed control algorithm is also evaluated from experimental studies. Three-phase unbalanced and distorted supply is required to establish for the experimental prototype. The unbalanced and distorted supply is created using a combination of three-phase auto transformer, three single-phase auto transformers, three-phase diode bridge rectifier and three inductors. The connection diagram of unbalanced and distorted supply is shown in Fig. 4.8. Initially, three single-phase auto transformers are supplied by a three-phase auto transformer. Then the three single-phase transformers are maintained at unequal voltages to get unbalanced supply. The unbalanced three phase supply is connected to a three-phase diode bridge rectifier feeding a resistive load through commutation inductors. The terminal points of the inductors are as shown in Fig. 4.8, which provides the required unbalanced and distorted supply for the experimental study. The other required parameters for experimental study are mentioned in Table. 4.5. Current and voltage sensors are used to sense the load currents, DSTATCOM currents and PCC voltages. The sensed signals are send to dSPACE MicroLabBox 1202 which is connected to a personnel computer (PC). After receiving the sensed signals in PC, the proposed control algorithm is implemented in dSPACE real time software. Finally, the generated gate pulses are given to FL-DSTATCOM using dSPACE MicroLabBox 1202.

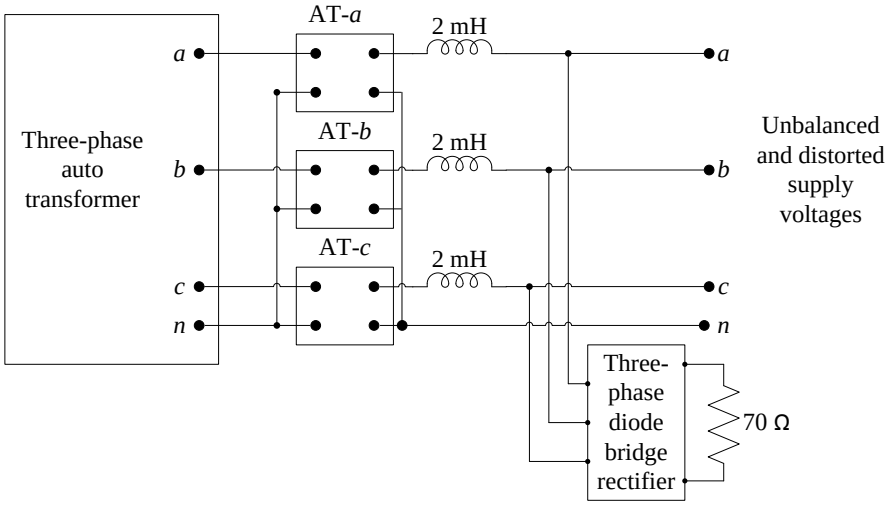


Fig. 4.8 Realization of three-phase unbalanced and distorted supply.

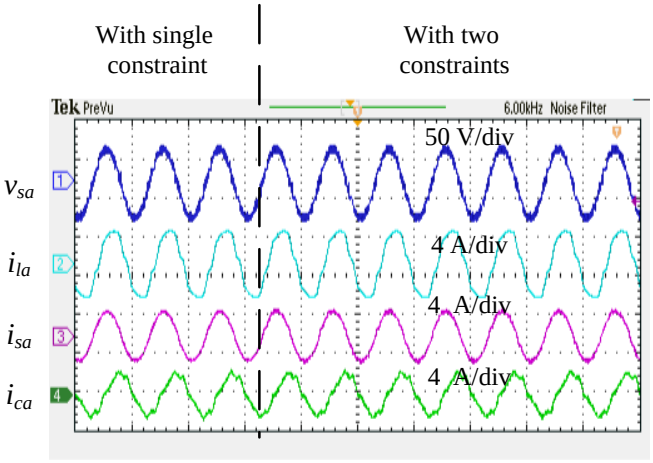
Fig. 4.9 shows the experimental results of PCC voltages, load currents and source currents. Fig. 4.9 (a), (b) and (c) shows results for phase-*a*, phase-*b* and phase-*c* respec-

Table. 4.5 Experimental parameters

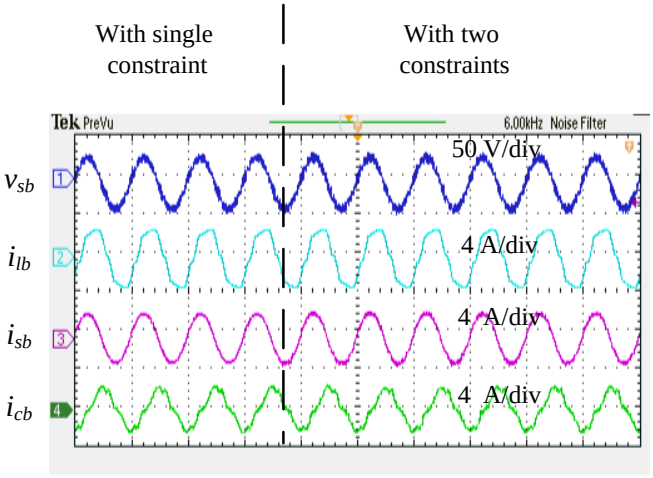
Parameters	Value
Unbalanced supply voltage	$V_{sa} = 28 \times 1.25$ V, $V_{sb} = 28$ V, $V_{sc} = 28 \times 0.75$ V
Interfacing inductance (L_f)	9 mH
DC link capacitance (C_{dc})	4700 μF
DC link voltage (V_{dc})	90 V
Load-1	Three-phase diode bridge rectifier load with 30 Ω, 150mH
Load-2	unbalanced linear load Phase-a : 18 Ω, 75 mH Phase-b : 18 Ω, 50 mH Phase-c : 18 Ω, 100 mH

tively. From the figure, it is observed that, even though the cost function varies from single constraint to multiple constraint, there is not much variation in the performance of the proposed control algorithm. Fig. 4.10 shows PCC voltages, load currents and source currents of three phases. In Fig. 4.10 (a) voltage scaling is 20 V/div., similarly, in Fig. 4.10 (b), (c) current scaling is 1 A/div. It is observed from Fig. 4.10 (a) that the supply voltage is unbalanced and distorted. Fig. 4.10 (b) shows that load currents are non-linear and unbalanced. After compensation, the source currents becomes balanced, sinusoidal and it can be observed from Fig. 4.10 (c).

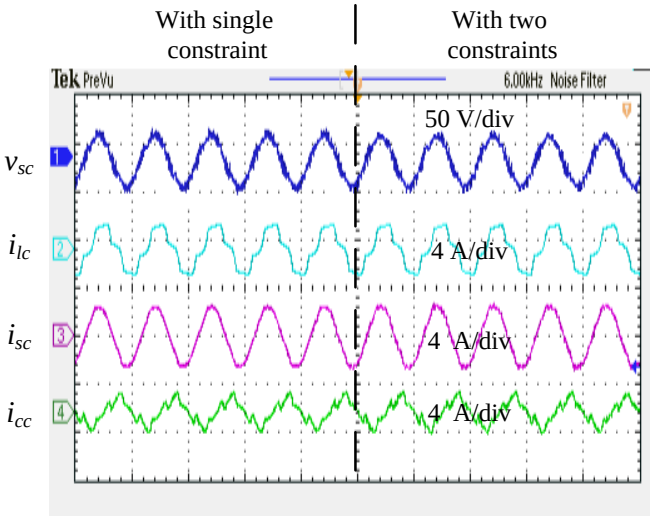
Fig. 4.11 shows the switching frequencies of neutral leg along with individual phases. The frequencies of phase-a, phase-b and phase-c with single constraint cost function are 4,785 Hz, 4,366 Hz and 4,711 Hz and they are shown in Fig. 4.11 (a), (b) and (c) respectively. The neutral leg switching frequency shown in Fig. 4.11 (d) is 5,770 Hz which is high compared to phase legs. The THD of source currents without switching frequency constraint are shown in Fig. 4.12. From the figure, it is observed that, the THD of source currents are 3.7%, 3.6% and 3.5% with only current control. The higher neutral leg frequency is reduced by adding an additional constraint to the cost function. The reduced neutral leg switching frequency is 2,661 Hz which is 53% less when compared to single constraint case. The reduction in neutral leg switching frequency will also reduce switching frequency of phase legs. The reduced phase leg switching frequencies are 2,703 Hz, 2,794 Hz and 2,691 Hz for phase-a, phase-b and phase-c respectively. Switching frequencies after adding additional constraints are shown in Fig. 4.13. The THD of source currents with switching frequency constraint are shown in Fig. 4.14. It is observed that, after adding switching frequency constraint the THDs are



(a)



(b)

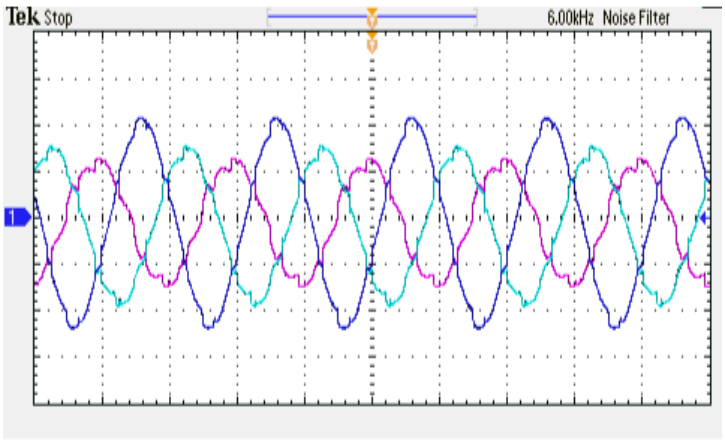


(c)

Fig. 4.9 Voltages and currents with single and two constraints of (a) Phase-*a* (b) Phase-*b*, and (c) Phase-*c*.

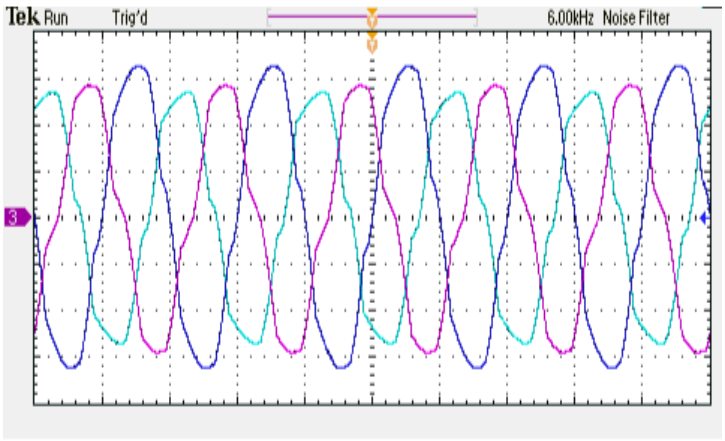
4.2%, 4.1% and 4.0% which are within the limits set by IEEE-519 standards (less than 5%).

v_{sabc}
(V)



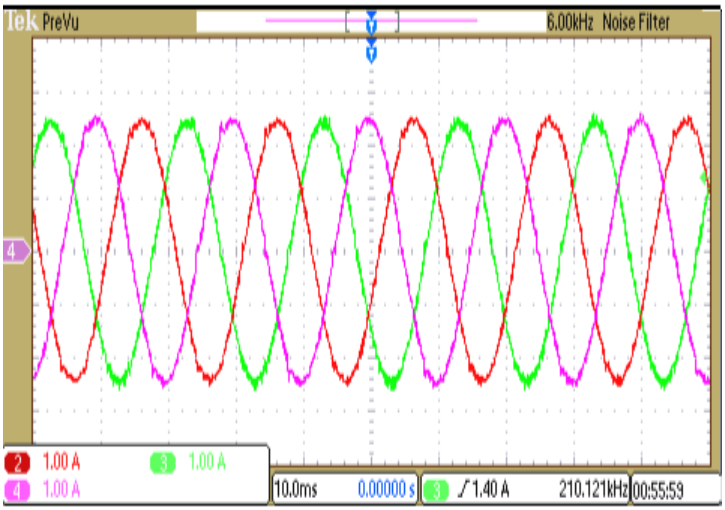
(a)

i_{labc}
(A)



(b)

i_{sabc}
(A)



(c)

Fig. 4.10 Experimental waveforms of (a) Unbalanced and distorted PCC voltages (b) Unbalanced and distorted load currents, and (c) Balanced and sinusoidal source currents.

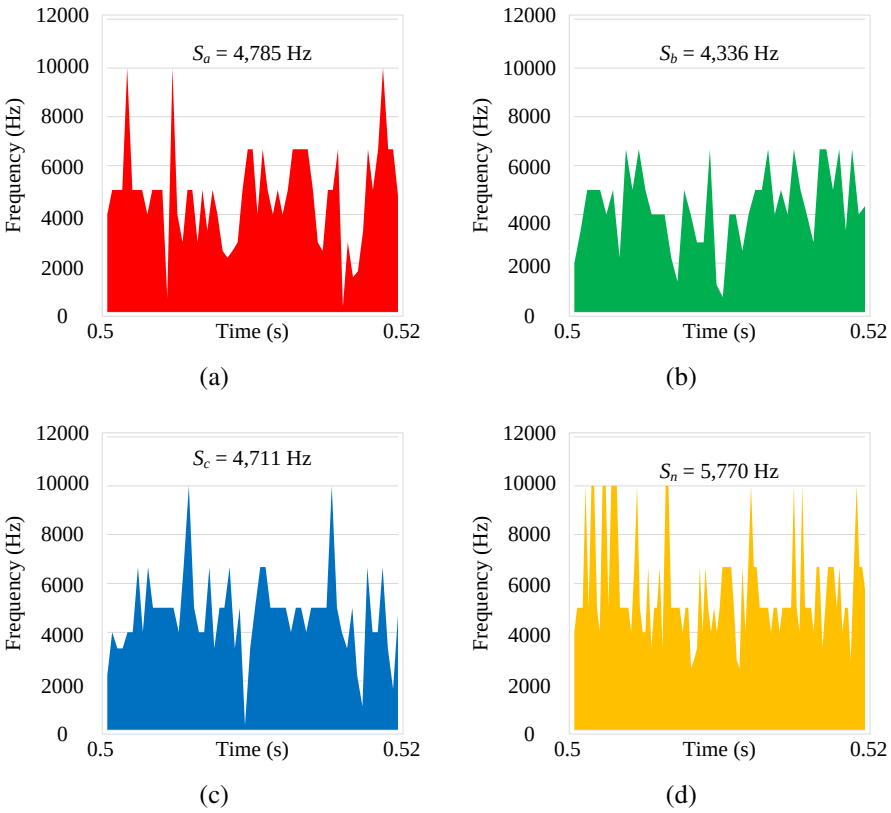


Fig. 4.11 Switching frequencies with current control (a) Phase-*a* (b) Phase-*b* (c) Phase-*c*, and (d) Neutral leg.

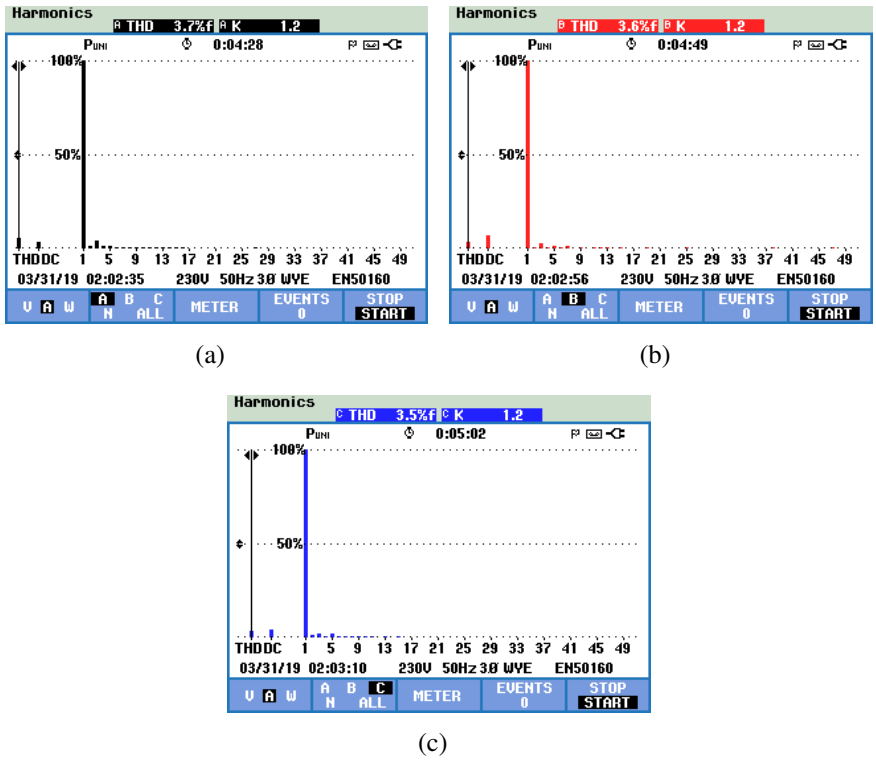


Fig. 4.12 Source currents THD with only current control (a) Phase-*a* (b) Phase-*b*, and (c) Phase-*c*.

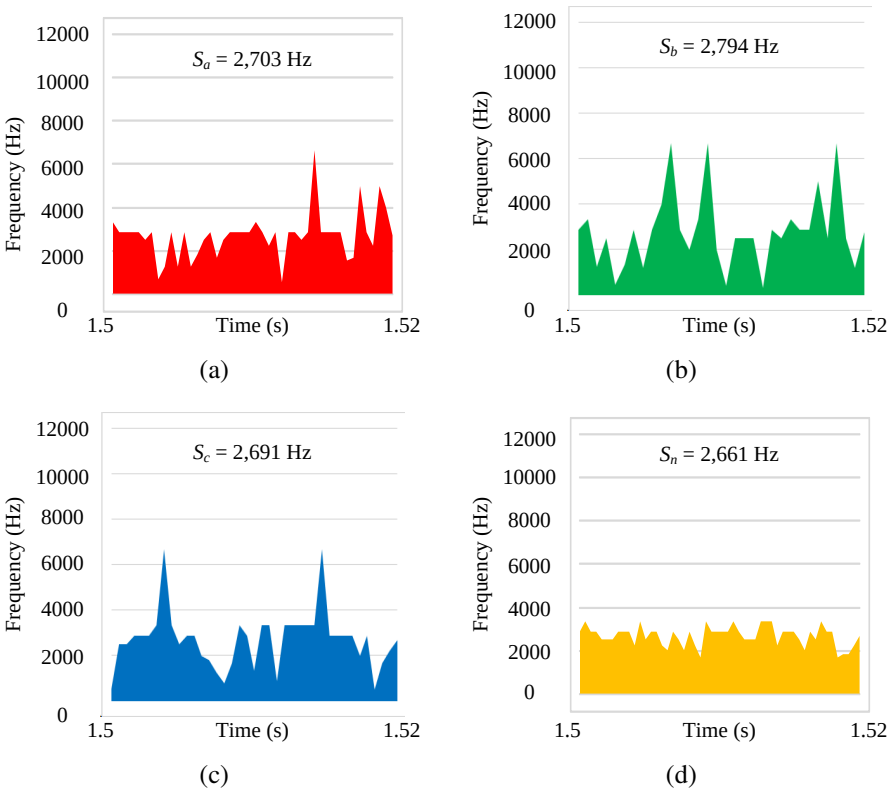


Fig. 4.13 Switching frequencies after including switching frequency reduction constraint (a) Phase-*a* (b) Phase-*b* (c) Phase-*c*, and (d) Neutral leg.

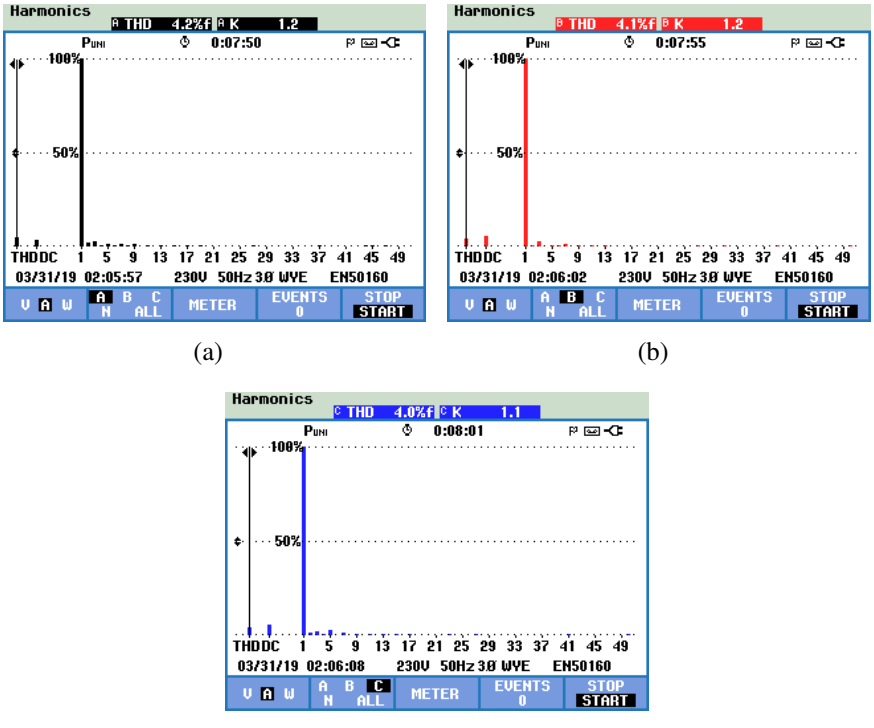


Fig. 4.14 THD of source currents during current control along with switching frequency reduction (a) Phase-*a* (b) Phase-*b*, and (c) Phase-*c*.

4.5 Summary

This chapter dealt primarily with compensation of current related power quality issues using FL-DSTATCOM and neutral leg switching frequency reduction of FL-DSTATCOM. The summary of the proposed work is as follows:

1. The complexity in the extraction of reference currents during unbalance and distorted supply conditions is reduced using state observers, theory of symmetrical components and conductance factors.

2. After extracting the reference currents, the difference between reference and actual currents is considered as a single constraint cost function to compensate current related power quality issues.

3. However, the higher neutral leg switching frequency, which is one of the limitations of FL-DSTATCOM urges one to consider switching frequency term as an additional constraint which makes a single constraint cost function as a multi constraint cost function.

4. Finally, the complexity in the weighting factor tuning for optimal switching state selection during multi constraint case is simplified using TOPSIS method by reducing its range from $(0 - \infty)$ to $(0 - 1)$.

CHAPTER 5

Model Predictive Control with Constant Switching Frequency for Four Leg DSTATCOM Using Three Dimensional Space Vector Modulation

Model predictive control (MPC) has the limitation of variable switching frequency and in most of the times the values are high and unequal. This leads to uneven stress across the switches and increase the switching losses. Therefore, in this chapter, constant switching frequency MPC is proposed for FL-DSTATCOM using three dimensional space vector modulation (3DSVM) to compensate the power quality issues.

5.1 Introduction

The advantages of model predictive control are convenience of adding additional control parameters and their treatment according to the importance, elimination of proportional and integral (PI) controllers, good transient and steady state performance. These features of MPC attracted the researchers towards its adaptation in DSTATCOM controllers [56], [57], [84], [85]. However, variable switching frequency limitation of MPC leads to uneven stress across switches and also higher switching losses [86].

Initially, a constant and user defined switching frequency hysteresis current control method is proposed in [86] for FL-DSTATCOM, but in this method additional constraints can not be incorporated. Switching frequency regulation of three-leg inverter is achieved by measuring and controlling the switching period, but this method cannot achieve constant switching frequency [87]. To achieve constant switching frequency, modulated MPC for a direct matrix converter is proposed in [88] and indirect matrix converter is proposed in [89], however these methods are not applicable to four leg inverters to achieve constant switching frequency. A neutral point clamped converter (NPC) is controlled by using fixed switching frequency MPC [90], but this topology

require higher number of switching components and not suitable for low power applications. In general, conventional sliding mode control is variable switching frequency control technique, however to overcome this limitation a fixed switching frequency sliding mode control technique is proposed for four leg inverter in [91]. In [92], a constant switching frequency MPC technique is proposed for three-phase inverter topology for DSTATCOM applications, in which the concept of conventional two dimensional space vector modulation (2DSVM) is used. Inverter topology used in [92], cannot compensate the unbalanced load currents due to the absence of fourth leg. The phase voltages of FL-DSTATCOM are not decoupled unlike three-phase split-capacitor (TPSC) topology, hence the application of 2DSVM is not possible. Therefore, in this chapter, constant switching frequency MPC for FL-DSTATCOM is achieved using the concept of three dimensional space vector modulation (3DSVM).

5.2 MPC algorithm with constant switching frequency

The schematic diagram of FL-DSTATCOM connected distribution system is shown in Fig. 5.1. The output of the inverter is connected through an interfacing inductors to eliminate switching harmonics in FL-DSTATCOM currents. Non-linear and unbalanced loads are connected to the supply to verify the efficacy of the proposed control

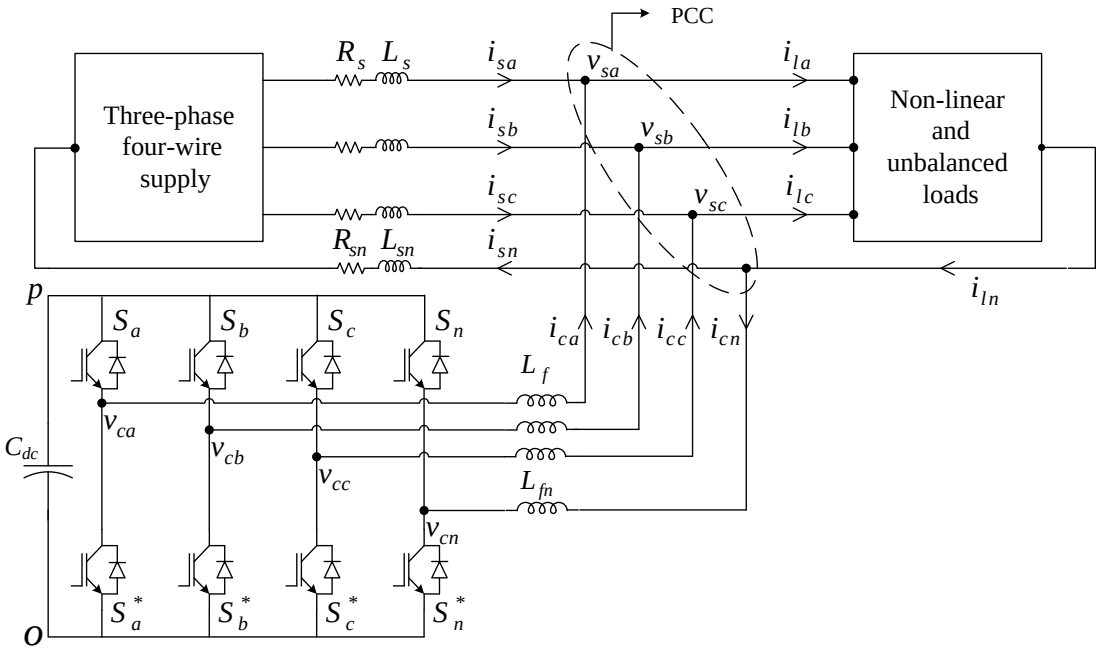


Fig. 5.1 Schematic diagram of FL-DSTATCOM connected distribution system.

algorithm. The operation of any DSTATCOM topology involves two main tasks. The first one is the selection of control algorithm for reference current generation and the other one is generation of switching pulses to operate the inverter as a controlled current source. In this work, synchronous reference frame (SRF) theory is used to generate reference DSTATCOM currents (i^*_{cabc}) from the unbalanced and non-linear load currents. MPC is used to generate switching pulses by comparing the actual currents with the reference currents.

5.2.1 Predictive model of FL-DSTATCOM

The schematic diagram of the complete control algorithm is shown in Fig. 5.2. Switching pulse generation using MPC involves the selection of switching state which minimizes the cost function. The primary objective of FL-DSTATCOM is to achieve source currents balanced, sinusoidal and in-phase with the voltage at the PCC. Therefore, cost function is considered as the difference between reference (i^*_{cabc}) and actual DSTATCOM currents (i_{cabc}). Reference DSTATCOM currents at $(k+1)^{th}$ state are obtained by applying the second order Lagrange's extrapolation to the currents obtained from SRF theory. Similarly, the model of DSTATCOM is used to estimate the actual currents at $(k+1)^{th}$ state (i.e., $i_{cabc}(k+1)$). The estimation of $i_{cabc}(k+1)$ starts by applying, KVL between the nodes v_c and v_s in Fig. 5.1.

$$v_c = L_f \frac{\mathrm{d}i_c}{\mathrm{d}t} + v_s. \tag{5.1}$$

In the above equation, v_c represents the inverter output voltage which is measured with respect to the mid-point of the fourth leg and it is completely dependent on switching states of the inverter. Switching states and their respective normalized voltages are given in Table. 5.1. The voltage of each phase at PCC is represented asv_s and it is measured with respect to source neutral. Solving (5.1) for $\frac{\mathrm{d}i_c}{\mathrm{d}t}$,

$$\frac{\mathrm{d}i_c}{\mathrm{d}t} = \frac{v_c - v_s}{L_f}. \tag{5.2}$$

According to Forward Euler's approximation method,

$$\frac{\mathrm{d}i_c}{\mathrm{d}t} = \frac{i_c(k+1) - i_c(k)}{T_s}. \tag{5.3}$$

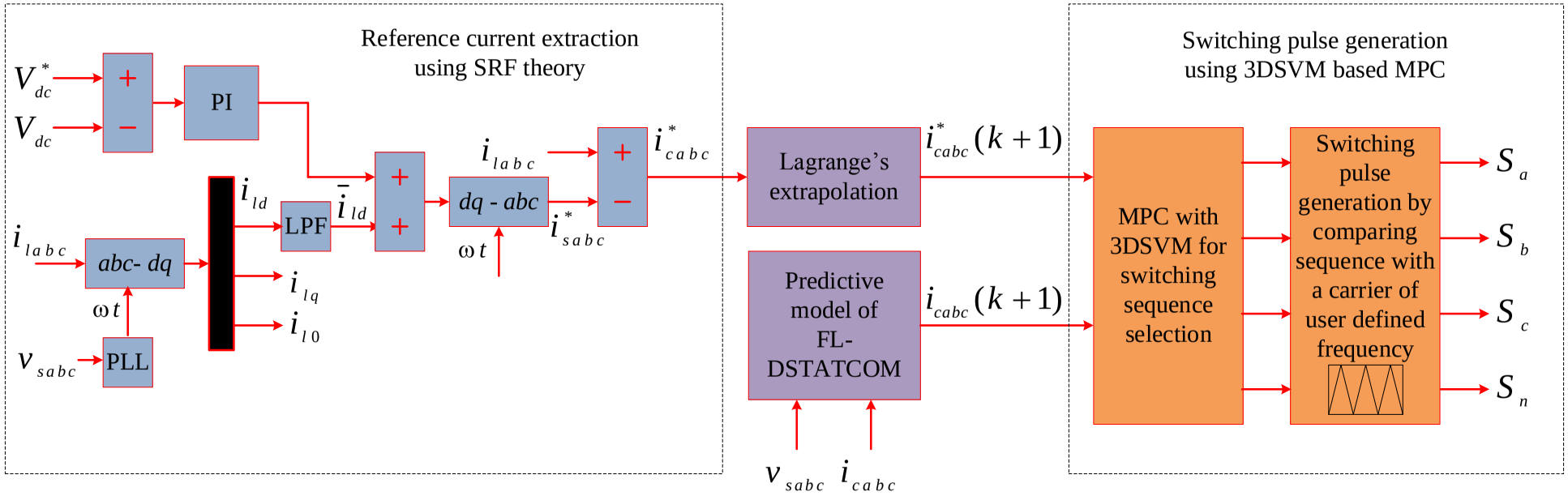


Fig. 5.2 Reference current extraction using SRF and switching pulse generation using MPC.

Table. 5.1 Switching states and voltage vectors of FL-DSTATCOM

State	S_a	S_b	S_c	S_n	v_{can}	v_{cbn}	v_{ccn}	Vector
1	0	0	0	0	0	0	0	V_1
2	0	0	0	1	-1	-1	-1	V_2
3	0	0	1	0	0	0	1	V_3
4	0	0	1	1	-1	-1	0	V_4
5	0	1	0	0	0	1	0	V_5
6	0	1	0	1	-1	0	-1	V_6
7	0	1	1	0	0	1	1	V_7
8	0	1	1	1	-1	0	0	V_8
9	1	0	0	0	1	0	0	V_9
10	1	0	0	1	0	-1	-1	V_{10}
11	1	0	1	0	1	0	1	V_{11}
12	1	0	1	1	0	-1	0	V_{12}
13	1	1	0	0	1	1	0	V_{13}
14	1	1	0	1	0	0	-1	V_{14}
15	1	1	1	0	1	1	1	V_{15}
16	1	1	1	1	0	0	0	V_{16}

Substitute, (5.3) in (5.2) to get DSTATCOM currents at $(k+1)^{th}$ state and it is given as,

$$i_c(k+1) = \frac{(v_c - v_s)T_s}{L_f} + i_c(k). \tag{5.4}$$

Therefore, in conventional MPC, cost function will be the difference between reference and actual DSTATCOM currents and it can be expressed as,

$$C = |i^*_{ca}(k+1) - i_{ca}(k+1)| + |i^*_{cb}(k+1) - i_{cb}(k+1)| + |i^*_{cc}(k+1) - i_{cc}(k+1)|. \tag{5.5}$$

For each available switching state calculate the value of $i_c(k+1)$ and find the cost function value. Among the available switching states, the state which gives the minimum value of C is applied for the next sampling to achieve proper control of FL-DSTATCOM. Using this method, the switches of FL-DSTATCOM will operate with variable switching frequency [84], [85]. To overcome this limitation, a constant and user defined switching frequency MPC is proposed in this chapter and explained in next section.

5.2.2 MPC with 3DSVM to achieve constant switching frequency

The concept of 3DSVM is proposed in [93]. In this thesis this concept is extended to achieve constant and user defined switching frequency MPC for FL-DSTATCOM. There are two different methods available to implement 3DSVM, based on the type of reference frame used. Between them, one uses $\alpha\beta\gamma$ frame [94] and the other is *abc* frame [95]. However, the method using $\alpha\beta\gamma$ involves complex calculations and difficult to implement [95]. Therefore, in the proposed work, 3DSVM is implemented in *abc* coordinates, which simplifies the selection of tetrahedron and switching sequence.

In conventional 2DSVM, all the switching vectors form a hexagonal shape. Similarly, in 3DSVM, available 16 switching states form into a dodecahedron as shown in Fig. 5.3. The dodecahedron can be further divided into 24 tetrahedrons. Each tetrahedron is formed by using 3 active vectors and two zero vectors. Tetrahedrons and their associated active voltage vectors are given in Table. 5.2. In this table, TH represents tetrahedron and VV represents voltage vectors. The procedure of proposed control algorithm is explained below.

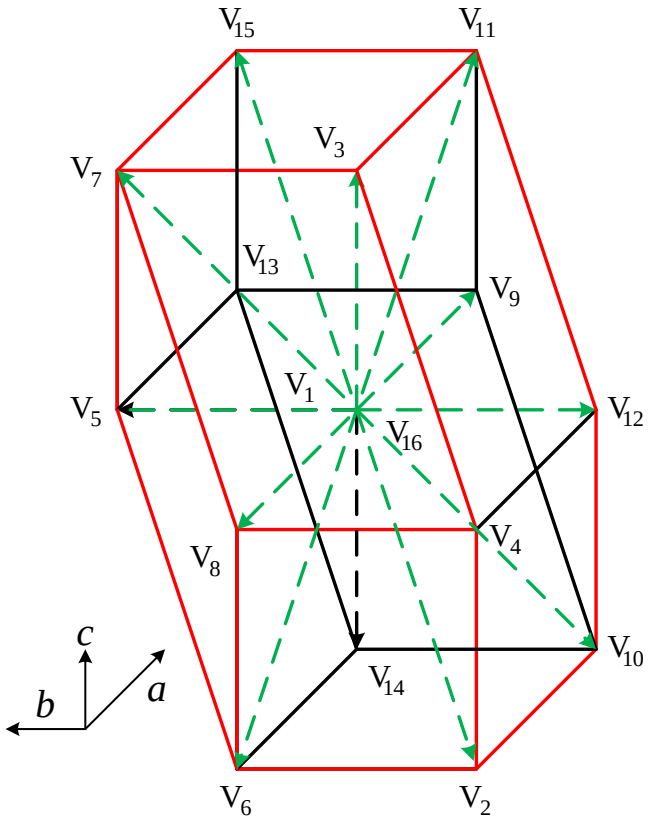


Fig. 5.3 Dodecahedron of all the voltage vectors.

Table. 5.2 Tetrahedrons and their associated voltage vectors of dodecahedron

TH	VV1	VV2	VV3	TH	VV1	VV2	VV3
1	V_9	V_{13}	V_{15}	13	V_9	V_{10}	V_{14}
2	V_5	V_{13}	V_{15}	14	V_2	V_{10}	V_{14}
3	V_5	V_7	V_{15}	15	V_2	V_6	V_{14}
4	V_5	V_7	V_8	16	V_2	V_6	V_8
5	V_9	V_{13}	V_{14}	17	V_9	V_{11}	V_{12}
6	V_5	V_{13}	V_{14}	18	V_3	V_{11}	V_{12}
7	V_5	V_6	V_{14}	19	V_3	V_4	V_{12}
8	V_5	V_6	V_8	20	V_3	V_4	V_8
9	V_9	V_{11}	V_{15}	21	V_9	V_{10}	V_{12}
10	V_3	V_{11}	V_{15}	22	V_2	V_{10}	V_{12}
11	V_3	V_7	V_{15}	23	V_2	V_4	V_{12}
12	V_3	V_7	V_8	24	V_2	V_4	V_8

1. Initially, calculate the value of cost function (C) using (5.5) for all 16 switching states.

$$C = [C_i]^T \quad \text{(where, } i = 1 : 16) \tag{5.6}$$

2. Using the cost function value of each voltage vector, calculate the duty cycles of associated voltage vectors in each tetrahedron. In each tetrahedron, the voltage vector with minimum C value has to be applied for higher duration and maximum C value to be applied for least duration. Therefore, the cost function value and the duty values are inversely proportional to each other. The equation used to calculate the duty values of zero vector (d_0) and active vectors (d_1,d_2 and d_3) are given as:

$$\begin{aligned}
\frac{1}{d_0(i)} &= C_{VV0}\left(\frac{1}{C_{VV0}} + \frac{1}{C_{VV1}} + \frac{1}{C_{VV2}} + \frac{1}{C_{VV3}}\right),\\
\frac{1}{d_1(i)} &= C_{VV1}\left(\frac{1}{C_{VV0}} + \frac{1}{C_{VV1}} + \frac{1}{C_{VV2}} + \frac{1}{C_{VV3}}\right),\\
\frac{1}{d_2(i)} &= C_{VV2}\left(\frac{1}{C_{VV0}} + \frac{1}{C_{VV1}} + \frac{1}{C_{VV2}} + \frac{1}{C_{VV3}}\right),\\
\frac{1}{d_3(i)} &= C_{VV3}\left(\frac{1}{C_{VV0}} + \frac{1}{C_{VV1}} + \frac{1}{C_{VV2}} + \frac{1}{C_{VV3}}\right).
\end{aligned} \tag{5.7}$$

In (5.7), i value varies from 1 to 24 (total 24 tetrahedrons), C_{VV0}, C_{VV1}, C_{VV2} and C_{VV3} represent the cost function values of zero voltage vector and three active vectors of a tetrahedron. To understand equation (5.7), tetrahedron 1 is taken as an example and duty cycle calculation of the associated voltage vectors V_1, V_9,

V_{13} and V_{15} are given here.

$$\begin{aligned} d_0 &= \frac{C_9C_{13}C_{15}}{C_1C_9C_{13} + C_9C_{13}C_{15} + C_{13}C_{15}C_1 + C_{15}C_1C_9}, \\ d_1 &= \frac{C_1C_{13}C_{15}}{C_1C_9C_{13} + C_9C_{13}C_{15} + C_{13}C_{15}C_1 + C_{15}C_1C_9}, \\ d_2 &= \frac{C_9C_1C_{15}}{C_1C_9C_{13} + C_9C_{13}C_{15} + C_{13}C_{15}C_1 + C_{15}C_1C_9}, \\ d_3 &= \frac{C_9C_{13}C_1}{C_1C_9C_{13} + C_9C_{13}C_{15} + C_{13}C_{15}C_1 + C_{15}C_1C_9}. \end{aligned} \tag{5.8}$$

Where, C_1, C_9, C_{13} and C_{15} represents the cost function values of voltage vectors V_1, V_9, V_{13} and V_{15}.

3. Calculate the new cost function (G) for each tetrahedron using duty cycle values and the cost function values of associated voltage vectors.

$$G_i = d_1(i)C_{VV1} + d_2(i)C_{VV2} + d_3(i)C_{VV3}. \tag{5.9}$$

Then, select the tetrahedron which has minimum G value and use the associated vectors to generate the switching sequence.

4. Pickup the switching sequence using Table. 5.1, for each switch depending on the selected tetrahedron and the voltage vectors. Each sequence is always started by a zero vector followed by three active vectors. For example, if the tetrahedron 1 is giving the minimum cost function value, the switching sequence will be $V_1 - V_9 - V_{13} - V_{15} - V_{16} - V_{15} - V_{13} - V_9 - V_1$. The pictorial representation of the switching sequence is shown in Fig. 5.4.

5. Finally, compare each switching sequence with a triangular carrier signal of constant switching frequency, to generate the switching pulses for FL-DSTATCOM.

Table. 5.3 shows the duty values and G values of each tetrahedron in a sample time. From this table, it is observed that, minimum value of G is obtained for tetrahedron 7 and it is shown with bold letters. Therefore, the associated voltage vectors V_1, V_5, V_6 and V_{14} are used to generate the switching sequence. The flowchart of the switching sequence generation using 3DSVM is provided in Fig. 5.12. The validation of the proposed work is carried out using simulation and experimental studeis.

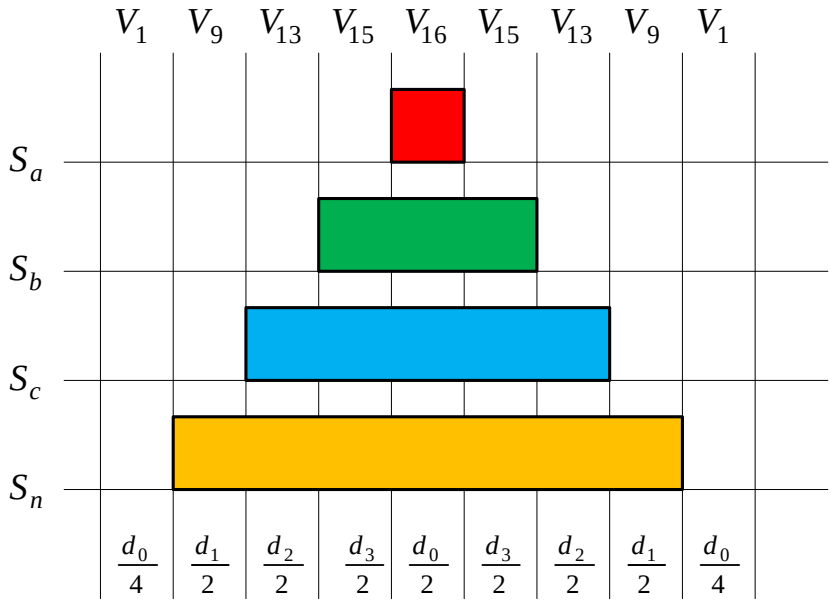


Fig. 5.4 Switching sequence for tetrahedron 1.

Table. 5.3 Example for tetrahedron selection using 3DSVM based MPC

TH	d_0	d_1	d_2	d_3	*G*
1	0.5318	0.1034	0.1414	0.2234	2.5679
2	0.3954	0.3335	0.1051	0.1661	1.909
3	0.3675	0.3099	0.1682	0.1544	1.7744
4	0.3817	0.322	0.1748	0.1215	1.8433
5	0.5318	0.1034	0.1414	0.2234	2.5679
6	0.3954	0.3335	0.1051	0.1661	1.909
7	**0.3663**	**0.309**	**0.1709**	**0.1539**	**1.7687**
8	0.3805	0.3209	0.1775	0.1211	1.8372
9	0.5318	0.1034	0.1414	0.2234	2.5679
10	0.4574	0.2289	0.1216	0.1921	2.2086
11	0.4205	0.2104	0.1925	0.1766	2.0303
12	0.4393	0.2198	0.2011	0.1398	2.1211
13	0.5318	0.1034	0.1414	0.2234	2.5679
14	0.4552	0.2325	0.121	0.1912	2.1982
15	0.4171	0.2131	0.1946	0.1752	2.1041
16	0.4356	0.2225	0.2032	0.1386	2.1034
17	0.5318	0.1034	0.1414	0.2234	2.5679
18	0.4574	0.2289	0.1216	0.1921	2.2086
19	0.4427	0.2215	0.1498	0.186	2.1378
20	0.4636	0.232	0.1568	0.1476	2.2387
21	0.5318	0.1034	0.1414	0.2234	2.5679
22	0.4552	0.2325	0.121	0.1912	2.1982
23	0.4407	0.2251	0.1491	0.1851	2.128
24	0.4614	0.2357	0.1561	0.1469	2.228

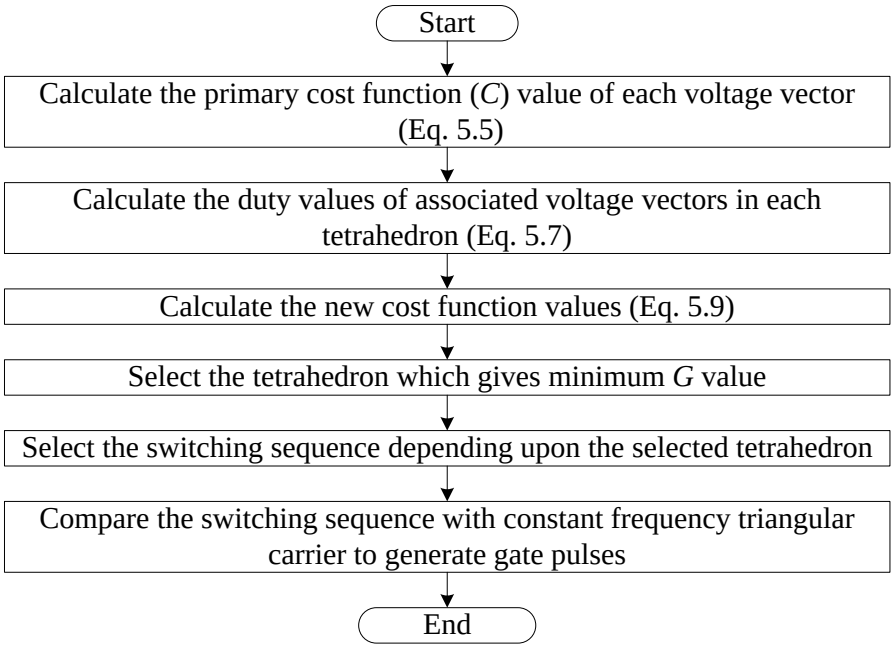


Fig. 5.5 Flowchart of switching pulse generation using 3DSVM.

5.3 Simulation studies

Parameters considered for the simulation studies are given in Table. 5.4. Simulation is carried out for two different load conditions to verify the efficiency of the proposed control algorithm. During load-1, FL-DSTATCOM is connected to the distribution system at 0.1 s. Fig. 5.6 shows various waveforms of the system for load-1. They are, PCC

Table. 5.4 Simulation parameters

Parameter	Value
Supply voltage	415 V
Interfacing inductor (L_f)	4.5 mH
Dc link voltage (V_{dc})	700 V
Dc link capacitance (C_{dc})	5000 μF
Load-1	Unbalanced non-linear load: Three single-phase diode bridge rectifiers feeding R=10 Ω, L=150 mH on phase-*a*, R=12.5 Ω, L=150 mH on phase-*b*, R=7.5 Ω, L=150 mH on phase-*c*. Balanced linear load: 10 kVA with 0.7 power factor.
Load-2	Non-linear load: Three single-phase diode bridge rectifiers feeding a parallel combination of R=10 Ω, C=500 μF on each phase.
Sampling Time (T_s)	10 μs
Switching frequency	10000 Hz

voltages (v_{sabc}), load currents (i_{labc}), source currents (i_{sabc}), compensator currents (i_{cabc}), load and source neutral currents (i_{ln} and i_{sn}). From this figure, it is observed that, the load currents are non-linear as well as unbalanced. During 0 to 0.1 s, source currents and load currents are same. The entire load neutral current is flowing through the source neutral conductor.

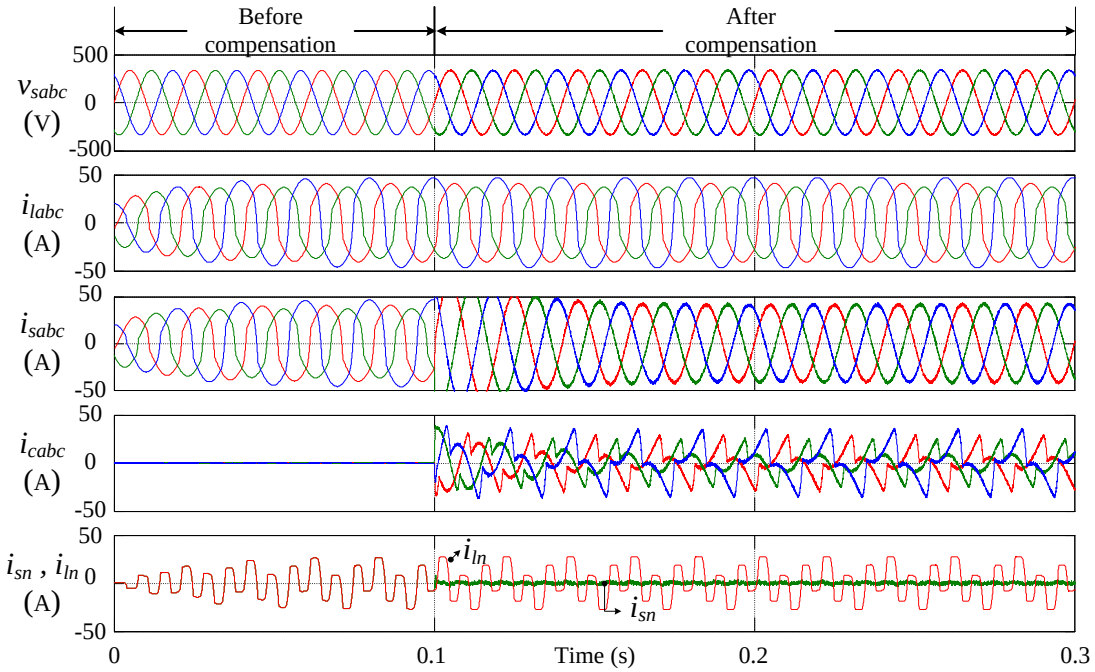


Fig. 5.6 Voltages and currents before and after connecting the FL-DSTATCOM to the distribution system.

After connecting FL-DSTATCOM, the source currents are balanced, distortion free and in-phase with the PCC voltages. The THD spectrum of DSTATCOM and source currents are given in Fig. 5.7. To compare the performance of the proposed control algorithm, the THD spectrum of DSTATCOM currents is provided for both conventional [84], [85] and proposed 3DSVM based MPC. From Fig. 5.7 (a), it is observed that, the harmonics are spread over a complete area which implies that the switching frequency is variable with conventional MPC. From Fig. 5.7 (b) and (c), it is observed that the harmonic components are spread over 10 kHz and integral multiples of 10 kHz, which implies that the switching frequency is constant and its value is 10 kHz. The rms values and THDs of source currents in Fig. 5.7 (c) indicate that, they are balanced and sinusoidal.

To evaluate the performance of proposed control algorithm for higher THD loads, three single-phase diode bridge rectifiers feeding a parallel combination of resistor and ca-

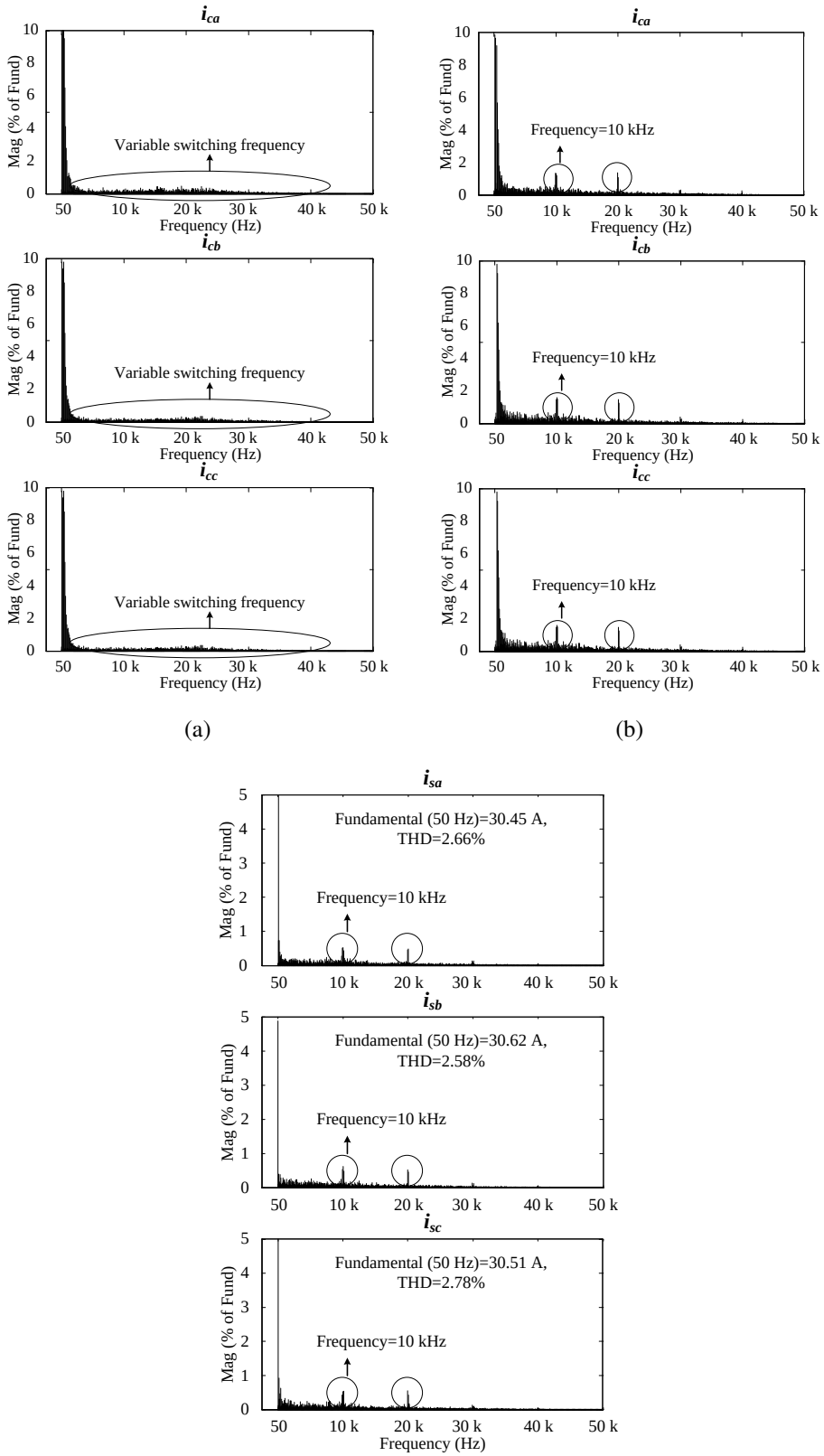


Fig. 5.7 Harmonic spectrum of FL-DSTATCOM and source currents for load-1 (a) DSTATCOM currents with conventional method (b) DSTATCOM currents with proposed method, and (c) Source currents with proposed method.

pacitor are connected to the supply as load-2. Fig. 5.8 shows the simulation results during load-2. Before connecting FL-DSTATCOM to the distribution system, the rms values of source currents are 34.27 A with THD 42.25%. These values indicates that, the load currents are balanced, distorted. From this figure, it is also observed that, the neutral current is high, even though the load is balanced. The reason for the neutral current is the presence of triplen harmonic currents generated by the loads. After connecting the FL-DSTATCOM to the system, the rms values of the source currents are 32.22 A, 32.24 A and 32.22 A with THDs of 3.11%, 3.13% and 3.16%, for phase-*a*, phase-*b* and phase-*c*, respectively, which indicate that they are balanced, sinusoidal and the source neutral current is almost zero, as observed from Fig. 5.8. The THDs of load currents and source currents for both load-1 and load-2 are given in Table. 5.5.

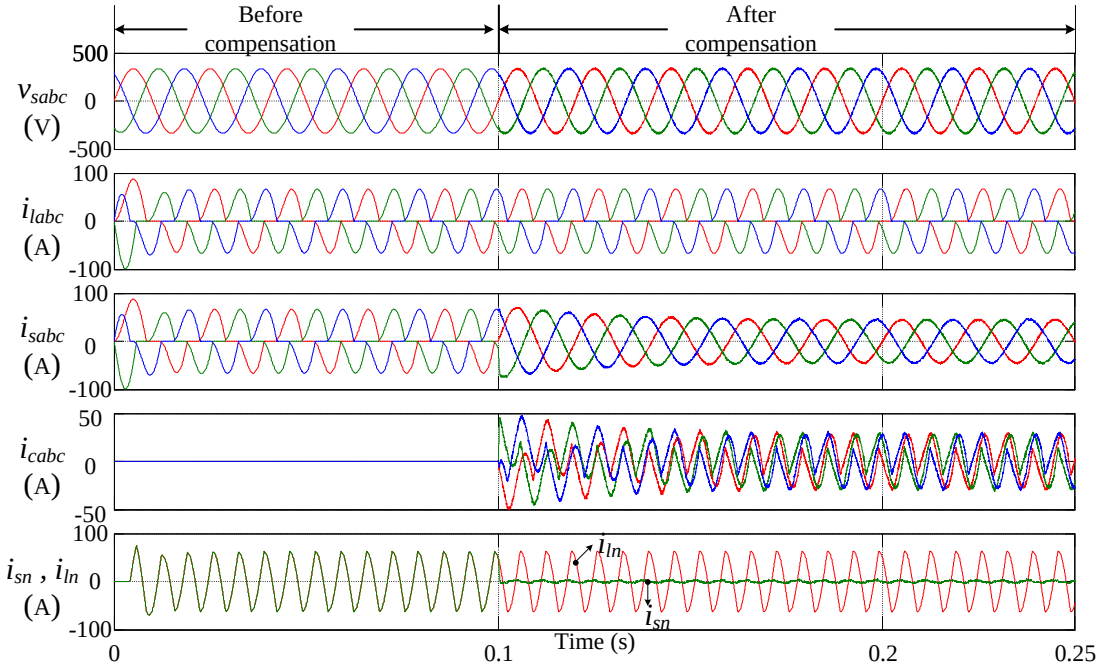


Fig. 5.8 Voltages and currents of the system during higher THD loads.

Table. 5.5 THDs of load and source currents for load-1 and load-2

Load	i_{la} (A)	i_{lb} (A)	i_{lc} (A)	i_{sa} (A)	i_{sb} (A)	i_{sc} (A)
Load-1	32.52 19.86%	29.04 18.08%	38.19 21.86%	30.45 2.68%	30.62 2.48%	30.51 2.84%
Load-2	34.27 42.26%	34.27 42.26%	34.27 42.26%	32.22 3.11%	32.24 3.13%	32.22 3.16%

5.3.1 Comparison of proposed method with conventional MPC and MPC with reduced switching frequency

As discussed earlier in this chapter, conventional MPC is leading to variable switching frequency and sometimes the switching frequencies are also very high, which further leads to higher switching losses. To reduce these losses, one method is adding switching frequency reduction constraint in the cost function, which further reduces switching losses. Using conventional MPC, to reduce the switching frequency of neutral leg an additional control parameter is required to be included in the cost function, and it is given by,

$$S = |S_a(k) - S_a(k-1)| + |S_b(k) - S_b(k-1)| + |S_c(k) - S_c(k-1)| + |S_n(k) - S_n(k-1)|. \tag{5.10}$$

Therefore, the complete cost function to compensate power quality issues along with the switching frequency reduction can be written as

$$C_f = C + \lambda S. \tag{5.11}$$

where, C is given in (5.5), λ is weighting factor and the reduction in the value of switching frequency completely depends on it. Table. 5.6 shows the comparison between, conventional MPC (CMPC), reduced switching frequency MPC (MPCSFR) and the proposed MPC in terms of THDs of source currents and switching losses. From the table, it is observed that the switching losses are reduced after adding switching frequency reduction constraint in the cost function with $\lambda = 0.2$, and they are further reduced by making $\lambda = 0.5$. However, with the proposed control technique, the losses are further reduced and also achieves constant switching frequency operation (10 kHz).

5.4 Experimental studies

The parameters considered for experimental studies are given in Table. 5.7. As per the rating constraints, the experimental parameters are considered for reduced rating compared to simulation studies.

Table. 5.6 Comparison of proposed method with conventional methods

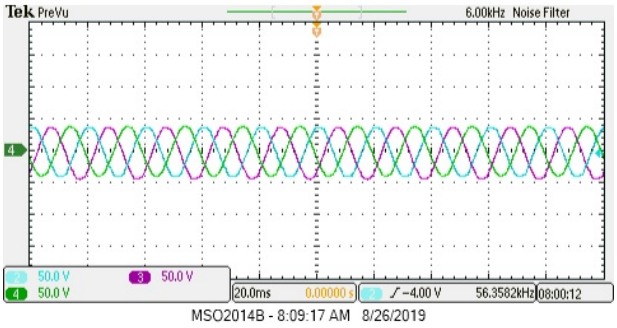
Parameter	CMPC	MPCSFR (λ=0.2)	MPCSFR (λ=0.5)	Proposed
i_{la} (A)	32.19 19.00%	32.19 19.00%	32.19 19.00%	32.19 19.00%
i_{lb} (A)	28.8 17.33%	28.8 17.33%	28.8 17.33%	28.8 17.33%
i_{lc} (A)	37.67 20.88%	37.67 20.88%	37.67 20.88%	37.67 20.88%
i_{sa} (A)	30.29 1.95%	30.3 2.01%	30.3 2.08%	30.32 2.66%
i_{sb} (A)	30.46 1.67%	30.45 1.76%	30.45 1.86%	30.45 2.58%
i_{sc} (A)	30.31 1.94%	30.31 2.00%	30.31 2.02%	30.34 2.78%
SL_a (W)	382.8	320	275.3	264.2
SL_b (W)	355	286.5	259.3	250.4
SL_c (W)	506.2	414.3	381.4	374.3
SL_n (W)	679.8	452.4	363.9	282.2

*where SL is the switching loss.

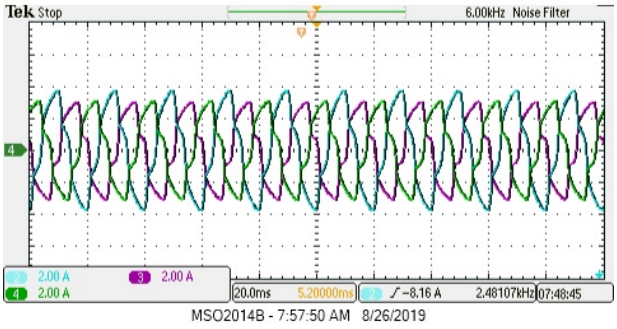
Table. 5.7 Experimental parameters

Parameter	Value
Supply voltage	50 V
Interfacing inductor (L_f)	9 mH
Dc link voltage (V_{dc})	100 V
Dc link capacitance (C_{dc})	4700 μF
Non-linear load	Three-phase diode bridge rectifier feeding R=20 Ω, L=150 mH Unbalanced linear load: R=12.5 Ω, L=60 mH on phase-*a* R=12.5 Ω, L=120 mH on phase-*b* R=12.5 Ω, L=80 mH on phase-*c*
Sampling Time (T_s)	50 μs
Switching frequency	2000 Hz

A combination of three unbalanced single-phase *RL* loads and a three-phase diode bridge rectifier is connected to the three-phase supply to realize non-linear and unbalance load currents. dSPACE MicroLabBox 1202 is used as an interfacing device between the real time environment and personal computer (PC). Fluke made power quality analyzer is used to measure the THDs of various currents and voltages of the system. Fig. 5.9 shows the PCC voltages, non-linear and unbalanced load currents, balanced and sinusoidal source currents and DSTATCOM currents with their scaling. From this figure, it is noticed that DSTATCOM is maintaining source currents balanced and



(a)



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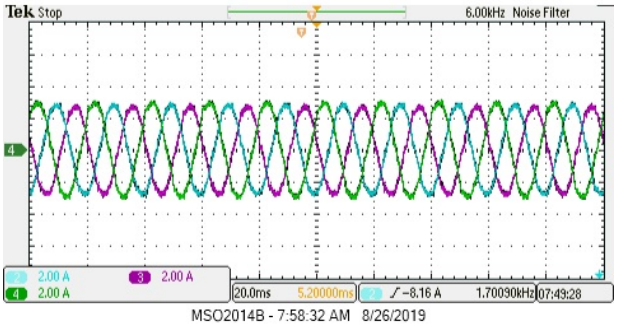
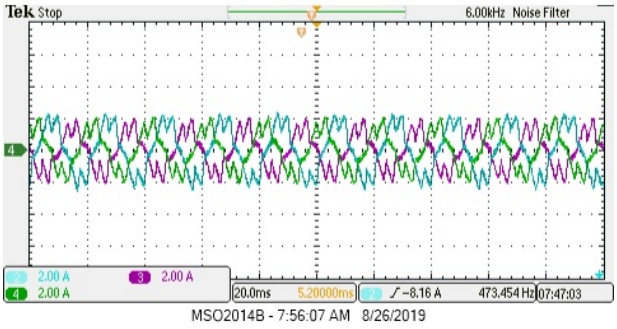


(c)



(d)

Fig. 5.9 Various parameters of the distribution system (a) PCC voltages (v_{sabc}) (b) Load currents (i_{labc}) (c) Source currents (i_{sabc}), and (d) DSTATCOM currents (i_{cabc}).

sinusoidal even though there is unbalance and distortions in the load currents. From Fig. 5.10, it is observed that the phase difference between the voltage and current at PCC is almost zero which implies that DSTATCOM is achieving unity power factor.

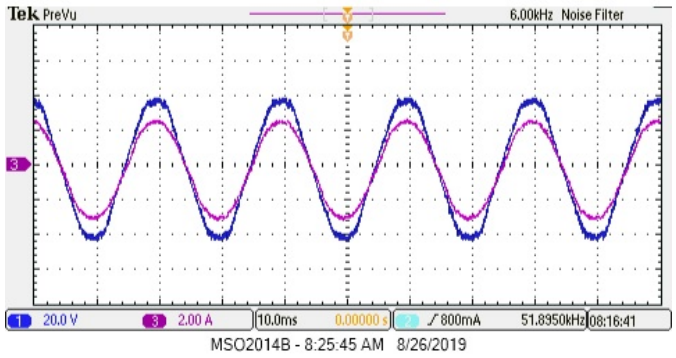


Fig. 5.10 v_{sa} and i_{sa} after compensation with FL-DSTATCOM.

The main objective of the proposed work is achieving fixed switching frequency MPC for FL-DSTATCOM. Fig. 5.11, shows that the THD spectrum of DSTATCOM currents of three phases using the proposed control algorithm. From the figure, it is observed that, the harmonic components are centered around 2 kHz and integral multiples of 2 kHz, which implies that the switching frequency is 2 kHz.

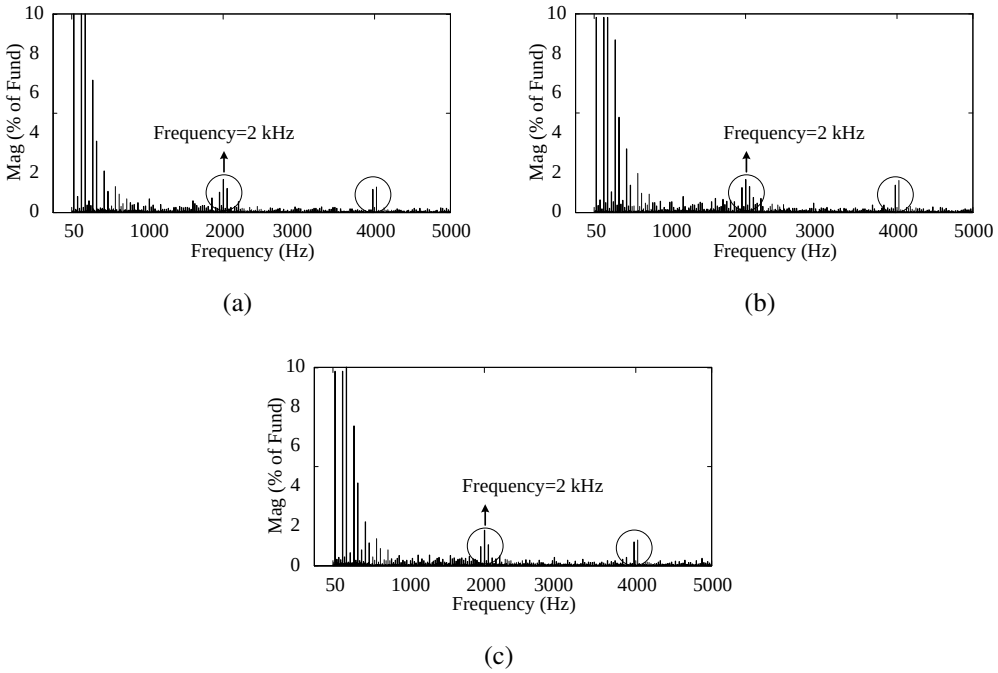


Fig. 5.11 Harmonic spectrum of FL-DSTATCOM currents (a) i_{ca} (b) i_{cb}, and (c) i_{cc}.

Fig. 5.12 shows the harmonic spectrum of source currents. From this figure, it also observed that, the THDs of source currents are 3.54%, 3.34% and 3.20% which are well within the limits of IEEE-519 standard (less than 5%). Similarly, the harmonics are centered around switching frequency (2 kHz).

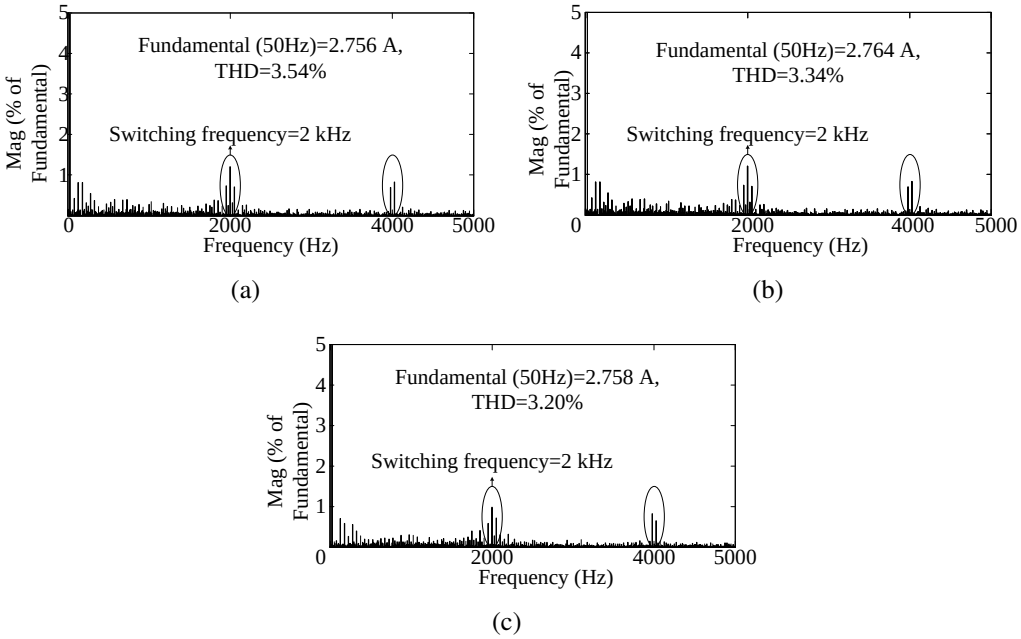


Fig. 5.12 Harmonic spectrum of source currents (a) i_{sa} (b) i_{sb}, and (c) i_{sc}.

5.5 Summary

In this chapter, constant switching frequency MPC for FL-DSTATCOM is proposed to compensate current related power quality issues. MPC has the limitation of variable switching frequency and it is overwhelmed with 3DSVM based constant switching frequency MPC. From simulation studies, it is observed that conventional MPC is providing variable switching frequency and the proposed 3DSVM based MPC is achieving constant switching frequency. Experimental results are also proved that, the proposed control algorithm is compensating current related power quality issues as well as achieving constant switching frequency.

CHAPTER 6

Three-Phase Four-Switch DSTATCOM Topologies with Special Transformers for Neutral Current Compensation and Power Quality Improvement

In this chapter, four different DSTATCOM topologies are proposed by combining four-switch one-capacitor (FSOC) and four-switch split-capacitor (FSSC) VSI topologies with two special purpose transformers namely zigzag and T-connected. These special transformers provides a path for neutral current, reduces the cost and rating of the inverter, improves the performance under stringent unbalanced currents generated by computer loads and also improves short duration overloading capability. The combination of three-phase four-switch (TPFS) inverter and special transformer can achieve power factor improvement, harmonic elimination, neutral current compensation and load balancing.

6.1 Introduction

In distribution system, most of the loads are single-phase, non-linear with unequal ratings, which causes unbalance in load currents. These unbalanced load currents lead to unnecessary neutral currents and harmonic losses in the system. The non-linear currents drawn by computer loads will generate high amount of neutral current even though the phase currents are balanced [8]. Sometimes, the value of neutral current is more than the load current and it causes severe damage to the distribution system. A survey was conducted to evaluate the effects of excessive neutral current which is presented in [8], [96]. To compensate the neutral current, several techniques are proposed in the literature and they are synchronous machines, passive filters, special transformers and 3P4W DSTATCOM [65]. The high maintenance and initial cost of the synchronous machine is limiting its use in many applications. Even though passive filters are simple to use, they

are expensive and occupy more space. In [97], [98] special transformer based DSTATCOM topologies are presented to reduce the overall rating of DSTATCOM. However, these topologies are complex and require more number of switching devices.

There are many DSTATCOM topologies available in the literature [22], [99], [100]. Among them, four leg DSTATCOM (FL-DSTATCOM) and three-phase split-capacitor (TPSC) topologies are suitable for 3P4W applications due to their simple structure and easy control [25], [27], [28], [101], [102]. These DSTATCOM topologies are used to control reactive power, harmonic currents and load balancing. In FL-DSTATCOM topology, the neutral wire is connected to an extra leg and the switches in this leg are controlled to compensate the neutral current. The presence of an extra leg will increase the number of power electronic devices, which increases the size, cost and control circuitry [97]. In TPSC DSTATCOM topology neutral conductor is connected to the mid-point of two capacitors. A large amount of load unbalance increases the difference between voltages across two capacitors which further affects the overall performance of the TPSC DSTATCOM [70].

In literature, to reduce the cost and size, TPFL and TPSC inverters are replaced with three-phase four-switch (TPFS) inverters [29], [30]. The available TPFS topologies are four-switch split-capacitor (FSSC) topology [31] and four-switch one-capacitor (FSOC) topology [32]. In these two topologies four switches are formed as two legs of DSTATCOM and they are connected to two phases at PCC. The third phase is connected to mid-point of the dc link in FSSC topology and in case of FSOC topology it is connected to the negative terminal of the dc link. In FSOC topology, the direct connection between supply and negative terminal of the capacitor shifts the voltage at PCC. Therefore, the third phase is connected through a passive filter tuned to dominant harmonics (usually 5^{th} and 7^{th}) in load current. This helps to enable coupling between the supply and negative terminal of the dc bus. The design for 5^{th} and 7^{th} order harmonic passive filters is given in [103]–[105]. In these two topologies, the third phase is automatically controlled by controlling the two phases [31], [32]. On the other hand, the absence of neutral wire in TPFS topologies does not allow DSTATCOM to compensate the neutral current created by harmonic and unbalanced loads.

Therefore, in this chapter, four different DSTATCOM topologies are proposed by combining FSSC or FSOC inverter configuration with zigzag or T-connected transformer.

FSSC or FSOC inverter configuration is responsible for the compensation of phase-current harmonics, reactive power and it also reduces the number of power devices and cost. Zigzag or T-connected transformer is connected in such a way that, it circulates the neutral current between load and transformer so that neutral currents flowing through the source will be nullified [59], [106]–[108]. The other advantages of these topologies are reduction in complexity, loading on four-switch inverter, reduction in overall cost of the inverter, improved performance under stringent unbalanced currents generated by computer loads and capacity to meet short duration overload conditions.

6.2 Configuration of TPFS topologies with special transformers

The schematic diagram of TPFS DSTATCOM connected to a three-phase distribution system is shown in Fig. 6.1. Design of various parameters of DSTATCOM are discussed in previous chapters [22], [25], [99]. The minimum dc bus voltage of DSTATCOM is 1.6 to 2 times peak value of phase voltage [25]. Here, for optimal performance, dc link voltage is considered to be twice that of the peak phase voltage [22].

$$V_{dc} = \frac{2\sqrt{2}V_{L-L}}{\sqrt{3}m} \tag{6.1}$$

where, V_{L-L} is the line voltage and m is the modulation index, usually the value of m is considered as unity. For simulation studies, supply voltage is considered as 415 V. Using (6.1) V_{dc} is obtained as 677.6 V and is selected as 700 V. In a similar way, for split-capacitor topology $V_{dc1} = V_{dc2} = 700$ V. In the experiment, supply voltage is considered as 50 V. Using (6.1) V_{dc} is equal to 81.54 V and is chosen as 100 V for FSOC and $V_{dc1} = V_{dc2} = 100$ V for FSSC. The output of DSTATCOM is connected at PCC through an interfacing inductor, which eliminates ripples in the compensating current. Here, a non-linear and unbalanced load is connected to the distribution system through the feeder impedance. A zigzag or T-connected transformer is connected across the load terminals to compensate neutral current caused by the unbalanced loads.

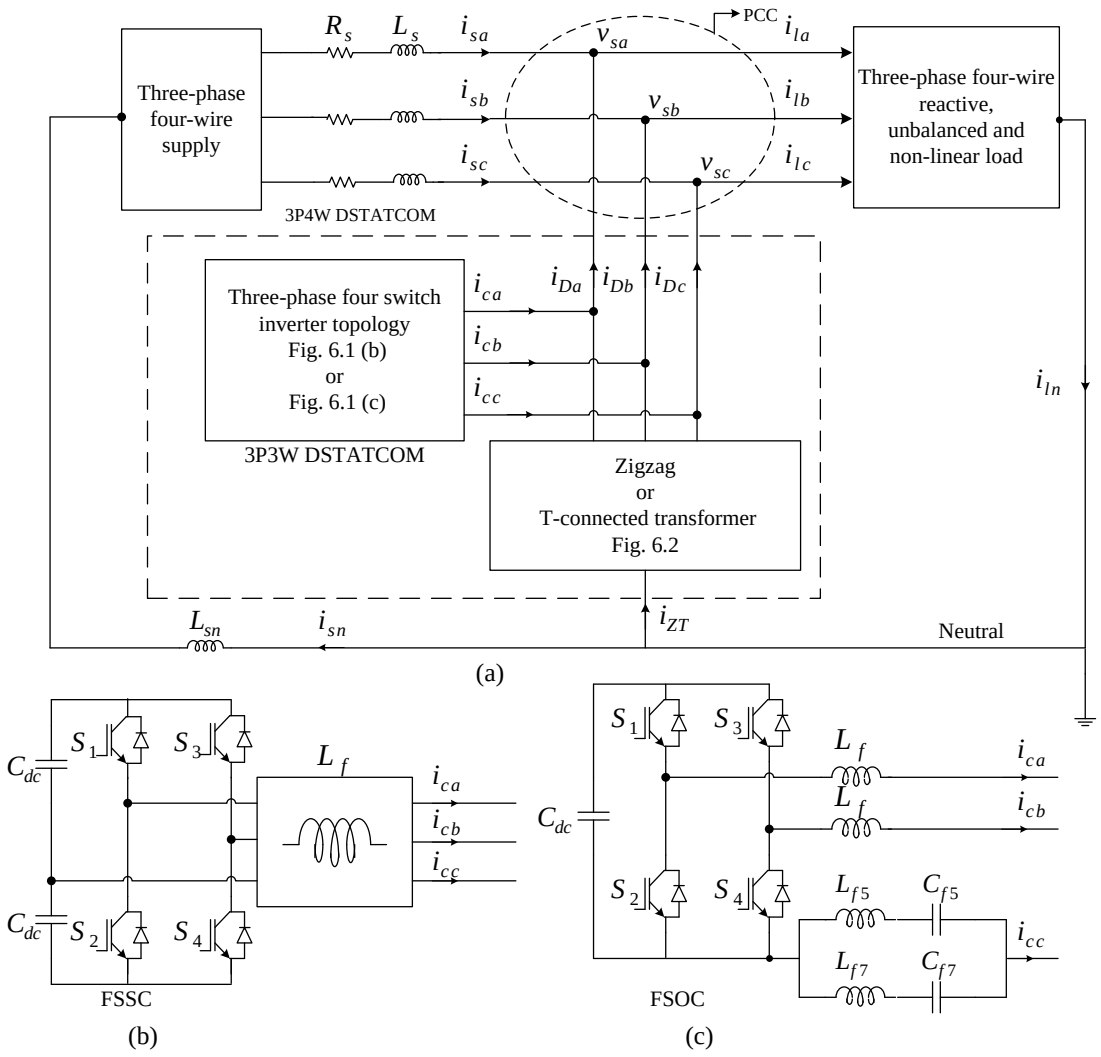


Fig. 6.1 (a) Schematic diagram of TPFS DSATCOM connected distribution system (b) FSSC topology, and (c) FSOC topology.

6.2.1 FSSC topology

FSSC inverter topology shown in Fig. 6.1 (b) is formed by eliminating one leg from the existing split-capacitor topology. The mid-point of two capacitors is connected to the third phase at PCC. By controlling the two legs of the inverter, third phase is automatically controlled for required compensation. But, the dc-link voltage is almost twice that of the conventional three-leg VSI. Cost and complexity of the inverter are reduced compared to TPSC topology because of fewer switches.

6.2.2 FSOC topology

In FSOC topology, shown in Fig. 6.1 (c), the third phase is connected to the negative terminal of the dc bus. Because of direct connection, there is an offset added to the third phase voltage. To compensate this, a passive filter is connected between PCC and inverter terminals. This passive filter is used to maintain the rated terminal voltage and to provide harmonic and reactive power to the distribution system. The values of inductor and capacitor of the passive filter depends on the load harmonic content. Therefore, these are designed to eliminate the dominant 5^{th} and 7^{th} order harmonics in addition to reactive power support. In general, large value of the capacitor will increase the filter size and small value of the inductor will not completely compensate the ripples in the DSTATCOM current [29].

6.2.3 Zigzag transformer

Zigzag transformer is a special transformer used to provide a neutral connection to allow the flow of neutral and zero-sequence currents developed by non-linear and unbalanced loads in three-phase distribution system. Three single-phase transformers with turns ratio 1:1 are connected in a zigzag manner to engender a three-phase zigzag transformer. The connection diagram and the phasor diagram of a three-phase zigzag transformer is shown in Fig. 6.2 (a). The voltages of primary and secondary winding's of three identical single-phase transformers are considered as 1/3 times of the rated PCC line to line voltage to achieve equal rated voltage at the terminal of the zigzag transformer and PCC. The amount of current flowing through the winding's of the three transformers is always same because of equal voltage and power ratings and the value of neutral current is one third of total neutral current. From the above voltages and currents, the rating of zigzag transformer is given as,

$$kVA_{Zigzag} = 3\frac{V_l}{3}\frac{I_n}{3} = \frac{V_l \times I_n}{3}. \tag{6.2}$$

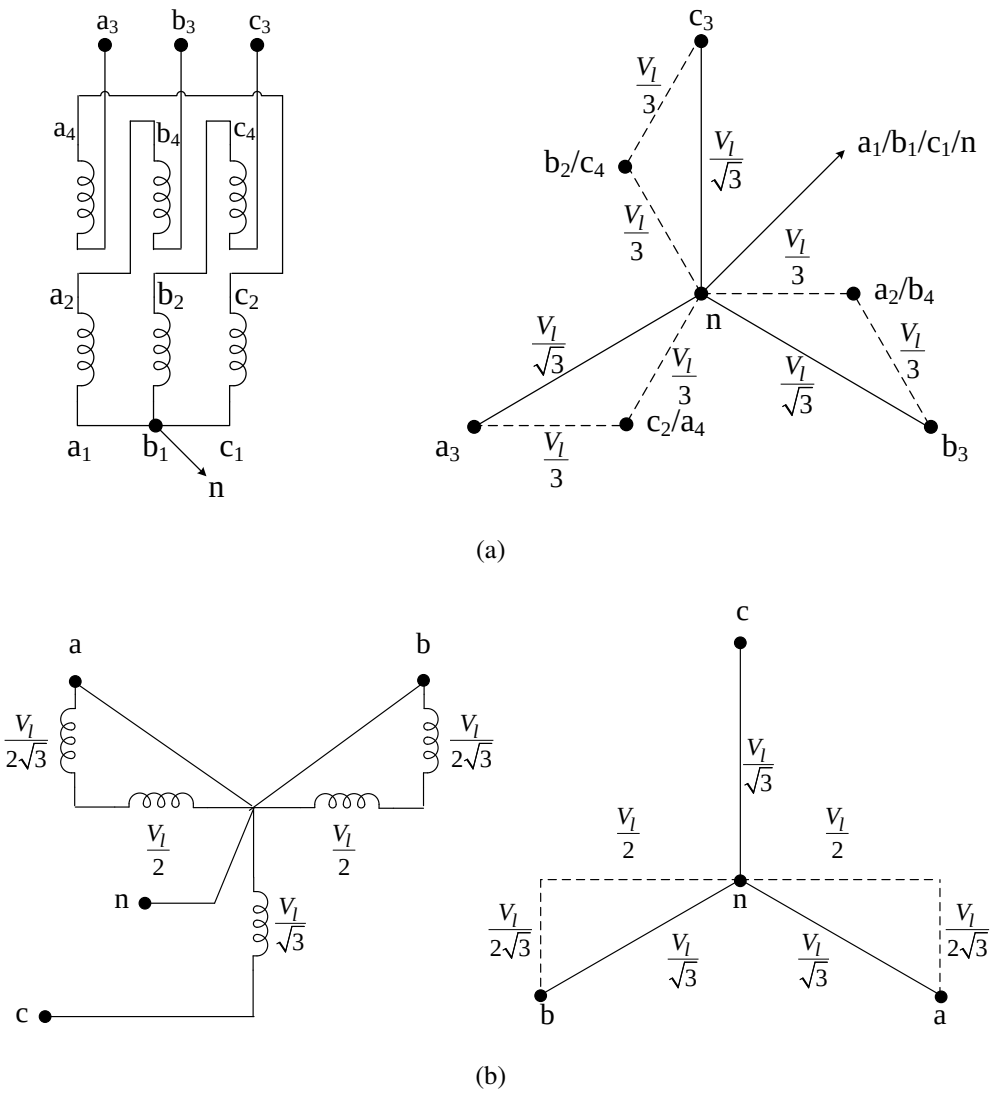


Fig. 6.2 Connection diagram and phasor diagram of (a) Zigzag transformer, and (b) T-connected transformer.

6.2.4 T-connected transformer

T-connected transformer is a special transformer formed by using a single-phase two winding transformer and a single-phase three winding transformer. Zigzag transformer can be replaced with a T-connected transformer having equal kVA rating, to further reduce the cost and foot print. The connection diagram and the phasor diagram are shown in Fig. 6.2 (b). The ratio between the voltages of primary and secondary winding of the three winding and two winding transformers are $\frac{V_l}{\sqrt{3}} : \frac{V_l}{2\sqrt{3}} : \frac{V_l}{2\sqrt{3}}$ and $\frac{V_l}{2} : \frac{V_l}{2}$, respectively [98], where V_l is the line to line voltage. The given voltage ratings of single-phase transformers make the rated voltage of the T-connected transformer and PCC are equal, which is shown by phasor diagram in Fig. 6.2(b). The kVA rating of

T-connected transformer is given by:

$$kVA_{T-Connected} = \left(\frac{V_l}{\sqrt{3}} \times \frac{I_n}{3} + \frac{V_l}{2} \times \frac{I_n}{3}\right) = \left(\frac{1}{3\sqrt{3}} + \frac{1}{6}\right) V_l I_n. \tag{6.3}$$

6.3 Instantaneous symmetrical component theory (ISCT)

Instantaneous symmetrical component theory (ISCT) with hysteresis controller is used here to generate gate pulses for both FSOC, FSSC topologies [108]. In this, by controlling two legs of FSOC or FSSC topologies, the third phase will be automatically controlled [29]. The block diagram for the control algorithm is shown in Fig. 6.3. Initially, PCC voltages and load currents are sensed to calculate instantaneous load power demand. The equation to calculate load power is given by:

$$p_l = v_{sa} i_{la} + v_{sb} i_{lb} + v_{sc} i_{lc}. \tag{6.4}$$

Instantaneous load power in (6.4) is the sum of a dc component power (p_{ldc}) and oscillating ac component power (p_{lac}). The sum of p_{ldc} and power required to maintain constant voltage across the dc link (p_{loss}) should be the total active power supplied by the source for harmonic free source current with unity power factor operation. Usually, instantaneous load power is passed through a low pass filter to extract an average load power demand (p_{ldc}). The difference between the measured and the actual dc link voltage is given to a PI controller to estimate the power required by DSTATCOM to maintain constant dc link voltage.

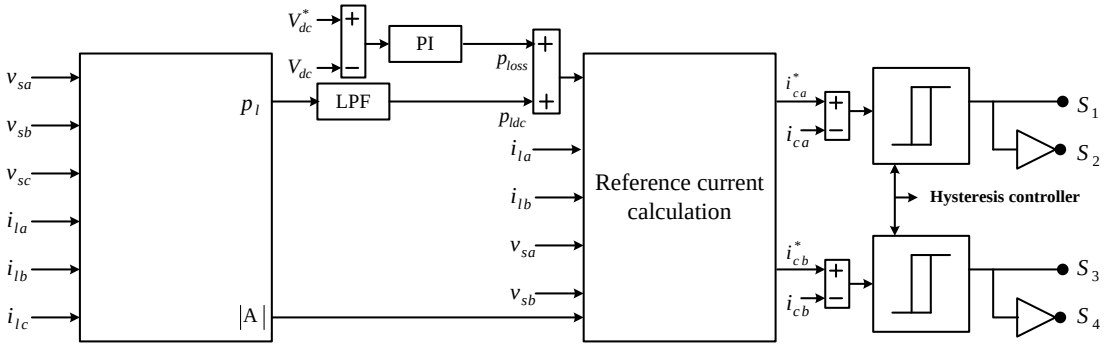


Fig. 6.3 Generation of gate pulses using instantaneous symmetrical component theory (ISCT).

$$p_{loss} = K_p(V_{dc}^* - V_{dc}) + K_i \times \int (V_{dc}^* - V_{dc}) \tag{6.5}$$

After estimating the active power supplied by the source the reference filter currents will be given as,

$$\begin{aligned} i_{ca}^* &= i_{la} - \frac{v_{sa} + \beta(v_{sb} - v_{sc})}{|A|} \times (p_{ldc} + p_{loss}) \\ i_{cb}^* &= i_{lb} - \frac{v_{sb} + \beta(v_{sc} - v_{sa})}{|A|} \times (p_{ldc} + p_{loss}) \end{aligned} \tag{6.6}$$

where, $|A| = v_{sa}^2 + v_{sb}^2 + v_{sc}^2$. The angle β is given as, $\beta = \dfrac{\tan\theta}{\sqrt{3}}$, where θ is the angular difference between PCC voltage and supply fundamental current. The amplitude of PCC voltage is given by:

$$V_{sm} = \sqrt{\frac{2}{3}(v_{sa}^2 + v_{sb}^2 + v_{sc}^2)}. \tag{6.7}$$

The difference between reference and actual amplitude of PCC voltage is passed through a PI controller to estimate β. However, in this chapter, to maintain unity power factor operation at PCC, the value of β should be zero. Finally, difference between the reference and actual DSTATCOM currents is given to a hysteresis controller to generate the gate pulses for the VSI in DSTATCOM.

6.4 Neutral current compensation

The zero sequence equivalent circuit of special transformer connected distribution system is shown in Fig. 6.4. There are two sources for zero sequence current, one is zero sequence voltage source (V_{s0}) due to the unbalance in the supply voltage and the other is zero sequence current source (i_{L0}) due to the unbalance and harmonics in load current. In the proposed work, supply voltage is considered as balanced and sinusoidal. Therefore, V_{s0} is considered as zero. In Fig. 6.4, Z_{s0} represents feeder impedance, Z_{sn} represents the impedance between the supply and neutral, Z_{ln} is the impedance between load and neutral and Z_{zn} is the impedance offered by the special transformer. The neutral current flowing through the source is calculated using current division rule and it is

given below

$$i_{sn} = \frac{Z_{tn}}{Z_{sn} + Z_{s0} + Z_{tn}} i_{L0}. \tag{6.8}$$

From the above equation, to minimize the current flowing through the source, the impedance offered by the transformer (Z_{tn}) should be minimum.

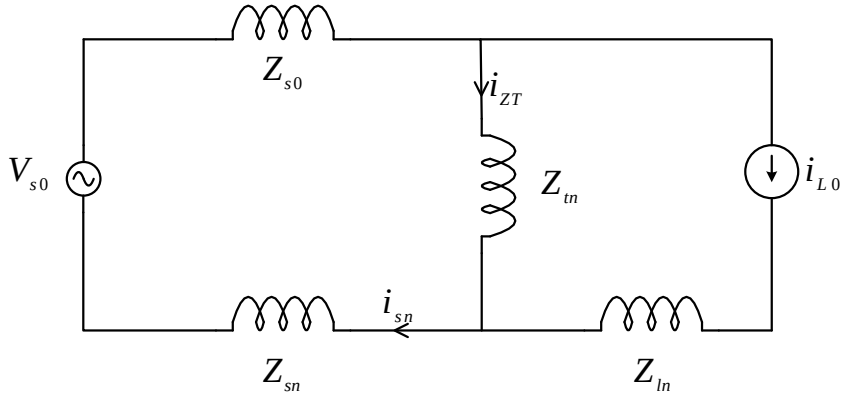


Fig. 6.4 Zero sequence equivalent circuit of special transformer connected distribution system.

6.5 Simulation studies

The parameters used in simulation studies are given in Table. 6.1. DSTATCOM is connected to distribution system at 0.1 s, during this period, initial capacitor voltage is considered as 90% rated voltage. During 0 to 0.35 s the three-phase diode bridge rectifier is connected to the PCC as a balanced load. A single-phase diode bridge rectifier is connected to phase-*a* only, which makes the load unbalanced and it is considered as load-1. At 0.35 s, a single-phase diode bridge rectifier is added to the existing load on phase-*b* and it is considered as load-2. These non-linear and unbalanced loads are collectively compensated by the inverter topology and transformer. Here, inverter will inject the required harmonic and reactive currents so that the source currents will be sinusoidal and in-phase with the voltages at PCC. To compensate neutral current, special transformer connected at PCC provide a low impedance path so that source neutral current is almost zero, which indicates the source phase currents are balanced. In simulation studies, inverter and special transformer is turned on at 0.1 s for all the four configurations.

Table. 6.1 Simulation parameters

Parameters	Values
Supply voltage	415 V
Feeder impedance (Z_s)	(0.7+j0.942) Ω
AC Load Inductor (L_{ac})	3 mH
Ripple Filter (R_f, C_f)	10 Ω, 10 μF
Neutral impedance (L_{sn})	1 mH
Filter Inductor (L_5, L_7)	8 mH, 4 mH
Filter Capacitor (C_5, C_7)	50 μF, 50 μF
FSSC Topology (V_{dc}, C_{dc})	1400 V, 4700 μF
FSOC Topology (V_{dc}, C_{dc})	700 V, 4700 μF
Zigzag Transformer	Three single-phase transformers of voltage rating 150/150 V with 3 kVA power rating.
T-Connected transformer	One single phase three winding transformer of voltage rating 240/120/120 V, and one single-phase two winding transformer of voltage rating 208/208 V with power rating of 5 kVA each.
Load	Three phase diode bridge rectifier with 20 Ω, 150 μF. Two Single-phase full bridge rectifiers one is connected to phase-a with 4 Ω, 100 μF, and the other is connected to phase-b at 0.6 s with 8 Ω, 200 μF.

6.5.1 Performance of FSOC with zigzag transformer

Fig. 6.5 shows the performance of FSOC inverter topology with zigzag transformer as DSTATCOM. In this figure, load currents, PCC voltages, source currents, DSTATCOM currents, load and source neutral currents and dc link voltage during load variation are shown. The rms values of source currents during load-1 without compensation are 72.19 A, 17.84 A and 19.73 A and the THDs are 8.43%, 47.05%, 53.47% for three phases respectively. After connecting DSTATCOM, rms values of the source currents are changed to 35.92 A, 36.14 A and 36.22 A, respectively which indicates that the source currents are balanced. Similarly THDs of source currents are observed to be 1.36%, 1.51%, 1.51% which are well within the limits of IEEE-519 standard. Similarly, rms values and THDs for load-2 are given in Table. 6.2 and Table. 6.3 respectively. The unbalanced load currents lead to a load neutral current of 52.91 A during load-1 and 51.83 A during load-2 but the source neutral current is almost zero because the entire load neutral current is circulating between load and transformer.

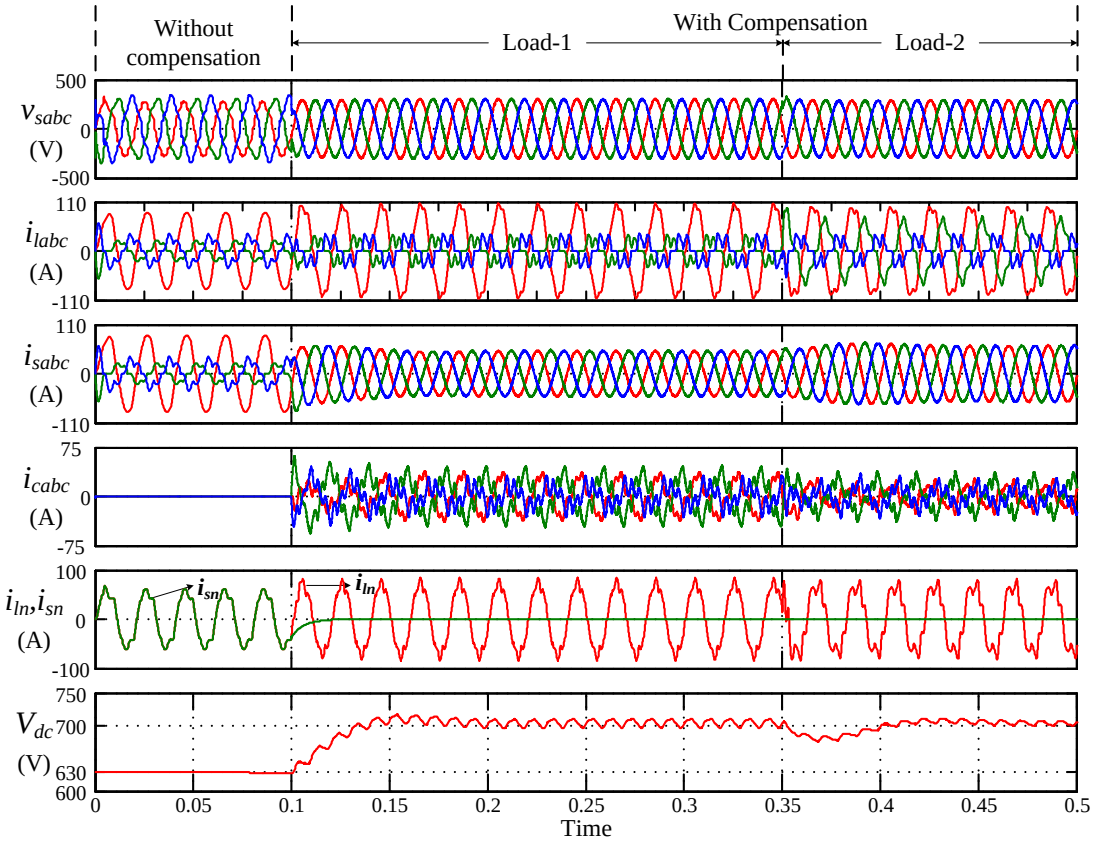


Fig. 6.5 FSOC topology with zigzag transformer.

6.5.2 Performance of FSOC with T-connected transformer

The performance of FSOC with T-connected transformer is similar to FSOC with zigzag transformer. But the only difference is the number of single-phase transformers required to implement a zigzag transformer is three, whereas only two transformers are enough to implement a T-connected transformer. Fig 6.6 shows the performance of FSOC with T connected transformer. During load-1, rms values of the source currents after compensation are 35.86 A, 36.07 A, 35.84 A which indicate that source currents are balanced and the THDs are observed as 1.40%, 1.55% and 1.63% which indicates they are well within IEEE-519 standard. During load-2, rms values of the source currents before compensation are 70.82 A, 44.90 A, 18.64 A with THDs 9.47%, 18.62%, 49.36%. After compensation rms values of source currents is modified to 44.36 A, 44.43 A, 44.39 A with THDs 1.14%, 1.20%, 1.17%. Load neutral currents during load-1 and load-2 are 52.91 A and 51.85 A but the source neutral current is almost zero which is shown in Fig. 6.6.

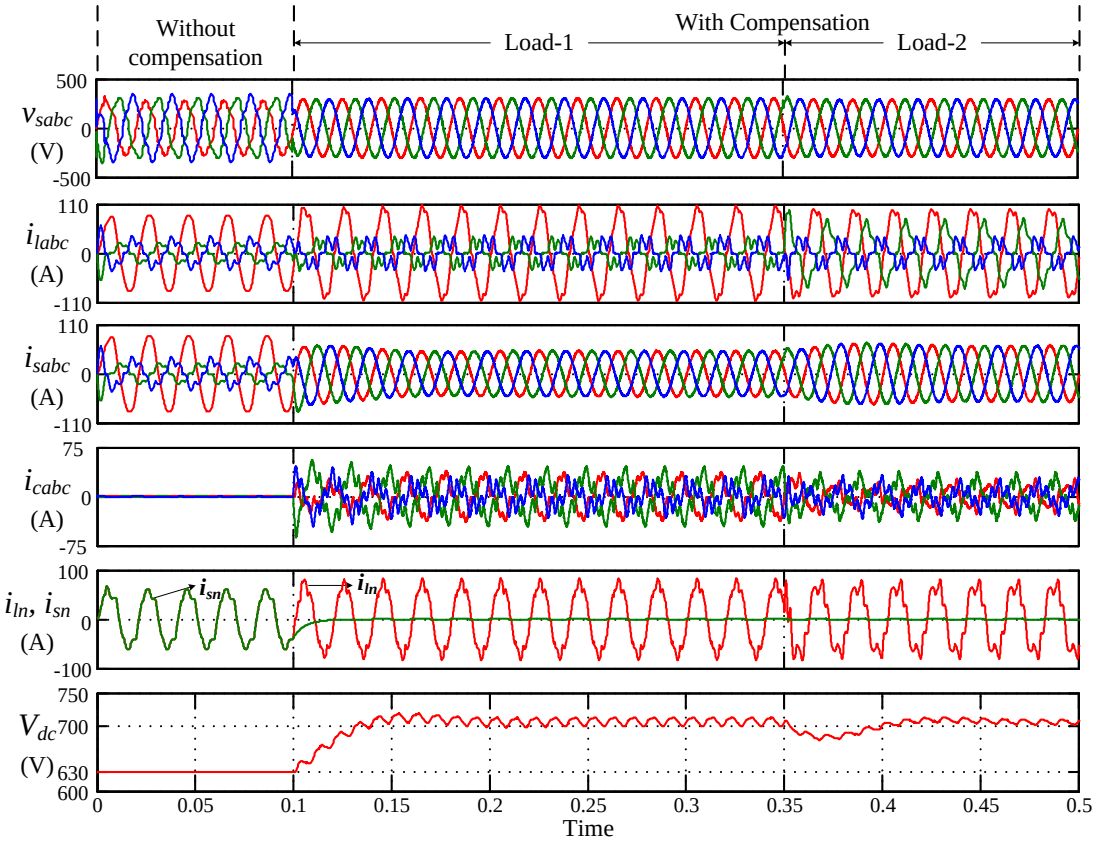


Fig. 6.6 FSOC topology with T-connected transformer.

6.5.3 Performance of FSSC with zigzag transformer

In this configuration, TPSC inveter topology is replaced with FSSC topology by eliminating two switches and the neutral current is compensated by connecting a zigzag transformer across the load terminals. Performance of FSSC inverter along with zigzag transformer is shown in Fig. 6.7. In the figure, load currents, PCC voltages, source currents, DSTATCOM currents, neutral currents and dc link voltage for different load conditions are shown. The rms values of balanced source currents during load-1 are 35.42 A, 35.99 A, 35.66 A with THDs 2.84%, 2.86%, 2.38%. During load-2, the rms values of source currents are 43.99 A, 44.29 A and 44.08 A and THDs are reduced to 2.28%, 2.24% and 1.82%. During 0 to 0.1 s, DSTATCOM and transformer is not connected to the distribution system so that the source neutral current is same as the load neutral current, which is shown in Fig. 6.7. The load neutral currents are 52.84 A and 51.67 A for load-1 and load-2. However, in these two load conditions source neutral current is almost zero.

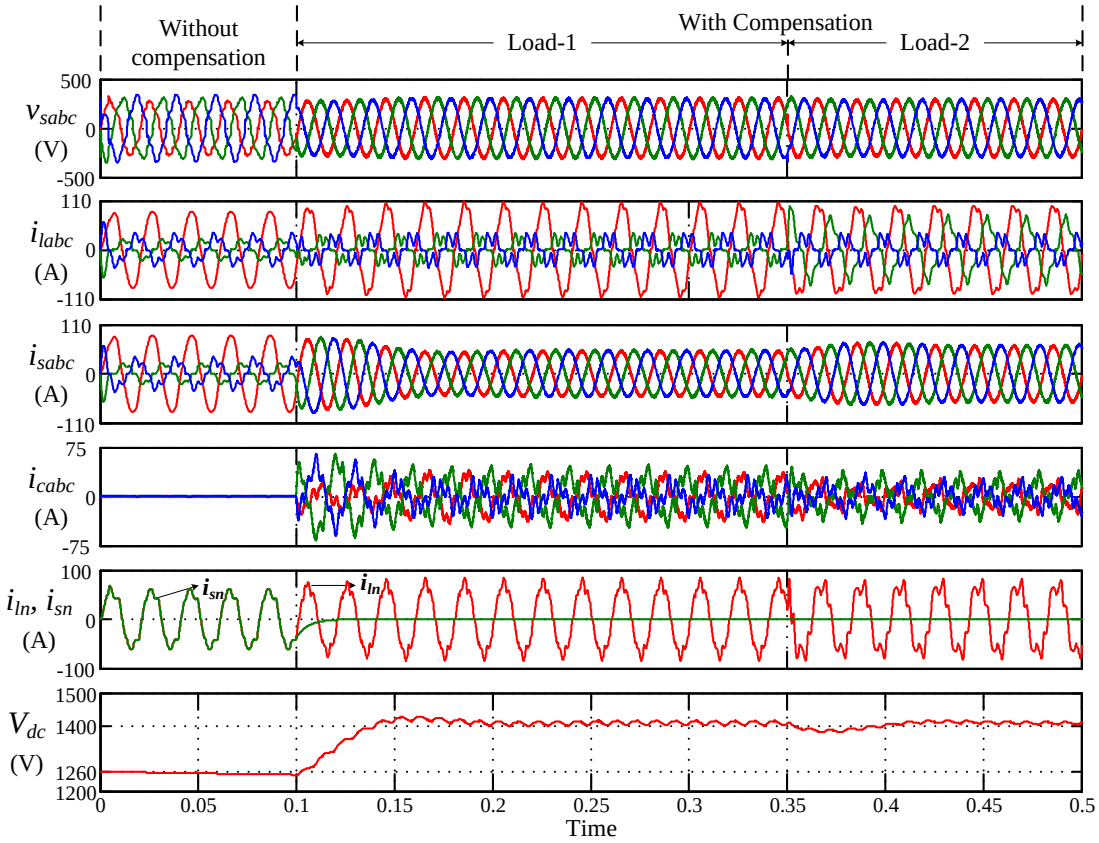


Fig. 6.7 FSSC topology with zigzag transformer.

6.5.4 Performance of FSSC with T-connected transformer

The performance of FSSC inverter topology with T-connected transformer is presented in Fig. 6.8. The rms values of load currents during load-1 are 71.90 A, 17.87 A and 19.76 A which shows they are unbalanced, but the rms values of source currents are 35.32 A, 35.85 A and 35.68 A which indicate that they are balanced. The THDs of source currents during load-1 are 2.84%, 2.90% and 2.89%. The rms values of balanced source currents during load-2 are 43.88 A, 44.26 A and 45.19 A and that of THD's 2.32%, 2.30% and 2.20% for phase-*a*, phase-*b* and phase-*c*, respectively.

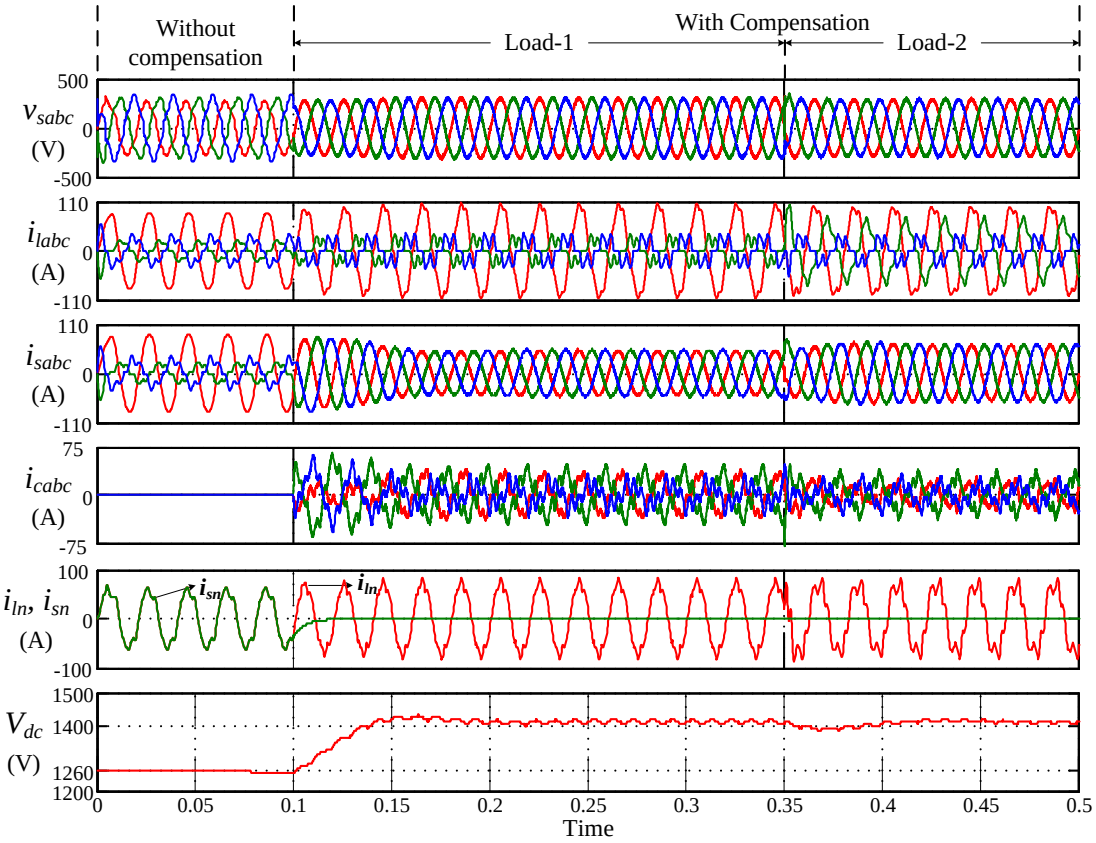


Fig. 6.8 FSSC topology with T-connected transformer.

6.5.5 Comparison of proposed topologies

In general, kVA rating of the TPFL or TPSC inverter is calculated using (6.9),

$$S = V_s(|i_{ca}| + |i_{cb}| + |i_{cc}| + |i_{cn}|). \tag{6.9}$$

Rating of the four switch inverter with zigzag transformer is calculated as,

$$S = V_s(|i_{ca}| + |i_{cb}| + |i_{cc}|) + \left(\frac{V_l \times I_n}{3}\right). \tag{6.10}$$

Similarly, rating of the four switch inverter with T-connected transformer is calculated as,

$$S = V_s(|i_{ca}| + |i_{cb}| + |i_{cc}|) + \left(\frac{1}{3\sqrt{3}} + \frac{1}{6}\right)V_l I_n. \tag{6.11}$$

Table. 6.2 Comparison of proposed topologies with conventional topologies

Duration	Topology	Source currents before compensation (in Amps)				Source currents after compensation (in Amps)			Filter currents (in Amps)				Loading of Inverter (in kVA)
		i_{sa}	i_{sb}	i_{sc}	i_{sn}	i_{sa}	i_{sb}	i_{sc}	i_{ca}	i_{cb}	i_{cc}	i_{cn} / i_{ZT}	
0.10 to 0.35 s	TPFL	72.24	17.84	19.72	52.93	35.88	36.15	35.96	37.45	19.48	17.18	52.93	30.436
	TPSC	72.28	17.82	19.70	53.08	35.92	36.14	36.22	37.59	19.49	17.43	52.93	30.534
	FSOC (Z)	72.19	17.84	19.73	52.91	35.90	36.12	35.96	20.70	24.17	11.69	52.75	20.844
	FSOC (T)	72.15	17.81	19.72	52.91	35.86	36.07	35.84	20.72	24.18	11.62	52.7	21.396
	FSSC (Z)	71.97	17.91	19.71	52.84	35.42	35.99	35.66	20.67	24.61	12.10	52.75	21.040
	FSSC (T)	71.90	17.87	19.76	52.82	35.32	35.85	35.68	20.63	24.61	12.17	52.61	21.595
0.35 s to 1 s	TPFL	70.85	44.89	18.62	51.86	44.3	44.42	44.45	27.85	0.5037	26.17	51.76	25.489
	TPSC	71.06	44.94	18.44	53.08	44.65	44.40	44.70	27.73	0.5453	26.50	52.05	25.590
	FSOC (Z)	70.81	44.91	18.62	51.83	44.37	44.35	44.43	12.18	17.42	10.61	51.67	16.777
	FSOC (T)	70.82	44.90	18.64	51.85	44.36	44.43	44.39	12.19	17.43	10.58	51.65	17.329
	FSSC (Z)	70.66	44.99	18.6	51.67	43.99	44.29	44.08	12.49	18.02	11.24	51.58	17.134
	FSSC (T)	70.61	45.07	18.6	51.68	43.88	44.26	45.19	12.56	18.03	11.48	51.48	17.752

* In this table (Z) implies zigzag transformer and (T) implies T-connected transformer.

The rms values of filter currents for all the topologies are given in Table. 6.2. Using the filter currents, the kVA loading of TPFL and TPSC topologies are calculated and they are obtained as 30 kVA for load-1 and 25 kVA for load-2. But, the kVA loading of the proposed configurations are 21 kVA for load-1 and 17 kVA for load-2. From the above values, it is observed that kVA loading of the proposed DSTATCOM configurations is significantly reduced compared to TPFL and TPSC topologies. Table. 6.2 also shows rms values of source currents before and after compensation, filter currents and loading of the inverter. From the table it is observed that the performance of all the proposed DSTATCOM configurations is almost similar in terms of harmonic compensation, load balancing, neutral current compensation and kVA rating of the inverter. The THD values of source currents are given in Table. 6.3 and they are well within the limits according to IEEE-519 standard.

The comparison between the proposed work and conventional topologies are given in Table. 6.4. In this table, Z represents zigzag transformer, T represents T-connected transformer and V_{mp} represnts amplitude of PCC voltage. Number of switches required in the proposed topologies are less when compared to existing four leg topology and split-capacitor topology. In general, rating of the switch means its voltage and current ratings. For a particular load, rating of the switches in the proposed FSOC and FSSC based DSTATCOM topologies is less when compared to the TPFL and TPSC topologies. This reduction in the number of switches, make the control circuitry simple, as only four switches are needs to be controlled. The voltage rating of the switches in TPSC and FSSC topologies are same and it is given as 1400 V. Similarly, in TPFL and FSOC topologies voltage rating of the switches is given as 700 V. But, from Table. 6.2, it is observed that the current flowing through the switches in proposed topologies is less when compared to existing TPFL and TPSC topologies.

In four switch topologies, FSSC topologies are preferred over FSOC, if the capacitor balancing problem and higher value of dc link voltage is not a constraint. Neglecting the size and other design issues created by the addition of passive filter, FSOC topologies are preferred over FSSC topologies. The rating of the zigzag transformer and T-connected transformer is nearly equal, but the T-connected transformer occupies less space. Quantity and cost of major components, namely, capacitors, IGBT module (one leg), driver circuits and special transformers are given in Table. 6.5. From the table, it is observed that cost offered by TPFS topologies is lower when compared to existing

TPFL and TPSC topologies. Because the cost added by including special transformer is lower when compared to cost reduced by eliminating IGBT modules. In four switch topologies, the cost of FSOC topology is lower when compared with FSSC topology due to the reduction in number of capacitors used for dc link. Therefore, after observing the above comparative analysis in terms control circuitry, cost and complexity, TPFS topologies are the effective solutions for DSTATCOM.

Table. 6.3 THD comparison of proposed four configurations

Duration	Topology	i_{sa} (% THD)	i_{sb} (% THD)	i_{sc} (% THD)
0.1 to 0.35 s	Without compensation	8.43	47.05	53.47
	FSOC (Z)	1.36	1.51	1.51
	FSOC (T)	1.40	1.55	1.63
	FSSC (Z)	2.84	2.86	2.38
	FSSC (T)	2.84	2.90	2.89
0.35 s to 1 s	Without compensation	9.47	18.62	49.36
	FSOC (Z)	1.19	1.18	1.26
	FSOC (T)	1.14	1.20	1.17
	FSSC (Z)	2.28	2.24	1.82
	FSSC (T)	2.32	2.30	2.20

Table. 6.4 Comparison in terms of various components

Parameters	TPFL [37], [38]	TPSC [34], [35]	FSOC (Z)	FSOC (T)	FSSC (Z)	FSSC (T)
Switches	8	6	4	4	4	4
Capacitors	1	2	1	1	2	2
LC Filters	0	0	2	2	0	0
Single-phase Transformers	0	0	3	2	3	2
V_{dc}	$2V_{mp}$	$4V_{mp}$	$2V_{mp}$	$2V_{mp}$	$4V_{mp}$	$4V_{mp}$

*where Z represents zigzag and T represents T-connected transformer.

Table. 6.5 Cost comparison of conventional and proposed topologies

Topology	Capacitor (4700 μF/450 V) B43743A5478 M000 (12143 Rs)	IGBT Module (SKM75GB 12T4=7051 Rs) (SKM75GB 17E4=8640 Rs)	Drivers (SKYPER 32R) (12593 Rs)	Special transformer (15000 Rs)	Total cost (Rs)
TPFL	1	4 (SKM75GB12T4)	4	0	90719
TPSC	2	3 (SKM75GB17E4)	3	0	87985
FSOC	1	2 (SKM75GB12T4)	2	1	66431
FSSC	2	2 (SKM75GB17E4)	2	1	81752

6.6 Experimental studies

Experimental studies are carried out for both FSOC and FSSC topologies with zigzag and T-connected transformer for supporting the simulation results presented in previous section. The parameters to implement the experimental setup is given in Table. 6.6. Supply voltages, load currents and dc link voltages are sensed using LEM made voltage and current transducers. The output the voltage and current transducers are given to dSPACE MicroLabBox 1202 which acts as an interface between real time environment and personnel computer (PC). ISCT is implemented using sensed signals to generate switching pulses and they are given to the inverter using MicroLabBox 1202. The photograph of the complete experimental setup is shown in Fig. 6.9. In the experimental setup, the required number of transducers are reduced because the number of phases to be controlled is two.

Table. 6.6 Experimental parameters

Parameters	Value
Supply voltage	50 V
Interfacing inductance (L_f)	8 mH
DC link capacitance (C_{dc})	3600 μF
DC link voltage (V_{dc}) (FSOC)	100 V
DC link voltage (V_{dc}) (FSSC)	200 V
Filter inductor (FSOC)	L_5 = 8 mH, L_7 = 4 mH
Filter Capacitor (FSOC)	C_5 = 50 μF, C_7 = 50 μF
Hysteresis band (h)	±0.1 A
Load-1	3-ϕ diode bridge rectifier load with 30 Ω, 150 mH
Load-2	unbalanced linear load Phase-a : 14 Ω, 18 mH, Phase-b : 14 Ω, 32 mH Phase-c : 14 Ω, 25 mH

6.6.1 Performance of FSOC inverter topology with special transformer

Fig. 6.10 shows the experimental results of FSOC topology with special transformers. In the figure, PCC voltages, load currents, source currents and filter currents are shown while load changing from balanced load to unbalanced load. A three-phase diode bridge rectifier is connected as a balanced load and the unbalanced load is realized by connecting three unequal values of impedance along with the balanced load. During balanced

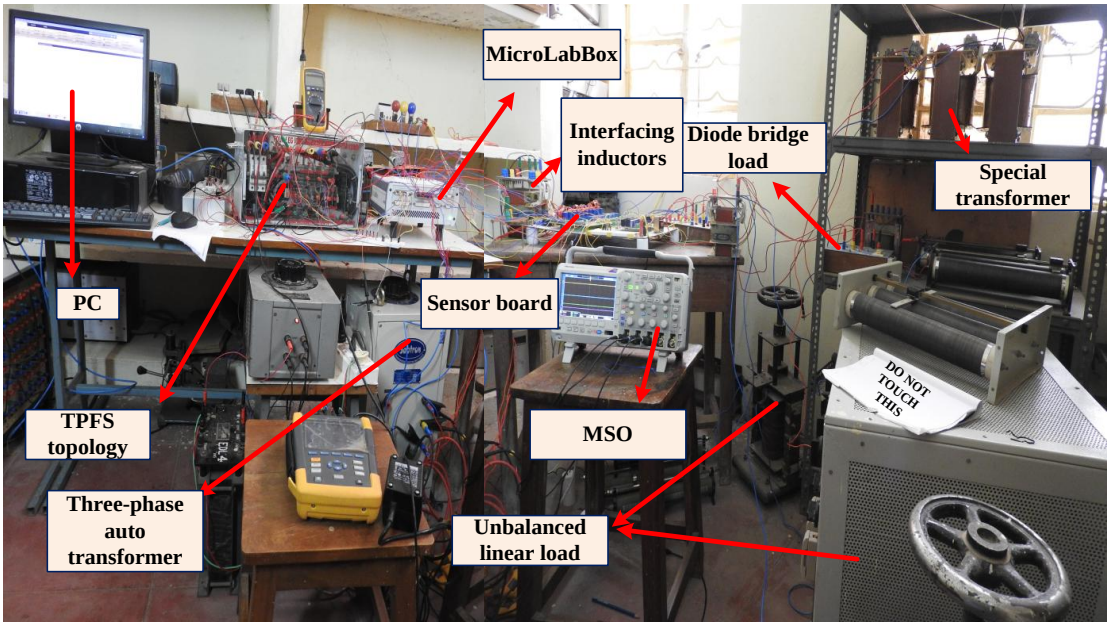


Fig. 6.9 Photograph of complete experimental setup.

load conditions, source and load neutral currents are zero. But during unbalanced load conditions, a considerable amount of neutral current will flow through the source before compensation, but after compensation the entire neutral current flows through the special transformer. Fig. 6.11 (a) shows, source neutral current, load neutral current, source current and dc link voltages before and after connecting DSTATCOM during unbalanced load. Before connecting DSTATCOM, source neutral and load neutral current are same, but after connecting the DSTATCOM, source neutral current is become zero which is shown in Fig. 6.11 (a). In FSOC topology, the required dc link voltage is 100 V for 50 V of line voltage and it is also shown in experimental results. Fig. 6.11 (b) also shows that the source neutral current, dc link voltage is not varying when the load is changing from balanced to unbalanced.

6.6.2 Performance of FSSC inverter topology with special transformer

Experimental results of FSSC inverter with zigzag and T-connected transformer connected as a DSTATCOM are shown in Fig. 6.12. In this figure, PCC voltages, load currents, source currents and filter currents are shown for both zigzag and T-connected FSSC DSTATCOM topologies. During non-linear balanced load condition, DSTATCOM makes source currents sinusoidal and in-phase with the respective voltages at

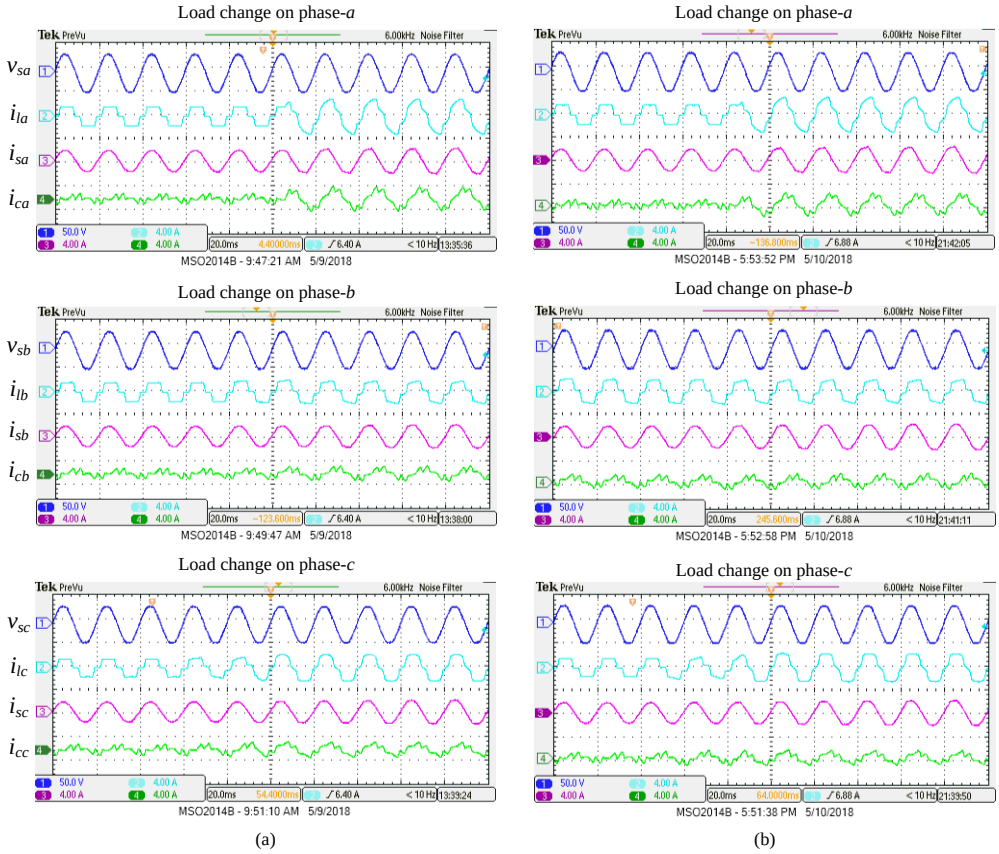


Fig. 6.10 Experimental results of FSOC with (a) Zigzag transformer, and (b) T-connected transformer.

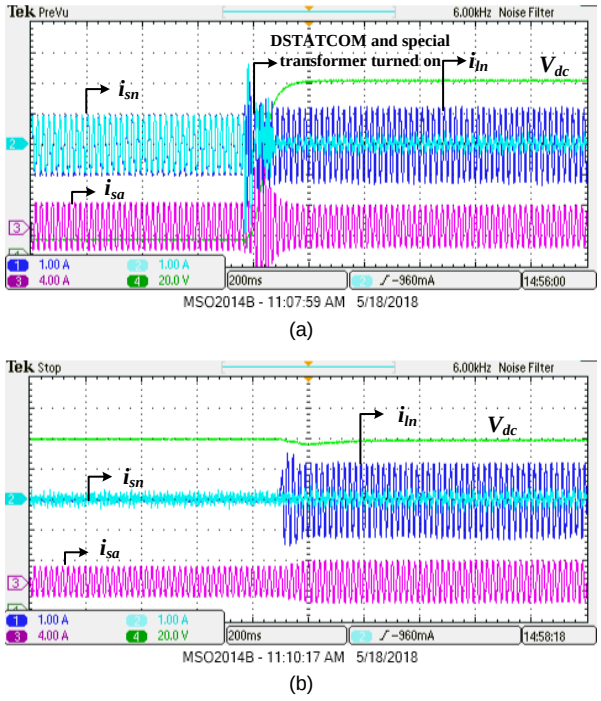


Fig. 6.11 Variation of neutral currents and dc link voltage (a) Before and after connecting DSTATCOM, and (b) During balanced and unbalanced load.

PCC. During unbalanced load, FSSC inverter topology achieved harmonic free source currents which are also in-phase with voltages at PCC. The special transformer provided a path for the entire neutral current so that the source currents become balanced.

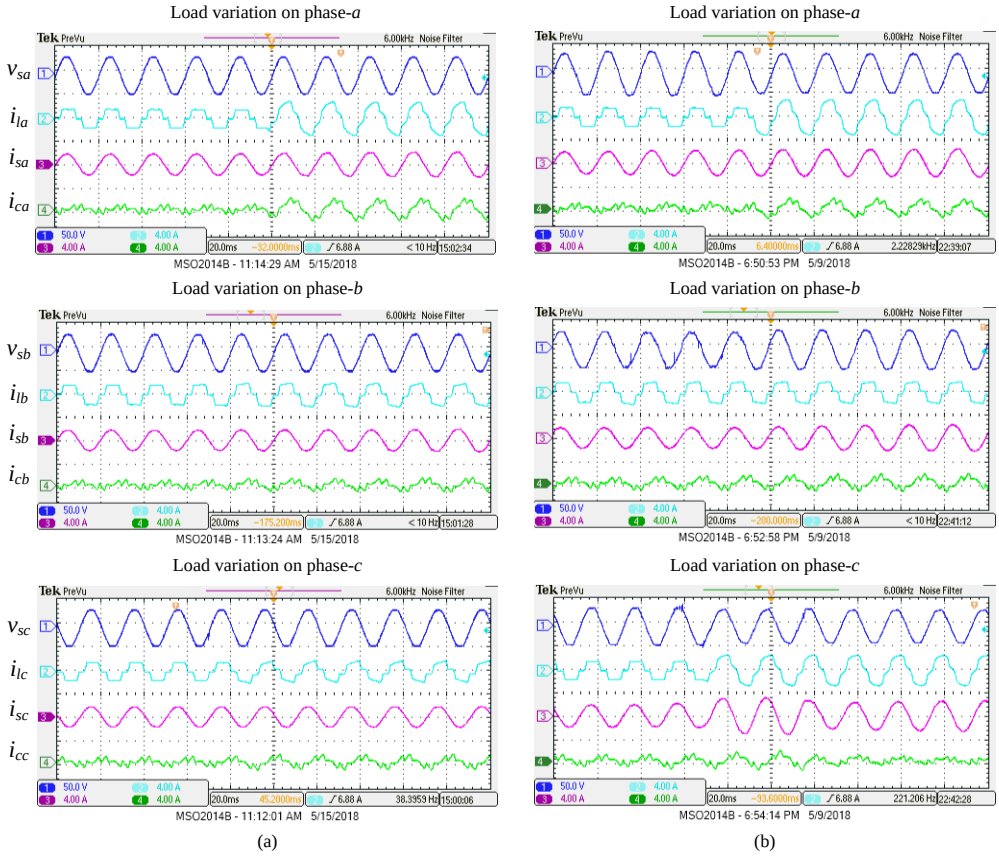


Fig. 6.12 Experimental results of FSSC with (a) Zigzag transformer, and (b) T-connected transformer.

6.7 Summary

In this chapter, four DSTATCOM topologies are proposed by using FSSC or FSOC inverter topology with zigzag transformer or T-connected transformer to compensate neutral current generated by non-linear and unbalanced loads. In addition to that, sinusoidal source currents with unity power factor is achieved. The other advantages of the proposed configurations are effective compensation during stringent load conditions, short term overloading capability and the low rating and cost compared to TPFL and TPSC topologies. The experimental studies are also proved that the performance is satisfactory during balanced and unbalanced load conditions.

CHAPTER 7

Conclusions and Future Scope of Research

7.1 Conclusions

The proliferation of power electronic devices in distribution systems degraded the quality of power supply. These power quality problems affect customers, manufacturers, leading to losses in production, wastage of raw material, missing data and equipment failure. Among the causes of power quality problems, operation of non-linear, unbalanced and reactive loads is considered to be significant reasons for power quality problems in modern distribution system. Therefore, the main objective of the research work considered in this thesis is compensation of current related power quality issues in three-phase four-wire distribution system.

With the continuous evolution of active power filters, the researchers are widened their compensation capabilities and formed a new group of compensating devices and they are named as custom power devices (CPD). DSTATCOM is a shunt connected CPD which is realized by using voltage or current source inverter with necessary passive elements and is connected at PCC. The inverter of the DSTATCOM is controlled to draw the compensating current from the ac power source, such that it cancels the reactive and harmonic current contained in the load current. Since voltage source inverter (VSI) is widely used in industrial applications, it has been considered in this thesis.

After going through the literature, it is observed that the conventional topologies namely three-phase split-capacitor (TPSC) and four leg DSTATCOM (FL-DSTATCOM) topologies are effectively compensating the current related power quality issues in 3P4W distribution system. However, TPSC topology has the limitation of capacitor voltage balancing. FL-DSTATCOM has the limitation of higher neutral leg switching frequency. The advantages of model predictive control (MPC) over conventional pulse width modulation (PWM) and hysteresis controllers motivated to apply it for TPSC and FL-DSTATCOM topologies to overcome the limitations along with compensation of power quality issues.

MPC with VlseKriterijumska Optimizacija I Kompromisno Resenje (VIKOR) method is proposed to overcome the limitations of TPSC DSTATCOM and MPC along with the compensation of power quality issues. From the simulation studies, it is observed that, with only current control the capacitor voltages are diverged during the compensation of unbalanced loads. The average switching frequency of IGBT switches of VSI is 22,405 Hz. Individual capacitor voltages are getting balanced by including capacitor voltage balancing constraint in the cost function. After including the switching frequency reduction constraint in the cost function average switching frequency is reduced by 42% (i.e., 12,818 Hz). The weighting factor selection is simplified using VIKOR method, so that proper balance is maintained among all control parameters of the cost function. From the experimental studies, it is observed that capacitor voltages are balanced and the average switching frequency is reduced by 40%. The simulation and experimental results prove that the proposed method is efficiently compensating the current related power quality issues, maintains equal voltage across two capacitors of dc link, reduces switching frequency and also simplified the weighting factor selection.

FL-DSTATCOM is controlled using MPC to compensate current related power quality issues under unbalanced and distorted supply conditions. The higher neutral leg switching frequency which is the limitation of FL-DSTATCOM is addressed by including an additional constraint in the cost function. The reduction in neutral leg switching frequency further reduce the phase leg switching frequencies. After including the switching frequency reduction constraint, switching frequency of neutral leg is reduced by 62% and phase leg is reduced by 32%. Finally, weighting factor selection during multi-constraint cost function is simplified using Technique for Order Preference by Similarity to the Ideal Solution (TOPSIS).

MPC has a limitation of variable switching frequency and it is addressed by the proposed constant switching frequency MPC with three dimensional space vector modulation (3DSVM). From the simulation studies of FL-DSTATCOM using conventional MPC, it is observed that the harmonic components are spread over entire area which implies that switching frequency is variable. However, with the proposed 3DSVM based MPC, the harmonics are centered around 10 kHz in simulation studies and 2 kHz in experimental studies. From these values it is observed that the switching frequency of the inverter is equal to the carrier signal frequency. The switching losses in phase legs are reduced by 28% and neutral leg is reduced by 58%. Finally, the simulation and ex-

perimental studies are also proved that the proposed control algorithm is compensated the current related power quality issues.

Finally, four different DSTATCOM configurations are proposed by using four-switch one-capacitor (FSOC) or four-switch split-capacitor (FSSC) inverter topology with a zigzag transformer or T-connected transformer. From the simulation and experimental studies, it is observed that, the proposed four configurations are compensating neutral current during stringent unbalanced loads along with harmonic elimination and reactive power compensation. It is also observed that the loading on VSI of proposed topologies is reduced by 30% for the considered load conditions. Similarly, the cost of the FSOC topology is 26% less and the cost of FSSC topology is 9% less compared to the conventional TPSC and FL-DSTATCOM topologies.

7.2 Future scope of research

The research work presented in this thesis discloses a number of issues that could be further investigated

- Two level VSI's are the viable solution for DSTATCOM applications in secondary distribution system where the voltage levels are either 415 V or 230 V. However, the limitations of two level VSI in primary distribution system are the requirement of higher rating switches or series connection of lower rating switches, which motivates the replacement of two level VSI's with multi-level inverters. Therefore, implementation of multilevel inverter based DSTATCOM topologies, for high power application is a potential area of research.

- Solar Photo-voltaic (SPV) energy is one of the important renewable energy, and in recent years it has been widely used in distributed generation systems. The proliferation SPV technologies and applications of SPVs in grid-connected systems indicate that SPVs are an attractive option to produce eco friendly electricity for diversified purposes. Therefore, application of MPC techniques to SPV supported grid connected inverters for active and reactive power control, active front end rectifier applications and solid state transformers.

- Another area will be on hybrid energy storage system based energy management scheme for SPV DSTATCOM. This research may include the selection of inverter topology, maximum power point tracking (MPPT) tracking techniques, compensation characteristics and cost of the system.

APPENDIX A

IMPORTANT DERIVATIONS

A.1 Derivation of In-Phase and Quadrature Unit Vectors

In a balanced three-phase system, the three-phase voltages are given as,

$$\begin{aligned} v_{sa} &= V_{sm}\sin\omega t \\ v_{sb} &= V_{sm}\sin(\omega t - 120^\circ) \\ v_{sc} &= V_{sm}\sin(\omega t + 120^\circ). \end{aligned} \tag{A.1}$$

Where v_{sa}, v_{sb}, and v_{sc} are the voltages at PCC and V_{sm} represents the amplitude of PCC voltage. V_{sm} is obtained by squaring and adding individual phase voltages and it is given as,

$$\begin{aligned} v_{sa}^2 + v_{sb}^2 + v_{sc}^2 &= \left(V_{sm}\sin\omega t\right)^2 + \left(V_{sm}\sin(\omega t - 120^\circ)\right)^2 + \left(V_{sm}\sin(\omega t + 120^\circ)\right)^2 \\ &= \left(\frac{3}{2}V_{sm}^2\right). \end{aligned} \tag{A.2}$$

From (A.1) and (A.2) it is observed that,

$$V_{sm} = \sqrt{\frac{2}{3}\left(v_{sa}^2 + v_{sb}^2 + v_{sc}^2\right)^2} \tag{A.3}$$

Required in-phase unit vectors (u_{pa}, u_{pb}, and u_{pc}) are obtained by dividing phase voltages with its amplitude (V_{sm}).

$$u_{pa} = \frac{v_{sa}}{V_{sm}}; \quad u_{pb} = \frac{v_{sb}}{V_{sm}}; \quad u_{pc} = \frac{v_{sc}}{V_{sm}}. \tag{A.4}$$

The phasor form of representing (A.4) is shown in Figure. Apply vector algebra to express the quadrature unit vectors (u_{qa}, u_{qb}, and u_{qc}) in terms of in-phase unit vectors

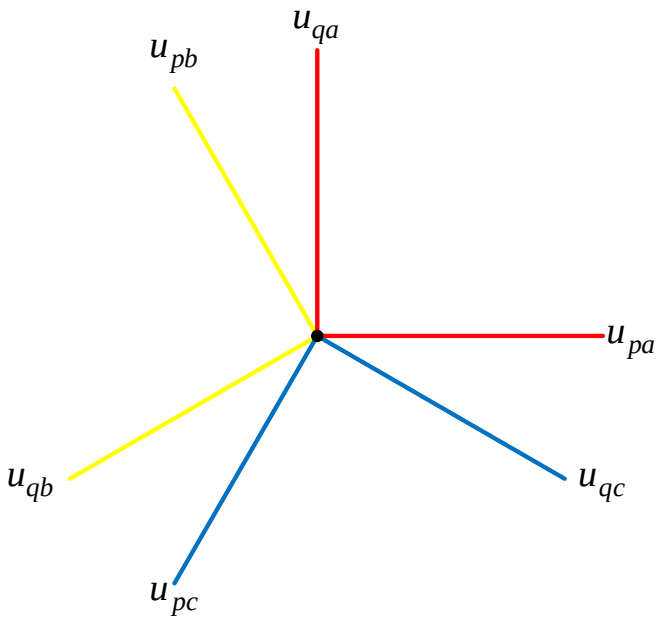


Fig. A.1 Phasor form of representing in-phase and quadrature unit vectors.

and they are given as,

$$u_{qa} = \frac{-u_{pb} + u_{pc}}{3}; \quad u_{qb} = \frac{3u_{pa} + u_{pb} - u_{pc}}{2\sqrt{3}}; \quad u_{qc} = \frac{-3u_{pa} + u_{pb} - u_{pc}}{2\sqrt{3}}. \tag{A.5}$$

A.2 Derivation of Lagrange's Second Oreder Extrapolation

Equation (3.26) represents the one-step-ahead prediction of reference currents and it is obtained using Lagranges extrapolation formula. Using this formula, nth order prediction is given as,

$$I^*(k+1) = \sum_{l=0}^{n} (-1)^{n-1} \binom{n+1}{l} I^*(k+l-n). \tag{A.6}$$

For n=1, (A.6) can be simplified as,

$$I^*(k+1) = 2I^*(k) - I^*(k-1). \tag{A.7}$$

Similarly, for n=2 the eqution will be,

$$I^*(k+2) = 3I^*(k) - 3I^*(k-1) + I^*(k-2). \tag{A.8}$$

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Journals

1. **A Pranay Kumar**, G Siva Kumar and D Sreenivasarao, "Three-phase four switch DSTATCOM topologies with special transformers for neutral current compensation and power quality improvement," ***IET Generation, Transmission & Distribution***, DOI: 10.1049/iet-gtd.2018.5841.

2. **A Pranay Kumar**, G Siva Kumar, D Sreenivasarao and H. Myneni, "Model predictive current control of DSTATCOM with simplified weighting factor selection using VIKOR method for power quality improvement," ***IET Generation, Transmission & Distribution***, DOI: 10.1049/iet-gtd.2018.6782.

3. **A Pranay Kumar**, G Siva Kumar and D Sreenivasarao, "Model predictive control with constant switching frequency for four leg DSTATCOM using three dimensional space vector modulation," ***IET Generation, Transmission & Distribution***, DOI: 10.1049/iet-gtd.2019.1775.

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1. **A Pranay Kumar**, G Siva Kumar and D Sreenivasarao, "Model predictive control with TOPSIS method for four leg DSTATCOM to improve power quality and reduce switching frequency," ***International Transactions on Electrical Energy Systems***, 2019 (Under review).

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1. **A Pranay Kumar**, G Siva Kumar and D Sreenivasarao, "Conductance factor based control method for DSTATCOM to improve power quality", *2017 7th International Conference on Power Systems (ICPS)*, Pune, 2017, pp. 307-312.

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