CONTROL OF REDUCED SWITCH COUNT MULTILEVEL INVERTERS IN GRID CONNECTED PV SYSTEMS

Submitted in partial fulfilment of the
requirements for the award of the
degree of

DOCTOR OF PHILOSOPHY

By

G Mahanandeswara Gowd

(Roll No. 714009)

Under the supervision of

Dr. D. Sreenivasarao

Assistant Professor

DEPARTMENT OF ELECTRICAL ENGINEERING

NATIONAL INSTITUTE OF TECHNOLOGY

WARANGAL – 506 004, TELANGANA, INDIA

APRIL - 2020

APPROVAL SHEET

This Thesis entitled "**Control of Reduced Switch Count Multilevel Inverters in Grid connected PV Systems**" by **G. Mahanandeswara Gowd (Roll No. 714009)** is approved for the degree of Doctor of Philosophy.

Examiners

_____

_____

_____

Supervisor

Dr. D. Sreenivasarao
Assistant Professor
EED, NIT Warangal

Chairman

Dr. Sailaja Kumari M
Professor & Head
EED, NIT Warangal

Date: _____

DEPARTMENT OF ELECTRICAL ENGINEERING
NATIONAL INSTITUTE OF TECHNOLOGY
WARANGAL – 506 004

DEPARTMENT OF ELECTRICAL ENGINEERING
NATIONAL INSTITUTE OF TECHNOLOGY WARANGAL

CERTIFICATE

This is to certify that the thesis entitled **"Control of Reduced Switch Count Multilevel Inverters in Grid connected PV Systems**,**"** which is being submitted by **G. Mahanandeswara Gowd (Roll No. 714009)**, is a bona fide work submitted to National Institute of Technology, Warangal in partial fulfilment of the requirement for the award of the degree of **Doctor of Philosophy** in Department of Electrical Engineering. To the best of my knowledge, the work incorporated in this thesis has not been submitted elsewhere for the award of any degree.

Supervisor

Dr. D. Sreenivasarao
Assistant Professor
EED, NIT Warangal

Date:
Place: NIT Warangal

DECLARATION

This is to certify that the work presented in the thesis entitled "Control of Reduced Switch Count Multilevel Inverters in Grid connected PV Systems" is a bona fide work done by me under the supervision of Dr. D. Sreenivasarao, Department of Electrical Engineering, National Institute of Technology Warangal, India and was not submitted elsewhere for the award of any degree.

I declare that this written submission represents my ideas in my own words and where others ideas or words have been included are adequately cited and referenced the original sources. I also declare that I have adhered to all principles of academic honesty and integrity and have not misrepresented or fabricated or falsified any idea/date/fact/source in my submission. I understand that any violation of the above will be a cause for disciplinary action by the institute and can also evoke penal action from the sources which have not been properly cited or from whom proper permission has not been taken when needed.

G. Mahanandeswara Gowd

(Roll No. 714009)

Date:
Place: NIT Warangal

ACKNOWLEDGEMENT

Apart from personal efforts and steadfastness to work, constant inspiration and encouragement given by a number of individuals acted as the driving force in attaining this day in my life. To quote them all may be an onerous task but direct and indirect assistance and guidance received is gratefully acknowledged. I would like to express my feelings of gratefulness and submit my acknowledgement for them further in the following lines.

I take this opportunity to express my sincere gratitude towards my supervisor **Dr. D. Sreenivasarao**, Assistant Professor, Electrical Engineering Department (EED), National Institute of Technology Warangal (NITW), for his proficient and enthusiastic guidance, valuable suggestions, discussions, continued encouragement and constant inspiration throughout the course and critically examining thesis write-up. I extend my gratitude to his families for their patience and perseverance for smooth completion of my course.

I also express my sincere gratitude towards my doctoral scrutiny committee (DSC) Chairman **Prof. M. Sailaja Kumari,** and members namely, **Prof. M. Sydulu** (EED), **Dr. G. Siva Kumar**, and **Dr. K. Kiran Kumar** (Mechanical Engineering Department) and Former co-supervisor **Dr. P. C Sekhar** (Assistant Professor, EED, IIT Bhubaneshwar) for their valuable suggestions and cooperation.

I wish to express my sincere thanks to **Prof. N.V. Ramana Rao**, Director, NIT Warangal for his official support and encouragement.

I am thankful to **Prof. S. Srinivasa Rao and Prof. V. T. Somasekhar**, Former Heads, EED for their constant encouragement, support and cooperation.

I also appreciate the encouragement from teaching, non-teaching members, and fraternity of Department of Electrical Engineering of NIT Warangal. They have always been encouraging and supportive.

I also acknowledge my sincere gratitude to the Ministry of Human Resources Development (MHRD), Government of India for their financial support to carry out this research.

I also acknowledge the warm support of my well-wishers and co-scholars for their instant help, cooperation, advice, suggestion, and moral support during my stay. The list may go long but I would like to mention some of them: Dr. Hareesh, Dr. Hari Priya, Dr. Jammy Rahul, Dr. Ratna Rahul, Mr. Ram Kumar, Dr. Bonala Anil kuamar, Mr. Pranay Kumar, Dr. Kiran, Dr. Praveen, Mr. Abhilash, Mr. Rambabu, Dr. Sachidananda Prasad, Mr. Anil Kumar, Mr. Kalyan Kumar, Mr. Jaya Krishna, Mr. Venkateshwar Reddy, Mr. Eshwar and Mr. Sagar.

Finally, I wish to express my deepest gratitude to my father **Late G. Gangadhara Goud**, mother **Eshwaramma**, Brother G. Sreeshaila Goud, Sisters Sharadha and Adilakshmi, nieces Shivani, Mythri, Chandrakala and Shanti, for their patience, endless support, trust and encouragement.

May all praises be to the Almighty, the most beneficent, and the most merciful.

(*G. Mahanandeswara Gowd*)

ABSTRACT

Photovoltaic (PV) energy is rapidly becoming an important part of the energy mix in all countries across the globe. The enormous growth in PV installations led to the reduction in the cost of PV modules and also caused the evolution of conventional PV power converters from classic single-phase grid-connected inverters to more complex topologies such as multilevel inverters (MLI) to increase capacity, efficiency and reliability. In recent years, focus on multilevel inverters (MLIs) has been increased due to their ability to improve the quality of output voltage, reducing the total harmonic distortion (THD), low *dv/dt* and operate medium-voltage semiconductor devices. Cascaded H-bridge (CHB), diode clamped (DCMLI), flying capacitor (FCMLI) are conventional MLI topologies. In particular, the CHB MLI is more dominant than DCMLI and FCMLIs in the domain of high-power grid connected applications. However, these conventional MLIs require large number of switch count to generate a high number of voltage levels. This leads to increase in complexity and cost of the MLI. To overcome these drawbacks in conventional MLIs, researchers are continuously working to reduce the switch count, thus emerged an area of research, named as reduced switch count (RSC) MLI topologies.

The objectives of RSC-MLI are to generate higher number of level with less number of switching devices, diodes and dc sources. The RSC-MLIs may operate with reduced switching and conduction losses as the reduction in on-state switches and operation of some switches at low frequency. From the past decade, various researchers carried out extreme innovations on RSC-MLIs and developed numerous topologies with significant reduction in component count, total blocking voltage, cost and ease of control. Several RSC-MLI topologies such as multilevel dc link (MLDCL), switched series parallel sources (SSPS), packed U-cell (PUC), cascaded bi-polar switched cells (CBSC), reverse voltage (RV), switched dc sources (SDS), T-type, hybrid T-type, basic unit MLI, envelope-type (E-type), square T-type (ST-type), series-connected switched sources (SCSS), and various other three-phase and cascaded topologies are reported in literature. In this thesis, qualitative and quantitative features of RSC-MLI topologies have been discussed and a comparison has been made to facilitate a well-informed selection of topology for grid connected applications.

Among these most attractive topologies are MLDCL, SSPS and T-type. T-type RSC-MLI offers significant decrease in switch count but lack of switching redundancies, inability to adapting with asymmetrical dc voltage sources, inability to attain uniform power distribution of dc sources, uneven blocking voltages acts as major limitation. On the other hand, MLDCL and SSPS RSC-MLIs consist of simplified, modular and generalized

topological structure with considerable decrease in switch count, multiple switching redundancies, possibility of connecting asymmetric dc sources and simplified switching operation, fault tolerant ability, uniform power distribution, uniform blocking voltages across switches and dc link voltage balancing capability. Due to these key and worthy merits, MLDCL and SSPS had gathered more attention and serve as an alternate to CHB MLI for applications such as grid connected PV system, active front-end converters, custom power devices, battery energy storage system and hybrid electric vehicle.

In most of the MLIs, the utilization of all the sources at all levels is seldom. These topologies will diminish the energy efficiency of the conversion system as all the sources will not deliver the power except at the highest level in the output voltage. These kinds of converters can hamper the penetration of renewable energy into the existing energy mix, as the energy capacity of the renewable source is undermined. In this connection, this thesis explores the series/parallel switching of dc sources in SSPS RSC-MLI. This inverter can extract the power from all the sources at all the levels through series/parallel switching. In addition, this thesis work introduces a new performance indicator named "utilization factor" (*UF*) to quantify the utilization of dc sources.

In this connection, a comprehensive comparison among CHB, MLDCL and SSPS RSC-MLI topologies has been carried out in terms of utilization factor (*UF*), switch count, current rating of the dc sources and switches, operating frequencies of switches and total blocking voltage. For this comparison, 11-level inverters are considered with input dc source voltage ratio of 1: 2: 2. Based on the comparative analysis, MLDCL and SSPS RSC-MLI topologies are most suitable and an effective alternate to conventional CHB MLI for interfacing unequal input dc sources such as PV to grid by using less complex and common control philosophy. In view of this, asymmetric SSPS and MLDCL RSC-MLIs are considered for further research.

In grid connected MLIs, for achieving decoupled active and reactive power control, conventional PI controllers are susceptible for different operating conditions. Since they tuned only for a particular operating point and their steady-state response time are also high. PI controllers cannot avoid the disturbances which exist in the system and those are sensitive to system parameters variations. Moreover, the MLI based systems are highly nonlinear and changes its connection configuration for every voltage level. Therefore, the linear controllers will not give satisfactory performance at all the operating points. The performance of MLIs further degrades with change in operating conditions, system parameter disturbances and during prevailing model oscillations.

To address all these issues, a sliding mode based nonlinear controller has been adapted for the closed-loop control of grid connected MLIs. In sliding mode control (SMC), the

switching action is in such a way that the state direction of the system is brought back to sliding surface and track the equilibrium point. SMC offer good robustness because sliding surface and switching are independent of system operating points and other circuit parameters. On the other hand, MLI based grid connected systems are highly nonlinear and coupled in nature. Therefore, to design a SMC for grid connected applications, a feedback linearization technique is adapted in the present work to convert into linear system designated by algebraic equations.

The performance of proposed SMC for grid connection of SSPS RSC-MLI is validated in MATLAB/Simulink environment and later verified in real-time environment using OPAL-RT system. For these studies a three-phase 11 kV, 1 MVA SSPS RSC-MLI with 1: 2: 2 dc voltage ratio is designed and connected to 11 kV grid. The performance of the proposed variable gain nonlinear controller is validated against the PI controller for delivering desired powers under different operating conditions/disturbances using simulations and real-time environment. To verify the performance of the proposed system in real-time environment, two OP4500 modules of OPAL-RT are integrated. Out of these two, the first module works as a plant, i.e., grid connected SSPS RSC-MLI whereas the second module works as controller, i.e., SMC or PI based PWM generator. The plant system along with its interface generates analog signals according to the operating conditions and disturbances, which will be acquired by controller through DB-37 communication channel.

Further, the research work continued towards the grid integration of RSC-MLI based MLDCL inverter for PV system. As similar to CHB, the structure of MLDCL allows even power distribution between equal rated input PV sources. Therefore, a common maximum power extraction control method can be applied for multiple equal rated PV sources, thereby reducing the control complexity. In this connection, a robust nonlinear SMC is designed to extract maximum power from each single-stage PV source. To validate the proposed control scheme, a single-stage, three-phase, 11 kV grid connected asymmetrical 11-level MLDCL inverter with PV sources in 1: 2: 2 voltage ratio has been considered. Two SMCs are developed to extract maximum power from each group of equal rating PV sources. The performance of SMC under variable irradiance conditions is verified against PI controller, and the results are analysed in MATLAB and hardware-in-loop OPAL-RT test beds.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF ACRONYMS

ac, AC	Alternating Current
AFC	Active Front-end Converter
ASD	Adjustable Speed Drive
BESS	Battery Energy Storage System
CBSC	Cascaded Bi-polar Switched Cell (RSC-MLI topology)
CHB	Cascaded H-bridge
CSI	Current Source Inverter
dc, DC	Direct Current
DCMLI	Diode Clamped Multilevel Inverter
E-type	Envelope Type (RSC-MLI topology)
FCMLI	Flying Capacitor Multilevel Inverter
HEV	Hybrid Electric Vehicle
IGBT	Insulated Gate Bipolar Transistor
LSPWM	Level-shifted Pulse width Modulation
MLDCL	Multilevel dc-link (RSC-MLI topology)
MLM	Multilevel Module (RSC-MLI topology)
MPPT	Maximum Power Point Tracking
PI	Proportional and Integral
PLL	Phase Locked Loop
PSPWM	Phase-shifted Pulse width Modulation
PWM	Pulse width Modulation
RMS	Root Mean Square
RSC	Reduced Switch Count
RSC-MLI	Reduced Switch Count Multilevel Inverter
SDS	Switched dc-sources (RSC-MLI topology)
SMC	Sliding Mode control
THD	Total Harmonic Distortion
VSI	Voltage Source Inverter

LIST OF SYMBOLS

UF	Utilization factor of input dc sources of a multilevel inverter
f_s	Switching frequency
f_m	Modulating signal frequency
v_{abc}	Three-phase supply voltages
i_{abc}	Three-phase source currents
v_{dg} ,v_{qg}	Grid voltages at PCC in the *d–q* frame of reference
i_{dg} , i_{qg}	Grid currents at PCC in the *d–q* frame of reference
$v_{d\text{inv}}$, $v_{q\text{inv}}$	Multilevel inverter voltages in the *d–q* frame of reference
ω	Angular frequency of grid voltage
σ, S_{pv}	Sliding surfaces
q_n	Relative degree of an output state variable
λ, δ_{pv}	State vector matrices
Y, Y_{pv}	Output state matrices
G, L	Lyapunov function
ρ, M	Sliding mode parameters
PV	Photo-voltaic
V_{PV}	PV voltage
I_{PV}	PV current
P_g	Grid power
Vg	Grid voltage
L_f	Filter inductance
T_s	Sample time

CHAPTER 1: INTRODUCTION TO GRID CONNECTED PV SYSTEMS

This chapter presents a brief introduction to high-power medium-voltage grid connected photovoltaic (PV) system. It starts with an overview of grid connected PV system layout and their control. Later, discusses the literature on dc to ac power converters and then address the importance of multilevel inverters (*MLIs*) *and then demonstrates the importance of reduced switch count (RSC) MLIs. Finally, motivation of the work, objectives and thesis organization are explained.*

1.1 Introduction

The photovoltaic (PV) energy has grown at an average annual rate of 60% in the last five years, surpassing one third of the cumulative wind energy installed capacity [1]. PV energy is quickly becoming an important part of the energy mix in all countries. The enormous growth in PV installations led to the reduction in the cost of PV modules and also caused the evolution of conventional PV power converters from classic single-phase grid-connected inverters to more complex topologies such as multilevel inverters (MLI). This will increase capacity of PV system, efficiency and reliability without affecting the cost. This chapter presents an overview of PV systems and power converter topologies that have found practical suitability in grid-connected applications.

1.2 Grid connected photovoltaic system

The PV sources are connected either in standalone mode or grid connected mode. In standalone mode, PV sources are directly connected to commercial or residential load centres. In grid connected mode, the PV system is in synchronism with grid and injects the generated PV power to grid. Nowadays, the grid integration of PV systems is enormously increasing in many countries. Nearly, 75% of the PV system installations around the world are operating in grid connected mode [2]. In the coming years, the supply of power from PV systems to the grid will further increase. The grid tied PV system comprises of PV sources, power converters and power controlling unit as shown in Fig. 1.1.

1.2.1 Photovoltaic sources

In PV system, the basic element is a semiconductor material called PV cell. This will convert sunlight into dc power based on the principle of photovoltaic effect. However, the voltage generated by a single PV cell is typically 0.5 V which is very less and it is not sufficient for the loads. Hence, several PV cells are connected in series to increase the voltage to higher levels. The series connection of PV cells called as PV module as shown Fig. 1.2. The PV modules can also

connected in series for further increase in voltage levels, which will make a PV panel. For high voltage and high power applications, to achieve the required voltage and currents, these PV panels connected in series and parallel respectively and this arrangement is known as PV array as shown in Fig. 1.2.

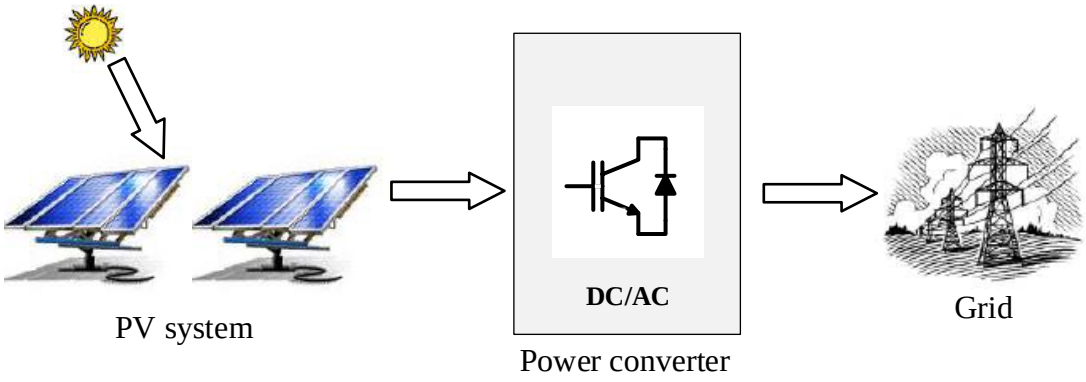


Fig. 1.1: Schematic view of grid connected PV system.

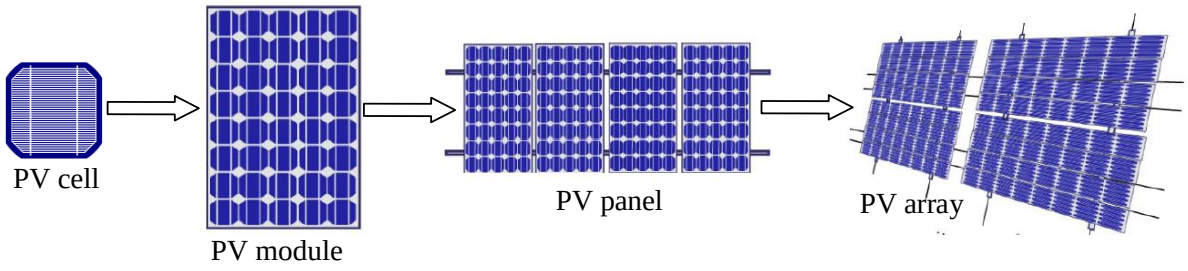


Fig. 1.2: Formation of PV module, PV panel and PV array using PV cells.

In grid connected PV system, the power converter plays an interface between PV source and grid. It converts the dc voltage generated by PV source to ac voltage and appropriately condition the available solar power before injecting into the grid. In general, photovoltaic conversion system mainly arrange in two ways. They are double-stage and single-stage conversion systems.

1.2.1.1 Double-stage PV conversion system

In double-stage system, there are two stages for converting the dc to ac voltage as shown in Fig. 1.3(a) [3]. The first stage incorporates a dc-dc converter and the second stage consists of dc to ac inverter. Conventionally, in first stage, the dc-dc converter is controlled in such a way that it boost the voltage of the PV array and then track the maximum solar power i.e., maximum power point tracking (MPPT). Typically, the first stage consists of either boost or buck-boost dc-dc converter. The second stage inverts the dc power into ac power. The purpose of control of dc to ac converter is to ensure proper power feeding into the grid. The design of the controllers for the double-stage system is easy. This is because, dc-dc convertor in the first stage and dc-ac converter in second stage have independent control objectives and configurations [3]. However, the efficiency of the double-stage conversion system is compromised due to the large number of

individual devices present in the dc-dc convertor and dc-ac inverter. Heavy weight, high cost and large size are the drawbacks of double-stage PV energy conversion system.

1.2.1.2 Single-stage PV conversion system

Nowadays, single-stage PV power conversion is increasingly popular [4]. In single-stage PV system, only one power handling stage is required to convert the PV power to ac supply. The single-stage power processing system is shown in Fig. 1.3(b). The single-stage system can perform both maximum power point tacking and the inversion. In this stage, the inverter has alone to achieve all control objectives. It has the advantages of lower cost, improved efficiency, modularity and less size as compared to double-stage. Further, this system has more reliability, since the chance of device failure is lower than other configurations with higher number of devices. Also, it has been specified that removing a dc-dc converter stage decreases the overall cost of grid-connected PV system and makes this selection more attractive in practical applications [4].

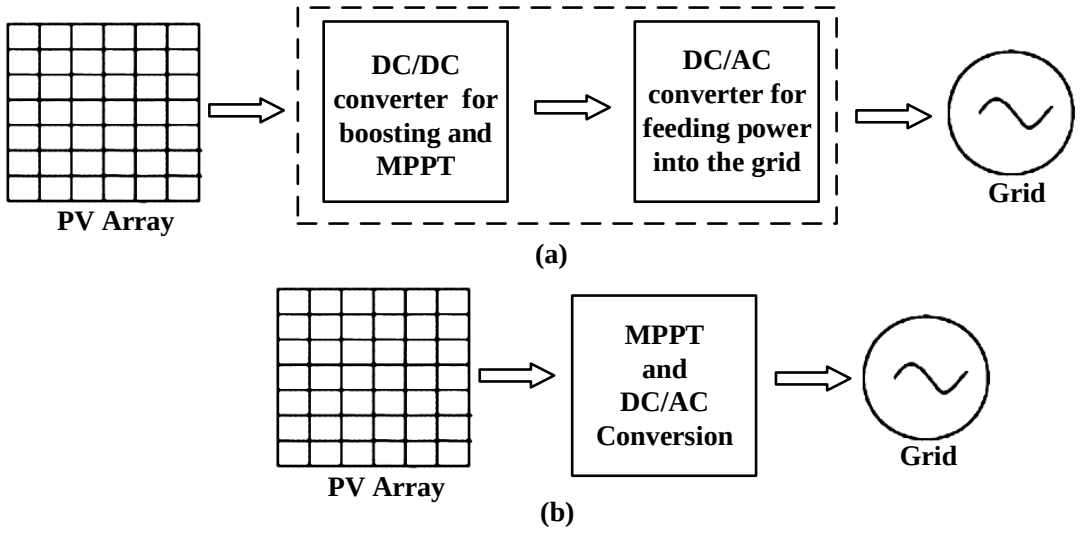


Fig. 1.3: PV system configurations: (a) Double-stage and (b) Single-stage conversion.

1.2.2 Maximum power point tracking (MPPT)

The voltage and power of a PV system have a non-linear relationship. Therefore, it is essential to operate the PV system at the point of maximum power. The maximum power point depends on environmental factors, such as insolation and temperature. The maximum power point tracking (MPPT) is required to improve the PV system efficiency. The MPPT algorithms are implemented in PV systems, which can always generate the maximum possible power irrespective of the environmental conditions. From past two decades, several MPPT methods have been established and employed such as perturb and observe method, incremental conductance method, constant voltage (CV) method, fuzzy logic and neural network based MPPT methods [5-11].

1.3 Control of grid connected PV systems

Grid interfaced PV systems requires a power-conditioning unit which is connected between the PV sources and the grid. These systems are intended to function in parallel with the grid as shown in Fig. 1.4 [12]. The power conditioning unit comprise of an MPPT algorithm, power converter and the grid interface control system. It has to perform two functions:

- Generate maximum power from PV arrays at difference irradiance levels.
- Inject the extracted maximum power into the grid at various insolation levels, i.e., control of inverter, which ensures the control of active and reactive powers injected into the utility grid.

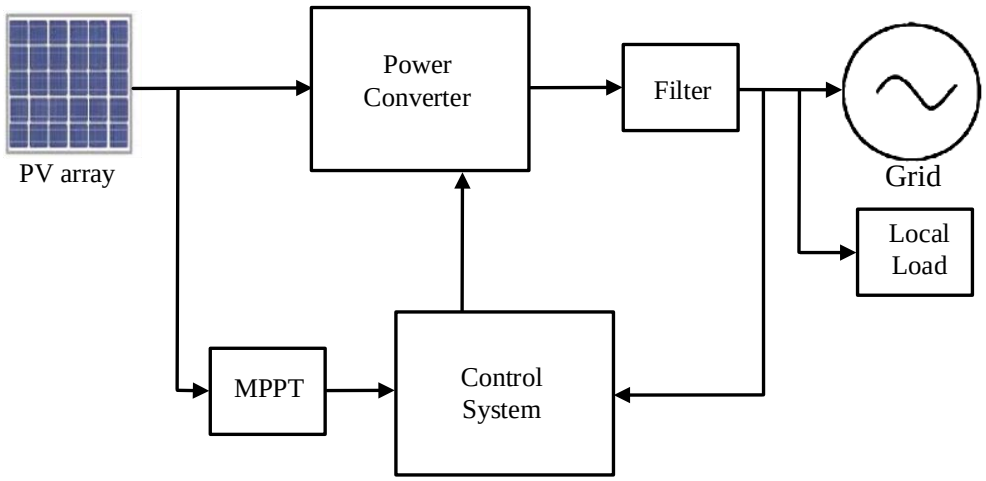


Fig. 1.4: Control of grid interfaced PV system.

In order to extract maximum power under varying irradiance conditions, most of the MPPT methods use PI controllers which are thoroughly used and well-known in many industrial applications [13]. The adaption of conventional PI control for extraction of maximum power from PV system is shown in Fig. 1.5. Here, the PI controller generates the duty cycle required for the switching operation of the buck-boost converter to track the reference voltage [13]. The reference voltage is generated from MPPT method and this voltage provides the corresponding maximum power, being extracted depending on the environmental conditions. Under steady-state, the actual PV voltage reaches the reference voltage by modulating the switches in dc-dc converter.

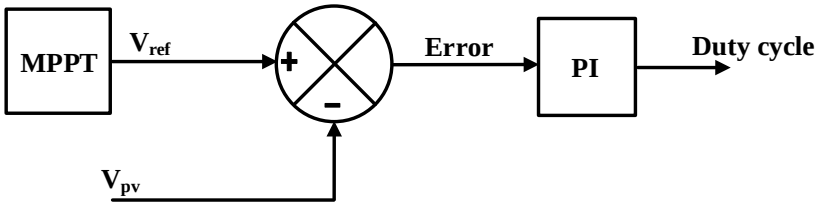


Fig. 1.5: The conventional PI for maximum power extraction.

The control of active and reactive power injected to the grid is achieved by controlling dc to ac inverter. In general the control methods for grid connected three-phase inverters are formulated

in *abc*, *αβ0* or *dq0* reference frame [14]. Among these, the simple and prominent method to control both active and reactive power is decoupled current controller in *dq* reference frame [14]. In this, the grid currents and voltages which are in *abc* reference frame are converted into the *dq* frame of reference by using Clark and Park transformations. This conversion can decouple the ac current into active (I_d) and reactive (I_q) components. These current components are controlled to reduce the error between actual and the reference values of active and reactive powers. In general, the *dq* control scheme for three-phase grid-tied PV inverters use conventional PI controller [15]. However, grid connected PV systems show nonlinear performance due to the inherent features of the PV cell and nonlinear switching function of the inverter [16]. Hence, the control of this non-linear system using conventional PI controller is a complex task. Further, nonlinearities in the system could adversely affect its performance, if they are not sufficiently compensated. The main challenge for controlling the nonlinear systems is the presence of inaccuracy in the system modelling. The nonlinear control schemes have improved the field of research and has demonstrated as most suitable for the control of nonlinear systems [17-20].

1.3.1 Modelling inaccuracies

The inaccuracy in nonlinear system model may arise due to the uncertainties around the plant (e.g., unidentified plant parameters), or due to the purposeful selection of a simplified description of the system's dynamics [21]. Modelling inaccuracies can be classified into two major categories: parametric (or structured) uncertainties and unmodelled dynamics (or unstructured uncertainties). The first kind relates to inaccuracies on the terms actually involved in the model, while the later one corresponds to inaccuracies in the system order. Modelling inaccuracies may leads to strong unfavourable effects on nonlinear control systems.

In order to deal with model uncertainty, one of the most significant method is robust control [22]. The general structure of a robust controller has a nominal part, a feedback control law, and extra terms directed to allocating with model uncertainties. Among the existed advanced robust control schemes, sliding mode control (SMC) and feedback linearization are popularly used. SMC strategy offers disciplined approach to retain stability and reliable performance in the face of modelling inaccuracies.

1.3.2 Sliding mode control (SMC)

Sliding mode control (SMC) is a nonlinear control method containing extraordinary properties such as accuracy, robustness, ease in implementation and tuning. SMC controllers are designed to force the system states onto a specific surface in the state-space, known as sliding surface. Once the sliding surface is achieved, sliding mode control retains the states on the near to region of the sliding surface. The SMC is a two part controller strategy. The first part includes the

design of a sliding surface so that the sliding motion fulfils the design specifications. The second part is concerned with the choice of a control law that will create the switching surface striking to the system state [23].

There are two major benefits with SMC. The first one is improvement in the dynamic performance of the system by the precise selection of sliding function. Secondly, the response of the system becomes entirely unaffected to specific uncertainties. This principle ranges to system parameter uncertainties, nonlinearity and disturbance which are bounded. From a real-time point of view, SMC permits for controlling nonlinear closed-loop systems under exterior disturbances and heavy system uncertainties. In general, in SMC, Lyaponov stability method is applied to keep the nonlinear system under control [22].

1.3.3 Lyaponov stability theory

The function of a control system is categorised into two types; (1) stabilization and (2) tracking [24]. In stabilization process, the control system is modelled in such a way that the state of the closed-loop system is settled about the equilibrium point. In tracking control process, a controller is designed in such that, the actual output track the desired trajectory and stabilize the complete system. Tracking process is more challenging than stabilization problem. This is because, tracking problem ultimately covers the stabilization problem [24]. The Lyapunov theory defined as, if a function is positive definite and its derivative is negative or zero, then that function is a positive constant or decrease to zero [25] i.e., the system is asymptotically stable.

Based on the Lyapunov theory, the control law is organized as feedforward and feedback measures to track the chosen trajectory besides stabilizing the closed-loop system. The feed forward part is responsible for the required input for tracking the chosen trajectory and nullifying the effects of identified disturbances, whereas the feedback part alleviates the tracking error dynamics [24]. The basic literature on Lyapunov theory are given in [24, 26].

Besides SMC, another advanced control solution for the nonlinearities existed in a system is feedback linearization technique and is explained below.

1.3.4 Feedback linearization

In general, grid connected converter and PV systems are highly nonlinear and coupled in nature. Hence, conventional PI controller will not give satisfactory performance for uncertain load changes and ever changing operating conditions. Feedback linearization [27] is a method in nonlinear system control, which converts all or part of nonlinear dynamic systems into linear system(s) by using algebraic equations. In other words, linearization scheme transforms main model of the system into a simple form of equivalent models that can be used in designing robust controller for nonlinear systems.

One of the limitation of the feedback linearization is lack of sufficient robustness in presence of uncertainties in system parameters [28] i.e., variation of parameters in the system. This may results in undesired response and unstable the system. Therefore, in nonlinear system with parameter uncertainties, feedback linearization may be linearize the system around some of its operating points in the parameter deviation region. Hence, the developed controller cannot deliver an appropriate response except in one or some points of parameter's variation region. In order to address the the issues of uncertainty and to add robustness to the control algorithm, SMC technique can be incorporated in the feedback linearized control and it is explored in this thesis work.

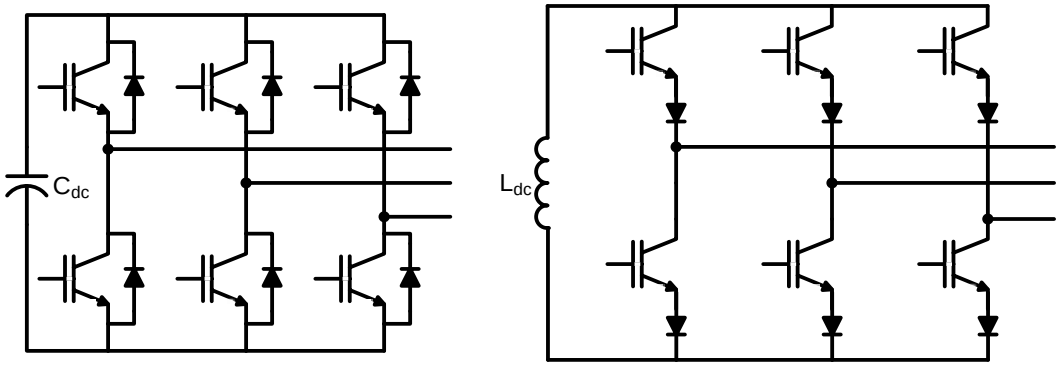
1.4 Introduction to dc-ac inverters

DC to ac static power inverter plays an important role in various power conversion stages in generation, transmission and distribution systems. High-performance and economical inverter is necessary for power electronics applications such as renewable energy generation, adjustable speed drives, high-voltage dc (HVDC) transmission, uninterruptible power supplies (UPS), flexible AC transmission system (FACTS), electric vehicles (EV) and battery energy storage systems (BESS). In early days, static power converters are developed with forced commutating switching devices such as thyristors. Conversely, with the advancement in the research of semiconductor devices and significant development of gate (or self) commutated semiconductor switches, attention has been shifted towards power electronic inverters with self-commutating switches.

Based on the dc link energy storage element, the inverters can be classified as voltage source inverters (VSIs) and current source inverters (CSIs) [29-31]. The voltage source dc-ac conversion system shown in Fig. 1.6(a) operates by applying a capacitor with a regulated dc voltage. Whereas the current source inverter, shown in Fig. 1.6(b) operates by using an inductor at the input side for supplying a regulated dc current. However, one may prefer CSI due to its robustness or the VSI due to its high efficiency, low initial cost, and smaller physical size [32, 33]. Since VSI technology is widely used in industrial applications, this has also been more common in applications such as FACTS, CPD, ASD and REG [29] and hence, VSI has been considered in this thesis.

The popular two-level VSI is also suitable for medium and high-power applications [34]. To produce the desired voltage and current levels in the inverter, several semiconductor switches are connected in series and parallel respectively. Hence, each inverter leg consists of two groups of active switches, each comprising of two or more switching devices connected in series/parallel, dependent on the ratings of dc link voltage, load current and available ratings of switches. Further,

several capacitors in series could be essential to realize the required voltage in dc link [34]. The structure of high-power two-level VSI is shown in Fig. 1.7. In this structure, each switch consists of three semiconductor devices connected in series and operate with a common gate signal.



(a) Voltage source inverter (b) Current source inverter

Fig. 1.6: Topologies of inverters.

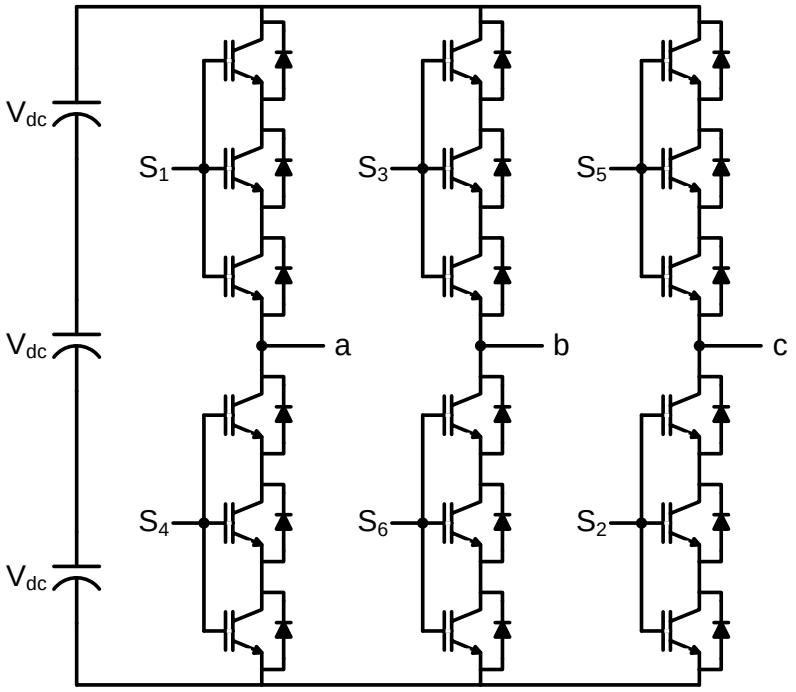
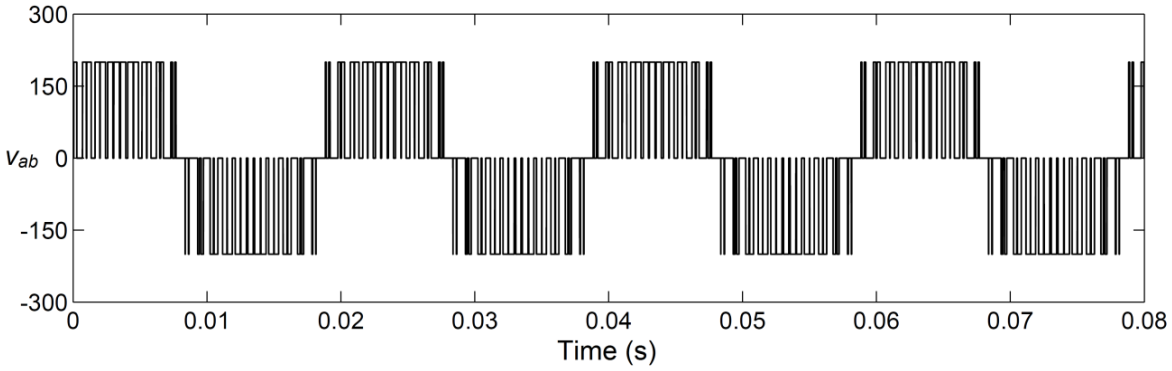


Fig. 1.7: Two-level high-power VSI.

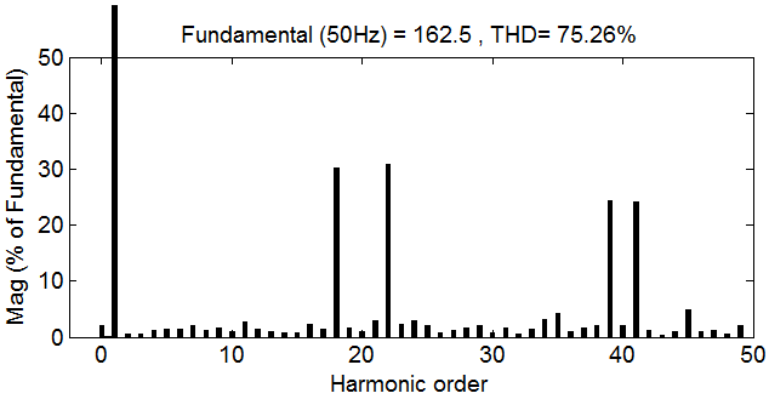
The output voltage of VSI with sinusoidal pulse width modulation (SPWM) method is shown in Fig. 1.8(a). The output voltage is quasi-square wave with a total harmonic distortion (THD) of 75.26% as shown in Fig. 1.8(b). However, the direct use of VSI for the purpose of high-power applications is impractical. This is because, the high harmonic content in the output voltage and increased number of switches in each leg of the inverter structure [34, 35].

In order to reduce the THD in the output voltage and improve the voltage waveform of the basic two-level VSI, large harmonic filters are necessary. In spite of using filters, several solutions are addressed in the literature [34, 35]. Among them, multilevel inverters (MLIs) are the most

popular. These MLI configurations deliver good THD performance and they are directly adapted for high-power medium-voltage applications with the available ratings of the semiconductor devices. Operating principle, merits and demerits of MLIs are explained below.



(a) Line-voltage (V)



(b) Harmonic spectrum

Fig. 1.8: Performance of two-level VSI.

1.5 Multilevel inverters (MLIs)

Multilevel inverters (MLIs) have become increasingly popular in recent years [34, 36-40]. It uses the concept of aggregating multiple small voltage levels to perform power conversion at an appropriate high-voltage level. The principle behind multilevel voltage generation and advantages offered by MLIs are explained here under.

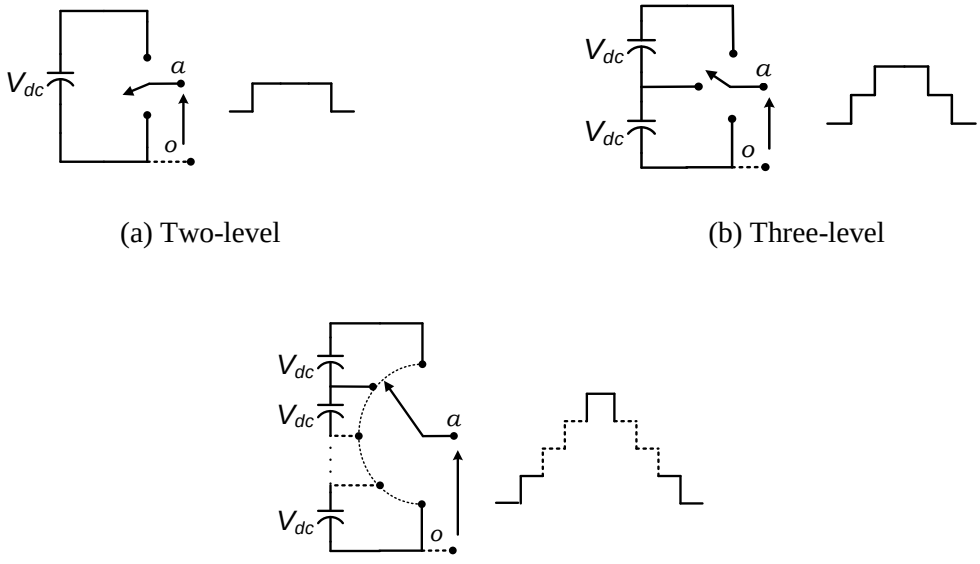
MLIs use several power semiconductor switches and dc voltage sources (or capacitors) to generate a stepped output voltage waveform. The switching action of these devices allow the addition of dc source voltages, and generate higher and different voltage levels in the output voltage without necessity of increasing the rating of power semiconductor devices. The fundamental operating principle of MLI to generate multiple levels in output voltage is shown in Fig. 1.9.

Fig. 1.9 shows the operation of a MLI by considering one phase leg. The switching action of power semiconductor devices is denoted by an ideal switch with multiple ports. By operating

an ideal switch, the structure of Fig. 1.9(a) produces two-levels in the output voltage, i.e., V_{dc} or zero level. In the same way, Fig. 1.9(b) generates three-levels in output voltage and Fig. 1.9(c) gives the output voltage with multiple levels. Consider, *m* is the number of levels in the output phase-voltage with respect to the negative terminal of the inverter, then the generated number of levels in the line-voltage is (2*m*–1). Benefits of MLIs are less THD, low *dv/dt* in the output voltage, low switching losses, good electromagnetic compatibility (EMC), and operate with high-voltage levels [37]. MLIs are considered today as a very attractive solution for high-power medium-voltage applications, because of the following reasons [34, 36-40]:

- Produce output voltages with matured medium-power semiconductor technology with low distortion and low dv/dt.
- Draw input current with very low distortion.
- Can operate with a lower switching frequency.
- Fault tolerant, less prone to failure and their cost is relatively low.
- Generate smaller common-mode (CM) voltage, thus reducing the stress in the motor bearings. In addition, using sophisticated modulation methods, CM voltages can be eliminated.

Owing to these reasons, MLIs are very attractive solutions for medium-voltage and high-power applications. In this connection, the next section describes an overview of classical topologies of MLIs.



(a) Two-level

(b) Three-level

(c) Multilevel

Fig. 1.9: Multilevel voltage generation.

1.5.1 Classical topologies of MLIs

There are three benchmark MLI configurations presented in the literature [34-39]. They are: diode clamped (DCMLI), flying capacitor (FCMLI) and cascade H-bridge (CHB). These three configurations are considered as classical/conventional MLIs and are highly integrated with many industrial applications since from last two decades [34, 35, 37, 38]. These MLIs are extensively recognized by both academia and industry, and these are motivation to investigate new MLI topologies. The structure of these configurations, principle of operation, features, modulation techniques, applications and other information is well described in [34-39] and a brief explanation is presented below.

1.5.1.1 Diode clamped multilevel inverter (DCMLI)

The diode clamped multilevel inverter (DCMLI) is described in [41] and it is considered as the first practically implemented MLI. This structure involves clamping diodes and multiple non-isolated dc sources for obtaining multilevel ac output voltage [41, 42]. This MLI is developed for generating both even and odd number of levels in the output voltage. If DCMLI produce odd levels in output phase-voltage, then it is normally named as neutral-point clamped (NPC) MLI. A three, four or five-level DCMLI are widely used in various industrial applications such as medium-voltage drives and renewable energy [34, 38, 41, 42]. The structure of five-level DCMLI topology is shown Fig. 1.10 [43]. Even though this configuration can be extended to higher number of levels, but they are seldom used due to unequal distribution of power losses in the switching devices [34].

The main drawback of DCMLI is unequal loss distribution which further leads to uneven distribution of junction temperature and imparts limitations on maximum power rating, output current, and switching frequency of the inverter [38, 44]. This unequal loss distribution can be substantially improved by replacing the clamping diodes with active switches. These active switches, forces the current to flow through upper or lower clamping path. This can be used to control the distribution of power loss and overcome the limitations of DCMLI, by substantially enabling the inverter for high power rating. These additional devices are called as active neutral clamping switches and shown in Fig. 1.11**.** Thus, this inverter configuration is named as active neutral point clamped (ANPC) or active diode-clamped multilevel inverter (ADCMLI) [44]. However, the advantages with ANPC come at the expense of more complex circuit and the need to control the additional switching devices.

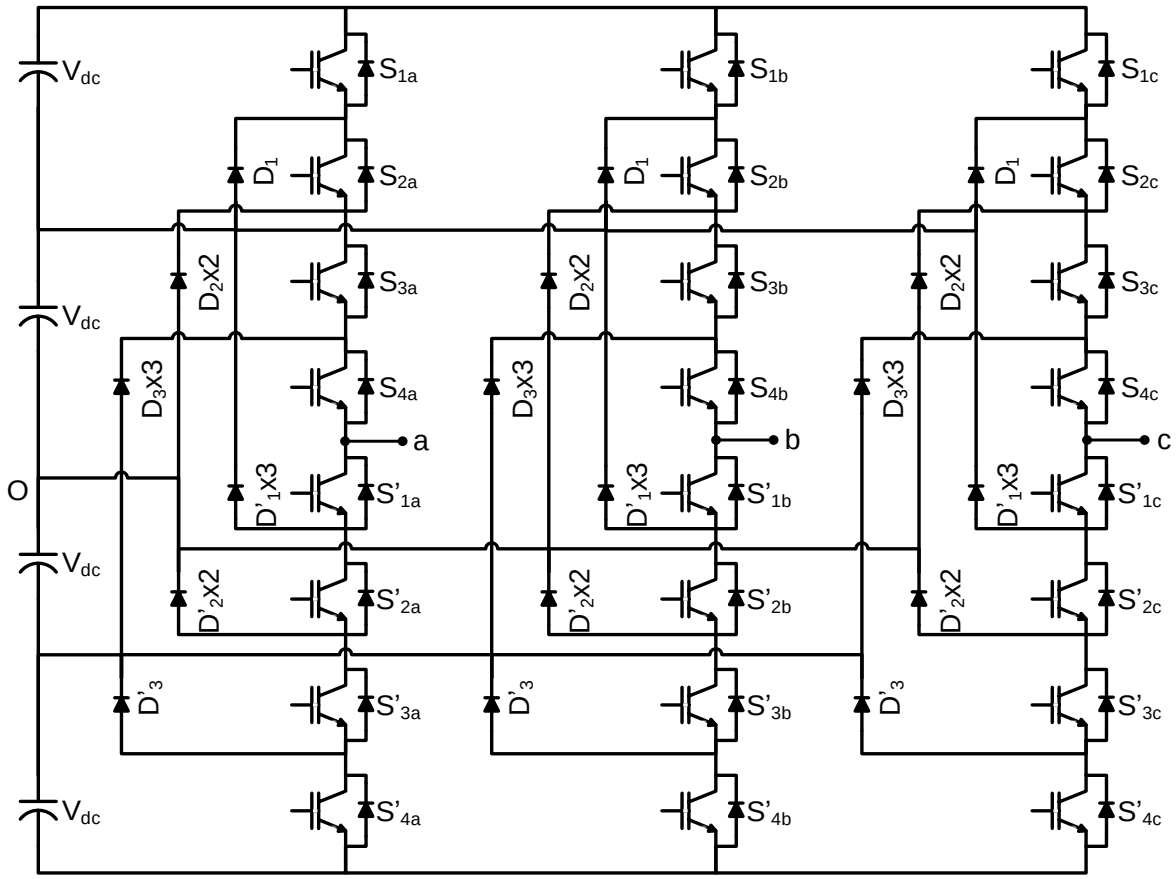


Fig. 1.10: A three-phase five-level DCMLI.

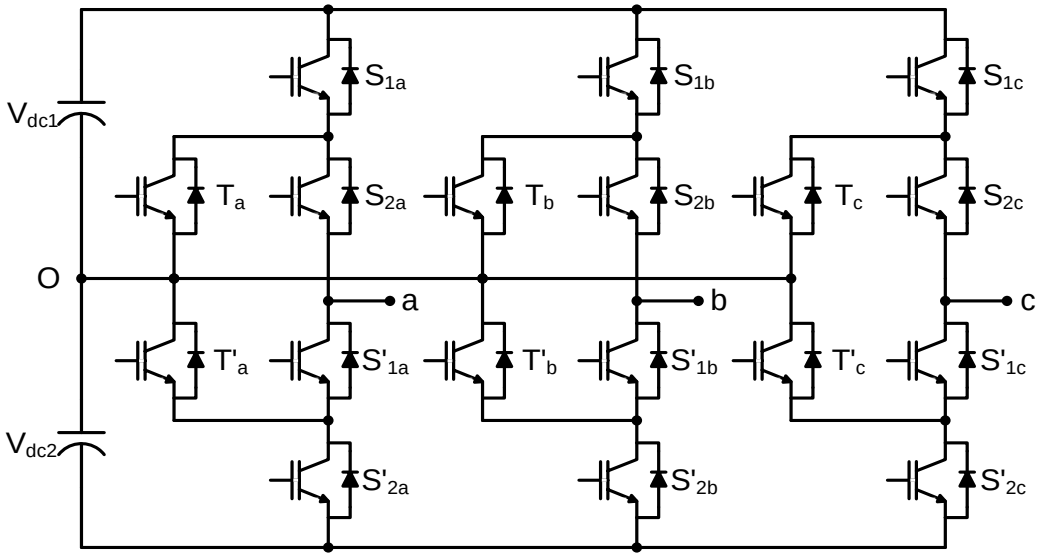


Fig. 1.11: A three-phase three-level active DCMLI.

1.5.1.2 Flying capacitor multilevel inverter (FCMLI):

Among the classical MLI configurations, flying capacitor MLI is a distinctive topology. This MLI includes a series connection of capacitor switching cells [36, 45, 46]. The structure of the five-level FCMLI is represented in Fig. 1.12.

The structural benefits of this topology are absence of clamping diodes. A natural balance of capacitor voltages and even distribution of switching losses can be obtained with the presence

of switching redundancies [36, 45-48]. Merits and demerits of FCMLI topology are summarized below:

Advantages:

- Large number of capacitors provide extra ride through capabilities during power outage [36].
- Modular and scalable topological structure.
- The switching state redundancy provides a great flexibility for the design of switching pattern for natural balancing of capacitor voltages [47, 48].
- Reconfiguration of circuit is possible during fault or under-rated conditions [49].

Disadvantages:

- At start-up, the capacitors have to be pre-charged to their nominal value [34, 37].
- The number of clamping capacitors increases with increase in number of levels phase-voltage and becomes excessive large at higher levels making the topology more complex, bulky and expensive [40].

The above disadvantages make this inverter limited to medium-voltage, high-power applications. However, FCMLI have found particularly viable for high bandwidth high switching frequency applications such as medium-voltage traction drives [36].

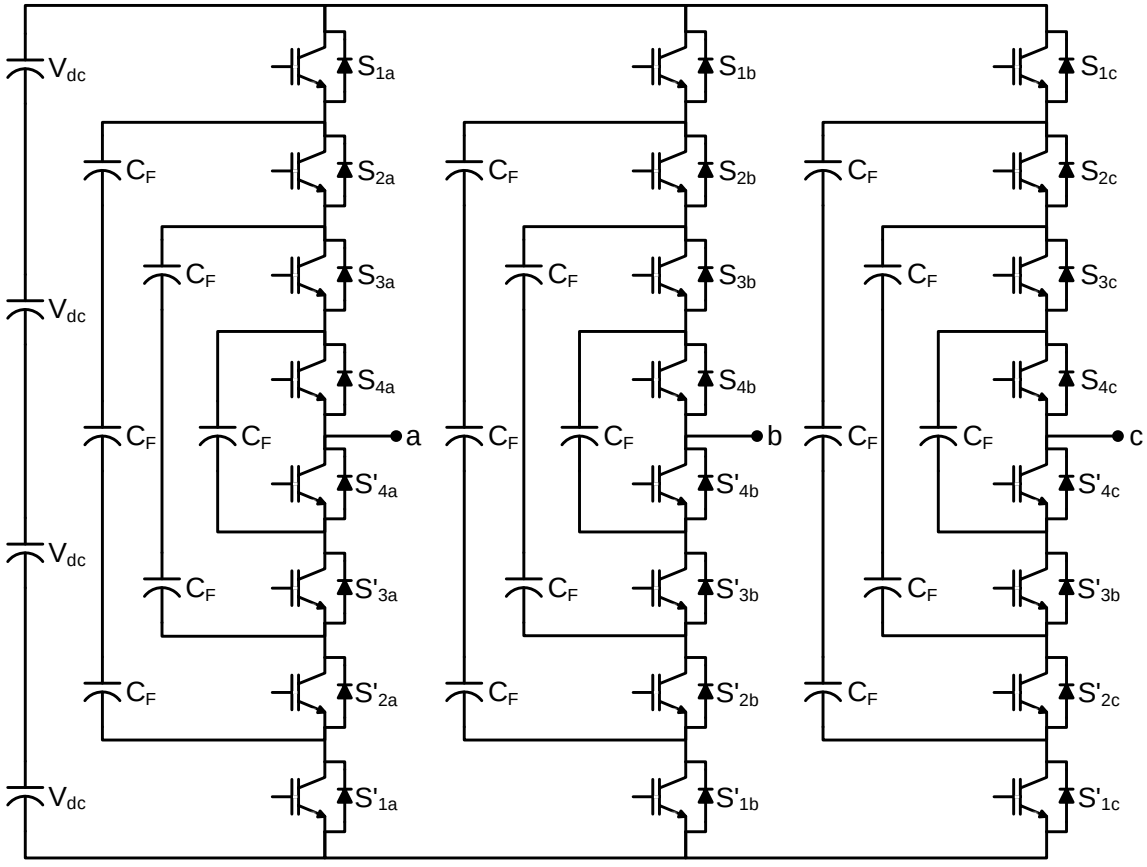


Fig. 1.12: A three-phase five-level FCMLI.

1.5.1.3 Cascaded H-bridge multilevel inverter (CHB MLI)

CHB MLI designed first in 1988, matured during 1990s and became popular after 1997 [50, 51]. CHB MLI is designed by cascading several H-bridge modules in each phase. This give the flexibility to construct the topology for high levels, and generates high-voltages by combining the outputs of each cascaded H-bridge module. Using n number of H-bridge modules per phase, the number of levels (m) in the output phase-voltage is $m = (2n+1)$. Fig. 1.13 presents the structure of a five-level CHB MLI in star connection. CHB can be adapted directly for high or medium-voltage power conversion applications without the use of line-frequency transformer and its performance motivates toward the design of new generation MLIs [52]. Topological advantages and disadvantages of CHB MLI are given below [38, 52-54].

Advantages:

- They can generate high or medium-voltage and power levels with the available medium-voltage rating semiconductor switches.
- Modular in structure, easily scalable.
- Due to the presence of switching redundancies, natural voltage balancing and even power distribution among H-bridges is possible. Further, all the switching devices have equal ratings [55].
- When compared to DCMLI and FCMLI, CHB doesn't need any extra clamping diodes and clamping capacitors.
- A direct connection to the system is possible by eliminating the line-frequency transformer. This is particularly advantageous, as the existence of the transformer makes the inverter heavy and bulky [56], and also induces a dc magnetic flux deviation during line-to-ground faults [57].
- Switching redundancies of CHB helps in reconfiguration of circuit during under-rated or fault conditions [53].
- Most suitable for applications such as photovoltaic energy conversion, BESS, HVDC, FACTS [38, 51, 52, 54, 58-61].

Disadvantages:

- Requires isolated dc voltage sources for power conversion.
- Requires complex phase-shifting transformer arrangement for real power transfer applications such as motor drives.

In CHB MLI, if the unequal dc sources are connected to each H-bridge module, then CHB can able to generate more number of levels in output voltage [54]. CHB with unequal dc voltages sources is called as asymmetrical CHB MLI. The ratio of unequal dc sources connected to MLIs can be in geometric progression (GP) and arithmetic progression (AP). In order to get significant

decrease in switch count, geometric progression based dc sources are typically used. Normally use of geometric progression ratio based dc sources are binary (2^0: 2^1: 2^2: 2^3…) and trinary (3^0: 3^1: 3^2: 3^3…) progression based voltage ratios.

The significant benefit with asymmetrical CHB MLI is to obtain more number of levels with less number of dc sources and switches. The will reduce the gate circuit requirements, consequently size and cost of the inverter is reduced as compared to its counter symmetrical MLI for generating same number of output voltage levels. By applying binary and trinary ratios based of dc voltage sources, the CHB MLI shown in Fig. 1.13 can generate seven and nine output voltage levels respectively. This will decrease the switch count to 50% for nine-level and 33.33% for seven-level as compared to symmetric CHB MLI for circuit shown in Fig. 1.13. On the other hand, in asymmetric CHB MLI, switching redundancies are reduced and leads to unequal use of dc sources.

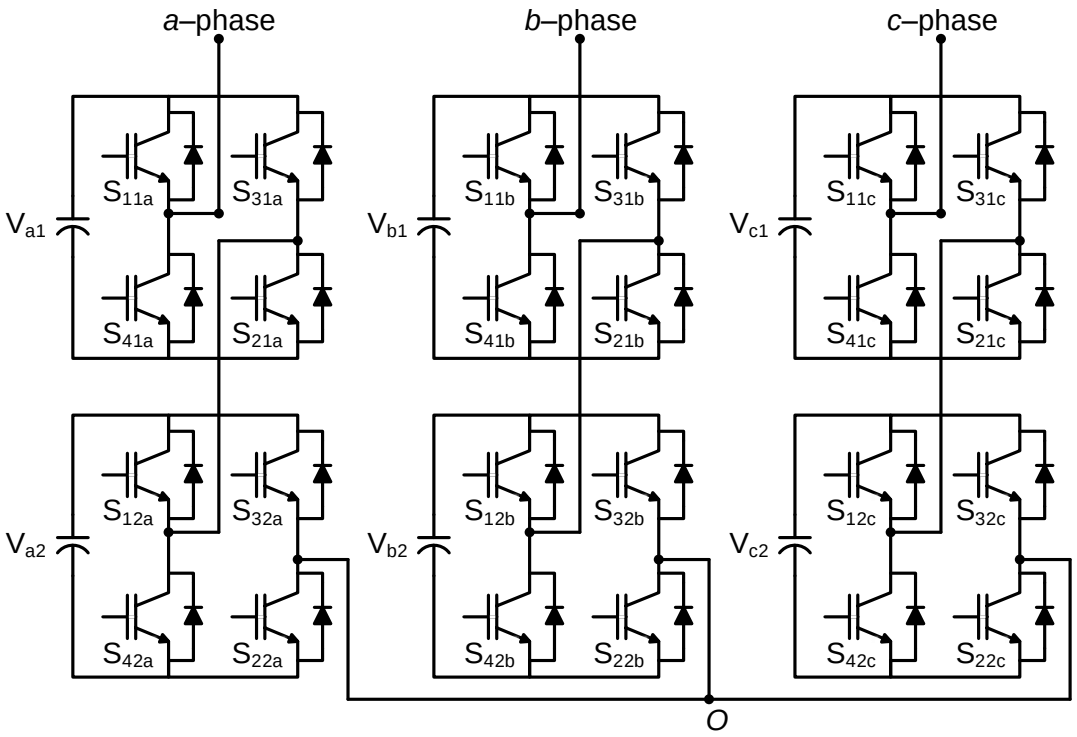


Fig. 1.13: A three-phase five-level CHB MLI.

Cascaded family of inverters are also characterized by cascade connection of modular chopper cells to form each cluster/phase-leg/arm. Cascaded MLI with H-bridge cells is known as cascade H-bridge (CHB) MLI. On the other hand, cascaded MLI composed with bi-directional chopper cells are known as modular multilevel inverters (MMI). However, the common concepts hidden in the family members are “modular” structure and “cascade” connection. These concepts allow power electronics engineers to use the common term “modular multilevel cascade inverter (MMCI)” as a family name [52].

1.5.2 Comparison of classical MLI topologies

Table 1.1 shows the comparison of per-phase components requirement among CHB, DCMLI, and FCMLI for obtaining *m* levels in phase-voltage.

From the above discussions on the classical MLIs and Table 1.1, the following remarks can be summarised:

- The requirement of large number of power components and voltage unbalance problem at higher levels, limits DCMLI for low to medium-power applications [62, 63].
- FCMLI is a modular structure with natural voltage balancing ability [48], but its application in realization of AFC and CPD is limited due the requirement of large number of capacitors. Further, the capacitors need to be pre-charged at start-up [38].
- Least component requirement, modular structure, fault tolerance ability and absence of pre-charging requirements makes CHB best suited for high-voltage, medium-power grid connected applications (13.8 kV, 30 MVA) [54].
- Similar to DCMLI and FCMLI, a large number of semiconductor device are required to develop a CHB MLI with high number of levels. This will increase size, cost, and control complexity of the MLI.

Hence, the increased device count in classical MLIs has led to the design of new area of power converters termed as reduced switch count multilevel inverters (RSC-MLI) [64, 65]. As the name suggests, a significant reduction in device count is obtained as compared to conventional MLIs. From the past decade, several researchers are developing new inverter configurations with substantial reduction in device count, cost and easy in control. The literature survey on RSC-MLIs is discussed in Chapter 2.

Table 1.1: Comparison of per phase-leg component requirement of classical MLI topologies.

Power component	**Inverter topology**		
	DCMLI	**FCMLI**	**CHB**
Main switching devices	$2(m-1)$	$2(m-1)$	$2(m-1)$
Anti-parallel diodes	$2(m-1)$	$2(m-1)$	$2(m-1)$
Clamping diodes	$(m-1)(m-2)$	0	0
DC bus capacitors	$(m-1)$	$(m-1)$	$\frac{(m-1)}{2}$
Flying capacitors	0	$\frac{(m-1)(m-2)}{2}$	0

1.6 Literature survey on control of grid connected systems

This research work focuses on control of three-phase single-stage grid-connected PV system. In this system, a dc to ac inverter has been connected between the PV system and the utility grid. In general, a three-phase VSI with a fast dynamic response is adapted in the grid-connected applications. The fundamental design objectives are improve the closed-loop controller performance to accomplish a fast transient response and simultaneously minimize the steady-state tracking error. These objectives must be balanced with assuring that the system is robust and stable in the presence of uncertainties, system parameter variations and measurement noises.

Three dominant controllers have been extensively studied over the last two decades. They are hysteresis controller, linear PI controller and predictive dead-beat controller [66-68]. The benefits of hysteresis controller is its simplicity, robustness and fast dynamic response. There are numerous active research works carried out to increase the performance of hysteresis current control scheme [69-71]. Nevertheless, the presence of variable switching frequency components in the output voltage of the inverter may cause unexpected resonance with other passive elements connected to the grid [67]. In many research investigations, PI controllers are adapted to regulate the ac side currents [66, 67, 72-77]. In these controllers, the dc link voltage is regulated by an outer voltage control loop, in which the input to the PI controller is dc voltage error and it generate references for the ac current in synchronous (*dq*) frame or stationary (*abc*) reference frames. PI current controllers assure that a clean in-phase ac current is injected into the grid [78]. Since PI controller has been extensively adapted in the grid-interfaced PV systems, this controller will be basic for any research study to compare with the advanced controllers. The other control method which has been adapted to the grid-connected system is the model predictive controller. The benefits of predictive dead-beat controller are fast dynamic response and accurate performance. Nevertheless, this control scheme has a model based regulator and hence it is quite sensitive to uncertainties, inaccuracies, parameter changes and delays [67, 72, 79, 80].

In order to obtain a satisfactory power transfer which is indeed dependent on PWM switching control, the required gating signals for the inverter from reference signal are obtained by conventional controllers [77, 81, 82]. The employed PI controllers in [77, 81] are linear and their number increases with increase in number of dc sources in inverter, hence their tuning is a challenging task to achieve satisfactory operation. Two other control schemes, namely plug-in repetitive control and model predictive control are employed in [83, 84] for reducing the circulating currents and balancing capacitor voltages in modular multilevel converters (MMC) system respectively. Even though the controllers in [77, 81-84], achieved closed-loop control, they used either linear controllers or the system is limited to islanding operation with linear

controllers. None of them have explored the closed-loop control of MLI with a nonlinear controller for feeding set-point powers into the grid.

The MLI based grid connected distributed generation system is a highly nonlinear as it involves more switching actions and the circuit seen from the grid side will be different at different output voltage levels. Since the structure of the converter is changing at every level, it is a cumbersome process to tune the PI controllers to achieve successful, decoupled and set-point real and reactive powers. Moreover, the PI controller performance degrades if the operating point and/or the disturbance is different from that for which the controllers have been tuned. In addition, the PI controllers do not have disturbance rejection property as well as their performance is prone to parameter changes and prevailing model oscillations.

To alleviate the short comings of PI controller, the nonlinear system has to be linearized and a suitable control philosophy has to be developed. One of such approach is sliding mode control (SMC) [85, 86]. SMC is suitable for linear and nonlinear systems, offer good robustness for systems like grid connected MLIs. It slides over the surface as defined and is asymptotically stable. The switching is independent of system operating points and other circuit parameters. One of such controller adapted in [87], however the MLI considered is a single source with relatively large number of switches. Moreover, it has considered "sign" based control, a hard switching control, which can result in chattering performance, hence the introduction of unmodelled frequency components into the output. Even though the literature in [77, 81-87] considered the closed-loop control, it is limited either to conventional MLI topologies or two-level inverters. The adaption of SMC for grid connected PV system had recently discussed in [88, 89]. The closed-loop control of RSC based MLIs using nonlinear control for grid connected operation to deliver set-point real and reactive powers is not explored in the literature. Therefore, an attempt is made in this thesis.

1.7 Literature survey on control of PV systems

Solar energy is the most abundant and the cleanest renewable energy source accessible in the world, technically feasible to use for numerous applications, such as feeding electricity to commercial, residential or industrial utilizations [12]. It has become a crucial part of present day energy systems due to the decrease in the PV module costs and the growth in design of the power converters from the point of view of reliability and cost [90]. Power electronic technology has grown into a crucial element in distributed generation (DG) and in promoting the integration of renewable energy sources into the grid [4]. Photovoltaic converters are broadly applied to convert the dc voltage generated by the PV source to ac voltage. Two-stage power converters are presently the popular approach to handle the dc voltage generated by the PV system [90]. This

structure consists of a dc to dc converter, which attains maximum power point tracking (MPPT) in association with maximum power point algorithm and a dc to ac inversion stage to supply power to the grid or local loads. The conventional MPPT control algorithms such as Perturb and Observe (P&O), constant voltage (CV) algorithms, incremental conductance (INC) and modified versions of these have been reported in [5, 91-96]. However, the two-stage power conversion approach discourages in terms of reliability, overall efficiency and increased cost [90, 97]. Therefore, from the perception of reliability and efficiency, single-stage grid interfaced PV structures are preferred choice in recent times. These single-stage approaches require a PV source and a dc to ac inverter with MPPT scheme. They have been proposed to control the active power and reactive power by adapting conventional PI linear control techniques [76, 97-104].

A three-phase two-stage power converter system with a nonlinear back-stepping control scheme for feeding active and reactive power into the grid is discussed in [28]. The scheme established in [28] is proposed for control of dc link voltage assuring MPPT as a first stage, and control of three-phase dc to ac converter to regulate the active and reactive power supplied to the grid as a next stage.

In [105-108], discusses two-stage single-phase grid-interfaced PV system under the control of back-stepping controller for power factor correction and maximum power tracking. In these schemes, a dc to dc boost conversion system is used to trace the maximum power from the PV source and to regulate the input voltage of the dc to ac converter to feed the active power with unity power factor. The main difference among these approaches is the way in which the input voltage to the inverter is controlled. In [106, 108], a conventional PI controller is adapted to control the output voltage of the dc to dc boost conversion system. In [109], a three-phase two-stage system with SMC is proposed. In this, the first stage is a dc to dc conversion with a coupled inductor for the purpose of voltage boosting. It uses the adaptive sliding surface for maximum power tracking. A dc to ac three-phase inverter for power factor correction makes the second stage.

The supply of maximum power from PV sources into the grid through conventional MLI topologies is carried out in [81, 110] with appreciable control objectives. For obtaining maximum powers from nonlinear PV sources, conventional PI controllers are adapted in [81, 110]. In general, the PI controller is linear controller and its performance is sensitive to operating point changes and/or to other disturbances. This is because the gains of PI controller are designed for a specific operating point only. If any changes in operating points or any short time uncertainties occur in the system, then the PI controller detunes and may result overshoots/undershoots with delayed response. Especially in high power applications, these overshoots in the response causes damage to switches of MLI. So that, the use of fixed gain PI controller is a cumbersome process

for extraction of maximum power from non-linear PV sources during irradiance varying conditions. Further, the tuning process of multiple PI controllers becomes a challenging task in the case of individual maximum power extraction of each PV sources connected to each H-bridge of CHB MLI [77, 81, 82, 110-113]. To overcome the drawback of the PI controller, it is necessary to linearize the non-linear PV source and a suitable controller needed to be implemented for extraction of maximum PV power. One of such controller is SMC, which is suitable for both linear and non-linear systems. The SMC is a robust control technique that deals with model uncertainties. SMC may offer better dynamic performance than PI controller and results in undershoots/overshoots free response for the PV based grid connected systems.

The other controllers such as fuzzy-logic control [114] and back-stepping control [115] are used for maximum power extraction. However, these controllers are adapted for two-level inverter based dual stage systems and extending to higher level topologies is a tedious task. The power control of grid connected two-level converter under system parameter variations using SMC is reported in [85, 86]. However, the dynamic performance of both PI controller and SMC for maximum power generation from single-stage asymmetric PV sources under variable irradiance conditions has not yet reported.

In literature, the linearization method is adapted to PV system [24]. The linearization technique converts the nonlinear system into a partial or fully linear equivalent. After linearizing the state-space equations, the control scheme can be developed for either tracing purpose or stability [24]. A multi-stage three-phase two-level inverter based on linearization procedure to supply maximum power to the grid from the PV array is described in [116]. Nevertheless, the linearization method could cause of stability problems during the variations in parameters of the system, or changes in the operating conditions. Two-stage PV systems under nonlinear control schemes have shown good performance. However, two-stage power conversion system decreases the reliability and overall energy efficiency of the PV system [90]. To date, only a few works have been addressed for single-stage two-level inverters under nonlinear control schemes. In [16], a partial feedback linearization scheme for a three-phase system is discussed by considering uncertainties of the system model. An input-output feedback linearization scheme for a three-phase inverter in *dq*0 frame of reference is discussed in [27]. All these research works are based on feedback linearization and shown appreciable performance for obtaining the desired results. But, this feedback linearization scheme is susceptible to the system parameters variations [28].

In this thesis, a nonlinear robust SMC control scheme based on Lyapunov stability is proposed for a single-stage three-phase RSC-MLI based grid-connected photovoltaic system. In order to address the issues of uncertainty and to add robustness to the control algorithm, SMC technique is incorporated in the feedback linearized control. The SMC controller is established to

attain maximum power point operation and set-point power control under wide variations of irradiance conditions without the requirement of a dc to dc conversion stage. The control structure is established in synchronous reference frame to convert time-varying measured quantities to constant values [117]. Furthermore, the perturb and observe MPPT algorithm is employed in this research, because of its robustness and simplicity in tracking the desired PV voltage for a wide range of irradiance conditions [5, 93]. Moreover, a Lyapunov stability analysis is presented to verify the stability of the proposed RSC-MLI based grid connected closed-loop control system. The effectiveness and robustness of the proposed nonlinear SMC against the conventional PI controller is verified in MATLAB/Simulink and OPAL-RT based real-time based test beds.

1.8 Scope of work and Author's contributions

The major contributions of this thesis are summarized below:

- The advent of matured medium-voltage self-commutating power electronic devices has increased the prominence of MLIs for medium-voltage high-power grid connected applications. Despite of this, the benchmark topologies of MLIs suffer with increased switch count and control complexity at higher levels. Hence the demand for reducing the size and switch count of MLI, has led to the development of RSC-MLIs. In last decade, a wide number of RSC-MLIs topologies are reported in the literature. Therefore, this thesis investigate the suitability of RSC-MLIs topologies in grid connected applications.
- This thesis, discuss the literature on various RSC-MLI topologies and classify them on their topological arrangement, switching operation, features and applications. Further, a comprehensive comparison in terms of their device count, utilization of dc sources, device blocking voltages and power distribution is presented. From the comparative study, it is observed that multilevel dc link (MLDCL) and switched series and parallel sources (SSPS) are most suitable for grid connected PV applications.
- A critical comparison is made among 11-level asymmetric CHB, MLDCL and SSPS by considering various factors. Further, to quantify the effective use dc sources in MLI, a parameter known as utilization factor (*UF*) of input dc sources is defined in this thesis. Due to the series/parallel connection of dc voltage sources, utilization factor for SSPS MLI is high when compared CHB, which is advantageous in grid connected PV applications. MLDCL is highly modular and requires less component as compared to SSPS. Owing to these reasons, SSPS and MLDCL are best alternative to grid connected applications and therefore, they are further evaluated in the thesis.

- In this connection, this work proposes an 11-level asymmetric three-phase SSPS RSC-MLI based grid connected closed-loop system with the objective of active and reactive power control using non-linear SMC. To achieve this, a nonlinear mathematical model is established between inverter and grid. Feedback linearization is used to transform the nonlinear system into a linear. The feedback linearization is sensitive to parameter variations, uncertainties and exogenous inputs. To overcome these limitations, this work is incorporated the SMC in the feedback linearized controller. The superior performance of the proposed system under the control of SMC is verified and compared with conventional PI controller. These comparative performances are verified through MATLAB/Simulink and the results are validated in OPAL-RT based real-time hardware-in-loop environment at different operating conditions and system parameter changes.
- Further, this work proposes a 11-level three-phase asymmetric MLDCL RSC-MLI based single-stage PV system for integration on to a 11 kV grid. In MLDCL RSC-MLI, asymmetric PV sources with 1: 2: 2 ratio is considered for generating more levels in the output voltage with minimum switch count. The structures of MLDCL MLI allow even power distribution between equal rated input sources. Therefore, a single maximum power extraction control method is proposed for multiple equal rated PV sources thereby reducing the control complexity.
- In this work, the conventional PI controller is replaced with non-linear SMC to extract maximum powers from PV sources in MLDCL RSC-MLI under wide variations of irradiation levels. A non-linear mathematical model of single-stage PV system is linearized using an effective feedback linearization scheme. Further, a common SMC is incorporated with feedback linearization scheme to extract the maximum PV power from equal rated PV sources. The total maximum PV power generated from all the PV sources is injected to the grid by controlling the inverter using two-loop PI controller. At various irradiance conditions, the superior performance of SMC against conventional PI controller for extraction of maximum PV power is analysed in MATLAB/Simulink and further validated in OPAL-RT 4500 hardware-in-loop simulator.

1.9 Organization of thesis

Apart from this chapter, this thesis contains five more chapters and the work included in each of these chapters is briefly outlined as follows:

CHAPTER 2 presents the detailed literature review and classification of reduced switch count multilevel inverter topologies.

CHAPTER 3 describes the structure and operation of the SSPS and MLDCL RSC-MLIs. Utilisation factor of dc sources of various MLI is introduced. Comparative analysis among CHB, SSPS and MLDCL RSC-MLIs in terms various factors are discussed in this chapter. This sets the motivation towards the selection of superior topology for grid-connected applications.

CHAPTER 4 presents various conventional controllers used for power control of grid connected inverter system along with their merits and demerits. Adaption of sliding mode controller for decoupled active power and reactive power control in MLI based grid connected system is introduced. Before adaption of SMC for proposed MLI based grid system, linearization scheme is discussed for proposed non-linear system. Validation of SMC against PI controller for controlling proposed system is discussed.

In **CHAPTER 5,** the PV power extraction using conventional controller and its demerits are addressed. PV power extraction from asymmetric PV sources of MLDCL RSC-MLI using SMC and PV power injection into grid using two-loop PI control scheme is discussed. The superior performance of SMC over PI for PV power extraction is verified. MATLAB and OPAL-RT 4500 based Hardwar-in-loop (HIL) results analysis concludes this chapter.

The **CHAPTER 6** highlights the main conclusions and significant contribution of the thesis and states the scope for further research in this area.

CHAPTER 2: LITERATURE SURVEY ON RSC-MLIs

This chapter presents literature survey on various reduced switch count multilevel inverter (RSC-MLI) topologies. Based on this, superior RSC-MLIs are identified for grid-connected application.

2.1 Introduction

Nowadays, MLIs are considered as a leading-edge technology for medium-voltage high-power applications. Conventional configurations i.e., DCMLI, CHB and FCMLI have their own advantages and drawbacks and are well fit for a particular application. Nevertheless, their device count considerably increases with increase in the number of levels of the output voltage. Increase in number of switch count includes additional gate drivers, isolation circuits, protection circuits and their corresponding heat-sinks. Furthermore, increment in switch count leads to additional increase in computations on the controller. Therefore, a considerable increase in size and complexity of conventional MLIs is present at higher levels. This leads to increase in cost of the inverter which discourages on its practical execution and market penetration [34, 35, 62, 63]. In order to overcome the above drawbacks, a new family of MLIs called as reduced switch count multilevel inverters (RSC-MLI) are recently introduced in literature. The main aim of these RSC-MLIs is to decrease the size, cost and complexity as compared to conventional MLIs. From the past decade, numerous RSC-MLI configurations are designed [64, 65]. Some of the recent RSC-MLI topologies are presented in [118-130] and [131-134].This chapter address a brief description of these topologies and studied the influence of reduced switch count on their structure along with operational features.

2.2 Factors motivated in designing new RSC-MLI configurations

In past few years, due to a vast research, numerous RSC-MLIs structures are proposed in literature. Investigators are frequently studied several performance features in suggesting an innovative RSC-MLI configuration and the main features are listed below.

- **Reduction in number of devices**: This feature specifies the decrease in number of switches, capacitors, diodes and additional supplementary components in comparison with conventional MLIs.
- **Blocking voltage of device**: Unlike in conventional MLIs, the blocking voltages of all/some devices in RSC-MLIs can be unequal. This provisions the necessity of devices with unequal voltage ratings.
- **Modularity in structure**: The arrangement of topology can be modular by connecting several basic modules in cascade or in series. An RSC-MLI with a feature of modularity in its structure can easily extended to generate higher voltage levels.

- **Presence of bi-directional switches**: In some inverter structures, bi-directional switches are required, which have a bi-directional current conducting and bi-directional voltage blocking ability.
- **Minimum switching and conduction losses**: Designing of a new RSC-MLI configuration in such a way that it can generate the desired number of output voltage levels by operating the switches with reduced switching and conduction losses.
- **Equal power sharing**: The RSC-MLI can able to generate desired phase-voltage by allocating equal power across all basic modules or H-bridges. This feature provides the facility of the charge balance among input capacitor voltages.
- **Application domain**: In this, a critical study is made on the newly designed topologies in concluding their best adaptable fields such as renewable [119, 120, 123, 124] and fuel cell energy conversion [119, 120], HVDC, FACTS, BESS, CPD, ASD, electric vehicles [118], motor drives [122] and user electronics.

2.3 Organization of RSC-MLI configurations

The RSC-MLI configurations can be categorized into several groups based on the features described above. The probable classification of these RSC-MLIs is given below.

2.3.1 Based on the physical structure or configuration arrangement

In view of the physical arrangement of semiconductor devices, dc sources and/or capacitors and additional auxiliary devices such as diodes, the following categorisations can be possible for the construction of RSC-MLI topologies.

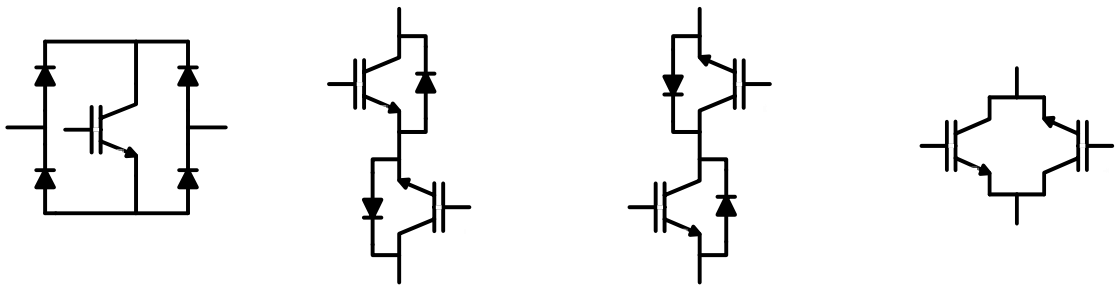
***(a) Modular topologies*:** The topological arrangement of most of the RSC-MLIs is designed by including multiple similar modules connected in cascade or series or parallel. These MLIs can easily be extended to higher number of levels and are termed as modular configurations. Each basic module unit of these MLIs generate a fixed number of output voltage levels.

***(b) Physical arrangement*:** The connection of the switches and dc voltage sources of RSC-MLIs include several units connected in a particular physical arrangement. This physical pattern may be of stair-case, ladder structured, U-shaped or column. They may also have cascade, series, and parallel structure or sometimes may not have any particular layout.

***(c) Configurations with H-bridge/HSC arrangement*:** Because of modular property of CHB when compared to other conventional MLIs, several RSC-MLIs are designed by including an H-bridge incorporated with several modular/non-modular structures. It is to be observed that the operation of the H-bridge in RSC-MLIs is dedicated for various purposes and may vary with topology. In other way, few RSC-MLIs include hexagon switched cell (HSC) rather than H-bridge module. Presence of HSC allows the inverter to generate output for multiple

switching redundancies. Examples of such topologies are cascaded MLI with HSC [135, 136] and hybrid T-type [137, 138].

***(d) Configurations with bi-directional switches*:** The topological design of few RSC-MLI configurations such as T-type [139-144], cascaded bipolar switched cells (CBSC) [145] require switches which can able to conduct current and block voltage in both directions. However, such type of switches is not available in current market. Hence, discrete semiconductor devices are combined to make a switch with bi-directional current conducting and voltage blocking ability. Fig. 2.1 shows the probable provisions with IGBT switches and diodes to realize a bi-directional switch. Fig. 2.1(a) represent bi-directional switch made with one regulated switch such as IGBT and four diodes. The four diodes are arranged in such a way that they form a bridge rectifier and an IGBT switch is positioned in between the legs of diode bridge rectifier. The formed bi-directional device structure shown in Fig. 2.1(a) needs only one IGBT and one gate driver. However, this structure produces relatively high conduction losses as three devices (two diodes and IGBT) in each conduction path. Moreover the direction of current through the switch cell cannot be controlled. The common emitter and common collector bi-directional switch cell provisions with two diodes and two IGBTs connected in antiparallel are shown in Fig. 2.1(b) and (c) respectively. There are some benefits with these structures when compared to the previous one. In these arrangements, it is possible to individually control the direction of the current.



(a) Diode-bridge (b) Common-emitter (c) Common-collector (d) Reverse-blocking IGBT

Fig. 2.1: Possible arrangement of bi-directional switch.

Furthermore, the conduction losses are also decreased, because only two devices (IGBT and diode) are in each conduction path. One possible drawback of Fig. 2.1(c) is that each IGBT needs a separate gate driver circuit and hence it is costly [145]. On the other hand, in common emitter configuration, the central connection allows both devices to be controlled from common gate driver circuit. Two reverse-blocking (RB) IGBTs in an antiparallel construction as shown in Fig. 2.1(d), can block voltage and current in both directions and provides an appropriate way to make a bi-directional switch. This arrangement offers the transient benefits while switching. The most significant benefit of Fig. 2.1(d) is the decrease

of conduction losses. Nevertheless, the reverse voltage blocking capability is limited as its attained by altering the construction of a normal IGBT.

***(e) Topologies with isolated (or) non isolated dc sources*:** Based on the topological arrangement, the dc voltage sources of RSC-MLIs may be separately connected or non-isolated. The dc link voltages supply to the input of RSC-MLI with separate dc sources can be attained from batteries or photo-voltaic (PV) systems. Similarly, few RSC-MLIs contain non-isolated dc sources or capacitors associated in series/parallel through multiple intermediary nodes [139-143, 146]. In particular, RSC-MLIs, such as nested and three-phase symmetrical configurations include non-isolated dc sources such that a dc link is common to all the three-phases [147-149]. These type of MLIs may be substitute for DCMLI or FCMLI.

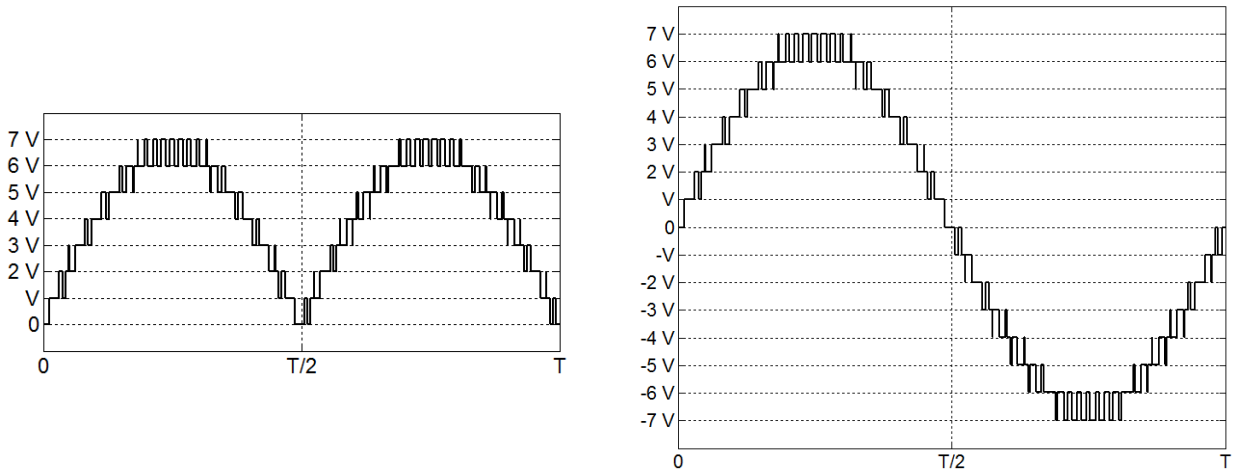
2.3.2 Based on operation and performance

Based on switching operation of RSC-MLI, ratio of dc link voltages of the sources, blocking voltages of the devices, utilization of dc sources, equal or unequal power distribution, the following categorisation can be made.

***(a) Symmetrical and asymmetrical source based RSC-MLIs*:** To achieve more number of output voltage levels, without changing the inverter physical arrangement, asymmetrical topologies are chosen. Asymmetrical RSC-MLI contains unequal magnitude of dc link voltages and achieves the desired number of output voltage levels for additive or subtractive combination of dc source voltages. Hence, RSC-MLI with equal ratio of input dc link voltages is termed as symmetrical topology and the RSC-MLI with unequal ratio of input dc link voltage is termed as asymmetrical topology. Unequal ratio of input dc voltage sources offers an appreciable reduction in number of switches as compared to symmetrical topologies. These voltage ratios can either be in geometric progression (GP) or arithmetic progression (AP). However, voltage ratios in GP produces more voltage levels with extensive reduction in switch count. Most often, GP with common ratio of two (binary) or three (trinary) is preferred. It is to be noted that an asymmetrical configuration with trinary voltage ratios will be realized, only if the inverter configuration can facilitate output for additive and subtractive combinations of dc link voltages. Asymmetrical RSC-MLI configurations reduces size and complexity, but reduces the switching redundancies drastically. This further restricts inverter fault tolerant ability, limits capacitor voltage balancing, increases device blocking voltages and produce non-uniform power distribution among basic units. E-type [150] and square T-type [151] are the examples of unit-based asymmetrical RSC-MLI configurations. The recent asymmetric RSC-MLIs are also introduced in [128, 129, 134, 152].

***(b) Configurations with separate polarity and level generators*:** To achieve the desired number of voltage levels, the arrangement of several RSC-MLIs consist of a separate level and

polarity generators. The level generator includes several switching devices connected to dc sources or capacitors to create a multilevel or staircase unipolar voltage waveform. On the other hand, polarity generator modifies this unipolar multilevel voltage to bipolar using an H-bridge structure. If a level generator produced an unipolar multilevel voltage with *n*-levels, then polarity generator alters this unipolar to bipolar voltage with (2*n*–1) levels. Fig. 2.2 shows the voltage waveforms generated from level and polarity generators. Few of such RSC-MLIs are MLDCL [153], SSPS [154, 155] and RV [146]. Most often, blocking voltage of each device in polarity generator is equal to the total dc link voltage. Therefore, device rating in polarity generator is quite high and operated at fundamental or low switching frequency.



(a) Output of level generator (unipolar) (b) Output of polarity generator (bipolar)

Fig. 2.2: Output voltage of level and polarity generators.

***(c) Topologies with uniform power sharing*:** In few topologies, input dc sources contribute uniform power to the load, commonly known as uniform power distribution or equal charge balance control [156]. Even power distribution is a feature of control aspect only when the topology permits. When the inverter is symmetric, the modulation methods are designed in such a way that the average current passing through each dc source is equal, and hence the average power delivered from each source is equal. For a considered topology, uniform power sharing is possible, if each dc source contributes to generate all the output levels per one or more cycles. For example, if a topology has three symmetric input dc sources V_{dc1}, V_{dc2} and V_{dc3} (V_{dc1} = V_{dc2} = V_{dc3} = V_{dc}), then a natural even power distribution is possible if all the combinations shown in Table 2.1 are permitted by the topology.

Table 2.1: Required switching combinations for even power distribution with three dc sources.

Output voltage level	Required combination of input dc levels
$\pm V_{dc}$	$\pm V_{dc1}$
$\pm V_{dc}$	$\pm V_{dc2}$
$\pm V_{dc}$	$\pm V_{dc3}$
$\pm 2V_{dc}$	$\pm(V_{dc1}+V_{dc2})$
$\pm 2V_{dc}$	$\pm(V_{dc2}+V_{dc3})$
$\pm 2V_{dc}$	$\pm(V_{dc3}+V_{dc1})$
$\pm 3V_{dc}$	$\pm(V_{dc1}+V_{dc2}+V_{dc3})$

***(d) Configurations with equal blocking voltages*:** Reduction in number of switches in RSC-MLIs has changed their topological structure by modifying the connection among dc link voltages, uni-directional and/or bi-directional switches. This construction of the dc link voltages and switching devices influences the rating and voltage stress of the switching devices, equal and unequal blocking voltages appears across the devices. Hence, by considering the blocking voltages of the devices, RSC-MLIs can be categorized into topologies with equal (uniform) and unequal blocking voltages. However, RSC-MLI topologies with uniform device blocking voltages are more preferred because they have a provision to operate with uniform conduction losses. In industrial applications, RSC-MLIs with modular structure, and uniform switch ratings have remarkable prominence. Further, the sum of the device blocking voltages of all the operating devices contribute to the maximum voltage blocking capability of the overall inverter. For example, if an inverter consists of six switches rated at V_{dc} and four switches rated at $2V_{dc}$, then the total voltage blocking capability of the inverter can be calculated as: $(6 \times V_{dc}) + (4 \times 2V_{dc}) = 14V_{dc}$.

Considering the above classification, the reported RSC-MLIs topologies can be categorized as shown in Table 2.2. It is to be noted that, this categorization is carried out by considering either the motivating factor behind the development of the topology or its key contributing features.

Table 2.2: Classification of RSC-MLI topologies.

Generalized RSC-MLIs: These topologies can easily be extended to higher levels and can be generalized for any number of odd level.

- With separate level and polarity generators
  - Multilevel dc-link (MLDCL) [153, 157]
  - Switched series parallel sources (SSPS) [154, 155]
  - Reverse voltage (RV) [146, 158]
  - Series connected switched sources (SCSS) [159, 160]
  - Multilevel module (MLM) [161]
- T-Type topologies
  - T-type [139, 141, 144, 162, 163] and [127, 164]
  - Cascaded T-type [143]
  - Three-leg T-type [165, 166]
- Hexagon switched cell (HSC) based topologies
  - Hybrid T-type Topologies [137, 138] (Topology-I and II)
  - Extension of HSC to higher levels [137, 138]
- Topologies with ladder based structures
  - Cascaded bi-polar switched cells (CBSC) [145]
  - Switched dc-sources (SDS) [167-169]
  - Packed U-cell (PUC) [65, 170]

Unit-based MLIs: These topologies can produce a definite number of levels. i.e., each unit of these topology is a RSC-MLI by-self.

- Ebrahim Babaei topologies
  - HSC based topology [135, 136]
  - Basic unit topology [171]
- Charles Ikechukwu Odeh topologies
  - Five-level symmetrical topology [172]
  - Nine-level symmetrical topology [173]
- Samrudei topologies
  - Envelope (E-type) type topology [150]
  - Square T-type (ST-type) topology [151]

Three-phase topologies: These topologies are developed either by using a common input dc-link to all phases or modifying the dc source in two-level inverter.

- Ahmed Salem Topologies [174]
- Ammar Masaoud Topologies [148, 149]
  - Topology-I
  - Topology-II
  - Topology-III
  - Topology-IV

2.4 RSC-MLI topologies reported in literature

In this Section, the switching operation, highlighted features, specifications and applications of various RSC-MLI topologies are reported. The main features of the topology is defined in terms of modularity, redundancy, ability to allow asymmetric dc voltage ratios and dc voltage requirement.

2.4.1 Multilevel dc-link (MLDCL) RSC-MLI

MLDCL RSC-MLI topology is introduced by S. Gui-Jia in 2005 [153, 157]. Among the newly designed RSC-MLI configurations, MLDCL topology is well recognized due to its modular structure. The configuration of MLDCL includes separate polarity and level generating units. The redundant and modular based structure of MLDCL with isolated input dc sources makes it to be an attractive substitute for conventional CHB MLI in applications such as power quality, grid integration and front-end applications. The level generator of this topology involves several basic modules connected in series. Each basic module comprises of a half-bridge with a separate dc source. Each half-bridge basic module produce an output voltage of V_{dc} or zero. If n number of basic modules connected in the level generator, then it generates (n+1) unipolar levels with magnitude varying from zero to nV_{dc}. Polarity generator includes an H-bridge which converts this (n+1) unipolar level to bipolar voltage with (2n+1) levels in phase-voltage. The switches of this H-bridge operate at fundamental frequency. The blocking voltage appears across the switches of H-bridge is equal to the sum of all dc link voltages (nV_{dc}). Uniform voltage stress and equal blocking voltages (V_{dc}) appears across the switches in level generator. This MLDCL topology operates as both symmetrical and asymmetrical configuration. Topological structure of MLDCL RSC-MLI with three dc sources is given in Fig. 2.3.

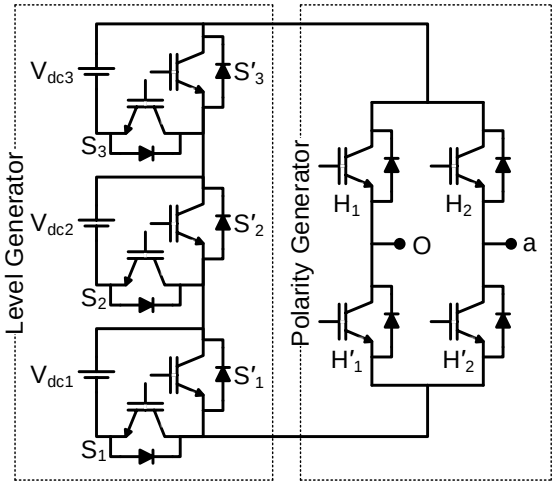


Fig. 2.3: Multilevel dc link (MLDCL) RSC-MLI with three dc sources.

If equal dc sources are connected to dc-link of MLDCL in Fig. 2.3, then this topology generates seven-level in output phase-voltage. If the voltages of dc sources with 1: 2: 3 ratio, Fig. 2.3 generates thirteen-levels in output voltage. Switching states of symmetrical and asymmetrical sources based MLDCL topology is given Table 2.3.

Table 2.3: Switching states of MLDCL inverter.

Num. of states	Voltage combinations	Switches in conduction		Output voltage	Output voltage
		Level generator	Polarity generator	$V_{dc1} = V_{dc2} = V_{dc3} = V_{dc}$	$V_{dc1}: V_{dc2}: V_{dc3} = 1: 2: 3\ V_{dc}$
1	$V_{dc1}+V_{dc2}+V_{dc3}$	S_1-S_2-S_3	H_1-H'_2	$+3V_{dc}$	$+6V_{dc}$
2			H_2-H'_1	$-3V_{dc}$	$-6V_{dc}$
3	$V_{dc2}+V_{dc3}$	S_1'-S_2-S_3	H_1-H'_2	$+2V_{dc}$	$+5V_{dc}$
4			H_2-H'_1	$-2V_{dc}$	$-5V_{dc}$
5	$V_{dc1}+V_{dc3}$	S_1-S_2'-S_3	H_1-H'_2	$+2V_{dc}$	$+4V_{dc}$
6			H_2-H'_1	$-2V_{dc}$	$-4V_{dc}$
7	$V_{dc1}+V_{dc2}$	S_1-S_2-S_3'	H_1-H'_2	$+2V_{dc}$	$+3V_{dc}$
8			H_2-H'_1	$-2V_{dc}$	$-3V_{dc}$
9	V_{dc3}	S_1'-S_2'-S_3	H_1-H'_2	$+V_{dc}$	$+3V_{dc}$
10			H_2-H'_1	$-V_{dc}$	$-3V_{dc}$
11	V_{dc2}	S_1'-S_2 -S_3'	H_1-H'_2	$+V_{dc}$	$+2V_{dc}$
12			H_2-H'_1	$-V_{dc}$	$-2V_{dc}$
13	V_{dc1}	S_1-S_2'-S_3'	H_1-H'_2	$+V_{dc}$	$+V_{dc}$
14			H_2-H'_1	$-V_{dc}$	$-V_{dc}$
15	0	S_1'-S_2'-S_3'	H_1-H'_2	0	0
16			H_2-H'_1		

2.4.2 Switched series parallel sources (SSPS) RSC-MLI

Switched series parallel sources (SSPS) RSC-MLI configuration generates the levels in the output voltage by switching of dc voltage sources in series/parallel connection. This topology was proposed by Hinago and Koizumi in 2009 [154, 155]. SSPS has a modular structure with separate level and polarity generator. Polarity generator converts unipolar multilevel voltage generated by level generator into bipolar voltage along with zero voltage level. The topological structure of SSPS MLI with three voltage sources is shown in Fig. 2.4. With *n* equal dc voltage sources, four switching devices in polarity generator and 3(*n*–1) switches in level generator, SSPS generates (2*n*+1) levels in output phase-voltage. With the series/parallel operation of dc sources of this topology, increases the utilization of dc sources and this feature explores in the later part of the thesis. The possible switching states of SSPS with equal and unequal dc sources are shown in Table 2.4. From this table it is observed that, to obtain any voltage level (either positive or negative polarity), only two switches of level generator are in conduction. If equal dc voltages sources are used then this topology produce seven-levels in output phase-voltage as shown in Table 2.4. The switching redundancies given in Table 2.4 of symmetrical SSPS benefits in improving its fault tolerant ability and achieving in equal utilization of input dc sources. In symmetrical SSPS MLI, the maximum blocking voltages appear across each device in polarity and level generating parts are nV_{dc} and V_{dc} respectively. Similar to MLDCL topology, SSPS MLI also cannot operate with trinary input dc voltage ratios. The possible switching states of

asymmetrical SSPS with input dc link voltage ratio of 1: 2: 3 to generate thirteen-levels in output phase-voltage is given in Table 2.4. A further significant reduction in number of device count can be achieved by adding of an extra H-bridge to SSPS is proposed in [154]. To reduce the switching losses, the additional H-bridge can be operated at carrier frequency and level generator at fundamental frequency.

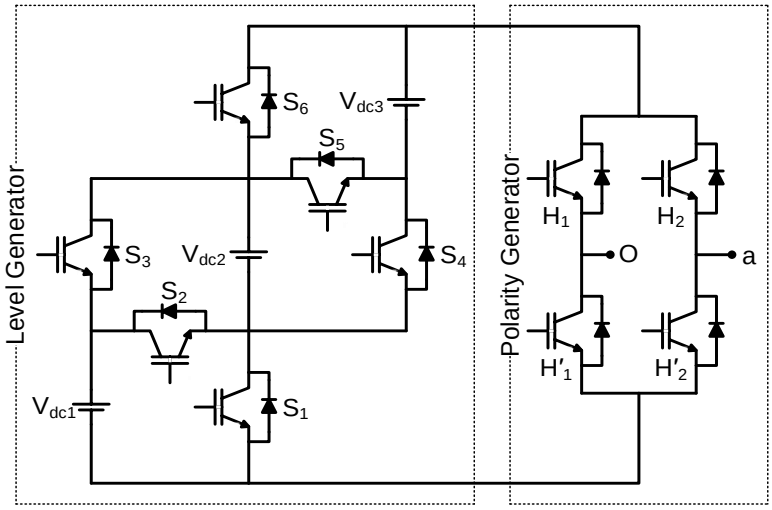


Fig. 2.4: Switched series parallel sources (SSPS) RSC-MLI with three dc sources.

Table 2.4: Switching states of SSPS inverter.

Num. of states	**Voltage combinations**	**Switches in conduction**		**Output voltage**	**Output voltage**
		Level generator	**Polarity generator**	**$V_{dc1} = V_{dc2} = V_{dc3} = V_{dc}$**	**$V_{dc1} : V_{dc2} : V_{dc3} = 1: 2: 3\ V_{dc}$**
1	$V_{dc1}+V_{dc2}+V_{dc3}$	S_2-S_5	H_1-H'_2	$+3V_{dc}$	$+6V_{dc}$
2			H_2-H'_1	$-3V_{dc}$	$-6V_{dc}$
3	$V_{dc2}+V_{dc3}$	S_1-S_5	H_1-H'_2	$+2V_{dc}$	$+5V_{dc}$
4			H_2-H'_1	$-2V_{dc}$	$-5V_{dc}$
5	$V_{dc1}+V_{dc3}$	S_3-S_5	H_1-H'_2	$+2V_{dc}$	$+4V_{dc}$
6			H_2-H'_1	$-2V_{dc}$	$-4V_{dc}$
7	$V_{dc1}+V_{dc2}$	S_2-S_6	H_1-H'_2	$+2V_{dc}$	$+3V_{dc}$
8			H_2-H'_1	$-2V_{dc}$	$-3V_{dc}$
9	V_{dc3}	S_1-S_4	H_1-H'_2	$+V_{dc}$	$+3V_{dc}$
10			H_2-H'_1	$-V_{dc}$	$-3V_{dc}$
11	V_{dc2}	S_1-S_6	H_1-H'_2	$+V_{dc}$	$+2V_{dc}$
12			H_2-H'_1	$-V_{dc}$	$-2V_{dc}$
13	V_{dc1}	S_3-S_6	H_1-H'_2	$+V_{dc}$	$+V_{dc}$
14			H_2-H'_1	$-V_{dc}$	$-V_{dc}$
15	0	----	H_1-H_2	0	0
16			H'_2-H'_1		

2.4.3 Reverse voltage (RV) RSC-MLI

In 2012, Ehsan Najafi introduced a new topology with a reversing-voltage phenomenon and thus named it as reverse voltage (RV) RSC-MLI [146, 158]. This configuration needs less switching devices especially at higher levels; consequently a reduction in total cost and complexity is achieved. The structure of RV RSC-MLI with three voltage sources is shown in Fig. 2.5. This configuration is modular in its structure with separate polarity and level generators. Number of levels in output voltage can be increased by duplicating the circled middle stage of level generator shown in Fig. 2.5.

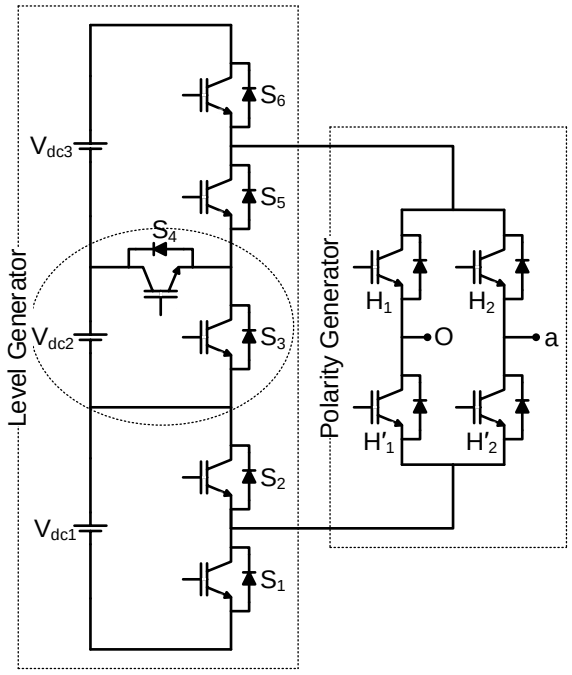


Fig. 2.5: Reverse voltage (RV) RSC-MLI with three dc voltage sources.

With *n* equal dc sources, this topology requires four switches in the polarity generator and 2*n* switches in level generator to generate (2*n*+1) levels in output phase-voltage. Moreover, with equal rating of dc sources, the blocking voltages of switches in level generator are equal. This topology requires isolated dc sources. However, by using isolation transformers at the load terminals, three-phase RV can be implemented with a common dc link for all the phases. This will reduce the requirement of dc sources to 1/3, as compared to CHB MLI [146]. An asymmetrical RV structure is also possible with suitable combination of input dc voltage sources. The switching operation of symmetrical and asymmetrical source based RV MLI (shown in Fig. 2.5) for generating seven and thirteen-levels in output phase-voltage is given in Table 2.5. From Table 2.5, it is confirmed that RV MLI generates output voltage levels for additive combinations of dc voltage sources and it doesn't have suitable switching redundancies to acquire uniform utilization of dc sources.

Table 2.5: Switching states of RV inverter.

Num. of states	Voltage combinations	Switches in conduction		Output voltage	Output voltage
		Level generator	Polarity generator	$V_{dc1} = V_{dc2} = V_{dc3} = V_{dc}$	$V_{dc1}: V_{dc2}: V_{dc3} = 1: 3: 2\ V_{dc}$
1	$V_{dc1}+V_{dc2}+V_{dc3}$	S_1-S_6	H_1-H'_2	$+3V_{dc}$	$+6V_{dc}$
2			H_2-H'_1	$-3V_{dc}$	$-6V_{dc}$
3	$V_{dc2}+V_{dc3}$	S_2-S_6	H_1-H'_2	$+2V_{dc}$	$+5V_{dc}$
4			H_2-H'_1	$-2V_{dc}$	$-5V_{dc}$
5	$V_{dc1}+V_{dc2}$	S_1-S_4-S_5	H_1-H'_2	$+2V_{dc}$	$+4V_{dc}$
6			H_2-H'_1	$-2V_{dc}$	$-4V_{dc}$
7	$V_{dc1}+V_{dc3}$	---	----------		
9	V_{dc2}	S_2-S_4-S_5	H_1-H'_2	$+V_{dc}$	$+3V_{dc}$
10			H_2-H'_1	$-V_{dc}$	$-3V_{dc}$
11	V_{dc3}	S_2-S_3-S_4-S_6	H_1-H'_2	$+V_{dc}$	$+2V_{dc}$
12			H_2-H'_1	$-V_{dc}$	$-2V_{dc}$
13	V_{dc1}	S_1-S_3-S_5	H_1-H'_2	$+V_{dc}$	$+V_{dc}$
14			H_2-H'_1	$-V_{dc}$	$-V_{dc}$
15	0	S_2-S_3-S_5	H_1-H'_2	0	0
16			H_2-H'_1		

2.4.4 Series connected switched sources (SCSS) RSC-MLI

The series connected switched sources (SCSS) proposed in [159, 160] consists of separate polarity and level generators. With *n* dc sources, SCSS generates (2*n*+1) levels in phase-voltage, by including four switches in polarity generator and 2*n* switches in level generator. Level generator possess multiple modular units connected in series and arranged in stair-case structure, as shown in Fig. 2.6.

Each module in level generator has a dc source with two switches operate in a complimentary manner. As the name of the MLI conveys, SCSS generates the necessary phase-voltage levels by connecting the dc sources in series through switches. The switches in the polarity generator operates at fundamental frequency and the devices in level generator are switching at carrier frequency. This topology can easily be extended to higher levels, however, the devices blocking voltages are unequal and increases with the maximum dc link voltage. The dc sources are non-isolated and can be replaced with PV or fuel cells in grid connected applications. The structure of SCSS RSC-MLI with three dc voltage sources is shown in Fig. 2.6 and its switching states for generating seven-levels in the output voltage is shown in Table 2.6. From this table, it is observed that the lack of switching redundancies in this structure increases the effort in balancing dc link voltages. This topology cannot support asymmetrical dc voltage ratios.

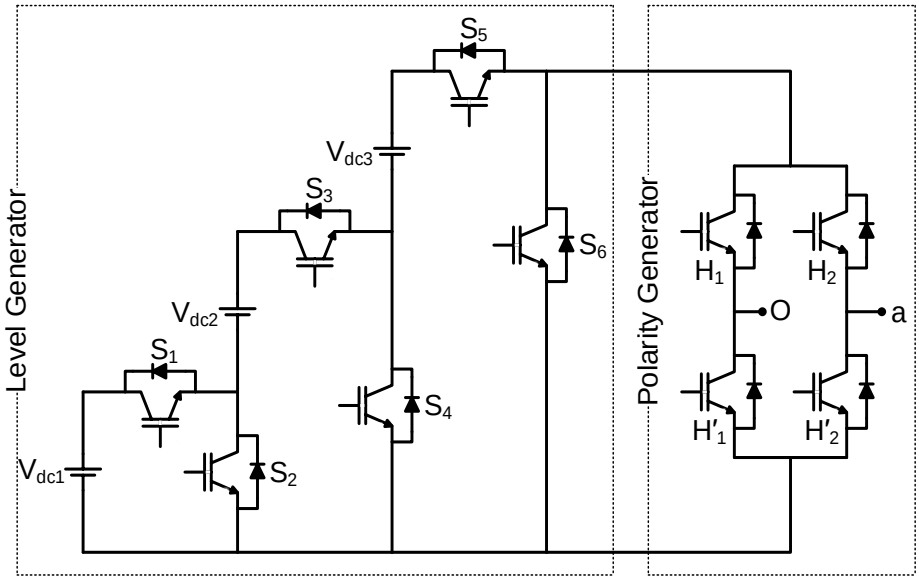


Fig. 2.6: Series connected switched sources (SCSS) RSC-MLI with three dc voltage sources.

Table 2.6: Switching states of seven-level SCSS topology.

Num. of states	Voltage combinations	Switches in conduction		Output voltage
		Level generator	Polarity generator	$V_{dc1}= V_{dc2}= V_{dc3} = V_{dc}$
1	$V_{dc1}+V_{dc2}+V_{dc3}$	S_1-S_3-S_5	H_1-H'_2	$+3V_{dc}$
2			H_2-H'_1	$-3V_{dc}$
3	$V_{dc2}+V_{dc3}$	S_2-S_3-S_5	H_1-H'_2	$+2V_{dc}$
4			H_2-H'_1	$-2V_{dc}$
5	V_{dc3}	S_4-S_5	H_1-H'_2	$+V_{dc}$
6			H_2-H'_1	$-V_{dc}$
7	0	S_6	H_1-H'_2	0
			H_2-H'_1	

2.4.5 T-type topologies

Among the various RSC-MLI topologies, T-type based topologies are the most popular with appreciable reduction in switch count. These topologies involve a combination of uni-directional and bi-directional switches. In literature, this topology is reported in three different arrangements. They are (a) T-type [139, 141, 144, 162, 163] (b) Half-leg T-type [165] and (c) Cascaded T-type [143]. All these topologies are modular in structure and can be generalized for any level, however each of them has their own advantages and drawbacks. Next section describes their topological arrangement, operation and features.

2.4.5.1 T-type RSC-MLI

T-type RSC-MLI is an H-bridge based configuration proposed by Ceglia *et al*. in 2006. It is well adapted in grid connected PV systems [139, 141, 144, 162, 163]. With *n* equal dc sources, this configuration requires four uni-directional switches and *n*–1 bi-directional switching device

and generates (2*n*+1) levels in the output voltage. The uni-directional devices are arranged to form an H-bridge and the mid-point of its one phase-leg is connected to input dc link through bi-directional switches as shown in Fig. 2.7. The switches in the phase-leg of the H-bridge to which the bi-directional devices are connected are operate at carrier frequency and the switches in the other phase-leg are operate at fundamental frequency. At any instant, only two switches will conduct, which benefits in decreasing the conduction losses. T-type MLI offers 24% decrease in switch count for five-level, and 37.5% for nine-level when compared to CHB MLI. The switching states to attain seven-levels in output voltage are shown in Table 2.7. From Fig. 2.7 and Table 2.7, it is observed that the T-type does not have switching redundancies and cannot operate with asymmetrical dc sources. Further, this topology does not facilitate even power distribution and produces unequal device blocking voltages. In Fig. 2.7, the maximum blocking voltage for S_5 and S_6 is $2V_{dc}$ and for switches in H-bridge is $3V_{dc}$.

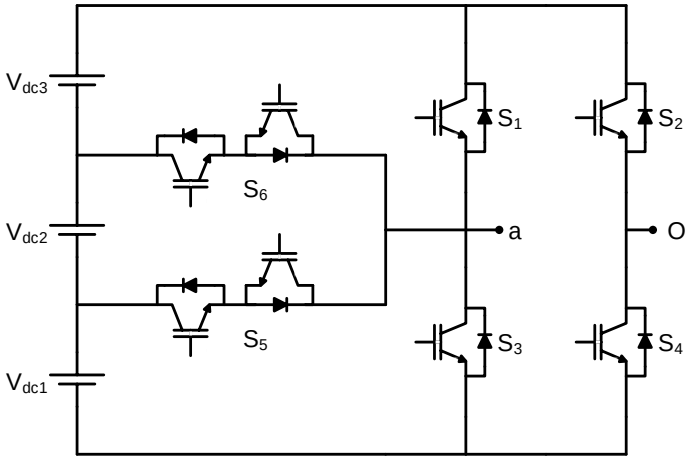


Fig. 2.7: Seven-level T-type RSC-MLI.

Table 2.7: Switching states of seven-level T-type RSC-MLI.

Num. of states	**Voltage combinations**	**Switches in conduction**	**Output voltage** $\mathbf{V_{dc1} = V_{dc2} = V_{dc3} = V_{dc}}$
1	$+(V_{dc1}+V_{dc2}+V_{dc3})$	S_1-S_4	$+3V_{dc}$
2	$+(V_{dc1}+V_{dc2})$	S_6-S_4	$+2V_{dc}$
3	$+V_{dc1}$	S_5-S_4	$+V_{dc}$
4	$-V_{dc3}$	S_6-S_2	$-V_{dc}$
5	$-(V_{dc2}+V_{dc3})$	S_5-S_2	$-2V_{dc}$
6	$-(V_{dc1}+V_{dc2}+V_{dc3})$	S_3-S_2	$-3V_{dc}$
7	0	(S_1-S_2) or (S_3-S_4)	0

2.4.5.2 Half-leg based T-type topology

A T-type topology [165, 166] which consists of half-bridge based structure, acts as a viable substitute to active neutral pointed clamped (ANPC) [175] and DCMLI configurations for high-power medium-voltage applications. The dc link of this structure is common to all the three

phases and each phase-leg is linked to the dc link by using bi-directional devices. The topological view of this MLI for a three-level output voltage is shown in Fig. 2.8 and its switching operation is given in Table 2.8. In this structure, at any instant, only two switches are in conduction which leads to the decrease of conduction losses as compared to DCMLI. With *n* equal voltage sources, this topology requires two uni-directional and (*n*–1) bi-directional switching devices in each phase-leg. This topology can able to generate odd and even levels in phase-voltage and can be further increased by connecting several number of dc sources along with bi-directional switches.

The voltage rating of bi-directional switches is lower than the devices in phase-leg. For example, with equal dc link voltages in Fig. 2.8, the maximum voltage rating of bi-directional switch is $V_{dc}/2$, whereas the devices in phase-leg are rated at V_{dc}.. Thus, this topological configuration produce lower conduction losses and blocking voltages compared to DCMLI, NPP and ANPC. This topology is reported for various PV and grid connected applications [176]. Fault tolerant strategies and reconfiguration of this inverter for OC switch faults is also reported in [166]. The main drawbacks of this MLI are lack of switching redundancies, operates with unequal blocking voltages and mandatorily requires dc voltage ratios to be symmetrical. However, the charge balance among the dc link voltages can be obtained by equalizing the rate of charge over a fundamental cycle as proposed in [144].

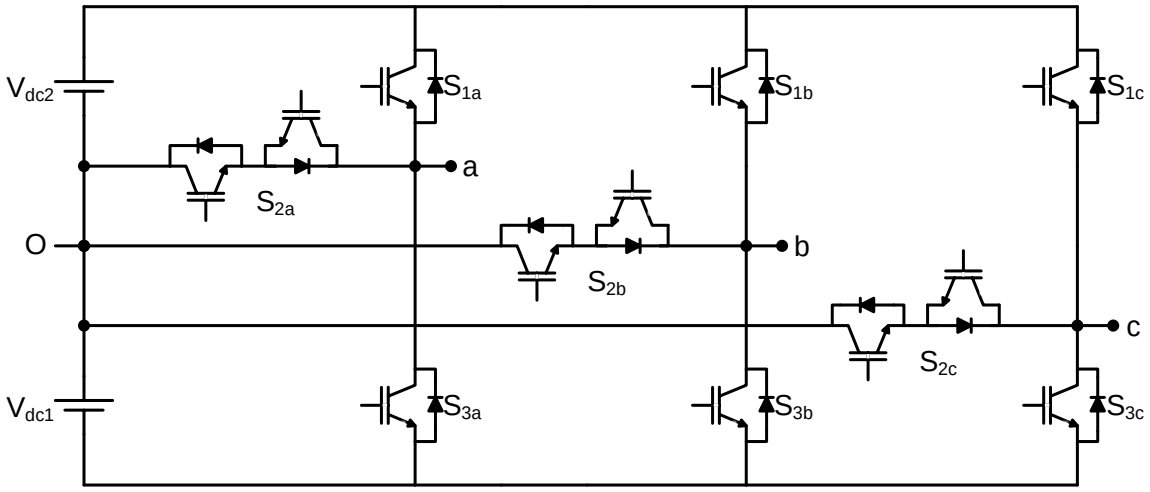


Fig. 2.8: Three-phase half-leg three-level T-type RSC-MLI.

Table 2.8: Switching states of three-level half-leg T-type RSC-MLI.

No. of states	Voltage combinations	Switches in conduction	Output voltage: $V_{dc1} = V_{dc2} = V_{dc}$
1	$+V_{dc1}$	S_1-S_2	$+V_{dc}$
2	0	S_2	0
3	$-V_{dc2}$	S_2-S_3	$-V_{dc}$

2.4.5.3 T-type Cascaded RSC-MLI

In order to increase the number of output voltage levels, T-type RSC-MLI can be extended in two ways. First one is by connecting several dc sources along with bi-directional devices as shown in Fig. 2.7. The other way is by connecting several T-type basic units in cascade [143]. Cascade connection of modules provide the facility to operate using both equal and unequal voltage ratios in dc sources. However, dc link voltage ratio in an individual T-type module should be identical. The number of phase-voltage levels of this cascaded configuration depends on the number of levels in each T-type module. Fig. 2.9 represents the cascade T-type topology with two five-level T-type basic units and its corresponding switching states are presented in Table 2.9.

Cascade connection of k number of l-level T-type modules with symmetric sources, generates $k(l–1)+1$ levels in the output phase-voltage. By considering symmetrical dc-link voltage ratios, Fig. 2.9 (k = 2 and l = 5) generates nine-levels in output voltage. Switching redundancies presented in Table 2.9 confirms the ability of cascaded T-type RSC-MLI to enable uniform power distribution among the cascaded T-type modules. In additional, operation of this MLI shown in Fig. 2.9 with binary (1: 2) dc-link voltage ratios, generates thirteen-levels in output voltage and its corresponding switching states are given in Table 2.9.

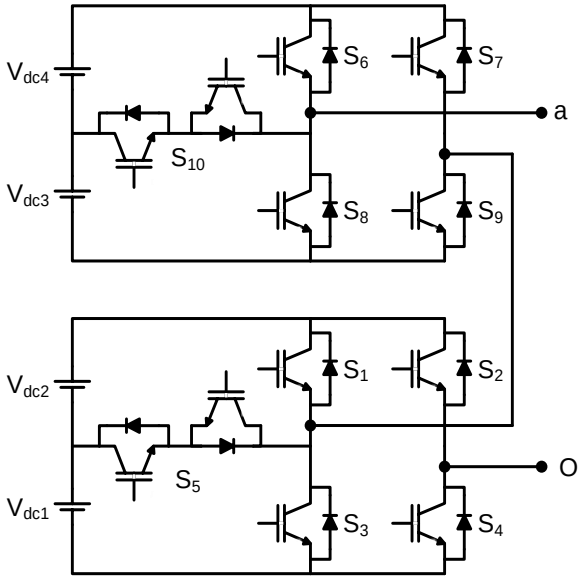


Fig. 2.9: Topological structure of cascaded T-type RSC-MLI.

Table 2.9: Switching operation of cascaded T-type RSC-MLI.

Num. of states	Voltage combinations	Switches in conduction	Output voltage	
			Symmetrical	Asymmetrical
			9-level	13-level
			$V_{dc1} = V_{dc2} = V_{dc3} = V_{dc4} = V_{dc}$	$V_{dc1} = V_{dc2} = V_{dc}$ $V_{dc3} = V_{dc4} = 2V_{dc}$
1	$(V_{dc1}+V_{dc2}+V_{dc3}+V_{dc4})$	S_4-S_1-S_9-S_6	$+4V_{dc}$	$+6V_{dc}$
2	$+(V_{dc1}+V_{dc3}+V_{dc4})$	S_4-S_5-S_9-S_6	$+3V_{dc}$	$+5V_{dc}$
3	$+(V_{dc1}+V_{dc2}+V_{dc3})$	S_4-S_1-S_9-S_{10}	$+3V_{dc}$	$+4V_{dc}$
4	$+(V_{dc3}+V_{dc4})$	S_3-S_4-S_6- S_9	$+2V_{dc}$	$+4V_{dc}$
5	$+(V_{dc1}+V_{dc3})$	S_4-S_5-S_9-S_2	$+2V_{dc}$	$+3V_{dc}$
6	$+(V_{dc3}+V_{dc4}–V_{dc2})$	S_2-S_5-S_9-S_6	$+V_{dc}$	$+3V_{dc}$
7	$+V_{dc3}$	S_3-S_4-S_9-S_{10}	$+V_{dc}$	$+2V_{dc}$
8	$+(V_{dc1}+V_{dc2})$	S_4-S_1-S_9-S_8	$+2V_{dc}$	$+2V_{dc}$
9	$+V_{dc1}$	S_4-S_5-S_9-S_8	$+V_{dc}$	$+V_{dc}$
10	0	S_4-S_3-S_9-S_8 (or) S_2-S_1-S_7-S_6	0	0
11	$–V_{dc2}$	S_2-S_5-S_7-S_6	$–V_{dc}$	$–V_{dc}$
12	$–V_{dc4}$	S_2-S_1-S_7-S_{10}	$–V_{dc}$	$–2V_{dc}$
13	$–V_{dc3}–V_{dc4}+V_{dc1}$	S_4-S_5-S_7-S_8	$–V_{dc}$	$–3V_{dc}$
14	$–(V_{dc1}+V_{dc2})$	S_2-S_3-S_7-S_6	$–2V_{dc}$	$–2V_{dc}$
15	$–(V_{dc2}+V_{dc4})$	S_2-S_5-S_7-S_2	$–2V_{dc}$	$–3V_{dc}$
16	$–(V_{dc3}+V_{dc4})$	S_2-S_1-S_7-S_8	$–2V_{dc}$	$–4V_{dc}$
17	$–(V_{dc1}+V_{dc2}+V_{dc4})$	S_2-S_3-S_7-S_{10}	$–3V_{dc}$	$–4V_{dc}$
18	$–(V_{dc2}+V_{dc3}+V_{dc4})$	S_2-S_5-S_7-S_8	$–3V_{dc}$	$–5V_{dc}$
19	$–(V_{dc1}+V_{dc2}+V_{dc3}+V_{dc3})$	S_2-S_3-S_9-S_6	$–4V_{dc}$	$–6V_{dc}$

2.4.6 Multilevel module (MLM) based RSC-MLI

Multilevel module (MLM) based RSC-MLI using three dc voltage sources is depicted in Fig. 2.10 and was introduced by E. Babaei in 2012 [161]. This MLI consists of separate level and polarity generating parts which includes bi-directional and uni-directional switching devices respectively. The level generating has bi-directional current conducting and bi-directional voltage blocking capabilities, whereas the polarity generator has bi-directional current conducting and uni-directional voltage blocking capability. Level generator is column based structure designed by connecting bi-directional switches and dc link voltages at various nodes. This MLI can be extended to higher levels by increasing voltage sources along with bi-directional switching

devices. At any voltage level, one bidirectional switch in level generating part and two switches in the polarity generating part remains in conduction.

By using *n* equal dc voltage sources, this MLI configuration requires (*n*+1) bi-directional switching devices in the level generator and four uni-directional switches in the polarity generator to obtain (2*n*+1) levels in the output phase-voltage. With symmetrical dc voltage sources, Fig. 2.10 generate seven-levels in output voltage and their corresponding switching states are presented in Table 2.10. Due to the absence of switching redundancies, it is difficult to achieve equal load distribution among the input dc sources. This structure does not allow unequal input dc-link voltages and further, blocking voltages of the switching devices are unequal.

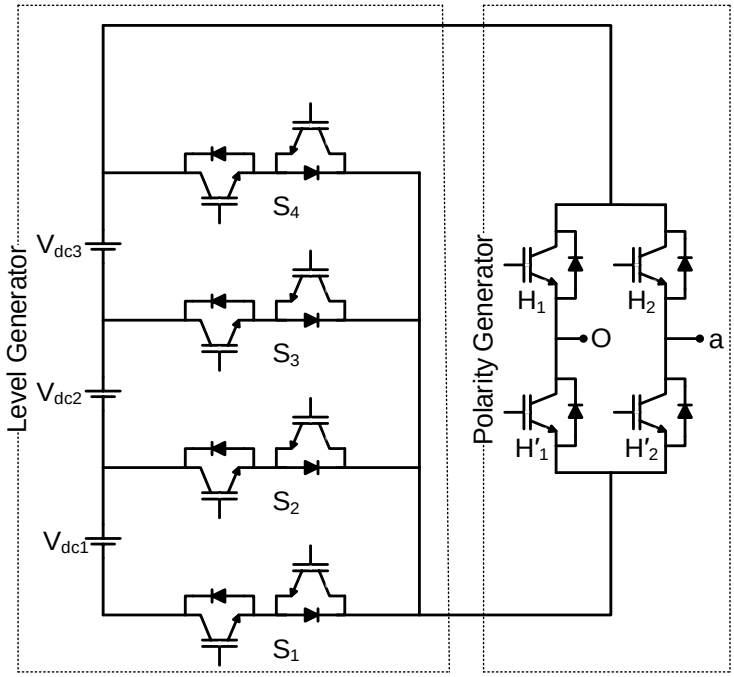


Fig. 2.10: Multilevel module (MLM) based RSC-MLI

Table 2.10: Switching states of MLM based RSC-MLI.

Num. of states	**Voltage combinations**	**Switches in conduction**		**Output voltage**
		Level generator	**Polarity generator**	$\mathbf{V_{dc1} = V_{dc2} = V_{dc3} = V_{dc}}$
1	$V_{dc1}+V_{dc2}+V_{dc3}$	S_1	H_1-H'_2	$+3V_{dc}$
2			H_2-H'_1	$-3V_{dc}$
3	$V_{dc2}+V_{dc3}$	S_2	H_1-H'_2	$+2V_{dc}$
4			H_2-H'_1	$-2V_{dc}$
5	V_{dc3}	S_3	H_1-H'_2	$+V_{dc}$
6			H_2-H'_1	$-V_{dc}$
7	0	S_4	H_1-H'_2	0
			H_2-H'_1	

2.4.7 Hybrid T-type RSC-MLIs

These topologies consist of both bi-directional and uni-directional switching devices and does not have a separate level or polarity generators. Six uni-directional switching devices are used to construct a hexagon switch cell (HSC) and bi-directional devices are connected between HSC and the dc link. In the other way, the back to back connection of two half-legs connected through a pair of uni-directional switches forms a HSC structure. This HSC structure allows these topologies to operate with multiple switching redundancies to achieve the desired output voltage. these topologies are extended to higher levels by increasing the number of bi-directional switches. These are similar to T-type, since its arrangement is analogous to back to back connection of two half-leg T-type cells through a pair of uni-directional switches. Hence, these topologies can be named as hybrid T-type or enhanced T-type RSC-MLI and was introduced by Shivam Prakash Gautam *et al*. in 2015. Based on the involvement and placing of bi-directional switches, two possible topological arrangements are reported [137, 138].

2.4.7.1 Topology – I

(*Hybrid T-type topology using bi-directional device on one side of HSC* [137, 138])

The structure of this topology with two dc voltage sources V_{S1} and V_{R1} on either side of HSC is shown in Fig. 2.11. Several dc link capacitors are linked to HSC through bi-directional switching devices. Voltage of V_{S1} source is equally shared by these dc link capacitors. By using n number of dc link capacitors, this MLI includes (n–1) bi-directional devices and six uni-directional switching devices. Number of levels in the output voltage can be increased in two possible ways. First one is extend the structure of this topology by using multiple bi-directional switching devices as shown in Fig. 2.12(a) and other way is by cascading several modules as given in Fig. 2.12(b).

From Fig. 2.11, it is confirmed that by open circuiting voltage source V_{R1} and, short circuiting of H_5 and H_2 switching devices in Fig. 2.11, modifies this MLI similar to five-level T-type topology as shown in Fig. 2.7. Therefore, the involvement of uni-directional devices i.e., H_5 and H_2 converts the H-bridge to HSC and, enables the structure to operate for unequal voltage source based topologies. Moreover, for V_{R1}= V_{S1}, the topology shown in Fig. 2.11 acts as symmetrical MLI and operates as an asymmetrical topology, if $V_{R1} \neq V_{S1}$. This structure with symmetrical dc voltage sources along with n dc link capacitors can able to generate ($4n$+1) levels in output phase-voltage. Hence, the MLI can be operated for 9, 13, 17, 21…. levels. Thus to operate the inverter for other voltage levels, asymmetrical configuration with appropriate voltage ratios should be selected.

For example, if $V_{R1} = V_{S1} = 2V_{dc}$ in Fig. 2.11, then $V_{C1} = V_{C2} = V_{S1}/2 = V_{dc}$ it operates as a nine-level inverter as presented in Table 2.11. If $2V_{R1} = V_{S1} = 2V_{dc}$, it generates seven-level in

phase-voltage with magnitude varying from $+3V_{dc}$ to $-3V_{dc}$ as shown in Table 2.11. Further, with $(2/3)V_{R1} = V_{S1} = 2V_{dc}$ in Fig. 2.11, generates eleven-level output phase-voltage as shown in Table 2.11. Cascade structure of this topology with two hybrid T-type modules (one bi-directional switch in each) is shown in Fig. 2.12(b). Thus, cascading two-modules with *n* dc link capacitors in each, then topological configuration of this inverter requires $2(n-1)$ bi-directional switches and 12 uni-directional switches.

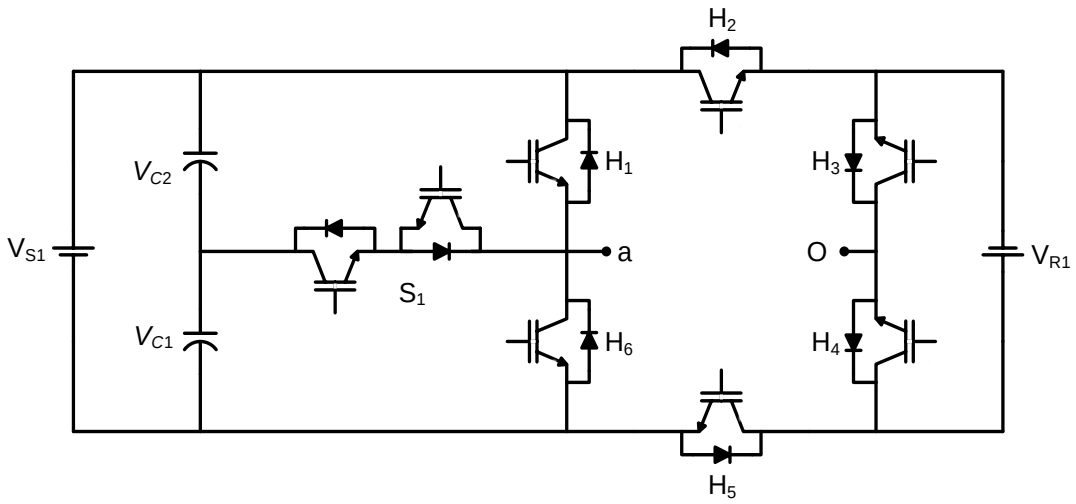
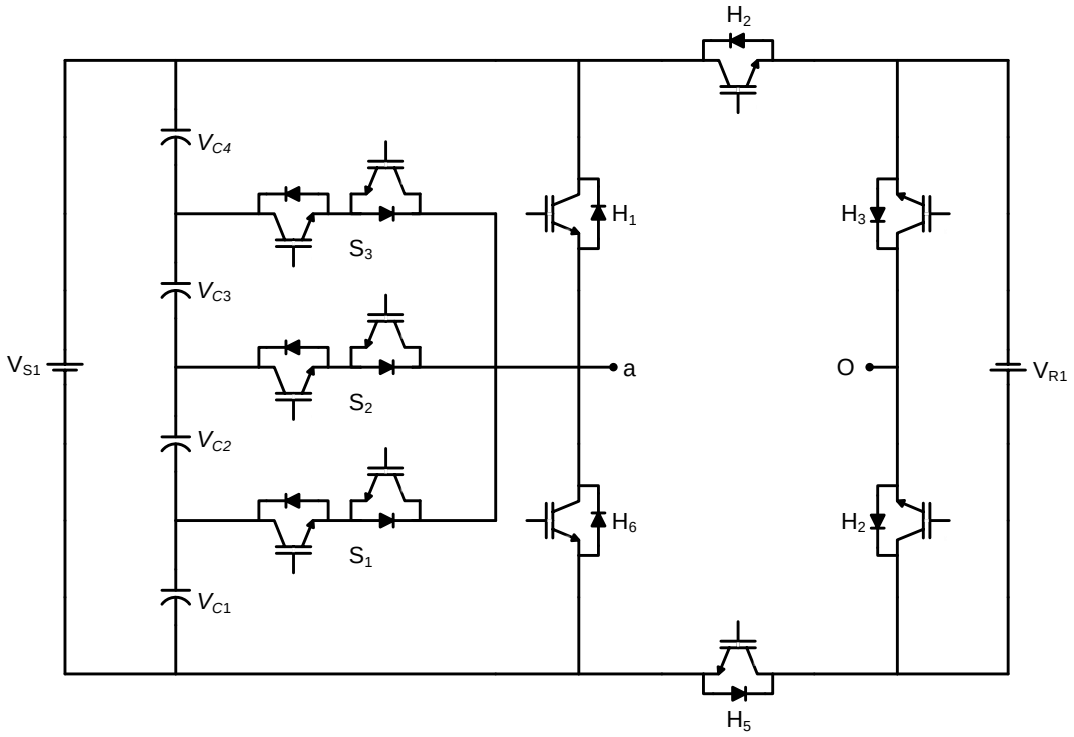


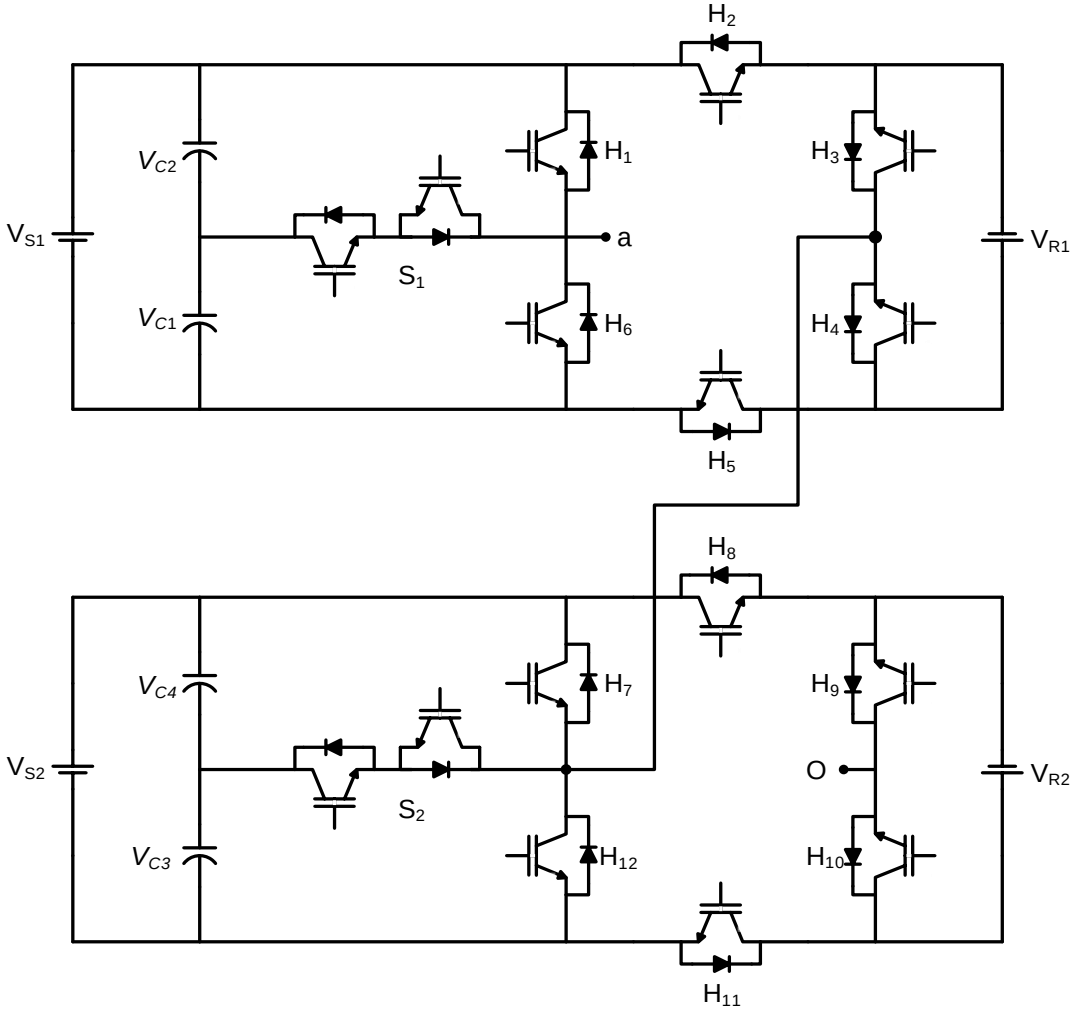
Fig. 2.11: Hybrid T-type MLI topology – I.

Table 2.11: Switching operation of hybrid T-Type HSC based topology – I.

Num. of states	**Voltage combinations (V_{C1}, V_{C2}, V_{R1})**	**Switches in conduction**	**Output voltage**		
			Symmetrical	**Asymmetrical**	
			Nine-level $V_{S1} = 2V_{dc}$ $V_{R1} = 2V_{dc}$ ($V_{C1} = V_{C2} = V_{dc}$)	**Seven-level** $V_{S1} = 2V_{dc}$ $V_{R1} = V_{dc}$ ($V_{C1} = V_{C2} = V_{dc}$)	**Eleven-level** $V_{S1} = 2V_{dc}$ $V_{R1} = 3V_{dc}$ ($V_{C1} = V_{C2} = V_{dc}$)
1	$+(V_{C1}+V_{C2}+V_{R1})$	H_3-H_5-H_1	$+4V_{dc}$	$+3V_{dc}$	$+5V_{dc}$
2	$+(V_{R1}+V_{C1})$	H_3-H_5-S_1	$+3V_{dc}$	$+2V_{dc}$	$+4V_{dc}$
3	$+(V_{C1}+V_{C2})$	H_4-H_5-H_1	$+2V_{dc}$	$+2V_{dc}$	$+3V_{dc}$
4	$+V_{R1}$	H_3-H_5-H_6	$+2V_{dc}$	$+V_{dc}$	$+2V_{dc}$
5	$+V_{C1}$	H_4-H_5-S_1	$+V_{dc}$	$+V_{dc}$	$+V_{dc}$
6	0	H_4-H_5-H_6	0	0	0
7	$-V_{C2}$	H_3-H_2-S_1	$-V_{dc}$	$-V_{dc}$	$-V_{dc}$
8	$-V_{R1}$	H_4-H_2-H_1	$-2V_{dc}$	$-V_{dc}$	$-2V_{dc}$
9	$-(V_{C1}+V_{C2})$	H_3-H_2-H_6	$-2V_{dc}$	$-2V_{dc}$	$-3V_{dc}$
10	$-(V_{R1}+V_{C2})$	H_3-H_2-S_1	$-3V_{dc}$	$-2V_{dc}$	$-4V_{dc}$
11	$-(V_{C1}+V_{C2}+V_{R1})$	H_4-H_2-H_6	$-4V_{dc}$	$-3V_{dc}$	$-5V_{dc}$



(a) Increasing number of levels without cascading



(b) Increasing number of levels with cascading Hybrid T-type module.

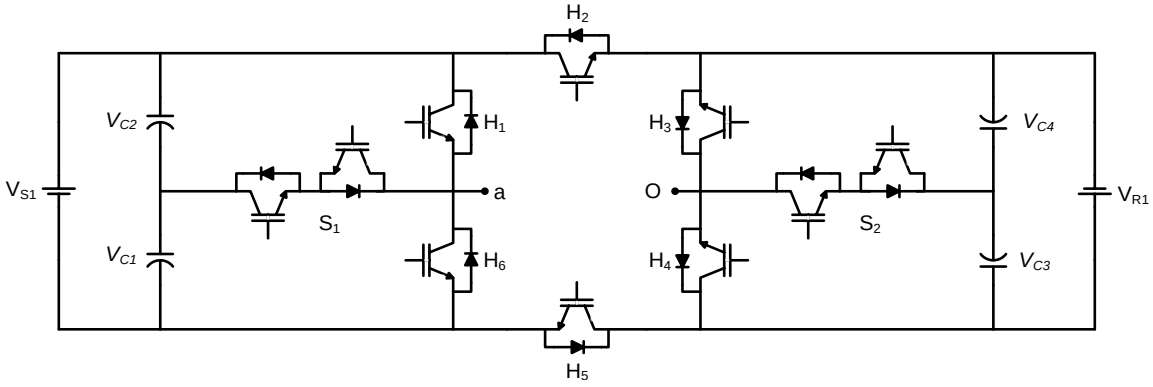
Fig. 2.12: Extension of hybrid T-type HSC based topology – I to higher levels.

2.4.7.2 Topology – II

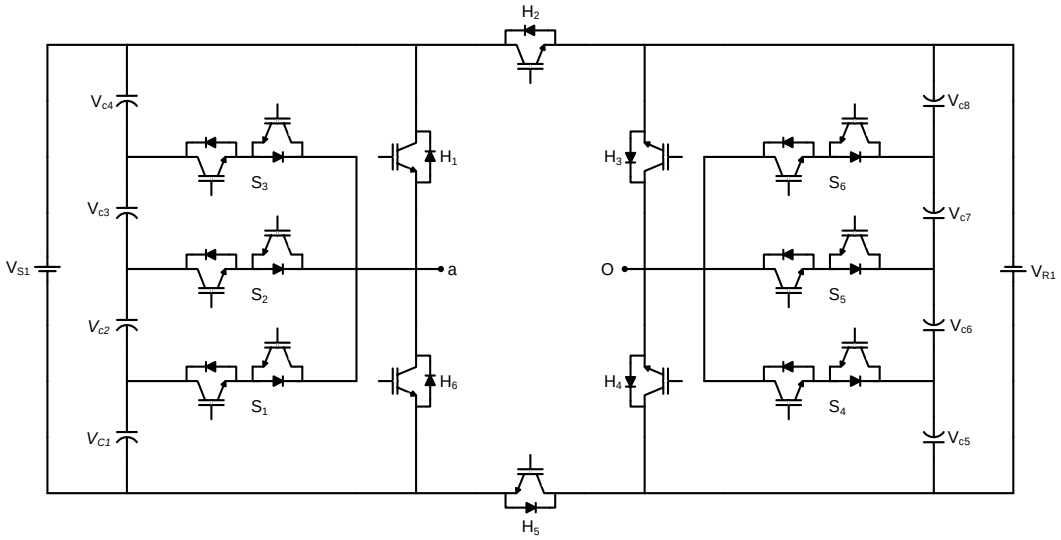
(*Hybrid T-type MLI with bi-directional switches on both sides of HSC* [137, 138])

This topology is similar to Topology-I described above, but here, bi-directional devices are inter connected to both sides of HSC for connecting the dc link. The structure of this MLI with one bi-directional device on both side of HSC is sown in Fig. 2.13(a). Extension of this configuration using additional bi-directional devices is represented in Fig. 2.13(b). Connecting bi-directional switches on both sides of HSC increases asymmetrical ability of the inverter and enables to obtain voltage levels with significant reduction in switch count. However, the remaining features and operation of this topology remains to be similar as Topology-I.

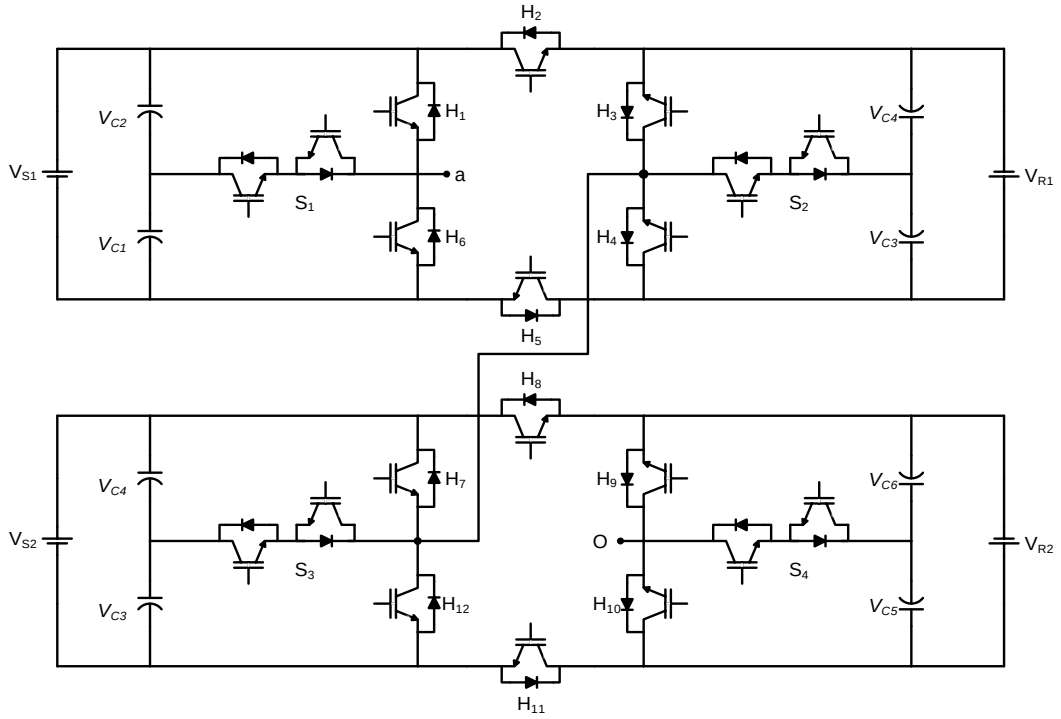
Nevertheless, the other features and principle of operation of this configuration is similar to topology-I. By using n dc-link capacitors shared by equal voltage sources on both sides of HSC, this MLI contains $2(n–1)$ bi-directional devices and six uni-directional devices and generates $(4n+1)$ levels in output phase-voltage. This topology is combination of two half-leg T-type RSC-MLIs connected in anti-parallel through a pair of uni-directional switching devices and it is observed from Fig. 2.13(a). Moreover, the extension of Fig. 2.13(a), by cascading multiple modules is shown in Fig. 2.13(c). Switching redundancies of Fig. 2.13(a) for symmetrical and asymmetrical configurations are given in Table 2.12. From Table 2.12, it is observed that, with $V_{C3} = V_{C4} = V_{R1}/2$ and $V_{C1} = V_{C2} = V_{S1}/2$, the structure shown in Fig. 2.13(a) generates a nine-level output voltage. If $V_{S1} = V_{dc}$ and $V_{R1} = 2V_{dc}$, generates thirteen-level output voltage varying from $+3V_{dc}$ to $–3V_{dc}$ as given in Table 2.12. Hence, the topologies in hybrid T-type facilitate to adapt with both symmetrical and asymmetrical dc voltage ratios and have significant decrease in switch count.



(a) Single module



(b) Increasing number of levels with increasing bidirectional switches.



(c) Increasing number of levels with cascading modules

Fig. 2.13: Hybrid T-type MLI topology – II.

Table 2.12: Switching operation of hybrid T-type topology – II.

Num. of states	Voltage combinations $V_{C1}= V_{C2}= \frac{V_{S1}}{2}$ $V_{C3} = V_{C4} = \frac{V_{R1}}{2}$	Switches in conduction	Output voltage	
			Symmetrical	Asymmetrical
			Nine-level	Thirteen-level
			$V_{S1}= 2V_{dc}$ $V_{R1} = 2V_{dc}$ $V_{C1}= V_{C2} = V_{dc}$ $V_{C1}= V_{C2} = V_{dc}$	$V_{S1} = V_{dc}$ $V_{R1} = 2V_{dc}$ $V_{C1}= V_{C2} = \frac{V_{dc}}{2}$ $V_{C3} = V_{C4} = V_{dc}$
1	$+(V_{C1}+V_{C2}+V_{C3}+V_{C4})$	H_3-H_5-H_1	$+4V_{dc}$	$+3V_{dc}$
2	$+(V_{C1}+V_{C3}+V_{C4})$	H_3-H_5-S_1	$+3V_{dc}$	$+(5/2)V_{dc}$
3	$+(V_{C3}+V_{C1}+V_{C2})$	S_2-H_5-H_1	$+3V_{dc}$	$+2V_{dc}$
4	$+(V_{C3}+V_{C4})$	H_3-H_5-H_6	$+2V_{dc}$	$+2V_{dc}$
5	$+(V_{C3}+V_{C1})$	S_2-H_5-S_1	$+2V_{dc}$	$+(3/2)V_{dc}$
6	$+V_{C3}$	S_2-H_5-H_6	$+V_{dc}$	$+V_{dc}$
7	$+(V_{C1}+V_{C2})$	H_4-H_5-S_1	$+2V_{dc}$	$+V_{dc}$
8	$+V_{C1}$	H_4-H_5-S_1	$+V_{dc}$	$+(1/2)\ V_{dc}$
9	0	H_3-H_2-H_1 (or) H_4-H_5-H_6	0	0
10	$-V_{C2}$	H_3-H_2-S_1	$-V_{dc}$	$-(1/2)V_{dc}$
11	$-(V_{C1}+V_{C2})$	H_3-H_2-H_6	$-2V_{dc}$	$-V_{dc}$
14	$-V_{C4}$	S_2-H_2-H_1	$-V_{dc}$	$-V_{dc}$
15	$-(V_{C2}+V_{C4})$	S_2-H_2-S_1	$-2V_{dc}$	$-(3/2)V_{dc}$
13	$-(V_{C3}+V_{C4})$	H_4-H_2-H_1	$-2V_{dc}$	$-2V_{dc}$
12	$-(V_{C1}+V_{C2}+V_{C4})$	S_2-H_2-H_6	$-3V_{dc}$	$-2V_{dc}$
16	$-(V_{C2}+V_{C3}+V_{C4})$	H_4-H_2-S_1	$-3V_{dc}$	$-(5/2)V_{dc}$
17	$-(V_{C1}+V_{C2}+V_{C3}+V_{C4})$	H_4-H_2-H_6	$-4V_{dc}$	$-3V_{dc}$

2.4.8 Cascaded bipolar switched cells (CBSC) based RSC-MLI

Cascaded bipolar switched cells (CBSC) based RSC-MLI is introduced by E. Babaei in 2008 [145]. This topology is highly modular and it is column based physical structure with involvement of bi-directional switching devices on both side of dc link at various nodes as shown in Fig. 2.14. This MLI does not contain a separate level and polarity generators and can easily extended to higher voltage levels by involving a pair of bi-directional devices and adding a voltage source. The topological structure of CBSC with three dc voltage sources is shown in Fig. 2.14 and its possible switching states for equal and unequal voltage sources for generating seven and thirteen-levels in the output voltage is presented in Table 2.13. For symmetrical dc-link voltage ratio, this topology require 2(n+1) bi-directional switches and generate (2n+1) levels in the output voltage. Even though, each bi-directional device consists of two IGBTs, the requirement of number of gate driver circuits are equal to the total number of bi-directional devices. This results in decrease in control complexity and overall cost the circuit. This topology does not have adequate switching redundancies to enable equal load distribution among input dc voltage sources.

In Fig. 2.14, if the equal voltage sources are considered, then the outermost switches i.e., S_1, S_2, S_7 and S_8 should block $3V_{dc}$.Whereas, inner switches S_3, S_4, S_5, and S_6 has to block $2V_{dc}$ only. This topology generates lesser conduction losses due to the operation of only two devices at any instant. Inability of this topology to realize output for subtractive combinations of dc sources limits its asymmetrical capability. CBSC can be extended to higher levels either by directly increasing the number of bi-directional switches or by connecting an additional CBSC modules in cascade. These topologies are reported as cascaded CBSC topologies [145]. Cascaded CBSC configuration can produce voltage levels for both additive and subtractive combination of dc sources and can be implemented for both symmetrical and asymmetrical configurations.

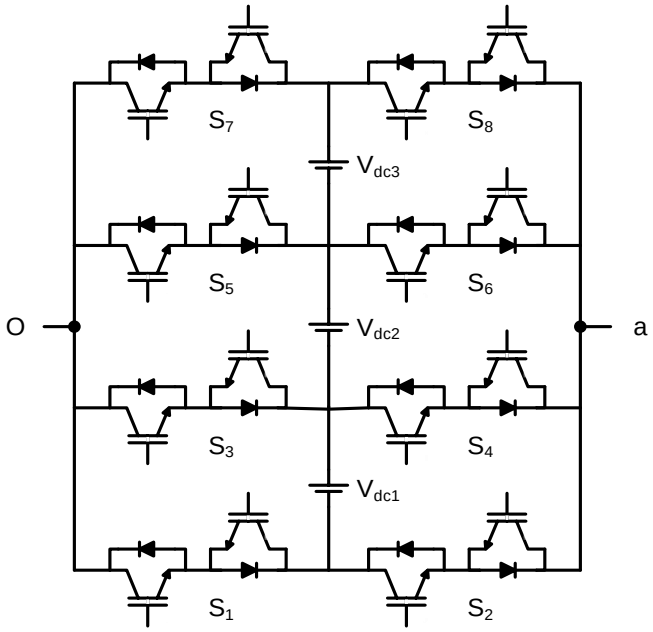


Fig. 2.14: Cascaded bipolar switched cells (CBSC) RSC-MLI.

Table 2.13: Switching operation of CBSC RSC-MLI.

Num. of states	**Voltage combinations**	**Switches in conduction**	**Output voltage**	
			Symmetrical	**Asymmetrical**
			$\mathbf{V_{dc1} = V_{dc2} = V_{dc3} = V_{dc}}$	$\mathbf{V_{dc1} = V_{dc}}$ $\mathbf{V_{dc2} = 3V_{dc}}$ $\mathbf{V_{dc3} = 2V_{dc}}$
1	$+ (V_{dc1}+V_{dc2}+V_{dc3})$	S_1-S_8	$+ 3V_{dc}$	$+ 6V_{dc}$
2	$+ (V_{dc2}+V_{dc3})$	S_3-S_8	$+ 2V_{dc}$	$+ 5V_{dc}$
3	$+ (V_{dc1}+V_{dc2})$	S_1-S_6	$+ 2V_{dc}$	$+ 4V_{dc}$
4	$+V_{dc2}$	S_3-S_6	$+ V_{dc}$	$+ 3V_{dc}$
5	$+V_{dc3}$	S_5-S_8	$+ V_{dc}$	$+ 2V_{dc}$
6	$+V_{dc1}$	S_1-S_4	$+ V_{dc}$	$+ V_{dc}$
7	0	S_1-S_2	0	0
8	$- V_{dc1}$	S_2-S_3	$- V_{dc}$	$- V_{dc}$
9	$- V_{dc2}$	S_4-S_5	$- V_{dc}$	$- 2V_{dc}$
10	$- V_{dc3}$	S_6-S_7	$- V_{dc}$	$- 3V_{dc}$
11	$- (V_{dc1}+V_{dc2})$	S_2-S_5	$- 2V_{dc}$	$- 4V_{dc}$
12	$- (V_{dc2}+V_{dc3})$	S_4-S_7	$- 2V_{dc}$	$- 5V_{dc}$
13	$- (V_{dc1}+V_{dc2}+V_{dc3})$	S_2-S_7	$- 3V_{dc}$	$- 6V_{dc}$

2.4.9 Packed U structure based RSC-MLIs

The packed U or ladder based topologies are modular with uni-directional devices connected on either sides of dc sources. The switches are connected such that the topology can conduct and block in both ways. These configurations do not include any level or polarity generators. They can generate output voltage for subtractive and additive combinations of dc voltages. Based on the connection of the switches and dc sources, there are two popular RSC-MLIs, which are described below.

2.4.9.1 Switched dc-sources (SDS) based RSC-MLI

In literature, this topology is introduced as switched dc sources (SDS) or cross connected sources (CCS) [167-169]. If *n* equal dc sources connected in dc link, then this structure requires 2(*n*+1) uni-directional switching devices and produce (2*n*+1) levels in the output voltage. Structure of SDS with three dc sources and eight uni-directional devices is given in Fig. 2.15 and it's possible switching states with equal and unequal dc voltage sources generates seven-levels and thirteen in output phase-voltage as given in Table 2.14.

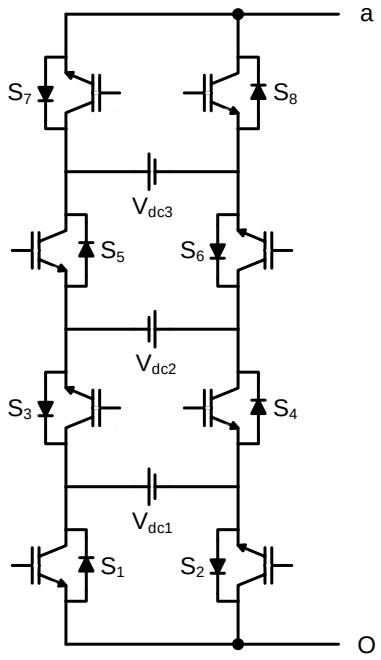


Fig. 2.15: Switched dc sources (SDS) based RSC-MLI topology.

From Table 2.14, it is observed that this RSC-MLI have multiple switching combinations for generating same voltage level. However, this topology generates uneven blocking voltages across switches and difficult to deliver equal power from dc sources. In Fig. 2.15, for switches S_1, S_2, S_7 and S_8 the blocking voltage is V_{dc} and whereas for switches S_3, S_4, S_5 and S_6 it is $2V_{dc}$.

Table 2.14: Switching states of SDS RSC-MLI.

Num. of states	Voltage combinations (V_{dc1}, V_{dc2}, V_{dc3})	Switches in conduction	Output voltage	
			Symmetrical	Asymmetrical
			Seven-level $V_{dc1} = V_{dc2} = V_{dc3} = V_{dc}$	Thirteen-level $V_{dc1} = V_{dc}$; $V_{dc2} = 3V_{dc}$; $V_{dc3} = 2V_{dc}$
1	$V_{dc1}+V_{dc2}+V_{dc3}$	S_2-S_3-S_6-S_7	$+3V_{dc}$	$+6V_{dc}$
2	$V_{dc2}+V_{dc3}$	S_1-S_3-S_6-S_7	$+2V_{dc}$	$+5V_{dc}$
3	$V_{dc1}+V_{dc2}$	S_2-S_3-S_6-S_8	$+2V_{dc}$	$+4V_{dc}$
4	V_{dc2}	S_1-S_3-S_6-S_8	$+V_{dc}$	$+3V_{dc}$
5	V_{dc3}	S_2-S_4-S_6-S_7	$+V_{dc}$	$+2V_{dc}$
6	V_{dc1}	S_2-S_3-S_5-S_7	$+V_{dc}$	$+V_{dc}$
7	$V_{dc3}-V_{dc1}$	S_1-S_4-S_6-S_7	0	$+V_{dc}$
8	0	S_1-S_3-S_5-S_7	0	0
		S_2-S_4-S_6-S_8		
10	$V_{dc1}-V_{dc3}$	S_2-S_3-S_5-S_8	0	$-V_{dc}$
11	V_{dc1}	S_1-S_4-S_6-S_8	$-V_{dc}$	$-V_{dc}$
12	V_{dc3}	S_2-S_4-S_5-S_7	$-V_{dc}$	$-2V_{dc}$
13	V_{dc2}	S_1-S_3-S_5-S_8	$-V_{dc}$	$-3V_{dc}$
14	$V_{dc1}+V_{dc2}$	S_1-S_4-S_5-S_7	$-2V_{dc}$	$-4V_{dc}$
15	$V_{dc2}+V_{dc3}$	S_2-S_4-S_5-S_8	$-2V_{dc}$	$-5V_{dc}$
16	$V_{dc1}+V_{dc2}+V_{dc3}$	S_2-S_3-S_6-S_7	$-3V_{dc}$	$-6V_{dc}$

2.4.9.2 Packed U-cell (PUC) structure based RSC-MLI

Topological structure of packed U-cell (PUC) based RSC-MLI is similar to SDS as described above, though this topology contains a few changes in arrangement of dc link voltage ratios and switches. Topological structure of PUC with three dc voltage sources is presented in Fig. 2.16 and it's possible switching states are given in Table 2.15 [65, 170]. This topology may suffer from unequal utilization of input dc sources. Table 2.15 confirms that PUC topology generates voltage levels for both additive and subtractive arrangements of dc links. Nevertheless by using equal dc voltage sources, the switching operation cannot generate more than three levels in the output phase-voltage. This is due to the consecutive additive and subtractive combination of dc voltages in any switching path as shown in Table 2.15. Thus, with any number of equal dc voltage sources, symmetric topology generate only three-levels in the output voltage changing in magnitude from V_{dc} to $-V_{dc}$. Hence, PUC topology is beneficial with unequal dc sources. Nevertheless, the maximum output voltage always lesser than the total input dc voltage. For example, consider the voltage sources as $V_{dc1} = V_{dc}$, $V_{dc2} = 3V_{dc}$ and $V_{dc3} = 6V_{dc}$ in Fig. 2.16 generates thirteen-levels in output voltage, with magnitudes varying from $+6V_{dc}$ to $-6V_{dc}$ as shown in Table 2.15. Even though the total input dc link voltage is $10V_{dc}$, but the peak value of output voltage (in phase) is $6V_{dc}$. Hence, this topology operates in buck-mode.

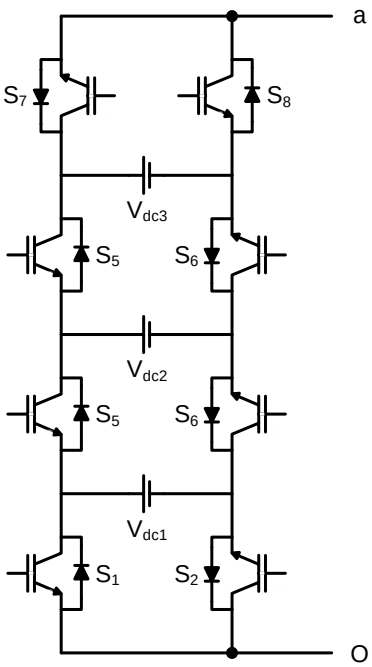


Fig. 2.16: Structure of PUC based RSC-MLI.

Table 2.15: Switching operation of PUC RSC-MLI topology.

Num. of states	**Voltage combinations (V_{dc1}, V_{dc2}, V_{dc3})**	**Switches in conduction**	**Output voltage**	
			Symmetrical	**Asymmetrical**
			$V_{dc1} = V_{dc2} = V_{dc3} = V_{dc}$	**$V_{dc1} = V_{dc}$; $V_{dc2} = 3V_{dc}$; $V_{dc3} = 6V_{dc}$**
1	V_{dc3}	S_2-S_4-S_6-S_7	$+V_{dc}$	$+6V_{dc}$
2	$-V_{dc1}+V_{dc3}$	S_1-S_4-S_6-S_7	0	$+5V_{dc}$
3	$V_{dc1}-V_{dc2}+V_{dc3}$	S_2-S_3-S_6-S_7	$+V_{dc}$	$+4V_{dc}$
4	V_{dc2}	S_2-S_4-S_5-S_7	$+V_{dc}$	$+3V_{dc}$
5	$-V_{dc2} + V_{dc3}$	S_1-S_3-S_6-S_7	0	$+3V_{dc}$
6	$-V_{dc1}+V_{dc2}$	S_1-S_4-S_5-S_7	0	$+2V_{dc}$
7	V_{dc1}	S_2-S_3-S_5-S_7	$+V_{dc}$	$+V_{dc}$
8	0	S_1-S_3-S_5-S_7 (or) S_2-S_4-S_6-S_8	0	0
9	$-V_{dc1}$	S_1-S_4-S_6-S_8	$-V_{dc}$	$-V_{dc}$
10	$V_{dc1}-V_{dc2}$	S_2-S_3-S_6-S_8	0	$-2V_{dc}$
11	$-V_{dc2}$	S_1-S_3-S_6-S_8	$-V_{dc}$	$-3V_{dc}$
12	$V_{dc2}-V_{dc3}$	S_2-S_4-S_5-S_8	0	$-3V_{dc}$
13	$-V_{dc1}+V_{dc2}-V_{dc3}$	S_1-S_4-S_5-S_8	$-V_{dc}$	$-4V_{dc}$
14	$V_{dc1}-V_{dc3}$	S_2-S_3-S_5-S_8	0	$-5V_{dc}$
15	$-V_{dc3}$	S_1-S_3-S_5-S_8	$-V_{dc}$	$-6V_{dc}$

2.4.10 Unit based RSC-MLIs

Few researchers introduced several new MLIs with fixed topological structure. Each unit/modules of these inverter acts as an MLI itself and generate a specific number of voltage levels such as five, seven, nine and thirteen-levels. Moreover, to develop the MLI to higher levels, these novel modules are connected in systematic arrangement such as series, parallel or cascade. Hence, unit based RSC-MLIs can generate only fixed number of output voltage levels. For generating particular range of voltage levels, these topologies offer significant reduction in device count when compared to other RSC-MLI topologies. Few of such MLIs are: Basic unit, envelope type (E-type), square T-type, and cascaded MLI (CMLI). In this thesis, these classification of RSC-MLIs is named as unit based RSC-MLIs. The topological structure, switching operation, merits, demerits, and applications of this unit based RSC-MLIs are presented below.

2.4.10.1 Basic unit RSC-MLI

Basic unit RSC-MLI is introduced by Ebrahim Babaei in 2015 [171]. This RSC-MLI comprises of separate level and polarity generators. The structure of this MLI is presented in Fig. 2.17. The arrangement of level generator involves single-cell and three-cell structure as shown in Fig. 2.17.

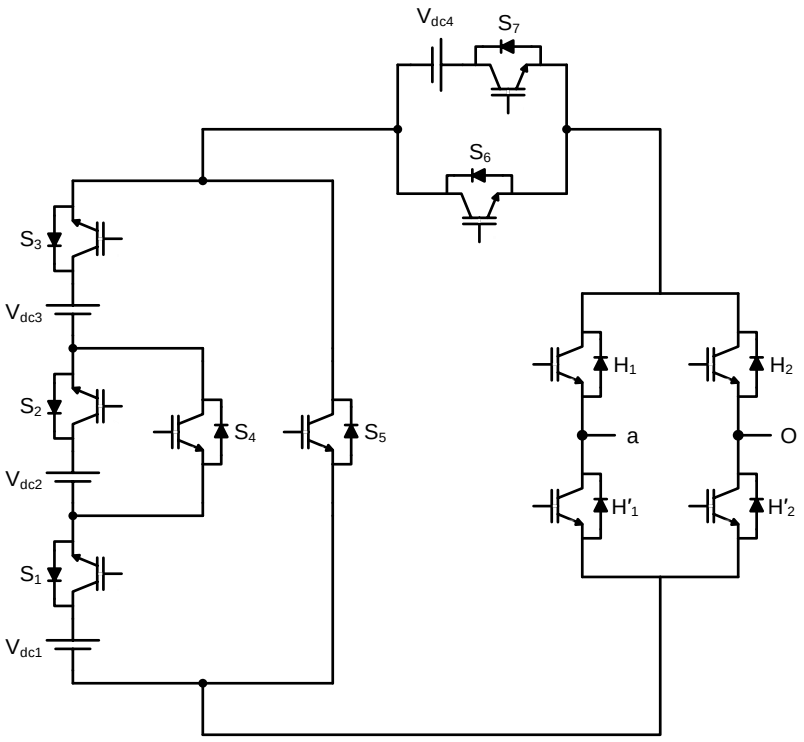


Fig. 2.17: Nine-level basic unit RSC-MLI topology.

Three cell structure consists of three input dc voltage sources and five switches. Single cell structure involves one voltage source and two switches. The objective of single-cell is to generate the voltage levels (i.e., missing levels in phase-voltage) which are not generated by three-cell

structure. By using equal dc voltage sources, level generator can produce unipolar voltage with five-levels as given in Table 2.16. The polarity generator converts this five-level unipolar voltage to nine-level bipolar.

From Table 2.16, it is observed that, this MLI contains inadequate switching redundancies and have uneven blocking voltages across the devices. To develop this RSC-MLI for generating higher voltage levels, multiple basic units (with separate level and polarity generators in each module) are in cascade connection. Further, higher number of voltage levels with significant decrease in device count can be achieved by connecting multiple three-cell structures in series along with common polarity generator as presented in Fig. 2.18. Cascaded basic unit RSC-MLI shown in Fig. 2.18 with identical voltage sources have switching redundancies and provide equal power share among the cascaded units.

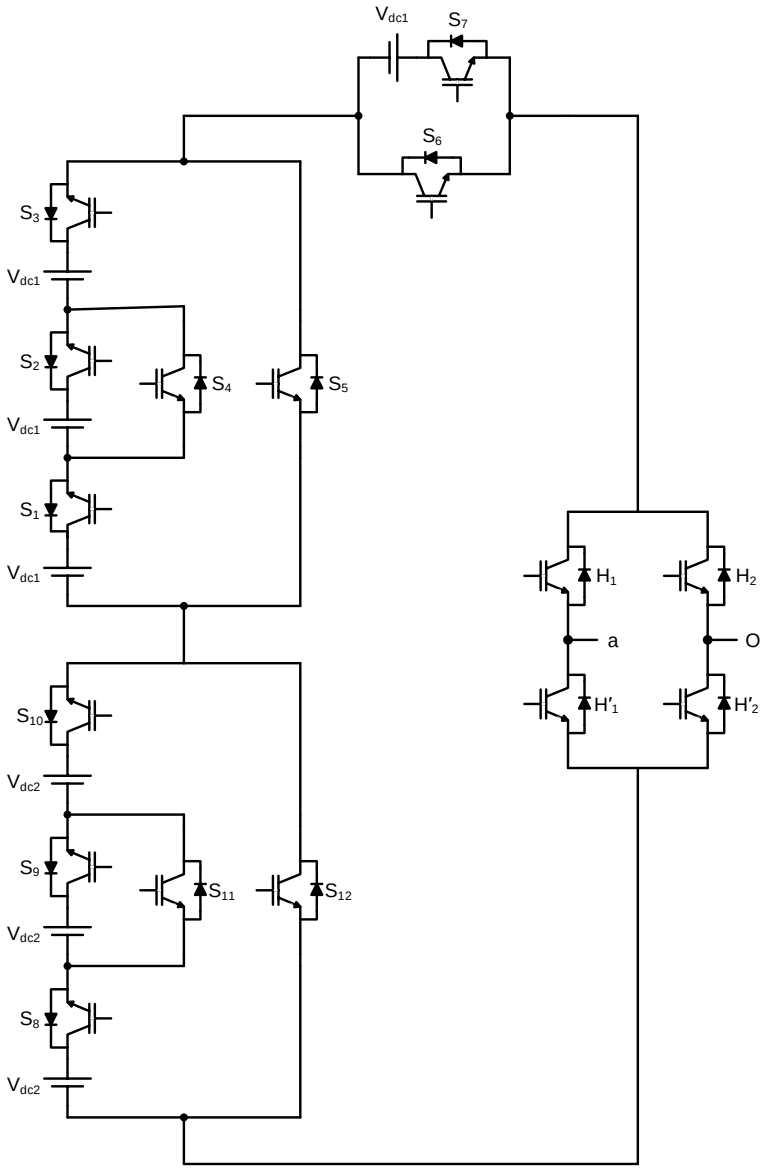


Fig. 2.18: Extension of basic unit RSC-MLI to higher levels.

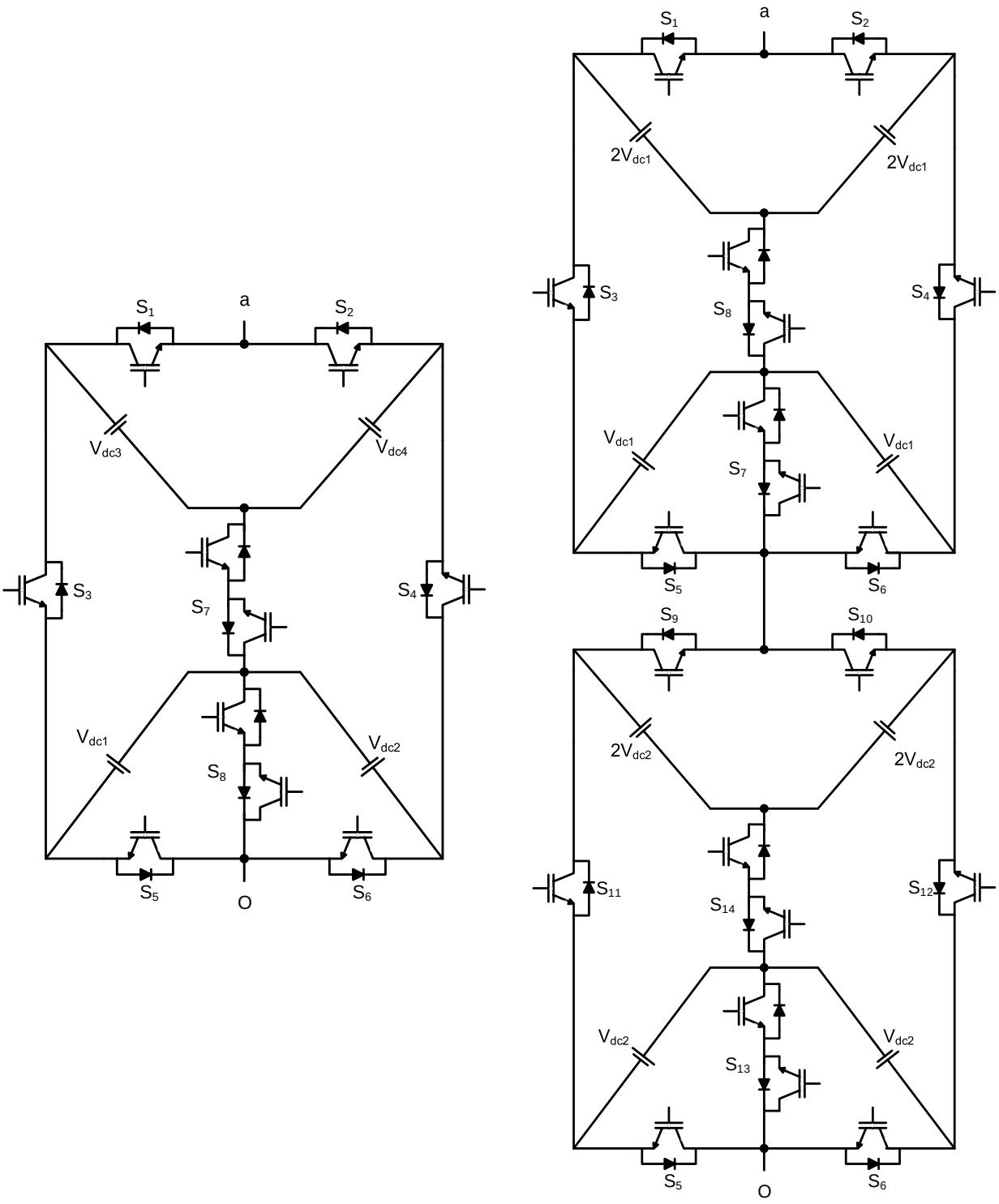
Table 2.16: Switching states of basic unit RSC-MLI.

Num. of states	Voltage combinations	Devices in conduction	Output voltage $V_{dc1} = V_{dc2} = V_{dc3} = V_{dc}$
1	$V_{dc1}+V_{dc2}+V_{dc3}+V_{dc4}$	S_1-S_2-S_3-S_7-H_1-H_2'	$+4V_{dc}$
2	$V_{dc1}+V_{dc3}+V_{dc4}$	S_1-S_4-S_3-S_7-H_1-H_2'	$+3V_{dc}$
3	$V_{dc1}+V_{dc2}+V_{dc3}$	S_1-S_2-S_3-S_6-H_1-H_2'	$+3V_{dc}$
4	$V_{dc1}+V_{dc3}$	S_1-S_4-S_3-S_6-H_1-H_2'	$+2V_{dc}$
5	V_{dc4}	S_5-S_7-H_1-H_2'	$+V_{dc}$
6	0	S_5-S_6-H_1-H_2' (or) S_5-S_6-H_2-H_1'	0

2.4.10.2 Envelope type (E-type) RSC-MLI

Envelope-type (E-type) configuration is an asymmetrical MLI reported by Emad Samadaei in 2017 [150]. Topological structure of an E-type unit is shown in Fig. 2.19(a). This RSC-MLI is developed for generating higher voltage levels by involving multiple E-type modules in series connection as shown in Fig. 2.19(b) and this structure does not include any separate level or polarity generator.

Each E-type module have a fixed topological arrangement and require four dc voltage sources with voltage ratio of 1: 2, six uni-directional and two bi-directional devices to generate thirteen-levels in the output phase-voltage. Hence, each E-type module operates as a thirteen-level inverter itself and its corresponding switching operation is given in Table 2.17. This topology has inadequate switching redundancies and generates unequal blocking voltages across the switches. With *n* identical E-type modules in series, this MLI comprises of 4*n* input dc sources, 2*n* bi-directional and 6*n* uni-directional switching devices, and generates (12*n*+1) levels in output phase-voltage.



(a) Each E-type unit (b) Connecting two E-type units

Fig. 2.19: Topological structure of E-type RSC-MLI.

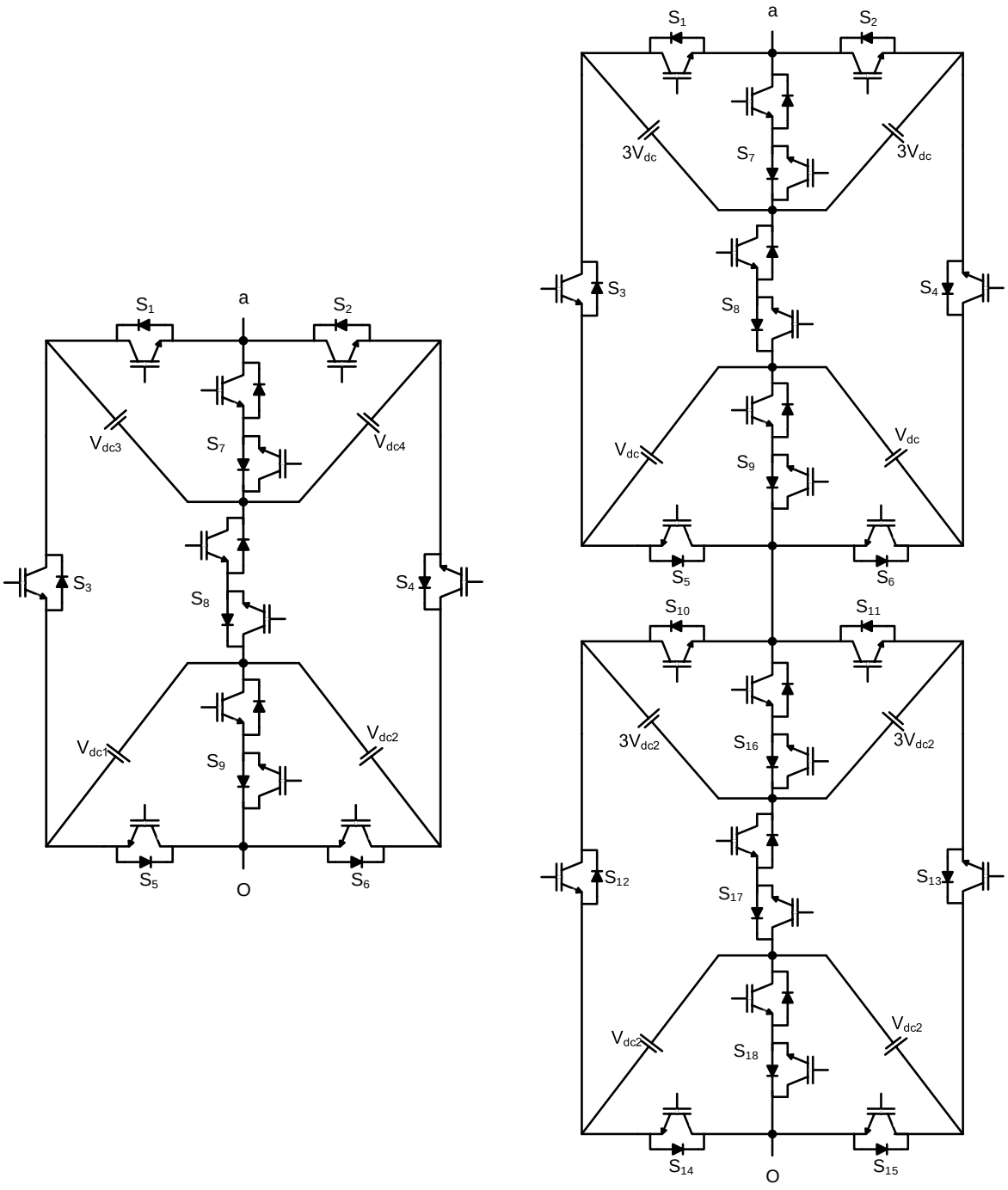
Table 2.17: Switching states in a single unit of E-type RSC-MLI.

Num. of states	Voltage combinations	Devices in conduction	Output voltage $V_{dc1}=V_{dc2}=V_{dc}$ $V_{dc3}=V_{dc4}=2V_{dc}$
1	$V_{dc1}+V_{dc2}+V_{dc3}+V_{dc4}$	S_5-S_4-S_1	$+6V_{dc}$
2	$V_{dc2}+V_{dc3}+V_{dc4}$	S_8-S_4-S_1	$+5V_{dc}$
3	$V_{dc3}+V_{dc4}$	S_6-S_4-S_1	$+4V_{dc}$
4	$V_{dc1}+V_{dc3}$	S_5-S_7-S_1	$+3V_{dc}$
5	$V_{dc1}+V_{dc2}$	S_5-S_4-S_2	$+2V_{dc}$
6	V_{dc3}	S_8-S_7-S_1	$+2V_{dc}$
7	V_{dc2}	S_8-S_4-S_2	$+V_{dc}$
8	$V_{dc3}-V_{dc2}$	S_6-S_7-S_1	$+V_{dc}$
9	0	S_6-S_4-S_2 (or) S_5-S_3-S_1	0
10	$V_{dc4}-V_{dc1}$	S_5-S_7-S_2	$-V_{dc}$
11	V_{dc1}	S_8-S_3-S_1	$-V_{dc}$
12	$V_{dc1}+V_{dc2}$	S_6-S_3-S_1	$-2V_{dc}$
13	V_{dc4}	S_8-S_7-S_2	$-2V_{dc}$
14	$V_{dc2}+V_{dc4}$	S_6-S_7-S_2	$-3V_{dc}$
15	$V_{dc3}+V_{dc4}$	S_5-S_3-S_2	$-4V_{dc}$
16	$V_{dc1}+V_{dc3}+V_{dc4}$	S_8-S_3-S_2	$-5V_{dc}$
17	$V_{dc1}+V_{dc2}+V_{dc3}+V_{dc4}$	S_6-S_3-S_2	$-6V_{dc}$

2.4.10.3 Square T-type (ST-type) RSC-MLI

The basic unit of square T-Type (ST-type) RSC-MLI shown in Fig. 2.20(a) and is motivated from E-type basic unit. The structure of ST-type consists of three bi-directional and six uni-directional switching devices, four dc voltage sources with 1: 3 voltage ratio and generates seventeen-levels in output voltage. Hence each basic ST-type module operates as a seventeen-level MLI by itself [151]. The possible switching states of ST-Type module of Fig. 2.20(a) is given in Table 2.18.

Similar to E-type, the structure of this configuration is modular and increases to higher levels in output voltage by involving multiple identical basic units in series as shown in Fig. 2.20(b). With *n* ST-type modules connecting in series, this topology requires 6*n* uni-directional and 3*n* bi-directional switching devices, 4*n* dc voltage sources, and generate (16*n*+1) levels in output phase-voltage. Nevertheless, this MLI have the similar demerits of E-type topology such as unequal power sharing among the input dc voltage sources and unequal blocking voltages across the switches.



(a) Square T-type unit (b) Series connection of two ST-type units

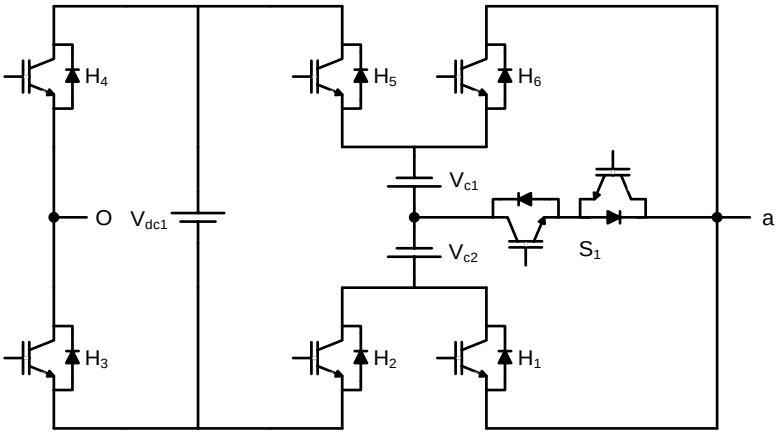
Fig. 2.20: Square T-type (ST-Type) RSC-MLI.

Table 2.18: Switching operation of Square T-type (ST-Type) module.

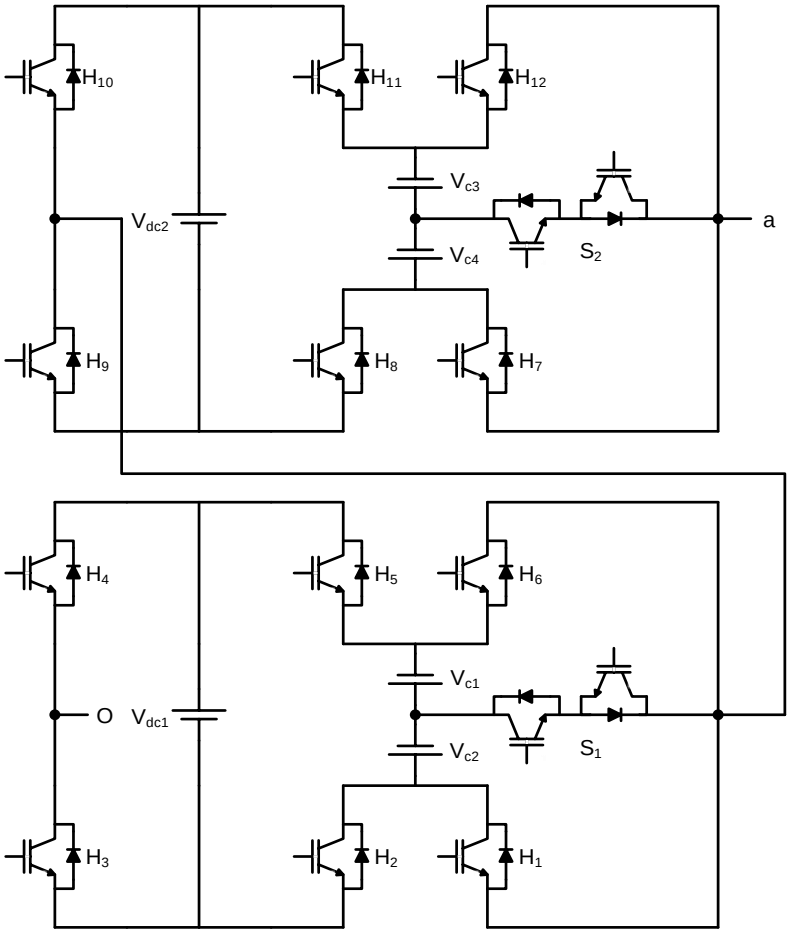
Num. of states	**Voltage combinations**	**Devices in conduction**	**Output voltage** $\mathbf{V_{dc1} = V_{dc2} = V_{dc}}$ $\mathbf{V_{dc3} = V_{dc4} = 3V_{dc}}$
1	$V_{dc1}+V_{dc2}+V_{dc3}+V_{dc4}$	S_5-S_4-S_1	$+8V_{dc}$
2	$V_{dc1}+V_{dc3}+V_{dc4}$	S_5-S_4-S_7	$+7V_{dc}$
3	$V_{dc1}+V_{dc2}$	S_5-S_4-S_2	$+6V_{dc}$
4	$V_{dc2}+V_{dc3}+V_{dc4}$	S_9-S_4-S_1	$+5V_{dc}$
5	$V_{dc2}+V_{dc4}$	S_9-S_4-S_7	$+4V_{dc}$
6	V_{dc2}	S_9-S_4-S_2	$+3V_{dc}$
7	$V_{dc3}+V_{dc4}$	S_6-S_4-S_1	$+2V_{dc}$
8	V_{dc3}	S_9-S_8-S_1	$+V_{dc}$
9	0	S_5-S_3-S_1 (or) S_6-S_4-S_2	0
10	V_{dc4}	S_9-S_8-S_2	$-V_{dc}$
11	$V_{dc3}+V_{dc4}$	S_5-S_3-S_2	$-2V_{dc}$
12	V_{dc1}	S_9-S_3-S_1	$-V_{dc}$
13	$V_{dc1}+V_{dc3}$	S_9-S_3-S_7	$-4V_{dc}$
14	$V_{dc1}+V_{dc3}+V_{dc4}$	S_9-S_3-S_2	$-5V_{dc}$
15	$V_{dc1}+V_{dc2}$	S_6-S_3-S_1	$-6V_{dc}$
16	$V_{dc1}+V_{dc2}+V_{dc3}$	S_6-S_3-S_7	$-7V_{dc}$
17	$V_{dc1}+V_{dc2}+V_{dc3}+V_{dc4}$	S_6-S_3-S_2	$-8V_{dc}$

2.4.10.4 Cascaded RSC-MLI: Topology – I

This RSC-MLI is introduced by Charles Ikechukwu Odeh in 2015 [173]. Basic unit of this topology is given in Fig. 2.21(a) and operates as a nine-level inverter itself. Further, extension of this structure using multiple modules connected in cascade for generating higher number of voltage levels is presented in Fig. 2.21(b). The structure of each module of this topology shown in Fig. 2.21(a) is identical to the Topology-I of hybrid T-type configuration. Nevertheless, the structure of this configuration includes only stiff sources in dc-link. Further, this configuration is only suitable for operating with asymmetrical voltage ratios. In each basic unit includes one bi-directional and six uni-directional switching devices, three dc sources (V_{dc1}, V_{c1} and V_{c2}). In any unit, V_{c1} and V_{c2} are arranged to form a split voltage dc source structure. The voltage of these split dc sources (V_{c1} and V_{c2}) are equal and twice of V_{dc1}. This configuration produces unequal device blocking voltages and operates with limited switching redundancies.



(a) Basic unit



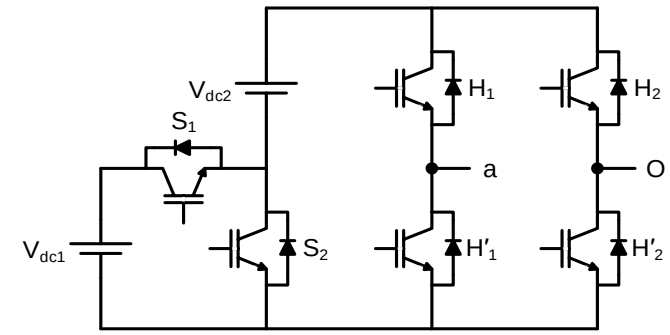
(b) Cascading two units

Fig. 2.21: Cascaded RSC-MLI Topology – I.

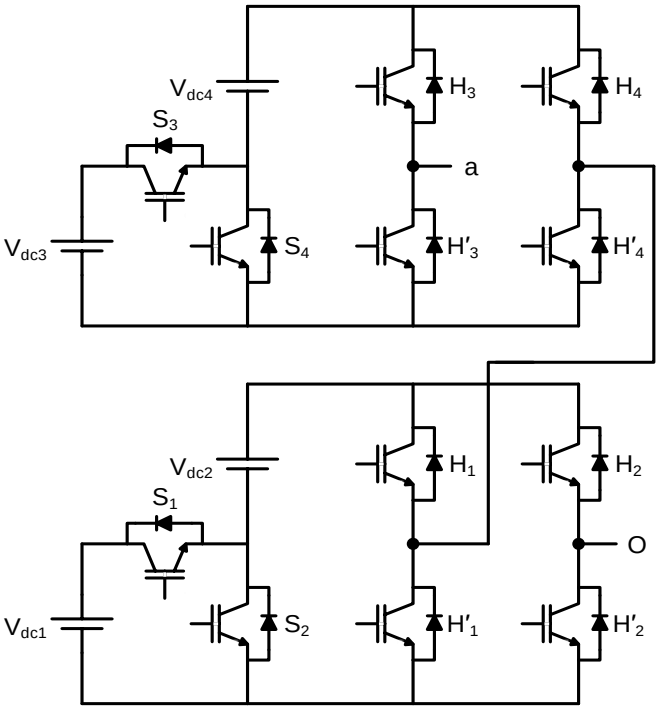
2.4.10.5 Cascaded RSC-MLI: Topology – II

This topology is also proposed by Charles Ikechukwu Odeh [172]. Each unit of this structure generates five-levels in output voltage and acts as an inverter itself by including two equal dc voltage sources and six uni-directional switching devices. The topological configuration is given in Fig. 2.22. The structure of basic unit of this topology is depicted in Fig. 2.22(a) and its

possible switching states are given in Table 2.19. This topology operates with uneven blocking voltages across the switching devices. For generating higher levels, multiple basic units are connected in cascade as shown in Fig. 2.22(b). This cascade structure operates with unequal dc voltage sources as well. The cascade connection of two basic units shown in Fig. 2.22(b), generates nine-levels in output voltage. If *n* similar modules are connected in cascade, then Fig. 2.22(b) needs 2*n* dc voltage sources and 6*n* uni-directional devices, and produce (4*n*+1) output voltage levels.



(a) Basic units



(b) Cascading two basic units

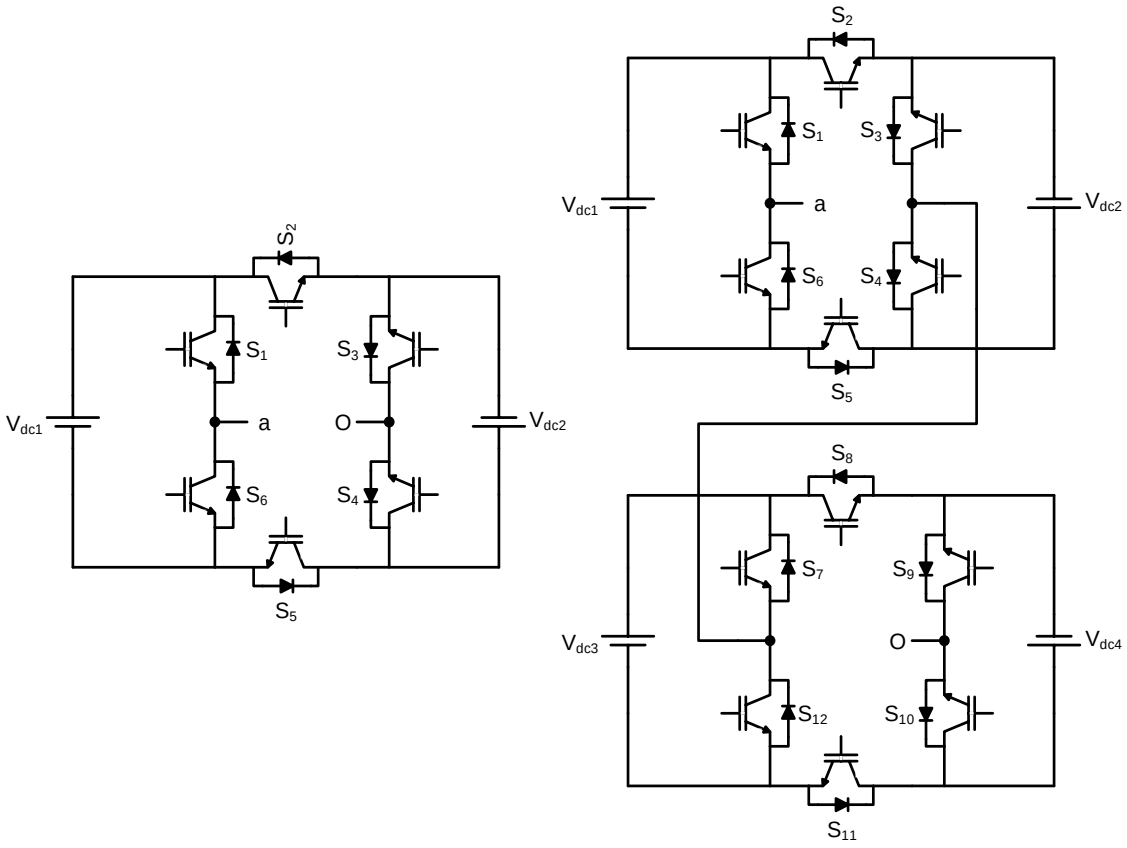
Fig. 2.22: Cascaded RSC-MLI Topology – II.

Table 2.19: Switching states of five-level cascaded RSC-MLI toplogy – II.

Num. of states	Voltage combinations	Devices in conduction	Output voltage $V_{dc1} = V_{dc2} = V_{dc}$
1	$V_{dc1}+V_{dc2}$	S_1-H_1-H_2'	$+2V_{dc}$
2	V_{dc2}	S_2-H_1-H_2'	$+V_{dc}$
3	0	H_1-H_2 (or) H_1'-H_2	0
4	$-V_{dc2}$	S_2-H_2-H_1'	$-V_{dc}$
5	$-(V_{dc1}+V_{dc2})$	S_1-H_2-H_1'	$-2V_{dc}$

2.4.10.6 Cascaded RSC-MLI with hexagonal switched cell (HSC)

This HSC based RSC-MLI topology is designed by E. Babaei in 2014 [135, 136]. The topological structure of this configuration is given in Fig. 2.23. Structural arrangement of basic module of this MLI is given in Fig. 2.23(a) and its cascade connection of two basic units is given in Fig. 2.23(b). Each basic unit of this topology have six uni-directional switching devices and two input dc voltage sources as described in Section 2.4.7.1. Each HSC module operates with equal and unequal voltage sources and generates the voltage levels for additive combinations of the dc voltage sources. With symmetrical voltage ratios, each unit of this cascaded topology presented in Fig. 2.23(a) acts as five-level MLI and it's possible switching states are given in Table 2.20. This topology have uneven blocking voltages across the switches. In Fig. 2.23(a) the blocking voltage appears across switches S_5 and S_6 is (V_{dc1}+V_{dc2}); S_3 and S_4 is V_{dc2}; S_1 and S_2 is V_{dc1}. For generating higher levels, this topology can be extended by cascading multiple basic HSC as presented in Fig. 2.23(b). By using n HSC modules in cascade, the symmetrical topology requires 2n dc sources and 6n uni-directional devices, and generate (4n+1) levels in output voltage, with levels varying from $-2nV_{dc}$ to $+2nV_{dc}$.



(a) Basic unit (b) Cascading two basic units

Fig. 2.23: Hexagonal switched cell (HSC) based RSC-MLI.

Table 2.20: Switching operation of basic HSC based RSC-MLI.

Num. of states	**Voltage combinations**	**Devices in conduction**	**Output voltage $V_{dc1} = V_{dc2} = V_{dc}$**
1	$V_{dc1}+V_{dc2}$	H_3-H_5-H_1	$+2V_{dc}$
2	V_{dc2}	H_5-H_6-H_3	$+V_{dc}$
3	V_{dc1}	H_1-H_4-H_5	$+V_{dc}$
4	0	H_1-H_2-H_3 (or) H_4-H_5-H_6	0
5	V_{dc1}	H_6-H_2-H_3	$-V_{dc}$
6	V_{dc2}	H_1-H_2-H_4	$-V_{dc}$
7	$V_{dc1}+V_{dc2}$	H_4-H_2-H_6	$-2V_{dc}$

2.4.11 Three-phase topologies

In above described RSC-MLI configurations, each phase is individually operated in such a way that the generated output voltage of each phase does not influence the output of other phase. However, in order to achieve significant saving in device count, three-phase RSC-MLIs are reported. The operation of these RSC-MLI is dependent on other phases as analogous to three-phase two-level inverter. The switching devices of these three-phase configurations should be properly operated such that the pole-voltage creates the required number of levels in line-voltage.

Basically, these three-phase configurations consist of a two-level three-phase inverter with few additional devices between input dc link and three-leg six switch inverter. The arrangement of dc link and additional switching devices mainly decides the topological structure of these configurations. A three-phase symmetrical dc-link multilevel inverter with reduced number of dc sources is presented in [130]. Popular configurations under this group of RSC-MLIs are described below.

2.4.11.1 Topology – I

A novel three-phase RSC-MLI topology is introduced by Ahmed Salem in 2015 [174]. The structure of this topology is highly modular and higher number of voltage level can be generated by extended modular part of this topology. This configuration involves a two-level inverter with upper switches of each leg connected to dc ink through multiple modular units connected in series. Each modular cell produces an output of either 0 or V_{dc}. Topological structure of this RSC-MLI for generating five-level line-voltage is presented in Fig. 2.24. The possible switching states of this topology to generate three-level pole-voltage is given in Table 2.21. This three-phase topology can be extended for generating higher number of levels is shown in Fig. 2.25, where the topology is given for generating seven-levels in output line-voltage. By using n number of modules, this topology requires $3(2n+2)$ switching devices to generate $(2n+3)$ levels in line-voltage and $(n+2)$ levels in pole-voltage. This topology enables equal utilization of input dc sources but suffers from unequal blocking voltages across devices.

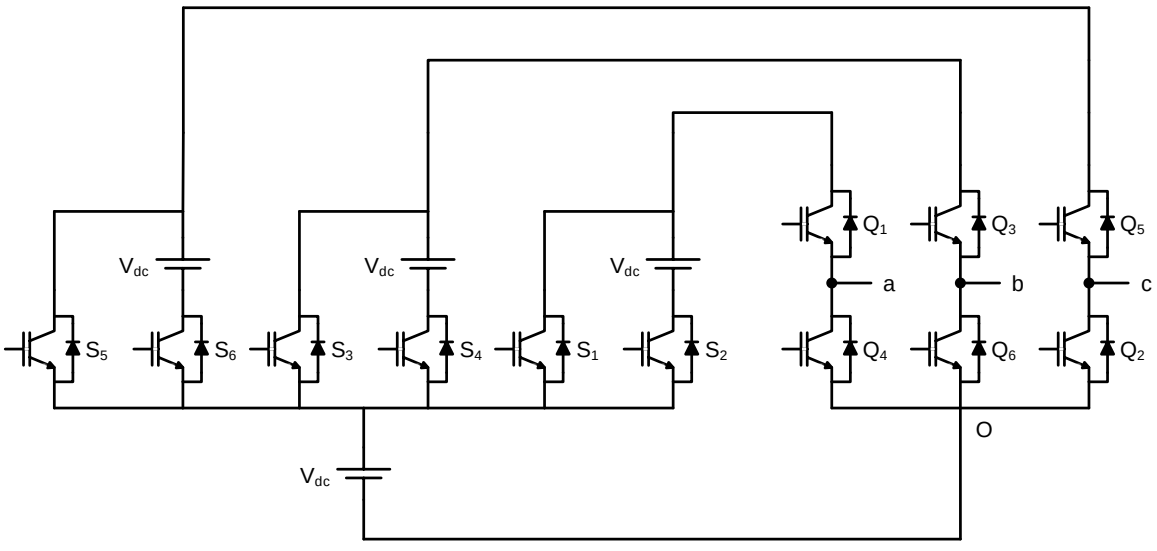


Fig. 2.24: Five-level three-phase RSC-MLI Topology- I.

Table 2.21: Switching operation of Topology- I for three-level pole-voltage.

Num. of states	Switches in conduction				Pole-voltage (V_{ao})
	S_1	S_2	Q_1	Q_2	
1	0	0	0	1	0

2	1	0	1	0	V_{dc}
3	0	1	1	0	$2V_{dc}$

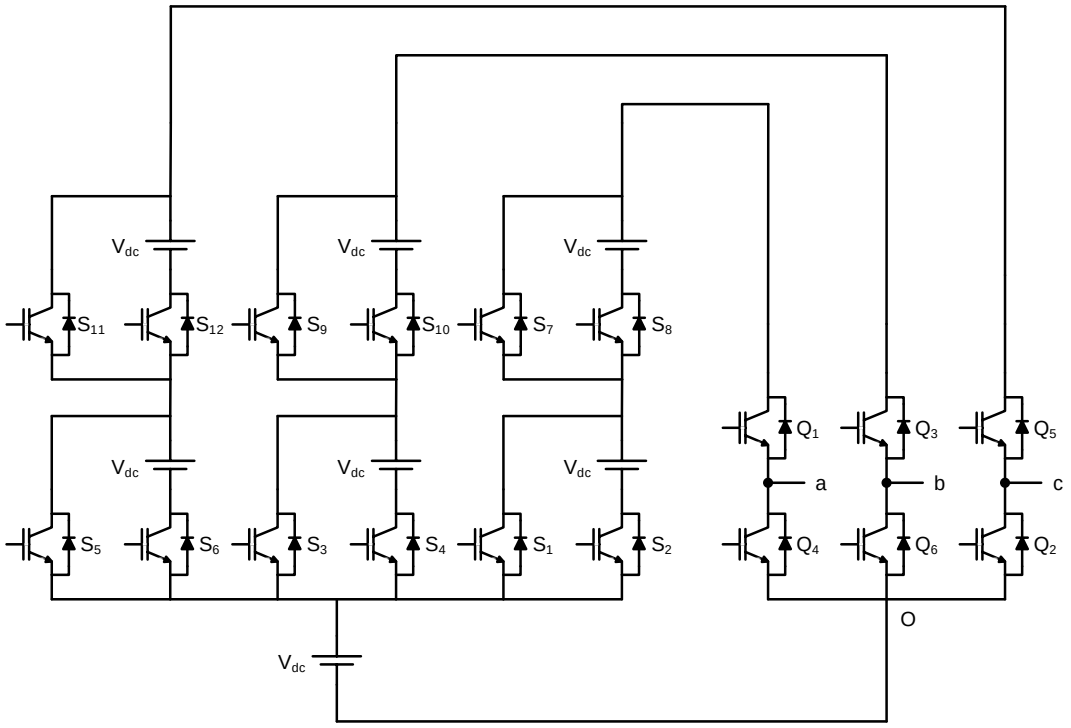


Fig. 2.25: Seven-level three-phase RSC-MLI Topology- I.

2.4.11.2 Topology – II

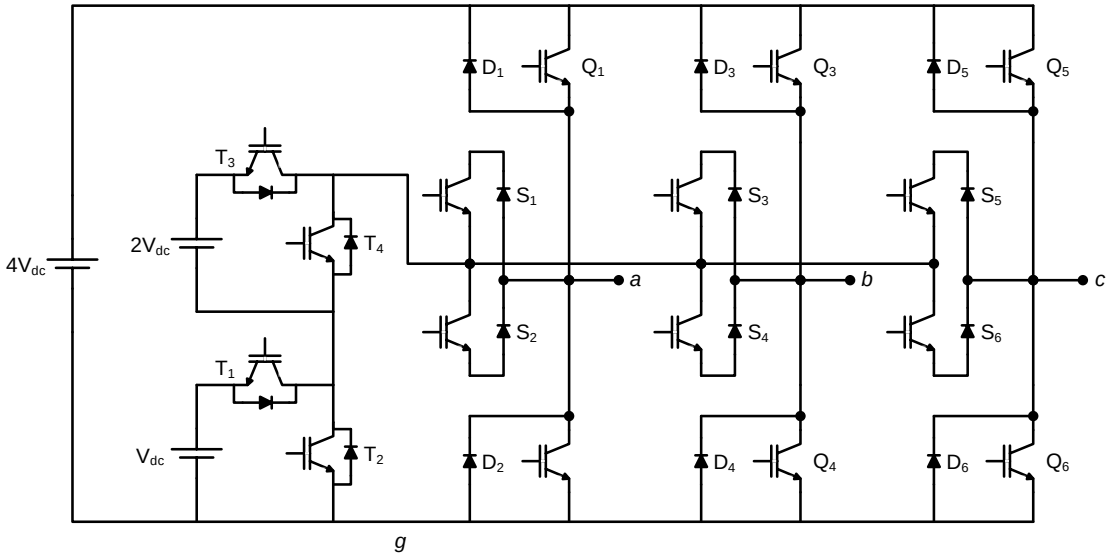
These new three-phase RSC-MLIs are introduced by Ammar Masaoud in 2014 [148, 149]. These topologies consist of a generalized structural arrangement and generate the voltage levels by using both asymmetrical and symmetrical dc voltage sources. Fig. 2.26 and Fig. 2.27 represent these three-phase MLIs for generating five-levels in output pole-voltage. From Fig. 2.26 and Fig. 2.27, it can be observed that, these topologies consist of few similarities in their structural arrangement, which are given below:

- Similarities in dc link: Maximum input dc voltage in all cases is fixed to $4V_{dc}$.
- Each phase-leg arrangement: Each leg of the inverter involves one bi-directional switch (S_1-S_2) and one complimentary uni-directional switch pair (Q_1 and Q_2).

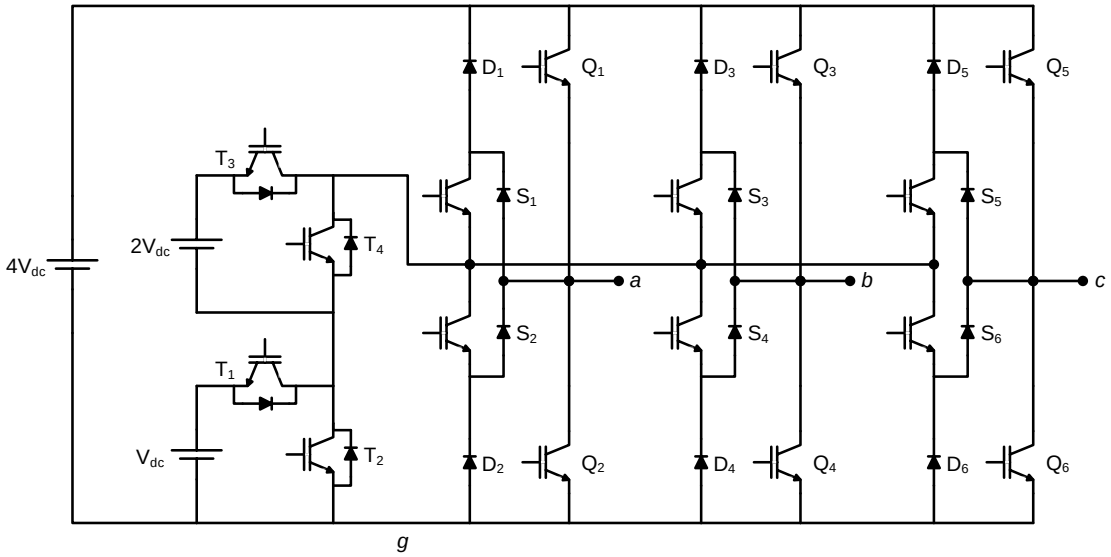
Further, Fig. 2.26(b) and Fig. 2.27(b) consists of similar leg structures, where, higher potential of dc link is connected to switch S_1 through D_1 and lower potential of dc link connected to switch S_2 through D_2. Moreover, all the mid-points of bi-directional switches of three legs are commonly connected to dc link through auxiliary switch. These auxiliary switches are responsible for obtaining multiple input dc voltages and thus form supporting unit for level generation.

In general, the benefit of any three-phase topology is achieved from structure of this supporting module. For the topologies shown in Fig. 2.26(b) and Fig. 2.27(b), the supporting module is designed by using two dc voltage sources and four uni-directional devices, though their

arrangement and position is different in both configurations. In the same way, Fig. 2.26(a) and Fig. 2.27(a), consists of similar leg structures, where the midpoints of bi-directional switches of each phase are commonly connected to input dc link through auxiliary switching devices. This auxiliary structure in both of these MLIs is not similar. However, the auxiliary module arrangement of Fig. 2.26(a) and (b) is same and similarly the auxiliary cell structure of Fig. 2.27(a) and (b) is same. Switching states of these three-phase RSC-MLIs shown in Fig. 2.26 and Fig. 2.27 is given in Table 2.22. It is observed that this switching operation is valid for producing of nine-levels in line-voltage and five-levels in pole-voltage. These topologies have uneven blocking voltages across devices, unequal utilization of input dc sources and limited switching redundancies. The configurations presented in Fig. 2.26(a) and (b) can be increased to higher number by adding additional modules in auxiliary structure [148, 149]. Generalized configuration shown in Fig. 2.26(a) and (b), with n sources (each V_{dc}) in the auxiliary module, then maximum dc link voltage is $(n+1)V_{dc}$ and produce pole-voltage with $(n+2)$ levels.

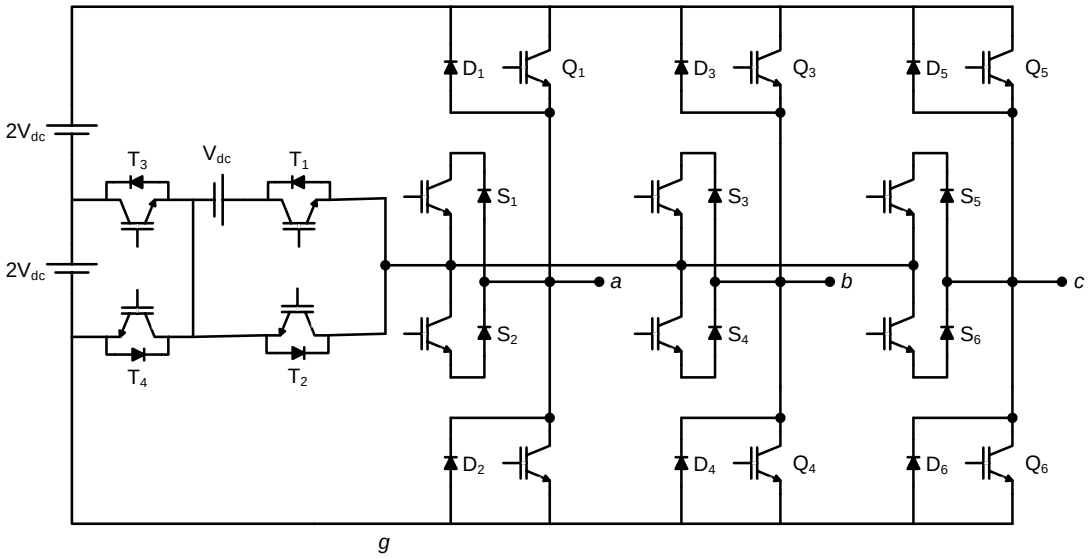


(a) Configuration – 1

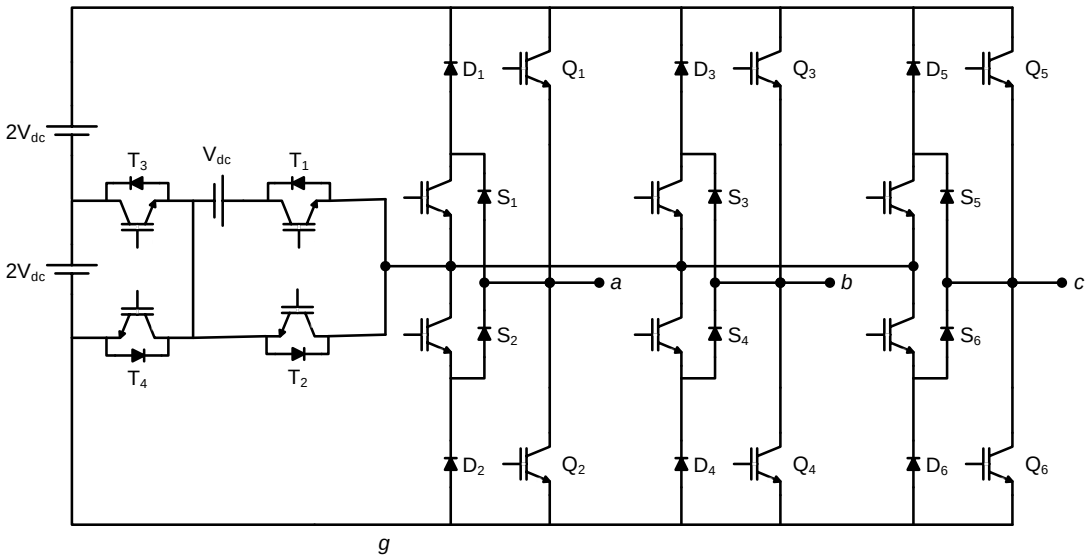


(b) Configuration – 2

Fig. 2.26: Three-phase asymmetrical five-level RSC-MLI configurations of Topology – II.



(a) Configuration – 3



(b) Configuration – 4

Fig. 2.27: Three-phase asymmetrical five-level RSC-MLI configurations of Topology – II.

Table 2.22: Switching states of five-level three-phase RSC-MLIs.

Q_1	S_1	S_2	Q_2	T_1	T_2	T_3	T_4	V_{ag}
1	0	0	0	1	0	1	0	$+4V_{dc}$
0	1	1	0	1	0	1	0	$+3V_{dc}$
0	1	1	0	0	1	1	0	$+2V_{dc}$
0	1	1	0	1	0	0	1	$+V_{dc}$
0	0	0	1	1	0	1	0	0

2.5 Summary

From the above discussions on several RSC-MLIs, the following remarks can be made:

1. Modularity in structure of RSC-MLIs: For generating higher voltage levels in the output voltage, topology can be extended by adding of new modules. This extension of RSC-MLI does not affect the rating of the existing devices and blocking voltage appears across the switches.
2. In HSC and H-bridge based structures, the voltage rating of the devices in HSC and H-bridge are greater than or equal to the total input dc voltage. The basic unit RSC-MLI, T-type, RV, SSPS, MLDCL, SCSS, MLM, improved T-type are few of such RSC-MLIs.
3. The structures of RSC-MLIs with separate level and polarity generators, involves similar switching states for both negative and positive voltage levels. Generally level generators produce the output voltage for additive combinations of input dc voltage sources and does not offer switching operation for subtractive combinations. This restricts the adaption of trinary voltage ratios in dc link voltages. Few of such RSC-MLIs are RV, MLDCL and SSPS.
4. Switching redundancies play an important role in design of the inverter for uniform utilization of input dc sources and reduced control complexity. Thus, inadequate or absence of switching redundancies in RSC-MLIs such as T-type, and E-type topologies, discourages their adaption in grid connected PV applications.
5. Necessity of dc supply: Several RSC-MLI consist the structural arrangement in such a way that a common dc link will be interfaced to all three phases. One of such MLI is three-phase RSC-MLIs. Also few other MLI configurations need non-isolated input dc voltages.

The leading factors for choosing a RSC-MLI is decided by:

- Uniform and unaffected blocking voltages (with increase in number of levels).
  Example: MLDCL, switched capacitor MLIs and SSPS.
- Modular and generalized structural arrangement.
  Example: SCSS, MLDCL, RV and SSPS.
- Significant reduction in device count at high levels
  Example: MLDCL, T-type, E-type, Square E-type and Improved T-type.
- Uniform utilization of dc sources and dc link voltage balancing
  Example: MLDCL and SSPS.
- Fault tolerant operation of the inverter, where a fault unit can be effectively bypassed
  Example: MLDCL

- Simplified topological structure

  Example: SCSS, T-type and MLDCL

Based on the above discussion, MLDCL, SSPS and T-type are well suited for grid connected applications. T-type RSC-MLI offers significant decrease in switch count but lack of switching redundancies, inability to adapting with asymmetrical dc voltage sources, inability to attain uniform power distribution of dc sources, uneven blocking voltages acts as major limitation. Owing to these reasons, T-type is limed to three-levels only [139, 141, 143, 144, 162, 163, 165].

On the other hand, MLDCL and SSPS RSC-MLIs consist of simplified, modular and generalized topological structure with considerable decrease in switch count, multiple switching redundancies, possibility of connecting asymmetric dc sources and simplified switching operation, fault tolerant ability, uniform power distribution, uniform blocking voltages across switches and dc link voltage balancing capability. Due to these key and worthy merits, MLDCL and SSPS had gathered more attention among other RSC-MLIs configurations. Moreover, MLDCL and SSPS serves as an alternate to conversional CHB MLI for applications such as grid connected PV system, active front-end converters, custom power devices, BESS, and HEV. Further, series/parallel operation of SSPS increases the utilization of input dc sources. Therefore in this thesis, to analyze closed-loop implementation of RSC-MLI topologies for supplying power to grid, MLDCL and SSPS RSC-MLI are adapted.

CHAPTER 3: COMPARISON OF 11-LEVEL ASYMMETRIC CHB, SSPS AND MLDCL RSC-MLIs

This chapter discusses about the structure and operation of asymmetric CHB, MLDCL and SSPS RSC-MLI topologies. A comprehensive comparison is carried among these asymmetric topologies in terms of various factors.

3.1 Introduction

The reduced switch count multilevel inverters (RSC-MLI) are the latest trend in power electronic converters due to its reduced switch count and cost. However, a large number of RSC-MLIs not yet reach application level due to the absence of modularity, unequal load-sharing among dc sources and limited switching redundancies. On the other hand, multilevel dc-link (MLDCL) and switched series/parallel sources (SSPS) RSC-MLIs [153, 157] are modular in structure with adequate switching redundancies and offers lesser switching count compared to CHB MLI and other MLIs. The asymmetric source configurations of these RSC-MLIs offers further reduction in switch count and are not yet addressed for closed-loop applications in literature. Therefore in this chapter, a comprehensive comparison among CHB, MLDCL and SSPS RSC-MLI topologies has been carried out for adapting a superior RSC-MLI in grid connected PV systems. For this comparison, 11-level inverters are considered with input dc source voltage in the ratio of 1: 2: 2, as shown in Fig. 3.1.

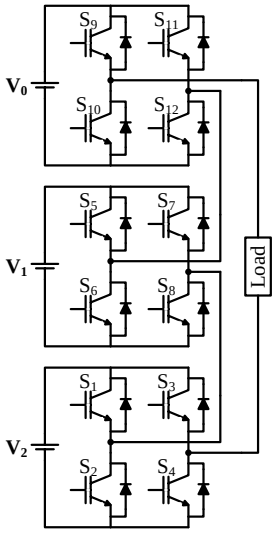
There are topologies such as CHB MLI shown Fig. 3.1(a), the utilization of all the sources at all levels is seldom. These topologies will diminish the energy efficiency of the conversion system as all the sources will not deliver the power except at the highest level in the output voltage. These kinds of converters can hamper the penetration of renewable energy into the existing energy mix, as the energy capacity of the renewable source is undermined. In this connection, this chapter explores the switched series/parallel sources (SSPS) based RSC-MLI [154, 155] that can extract the power from all the sources at most of the levels through series/parallel switching. Even though the MLIs are well researched, the thrust is there in producing number of levels with minimum THD, switch stress and loss minimization. However, the utilization of the dc sources in a fundamental cycle of output voltage is not explored to sufficient extent in the literature. Therefore, in this chapter a new performance indicator is introduced to quantify the utilization of dc sources.

3.2 Asymmetric RSC-MLI topologies

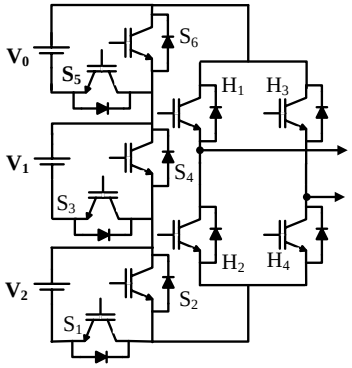
Among the existing RSC-MLI topologies, MLDCL [153, 157] and SSPS [154, 155] MLIs are dominant topologies for control of grid connected applications. These topologies not only

require reduced number of switch count but they are also highly modular in their structure and offer the following structural benefits.

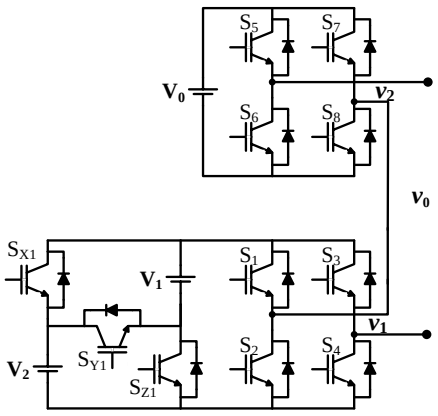
- There is a possibility to connect asymmetrical or unequal rated input sources such as PVs to further reduce switch count.
- The structures of MLDCL and SSPS inverters allow even power distribution between equal rated input sources [65]. Therefore, a single maximum power extraction control method can be applied for multiple equal rated PV sources, thereby reducing the control complexity.
- Due to series/parallel connection of dc voltage sources in SSPS, all input dc sources are utilised in most of the voltage levels.
- Further, the highest rating switches in polarity generator of MLDCL and SSPS inverters in Fig. 3.1(b) and Fig. 3.1(c) are operating at fundamental frequency. This will reduce switching losses.



(a) 11-level asymmetric (V_0: V_1: V_2= 1: 2: 2) CHB MLI



(b) 11-level asymmetric (V_0: V_1: V_2= 1: 2: 2) MLDCL RSC-MLI



(c) 11-level asymmetric (V_0: V_1: V_2= 1: 2: 2) SSPS RSC-MLI

Fig. 3.1: 11-level asymmetric CHB and RSC-MLI topologies.

Owing to these reasons, MLDCL and SSPS RSC-MLIs have the potential to be viable alternative to CHB MLI. To further identify the superiority of SSPS and MLDCL over conventional CHB for injection of controlled power into grid systems, a comprehensive comparison is presented among CHB, MLDCL and SSPS topologies.

3.2.1 Single-phase 11-level asymmetric MLDCL MLI

The per-phase structure of 11-level asymmetric MLDCL topology with 1: 2: 2 dc voltage ratio is shown in Fig. 3.1(b). The structure of this topology is divided into two parts, namely, level generator and polarity generator. The first one is responsible for generation of unipolar voltage levels, while the other one converts this unipolar voltage into bipolar. The level generation part can be formed by cascade connection of half bridge cells. Each half bridge cell consists of an isolated dc voltage source (or PV source) with complementary switch pair and produces an output voltage equal to dc source voltage or zero. On the other hand, the polarity generator consists of an H-bridge with switches operate at fundamental frequency. The operation of MLDCL as an inverter is explained in Section 2.4.1. The switching table of MLDCL RSC-MLI shown in Fig. 3.1(b) to obtain eleven-levels in phase-voltage is given in Table 3.1.

Table 3.1: Switching states and phase-voltage of 11-level asymmetric MLDCL RSC-MLI

Phase-voltage level	**Switches operate in level generator**	**Switches operate in polarity generator**
$+5V_{dc}$	S_1-S_3-S_5	H_1-H_4
$-5V_{dc}$		H_2-H_3
$+4V_{dc}$	S_2-S_3-S_5	H_1-H_4
$-4V_{dc}$		H_2-H_3
$+3V_{dc}$	S_1-S_3-S_6 (or) S_1-S_4-S_5	H_1-H_4
$-3V_{dc}$		H_2-H_3
$+2V_{dc}$	S_2-S_3-S_6 (or) S_2-S_4-S_5	H_1-H_4
$-2V_{dc}$		H_2-H_3
$+V_{dc}$	S_1-S_4-S_6	H_1-H_4
$-V_{dc}$		H_2-H_3
0	----	H_1-H_3 (or) H_2-H_4

From this table, it can be observed that MLDCL have following features.

- Identical switching operation in level generator for obtaining positive and negative voltages levels.
- Voltage stress on the operating devices (level generator) remains same for any number of levels.

- The dc link voltage balance is possible with the presence of adequate switching redundancies.

In this thesis work, the author's main reasons to choose 1: 2: 2 asymmetric sources configurations instead of other asymmetric sources is given below.

- The trinary (1: 3: 3^2…) source based configuration cannot be employed for this MLDCL topology since subtractive combinations of the input dc levels cannot be synthesized and hence some of the levels are not produced in the output voltage.
- A binary (1: 2: 2^2...) or 1: 2: 3… source configurations are possible for MLDCL MLI since all the voltage levels in the output voltage are synthesized. However, as the number of sources increase, the voltage stress appear across the switches in H-bridge of MLDCL MLI becomes too high. Further, redundancies are absent in these type of source configuration since all the sources are with different voltage values. Hence multiple switching operations cannot be existing in order to generate same voltage level. Because of this, control complexity will increase. For example, if the 1: 2: 2^2… and 1: 2: 3… sources based MLDCL MLIs will be used in the PV applications, then for every individual PV sources, there should be a need of a separate MPPT control scheme. Because of this, simultaneous design of the parameters for every controller will become a critical task. Tuning of the gains of the controllers is a challenging task as the number of different rated PV sources increases.
- The proposed PV power extraction control scheme of this thesis work is also effective for any other common asymmetric sources (i.e., 1: 3: 3 or 1: 4: 4 or 1: 5: 5 etc.). However, before selecting any asymmetrical based input sources, it is necessary to observe that whether all the levels in the output voltage will generate from these asymmetric sources or not. Hence, in this case a common asymmetric sources (i.e., 1: 3: 3 or 1: 4: 4 or 1: 5: 5) source based configuration cannot be employed for MLDCL topology since subtractive combinations of the input dc levels cannot be synthesized and hence some of the levels will be missed in the output voltage. Further, these common asymmetric sources create a very high voltage stress across the switches in H-bridge of MLDCL MLI.
- On the other hand, using 1: 2: 2 asymmetric sources satisfied the primary requirement i.e., from this asymmetric topology all the 11-levels in the output voltage can be synthesized as shown in Table 3.1. Further, 1: 2: 2 asymmetric sources based MLDCL MLI has adequate switching redundancies.
- Hence, In this thesis work, a common sliding mode based MPPT controller is implemented to extract maximum power from each group of equal rating PV sources of

three-phase asymmetric MLDCL MLI. So that control complexity is reduced, which is explained in next Chapter of this thesis. Moreover, this topology can produce significantly less THD in output voltage. Even though high-voltage stress appear across the switches in the H-bridge of the chosen 11-level asymmetric MLDCL MLI, however this voltage stress is less when compared to other asymmetric sources such as 1: 2: 2^2.. input dc voltage ratio. Further, with the precise control of SMCs, the PV source voltages of MLDCL are maintained at 1: 2: 2 with very less steady-state difference.

3.2.2 Single-phase 11-level asymmetric SSPS MLI

Among the various RSC-MLI topologies reported so far, SSPS is an efficient topology with self-balancing nature of dc voltages by series/parallel operation of capacitor or dc sources. In general, for any topology, voltage level is obtained by series-connected operation of capacitors or dc voltages sources. However in SSPS topology, different voltage levels can be achieved through series/parallel-connected operation of dc voltages sources, which increases the utilization of dc sources. The considered SSPS RSC-MLI is shown in Fig. 3.1(c). The voltage sources of the upper and lower part of the SSPS inverter are considered as $V_0 = V_{dc}$ and $V_1 = V_2 = 2V_{dc}$ When S_{Y1} is ON, V_1 and V_2 are in series, when S_{X1} and S_{Z1} are ON, V_1 and V_2 are in parallel. The switching operation this topology and corresponding input dc sources connection at every level is given in Table 3.2. This operation will holds good for any number of levels by increasing modules in the lower part of the converter. This 11-level asymmetric MLI has been adapted from [154, 155] and is developed for a three-phase system in this thesis work.

Table 3.2: Switching states and their corresponding dc sources to obtain a particular level in phase-voltage for 11-level asymmetric SSPS MLI with V_0=V and V_1=V_2=2V.

Phase voltage level	Switching path	Connected dc sources
$+5V_{dc}$	S_{y1}-S_1-S_8-S_5-S_4	V_1,V_2,V_0
$+4V_{dc}$	S_{y1}-S_1-S_7-S_5-S_4	V_1,V_2
$+3V_{dc}$	S_{x1}-S_1-S_8-S_5-S_4-S_{z1}	V_1,V_2,V_0
$+2V_{dc}$	S_{x1}-S_1-S_7-S_5-S_4-S_{z1}	V_1,V_2
$+V_{dc}$	S_{x1}-S_1-S_7-S_6-S_4-S_{z1}	V_1,V_2,V_0
0	S_2-S_8-S_6-S_4	0
$-V_{dc}$	S_{z1}-S_2-S_8-S_5-S_3-S_{x1}	V_1,V_2,V_0
$-2V_{dc}$	S_{z1}-S_2-S_8-S_6-S_3-S_{x1}	V_1,V_2
$-3V_{dc}$	S_{Y1}-S_2-S_8-S_5-S_3	V_1,V_2,V_0
$-4V_{dc}$	S_{Y1}-S_2-S_8-S_6-S_3	V_1,V_2
$-5V_{dc}$	S_{Y1}-S_2-S_7-S_6-S_3	V_1,V_2,V_0

In this thesis work, the author's main reasons to choose 1: 2: 2 asymmetric sources based SSPS MLI configuration are same as the reasons of selection of 1: 2: 2 asymmetric MLDCL as discussed above. The concept of generation of voltage levels through series/parallel connected operation of the capacitors or dc voltages sources in SSPS topology encouraged the authors to introduce a new factor called as "utilization factor" of input dc sources of an MLI and it is explained below.

3.3 Comparison among CHB, MLDCL and SSPS RSC-MLIs

A comprehensive comparison among CHB, MLDCL and SSPS RSC-MLI topologies has been carried out in terms of utilization factor (*UF*), switch count, current rating of the dc sources and switches, operating frequencies of switches and total blocking voltage.

3.3.1 Utilization factor of input dc sources

One of the contributions of this thesis work is to identify the RSC-MLI topology which utilizes the available dc sources to the maximum possible extent in a full cycle of output voltage. Even though the MLIs are well researched, the thrust is there in producing number of levels with minimum THD, switch stress and loss minimization. However, the utilization of the dc source in a full cycle of output voltage is not explored to sufficient extent in the literature. Therefore, in this thesis a new performance indicator is introduced in the name of "utilization factor (*UF*)" to quantify the utilization of dc sources.

Consider *N* is number of dc sources, *n* is the number of phase-voltage levels, and *Xj* is the number of dc sources connected in series/parallel to obtain the j^{th} level in phase-voltage, then the *UF* can be defined as:

$$UF = \frac{\text{Sum of the number of voltage sources connected to MLI at each phase voltage level}}{\text{(Total number of phase voltage levels)} \times \text{(Total number of sources of the MLI)}}$$

$$UF = \frac{\sum_{i=1}^{n} X_i}{N \times M} \tag{3.1}$$

Table 3.3 shows the number of dc sources in connection for obtaining a particular level in phase-voltage of the considered CHB, MLDCL and SSPS MLIs, as shown in Fig. 3.1. For example, number of dc sources connected to obtain a voltage level of $+V$ in the CHB and MLDCL is 2, whereas in the SSPS inverter, it is 3. Further, from Table 3.3, it is observed that the number of connected dc sources to CHB and MLDCL are the same at every voltage level. Hence, *UFs* of CHB and MLDCL MLI are equal. Therefore, the *UF*s of dc sources of 11-level considered MLIs of Fig. 3.1 can be calculated using (3.1) and Table 3.3 as.

$$UF_{SSPS} = (3+2+3+2+3+0+3+2+3+2+3)/(11\times 3) = 0.79$$

$$UF_{CHB(or)MLDCL} = (3+2+3+1+2+0+2+1+3+2+3)/(11\times 3) = 0.66$$

From the above calculations it is observed that utilisation factor of input dc sources for SSPS topology is more when compared to conventional CHB MLI and MLDCL MLIs.

Table 3.3: Input dc sources connected to MLI at each phase-voltage level for 11-level asymmetric SSPS and MLDCL (or) CHB MLIs with $V_1 = V_2 = 2V_{dc}$ and $V_0 = V_{dc}$.

Phase voltage level	**No. of Connected dc sources in SSPS**		**No. of Connected dc sources in CHB (or) MLDCL**	
$+5V_{dc}$	V_1, V_2, V_0	(3)	V_1, V_2, V_0	(3)
$+4V_{dc}$	V_1, V_2	(2)	V_1, V_2	(2)
$+3V_{dc}$	V_1, V_2, V_0	(3)	V_1, V_2, V_0	(3)
$+2V_{dc}$	V_1, V_2	(2)	V_2	(1)
$+V_{dc}$	V_1, V_2, V_0	(3)	V_1, V_0	(2)
0	0		0	
$-V_{dc}$	V_1, V_2, V_0	(3)	V_1, V_0	(2)
$-2V_{dc}$	V_1, V_2	(2)	V_1	(1)
$-3V_{dc}$	V_1, V_2, V_0	(3)	V_1, V_2, V_0	(3)
$-4V_{dc}$	V_1, V_2	(2)	V_1, V_2	(2)
$-5V_{dc}$	V_1, V_2, V_0	(3)	V_1, V_2, V_0	(3)

The percentage increase in utilization of dc sources in SSPS MLI with respect to CHB MLI can be calculated as $[(UF_{SSPS} - UF_{CHB})/UF_{CHB}]\times 100$. Therefore from the above calculations, it can be inferred that the utilization of dc voltage sources in SSPS topology is increased by 19.6% when compared with CHB topology. In case for 19 levels, the percentage increase in utilization of dc sources in SSPS topology is 23.7% as compared to same level CHB, as given in Table 3.4.

This specific merit of SSPS is found to be advantageous for various grid connected applications, as it helps in better utilization of PV and other renewable energy based sources. This feature of SSPS is also important as it ensures uniform utilization of dc sources; hence the ageing of sources will be more or less uniform. Therefore, SSPS topology calls for less maintenance and replacement costs when compared with CHB topologies as their non-uniform utilization will call for frequent replacement of one or other sources.

Table 3.4: Utilization factors of SSPS & CHB for different phase voltage levels.

Phase voltage levels	***UF* of SSPS**	***UF* of CHB**	**% Increase in *UF***
11	0.79	0.66	19.6%
19	0.88	0.715	23.7%

3.3.2 Switch count of the considered MLIs

In asymmetric CHB MLI shown in Fig. 3.1(a), the number of switches required for phase to obtain 11-levels in phase-voltage is 12, whereas in asymmetric SSPS MLI and MLDCL MLI, the switch count is 11 and 10 respectively. Hence in order to obtain voltage levels in the output voltage, more number of switches should conduct in CHB compared to SSPS and MLDCL. For example, the number of switches in conduction for obtaining $3V_{dc}$ voltage level of 11-level output voltage of CHB, MLDCL and SSPS MLIs shown in Fig. 3.1 are 6, 5 and 5 per phase respectively. Hence, conduction losses in CHB MLI are more as compared to MLDCL and SSPS MLI. The losses are highly considerable if the number of voltage levels increases in the output voltage.

3.3.3 Current rating of dc sources and switches

In order to record the currents delivered by each dc source in the considered inverters, a simulation study is performed. In this study, the dc voltages are selected as 1600 V, 3200 V and 3200 V. Fig. 3.2, Fig. 3.3 and Fig. 3.4 show the current waveforms of each dc sources in 11-level asymmetric CHB, MLDCL and SSPS inverters respectively for a resistive load of 0.8 MW/ph. Since utilization of dc sources of both CHB and MLDCL MLIs is equal, the peak currents delivered from their dc sources are same. Hence, the waveform of currents passing through dc sources of MLDCL and CHB MLI are identical.

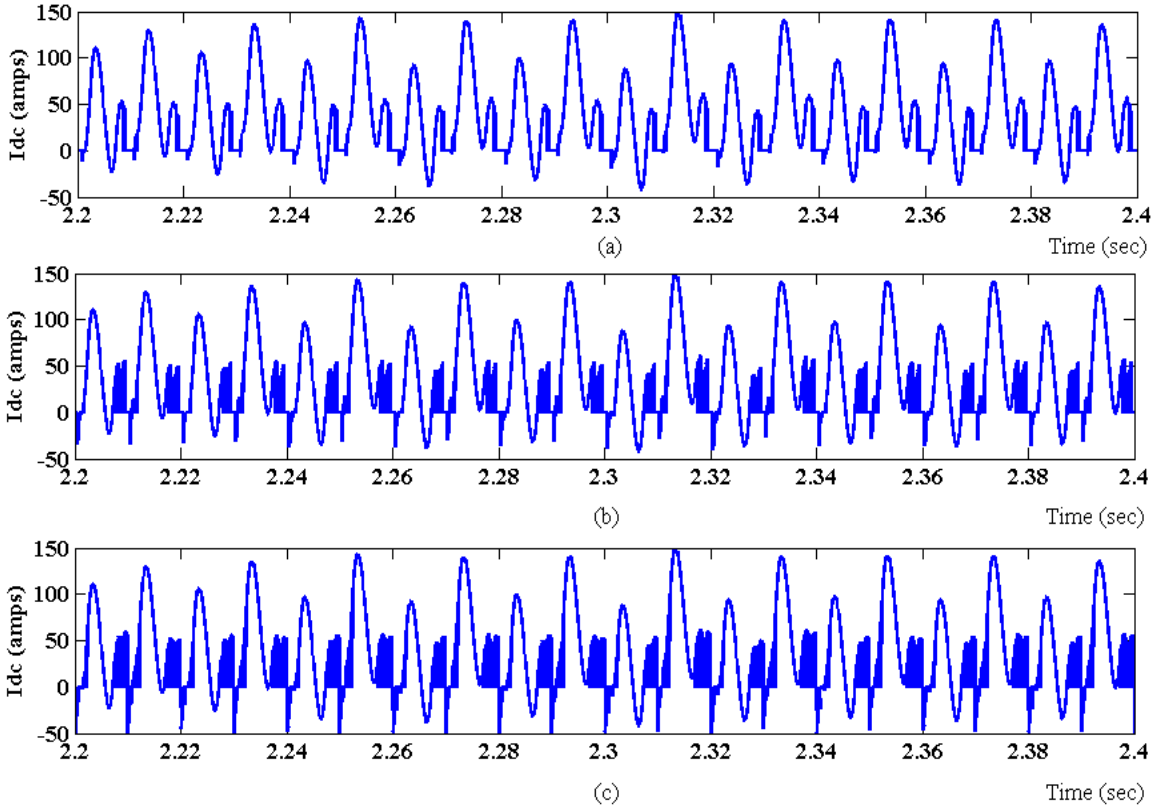


Fig. 3.2: Currents passing through dc voltage source of CHB MLI

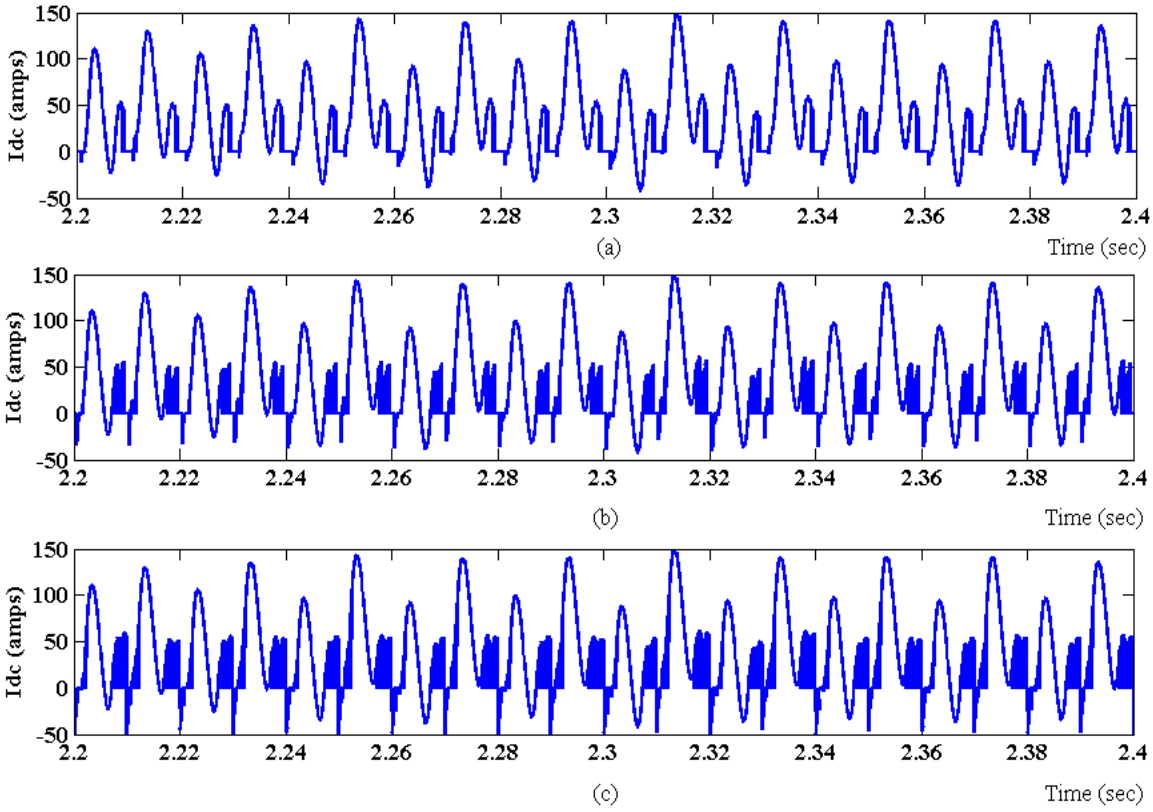


Fig. 3.3: Currents passing through dc voltage source of MLDCL MLI.

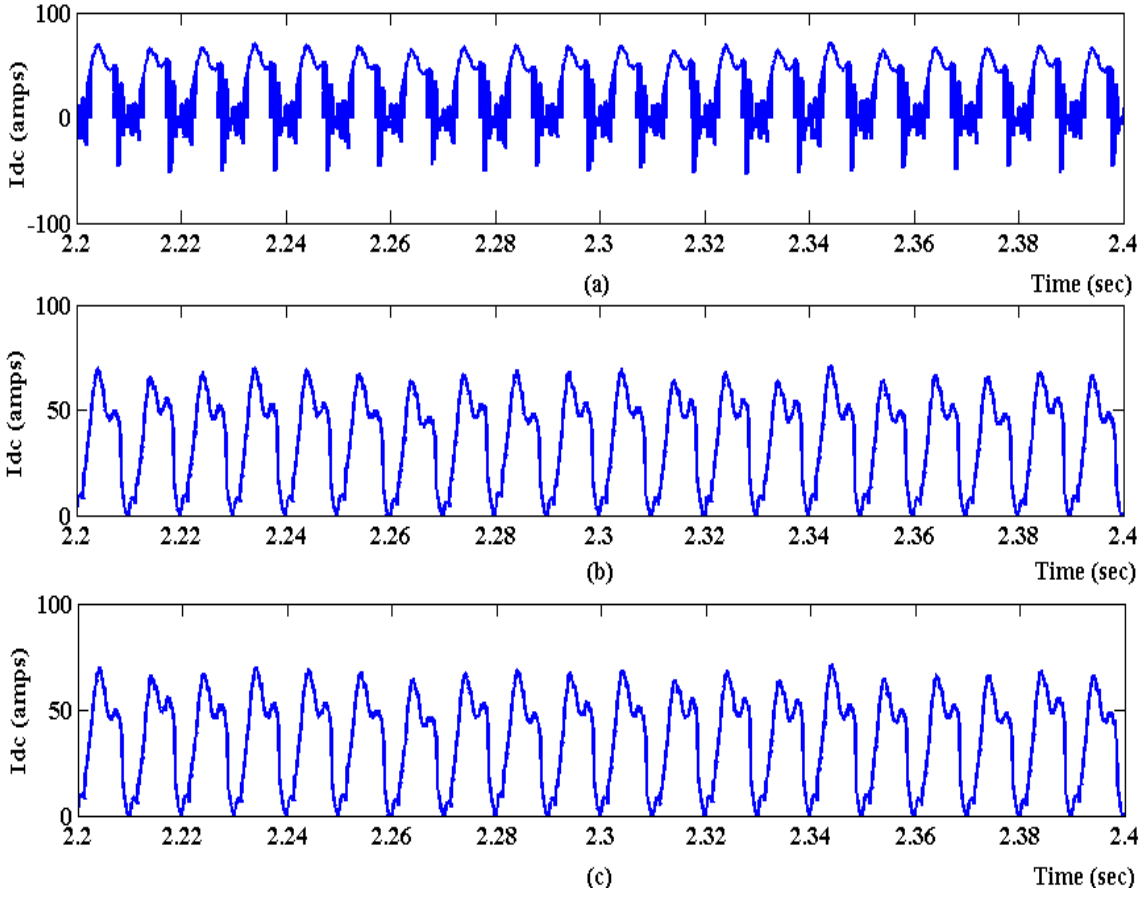


Fig. 3.4: Currents passing through dc voltage source of SSPS MLI

From Fig. 3.2, Fig. 3.3 and Fig. 3.4, it can be observed that the peak value of the current waveforms of the dc sources in CHB and MLDCL is nearly double that of the peak value of

current waveforms of dc sources in SSPS inverter. Therefore, for a given number of voltage levels, phase-voltage value and power rating, the switches and dc sources in SSPS inverter require lower current ratings as compared to CHB and MLDCL.

3.3.4 Operating frequency of the switches

Table 3.5 shows the operating frequency of each switch in CHB, SSPS and MLDCL MLIs of Fig. 3.1. Here, f_c and f_m are carrier and modulating signal frequencies respectively. From Table 3.5, it is clear that level generating switches i.e., S_1 to S_6 in the 11-level asymmetric MLDCL MLI shown in Fig. 3.1(b) operate at carrier frequency and polarity generating switches (H_1 to H_4) operate at fundamental frequency (f_m). Whereas in SSPS MLI shown in Fig. 3.1(c), the switches S_5, S_6, S_7, S_8 operate at f_c and switches S_1, S_2, S_3, S_4 operate at f_m. Therefore, more switches in 11-level asymmetric MLDCL MLI are operating at carrier frequency compared to SSPS. Therefore, switching losses in asymmetric MLDCL are more compared to SSPS. In case of CHB MLI shown in Fig. 3.1(a), all the switches i.e., S_1 to S_{12} are operate at carrier frequency, f_c. Hence, switching losses of CHB MLI are higher as compared to MLDCL and SSPS MLI.

Table 3.5: Operating frequencies of various switches of asymmetric CHB, MLDCL and SSPS MLIs.

CHB MLI		**SSPS MLI**		**MLDCL MLI**	
Switches	**Operating frequency**	**Switches**	**Operating frequency**	**Switches**	**Operating frequency**
None		S_{x1}, S_{y1}, S_{z1}	$2f_m$	None	
S_1 to S_{12}	f_c	S_5, S_6, S_7, S_8	f_c	S_1, S_2, S_3, S_4, S_5, S_6	f_c

3.3.5 Total blocking voltage of an inverter

The voltage stresses of all the switches in 11-level asymmetric CHB, MLDCL and SSPS MLIs of Fig. 3.1 is presented in Table 3.6. By observing the Table 3.6, the 'total blocking voltage [65]' of CHB, SSPS and MLDCL inverters are $20V_{dc}$, $26V_{dc}$ and $30V_{dc}$ respectively.

Table 3.6: Voltage stress appears across switches of asymmetric CHB, MLDCL and SSPS MLIs.

Voltage stress appears across switches	**Switches of 11-level asymmetric CHB MLI**	**Switches of 11-level asymmetric MLDCL MLI**	**Switches of 11-level asymmetric SSPS MLI**
V_{dc}	S_9, S_{10}, S_{11}, S_{12}	S_5 and S_6	S_5, S_6, S_7 and S_8
$2V_{dc}$	S_1, S_2, S_3, S_4, S_5, S_6, S_7, S_8	S_1, S_2, S_3, S_4	S_{X1}, S_{Y1} and S_{Z1}
$4V_{dc}$	None	None	S_1, S_2, S_3, and S_4
$5V_{dc}$	None	H_1, H_2, H_3, H_4	None

From the above table, the following conclusions are made.

- The number of switches which have voltage stresses of V_{dc} and $2V_{dc}$ in CHB MLI are more compared to MLDCL and SSPS MLIs. Hence, the cost required for these switches of the CHB MLI is more compared to MLDCL and SSPS MLIs.
- The number of switches which have voltage stress of $4V_{dc}$ in 11-level asymmetric CHB, MLDCL and SSPS MLIs are zero, zero and four respectively. Hence, additional cost requires for the switches which have $4V_{dc}$ voltage stress in SSPS MLI as compared to CHB and MLDCL MLI.
- The number of switches which have voltage stress of $5V_{dc}$ in 11-level asymmetric CHB, MLDCL and SSPS MLIs are zero, four and zero respectively. Hence, additional cost requires for the switches which have $5V_{dc}$ voltage stress in MLDCL MLI as compared to CHB and SSPS MLI.

However, the 11-level asymmetric MLDCL MLI requires 10 switches/phase, whereas for CHB MLI is 12 per phase as shown in Fig. 3.1. Hence, even though MLDCL MLI require additional cost for the switches with a high voltage stress of $5V_{dc}$, this additional cost could be offset by the savings from the eliminated gate drivers and from fewer assembly steps because of the substantially reduced number of components, which also leads to a smaller size and volume.

From the above five factors, it is observed that asymmetric SSPS RSC-MLI is superior to both CHB MLI and MLDCL RSC-MLI, especially in device switching frequency, utilization of dc sources and current rating of switches. However, the asymmetric MLDCL RSC-MLI is superior to both SSPS and CHB MLIs in terms of switching count and number of conduction of switches at each voltage level. In most of the cases, both SSPS and MLDCL are superior than the conventional asymmetric CHB. Hence, rest of the thesis discusses the capabilities of MLDCL and SSPS RSC-MLI topologies in grid connected system.

In order to achieve satisfactory operation of 11-level asymmetric SSPS, MLDCL and CHB MLI and for obtaining the less THD in the output voltage, authors implemented the hybrid modulation scheme [177] and is explained below.

3.4 Hybrid SPWM for asymmetrical RSC-MLIs

Classical pulse width-modulation (PWM) are not directly applicable for unequal sources based MLIs. Because, the switches of the higher voltage modules have to be switching at high frequency during some time of intervals [178, 179]. On the other hand, by implementing a hybrid modulation method [177] to the asymmetric MLIs, the higher input voltage cell operate at low switching frequency and the lower voltage cells operate with PWM switching frequency. With

this method, it is possible to use slow semiconductor switches in the higher input voltage modules and high frequency semiconductor devices in the other cells.

3.4.1 Generalized hybrid PWM method

A hybrid modulation strategy can be easily implemented for an asymmetrical multilevel inverter shown in Fig. 3.5. In Fig. 3.5, *n*-modules with unequal input voltages are in cascaded ($V_{dc1}<V_{dc2}<\ldots V_{dcn}$). The lowest power cell with V_{dc1} as input source will operate in PWM mode. Other cells, with higher voltage levels may operate at low frequency.

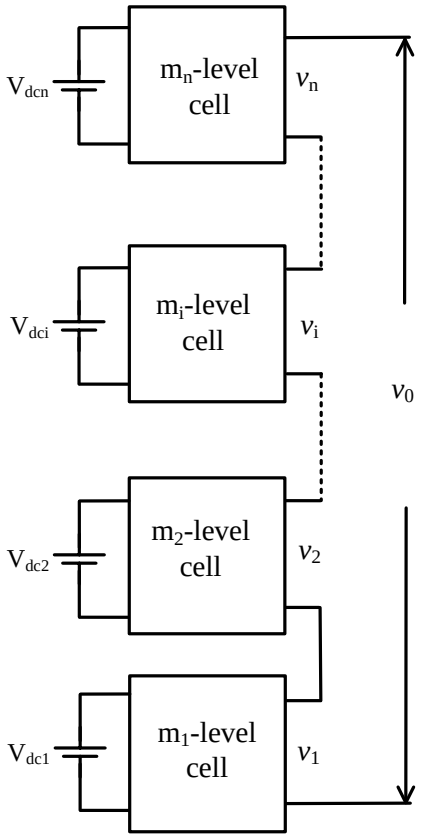


Fig. 3.5: Generalized structure of asymmetric cascaded multilevel inverter.

Hybrid modulation method can be generalized for multilevel cells, as shown in the block diagram of Fig. 3.6. One can observe from Fig. 3.6 that the reference signal of the asymmetric multilevel inverter is the reference signal (r_n) of the n^{th} module. This reference signal is compared with a given number of constant levels, which depends on the number of levels synthesized by this cell. Once the required output voltages (v_n, $v_{n-1}\ldots$) of the higher power modules are determined, the reference signal of the i^{th} modules (r_i) is acquired by subtracting the output voltage (v_{i+1}) of the $(i+1)^{th}$ module from its corresponding reference signal (r_{i+1}). This reference signal, responsible to synthesize the given number of voltage levels which are not synthesized by higher power modules, is also compared to several constant levels. Finally, the reference signal of the lowest voltage module is compared to high-frequency carrier signals, generating a high-frequency voltage v_1. Since the *n* number of modules is in cascade, hence the final output voltage

(v_0) of this asymmetric MLI of Fig. 3.5 is obtained by adding v_1, v_2,…, v_n as shown in Fig. 3.6. The description of implementation of hybrid PWM method for asymmetric MLI is discussed in [177]. The example for the implementation of hybrid PWM method for operation of considered 11-level asymmetric SSPS RSC-MLI shown in Fig. 3.1(c) is discussed below.

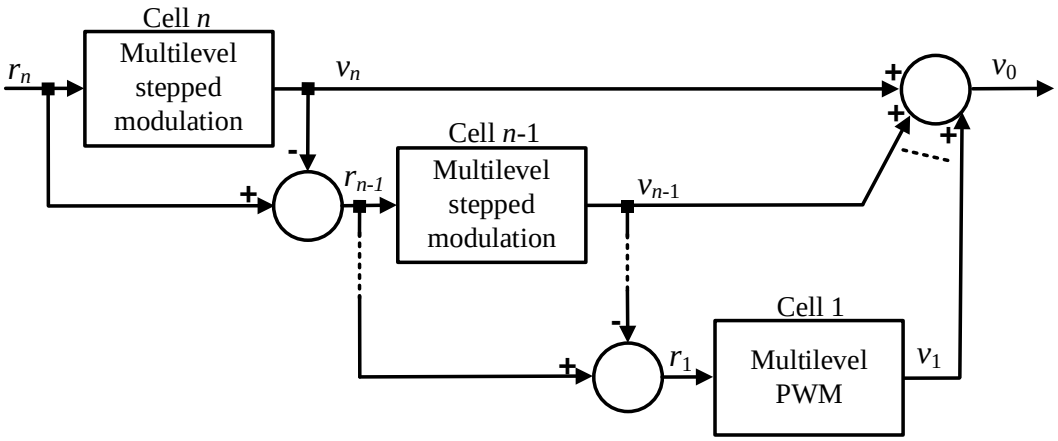


Fig. 3.6: Block diagram of generalized hybrid modulation strategy

3.4.2 Hybrid modulation method for 11-level asymmetric SSPS RSC-MLI

The hybrid modulation method can be directly applied for the considered 11-level asymmetric SSPS MLI due to its cascading structure as similar to Fig. 3.5. Hence, the devices of lower part (or higher voltage part of the SSPS) are operating at low frequency and high frequency PWM driving scheme is adapted to the upper H-bridge. Using this method, the voltage v_1 is obtained from the lower part i.e., higher power H-bridge and voltage v_2 are obtained from upper part i.e., lower power H-bridge cell of SSPS. In order to generate the voltage levels (i.e., $\pm 4V_{dc}$ and $\pm 2V_{dc}$ levels) in v_1 as shown in Fig. 3.7, the constant levels of $4V_{dc}$ and $2V_{dc}$ are compared with the reference signal ref_1. Once the required output voltage of lower part of H-bridge i.e., v_1 is obtained, the reference signal (ref_2) for the upper H-bridge cell is obtained by subtracting the output voltage, v_1 of the lower part from its corresponding reference signal ref_1. This reference signal, ref_2 is compared to high-frequency carrier signals of magnitude varying from $+V_{dc}$ to $-V_{dc}$ and generating a high-frequency voltage as v_2 which varying between $+V_{dc}$ and $-V_{dc}$ as shown in Fig. 3.7. Since the upper and lower part of the SSPS structure are in cascade connection, hence the final output voltage (v_0) with 11-levels varying from $+5V_{dc}$ to $-5V_{dc}$ is obtained by adding v_1 and v_2 as shown in Fig. 3.7.

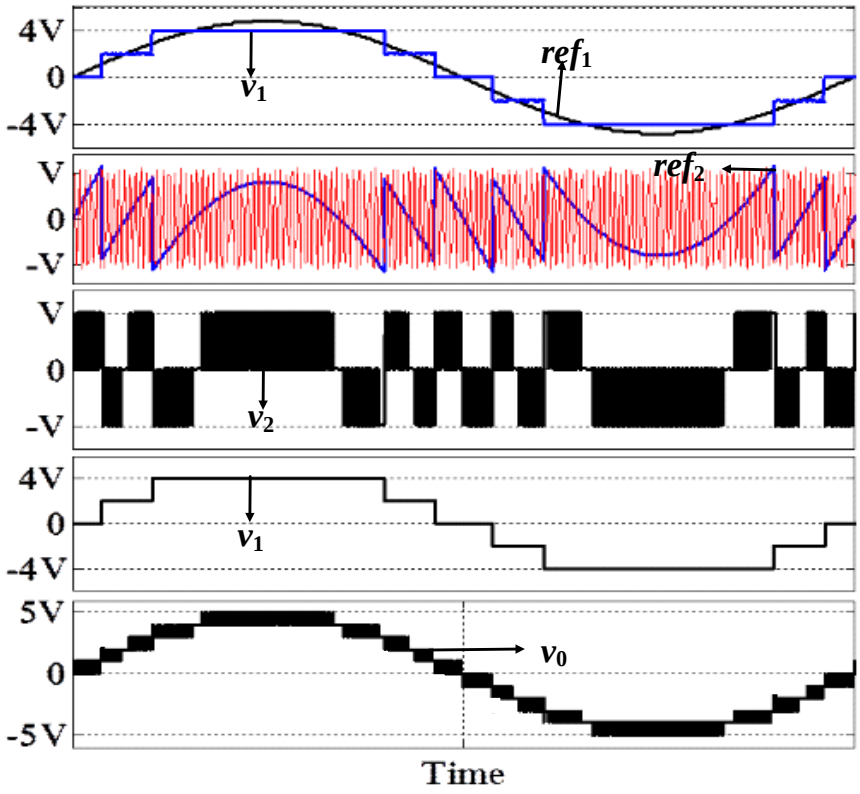


Fig. 3.7: Hybrid modulation method of the proposed asymmetric 11-level SSPS RSC-MLI.

3.5 Conclusion

In this Chapter, the structure and operation of 11-level asymmetric CHB, MLDCL and SSPS MLIs are discussed. The concept of generation of voltage levels through series/parallel connected operation of the capacitors or dc voltages sources in SSPS topology is encouraged the author to introduce a new factor called as "utilization factor" and is explored in this chapter. From the structure and operation of these asymmetric MLIs, the following observations are made.

- The series/parallel connection of dc sources in the SSPS inverter is possible to increase the utilization of dc sources when compared to CHB, which is advantageous in PV applications.
- The considered asymmetric SSPS RSC-MLI is superior to conventional CHB MLI in terms of switch count, device switching frequency and current rating of switches.
- The other popular topology is MLDCL RSC-MLI which is simple and highly modular in its structure requires uni-directional switches only, and the high rating switches operate at fundamental frequency. The MLDCL inverter has significant reduction in switching count compared to conventional CHB MLI. The asymmetric source based MLDCL is presented in this chapter to further reduce the device count.
- Further, the highest rating switches in polarity generator of MLDCL and SSPS inverters are operating at fundamental frequency. This will reduce switching losses. Whereas in conventional CHB MLI, all the switches operate at switching frequency.

- ❖ The presence of redundancies in the operation of MLDCL and SSPS inverters allow even power distribution between equal rated input sources [65]. Therefore, a single MPPT controller can be used for all equal rated PV sources, thereby reducing the control complexity.

Owing to the above conclusions, MLDCL and SSPS RSC-MLI topologies are most suitable and an effective alternate to conventional CHB MLI for interfacing unequal input dc sources such as PV to grid by using less complex and common control philosophy. In view of this, asymmetric SSPS and MLDCL RSC-MLIs are considered for further research.

CHAPTER 4: REAL-TIME VALIDATION OF SMC FOR CLOSED-LOOP OPERATION OF RSC-MLI

This chapter presents the active and reactive power control of three-phase SSPS RSC-MLI based grid connected system under feedback linearized sliding mode control (FBLSMC). A comprehensive performance comparison for the proposed closed-loop system with conventional two-loop PI control and SMC are discussed in this chapter.

4.1 Introduction

In order to obtain satisfactory PWM switching control of inverters, the required reference signal is obtained from the conventional PI controller. In grid connected multilevel inverters, for achieving decoupled active and reactive power control, conventional PI controllers are not suitable for different operating conditions. Since they tuned only for a particular operating point and their steady-state response time are also high. For achieving rise-time within a boundary value, it may bring to large overshoot. There are number of tuning methodologies for PI controllers, however, those are complex and time consuming processes. Moreover PI controllers cannot avoid the disturbances which exist in the system and those are sensitive to system parameters variations.

If the system model is exact, then the design of the controller can cancel all the unresolved issues in the system. However it is very difficult to design the exact model of the system especially when the system parameters are uncertain. Further, the MLI based grid connected systems are highly nonlinear and coupled in nature. Feedback linearization technique converts all or part of dynamic systems into linear system(s) designated by algebraic equations. In other words, linearization theory converts main model of the system into a simple form of corresponding models. Hence, it can be used in designing robust controllers for nonlinear systems. One of such robust controller is sliding mode control (SMC) technique [85, 86]. SMC is well suitable for power electronics applications because it has inherent discrete switching action. In this SMC, the switching action is in such a way that the state direction of the system is brought back to sliding surface and track the equilibrium point. SMC offer good robustness because sliding surface and switching are independent of system operating points and other circuit parameters.

In this chapter, sliding mode control technique has been incorporated in the feedback linearized control to address the decoupled active and reactive power control and to add robustness during operating point changes and system parameter variations.

4.2 System configuration

The block diagram for the proposed system considered with SSPS RSC-MLI, feeding set point real and reactive powers (P_{ref} and Q_{ref}) to three-phase grid is shown in Fig. 4.1. The closed-loop control of RSC-MLI SSPS is achieved by employing either a PI controller or by developing by a sliding mode based nonlinear controller. The controller in turn generates the reference modulating signals ($v_{abc\text{-}ref}$) for the generation of switching pulses for the MLI, as shown in Fig. 4.1. The structure and operation of considered 11-level asymmetric SSPS RSC-MLI was discussed in Chapter 3.

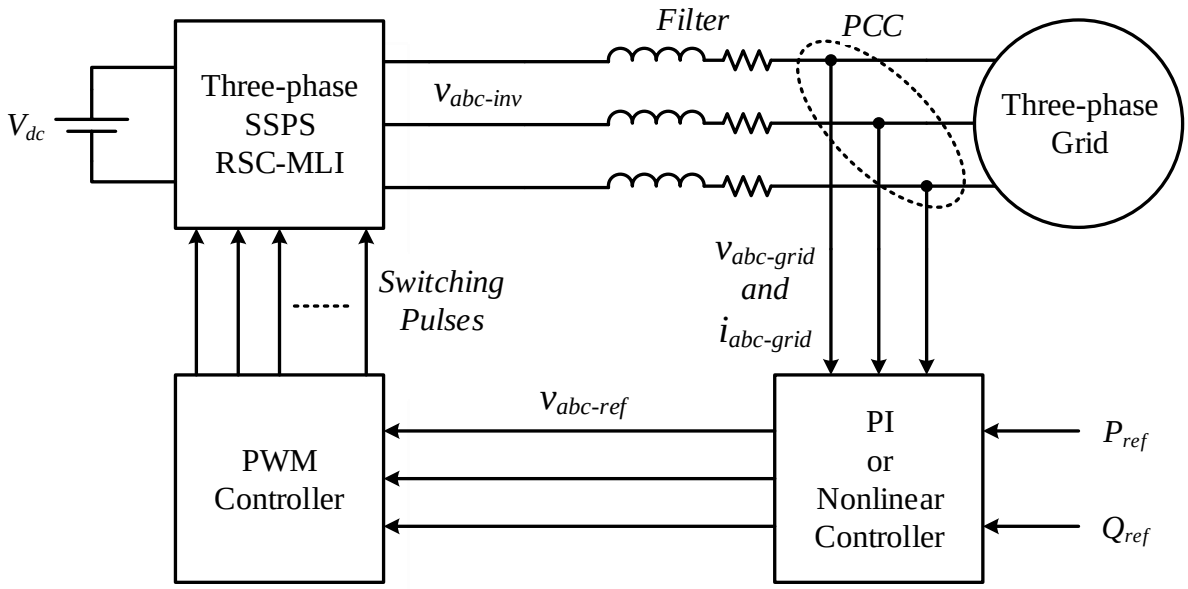


Fig. 4.1: Grid connected MLI System layout.

4.2.1 Conventional control strategy for grid connected SSPS RSC-MLI

The main control objective in this inverter based distributed generation (DG) system is to supply the required amount of powers to the grid. This can be achieved by controlling the inverter with conventional PI controller, in which the modulating voltages are derived by PI controllers, after directly processing the errors in the powers as shown in Fig. 4.2. However, due to the lack of inner current loop, this direct power control mechanism may result in current overshoots there by activating the protection circuitry of the power converter. In some cases, these high converter currents can damage the switches and its associated devices. Hence a two-loop based power control mechanism is considered in this chapter as shown in Fig. 4.3. However, in two-loop control, the reference currents are generated by PI controllers which process the power errors. These current references are compared with actual currents. These current errors are further processed in second set of PI controllers to generate the modulating voltages. Therefore, this methodology involves two sets of PI controllers to deliver desired real and reactive powers. The MLI based grid connected DG system is a highly nonlinear system with multiple switching across

different voltage sources within a single cycle to achieve multi levels in its output. With this highly nonlinear converter based DG system, the tuning of PI controller is a challenging task. With two sets of PI controllers in the control loop, the tuning process becomes much more complex. Hence, to minimize the tuning complexity, a modified two-loop control mechanism with limited current references is developed in this thesis as shown in Fig. 4.4.

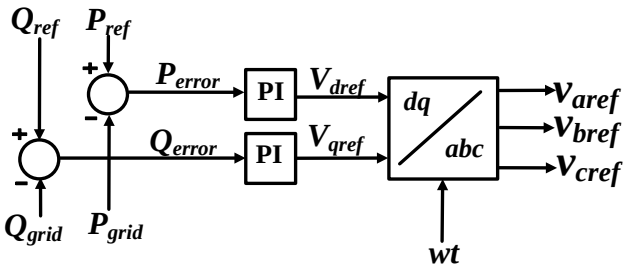


Fig. 4.2: Active and reactive power control using conventional PI controller.

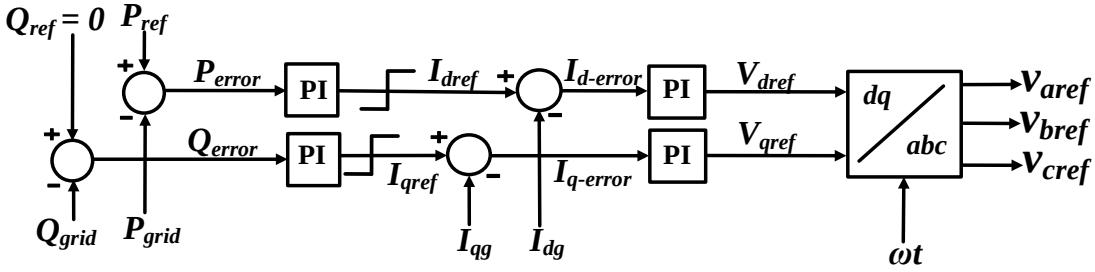


Fig. 4.3: Active and reactive power control using two sets of PI controllers.

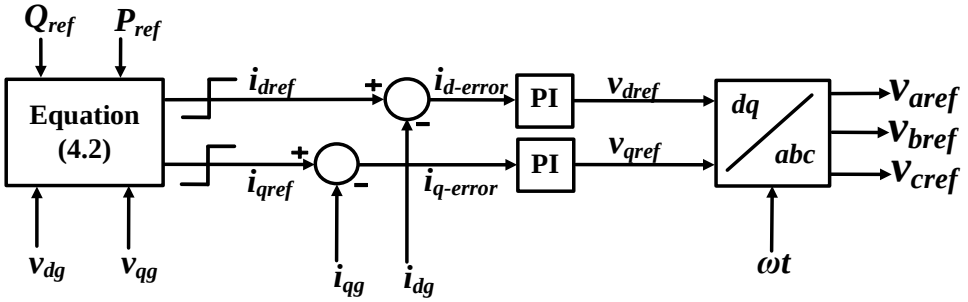


Fig. 4.4: Active and reactive power control using modified two loop PI controller.

The real and reactive powers (P_g and Q_g) flowing in the system are given by (4.1). The current references (i_{dref} and i_{qref}) are estimated using (4.2). These estimated current references are in turn used to generate the modulating voltages, thereby eliminating one set of PI controllers.

$$P_g = (v_{dg} i_{dg}) + (v_{qg} i_{qg}) \text{ and } Q_g = (v_{qg} i_{dg}) - (v_{dg} i_{qg}) \tag{4.1}$$

$$i_{dref} = \frac{v_{qg} Q_{ref} + v_{dg} P_{ref}}{v^2_{dg} + v^2_{qg}} \text{ and } i_{qref} = \frac{v_{qg} P_{ref} - v_{dg} Q_{ref}}{v^2_{dg} + v^2_{qg}} \tag{4.2}$$

Even though, the modified two-loop PI control reduce the complexity, its capability in decoupling the real and reactive power controls is poor. It is due to the multivariable structure and highly coupled nonlinearity of the MLI based grid connected system. Moreover, the PI controller

is sensitive to system parameter variations. Hence, it is necessary to transform the coupled and nonlinear system into decoupled and linear system by adapting feedback linearization technique which is explained as follows.

4.2.2 Feedback linearization technique

The interconnecting system shown in Fig. 4.5, from the output voltage of MLI (v_{dqinv}) after transforming into *dq* reference frame can be represented in a nonlinear dynamic mathematical model as:

$$v_{dinv} - R_f i_{dg} - L_f \frac{di_{dg}}{dt} + \omega L_f i_{qg} - v_{dg} = 0 \tag{4.3}$$

$$v_{qinv} - R_f i_{qg} - L_f \frac{di_{qg}}{dt} - \omega L_f i_{dg} - v_{qg} = 0 \tag{4.4}$$

Consider the standard state-space representation as:

$$\frac{dx}{dt} = f(x) + g(x)u \tag{4.5}$$

The coupled and nonlinear system can be transformed into decoupled and linear system by rearranging (4.3) and (4.4), in the form of equation (4.5) with i_{dg} and i_{qg} as state variables which results equation (4.6).

$$f(x) = \begin{bmatrix} -\frac{R_f}{L_f} i_{dg} + \frac{X_f}{L_f} i_{qg} - \frac{1}{L_f} v_{dg} \\ -\frac{R_f}{L_f} i_{qg} - \frac{X_f}{L_f} i_{dg} - \frac{1}{L_f} v_{qg} \end{bmatrix} \qquad g(x) = \begin{bmatrix} \frac{1}{L_f} & 0 \\ 0 & \frac{1}{L_f} \end{bmatrix} \quad x = \begin{bmatrix} i_d \\ i_q \end{bmatrix} \quad u = \begin{bmatrix} v_{dinv} \\ v_{qinv} \end{bmatrix} \tag{4.6}$$

From the above equation (4.6), it is observed that there is a possible decoupling existing between the currents i_{dg} and i_{qg}.

After linearization, the system can be represented as:

$$\lambda = A(x) + B(x)U \tag{4.7}$$

In order to obtain the control input to the MLI switching operation, the above equation can be written as,

$$U = (-B^{-1}(x) * A(x)) + (B^{-1}(x) * \lambda) \text{ or } U = \alpha(x) + \beta(x)\lambda \tag{4.8}$$

Where, $\alpha(x) = -B^{-1}(x) * A(x)$ and $\beta(x) = B^{-1}(x)$

$$B(x) = \begin{bmatrix} g_{11}(x) & 0 \\ 0 & g_{22}(x) \end{bmatrix} A(x) = \begin{bmatrix} f_{11}(x) \\ f_{21}(x) \end{bmatrix}$$

$$\lambda = [\lambda_{11} \quad \lambda_{12}]^T = \begin{bmatrix} \frac{di_{dg}}{dt} & \frac{di_{qg}}{dt} \end{bmatrix}^T \tag{4.9}$$

In this thesis, the MLI is operating in active and reactive power control mode and the output states are taken as

$$Y = [i_{dg} \quad i_{qg}]^T \tag{4.10}$$

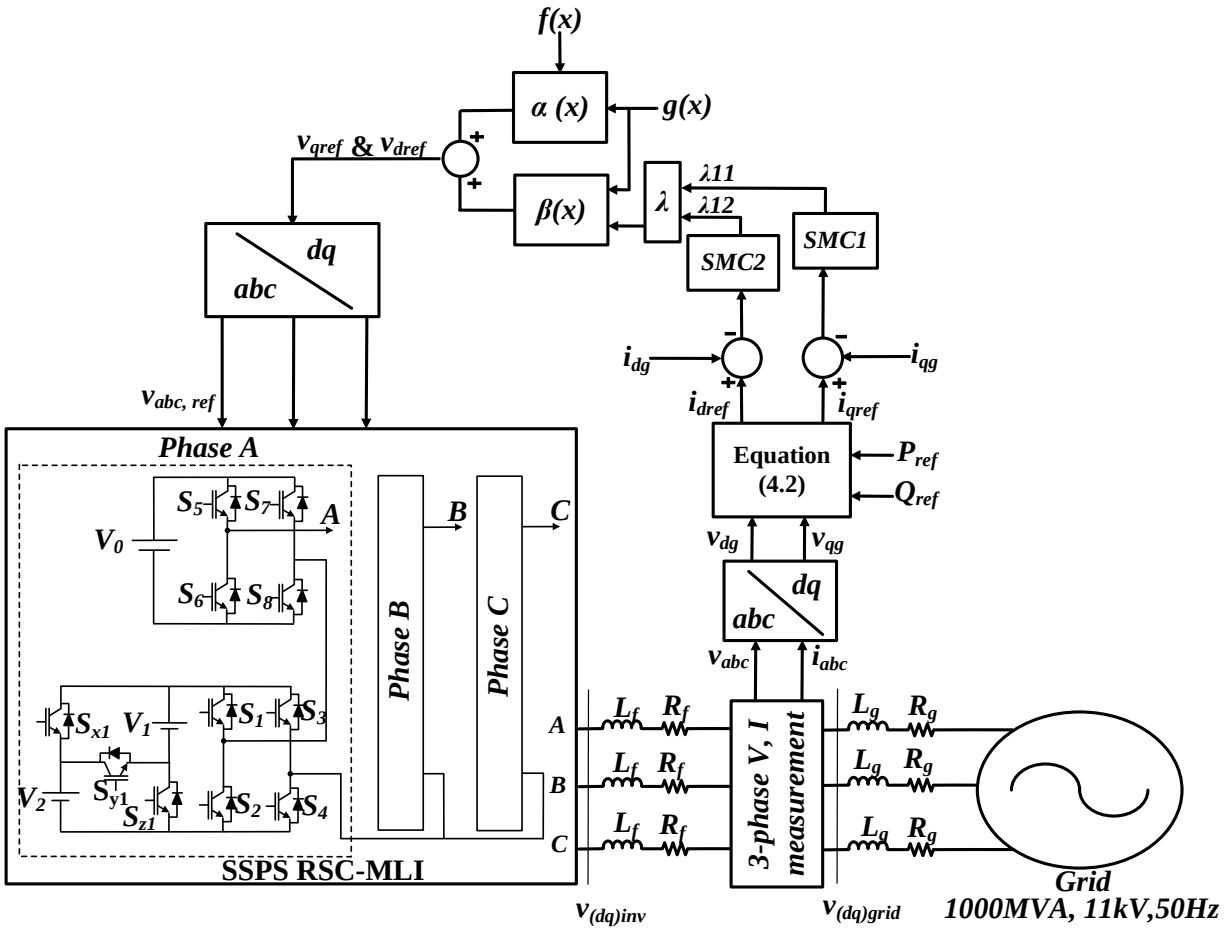


Fig. 4.5: Active and reactive power control using SMC.

4.3 Adaption of sliding mode control

The feedback linearization as discussed in the earlier section can only be effectively adapted if the exact model of the system is known. However, it is not an easy task to obtain all the parameters of the system. Moreover, as the MLI involves many switching within a single cycle across different voltage levels, even the parameters are known, the accurate model with prevailing nonlinearities is difficult to obtain. Further, as the system operating point and parameters are subjected to change in the due course of operation, the developed model cannot represent the system accurately in succeeding operations. To resolve this, SMC [85, 86] technique is incorporated in the controller. In SMC, the discrete switching action is generated in such a way that the state direction of the system is brought back to sliding surface and traced up to the equilibrium point.

4.3.1 Constitution of sliding surface and stability criterion

The state vector which is obtained in linearization process as in Section 4.2.2 will be transformed into a new state vector, and subsequently the new control input, once the SMC is

incorporated in the controller. The SMC can be viewed as combination of equivalent control and a switching control as represented in (4.11). The equivalent control can be adapted from linearization process as described in Section 4.2.2 while the switching control is responsible for nullifying the errors resulting from parameter variations changes, operating point changes.

$$U(t) = U_{eq}(t) + U_{sw} = U_{eq}(t) + \rho.tanh(\sigma) \tag{4.11}$$

where, ρ is a positive constant and σ is the sliding surface. For the satisfactory operation of the controller, it is necessary to define sliding surface. Here, two sliding surfaces, namely σ_1 and σ_2 are to be defined, since (4.10) has two output states, i_{dg} and i_{qg}. For the second order state variables, the sliding surface $\sigma(t)$ can be defined as:

$$\sigma(t) = \frac{d\ er(t)}{dt} + K_i\ er(t) \tag{4.12}$$

where K_i the positive constant, $er(t)$ is the error in the output. In this work, by considering the relative degree for both i_{dg} and i_{qg} as 1, the error in DG current is chosen as sliding surface. Hence, $\sigma_1 = er_1 = i_{dg} - i_{dref}$ and $\sigma_2 = er_2 = i_{qg} - i_{qref}$. The sliding surface matrix σ with σ_1 and σ_2 as elements can be defined as:

$$\sigma = \begin{bmatrix} \sigma_1 & \sigma_2 \end{bmatrix} \tag{4.13}$$

For extract conditions on the SMC control law which can run the state path to the equilibrium point, Lyapunov approach is considered here. The Lyapunov function can be represented as:

$$G = \frac{1}{2}\sigma^2 \tag{4.14}$$

Lyapunov stability criterion states that "if G is a positive definite function and its derivative, dG/dt is negative definite, then the system is asymptotically stable."

$$\frac{dG}{dt} = \sigma\dot{\sigma}^T < 0 \tag{4.15}$$

To satisfy the condition $\sigma\dot{\sigma}^T < 0$, the $\dot{\sigma}$ can be considered as $\rho tanh(\sigma)$.

$$\dot{\sigma}_1 = -\rho_1.\tanh(\sigma_1) \text{ and } \dot{\sigma}_2 = -\rho_2.\tanh(\sigma_2) \tag{4.16}$$

Substituting (4.13) in (4.16),

$$\dot{\sigma}_1 = -\rho_1.\tanh(i_{dg} - i_{dref}) \text{ and } \dot{\sigma}_2 = -\rho_2.\tanh(i_{qg} - i_{qref}) \tag{4.17}$$

With the obtained new dynamics using SMC, the state vector can be represented as:

$$\lambda_1 = \begin{bmatrix} \lambda_{11} \\ \lambda_{12} \end{bmatrix} = \begin{bmatrix} -\rho_1.\tanh(i_{dg} - i_{dref}) \\ -\rho_2.\tanh(i_{qg} - i_{qref}) \end{bmatrix} \tag{4.18}$$

The values of i_{dref} and i_{qref} can be obtained from (4.2). If the parameter of the system changes then change in the system matrix is ΔA, the system can be represented as:

$$\dot{X} = (A + \Delta A)X + B(U_{eq} + U_{sw}) \tag{4.19}$$

$$\dot{X} = AX + BU_{eq} + \Delta AX + B\rho \tanh(\sigma) \tag{4.20}$$

The parameter dependency part ΔAX will be compensated by switching part $B\rho \tanh(\sigma)$. Hence, the barrier condition for the selection of ρ is

$$B\rho > \Delta AX \text{ (or) } \rho > [B^{-1}\Delta AX] \tag{4.21}$$

As aforesaid, ρ is a positive constant, however, to cancel out the errors resulting from parameter variations and operating point changes, external disturbances, the ρ should be large. However, large value of ρ will just convert the smooth transition action of *tanh* into hard switching function, *sign* which will results in chattering in the output. On contrary, very small value of ρ is not enough to cancel the parameter and operating point dependencies. Moreover, small ρ will result in sluggish response. Hence, in this work a sufficiently large value of ρ is selected so that the controller will render quick response while not entering the chattering zone. With the small value of the ρ, say 0.5, the response will be sluggish as shown in the following Fig. 4.6. For the same system, if the ρ is 8, the system response is highly chattering as shown in the Fig. 4.6. This is due to the fact that, with large value of ρ, though the switching function is *tanh* (a smooth switching function), it is behaving like *sign* function. Indicating that large gain with *tanh* function will hit the boundaries even for a small error, hence transforming it as a bang-bang type control. Hence in this work ρ is selected as 2 so that quick control can be achieved without any chattering.

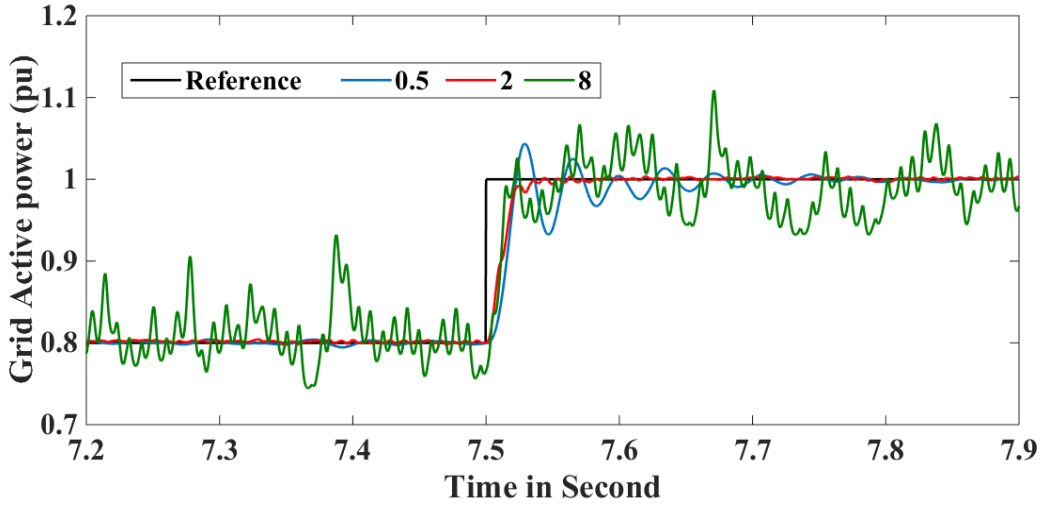


Fig. 4.6: Power respose for various values of ρ.

4.4 Results and validations

This section discusses the performance of the SSPS RSC-MLI based grid system with PI and SMC. Simulation studies are presented for different case studies in MATLAB/Simulink environment and later validated in real-time environment using OPAL-RT system.

4.4.1 Simulation results

The SSPS RSC-MLI based grid connected system with PI controller as well as with SMC is developed as shown in Fig. 4.4 and Fig. 4.5 using MATLAB/Simulink environment. The PI controller is designed as per the procedure outlined in Section 4.2.1 and its gain parameters are tuned using integral time squared error criterion. The SMC is designed according to the procedure discussed in Section 4.3. The parameters of the system considered for various studies are given in Table 4.1.

Table 4.1: System parameters

Parameter	**Value**
Grid Voltage, V_g	11 kV
Grid frequency, f	50 Hz
Filter inductance, L_f	8 mH
Filter Resistance, R_f	0.2Ω
Voltages sources, V_0, V_k	1600 V, 3200 V
Switching frequency, f_s	5 kHz
Sample time, T_s	50μs
Base power	1 MVA
Short circuit MVA	1000 MVA
Sliding mode parameter ρ	2

The PWM scheme is designed such that the SSPS inverter synthesizes 11-levels in its output phase-voltage as depicted in Fig. 4.7 and its corresponding harmonic spectrum is shown in Fig. 4.8, which shows the total harmonic distortion (THD) in voltage is 11.93%. The performance of the MLI with designed PI and SMC controllers are examined for set-point power feedings to the grid under different operating conditions. For simplicity, the powers in results are represented in per unit (pu) with a base value of 1 MVA. The simulation study has been carried out with the following case studies:

Case 1: Step change in active and reactive power references.

Case 2: Step change in reference reactive power with constant active power reference.

Case 3: Step change in grid frequency.

Case 4: Continuous step change in grid frequency

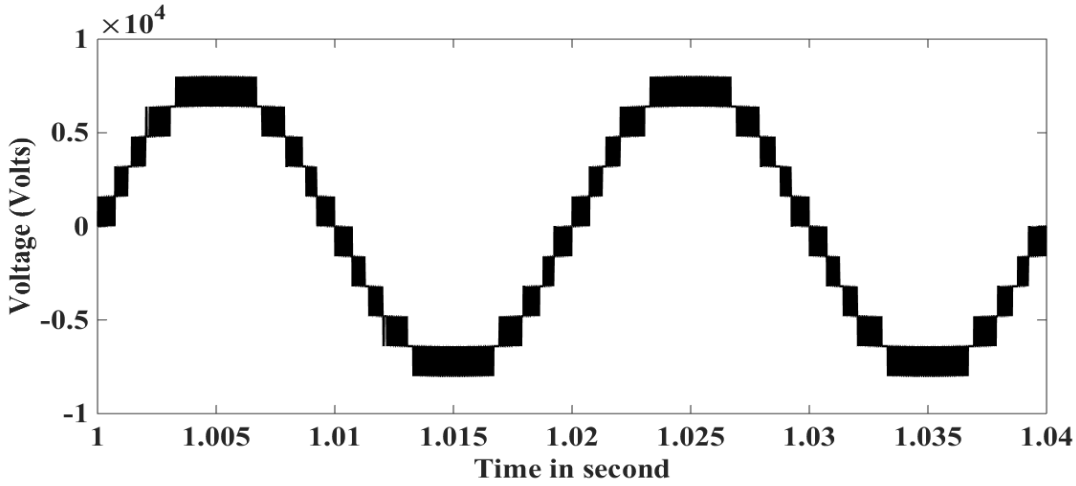


Fig. 4.7: Phase voltage waveform of the RSC SSPS MLI for 11-levels**.**

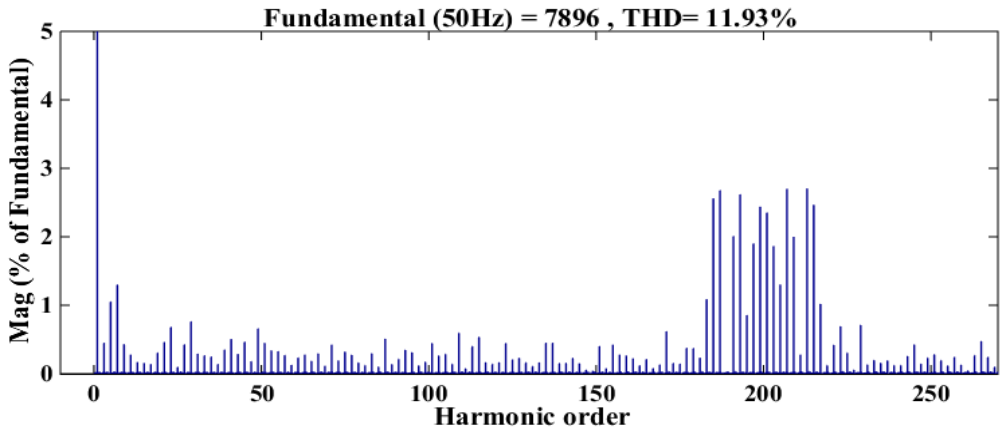


Fig. 4.8: Harmonic spectrum of phase voltage of RSC SSPS MLI for 11-levels**.**

4.4.1.1 Step change in active and reactive power references

This case study is considered to evaluate the performance of the proposed system with set-point change in real and reactive power references. As shown in Fig. 4.9, active power reference (P_{ref}) is changed from 0.8 pu to 1 pu and reactive power reference (Q_{ref}) is changed from 0.3 pu to 0.4 pu at 17 s. It can be observed that SMC is able to track new P_{ref} within 3 to 4 cycles. The performance of PI is on par with SMC, except a little delay in settling at the new reference powers. However, none of the controllers are resulting in any appreciable over/undershoots which can be seen in Fig. 4.9. Similarly, both SMC and PI are exhibiting very good performances for the decrease of reference powers as shown in Fig. 4.10.

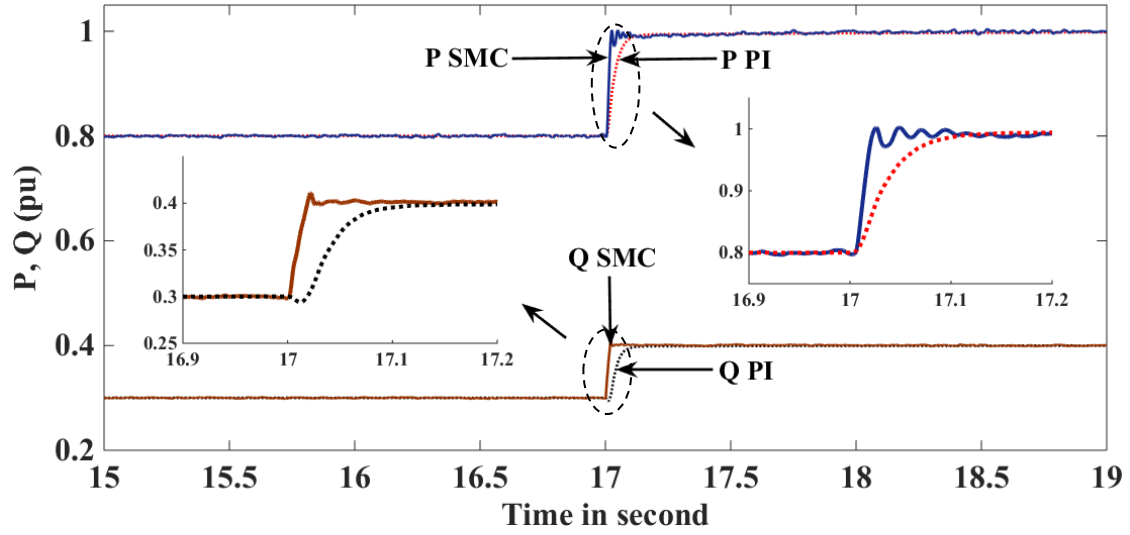


Fig. 4.9: Performance comparison of SMC and PI for step increase in active and reactive powers references.

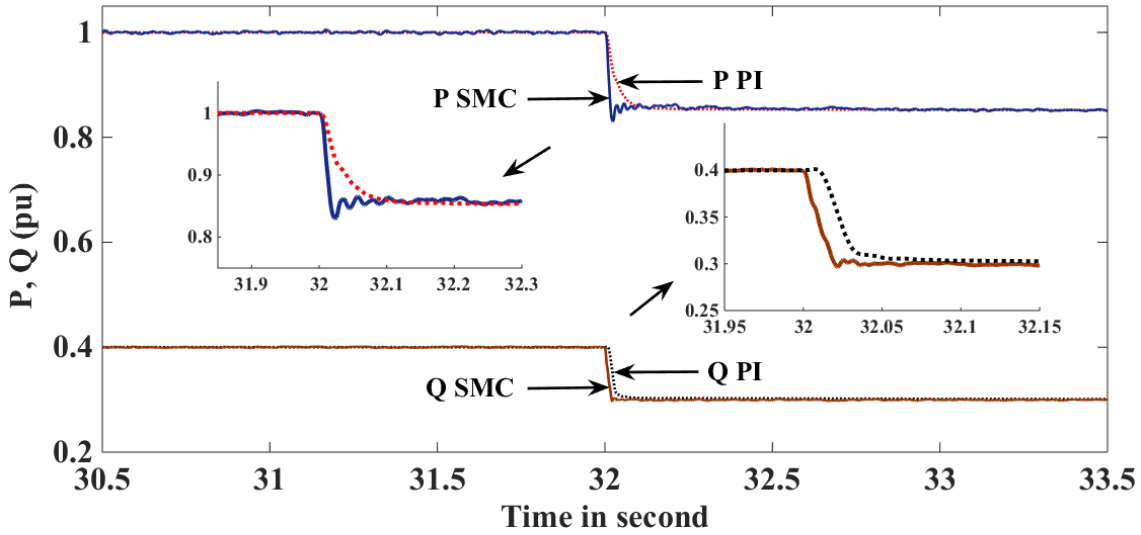


Fig. 4.10: Comparison between SMC and PI for step decrease in active and reactive powers.

4.4.1.2 Change in reference reactive power with constant active power

In this case, the Q_{ref} is changed from 0.4 pu to 0.3 pu while keeping the P_{ref} as constant at 0.8 pu. Performance of the MLI with SMC and PI controllers are shown in Fig. 4.11. It can be observed that, the PI based approach is resulting a larger undershoot when compared with SMC. This confirms the better decoupling control capability of SMC as active power is almost unaffected by change in reactive power due to the decoupling between active and reactive powers provided by FBLSMC. Similar characterization can be observed for change in real power reference while keeping the reactive power as constant.

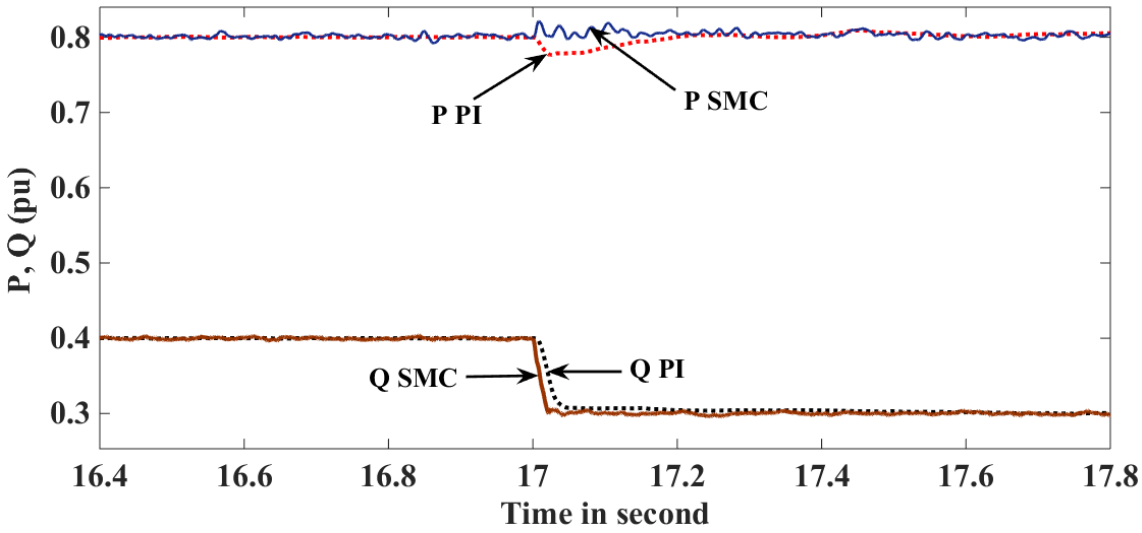


Fig. 4.11: Performance of PI and SMC for a step change in reactive power and constant active power.

4.4.1.3 Change in grid frequency

This case study is to examine the adaptability of gains in both the controllers for a small deviation in grid frequency. At first, the grid frequency is considered to be varied by 1 Hz at 20 s (i.e. from 50 Hz to 51 Hz) and returns to 50 Hz at 30 s. For this step change in grid frequency the performance of these two controllers are shown in Fig. 4.12. Even though, both the controllers are driven by same PLL, the SMC is able to adjust its gain very quickly and delivering extraordinary performance without any over/undershoots and with very small settling time as shown in Fig. 4.12.

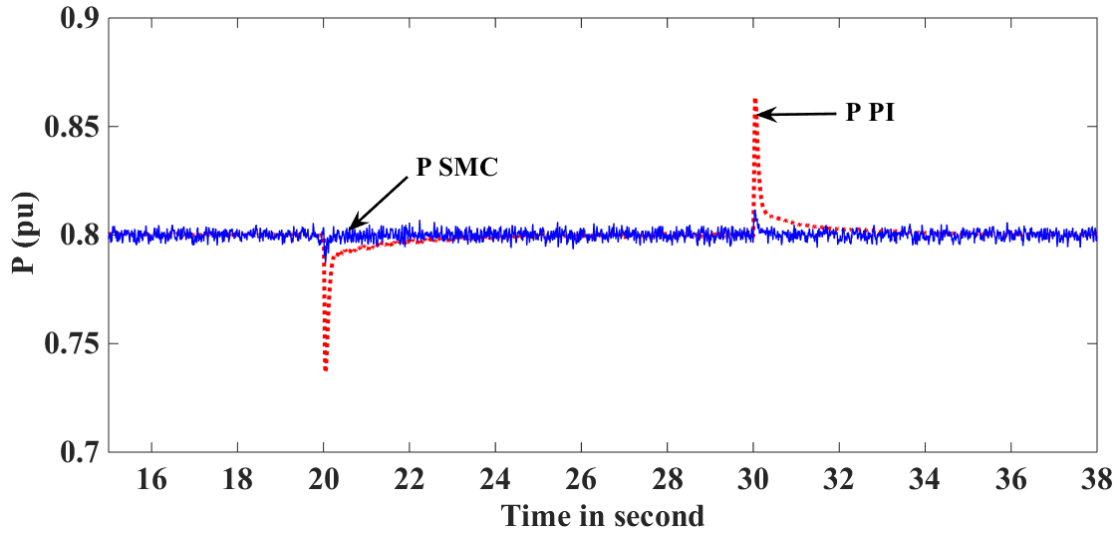


Fig. 4.12: Active power for step change in frequency under SMC and PI.

4.4.1.4 Continuous step change in grid frequency

To further validate the controllers under varying grid frequencies, a continuous variation in grid frequency of 0.25 Hz (0.5 %) is considered from 20s to 30s to represent the modal frequency oscillations in power system. The performance of the controllers is depicted in Fig. 4.13. Since the

PI controller is fixed gain controller, it is unable to adapt its gains and delivering highly oscillating performance as shown in Fig. 4.13. However, the SMC is delivering superior performance with very minimum oscillations when compared with PI controller. This is due to the inherent nature of SMC which is capable of adapting its gain according to the distance of error from the defined error sliding surface.

Another important conclusion that can be drawn from this case is that with slight change in frequency, be it a step change or continuous change, PI controller resulting high oscillatory performance with large overshoots/undershoots. This nature of performance with PI controller may activate the over current protection gear in the system, hence completely disconnects the inverter from the system, otherwise the switches in the inverter may get damaged. On the other hand, SMC is delivering the required set-point powers without any deviations even under variations in frequency. Hence, the protection gear will remain inactive. Thereby, SMC eliminates the necessity of disconnection of inverter by keeping the currents or powers well within the limits, hence contributing to the system stability and reliability under these operating disturbances.

Therefore, it can be concluded from the above discussions that for all the test cases considered, SMC is delivering either superior performance or its performance is on par with the PI controller. In no case the performance of SMC is inferior to the PI controller. Moreover, SMC is exhibiting extraordinary performance under grid frequency variations while feeding set-point real and reactive powers from SSPS RSC-MLI.

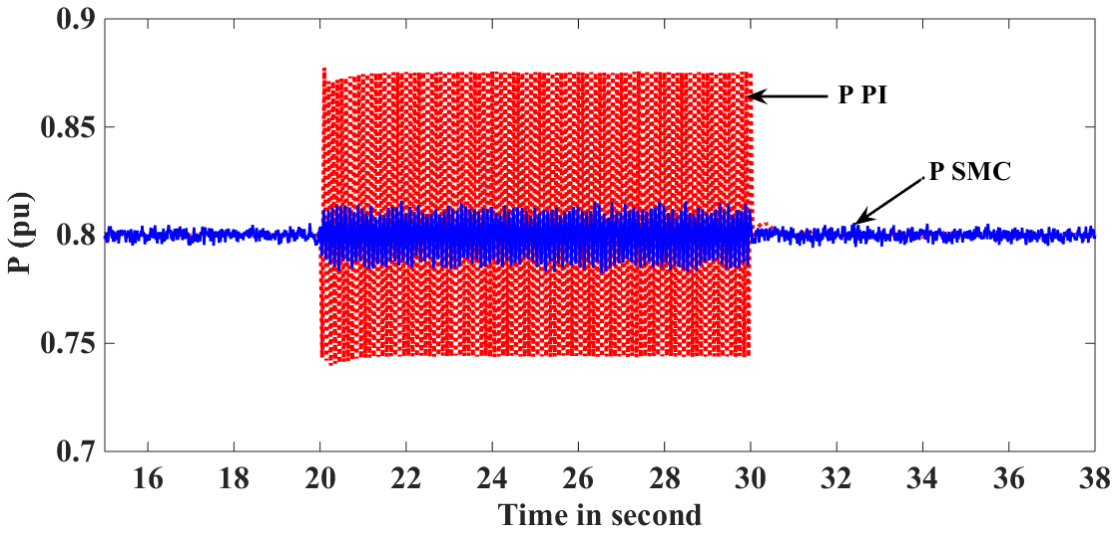


Fig. 4.13: active power for step change in frequency under SMC and PI.

4.4.2 Real-time validation with OPAL-RT

The OPAL-RT systems have proven record in validating the complex systems and their controls. Hence, this work considered this platform to validate the performance of proposed SSPS RSC-MLI based grid connected closed-loop system. This MLI is controlled either by SMC or PI controller. To verify the performance of the proposed system in real-time environment, two

OP4500 modules of OPAL-RT are integrated as shown in Fig. 4.14 and the corresponding photograph is shown in Fig. 4.15.

To analyze the complete grid interfacing system, one of the module works as a plant, that is grid connected SSPS MLI whereas the second module works as controller, i.e., SMC or PI based PWM generator. The plant system along with its interface generates analog signals according to the operating conditions and disturbances which will be acquired by controller through communication channel. The controller system generates necessary control actions according to the selected control scheme. The controller communicates the pulses to the plant in the form of digital signals. In order to validate the proposed closed-loop grid connected MLI based system in real-time using OPAL-RT systems, the sampling time is taken as 50 μs, which gives the sampling frequency of 20 kHz. With this selection of sample time, the overrun errors are made zero, so that the real-time implementation will be more accurate. The rear view of OPAL-RT module is shown in Fig. 4.16 with the typical access points for the digital input/output port (Block A), analog input/output port (Block C), differential input/output port (Block B), and standard computer connection port (Block D).

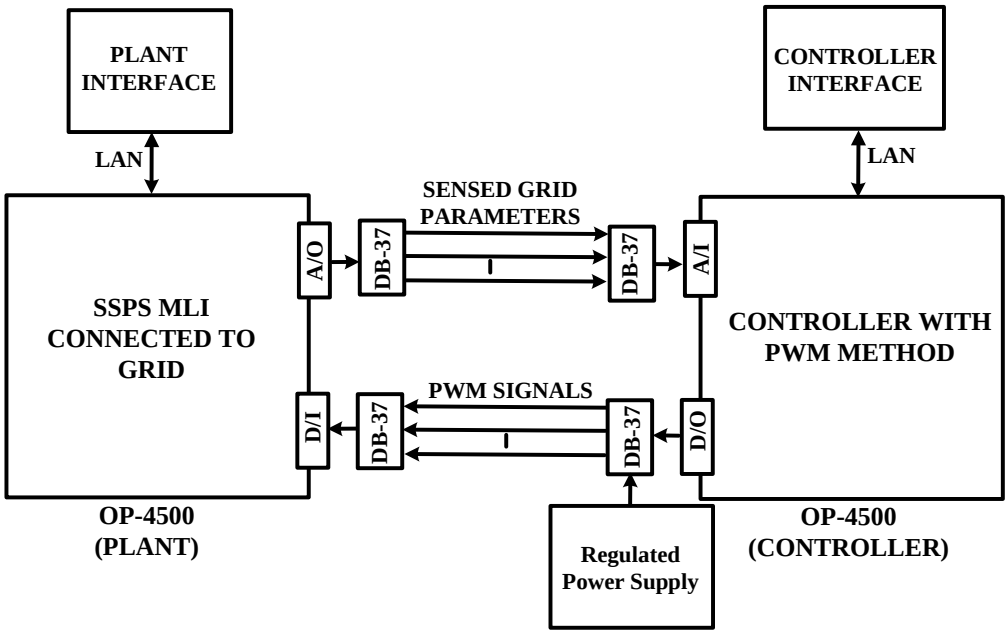


Fig. 4.14: Schematic layout of OPAL-RT Real time environmental setup.

The connector DB37, which is shown in Fig. 4.17 is useful for the digital inputs/outputs and analog inputs/outputs of A and C blocks respectively. As shown in Fig. 4.17, each DB37 connector is used to access 16 channels of the associated I/Os (either analog or digital). With these interfacings, and involved interactions between two OP4500 modules, a hardware-in-loop (HIL) system of the proposed SSPS RSC-MLI is realized.

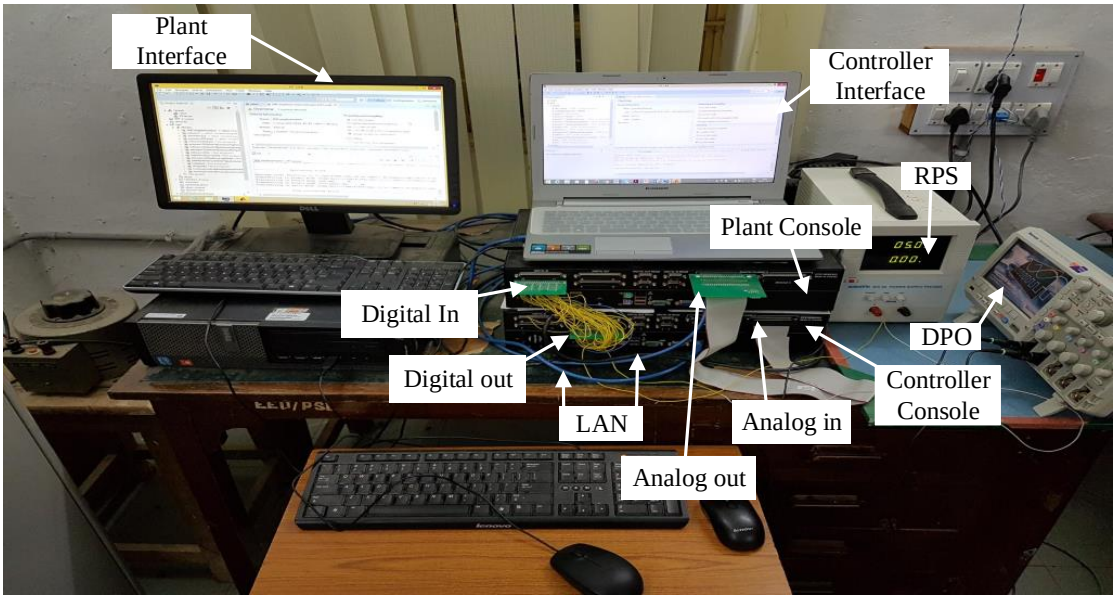


Fig. 4.15: HIL setup for the proposed system in real time.

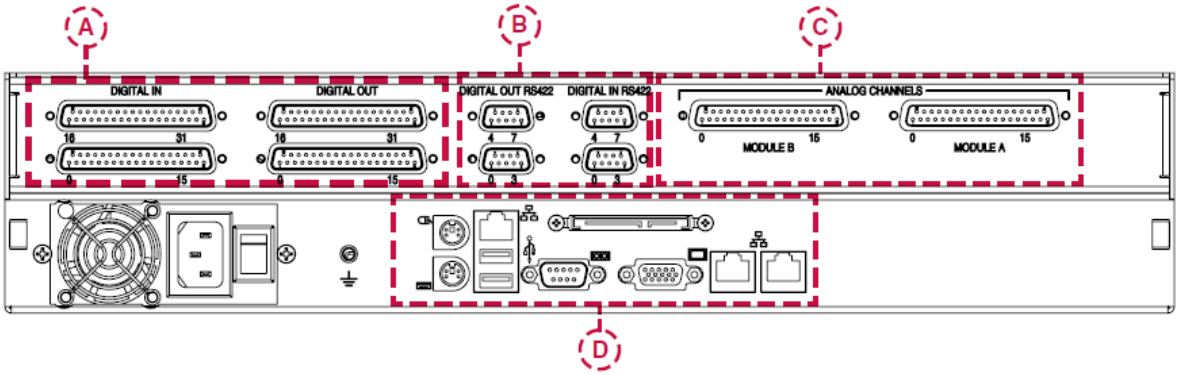


Fig. 4.16: View of rear interface OP4500 [180].

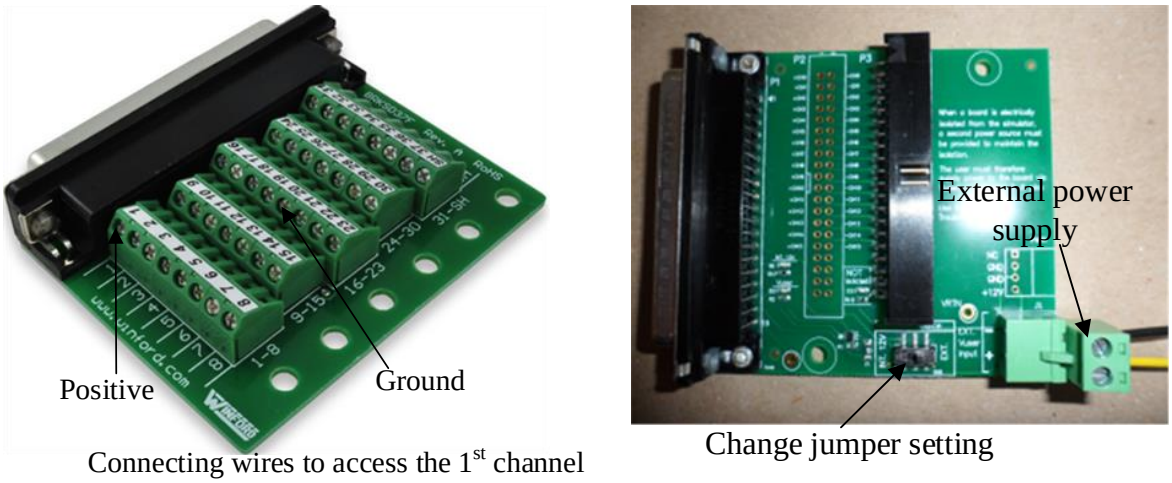
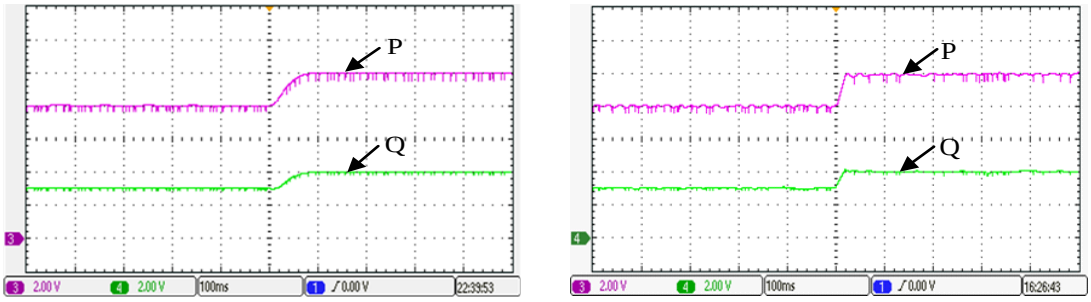


Fig. 4.17: DB 37 Screw terminals [180].

The responses for the closed-loop control system with SMC and PI control schemes are recorded by using digital storage oscilloscope (DSO). The performance comparison of the proposed three-phase RSC-SSPS based MLI in real-time environment is shown in Fig. 4.18 to Fig. 4.22, respectively for simulation responses given in Fig. 4.9 to Fig. 4.13. As it is inferred in

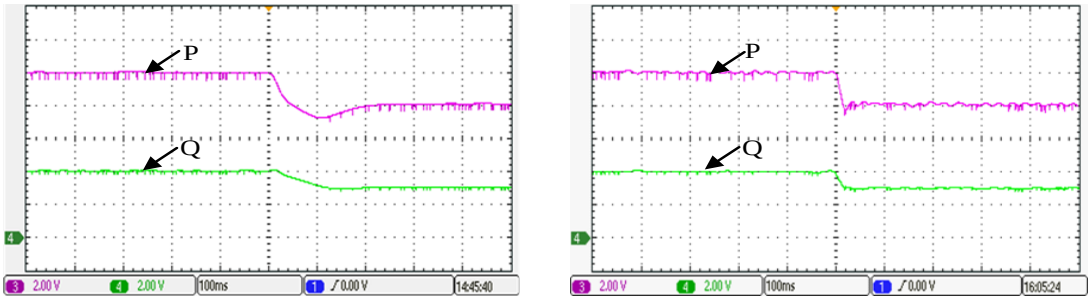
simulation results, except the slight delay in PI controller settling, both the PI and SMC are performing satisfactorily for both increase and decrease of power references which can be seen in Fig. 4.18 and Fig. 4.19.

The real-time validation of decoupling capability of SMC between real and reactive powers, as compared to PI controller, is shown in Fig. 4.20. In this case study, only reactive power reference is changed while keeping the real power reference as constant. As shown in Fig. 4.20(a), though the real power feeding is maintained at the reference value, it is experiencing transients with the only change in reactive power reference, if it is controlled by PI controller. Unlike, the real power feeding is unaffected by the disturbance in the reactive power feeding when the MLI is controlled by SMC as shown in Fig. 4.20(b).



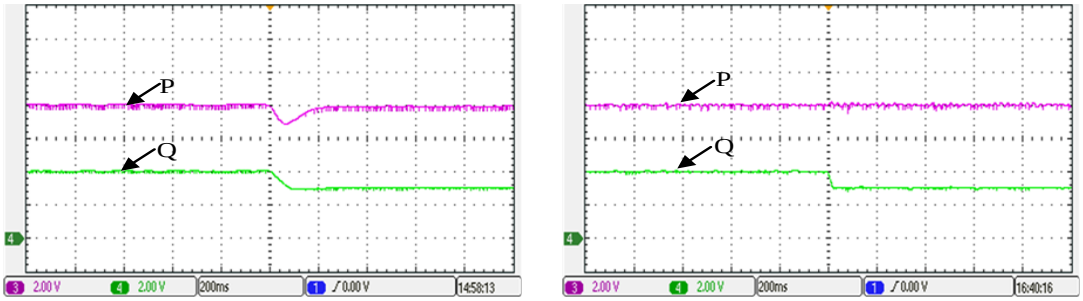
(a) (b)

Fig. 4.18: Powers feedings of MLI to the grid for step increase in reference with (a) PI controller (b) SMC (X-axis: 100 ms/div, Y-axis: 0.2 pu/div).



(a) (b)

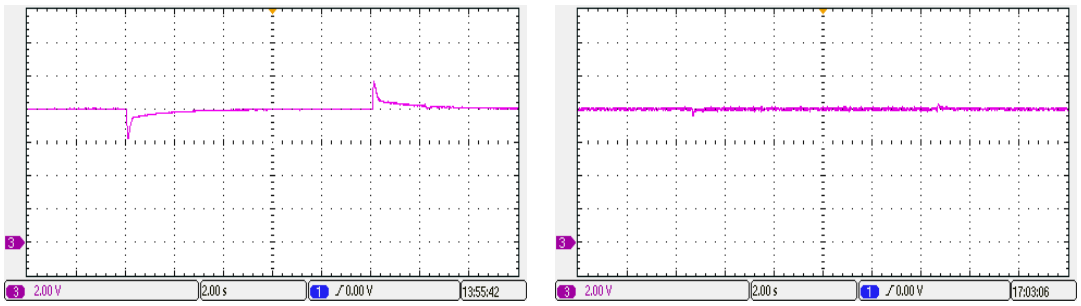
Fig. 4.19: Powers feedings of MLI to the grid for step decrease in reference with (a) PI controller (b) SMC (X-axis: 100 ms/div, Y-axis: 0.2 pu/div)



(a) (b)

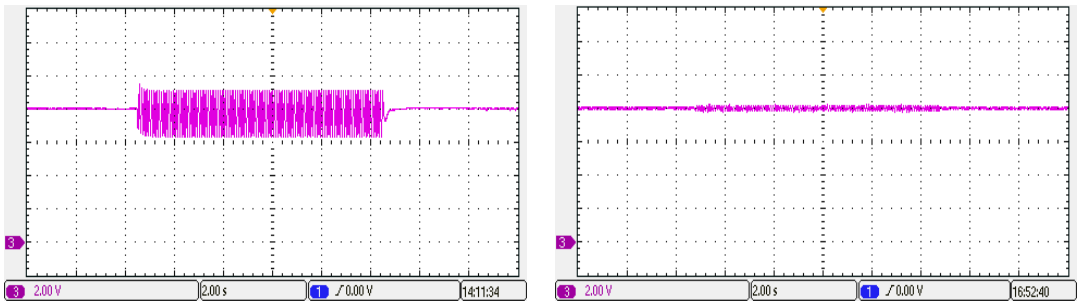
Fig. 4.20: Performance of MLI for decoupling control of real and reactive Powers feedings with (a) PI controller (b) SMC (X-axis: 200 ms/div, Y-axis: 0.2 pu/div)

The performance of the system with both the control schemes under grid frequency variations is shown in Fig. 4.21 and Fig. 4.22. For the change in grid frequency of 1 Hz, the PI controller is delivering power with overshoots/undershoots as shown in Fig. 4.21(a), while the SMC is able to adapt its gain and is ensuring smooth power delivery to the grid as shown in Fig. 4.21(b). For a continuous change in grid frequency which represents modal frequency oscillations, the PI is delivering quite oscillatory performance with large amount of power deviations as shown in Fig. 4.22(a). It can trigger the overcurrent protection of the converter. Hence, the response of PI controller which cannot adapt its gains, is a potential candidate to create instability in the system by disconnecting the converter which is supplying power to the grid. On contrary, the system with SMC is delivering almost a smooth power as shown in Fig. 4.22(b), thereby ensures that the converter remains connected to the grid during the disturbances. Therefore, it can be understood that the SSPS inverter with SMC can operate more firmly and can override the disturbances. Hence, confirming all the simulation responses discussed in Section 4.4.1.



(a) (b)

Fig. 4.21: P_{grid} for step changes in grid frequency with (a) PI controller (b) SMC (X-axis: 2s/div, Y-axis: 0.2 pu/div).



(a) (b)

Fig. 4.22: Real power feeding by RSC-SSPS based MLI to the grid for frequency oscillations with (a) PI controller (b) SMC (X-axis: 2 s/div, Y-axis 0.2 pu/div).

4.5 Summery

Sliding mode based nonlinear controller for the closed-loop operation of three-phase SSPS RSC-MLI with reduced number of switches is developed in this chapter. It is concluded that the control of MLI with PI is experienced large overshoots/undershoots in power delivery under grid frequency variations, there by activating the protection system of converter which disconnects the MLI from the rest of the system. On the other hand, with negligible overshoots/undershoots, the MLI with SMC has overridden the frequency disturbances and retained the inverter connected with the grid even under disturbances, thereby supporting system to regain its stability. The conclusions drawn from simulations are in corroboration with real-time results obtained from OPAL-RT 4500 controller.

CHAPTER 5: SMC FOR PV POWER EXTRACTION IN SINGLE-STAGE MLDCL RSC-MLI BASED GRID CONNECTED PV SYSTEM

This chapter presents the maximum power extraction control of three-phase single-stage asymmetric MLDCL RSC-MLI based grid connected PV system using common feedback linearized sliding mode control (FBLSMC) philosophy. A comprehensive comparison is presented in-between the proposed SMC and conventional PI control for PV power extraction under wide variations of irradiance conditions.

5.1 Introduction

The maximum power injection of PV sources into the grid through conventional MLI topologies is presented in [81, 110] with appreciable control objectives. In these approaches, the maximum powers from the nonlinear PV sources is obtained by conventional PI controllers. In general, the PI is linear controller and its performance is sensitive to operating point changes and/or to other disturbances. This is because the gains of PI controller are designed for a specific operating point only. If any changes in operating points or any short time uncertainties occur in the system, then the PI controller detunes and may result overshoots/undershoots with delayed response. Especially in high power applications, these overshoots in the response causes damage to switches in the inverter. So that, the use of fixed gain PI controller is a cumbersome process for extraction of maximum power from nonlinear PV sources during irradiance varying conditions. Further, the tuning process of multiple PI controllers becomes a challenging task in the case of individual maximum power extraction of each PV sources connected to individual H-bridges in CHB MLI [77, 81, 82, 110-113]. To overcome the drawback of the PI controller, it is necessary to linearize the nonlinear PV source and a suitable controller needed to be implemented for extraction of maximum PV power.

One of such controller is sliding mode controller (SMC), as introduced in Chapter 4, is suitable for both linear and nonlinear systems. SMC offer better dynamic performance than PI controller and results in undershoots/overshoots free response. The other controllers such as fuzzy-logic control [114] and back-stepping control [115] are used for maximum power extraction. However, these controllers are adapted for two-level inverter based dual stage systems and extending to higher level topologies is a tedious task. The power control of grid connected two-level converter under system parameter variations using SMC is reported in [85, 86]. However, the dynamic performance of both PI controller and SMC for maximum power generation from single-stage asymmetric PV sources under variable irradiance conditions has not yet reported.

Hence, this thesis proposes a 11-level asymmetric MLDCL RSC-MLI based PV system for integration to a 11 kV grid. In MLDCL RSC-MLI, asymmetric PV sources with 1: 2: 2 ratio is considered for generating 11-levels in the output voltage with minimum switch count. Furthermore, two SMCs are developed to extract maximum power from each group of equal rating PV sources. The superiority of SMC against PI controller for generation of maximum power from asymmetric PV sources under varying irradiance conditions is established in both MATLAB and hardware-in-loop OPAL-RT [181] based environments.

5.2 Proposed asymmetric 11-level MLDCL RSC-MLI based PV system

The proposed 11 kV grid connected system consists of three-phase 11-level MLDCL RSC-MLI with input PV sources is shown in Fig. 5.1. The maximum power of the PV source at different irradiance level can be obtained under the control of either conventional PI or SMC. In order to supply maximum power (P_{ref}) generated from the PV sources to the grid, a two-loop PI controller is involved to generate reference modulating voltages for inverter. The switching operation of inverter allows the controller to carry out its control objectives.

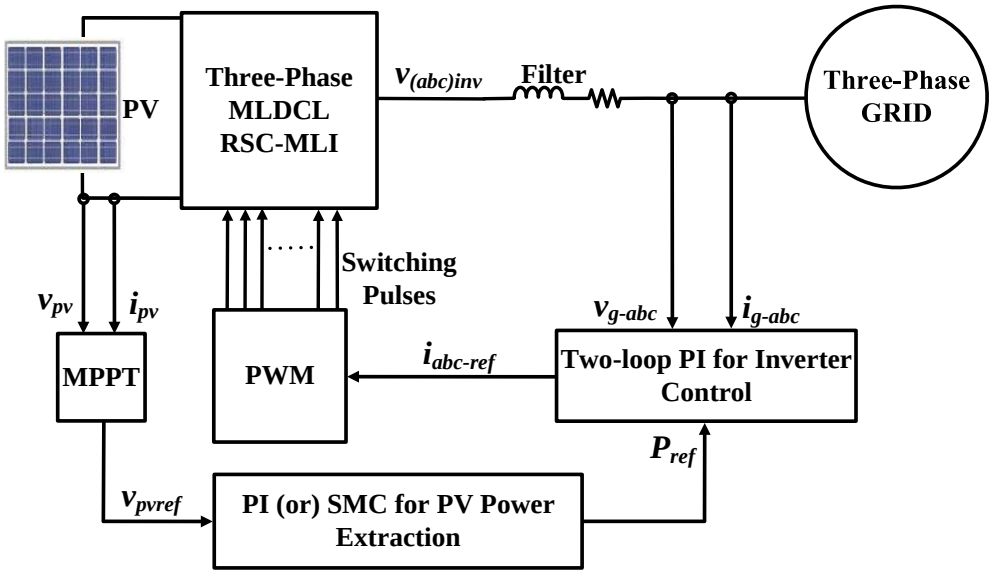


Fig. 5.1: Schematic layout of proposed grid integration of PV based MLI system.

5.2.1 Asymmetric 11-level MLDCL RSC-MLI

The three-phase structure of 11-level asymmetric MLDCL topology is shown in Fig. 5.2. In each phase of MLDCL RSC-MLI, three PV sources (i.e., PV_0, PV_1 and PV_2) are powering each sub module in the phase. The PV sources, PV_0, PV_1 and PV_2 are in 1: 2: 2 voltage ratio, corresponding to their MPPT powers. In Fig. 5.2, there are three PV_0, six PV_1 (i.e., three PV_1 and three PV_2) sources are connected to three-phase of 11-level MLDCL topology. As discussed in Section 3.2.1, the structure of this topology is divided into two parts, namely, level generator and

polarity generator. The level generation part can be formed by cascade connection of half bridge cells. Each half bridge cell is powered from a PV source of two different voltage levels. The switching states of MLDCL RSC-MLI shown in Fig. 5.2 to obtain 11-levels in phase-voltage is given in Table 5.1. From this table, it can be observed that MLDCL have following features.

- ❖ Identical switching operation in level generator for obtaining positive and negative voltages levels.
- ❖ Voltage stress on the operating devices (level generator) remains same for any number of levels.
- ❖ The dc link voltage balance is possible with the presence of adequate switching redundancies.

In order to obtain 11-levels with PV voltage ratio of 1: 2: 2, the number of switches required for three-phase asymmetric CHB is 36 as compared to 30 in MLDCL. Hence, Asymmetric configuration will reduce the switch count. Further, a common maximum power extraction control can be used for all equal voltage rated PV sources. This will reduce the cost and complexity of controller. In this work, the designed PV based asymmetric MLDCL is connected to 11 kV grid for supply of PV power. For generating 11 kV line-voltage (RMS) from the output of MLDCL, the required voltages (V_{mppt}) which would be generated from individual PV sources (PV_1, PV_2 and PV_0) of each phase of MLDCL MLI at 100% of irradiance (1000 W/m^2) are PV_1 = 3200 V, PV_2 = 3200 V and PV_0 = 1600 V. The required data for design of PV_1 (or PV_2) and PV_0 source is given in Table 5.2. In simulation study, to obtain 1600 V PV source, 5 parallel and 2020 series PV cells are required. Similarly for 3200 V PV source, 5 parallel and 4040 series PV cells are required.

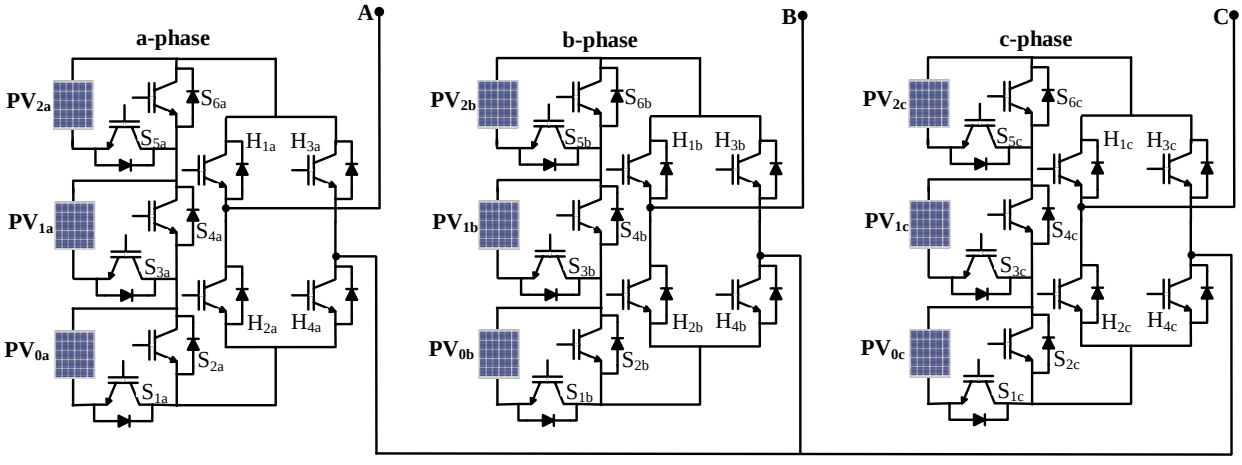


Fig. 5.2: Three-phase 11-level asymmetric (PV_0 = V, PV_1 = PV_2 = 2V) MLDCL RSC-MLI.

Table 5.1: Switching states and phase voltage of 11-level asymmetric MLDCL MLI.

Phase-voltage level	Switches operate in level generator	Switches operate in polarity generator
+5V	S_1-S_3-S_5	H_1-H_4
–5V		H_2-H_3
+4V	S_2-S_3-S_5	H_1-H_4
–4V		H_2-H_3
+3V	S_1-S_3-S_6 (or) S_1-S_4-S_5	H_1-H_4
–3V		H_2-H_3
+2V	S_2-S_3-S_6 (or) S_2-S_4-S_5	H_1-H_4
–2V		H_2-H_3
+V	S_1-S_4-S_6	H_1-H_4
–V		H_2-H_3
0	----	H_1-H_3 (or) H_2-H_4

Table 5.2: The data regarding PV_1 (or PV_2) and PV_0 source

Parameter	Value
Number of parallel and series cells (*Np* and *Ns*) for generate MPPT voltage of 3200 V from PV_1 (or PV_2) source	5 and 4040
Number of parallel and series cells (*Np* and *Ns*) for generate MPPT voltage of 1600 V from PV_0 source	5 and 2020
Cell's short circuit current (I_{sc})	8.03 A
Cell reverse saturation current, I_{rs}	$1.2e^{-7}$A
Charge of an electron, q	1.602×10^{-19} C
Boltzmann's constant, k	1.38×10^{-23} J/K
Ideality factor, A, Cell's reference temp, T_{ref}	1.92, 300 K
Short circuit current temperature co-efficient of cell, K_I	0.0017

5.2.2 Control of power from PV sources of asymmetric MLDCL RSC-MLI

In solar based energy generation system, the primary element is PV module. The characteristics and its design considerations PV module explained in [182] is considered in this thesis. The methodology of the proposed system (shown in Fig. 5.1) to extract maximum power from PV sources and injection of extracted power to the grid with PI and proposed SMC are explained below.

5.2.2.1 Extraction of maximum power from PV with PI control

For extracting maximum power (P_{max}) from PV source, in literature, conventional PI controller along with maximum power point tracking algorithm (MPPT) is used [86]. The process of deriving P_{max} from conventional PI control is given in Fig. 5.3. In Fig. 5.3, the input to the PI controller is the error between V_{dcref} and actual V_{pv} and the output is I_{dcref}. In this thesis, the voltage (V_{dcref}) which is corresponding to maximum power of PV source is obtained by P & O MPPT algorithm [86].

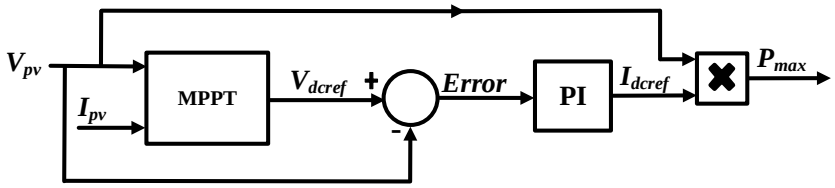


Fig. 5.3: Maximum power extraction from PV source using conventional PI controller.

Power extraction using PI based MPPT controller is a simple method. However, the three-phase proposed 11-level asymmetric MLDCL MLI consists of multiple PV sources with two different voltage ratings i.e., V and 2V as shown in Fig. 5.2. In order to extract maximum power from PV sources, two PI controller are required, one for V (i.e., PV_0) and other for 2V source (i.e., PV_1 and PV_2). Tuning of two PI controllers for extracting the powers from two different ratings of non-linear PV sources in the grid connected MLI system is a challenging task. Further, during the insolation changes, the conventional PI control may generate overshoots/undershoots with delayed response of P_{max}. In order to avoid these disadvantages, it necessary to linearize the non-linear PV sources using an effective linearization scheme and a robust nonlinear controller can be adapted instead of conventional linear PI controller for extracting maximum power from PV sources. Further, the proposed non-linear controller should able to give fast dynamic response without any overshoots/undershoots in response to irradiance changes. One of such linearization scheme is feedback linearization technique and one of such non-linear controller is SMC and explained below.

5.2.2.2 Linearization of non-linear PV source

This section describes the input-output linearization scheme to develop non-linear controller to extract maximum power from PV source. Once the linearized model is developed for non-linear PV system, a robust SMC can be developed to obtain non-linear control quantities. The non-linear transformation of PV system involves the implementation of feedback linearization scheme. This technique can avoid degraded performance of controller because of irradiance changes. Further, this in turn allows the PV source to be controlled for wide range of irradiance levels.

The PV source shown in Fig. 5.4 with a parallel capacitor *C* can be represented as mathematical equations (5.1) and (5.2).

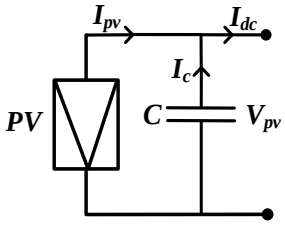


Fig. 5.4: Photovoltaic source.

$$I_c + I_{pv} = I_{dc} \tag{5.1}$$

$$I_{pv} + C\frac{dV_{pv}}{dt} = I_{dc} \text{ (or) } \frac{dV_{pv}}{dt} = -\frac{1}{C}I_{pv} + \frac{1}{C}I_{dc} \tag{5.2}$$

Where, I_{pv}, I_c and I_{dc} are PV current, capacitor current and dc-link current respectively.

The above non-linear equation (5.2) can be converted to linear equation by converting into state-space representation, which is shown below.

$$\frac{dh}{dt} = f_{pv}(h) + g_{pv}(h).u_{pv} \tag{5.3}$$

The state-space equation of PV source is obtained by converting equation (5.2) into (5.3) and results as (5.4) with V_{pv} as state variable.

$$h = [V_{pv}] \quad g_{pv}(h) = \left[\frac{1}{C}\right] \quad f_{pv}(h) = \left[\frac{-1}{C}I_{pv}\right] \quad u_{pv} = [I_{dc}] \tag{5.4}$$

After linearization, the new transferred PV system can be represented as

$$U_{pv} = (-g_{pv}{}^{-1}(h) \times f_{pv}(h)) + (g_{pv}{}^{-1}(h) \times \delta_{pv}) \tag{5.5}$$

Equation (5.5) can also represented in the following form as

$$U_{pv} = \alpha_{pv}(h) + (\beta_{pv}(h) \times \delta_{pv}) \tag{5.6}$$

Where $\alpha_{pv}(h) = -g_{pv}{}^{-1}(h) \times f_{pv}(h)$, $\beta_{pv}(h) = g_{pv}{}^{-1}(h)$ and δ_{pv} is the state vector matrix with dV_{pv}/dt is as an element.

$$\text{i.e., } \quad \delta_{pv} = [\delta_{11}]^T = \left[\frac{dV_{pv}}{dt}\right]^T \tag{5.7}$$

For PV source, the output parameter is also V_{pv} and hence the output matrix is defined as equation (5.8):

$$Y_{pv} = [V_{pv}] \tag{5.8}$$

5.2.2.3 Adaption of SMC for PV power extraction

Sliding mode control [85, 86] is a robust control method and it is successfully tested for control of linear and non-linear systems. Due to its infinite gain, it nullifies the errors associated with system parameter changes, operating point changes and uncertainties in the system. In this control technique, the state of the system is brought back toward the sliding surface and commutated up to the equilibrium point. The switching and sliding surface do not depend upon the operating point, circuit parameters and converter dynamics. In this chapter, SMC is used to obtain new δ_{pv} and subsequently U_{pv} as in (5.5) for achieving controlled PV power.

5.2.3 Development of sliding surface and its stability concept

The obtained state matrix δ_{pv} in linearization of PV source as discussed in previous section is the input for SMC and it is going to change from old to new state vector until the actual value of a quantity reached reference value. The output of SMC is reference control $U_{pv}(t)$, i.e., I_{dcref} which is responsible for obtaining maximum PV power. $U_{pv}(t)$ is a combination of equivalent control and switching control. Equivalent control can be obtained from the process of system linearization while switching function has accomplished the process of cancelling the error in output states V_{pv}.

$$U_{pv}(t) = U_{pr}(t) + U_{sw} = U_{pr}(t) + M \tanh(S_{pv}) \tag{5.9}$$

Where, M is a constant and S_{pv} is a sliding surface. For efficient operation of the controller, it is necessary to define sliding surface. There exists one sliding surface S_{PV}, since equation (5.8) has only one output state, V_{pv}. The sliding surface which is a function of error is defined below.

$$S_{pv} = error = (V_{pv} - V_{dcref}) \tag{5.10}$$

Hence in this work, error in variable parameter V_{pv} is chosen as the sliding surface. The state of the PV system is directed by the SMC towards the equilibrium point at which the error becomes zero and it is achieved by considering Lyapunov approach as shown below.

$$L = \frac{1}{2} {S_{pv}}^2 \tag{5.11}$$

As stated in Lyapunov stability concept, the PV system is asymptotically stable if L is positive definite and its derivative i.e., dL/dt is negative.

$$\text{i.e., } \frac{dL}{dt} = (S_{pv} \times \dot{S}_{pv}{}^T) < 0 \tag{5.12}$$

To satisfy the above condition $(S_{pv} \times \dot{S}_{pv}{}^T) < 0$, $\dot{S}_{pv}$ is represented as $M.sign(S_{pv})$.

$$\text{i.e., } \dot{S}_{pv} = -M.sign(S_{pv}) \tag{5.13}$$

However, the controller performance is highly chattering because of the *sign* function which is a hard switching function. In order to improve the controller performance with chattering free and for continuous switching, a hyperbolic tangent function [85] is considered in this work. Hence, according to the new chosen soft switching function, equation (5.13) is modified as,

$$\dot{S}_{pv} = -M.\tanh(S_{pv}) \tag{5.14}$$

Substituting (5.10) in (5.14),

$$\dot{S}_{pv} = -M.\tanh(V_{pv} - V_{dcref}) \tag{5.15}$$

Using the new dynamics of SMC, the new state vector of PV source can be represented as:

$$\delta_{pv-new} = [\delta_{11}] = [-M.\tanh(V_{pv} - V_{dcref})] \tag{5.16}$$

Where, V_{dcref} can be obtained from P & O MPPT algorithm. Fig. 5.5 shows the schematic of achieving for maximum power of PV source, P_{max} using SMC. The same procedure is implemented for PV sources (PV_0, PV_1 and PV_2) of the proposed asymmetric three-phase MLDCL RSC-MLI to achieve maximum power from all of them.

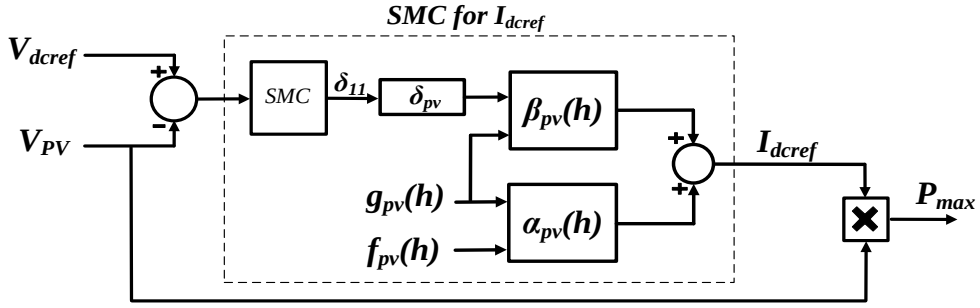


Fig. 5.5: Realization of maximum power from PV source using SMC.

5.3 Control of MLDCL RSC-MLI using two-loop PI controller

The main control objective of the proposed system is to supply all the maximum powers of asymmetric PV sources into the grid at various irradiance conditions. This objective can be attained by controlling MLDCL RSC-MLI using a single-loop based PI controller to which the input is error between the sum of the powers of PV sources as P_{ref} and grid power, P_g. The output of this controller is modulating or reference voltages required for PWM scheme. However, this single-loop direct power control scheme cannot process the errors in the currents. Due to the absence of current loop, it may results overshoots in the current and activates protection circuits in the converters which lead to discontinuity in the operation. In order to avoid the overshoots in the currents, a two-loop PI control scheme is considered as shown in Fig. 5.6. In this control scheme, two sets of PI controllers are involved. The first set of PI controller processes the power error and generates reference currents in *d-q* frame of reference. These reference currents are compared

with grid currents and generate current error. The derived current error is given as input for second set of PI controller which gives modulating voltages as output as shown in Fig. 5.6.

Fig. 5.6 shows the grid integration of asymmetric PV sources (PV_1= PV_2= 2V and PV_0=V) through three-phase MLDCL RSC-MLI. The extraction and injection of PV power into the grid is carried out using SMC and two-loop PI controllers respectively and the schematic procedure is shown in Fig. 5.6. Since the proposed asymmetric MLDCL MLI facilitate the redundancies for obtaining the output voltage levels, there is a benefit of uniform or even power distribution between equal rated PV_1 and PV_2 sources. Thus, a common MPPT control mechanism can be used for both PV_1 and PV_2 sources thereby avoiding one extra controller and hence reducing the control complexity. The other PV source, PV_0 is controlled by another MPPT controller since it has half of the *I-V* ratings as compared to PV_2 or PV_1. Therefore, two SMCs are developed to extract maximum power from each group of equal rating PV sources. In three-phase MLDCL MLI, there are six equal *I-V* rated PV sources (i.e., three PV_2 and three PV_1) and three PV_0 sources. Therefore, in order to extract maximum power from each group of equal rating PV sources, the power of single PV_1 source is multiplied with a gain of six. Similarly, a gain of three is used to the power of single PV_0 source as shown in Fig. 5.6. The total PV power is sum of the powers of six PV_1 (or PV_2) sources and three PV_0 sources and it is considered as P_{ref} to two-loop PI control strategy.

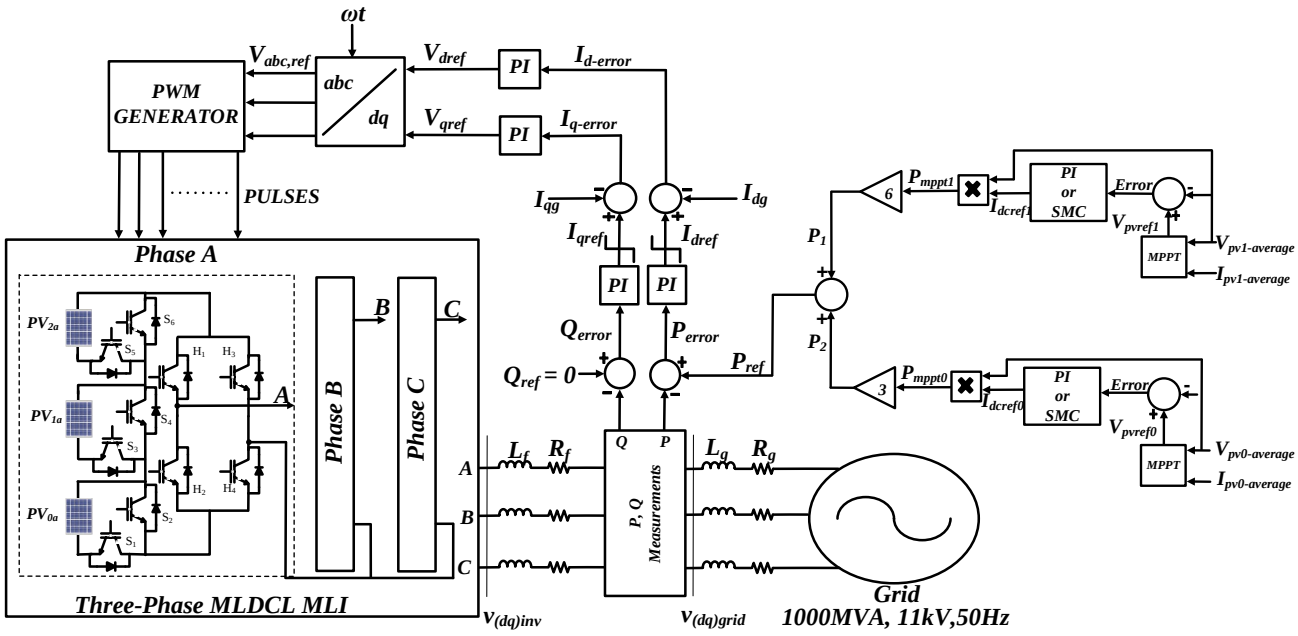


Fig. 5.6: The schematic diagram of grid connected PV based MLDCL MLI system using SMC and PI controllers.

5.4 Results analysis

In this section, the performance of PI and SMC controllers for maximum power generation from input PV sources of the proposed closed-loop MLI based grid connected system under

various irradiance conditions is studied in MATLAB/Simulink and the results obtained are validated in real-time OPAL-RT platform.

5.4.1 MATLAB/Simulink results

The maximum power generation from PV sources using PI controller and SMC is discussed in Section 5.2.2. The injection of generated power to the grid using two-loop PI controller is developed as shown in Fig. 5.6. The comparative analysis between PI and SMC is considered for 1200 W/m^2, 1000 W/m^2, 900 W/m^2, 800W/m^2 and 600 W/m^2 irradiance levels. In this work, 1000 W/m^2 is considered as 100% irradiance. The PV_0, PV_1 and PV_2 sources have MPPT voltages of 1600 V, 3200 V and 3200 V at an irradiance of 1000 W/m^2 (100%) respectively. The maximum powers and corresponding voltages of PV sources at different irradiance levels is shown in Fig. 5.7. The parameters taken for the proposed system is listed in Table 5.3. The generated 11-level output voltage from the proposed MLI is shown in Fig. 5.8. The percentage of THD in the generated output voltage is 12.1%. All the PV powers are represented in per unit (pu) based system with a base power of 1 MVA.

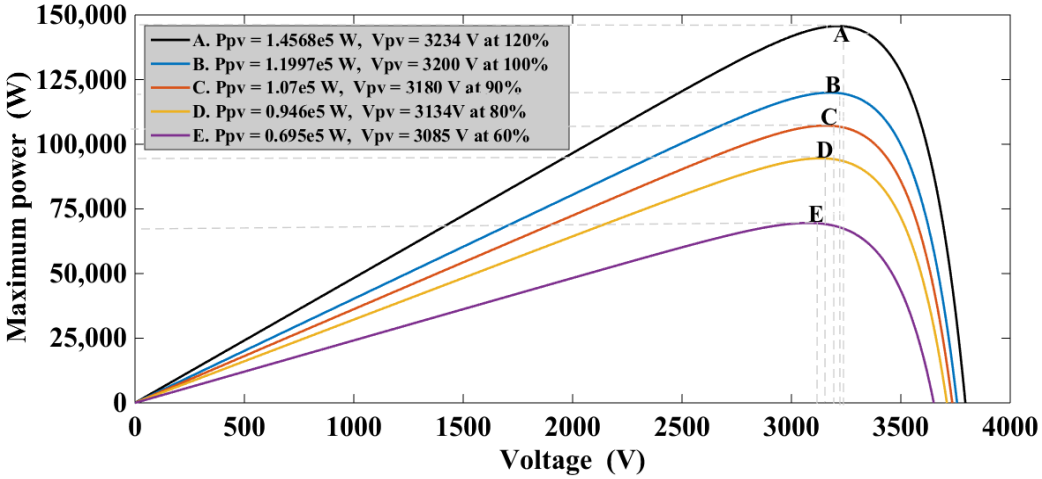


Fig. 5.7: *P-V* characteristics of PV source under various irradiance levels.

Table 5.3: Parameters considered for the proposed system

Parameter	Value
Grid Voltage, V_g	11 kV
Grid frequency, f	50 Hz
Filter inductance, L_f	50 mH
Filter Resistance, R_f	0.2 Ω
Capacitor across PV panel, C	0.01 F
Switching frequency, f_s	5 kHz
Sample time, T_s	50 µs
Base power	1 MVA
Short circuit MVA	1000 MVA

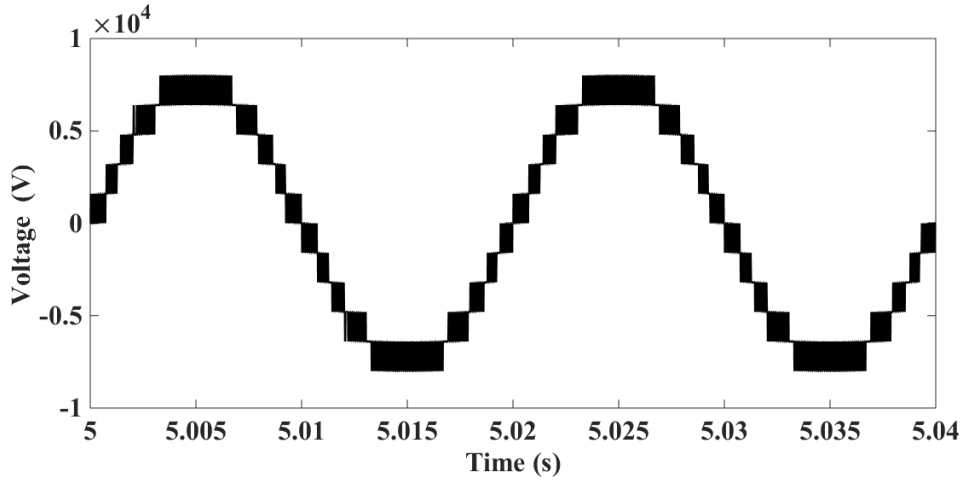


Fig. 5.8: Output voltage of Single-phase 11-level MLDCL MLI.

The design of filter inductance, L_f mainly depends on the grid current ripples and switching frequency f_s. The filter inductance is given as in [183]

$$L_f = \frac{1.6V_m}{4hf_{s\max}} \tag{5.17}$$

Where, V_m is peak of the phase-voltage and h is allowable ripple band in grid current of 1 MVA, 11 kV system. Normally h is taken as 5% of the grid current. f_{smax} is the maximum switching frequency and it is considered as 20 kHz. The design value of capacitor (C) across the PV sources is given by [184].

$$C = \frac{2 \times P_{pv}}{4 \times (2 \times \pi \times f) \times V_{pv} \times \Delta V_{pv}} \tag{5.18}$$

Where ΔV_{pv} is the maximum value of the allowed ripple in the voltage (V_{pv}) of the PV source and f is the fundamental frequency of the grid voltage. The value of V_{pv} of the PV source is taken is 3200 V and its corresponding power (P_{pv}) is 0.12MW as shown in Fig. 5.7.

Fig. 5.9 shows the maximum power of PV_1 or PV_2 source using PI controller and SMC. From Fig. 5.9 it is observed that during irradiance changes, the maximum power extraction using PI results larger overshoot and undershoots when compared with SMC. Fig. 5.10 represents the maximum power of PV_0 source using PI and SMC. Both Fig. 5.9 and Fig. 5.10 confirm that the delayed performance of PI controller during irradiance changes. On the other hand, SMC gives faster response.

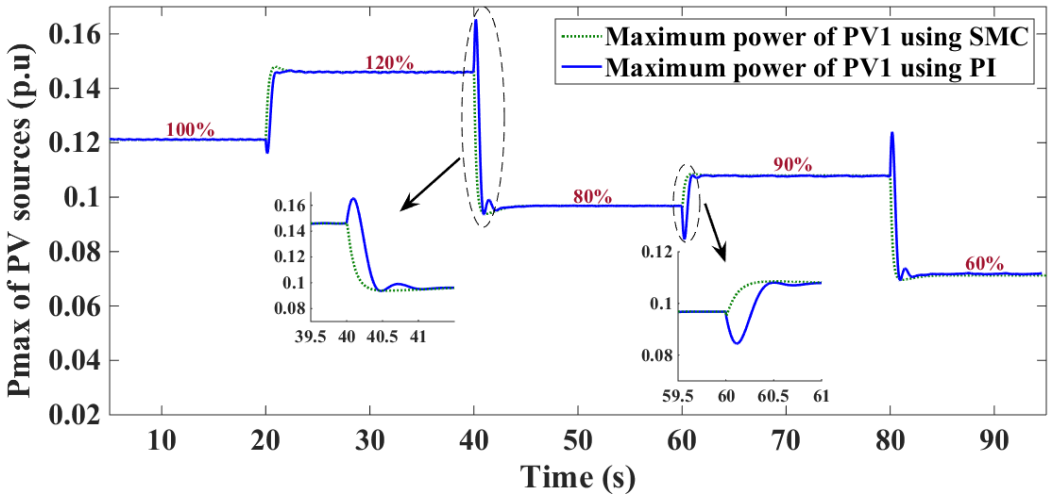


Fig. 5.9: Comparative performance of PI and SMC for extraction of maximum power from PV_1 (or) PV_2 source of MLDCL MLI at various irradiance levels.

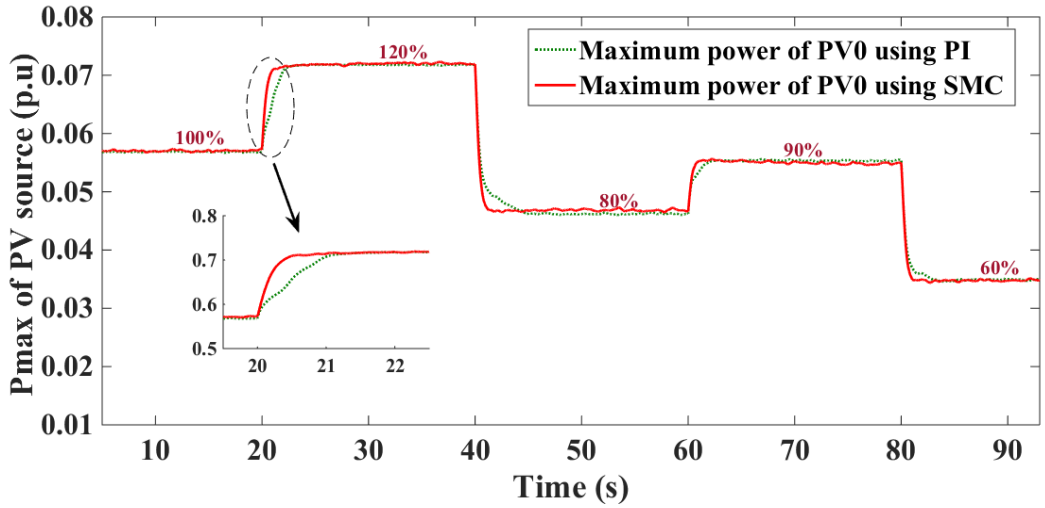


Fig. 5.10: Comparative performance of PI and SMC for extraction of maximum power from PV_0 source at various irradiance levels.

The performance of both PI and SMC controllers for achieving MPPT voltage across PV_1 or PV_2 is shown in Fig. 5.11. Whenever the irradiance changing from 100% to 120%, a large overshoot in the voltage (V_{PV1}) is observed and this is because of degraded performance of PI controller. Similarly at 40 s, the PI controller performance causes undershoot in the output voltage as shown in Fig. 5.11. Since the PI controller consists of fixed gains and is unable to adapt the gains according to irradiation changes and error, it delivers highly oscillating performance with large overshoots/undershoots in PV power and in corresponding voltages. Whereas SMC can adapt its gains according to error ($V_{dcref}-V_{pv}$), quick irradiance changes and exhibits extraordinary performance while delivering the output with very less overshoots/undershoots and settles within very less time as shown in Fig. 5.11. Similarly the superior performance of the SMC while achieving the desired voltage (V_{PV0}) corresponding to maximum power of PV_0 is shown in Fig. 5.12.

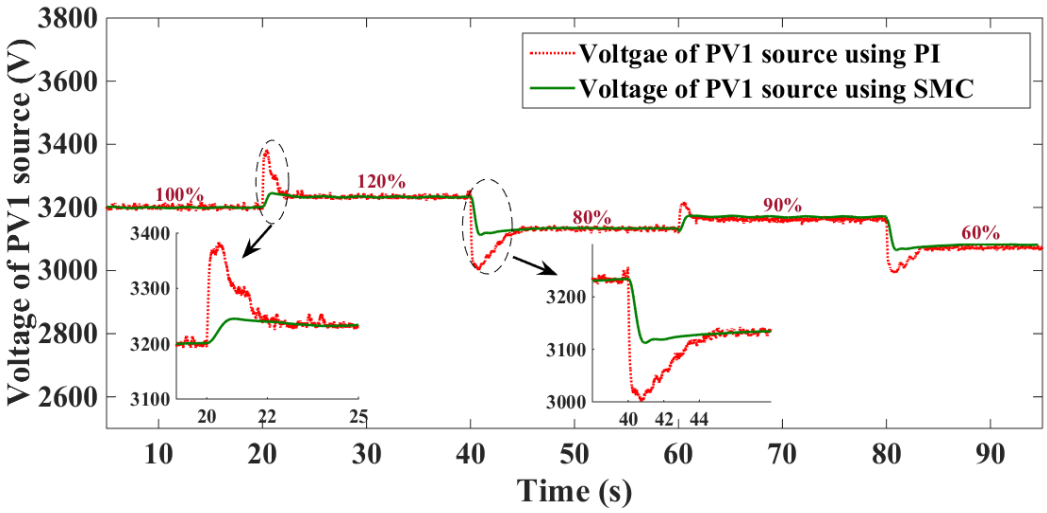


Fig. 5.11: Comparative performance of PI and SMC for obtaining desired voltage across PV_1.

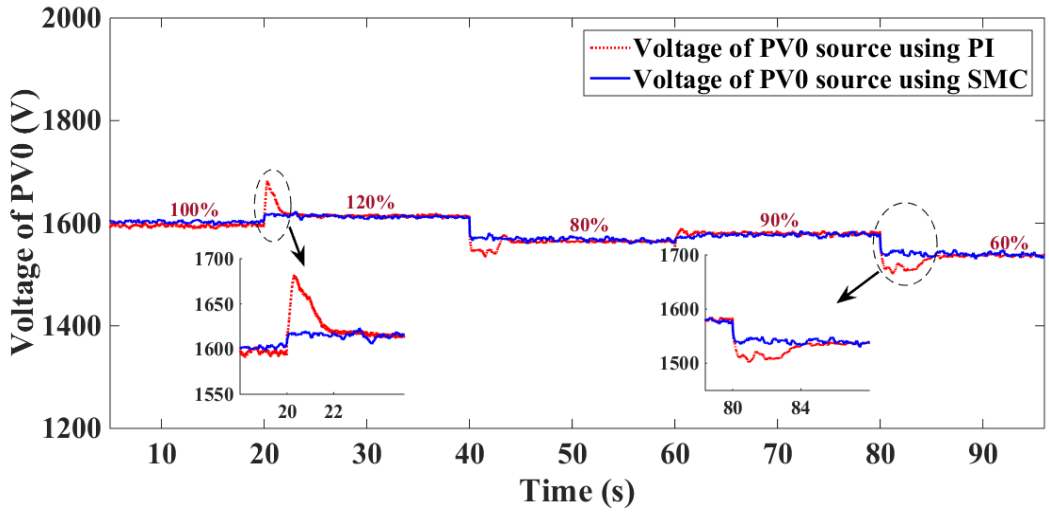


Fig. 5.12: Comparative performance of PI and SMC for obtaining desired voltage across PV_0.

Fig. 5.13 and Fig. 5.14 represent the sum of the maximum powers of six PV sources (i.e., $3PV_1$ and $3PV_2$) and maximum power of $3PV_0$ sources of the proposed three-phase MLDCL MLI respectively. By observing the sum of individual PV powers at different irradiance levels as shown in Fig. 5.13 and Fig. 5.14, it is confirmed that all the individual PV sources of three-phase MLDCL inverter are delivering their maximum powers according to their PV characteristics. Further, Fig. 5.13 and Fig. 5.14 again confirm superior performance of SMC over PI controller during the maximum power extraction from all PV sources of the three-phase system.

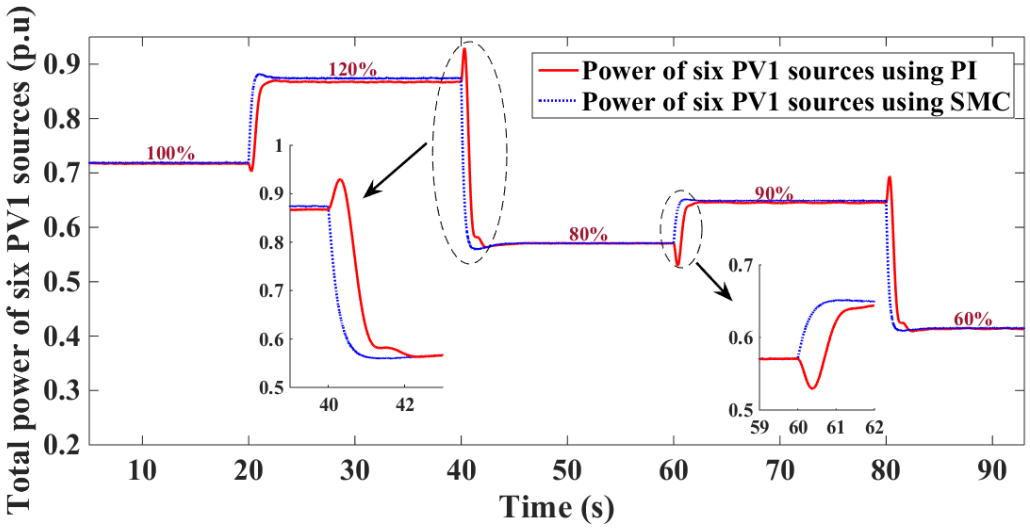


Fig. 5.13: Total power extraction of six PV_1 (or PV_2) sources of three-phase MLDCL RSC-MLI using PI and SMC.

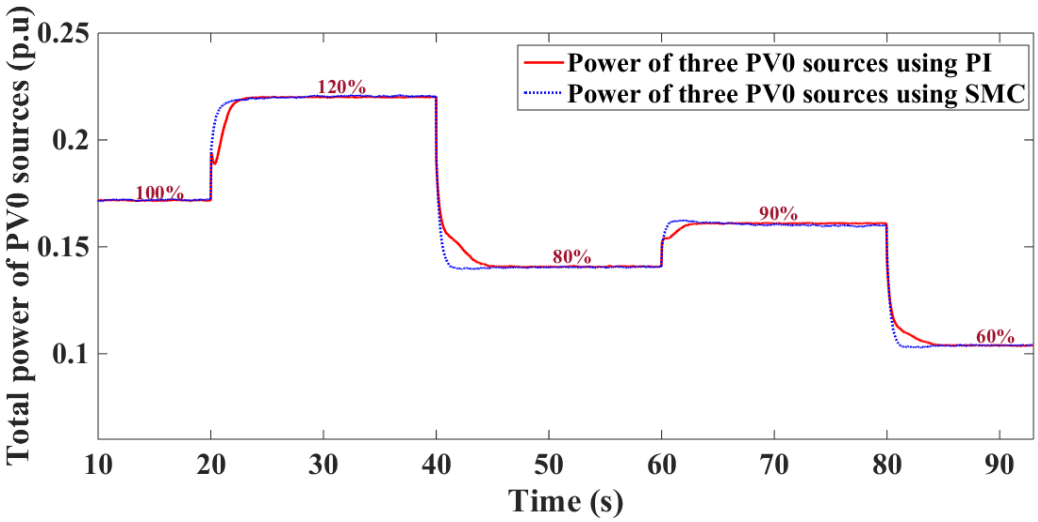


Fig. 5.14: Total power extraction of three PV_0 sources of three-phase MLDCL RSC-MLI using PI and SMC.

Fig. 5.15 shows the injected PV power to grid and final grid power (P_g). The total injected PV power is considered as reference (P_{ref}) to the two-loop PI controller which controls the MLI in such a way that it can supply P_{ref} to the grid for the considered irradiance levels. From Fig. 5.15, it is confirmed that the PV power generated is completely supplied to the grid under the control of two-loop PI control.

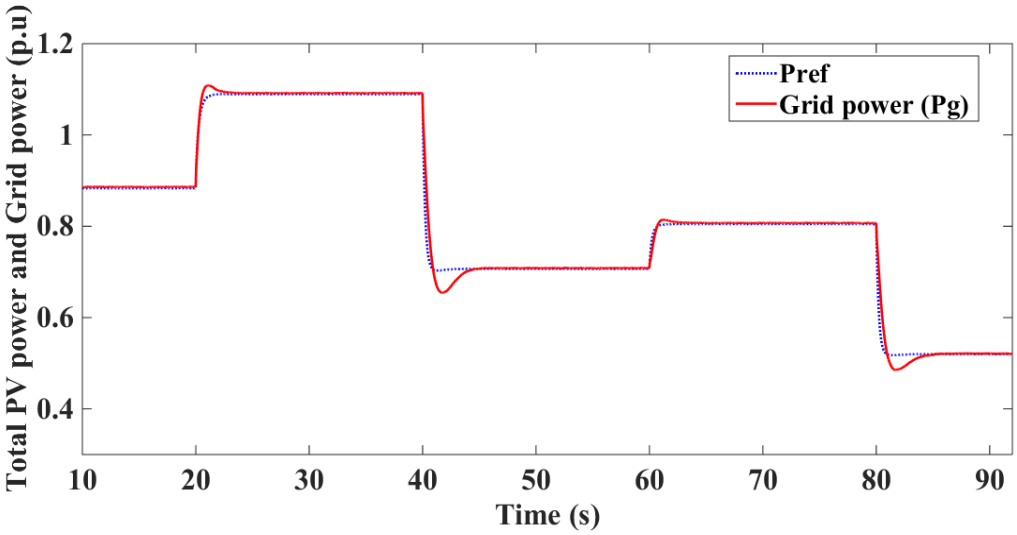


Fig. 5.15: Total generated PV power as P_{ref} and grid power (P_g).

5.4.2 OPAL-RT hardware-in-the-loop (HIL) results

The proposed grid connected PV based MLI system under the control of SMC and PI controller is validated in real-time using OPAL-RT modules. The schematic view of hardware-in-the-loop [181] testing of the proposed system using two OP-4500 modules is shown in Fig. 5.16 and the corresponding photograph is shown in Fig. 5.17. The control signals between two OPAL-RT modules are processed by considering three-phase MLDCL MLI connected to the grid is in one module works as plant and SMC or PI controller with PWM method is in another module as a controller. The communication between plant and controller systems is made through DB-37 connecter by scaling down the real-time control parameters shown in Fig. 5.16. The sample time and system parameters considered for execution of proposed system in real-time environmental setup is the same as simulation study. The PWM strategy is designed in such a way that the MLDCL RSC-MLI considered in the study generates 11-level phase-voltages as shown in Fig. 5.18.

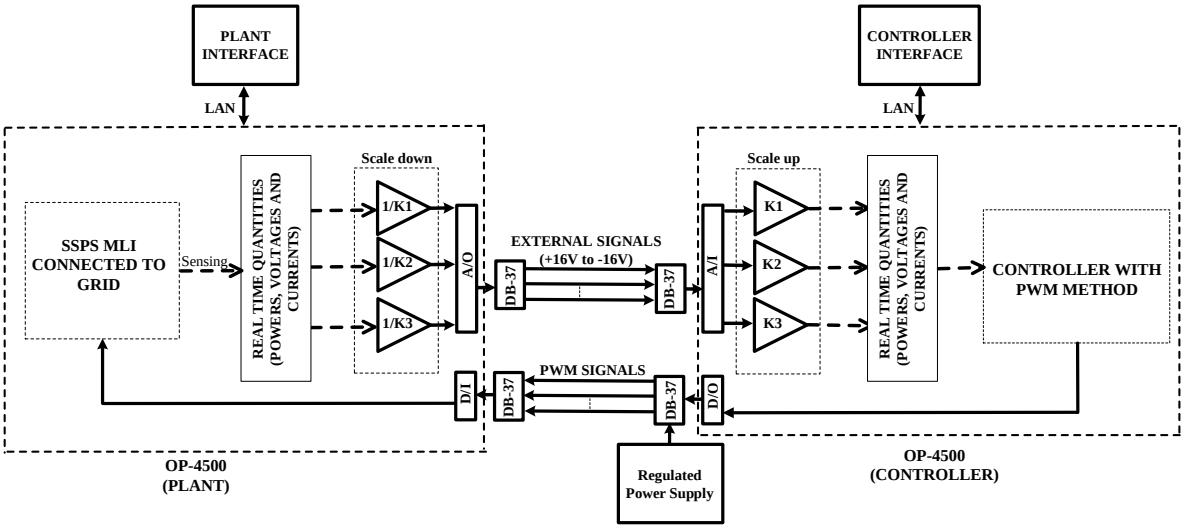


Fig. 5.16: Schematic layout of the proposed closed-loop system in HIL environment.

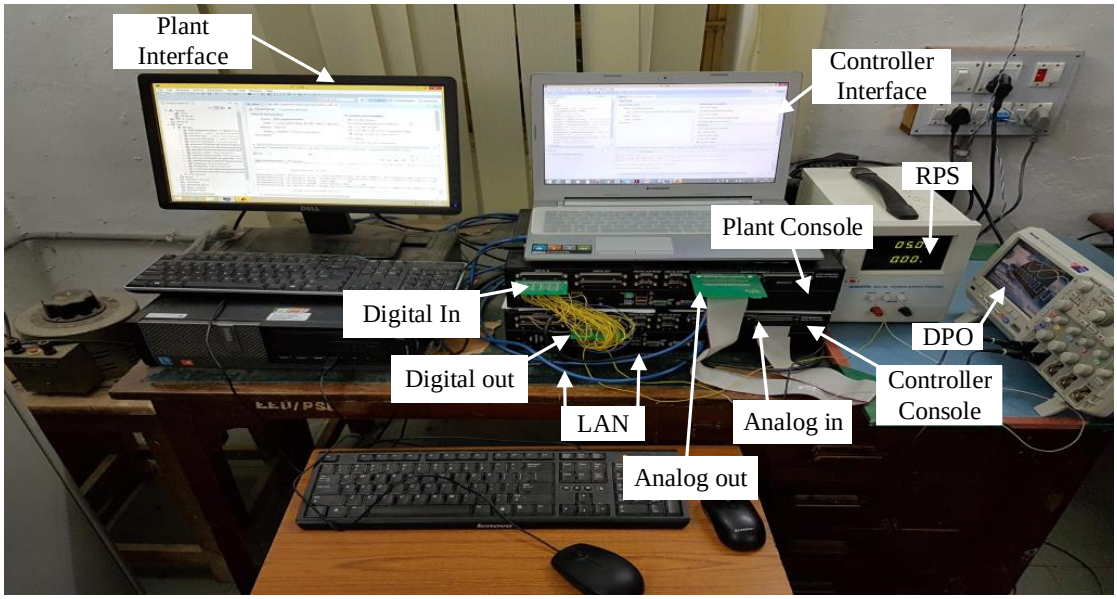


Fig. 5.17: HIL setup for the proposed system in real time.

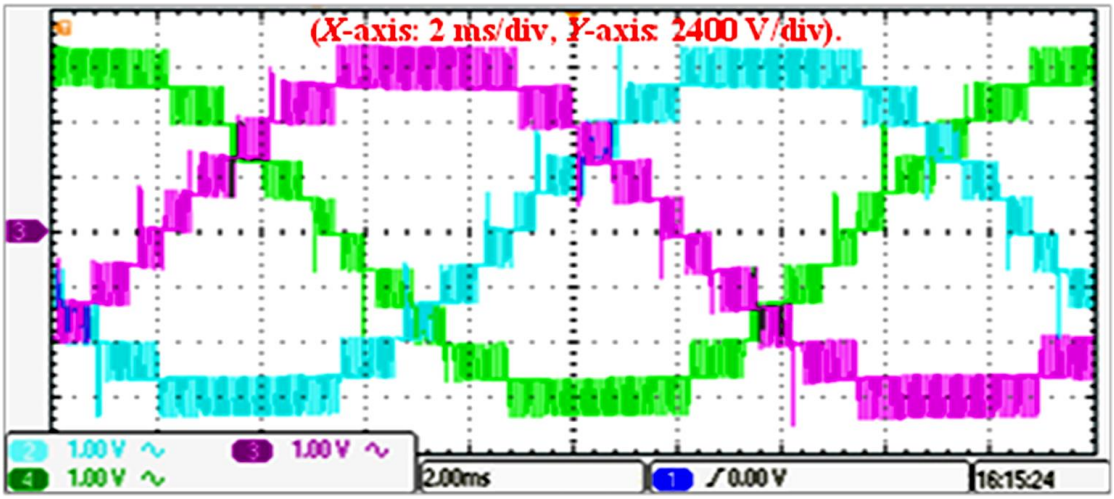
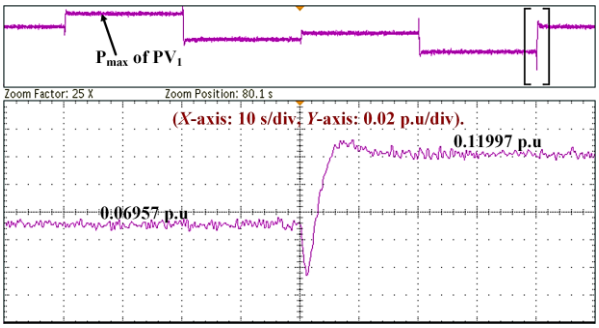
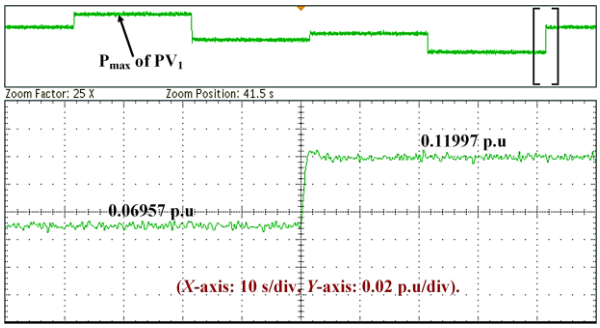


Fig. 5.18: Three-phase voltages of eleven-level MLDCL RSC-MLI.

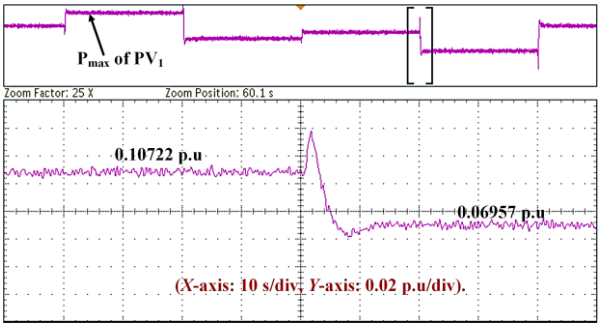
Fig. 5.19(a) and Fig. 5.19(b) represent the change of maximum power of PV_1 source under control of PI and SMC respectively. From Fig. 5.19(a), it is observed that while irradiance is changing from 60% to 100%, PI controller results a large undershoot in the power and it settles in nearly 20 cycles which is high in real case. On the other hand, PV power extraction using SMC results good response without under/overshoot and settles to new maximum power point within 3 to 4 cycles and this is confirmed by observing Fig. 5.19(b). Similarly PI controller results a large overshoot in power response as shown in Fig. 5.19(c) and Fig. 5.19(g) during irradiance transition from 90% to 60% and 120% to 80% respectively. These large overshoots may damage the switches in inverter and cause discontinuity in system operation. In order to avoid this, an extra protection circuit is needed, which leads to increase in complexity and cost. Whereas the power extraction with SMC shows better performance without overshoot and with faster dynamic response rather than PI controller and it is confirmed by observing the Fig. 5.19(d) and Fig. 5.19(h).



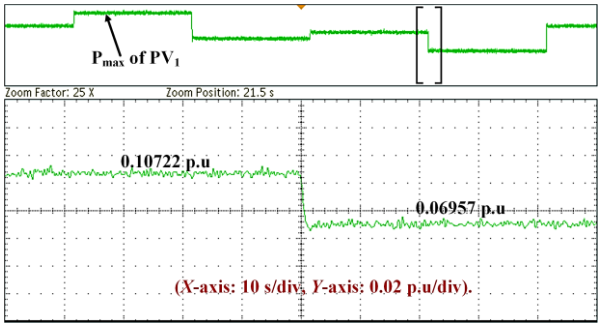
(a) change in irradiance level from 60% to 100% with PI



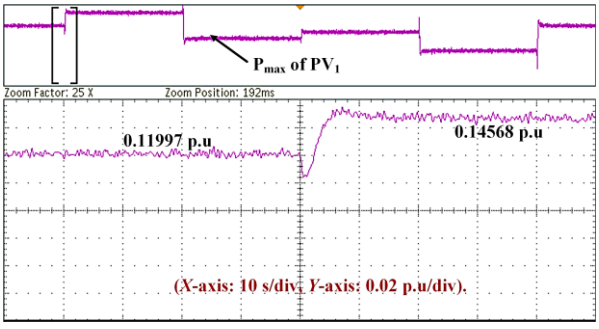
(b) change in irradiance level from 60% to 100% with SMC



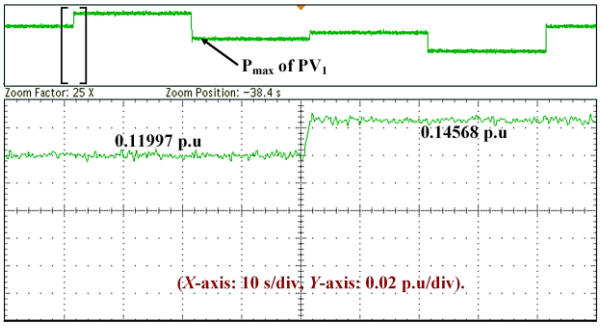
(c) change in irradiance level from 90% to 60% with PI



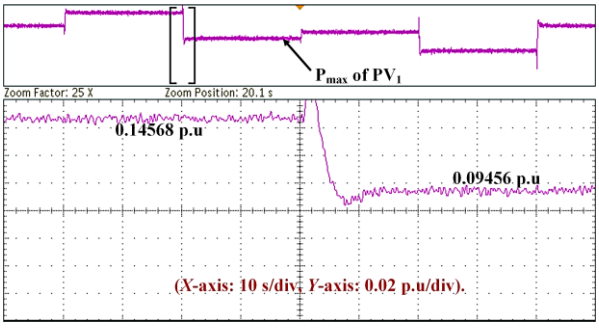
(d) change in irradiance level from 90% to 60% with SMC



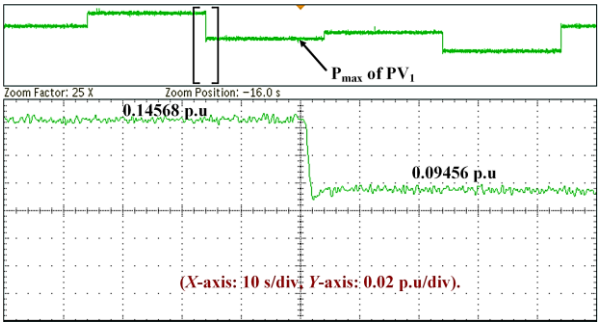
(e) change in irradiance level from 100% to 120% with PI



(f) change in irradiance level from 100% to 120% with SMC

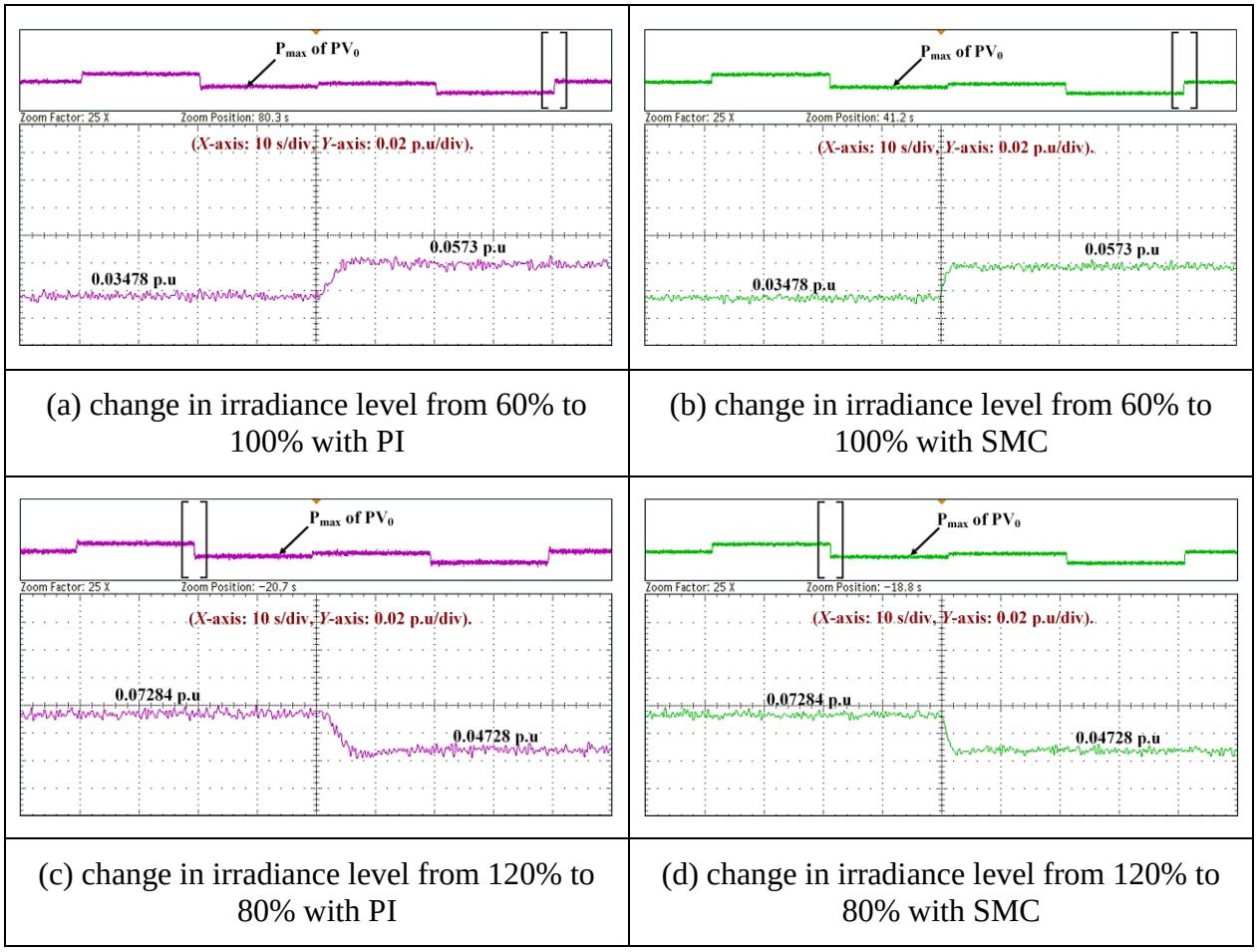


(g) change in irradiance level from 120% to 80% with PI



(h) change in irradiance level from 120% to 80% with SMC

Fig. 5.19: Performance of PI and SMC for generation of maximum Power of PV_1 (or PV_2) source under various irradiance conditions.



(a) change in irradiance level from 60% to 100% with PI

(b) change in irradiance level from 60% to 100% with SMC

(c) change in irradiance level from 120% to 80% with PI

(d) change in irradiance level from 120% to 80% with SMC

Fig. 5.20: Performance of PI and SMC for generation of maximum Power of PV_0 source under various irradiance conditions.

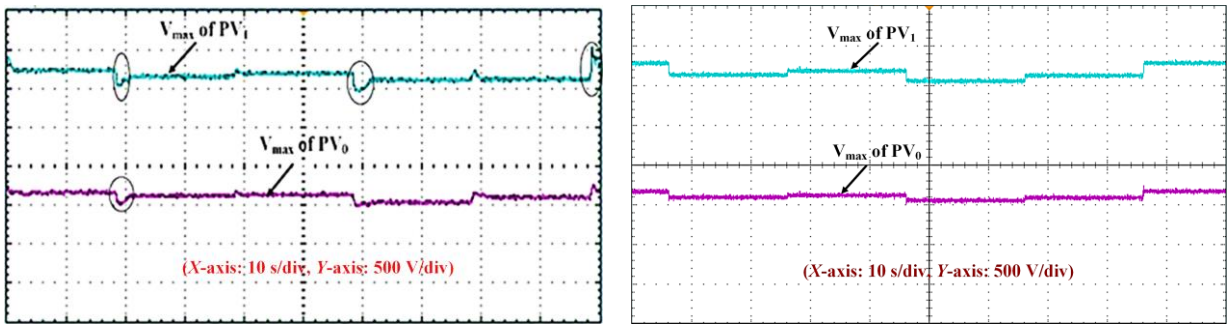
Fig. 5.20(a) and Fig. 5.20(b) show the variation in power of the PV_0 source under control of PI and SMC respectively during irradiance level changing from 60% to 100% in HIL environment. In this case, the performance of PI controller is similar to SMC except a delay in reaching new PV power. Similarly, both PI controller and SMC exhibit similar dynamic performance for extracting PV_0 power during other irradiance changing condition also. Further, both controllers show good performance in steady-state without error since maximum powers of PV_1 and PV_0 sources are obtained and follow according to the PV characteristics shown in Fig. 5.7 at given irradiance levels. The performance comparison of PI and SMC for extracting maximum power from PV_1 and PV_0 sources at various irradiance levels is given in Table 5.4.

Table 5.4: Performance comparison of PI and SMC for maximum PV power extraction.

Irradiance changes (In %)	Performance of PI	Performance of SMC
60% to 100%	Results a large undershoots in the power of PV_1 and it settles nearly in 15 cycles (Fig.	Result a good response without under/overshoot in power of PV_1 and settles within 3 to 4 cycles

	5.19(a)). And the performance of PI controller for extracting power from PV_0 source is better but reaches new power within 8 to 10 cycles (Fig. 5.20(a)).	(Fig. 5.19(b)). The performance of SMC controller for extracting power from PV_0 source is similar to PI and reaches new power within 3 to 4 cycles (Fig. 5.20(b)).
90% to 60%	Results a large overshoot in the power of PV_1 and it settles in nearly 15 to 20 cycles (Fig. 5.19(c)).	Result a better response without overshoot in power of PV_1 and settles within 3 to 4 cycles (Fig. 5.19(d)).
120% to 80%	Results a large overshoot in the power of PV_1 and it settles in nearly 15 to 20 cycles (Fig. 5.19(g)).	Result a better response without under/overshoot in power of PV_1 and settles within 4 to 5 cycles (Fig. 5.19(h)).
100% to 120%	PI controller results an undershoot in the power of PV_1 and it settles in nearly 10 to 15 cycles (Fig. 5.19(e)).	SMC controller results good response without any undershoots in the power of PV_1 and it settles in nearly 3 to 4 cycles (Fig. 5.19(f)).

Further, at the respective irradiance of 120%, 90%, 100%, 60% and 80%, the change in voltages of the PV sources (i.e., PV_1 or PV_2 and PV_0) corresponding to their maximum powers under the control of PI and SMC are shown in Fig. 5.21(a) and Fig. 5.21(b) respectively. The superior performance of SMC controller for obtaining desired voltages of PV sources of MLDCL RSC-MLI is shown in Fig. 5.21(b) in which, transient free and fast dynamic response is observed.



(a) with PI (b) with SMC

Fig. 5.21: Voltages of PV_1 (or PV_2) and PV_0 sources at various irradiance conditions using PI and SMC controllers.

Grid power and total powers of all the PV sources in three-phase MLDCL MLI:

Fig. 5.22 shows the grid power and sum of the total power of all PV sources (i.e., $3PV_1$, $3PV_2$ and $3PV_0$) of asymmetric three-phase MLDCL RSC-MLI. From Fig. 5.22, it is confirmed that at various percentage of irradiance conditions, the objective of injection of PV power into the grid is satisfied under the effective control of SMC and two-loop PI controller. Therefore, the entire maximum PV power generated from all the PV sources is injected into the grid.

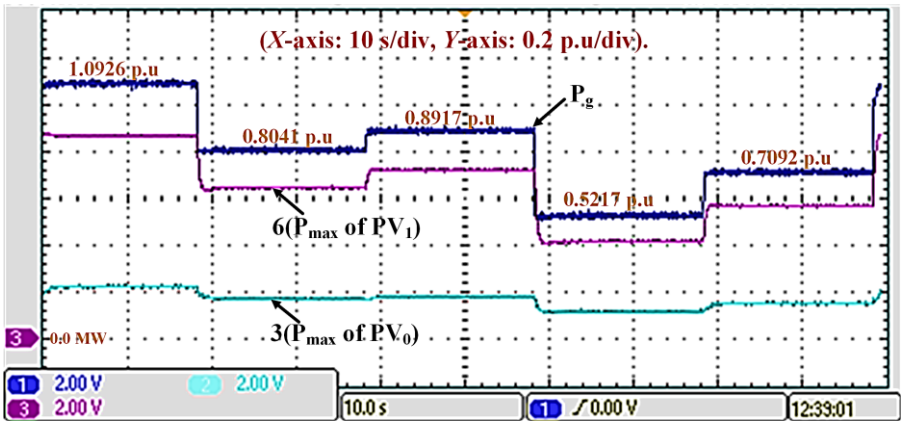


Fig. 5.22: Powers of six PV_1 (or PV_2) sources and three PV_0 sources of three-phase MLDCL MLI and grid power (P_g).

5.5 Conclusion

In this chapter, the grid integration of PV sources through a three-phase asymmetric MLDCL RSC-MLI is discussed. The proposed inverter facilitates less switch count, high modularity, and enables the operation of unequal rated PV sources, and hence it can be an alternate to conventional CHB for closed-loop power control in grid integration of PV based applications. The superior performance of variable gain SMC results in fast dynamic PV power response under irradiance varying conditions and it is verified against fixed gain PI controller, which results in large overshoots/undershoots with delayed response. Further, SMC enables the extraction of maximum power from multiple PV sources with ease. The maximum PV power

generated under the efficient control of SMC is successfully injected to 11 kV grid through MLDCL RSC-MLI.

CHAPTER 6: CONCLUSION AND FUTURE SCOPE

The main conclusions of the presented work and possible future research have been summarised in this chapter.

6.1 Conclusion

This thesis explored the closed-loop control of SSPS and MDLCL RSC-MLI based grid connected dc or PV system using conventional PI and SMC for power extraction and feeding into the grid. The key conclusions of this thesis are given here under.

- This thesis initially presented the qualitative and quantitative features of RSC-MLI topologies. Further, a comprehensive comparison has been made among 11-level conventional asymmetric CHB MLI, SSPS and MLDCL RSC-MLIs to facilitate a well-informed selection of topology for grid connected power feeding applications. Based on this study, it is observed that the series/parallel connection of dc sources in the SSPS RSC-MLI is possible to use all of the sources for generating most of the levels in output voltage. To quantify the effective use of different dc sources in MLI, a parameter known as utilization factor (*UF*) of input dc sources was introduced in this work. The calculations are confirmed that $UF_{SSPS} > UF_{CHB\ or\ MLDCL}$. Further, the considered asymmetric SSPS RSC-MLI is superior to conventional CHB MLI in terms of device switching frequency and current rating of switches.
- The other popular topology is MLDCL RSC-MLI which is simple and highly modular in its structure requires uni-directional switches only, and the high rating switches operate at fundamental frequency. The MLDCL RSC-MLI has significant reduction in switching count compared to conventional CHB MLI. Further, the highest rating switches in polarity generator of MLDCL and SSPS RSC-MLI are operating at fundamental frequency. This will reduce switching losses. Whereas in conventional CHB MLI, the switches operate at carrier frequency. Further, the presence of redundancies in the operation of MLDCL MLI allows even power distribution between equal rated input PV sources. Therefore, a common maximum power extraction control method can be applied for multiple equal rated input PV sources of MLDCL RSC-MLI, thereby reducing the control complexity.
- Owing to the above features, SSPS and MLDCL RSC-MLIs are most suitable and an effective alternate to conventional CHB MLI. Hence, SSPS and MLDCL MLIs were considered for adapting as power converters in dc to ac power conversion stage in grid connected system using linear and non-linear controllers. In this thesis, the performance

analysis of linear PI controller and non-linear SMC for extraction and injection of PV power into the grid through asymmetric SSPS and MLDCL RSC-MLIs are addressed.

- Sliding mode based nonlinear controller was proposed for the closed-loop operation of three-phase SSPS RSC-MLI. To verify the performance of proposed scheme, a three-phase 11 kV, 1 MVA SSPS RSC-MLI with 1: 2: 2 dc voltage ratio was designed and connected to 11 kV grid. Results are presented in MATLAB/Simulink environment and later corroborated in real-time environment using OPAL-RT system. Further, the proposed variable gain nonlinear controller was validated against the PI controller for delivering desired powers under different operating conditions/disturbances. It is concluded that the system with PI controllers experienced large overshoots/undershoots in power delivery under grid frequency variations, thereby activating the protection system of the converter, which disconnects the MLI from the rest of the system. On the other hand, with negligible overshoots/undershoots, the system with SMC overridden the frequency disturbances and retained the MLI with the grid even under disturbances, thereby supporting system to regain its stability.
- Further, this work proposed an 11-level asymmetric MLDCL RSC-MLI based single-stage PV system for integration to an 11 kV grid. In MLDCL RSC-MLI, asymmetric PV sources with voltage ratio of 1: 2: 2 was considered for generating more levels in the output voltage with minimum switch count. The proposed efficient SMC extracted the maximum power from single-stage PV sources. Along with MPPT algorithm, a single SMC was enough to extract the maximum power form all equal voltage rating PV sources. The results are presented in both MATLAB and hardware-in-loop OPAL-RT–based environments. The superior performance of variable gain SMC resulted in fast dynamic PV power response under variable irradiance conditions. The results are verified against fixed gain PI controller, which resulted in large overshoots/undershoots with delayed response. The maximum PV power generated under the efficient control of SMC was injected to 11 kV grid through MLDCL RSC-MLI.

6.2 Future scope

The research work presented in this thesis discloses a number of issues that could be further investigated.

- Designing a new RSC-MLI suitable for grid connected PV applications.
- Adaption of SMC to other closed-loop applications such as dc-dc converters and electric vehicles.
- The extension of fractional order controllers for grid connected systems.

- ❖ Applying the fractional order controllers and MPPT algorithms to other grid connected PV system topologies.

PUBLICATIONS FROM THE WORK

INTERNATIONAL JOURNALS

1. G. Eshwar Gowd and D Sreenivasarao "Non-linear controller for maximum power extraction in asymmetric multilevel dc link reduced switch count inverter based grid connected PV system," in **International Transactions on Electrical Energy Systems,** Wiley, vol. 30, no. 2, pp. 1–17, Feb. 2020.
   DOI:10.1002/2050-7038.12206.

2. G. Eshwar Gowd, P. C. Sekhar, and D Sreenivasarao "Real-time validation of a sliding mode controller for closed-loop operation of reduced switch count multilevel inverters," **IEEE Systems Journal**, vol. 13, no. 1, pp. 1042–1051, Mar 2019.
   DOI: 10.1109/JSYST.2018.2833867.

3 G. Eshwar Gowd and D Sreenivasarao "Sliding mode controllers for extraction and supply of photovoltaic power using switched series parallel sources reduced switch count multilevel inverter," **IET Power Electronics,** 1–17, 2020;
   DOI: 10.1049/pel2.12068

BIBLIOGRAPHY

[1] **S. Kouro, J. I. Leon, D. Vinnikov, and L. G. Franquelo**, "Grid-connected photovoltaic systems: An overview of recent research and emerging PV converter technology," IEEE Industrial Electronics Magazine, vol. 9, no. 1, pp. 47–61, Mar. 2015.

[2] **X. Yuan and Y. Zhang**, "Status and opportunities of photovoltaic inverters in grid-tied and micro-grid systems," in *2006 CES/IEEE 5th International Power Electronics and Motion Control Conference*, 2006, pp. 1–4.

[3] **P. G. Barbosa, H. A. C. Braga, M. d. C. B. Rodrigues, and E. C. Teixeira**, "Boost current multilevel inverter and its application on single-phase grid-connected photovoltaic systems," IEEE transactions on power electronics, vol. 21, no. 4, pp. 1116–1124, Jul. 2006.

[4] **J. M. Carrasco, L. G. Franquelo, J. T. Bialasiewicz, E. Galván, R. C. PortilloGuisado, M. M. Prats, J. I. León, and N. Moreno-Alfonso**, "Power-electronic systems for the grid integration of renewable energy sources: A survey," IEEE Transactions on industrial electronics, vol. 53, no. 4, pp. 1002–1016, June 2006.

[5] **T. Esram and P. L. Chapman**, "Comparison of photovoltaic array maximum power point tracking techniques," IEEE Transactions on energy conversion, vol. 22, no. 2, pp. 439–449, June 2007.

[6] **K. Hussein, I. Muta, T. Hoshino, and M. Osakada**, "Maximum photovoltaic power tracking: an algorithm for rapidly changing atmospheric conditions," IEE Proceedings-Generation, Transmission and Distribution, vol. 142, no. 1, pp. 59–64, Jan. 1995.

[7] **S. Jain and V. Agarwal**, "A new algorithm for rapid tracking of approximate maximum power point in photovoltaic systems," IEEE power electronics letters, vol. 2, no. 1, pp. 16–19, March 2004.

[8] **A. Brambilla, M. Gambarara, A. Garutti, and F. Ronchi**, "New approach to photovoltaic arrays maximum power point tracking," in *30th Annual IEEE Power Electronics Specialists Conference. Record.(Cat. No. 99CH36321)*, 1999, pp. 632–637.

[9] **J. Schoeman and J. Van Wyk**, "A simplified maximal power controller for terrestrial photovoltaic panel arrays," in *1982 IEEE Power Electronics Specialists conference*, 1982, pp. 361–367.

[10] **C.-Y. Won, D.-H. Kim, S.-C. Kim, W.-S. Kim, and H.-S. Kim**, "A new maximum power point tracker of photovoltaic arrays using fuzzy controller," in *Proceedings of 1994 Power Electronics Specialist Conference-PESC'94*, 1994, pp. 396–403.

[11] **T. Hiyama, S. Kouzuma, and T. Imakubo**, "Identification of optimal operating point of PV modules using neural network for real time maximum power tracking control," IEEE Transactions on Energy Conversion, vol. 10, no. 2, pp. 360–367, June 1995.

[12] **M. H. Rashid**, *Alternative energy in power electronics*: Butterworth-Heinemann, 2014.

[13] **A. D. Martin and J. R. Vazquez**, "MPPT algorithms comparison in PV systems: P&O, PI, neuro-fuzzy and backstepping controls," in *2015 IEEE International Conference on Industrial Technology (ICIT)*, 2015, pp. 2841–2847.

[14] **O. P. Mahela and A. G. Shaik**, "Comprehensive overview of grid interfaced solar photovoltaic systems," Renewable and Sustainable Energy Reviews, vol. 68, pp. 316–332, Feb. 2017.

[15] **M. Liang and T. Q. Zheng**, "Synchronous PI control for three-phase grid-connected photovoltaic inverter," in *2010 Chinese Control and Decision Conference*, 2010, pp. 2302–2307.

[16] **M. A. Mahmud, H. Pota, M. Hossain, and N. K. Roy**, "Robust partial feedback linearizing stabilization scheme for three-phase grid-connected photovoltaic systems," IEEE Journal of photovoltaics, vol. 4, no. 1, pp. 423–431, Jan. 2014.

[17] **S.-S. MEO, V. ZOHOORI, and A. VAHEDI**, "A.: Second-Order Sliding Mode Control of a Smart Inverter for Renewable Energy System," International Review of Electrical Engineering (IREE), vol. 9, no. 6, pp. 1090–1096, 2014.

[18] **M. Guisser, M. Aboulfatah, E. Abdelmounim, H. Medromi, and J. Saadi**, "Nonlinear Control Design for Maximum Power Point Tracking and Unity Power Factor of a Grid-Connected Photovoltaic Renewable Energy Systems," IOSR Journal of Electronics and Communication Engineering, vol. 9, no. 5, pp. 62–71, Sep./Oct. 2014.

[19] **H. Malek and Y. Chen**, "A single-stage three-phase grid-connected photovoltaic system with fractional order MPPT," in *2014 IEEE Applied Power Electronics Conference and Exposition-APEC 2014*, 2014, pp. 1793–1798.

[20] **R. Errouissi, S. Muyeen, A. Al-Durra, and S. Leng**, "Experimental validation of a robust continuous nonlinear model predictive control based grid-interlinked photovoltaic inverter," IEEE Transactions on Industrial Electronics, vol. 63, no. 7, pp. 4495–4505, Jul. 2016.

[21] **S. Ding, J. Wang, and W. X. Zheng**, "Second-order sliding mode control for nonlinear uncertain systems bounded by positive functions," IEEE Transactions on Industrial Electronics, vol. 62, no. 9, pp. 5899–5909, Sept. 2015.

[22] **P. Sekhar and S. Mishra**, "Sliding mode based feedback linearizing controller for grid connected multiple fuel cells scenario," International Journal of Electrical Power & Energy Systems, vol. 60, pp. 190–202, March 2014.

[23] **V. Utkin**, "Variable structure systems with sliding modes," IEEE Transactions on Automatic control, vol. 22, no. 2, pp. 212–222, Apr. 1977.

[24] **J.-J. E. Slotine and W. Li**, *Applied nonlinear control* vol. 199: Prentice hall Englewood Cliffs, NJ, 1991.

[25] **W. E. Dixon, A. Behal, D. M. Dawson, and S. P. Nagarkatti**, *Nonlinear control of engineering systems: a Lyapunov-based approach*: Springer Science & Business Media, 2013.

[26] **H. J. Marquez**, *Nonlinear control systems: analysis and design* vol. 161: John Wiley Hoboken^ eN. JNJ, 2003.

[27] **D. Lalili, A. Mellit, N. Lourci, B. Medjahed, and E. Berkouk**, "Input output feedback linearization control and variable step size MPPT algorithm of a grid-connected photovoltaic inverter," Renewable energy, vol. 36, no. 12, pp. 3282–3291, Dec. 2011.

[28] **T. Roy, M. Mahmud, M. Hossain, and A. Oo**, "Nonlinear backstepping controller design for sharing active and reactive power in three-phase grid-connected photovoltaic systems," in *2015 Australasian Universities Power Engineering Conference (AUPEC)*, 2015, pp. 1–6.

[29] **A. Moreno-Munoz**, *Power quality: mitigation technologies in a distributed environment*: Springer-Verlag Limited, London, 2007.

[30] **J. Dixon, L. Moran, J. Rodriguez, and R. Domke**, "Reactive power compensation technologies: State-of-the-art review," Proceedings of the IEEE, vol. 93, no. 12, pp. 2144–2164, Dec. 2005.

[31] **N. G. Hingorani and L. Gyugyi**, *Understanding FACTS: concepts and technology of flexible AC transmission systems*: IEEE Press, New York, 1999.

[32] **B. Sahan, S. Araujo, C. Noding, and P. Zacharias**, "Comparative evaluation of three-phase current source inverters for grid interfacing of distributed and renewable energy systems," IEEE Transactions on Power Electronics, vol. 26, no. 8, pp. 2304–2318, Aug. 2011.

[33] **M. Routimo, M. Salo, and H. Tuusa**, "Comparison of voltage-source and current-source shunt active power filters," IEEE Transactions on Power Electronics, vol. 22, no. 2, pp. 636–643, Mar. 2007.

[34] **J. RodrÃguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro**, "Multilevel voltage-source-converter topologies for industrial medium-voltage drives," IEEE Transactions on Industrial Electronics, vol. 54, no. 6, pp. 2930–2945, Dec. 2007.

[35] **L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo, and M. A. M. Prats**, "The age of multilevel converters arrives," IEEE Industrial Electronics Magazine, vol. 2, no. 2, pp. 28–39, Jun. 2008.

[36] **T. A. Meynard, H. Foch, P. Thomas, J. Courault, R. Jakob, and M. Nahrstaedt**, "Multicell converters: basic concepts and industry applications," IEEE Transactions on Industrial Electronics, vol. 49, no. 5, pp. 955–964, Oct. 2002.

[37] **J. Rodriguez, J. S. Lai, and F. Z. Peng**, "Multilevel inverters: a survey of topologies, controls, and applications," IEEE Transactions on Industrial Electronics, vol. 49, no. 4, pp. 724–738, Aug. 2002.

[38] **S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. A. Perez, and J. I. Leon**, "Recent advances and industrial applications of multilevel converters," IEEE Transactions on Industrial Electronics, vol. 57, no. 8, pp. 2553–2580, Aug. 2010.

[39] **S. Bernet**, "Recent developments of high power converters for industry and traction applications," IEEE Transactions on Power Electronics, vol. 15, no. 6, pp. 1102–1117, Nov. 2000.

[40] **J. S. Lai and F. Z. Peng**, "Multilevel converters-a new breed of power converters," IEEE Transactions on Industry Applications, vol. 32, no. 3, pp. 509–517, May/Jun. 1996.

[41] **A. Nabae, I. Takahashi, and H. Akagi**, "A new neutral-point-clamped PWM inverter," IEEE Transactions on Industry Applications, vol. IA-17, no. 5, pp. 518–523, Sep./Oct. 1981.

[42] **J. Rodriguez, S. Bernet, P. K. Steimer, and I. E. Lizama**, "A survey on neutral-point-clamped inverters," IEEE Transactions on Industrial Electronics, vol. 57, no. 7, pp. 2219–2230, Jul. 2010.

[43] **B. Wu**, *High-power converters and AC drives*: Piscataway, NJ: IEEE Press, 2006.

[44] **T. Bruckner, S. Bernet, and H. Guldner**, "The active NPC converter and its loss-balancing control," IEEE Transactions on Industrial Electronics, vol. 52, no. 3, pp. 855–868, Jun. 2005.

[45] **T. Meynard and H. Foch**, "Electronic device for electrical energy conversion between a voltage source and a current source by means of controllable switching cells," European Patent, 92/916336.8, 1992.

[46] **M. Marchesoni, M. Mazzucchelli, and S. Tenconi**, "A non conventional power converter for plasma stabilization," IEEE Transactions on Power Electronics, vol. 5, no. 2, pp. 122–129, Apr. 1990.

[47] **R. H. Wilkinson, T. A. Meynard, and H. du Toit Mouton**, "Natural balance of multicell converters: The general case," IEEE Transactions on Power Electronics, vol. 21, no. 6, pp. 1658–1666, Nov. 2006.

[48] **B. P. McGrath and D. G. Holmes**, "Natural capacitor voltage balancing for a flying capacitor converter induction motor drive," IEEE Transactions on Power Electronics, vol. 24, no. 6, pp. 1554–1561, Jun. 2009.

[49] **C. Turpin, P. Baudesson, F. Richardeau, F. Forest, and T. A. Meynard**, "Fault management of multicell converters," IEEE Transactions on Industrial Electronics, vol. 49, no. 5, pp. 988–997, Oct. 2002.

[50] **P. W. Hammond**, "A new approach to enhance power quality for medium voltage AC drives," IEEE Transactions on Industry Applications, vol. 33, no. 1, pp. 202–208, Jan./Feb. 1997.

[51] **F. Z. Peng, J. S. Lai, J. W. McKeever, and J. VanCoevering**, "A multilevel voltage-source inverter with separate dc sources for static var generation," IEEE Transactions on Industry Applications, vol. 32, no. 5, pp. 1130–1138, 1996.

[52] **H. Akagi**, "Classification, terminology, and application of the modular multilevel cascade converter (MMCC)," IEEE Transactions on Power Electronics, vol. 26, no. 11, pp. 3119–3130, Nov. 2011.

[53] **P. Lezana and G. Ortiz**, "Extended operation of cascade multicell converters under fault condition," IEEE Transactions on Industrial Electronics, vol. 56, no. 7, pp. 2697–2703, Jul. 2009.

[54] **M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Pérez**, "A survey on cascaded multilevel inverters," IEEE Transactions on Industrial Electronics, vol. 57, no. 7, pp. 2197–2206, Jul. 2010.

[55] **J. Peralta, H. Saad, S. Dennetière, J. Mahseredjian, and S. Nguefeu**, "Detailed and averaged models for a 401-level MMC–HVDC system," IEEE Transactions on Power Delivery, vol. 27, no. 3, pp. 1501–1508, Jul. 2012.

[56] **H. Akagi, H. Fujita, S. Yonetani, and Y. Kondo**, "A 6.6-kV transformerless STATCOM based on a five-level diode-clamped PWM converter: System design and experimentation of a 200-V 10-kVA laboratory model," IEEE Transactions on Industry Applications, vol. 44, no. 2, pp. 672–680, Mar./Apr. 2008.

[57] **M. Hagiwara, P. Phuong Viet, and H. Akagi**, "Calculation of dc magnetic flux deviation in the converter-transformer of a self-commutated BTB system during single-line-to-ground faults," IEEE Transactions on Power Electronics, vol. 23, no. 2, pp. 698–706, Mar. 2008.

[58] **M. I. Marei, A. B. Eltantawy, and A. A. El-Sattar**, "An energy optimized control scheme for a transformerless DVR," Electric Power Systems Research, vol. 83, no. 1, pp. 110–118, Feb. 2012.

[59] **L. Maharjan, S. Inoue, and H. Akagi**, "A transformerless energy storage system based on a cascade multilevel PWM converter with star configuration," IEEE Transactions on Industrial Electronics, vol. 44, no. 5, pp. 1621−1630, Sep./Oct. 2008.

[60] **H. Akagi, M. Hagiwara, and R. Maeda**, "Negative-sequence reactive-power control by a PWM STATCOM based on a Modular Multilevel Cascade Converter (MMCC-SDBC)," IEEE Transactions on Industry Applications, vol. 48, no. 2, pp. 720–729, Mar./Apr. 2012.

[61] **H. Akagi, S. Inoue, and T. Yoshii**, "Control and performance of a transformerless cascade PWM STATCOM with star configuration," IEEE Transactions on Industry Applications, vol. 43, no. 4, pp. 1041–1049, Jul./Aug. 2007.

[62] **D. Krug, S. Bernet, S. S. Fazel, K. Jalili, and M. Malinowski**, "Comparison of 2.3-kV medium-voltage multilevel converters for industrial medium-voltage drives," IEEE Transactions on Industrial Electronics, vol. 54, no. 6, pp. 2979–2992, Dec. 2007.

[63] **S. S. Fazel, S. Bernet, D. Krug, and K. Jalili**, "Design and comparison of 4-kV neutral-point-clamped, flying-capacitor, and series-connected H-bridge multilevel converters," IEEE Transactions on Industry Applications, vol. 43, no. 4, pp. 1032–1040, Jul./Aug. 2007.

[64] **P. Omer, J. Kumar, and B. S. Surjan**, "A Review on Reduced Switch Count Multilevel Inverter Topologies," IEEE Access, vol. 8, pp. 22281–22302, Feb. 2020.

[65] **K. K. Gupta, A. Ranjan, P. Bhatnagar, L. K. Sahu, and S. Jain**, "Multilevel inverter topologies with reduced device count: A review," IEEE Transactions on Power Electronics, vol. 31, no. 1, pp. 135−151, Jan. 2016.

[66] **M. P. Kazmierkowski, R. Krishnan, and F. Blaabjerg**, *Control in power electronics*: Elsevier, 2002.

[67] **S. Buso and P. Mattavelli**, "Digital control in power electronics," Lectures on power electronics, vol. 1, no. 1, pp. 1–158, 2006.

[68] **M. P. Kazmierkowski and L. Malesani**, "Current control techniques for three-phase voltage-source PWM converters: A survey," IEEE Transactions on industrial electronics, vol. 45, no. 5, pp. 691–703, Oct. 1998.

[69] **C. N.-M. Ho, V. S. Cheung, and H. S.-H. Chung**, "Constant-frequency hysteresis current control of grid-connected VSI without bandwidth control," IEEE Transactions on power electronics, vol. 24, no. 11, pp. 2484–2495, Nov. 2009.

[70] **L. Malesani, P. Mattavelli, and P. Tomasin**, "Improved constant-frequency hysteresis current control of VSI inverters with simple feedforward bandwidth prediction," IEEE Transactions on industry applications, vol. 33, no. 5, pp. 1194–1202, Sept./Oct. 1997.

[71] **J. Yu, M. Su, and Y. Sun**, "A novel current control method for grid connected photovoltaic system," in *2011 Asia-Pacific Power and Energy Engineering Conference*, 2011, pp. 1–4.

[72] **M. Liserre*, F. Blaabjerg, and A. Dell'Aquila**, "Step-by-step design procedure for a grid-connected three-phase PWM voltage source converter," International journal of electronics, vol. 91, no. 8, pp. 445–460, Aug. 2004.

[73] **S. Golestan, M. Monfared, J. M. Guerrero, and M. Joorabian**, "A DQ synchronous frame controller for single-phase inverters," in *2011 2nd Power Electronics, Drive Systems and Technologies Conference*, 2011, pp. 317–323.

[74] **S. Nandurkar and M. Rajeev**, "Design and Simulation of three phase Inverter for grid connected Photovoltic systems," Power, vol. 10, pp. 30KW, 2012.

[75] **J. Selvaraj and N. A. Rahim**, "Multilevel inverter for grid-connected PV system employing digital PI controller," IEEE transactions on industrial electronics, vol. 56, no. 1, pp. 149–158, Jan. 2009.

[76] **M. Ciobotaru, R. Teodorescu, and F. Blaabjerg**, "Control of single-stage single-phase PV inverter," EPE Journal, vol. 16, no. 3, pp. 20–26, 2006.

[77] **E. Villanueva, P. Correa, J. Rodríguez, and M. Pacas**, "Control of a single-phase cascaded H-bridge multilevel inverter for grid-connected photovoltaic systems," IEEE Transactions on industrial electronics, vol. 56, no. 11, pp. 4399–4406, Nov. 2009.

[78] **H. Komurcugil and O. Kukrer**, "A novel current-control method for three-phase PWM AC/DC voltage-source converters," IEEE Transactions on Industrial Electronics, vol. 46, no. 3, pp. 544–553, June 1999.

[79] **N. R. Zargari and G. Joos**, "Performance investigation of a current-controlled voltage-regulated PWM rectifier in rotating and stationary frames," IEEE Transactions on Industrial Electronics, vol. 42, no. 4, pp. 396–401, Aug. 1995.

[80] **M. Odavic, P. Zanchetta, M. Sumner, and Z. Jakopovic**, "High performance predictive current control for active shunt filters," in *2006 12th International Power Electronics and Motion Control Conference*, 2006, pp. 1677–1681.

[81] **B. Xiao, L. Hang, J. Mei, C. Riley, L. M. Tolbert, and B. Ozpineci**, "Modular cascaded H-bridge multilevel PV inverter with distributed MPPT for grid-connected applications," IEEE Transactions on Industry Applications, vol. 51, no. 2, pp. 1722–1731, Mar./Apr. 2015.

[82] **Y. Shi, R. Li, Y. Xue, and H. Li**, "High-frequency-link-based grid-tied PV system with small DC-link capacitor and low-frequency ripple-free maximum power point tracking," IEEE Transactions on Power Electronics, vol. 31, no. 1, pp. 328–339, Jan. 2016.

[83] **L. He, K. Zhang, J. Xiong, and S. Fan**, "A repetitive control scheme for harmonic suppression of circulating current in modular multilevel converters," IEEE transactions on power electronics, vol. 30, no. 1, pp. 471–481, Jan. 2015.

[84] **L. Ben-Brahim, A. Gastli, M. Trabelsi, K. A. Ghazi, M. Houchati, and H. Abu-Rub**, "Modular multilevel converter circulating current reduction using model predictive control," IEEE Transactions on Industrial Electronics, vol. 63, no. 6, pp. 3857–3866, June 2016.

[85] **A. Moharana and P. Dash**, "Input-output linearization and robust sliding-mode controller for the VSC-HVDC transmission link," IEEE Transactions on Power Delivery, vol. 25, no. 3, pp. 1952–1961, Jul. 2010.

[86] **S. Mishra and P. Sekhar**, "Sliding mode based feedback linearizing controller for a pv system to improve the performance under grid frequency variation," in *2011 International Conference on Energy, Automation and Signal*, 2011, pp. 1–7.

[87] **F. Sebaaly, H. Vahedi, H. Y. Kanaan, N. Moubayed, and K. Al-Haddad**, "Design and implementation of space vector modulation-based sliding mode control for grid-connected 3L-NPC inverter," IEEE Transactions on Industrial Electronics, vol. 63, no. 12, pp. 7854–7863, Dec. 2016.

[88] **A. Bag, B. Subudhi, and P. K. Ray**, "A combined reinforcement learning and sliding mode control scheme for grid integration of a PV system," CSEE Journal of Power and Energy Systems, vol. 5, no. 4, pp. 498-506, 2019.

[89] **A. Merabet, L. Labib, A. M. Ghias, C. Ghenai, and T. Salameh**, "Robust feedback linearizing control with sliding mode compensation for a grid-connected photovoltaic inverter system under unbalanced grid voltages," IEEE Journal of Photovoltaics, vol. 7, no. 3, pp. 828-838, 2017.

[90] **S. Kouro, J. I. Leon, D. Vinnikov, and L. G. Franquelo**, "Grid-connected photovoltaic systems: An overview of recent research and emerging PV converter technology," IEEE Industrial Electronics Magazine, vol. 9, no. 1, pp. 47–61, March 2015.

[91] **D. Sera, T. Kerekes, R. Teodorescu, and F. Blaabjerg**, "Improved MPPT algorithms for rapidly changing environmental conditions," in *2006 12th International Power Electronics and Motion Control Conference*, 2006, pp. 1614–1619.

[92] **A. Mohapatra, B. Nayak, and B. Misra**, "Model validation and maximum power point tracking of photovoltaic module," in *2014 POWER AND ENERGY SYSTEMS: TOWARDS SUSTAINABLE ENERGY*, 2014, pp. 1–4.

[93] **M. A. Farahat, M. A. Enany, and A. Nasr**, "Assessment of maximum power point tracking techniques for photovoltaic system applications," Journal of Renewable and Sustainable Energy, vol. 7, no. 4, pp. 1–7, 2015.

[94] **Z. Dejia, Z. Zhengming, M. Eltawil, and Y. Liqiang**, "Design and control of a three-phase grid-connected photovoltaic system with developed maximum power point tracking," in *2008 Twenty-Third Annual IEEE Applied Power Electronics Conference and Exposition*, 2008, pp. 973–979.

[95] **F. Liu, S. Duan, F. Liu, B. Liu, and Y. Kang**, "A variable step size INC MPPT method for PV systems," IEEE Transactions on industrial electronics, vol. 55, no. 7, pp. 2622–2628, Jul. 2008.

[96] **D. Sera, L. Mathe, T. Kerekes, S. V. Spataru, and R. Teodorescu**, "On the perturb-and-observe and incremental conductance MPPT methods for PV systems," IEEE journal of photovoltaics, vol. 3, no. 3, pp. 1070–1078, Jul. 2013.

[97] **R. Kadri, J.-P. Gaubert, and G. Champenois**, "An improved maximum power point tracking for photovoltaic grid-connected inverter based on voltage-oriented control," IEEE transactions on industrial electronics, vol. 58, no. 1, pp. 66–75, Jan. 2011.

[98] **H. Zhang, H. Zhou, J. Ren, W. Liu, S. Ruan, and Y. Gao**, "Three-phase grid-connected photovoltaic system with SVPWM current controller," in *2009 IEEE 6th International Power Electronics and Motion Control Conference*, 2009, pp. 2161–2164.

[99] **G. Tsengenes and G. Adamidis**, "Investigation of the behavior of a three phase grid-connected photovoltaic system to control active and reactive power," Electric Power Systems Research, vol. 81, no. 1, pp. 177–184, Jan. 2011.

[100] **M. F. Schonardie and D. C. Martins**, "Three-phase grid-connected photovoltaic system with active and reactive power control using dq0 transformation," in *2008 IEEE Power Electronics Specialists Conference*, 2008, pp. 1202–1207.

[101] **Y. Huang, M. Shen, F. Z. Peng, and J. Wang**, "$ Z $-Source Inverter for Residential Photovoltaic Systems," IEEE transactions on power electronics, vol. 21, no. 6, pp. 1776–1782, Nov. 2006.

[102] **B. N. Alajmi, K. H. Ahmed, G. P. Adam, and B. W. Williams**, "Single-phase single-stage transformer less grid-connected PV system," IEEE transactions on power electronics, vol. 28, no. 6, pp. 2664–2676, June 2013.

[103] **B. Crowhurst, E. El-Saadany, L. El Chaar, and L. Lamont**, "Single-phase grid-tie inverter control using DQ transform for active and reactive load power compensation," in *2010 IEEE International Conference on Power and Energy*, 2010, pp. 489–494.

[104] **F. El Aamri, H. Maker, A. Mouhsen, and M. Harmouchi**, "A new strategy to control the active and reactive power for single phase grid-connected PV inverter," in *2015 3rd International Renewable and Sustainable Energy Conference (IRSEC)*, 2015, pp. 1–6.

[105] **C. Aouadi, A. Abouloifa, A. Hamdoun, and Y. Boussairi**, "Nonlinear controller design for single-phase grid-connected photovoltaic systems," in *2015 3rd International Renewable and Sustainable Energy Conference (IRSEC)*, 2015, pp. 1–5.

[106] **H. El Fadil, F. Giri, and J. M. Guerrero**, "Grid-connected of photovoltaic module using nonlinear control," in *2012 3rd IEEE international symposium on power electronics for distributed generation systems (PEDG)*, 2012, pp. 119–124.

[107] **A. A. Elmahjoub, A. Ailane, M. Rachik, E. H. Labriji, A. Abouloifa, and A. Essadki**, "A non-linear controller for single-phase DC-AC power converter using in the grid-connected photovoltaic," in *2012 IEEE International Conference on Complex Systems (ICCS)*, 2012, pp. 1–6.

[108] **N. Skik and A. Abbou**, "Nonlinear control for MPPT and UPF of PV system connected to the grid," in *2016 7th International Renewable Energy Congress (IREC)*, 2016, pp. 1–6.

[109] **D. Lauria and M. Coppola**, "Design and control of an advanced PV inverter," Solar Energy, vol. 110, pp. 533–542, Dec. 2014.

[110] **O. Alonso, P. Sanchis, E. Gubia, and L. Marroyo**, "Cascaded H-bridge multilevel converter for grid connected photovoltaic generators with independent maximum power point tracking of each solar array," in *IEEE 34th Annual Conference on Power Electronics Specialist, 2003. PESC'03.*, 2003, pp. 731–735.

[111] **L. Liu, H. Li, Y. Xue, and W. Liu**, "Decoupled active and reactive power control for large-scale grid-connected photovoltaic systems using cascaded modular multilevel converters," IEEE Transactions on Power Electronics, vol. 30, no. 1, pp. 176–187, Jan. 2015.

[112] **M. Coppola, F. Di Napoli, P. Guerriero, D. Iannuzzi, S. Daliento, and A. Del Pizzo**, "An FPGA-based advanced control strategy of a gridtied PV CHB inverter," IEEE Transactions on Power Electronics, vol. 31, no. 1, pp. 806–816, Jan. 2016.

[113] **H. Iman-Eini and S. B. Tennakoon**, "Investigation of a cascaded H-bridge photovoltaic inverter under non-uniform insolation conditions by hardware-in-the-loop test," International Journal of Electrical Power & Energy Systems, vol. 105, pp. 330–340, Feb. 2019.

[114] **B. N. Alajmi, K. H. Ahmed, S. J. Finney, and B. W. Williams**, "Fuzzy-logic-control approach of a modified hill-climbing method for maximum power point in microgrid standalone photovoltaic system," IEEE transactions on power electronics, vol. 26, no. 4, pp. 1022–1030, Apr. 2011.

[115] **A. Abbou, S. Rhaili, and M. Salimi**, "Maximum power point tracking of photovoltaic systems using backstepping controller," in *2017 International Conference on Engineering and Technology (ICET)*, 2017, pp. 1–6.

[116] **P. Henriquez, S. Cuevas, J. Rohten, S. Araya, V. Esparza, G. Sanhueza, and P. Melin**, "Nonlinear control for power converters injecting the maximum power from PV arrays," in *2016 IEEE International Conference on Automatica (ICA-ACCA)*, 2016, pp. 1–6.

[117] **F. Blaabjerg, R. Teodorescu, M. Liserre, and A. V. Timbus**, "Overview of control and grid synchronization for distributed power generation systems," IEEE Transactions on industrial electronics, vol. 53, no. 5, pp. 1398–1409, Oct. 2006.

[118] **S. R. Meher, S. Banerjee, B. T. Vankayalapati, and R. K. Singh**, "A Reconfigurable On-Board Power Converter for Electric Vehicle With Reduced Switch Count," IEEE Transactions on Vehicular Technology, vol. 69, no. 4, pp. 3760-3772, Apr. 2020.

[119] **A. Lashab, D. Sera, F. Hahn, L. Camura, M. Liserre, and J. Guerrero**, "A Reduced Power Switches Count Multilevel Converter-Based Photovoltaic System with Integrated Energy Storage," IEEE Transactions on Industrial Electronics, 2020.

[120] **C. Dhanamjayulu, S. R. Khasim, S. Padmanaban, G. Arunkumar, J. B. Holm-Nielsen, and F. Blaabjerg**, "Design and Implementation of Multilevel Inverters for Fuel Cell Energy Conversion System," IEEE Access, vol. 8, pp. 183690-183707, 2020.

[121] **Z. Li, J. K. Motwani, Z. Zeng, S. Lukic, A. V. Peterchev, and S. Goetz**, "A Reduced Series/Parallel Module for Cascade Multilevel Static Compensators Supporting Sensorless Balancing," IEEE Transactions on Industrial Electronics, vol. 68, no. 1, Jan. 2020.

[122] **A. Karthik and U. Loganathan**, "A reduced component count five-level inverter topology for high reliability electric drives," IEEE Transactions on Power Electronics, vol. 35, no. 1, pp. 725-732, 2019.

[123] **N. Osman, M. F. M. Elias, and N. A. Rahim**, "Design and analysis of three-level hybrid boost converter based on T-type inverter for solar photovoltaic system," IET Power Electronics, vol. 13, no. 9, pp. 1848-1857, 2020.

[124] **P. R. Bana, K. P. Panda, R. Naayagi, P. Siano, and G. Panda**, "Recently developed reduced switch multilevel inverter for renewable energy integration and drives application: topologies, comprehensive analysis and comparative evaluation," IEEE access, vol. 7, pp. 54888-54909, 2019.

[125] **S. S. Lee, K.-B. Lee, I. M. Alsofyani, Y. Bak, and J. F. Wong**, "Improved switched-capacitor integrated multilevel inverter with a dc source string," IEEE Transactions on Industry Applications, vol. 55, no. 6, pp. 7368-7376, 2019.

[126] **P. Bhatnagar, R. Agrawal, N. K. Dewangan, S. K. Jain, and K. K. Gupta**, "Nine-level voltage-doubler bi-polar module for multilevel DC to AC power conversion," IET Power Electronics, vol. 12, no. 15, pp. 4079-4087, 2019.

[127] **S. T. Meraj, K. Hasan, and A. Masaoud**, "A novel configuration of cross-switched T-type (CT-type) multilevel inverter," IEEE Transactions on Power Electronics, vol. 35, no. 4, pp. 3688-3696, 2019.

[128] **S. Yousofi-Darmian and S. M. Barakati**, "A new asymmetric multilevel inverter with reduced number of components," IEEE Journal of Emerging and Selected Topics in Power Electronics, 2019.

[129] **M. D. Siddique, S. Mekhilef, A. Sarwar, A. Alam, and N. M. Shah**, "Dual asymmetrical dc voltage source based switched capacitor boost multilevel inverter topology," IET Power Electronics, vol. 13, no. 7, pp. 1481-1486, 2020.

[130] **M. M. Hasan, A. Abu-Siada, and M. S. Dahidah**, "A three-phase symmetrical dc-link multilevel inverter with reduced number of dc sources," IEEE Transactions on Power Electronics, vol. 33, no. 10, pp. 8331-8340, 7 Dec. 2017.

[131] **Y. Ye, S. Chen, X. Wang, and K. W. E. E. Cheng**, "Self-Balanced 13-Level Inverter Based on Switched-Capacitor Structure and Hybrid PWM Algorithm," IEEE Transactions on Industrial Electronics, 2020.

[132] **W. Peng, Q. Ni, X. Qiu, and Y. Ye**, "Seven-level inverter with self-balanced switched-capacitor and its cascaded extension," IEEE Transactions on Power Electronics, vol. 34, no. 12, pp. 11889-11896, 2019.

[133] **M. D. Siddique, A. Iqbal, M. A. Memon, and S. Mekhilef**, "A new configurable topology for multilevel inverter with reduced switching components," IEEE Access, vol. 8, pp. 188726-188741, 2020.

[134] **K. Boora and J. Kumar**, "General topology for asymmetrical multilevel inverter with reduced number of switches," IET Power Electronics, vol. 10, no. 15, pp. 2034-2041, 15 Dec 2017.

[135] **E. Babaei, S. Laali, and S. Alilu**, "Cascaded multilevel inverter with series connection of novel H-bridge basic units," IEEE Transactions on Industrial Electronics, vol. 61, no. 12, pp. 6664−6671, Dec. 2014.

[136] **E. Babaei, S. Alilu, and S. Laali**, "A new general topology for cascaded multilevel inverters with reduced number of components based on developed H-bridge," IEEE Transactions on Industrial Electronics, vol. 61, no. 8, pp. 3932−3939, Aug. 2014.

[137] **S. P. Gautam, L. Kumar, and S. Gupta**, "Hybrid topology of symmetrical multilevel inverter using less number of devices," IET Power Electronics, vol. 8, no. 11, pp. 2125−2135, Nov. 2015.

[138] **S. P. Gautam, L. K. Sahu, and S. Gupta**, "Reduction in number of devices for symmetrical and asymmetrical multilevel inverters," IET Power Electronics, vol. 9, no. 4, pp. 698−709, Mar. 2016.

[139] **S.-J. Park, F.-S. Kang, M. H. Lee, and C.-U. Kim**, "A new single-phase five-level PWM inverter employing a deadbeat control scheme," IEEE Transactions on Power Electronics, vol. 18, no. 3, pp. 831−843, May 2003.

[140] **J.-S. Choi and F.-S. Kang**, "Seven-level PWM inverter employing series-connected capacitors paralleled to a single DC voltage source," IEEE Transactions on Industrial Electronics, vol. 62, no. 6, pp. 3448−3459, June 2015.

[141] **N. A. Rahim, K. Chaniago, and J. Selvaraj**, "Single-phase seven-level grid-connected inverter for photovoltaic system," IEEE transactions on Industrial Electronics, vol. 58, no. 6, pp. 2435−2443, June 2011.

[142] **R. S. Alishah, D. Nazarpour, S. H. Hosseini, and M. Sabahi**, "Reduction of power electronic elements in multilevel converters using a new cascade structure," IEEE Transactions on Industrial Electronics, vol. 62, no. 1, pp. 256−269, Jan. 2015.

[143] **N. A. Rahim, M. F. M. Elias, and W. P. Hew**, "Transistor-clamped H-bridge based cascaded multilevel inverter with new method of capacitor voltage balancing," IEEE transactions on Industrial Electronics, vol. 60, no. 8, pp. 2943−2956, Aug. 2013.

[144] **G. Ceglia, V. Guzman, C. Sanchez, F. Ibanez, J. Walter, and M. I. Gimenez**, "A new simplified multilevel inverter topology for DC–AC conversion," IEEE transactions on Power Electronics, vol. 21, no. 5, pp. 1311−1319, 2006.

[145] **E. Babaei**, "A cascade multilevel converter topology with reduced number of switches," IEEE Transactions on Power Electronics, vol. 23, no. 6, pp. 2657–2664, Nov. 2008.

[146] **E. Najafi and A. H. M. Yatim**, "Design and implementation of a new multilevel inverter topology," IEEE Transactions on Industrial Electronics, vol. 59, no. 11, pp. 4148−4154, Nov. 2012.

[147] **E. C. dos Santos, J. H. G. Muniz, E. R. C. da Silva, and C. B. Jacobina**, "Nested multilevel topologies," IEEE Transactions on Power Electronics, vol. 30, no. 8, pp. 4058−4068, Aug. 2015.

[148] **A. Masaoud, H. W. Ping, S. Mekhilef, and A. S. Taallah**, "New three-phase multilevel inverter with reduced number of power electronic components," IEEE Transactions on Power Electronics, vol. 29, no. 11, pp. 6018−6029, Nov. 2014.

[149] **A. Masaoud, H. W. Ping, S. Mekhilef, and A. Taallah**, "Novel configuration for multilevel DC-link three-phase five-level inverter," IET Power Electronics, vol. 7, no. 12, pp. 3052−3061, Dec. 2014.

[150] **E. Samadaei, S. A. Gholamian, A. Sheikholeslami, and J. Adabi**, "An envelope type (E-Type) module: asymmetric multilevel inverters with reduced components," IEEE Transactions on Industrial Electronics, vol. 63, no. 11, pp. 7148−7156, Nov. 2016.

[151] **E. Samadaei, A. Sheikholeslami, S. A. Gholamian, and J. Adabi**, "A square T-type (ST-Type) module for asymmetrical multilevel inverters," IEEE Transactions on Power Electronics, vol. 33, no. 2, pp. 987−996, Feb. 2018.

[152] **J. Liu, J. Wu, and J. Zeng**, "Symmetric/asymmetric hybrid multilevel inverters integrating switched-capacitor techniques," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 6, no. 3, pp. 1616−1626, Sept. 2018.

[153] **G.-J. Su**, "Multilevel DC-link inverter," IEEE Transactions on Industry Applications, vol. 41, no. 3, pp. 848−854, May/June 2005.

[154] **Y. Hinago and H. Koizumi**, "A single-phase multilevel inverter using switched series/parallel dc voltage sources," IEEE Transactions on Industrial Electronics, vol. 57, no. 8, pp. 2643−2650, Aug. 2010.

[155] **Y. Hinago and H. Koizumi**, "A switched-capacitor inverter using series/parallel conversion with inductive load," IEEE Transactions on Industrial Electronics, vol. 59, no. 2, pp. 878−887, Feb. 2012.

[156] **C.-C. Hua, C.-W. Wu, and C.-W. Chuang**, "A novel dc voltage charge balance control for cascaded inverters," IET Power Electronics, vol. 2, no. 2, pp. 147−155, Mar. 2009.

[157] **G.-J. Su**, "Multilevel DC link inverter," in *Industry Applications Conference, 2004. 39th IAS Annual Meeting. Conference Record of the 2004 IEEE*, 2004, pp. 806-812.

[158] **E. Najafi, A. Yatim, and A. Samosir**, "A new topology-Reversing Voltage (RV)-for multi level inverters," in *Power and Energy Conference, 2008. PECon 2008. IEEE 2nd International*, 2008, pp. 604-608.

[159] **W. K. Choi and F. S. Kang**, "H-bridge based multilevel inverter using PWM switching function," in *31st International Conference on Telecommunications Energy, INTELEC 2009*, Oct. 2009, p. 1−5.

[160] **S. Lee and F. Kang**, "A new structure of H-bridge Multilevel inverter," in *Proc. KIPE Conf*, 2008, p. 388−390.

[161] **J. Ebrahimi, E. Babaei, and G. B. Gharehpetian**, "A new multilevel converter topology with reduced number of power electronic components," IEEE Transactions on Industrial Electronics, vol. 59, no. 2, pp. 655−667, Feb. 2012.

[162] **N. A. Rahim and J. Selvaraj**, "Multistring five-level inverter with novel PWM control scheme for PV application," IEEE transactions on Industrial Electronics, vol. 57, no. 6, pp. 2111−2123, Jun. 2010.

[163] **J. Selvaraj and N. A. Rahim**, "Multilevel inverter for grid-connected PV system employing digital PI controller," IEEE transactions on Industrial Electronics, vol. 56, no. 1, pp. 149–158, Jan. 2009.

[164] **M. Khenar, A. Taghvaie, J. Adabi, and M. Rezanejad**, "Multi-level inverter with combined T-type and cross-connected modules," IET Power Electronics, vol. 11, no. 8, pp. 1407−1415, 15 Feb 2018.

[165] **M. Schweizer and J. W. Kolar**, "Design and implementation of a highly efficient three-level T-type converter for low-voltage applications," IEEE Transactions on Power Electronics, vol. 28, no. 2, pp. 899−907, Feb. 2013.

[166] **U. M. Choi, F. Blaabjerg, and K. B. Lee**, "Reliability Improvement of a T-Type Three-Level Inverter With Fault-Tolerant Control Strategy," IEEE Transactions on Power Electronics, vol. 30, no. 5, pp. 2660−2673, May 2015.

[167] **K. K. Gupta and S. Jain**, "A novel multilevel inverter based on switched DC sources," IEEE Transactions on Industrial Electronics, vol. 61, no. 7, pp. 3269−3278, July 2014.

[168] **K. K. Gupta and S. Jain**, "Comprehensive review of a recently proposed multilevel inverter," IET Power Electronics, vol. 7, no. 3, pp. 467–479, Jan. 2014.

[169] **Y.-H. Liao and C.-M. Lai**, "Newly-constructed simplified single-phase multistring multilevel inverter topology for distributed energy resources," IEEE Transactions on Power Electronics, vol. 26, no. 9, pp. 2386–2392, Sep. 2011.

[170] **Y. Ounejjar, K. Al-Haddad, and L.-A. Gregoire**, "Packed U cells multilevel converter topology: theoretical study and experimental validation," IEEE Transactions on Industrial Electronics, vol. 58, no. 4, pp. 1294–1306, Apr. 2011.

[171] **E. Babaei, S. Laali, and Z. Bayat**, "A single-phase cascaded multilevel inverter based on a new basic unit with reduced number of power switches," IEEE Transactions on Industrial Electronics, vol. 62, no. 2, pp. 922–929, Feb. 2015.

[172] **C. I. Odeh**, "A cascaded multi-level inverter topology with improved modulation scheme," Electric Power Components and Systems, vol. 42, no. 7, pp. 768−777, Apr. 2014.

[173] **C. I. Odeh, E. S. Obe, and O. Ojo**, "Topology for cascaded multilevel inverter," IET Power Electronics, vol. 9, no. 5, pp. 921−929, Apr. 2016.

[174] **A. Salem, E. M. Ahmed, M. Orabi, and M. Ahmed**, "New three-phase symmetrical multilevel voltage source inverter," IEEE Journal on Emerging and Selected Topics in Circuits and Systems, vol. 5, no. 3, pp. 430−442, Sept. 2015.

[175] **J. Li, J. Liu, D. Boroyevich, P. Mattavelli, and Y. Xue**, "Three-level active neutral-point-clamped zero-current-transition converter for sustainable energy systems," IEEE Transactions on Power Electronics, vol. 26, no. 12, pp. 3680–3693, Dec. 2011.

[176] **G. M. Martins, J. A. Pomilio, S. Buso, and G. Spiazzi**, "Three-phase low-frequency commutation inverter for renewable energy systems," IEEE Transactions on Industrial Electronics, vol. 53, no. 5, pp. 1522–1528, Oct. 2006.

[177] **C. Rech and J. R. Pinheiro**, "Hybrid multilevel converters: Unified analysis and design considerations," IEEE Transactions on Industrial Electronics, vol. 54, no. 2, pp. 1092–1104, Apr. 2007.

[178] **R. Lund, M. D. Manjrekar, P. Steimer, and T. A. Lipo**, "Control strategies for a hybrid seven-level inverter," in *Proceedings of the European Power Electronic Conference*, 1999.

[179] **Y. Wang, H. Li, X. Shi, and B. Xu**, "A novel carrier-based PWM strategy for hybrid multilevel inverters," in *2004 IEEE 35th Annual Power Electronics Specialists Conference (IEEE Cat. No. 04CH37551)*, 2004, pp. 4233–4237.

[180] **Online:**, "http://www.opal-rt.com/wp-content/themes/enfold-opal/pdf/L001610331.pdf."

[181] **J. Bélanger, P. Venne, and J.-N. Paquin**, "The what, where and why of real-time simulation," Planet Rt, vol. 1, no. 1, pp. 37–49, 2010.

[182] **O. Wasynczuk**, "Modeling and dynamic performance of a line-commutated photovoltaic inverter system," IEEE Power Engineering Review, vol. 9, no. 9, pp. 35–36, Sept. 1989.

[183] **M. V. M. Kumar and M. K. Mishra**, "Three-leg inverter-based distribution static compensator topology for compensating unbalanced and non-linear loads," IET power electronics, vol. 8, no. 11, pp. 2076–2084, Nov. 2015.

[184] **S. Jain and V. Agarwal**, "A single-stage grid connected inverter topology for solar PV systems with maximum power point tracking," IEEE transactions on power electronics, vol. 22, no. 5, pp. 1928–1940, Sept. 2007.