Thermal Evaluation of Space Vector PWM Based Four- level Dual Inverter Fed Open -End Winding Induction Motor Drive

B.Venugopal Reddy, V.T.Somasekhar
Electrical Engineering Department
National Institute of Technology, Warangal
Andhra Pradesh, India
bvenugopal_reddy@yahoo.co.in, vtsomasekhar@rediffmail.com

Abstract—**Multilevel inverters are increasingly being used due to their superior performance compared to two-level inverters. Different circuit topologies on multilevel inverters have been extensively researched. Conduction and switching losses of IGBT in multilevel inverter is the key factor which could influence the converter reliability and efficiency. In this paper, thermal evaluation is described for four level Neutral Point Clamped inverter and four-level dual inverter fed open-end winding induction motor drive using Space Vector Modulation.**

Keywords- Four-level inverter, Induction motor, Neutral Point Clamped Inverter, Space vector modulation, Thermal Analysis, Unequal DC-link voltages.

I. INTRODUCTION

There are four main topologies of multilevel inverters [1] relevant for large induction motor drive applications. They are neutral-point clamped inverters [2], series-connected H-bridge inverters [3], flying capacitor inverters [4] and dual-inverter fed open-end winding induction motor drives [5]. Advantages of open-end winding configuration is multilevel inversion is achieved using the conventional two-level inverters, redundancy of the space vector combinations for same space vector locations and the absence of neutral point fluctuations.

The thermal evaluation can be done by the characterization of loss parameters like switching loss and conduction loss as a function of device count and PWM strategy applied. At high switching frequencies, switching losses constitute a considerable portion of the device power dissipation. Numerical solution [9] of the junction temperature is possible by setting up a thermal model of power semiconductors and cooling systems, and connecting these thermal equivalent circuits, typically composed of RC networks to calculated power losses at different sections of the of the semiconductor switching device. Calculation of conduction losses and switching losses has been described in this paper.

In this paper conduction loss, switching loss and junction temperature rise have been calculated for four-level neutral point clamped inverter and dual inverter fed open-end winding induction motor drive configuration for same modulation index and performance is evaluated.

II. POWER CIRCUIT CONFIGURATIONS

A. Four-level dual inverter fed open-end winding induction motor power circuit configuration:

Four-level Power circuit configuration [6] of a dual inverter fed open-end winding induction motor with asymmetrical DC link voltages is shown in Fig.1. Inverter-1 is operated with a DC-link voltage of $2V_{dc}/3$, while inverter-2 is operated with a DC-link voltage of $V_{dc}/3$. Thus, the sum of the two DC-link voltages is equal to V_{dc}, which is the DC-link voltage of an equivalent conventional two-level inverter drive.

The implementation of this PWM strategy requires only instantaneous phase reference [7] voltages and does not require any lookup tables.

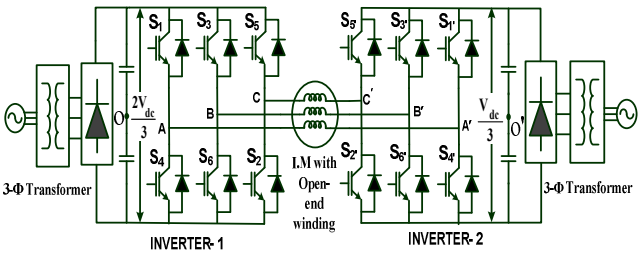

Fig.1: The four-level inverter drive with open-end winding topology

The symbols V_{AO}, V_{BO} and V_{CO} denotes the pole voltages of inverter-1, while the symbols $V_{A'O'}$, $V_{B'O'}$ and $V_{C'O'}$ denotes the pole voltages of inverter-2. Space vector locations from individual inverters are shown in Fig.2.

The numbers 1 to 8 refer to the states assumed by inverter-1. Similarly the numbers 1' to 8' indicate the states assumed by inverter-2(Fig.2). Combined 64 voltage space vectors are placed in 37 locations formed by 54 equilateral triangles of sides $V_{dc}/3$ is shown in fig.3. Table-I shows the states offered by both of these individual inverters. **OA3** represents the DC link voltage of the equivalent four-level inverter which is equal to V_{dc}.

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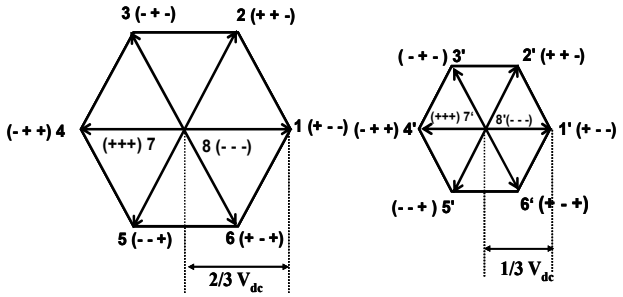

Fig.2 .Space vector locations for inverter-1 (Left) and inverter-2 (Right)

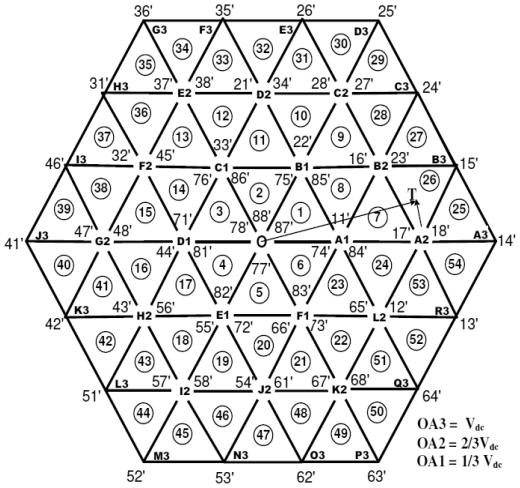

Fig.3 Resultant space-vector combinations of the dual-inverter scheme

TABLE -I

State of Inverter-1	Switches turned on	State of Inverter-2	Switches turned on
1 (+ - -)	S_6, S_1, S_2	1' (+ - -)	$S_{6'}$, $S_{1'}$, $S_{2'}$
2 (+ + -)	S_1, S_2, S_3	2' (+ + -)	$S_{1'}$, $S_{2'}$, $S_{3'}$
3 (- + -)	S_2, S_3, S_4	3' (- + -)	$S_{2'}$, $S_{3'}$, $S_{4'}$
4 (- + +)	S_3, S_4, S_5	4' (- + +)	$S_{3'}$, $S_{4'}$, $S_{5'}$
5 (- - +)	S_4, S_5, S_6	5' (- - +)	$S_{4'}$, $S_{5'}$, $S_{6'}$
6 (+ - +)	S_5, S_6, S_1	6' (+ - +)	$S_{5'}$, $S_{6'}$, $S_{1'}$
7 (+ + +)	S_1, S_3, S_5	7' (+ + +)	$S_{1'}$, $S_{3'}$, $S_{5'}$
8 (- - -)	S_2, S_4, S_6	8' (- - -)	$S_{2'}$, $S_{4'}$, $S_{6'}$

Switching states of the individual inverters

The reference voltage space vector (**OT,** Fig.3) is sampled for a fixed number of times (42) per one revolution. A Proposed [10] Inverter clamping PWM strategy (NSHC) for a four-level inverter is realized with the open-end winding configuration is extended to the four-level inverter in this paper.

The principle of the Inverter clamping is shown in Fig. 3. The reference vector OT can be split into two components namely OA2 and A2T. The component OA2 is obtained by clamping inverter-1and the other component A2T is realised in the average sense by switching inverter-2 around the sub hexagon center 'A'. The switching algorithm described in reference [7] for the implementation of centre- space SVM for a 2-level inverter feeding a conventional induction motor is extended for the computation of the switching timings for inverter-2 of the dual-inverter system.

Pole voltage of inverter-1(let V_{AO}), assumes two values, which are $V_{dc}/3$ and $-V_{dc}/3$. Similarly, the pole voltage corresponding to the A-phase leg of inverter-2, denoted as $V_{A'O'}$, assumes two values, $V_{dc}/6$ and $-V_{dc}/6$. As the pole voltage of each inverter is capable of assuming two values independently of the other, the difference of pole voltages assumes four values as shown in Table-II.

TABLE -II

Pole-voltage of inverter-1(V_{A0})	Pole-voltage of inverter-2 ($V_{A0'}$)	Motor phase voltage $V_{AA'} = V_{A0} - V_{A0'}$
$-V_{DC}/3$	$V_{DC}/6$	$-V_{DC}/2$
$-V_{DC}/3$	$-V_{DC}/6$	$-V_{DC}/6$
$V_{DC}/3$	$V_{DC}/6$	$V_{DC}/6$
$V_{DC}/3$	$-V_{DC}/6$	$V_{DC}/2$

The sum of the motor phase voltages $v_{AA'}$, $v_{BB'}$ and $v_{CC'}$ do not add to zero, meaning that there exists a large zero-sequence voltage. However, in this circuit configuration, a path is denied to the zero-sequence currents, as each inverter is operated with an isolated power supply. Consequently, the zero-sequence voltage is dropped across the points O and O'. This zero-sequence voltage is given by:

$$v_{zs} = \frac{1}{3}\left[\left(v_{AA'}\right)+\left(v_{BB'}\right)+\left(v_{CC'}\right)\right]$$

Where $v_{AA'} = v_{OA} - v_{O'A'}$

B. Four-level Neutral point clamped inverter power circuit configuration:

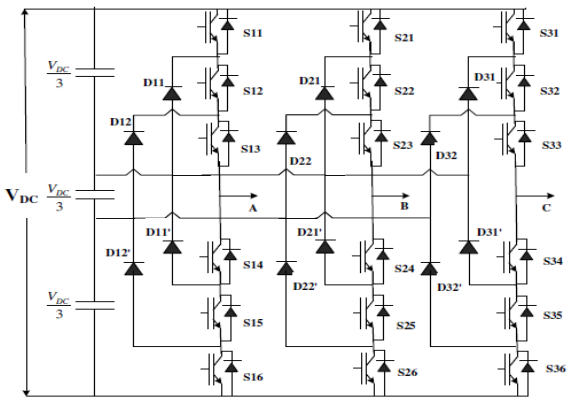

Fig.4. Power circuit configuration of Neutral Point Clamped inverter

From fig.4, it can be observed that each leg of the of the Neutral Point Clamped inverter [8] attain four levels ie., V_{dc}, $2*V_{dc}/3$, $V_{dc}/3$ and 0 (with respect to –ve rail of the DC bus) which depend on the state of the switching devices. The a-phase pole voltage 'v_{ao}' attains four-levels, which is shown in the Table-III. A '+' sign means that given switch is ON, '-' sign means that given switch is 'OFF'.

As each of the legs can attain four levels independently of the other, a total of 4^3 i.e. 64 switching combinations are possible with the switching devices of the above circuit.

In four-level NPC configuration the number of commutation paths is substantially higher and leading to a more conduction loss for the individual clamp diode or IGBT switch.

TABLE- III.

S11	S12	S13	S14	S15	S16	Vao
+	+	+	-	-	-	V_{dc}
-	+	+	+	-	-	$2V_{dc}/3$
-	-	+	+	+	-	$V_{dc}/3$
-	-	-	+	+	+	0

Switch states and output pole voltages of a-phase

III. Switching Loss, Conduction Loss and Junction Temperature Calculations

Practical switch has limited power handling capabilities. Switching losses occur at both turn-on and turnoff. For high-frequency operation the rising and falling times for voltage and current transitions play an important role.

The switching and conduction losses can be obtained for the top and bottom controlled switches and conduction losses in clamping diodes for NPC inverter which together add up to leg-losses of the inverter. Fig.5.shows one of A-phase leg of the dual inverter system. In this figure, pairs T_A^+ , D_A^+ and T_A^- , D_A^- are top and bottom controlled switches and their anti parallel diodes. Thus, the diodes along with the switches enable bidirectional current flow through the load. Diode losses are small as compared to the switch losses [9, 10]. Hence, the anti-parallel diodes are assumed to be ideal (loss free). Voltage across the switch and current through the switch (for $i_a > 0$) is shown in the Fig. 6, when it is operated with a switching time period of T_S .

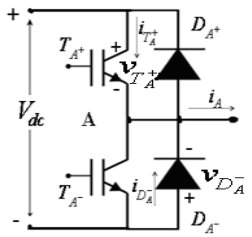

Fig.5. A-phase leg of an dual inverter system

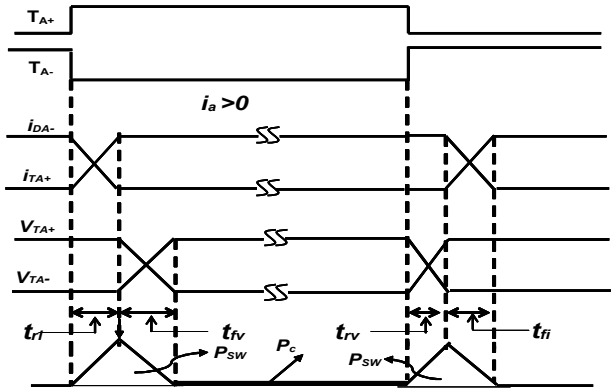

Fig.6. Switch current and voltage-drop across the switches of the inverter leg -A for $i_a>0$

The switching power loss in a power semi-conductor device is given by the following expression.

$$P_{loss} = \frac{V_{sw}\, I_{sw}\, (t_{ri} + t_{fv} + t_{rv} + t_{fi})\, f_s}{2} \qquad (1)$$

$$P_{loss} = \frac{V_{sw}\, I_{sw}\, (t_{on} + t_{off})\, f_s}{2} \qquad (2)$$

In the above expression, V_{SW} , I_{sw} , t_{on} , t_{off} and f_s respectively denote the voltage blocked by the switch when it is turned off, the current through the device when it is turned on, the turn-on time delay, the turn-off time delay and turn on, turn off transitions per second(f_s) of the device.

After obtaining the device loss (conduction + switching), these losses are given to an R-C thermal network in order to estimate the junction temperature rise of the device with respect to the ambient temperature. Three thermal impedances are normally considered in the thermal design of power converters. These thermal impedances are - junction to case impedance, case to heat-sink impedance and heat-sink to ambient impedance. The thermal resistance determines the steady state temperature, while the thermal capacitor determines the dynamics of the temperature rise. Same conditions as that of dual inverter system is considered for Neutral point clamped inverter for thermal analysis.

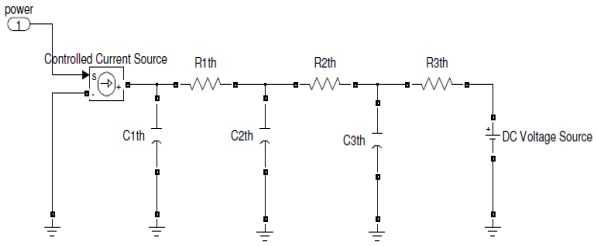

Fig.7. R-C electro-thermal model of the switching device

IV. SIMULATION RESULTS

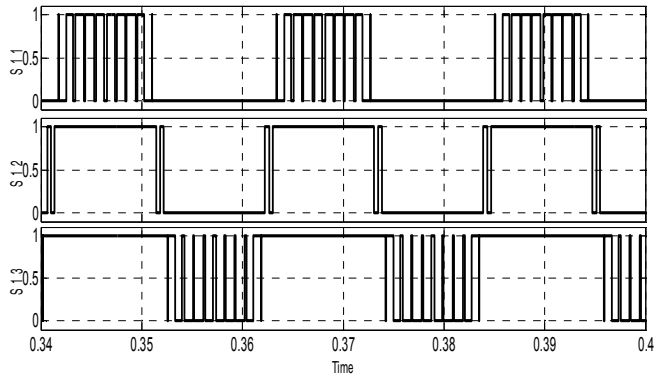

Fig.8. Gating pulses for the switches S_{11} , S_{12} and S_{13} of 4-level NPC inverter at m_a of 0.8.

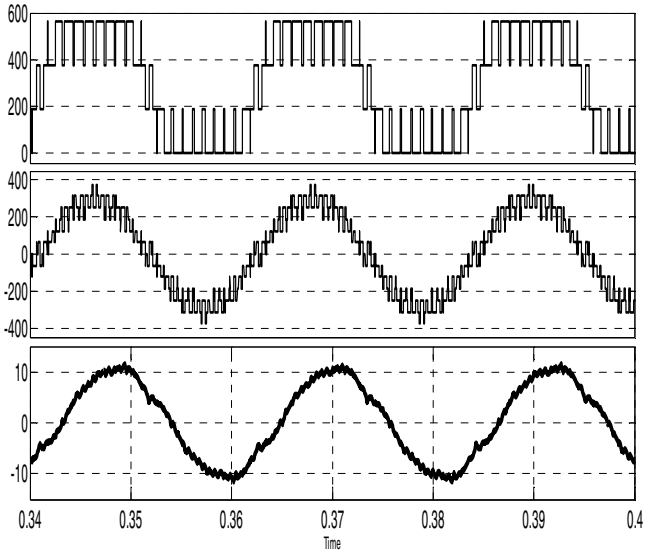

Fig.9. A-phase Pole voltage (top), phase voltage (middle) and phase current for ma= 0.8.

The secondary effects of switching such as the over-voltage across the switch while turn-off and blanking time are not considered in the in the given model.

Fig.8 shows the gating pulses for the switches S_{11} , S_{12} and S_{13}. Pole voltage, phase voltage and phase current are shown in fig.9 for modulation index of 0.8. Figure10 shows the each switching device power loss and corresponding junction temperature rise. From fig.10.it is clearly evident that the total average switch power loss for A-phase leg (conduction + switching) is 49W.

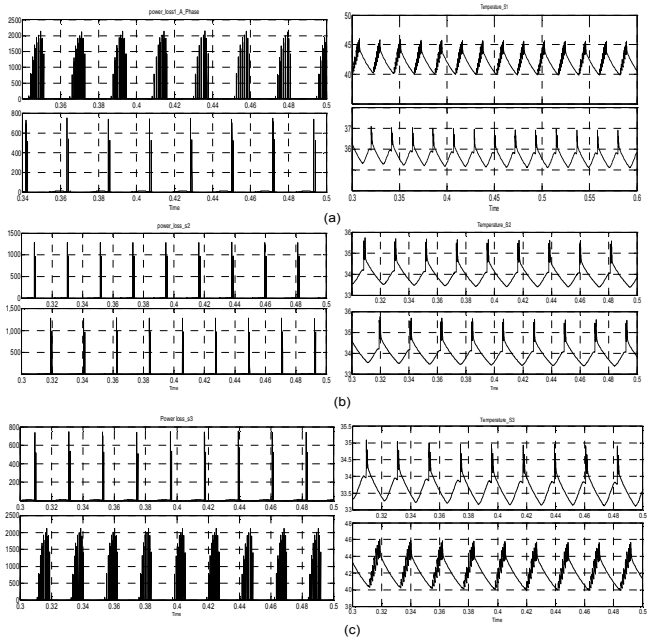

Fig.10. Power loss and junction temperature of 4-level NPC inverter for a A-phase leg a) S_{11}, $S_{11'}$ b) S_{12}, $S_{12'}$ c) S_{13}, $S_{13'}$.

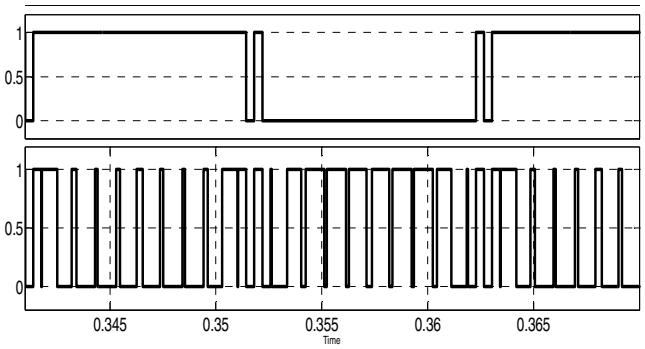

Fig.11. Reference waveforms (top) and gating pulses (a-phase) for the switches S_1 and $S_{1'}$ of dual inverter system for m_a=0.8

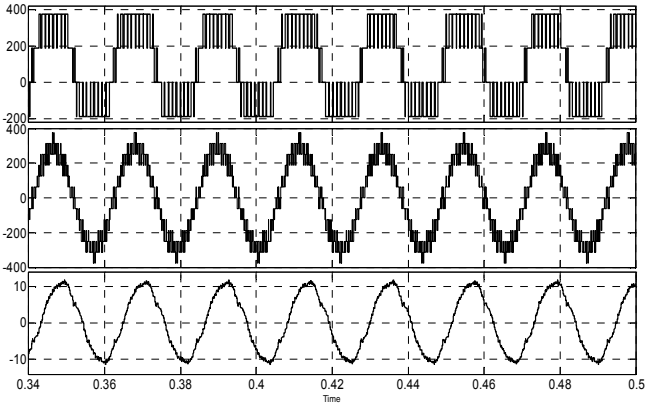

Fig.12. Difference of Pole voltages across the winding (top), phase voltage (middle) and phase current for an A-phase of 4-level Dual inverter system.

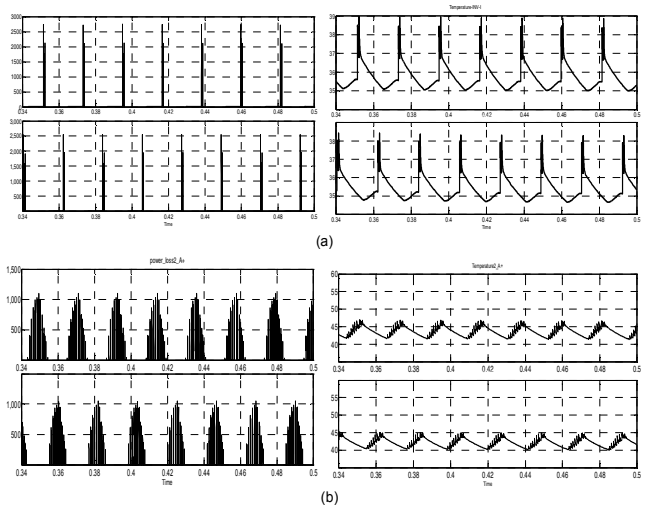

Fig.13. Power loss and junction temperature for a A-phase leg of 4-level Dual inverter system a) S_1, $S_{1'}$ b) S_2, $S_{2'}$.

Figure11 shows the switching pulses for the switches S_1 and $S_{1'}$ of dual inverter open-end winding induction motor drive corresponding A-Phase voltage and phase current is shown in fig.12. Fig13 shows that each switch power loss and corresponding junction temperature rise. From fig.13.it is clearly evident that the total average switch power loss of A-phase leg is 44.95W. Power loss obtained from the simulation results can manifest dual inverter system power loss can be reduced by 4.05W per leg hence overall dual inverter system loss is reduced by 12.15W compared to NPC inverter.

V. CONCLUSION

Four-level dual inverter fed open-end winding induction motor drive is realized with two 2-level inverters feeding an open-end winding induction motor drive from both ends. Thermal analysis for two different 4-level inverter topologies, namely Neutral point clamped inverter and Dual inverter system with open-end winding induction motor drive has been explained for same modulation index. From the results it can be conclude that the open-end winding induction motor drive system has less thermal loss compared to NPC 4-level inverter. Dual inverter system does not experience any neutral-point fluctuation as compared to NPC and the DC link capacitors carry only the ripple current as isolated DC supplies are used for the DC links. Switching device count is reduced, which reduces the cost of the Dual inverter system.

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