IET Power Electronics

Research Article

IET Journals
The Institution of Engineering and Technology

Capacitor-sharing two-output series-resonant inverter for induction cooking application

ISSN 1755-4535
Received on 14th February 2016
Revised on 4th May 2016
Accepted on 26th May 2016
doi: 10.1049/iet-pel.2016.0114
www.ietdl.org

Vijaya Bhaskar Devara[1], Vishwanathan Neti[2], Tanmoy Maity[3], Porpandiselvi Shunmugam[2] ✉

[1]*Electrical Engineering Department, Indian School of Mines, Dhanbad, Bihar 826004, India*
[2]*Department of Electrical Engineering, NIT Warangal, Warangal, Andhra Pradesh 506004, India*
[3]*Department of Mining Machinery Engineering, Indian School of Mines, Dhanbad, Jharkhand 826004, India*
✉ *E-mail: porpandiselvi@gmail.com*

Abstract: Induction heating (IH) technique has been widely used in industrial and domestic heating applications. In IH cooking applications, multi-output IH systems are increasing in demand. In this study, an inverter configuration is proposed for two-output IH cooking applications. The objective of this proposal is to reduce the component count and thereby the size of the circuit and cost. In this proposed configuration, two IH loads are connected to a full-bridge inverter output and these loads are sharing a common resonant capacitor. The output power is controlled using on–off control. Switching losses are reduced due to zero voltage switching operation. The two loads are independently controlled with high efficiency. The control logic of the proposed system is described in detail and prototype is designed, implemented and the validity is verified through experimental and simulation results.

1 Introduction

Induction heating (IH) plays a major role in industrial heating applications. It is a non-contact heating process and the heat is generated in the material itself [1]. IH technique is rapidly replacing the conventional heating methods used in industrial heating processes like welding, annealing, melting, surface hardening, and also in domestic cooking [2]. IH works on the principle of electromagnetic induction. In IH, an alternating magnetic field is produced by a high-frequency current carrying coil, placed around or below the specimen to be heated. This alternating magnetic field induces emf and thereby eddy currents in the specimen. These eddy currents are heating the specimen due to I^2R losses [1–3].

The IH system is modelled as a transformer with short-circuited single-turn secondary winding. Hence, the IH load can be represented as a series combination of equivalent inductance L_{eq} and resistance R_{eq}, where L_{eq} and R_{eq} are the equivalent inductance and resistance of the load as seen from the work coil [4]. Electromagnetic field analysis softwares can be used in modelling the IH load system [5, 6]. IH applications are operated with high-frequency inverters. The frequency range used in IH cooking applications is 20–150 kHz. Power metal–oxide–semiconductor field-effect transistors (MOSFETs) are preferable switching devices in this range. IH load has inherently a poor power factor. For this reason, the load is resonated by adding a resonant capacitor in series with IH load to improve the power factor. Hence, resonant inverters are used in supplying power to the induction coil at the desired frequency [7–9].

The commonly used inverter topologies in IH cooking applications are half-bridge [10–12] and full-bridge [13]. In some IH inverter circuits, output power is controlled by varying the switching frequency [14]. Variable frequency control is not a good solution in IH applications. It has several limitations like electromagnetic interference (EMI), low efficiency of the inverter and so on. These problems can be overcome by using fixed frequency control. The control techniques used with constant frequency operation are phase shift control (PSC) [15], asymmetrical duty cycle (ADC) [16], asymmetrical voltage cancellation (AVC) [17] and pulse density modulation (PDM) control [18, 19]. Among the above control techniques, PSC, ADC and AVC are duty cycle control methods, whereas PDM technique is on–off control [20].

In IH cooking applications, one load is powered by single inverter. Hence, for multiple loads, multiple inverters may be required. Disadvantages of this method are larger size, more number of components and high cost. An alternative solution for multiple loads is using a single inverter topology which can supply multiple loads. This method will be cost effective. Hence, for multi-output IH applications, there is a need for development of inverter topologies and control techniques. In the literature, some single inverter topologies are available for multi-output IH system.

In [21], a multi-load single converter system is proposed for low-power IH application. Single inverter is powering two series-resonant loads consisting of IH coils and resonant capacitors. First load is considered as master load and its power control is achieved by varying the switching frequency. Power in second load is controlled by changing the value of resonant capacitor. This is done by changing the number of capacitors connected in parallel by activating corresponding electromechanical switches. However, variable frequency control and use of electromechanical switches may lead to acoustic noise and EMI problems. A two-output series-resonant inverter has been proposed in [22]. The load powers are controlled by asymmetric voltage cancellation control method. Simultaneous and independent output control is achieved. In [23], two topologies for frequency synchronised resonant converters are proposed for multi-winding IH applications. In the first topology, a half-bridge inverter configuration with three switches is proposed to control two IH loads. Power in first coil is controlled by variable frequency control method and the second coil output power is controlled by duty cycle control. In the second topology, two half bridges are associated in a full-bridge configuration in order to reduce switching device stresses. Both loads are operated at constant frequency. However, the presence of average current in the induction coil and losses due to diode conduction makes these topologies suitable only for low-power applications. A two-output full-bridge high-frequency inverter is proposed with power factor improvement in [24]. Boost circuit in discontinuous conduction mode operation is used as power factor correction unit. Two switches of the inverter are shared by this boost circuit. AVC control is used for output power control. In [25], multi-load control is achieved using electromechanical relays which leads to EMI and acoustic noise problems. In [26], matrix converter is proposed for multi-output IH applications. PDM control is used for individual load power control. This topology has the combined advantages of

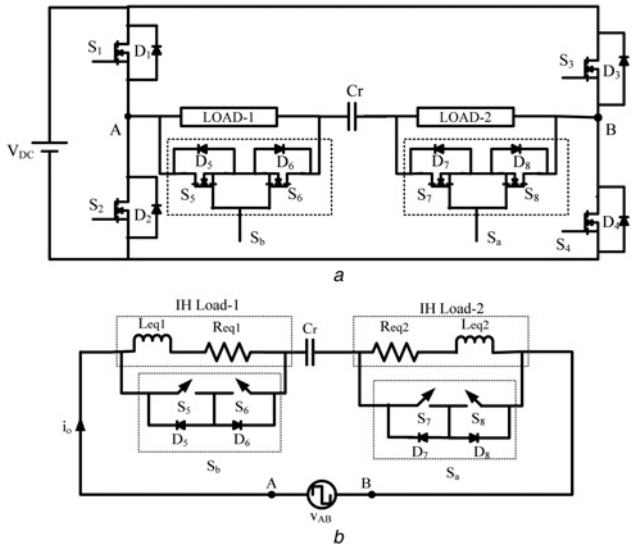


Fig. 1 *Proposed dual-output capacitor-sharing inverter*

a Circuit diagram
b Equivalent circuit

matrix converter and series-resonant multi-inverter. The limitation of this circuit is increased current harmonics under unbalanced operation of the circuit. Hence, proper design of electromagnetic compatibility filter is required. Discontinuous mode operation based control strategies have been proposed in [27] to improve converter performance at light-load conditions for multi-load systems.

There are limited number of circuits available in the literature for multi-output IH. Each circuit has its own advantages and limitations. This paper aims at introducing a resonant inverter configuration for the above said application with low component count and simple control. In this paper, a series-resonant inverter configuration is proposed for two-output IH cooking application. In this topology, a full-bridge inverter is operated with on–off control strategy and is supplying power to two IH coils. Conventionally, for each load coil, a resonant capacitor is required in IH applications. However, in the proposed topology, a single resonant capacitor is shared by two loads. Both the loads are operating simultaneously at same frequency. By using on–off control technique, wide range of output power control is achieved with high efficiency. The number of devices used in the proposed topology is less compared with the existing two-output IH cooking systems. Thus, cost of the system will be reduced.

2 Proposed inverter topology

The proposed capacitor-sharing dual-output IH system is shown in Fig. 1*a*. Load-1, load-2 and resonant capacitor (C_r) are connected in series across the output terminals (A and B) of a full-bridge inverter. The output voltage of inverter is v_{AB}. S_1, S_2, S_3 and S_4 are switching devices of the inverter, S_5 and S_6 are back-to-back connected switches and this switch pair is named as S_b and similarly S_7 and S_8 switch pair is named as S_a. These switch pairs S_a and S_b are connected across load-2 and load-1, respectively. S_a and S_b can conduct in either direction when the corresponding switches S_5 and S_6 or S_7 and S_8 are on. Also they do not conduct when the corresponding switches are off. In the proposed configuration, the switching devices used are power MOSFETs with low on-state resistance.

The equivalent circuit of the proposed configuration is shown in Fig. 1*b*, where L_{eq1} and R_{eq1} are equivalent inductance and resistance of the IH coil and vessel of IH load-1 referred to coil side, respectively. Similarly, L_{eq2} and R_{eq2} are, respectively, the equivalent inductance and resistance of the IH coil and vessel of the IH load-2 referred to the coil side. A single capacitor C_r is connected in series with two loads. In the proposed configuration, IH load-1 and IH load-2 are selected to be identical. Hence, the equivalent inductance of the IH loads are $L_{eq1} = L_{eq2} = L_{eq}$ and resistance of the IH loads are $R_{eq1} = R_{eq2} = R_{eq}$. IH load-1 and capacitor C_r are forming resonant load-1 and IH load-2 and same capacitor C_r are forming resonant load-2. As the load parameters are equal, the resonant frequencies of load-1 and load-2 are same and is expressed as

$$\text{Resonant frequency}, f_r = \frac{1}{2\pi\sqrt{L_{eq}C_r}}.$$

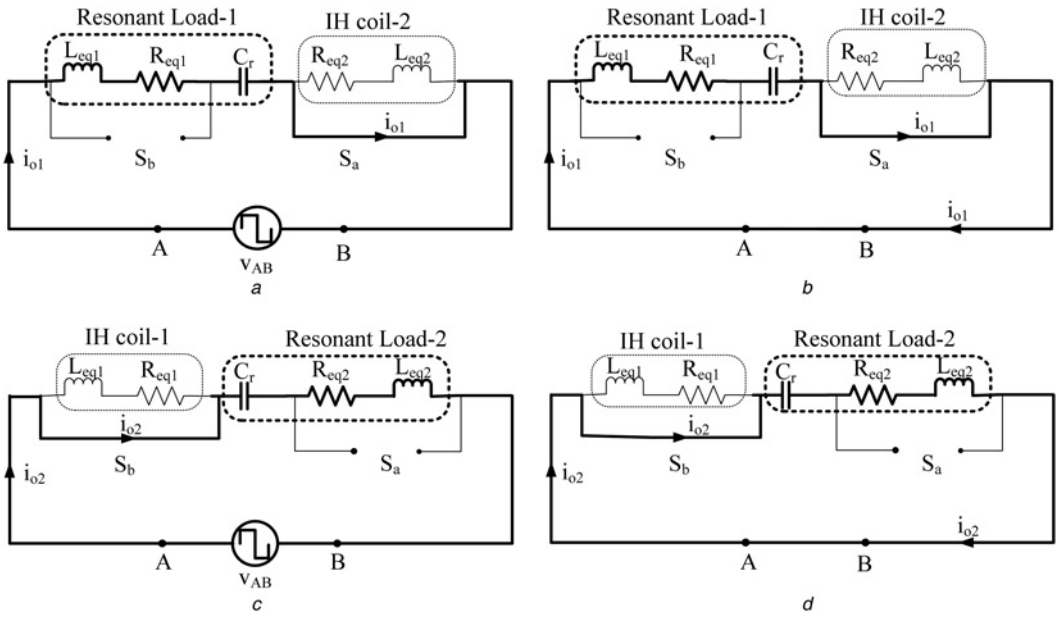


Fig. 2 *Load equivalent circuit during different modes of operation*

a Mode-1
b Mode-2
c Mode-3
d Mode-4

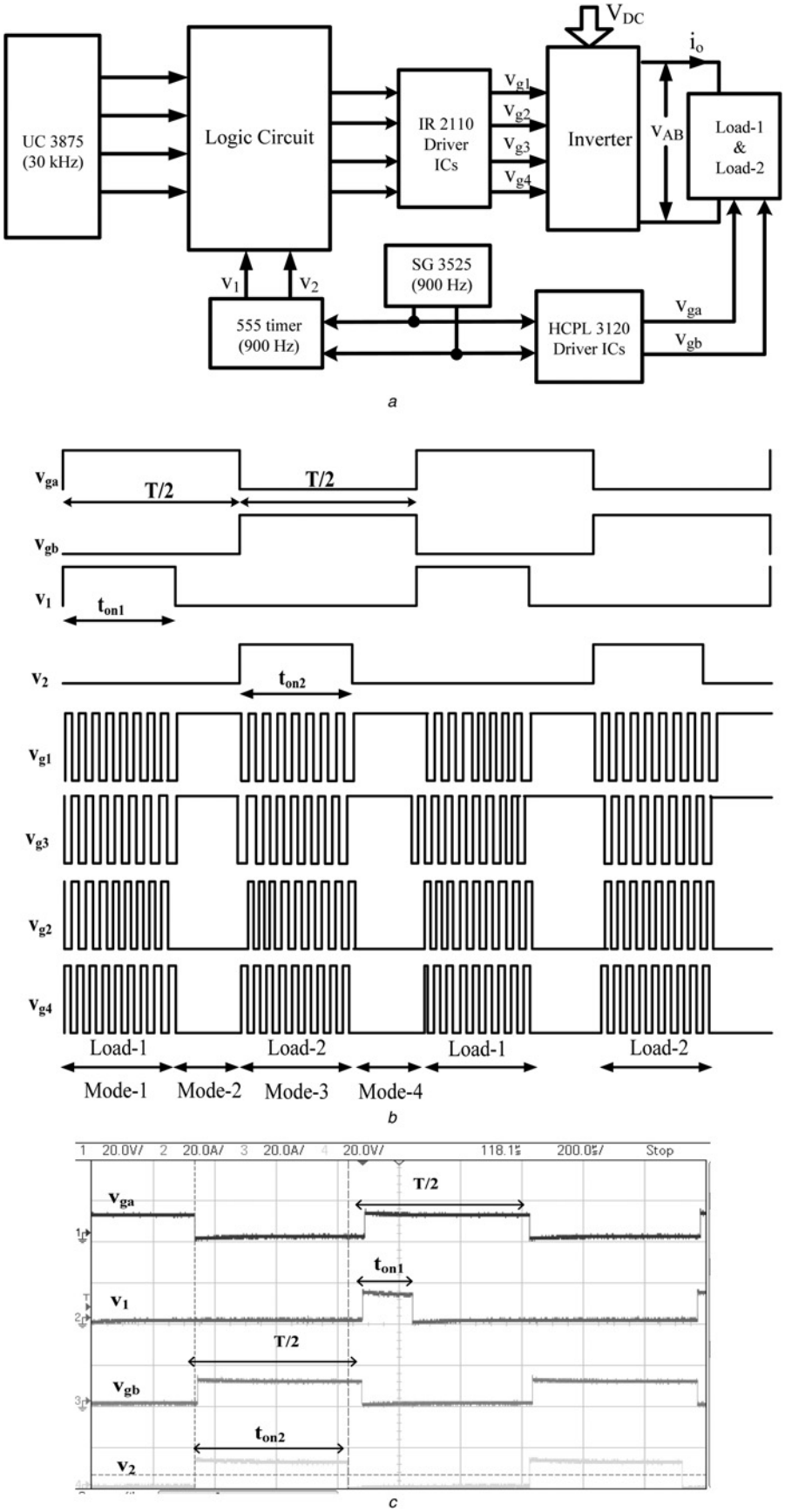


Fig. 3 *Control circuit*

a Block diagram
b Switching pulses
c Experimental switching pulses v_{ga}, v_{gb}, v_1 and v_2

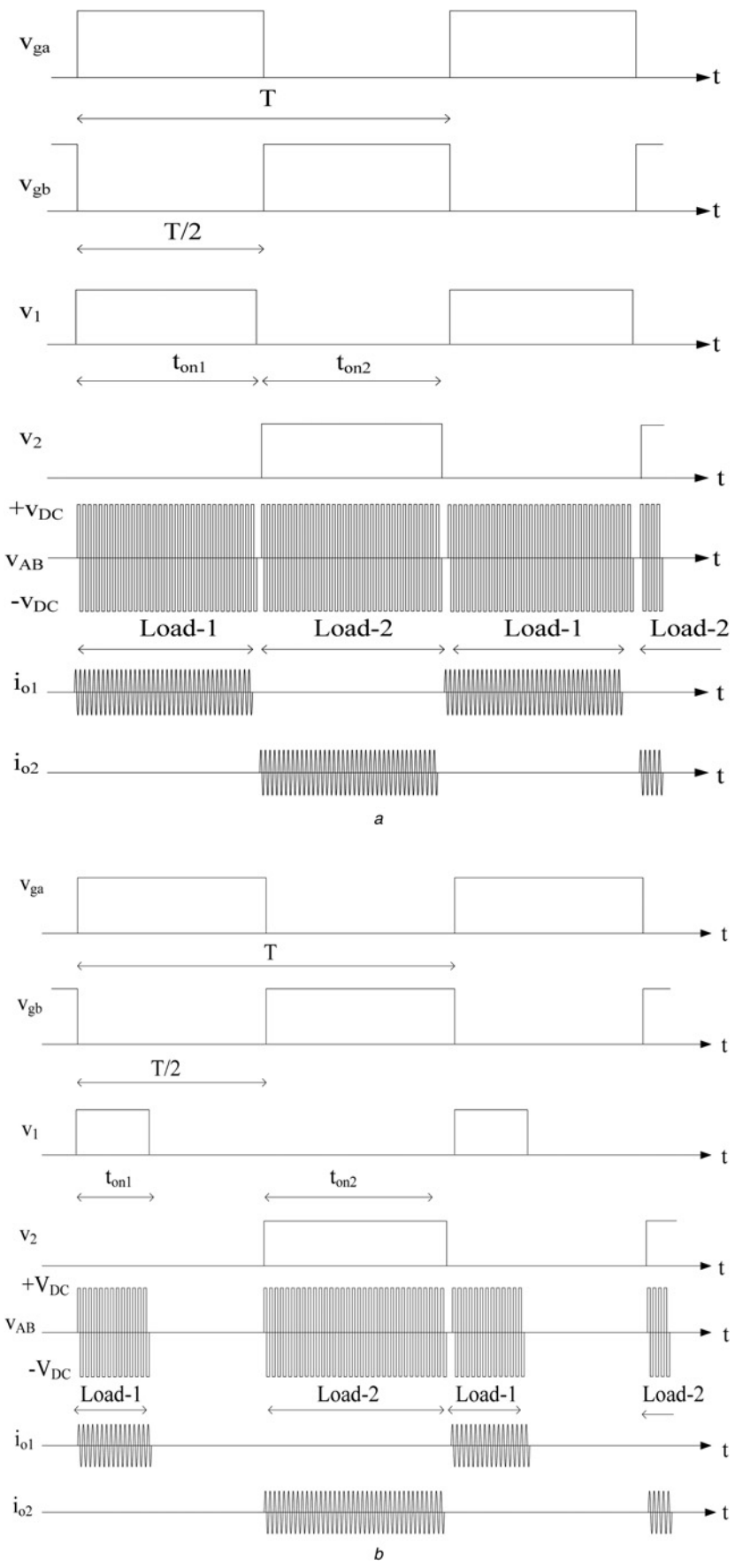


Fig. 4 *Waveforms for v_{ga}, v_{gb}, v_1, v_2, output voltage and load currents*

a $d_1 = d_2 = 0.48$
b $d_1 = 0.2$, $d_2 = 0.48$
c $d_1 = 0.48$, $d_2 = 0.35$

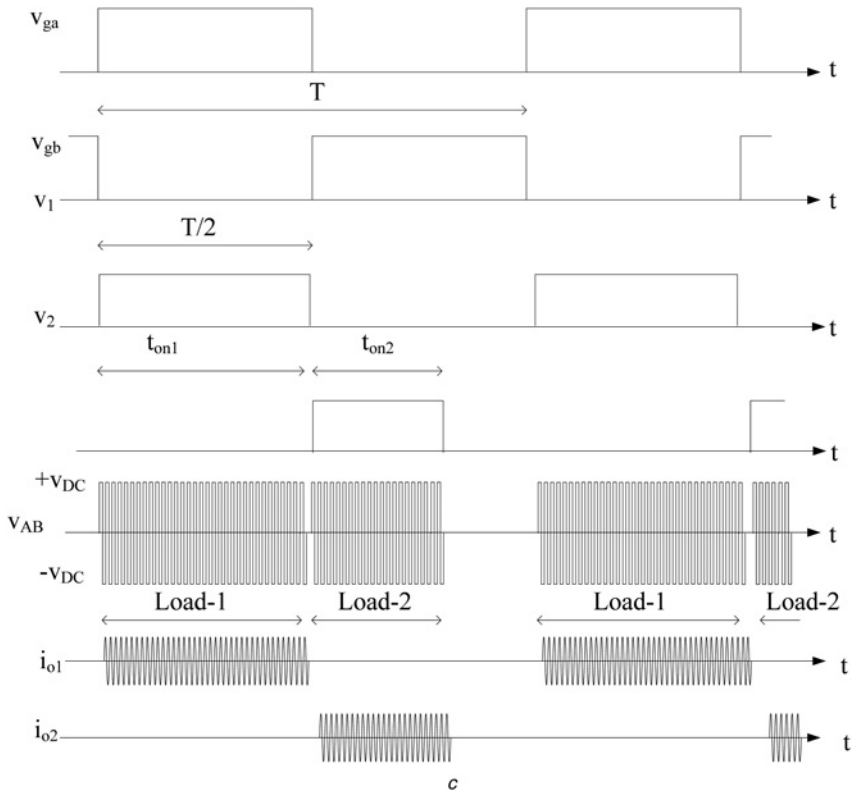


Fig. 4 *Continued*

The inverter switching frequency (f_s) is selected to be slightly above the resonant frequency (f_r) in order to achieve zero voltage switching (ZVS) and hence high efficiency. In the proposed configuration, inverter is operating at a constant frequency of 30 kHz.

3 Modes of operation

Switching devices of the inverter are controlled by high-frequency switching pulses $v_{g1} - v_{g4}$ and generate a square wave output voltage. The load control switch pairs S_a and S_b are switched at low frequency. Their switching pulses v_{ga} and v_{gb} are generated at 900 Hz with 0.5 duty cycle and they are complementary to each other. The proposed inverter operation can be divided into four modes. The equivalent circuits of the inverter load circuit during different modes are shown in Fig. 2.

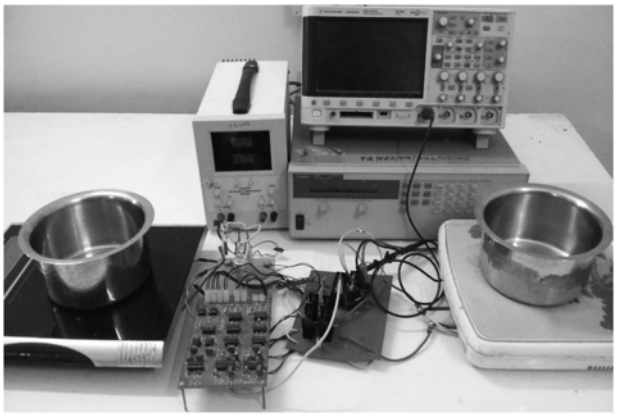
Mode-1: During mode-1, switch pair S_a is on and switch pair S_b is off. Hence, load-2 is short circuited and load-1 and C_r are connected across the inverter terminals. Series combination of load-1 and C_r forms resonant load-1. High-frequency inverter output voltage is applied across resonant load-1 and it draws a sinusoidal current. Hence, IH coil-1 is powered during this mode. The amount of power supplied to IH coil-1 depends on the duration of this mode. i_{o1} is the load-1 current in this mode.
Mode-2: During mode-2, S_a and S_b remain in same switching states as during mode-1. Before powering load-2, the energy stored in L_{eq1} should be transferred to the load. To achieve this, inverter switches S_1 and S_3 are kept in 'on-state' while S_2 and S_4 are in 'off-state'. Inverter output voltage $v_{AB} = 0$. Energy in L_{eq1} is free wheeled through S_1 and S_3. The current in IH coil-1 becomes zero during this mode.
Mode-3: Switch pair S_a is turned off and switch pair S_b is on. Hence, load-1 is short circuited and load-2 and C_r are connected across the inverter terminals. Series combination of load-2 and C_r forms resonant load-2. High-frequency inverter output voltage is applied across resonant load-2 and it draws a sinusoidal current. Thus, during this mode, high-frequency current flows through IH coil-2 and load-2 is powered. i_{o2} is the load-2 current in this mode.
Mode-4: Mode-4 operation is similar to that of mode-2. S_a and S_b remain in same switching states as during mode-3. S_1 and S_3 are in 'on-state' and S_2 and S_4 are in 'off-state'. Inverter output voltage $v_{AB} = 0$. During this mode energy stored in L_{eq2} is transferred to the load through S_1 and S_3. The current in IH coil-2 reduces to zero.

4 Control circuit design

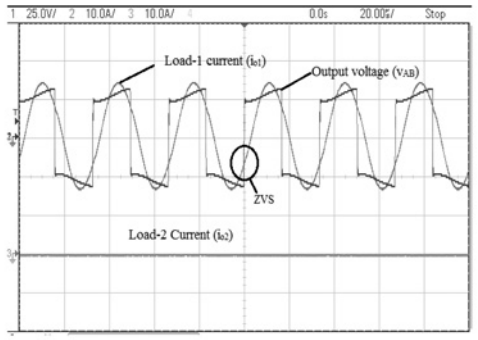
The block diagram of the control circuit is shown in Fig. 3*a*. UC3875 PWM integrated circuit (IC) is used to generate the inverter switching pulses. This IC generates switching pulses at a frequency of 30 kHz. The switching pulses v_{ga} and v_{gb} for load control devices S_a and S_b, respectively, are derived from another control IC SG3525 at a frequency of 900 Hz. These pulses are complementary to each other with 50% duty cycle. On–off control pulses v_1 and v_2 are derived from 555 timer ICs. These pulses v_1 and v_2 are synchronised with v_{ga} and v_{gb}, respectively. The on duration of v_1 and v_2 are t_{on1} and t_{on2}, respectively. The durations for which load-1 and load-2 are powered is controlled by t_{on1} and t_{on2}, respectively. v_1 and v_2 are logically combined with 3875 output pulses to generate switching pulses of inverter devices (v_{g1}, v_{g2}, v_{g3} and v_{g4}). IR2110 and HCPL 3120 are the driver ICs used. Switching pulses to inverter devices, load control devices and on–off control pulses are shown in Fig. 3*b*. Experimental switching pulses v_{ga} and v_{gb} and on–off control pulses v_1 and v_2 are shown in Fig. 3*c*.

As shown in Fig. 3*b*, when v_{ga} and v_1 are high, inverter switching pulses are generated corresponding to mode-1 operation. In this duration, load-1 is powered by the inverter. When v_{ga} is high and v_1 is low, the switching pulses generated are corresponding to mode-2 operation. Now v_{g2} and v_{g4} are low, and v_{g1} and v_{g3} are maintained at high level. With this switching pattern upper switching devices S_1 and S_3 are on and lower devices S_2 and S_4 are off. Inverter output voltage $v_{AB} = 0$ and energy in load-1 freewheels through S_1 and S_3. When v_{gb} and v_2 are high, the

IET Power Electron., 2016, Vol. 9, Iss. 11, pp. 2240–2248



a



b

Fig. 5 *Experimental setup and waveforms showing ZVS*

a Experimental setup for two-output IH cooking system
b Experimental waveforms of inverter output voltage and output currents

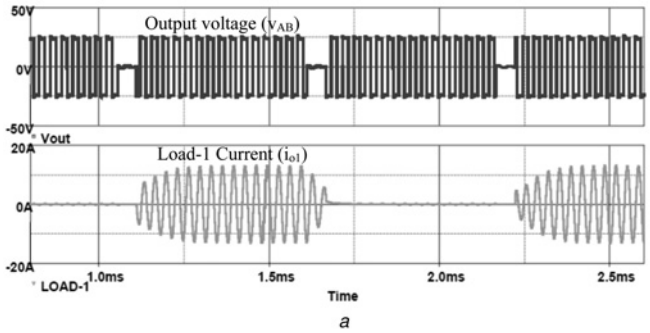
Table 1 Parameters of proposed dual-load configuration

Description	Symbol	Value
source voltage	V_{DC}	25 V
equivalent resistance of each load	$R_{eq1} = R_{eq2} = R_{eq}$	1.96 Ω
equivalent inductance of each load	$L_{eq1} = L_{eq2} = L_{eq}$	68 μH
resonant capacitor of the circuit ($2 \times 0.22\ \mu F = 0.44\ \mu F$)	C_r	0.44 μF
resonant frequency of the each load	f_r	29.09 kHz
switching frequency of the circuit	f_s	30 kHz
MOSFETs used	IRFP4110PbF	100 V, 180 A, $r_{DS} = 3.7\ m\Omega$
control ICs	UC3875, SG3525 and 555 timer	
driver IC	IR2110 and HCPL3120	

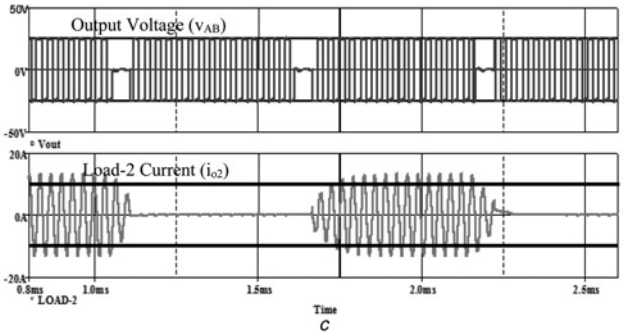
switching pulses are generated corresponding to mode-3 operation during which load-2 is powered. When v_{gb} is high and v_2 is low, the switching pulses are generated for mode-4 operation which is identical to mode-2 operation. Inverter output voltage $v_{AB} = 0$ and energy in load-2 freewheels through S_1 and S_3.

5 Output power control

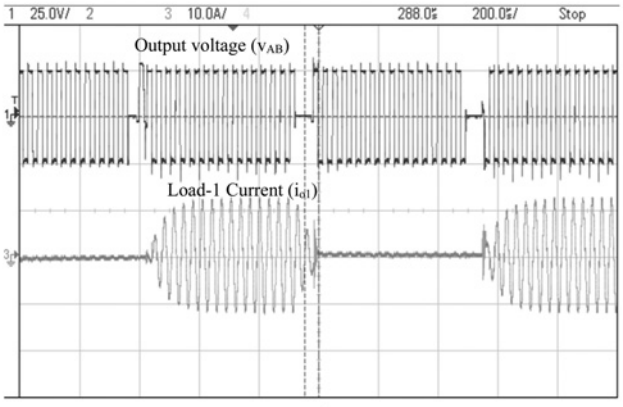
In the proposed capacitor-shared dual-output IH system, on–off control is used to control load power. The loads are alternatively supplied, for duration of $T/2$, where T is the switching period of the devices S_a and S_b. These devices are switched at 900 Hz. When S_a is on, load-1 is connected to inverter output voltage v_{AB} and when S_b is on, load-2 is supplied with v_{AB}. The load output



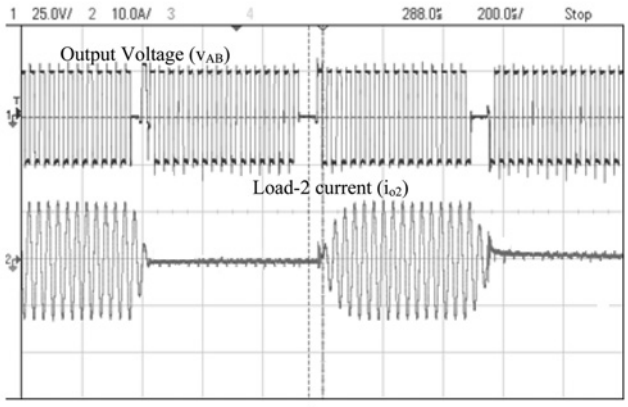
a



c



b



d

Fig. 6 *Simulation and experimental waveforms at $d_1 = d_2 = 0.45$*

a Simulation waveforms of v_{AB} and i_{o1}
b Experimental waveforms of v_{AB} and i_{o1} (scale: voltage: 25 V/div, current: 10 A/div)
c Simulation waveforms of v_{AB} and i_{o2}
d Experimental waveforms of v_{AB} and i_{o2} (scale: voltage: 25 V/div, current: 10 A/div)

powers are independently controlled by on–off control technique. The duration for which voltage is applied to loads is controlled by the on duration of control pulses v_1 and v_2. The duty cycles of load-1 and load-2 are expressed as $d_1 = t_{on1}/(T/2)$ and $d_2 = t_{on2}/(T/2)$, respectively. During t_{on1}, S_a is on and load-2 is bypassed through S_a. Hence, load-1 is connected to the inverter output and output current i_{o1} flows through load-1. In the next half cycle, S_b is on and during t_{on2}, V_{AB} is applied to load-2 and a current of i_{o2} flows through load-2. By varying t_{on1} and t_{on2}, respective duty cycles d_1 and d_2 are varied, thereby the output powers of load-1 and load-2 can be controlled accordingly. The waveforms of v_{ga}, v_{gb}, v_1, v_2, corresponding inverter output voltage V_{AB} and load currents are shown in Fig. 4 for different combinations of duty cycles d_1 and d_2. For $d_1 = d_2 = 0.48$, the output powers to load-1 and load-2 are maximum as seen in Fig. 4*a*. Fig. 4*b* shows the outputs for $d_1 = 0.2$, $d_2 = 0.48$ and Fig. 4*c* shows outputs corresponding to $d_1 = 0.48$, $d_2 = 0.35$. From this figure, it is seen that the density of output voltage pulses and current to the loads are changing according to corresponding duty cycles of the loads. This shows that independent output power control is possible with this proposed topology.

In the proposed circuit, load-1 and load-2 currents become zero during t_{off1} and t_{off2}, respectively, where $t_{off1} = (T/2) - t_{on1}$ and $t_{off2} = (T/2) - t_{on2}$. The condition for this operation is, $t_{off1} \gg \tau$ and $t_{off2} \gg \tau$, where characteristic delay time of load circuit $\tau = 2L_{eq1}/R_{eq1} = 2L_{eq2}/R_{eq2}$. With on–off control [18], output power is proportional to the pulse density duty cycle when $T \gg \tau$.

The peak value of fundamental component of inverter output voltage (v_{AB}) is expressed as

$$v_{AB} = \frac{4}{\pi} V_{DC} \tag{1}$$

$$\text{Average power of load-1, } P_{o1} = I_{o1}^2 \cdot R_{eq1} \cdot d_1 = \left(\frac{v_{AB}}{\sqrt{2}Z_{eq1}}\right)^2 R_{eq1} d_1 \tag{2}$$

$$\text{Average power of load-2, } P_{o2} = I_{o2}^2 \cdot R_{eq2} \cdot d_2 = \left(\frac{v_{AB}}{\sqrt{2}Z_{eq2}}\right)^2 R_{eq2} d_2 \tag{3}$$

Total output power of the inverter, $P_o = P_{o1} + P_{o2}$

$$P_o = I_{o1}^2 \cdot R_{eq1} \cdot d_1 + I_{o2}^2 \cdot R_{eq2} \cdot d_2 \tag{4}$$

where I_{o1} is rms load current of load-1 during mode-1, I_{o2} is rms load current of load-2 during mode-3. d_1 and d_2 are duty cycles of load-1 and load-2, respectively.

6 Experimental and simulation results

A 138 W prototype of dual-output inverter with capacitor sharing has been implemented for IH cooking application. The experimental setup is shown in Fig. 5*a*. The circuit parameters used are shown in Table 1. The input voltage $V_{DC} = 25$ V. The equivalent load-1 and load-2 parameters are measured from the coil side with the vessels kept over the IH coils. The load parameters are chosen to be identical. Hence, the resonant frequencies of resonant load-1 and resonant load-2 are same. The inverter switching frequency is 30 kHz and resonant frequency of the load is 29.09 kHz. As $f_s > f_r$, the series-resonant load circuit operates effectively in inductive mode. Hence, load current lags behind the output voltage and makes turn off current positive in the switching devices. This ensures ZVS in each cycle of operation in the proposed inverter configuration. Fig. 5*b* shows experimental waveforms of output voltage and load currents when load-1 is on. It is observed that ZVS is maintained during the operation. During load-2 operation also ZVS exists due to the similar load parameters.

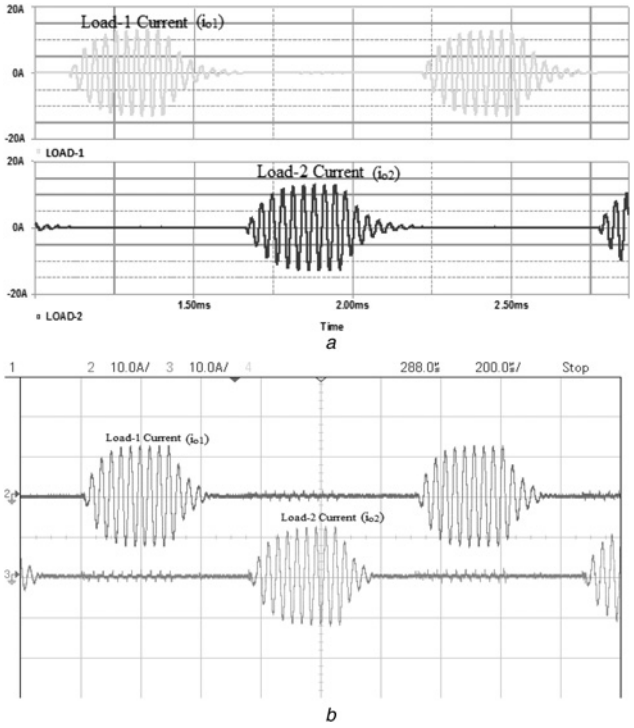


Fig. 7 *Simulation and experimental waveforms at $d_1 = d_2 = 0.25$*
a Simulation waveforms of i_{o1} and i_{o2}
b Experimental waveforms of i_{o1} and i_{o2} (scale: current: 10 A/div)

Load-1 and load-2 output powers are independently controlled by on–off control technique. The simulation and experimental results

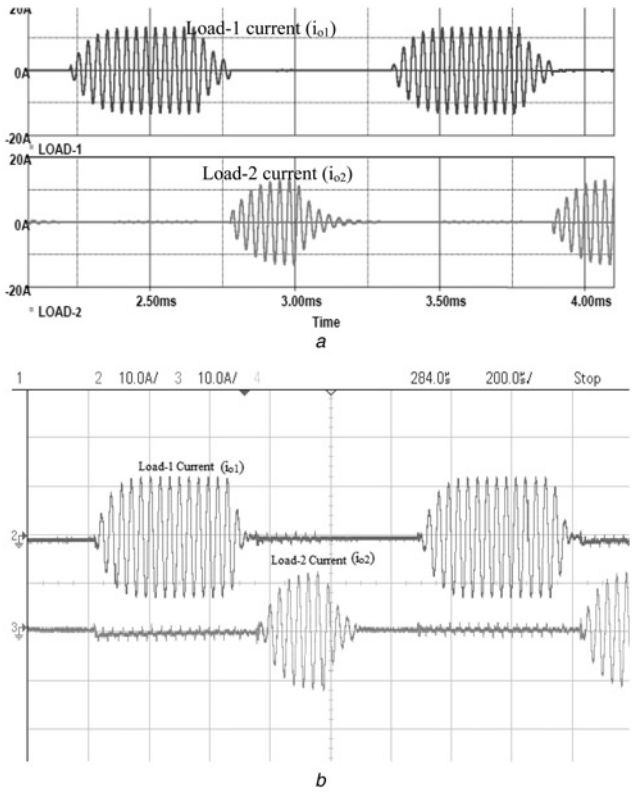


Fig. 8 *Simulation and experimental waveforms at $d_1 = 0.36$ and $d_2 = 0.25$*
a Simulation waveforms of i_{o1} and i_{o2}
b Experimental waveforms of i_{o1} and i_{o2} (scale: current: 10 A/div)

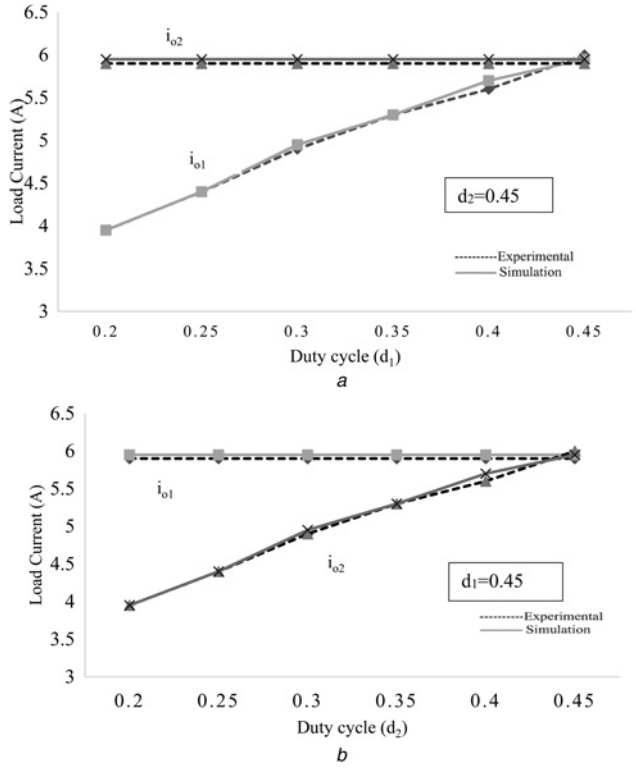


Fig. 9 *Load currents against duty cycle*

a i_{o1} and i_{o2} against load-1 duty cycle (d_1)
b i_{o1} and i_{o2} against load-1 duty cycle (d_2)

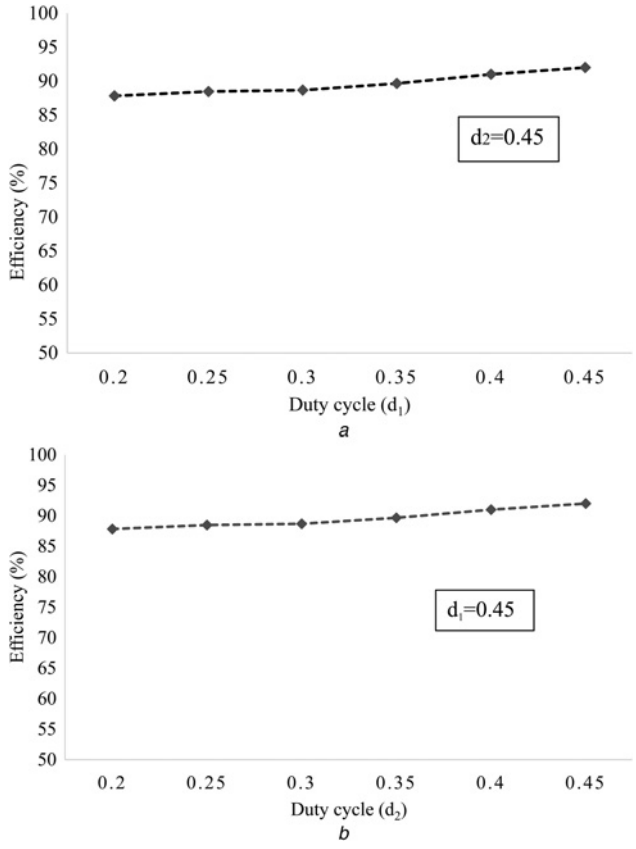


Fig. 10 *Overall efficiency against duty cycle*

a Overall efficiency against load-1 duty cycle (d_1)
b Overall efficiency against load-2 duty cycle (d_2)

are shown for different combinations of load-1 and load-2 duty cycles d_1 and d_2, respectively. Fig. 6 shows the simulation and experimental waveforms of the inverter at $d_1 = d_2 = 0.45$. Fig. 6*a* shows the simulation waveforms of v_{AB} and i_{o1}. Fig. 6*b* shows experimental waveforms of inverter output voltage v_{AB} and i_{o1}. Figs. 6*c* and *d* show the simulation and experimental waveforms of inverter output voltage v_{AB} and i_{o2}.

Fig. 7 shows the simulation and experimental waveforms of load-1 current (i_{o1}) and load-2 current (i_{o2}) for $d_1 = d_2 = 0.25$. Fig. 8 shows the simulation and experimental waveforms for load-1 current (i_{o1}) and load-2 current (i_{o2}) for $d_1 = 0.36$ and $d_2 = 0.25$, respectively. From Figs. 6–8, it is observed that the maximum value of the load currents are equal and remaining same for any value of duty cycle. However, the duration of this current waveform changes according to the corresponding duty cycle. Hence, the output currents and corresponding output powers can be controlled by varying duty cycles. Thus, two loads are independently controlled by varying corresponding duty cycle. It is also observed that experimental results are in good agreement with the simulation results.

7 Analysis of results and overall efficiency

In the proposed single capacitor-sharing dual-output inverter, power control is achieved through on–off control. The plot of load currents against load-1 duty cycle (d_1) is shown in Fig. 9*a*. It can be observed that load-1 current is varying with its duty cycle d_1 and load-2 current remains almost constant. Simulation and experimental results are in good agreement with each other. Similarly, load-1 and load-2 currents with varying load-2 duty cycle (d_2) are shown in Fig. 9*b*. It can be observed that load-2 current is varying with its duty cycle d_2 and load-1 current remains almost constant. It is also observed that simulation and experimental results are in good agreement with each other. Hence, independent control of load-1 and load-2 currents is possible with this circuit, where single resonant capacitor is shared by two loads.

The total inverter output power is the sum of output powers of load-1 (P_{o1}) and load-2 (P_{o2}). The output power is calculated based on (4). The input power of the inverter is calculated as the product of input voltage (V_{DC}) and input current (I_{DC}) of the inverter. Overall efficiency is calculated from the total output power and input power.

Overall efficiency curves of the proposed inverter are shown in Figs. 10*a* and *b*. In Fig. 10*a*, load-1 output power is varied while load-2 output power is kept constant. In Fig. 10*b*, load-2 output power is varied while load-1 output power kept constant. It can be observed that the overall efficiency remains considerably high for wide variation of duty cycle under both situations.

As the number of resonant capacitors is reduced in the proposed configuration, cost is also reduced as compared with dual-load IH inverters which are using two resonant capacitors. The number of switching devices used is same as that of two inverter circuits. However, the switching loss in S_a and S_b is less due to low operating frequency (900 Hz). Hence, the efficiency is higher than two inverter topologies for IH applications. The proposed system is simple, cost effective and also has higher efficiency and wider range of power control. The proposed configuration can be extended for more than two loads also.

8 Conclusion

In this paper, a two-load inverter for IH application has been proposed with a single resonant capacitor shared by both loads. This proposed IH system possesses many advantages compared with the existing two-load IH inverter circuits. The number of passive components used in the proposed circuit is less, as single capacitor is used for two loads. Reduction in the number of resonant capacitors used leads to decrease in the cost of the proposed system. As the switching devices used in switching pairs S_a and S_b are operating at low frequency, the switching losses are

less and can be ignored. The control technique used is also simple and effective. Independent load power control is achieved in the proposed circuit. The proposed circuit has been implemented and the experimental and simulation results are found to be in good agreement with each other. High efficiency is achieved over wide on–off control ranges due to ZVS operation of the switching devices. The proposed system is designed for two-load IH cooking application but the design can be implemented for higher number of loads also. It can be used for more number of loads with considerable reduction of overall cost.

9 References

1 Lucıa, O., Maussion, P., Dede, E.: 'Induction heating technology and its applications: past developments, current technology, and future challenges', *IEEE Trans. Ind. Electron.*, 2014, **61**, (5), pp. 2509–2520

2 Porpandiselvi, S., Vishwanathan, N.: 'Three-leg inverter configuration for simultaneous dual-frequency induction hardening with independent control', *IET Power Electron. J.*, 2015, **8**, (9), pp. 1571–1582

3 Porpandiselvi, S., Vishwanathan, N.: 'Single inverter configuration for simultaneous dual frequency induction hardening with independent control', *Eur. Power Electron. Drives J.*, 2014, **24**, (1), pp. 5–13

4 Nabil Ahmed, A.: 'High-frequency soft-switching AC conversion circuit with dual-mode PWM/PDM control strategy for high-power IH applications', *IEEE Trans. Ind. Electron.*, 2011, **58**, (4), pp. 1440–1448

5 Carretero, C., Lucia, O., Acero, J., Alonso, R., Burdio, J.M.: 'Frequency-dependent modeling of domestic induction heating systems using numerical methods for accurate time-domain simulation', *IET Power Electron.*, 2012, **5**, (8), pp. 1291–1297

6 Wojda, R.P., Kazimierczuk, M.K.: 'Winding resistance of litz-wire and multi-strand inductors', *IET Power Electron.*, 2012, **5**, (2), pp. 257–268

7 Kifune, H., Hatanaka, Y., Nakaoka, M.: 'Quasi-series-resonant-type soft-switching phase shift modulated inverter', *Proc. Inst. Electr. Eng., Electr. Power Appl.*, 2003, **150**, (6), pp. 725–732

8 Ogura, K., Gamage, L., Ahmed, T., Nakaoka, M., Hirota, I., Yamashita, H., Omori, H.: 'Performance evaluation of edge-resonant ZVS-PWM high-frequency inverter using trench-gate IGBTs for consumer induction cooking heater', *Proc. Inst. Electr. Eng., Electr. Power Appl.*, 2004, **151**, (5), pp. 563–568

9 Sarnago, H., Lucia, O., Mediano, A., Burdio, J.M.: 'High efficiency parallel quasi-resonant current source inverter featuring SiC MOSFETs for induction heating systems with coupled inductors', *IET Power Electron.*, 2013, **6**, (1), pp. 183–191

10 Koertzen, H.W., Van Wyk, J.D., Ferreira, J.A.: 'Design of the half-bridge series resonant converter for induction cooking'. Proc. of IEEE Power Electronics Specialists Conf. (PESC), 1995, pp. 729–735

11 Kwon, Y.S., Yoo, S., Hyun, D.: 'Half bridge series resonant inverter for induction heating applications with load adaptive PFM control strategy'. Proc. of IEEE Applied Power Electronics Conf., 1999, pp. 575–581

12 Ahmed, N.A., Nakaoka, M.: 'Boost-half-bridge edge resonant soft switching PWM high-frequency inverter for consumer induction heating appliances', *Proc. Inst. Electr. Eng., Electr. Power Appl.*, 2006, **153**, (6), pp. 932–938

13 Dede, E.J., Gonzalez, J.V., Linares, J.A., *et al.*: '25-kW/50-kHz generator for induction heating', *IEEE Trans. Ind. Electron.*, 1991, **38**, (3), pp. 203–209

14 Isobe, T., Usuki, K., Arai, N., *et al.*: 'Variable frequency induction heating using magnetic energy recovery switch (MERS)'. Proc. of IEEE PESC, 2008, pp. 2139–2145

15 Zhongming, Y., Jain, P.K., Sen, P.C.: 'A full-bridge resonant inverter with modified phase-shift modulation for high-frequency AC power distribution systems', *IEEE Trans. Ind. Electron.*, 2007, **54**, (5), pp. 2831–2845

16 Ahmed, T., Ogura, K., Chandhaket, S., *et al.*: 'Asymmetrical duty cycle controlled edge resonant soft switching high frequency inverter for consumer electromagnetic induction fluid heater'. AUTOMATIKA 44, 2003, pp. 21–26

17 Burdío, J.M., Barragán, L.A., Monterde, F., *et al.*: 'Asymmetrical voltage-cancellation control for full-bridge series resonant inverters', *IEEE Trans. Power Electron.*, 2004, **19**, (2), pp. 461–469

18 Fujita, H., Akagi, H.: 'Pulse-density-modulated power control of a 4 kW, 450 kHz voltage-source inverter for induction melting applications', *IEEE Trans. Ind. Appl.*, 1996, **32**, (2), pp. 279–286

19 Esteve, V., Sanchis-Kilders, E., Jordan, J.: 'Improving the efficiency of IGBT series-resonant inverters using pulse density modulation', *IEEE Trans. Ind. Electron.*, 2011, **58**, (3), pp. 979–987

20 Park, N.J., Lee, D.Y., Hyun, D.S., *et al.*: 'A power-control scheme with constant switching frequency in class-D inverter for induction-heating jar application', *IEEE Trans. Ind. Electron.*, 2007, **23**, (3), pp. 1252–1260

21 Forest, F., Laboure, E., Costa, F., *et al.*: 'Principle of a multi-load/single converter system for low power induction heating', *IEEE Trans. Power Electron.*, 2000, **15**, (2), pp. 223–230

22 Burdio, J.M., Monterde, F., Garcia, J.R., *et al.*: 'A two-output series-resonant inverter for induction-heating cooking appliances', *IEEE Trans. Power Electron.*, 2005, **20**, (4), pp. 815–822

23 Forest, F., Faucher, S., Gaspard, J.Y., *et al.*: 'Frequency-synchronized resonant converters for the supply of multi-winding coils induction cooking appliances', *IEEE Trans. Ind. Electron.*, 2007, **54**, (1), pp. 441–452

24 Zenitani, S., Okamoto, M., Hiraki, V., *et al.*: 'A charge boost type multi output full-bridge high frequency soft switching inverter for IH cooking appliance'. 14th Int. Power Electronics and Motion Control Conf. (EPE-PEMC), 2010, pp. T2-127–T2-133

25 Saoudi, M., Puyal, D., Anton, D., *et al.*: 'Domestic induction cooking with a new loads multiplexing topology using mechanical switches'. IEEE Int. Symp. on Industrial Electronics (ISIE), 2011, pp. 233–238

26 Lucia, O., Carretero, C., Burdio, J.M., *et al.*: 'Multiple-output resonant matrix converter for multiple induction heaters', *IEEE Trans. Ind. Appl.*, 2012, **48**, (4), pp. 1387–1396

27 Lucia, O., Burdio, J.M., Barragan, A., *et al.*: 'Series resonant multi-inverter with discontinuous-mode control for improved light-load operation', *IEEE Trans. Ind. Electron.*, 2011, **58**, (11), pp. 5163–5171