An SVPWM Scheme for the Suppression of Zero-Sequence Current in a Four-Level Open-End Winding Induction Motor Drive With Nested Rectifier–Inverter

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***Abstract*—A four-level open-end winding induction motor (OEWIM) drive is known to suffer from two perennial problems. One is the problem of zero-sequence current in the motor phases, which is caused by the existence of zero-sequence voltage in them. The other is the overcharging of the dc-link capacitor of the inverter operated with lower dc-link voltage by its counterpart operated with a higher dc-link voltage. This paper investigates the applicability of a special variant of space vector pulse width modulation (SVPWM) scheme for a recently proposed power circuit configuration, in which a rectifier–inverter combination is nested within the conventional two-level inverter configuration to achieve four-level inversion. This PWM scheme is named as the sample-averaged zero-sequence elimination (SAZE) SVPWM scheme, wherein the zero sequence voltage is suppressed in each sampling time period in the average sense. Both of the aforementioned problems encountered in this drive are successfully overcome for this power circuit configuration by resorting to the proposed SVPWM strategy.**

***Index Terms*—Four-level inversion, open-end winding induction motor (OEWIM), overcharging phenomenon, suppression of zero-sequence current.**

I. Introduction

CONTEMPORARY researchers have envisaged several topologies and the associated pulse-width modulation (PWM) techniques for multilevel inverters (MLIs). The repertoire of power circuit configurations for multilevel inversion is principally categorized as neutral point clamped (NPC), flying capacitor (FC), and cascaded H-bridge (CHB) types [1], [2]. Although each of these circuit configurations is more than two decades old, research is still being carried out to improvise them. The recent work pertinent to NPC configuration is reported in [3]–[7], while [8]–[10] describe the advancements in the FC and HB topologies.

Compared to these power circuit configurations, the open-end winding induction motor (OEWIM) drive, which has extensively been investigated in the recent past [11]–[25], possesses the following advantages.

It uses the easy-to-make and well proven two-level voltage source inverter (VSI) as a building block. It is, therefore, easy to engineer them.

1) The dc-link capacitors in NPC MLIs carry load current, while those in two-level inverters carry ripple current. Hence, the OEWIM drive does not suffer from the problems such as neutral point instability as in NPC MLIs, the initialization, and distribution of capacitor voltages pertinent to the FC MLIs.
2) It does not need the fast recovery diodes (which are often rated conservatively) as in the case of NPC MLIs and in general needs fewer dc power supplies compared to the CHB configuration.

On the negative side, an OEWIM drive needs six cables, restricting its applicability, where the motor is situated remotely to the inverter. It also suffers from the problem of zero-sequence current, if the constituent dc input voltage sources are not electrically isolated. The zero-sequence current is harmful to the motor, as this current does not participate in the process of electro-mechanical energy conversion, but heats up the motor windings. It is also deleterious to the power semiconductor switching devices and calls for a conservative rating of them in terms of the peak current handling capability. It should be noted that the cause for the zero-sequence current is the zero-sequence voltage of the motor phases, which stems from the fact that the motor phase voltages in an OEWIM drive do not add to zero. To worsen the matter, the zero-sequence current is limited by the zero-sequence impedance, which in general is small, owing to the fact that it is determined by the leakage inductance of the motor (which in general is quite small, compared to the magnetizing inductance of the motor).

In literature, several circuit topologies and PWM techniques have been reported for OEWIM drives and their derivatives for more than three levels. However, engineering systems demand that MLI systems be simple to manufacture, operate, and maintain. It has also been observed that, beyond four-level systems,

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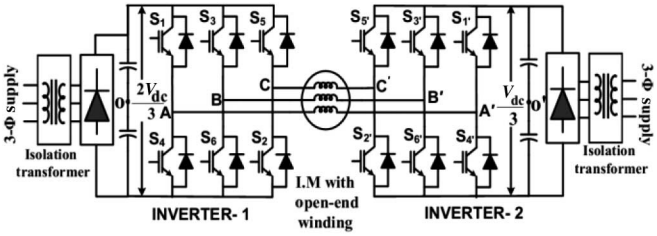

Fig. 1. Dual two-level inverter fed open-end winding Topology with unequal dc-link voltages.

TABLE I
SWITCHING STATES AND CORRESPONDING ZERO-SEQUENCE VOLTAGES OF INDIVIDUAL INVERTERS

State*	Pole voltages			Zero-sequence voltage	
	v_{AO} /$v_{A'O}$	v_{BO} / $v_{B'O}$	v_{CO} / $v_{C'O}$	Inverter-1	Inverter-2
1 & 1'	+	–	–	$-\frac{2V_{dc}}{9\sqrt{3}}$	$-\frac{2V_{dc}}{18\sqrt{3}}$
3 &3'	–	+	–		
5 & 5'	–	–	+		
2 & 2'	+	+	–	$+\frac{2V_{dc}}{9\sqrt{3}}$	$+\frac{2V_{dc}}{18\sqrt{3}}$
4 & 4'	–	+	+		
6 & 6'	+	–	+		
7 & 7'	+	+	+	$+\frac{2V_{dc}}{3\sqrt{3}}$	$+\frac{V_{dc}}{3\sqrt{3}}$
8 & 8'	–	–	–	$-\frac{2V_{dc}}{3\sqrt{3}}$	$-\frac{V_{dc}}{3\sqrt{3}}$

* The states of inverter-1 and inverter-2 are distinguished by the apostrophe.

the *principle of diminishing returns* sets in quickly [20]. The motivation to improvise the existing four-level OEWIM drive springs from this consideration.

The power circuit configuration to derive four-level inversion with OEWIM has been presented in [21]. This circuit employs two inverters with dc-link voltages in the ratio of 2:1, and is shown in Fig. 1.

Table I summarizes the switching states of both inverters. The signs "+" and "−" indicate the turn-ON of the top and bottom switches, respectively, pertaining to a given phase leg.

However, this power circuit is plagued with the problem of overcharging of the capacitor of the inverter operating with a lower dc-link voltage (inverter-2, Fig. 1). Fig. 2(a) shows the mechanism for such an overcharging. When both of the inverters are switched with the voltage space vector $(+\,-\,-)$, the dc-link capacitor of inverter-1 is directly connected to that of inverter-2 and overcharge it [22]. Such an overcharging disturbs the ratio of the respective dc-link voltages of the individual inverters (which is 2:1). The left trace of Fig. 2(b) shows the simulated study of the overcharging phenomenon associated with inverter-2 (Fig. 1), which is operated with lower dc-link voltage. Fig. 2(c) shows an experimental result, which confirms this possibility. This disturbance could profoundly distort the motor phase voltages. Fig. 2(b) and (c) presents the simulation and experimental results, which clearly show this undesirable tendency.

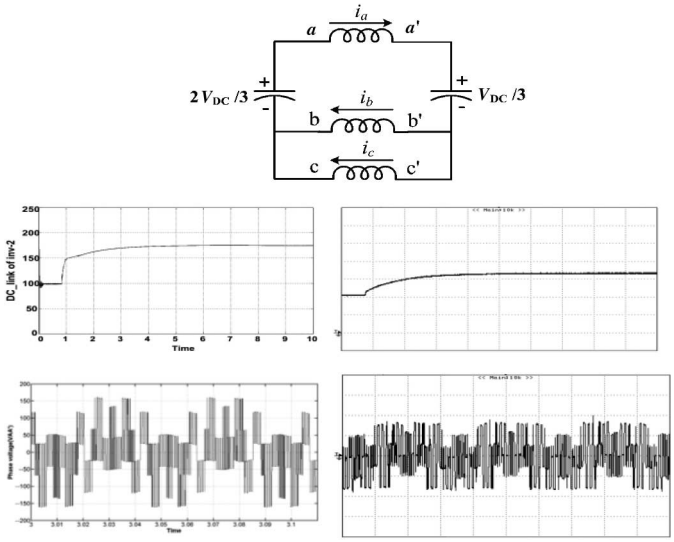

Fig. 2. (a) Direction of charging currents when both of the inverters are switched with the vector $(+\,-\,-)$. (b) Simulated and dc-link voltage of inverter-2 (left) and experimentally obtained dc-link voltage of inverter-2, scale: *X*-axis: 5 s/div; *Y*-axis: 50 V/div. (c) Simulated result of the actual motor phase voltage (left) experimentally obtained result of the actual motor phase voltage (right), scale: *X*-axis: 10 ms/div (for both); *Y*-axis: 50 V/div (left) 100 V/div (right).

II. A FOUR-LEVEL DUAL-INVERTER-FED OEWIM DRIVE WITH A NESTED RECTIFIER–INVERTER

This paper employs a recently proposed power circuit configuration [23], in which a rectifier–inverter combination is nested within the conventional two-level inverter configuration (Fig. 3). It is shown in [23] that this configuration avoids the overcharging of the dc-link capacitor corresponding to the inverter operating with the lower voltage. Fig. 4 shows the motor phase winding connections across the dc-link capacitors for the switching combination, when *both* inverters are switched with the voltage vector $(+\,-\,-)$. This is the situation, which is known to cause the overcharging of the capacitor of inverter-2 in the power circuit shown in Fig. 1 (as described in the previous section). It may be noted that, unlike the situation of the previous circuit (Fig. 1), this circuit successfully avoids a direct connection of the dc-link capacitors through motor phases, when troublesome switching combinations such as $11'$ are deployed.

It has been shown that, this power circuit requires dc-link voltages given by $(4V_{dc}/3\sqrt{3})$ and $(2V_{dc}/3\sqrt{3})$ for the individual inverters, which are higher by a factor of $(2/\sqrt{3})$ compared to the circuit shown in Fig. 1 [23]. However, it is possible to derive a reference voltage space vector of 1.0 p.u. with a total dc-link voltage of 0.77 $(4/3\sqrt{3})$ p.u. with this power circuit configuration.

It may be noted that with the power circuit configuration, shown in Fig. 3, each motor phase is directly connected across an isolated dc power supply as shown in Fig. 4. Thus, a direct confrontation of unequally charged dc-link capacitors of the constituent inverters is avoided unlike the previously proposed circuit (Fig. 1). In this way, the proposed power circuit configuration (Fig. 3) successfully achieves the prevention of overcharging of the dc-link capacitor of inverter-2.

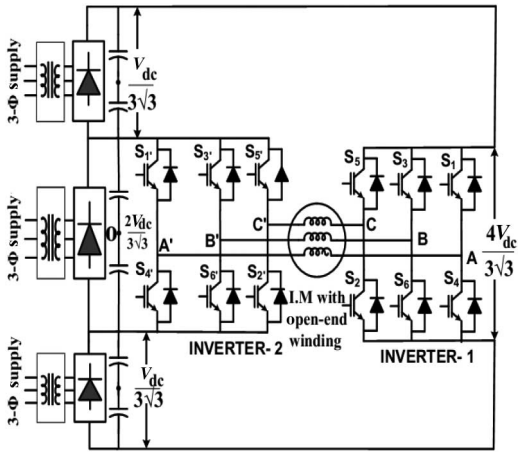

Fig. 3. Nested rectifier–inverter-fed four-level dual-inverter OEWIM drive.

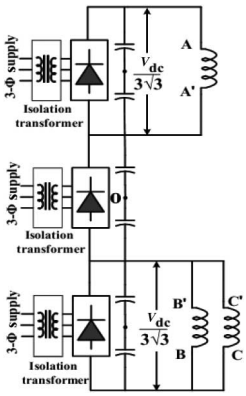

Fig. 4. Connection of motor phases to the dc-link capacitors when both inverters are switched with vector $(+--)$.

III. Suppression of Zero-Sequence Current for the Proposed Four-Level OEWIM Drive

As mentioned earlier, the four-level OEWIM drive shown in Fig. 1 is plagued with two problems: 1) the problem of overcharging of the dc-link capacitor of the inverter operated with lower dc-link by its counterpart operated with higher dc-link voltage and 2) the problem of zero-sequence current, which is caused by the existence of zero-sequence voltage. It has already been explained as to how the problem of overcharging is avoided by the proposed power circuit.

The best proposition to synthesize the reference voltage space vector in any MLI system, using the principles of space vector PWM (SVPWM), is to switch the vector combinations situated at the nearest vertices to it. Fig. 5 shows the space vector diagram corresponding to the power circuit shown in Fig. 4.

In this paper, it is shown that the sample-averaged zero-sequence elimination (SAZE) SVPWM technique, which was originally developed for the three-level OEWIM drive [25], is capable of suppressing the zero-sequence voltage in the case of the proposed four-level OEWIM drive as well with certain refinements. The SAZE SVPWM technique views the dual-inverter system as a *single entity* and suppresses the

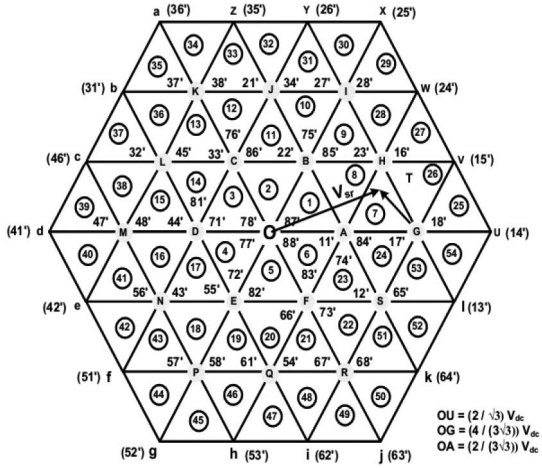

Fig. 5. Resultant space-vector combinations of the dual-inverter scheme.

zero-sequence voltages to zero, in the average sense, in every sampling time period [25].

The symbols v_{AO}, v_{BO}, and v_{CO} denote the three-phase pole voltages of inverter-1, whereas the symbols $v_{A'O}$, $v_{B'O}$, and $v_{C'O}$ denote the same for inverter-2 (Fig. 3). The actual motor phase voltages are $v_{AA'}$, $v_{BB'}$, and $v_{CC'}$ (Fig. 3). The motor phase voltages are obtained by taking the difference of the sets of pole voltages (e.g., $v_{AA'} = v_{AO} - v_{A'O}$).

Let it be assumed that inverter-1 and inverter-2 are switched with states 5 and 6′, i.e., $(--+)$, $(+-+)$ respectively.

The pole voltages of inverter-1 for the switching state of *5* $(--+)$ are given by (Fig. 3)

$$v_{ao} = v_{bo} = -K_1 \;\; ; v_{co} = K_1, \;\; \text{where } K_1 = 2V_{\text{dc}}/3\sqrt{3}. \tag{1}$$

Similarly, the pole voltages for inverter-2 for the switching state of $6(+-+)$ are given by

$$v_{a'o} = v_{c'o} = K_2; \;\; v_{b'o} = -K_2, \;\; \text{where } K_2 = V_{\text{dc}}/3\sqrt{3}. \tag{2}$$

The motor phase voltages $v_{aa'}$, $v_{bb'}$, and $v_{cc'}$ are given by the difference of respective pole voltages as

$$\begin{aligned} v_{aa'} &= v_{ao} - v_{a'o} = -V_{\text{dc}}/\sqrt{3} \\ v_{bb'} &= v_{bo} - v_{b'o} = -V_{\text{dc}}/3\sqrt{3} \\ v_{cc'} &= v_{co} - v_{c'o} = V_{\text{dc}}/3\sqrt{3}. \end{aligned} \tag{3}$$

The space vector corresponding to the above set of motor phase voltages is defined as

$$V_{\text{S}} = v_{aa'} + v_{bb'} \exp(-2\pi/3) + v_{cc'} \exp(2\pi/3). \tag{4}$$

From (3) and (4), one obtains

$$\begin{aligned} V_{\text{S}} = &\left(-V_{\text{dc}}/\sqrt{3}\right) + \left(-V_{\text{dc}}/3\sqrt{3}\right) \exp(-2\pi/3) \\ &+ \left(V_{\text{dc}}/3\sqrt{3}\right) \exp(2\pi/3). \end{aligned} \tag{5}$$

Simplification of (5) gives

$$V_{\text{S}} = \left(-V_{\text{dc}}/\sqrt{3}\right) - j\,(V_{\text{dc}}/3) = (2V_{\text{dc}}/3)\angle(7\pi/6). \tag{6}$$

From (6), it is evident that the space vector produced by the dual-inverter system for the switching vector combination $56'$ is given by the vector ***ON*** (Fig. 5).

As each inverter assumes 8 states *independently* of the other, the total number of state combinations deliverable by the dual-inverter system is 64. The space vectors obtained by the rest of the 63 combinations may be evaluated using the procedure outlined above. Fig. 5 pictorially depicts the positions of the space vector combinations arising out of the dual-inverter system.

The zero-sequence voltage corresponding to the motor phase voltages $v_{AA'}$, $v_{BB'}$, and $v_{CC'}$is defined as

$$V_{\text{zs}} = (1/3) \quad [v_{AA'} + v_{BB'} + v_{CC'}]. \tag{7}$$

It is easy to see that the zero-sequence voltage in the motor phase voltages is equal to the difference of the zero-sequence voltages of individual inverters V_{zs1} and V_{zs2}, which are individual average of pole voltages of respective inverters. Table I summarizes the zero-sequence voltages of individual inverters for all the 8 switching states of individual inverters.

A model calculation of the zero-sequence voltage corresponding to the switching combination $18'$ is shown below.

From Table I, the zero-sequence voltages corresponding to the switching states-1 $(+\,-\,-)$ for inverter-1 and $8'$ $(-\,-\,-)$ for inverter-2 are given by

$$V_{\text{zs1}} = -\frac{2V_{\text{dc}}}{9\sqrt{3}} \text{ and } V_{\text{zs2}} = -\frac{V_{\text{dc}}}{3\sqrt{3}}.$$

Hence,

$$V_{\text{zs}}(18') = V_{\text{zs1}} - V_{\text{zs2}} = -\frac{2V_{\text{dc}}}{9\sqrt{3}} - \left(-\frac{V_{\text{dc}}}{3\sqrt{3}}\right) = \left(\frac{V_{\text{dc}}}{9\sqrt{3}}\right).$$

As each inverter of Fig. 3 can assume 8 states independently of the other, a total of 64 state combinations emanate out of the dual-inverter scheme. Adopting the procedure outlined above, the zero-sequence voltages corresponding to all of these combinations can be computed in a similar manner.

For the dual-inverter scheme, it is desirable to keep one inverter clamped, while the other is switched. Besides achieving a reduced switching power loss, such a switching would achieve the switching of the closest vertices situated to the tip of the reference vector, reducing the switching ripple of the output voltage of the inverter.

For example, when the sample is situated in sector-26 (Fig. 5), inverter-1 should be clamped to sate-1 $(+\,-\,-)$, while inverter-2 should be switched through the switching states: $8'$ $(-\,-\,-)$, $5'(-\,-\,+)$, $6'(+\,-\,+)$, and $7'(+\,+\,+)$ resulting in the sequence $18' - 15' - 16' - 17'$.

With the conventional *center spaced* SVPWM, the vector combination $18'$ and $17'$ are switched for an equal duration of $T_0/2$, where T_0 is the time duration for which the zero-vector combination is switched. This is achieved by using an offset time [24]

$$T_{\text{offset}} = T_0/2 - T_{\min}. \tag{8}$$

It can be shown that the zero-sequence voltage corresponding to the switching combinations $18' - 15' - 16' - 17'$, respectively, are $\left(V_{\text{dc}}/9\sqrt{3}\right)$, $\left(-V_{\text{dc}}/9\sqrt{3}\right)$, $\left(-V_{\text{dc}}/3\sqrt{3}\right)$, and $\left(-5V_{\text{dc}}/9\sqrt{3}\right)$. These vector combinations are switched for the respective time periods of $T_0/2$, T_1, T_2, and $T_0/2$.

Resorting to this switching scheme, the sampled average of the zero-sequence voltage is given by (9), shown at the bottom of the page.

Thus, it is evident that the averaged zero-sequence voltage over a sampling time interval *will not be equal* to zero with the centre spaced SVPWM technique (unless $T_2 - T_1 = 2T_s$, which is impossible, as $T_1 + T_2 + T_0 = T_s$). This nonzero-averaged zero-sequence voltage would cause a significant zero-sequence current through the motor phases making the electrical isolation mandatory to suppress the zero sequence current (Fig. 1).

IV. SAZE SVPWM Strategy

The principle of the SAZE PWM scheme is explained with the help of Fig. 6. The space vector diagram of the four-level OEWIM drive presented in Fig. 5 is divided into seven regions as shown in Fig. 6. Of these, regions 1, 3, and 5 are colored in solid grey, while regions 2, 4, and 6 are shown hatched. Region-7 is constituted by the sectors of the innermost hexagon and interspatial sectors of regions 1 and 2 shown in white color.

Let it be assumed that the sample (the tip of the reference vector ***OT***) to be synthesized is situated in the sector GVH (sector numbered 26 in Fig. 5). The vector combinations located at the vertices G, V, and H are switched, respectively, for the time periods T_0, T_1, and T_2 to produce the reference voltage vector ***OT*** in the average sense, using the principles of SVPWM.

Of the three switching time periods— T_0, T_1, and T_2—for which the vertices G, V, and H are switched, respectively, the sum of T_1 and T_2 is termed as *effective time period* and is sandwiched between the two equal halves of the time period T_0 (termed as the *null time period* in the parlance of space vector modulation). In the case of a conventional (three-wired) induction motor drive, there is no power flow between the dc and ac sides of the inverter when a null vector is switched. However, in the case of OEWIM drives, the so-called *null vector combinations* (such as $18'$) also facilitate power flow between the dc and ac sides of the dual-inverter system, even though the same terminology is used.

It was shown in the earlier section that, with the conventional centre-spaced SVPWM technique, the sample-averaged zero-sequence voltage will not be equal to zero, which would in

$$V_{\text{zs}}^{\text{SA}} \quad (\text{centre spaced}) = \frac{\left[\left(V_{\text{dc}}/9\sqrt{3}\right)(T_0/2) + \left(-V_{\text{dc}}/9\sqrt{3}\right)(T_2) + \left(-V_{\text{dc}}/3\sqrt{3}\right)(T_1) + \left(-5\,V_{\text{dc}}/9\sqrt{3}\right)(T_0/2)\right]}{T_s}$$
$$= -\frac{2V_{\text{dc}}}{9\sqrt{3}} + \left(\frac{V_{\text{dc}}}{9\sqrt{3}}\right)\left(\frac{T_2 - T_1}{T_s}\right) \tag{9}$$

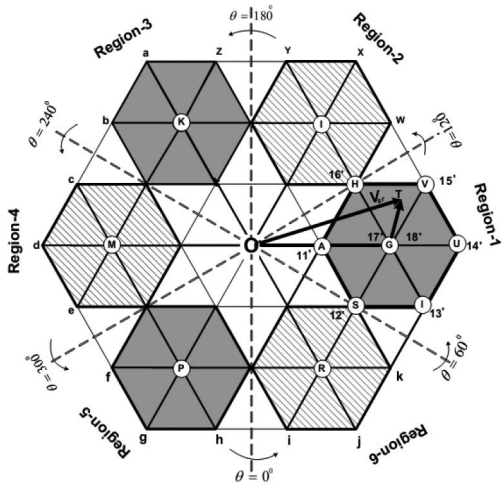

Fig. 6. Principle of SAZE-SVPWM strategy.

turn manifest as the zero-sequence current in the motor-phase windings.

The central theme of the SAZE PWM strategy is based on the observation that, if the effective time period block constituted by the total switching time periods of the combinations $15'$ and $16'$ (for the time duration of T_1 and T_2, respectively), is *strategically placed* within a given sampling time period T_S, it is possible to force the average value of the zero-sequence voltage, over a sampling time period (T_S) to a value of zero. This assertion is based on the following observations.

1) Placement of the zero-vector periods offers a degree of freedom in realizing the reference vector.
2) Pivotal vertices (such as G) exhibit redundant switching vector combinations (such as $18'$ and $17'$, Fig. 6).
3) The inverter state combinations corresponding to the same space vector location exhibit different zero-sequence voltages (Fig. 5 and Table I).

The generalized time offset to place the effective time block anywhere in the sampling time period is given by

$$T_{\text{offset, gen}} = xT_0 - T_{\min}, \qquad 0 \le x \le 1. \tag{10}$$

From (8), it is obvious that $x = 0.5$ for centre-spaced SVM. One may find the offset time required to force the sample averaged zero-sequence voltage, by equating the zero-sequence volt-seconds to a value of zero [25].

In the SAZE SVPWM strategy, the time durations for which these combinations switched are given by $(1-x)T_0$, T_2, T_1, and xT_0, respectively (instead of $T_0/2$, T_1, T_2, and $T_0/2$ as in the case of the centre-spaced SVPWM scheme). Thus, to force the sample-averaged zero-sequence voltage to zero

$$V_{zs}^{SA} = \frac{1}{T_s}\left[\left(\frac{V_{dc}}{9\sqrt{3}}\right)(1-x)T_0 + \left(-\frac{V_{dc}}{9\sqrt{3}}\right)T_2 + \left(-\frac{V_{dc}}{3\sqrt{3}}\right)T_1 + \left(-\frac{V_{dc}}{9\sqrt{3}}\right)(xT_0)\right] = 0. \tag{11}$$

The above expression leads to (see the Appendix)

$$T_{\text{offset}}(\text{Regions } 1,\ 3,\ 5) = \frac{T_s}{6}. \tag{12}$$

Thus, by simply affecting the offset-time given by (12), one would succeed in forcing the average value of the zero-sequence voltage over a sampling time interval to zero *for any sample situated in Region-1*. Resorting to this method, it can be proved that this value of offset-time period is applicable for any sample, which is situated in *Region-3* and *Region-5* (Fig. 6) as well.

By adopting a similar procedure, it can be shown that the offset time to force the average value of the zero-sequence voltage to zero, over a sampling time interval in the Regions 2, 4, and 6 (e.g., Sector-29, Figs. 5 and 6) is given by:

$$T_{\text{offset}} \quad (\text{Regions } 2,\ 4,\ 6) = \frac{5T_s}{6}. \tag{13}$$

It can also be proved that the corresponding expression for the sectors, of Region-7, which includes the inner hexagon (e.g., sector-1, Figs. 5 and 6) and the interspatial regions between Regions-1 and 2 (e.g., sector-27, Figs. 5 and 6) is given by

$$T_{\text{offset}}(\text{Region } 7) = \frac{T_s}{2}. \tag{14}$$

Equation (14) is interesting because of two reasons.

1) Intuitively, one may expect that the offset time for the interspatial sectors (such as sector-27) to be the average of offsets of Regions 1 and 2, as the interspatial regions are situated in the midst of Regions 1 and 2

$$T_{\text{offset}}(\text{Region } 7) = \frac{T_{\text{offset}}(\text{Regions } 1,\ 3,\ 5) + T_{\text{offset}}(\text{Regions } 2,\ 4,\ 6)}{2} = \frac{1}{2}\left(\frac{T_S}{6} + \frac{5T_S}{6}\right) = \frac{T_S}{2}. \tag{15}$$

2) If one intends to eliminate the zero-sequence component in motor phase voltages in the core hexagon (sectors 1–6, Fig. 5), the instantaneous phase reference voltages for the *individual inverters* should be purely sinusoidal. When the sample is situated within the core hexagon (e.g., sector-1, Fig. 5), *both inverters must be switched* to eliminate the zero-sequence current. In sector-1, the dual-inverter system should be switched through the switching combinations: $88' - 11' - 22' - 77'$. Each inverter is switched with an offset time given by (14). It was shown in [24] that a time-offset given by (14) results in the implementation of sinusoidal PWM technique from an algorithm, which is originally developed to implement the SVPWM technique. This further reinforces the fact that the sinusoidal modulation is a special case of a more generalized SVPWM technique.

V. Simulation and Experimental Results

Simulation studies are carried out, using MATLAB, to verify the applicability of the SAZE-SVPWM to the power circuit configuration shown in Fig. 3. A synchronized SVPWM scheme is used, wherein 42 samples are used per one cycle

of the fundamental component irrespective of the modulation index. The depth of modulation is quantified in terms of modulation index, which is defined as

$$m_a = \frac{|V_{sr}|}{V_{\text{dc}}} \tag{16}$$

where $|V_{sr}|$ is the length of the space vector (***OT*** , Fig. 6) and V_{dc} is the total dc-link voltage (***OU*** , Fig. 6).

Fig. 7(a) shows the motor phase voltage and current, when the dual-inverter system is operated with a modulation index of 0.4, with center-spaced SVPWM.

When the modulation index is 0.4, the tip of the reference vector traverses a circular path in such a way that the vertices A, B, C, D, E, and F provide the biasing vectors. When the tip of the reference vector ***OT*** (Figs. 5 and 6) is situated in the sector 7, inverter-1 can be clamped to the state -1 (i.e. $+--$) as the vector combinations $17'-16'-11'-18'$ are switched. However, in sector-8, the vertices **A**, **H**, and **B** are to be switched. A glance at the switching combinations available at these vertices reveals that it is impossible to clamp inverter-1 at a given state. The combinations switched (in sector-8) are: **A** $(11')$–**H** $(16')$–**B** $(85')$ and back to **A** $(84')$. In other words, inverter-1 is clamped to the state -1 $(+--)$ for the time period of (xT_0+T_1) and state-8 $(---)$ for the time period $[(1-x)T_0+T_2]$. Thus, phase-A of inverter-1 is switched from "+" to "−" half way through the sampling time interval. Furthermore, all the samples situated in sector-8 are switched in this manner and phase-A is switched from the states "+" and "‘ −." This explains as to why some switching is inevitable even for the so-called *clamped inverter*.

The current waveform reveals the presence of a pronounced zero-sequence current, which is constituted by the components of the triplen order. As mentioned earlier, the root cause for the existence of the zero-sequence current in the motor phase current is the zero-sequence voltage present in the motor phase voltage, which is presented in Fig. 7(b). It may be noted that the motor phase voltage contains zero-sequence components (harmonics of triplen order). Particularly, the 3rd and 21st harmonic components are clearly discernible.

Fig. 7(c) shows the experimentally obtained pole-voltages of the individual inverters. It may be noted that inverter-1 is switched with a much lesser frequency compared to inverter-2 as inverter-1 serves as the clamping inverter, while inverter-2 works as the switching inverter. It may also be noted that the magnitude of the pole voltage of inverter-1 is twice compared to that of inverter-2. The left trace of Fig. 7(d) shows the motor phase voltage, which is the difference of the two pole voltages shown in Fig. 7(c). Four voltage levels are clearly identifiable in this waveform indicating that it is a four-level OEWIM drive.

The experimental results confirm that the motor phase voltage and therefore current have a considerable zero-sequence content, when the conventional centre-spaced SVPWM technique is employed to modulate the four-level inverter system shown in Fig. 3. Thus, the motivation to investigate the employability of the SAZE PWM to this circuit is justified.

The simulated and experimental results pertaining to the SAZE SVPWM technique are presented in Fig. 8. Fig. 8(a) shows the motor phase voltage and the current with the SAZE-SVPWM technique. It may be noted that the current does not show the zero-sequence (triplen harmonic) content. It is interesting to note that the normalized harmonic spectrum of the motor phase voltage, shown in Fig. 8(b) shows the presence of the components of the triplen order.

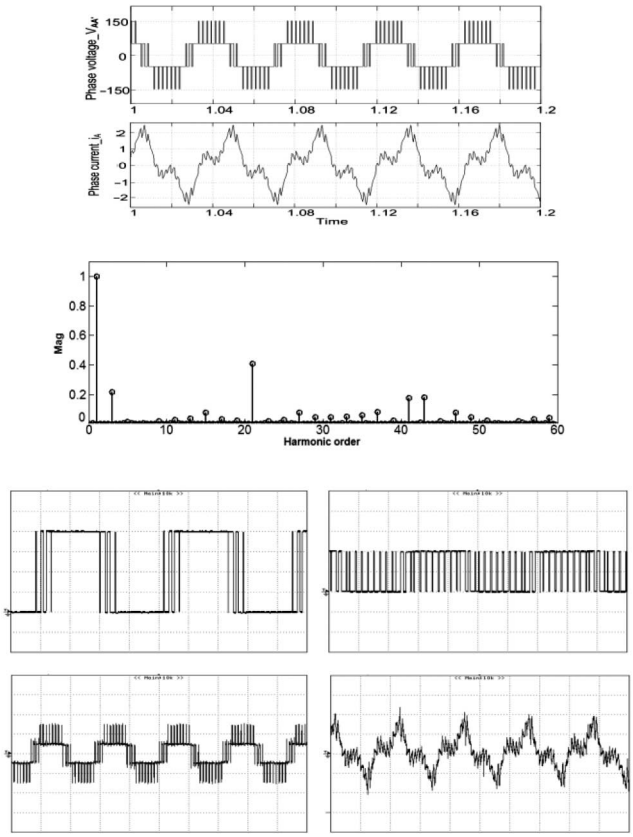

Fig. 7. (a) Simulated results of motor phase voltage and current. (b) Normalized harmonic spectrum of the difference in a-phase pole voltages for center spaced SVM at $m_a = 0.4$. (c) Experimentally obtained result (right) of A-phase pole voltage of inverter-2 for an $m_a = 0.4$, scale: *X*-axis: 10 ms/div; *Y*-axis: 50/div. (d) Experimental motor phase voltage (left) and motor phase current (right) for $m_a = 0.4$ with the center-spaced SVPWM technique (voltage scale: *X*-axis: 20 ms/div; *Y*-axis: 100 V/div and current scale: *X*-axis: 20 ms/div; *Y*-axis: 1 A/div.

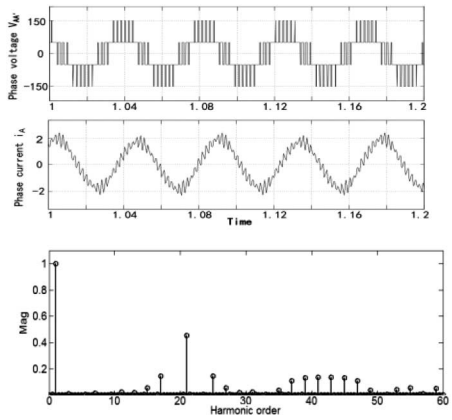

Fig. 8. (a) Simulated motor phase voltage (top) and current (bottom) with the SAZE PWM for $m_a = 0.4$. (b) Normalized harmonic spectrum of the phase voltage with the SAZE PWM for $m_a = 0.4$.

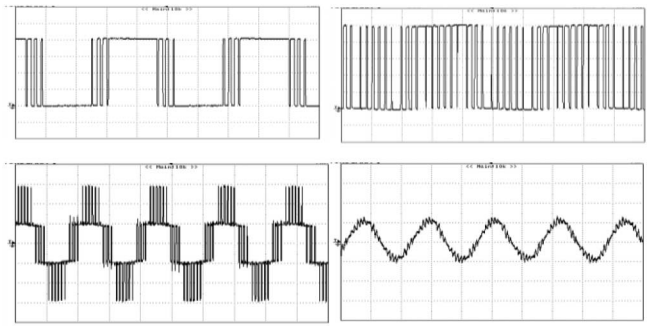

Fig. 9. (a) Experimentally obtained result of pole voltage of inverter-1 (left) and inverter-2 (right) for an $m_a = 0.4$ with the SAZE PWM technique (scale: *X*-axis: 10 ms/div; *Y*-axis: 50 V/div). (b) Experimentally obtained result of motor phase voltage (left) and the no-load motor phase current (right) for an $m_a = 0.4$ with the SAZE PWM technique, scale: *X*-axis: 20 ms/div; *Y*-axis: 50 V/div; and 1 A/div.

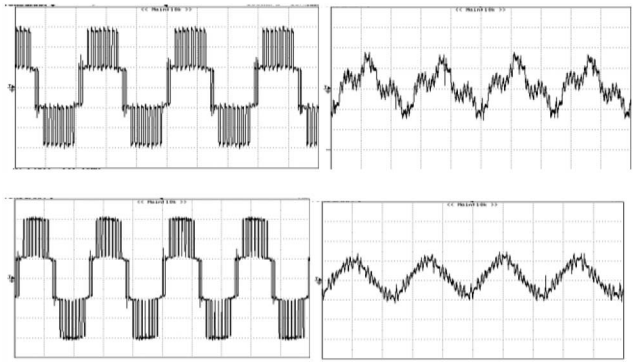

Fig. 10. (a) Experimentally obtained result (right) of motor voltage for an $m_a = 0.7$ with center-spaced PWM, scale: *X*-axis: 20 ms/div; *Y*-axis: 50 V/div and 1 A/div. (b) Experimentally obtained result (right) of motor voltage for an $m_a = 0.7$ with SAZE PWM, scale: *X*-axis: 20 ms/div; *Y*-axis: 50 V/div and 1 A/div.

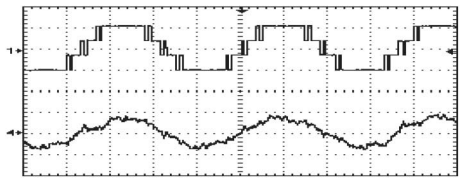

Fig. 11. Experimentally obtained result of motor voltage (top) and motor phase current (bottom) for an $m_a = 0.95$ with SAZE PWM, scale: *X*-axis: 5 ms/div; *Y*-axis: 100 V/div and 1 A/div.

It is, therefore, evident that, even though the instantaneous value of the zero-sequence voltage is not equal to zero, its sampled average is forced to become equal to zero with the SAZE PWM algorithm. As result, the zero-sequence current is dynamically balanced around the average value of zero even though its instantaneous value is nonzero. In other words, the instantaneous (nonzero) value of the zero-sequence current manifests as the ripple in motor phase current. This result proves the effectiveness of the SAZE-SVPWM for the proposed four-level OEWIM drive.

To prove the practical viability of the SAZE SVPWM technique, an OEWIM (5 HP, 1430 RPM, 50 Hz, 400 V line-line) was run with V/Hz control scheme. As in the case of simulation studies, synchronized SVPWM technique was employed with 42 samples per cycle irrespective of the modulation index. The SAZE SVPWM technique is implemented with the dSPACE-1006 platform, with a total dc-link voltage of 200 V.

The experimental results for $m_a = 0.4$ are presented in Fig. 9. From Figs. 8 and 9, it is evident that the pulse pattern of the pole voltages is considerably different with the SAZE PWM technique in comparison to the center-spaced PWM technique. The experimental results are in agreement with the simulation results, proving the experimental viability of the SAZE PWM technique.

Fig. 10 shows the experimental results corresponding to $m_a = 0.7$. In the interest of brevity, only motor phase voltages and currents are shown for the conventional and the SAZE PWM techniques.

The motor phase voltage waveforms resemble each other with both the conventional SVPWM algorithm as well as with the SAZE SVPWM algorithm [Figs. 7(d), 9(b), 10(a), and 10(b)]. However, the readjustment of pulse widths calculated by the SAZE PWM, which is facilitated by the relocation of the effective time period, suppresses the zero sequence current in the average sense. Thus, the applicability of the SAZE PWM to the power circuit shown in Fig. 3 is ascertained.

Similar results are presented for the modulation index of 0.95 in Fig. 11. In this case, the locus of the tip of the reference vector lies mostly outside the hexagon "*uxadgj*" (Fig. 5), barring a few samples around the vicinity of the vertices. In other words, the dual-inverter system is operated in the nonlinear range as the modulation index of 0.866 represents the limit of linear modulation.

The four levels present in the motor phase voltage are clearly distinguishable in this case too. As one might expect, the motor phase current is slightly deviant from a sinusoidal waveform owing to the fact that the dual-inverter system is operated in the nonlinear region.

As mentioned in the earlier section, both inverters should be switched to suppress the zero-sequence current when the tip of the reference vector is confined to the core hexagon "*ABCDEF*." Fig. 12 presents the experimental results corresponding to this condition, wherein $m_a = 0.2$. Fig. 12(a) shows the pole voltages, while the motor phase voltage and the motor phase current are presented in Fig. 12(b). It is evident from Fig. 12(a) that both inverters are switched in this case.

A. DC-Link Stability of the Dual-Inverter System With Nested Rectifier–Inverter

For the dual-inverter system shown in Fig. 1, it has been stated in section-1 that the dc-link voltage of inverter-2 is overcharged by its counterpart of inverter-1 making the dual-inverter system impracticable [Fig. 2(b) and (c)]. However, with the employment of redundant switching combinations available for a vector location, this problem can be solved to a certain extent. For example, by employing redundant switching combinations available at the location *A* ($84'$ and $74'$, Fig. 5) instead of the most natural choice based on switching performance (which is $11'$, Fig. 5), a direct showdown [as shown in Fig. 2(a)], of the respective dc-link capacitors of the inverters can be avoided. However, for some vector locations (such as *H*, Fig. 5), this

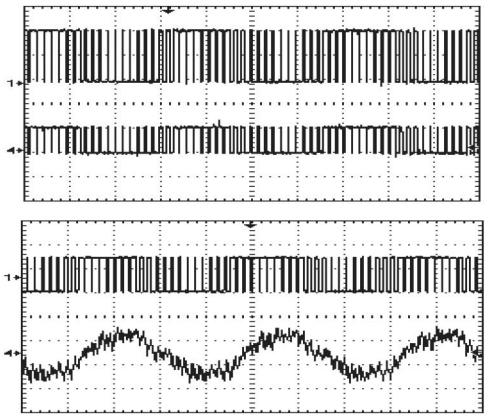

Fig. 12. (a) Pole voltages of inverter-1 (top) and inverter-2 (bottom) for $m_a = 0.2$ with SAZE PWM, scale: *X*-axis: 25 ms/div; *Y*-axis: 100 V/div. (b) Experimentally obtained result of motor voltage (top) and motor phase current (bottom) for an $m_a = 0.2$ with SAZE PWM, scale: *X*-axis: 25 ms/div; *Y*-axis: 100 V/div and 1 A/div.

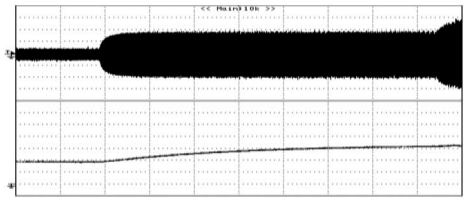

Fig. 13. Motor phase current (top trace) and dc-link voltage (bottom trace) of inverter-2 under loading condition for $m_a = 0.6$. Scale: *X*-axis: 2 s/div; *Y*-axis: 2 A/div (top trace) and 50 V/div (bottom trace).

strategy cannot be adopted owing to the fact that all switching combinations ($16'$ and $23'$ in the case of location *H*) fall in the category mild charging combinations [22]. Owing to this fact, the dc-link capacitor of inverter-2 could still be overcharged as the possibility of such a charging depends not only on the dwell-time of locations such as *H*, but also on the value of the instantaneous load current.

To verify the occurrence of overcharging with this mechanism, the dual-inverter system of Fig. 1 is operated with a modulation index of 0.6, which increases the dwell times of vector locations such as *H*. The top trace of Fig. 13 shows the load current of the dual-inverter system, while the dc-link Capacitor voltage of inverter-2 is presented in the bottom trace. The experimental results reveal that, while the system operates satisfactorily at no-load, the dc-link capacitor of inverter-2 is overcharged under loaded conditions.

To verify if the nested rectifier–inverter power circuit configuration (Fig. 3) also suffers from such a shortcoming, the motor is loaded and the dc-link voltage of inverter-2 is monitored. The upper trace of Fig. 14 shows the motor phase current under loaded condition, when the motor is suddenly loaded to two different values of load current when the modulation index is equal to 0.6. The lower trace of Fig. 14 shows the dc-link voltage of inverter-2. It may be noted that the dc-link voltage is stable and shows the usual phenomenon of voltage regulation, i.e., lowered voltage when the power supply is loaded.

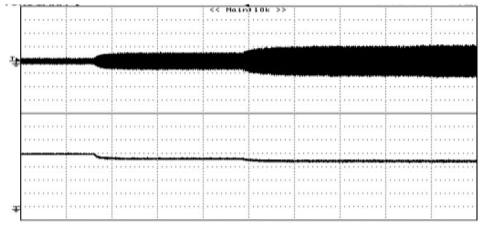

Fig. 14. Motor phase current in loaded condition for $m_a = 0.6$. Scale: *X*-axis:2 s/div; *Y*-axis:5 A/div.

Thus, it is shown that, unlike the power circuit topology described shown Fig. 1, the nested rectifier–inverter-fed four-level OEWIM drive does not suffer from the disadvantage of an overcharged dc-link capacitor of inverter-2 when the motor is loaded. These experimental results convincingly show the effectiveness and the applicability of the SAZE-SVPWM scheme for the nested rectifier–inverter configuration.

VI. Conclusion

In this paper, it is shown that the power circuit configuration reported in the earlier literature for a four-level OEWIM drive suffers from a potential problem; the dc-link capacitor of the dc power supply with lower voltage is overcharged by the high voltage dc power supply. Avoidance of this problem involves the identification of the space vector combinations, which result in such an overcharging and avoid their use.

To avoid this problem, a recently reported power circuit is used in this work. The proposed power circuit uses three dc power supplies. However, the total dc-link voltage needed in this power circuit is only 77% of the total dc-link voltage requirement of the earlier power circuit configuration. With this power circuit topology, all possible space vector combinations arising out of the dual-inverter scheme can be used without resulting in the aforementioned overcharging phenomenon.

The SAZE-SVPWM strategy, which is modified to suit the need of the nested circuit configuration, results in the switching of the nearest space vector combinations. It also ensures an optimized switching performance as the inverter operated with higher dc-link voltage is clamped (providing the vectored offset), while the other inverter switches around this vectored bias. The proposed SAZE SVPWM technique suppresses the zero-sequence voltages to zero, in the average sense, in every sampling time period. The stability of dc-link voltage with this PWM strategy is also verified experimentally and the results are found to be encouraging. It could be interesting to explore the applicability of the SAZE PWM technique for higher number of levels for OEWIM drives and the possibility of developing a rigorous theoretical framework.

Appendix

The zero-sequence voltages corresponding to the vector combinations $18'$, $15'$, $16'$, and $17'$, respectively, are given by $\frac{V_{dc}}{9\sqrt{3}}$, $-\frac{V_{dc}}{9\sqrt{3}}$, $-\frac{V_{dc}}{3\sqrt{3}}$, and $-\frac{V_{dc}}{9\sqrt{3}}$. The time durations for which these combinations switched are given by $(1-x)T_0$, T_2, T_1,

and xT_0, respectively. Thus, to force the sample-averaged zero-sequence voltage to zero

$$V_{\text{ZS,Samp,avg}} = \frac{1}{T_s}\left[\left(\frac{V_{dc}}{9\sqrt{3}}\right)(1-x)T_0 + \left(-\frac{V_{\text{dc}}}{9\sqrt{3}}\right)T_2 + \left(-\frac{V_{\text{dc}}}{3\sqrt{3}}\right)T_1 + \left(-\frac{V_{\text{dc}}}{9\sqrt{3}}\right)(xT_0)\right] = 0. \tag{A.1}$$

From the above equation one obtains: $-\frac{5T_0}{6} + \frac{5xT_0}{6} - \frac{T_2}{2} - \frac{T_1}{6} + \frac{xT_0}{6} = 0$

$$\text{i.e., } xT_0 = \frac{5T_0}{6} + \frac{3T_2 + T_1}{6}. \tag{A.2}$$

The offset time period corresponding to this region is denoted by the symbol T_{offset} (Regions 1, 3, 5).

Thus,

$$T_{\text{offset}-1} = (1-x)T_0 - T_{\min}$$
$$T_{\text{offset}-1} = T_0 - xT_0 - T_{\min}$$

From (A.2)

$$T_{\text{offset}-1} = T_0 - \left[\frac{5T_0}{6} + \frac{3T_2 + T_1}{6}\right] - T_{\min}$$
$$T_{\text{offset}-1} = \frac{T_0 - 3T_2 - T_1 - 6T_{\min}}{6}. \tag{A.3}$$

From the PWM implementation strategy described in [24]

$$\left.\begin{array}{l} T_{\max} = \max(T_{as}, T_{bs}, T_{cs}) \\ T\min = \min(T_{as}, T_{bs}, T_{cs}) \\ T_{\text{mid}} = \text{mid}(T_{as}, T_{bs}, T_{cs}) \\ T1 = T\max - T\text{mid} \\ T2 = T\text{mid} - T\min \\ T\text{eff} = T\max - T\min \\ T0 = Ts - T\text{eff} \\ T\max + T\text{mid} + T\min = 0 \end{array}\right\}. \tag{A.4}$$

Substituting the above in (A.3), one obtains

$$T_{\text{offset}}(\text{Regions } 1,\ 3,\ 5) = \frac{T_0 - 3(T_{\text{mid}} - T_{\min}) - (T_{\max} - T_{\text{mid}}) - 6T_{\min}}{6} \tag{A.5}$$

$\because T_{\max} + T_{\text{mid}} + T_{\min} = 0$ (A.4), it follows that

$$T_{\text{mid}} = -(T_{\max} + T_{\min}). \tag{A.6}$$

Substituting (A.6) into (A.5) and simplifying one gets

$$T_{\text{offset}-1} = \frac{T_0 + T_{\max} - T_{\min}}{6}. \tag{A.7}$$

From (A.4), $T_{\max} - T_{\min} = T_{\text{eff}}$

$$T_{\text{offset}-1} = \frac{T_0 + T_{\text{eff}}}{6}.$$

As $T_0 + T_{\text{eff}} = T_s$ (A.4), one finally obtains

$$T_{\text{offset}-1} = \frac{T_s}{6}. \tag{A.8}$$

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