A New 3-Phase Hybrid Matrix Multilevel Inverter

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***Abstract*—This paper presents a new topology of 3-Phase Hybrid Matrix multilevel inverter with reduced number switches and electrical isolation. Each phase consists of two cascaded units; the first unit is used for level generation whereas the second one doubles the number of levels and provides electrical isolation and step up the voltage to required range. The proposed topology show significance in design, reduced components, simplicity compared to conventional topologies for more than five level productions. Therefore, in this paper, operation and switching control scheme for the proposed topology is presented for five level output. Moreover, the performance of the proposed model is analyzed in MATLAB-SIMULINK environment and their results are presented.**

***Keywords*—Multilevel inverter, Pulse width modulation, Total harmonic distortion (THD),**

I. INTRODUCTION

In present scenario, multilevel inverters getting popularity in modern industries and new renewable sources such as PV/FC power production applications due to advancement in power electronics and the rising energy demands. Also it has added advantages of reduced voltage stress, low EMI and %THD compared to conventional two level inverters. Hence the following conventional topologies such as diode clamped, flying capacitors and cascaded H-bridge structures were investigated [1-3]. Here each topology has its own merit and demerits. Especially in diode clamped inverter and flying capacitors inverters balancing of voltage across capacitors are difficult. Cascaded H-bridge converter overcomes this problem with increased DC sources and switches. Hence, the challenge is going on development of multilevel inverters with reduced number of DC sources and switching devices. Several combinational designs have also emerged by means of cascading the fundamental topologies that they are called hybrid topologies [4-6].But, most of the topologies were developed have increased circuit complexity, size and cost.Recently, several multilevel converter topologies have been developed in [7-14].Some novel topologies of cascaded multilevel inverters using reduced number of switches and gate driver circuits are presented in [7-9].A new cascaded multilevel inverter with sub modules used for dynamic voltage restorer to compensate the voltage sag and swell is given in [10]. A low frequency 3-phase multilevel inverter using three single phase transformer with single DC source operating is presented [14]. Here each sub modules is operated using phase angle control at fundamental frequency to produce the required output voltage level.

Therefore in this paper a new 3- phase Hybrid Matrix multilevel inverter is proposed. In this topology as the number of number of output voltage levels increasing number of switches, DC sources and size will reduce. The proposed topology is also a hybrid one and consists of two units. First unit is used for the level generation and second one used for both positive and negative signal generation. The complete structure and switching operation of the proposed topology is presented in section II. A comparison of proposed topology with conventional topologies is also presented. Further, the simulation results are extensively analyzed in section III.

II. PROPOSED TOPOLOGY

The schematic arrangement of proposed 3-phase hybrid matrix multilevel inverter with reduced switches and electrical isolation is shown in Fig.1. Here each phase module is similar and consists of eight switches. Out of which four is used for the level generation and remaining four switches were used just like a conventional H-bridge inverter for both positive and negative side production. So it consists of two cascading units. One of the most important things considered in each phase that the level production module (unit1) structure which is used similar for matrix converter (shaded portion) and cascaded with a conventional H-bridge inverter (unit2). Hence the level production in each phase is decided from the number of source required and increased arms. Moreover the identification of required number of DC sources and number of arms is most important for level generation. So the calculation of number of DC sources, number of arms and level generation per phase are as follows;

For even number
Number of DC sources = (N-1)/2,
Number of arms per phase=M+1
Number of levels per phase=2N-1
For odd number
Number of DC sources = (N)/2,
Number of arms per phase=M
Number of levels per phase=2N

Where M is the number of DC sources, N is the number of arms. One of the main advantage is here all the arms in each phase have the ability to flow the current in both directions. But during the operation external arms in each phase has to block the voltages only in one direction and remaining arms have to block voltage in both the directions. Hence external arms in each phase contain one IGBT (switch) and remaining arms contains two IGBT transistors connected in series by their emitter as shown in the Fig.1.

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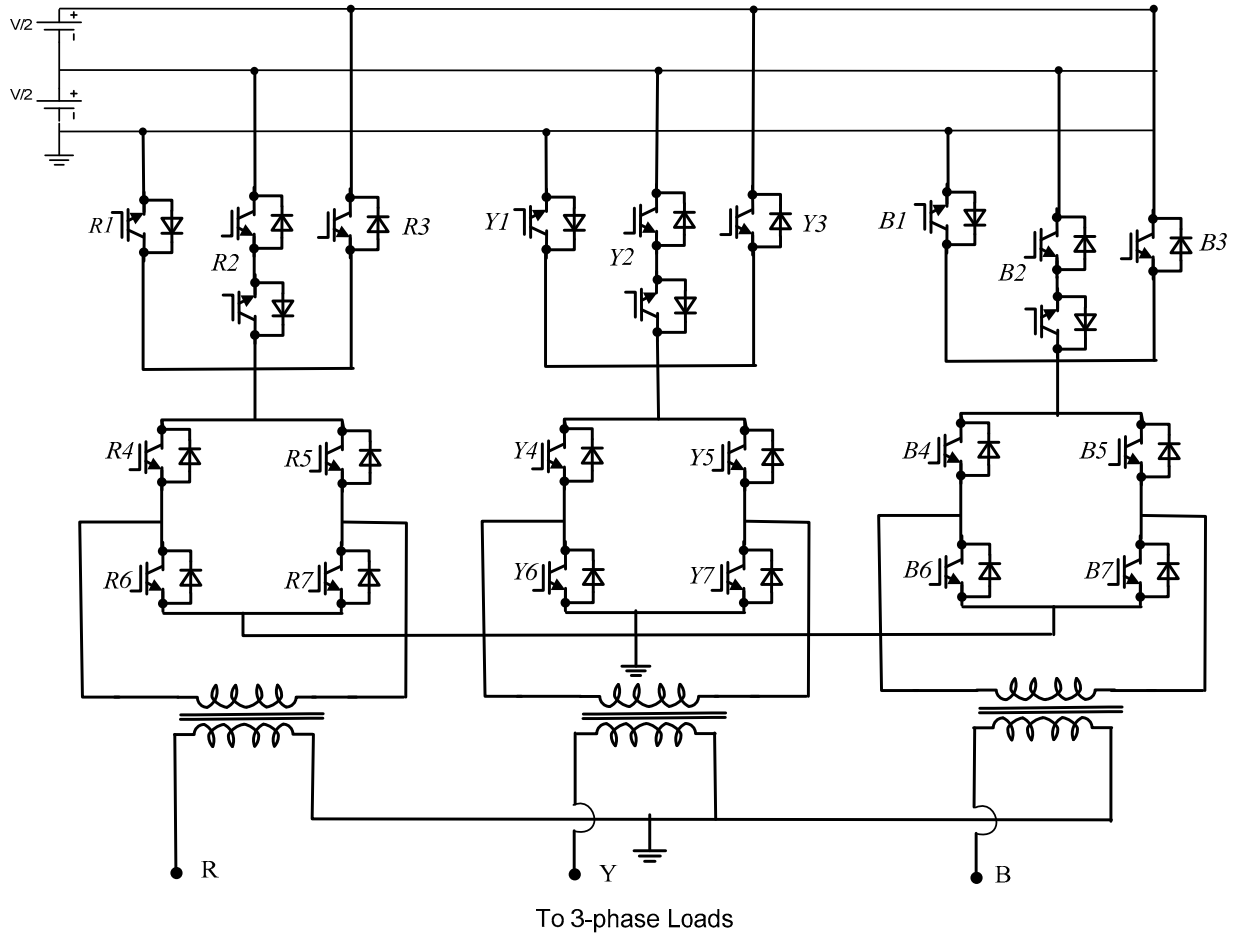

Fig. 1. Proposed 3-phase five level inverter

Here switches in the middle arm(R2,Y2,B2) needs to have the maximum blocking voltage capability of V/2 whereas for remaining switches it is V. Total number of switches in first unit =3(N-1) when n is odd. Total number of switches required for first unit = 3(N-2) when n is even, this is achieved just by subtracting the switches required for zero level. Moreover in each phase each arm corresponds to different voltage levels, as number of arms increasing, number of voltage levels increases. When external arms are turn on we get zero and highest voltage levels, remaining arms will give the intermediate levels. In order to avoid the internal short circuit across DC sources, no two arms switch on at the same time. Finally all the arms in each phase connected at one common point as shown in the Fig.1. Further it is cascaded to unit2 which contains conventional H-bridge units one for each phase and 3-phase transformer. In R-phase the switches R4&R7 must be turn to get the positive voltage levels. Similarly by turning on switches R5&R7 the negative voltage levels can be generated. Above explanation can be extended to other two phases Y and B with 120 degree phase shift apart each phases. Output of H-bridge units given to the load by using 3-phase transformer which provides electrical isolation and also boosting(step up) if required.

In second unit number of switches is constant irrespective of number of voltage levels.Hence for proposed topology total number of switches required for N level inverter is equal to 3N+9,if n is odd and 3N+6,if n is even. Complete operation of the proposed topology can be understood from the following Table I. The switching sequence and the corresponding voltage level production are given for R phase only for better understanding. This can be extended to Y and B phases, only difference is their phase difference.

TABLE I. SWITCHING STATES (FOR R-PHASE)

R1	R2	R3	R4	R5	R6	R7	Voltage levels
on	off	off	on	off	off	on	0
off	on	off	on	off	off	on	+V/2
off	off	on	on	off	off	on	+V
on	off	off	off	on	on	off	0
off	on	off	off	on	on	off	-V/2
off	off	on	off	on	on	off	-V

Moreover, the comparison of the proposed topology along with conventional topologies is given in Table II. It is observed that the total number of switches and driver circuits required for the all the topologies are remains is almost remains equal up to five level operations. But there is a difference six switches is exit for more than five level operation compared to conventional topologies. Hence the proposed topology reduces the complexity in circuit and control. In addition, this topology doesn't require any capacitors, clamping diodes and number of DC sources requires is one third of number of DC sources compared to symmetric cascaded H-bridge circuit.

TABLE II. COMPARISONBETWEEN PROPOSED TOPOLOGY AND CONVENTIONAL TOPOLOGIESIN TERMS OF SWITCHES

Diode Clamped	Flying Capacitor	Cascaded H-bridge	Proposed Topology	Voltage levels
24	24	24	24	5
36	36	36	30	7
48	48	48	36	9
60	60	60	42	11
72	72	72	48	13
84	84	84	54	15

III. SIMULATION RESULTS

To evaluate the performance of proposed topology a 5-level inverter configuration is developed in Matlab/Simulink environment.The switching pulses are generated using sinusoidal pulse width modulation technique. Two level shifted carrier waves are used to generate the control pulses for level generation as per the switching states specified in Table. I and switching frequency of H-bridge is taken equal to line frequency. Fig. 2 shows the simulated results of output voltage waveforms for step changes in ref signal from 0.5 to 1 pu for 20Ω and 10 mH balanced three phase RL load. It is observed that the output voltage level is varying 115Vrms to 230Vrms during .5sec time as per the change in reference signal. Similarly, the magnitude of current flowing in the load is also increased during rise in voltage level as shown in Fig.3. So the performance of the proposed topology is analyzed during step changes in input reference signal. It can be observed that the PI control gives better response of change in output as per the required value and the corresponding change in modulation index is given in Fig. 4. The frequency spectrum of output phase voltage is shown in Fig. 5.

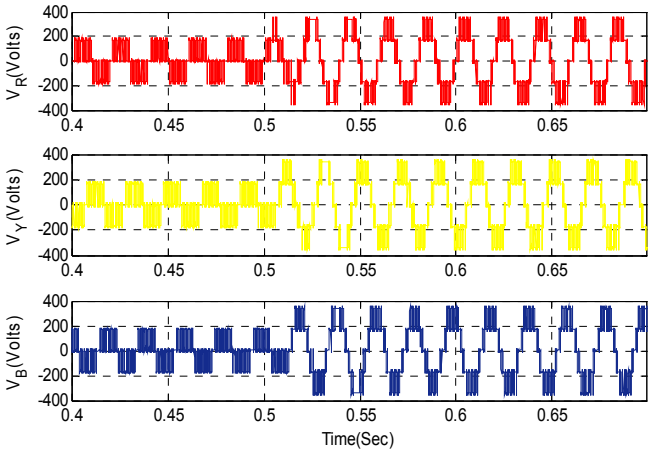

Fig.2. Output voltage waveforms for step changes in input reference signal from .5 to 1 for a constant RL load of 20Ω and 10mH

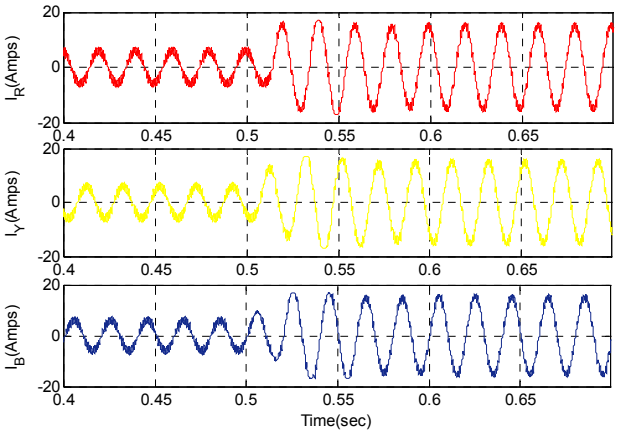

Fig.3. Load current waveforms for step changes in input reference signal from .5 to 1 and for a constant RL load of 20Ω and 10mH

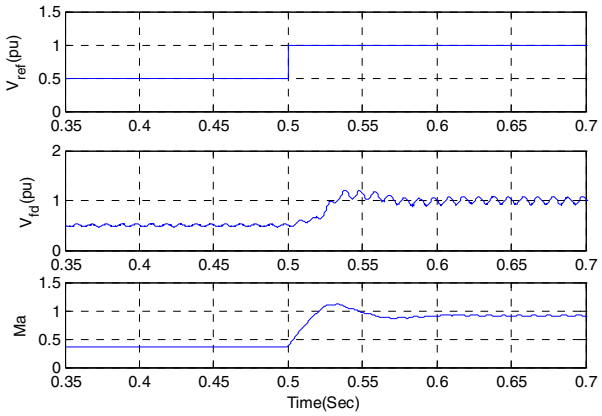

Fig.4. Output waveform of reference voltage, feedback voltage and Modulation Index (Ma)

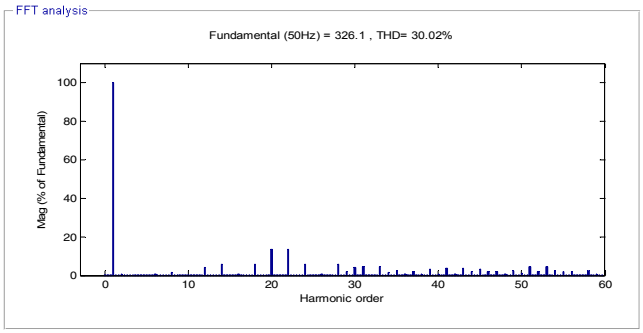

Fig.5. FFT Analysis of output voltage waveforms for m_a=1.

V.CONCULSION

In this paper a new topology, 3-phase hybrid matrix multilevel inverter is proposed with reduced number of switches and DC source. The complete operation and switching schemes are presented. The proposed topology doesn't require any clamping diodes and capacitors which is mandatory for diode clamped and flying capacitor topologies. It is observed from the comparison, the proposed topology will give better dealing compared to conventional topologies in terms of reduced components, size and installation cost for more than five level voltage outputs. Further simulation results are presented for step change in input signal and their performance are exhaustively analyzed.

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