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Dynamic dc voltage regulation of split-capacitor DSTATCOM for power quality improvement

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Abstract: A distribution static compensator (DSTATCOM) is used for power quality improvement in the distribution system. In the conventional DSTATCOM, the dc voltage is kept constant and it is selected based on rated reactive load. Under light load or reduced load conditions, the compensator works perfectly even though the dc voltage is reduced from its rated value. Maintaining the dc voltage constant under reduced or light load conditions leads to unnecessary voltage stress across the switching devices. Therefore, in this study, a simple dynamic dc voltage regulation is proposed to reduce the voltage stress across switching devices under the reduced load conditions. The proposed algorithm optimises the value of dc voltage based on reactive load without compromising the performance of the DSTATCOM. To validate the proposed method, simulation and experimental studies were carried out on the three-phase two-level split-capacitor DSTATCOM for harmonic mitigation, reactive power compensation and load balancing.

1 Introduction

The increase of non-linear loads due to the proliferation of power electronic devices and inductive loads in a three-phase four-wire (3P4W) distribution system results in power quality issues such as current harmonics, poor voltage regulation, load unbalancing and excessive neutral current, which are extensively reported in the literature [1–3]. The solutions to these distribution system problems are investigated and reported in the literature [4–6]. A distribution static compensator (DSTATCOM) is one of the suitable solutions to compensate for the above distribution system problems [7–9].

In the 3P4W distribution system, three individual single-phase DSTATCOMs, four-leg DSTATCOM and split-capacitor DSTATCOM topologies are widely used for harmonic mitigation, reactive power compensation, load balancing and neutral current compensation [10–13]. The first two topologies require more number of switching devices, which leads to high switching losses and increases the cost. The split-capacitor DSTATCOM topology suffers from dc capacitor voltage unbalancing due to dc loads. However, there are several techniques proposed in the literature to overcome the capacitor voltage unbalancing problem [14–16]. In general, the dc voltage in any topology is maintained at twice the peak of point of common coupling (PCC) voltage [17]. In [18], compensation performance was investigated by varying the dc voltage and interfacing inductance; it has been concluded from the empirical relation and the analytical expression that, the required dc voltage is 1.6 times the peak of PCC voltage. An optimum dc voltage for an active filter is defined based on vector trajectories by theoretical analysis, but it is considered only harmonic compensation [19]. In [20], a transformer-less hybrid series active filter was proposed to improve the power quality with reduced dc voltage. This topology does not require an isolation transformer. However, it requires three H-bridges with isolated dc sources fed from auxiliary power supply. In [21], dc-link voltage was reduced by connecting an ac capacitor in series with the DSTATCOM, so that the ac capacitor voltage was added to ac voltage of the DSTATCOM and leads to reduction in the dc voltage requirement. Further, hybrid filter topologies are proposed to reduce the dc voltage with the combination of active and passive filters [22, 23]. In the above discussed DSTATCOM topologies, the dc voltage is constant and its value is selected based on rated reactive load. In general, the system may not always operate at rated load condition, under this condition, the required dc voltage is less when compared to dc voltage requirement at rated or full load condition. However, in the above-discussed DSTATCOM methods, even the system is operating under reduced or light load conditions, the voltage stress across switching devices will be the same as that of rated load condition.

An adaptive dc voltage regulation method has been discussed in the literature to minimise the switching loss of voltage source inverter (VSI). In [24], an *LC* hybrid active power filter (*LC*-HAPF) with adaptive dc voltage regulation is presented for only reactive power compensation. In [25], *LC*-HAPF is extended to fifth harmonic mitigation and reactive power compensation. However, these approaches require the calculation of reactive power supplied by passive and active power filters, which increases the number of sensing elements. In [26], a combination of active filters with thyristor controlled *LC* (TC*LC*) is developed to reduce dc voltage. This approach increases the cost and switching loss because of many switching devices. Moreover, the gate pulses generation for both the active filter and TC*LC* makes the system more complex. The topologies discussed in [24–26], require more transformations to calculate dc voltage, which leads to computational burden on the controller. The hybrid filter topologies suffer from resonance, slow in response and complex in design. In [27], a DSTATCOM with adaptive dc-link voltage regulation under load variations is discussed based on minimum dc-link voltage and minimum filter current. However, the maximum dc voltage limit is not defined and experimental validation is not presented.

In this study, an algorithm is proposed for dynamic dc voltage regulation of the DSTATCOM based on reference filter currents derived from instantaneous symmetrical component theory (ISCT). These reference filter currents are used to compute the reference dc voltage. In the case of an unbalanced system, a maximum of three reference filter currents is selected to calculate the reference dc voltage. The proposed dynamic dc voltage regulation method maintains optimum dc voltage corresponding to DSTATCOM burden. Therefore, the voltage stress across switching devices is minimised under reduced reactive load conditions, which in turn reduces switching loss and increases the inverter reliability. The effectiveness of the proposed method is validated through simulation and experimental studies.

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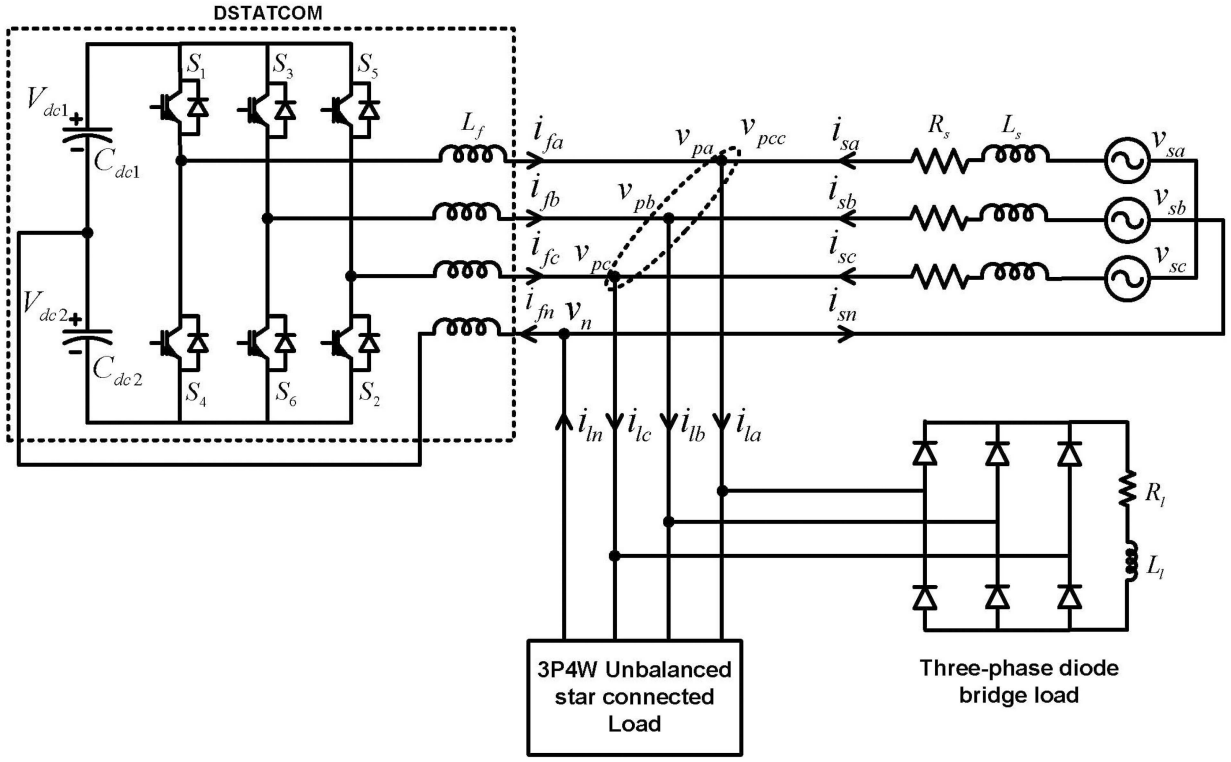

Fig. 1 *Three-phase two-level split-capacitor DSTATCOM for power quality improvement in the distribution system*

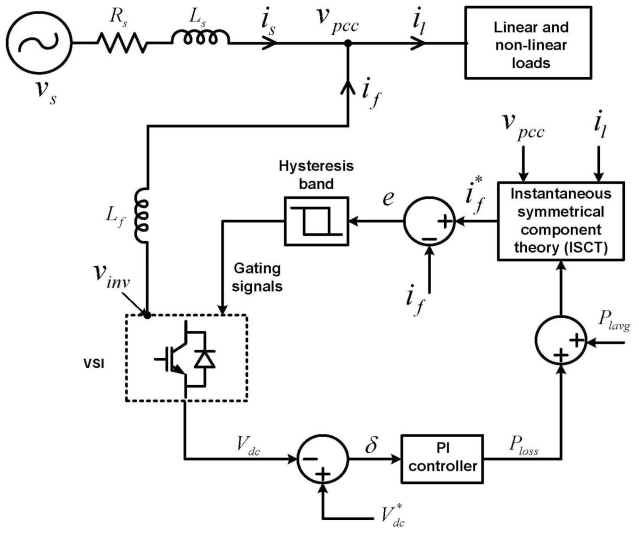

Fig. 2 *Single-line diagram of the split-capacitor DSTATCOM in the conventional method*

2 Operation of conventional split-capacitor DSTATCOM

In this study, a split-capacitor DSTATCOM is considered because of less number of switching devices compared to three single-phase DSTATCOMs and four-leg DSTATCOM, which will reduce the cost of DSTATCOM and switching loss. The three-phase two-level split-capacitor DSTATCOM topology in the distribution system is shown in Fig. 1.

During the operation of the DSTATCOM, the filter currents i_{fa}, i_{fb}, i_{fc} and i_{fn} are injected into the system such that source currents become sinusoidal, balanced and in-phase with respective source voltage. The filter currents injected by the DSTATCOM depend on control algorithm, which is explained with the help of a single-line diagram of the split-capacitor DSTATCOM, is shown in Fig. 2. The reference filter currents (i_f^*) are calculated based on PCC voltages (v_{pcc}), load currents (i_l), average real power (P_{lavg}) and power loss in VSI (P_{loss}) using ISCT [28]. Here, ISCT is considered for a three-phase four-wire system supplying star-connected load. Then, the reference filter currents from ISCT are given as

$$\left.\begin{aligned} i_{fa}^* &= i_{la} - \left(\frac{v_{pa} - v_{p0}}{\Sigma_{j=a,b,c} v_{pj}^2 - 3v_{p0}^2}\right)(P_{lavg} + P_{loss}) \\ i_{fb}^* &= i_{lb} - \left(\frac{v_{pb} - v_{p0}}{\Sigma_{j=a,b,c} v_{pj}^2 - 3v_{p0}^2}\right)(P_{lavg} + P_{loss}) \\ i_{fc}^* &= i_{lc} - \left(\frac{v_{pc} - v_{p0}}{\Sigma_{j=a,b,c} v_{pj}^2 - 3v_{p0}^2}\right)(P_{lavg} + P_{loss}) \end{aligned}\right\} \quad (1)$$

where $v_{p0} = (1/3)(v_{pa} + v_{pb} + v_{pc})$ is zero sequence voltage, and P_{loss} indicates losses in the VSI. If the dc capacitors are in self-charging mode, the dc voltage is reduced due to losses in VSI.

This will deteriorate the performance of the DSTATCOM. To overcome this, the dc voltage (V_{dc}) is maintained constant to a fixed reference dc voltage (V_{dc}^*) by a proportional integral (PI) controller and the output of the PI controller is considered as a real component (P_{loss}), which is included in control algorithm, as shown in Fig. 2. To track the reference filter current, hysteresis current control technique is used. The input for the hysteresis controller is error (e), which is the difference between the reference filter current (i_f^*) and actual filter current (i_f). Depending on the error (e), the hysteresis controller generates gating pulses, which are applied to insulated gate bipolar transistor (IGBT) switches. According to gating pulses, the DSTATCOM will inject filter currents to achieve perfect compensation.

In general, the dc voltage is maintained constant at twice the peak of PCC voltage during DSTATCOM operation [17]. This high dc voltage requirement increases the stress in switching devices under light load conditions. The dc voltage can be reduced without affecting DSTATCOM compensation performance under reduced or light load conditions. The proposed method to compute the required dc voltage is explained in the next section.

3 Proposed algorithm for dynamic dc voltage regulation

In the proposed method, the dc voltage is varied dynamically based on load but the maximum dc voltage is limited to twice the peak of

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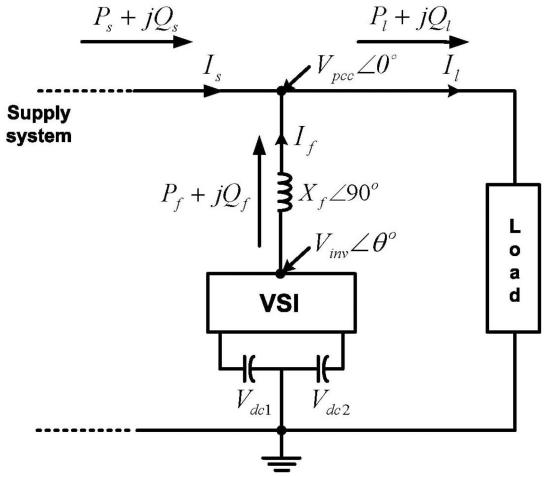

Fig. 3 *Power flow diagram of the single-phase system*

PCC voltage. Since, the DSTATCOM injects maximum reactive power at $V_{dc} = 2V_{pcc}$, which is explained from the power flow between VSI and PCC. The power flow diagram of a single-phase system is shown in Fig. 3, where P_s and Q_s are real and reactive powers supplied by the source, respectively; P_l and Q_l are real and reactive powers drawn by the load, respectively; P_f and Q_f are real and reactive powers injected by the DSTATCOM, respectively.

The current and power injected by the DSTATCOM are derived from the power flow diagram shown in Fig. 3, and are given below

$$I_f = \frac{V_{inv}\angle\theta^\circ - V_{pcc}\angle 0^\circ}{X_f\angle 90^\circ} \tag{2}$$

$$P_f + jQ_f = V_{pcc}\text{conjugate}(I_f) \tag{3}$$

By substituting I_f in (3) and rearranging the real and imaginary parts, the real (P_f) and reactive (Q_f) powers are given below

$$P_f = \frac{V_{pcc}V_{inv}}{X_f}\sin\theta, \tag{4}$$

$$Q_f = \frac{V_{pcc}\,V_{inv}}{X_f}\cos\theta - \frac{V_{pcc}^2}{X_f}, \tag{5}$$

where θ is the angle between the output voltage of VSI and PCC voltage. In general, dc voltage design is carried out based on the reactive power injection, Q_f by the DSTATCOM into the system, because there is no real power injection, P_f by the DSTATCOM. In that case, the possibility of real power injection, P_f is zero only when θ is very small (i.e. ;0°) and it is observed from (4). By substituting $\theta = 0^\circ$ in (5), the reactive power (Q_f) is

$$Q_f = \frac{V_{pcc}\,V_{inv}}{X_f} - \frac{V_{pcc}^2}{X_f}. \tag{6}$$

In (6), the V_{inv} is dependent on the amplitude modulation index of VSI is m. So, ac side voltage of VSI, V_{inv}, is m times the dc side voltage (V_{dc}) of VSI, i.e. $V_{inv} = mV_{dc}$. By substituting V_{inv} in (6), Q_f is expressed as

$$Q_f = \frac{V_{pcc}(mV_{dc})}{X_f} - \frac{V_{pcc}^2}{X_f}. \tag{7}$$

The DSTATCOM injects reactive power (Q_f) when $mV_{dc} > V_{pcc}$, as observed from the above equation. During the process of reactive power injection by the DSTATCOM into the system, the PCC voltage, V_{pcc} will vary. By $dQ_f/dV_{pcc} = 0$, the condition for maximum reactive power injected by the DSTATCOM is as

$$V_{pcc} = \left(\frac{m}{2}\right)V_{dc}. \tag{8}$$

In the design of DSTATCOM, m value is selected as unity and the dc voltage of VSI is equal to twice the peak of PCC i.e. $V_{dc} = 2V_{pcc}$. Thus, the maximum dc voltage is limited to twice the peak of PCC voltage in the proposed method. The maximum reactive power ($Q_{f,max}$) compensated by the DSTATCOM is derived by substituting maximum dc voltage ($V_{dc,max} = 2V_{pcc}$) in (7) and is given as

$$Q_{f,max} = \frac{V_{pcc}^2}{X_f} = V_{pcc}I_{f,max}, \tag{9}$$

where $I_{f,max} = \dfrac{V_{pcc}}{X_f}$ is the maximum filter current corresponding to $Q_{f,max}$.

In general, the reactive power required by load is not always $Q_{f,max}$. Under the reduced reactive load conditions, the required reactive power injection by the DSTATCOM is achieved with a reduced value of dc voltage. The reactive power injected by the DSTATCOM is dependent on the dc voltage, which can be observed from (7). This motivates to reduce the dc voltage whenever the reactive load is less than the $Q_{f,max}$, which reduces the voltage stress across switching devices. An algorithm is proposed to find the optimum dc voltage, which is as follows. In the case of reduced load conditions, the required reactive power injected by the DSTATCOM and dc voltage is considered as Q_f^* and V_{dc}^*, respectively. Then, Q_f^* is expressed from (7) as

$$Q_f^* = \frac{V_{pcc}(mV_{dc}^* - V_{pcc})}{X_f} = V_{pcc}I_f^*, \tag{10}$$

where I_f^* is the reference filter current corresponding to Q_f^*. Using (9) and (10), I_f^* is expressed in terms of $I_{f,max}$ and is given below

$$I_f^* = \frac{(mV_{dc}^* - V_{pcc})}{V_{pcc}}I_{f,max}. \tag{11}$$

By rearranging the above equation, the reference dc voltage is expressed as

$$V_{dc}^* = \frac{V_{pcc}}{m}\left(\frac{I_f^* + I_{f,max}}{I_{f,max}}\right). \tag{12}$$

Therefore, the reference dc voltage, V_{dc}^*, is computed from the reference filter current (I_f^*).

In general, load changes frequently, so that it requires the frequent change of reference dc voltage, this will affect the performance of the DSTATCOM. To eliminate this problem, the final dc voltage is selected from the look-up table in step variations. These step variations are done in between minimum to maximum dc voltage values. If the calculated reference dc voltage falls between the specified step variation, the higher value is selected as the final dc voltage reference.

The single-line diagram of the proposed method is shown in Fig. 4*a*. Here, the dc voltage is varied dynamically when compared to the conventional method of Fig. 2. The dynamic dc voltage reference generation is explained with the help of a flow chart as shown in Fig. 4*b*. First, initialise $V_{dc,max}$ and $I_{f,max}$ corresponding to the rated reactive load. Among the generated three reference filter currents from ISCT, the maximum reference filter current is selected to decide the reference dc voltage. If the difference between the maximum filter current $I_{f,max}$ and the reference filter current (I_f^*) is equal to zero, then the maximum dc voltage (i.e. $V_{dc,max} = 2V_{pcc}$) is considered as a reference dc voltage. Otherwise, the optimum V_{dc}^* is computed from (12) and the final value is selected from the look-up table. The advantage of the proposed

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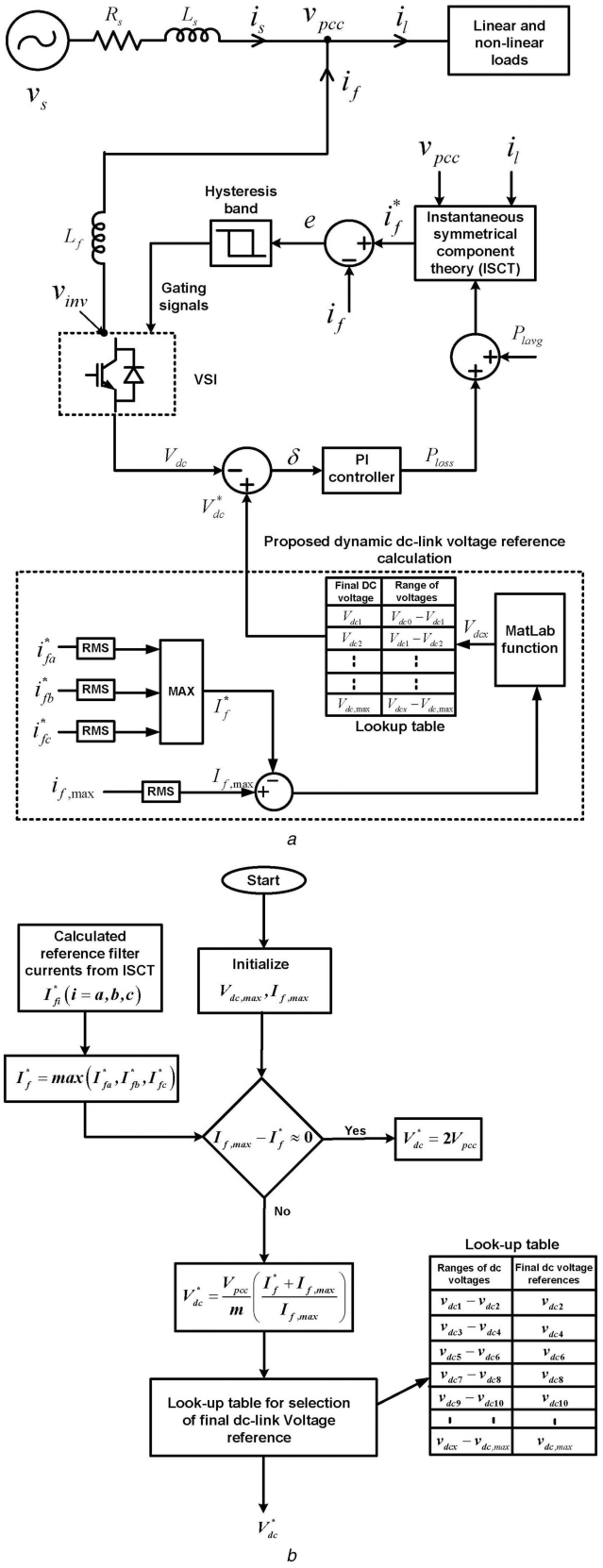

Fig. 4 *Single-line diagram and control algorithm of the proposed method*
(a) Proposed dynamic dc voltage regulation-based DSTATCOM, ***(b)*** Flow-chart for the selection of reference dc voltage

method is evaluated based on the IGBT switching losses, and the methodology is explained below.

The switch (IGBT) loss is calculated from the switching frequency (f_{sw}) and energy dissipation (E_{sw}) of the switch, i.e. $P_{sw} = E_{sw} f_{sw}$. The energy dissipation of switch is dependent on the current through switch (I_f), voltage across switch (V_{dc}) during OFF-state and junction temperature (T_j). The energy dissipation under working conditions with respect to nominal test conditions is obtained from (13) [29, 30].

$$E_{sw} = E_{sw,n}\left(\frac{I_f}{I_{fn}}\right)^{k_i}\left(\frac{V_{dc}}{V_{dc,n}}\right)^{k_v}\left(1 + TC_{sw}(T_j - T_{jn})\right), \quad (13)$$

where I_{fn}, $V_{dc,n}$, T_{jn} and energy dissipation $E_{sw,n}$ are reference values at nominal test conditions, by the data sheet of the IGBT switch (SKM 75GB123D), k_i is the current dependency (for IGBT ; 1, diode ; 0.5), k_v is the voltage dependency (for IGBT ; 1.2 or 1.4, diode ; 0.6), TC_{sw} is the temperature coefficient of switching losses (for IGBT ; 0.003, diode ; 0.005). The reduction in the switching losses with the proposed method is validated with the simulation and experimental studies, discussed in below sections.

4 Simulation studies

To verify the proposed dynamic dc-link voltage regulation, simulation is carried out in MATLAB simulink software. The parameters used for simulation studies are given in Table 1. The simulation results for both conventional and proposed dynamic dc-link voltage methods are presented here. In simulation results, the variables are named as: PCC voltage (v_{pcc}); source phase currents (i_s); load current (i_l); filter currents (i_f); source side neutral current (i_{sn}); total dc-link voltage (V_{dc}); voltage across switch (V_{sw}); inverter ac side line voltage (V_{inv}).

4.1 Simulation results for stiff voltage source

The simulation results of the 3P4W distribution system with the conventional split-capacitor DSTATCOM supplying unbalanced star-connected linear load and three-phase diode bridge load are shown in Fig. 5. To study the performance of the DSTATCOM, the following events are considered to occur in the system for simulation studies.

(i) At $t = 0.04$ s, an unbalanced star-connected linear load is connected without the DSTATCOM.
(ii) At $t = 0.12$ s, the DSTATCOM is connected to PCC.
(iii) At $t = 0.3$ s, load is increased by connecting a three-phase diode bridge.

It is observed from Fig. 5, from $t = 0.04$ s to $t = 0.12$ s the load and source currents are the same, and the unbalance load current flow through a neutral conductor. The DSTATCOM is connected at $t = 0.12$ s, and the compensation starts in 1–2 cycles, and the source currents become balanced, sinusoidal and in-phase with the PCC voltages, while the source side neutral current becomes zero. The dc-link capacitors charged to reference voltage (1200 V) and maintained constant with the PI controller. At $t = 0.3$ s, load is increased by connecting a three-phase diode bridge load, under this load condition also the dc voltage is maintained at 1200 V. The voltage across the switch (V_{sw}) is shown in Fig. 5. The inverter ac side line voltage (V_{inv}) is maintained constant even if the load is varied because of constant dc voltage regulation in the conventional method. From the above simulation studies, it is observed that, in the conventional method of dc voltage regulation, the voltage across switch is constant (i.e. equal to dc voltage of 1200 V) irrespective of load variation. It leads to high voltage stress across switching devices during reduced or light loaded conditions. To show the effectiveness of the DSTATCOM with dynamic dc voltage regulation, the same simulation events (i.e. in the conventional method) are considered in the proposed method.

The simulation waveforms with the proposed dynamic dc voltage regulation are shown in Fig. 6. It is observed from Fig. 6 that during the DSTATCOM operation, the source currents become sinusoidal, balanced and in-phase with PCC voltages. If the load is increased by connecting a three-phase diode bridge load at $t = 0.3$ s, the compensation is not affected. The required dc voltages for both the load conditions are calculated from the proposed method and

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Table 1 Simulation parameters

Symbol	System parameters	Values
V_s	supply voltage	440 V, 50 Hz
R_s, L_s	source impedance	0.2 Ω, 1 mH
L_f	interfacing inductance	12 mH
C_{dc}	dc-link capacitance	1600 μF
k_P, k_I	PI controller gains	10, 0.01
h	hysteresis band	±0.1 A
	unbalanced linear load	*a*-ph: 20 Ω, 32 mH
	(Y-connected load)	*b*-ph: 16 Ω, 42 mH
		c-ph: 10 Ω, 60 mH
	three-phase diode bridge load	36 Ω, 128 mH
V_{dc}	rated dc voltage	1200 V

Non-stiff source parameters: R_s, L_s −0.8 Ω and 3.5 mH; Ripple filter −28 Ω and 5 μF.

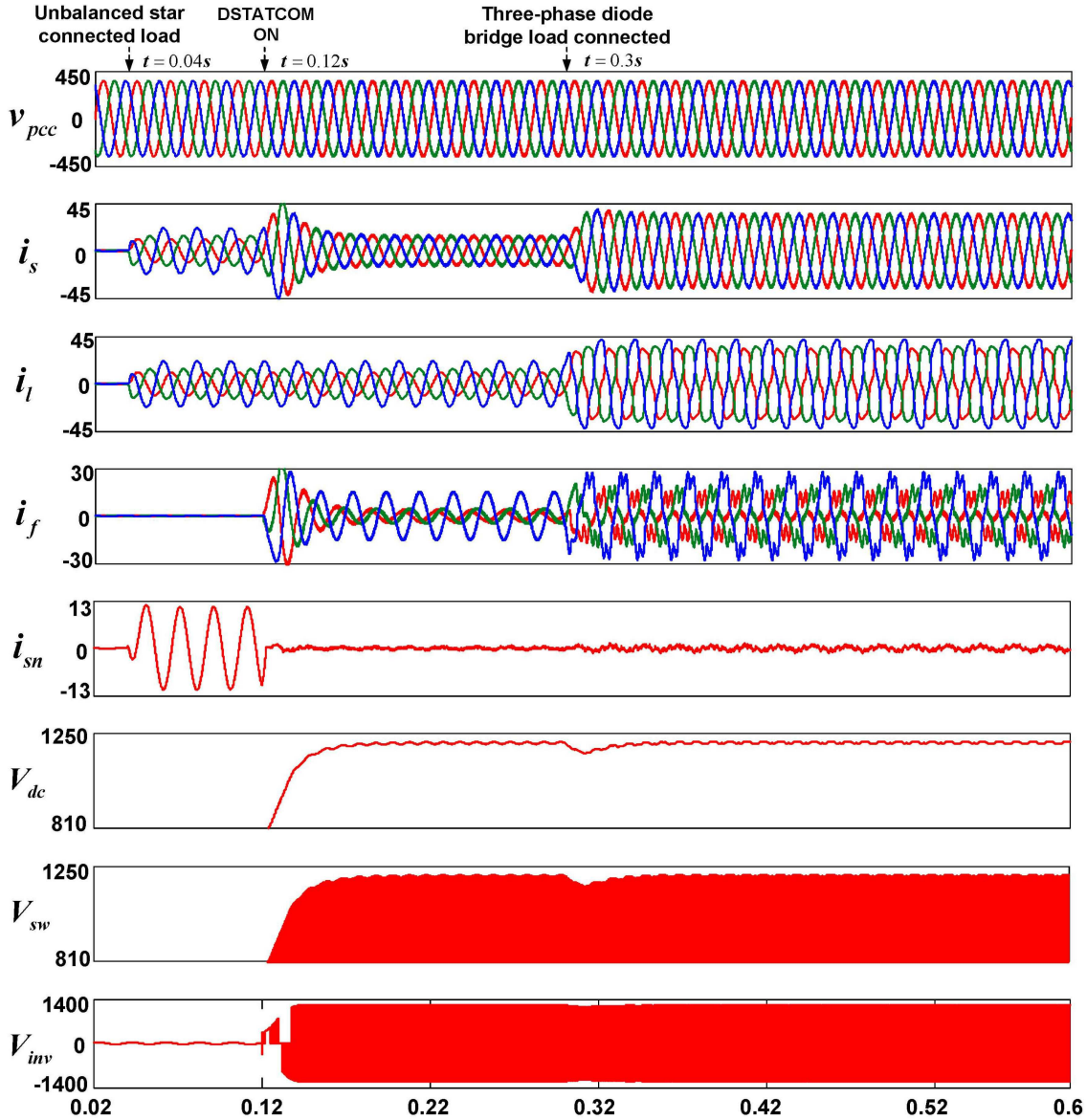

Fig. 5 *Performance of DSTATCOM with constant dc voltage regulation (conventional method)*

are given in Table 2. In the case of unbalanced star-connected linear load, the required dc-link voltage is computed from (12) as 768 V. However, the final dc voltage is selected from the look-up table, which is equal to 780 V. At $t = 0.3$ s, the load is increased by connecting a three-phase diode bridge, then the dc voltage is computed from the proposed algorithm is 861 V. However, the final dc voltage is selected from the look-up table, which is equal to 880 V. Therefore, the proposed dynamic dc voltage regulation method maintains less dc voltages (i.e. 780 and 880 V for two load conditions) than the conventional fixed dc voltage regulation (i.e. 1200 V) for the same load. The voltage across the switching device V_{sw} is shown in Fig. 6. The inverter ac side line voltage (V_{inv}) is varied when the load is varied because of the proposed dynamic dc voltage regulation.

The switching losses in conventional and dynamic methods are calculated from the energy dissipation across switch, which is

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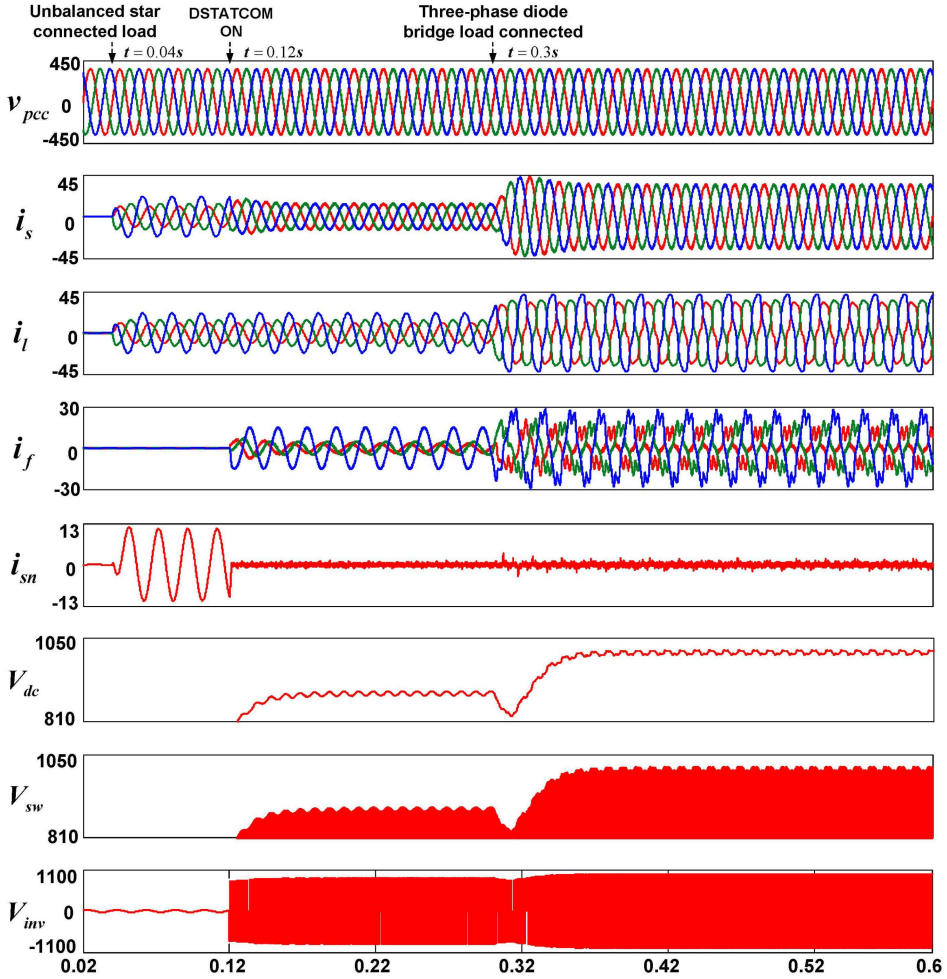

Fig. 6 *Performance of DSTATCOM with dynamic dc voltage regulation (proposed method)*

Table 2 Reference dc voltages corresponding to loads

Type of connected load	Load current (A)			Filter current (A)			Proposed (V^*_{dc}), V		Conventional (V^*_{dc}), V
	I_{la}	I_{lb}	I_{lc}	I^*_{fa}	I^*_{fb}	I^*_{fc}	Cal[a]	Final[b]	
unbalanced linear load	7.5	10	16	2.2	3.4	10.4	768	780	1200
unbalanced plus diode bridge loads	24.5	26.8	31	8.7	11.6	18	861	880	1200

[a]Cal: calculated from (12).

[b]Final: selected from the look-up table.

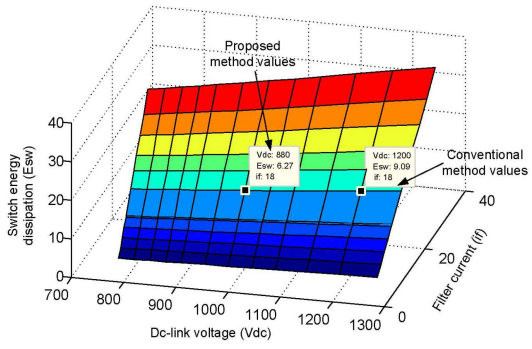

Fig. 7 *Variation of switching energy dissipation with respect to dc voltage and filter current*

explained below. The variation of switching energy dissipation with respect to the variation of dc voltage and filter current is shown in Fig. 7. It is observed that in the proposed method for the filter current 18 A and dc voltage 880 V, the switching energy dissipation is 6.27 mJ, which is less compared to 9.09 mJ in the conventional method. The corresponding switching loss (P_{sw}) in the proposed method is 31.35 W, which is less compared to 45.48 W in the conventional method.

4.2 Simulation results for non-stiff voltage source

A combination of three-phase diode bridge load and unbalance star connected linear load, and non-stiff parameters which are given in Table 1 are considered for simulation. The simulation waveforms for the conventional and proposed dynamic dc voltage regulation DSTATCOM with non-stiff voltage source are shown in Figs. 8*a* and *b*, respectively. It is observed in Fig. 8*a*, before DSTATCOM connection, PCC voltages are distorted and non-sinusoidal. After the DSTATCOM is ON at $t = 0.06$ s, the PCC voltages and source currents become sinusoidal, source currents in-phase with the PCC voltages, respectively. Here, an extra ripple filter is connected at PCC to eliminate the high frequency ripples in PCC voltage. Initially, the dc capacitors are charged to 85% of rated dc voltage and when the DSTATCOM is ON, the dc voltage is maintained to 1200 V with a dc voltage regulation loop.

It is observed from the proposed results shown in Fig. 8*b* that the compensation performance in the case of PCC voltage and source current is the same as that of the conventional method. During the transient period, that is the DSTATCOM is ON at $t =$ 0.06 s, the magnitudes of source and filter currents are high and

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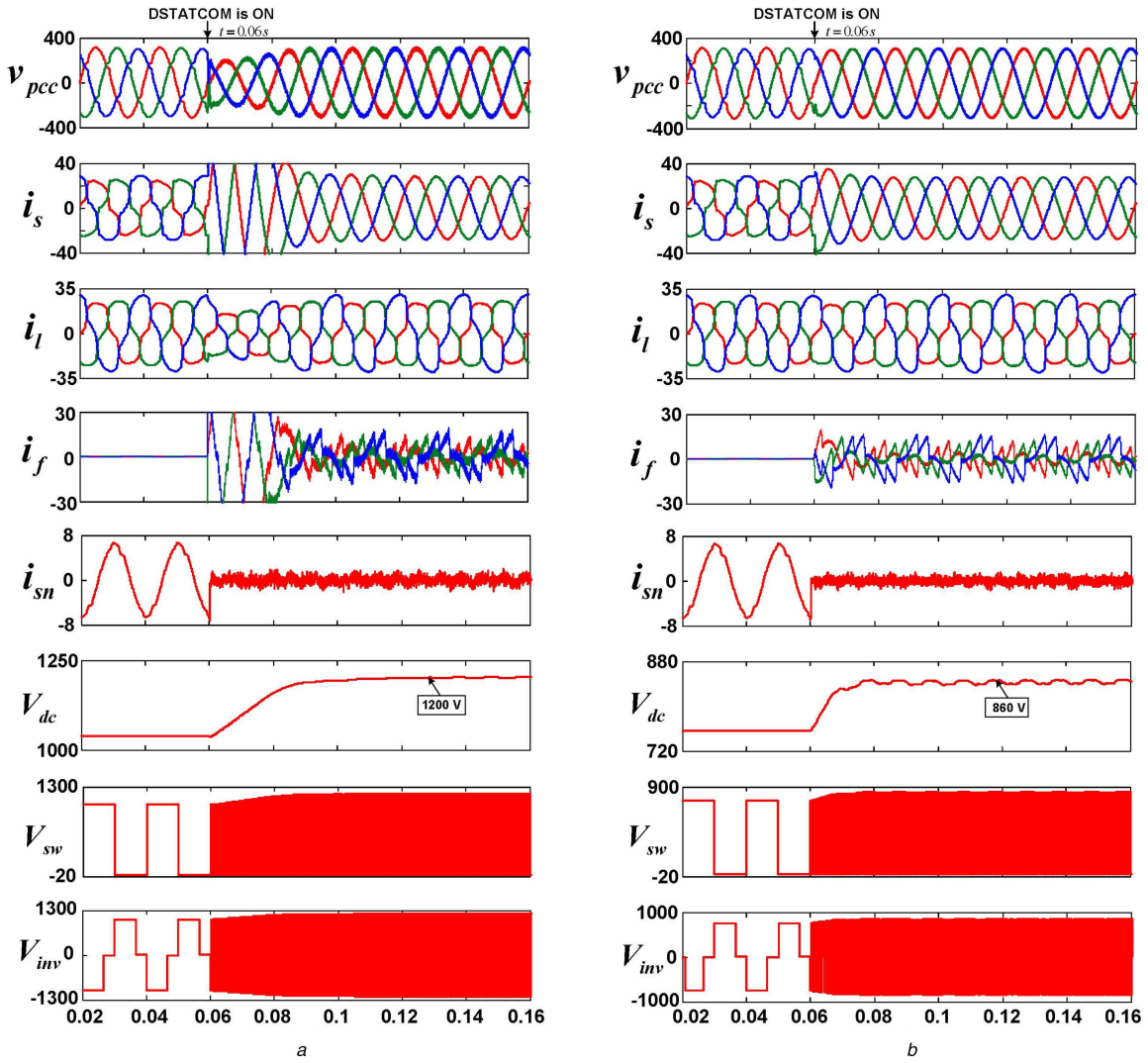

Fig. 8 *Simulation results for non-stiff voltage source with considering source impedance*
(a) Conventional DSTATCOM method, ***(b)*** Proposed DSTATCOM method

Table 3 Experimental parameters

Symbol	Parameters	Values
V_s	supply voltage	50 V, 50 Hz
L_f	interfacing inductance	8 mH
C_{dc}	dc-link capacitance	3600 μF
k_P, k_I	PI controller gains	20, 0.04
h	hysteresis band	±0.1 A
Load-1	three-phase diode bridge load	30 Ω, 150 mH
Load-2	unbalanced linear load	*a*-ph: 14 Ω, 18 mH
		b-ph: 14 Ω, 32 mH
		c-ph: 14 Ω, 25 mH
V_{dc}	rated dc voltage	160 V

takes more time to settle in the conventional method compared to the proposed method because of higher dc voltage. Initially, the dc capacitor is charged to 65% of rated dc voltage. The DSTATCOM is ON at $t = 0.06$ s, then the dc voltage is maintained to 860 V, which is derived from the proposed adaptive dc voltage regulation method. Therefore, the voltage stress appearing across the switch is 860 V in the proposed method, which is less compared to 1200 V in the conventional method.

5 Experimental results

The performance of the proposed dynamic dc-link voltage regulation method is verified with experimental studies. dSPACE DS-1104 is used to implement the control algorithm for the DSTATCOM. The experimental parameters are given in Table 3. The experimental setup consists of IGBT switches based three-leg split-capacitor VSI DSTATCOM. The required feedback signals such as PCC voltages, load currents, filter currents and dc-link voltages are measured by using Hall-effect voltage and current transducers. dSPACE DS-1104 acquires current and voltage signals, as well as processes to generate reference filter currents, dc voltage and switching signals for IGBTs. The switching command signals are taken out from the master I/O pins of dSPACE and given to inverter switches with proper isolation.

5.1 Steady state performance of the proposed dynamic dc voltage regulation method

The dynamic dc voltage regulation of the DSTATCOM has been tested for harmonic mitigation, reactive power compensation and balancing in the presence of non-linear three-phase diode bridge load. The source voltage, source current after compensation, load current and filter current under steady state conditions with the proposed method for three phases are shown in Figs. 9*a*–*c*. In these figures, the different waveforms are: trace 1: source voltage (*X*-axis: 10 ms/div and *Y*-axis: 50 V/div); trace 2: source current after DSTATCOM compensation (*X*-axis: 10 ms/div and *Y*-axis: 4 A/div); trace 3: current drawn by load (*X*-axis: 10 ms/div and *Y*-axis: 4 A/div); and trace 4: filter current inject by the DSTATCOM (*X*-axis: 10 ms/div and *Y*-axis: 2 A/div). It is observed from Figs. 9*a*–*c*, that the source currents become sinusoidal and in-phase with respective phase voltages. The harmonic spectra of phase-*a* source current before and after compensation are shown in Figs. 10*a* and

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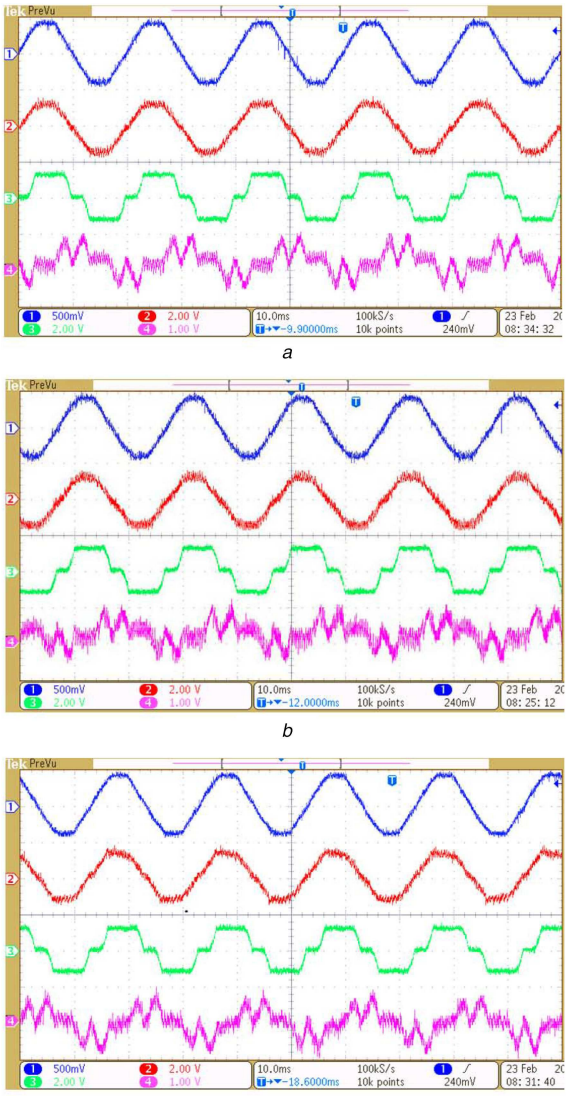

Fig. 9 *Experimental waveforms obtained with the proposed dynamic dc voltage regulation DSTATCOM under steady state conditions*
(a) Phase-*a* waveforms, ***(b)*** Phase-*b* waveforms, ***(c)*** Phase-*c* waveforms

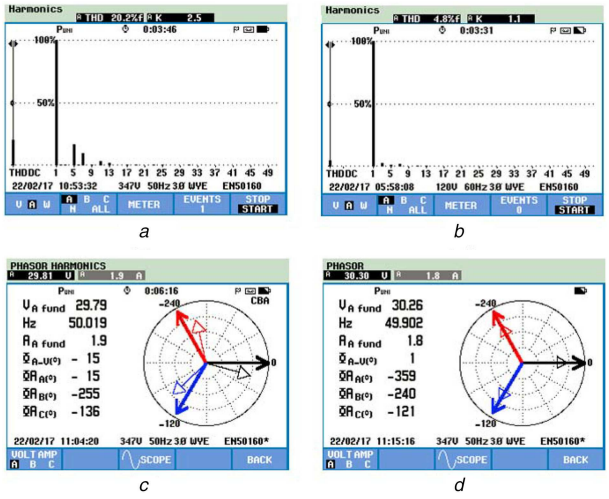

Fig. 10 *Harmonic spectra and phasor diagram of currents and voltages for load-1*
(a) Phase-*a* source current harmonic spectra before compensation, ***(b)*** Phase-*a* source current harmonic spectra after compensation, ***(c)*** Phasor diagram of source voltages and source currents before compensation, ***(d)*** Phasor diagram of source voltages and source currents after compensation

b, respectively. Before compensation, the source current total harmonic distortion (THD) is 20.2%, after compensation the THD is reduced to 4.8%, which is <5% of the IEEE-519 recommended value. The phasor diagram of source voltages and source currents before compensation is shown in Fig. 10*c*. It is observed that the three-phase source currents lag the respective phase voltages by 15°, 15° and 16°. The phasor diagram of source voltages and source currents after compensation is shown in Fig. 10*d*. The source currents are in-phase with respective source voltages after compensation.

5.2 Transient performance of the proposed method

The proposed dynamic dc voltage regulation for the DSTATCOM has been tested under transient load conditions for harmonic mitigation, reactive power compensation and load balancing. In this case, the load is increased by connecting an additional unbalanced three-phase linear load to the previous three-phase diode bridge load. Before and after transient load conditions, the source voltage, source current, load current and filter current for three phases are shown in Figs. 11*a–c*, respectively. The different waveforms in Fig. 11*a–c* are: trace 1: source voltage (*X*-axis: 10 ms/div and *Y*-axis: 50 V/div); trace 2: source current after DSTATCOM compensation (*X*-axis: 10 ms/div and *Y*-axis: 4 A/div); trace 3: current drawn by load (*X*-axis: 10 ms/div and *Y*-axis: 4 A/div); and trace 4: filter current injected by the DSTATCOM (*X*-axis: 10 ms/div and *Y*-axis: 4 A/div). It is observed that the source currents are in-phase with respective source voltages. The dc-link voltage (V_{dc}) and switch voltage (V_{sw}) for transient load variation are shown in Fig. 11*d* as *X*-axis: 1 s/div and *Y*-axis: 40 V/div. It is observed from Fig. 11*d* that the dc-link voltage is maintained at 82 V for load-1 and it is increased to 126 V when both the loads are connected. These dc voltage magnitudes will appear across the switches. However, in the case of the conventional split-capacitor DSTATCOM, the total dc-link voltage is maintained constant (i.e. ;160 V) without considering load conditions. Due to the proposed method, the voltage stress across switches decreased under reduced or light loaded conditions. It leads to reduction of the switching losses.

The harmonic spectra of phase-*a* source current before compensation for change in load are shown in Fig. 12*a* having THD 9.8%. After compensation the harmonic spectra of phase-*a* source current are shown in Fig. 12*b*. It is observed that the THD of the source current is reduced to 3.6%. The phasor diagram of source voltages and source currents before compensation is shown in Fig. 12*c*. It is observed that the phase-*a*, *b*, *c* source currents lag the phase-*a*, *b*, *c* source voltages by 30°, 32° and 35°, respectively. After compensation the phasor diagram of the source voltages and source currents is shown in Fig. 12*d*. The source currents are in-phase with respective source voltages after compensation. The experimental %THD of the source current before and after compensation in the proposed and conventional methods are shown in Table 4.

6 Comparison of the proposed DSTATCOM with other topologies

The comparison of different DSTATCOM topologies for 3P4W distribution systems in terms of switch count, ratings and cost is given in Table 5. The switch count is less in the proposed method, even though the dc capacitors are more than other topologies.

The dc voltage is maintained fixed in first three topologies, but in the proposed method dc voltage is varied. Therefore, the switching voltage stress and losses are less in the proposed dynamic three-leg split capacitor DSTATCOM. Further, the switching losses are minimised with the proposed dynamic dc voltage regulation because of the optimisation of dc voltage corresponding to reactive load conditions. The advantages and disadvantages between existing topologies in the literature and proposed method are listed in Table 6.

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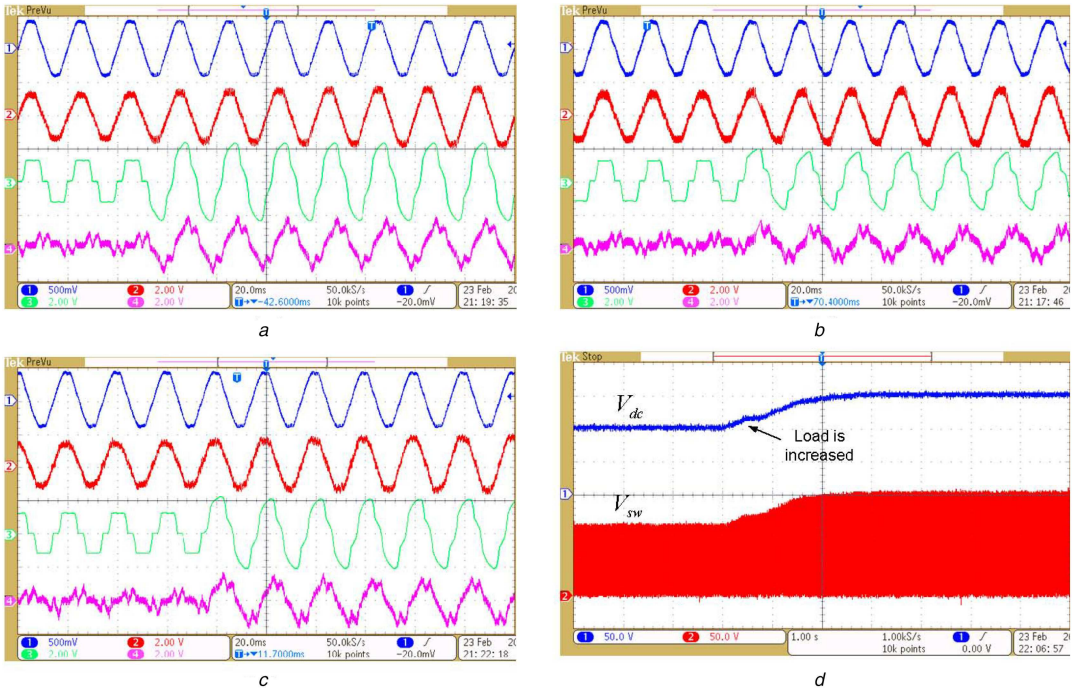

Fig. 11 *Experimental waveforms for the proposed dynamic dc voltage regulation DSTATCOM under transient load conditions*
(a) Phase-*a*, ***(b)*** Phase-*b* and ***(c)*** Phase-*c* waveforms, ***(d)*** Dc voltage (V_{dc}) and voltage across switch (V_{sw}) waveforms

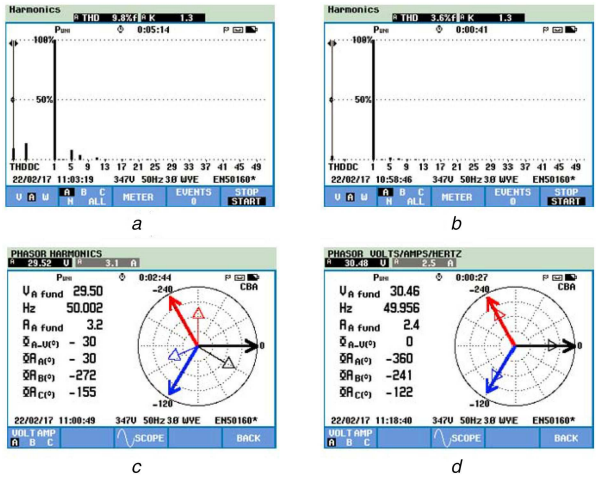

Fig. 12 *Harmonic spectra and phasor diagram of current and voltage, when both the loads are connected*
(a) Phase-*a* source current harmonic spectra before compensation, ***(b)*** Phase-*a* source current harmonic spectra after compensation, ***(c)*** Phasor diagram of source voltages and source currents before compensation, ***(d)*** Phasor diagram of source voltages and source currents after compensation

Table 4 Experimental %THDs of source currents

Type of load		Before compensation (%THD)	After compensation (%THD)	
			Proposed method	Conventional method
load-1	i_{sa1}	20.2	4.8	4.6
	i_{sb1}	20.6	4.2	4.5
	i_{sc1}	20.1	4.3	4.4
load-2	i_{sa2}	9.8	3.6	3.9
	i_{sb2}	10.3	4.1	4.2
	i_{sc2}	13.8	3.8	3.8

7 Conclusion

This study presents an algorithm for dynamic dc voltage regulation for a DSTATCOM to compensate unbalanced and non-linear loads in a 3P4W distribution system. The performance of the proposed dynamic dc voltage method has been investigated through simulation and experimental studies. It is observed that the proposed method compensates the reactive power, source current harmonics and neutral current with dynamic dc voltage variations.

The advantage of the proposed method is evaluated based on the IGBT switching losses. In the proposed method of DSTATCOM operation, a significant reduction in switching losses is observed when compared to the conventional method. The voltage stress across the switching devices also reduced, which in turn extends the life time of switching devices.

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Table 5 Comparison of DSTATCOM topologies in terms of device count, ratings and cost

Topology features	Three single-phase DSTATCOMs [10]	Four-leg DSTATCOM [31]	Conventional 3-leg split-capacitor [12]	Proposed dynamic 3-leg split-capacitor
number of switches	12	8	6	6
no. of dc capacitors	1	1	2	2
DC voltage	fixed	fixed	fixed	variable
voltage stress across each switch	$\frac{2}{\sqrt{3}}(V_{sm})_{L-L}$	$2(V_{sm})_{L-L}$	$\frac{4}{\sqrt{3}}(V_{sm})_{L-L}$	variable & reduced[a]
switching loss	very high	high	moderate	low
unbalance compensation	yes	yes	yes	yes
cost	highest	medium	low	low

[a]Under reduced reactive load conditions.

Table 6 Comparison of different DSTATCOM topologies with the proposed method for power quality improvement

Topologies	Advantage	Disadvantage
Singh *et al*. [17]	better compensation at full load	higher dc link voltage (i.e. two times peak of PCC voltage)
		switching losses are more
Mishra and Karthikeyan [18] and Manoj Kumar and Mishra [32]	compensation is good	switching losses are more under reduced or light load conditions
	dc voltage is reduced to 1.6 times peak of PCC voltage	
Javadi *et al*. [20]	DC voltage is reduced	requires three H-bridges with isolated dc sources fed from the auxiliary power supply
	does not require an isolation transformer	
Lam *et al*. [24, 25]	reactive power compensation with optimum dc voltage	limited to reactive power and fifth harmonic compensation
		it requires three extra ac capacitors
	switching losses are reduced	resonance problem
Lam *et al*. [26]	reduced dc voltage	more number of switches required
	switching losses are reduced	complex control and cost high
Wei *et al*. [23]	low cost	more number of switches required
	DSTATCOM rating is low	large-rating of thyristor switched capacitors required
		compensation fails in the presence of dc off-set in load current
Proposed method	dynamic dc voltage regulation	under full load conditions, the switching losses are high compared to hybrid reduced dc voltage topologies [23, 25, 26]
	switching losses are optimised	
	no resonance problem	
	easy to implement the control algorithm	

8 References

[1] Bollen, M.H.: '*Understanding power quality problems*', vol. **1** (IEEE, Piscataway, NJ, USA, 2000), pp. 1–35

[2] Arrillaga, J., Watson, N.R.: '*Power system harmonics*' (John Wiley and Sons, Chichester, UK, 2004)

[3] Kusko, A., Thompson, M.T.: '*Power quality in electrical systems*' (McGraw-Hill, New York, NY, USA, 2007)

[4] Akagi, H.: 'Active harmonic filters', *Proc. IEEE*, 2005, **93**, pp. 2128–2141

[5] Sreenivasarao, D., Agarwal, P., Das, B.: 'Neutral current compensation in three-phase, four-wire systems: a review', *Electr. Power Syst. Res.*, 2012, **86**, pp. 170–180

[6] Mishra, M.K., Ghosh, A., Joshi, A.: 'Load compensation for systems with non-stiff source using state feedback', *Electr. Power Syst. Res.*, 2003, **67**, pp. 35–44

[7] Ghosh, A., Ledwich, G.: '*Power quality enhancement using custom power devices*' (Springer Science and Business Media, New York, NY, USA, 2012)

[8] Venkatraman, K., Selvan, M.P., Moorthi, S.: 'Predictive current control of distribution static compensator for load compensation in distribution system', *IET Gener. Transm. Distrib.*, 2016, **10**, pp. 2410–2423

[9] Arya, S.R., Singh, B.: 'Implementation of distribution static compensator for power quality enhancement using learning vector quantisation', *IET Gener. Transm. Distrib.*, 2013, **7**, pp. 1244–1252

[10] Khadkikar, V., Chandra, A.: 'An independent control approach for three-phase four-wire shunt active filter based on three H-bridge topology under unbalanced load conditions'. IEEE Power Electronics Specialists Conf., 2008, pp. 4643–4649

[11] Singh, B., Arya, S.R., Jain, C., *et al.*: 'Implementation of four-leg distribution static compensator', *IET Gener. Transm. Distrib.*, 2014, **8**, pp. 1127–1139

[12] Singh, B., Rastgoufard, P., Singh, B., *et al.*: 'Design, simulation and implementation of three-pole/four-pole topologies for active filters', *IEE Proc.-Electr. Power Appl.*, 2004, **151**, pp. 467–476

[13] Gawande, S.P., Ramteke, M.R., Pande, N.: 'Improved equal current approach for reference current generation in shunt applications under unbalanced and distorted source and load conditions', *IET Gener. Transm. Distrib.*, 2016, **10**, pp. 995–1005

[14] Shukla, A., Ghosh, A., Joshi, A.: 'Control schemes for DC capacitor voltages equalization in diode-clamped multilevel inverter-based DSTATCOM', *IEEE Trans. Power Deliv.*, 2008, **23**, pp. 1139–1149

[15] Shu, Z., Zhu, H., He, X., *et al.*: 'One-inductor-based auxiliary circuit for dc-link capacitor voltage equalisation of diode-clamped multilevel converter', *IET Power Electron.*, 2013, **6**, pp. 1339–1349

[16] Gawande, S., Ramteke, M.R.: 'State feedback-based capacitor voltage equalisation scheme in distribution static compensator for load compensation', *IET Gener. Transm. Distrib.*, 2015, **9**, pp. 2188–2197

[17] Singh, B., Jayaprakash, P., Kothari, D.: 'A T-connected transformer and three-leg VSC based DSTATCOM for power quality improvement', *IEEE Trans. Power Electron.*, 2008, **23**, pp. 2710–2718

[18] Mishra, M., Karthikeyan, K.: 'An investigation on design and switching dynamics of a voltage source inverter to compensate unbalanced and nonlinear loads', *IEEE Trans. Ind. Electron.*, 2009, **56**, pp. 2802–2810

[19] Tangtheerajaroonwong, W., Hatada, T., Wada, K., *et al.*: 'Design and performance of a transformerless shunt hybrid filter integrated into a three-phase diode rectifier', *IEEE Trans. Power Electron.*, 2007, **22**, pp. 1882–1889

[20] Javadi, A., Woodward, L., Al-Haddad, K.: 'Real-time implementation of a three-phase THSeAF based on VSC and P + R controller to improve power quality of weak distribution systems', *IEEE Trans. Power Electron.*, **PP**, (99), p. 1, doi: 10.1109/TPEL.2017.2697821

[21] Karanki, S.B., Geddada, N., Mishra, M.K., *et al.*: 'A DSTATCOM topology with reduced dc-link voltage rating for load compensation with non-stiff source', *IEEE Trans. Power Electron.*, 2012, **27**, pp. 1201–1211

[22] Akagi, H., Srianthumrong, S., Tamai, Y.: 'Comparisons in circuit configuration and filtering performance between hybrid and pure shunt active filters', IAS Industry Applications Conf., 2003, **2**, pp. 1195–1202

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[23] Wei, T., Mao, C., Lu, J., *et al.*: 'Low cost hybrid reactive power compensator using coordination control strategies', *IET Gener. Transm. Distrib.*, 2016, **10**, pp. 1805–1814
[24] Lam, C.-S., Choi, W.H., Wong, M.C., *et al.*: 'Adaptive DC-link voltage-controlled hybrid active power filters for reactive power compensation', *IEEE Trans. Power Electron.*, 2012, **27**, pp. 1758–1772
[25] Lam, C.S., Wong, M.C., Choi, W.H., *et al.*: 'Design and performance of an adaptive low-DC-voltage-controlled LC-hybrid active power filter with a neutral inductor in three-phase four-wire power systems', *IEEE Trans. Ind. Electron.*, 2014, **61**, pp. 2635–2647
[26] Lam, C.S., Wang, L., Ho, S.I., *et al.*: 'Adaptive thyristor controlled LC-hybrid active power filter for reactive power and current harmonics compensation with switching loss reduction', *IEEE Trans. Power Electron.*, 2017, **32**, (10), pp. 7577–7590
[27] Myneni, H., Kumar, G.S., Sreenivasarao, D.: 'Adaptive dc-link voltage regulation for DSTATCOM under load variations'. Region 10 Conf. (TENCON), 2016, pp. 2909–2913
[28] Ghosh, A., Joshi, A.: 'A new approach to load balancing and power factor correction in power distribution system', *IEEE Trans. Power Deliv.*, 2000, **15**, pp. 417–422
[29] Wintrich, A., Nicolai, U., Tursky, W., *et al.*: 'Application manual power semiconductors', 2015
[30] Nicolai, U., Wintrich, A.: 'Determining switching losses of SEMIKRON IGBT modules SEMIKRON INTERNATIONAL GmbH', Nuremberg, Germany, Application Note AN 1403, 2014
[31] George, V., Mishra, M.K.: 'Design and analysis of user-defined constant switching frequency current-control-based four-leg DSTATCOM', *IEEE Trans. Power Electron.*, 2009, **24**, pp. 2148–2158
[32] Manoj Kumar, M.V., Mishra, M.K.: 'Three-leg inverter-based distribution static compensator topology for compensating unbalanced and non-linear loads', *IET Power Electron.*, 2015, **8**, pp. 2076–2084

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