Adaptive dc-link voltage regulation for DSTATCOM under load variations

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***Abstract*—A new algorithm is proposed for adaptive dc-link voltage regulation in DSTATCOM for power quality improvement. Generally, in conventional DSTATCOM operation, the dc-link voltage is maintained constant by PI controller ($i.e$, 2 times peak of PCC voltage). Because of fixed voltage, the switches of Voltage Source Inverter (VSI) are subjected to high voltage stresses during off-peak load conditions. It leads to increase in switching losses and deterioration of inverter reliability. During off-peak load, lesser value of dc-link voltage is sufficient to improve power quality. The proposed algorithm will give the reference dc-link voltage corresponding to load rating, and it is computed based on filter burden. The advantage of proposed algorithm is switching stresses reduced. The proposed algorithm is validated through detailed simulation studies.**

***Index Terms*—Adaptive dc-link voltage, DSTATCOM, power quality, voltage source inverter.**

I. Introduction

Harmonic mitigation, reactive power compensation and load balancing are the main objectives in power quality applications. Active filters are one of the solution for power quality improvement. The concept of "active power filter" was first developed by Gyugyi and Strycula in 1976 [1]. Under active filter category, DSTATCOM is one of the suitable solution in distribution system to compensate reactive power and mitigate source harmonics, in such a way that to make source currents balanced, sinusoidal and in-phase with source voltages [2].

The currents injected by voltage source inverter (VSI) of DSTATCOM, depends upon the dc-link voltage value, reference filter current generation and switching control algorithm. But, the switching and conduction losses of VSI are mainly depends on the dc-link voltage appear across the switches, switching frequency, current flow during ON and OFF condition of switches [3]. In general, DSTATCOMs are operated at a fixed dc-link voltage value [4], [5]. Because of fixed dc-link voltage, the voltage stress on semiconductor switches is high [6], it leads to increase in switching losses and deterioration of VSI reliability.

The losses during off-peak load conditions can be reduced by reducing dc-link voltage. The reduction of dc-link voltage depends upon load reactive power demand, unbalance and harmonics. In literature [7], [8], variable dc-link voltage regulation is applied to hybrid filter for reactive power compensation only. In [7], dc-link voltage calculation involves reactive powers, supplied by passive and active filters. Moreover, the calculation of dc-link voltage reference require more conversions and it leads to computational burden. The authors in [9], have proposed an adaptive dc-link voltage regulation for reactive power compensation, when load current having third harmonic current. In literature, unbalance current injection by the DSTATCOM is not considered during the evaluation of reference dc-link voltage.

In this paper, a new algorithm is proposed to compute dc-link voltage reference by considering unbalance currents and harmonics. The reference dc-link voltage is derived based upon rms values of reference filter currents. Here, unbalance, reactive power and harmonics are considered in generating the reference dc-link voltage value. The reference dc-link voltage is computed from the proposed method is sufficient to improve power quality, which will be discussed in simulation studies Section- IV. The advantaged of proposed method is reduction in dc-link voltage during off-peak loads which indirectly reduces switching stress.

II. Basic DSTATCOM Topology and Design of Parameters

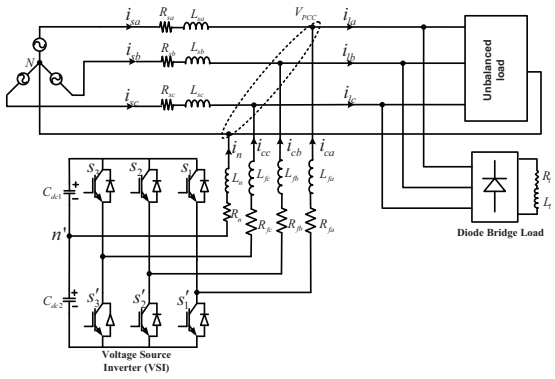

Fig. 1: Three-phase DSTATCOM topology in distribution system

The basic DSTATCOM with split capacitor topology is as shown in Fig. 1. A three-phase source is connected to three-phase unbalanced and non-linear diode bridge loads. The feeder resistances denoted as R_{sa}, R_{sb}, R_{sc} and inductances

denoted as L_{sa}, L_{sb}, L_{sc}. The three-legs of the voltage source inverter are connected to the point of common coupling (PCC) through interfacing inductors L_{fa}, L_{fb}, L_{fc} whose internal resistances are denoted as R_{fa}, R_{fb}, R_{fc}. The mid point (n') of split capacitor is connected to the neutral point (N) of the three-phase system. The DSTATCOM parameters are explained below.

A. Fixed dc-link voltage reference $(V_{dc,ref})$

The selection of dc-link voltage reference plays a very important role in design parameters and compensation performance of DSTATCOM. The reference dc-link voltage is taken as fixed value of 2 times peak of PCC voltage. $i.e.$,

$$V_{dc,ref} = 2\ (V_{pcc})_{peak} \tag{1}$$

$$(V_{pcc})_{peak} = \frac{\sqrt{2}V_{LL}}{\sqrt{3}m}. \tag{2}$$

Where, V_{dc} is dc-link voltage, V_{pcc} is voltage at Point of Common Coupling (PCC), V_{LL} is line-to-line voltage and m is modulation index [10].

B. DC-link capacitors (C_{dc1}, C_{dc2})

The dc-link capacitor (C_{dc1}, C_{dc2}) values are derived from maximum reactive power that can be compensate by DSTATCOM and energy storage capacity of dc-link capacitors. The dc-link capacitor values are calculated from

$$C_{dc1} = C_{dc2} = \frac{2pQT}{(1.8V_m)^2 - (1.6V_m)^2} \tag{3}$$

where, C_{dc1}, C_{dc2} are dc-link capacitors, V_m is peak of PCC voltage, Q is maximum reactive power that can be supplied by DSTATCOM for load demand, p is number of cycles required during dynamic load variations and T is time period

The interfacing inductance of DSTATCOM is designed from [11]. The hysteresis current controller is applied for gate pulses generation because of its simplicity, outstanding robustness with minimum tracking error [12].

The DSTATCOM with design parameters explained above is used in conventional method and the dc-link voltage is maintained constant by PI controller. It is having disadvantages of continuous high voltage switching stresses and increase of inverter switching losses during off-peak load conditions and it leads to deterioration of inverter reliability. These disadvantages are reduced by proposed adaptive dc-link voltage method, which is explained in Section-III.

III. Proposed Adaptive dc-link Voltage Reference Calculation under Load Variations

The operation of DSTATCOM is explained by single line diagram as shown in Fig. 2, in which reference filter currents are generated by instantaneous symmetrical component theory [13]. The gate pulses to inverter are generated based on hysteresis current controller depending upon error and hysteresis band (h) [14]. Here, error is difference between reference filter current and the actual filter current. The calculation of variable

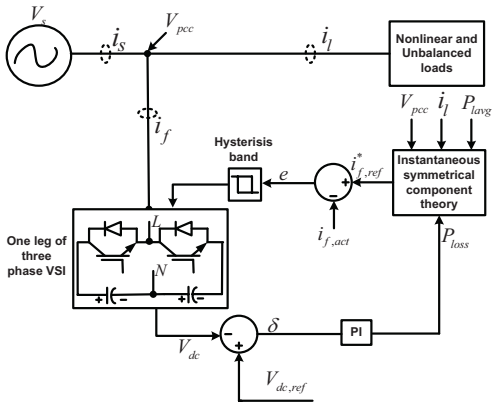

Fig. 2: Single line diagram of DSTATCOM

dc-link voltage reference, $V_{dc,ref}$ in the proposed method is explained as below.

Basically, when DSTATCOM is connected at PCC point without applying gate signals, the two dc-link capacitors are charged to peak of PCC voltage through an anti-parallel diodes of IGBT switches. From the above statement, the charged voltage is termed as minimum dc-link voltage $(V_{dc,min})$, therefore $V_{dc,min} = (V_{pcc})_{peak}$. The available reactive power supplied by DSTATCOM to load with respect to $V_{dc,min}$ is

$$Q_f = \frac{[V_{dc,min}]^2}{X}. \tag{4}$$

Where, X is equivalent impedance.

The filter current (rms) corresponding to reactive power (Q_f) and minimum dc-link voltage $(V_{dc,min})$ is termed as minimum filter current, $I_{f,min}$. The minimum dc-link voltage is sufficient to improve power quality, if the reactive power compensated by DSTATCOM is within the specified limits, $(i.e.\ 0 < Q < Q_f)$. But, the minimum dc-link voltage $(V_{dc,min})$ is not sufficient to compensate highly unbalance and more reactive power. In order to compensate highly unbalance and more reactive power, dc-link voltage is to be increased. The increased value of dc-link voltage is computed by the proposed adaptive dc-link voltage method, which as follows.

$$V_{dc,ref} = V_{dc,min} + \Big(\frac{x}{I_{f,min}}\Big)V_{dc,min}. \tag{5}$$

where, x is the difference between the reference filter current and minimum reference filter current for load variation. In the proposed approach unbalance and harmonics are included in the adaptive dc-link voltage reference calculation by means of reference filter current obtained from instantaneous symmetrical component theory. The dc-link voltage is to be increased up to a maximum value of 2 times PCC voltage, $i.e.\ (V_{dc,ref})_{max} = 2(V_{pcc})_{peak}$.

Flow chart for, the adaptive dc-link voltage reference generation is shown in Fig. 3. First, initialize $V_{dc,min}$ and $I_{f,min}$

corresponding to specified reactive power. During load variations, the reference filter current is varied, so compute the difference between reference filter current, I_f and minimum reference filter current, $I_{f,min}$.

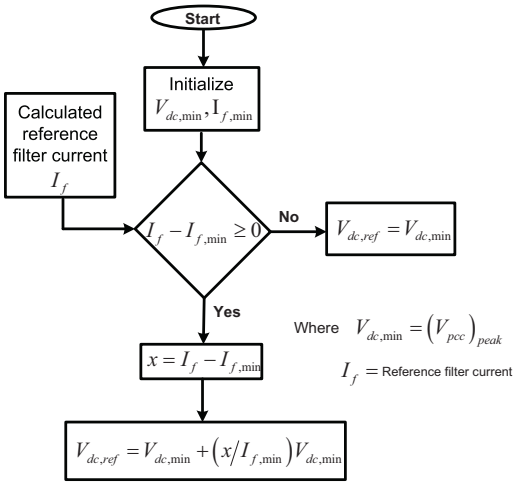

Fig. 3: Flow chart for the adaptive dc-link voltage

If the difference is positive then the new $V_{dc,ref}$ is computed from equation (5), otherwise minimum dc-link voltage $V_{dc,min}$ is considered as reference dc-link voltage. Thus, the switching losses will be reduced with the reduced dc-link voltage during off-peak load conditions and is explained below.

The switching losses of voltage source inverter are classified as turn-on and turn-off losses. The total switching losses are computed from following equation,

$$P_{loss} = V_{cc} I_{cm} f_{sw} \left(t_{r-on} + t_{f-off} \right). \quad (6)$$

Where, V_{cc} is collector voltage nothing but dc-link voltage, I_{cm} is rated collector current equal to filter current, f_{sw} is switching frequency, t_{r-on} and t_{f-off} are current rise time and fall time respectively. It is observed from equation (6), that the switching losses are proportional to dc-link voltage. So, the reduction of dc-link voltage by proposed algorithm leads to reduction in the switching losses of the voltage source inverter.

IV. Simulation Studies

The simulation parameters are given in Table. I. The simulation studies with fixed dc-link voltage and adaptive dc-link voltage reference regulation are considered to show the performance.

A. Fixed dc-link voltage reference regulation, (i.e, $V_{dc,ref} = 2(V_{pcc})_{peak}$).

Two types of loads (Nonlinear and linear unbalance) are considered for simulation studies with constant dc-link voltage regulation method. The source voltage applied is 254 V phase to phase rms, because of impedance drop the PCC voltage is 348 V peak. For both load conditions, the load currents, filter currents, source currents and dc-link voltages are shown

TABLE I: SIMULATION PARAMETERS

System Parameters		Value
Supply voltage		440 V rms (L-L)
Supply frequency		50 Hz
Source impedance (R_s, L_s)		1 Ω, 0.1 mH
Interfacing inductor (L_f)		12 mH
DC-link capacitance and maximum voltage		1400 μF, 696 V
Load - 1	Diode bridge load (3-ϕ)	(170 + j 20) Ω
	$R-L$ loads (Ω)	26 + j 6.3 , 34 + j 12.5 , 60 + j 18.4
Load - 2	Diode bridge load (3-ϕ)	(170 + j 20) Ω
	$R-L$ loads (Ω)	11 + j 3.4 , 17 + j 6.5 , 30 + j 9.2

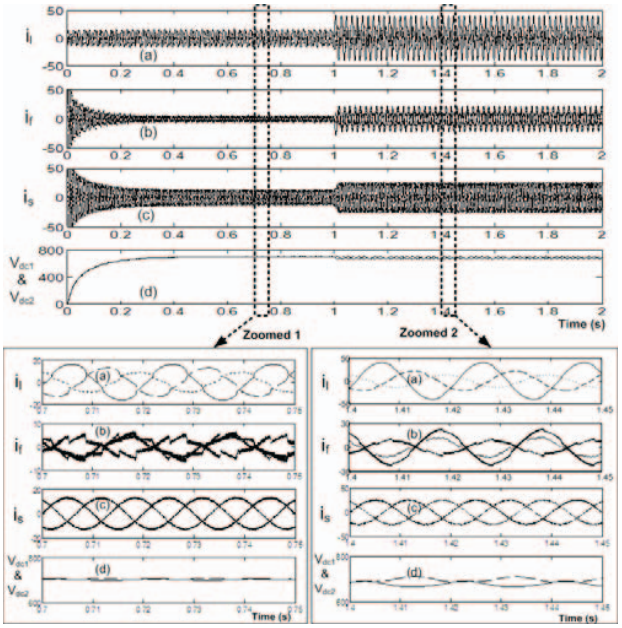

Fig. 4: Fixed dc-link voltage reference method (a) load currents (i_l), (b) filter currents (i_f), (c) source currents (i_s) and (d) dc-link voltages (V_{dc1}, V_{dc2})

in Fig. 4(a)-(d) respectively. It is observed from zoomed-1 and zoomed-2 of Fig. 4, that the source currents are perfect balanced and sinusoidal. In conventional method, the dc-link voltages are maintained 2 times peak of PCC voltage, i.e. 696 V as shown in Fig. 4(d). The dc-link voltages are maintained constant for any load (load-1 or load-2) in fixed dc-link voltage regulation method, because of this during off-peak load conditions, the switching losses are increased.

B. Proposed adaptive dc-link voltage reference regulation.

To show the effectiveness of the proposed method two loads are considered, load - 1 from $t = 0$ s to $t = 1$ s and load - 2 from $t = 1$ s to $t = 2$ s. The rms PCC voltages, load currents, filter currents, source currents and dc-link voltages are shown in Fig. 5(a)-(e) respectively. During load - 1, minimum dc-link voltage ($V_{dc,min}$) is sufficient to improve the power quality,

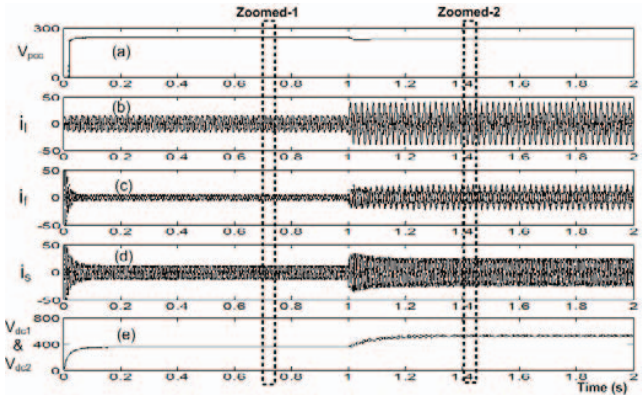

Fig. 5: Proposed adaptive dc-link voltage reference method (a) rms PCC voltage (V_{pcc}), (b) load currents (i_l), (c) filter currents (i_f), (d) source currents (i_s) and (e) dc-link voltages (V_{dc1}, V_{dc2})

so the dc-link voltage maintained at 360 V. During load - 2, $V_{dc,min}$ is not sufficient, the proposed new algorithm compute the reference voltage as 540 V, so that the dc-link voltage maintained at 540 V as shown in Fig. 5(d). In both the load conditions, the source currents are balanced and sinusoidal as shown in Fig. 6(d) and Fig. 7(d). It is observed from Fig. 6(e) and Fig. 7(e), during load - 2 the ripple present in dc-link voltage is more than load -1, because of filter current is high. However, ripple is with in the limits. For same load conditions, the proposed adaptive dc-link voltage reference regulation method requires less dc-link voltages ($i.e.$ 360 V and 540 V) than conventional fixed dc-link voltage reference regulation method ($i.e.$ 696 V).

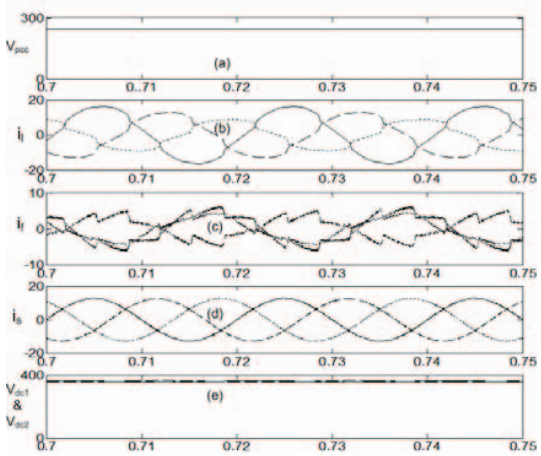

Fig. 6: Zoomed-1 part of Fig. 5.

The dc-link voltages for load -1 and load -2 in conventional and proposed method are mentioned in Table. II. The reduction of dc-link voltage magnitude reduces switching stresses and losses, and it leads to increases of inverter reliability.

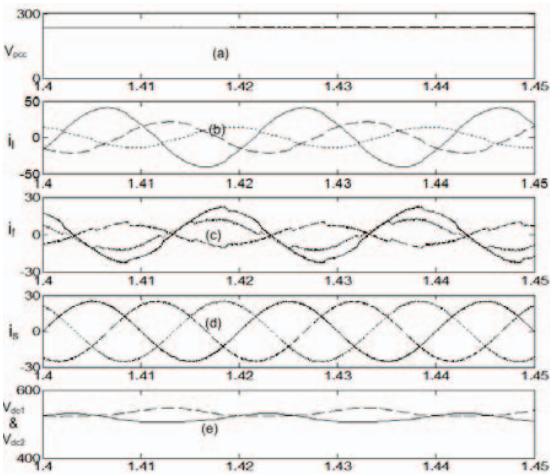

Fig. 7: Zoomed-2 part of Fig. 5.

TABLE II: DC-LINK VOLTAGES

Loads \ dc-link voltage	In conventional method	In proposed method
Load - 1	696 V	360 V
Load - 2	696 V	540 V

V. Conclusion

A new algorithm is proposed for adaptive dc-link voltage regulation in DSTATCOM for power quality improvement, without compromising its compensation capability. The advantage of the proposed method is reduction in voltage stress across switches when compared with the fixed dc-link voltage reference during off-peak loads.

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