Improvised SVPWM Strategies for an Enhanced Performance for a Four-Level Open-End Winding Induction Motor Drive

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***Abstract*—A four-level open-end winding induction motor drive (OEWIMD) is obtained when an induction motor with open windings is fed from either side with two two-level 3-Ph voltage-source inverters (VSIs) with unequal dc-link voltages, which are in the ratio of 2:1. This drive principally suffers from two problems namely: the circulation of zero sequence current in motor phases and overcharging of the lower dc-link capacitor by its counterpart with higher dc-link voltage. It has been reported earlier, that the decoupled space vector pulse width modulation (SVPWM) control strategies avoid both of these problems. This paper proposes an improvised SVPWM scheme that achieves a better harmonic performance compared to the decoupled SVPWM scheme without altering either the power circuit configuration or the voltage ratings of the devices. The proposed PWM strategy clamps the inverter with lower dc-link voltage with an active state, while the other inverter is switched around it. It has been shown that the proposed SVPWM scheme results in an overall reduction of losses for the drive system while resulting in a considerably lower dv/dt compared to the decoupled SVPWM schemes. The four-level OEWIMD employing the proposed SVPWM scheme is simulated and is validated with experimental results.**

***Index Terms*—*dv/dt*, four-level inversion, open-end winding induction motor drive (OEWIMD), over charging, space vector pulse width modulation (SVPWM).**

I. Introduction

HIGH-POWER medium-voltage induction motor drives, which are controlled by voltage-source inverters (VSIs), are widely being used in the present day industry. The modern trend is to use multilevel inverter (MLI) configurations to realize medium-voltage VSIs [1]. Neutral point clamped (NPC), flying capacitor (FC), and cascaded H-bridge (CHB) power circuit configurations are now being used widely in applications such as motor drives, static power compensation, renewable energy conditioning, power quality improvement, uninterruptable power supply systems and the like. The most recent research in the area of MLIs and their pulse width modulation (PWM) techniques for multilevel inverters is reported in [3], [4], [5], and [6].

The NPC inverter has its own drawbacks, such as requirement of additional clamping diodes, complex implementation of PWM, and fluctuations in neutral point voltage. The FC inverter needs a large number of dc capacitors with precharging circuit and complex capacitor voltage control. The CHB inverter needs several dc voltage sources.

The dual-inverter fed OEWIMD, can be considered as an alternative approach to multilevel inversion. Compared to the above mentioned MLIs topologies, this circuit configuration offers the following advantages:

1) adequacy of conventional two- level VSIs to obtain multilevel inversion;
2) absence of neutral voltage fluctuations and clamping diodes compared to the NPC topology;
3) rich redundancy of space vector combinations, which offers a multitude of possibilities to devise PWM schemes;
4) smaller number of capacitors and simple control compared to FCMLIs;
5) fewer dc power supplies compared to the CHB configuration; and
6) capability of operating under faulted conditions [7].

The OEWIMD may offer interesting possibilities in applications such as electric vehicles (EVs), hybrid EVs [8], [9], electric ship population [10], rolling mills [11], and renewable energy systems [12], [13]. Recently, a five-level OEWIMD is proposed with a single dc-link by feeding an open-winding induction motor with two three-level NPC inverters from either side [14].

Though it is possible to implement higher number of levels with this power circuit configuration, four-level inversion seems to be an optimal proposition, as the spectral performance would not be proportional to the switching resources above four-levels [7]. This is the motivating factor to embark upon the research to improvise the four-level OEWIMD.

In the work reported in [15], a method of obtaining four-level inversion with open end winding configuration has been described, which uses unequal dc–link voltages in the ratio of 2:1, and is shown in Fig. 1.

The power circuit shown in Fig. 1 suffers from a severe shortcoming. To be able to implement the minimum-ripple

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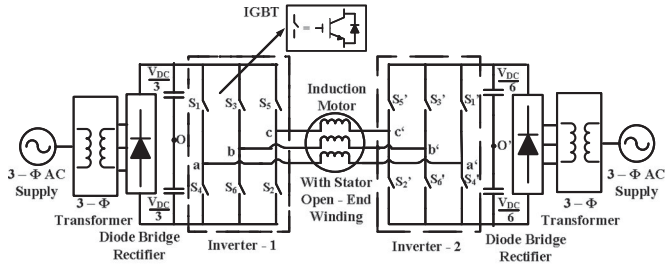

Fig. 1. Four-level OEWIMD with unequal dc-link voltages.

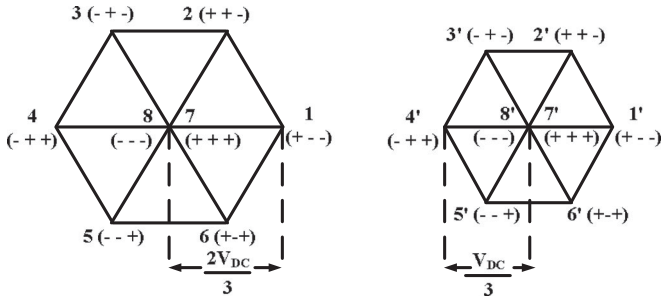

Fig. 2. Space vector locations of inverter-1 & inverter-2.

space vector PWM (SVPWM) technique [7], it is imperative to have inverter-1 clamped to a fixed state in any given sampling time period, while inverter-2 is switched. However, some space vector combinations, which are pivotal to implement this scheme (i.e., switching the vertices situated in the closest vicinity to the sample), cannot be employed [15]. When these troublesome combinations are used, the capacitor of the lower dc-link voltage, which feeds inverter-2, is overcharged by its counterpart feeding inverter-1 (which is of a higher voltage). Thus, the required dc-link ratio of 2:1 is disturbed, which distorts the motor-phase voltages and currents rendering the circuit unusable.

To circumvent this problem, the work reported in [15] employs the decoupled SVPWM technique, which proposes to resolve the overall reference voltage vector of the dual-inverter system into two antiphased components, which are in the ratio of 2:1. These components are then individually synthesized by the respective inverters. Two versions of the decoupled SVPWM technique are reported in [15], namely: the equal duty scheme and the proportional duty scheme. It has been shown that both of these PWM schemes avoid the overcharging phenomenon. However, the price paid to avoid this overcharging is excessive switching, as both inverters are switched. The switching power loss is therefore higher with both of these schemes. It is shown in [15] that the latter scheme is slightly better compared to the former in this aspect. The other disadvantages include a high dv/dt in the output voltage waveform and an inferior spectral performance.

A new circuit topology for a four-level OEWIMD was proposed in [17] to solve the dual problems of capacitor overcharging and zero-sequence current suppression. In this circuit, a rectifier-inverter set, operating with lower dc-link voltage is nested within the main dc-link of higher voltage, which feeds an outer inverter. However, this power circuit needs three isolated dc power supplies, while the power circuit, shown in Fig. 1, needs only two. Another power circuit configuration is reported in [16], in which the overall dc-link utilization is further increased. This circuit needs an overall dc-link voltage of 0.66 p.u. compared to the one shown in Fig. 1. However, this circuit has a restricted applicability in that, it is suitable to feed open-winded induction motors having "6n" number of poles only ($n = 1, 2 \ldots$) [16]. This survey of the literature indicates that the new circuit topologies reported in [16] and [17] also suffer from their own shortcomings and none of the four-level open-end winding induction motor (OEWIM) drives reported so far is ideal. This is the motivating factor to explore if the circuit shown Fig. 1 possesses any unexplored aspects.

This paper suggests simple improvisations in the SVPWM techniques to enhance the performance of the four-level OEWIM, shown in Fig. 1. It is shown that clamping inverter-2 (the one operating with lower dc-link voltage) and switching inverter-1 (the one operating with higher dc-link voltage) would yield considerably better results compared to both of the decoupled SVPWM strategies reported in [15]. Various indices of performance such as total harmonic distortion (THD) in voltage, weighted THD (WTHD), power losses in the dual inverter system (comprising of switching and conduction losses) with the proposed SVPWM technique are simulated and compared with the decoupled SVPWM techniques presented in [15]. Simulation and experimental results show that the proposed SVPWM technique, while avoiding the overcharging of the capacitor corresponding to the lower Voltage dc link, results in a better performance compared to both of the decoupled SVPWM techniques.

II. Four-Level OEWIMD

The power circuit configuration of the OEWIMD described in [15] is shown in Fig. 1, wherein two unequal dc sources, which are in the ratio of 2:1 feed an OEWIM from either side. Inverter-1 is fed with a dc-link voltage of $2\,V_{\rm DC}/3$, whereas inverter-2 is fed with a dc-link voltage of $V_{\rm DC}/3$. The states of inverter-1 and inverter-2 are numbered 1 to 8 and 1' to 8', respectively, as shown in Fig. 2.

The resultant space vector diagram of the dual-inverter system with 64(8×8) space vector combinations, spread over 37 locations with 54 sectors is shown in Fig. 3.

The pole voltages of inverter-1 are denoted as $v_{\rm ao}$, $v_{\rm bo}$, and $v_{\rm co}$. The pole voltages for inverter-2 are denoted as $v_{a'o'}$, $v_{b'o'}$, and $v_{c'o'}$. The pole voltage of Inverter-1 $(v_{\rm ao})$ assumes one of the two possible values amongst $V_{\rm DC}/3$ and $-V_{\rm DC}/3$. Similarly, the pole voltage of Inverter-2 $(v_{a'o'})$ toggle between $V_{\rm DC}/6$ and $-V_{\rm DC}/6$. As one might expect the difference of these pole voltages take four values [15]. The difference of pole voltages $(v_{\rm ao} - v_{a'o'})$, $(v_{\rm bo} - v_{b'o'})$, and $(v_{\rm co} - v_{c'o'})$, assuming that the points 'o' and 'o'' are connected together (see Fig. 1), do not add to zero, indicating that the existence of zero sequence voltage in the motor phases. This zero-sequence voltage tries to circulate a zero-sequence current in the motor phase windings. The zero-sequence components flowing through the motor phase windings are cophasal, as they are caused by the components of triplen order. Owing to the

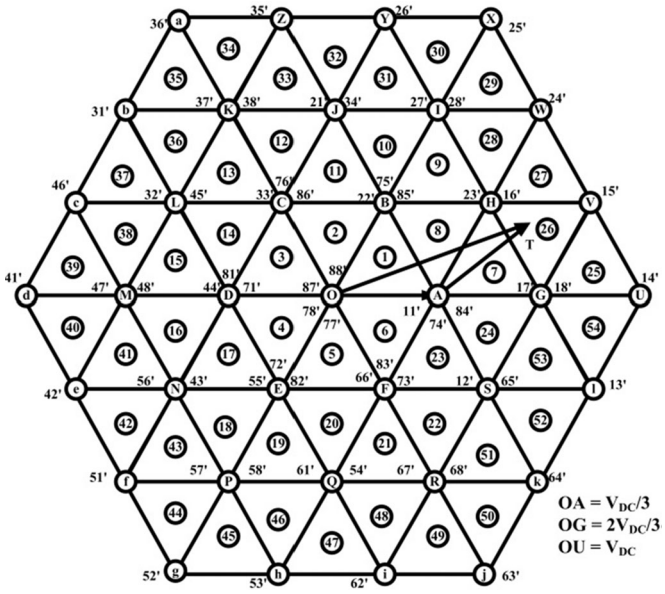

Fig. 3. Space vector combinations of dual inverter system.

electrical isolation of the constituent inverters, there exists no return path for the zero-sequence currents to flow in the motor phases. Thus, the zero-sequence currents are prevented in the motor phases.

The difference of pole voltages is given by

$$\Delta v_{aa'} = v_{ao} - v_{a'o'} \tag{1}$$

$$\Delta v_{bb'} = v_{bo} - v_{b'o'} \tag{2}$$

$$\Delta v_{cc'} = v_{co} - v_{c'o'}. \tag{3}$$

Zero sequence voltages are defined as

$$v_z = \frac{1}{3}\left[\Delta v_{aa'} + \Delta v_{bb'} + \Delta v_{cc'}\right]. \tag{4}$$

The phase voltages of the OEWIM for an isolated power supply is determined by assuming the 'o' and 'o'' points of dual inverter drive are shorted and their expressions are given as

$$v_{aa'} = \Delta v_{aa'} - v_z. \tag{5}$$

From (5), the OEWIM phase voltage in terms of inverter pole voltages can be written as

$$v_{aa'} = \frac{2}{3}\left(\Delta v_{aa'}\right) - \frac{1}{3}\left[\left(\Delta v_{bb'}\right) + \left(\Delta v_{cc'}\right)\right]. \tag{6}$$

III. Principle of Improvised SVPWM Strategy

In the PWM strategy reported in [15], both inverters are switched with antiphased reference vectors, which are in the ratio of 2:1. In contrast, the proposed PWM scheme uses inverter-2 as the clamping inverter, which provides a vectored offset. Inverter-1 is switched around this vectored offset, so that the reference voltage vector for the dual-inverter scheme is produced. Admittedly, such a method would not result in the switching of nearest vectors situated around the sample. However, it is shown in this paper that this simple alteration considerably improves the performance of the OEWIMD compared to the decoupled SVPWM techniques proposed in [15].

The proposed PWM scheme can be explained with the help of Fig. 3, which shows a core hexagon ABCDEF, centered around O. Fig. 3 also shows six more hexagons, termed subhexagons, which are OBHGSF, OCJIHA, ODLKJB, OENMLC, OFQPND, and OASRQE, respectively, centered around the so-called subhexagonal centers A,B,C,D,E, and F.

Let it be assumed that the reference voltage space vector ($\mathbf{v}_{sr}$) **OT**, located in sector 26 (see Fig. 3), is to be synthesized by the dual-inverter system shown in Fig. 1. The overall dc-link voltage (V_{DC}) is given by the vector **OU** (see Fig. 3). The modulation index m_a is defined as

$$m_a = \frac{\mathbf{OT}}{\mathbf{OU}} = \frac{|v_{sr}|}{V_{DC}}. \tag{7}$$

The dual-inverter system is so scaled that the rated frequency (50 Hz) and rated line voltage (400 V, line–line) are delivered at the limit of liner modulation, which is $(\sqrt{3}/2)$ with the SVPWM scheme. With this scaling, the frequency of the fundamental component of the dual inverter system at a modulation index of m_a would become

$$f_1 = \frac{m_a}{\sqrt{3}/2} \times 50. \tag{8}$$

Further, the reference phase voltages, which constitute the reference voltage space vector of the dual-inverter system, are sampled 42 times per one cycle irrespective of the frequency. This results in seven samples per sector. In order to obtain waveform symmetries, samples at sector boundaries are avoided [15]. The angle between successive samples is 8.57° (i.e. , $360^\circ/42$). The sampling time period is given as

$$T_s = \frac{1}{f_1 \times 42}. \tag{9}$$

Now the reference vector **OT** can be resolved into two components **OA** and **AT** (see Fig. 3)**,** which, respectively, constitute the biasing and switching vectors. The column vectors corresponding to the instantaneous phase reference voltages of vectors **OT** and **AT** are, respectively, given by $[v_a{}^* \; v_b{}^* \; v_c{}^*]^T$ and $[v_a \; v_b \; v_c]^T$. With an appropriate coordinate transformation it can be shown that:

$$\begin{aligned}&[v_a \quad v_b \quad v_c\ ]^T \\ &= I_3\left[v_a^* \quad v_b^* \quad v_c^*\right]^T + \frac{2V_{dc}}{9}\begin{bmatrix} -\cos\left((m-1)\times\pi/3\right) \\ \cos\left(m\pi/3\right) \\ \cos\left((m-2)\times\pi/3\right)\end{bmatrix}\end{aligned} \tag{10}$$

where $I_3 = 3 \times 3$ unity diagonal matrix, $m = 1, 2 \ldots, 6$ corresponding to the subhexagonal centers A, B, C, D, E, and F (see Fig. 3).

It can be so arranged that the vector **OA** is output by inverter-2 in a given sampling time interval. The vector **AT** is synthesized, in the average sense with inverter-1 by switching amongst the vertices **A**, **U,** and **W** (see Fig. 3). This would clamp inverter-2 at the state 4' $(-++)$ during the sampling time period, whereas

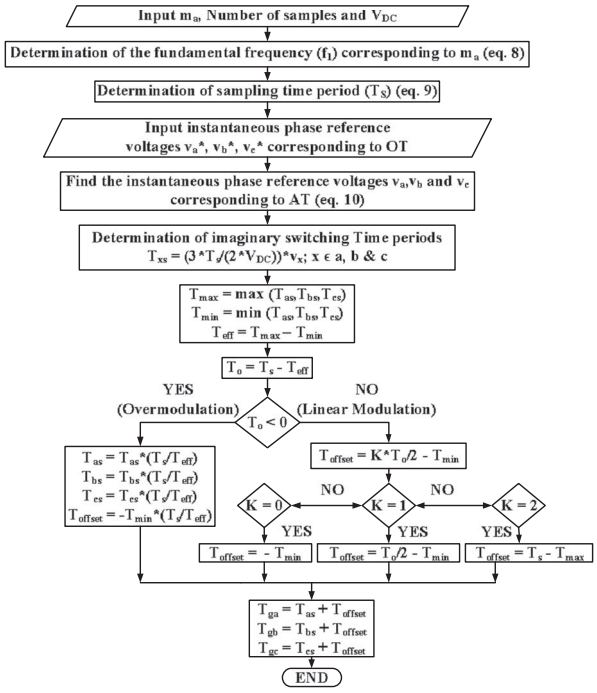

Fig. 4. Flowchart of proposed SVPWM strategy.

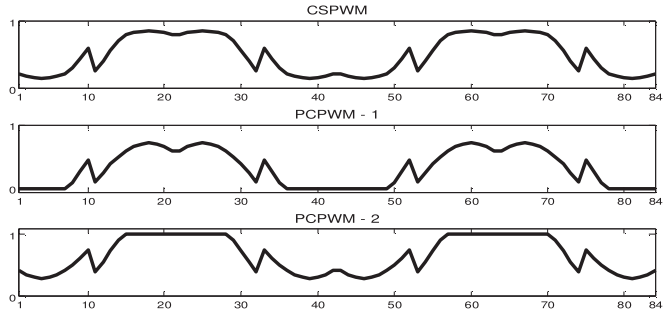

Fig. 5. Modulating signals for CSPWM, PCPWM-1, and PCPWM-2.

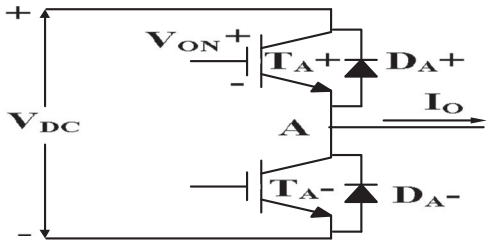

Fig. 6. Phase-A leg of inverter.

inverter-1 switches through the states 8(—), 1(+ − −), 2(++ −), and 7(+++). Thus, the space vector combinations 84', 14', 24', and 74' are sequentially deployed with this switching strategy. The sum of the time periods for which states 14' and 24' are switched is called the effective time period and is denoted by "T_{eff}". The sum of the time periods for which the vector combinations 84' and 74' are switched is denoted by the symbol "T_0". To obtain the gating pulses for the switching inverter, the switching algorithm reported in [18] is employed, which is based on the concept of imaginary switching time periods. The flowchart of the switching algorithm is presented in Fig. 4.

Depending on the distribution of the time interval "T_0" amongst the contending vector combinations 84' and 74', following three possibilities arise (see Fig. 3).

1) The time period "T_0" is equally distributed among them.
2) The combination 84' is switched for the entire time period "T_0".
3) The combination 74' is switched for the entire time period "T_0" [18].

Of these three variants, the first is known as the center spaced PWM (CSPWM) technique, while the latter two are known as the phase clamped PWM-1 (PCPWM-1) and phase clamped PWM-2 (PCPWM-2) strategies, respectively. The generalized offset time period to realize these three variants is given by the expression

$$T_{\text{offset}} = KT_o/2 - T_{\min} \tag{11}$$

where $K = 1, 0, 2$ for CSPWM, PCPWM-1, and PCPWM-2, respectively.

In other words, PCPWM-1 and PCPWM-2 are realized by placing the effective time period (T_{eff}) either at the left edge (i.e., $K = 0$) or at the right edge (i.e., $K = 2$). It may be noted that $K = 1$ corresponding to the case of CSPWM.

The modulating functions for the three variants, i.e., CSPWM, PCPWM-1, and PCPWM-2 are presented in Fig. 5.

From the traces presented in Fig. 5, it is evident that a given phase is clamped either to the positive or negative state for a time duration corresponding to 120°. It may therefore be expected that the switching losses with PCPWM-1 and PCPWM-2 would be significantly lesser than the CSPWM case.

IV. Loss Model of OEWIMD System

As explained in the earlier section, the improvised SVPWM proposed in this paper switches the so-called clamped inverter (inverter-2, Fig. 1) with the fundamental frequency, while the switching inverter (inverter-1, Fig. 1) is switched with the switching frequency (which is half of the sampling frequency). With the aid of the loss-model suggested in [19], the switching and conduction losses are estimated for the four-level dual-inverter system. However, the model developed in [19] assumes that the antiparallel diodes attached to the power semiconductor switching devices are ideal and are therefore lossless. The model developed in this paper accounts for the nonidealities of the diode and considers the conduction loss as well as the contribution of the reverse recovery current to the diode loss.

It is a well-known fact that the switching power loss in the power semiconductor devices is proportional to the switching frequency. The switching loss, which occurs during the time periods of both turn-ON and turn-OFF, is principally determined by the rise and fall time periods of the switch voltage and the switch current [2]. Fig. 6 shows the phase-A leg of one of the inverters. In this figure, T_{A^+} and , T_{A^-} are top and bottom switches, and D_{A^+} , and D_{A^-} are the respective antiparallel

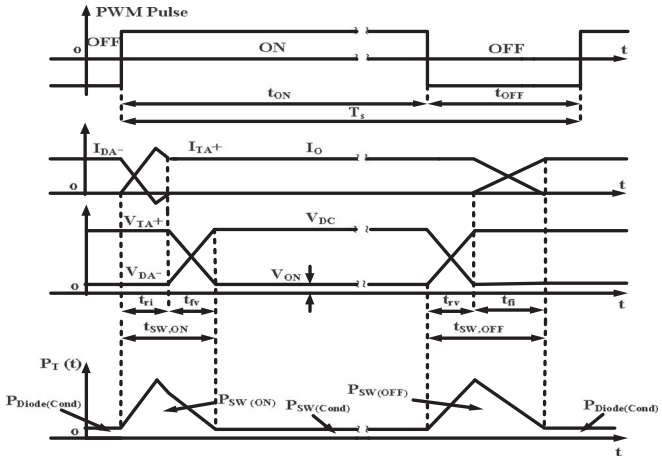

Fig. 7. Current through and Voltage drop across the switches of the inverter phase-A leg [2].

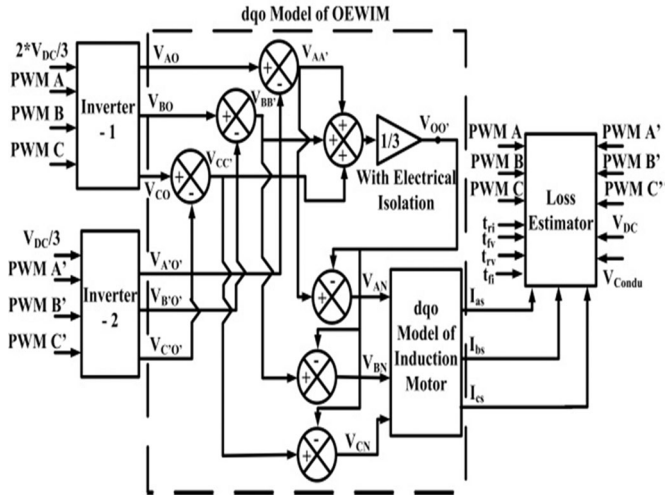

Fig. 8. Loss model of the four-level OEWIM.

diodes. The voltage across and current through the switch and the antiparallel diode are shown in Fig. 7 for $I_0 > 0$.

The switching power loss ($P_{\rm SW}$) and conduction power loss ($P_{\rm CON}$) expression are given as

$$P_{\rm SW} = \left[\frac{1}{2}\, v_{\rm SW}\, i_{\rm SW}\, (t_{\rm ri} + t_{\rm fv}) + \frac{1}{2} v_{\rm SW}\, i_{\rm SW}\, (t_{\rm rv} + t_{\rm fi})\right] \times f_s$$

$$P_{\rm SW} = \left[\frac{1}{2} v_{\rm SW}\, i_{\rm SW}\, (t_{\rm SW,ON} + t_{\rm SW,OFF})\right] \times f_S \quad (12)$$

$$P_{\rm CON,SW} = \frac{V_{\rm ON,\,Sw}\; I_{\rm ON} t_{\rm ON}}{T_S}. \quad (13)$$

From expressions (12) and (13), it is evident that the data required for the computation of inverter loss are: PWM gating signals, the instantaneous phase current, the rise and fall time of voltage and current $(t_{\rm fv},\ t_{\rm rv},\ t_{\rm fi},\ t_{\rm ri})$, the *ON-state* voltage drop $(v_{\rm ON})$, switching frequency (f_s), and blocking voltage of the switch $(v_{\rm SW})$. The detailed simulation block diagram (implemented with MATLAB/SIMULINK) for the loss estimation of dual inverter system is shown in Fig. 8. The following data are assumed to compute the switching and conduction loss in each device: $t_{\rm fv} = 1\ \mu$s, $t_{\rm rv} = 2\ \mu$s, $t_{\rm fi} = 4\ \mu$s, $t_{\rm ri} = 2\ \mu$s, and $v_{\rm ON} = 1$ V. To facilitate a fair comparison, these data are kept the same for all the five PWM schemes.

As mentioned in the earlier section, the performance of the four-level OEWIMD incorporating the PWM scheme proposed in this paper is compared with that of the one employing the decoupled SVPWM techniques proposed in [15]. The comparison is in terms of:

1) switching losses;
2) conduction losses;
3) THD in motor phase voltage; and
4) the WTHD,

which is a measure of the harmonic distortion in the motor current.

The parameters of the OEWIM, employed for the computation of the current, are presented in Appendix I.

V. Simulation & Experimental Results

The four-level OEWIMD, shown in Fig. 1, with the proposed SVPWM scheme is simulated using MATLAB and is implemented experimentally with *dSPACE-1104* system. The drive is operated with V/Hz control in open-loop and its performance is compared with the decoupled SVPWM techniques. The dc-link voltages used in the present work are 200 V for inverter-1 and 100 V for inverter-2, respectively. In other words, the effective dc-link voltage is equal to 300 V.

The four-level OEWIMD could be operated at various modulation indices covering the entire speed range. When, the modulation index $m_{\rm a} \le 0.33$, the sample is situated within the core hexagon ABCDEF (see Fig. 3). It is obvious that one does not need both inverters to synthesize the sample in this case. Hence only inverter-2 is switched, clamping inverter-1 to a null state (see Fig. 1).

In the interest of brevity, simulation and experimental results are presented only at a modulation index of 0.7 and the case of over modulation. As mentioned earlier, the fundamental frequency varies linearly with respect to the modulation index up to 0.866. Above this limit, the dual-inverter system operates in the region of over modulation and the relation between them becomes nonlinear.

It is possible to reduce the switching loss of the dual-inverter system by clamping one of the phases of the switching inverter (i.e., inverter-1). As mentioned in Section-III, it is accomplished by a simple alteration of the offset time $T_{\rm offset}$ either to $-T_{\rm min}$ (for PCPWM-1) or $T_s - T_{\rm max}$ (for PCPWM-2). Similarly, the SVPWM technique with center spacing (wherein $T_{\rm offset} = T_o/2 - T_{\rm min}$) is referred as the CSPWM technique.

The simulated and experimental results obtained for the CSPWM are shown in Figs. 9–14. Figs. 9 and 10, respectively, show the simulated and experimentally obtained pole voltages of

Fig. 9. Simulated (top) and experimentally (bottom) obtained inverter-1 pole voltage at $m_a = 0.7$. Scale (bottom trace): *X*-axis: 10 ms/div; *Y*-axis: 50 V/div.

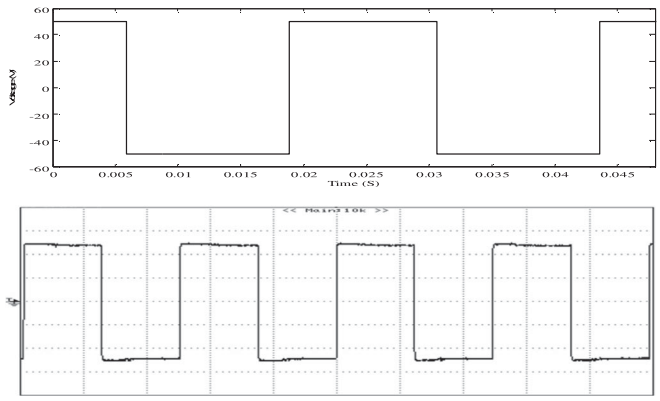

Fig. 10. Simulated (top) and experimentally (bottom) obtained inverter-2 pole voltage at $m_a = 0.7$. Scale (bottom trace): *X*-axis: 10 ms/div; *Y*-axis: 20 V/div.

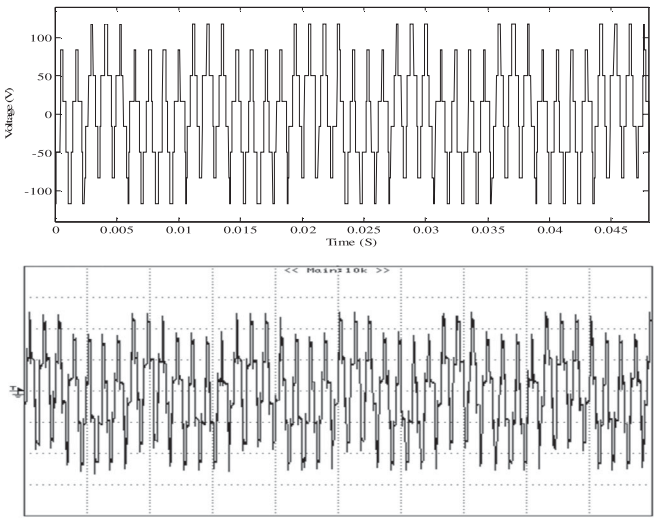

Fig. 11. Simulated (top) and experimentally (bottom) obtained common mode voltage at $m_a = 0.7$. Scale (bottom trace): *X*-axis: 5 ms/div; *Y*-axis: 50 V/div.

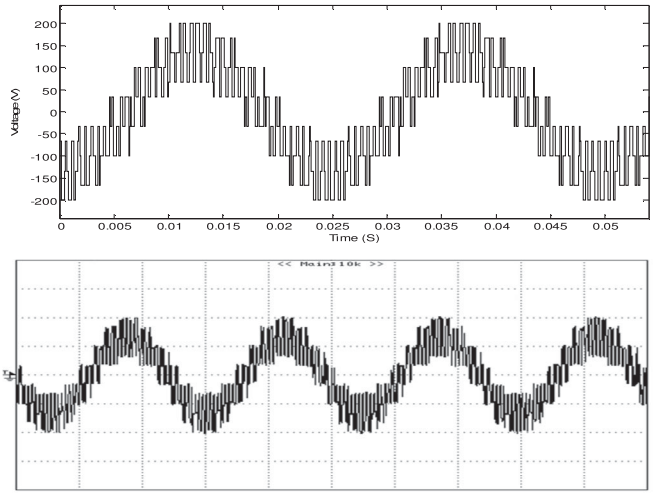

Fig. 12. Simulated (top) and experimentally (bottom) obtained phase-A voltage at $m_a = 0.7$. Scale (bottom trace): *X*-axis: 10 ms/div; *Y*-axis: 100 V/div.

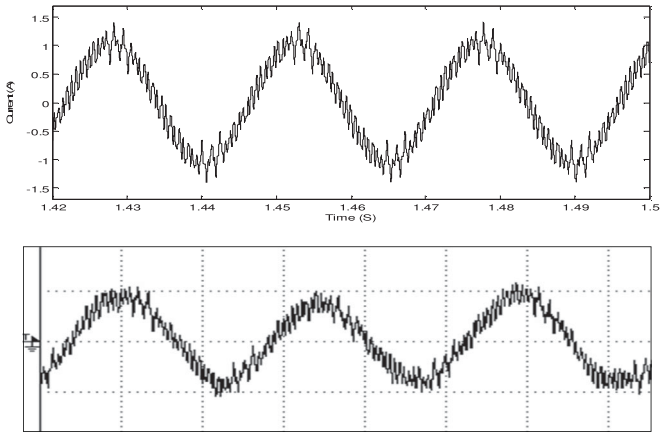

Fig. 13. Simulated (top) and experimentally (bottom) obtained phase-A current at $m_a = 0.7$. Scale (bottom trace): *X*-axis: 10 ms/div; *Y*-axis: 1 A/div.

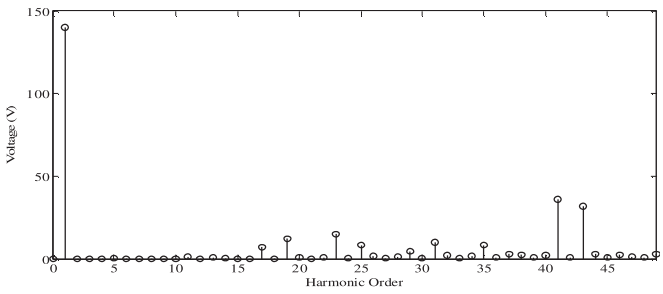

Fig. 14. FFT analysis of phase-A voltage at $m_a = 0.7$.

inverter-1 and 2 for the modulation index $m_a = 0.7$. The fundamental frequency for this modulation index is 40.4 Hz (8). The simulated and experimentally obtained zero-sequence voltage, which is dropped across the points o and o', is shown in Fig. 11. The simulated and experimental motor phase voltage (which is obtained after the subtraction of the common mode volt-

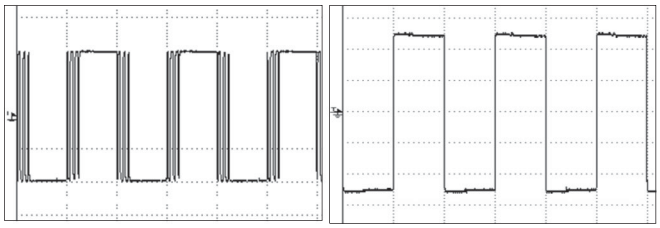

Fig. 15. Experimentally obtained pole voltages of inverter-1 (left) and inverter-2 (right) at $m_a = 1.2$. Scale: *X*-axis: 10 ms/div; *Y*-axis: 50 V/div (left trace), 20 V/div (right trace).

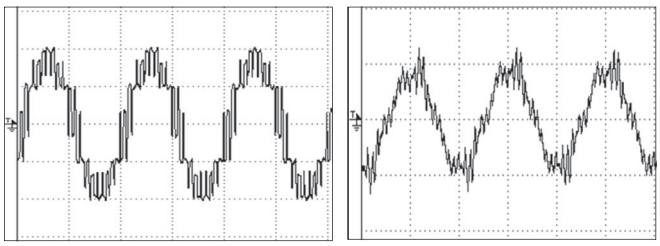

Fig. 16. Experimentally obtained phase-A voltage (left) and current (right) at $m_a = 1.2$. Scale: *X*-axis: 10 ms/div; *Y*-axis: 100 V/div (left trace), 1 A/div (right trace).

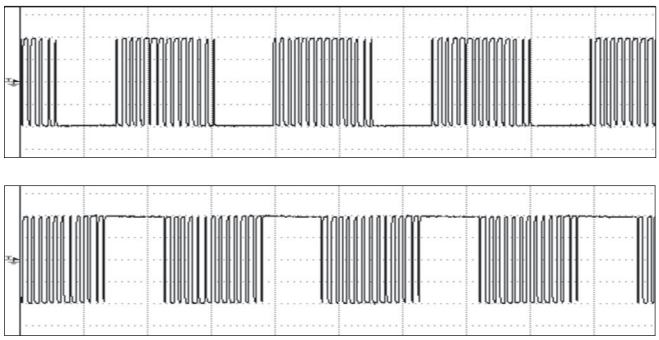

Fig. 17. Experimentally obtained pole voltage of inverter-1 for PCPWM-1 (top) and PCPWM-2 (bottom) at $m_a = 0.7$. Scale: *X*-axis: 10 ms/div; *Y*-axis: 50 V/div.

age from the difference of pole voltages) and no-load phase current of dual inverter drive system is shown in Figs. 12 and 13. Fig. 14 shows the harmonic spectrum of the motor phase voltage.

Fig. 15 shows the experimentally obtained pole voltages of inverter-1 and inverter-2 and Fig. 16 shows the experimentally obtained motor phase voltage and current waveforms for the case of over modulation (i.e., $m_a = 1.2$).

Fig. 17 presents the experimental pole voltage of inverter-1 for both PCPWM-1 (top trace) and PCPWM-2 (bottom trace). The pole voltage of inverter-2 is identical to the one obtained with CSPWM (Fig. 10 and right trace of Fig. 15). From these traces, it is evident that the pole voltages are clamped for the duration of 120° in a fundamental cycle. The clamping (i.e., reduced switching) manifests as higher ripple in the motor phase voltages as is evident from the motor phase voltage waveforms presented in Fig. 18. The corresponding motor phase currents at no-load are presented in Fig. 19. As expected, the ripple in the motor phase current increases with these two PWM schemes when compared to the case of center-spaced SVPWM.

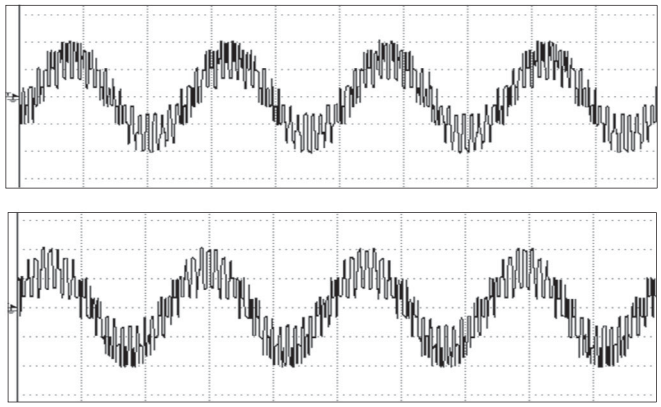

Fig. 18. Experimentally obtained phase-A voltage of PCPWM-1 (top) and PCPWM-2 (bottom) at $m_a = 0.7$. Scale: *X*-axis: 10 ms/div; *Y*-axis: 100 V/div.

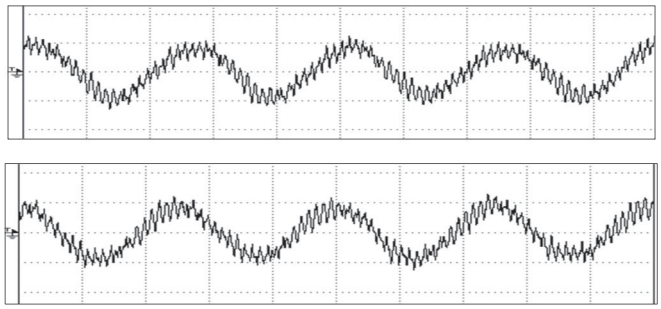

Fig. 19. Experimentally obtained phase-A current of PCPWM-1 (top) and PCPWM-2 (bottom) at $m_a = 0.7$. Scale: *X*-axis: 10 ms/div; *Y*-axis: 1 A/div.

VI. Comparative Performance Analysis of Improvised SVPWM

In this section, the performance of the three variants of the SVPWM technique proposed in this paper (namely, CSPWM, PCPWM-1, and PCPWM-2) are compared with the two variants of decoupled SVPWM technique proposed in [15], which are named as the equal duty SVPWM technique and the proportional duty SVPWM technique, respectively. For the ease of reference, these two SVPWM techniques are abbreviated as equal duty PWM (EDPWM) and proportional duty PWM (PDPWM) techniques. It should be reiterated here that all the five SVPWM techniques achieve the prevention of overcharging of the dc-link capacitor of inverter-2 (the one with lower input voltage) as well as the avoidance of the zero sequence current.

For fairness of comparison, the switching inverter in all the PWM schemes is switched with 42 samples/cycle except for the PDPWM. For PDPWM, inverter-1 (high-voltage inverter, Fig. 1) is switched with 30 samples/cycle, whereas inverter-2 (low-voltage inverter, Fig. 1) is switched with 54 samples/cycle. This keeps the total number of switching samples the same amongst the two versions of the decoupled SVPWM schemes, as suggested in [15]. To evaluate the conduction loss in the dual-inverter scheme, which depends on the motor load current, a load torque of 20 N·m is applied to the shaft of the OEWIM. This torque is about 80% of the full-load torque of the 3.7-KW motor chosen for analysis (see Appendix I). The dc-link

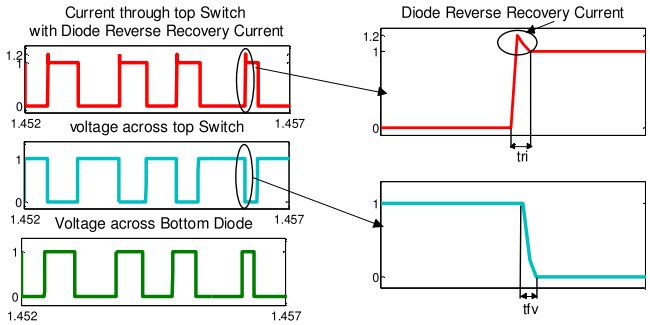

Fig. 20. Simulated voltage and current through a typical semiconductor switching device taking the diode reverse recovery current and the voltage drop across the diode.

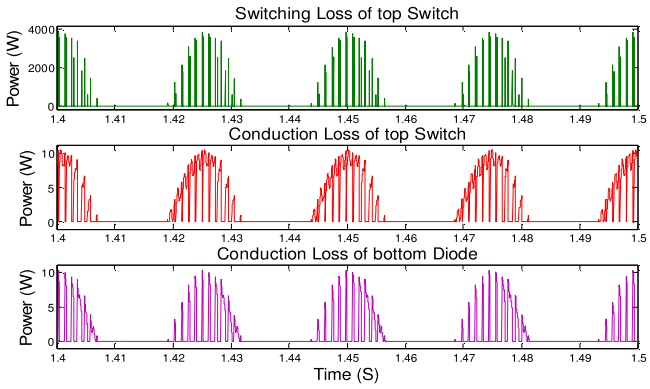

Fig. 21. Simulated switching loss and conduction loss of a typical semiconductor switch and diode.

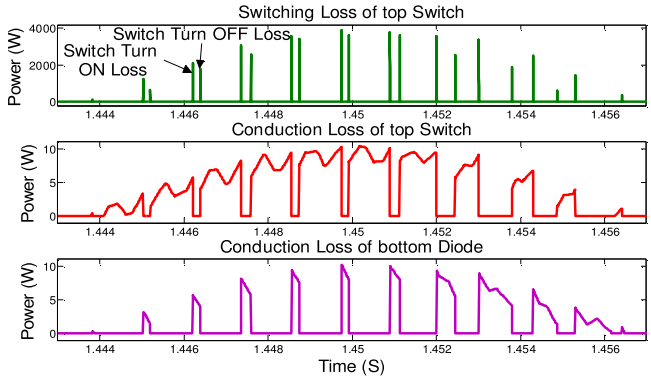

Fig. 22. Simulated switching loss and conduction loss of a typical semiconductor switch and diode (zoomed version of Fig. 21).

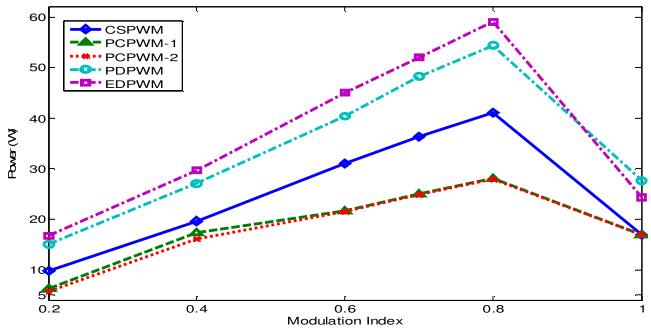

Fig. 23. Total dual inverter switching losses of 4-level OEWIMD.

voltages of the dual-inverter scheme sum to a total of 564 V, which is the total dc-link voltage needed to apply rated voltage to the motor at the brink of linear modulation (i.e., $m_a = 0.866$). As mentioned earlier, the currents obtained with the model of the OEWIMD (see Fig. 8) are used to compute the switching and conduction power losses in the semiconductor devices. It should be noted that ripple in the motor current would not only influence the motor ohmic loss, but also the conduction loss in the individual power semiconductor devices, as the motor current is routed through the devices.

As mentioned in the Section IV, the loss model used in [19] is improvised in this paper and includes the nonidealities associated with the diode. Fig. 20 shows the simulated voltage and current through a switching device during a typical sampling time period. It may be noted that the switch current (say the top switch in a leg) carries the reverse recovery current of the diode (of the bottom switch). Also, the voltage drop across the conducting diode, which was neglected in [19], is taken into account in this paper.

The top and middle traces of Fig. 21, respectively, present the simulated switching and conduction power loss in a "top" device, while the bottom trace shows the conduction loss in the antiparallel diode of the "bottom" device, in a steady-state condition. Fig. 22 presents the zoomed portion of Fig. 21 between a certain time periods (1.44–1.46 s). As one might expect, the switching power loss is highly pulsed, occurring in spurts of high intensity but of very short duration. It may also be observed that both the "top" switch and the "bottom" diode carry the ripple content of the motor phase current and are complimentary (as the sum of these two currents is equal to the motor phase current). It may further be observed that the switching power loss in the "top" device occurs at the edges of its conducting regime (top and middle traces, Fig. 22).

Fig. 23 presents the sum of the inverter-1 and inverter-2 switching losses incurred with these five versions of the SVPWM techniques. It may be noted that, in all the five cases, these losses increase uniformly till the edge of linear modulation, wherefrom all of them decrease uniformly. As the number of samples are fixed at 42/cycle irrespective of the modulation index, the frequency of the fundamental component, which in turn determines the sampling frequency and hence the switching power loss, uniformly increases till the edge of linear modulation ($m_a = 0.866$). The fundamental component is clamped to the rated frequency when $m_a \geq 0.866$, this reduces switching and hence the switching loss.

It is apparent that the three variants proposed in this paper (CSPWM, PCPWMs 1 & 2) perform better than both of the versions of decoupled SVPWM techniques proposed in [15] in this aspect. This is due to the fact that in the proposed PWM schemes, one of the inverters (inverter-2) of the dual-inverter system is clamped in any given sampling time period. As one may anticipate, amongst these three PWMs, the PCPWMs incur lesser switching loss compared to the CSPWM.

The total conduction loss is the sum of the individual conduction losses of the constituent inverters of the dual-inverter system. Again, the conduction loss incurred in each inverter is the sum of both the switch conduction losses and the diode conduction losses. The total conduction loss with all the five PWM

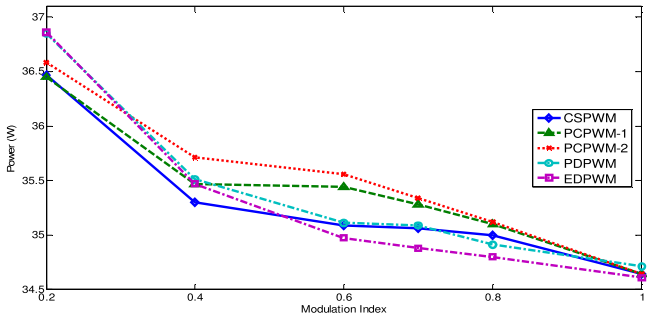

Fig. 24. Total dual inverter conduction losses of 4-level OEWIMD.

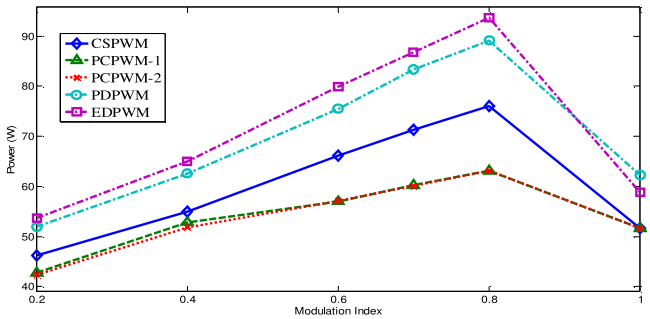

Fig. 25. Total dual inverter losses of 4-level OEWIMD.

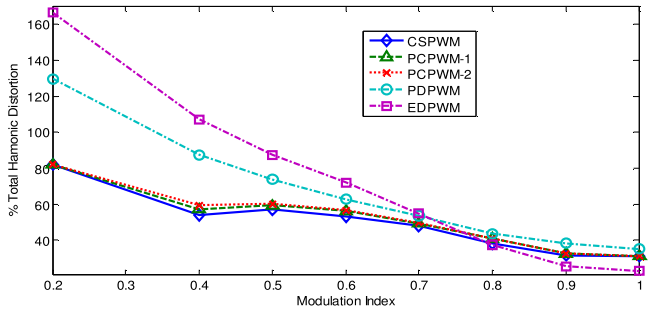

Fig. 26. Modulation index versus phase voltage THD of five PWM techniques.

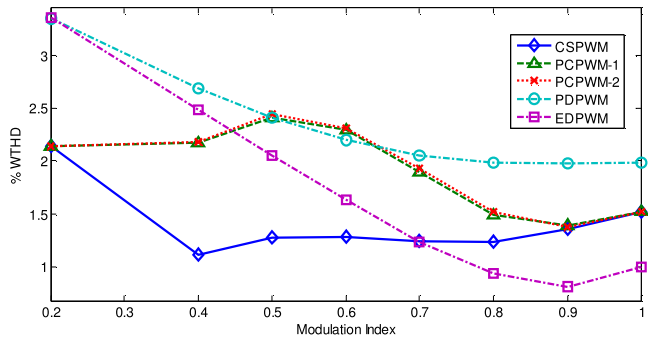

Fig. 27. Modulation index versus WTHD of five PWM techniques.

schemes is shown in Fig. 24. It may be observed that the conduction loss in the PCPWM schemes is higher compared to the CSPWM scheme, as each phase is clamped for a duration corresponding to 120°, even in the switching inverter.

It should be noted that the total conduction loss for the dual-inverter system with all the five PWM schemes is within 34.5–37 W (app.). This narrow disposition of the conduction loss is attributed to the fact that the voltage drop across a conducting diode is considered to be equal to the voltage drop across a conducting switch. Also, the conduction regimes of switches and diodes are approximately equal for all the modulation schemes when all the 12 constituent switches and their antiparallel diodes are considered at any modulation index (see Fig. 7).

The total inverter loss (the sum of switching and conduction loss) for all the PWM schemes is presented in Fig. 25. As the conduction losses of all the five PWM schemes are narrowly disposed, the differences in the total loss are determined principally by the differences in the switching power loss. Hence the trend followed by the total loss (see Fig. 25) is similar to the trend in the switching loss (see Fig. 23).

It is interesting to note from Figs. 23, 24, and 25 that amongst the three PWM schemes proposed (CSPWM, PCPWMs 1 & 2), the advantage of reducing the switching frequency outweighs the disadvantage associated with the increase of the conduction loss in the power semiconductor devices. The simulation results presented in Fig. 25 suggest that an energy efficient OEWIMD should employ the PCPWM techniques, rather than the CSPWM scheme.

The THD is a widely used measure to quantify the spectral performance of the inverter. THD in the output of the voltage is defined as

$$V_{\mathrm{THD}} = \frac{\sqrt{\sum_{n=2}^{\infty} \mathrm{v}_n^2}}{v_1} \tag{14}$$

where V_1 and V_n are the rms values of the fundamental component and nth harmonic components of the phase voltage. THD in voltage is a measure of harmonic contamination, which is normalized w.r.t. the fundamental quantity. The THD in voltage is evaluated for all the five PWM techniques. It may be noted that the PWM techniques proposed in this paper perform better than the decoupled SVPWM schemes in the lower and middle range of modulation, while the EDPWM performs slightly better in the upper range of modulation. As one may anticipate, among the PWM schemes proposed in this paper, the CSPWM performs better than the PCPWMs, as shown in Fig. 26.

The effectiveness of a modulation scheme can also be assessed by the weighted THD. It is generally reckoned that WTHD captures the performance of a PWM scheme in a better way than the THD in voltage. When an induction motor is fed by a sinusoidal voltage source, the motor draws a magnetizing current, which is given by $(V_1/\omega L_m)$. However, when the motor is supplied with a nonsinusoidal input, any harmonic current component of nth order is given by $(V_n/n\omega L_m)$. Thus, the quantity $\sum_{n\neq 1}(V_n/n\omega L_m)^2$ represents the rms value of all harmonic components put together. Thus, the WTHD represents the normalized harmonic contamination in current, with the fundamental component chosen as the base value. The WTHD is defined as

$$V_{\mathrm{WTHD}} \triangleq \frac{\sqrt{\sum_{n=2}^{\infty}\left(\frac{v_n}{n}\right)^2}}{v_1}. \tag{15}$$

Fig. 27 shows that the WTHD of all the five PWM schemes. From Fig. 27, as per the expectation, the CSPWM scheme performs better in the lower and middle range of modula-

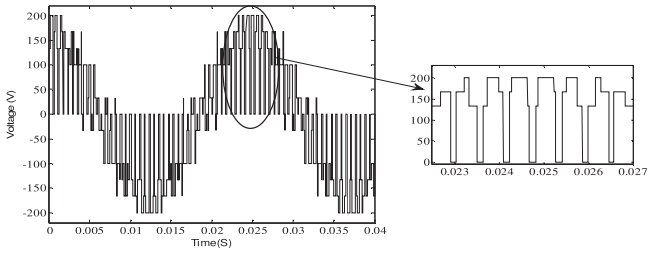

Fig. 28. Phase voltage of decoupled PWM scheme.

tion, whereas the EDPWM performs slightly better in the upper range.

From Figs. 23–27, it is apparent that SVPWM techniques proposed in this paper perform better than the decoupled SVPWM techniques proposed in [15]. There is another important advantage with the SVPWM schemes proposed in this paper vis-à-vis the decoupled SVPWM schemes. The simulated motor phase voltage waveforms with the decoupled SVPWM schemes are shown in Fig. 28, of which the central part is zoomed. It may be noted that higher voltage pulses appears across the motor phase windings. This indicates that the motor phase windings are subject to larger dv/dt. The deleterious effects associated with the application of such a large dv/dt are well documented [1]. In contrast, the proposed PWM techniques in this paper result considerably lesser dv/dt across the motor windings as is evident in Fig. 12 (CSPWM), top trace of Fig. 18 (PCPWM-1), and bottom trace of Fig. 18 (PCPWM-2).

VII. Conclusion

This paper suggested three variants of a simple SVPWM scheme to improvise the performance of a four-level OEWIMD, which is obtained by feeding an OEWIM with two two-level inverters from either side. The constituent inverters were operated with unequal dc-link voltages, which are in the ratio of 2:1. The performance of the OEWIMD employing these PWM techniques was compared with the two variants of the decoupled SVPWM strategies reported in the earlier literature. The common objective of all these five PWM strategies was to avoid the overcharging of the dc-link capacitor of the inverter operating with lower input voltage.

Using both simulation studies and experimentation, it is shown that the proposed SVPWM strategies perform better compared to the decoupled SVPWM strategies to an appreciable extent. The proposed PWM techniques resulted in lower THDs in output voltages, lower losses in the switching devices, lower overall conduction loss of the drive system, throughout the range of modulation. Also, with the proposed PWM techniques, the motor phase windings experienced considerably lower dv/dt across them. This results in the longevity of the life of insulation and lower bearing currents, which increases the life of bearings.

Appendix

Motor Parameters:

$P = 4$; $R_s = 4.215\ \Omega$; $R_{r'} = 4.185\ \Omega$; $x_{\mathrm{ls}} = x_{\mathrm{lr}'} = 5.502\ \Omega$; $X_m = 162.3\ \Omega$; $J = 0.0131\ \mathrm{kg} - \mathrm{m}^2$; $B = 0.002985\ \mathrm{N{\cdot}m{\cdot}s}$.

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Authors' photographs and biographies not available at the time of publication.