A Novel Three-Phase Seven-Level Inverter

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Abstract—**Recently, multilevel-inverters with less number of switching devices are becoming more popular due to compact size, reduced cost and higher efficiency. Though the multilevel inverter has significant advantages most of the recent works are addressed for single phase applications. Therefore, in this paper, a novel three-phase seven-level inverter is proposed with the inherent benefits of reduced switches and isolated DC sources. The proposed topology is developed with the combination of a three-level inverter and a full-bridge flying capacitor circuit for medium voltage applications. The three-level inverter part alleviates the undesired positive and negative spikes as generated by a conventional three-level inverter. The performance of the proposed seven-level inverter is studied for different modulation indices with RL load and their results are presented.**

Keywords—Flying capacitor, Three-level inverter, Multilevel inverter, Medium voltage, Pulse width modulation.

I. INTRODUCTION

In multilevel conversion the higher power rating is derived from a series of lower rating voltage sources and also stepped output voltage waveform is synthesized close to the sinusoidal wave. Recently, the multi-level inverter has become popular for large capacity power generations using renewable energy sources [1-4]. The lower rating of photovoltaic and fuel cells can be easily merged in series to extend the power and voltage ranges for grid connected applications. It also helps to handle large DC link voltages with reduced device stress and reduced harmonics for higher level medium voltage applications.

The benchmark of MLIs was started with the three basic topologies of (i) Neutral point clamped, (ii) Flying capacitor and (iii) Cascaded H-bridge inverters [5-8]. These conventional topologies shows extreme performance and well suited for medium voltage applications. However, the inherent drawbacks are variation in losses between the devices and demands more clamping diodes in NPC. Flying capacitor gives better performance for the number of levels more than 3, but the problem of capacitor voltage balancing becomes harder. It demands a separate auxiliary voltage balancing circuit or control technique. Cascaded H-bridge inverter gives higher output levels with asymmetrical voltage sources [9]. But, it requires more number of switches, driver circuits, separate isolated DC source for each H-bridge and increased control complexity for higher output levels.

Many new and hybrid topologies have been developed to address the problems of conventional topologies [10-12]. A new three-phase five-level inverter is presented by combining a three-level ANPC inverter with flying capacitor cell. A new control strategy to balance the flying capacitor voltage is also presented in [13]. An efficient closed loop controller for balancing the FC voltage during transients is given in [15]. Recently, a 3-phase 6-level inverter is proposed for medium voltage applications with the combination of two-level inverter and three-level FC inverter [16]. But it needs unequal splitting of dc-link voltages and more switching devices.

Therefore, in this paper, a new configuration of three-level inverter is used at the dc link rather than a conventional three-level inverter [17]. In a conventional three-level inverter, an unwanted negative spike occurs during positive voltage levels and positive spike during negative voltage levels. The unwanted positive spikes in the output voltage while switching between negative and zero levels has been eliminated in this topology. The concept of the proposed topology is obtained from a 5-level ANPC [13] and a five-level inverter for OEWIM drives [14]. The proposed 3-phase seven-level inverter has inherent benefits of higher output voltage levels with lower switching devices. In this topology, a three-level inverter is combined with a H-bridge FC circuit for 3-phase applications. The performance of the developed seven-level inverter is evaluated in Matlab/Simulink environment for different modulation indices.

II. PROPOSED TOPOLOGY

The schematic arrangement of the proposed seven-level inverter is shown in Fig.1. The DC-link is common for all the three phases. Each phase consists of a three-level structure connected to common DC-link and a full-bridge with FC coupled at the output of three-level structure. The operation of three-level structure and full-bridge circuit are mutually dependent to generate a required voltage level at the output.

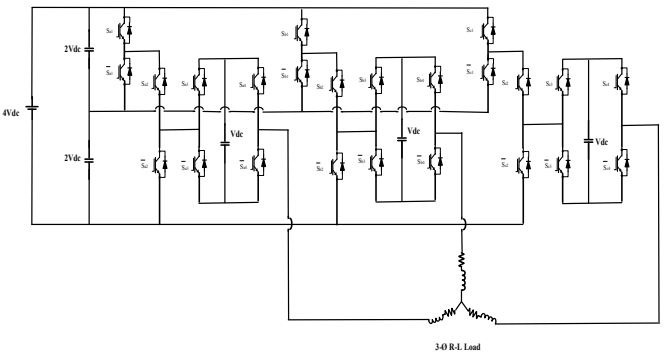

Fig.1. Proposed Topology.

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To understand the operation, a single phase diagram of the proposed seven-level inverter is shown in Fig. 2. A phase-leg of the seven-level inverter has eight switches and three capacitors, among two capacitors form the common dc-link are shared by three phase legs of inverter and the other one belongs to each phase to generate the desired seven-level output. The seven-level inverter requires equal voltage sharing among dc-link capacitors. Four switches of $S_{a3}, \overline{S}_{a3}, S_{a4}$ and $\overline{S}_{a4}$ have a lower voltage rating of V_{dc}, and three switches $S_{a1}, \overline{S}_{a1}$ and S_{a2} have a higher voltage rating of $2V_{dc}$ and only one switch $\overline{S}_{a2}$ has a voltage rating of $4V_{dc}$.

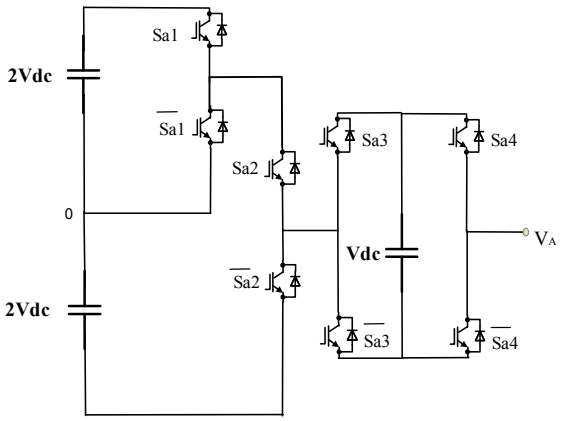


Fig.2. Single-phase diagram of the proposed seven-level inverter.

Table-I lists the nine switching states of seven-level operation with one inverter leg with the step of V_{dc}. Where "1" and "0" indicates the ON and OFF states of the switches respectively. V_{AO} is the pole voltage which is the measured potential between phase A and the neutral point. It should be noted that there are two redundant switching states in V_{dc} and $-V_{dc}$voltage levels, which affects the FC voltages differently. One switching state charges and other switching state discharges the FC according to the phase current direction. The switching states V_0, V_4 and V_8 do not affect the FC voltage since no current is flowing through the FC.

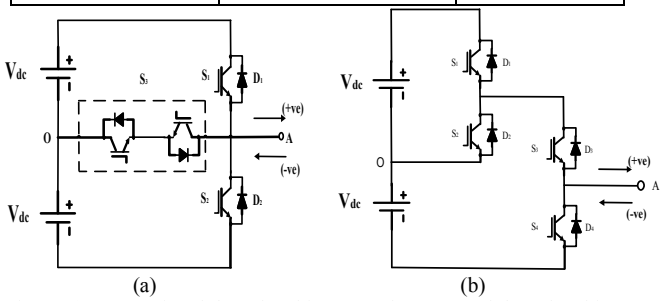
Fig. 3 shows the current directions for different operating modes of seven-level inverter. The corresponding conducting switches and inverter output voltage levels are given in Table II. It can be understand that the number of conducting switches for each level is very less. This ensures the higher efficiency of the proposed seven-level inverter.

TABLE-I SWITCHING STATES OF SEVEN-LEVEL INVERTER

Switching states	V_{AO}	S_{a1}	S_{a2}	S_{a3}	S_{a4}
V_0	0	0	1	1	1
V_1	V_{dc}	0	1	0	1
V_2	V_{dc}	1	1	1	0
V_3	$2V_{dc}$	1	1	1	1
V_4	$3V_{dc}$	1	1	0	1
V_5	$-V_{dc}$	0	1	1	0
V_6	$-V_{dc}$	0 (or)1	0	0	1
V_7	$-2V_{dc}$	0 (or)1	0	1	1
V_8	$-3V_{dc}$	0 (or)1	0	1	0

TABLE-II CONDUCTING SWITCHES AT DIFFERENT LEVELS OF OUTPUT VOLTAGE

OUTPUT VOLTAGE LEVEL (V_{AO})	CONDUCTING SWITCHES	NUMBER OF CONDUCTING SWITCHES
0	$\overline{S}_{a1}, S_{a2}, S_{a3}, S_{a4}$	4
V_{dc}	$\overline{S}_{a1}, S_{a2}, \overline{S}_{a3}, S_{a4}$	4
2 V_{dc}	$S_{a1}, S_{a2}, S_{a3}, S_{a4}$	4
3 V_{dc}	$S_{a1}, S_{a2}, \overline{S}_{a3}, S_{a4}$	4
- V_{dc}	$\overline{S}_{a1}, S_{a2}, S_{a3}, \overline{S}_{a4}$	4
-2 V_{dc}	$\overline{S}_{a2}, S_{a3}, S_{a4}$	3
-3 V_{dc}	$\overline{S}_{a2}, S_{a3}, \overline{S}_{a4}$	3



(a) (b)

Fig.4. (a) Conventional three-level inverter, (b) Proposed three-level inverter.

Moreover the performance of the proposed topology is compared with the conventional three-level inverter and a full-bridge with FC [18]. In a conventional three-level inverter shown in Fig. 4(a), when S_1 is on $V_{AO}= V_{dc}$, the load current can be either positive or negative, while switching from V_{dc} to 0, S_1 has to turn-off and after a dead band of nearly 0.4µs, S_3 is to be on. During this dead band interval when both S_1 and S_3 are off, if the load current is +ve, then it will be forced to flow through diode D_2, which results in $V_{AO}= -V_{dc}$(negative spike), which is an undesirable condition. Similarly, while switching from $-V_{dc}$ to 0, S_2 has to turn-off and after a dead band S_3 is to be on. When both S_2 and D_2 are off during dead band, if the load current is –ve, then it will be forced to flow through diode D_1, which results in $V_{AO}=+V_{dc}$(positive spike).

However, in the proposed three-level inverter shown in Fig. 4(b), when $V_{AO}=V_{dc}$, and load current is positive, S_1 and S_3 conducts when $V_{AO}=0$, D_2 and S_3 conducts for zero voltage level. While switching from V_{dc} to zero, S_1 has to be turned-off and after a dead band of 0.4µs, S_2 is to be turned on. During the dead band period even though S_2 and S_1 are off, the positive load current will flow through D_2 and S_3, since S_3 is not turned off, which can maintain the zero level during the dead band. When $V_{AO}=-V_{dc}$, and load current is negative, only S_4 conducts. When $V_{AO}=0$, D_3 and S_2 conducts. While switching from $-V_{dc}$ to zero, S_4 is to be turned off and after a dead band S_3 is to be turned on, whereas S_2 can be turned on immediately. Hence, the negative load current will flow through D_3 and S_2 maintaining the zero voltage level. This clearly shows that the undesired positive and negative spikes can be eliminated in the proposed three-level topology.

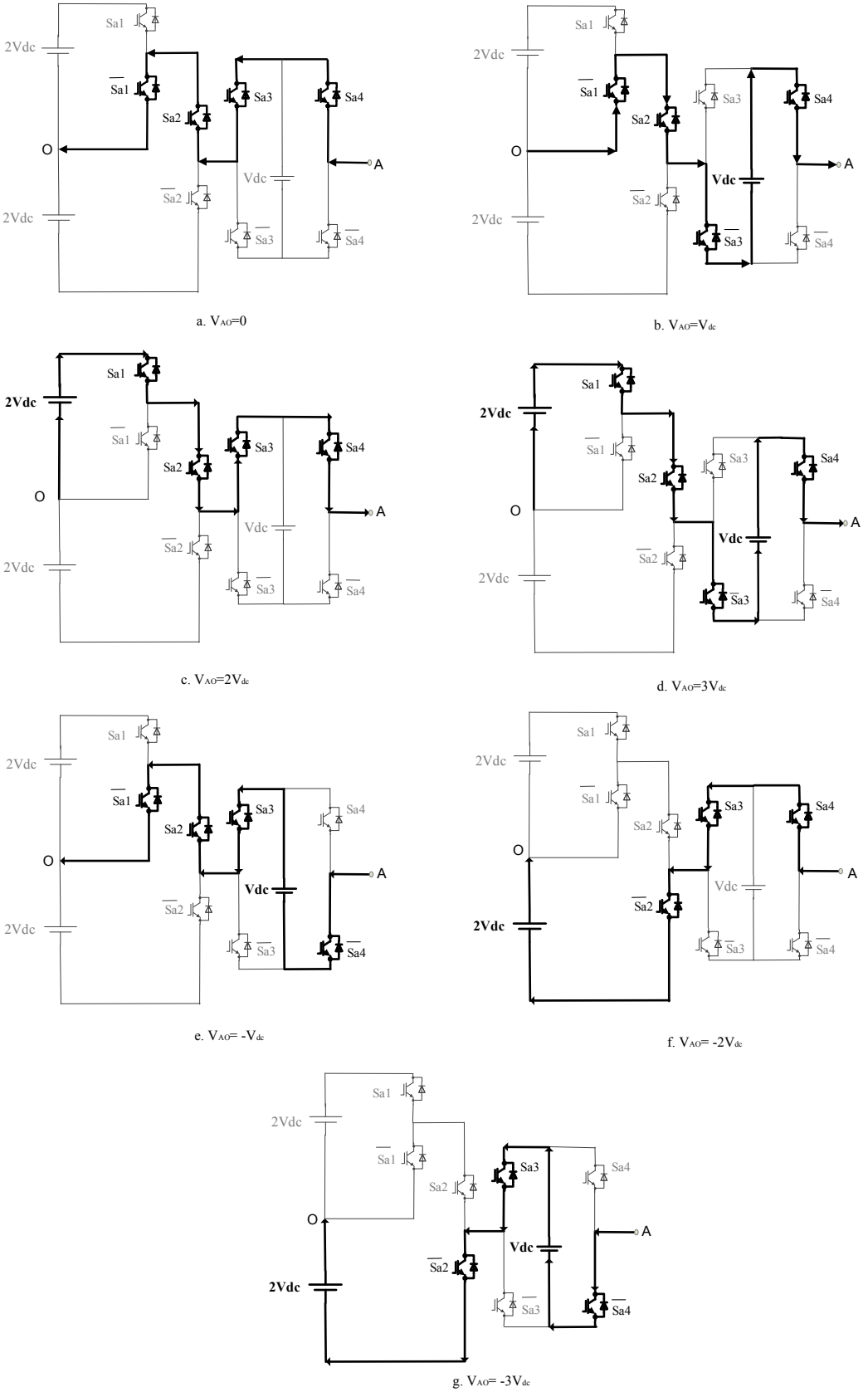
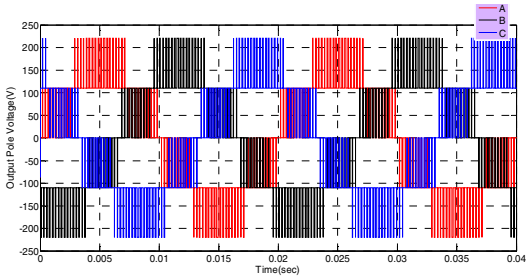


Fig.3. Operating modes of seven-level inverter (single phase only).

III. SIMULATION RESULTS

To verify the performance of the proposed 3-phase seven-level inverter a simulation work has been carried out in Matlab/Simulink environment. The system parameters are of 440 DC link voltage and 110V FC voltages are chosen to produce a desired output voltage of 400Vrms. In order to verify the results, DC sources are only considered for the study. The seven-level inverter is modulated using sine triangle level shifted-PWM technique. To show the feasibility of the proposed work a switching frequency of 4.05 kHz is considered for simulation. For any value of pure resistive load, the current direction is always from source to load, for R-L type of loads, the current also flow from load to source due to lagging nature of the load which is also called reverse current. Hence bi-directional conducting switches are required to carry the reverse current. The duration for which this reverse current flow occurs, depends on the amount of inductance in the load circuit. For R=10Ω and L=20mH, the reverse current duration in each half cycle is around 1.8ms. The proposed topology has the ability to operate at any value of load inductance. Therefore, the proposed model is tested for different modulation indices with an RL load of 10Ω and 20mH respectively. Figs. 5(a-c) & 6(a-c) shows the various inverter output results of the pole voltages, line voltages, phase voltages and current waveforms for different modulation indices of 0.45 and 0.9. Figs. 5(d) & 6(d) shows the harmonic spectrum of these synthesized inverter output phase-A voltage waveform. It has been observed that the THD value decreases from 24.57% to 12.87% for the MI value changes from 0.45 to 0.9 respectively, due to increase in output voltage levels.



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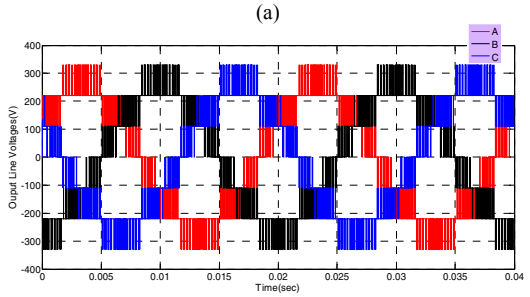

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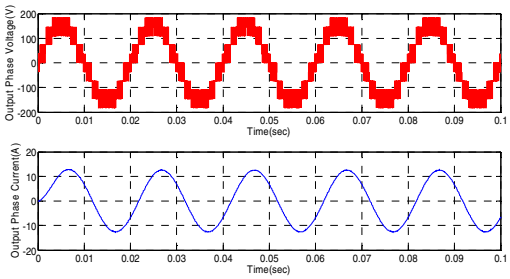

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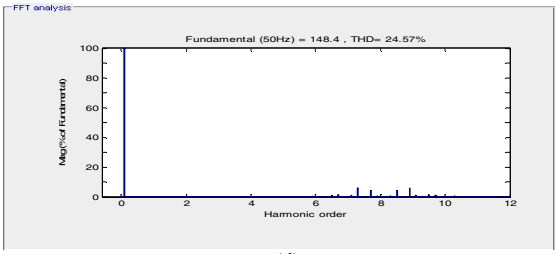
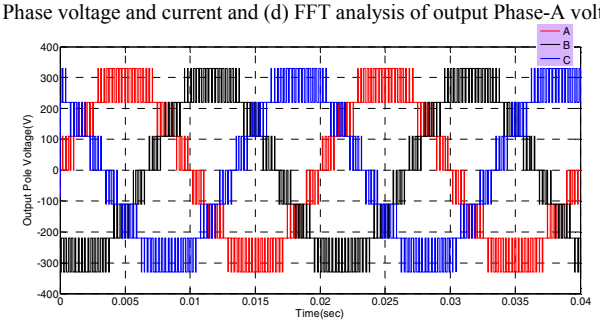


(d)

Fig.5. Simulation results for $m_a = 0.45$ (a) Pole voltages, (b) Line voltages, (c) Phase voltage and current and (d) FFT analysis of output Phase-A voltage.



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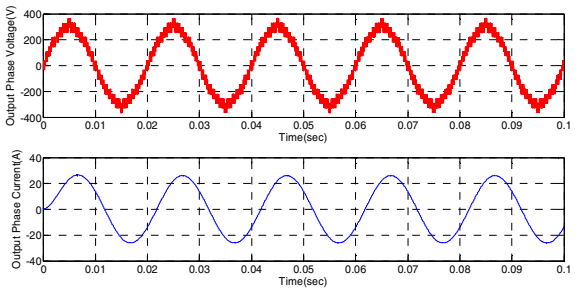

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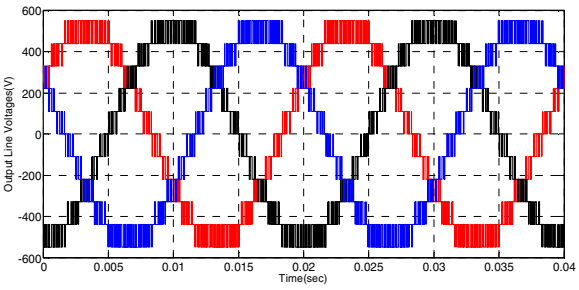

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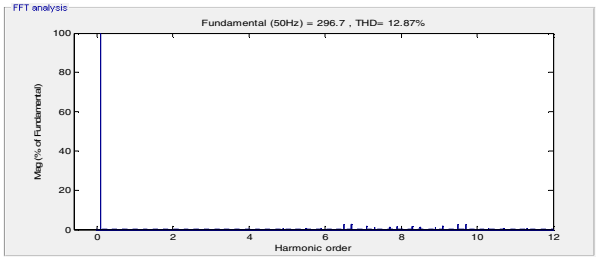

(d)

Fig.6. Simulation results for $m_a = 0.9$ (a) Pole voltages, (b) Phase voltage and current,(c) Line voltages and (d) FFT analysis of output phase-A voltage.

IV. CONCLUSION

In this paper, a novel seven-level inverter with reduced switching devices has been proposed. This model is developed with the combination of a three-level inverter and full-bridge FC circuit. The proposed circuit requires reduced component count and alleviates the issues of undesirable reverse spikes as generated by a conventional three-level inverter. The seven-level inverter is tested for different modulation indices and the corresponding results are presented. The proposed configuration can be extended for wide use of renewable based medium power applications.

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