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Reduced carrier PWM scheme with unified logical expressions for reduced switch count multilevel inverters

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Abstract: The significant reduction in switch count of symmetrical/asymmetrical reduced switch count multilevel inverters (RSC-MLI) topologies has modified the operation of inverter such that the conventional carrier-based pulse width modulation (PWM) schemes such as level-shifted PWM and phase-shifted PWM can no more realise them. To control these RSC-MLI topologies, reduced carrier PWM schemes with modified switching logic gained more prominence. These schemes involve suitable logical expressions to realise the switching states of the inverter. However, these logical expressions vary with topological arrangement and number of levels. Moreover, these schemes produce high total harmonic distortion (THD) in line-voltages. Therefore, to improve the line-voltage THD and generalise the switching logic, a modified reduced carrier PWM scheme with unified logical expressions is presented here. The proposed PWM scheme is directly valid for any topology and can be easily scalable to any number of levels in the inverters. To validate the implementation of the proposed PWM to control any RSC-MLI, experimental studies of various asymmetrical RSC-MLI topologies with the proposed PWM scheme are carried out. Further, to verify the superiority of the proposed scheme in terms of THD, complexity, scalability, and computation burden, its performance is compared with carrier-based PWM schemes reported in the literature.

1 Introduction

The demand for reducing the size of multilevel inverters (MLI) has led to a new domain of MLIs, named as reduced switch count (RSC) MLIs [1]. Depending on dc source voltage ratios, these RSC-MLIs are classified as symmetrical and asymmetrical. With asymmetrical dc source voltages, further reduction in switch count can be achieved. Several RSC-MLI topologies such as multilevel dc link (MLDCL) [2], packed U-cell (PUC) [3], cascaded bi-polar switched cells (CBSC) [4], reverse voltage (RV) [5], switched dc sources [6], basic unit MLI [7], envelope-type (E-type) [8], T-type [9–13], hybrid T-type [14, 15], series-connected switched sources (SCSS) [16], switched series parallel sources (SSPS) [17, 18], nested MLI [19], switched capacitor unit [20, 21], reduced cascaded [22–25], and various other topologies [26–28] are reported in the literature. Fig. 1 shows the circuit configuration of various single-phase 13-level asymmetrical RSC topologies such as switched dc sources, PUC, cascaded T-type, hybrid T-type, CBSC, SSPS, RV, MLDCL, and E-type.

Among the pulse width modulation (PWM) schemes reported for MLIs, carrier-based schemes such as level-shifted PWM (LSPWM) and phase-shifted PWM (PSPWM) are the simplest due to their easiness in implementation [29–31]. These PWM schemes can realise inverter switching states in which devices conducting for achieving lower levels remain in conduction at higher levels as well. This acted as a limitation of the conventional carrier-based schemes to realise RSC-MLIs, since these topologies has limited redundancies and possess the switching action where the lower level conduction devices may not remain in conduction at higher level.

In the literature, various modulation schemes are reported for controlling symmetrical and asymmetrical RSC-MLI configurations. Among them, hybrid PWM is one of the popular schemes for implementing asymmetrical cascaded topologies such as Cascade H-bridge [20, 22, 32]. This scheme can also be implemented to non-cascaded topologies such as SSPS by adding an additional H-bridge in each phase [17]. In this scheme, measurement or estimation of output voltage of the higher voltage bridge/units is necessary, to derive the reference signal for the lower voltage bridge/units. Hence, any lag or errors in the estimation or measurement will impact the output voltage. PWM schemes such as selective harmonic elimination [8] and space vector [3, 19, 26, 28] are reported for E-type, PUC, nested cell, and various three-phase RSC topologies. These switching schemes can be generalised to higher levels, but requires elusive calculations to obtain switching instants.

Switching schemes using low-frequency carrier (50 or 100 Hz) with and without logical operators are reported for various RSC MLIs such as MLDCL, CBSC, basic unit MLI, T-type, and hybrid T-type [2, 4, 7, 12, 14, 15, 20, 28]. These low-frequency PWM schemes results in lower order harmonics and poor THD. To obtain better THD and reduce the complexity in implementation, various novel PWM schemes are reported. Multi-reference modulation scheme is one of such scheme reported for T-type, cascaded T-type, and few other cascaded topologies [11, 13, 23, 25]. This scheme can be applicable to any MLI with any number of levels, but this scheme results high THD in line-voltages [33]. Switching function PWM is the other popular scheme reported for PUC, switched dc sources, and hybrid T-type topologies [6, 16]. To obtain the switching pulses, this scheme develops a hybrid function using minimum and maximum limits of each carrier. Therefore, to realise these carrier constraints, controller requires numerous comparators, which increases the complexity at higher levels.

Reduced carrier PWM [5, 9, 10, 27] is the other popular PWM, which involves a unipolar modulating and level-shifted carrier signals. In this scheme, pulses are generated by directly comparing reference with its carriers and further operated with user-defined logical expressions to obtain desired switching pulses to control the inverter. However, these logical expressions vary with topological arrangement and number of phase-voltage levels. Further, this conventional reduced carrier arrangement results high THD in line-voltage [33]. Hence, an alternate modulating signal and reduced carrier arrangement is reported [33]. The switching logic of this scheme involves minimum and maximum constraints of each carrier to obtain desired operation. However, it is to be noted that

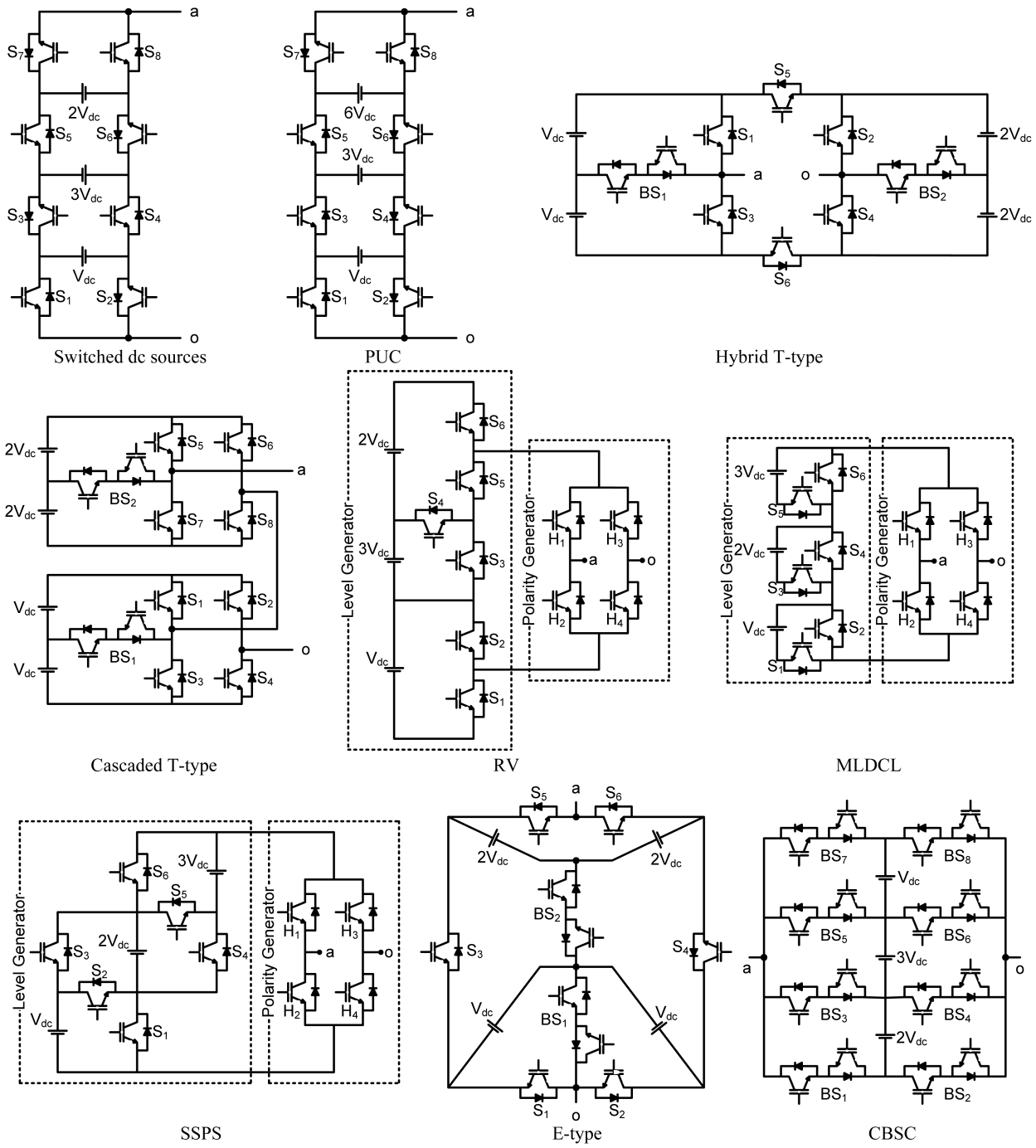

Fig. 1 *Thirteen-level RSC-MLI topologies for asymmetrical single-phase configurations*

reduced carrier PWM schemes with generalised logical expressions are the simplest and much easier to implement compared to switching scheme involving carrier minimum and maximum constraints.

By reviewing the various modulations of RSC-MLI topologies, the following conclusions can be drawn

i. Among the modulation schemes reported for RSC-MLIs, reduced carrier PWM scheme with logical expressions are the simplest. However, these logical expressions are not generalised and vary with inverter topology and number of levels.
ii. Conventional reduced carrier PWM scheme results degraded line THD performance, as its carrier arrangement is similar to LSPWM–opposite phase disposition (OPD) [33].

Hence, in this paper, a modified reduced carrier PWM scheme with generalised logical expressions is proposed, such that the proposed switching logic can control any RSC-MLI irrespective to the voltage ratios and topological arrangement. To derive these unified logical expressions, limitations of conventional reduced carrier modulation scheme in controlling RSC-MLI topologies are analysed. To verify the efficiency of the proposed PWM scheme, its performance in controlling various 13-level asymmetrical RSC-MLI topologies is investigated. Further, to ensure the superior performance of the proposed scheme, a comprehensive experimental comparison with state of the art schemes reported in the literature is presented.

This paper is laid out as follows: Section 2 investigates the limitations of conventional reduced carrier modulation schemes and presents the necessity of unified logical expressions to realise RSC-MLI topologies. Section 3 presents the methodology of the proposed scheme and derivation of unified logical expressions. Experimental performance of the proposed scheme to various RSC topologies are discussed in Section 4.

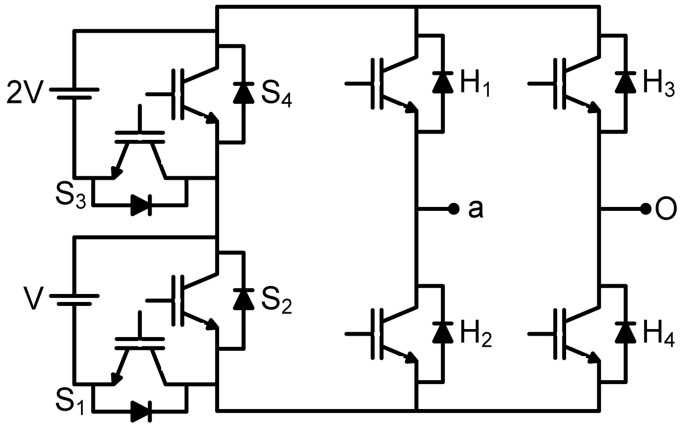

Fig. 2 *Seven-level single-phase configuration of RSC-MLI-based MLDCL*

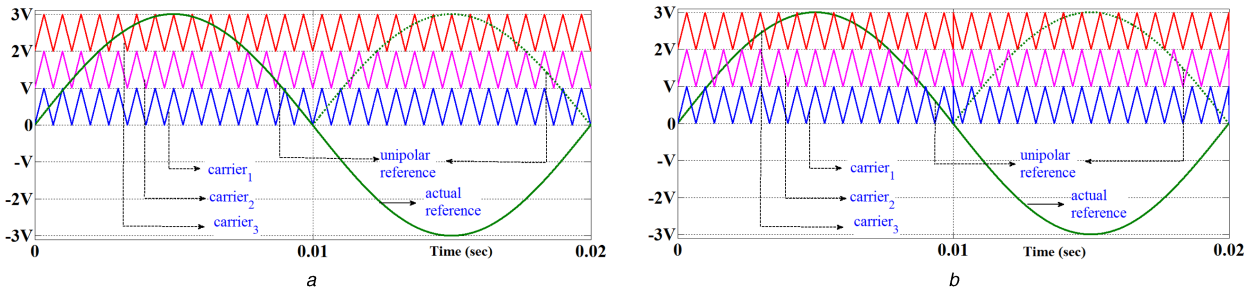

Fig. 3 *Reduced carrier PWM for seven-levels in phase-voltage*
(a) Conventional reduced carrier arrangement, ***(b)*** alternative carrier arrangement

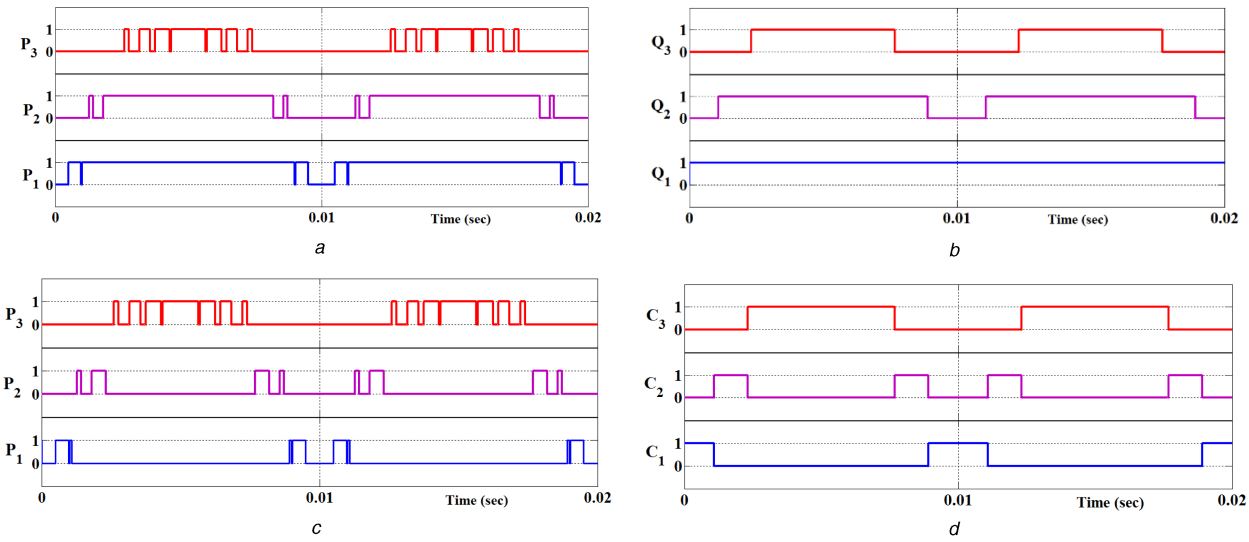

Fig. 4 *Switching pulses (P) and conduction intervals (Q and C) of seven-level reduced carrier PWM scheme:*
(a) Overlapped switching pulses, ***(b)*** Overlapped conduction intervals (*Q*), ***(c)*** Non-overlapped switching pulses, ***(d)*** Non-overlapped conduction interval (*C*)

2 Reduced carrier-based modulation schemes: limitations

Reduced carrier modulation schemes uses unipolar reference and $(n-1)/2$ level-shifted carriers to obtain 'n' levels in phase-voltage [5, 9, 10, 27]. Fig. 2 shows one of the RSC-MLI topologies for seven level. To control this inverter with reduced carrier modulation scheme, Fig. 3 shows two possible approaches for arranging the unipolar level-shifted carriers for obtaining seven-levels in phase-voltage.

Fig. 3*a* depicts the conventional reduced carrier arrangement. This type of reduced carrier PWM scheme results high THD in line-voltages as its carrier alignment is similar to LSPWM with OPD [29]. Hence to improve THD, an alternate carrier arrangement shown in Fig. 3*b* is presented in [33].

Fig. 4*a* depicts the switching pulses (P) obtained from Fig. 3*a*, by comparing unipolar reference with carrier signals (conventional switching logic). From Figs. 3*a* and 4*a*, it is observed that P_3 is active when reference is greater than $\text{carrier}_{3\text{-min}}$ and is responsible for obtaining voltage band of 2 V to 3 V, if the reference is in between carrier_3 limits. Similarly, P_2 and P_1 are responsible for obtaining voltage bands V to 2 V and 0 to V, respectively. It is observed that when P_3 is active, the remaining lower pulses P_2 and P_1 are high. This nature of switching pulses can be analysed by observing their conduction intervals (Q) shown in Fig. 4*b*. This conduction interval show the duration over which each switching pulse is active and is defined in the below equation

$$\begin{aligned} Q_i &= 1; \quad \text{reference} > \text{Carrier}_{i_{\min}} \\ Q_i &= 0; \quad \text{else} \end{aligned} \tag{1}$$

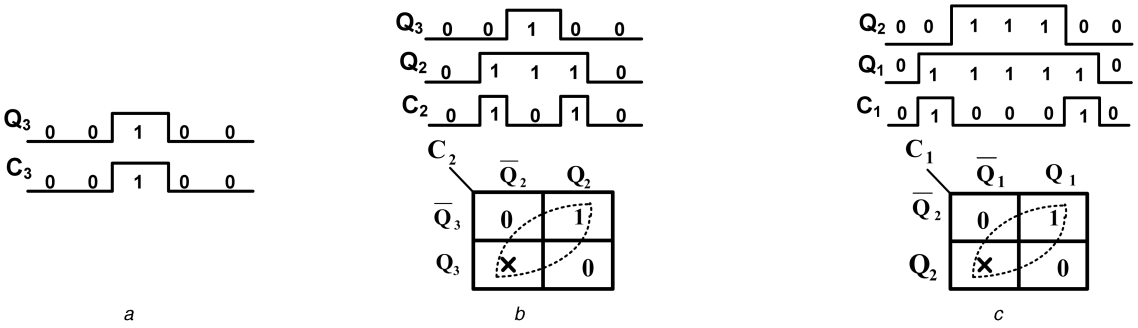

Fig. 5 *Mapping of overlapped conduction intervals (Q) with non-overlapped conduction intervals (C) and their associated K-maps*

From Fig. 4*b*, the overlapped nature of these conduction intervals (Q) can be clearly observed. Hence, applying these pulses directly to an inverter reflects that devices responsible for obtaining lower levels are remain in conduction at higher levels as well. However, this nature of switching cannot realise RSC-MLIs, as they possess the switching states where lower level conduction devices may not remain in conduction at higher levels [1]. Further with asymmetrical RSC-MLI topologies, these switching states turn more difficult to realise with conventional reduced carrier PWM scheme. This observation plays a vital role in proposing a modified switching logic to control RSC-MLIs.

Therefore, to control these asymmetrical RSC-MLI topologies with carrier-based PWM schemes, modifications in the conventional switching scheme are required. One simplest possible approach is to control these RSC-MLIs topologies by performing logical operations between the pulses obtained from conventional switching logic. These logical expressions modify the nature of the switching pulses such that they can be directly applied to control the considered inverter. As these expressions depend on switching pattern of the devices in the considered inverter, any change in the topological arrangement or number of levels needs a change in the logical expressions.

In case, if the nature of the switching pulses is non-overlapped, then they can realise any RSC-MLI, irrespective to its topological arrangement. Fig. 4*c* shows the non-overlapped switching pulses, obtained from the carrier arrangement shown in Fig. 4*b*, where each pulse is active when the reference is in between minimum and maximum value of its respective carrier. The non-overlapping nature of these pulses can be verified by observing their conduction intervals (C) shown in Fig. 4*d*. From Figs. 4*c* and *d*, it is observed that at any instant, only one among these pulse is active and is responsible for attaining a specific phase-voltage level. Hence, the methodology to obtain non-overlapped switching pulses by controlling their conduction intervals using unified logical expression is discussed in the below section.

3 Methodology and implementation of the proposed modulation scheme

To derive a unified logic expression for obtaining non-overlapped interval (C) from the overlapped interval (Q), the nature of both these conduction intervals should be analysed. Fig. 5 (obtained from Figs. 4*b* and *d*) shows the conduction intervals Q and C together. This figure infers that the desired conduction interval C can be obtained by performing a logical operation on Q with its adjacent bands. From Fig. 5*a*, by observing Q_3 and C_3 reveals their identical nature of switching and hence

$$C_3 = Q_3 \tag{2}$$

However, Q_2 and C_2 are different from each other and from Fig. 5*b*, the following relationships are obtained.

If $Q_3 = 0$ and $Q_2 = 0$, then $C_2 = 0$;

if $Q_3 = 1$ and $Q_2 = 1$, then $C_2 = 0$;

if $Q_3 = 0$ and $Q_2 = 1$, then $C_2 = 1$.

It should be noted that $Q_3 = 1$ and $Q_2 = 0$ case does not appear as lower conduction interval Q_2 always remains high when upper conduction interval Q_3 is high. To obtain a logical relation for C_2 in terms of Q_3 and Q_2, a two-variable Karnaugh-map (K-map) is implemented in Fig. 5*b*. From Fig. 5*b*, logical relation for C_2 is obtained as $C_2 = \bar{Q}_3 Q_2$. To realise this logic in hardware, two logic gates NOT and AND are required. To reduce these logic gates, a *do not care* variable is included in K-map and the logical relation (3) is obtained, which requires an Ex-OR gate only

$$C_2 = \bar{Q}_3 Q_2 + Q_3 \bar{Q}_2 = Q_2 \oplus Q_3 \tag{3}$$

To obtain conduction interval C_1, Fig. 5*c* is considered and following relationships are obtained.

If $Q_2 = 0$ and $Q_1 = 0$, then $C_1 = 0$;

if $Q_2 = 1$ and $Q_1 = 1$, then $C_1 = 0$;

if $Q_2 = 0$ and $Q_1 = 1$, then $C_1 = 1$.

With the help of K-map shown in Fig. 5*c*, logical relation (4) is obtained for conduction interval C_1

$$C_1 = Q_1 \oplus Q_2 \tag{4}$$

Generalising (2)–(4), (5) can be obtained, where i is the carrier number

$$\begin{aligned} &\text{for} \quad i = (n-1)/2 \\ &\qquad C_i = Q_i \\ &\text{for} \quad 1 \le i < (n-1)/2 \\ &\qquad C_i = Q_i \oplus Q_{i+1} \end{aligned} \tag{5}$$

Applying the pulse P_i ($|\text{ref}| > \text{carrier}_i$) over the interval C_i results in desired non-overlapped switching pulses. This switching action of the proposed modulation scheme to control seven-level inverter is shown in Fig. 6.

In Fig. 6, C_3 should be active to obtaining voltage band of 3 V to 2 V. Similarly, C_2 and C_1 should be active for obtaining voltage band of 2 V to V and V to 0, respectively. C_3 high with P_3 high, i.e. pulse C_3P_3 is responsible for obtaining 3 V voltage state. C_3 high with P_3 low or C_2 high with P_2 high, i.e. pulse $C_3\bar{P}_3 + C_2P_2$ obtains 2 V voltage state. Similarly, C_2 high with P_2 low or C_1 high with P_1 high, i.e. $C_2\bar{P}_2 + C_1P_1$ results in V voltage state. C_1 high with P_1 low, i.e. pulse $C_1\bar{P}_1$ results in zero voltage. The polarity of these voltage states is decided by the polarity of the modulating signal, where positive voltage levels are obtained for the positive half of the reference and negative voltage levels are obtained for negative half of the modulating signal. Table 1 shows the implementation of the proposed switching logic to realise a seven-level inverter topology shown in Fig. 1. For example, to obtain +3 V voltage-level, switches H_4, S_1, S_3, and H_1 should be in conduction. Therefore, these switches are applied with pulse C_3P_3 for the positive half of the reference. Similarly, to obtain −3 V voltage-level, pulse C_3P_3 applied to switches H_2, S_1, S_3, and H_3 for the negative half of the reference. A similar explanation holds good for remaining voltage level as presented in Table 1.

In this proposed scheme, the obtained number of desired pulses will be equal to the number of phase-voltage levels, where each

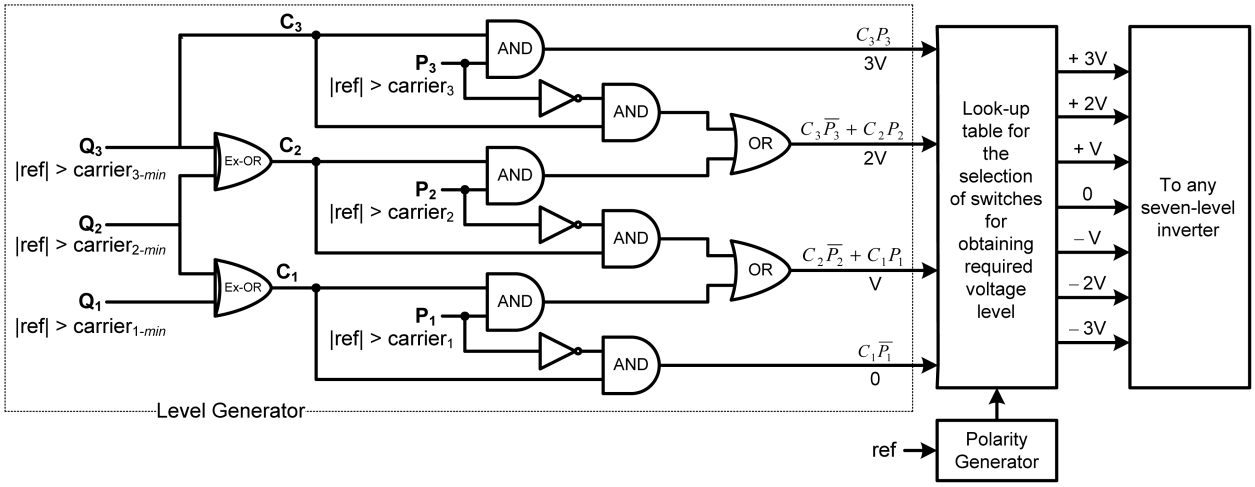

Fig. 6 *Implementation of the proposed PWM scheme for seven-level phase-voltage*

Table 1 Selection of switching devices to control seven-level inverter with the proposed scheme

Polarity generation	Voltage level	Switching pulse	Devices to be in on to obtain the respective voltage level in Fig. 2
ref ≥ 0	+3 V	C_3P_3	H_4–S_1–S_3–H_1
	+2 V	$C_3\bar{P}_3 + C_2P_2$	H_4–S_2–S_3–H_1
	+V	$C_2\bar{P}_2 + C_1P_1$	H_4–S_1–S_4–H_1
for zero-level	0	$C_1\bar{P}_1$	H_4–S_2–S_4–H_1 or H_2–S_2–S_4–H_3
	—	—	
ref < 0	−V	$C_2\bar{P}_2 + C_1P_1$	H_2–S_1–S_4–H_3
	−2 V	$C_3\bar{P}_3 + C_2P_2$	H_2–S_2–S_3–H_3
	−3 V	C_3P_3	H_2–S_1–S_3–H_3

Table 2 Experimental parameters

Circuit/parameter	Component/value
30 V isolated dc power supplies (12 no.)	30 V, 3 A dual channel regulated power supply
13-level asymmetrical RSC-MLI	developed using 2 modules of generalised converter with 24 IGBTs each
IGBT model and rating	IKW40T120, 40 A and 1200 V
carrier frequency (f_{cr})	2 kHz
amplitude modulation index (m_a)	0.98
load	three-phase star-connected 1 kW 0.85 power factor lagging.
controller (to obtain firing signals for IGBTs)	dSPACE micro-lab box RTI1202 R&D controller sampling time (20 μs)

pulse is responsible for obtaining a particular voltage level. Further, each of these desired pulse will be given to the devices (of the considered inverter) to be in conduction to achieve the respective voltage state. Further, generalising these obtained switching pulses for higher voltage levels (6) is obtained

$$\begin{aligned}
&\text{for} \quad \frac{n-1}{2}V \\
&\quad \Rightarrow \text{switching pulse} = C_{\frac{n-1}{2}}P_{\frac{n-1}{2}} \\
&\text{for} \quad V \le iV \le \left(\frac{n-1}{2}-1\right)V \\
&\quad \Rightarrow \text{switching pulse} = C_{i+1}\bar{P}_{i+1} + C_iP_i \\
&\text{for} \quad 0\,V \\
&\quad \Rightarrow \text{switching pulse} = C_1\bar{P}_1
\end{aligned} \tag{6}$$

4 Implementation of the proposed scheme to 13-level asymmetrical RSC-MLI topologies

The performance of the proposed PWM scheme is validated by developing experimental set-ups of different three-phase IGBT-based 13-level asymmetrical RSC-MLI topologies. The developed topologies are MLDCL, SSPS, switched dc sources, hybrid T-type, and E-type (as shown in Fig. 1). Further, to validate the superiority of the proposed PWM scheme, the above selected topologies are also controlled using conventional reduced carrier PWM scheme. Different inverter topologies are developed by using two inverter modules with 24 individual IGBTs in each. The modulation schemes are implemented in dSPACE Micro-lab box RTI1202 R&D controller. The carrier signal frequency (f_{cr}) and amplitude modulation index (m_a) are selected as 2 kHz and 0.98, respectively. The dc input source voltage (V_{dc}) is selected as 30 V and with this, the maximum amplitude of phase-voltage is 180 V. The complete list of parameters used in experimental study is given in Table 2 and the photograph of the experimental set-up is shown in Fig. 7. Table 3 shows the implementation of the proposed switching logic to realise these selected RSC-MLI topologies.

Fig. 8 shows the experimental performance of phase-voltages and their corresponding harmonic spectra. Figs. 8*a*–*e* show the phase-voltage performance of 13-level MLDCL, SSPS, switched dc sources, hybrid T-type, and E-type asymmetrical topologies with the proposed PWM scheme. Fig. 8*f* depicts the phase-voltage performance of 13-level MLDCL with conventional reduced carrier PWM scheme. Similarly, Fig. 9 depicts the experimental line-voltage performance of these RSC topologies with the proposed PWM scheme and conventional reduced carrier PWM scheme. Line-voltages and their corresponding harmonic spectra of the proposed scheme for considered 13-level asymmetrical topologies are shown in Figs. 9*a*–*e*. Fig. 9*f* depicts the line-voltage

Fig. 7 *Photograph of the experimental set-up for realising 13-level asymmetrical switched dc source inverter*

Table 3 Selection of switching devices to control 13-level inverter with the proposed scheme

Polarity generation	Level	Switching pulse	Devices to be in conduction to obtain the respective voltage level				
			MLDCL	SSPS	Switched dc sources	Hybrid T-type	E-type
ref ≥ 0	+6 V	C_6P_6	H_4–S_1–S_3–S_5–H_1	H_4–S_2–S_5–H_1	S_2–S_3–S_6–S_7	S_2–S_6–S_1	S_1–S_4–S_5
	+5 V	$C_6\bar{P}_6 + C_5P_5$	H_4–S_2–S_3–S_5–H_1	H_4–S_1–S_5–H_1	S_1–S_3–S_6–S_7	S_2–S_6–BS_1	BS_1–S_4–S_5
	+4 V	$C_5\bar{P}_5 + C_4P_4$	H_4–S_1–S_4–S_5–H_1	H_4–S_2–S_4–H_1	S_2–S_3–S_6–S_8	BS_2–S_6–S_1	S_2–S_4–S_5
	+3 V	$C_4\bar{P}_4 + C_3P_3$	H_4–S_1–S_3–S_6–H_1	H_4–S_1–S_4–H_1	S_1–S_3–S_6–S_8	BS_2–S_6–BS_1	S_1–BS_2–S_5
	2 V	$C_3\bar{P}_3 + C_2P_2$	H_4–S_2–S_3–S_6–H_1	H_4–S_1–S_6–H_1	S_2–S_4–S_6–S_7	S_4–S_6–S_1	S_1–S_4–S_6
	V	$C_2\bar{P}_2 + C_1P_1$	H_4–S_1–S_4–S_6–H_1	H_4–S_3–S_6–H_1	S_2–S_3–S_5–S_7	S_4–S_6–BS_1	BS_1–S_4–S_6
for zero-level	0	$C_1\bar{P}_1$	H_4–S_2–S_4–S_6–H_1 or H_2–S_2–S_4–S_6–H_3	H_1–H_3 or H_2–H_4	S_1–S_3–S_5–S_7	S_4–S_6–S_3	S_1–S_3–S_5
ref< 0	−V	$C_2\bar{P}_2 + C_1P_1$	H_2–S_1–S_4–S_6–H_3	H_2–S_3–S_6–H_3	S_1–S_4–S_6–S_8	S_2–S_5–BS_1	BS_1–S_3–S_5
	−2 V	$C_3\bar{P}_3 + C_2P_2$	H_2–S_2–S_3–S_6–H_3	H_2–S_1–S_6–H_3	S_1–S_3–S_5–S_8	S_2–S_5–S_3	BS_1–BS_2–S_6
	−3 V	$C_4\bar{P}_4 + C_3P_3$	H_2–S_1–S_3–S_6–H_3	H_2–S_1–S_4–H_3	S_2–S_4–S_5–S_7	BS_2–S_5–BS_1	S_2–BS_2–S_6
	−4 V	$C_5\bar{P}_5 + C_4P_4$	H_2–S_1–S_4–S_5–H_3	H_2–S_2–S_4–H_3	S_1–S_4–S_5–S_7	BS_2–S_5–S_3	S_1–S_3–S_6
	−5 V	$C_6\bar{P}_6 + C_5P_5$	H_2–S_2–S_3–S_5–H_3	H_2–S_1–S_5–H_3	S_2–S_4–S_5–S_8	S_4–S_5–BS_1	BS_1–S_3–S_6
	−6 V	C_6P_6	H_2–S_1–S_3–S_5–H_3	H_2–S_2–S_5–H_3	S_1–S_4–S_5–S_8	S_4–S_5–S_3	S_2–S_3–S_6

performance of 13-level MLDCL with conventional reduced carrier PWM scheme.

In order to evaluate the whole inverter system, it is necessary to show the performance of the inverter currents. Fig. 10 depicts the experimental line-current performance of RSC topologies with proposed and conventional reduced carrier PWM schemes for three-phase star-connected load. Line-current and their corresponding harmonic spectra of the proposed scheme for considered 13-level asymmetrical topologies are shown in Figs. 10*a–e*. Fig. 10*f* depicts the line-current performance of 13-level MLDCL with conventional reduced carrier PWM scheme.

In a view to estimate the effectiveness of the proposed PWM scheme, a comprehensive comparison is carried out with carrier-based PWM schemes reported in the literature. For this, the PWM scheme along with the inverter reported in the literature is implemented experimentally and compared with the proposed PWM scheme in terms of harmonic performance, complexity in implementation, and computation burden. The summary of merits and demerits are presented in Table 4. Comparing Figs. 8–10 along with Table 4, the following conclusions are derived.

i. From Figs. 8*a–e*, it is observed that all the phase-voltage waveforms and their harmonic spectra are identical with dominant harmonic appeared at frequency modulation index ($m_f = 40$).
ii. Comparing Fig. 8*f* with Figs. 8*a–e*, it can be observed that THD values of conventional reduced carrier scheme (6.1%) are less when compared with the proposed scheme (7.8%). Nevertheless, the conventional reduced carrier PWM scheme has less THD value but its side-band harmonics are different and centred at m_f. The magnitude of the harmonics are also different in both methods, which leads to significant difference in line-voltage THD.
iii. The line-voltage waveforms and their corresponding harmonic spectra with the proposed PWM scheme shown in Figs. 9*a–e* are identical in terms of waveform shape and harmonic performance. The obtained THD are identical with side-band harmonics centred at $m_f = 40$.
iv. Comparing Figs. 9*a–e* with Fig. 9*f*, it can be observed that the proposed scheme produces improved harmonic performance (2.8%) when compared with conventional reduced carrier PWM scheme (6.0%). The reason for this is the proposed PWM scheme will help for better cancellation of harmonics presented in phase-voltages.
v. From line-current performance shown in Fig. 10, it is observed that line-current waveforms and their corresponding harmonic spectra with the proposed PWM scheme are identical in terms of waveform shape and harmonic performance. It can also be observed that the proposed scheme produces improved harmonic performance (2.3%) when compared with conventional reduced carrier PWM scheme line-currents (5.4%) shown in Fig. 10*f*.
vi. The proposed scheme can be directly applicable to any MLI topology and easily scalable to higher number of levels irrespective of topological arrangement and dc voltage ratios.
vii. The proposed PWM scheme produces improved line THD performance compared with conventional reduced carrier and

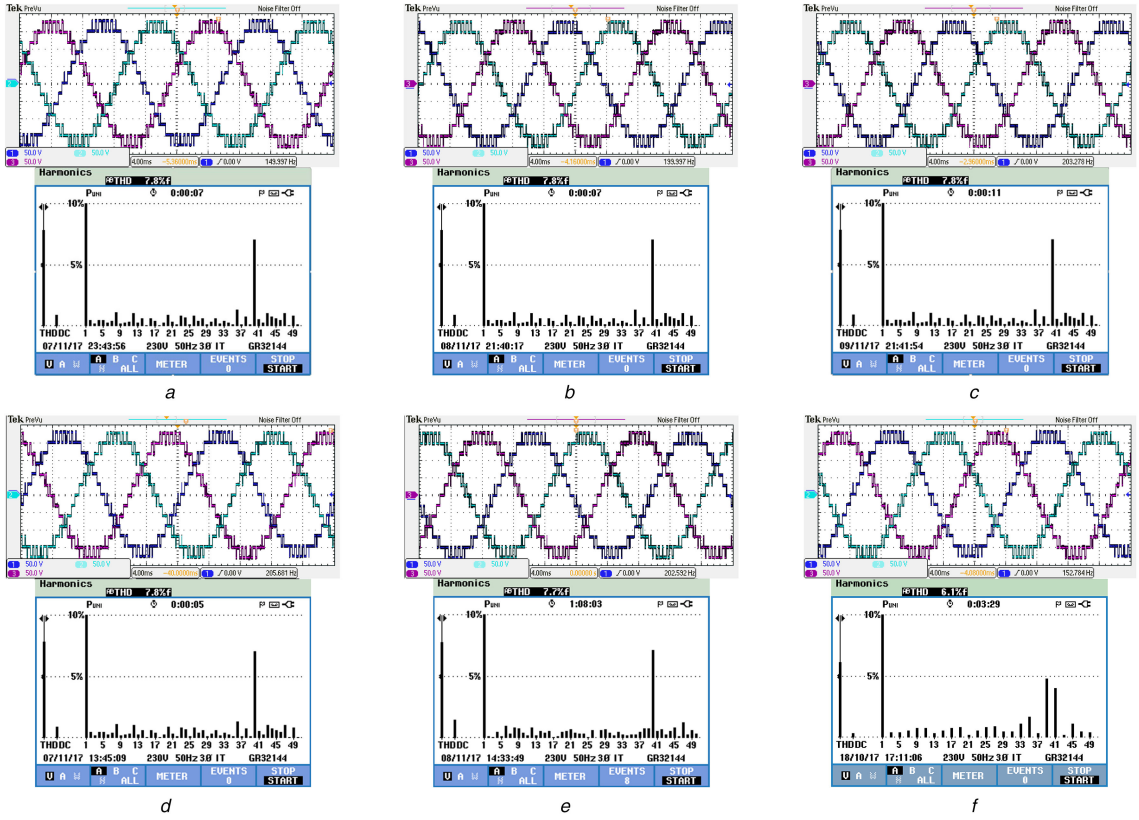

Fig. 8 *Phase-voltage waveforms and their corresponding harmonic spectra (scale: X-axis: 4 ms/div and Y-axis: 50 V/div)*
(a) MLDCL, ***(b)*** SSPS, ***(c)*** Switched dc sources, ***(e)*** E-type, ***(f)*** MLDCL with conventional reduced carrier PWM

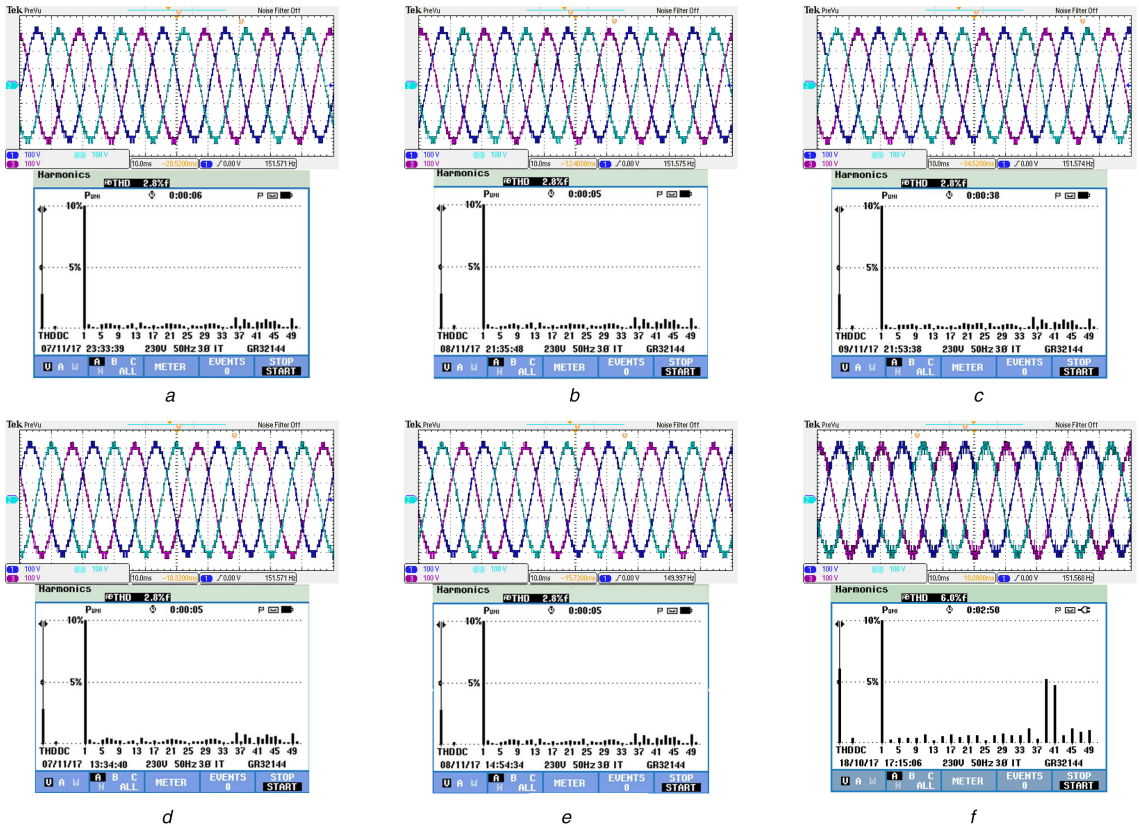

Fig. 9 *Line-voltage waveforms and their corresponding harmonic spectra (scale: X-axis: 10 ms/div and Y-axis: 100 V/div)*
(a) MLDCL, ***(b)*** SSPS, ***(c)*** Switched dc sources, ***(d)*** Hybrid T-type, ***(e)*** E-type, ***(f)*** MLDCL with conventional reduced carrier PWM

multicarrier PWM schemes and similar THD performance when compared with switching function PWM scheme.

vii i. The turnaround time for implementation of the proposed PWM scheme is significantly reduced and remains almost same for a given number of level in any inverter topology. The less computation burden of the proposed scheme will allow the controller to accurately implement higher switching frequencies.

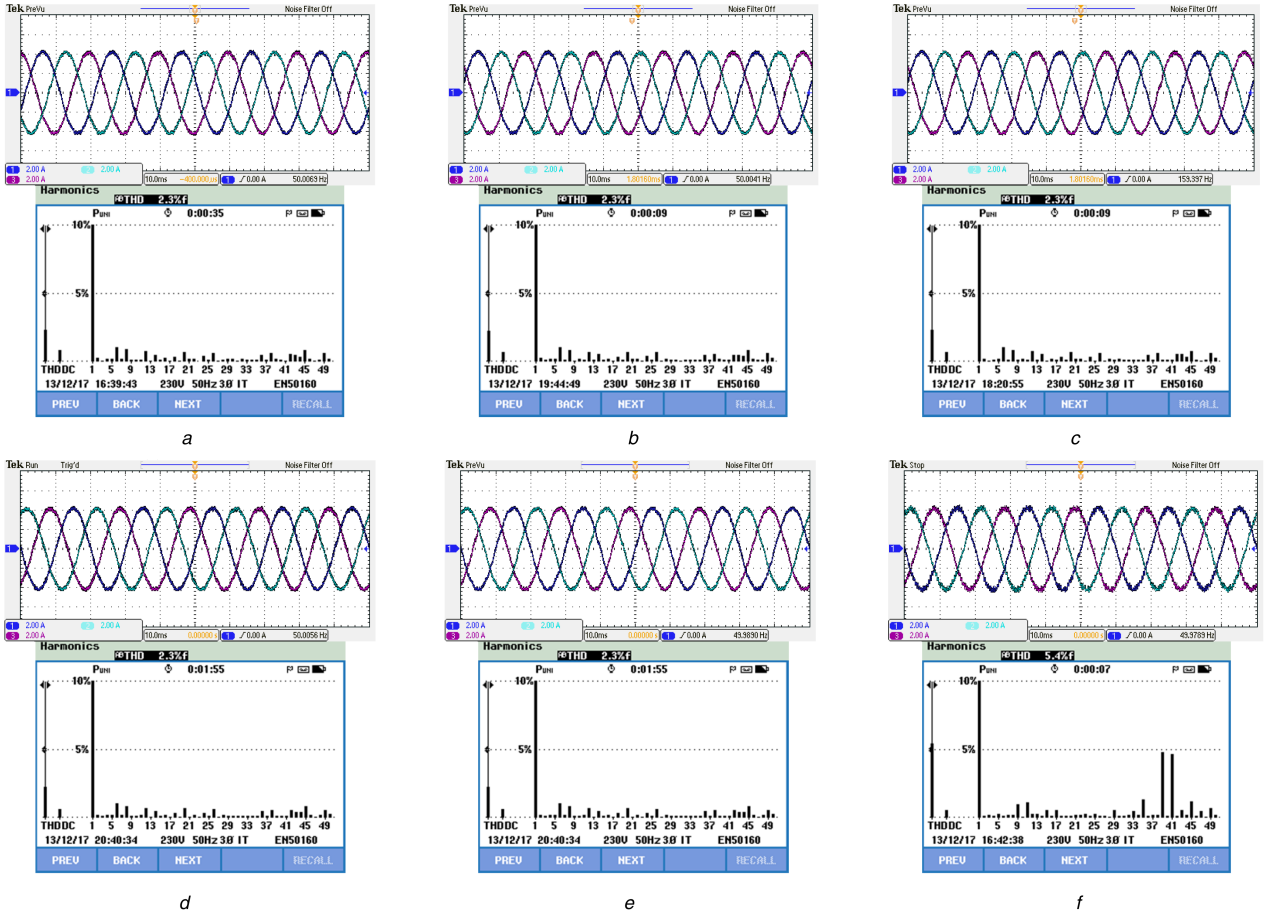

Fig. 10 *Line-current waveforms and their corresponding harmonic spectra (scale: X-axis: 10 ms/div and Y-axis: 2 A/div)*
(a) MLDCL, ***(b)*** SSPS, ***(c)*** Switched dc sources, ***(d)*** Hybrid T-type, ***(e)*** E-type, ***(f)*** MLDCL with conventional reduced carrier PWM

5 Conclusion

To overcome the limitations of conventional reduced carrier PWM scheme, this paper presented a modified reduced carrier PWM scheme with unified logical expressions. The efficacy of the proposed switching logic is validated with experimental studies on various 13-level asymmetrical RSC-MLI topologies. Further, superior performance of the proposed scheme is verified by comparing its performance with conventional carrier PWM schemes. Topology-independent operation, simplified switching logic generalisation to higher levels, less computation burden, and improved line-voltage THD performance of the proposed reduced carrier PWM scheme serves as a viable solution to overcome the demerits of conventional multicarrier, reduced carrier, and multi-reference PWM schemes.

Table 4 Performance comparison of carrier-based PWM schemes reported in the literature with the proposed PWM scheme

Carrier-based PWM scheme and topology reported in the literature					With the proposed PWM scheme			Merits and demerits of PWM scheme reported in the literature
PWM scheme	Topology	Phase-voltage THD, %	Line-voltage THD, %	Turnaround time, μs	Phase-voltage THD, %	Line-voltage THD, %	Turnaround time, μs	
multi-reference [11, 13, 23, 25]	T-type seven-level [11]	15.7	14.8	6.5	15.7	4.9	6.2	✓ require less computational time ✓ scalable to higher levels ✓ directly applicable to all topologies ✗ high line-voltage THD ✗ difficulty in implement for closed-loop applications due to the presence of multiple references
reduced carrier with logic gates [9, 10, 27]	modified T-type seven-level [10]	15.8	15.0	19	15.6	4.8	5.9	✗ high line-voltage THD ✗ switching logic is complex and requires more computational time ✗ neither scalable nor directly applicable to all topologies
switching function PWM [6, 16]	symmetrical seven-level switched dc-sources [6]	15.6	4.8	7.5	15.5	4.7	6.0	✓ good line-voltage THD performance ✓ scalable and applicable to all topologies ✗ involves large number of comparators which occupies more memory and requires more computation time to realise the switching pulses
reduced carrier [5]	RV seven-level [5]	15.7	14.9	5.3	15.6	4.8	6.1	✓ scalable with simplified switched logic and takes very less computational time ✗ not applicable to all topologies ✗ high line-voltage THD
hybrid PWM [17, 20, 22, 32]	asymmetrical SSPS with H-bridge eleven-level [17]	9.9	3.1	6.6	9.6	3.0	7.2	✓ good line-voltage THD performance ✓ scalable and possess simplified switched logic and takes very less computational time ✗ applicable only to asymmetrical cascaded topologies ✗ may involve mixed switching frequencies, hence may produce unwanted voltage spikes in phase and line-voltages

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