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Zero-sequence voltage injected fault tolerant scheme for multiple open circuit faults in reduced switch count-based MLDCL inverter

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Abstract: Neutral shifting (NS) is a popular scheme to achieve fault tolerance operation (FTO) of multilevel inverters (MLIs) such as cascaded H-bridge (CHB). This fault tolerance scheme (FTS) can be realised with/without zero-sequence voltage injection. Among these, NS with zero-sequence injection FTS is relatively easier to implement. However, this scheme is not generalised for multiple open-circuit faults. Moreover, NS-FTS schemes are not directly applicable for fault tolerance of reduced switch count (RSC)-MLIs, as these inverters have limited redundancies. Therefore in this study, FTO for RSC-based multilevel dc-link (MLDCL) inverter using NS zero-sequence injection FTS is proposed for simultaneous failure of multiple switch faults. Generalised mathematical equations are derived to calculate the magnitude and phase angle of injected zero-sequence voltage for obtaining balanced line voltages with uniform power sharing among all healthy units. The proposed generalised NS-FTS with zero-sequence injection is implemented on three-phase 15-level MLDCL inverter for various fault conditions. The obtained simulation results are validated experimentally on nine-level MLDCL inverter.

1 Introduction

Reduction in switch count of reduced switch count (RSC) multilevel inverters (MLIs) has increased the reliability of inverter by decreasing the probability of fault occurrence. On the other hand, this reduction in switch count has reduced the switching redundancies as each switch is involved in attaining more than one voltage level [1, 2]. In general, switching redundancies play a key role in reconfiguration of the inverter under faulted condition [3–6]. Therefore, the reduction in switching redundancies has increased the difficulty of fault compensation [1, 2, 6].

There are multiple internal and external reasons for occurrence of fault in power converters; however, every fault ends up with either open-circuit (oc) or short circuit (sc) of a particular switch or associated unit/bridge and results in malfunction/unbalance operation [6–8]. sc fault results in dangerously high current not only through the faulted switch but also through faulted phase and cause a possible damage to the inverter. Therefore, to avoid these faults a fast acting over current protection circuits are required [6–9]. On the other hand, oc faults are not severe and can be compensable [8]. Hence, this paper analyses effect of oc faults only.

Under faulted condition, the operation of inverter is restricted and produces unbalance in output voltage. In literature, various methods have been reported to diagnosis, isolate and compensate oc faults [3–13]. These methods involve either passive protection devices such as fuses or active protection devices such as relays or triodes for alternating currentss. However, involvement of these auxiliary equipment for fault compensation complicates the topology and raises the cost [4–6, 11, 12]. Hence, various pulsewidth modulation (PWM) schemes which does not require any auxiliary equipment to obtain fault tolerant operation (FTO) are reported [4, 6, 12–22]. PWM schemes such as space vector modulation (SVM) and carrier-based schemes are reported for compensating single switch/bridge/basic unit fault in two level or MLI/RSC-MLI such as T-type are reported [4, 6, 14, 15]. Among these PWM-based schemes, SVM is an attractive scheme which can achieve FTO by creating switching redundancies [4–6, 15]. However, its complex implementation acts as a limitation to the scheme.

Among the various fault tolerant schemes (FTS) reported in literature, by-passing method is one of the most feasible approach to restore balanced operation [4, 6, 16–18]. During the fault condition, this method by-passes few healthy units in one or more phases, such that the number of operating units per phase is same. This method of fault tolerance achieves balanced operation but derates the inverter. Therefore, to obtain FTO without derating the inverter, the idea of 'increasing the burden on healthy units/cells' method is presented in [18]. In this scheme, the burden of faulty units of one phase is shared across the healthy units of same phase such that its overall phase voltage is equal to pre-fault voltage. This method of fault compensation obtains balanced phase-voltages nevertheless, results in non-uniform burdening of healthy units, which effects their dc-link voltages and power distribution among operating units.

Therefore, to obtain balanced operation with equal power distribution among the healthy units, neutral shifting (NS) FTS is reported in [6, 16–22]. This scheme modifies the magnitude and angle between phase voltages such that the inverter produces balanced line voltages with uniform burden on all healthy units. The magnitude unbalance due to faulty units and changing the angles between phase-voltages shifts the neutral point of the inverter and thus name NS is derived. Usually, this method of NS involves manual calculations to modify angles between phase voltages to ensure balanced line voltages [6, 16, 17, 19–21]. This method of NS with selective harmonic elimination (SHE) PWM is reported for single/multiple faults in cascaded H-bride (CHB) MLI [20, 21]. In [20], this method is generalised for multiple switch faults on all phases but can be implemented only if the number of faulty units in any two phases are same. If the number of faulty units on all the phases is different then, few healthy units on any phase are bypassed such that the number of operating units on any two phases are same. This method of bypassing healthy units reduces the performance and derates the inverter and therefore is not preferable. In [21], multi-fault NS-FTS with modified SHE is reported. However, this method of NS-FTS involves complex mathematical calculations and is difficult to implement in closed-loop applications.

Another approach to achieve NS is to inject a zero-sequence voltage in each phase such that they result in balanced line voltages with uniform burdening of all healthy units [16, 18, 22]. Addition of zero-sequence voltage shifts the neutral point of inverter [18]. The magnitude of injected zero-sequence voltage depends on the number of faulty units and plays a crucial role in retrieving FTO of

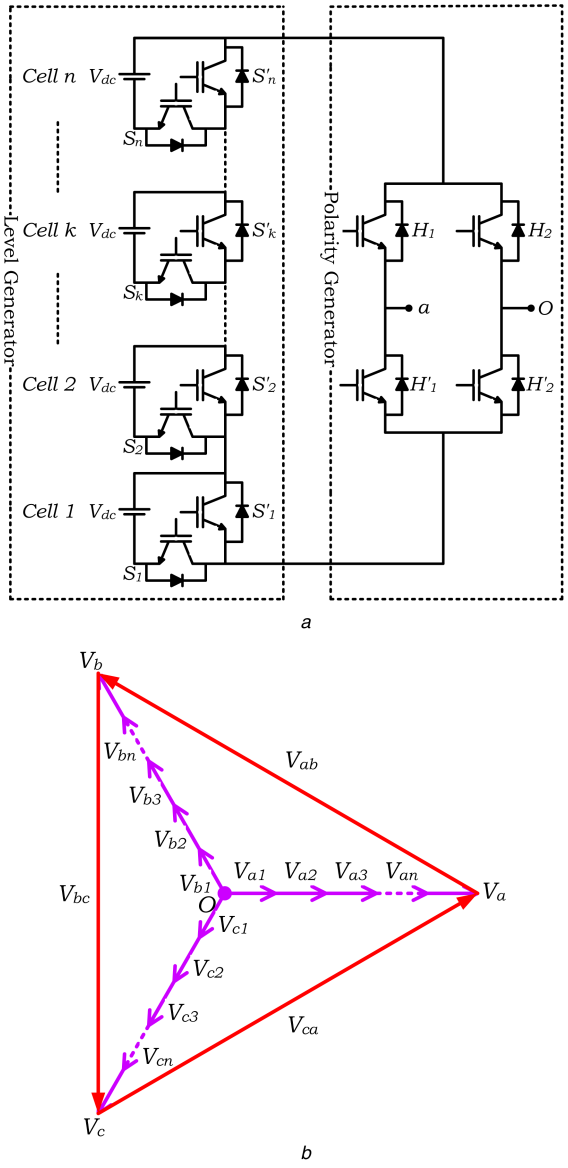

Fig. 1 *Generalised structure of MLDCL and its phasor diagram*
(a) Single-phase MLDCL circuit, ***(b)*** Three-phase phasor diagram of inverter voltages

the inverter. In literature, this scheme is reported to CHB for failure of single unit per phase [18, 22].

Therefore by reviewing various FTS for oc faults, the following conclusions can be drawn:

i. Among the various FTS reported in the literature, NS is an attractive scheme to tolerate oc faults in MLIs.
ii. Even though NS schemes are reported for CHB, it can be applicable to modular RSC-MLIs topologies such as multilevel dc-link (MLDCL) [1, 23]. However, direct implementation to these inverters is not possible.
iii. NS method with SHE PWM scheme involves elusive mathematical calculations to determine switching instants for FTO.
iv. NS method reported in [20] is generalised for multiple faults, however requires by-passing of healthy units and thus derates the inverter.
v. NS with zero-sequence injection FTS reported in [18, 22] is demonstrated only for single unit fault per phase.

Therefore, this paper contributes to:

i. To propose NS zero-sequence injection FTS to RSC-based MLDCL inverter.
ii. The proposed FTS can compensate simultaneous failure of multiple switches on all phases.
iii. Generalised equations are presented to determine the magnitude of injected zero-sequence voltage and fault tolerant modulating signals for any fault case.
iv. The proposed FTS obtains balanced line voltages with uniform burden among all basic units of MLDCL.
v. The proposed FTS is implemented with carrier rotation-based reduced carrier PWM scheme [24, 25].

The efficacy of the proposed scheme for obtaining balanced line voltages and currents is verified for various fault cases on 15- and nine-level MLDCL. In addition, uniform performance of all the healthy units is ensured by observing their powers. Furthermore, obtained simulation results are validated experimentally with hardware setup controlled with OPAL-RT 4500 controller.

The structure of this paper is as follows: In Section 2, analysis of MLDCL for various fault conditions is studied and their effect on phase voltage is observed. Also, limitations of conventional NS methodologies are discussed. In Section 3, generalisation of NS zero-sequence injection FTS for simultaneous failure of multiple switches is carried out. In Sections 4 and 5, simulation and experimental results on three-phase MLDCL are discussed.

2 Fault analysis of MLDCL inverter and limitations of conventional fault tolerant schemes

Among the recently reported RSC-MLI topologies, MLDCL is one of the popular topology with modular structure and adequate switching redundancies [1, 23]. The redundant structure of MLDCL with floating dc-link capacitors turns it to be an attractive alternative to CHB for regenerative front-end converters, power quality improvement and grid connected applications. This section presents the operation of MLDCL inverter for normal and faulty operating conditions. Generalised circuit of MLDCL with 'n' basic units per phase is shown in Fig. 1*a*. The structure of MLDCL is divided into level generator and polarity generator. Level generator is responsible for producing n-level uni-polar voltage. Polarity generator has an H-bridge in each phase with switches operating at fundamental frequency and converts this uni-polar voltage to bipolar with $(2n-1)$ levels in phase voltage. The switching operation of MLDCL can be refereed from the study [1]. From the switching operation, it can be observed that each basic unit of level generator has one isolated dc source with complimentary switch pair (S_k and S_k') and produces either $V_{\rm dc}$ or zero, where k can be intermediate unit from 1 to n. In any unit, conduction of S_k produces $V_{\rm dc}$ across the respective unit and conduction of S_k' forces the voltage across the respective unit to zero.

If v_{a1}, v_{a2}, …., and v_{an} are the output voltages of each basic unit of phase a, obtained after processing through the polarity generator, then the total voltage of phase a (v_a) is expressed as (1) [18]. The modulating signals for phase voltages are expressed in (2)–(4). The phasor diagram for balanced operation of the inverter is shown in Fig. 1*b*.

$$v_a = \sum_{k=1}^{n} v_{ak} = v_{a1} + v_{a2} + \cdots + v_{an} \tag{1}$$

where $v_{a1} = v_{a2} = v_{an} = m_{\rm a} V_{\rm dc} \sin \omega t$ and $m_{\rm a}$ is the amplitude modulation index.

Similarly, for phases b and c, $v_b = \sum_{k=1}^{n} v_{bk}$ and $v_c = \sum_{k=1}^{n} v_{ck}$.

Therefore

$$v_a = n\, m_{\rm a} V_{\rm dc} \sin \omega t \tag{2}$$

$$v_b = n\, m_{\rm a} V_{\rm dc} \sin(\omega t - 120^{\circ}) \tag{3}$$

$$v_c = n\, m_{\rm a} V_{\rm dc} \sin(\omega t - 240^{\circ}) \tag{4}$$

oc faults in MLDCL can occur either in polarity generator or in level generator or in both. However, as the switches in polarity generator operate at fundamental frequency, any fault(s) on polarity

Table 1 Effect of Type 1 fault on phase-voltage levels

oc fault of S_k	Missing levels
no fault	none
fault in one basic unit	$\pm nV_{dc}$
fault in two basic units	$\pm nV_{dc}$ and$\pm(n-1)V_{dc}$
fault in 'k' basic units	$\pm nV_{dc}$, $\pm(n-1)V_{dc}$… and $\pm(n-k+1)V_{dc}$

Table 2 Effect on Type 2 fault on phase-voltage levels

oc fault of S'_k	Missing levels
no fault	none
fault in one basic unit	none
fault in two basic units	$\pm V_{dc}$
fault in three basic units	$\pm V_{dc}$ &$\pm 2V_{dc}$
fault in 'k' basic units	$\pm V_{dc}$, $\pm 2V_{dc}$, …, $\pm(k-1)V_{dc}$

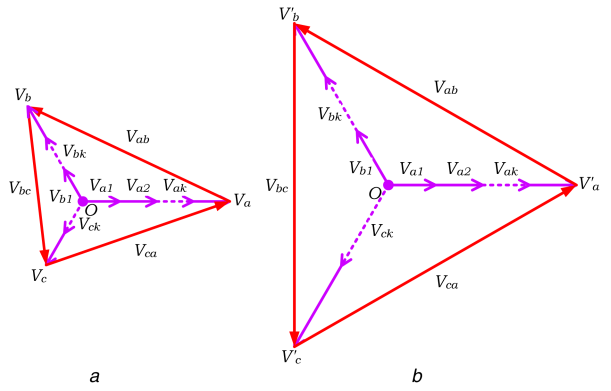

Fig. 2 *Phasor diagram of inverter voltages with x, y and z faulty units in phases a, b and c, respectively*

(a) Unbalanced operation under faulted condition, ***(b)*** Balanced operation with increasing the burden of healthy units in each phase

generator result in missing of either positive/negative half cycle or complete waveform. Under such conditions, FTO is not feasible. On the other hand, oc faults on level generator can be partially/fully compensated due to its modular structure with identical basic units. oc faults on level generator are analysed by considering the deviations in phase-voltage levels. Referring to Fig. 1*a*, oc faults in MLDCL (on level generator) are classified into Type 1 (oc of S_k) and Type 2 (oc of S'_k) faults.

Type 1 fault (*oc fault on switch* S_k): Considering a basic unit k, with switches S_k and S'_k. As switches on any basic unit are operated complimentarily, oc fault on S_k ensures S'_k to remain in conduction. This results in zero voltage across the kth basic unit and further limit the maximum voltage across level generator to $(n-1)V_{dc}$ and phase-voltage levels to $\pm(n-1)V_{dc}$. Effect of Type 1 fault on phase-voltage levels is presented in Table 1. This type of switching action leads to inverter unbalance, which can be compensated by using FTS.

Type 2 fault (*oc fault on* S_k'): oc of S_k' ensures S_k to remain in conduction. This maintains the voltage across the kth basic unit (faulted unit) as V_{dc}. Therefore, the minimum voltage of the level generator raises to V_{dc} and output of the level generator varies from V_{dc} to nV_{dc}. This results in missing of zero level in phase voltage. However, this zero level can be achieved in polarity generator. Hence, Type 2 fault on any single unit is compensable and does not require FTS. However, if such a fault appears on two units of same phase, then the minimum voltage of the level generators raises to $2V_{dc}$, which results in missing of $\pm V_{dc}$ and 0 levels in phase voltage. Missing of $\pm V_{dc}$ level cannot be compensable by any other switching path and results in unequal dv/dt. Hence, this type of fault is intolerable and further cannot be compensated by any FTS. The effect of Type 2 faults on phase-voltage levels is given in Table 2.

From Tables 1 and 2, it can be concluded that FTO can be achieved only for Type 1 faults and therefore these faults are only considered in this paper. Effect of Type 1 fault on MLDCL is similar to the effect of an oc fault of an H-bridge of CHB. To tolerate such type of faults, CHB is reported with several FTSs. Merits and limitations of these schemes are discussed below.

Assume an oc fault on multiple units of an inverter shown in Fig. 1*a*, such that x units in phase a, y units in phase b and z units in phase c are faulty. This creates an unbalance in phase and line voltages as shown in Fig. 2*a*, where $k=1, 2, \ldots, (n-x)$ for phase a; $k=1, 2, \ldots, (n-y)$ for phase b and $k=1, 2, \ldots, (n-z)$ for phase c. In such condition, to compensate the fault, the burden of x faulty units is shared across $(n-x)$ healthy units, such that $(n-x)$ healthy units contribute the same amount of voltage as of n healthy units. Similarly for phases b and c, FTO by increasing the burden on healthy units obtains balanced phase voltages as shown in Fig. 2*b* and given in (5)–(7) [18]. From Fig. 2*b*, it can be observed that the individual voltage contributed by $(n-x)$ healthy units in phase a is different from $(n-y)$ and $(n-z)$ healthy units in phases b and c, respectively. This leads to non-uniform power distribution across all the healthy units of three phases and reflects unequal dc-link voltages which is not desired in applications such as photo voltaic, battery energy storage system, active rectifier and active power filter

$$v'_a = (n-x)\frac{n}{n-x}[m_a V_{dc}\sin\omega t] \tag{5}$$

$$v'_b = (n-y)\frac{n}{n-y}\left[m_a V_{dc}\sin\left(\omega t - \frac{2\pi}{3}\right)\right] \tag{6}$$

$$v'_c = (n-z)\frac{n}{n-z}\left[m_a V_{dc}\sin\left(\omega t + \frac{2\pi}{3}\right)\right] \tag{7}$$

Implementation of NS zero-sequence injection FTS scheme for single switch fault in phase a is shown in Fig. 3 [18]. To overcome the demerit of unequal voltage distribution across the operating units, a zero-sequence voltage component (v_{of}) is injected in phase opposition to the faulty phase as shown in Fig. 3*a*. Thus, a voltage component of $-v_{of}\sin\omega t$ is injected in each operating unit of all phases, which results in injection of zero-sequence voltage $v_{oz} = -nv_{of}\sin\omega t$ in each phase-voltage v_a', v_b' and v_c'. The injection v_{oz} shifts the neutral point of inverter from O to M as shown in Fig. 3*b* and results new set of phase voltages (v_a'', v_b'' and v_c'') as given in (8)–(10). From these new phase voltages, a balanced set of line voltages are achieved

$$v''_a = (n-1)\left[\frac{n}{n-1}(m_a V_{dc}\sin\omega t - v_{of}\sin\omega t)\right] \tag{8}$$

$$v''_b = n\left(m_a V_{dc}\sin(\omega t - 120^\circ) - v_{of}\sin\omega t\right) \tag{9}$$

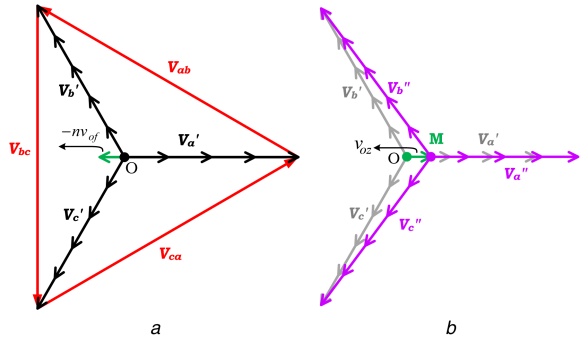

Fig. 3 *NS zero-sequence injection FTS for single unit fault in phase a*
(a) Injection of zero-sequence voltage, ***(b)*** Shifting of neutral to obtain balanced operation

$$v_c'' = n\left(m_a V_{dc}\sin(\omega t - 240^\circ) - v_{of}\sin\omega t\right) \tag{10}$$

Therefore, above analysis concludes that the magnitude of v_{oz} depends on the number of faulty units in each phase. Determination of v_{oz} reported in [18] is valid only for single unit fault and cannot be applicable for simultaneous failure of multiple switches on two or more phases [18, 22]. In addition, these NS schemes are reported only for CHB. Hence to implement NS-FTS for multiple switch faults in MLDCL, next section presents generalised equations to determine v_{oz} and modified modulating signals to control the inverter.

3 Proposed NS zero-sequence injection FTS for multiple switch faults in MLDCL inverter

This section generalises NS-FTS for simultaneous failure of multiple switches on all phases and proposes formulae to determine zero-sequence voltage for the given fault condition. The phasor diagram for implementation of NS zero-sequence injection FTS for simultaneous oc fault on multiple switches is shown in Fig. 4. In this figure, v_a', v_b' and v_c' represent the balanced phase voltages obtained from increasing burden method for various fault conditions. From Fig. 4, it can be observed that the magnitude of phase-voltages v_a', v_b' and v_c' remains to be same for different fault conditions. This leads to the non-uniform voltage distribution and power sharing among the operating units. Therefore to ensure uniform burdening among the operating units of all phases, the proposed method injects a zero-sequence voltage (v_{oz}) into the phase-voltages v_a', v_b' and v_c'. Fig. 4*a* shows the injection of v_{oz} for x number of faulty units in phase a. Fig. 4*b* presents the injection of v_{oz} for multiple faults in two phases, i.e. x and y faulty units in phases a and b, respectively. Similarly, Fig. 4*c* depicts injection of v_{oz} for multiple faults on all phases, i.e. x, y and z faulty units in phases a, b and c, respectively.

In Fig. 4*a*, as faulty units (x) are only in phase a, a voltage component of xv_{of} in phase opposition to phase a is injected into the operating units of all phases. Where v_{of} corresponds to the fraction of burden due to each faulty unit. Therefore for the considered fault case, a zero-sequence voltage $v_{oz} = -nxv_{of}\sin\omega t$ is injected into v_a', v_b' and v_c' which results new set of phase voltages (v_a'', v_b'' and v_c'') as given in (11)–(13). For simultaneous failure of x units in phase a, and y units in phase b shown in Fig. 4*b*, a voltage component of xv_{of} in phase opposition to phase a and yv_{of} in phase opposition to phase b is injected in each operating unit of all phases. Therefore, this results injection of zero-sequence voltage $v_{oz} = -nxv_{of}\sin\omega t - ny\,v_{of}\sin(\omega t - 120^\circ)$ into v_a', v_b' and v_c' resulted as in (14)–(16).

For x, y and z faulty units in phases a, b and c, respectively, injected zero-sequence voltage v_{oz} has three components of v_{of}, i.e. xv_{of}, yv_{of} and zv_{of} acting in phase opposition to phases a, b and c, respectively. This results in injection of $v_{oz} = -nxv_{of}\sin\omega t - ny\,v_{of}\sin(\omega t - 120^\circ) - nzv_{of}\sin(\omega t - 240^\circ)$ into v_a', v_b' and v_c' as shown in Fig. 4*c* and given in (17)–(19). For any fault case, injection of v_{oz} into the balanced and burdened phase-voltages v_a', v_b' and v_c' redistributes the burden of faulty units among the operating units of all phases and shifts the neutral point of the inverter from O to M. Shifting of this neutral modifies the angle and magnitude of phase voltages and obtains new set of phase-voltages v_a'', v_b'' and v_c''. However, these modified phase voltages results in balanced line voltages with equal power sharing across all healthy units.

The final extraction of generalised equation for fault tolerant modulating signals (v_a'', v_b'' and v_c'') to compensate simultaneous failure of multiple switches on all phases is given in (17)–(19). By observing (11)–(19), it can be concluded that magnitude of v_{of} plays a key role in achieving FTO of the inverter. Therefore, the magnitude v_{of} should calculated such that it results balanced line voltages and operates healthy units on all phases uniformly.

To ensure equal power distribution across all the operating units, the individual powers of each healthy basic unit in phases a, b and c should be same. To determine the power delivered by each healthy unit, the voltage across and current through each healthy unit are required. The voltage across each healthy unit is given in (20)–(22). After fault compensation, it is expected that the line currents become balanced as shown in (23)–(25). Therefore, the power delivered by each healthy basic unit in phases a, b and c are calculated over one fundamental time period as given in (26)–(31). By equating these powers as shown in (32)–(34), magnitude of v_{of} for any fault condition is obtained and is given in (35).

For x faulty units in phase a:

$$\begin{aligned} v''_a &= (n-x)\left[\frac{n}{n-x}(m_a V_{dc}\sin\omega t)\right] + v_{oz} \\ &= (n-x)\left[\frac{n}{n-x}(m_a V_{dc}\sin\omega t - x\,v_{of}\sin\omega t)\right] \end{aligned} \tag{11}$$

$$\begin{aligned} v''_b &= nm_a V_{dc}\sin(\omega t - 120^\circ) + v_{oz} \\ &= n\left[m_a V_{dc}\sin(\omega t - 120^\circ) - xv_{of}\sin\omega t\right] \end{aligned} \tag{12}$$

$$\begin{aligned} v_c'' &= n\,m_a V_{dc}\sin(\omega t - 240^\circ) + v_{oz} = \\ &\quad n\left[m_a V_{dc}\sin(\omega t - 240^\circ) - xv_{of}\sin\omega t\right] \end{aligned} \tag{13}$$

If x and y units are faulty in phases a and b then (see (14))

$$\begin{aligned} v''_b &= (n-y)\left[\frac{n}{n-y}(m_a V_{dc}\sin(\omega t - 120^\circ))\right] + v_{oz} \\ &= (n-y)\left[\frac{n}{n-y}(m_a V_{dc}\sin(\omega t - 120^\circ)\right. \\ &\quad \left.-(x\,v_{of}\sin\omega t + y\,v_{of}\sin(\omega t - 120^\circ))\right] \end{aligned} \tag{15}$$

$$\begin{aligned} v_c'' &= n\,m_a V_{dc}\sin(\omega t - 240^\circ) + v_{oz} = \\ &n\left[m_a V_{dc}\sin(\omega t - 240^\circ) - (x\,v_{of}\sin\omega t + y\,v_{of}\sin(\omega t - 120^\circ))\right] \end{aligned} \tag{16}$$

For simultaneous failure of multiple switches on all phases

$$\begin{aligned} v''_a &= (n-x)\left[\frac{n}{n-x}m_a V_{dc}\sin\omega t\right] + v_{oz} \\ &= (n-x)\left[\frac{n}{n-x}(m_a V_{dc}\sin\omega t - xv_{of}\sin\omega t\right. \\ &\quad \left.-y\,v_{of}\sin(\omega t - 120^\circ) - z\,v_{of}\sin(\omega t - 240^\circ))\right] \end{aligned} \tag{17}$$

$$\begin{aligned} v''_b &= (n-y)\left[\frac{n}{n-y}m_a V_{dc}\sin(\omega t - 120^\circ)\right] + v_{oz} \\ &= (n-y)\left[\frac{n}{n-y}(m_a V_{dc}\sin(\omega t - 120^\circ) - xv_{of}\sin\omega t\right. \\ &\quad \left.-y\,v_{of}\sin(\omega t - 120^\circ) - z\,v_{of}\sin(\omega t - 240^\circ))\right] \end{aligned} \tag{18}$$

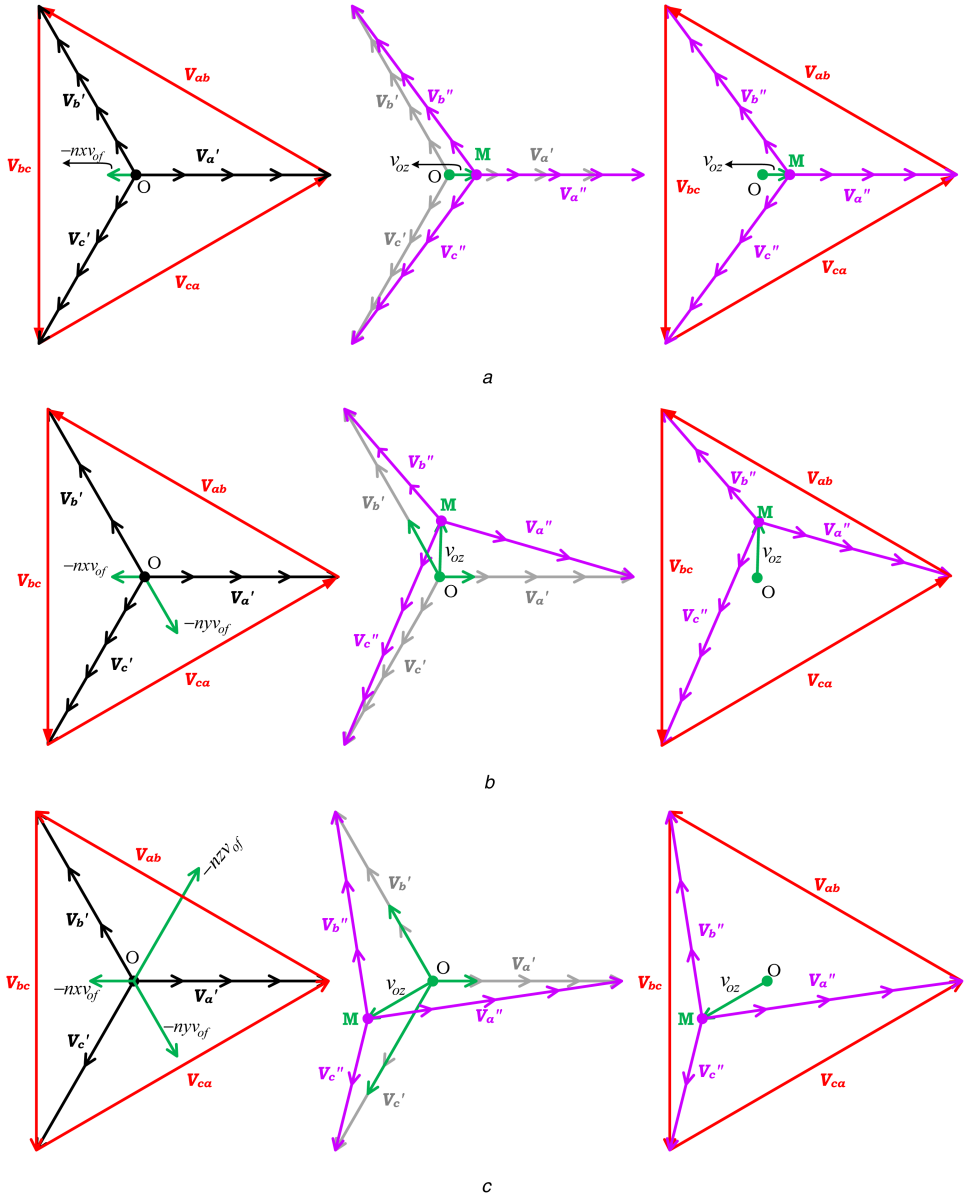

Fig. 4 *Phasor diagram of NS-FTS with zero-sequence injection (considering $x < y < z$)*
(a) *x faulty units in phase a,* ***(b)*** *x and y faulty units in phases a and b, respectively,* ***(c)*** *x, y and z faulty units in phases a, b and c, respectively*

$$\begin{aligned} v''_c &= (n-z)\left[\frac{n}{n-z}m_a V_{dc}\sin(\omega t - 240^\circ)\right] + v_{oz} \\ &= (n-z)\left[\frac{n}{n-z}(m_a V_{dc}\sin(\omega t - 240^\circ) - x v_{of}\sin\omega t \right. \\ &\quad \left. - y\, v_{of}\sin(\omega t - 120^\circ) - z\, v_{of}\sin(\omega t - 240^\circ))\right] \end{aligned} \tag{19}$$

From (17)–(19) after the injection of v_{oz}, the voltage produced by any healthy unit can be given as (see (20))

$$\begin{aligned} v''_{bk} &= \left[\frac{n}{n-y}(m_a V_{dc}\sin(\omega t - 120^\circ) - x v_{of}\sin\omega t \right. \\ &\quad \left. - y\, v_{of}\sin(\omega t - 120^\circ) - z\, v_{of}\sin(\omega t - 240^\circ))\right] \end{aligned} \tag{21}$$

$$\begin{aligned} v''_{ck} &= \left[\frac{n}{n-z}(m_a V_{dc}\sin(\omega t - 240^\circ) - x v_{of}\sin\omega t \right. \\ &\quad \left. - y\, v_{of}\sin(\omega t - 120^\circ) - z\, v_{of}\sin(\omega t - 240^\circ))\right] \end{aligned} \tag{22}$$

where $k = 1, 2, \ldots, (n-x)$ for phase a; $1, 2, \ldots, (n-y)$ for phase b and $1, 2, \ldots, (n-z)$ for phase c.

Let the resultant balanced line–line currents are

$$\begin{aligned} v''_a &= (n-x)\left[\frac{n}{n-x}(m_a V_{dc}\sin\omega t)\right] + v_{oz} \\ &= (n-x)\left[\frac{n}{n-x}(m_a V_{dc}\sin\omega t - (x\, v_{of}\sin\omega t + y\, v_{of}\sin(\omega t - 120^\circ)))\right] \end{aligned} \tag{14}$$

$$\begin{aligned} v''_{ak} &= \left[\frac{n}{n-x}(m_a V_{dc}\sin\omega t - x v_{of}\sin\omega t - y\, v_{of}\sin(\omega t - 120^\circ) \right. \\ &\quad \left. - z\, v_{of}\sin(\omega t - 240^\circ))\right] \end{aligned} \tag{20}$$

$$i_a(t) = I\sqrt{2}\sin\omega t \tag{23}$$

$$i_b(t) = I\sqrt{2}\sin(\omega t - 120^\circ) \tag{24}$$

$$i_c(t) = I\sqrt{2}\sin(\omega t - 240^\circ) \tag{25}$$

The output electric power of each healthy basic unit in phase a is given by (see (26))

(see (27))

$$p_{ak} = \frac{1}{T}\left(\frac{n\ I\sqrt{2}}{n-x}\right)\left(\frac{\pi}{\omega}\right)\left(V_{\rm dc}m_{\rm a} - x\,v_{of} + \frac{y\,v_{of}}{2} + \frac{z\,v_{of}}{2}\right) \tag{28}$$

$$p_{ak} = \left(\frac{n}{n-x}\right)I\frac{1}{\omega\sqrt{2}}\left[V_{\rm dc}\,m_{\rm a} - x\,v_{of} + \frac{y\,v_{of}}{2} + \frac{z\,v_{of}}{2}\right] \quad \text{for } k = 1, 2, 3, \ldots, (n-x) \tag{29}$$

Similarly, the output electric power of each healthy basic unit in phases b and c is given as (see (30))

(see (31))

To ensure uniform burden among all healthy basic units, v_{of} is selected such a way that these powers ($p_{ak,}$ p_{bk} and p_{ck}) are equal. To determine v_{of}, (32) is considered

$$p_{ak} + p_{bk} = 2p_{ck} \tag{32}$$

Substituting (29)–(31) into (32), v_{of} is obtained in (35) (see (33))

(see (34))

$$v_{of} = \frac{2m_{\rm a}V_{\rm dc}}{3n - (x + y + z)} \tag{35}$$

Substituting (35) into (17)–(19), results fault tolerant modulating signals (36)–(38) in terms of x, y, z, n, $m_{\rm a}$ and $V_{\rm dc}$

$$v''_a = (n-x)\left[\frac{\sqrt{3}nm_{\rm a}V_{\rm dc}\sqrt{3(n-x)^2 + (y-z)^2}}{(n-x)(3n-x-y-z)}\sin\left(\omega t + \sin^{-1}\left(\frac{(y-z)}{\sqrt{3(n-x)^2 + (y-z)^2}}\right)\right)\right] \tag{36}$$

(see (37))

(see (38))

From (36)–(38), it can be observed that during FTO the pre-fault $m_{\rm a}$ is multiplied by a different scaling factor as given in (39)–(41). This increases $m_{\rm a}$ of the modified modulating signals ($m_{\rm a}$*) and may drive the inverter into overmodulation. This results in reduced RMS values of line voltages and lower-order harmonics. Therefore to avoid overmodulation during fault condition, if the inverter application permits, the modulation index can be suitability adjusted as given in (42)

$$m^*_{\rm a(a-ph)} = \frac{\sqrt{3}n\sqrt{3(n-x)^2 + (y-z)^2}}{(n-x)(3n-x-y-z)}m_{\rm a} \tag{39}$$

$$\begin{aligned} p_{ak} &= \frac{1}{T}\int_0^{2\pi/\omega} v''_{ak}(t)\,i_a(t)\mathrm{d}t \\ &= \frac{1}{T}\left(\frac{n}{n-x}\right)\int_0^{2\pi/\omega}\left(m_{\rm a}V_{\rm dc}\sin\omega t - x\,v_{of}\sin\omega t - y\,v_{of}\sin(\omega t - 120^\circ)\right. \\ &\quad \left. - z\,v_{of}\sin(\omega t - 240^\circ)\right)\sqrt{2}\,I\sin\omega t\mathrm{d}t \end{aligned} \tag{26}$$

$$\begin{aligned} p_{ak} &= \frac{1}{T}\left(\frac{n\,I\sqrt{2}}{n-x}\right)\int_0^{2\pi/\omega}\left(m_{\rm a}V_{\rm dc} - x\ v_{of}\right)\sin^2\omega t - y\,v_{of}\sin(\omega t - 120^\circ)\sin\omega t \\ &\quad - z\,v_{of}\sin(\omega t - 240^\circ)\sin\omega t\mathrm{d}t \end{aligned} \tag{27}$$

$$\begin{aligned} p_{bk} &= \frac{1}{T}\int_0^{2\pi/\omega} v''_{bk}(t)\,i_b(t)\mathrm{d}t \\ &= \frac{n}{n-y}I\frac{1}{\omega\sqrt{2}}\left[V_{\rm dc}\,m_{\rm a} - y\,v_{of} + \frac{x\,v_{of}}{2} + \frac{z\,v_{of}}{2}\right] \quad \text{for } k = 1, 2, 3, \ldots, (n-y) \end{aligned} \tag{30}$$

$$\begin{aligned} p_{ck} &= \frac{1}{T}\int_0^{2\pi/\omega} v''_{ck}(t)\,i_c(t)\mathrm{d}t \\ &= \frac{n}{n-z}I\frac{1}{\omega\sqrt{2}}\left[V_{\rm dc}\,m_{\rm a} - z\,v_{of} + \frac{y\,v_{of}}{2} + \frac{x\,v_{of}}{2}\right] \quad \text{for } k = 1, 2, 3, \ldots, (n-z) \end{aligned} \tag{31}$$

$$\begin{aligned} &\frac{1}{n-x}\left[m_{\rm a}V_{\rm dc} - x\,v_{of} + \frac{y\,v_{of}}{2} + \frac{z\ v_{of}}{2}\right] + \frac{1}{n-y}\left[m_{\rm a}V_{\rm dc} - y\,v_{of} + \frac{x\,v_{of}}{2} + \frac{zv_{of}}{2}\right] \\ &= \frac{2}{n-z}\left[m_{\rm a}V_{\rm dc} - z\,v_{of} + \frac{y\,v_{of}}{2} + \frac{xv_{of}}{2}\right] \end{aligned} \tag{33}$$

$$\begin{aligned} v_{of} &= \frac{m_{\rm a}V_{\rm dc}\left[\frac{1}{(n-x)} + \frac{1}{(n-y)} - \frac{2}{(n-z)}\right]}{\left[(x+y-2z)\frac{1}{(n-z)}\right] + \left[\left(x - \frac{y}{2} - \frac{z}{2}\right)\frac{1}{(n-x)}\right] + \left[\left(y - \frac{x}{2} - \frac{z}{2}\right)\frac{1}{(n-y)}\right]} \\ &= \frac{[(x+y-2z)n - (2xy - yz - zx)]2\,m_{\rm a}V_{\rm dc}}{[(x+y-2z)n - (2xy - yz - zx)]\,(3n - x - y - z)} \end{aligned} \tag{34}$$

$$m^*_{\mathrm{a(b-ph)}} = \frac{n\sqrt{9(-n-x+y+z)^2+3(-3n+x+3y-z)^2}}{2(n-y)(3n-x-y-z)} m_{\mathrm{a}} \quad (40)$$

$$m^*_{\mathrm{a(c-ph)}} = \frac{n\sqrt{9(-n-x+y+z)^2+3(3n-x+y-3z)^2}}{2(n-z)(3n-x-y-z)} m_{\mathrm{a}} \quad (41)$$

$$m^*_{\mathrm{a}} = \min\left(m_{\mathrm{a}^*(a-ph)} \le 1, m_{\mathrm{a}^*(b-ph)} \le 1 \text{ and } m_{\mathrm{a}^*(c-ph)} \le 1\right) \quad (42)$$

In next sections, the ability of these proposed generalised equations in obtaining FTO for multiple switch/unit faults in MLDCL is demonstrated with simulation and experimental studies. In simulation study, to show the wide variations in fault conditions, a 15-level MLDCL is considered. Owing to large number of switching devices in 15-level MLDCL, in experimental study only nine-level inverter is considered. However, to corroborate experimental studies, a comprehensive comparison between nine-level simulation and experimental studies are presented under different fault conditions.

4 Simulation studies of proposed fault tolerant scheme for MLDCL

In order to demonstrate the proposed FTS, a 3.3 kV, 200 kVA, 50 Hz and 15-level MLDCL is considered with seven basic units in each phase and each unit is fed from an isolated 385 V dc supply. To obtain uniform power sharing among all basic units, a carrier rotation-based reduced carrier PWM technique [24, 25] with 2.5 kHz switching frequency (f_{cr}) is used to control this MLDCL configuration. It should be noted that during fault compensation, the switching pulses to the faulted unit are seized and the carriers are rotated across the remaining healthy units of the phase. Modulating signals for phase voltages to compensate the appeared fault are extracted from (36)–(38).

To observe the efficacy of the proposed method, the following simulation studies are performed:

i. *One basic unit failure*: Failure of one unit in phase *a* ($x = 1, y = 0$ and $z = 0$)
ii. *Three basic unit failure*: Failure of two units in phase *a* and one unit in phase *b* ($x = 2, y = 1$ and $z = 0$)
iii. *Six basic unit failure*: Failure of two units in phase *a*, three units in phase *b* and one unit in phase *c* ($x = 2, y = 3$ and $z = 0$)

In simulation study, it is assumed that for first two cycles, the inverter is healthy. At 0.04 s, fault is assumed to be occurred and the effect of fault is studied for subsequent two cycles. At 0.08 s FTS is enabled.

Case i: For single unit failure ($x = 1, y = 0$ and $z = 0$).

The obtained simulation waveforms of phase-voltage, line voltage and line currents are shown in Fig. 5*a* and their corresponding RMS values are shown in Fig. 5*b*. From Figs. 5*a* and *b*, under healthy condition, the inverter is in balanced operation with phase and line-voltage RMS values of 1722 and 2974 V, respectively.

At 0.04 s, an oc fault in one basic unit of phase *a* is occurred and this results in unbalanced phase and line voltages as shown in Fig. 5*a*. This unbalance in their RMS values can be observed in Fig. 5*b*. The RMS values unbalanced phase voltages are 1470, 1722 and 1722 V, line voltages are 2765, 2780 and 2795 V and line currents are 28.4, 30.6 and 30.4 A. At 0.08 s FTS is enabled and new modulating signals given in (43) are generated by substituting the values of x, y, z, m_{a} and n in modulating signals given in (36)–(38). The balanced operation of inverter under faulted condition can be observed from Figs. 5*a* and *b*. After fault compensation, the unbalanced phase voltages (with RMS values of 1522, 1814 and 1814 V) produced a balanced set of line voltage and currents with RMS values of 2974 V and 31.4 A, respectively

$$\left.\begin{aligned} v''_a &= 5.67V_{\mathrm{dc}}\sin\omega t \\ v''_b &= 6.60V_{\mathrm{dc}}\sin(\omega t - 124.1^\circ) \\ v''_c &= 6.60V_{\mathrm{dc}}\sin(\omega t + 124.1^\circ) \end{aligned}\right\} \quad (43)$$

Case ii: For three-unit failure ($x = 2, y = 1$ and $z = 0$).

Simulated waveforms and their RMS values for this fault condition are shown in Figs. 5*c* and *d*, respectively. In Figs. 5*c* and *d*, during the fault condition, the unbalance in phase voltages (1277, 1482 and 1722 V), line voltages (2356, 2768 and 2615 V) and line currents (25, 27 and 26 A) are observed. During FTO, the modified modulating signals given in (44) produces balanced line voltages (~2928 V) and line currents (~30.9 A) from unbalanced phase voltages (1423, 1718, 1986 V). It is to be noted that even though the inverter is desired to operate in undermodulation ($m_{\mathrm{a}} = 0.9$); however with FTO, the modulating signals are driven to overmodulation ($m_{\mathrm{a}}^* = 1.05$, 1.06 and 1.05) to compensate the burden of faulty units

$$\left.\begin{aligned} v''_a &= 5.28\ V_{\mathrm{dc}}\sin(\omega t + 6.6^\circ) \\ v''_b &= 6.40\ V_{\mathrm{dc}}\sin(\omega t - 130.9^\circ) \\ v''_c &= 7.37\ V_{\mathrm{dc}}\sin(\omega t + 124.7^\circ) \end{aligned}\right\} \quad (44)$$

Case iii: For six-unit failure ($x = 2, y = 3$ and $z = 1$).

During FTO, high value of pre-fault m_{a} with increased number of faulted units, the burden on healthy units further increases and drives the modulating signals to high overmodulation. In such a case, the RMS value of the line voltages and currents are almost same but their waveforms are distorted. This can be observed by considering six faulty units. For $m_{\mathrm{a}} = 0.9$ and 0.7, modified modulating signals for the assumed fault condition are given in (45) and (46), respectively. Simulated waveforms and their RMS values for this fault condition are shown in Figs. 6*a* and *b* for $m_{\mathrm{a}} = 0.9$ and in Figs. 6*c* and *d* for $m_{\mathrm{a}} = 0.7$, respectively.

With $m_{\mathrm{a}} = 0.9$, during FTO the inverter is operated in overmodulation ($m_{\mathrm{a}}^* = 1.29$, 1.27 and 1.26). This results in distorted shape for line-voltage waveforms but achieves almost equal RMS line voltages (~2630 V) and currents (~27.8 A), as shown in Figs. 6*a* and *b*. However, with of $m_{\mathrm{a}} = 0.7$, the modified modulating signals are within the linear range of m_{a}^* (1.0, 0.98 and 0.98) and obtain balanced line voltages and currents, both in terms of wave shape and RMS values (2315 V and 24.4 A) as shown in Figs. 6*c* and *d*

$$v''_b = (n-y)\left[\frac{nm_{\mathrm{a}}V_{\mathrm{dc}}\sqrt{9(-n-x+y+z)^2+3(-3n+x+3y-z)^2}}{2(n-y)(3n-x-y-z)} \sin\left(\omega t - \pi - \sin^{-1}\left(\frac{\sqrt{3}(-3n+x+3y-z)}{\sqrt{9(-n-x+y+z)^2+3(-3n+x+3y-z)^2}}\right)\right)\right] \quad (37)$$

$$v''_c = (n-z)\left[\frac{nm_a V_{dc}\sqrt{9(-n-x+y+z)^2+3(3n-x+y-3z)^2}}{2(n-z)(3n-x-y-z)} \sin\left(\omega t + \pi - \sin^{-1}\left(\frac{\sqrt{3}\,(3n-x+y-3z)}{\sqrt{9\,(-n-x+y+z)^2+3\,(3n-x+y-3z)^2}}\right)\right)\right] \quad (38)$$

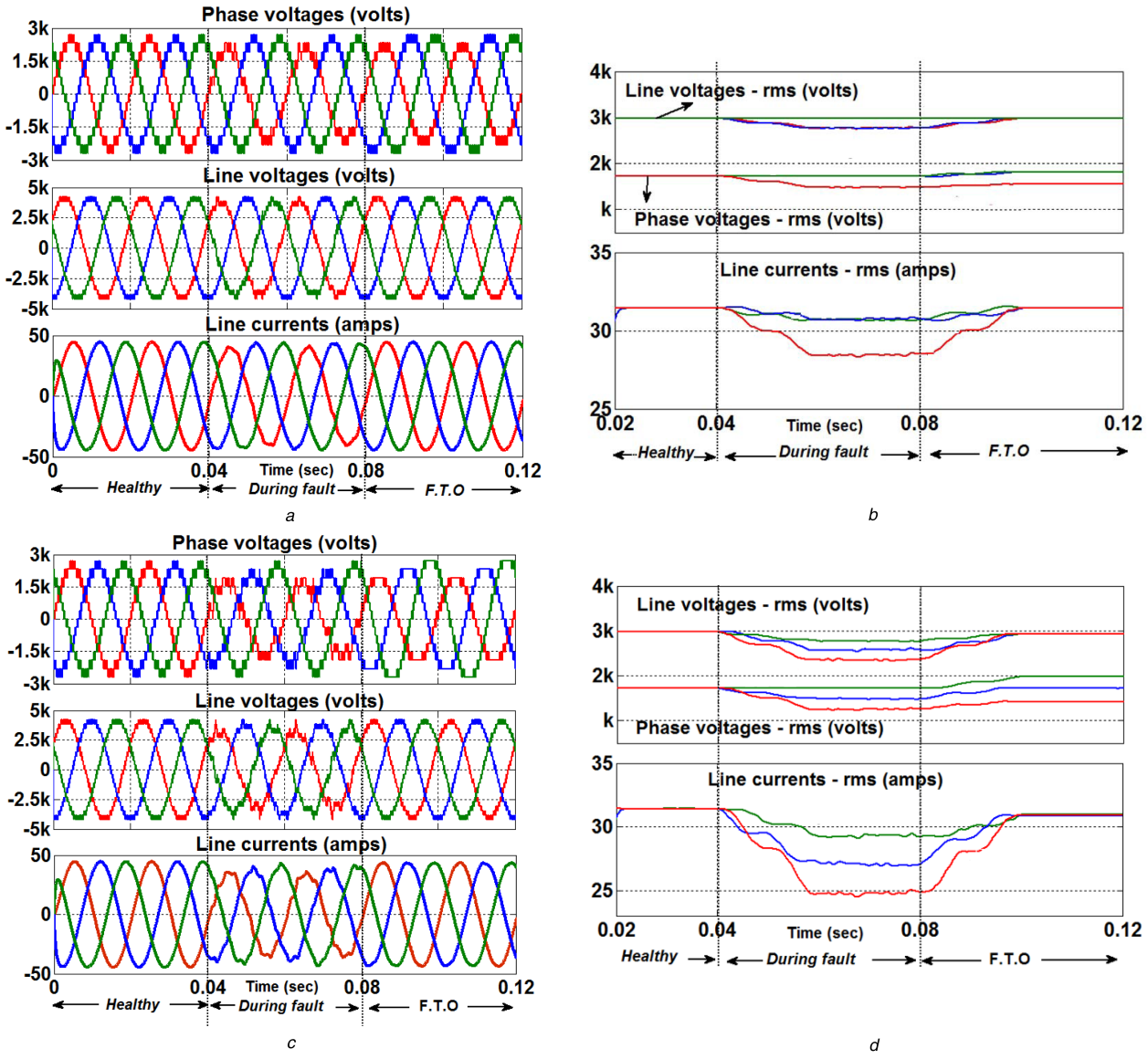

Fig. 5 *Simulation results of phase voltage, line voltage and line current waveforms with their corresponding RMS values for healthy, faulty and fault with compensation using proposed FTS for one- and three-unit failure*

(a) Waveforms for $x = 1$, $y = 0$ and $z = 0$ with $m_a = 0.9$, ***(b)*** RMS values for $x = 1$, $y = 0$ and $z = 0$ with $m_a = 0.9$, ***(c)*** Waveforms for $x = 2$, $y = 1$ and $z = 0$ with $m_a = 0.9$, ***(d)*** RMS values for $x = 1$, $y = 0$ and $z = 0$ with $m_a = 0.9$

$$\left.\begin{aligned} v''_a &= 6.46V_{dc}\sin(\omega t + 13^\circ) \\ v''_b &= 5.08V_{dc}\sin(\omega t - 153^\circ) \\ v''_c &= 7.60V_{dc}\sin(\omega t + 114.6^\circ) \end{aligned}\right\} \quad (45)$$

$$\left.\begin{aligned} v''_a &= 5.02V_{dc}\sin(\omega t + 13^\circ) \\ v''_b &= 3.95V_{dc}\sin(\omega t - 153^\circ) \\ v''_c &= 5.90V_{dc}\sin(\omega t + 114.6^\circ) \end{aligned}\right\} \quad (46)$$

Ability of the proposed generalised scheme to obtain FTO for various fault conditions with different values of m_a is presented in Table 3. From this table, it can be observed that high value of pre-fault m_a with increased number of faulty units the inverter may produce balanced line voltages. However, it may drive inverter to overmodulation and may not reach its pre-fault voltage. Therefore, to reduce the risk of going to high overmodulation, the inverter m_a should be appropriately adjusted.

Power distribution during the fault compensation: Apart from the balanced line voltages and currents during FTO, equal power sharing among the basic units can also be achieved. Fig. 7 shows the power delivered by all the basic units for the above assumed fault cases. From Fig. 7, it can be observed that the power delivered by all the basic units during healthy condition is same; however, during the fault condition, the power sharing among the healthy units is disturbed and the power delivered by faulty units is zero. With FTO, the power delivered by all healthy units is uniform and slightly increased as the burden of faulted units is shared across the healthy units.

5 Experimental results

To validate the efficacy of the proposed FTS experimentally, a nine-level, three-phase, 170 V and 2 kVA IGBT-based MLDCL is developed in the laboratory. The required isolated dc supplies are obtained from single-phase isolation transformer with diode bridge rectifier and filter capacitor. Each dc source is maintained at 30 V and a three-phase star-connected 1 kW with 0.8 power factor lagging load is used for experimentation. The experimental parameters are given in Table 4. The proposed FTS is implemented on OPAL-RT controller and obtained firing pulses are given to the developed inverter. To observe the efficacy of the proposed FTS, the following experimental studies are performed:

Case 1: One basic unit failure: with one unit in phase *a* ($x = 1$, $y = 0$ and $z = 0$)

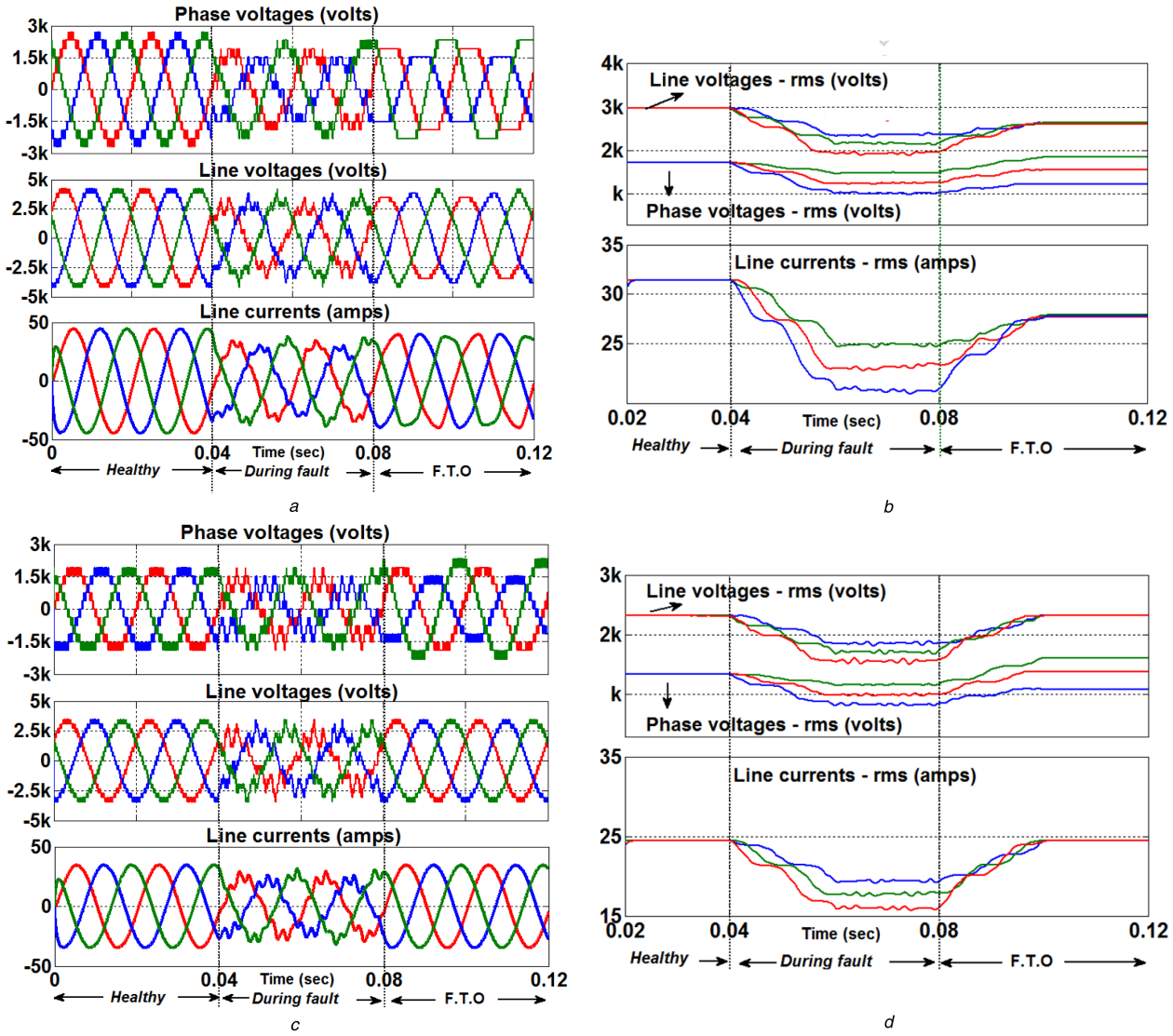

Fig. 6 *Simulation results of phase-voltage, line-voltage and line-current waveforms with their corresponding RMS values for healthy, faulty and fault with compensation using proposed FTS for six unit failure*

(a) Waveforms for $x = 2$, $y = 3$ and $z = 1$ with $m_a = 0.9$, ***(b)*** RMS values for $x = 2$, $y = 3$ and $z = 1$ with $m_a = 0.9$, ***(c)*** Waveforms for $x = 2$, $y = 3$ and $z = 1$ with $m_a = 0.7$, ***(d)*** RMS values for $x = 2$, $y = 3$ and $z = 1$ with $m_a = 0.7$

Case 2: Three basic unit failure: with two units in phase *a* and one unit in phase *b* ($x = 2$, $y = 1$ and $z = 0$)

Case 3: Four basic unit failure: with two units in phase *a*, one unit in phases *b* and *c*. ($x = 2$, $y = 1$ and $z = 1$)

Fig. 8 shows the experimental results for fault compensation of above case studies for $m_a = 0.9$. Experimental variation in their phase and line voltages and currents for case studies 1, 2 and 3 is shown in Figs. 8*a*–*c*, respectively. In Fig. 8, the balanced operation of inverter during healthy condition is observed in first cycle. In subsequent two cycles, the unbalance in voltages and currents due to fault initiation are clearly observed. The FTS is enabled after two cycles of fault occurrence. After fault compensation, balanced set of line voltages and currents are clearly observed. From Figs. 8*b* and *c*, with increase in number of faulty units, the proposed FTS drives the inverter to overmodulation. This leads to a little distortion (nevertheless, the RMS values are almost same) in compensated line voltages and currents as discussed in Fig. 6*a*. Experimental variation in their phase and line voltages and currents for case studies 2 and 3 with $m_a = 0.7$ is shown in Figs. 9*a* and *b*, respectively. From this figure, it can be observed that the modified modulating signals are just over the linear range and obtains balanced line voltages and currents, both in terms of wave shape and RMS values and in compliance with simulation results are shown in Fig. 6*b*.

Experimental harmonic performance of the phase and line voltages of nine-level MLDCL in healthy condition is shown in Fig. 10. Phase and line-voltages harmonic spectra for pre-fault condition (healthy condition) for $m_a = 0.9$ and 0.7 is shown in Figs. 10*a* and *b*, respectively. For $m_a = 0.9$, phase and line-voltage THD is found to be 3.5 and 2.9%, respectively. Similarly, for $m_a = 0.7$, phase and line-voltage THD is found to be 4.2 and 3.5%, respectively.

Experimental phase and line-voltage THD recorded after compensation of 2-1-0 fault using the proposed FTS is shown in Fig. 11. The harmonic spectra of phase and line voltages for $m_a = 0.9$ and 0.7 are shown in Figs. 11*a* and *b*, respectively. Effect of 2-1-0 fault on phase and line voltages with high m_a (0.9) can be verified from Fig. 11*a*. As the inverter drives to overmodulation, a significant increase in THDs of phase and line voltage is observed after fault compensation. This is due to the presence of lower-order harmonics. The obtained THD values are 12.4, 9.8 and 6.5% for phase and 7.7, 7.0 and 4.4% for line voltages.

With reduction in m_a to 0.7, inverter operates in linear range and tends to compensate the fault effectively. From Fig. 11*b*, THD of compensated phase voltages is 5.1, 4.2 and 3.6%, respectively. Also, the THD of compensated line voltages is 3.6. 3.7, 3.2%, respectively, which is nearly equal to pre-fault performance as shown in Fig. 10*b* for $m_a = 0.7$. To further verify the efficacy of the proposed FTS scheme, simulation studies are performed on nine-

Table 3 RMS values of phase and line voltages for various fault conditions after fault compensation

x–y–z		Phase voltages (rms, V)			Line voltages (rms, V)		
	m_a	V_a	V_b	V_c	V_{ab}	V_{bc}	V_{ca}
0–0–0 (healthy)	0.9	1722	1722	1722	2974	2974	2974
	0.8	1533	1533	1533	2645	2645	2645
	0.7	1533	1533	1533	2315	2315	2316
1–0–1	0.9	1639	1902	1639	2974	2974	2974
	0.8	1459	1691	1459	2645	2645	2645
	0.7	1280	1483	1280	2316	2316	2316
2–0–0	0.9	1362	1925	1925	2973	2973	2973
	0.8	1214	1714	1715	2645	2645	2645
	0.7	1065	1503	1503	2316	2316	2316
3–0–0	0.9	1138	2016	2016	2914	2903	2914
	0.8	1029	1839	1839	2645	2645	2645
	0.7	902	1611	1611	2316	2316	2316
3–0–1	0.9	1179	2058	1786	2845	2827	2819
	0.8	1097	1914	1677	2645	2639	2636
	0.7	965	1677	1478	2315	2315	2316
2–3–0	0.9	1535	1224	2103	2685	2740	2737
	0.8	1463	1985	1985	2557	2594	2587
	0.7	1333	1054	1764	2317	2314	2316
2–2–2	0.9	1539	1539	1539	2652	2652	2652
	0.8	1469	1469	1469	2537	2537	2537
	0.7	1343	1343	1343	2316	2316	2316

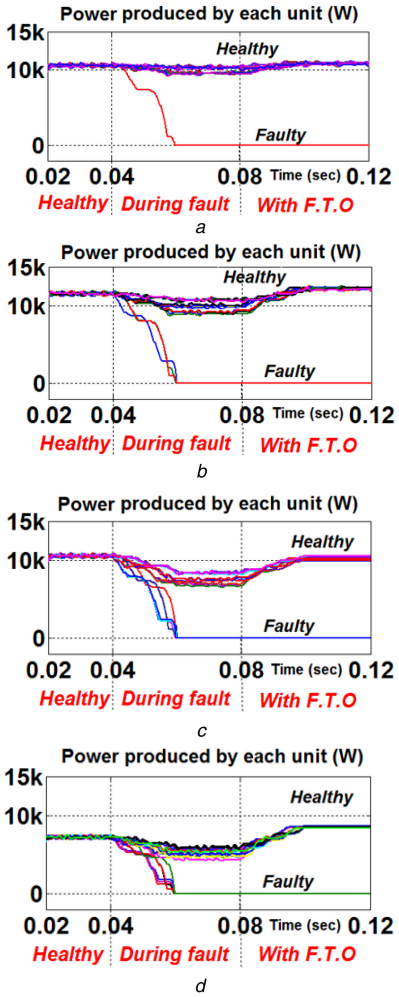

Fig. 7 *Power delivered by all the basic units of 15-level MLDCL under various fault conditions*

(a) $x = 1$, $y = 0$ and $z = 0$ with $m_a = 0.9$, ***(b)*** $x = 2$, $y = 1$ and $z = 0$ with $m_a = 0.9$, ***(c)*** $x = 2$, $y = 3$ and $z = 1$ with $m_a = 0.9$, ***(d)*** $x = 2$, $y = 3$ and $z = 1$ with $m_a = 0.7$

level MLDCL inverter with same experimental parameters. A comprehensive comparison between nine-level simulation and experimental studies is presented in Table 5. From this table, it can be observed that the simulation results are in good agreement with experimental results and further supports the effectiveness of the proposed FTS. It should be noted that in experimental harmonic spectra, up to 49th order harmonics are considered.

6 Conclusion

In this paper, NS-FTS is proposed for compensating multiple oc faults in RSC-based MLDCL topology. Mathematical equations for obtaining the modified modulating signals for achieving FTO for a generalised fault condition are derived. Simulation and experimental studies are carried out under various fault conditions on 15- and nine-level MLDCL, respectively. From these results, the following conclusions are derived:

i. The unbalanced phase voltages produced a balanced set of line voltages and currents with equal RMS values.
ii. During FTO, if the inverter is operating in overmodulation, then it results in lower-order harmonics in the compensated line voltages. However, their RMS values remain almost equal.
iii. This scheme achieved fault compensation for multiple faulty units along with uniform power distribution among all the healthy units.
iv. Uniform power distribution among the healthy units will ensure balancing of dc capacitor voltages and equal heat distribution even under fault conditions.

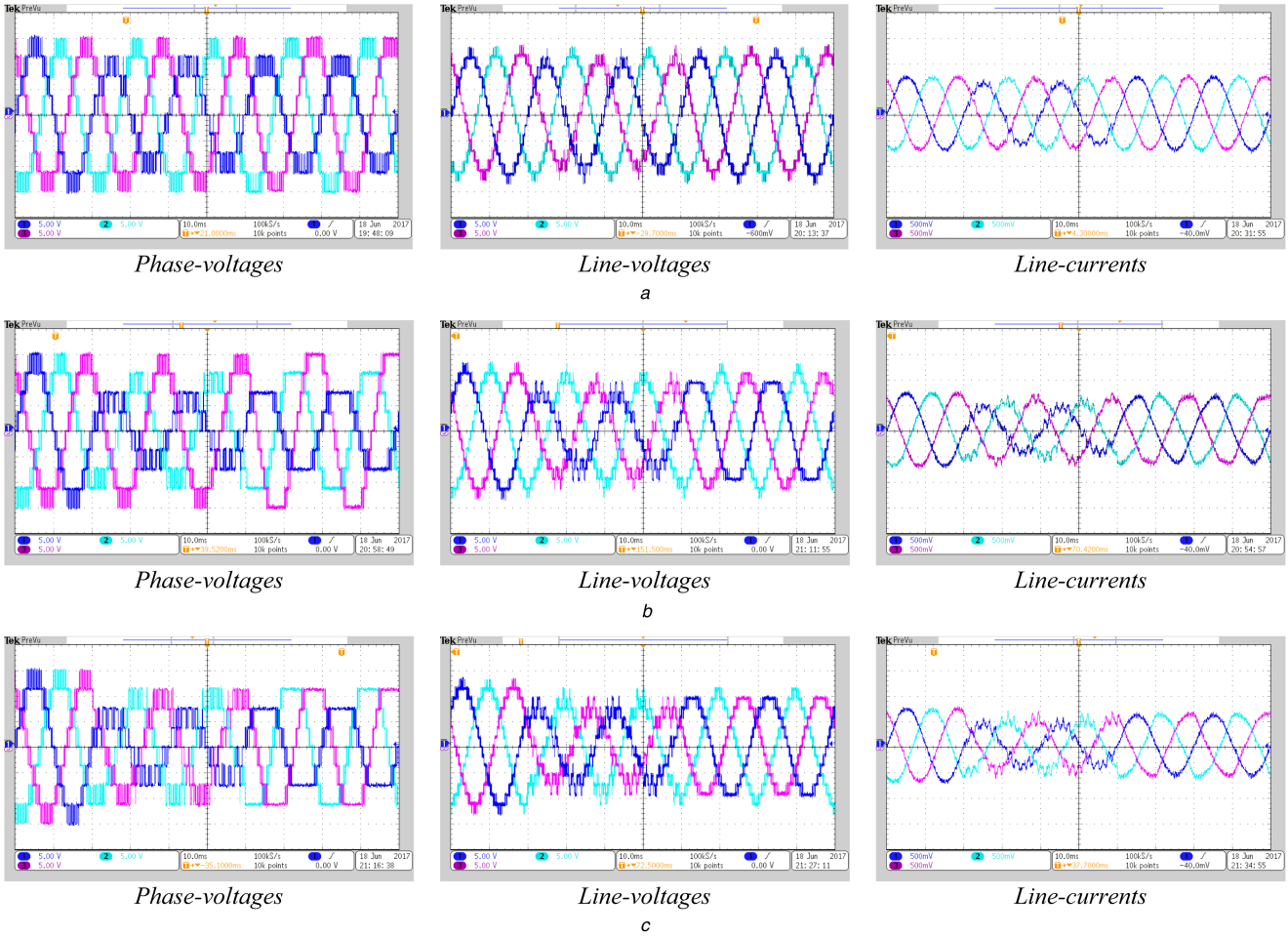

Fig. 8 *Experimental results of three-phase nine-level MLDCL with proposed FTS with multiple switch faults for $m_a = 0.9$. (Scale: X-axis 10 ms/div. and Y-axis: 40 V/div. for phase voltages, 80 V/div. for line voltages and 5 A/div. for line currents.)*
(a) Waveforms for $x = 1$, $y = 0$ and $z = 0$., ***(b)*** Waveforms for $x = 2$, $y = 1$ and $z = 0$., ***(c)*** Waveforms for $x = 2$, $y = 1$ and $z = 1$

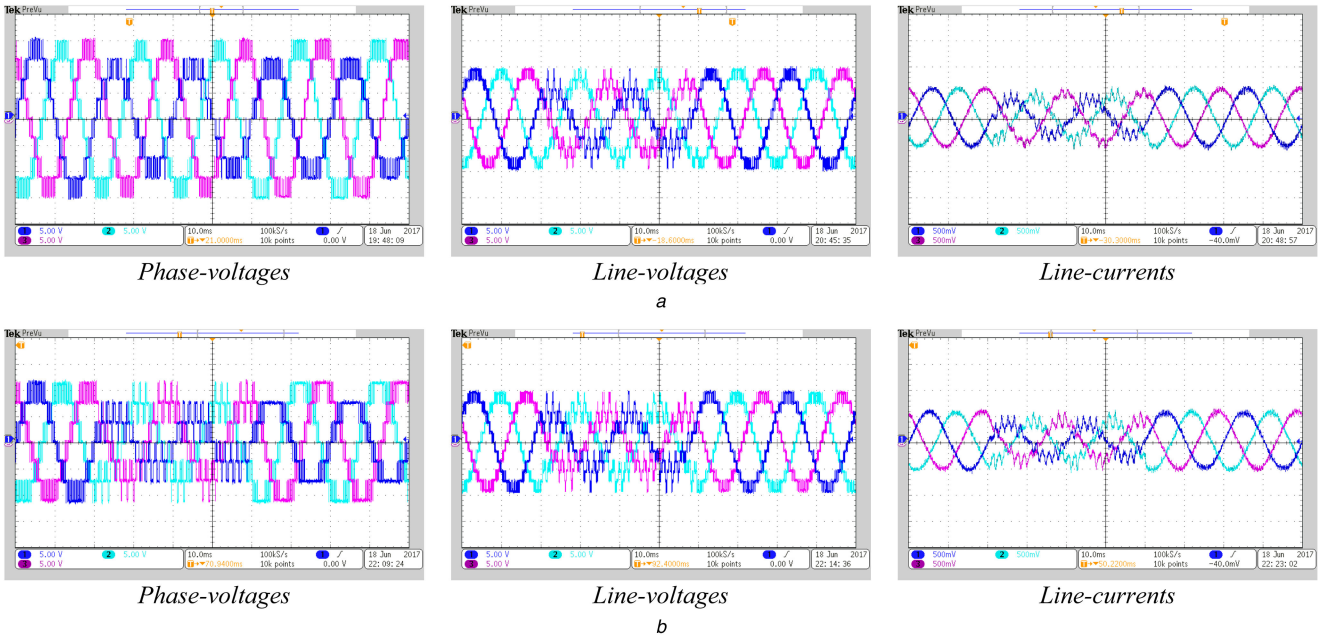

Fig. 9 *Experimental results of three-phase nine-level MLDCL with proposed FTS with multiple switch faults for $m_a = 0.7$. (Scale: X-axis 10 ms/div. and Y-axis: 40 V/div. for phase voltages, 80 V/div. for line voltages and 5 A/div. for line currents.)*
(a) Waveforms for $x = 2$, $y = 1$ and $z = 0$., ***(b)*** Waveforms for $x = 2$, $y = 1$ and $z = 1$

Table 4 Experimental parameters

Circuit	Component
30 V isolated dc power supplies (12 No.)	bridge rectifier (KBPC3510) with filter capacitance (450 V, 4700 μF)
nine-level, three-phase MLDCL	Two modules of generalised converter with 24 IGBTs each (only 36 switches are used) IGBT model and rating (IKW40T120, 40 A and 1200 V)
switching frequency (f_{cr})	2.5 kHz
load	three-phase 1 kW *RL* load with 0.8 pf lagging
controller (to obtain firing signals for IGBTs)	OPAL-RT (OP4500 RT Lab RCP/HIL system) sampling time (40 μs)

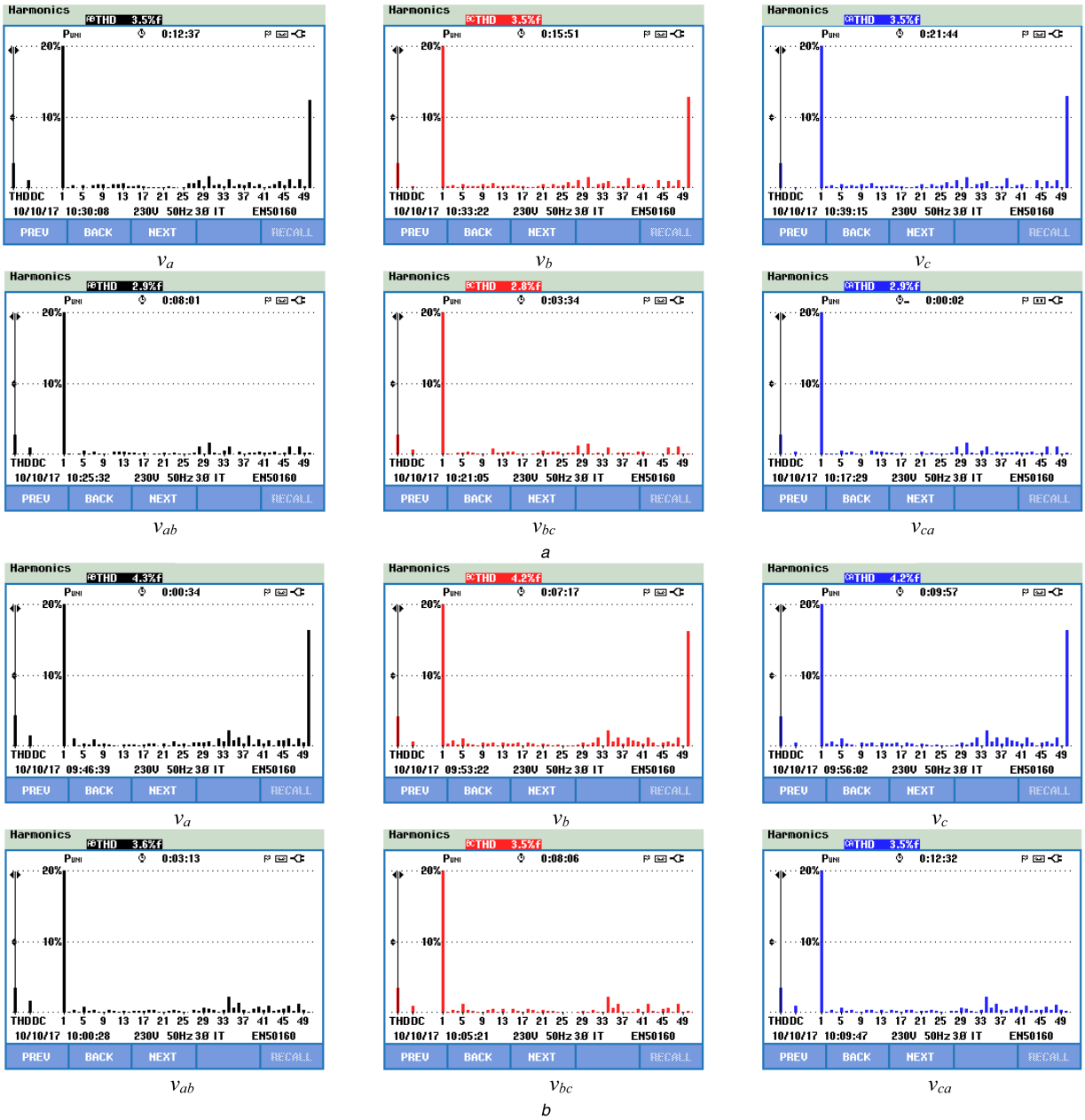

Fig. 10 *Experimental phase and line-voltage harmonic spectra for nine-level MLDCL in healthy condition*

(a) Harmonic spectra of phase and line voltages in healthy condition for $m_a = 0.9$, ***(b)*** Harmonic spectra of phase and line-voltages in healthy condition for $m_a = 0.7$

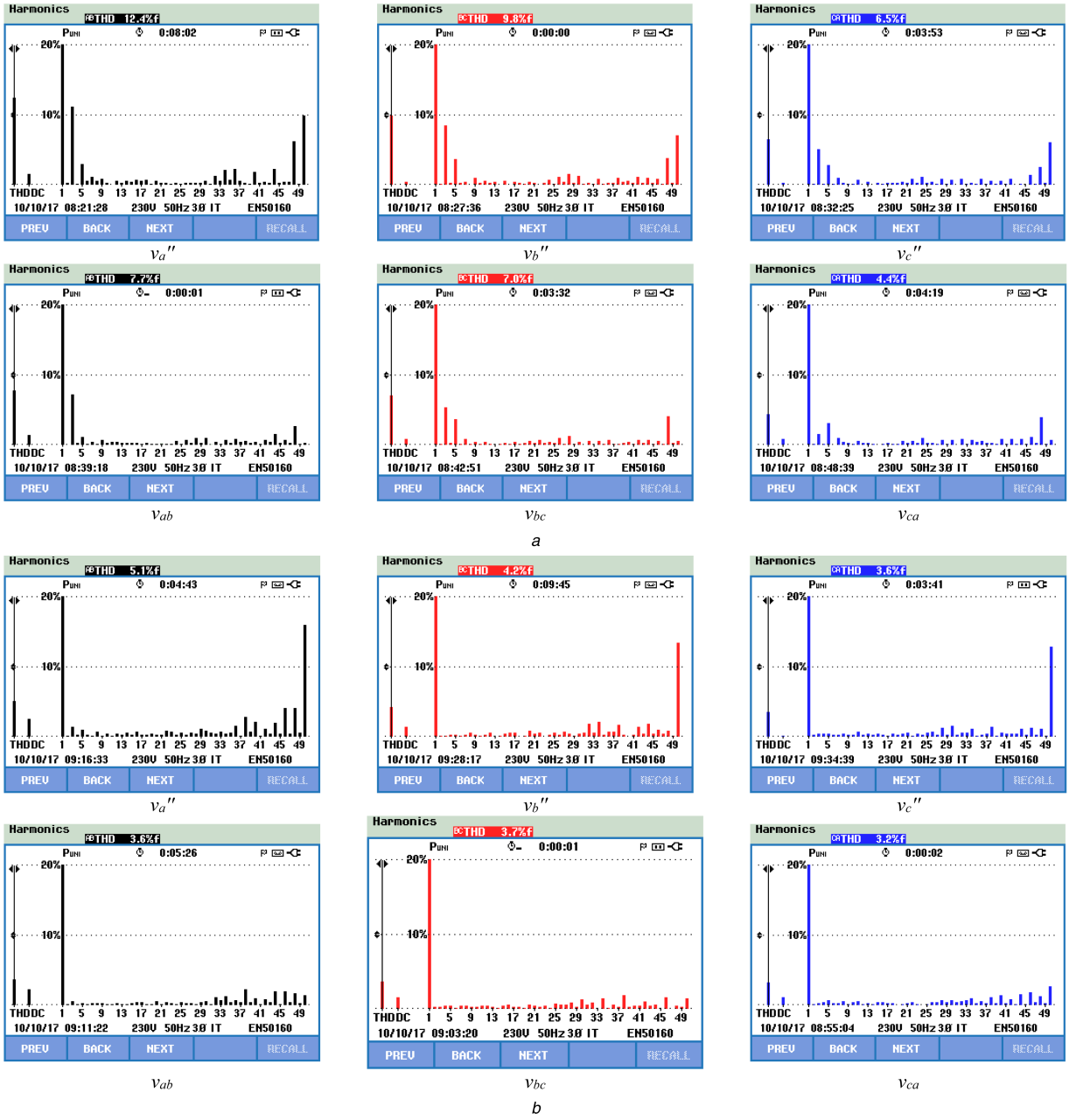

Fig. 11 *Experimental phase and line THD after compensation of 2-1-0 fault on nine-level MLDCL*
(a) Harmonic spectra of phase and line-voltage after 2-1-0 fault compensation with $m_a = 0.9$, ***(b)*** Harmonic spectra of phase and line voltage after 2-1-0 fault compensation with $m_a = 0.7$

Table 5 Comparison of nine-level simulation and experimental studies of the proposed FTS for various fault conditions

Experimental performance								Simulation performance					
Fault case		Phase-voltage RMS (%THD)			Line-voltage RMS (%THD)			Phase-voltage RMS (%THD)			Line-voltage RMS (%THD)		
x–y–z	m_a	V_a''	V_b''	V_c''	V_{ab}	V_{bc}	V_{ca}	V_a''	V_b''	V_c''	V_{ab}	V_{bc}	V_{ca}
0–0–0	0.9	76.3	76.8	76.1	131.2	131.9	132.0	77.8	77.2	77.3	132.8	132.7	132.8
		(3.5%)	(3.5%)	(3.5%)	(2.9%)	(2.8%)	(2.9%)	(17.0%)	(16.9%)	(16.9%)	(8.7%)	(8.8%)	(8.6%)
1–0–0	0.9	62.3	83.4	83.7	130.7	130.9	131.0	63.5	84.6	84.6	132.3	131.9	132.3
		(3.9%)	(2.9%)	(2.9%)	(2.5%)	(2.5%)	(2.5%)	(19.5%)	(14.8%)	(14.8%)	(9.2%)	(8.7%)	(9.2%)
2–1–0	0.9	41.4	71.6	93.0	116.6	118.6	119.1	42.2	72.9	94.8	117.7	120.1	120.8
		(12.4%)	(9.8%)	(6.5%)	(7.7%)	(7.0%)	(4.4%)	(22.2%)	(16.7%)	(13.0%)	(11.7%)	(13.5%)	(11.7%)
2–1–1	0.9	48.7	72.6	72.5	110.4	110.0	110.5	49.7	74.09	74.0	111.8	111.4	111.8
		(15.5%	(11.3%)	(11.3%)	(4.7%)	(7.2%)	(4.5%)	(22.2%)	(17.3%)	(17.3%)	(11.2%)	(14.4%)	(11.2%)
0–0–0	0.7	59.9	58.9	59.3	101.3	102.0	102.6	60.8	61.0	61.0	103.9	104.1	103.9
		(4.3%)	(4.2%)	(4.2%)	(3.6%)	(3.5%)	(3.6%)	(21.2%)	(21.4%)	(21.4%)	(12.0%)	(11.9%)	(12.0%)
2–1–0	0.7	41.7	63.2	79.3	102.2	101.6	101.9	42.5	64.4	80.9	102.8	103.2	103.0
		(5.1%)	(4.2%)	(3.6%)	(3.6%)	(3.7%)	(3.2%)	(30.5%)	(19.3%)	(16.5%)	(12.1%)	11.7%)	(11.9%)
2–1–1	0.7	44.2	66.1	66.2	101.0	100.6	101.9	45.1	67.4	67.4	101.6	101.2	101.6
		(7.5%)	(4.3%)	(4.3%)	(4.4%)	(4.2%)	(4.4%)	(25.6%)	(16.7%)	(16.7%)	(12.4%)	(12.6%)	(12.4%)

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