Sample-Averaged Zero-Sequence Current Elimination PWM Technique for Five-Phase Induction Motor With Opened Stator Windings

Ramsha Karampuri, Sachin Jain, *Member, IEEE*, and V. T. Somasekhar, *Member, IEEE*

***Abstract*— The five-phase dual-inverter connected to the five-phase open-end winding induction motor (FPOEWIM) with a single dc source could result in the flow of common-mode current (CMC) through the common dc bus and motor phase windings. In addition, the FPOEWIM drive contains third-harmonic content which do not contribute for torque generation in a distributed wound motor. So, to nullify the CMC as well as the third-harmonic content the sample-averaged zero-sequence current elimination (SAZE) pulsewidth modulation (PWM) technique is proposed in this paper. Wherein, the concept of alternative clamping of the inverters is used with the generation of virtual vector to eliminate third-harmonic content and the effective time region is moved to eliminate the CMC in average sense. The detailed analysis of the proposed SAZE PWM technique is presented along with the simulation results and experimental verification.**

***Index Terms*— Common-mode current (CMC), common-mode voltage (CMV), five-phase induction motor, open-end winding (OEW), pulsewidth modulation (PWM) technique.**

I. Introduction

DUE to the diminishing natural oil reserves, the research interest in the area of transportation is attracting toward the electric vehicles (EVs) [1], [2]. The EVs could be replacing the diesel/petrol driven vehicles in near future [3]. The basic equipments of the electric system in EVs are: power source, electric motor, power converter, and controller. The power source required to drive the electric motor could be either precharged battery or fuel cell. One of the popular electric motor used in the EV applications is the conventional three-phase induction motor and the power converter being three-phase H-bridge dc–ac inverter with a suitable controller [4]. The three-phase H-bridge inverter generates only two-levels in the inverter output voltage. This is replaced by a three-level neutral point clamped (NPC) inverter and presented in [5], which could improve the performance of the motor. However, some researchers have been attracted toward the multiphase induction motors for EVs because they offer the advantages like fault-tolerance, reduced torque ripple, reduced per phase current without increasing per phase voltage, reduced VA rating of the power semiconductor devices, etc. [6]–[10].

Furthermore, the most popular configuration of the induction motor which has gained the interest of many researchers in recent times is the open-end winding (OEW) topology. The OEW topology is formed by opening either the star or delta connected stator winding from both the ends [11]. Many investigations on the three-phase OEW induction motor (TPOEWIM) were reported in [12]–[15]. Wherein, the advantages of OEW topology are mentioned like: the OEW topology helps to generate a higher number of levels in the motor phase voltage, it will not provide any room for neutral point fluctuations as in the case of NPC inverter, it increases the fault-tolerance capability, etc. [12]–[15]. This paper proposes the use of five-phase OEW induction motor (FPOEWIM) for EV applications, which coalesces the merits of multiphase machines and OEW topology [16].

The induction motor with OEW topology can be powered from both the ends of the stator winding through two dc–ac inverters. The inverters can be connected either to two electrically isolated dc power sources or a single dc source. In the battery driven EVs, the isolation between the power sources is naturally available. However, the use of two units of power sources for the given power requirement could result in increased size, weight, and hence cost when compared to the single unit. On the other hand, the use of single dc source with the common dc bus results in the flow of common-mode current (CMC) through the motor phase windings. This may lead to the heating of the motor phase windings [17], which would be undesirable in the EV application. However, the flow of CMC could be avoided by the use of suitable pulsewidth modulation (PWM) techniques to operate the inverters. In case of TPOEWIM, some of the accepted investigations to eliminate/suppress the CMC include sample-averaged zero-sequence current elimination (SAZE) PWM technique [17]–[21].

Somasekhar *et al.* [18] used two two-level H-bridge inverters connected to the single dc source. Each inverter consists

Manuscript received March 9, 2017; revised June 19, 2017 and August 18, 2017; accepted September 13, 2017. Date of publication October 5, 2017; date of current version May 1, 2018. Recommended for publication by Associate Editor Luca Zarri. *(Corresponding author: Sachin Jain.)*

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Digital Object Identifier 10.1109/JESTPE.2017.2759965

of eight switching states and result in 64 switching combinations when combined together. According to the SAZE PWM technique proposed in [18] one of the inverter is clamped to corresponding switching state in a sector, while the other inverter is being switched. This result in different switching combinations and their corresponding common-mode voltage (CMV) contribution can be calculated. The CMVs are averaged to zero within a sampling time interval and thus the offset time is obtained. The offset time is used to move the effective time region (region where only the active vectors are switched) to nullify the CMC in average sense. Recently, this technique was adopted for a solar PV powered water pumping system with the TPOEWIM [19].

Most recently, Reddy and Somasekhar [17] and Reddy [20] used similar kind of SAZE PWM technique to suppress the CMC in a four-level TPOEWIM drive with nested rectifier–inverter. In this paper [17], [20], the CMV is averaged to zero in even and odd regions separately to calculate the offset time period. Then, the obtained offset time periods are averaged to make the CMC zero in the interspatial parts between the regions. Similar approach has been extended to a TPOEWIM drive which uses two three-level NPC inverters connected to the common dc bus [21]. Wu *et al*. [21] have used two different offset time periods, one for the even sectors and the other for the odd sectors.

The above discussion gives the motivation to extend the SAZE PWM technique to a FPOEWIM drive with two two-level five-phase inverters connected to the either ends of the OEWs with the common dc bus. The five-phase dual-inverter (FPDI) connected FPOEWIM system contains a large number of switching state combinations when compared to the TPOEWIM drive. In addition, the space vectors (SVs) have three different magnitudes and are represented in two separate subspaces. The challenging task here is to extract the possibilities of using particular switching state combinations at selected SV locations so that the CMC as well as the third order components could be eliminated. Hence, this paper proposes the SAZE PWM technique which achieves both the tasks for the FPOEWIM drive system.

The ensuing sections contain a brief description of the FPDI along with the details of the CMV contributions. Later, the detailed mathematical analysis of the proposed PWM technique is presented. After that, the simulation results along with the experimental verification are furnished. The conclusion from the proposed work is presented at the end of this paper.

II. Five-Phase Dual-Inverter and Associated Common Mode Voltage

The FPOEWIM is powered from both the ends of the stator winding *via* FPDI. The FPDI is connected to a single dc source using a common dc bus as shown in Fig. 1. The dynamic model of a symmetrical distributed wound FPOEWIM is used in this paper which is presented in [22]. The FPDI is modeled considering the ideal power semiconductor switches. The inverters I and II shown in Fig. 1 consists of 20 switches in ten legs *viz. a, b, c, d, e, a′, b′, c′, d′* and *e′*, which form the phases *aa′*, *bb′*, *cc′*, *dd′*, and *ee′* for the FPOEWIM. The switching

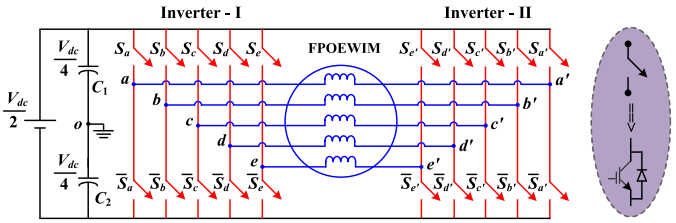

Fig. 1. Three-level dual-inverter connected five-phase open-end winding induction motor drive with single dc source.

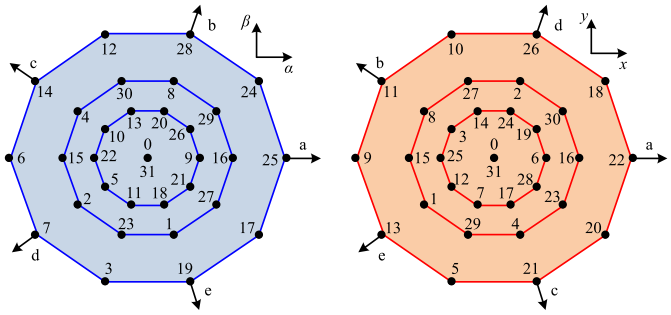

Fig. 2. SV locations and switching states corresponding to inverter-I in $\alpha-\beta$ (left) and *x-y* (right) subspaces.

states of inverter-I and inverter-II can be characterized by the vector $[S_a S_b S_c S_d S_e]^T$ and $[S_{a'} S_{b'} S_{c'} S_{d'} S_{e'}]^T$, respectively. This results in 32 switching states (from 0 to 31) in 31 SV locations for an individual inverter. The switching state "0" corresponds to the vector [0 0 0 0 0], "1" corresponds to [0 0 0 0 1] and so on up to the switching state "31" which represents the vector [1 1 1 1 1]. These switching states correspond to inverter-I, similarly switching states for inverter-II are represented using "′" "' mark as superscript *viz.* 0′ to 31′.

The switching states for one of the FPDI, say, inverter-I are mapped into two orthogonal subspaces ($\alpha-\beta$ and *x-y* subspaces) using (1) as shown in Fig. 2 (this is similar for inverter-II). The $\alpha-\beta$ subspace includes the fundamental components, whereas the *x-y* subspace represents the third-harmonic components [23]. The difference in phase sequence for $\alpha-\beta$ and *x-y* subspaces for a distributed wound five-phase motor is shown in Fig. 2

$$\vec{v}_{\alpha-\beta} = \frac{2}{5}(v_a + kv_b + k^2 v_c + k^3 v_d + k^4 v_e)$$
$$\vec{v}_{x-y} = \frac{2}{5}(v_a + kv_d + k^2 v_b + k^3 v_e + k^4 v_c) \quad (1)$$

where $k = \exp(j2\pi/5)$; v_a, v_b, v_c, v_d, and v_e are the reference voltage vectors for inverter-I.

The $\alpha-\beta$ and *x-y* subspaces consist of three groups of vectors *viz.* large, medium, and small with the magnitudes $0.6472 \times (V_{dc}/2)$, $0.4 \times (V_{dc}/2)$, and $0.247 \times (V_{dc}/2)$, respectively, defined by (1). The large vectors mapped in the $\alpha-\beta$ subspace are corresponding to the small vectors in the *x-y* subspace and vice-versa. Whereas, the medium vectors in both the planes remain the same. The large, medium, and small vectors of inverter-I and inverter-II are combined for the dual inverter, which results in 211 SV locations

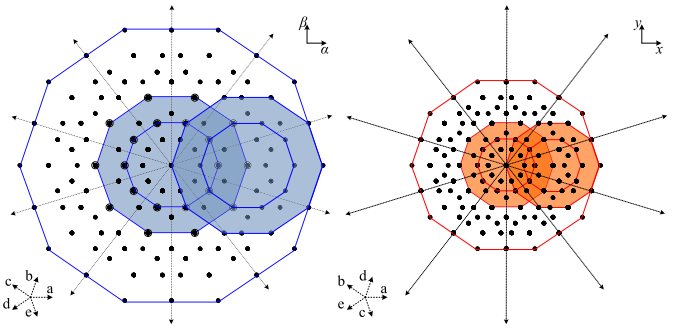

Fig. 3. SV locations corresponding to FPDI in $\alpha-\beta$ (left) and x-y (right) subspaces using only large and medium vectors.

and 1024 (i.e., 32×32) switching state combinations. A large number of switching state combinations and the locations portray the complexity associated with the implementation of a PWM technique to realize the reference voltage vector. The SV locations and the switching state combinations can be reduced by neglecting the small vectors in $\alpha-\beta$ subspace (i.e., large vectors in x-y subspace). This helps in avoiding the injection of lower order harmonics (less than 5) into the system.

The SV diagram for the FPDI in $\alpha-\beta$ and x-y subspaces using the large and medium vectors of $\alpha-\beta$ subspace is shown in Fig. 3. It is formed by overlapping the SV diagram of inverter-I and inverter-II for all the large and medium vectors (i.e., medium and small vectors in x-y subspace). This results in 131 SV locations and 484 (22×22) switching state combinations in both the subspaces in ten sectors with a span of $\pi/5$ radians between each sector.

The CMV associated with the FPDI ($V_{\rm cm}$) can be derived from the CMVs of both the inverter-I ($V_{\rm cm1}$) and inverter-II ($V_{\rm cm2}$) as given in (2)–(5). The CMV contributions for all the possible switching state combinations at the SV locations shown in Fig. 3 could be $\pm V_{\rm dc}/2$, $\pm 2V_{\rm dc}/5$, $\pm 3V_{\rm dc}/10$, $\pm V_{\rm dc}/5$, $\pm V_{\rm dc}/10$, and 0(for the dc bus voltage of "$V_{\rm dc}/2$")

$$V_{\rm cm1} = \frac{1}{5}\left(v_{ao} + v_{bo} + v_{co} + v_{do} + v_{eo}\right) \tag{2}$$

$$V_{\rm cm2} = \frac{1}{5}\left(v_{a'o} + v_{b'o} + v_{c'o} + v_{d'o} + v_{e'o}\right) \tag{3}$$

$$V_{\rm cm} = V_{\rm cm1} - V_{\rm cm2} \tag{4}$$

$$V_{cm} = \frac{1}{5}\left(v_{aa'} + v_{bb'} + v_{cc'} + v_{dd'} + v_{ee'}\right) \tag{5}$$

where v_{ao}, v_{bo}, v_{co}, v_{do}, and v_{eo} are the pole voltages of inverter-I; $v_{a'o}$, $v_{b'o}$, $v_{c'o}$, $v_{d'o}$, and $v_{e'o}$ are the pole voltages of inverter-II; and $v_{aa'}$, $v_{bb'}$, $v_{cc'}$, $v_{dd'}$, and $v_{ee'}$ are the phase voltages of FPOEWIM.

III. The SAZE PWM Technique to Eliminate CMC and Third-Harmonic Content

Since a single dc source is used to drive the FPOEWIM, the common dc bus connected to FPDI is responsible for the flow of CMC through the motor phase winding. This section gives the detailed analysis of the SAZE PWM technique for eliminating the CMC in an average sense as presented

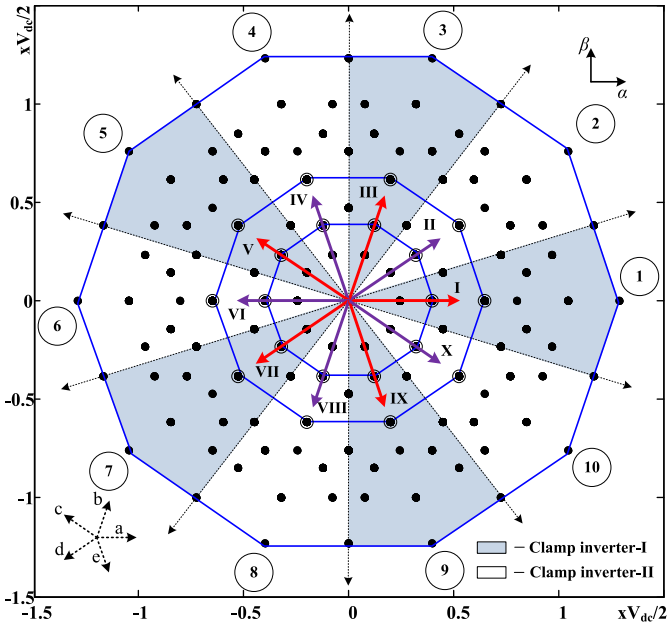

Fig. 4. SV locations for FPDI in $\alpha-\beta$ subspace using only large and medium vectors and the generated virtual vectors in all the ten sectors.

in [17]–[21] for the TPOEWIM. The proposed SAZE PWM technique for the FPOEWIM is intricate compared to that of the three-phase drive. The complexity is mainly because of three reasons: 1) a large number of switching states; 2) the vectors are mapped in two different subspaces (fundamental and third-harmonic components); and 3) presence of the large and medium vectors (even if small vectors are ignored).

The very first SAZE PWM technique for the TPOEWIM drive presented in [17] uses the equilateral triangles present in the SV diagram. The CMV is averaged to zero by moving the region of effective time period $T_{\rm eff}$ within a sampling time interval T_s. This is achieved by using the switching state combinations located at the vertices of an equilateral triangle. However, in case of the FPOEWIM drive the SV diagram has neither equilateral triangles nor equilateral pentagons as shown in Fig. 4. So, it is quite difficult to decide as to which group of switching state combinations should be used to eliminate the CMV.

In addition to the above, the SAZE PWM technique for TPOEWIM drive [17] uses the concept of alternate switching and clamping of the inverters to reduce the switching losses. The clamping of the inverter is done using the switching state combination which is present at the nearest subhexagonal center. In case of the FPOEWIM drive, the clamping of one of the inverter could be achieved by using either only medium or large vectors. This may reduce the switching losses, but this would lead to the presence of third-harmonic components in the motor phase voltage. This is because, if only large vector of $\alpha-\beta$ subspace is clamped for one of the inverter, it results in small vector in x-y subspace. While, clamping the medium vector in $\alpha-\beta$ subspace will result in medium vector in x-y subspace. Hence in this paper, the clamping is achieved using both the large and medium vectors by generating a virtual vector as proposed in [24] and [25].

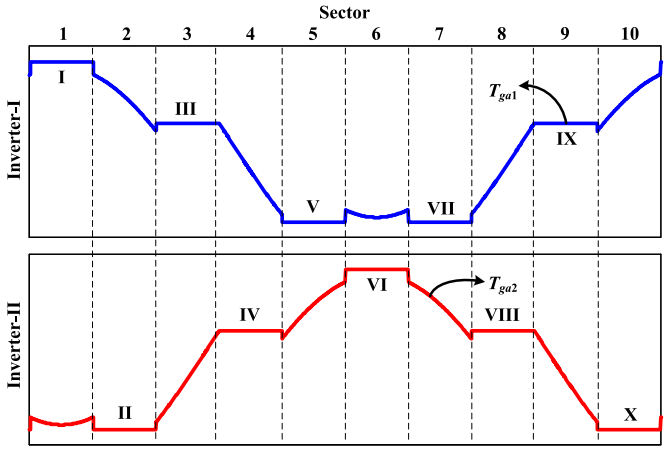

Fig. 5. Modulating (gate timing) waveforms used to implement the proposed PWM technique and depicting the clamping and switching behavior for inverter-I and inverter-II alternatively.

The generation of virtual vector with a proper dwell time ratio (0.618) helps in eliminating the third-harmonic components which are mapped into *x-y* subspace [24]. Fig. 4 demonstrates the generation of the virtual vectors (I to X) that to be clamped for inverter-I and -II alternatively. The set of virtual vectors {I, III, V, VII, and IX} and {II, IV, VI, VIII, and X} are realized by inverter-I and inverter-II in alternative sectors, respectively. When the inverter-I is clamped to a particular virtual vector, the other inverter is switched. For example, if the reference SV is in sector-1, inverter-I is clamped to the virtual vector I while inverter-II being switched. The clamping and switching behavior of both the inverters is demonstrated in Fig. 5.

Now, consider the reference voltage vector to be realized is currently in sector-1 of Fig. 4. Each sector can be divided into two halves as shown in Fig. 6(a). If the reference voltage vector lies in the upper half of the sector, it can be realized as

$$\mathrm{OU}_1 = \mathrm{OU} + \mathrm{UU}_1. \tag{6}$$

And, if the reference voltage vector lies in the lower half of the sector then

$$\mathrm{OU}_2 = \mathrm{OU} + \mathrm{UU}_2 \tag{7}$$

where OU is the common voltage vector (virtual vector) which is realized using the medium and large voltage vectors of the clamping inverter (say, inverter-I for sector-1). Consider the upper half of sector-1 to analyze how the CMC is eliminated by making the CMV zero in the average sense. The analysis is presented in two different parts; wherein the CMV is averaged to zero by moving the region of T_{eff} within T_s using the large and medium voltage vectors separately. Later, both are combined and averaged to get the net CMV equals to zero.

A. Clamping the Large Voltage Vector

In sector-1, for inverter-I, the large voltage vector can be realized using the switching state "25" which is fixed (clamped). As shown in Fig. 6(b), inverter-II has different combinations of switching states which are chosen particularly to make the average CMV equal to zero. The selected

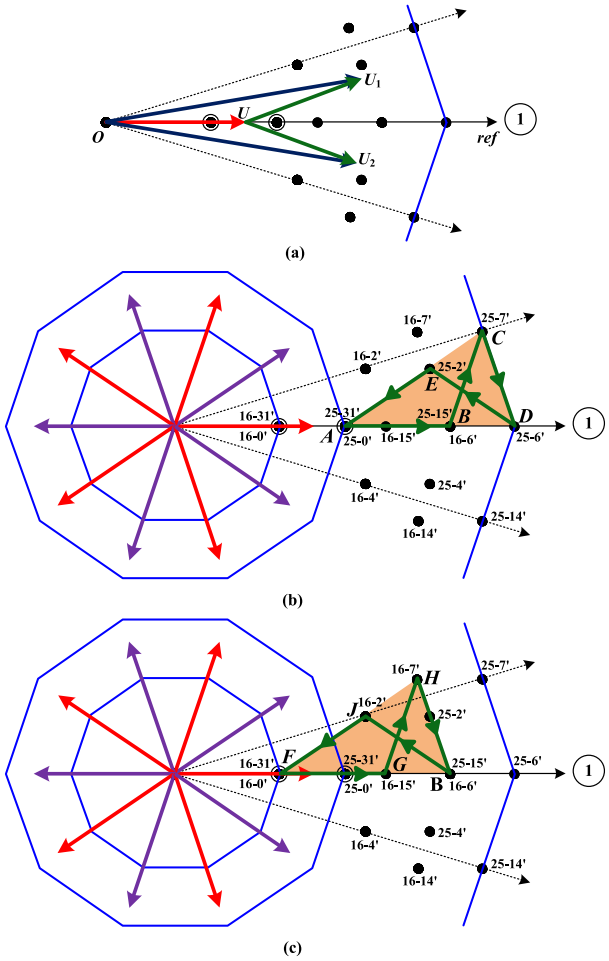

Fig. 6. Zoomed part of sector-1 in Fig. 4 showing (a) realization of the reference voltage vector, (b) switching trajectory when large voltage vector of inverter-I is clamped, and (c) switching trajectory when medium voltage vector of inverter-I is clamped.

TABLE I

SWITCHING STATE COMBINATIONS USED WHEN THE LARGE VOLTAGE VECTOR IS CLAMPED IN SECTOR-1

Switching state combination (location)	CMV contribution	Time for realization
25-31' (*A*)	$V_{dc}/5$	$(1\text{-}x)T_0$
25-15' (*B*)	$V_{dc}/10$	T_4
25-7' (*C*)	0	T_3
25-6' (*D*)	$-V_{dc}/10$	T_2
25-2' (*E*)	$-V_{dc}/5$	T_1
25-0' (*A*)	$-3V_{dc}/10$	xT_0

switching states along with their realization times are furnished in Table I. The corresponding switching trajectory is indicated in Fig. 6(b).

Now, for making CMV zero

$$\frac{\text{CMV contribution} \times \text{Realization time}}{T_s} = 0. \tag{8}$$

So, substituting the CMV contributions and the realization times for particular switching state combinations from Table I in (8) results in

$$\frac{V_{\rm dc}}{T_s}\left[\frac{(1-x)\,T_0}{5}+\frac{T_4}{10}+0\times T_3-\frac{T_2}{10}-\frac{T_1}{5}-\frac{3xT_0}{10}\right]=0. \tag{9}$$

Rewriting (9)

$$xT_0=\frac{2}{5}T_0+\frac{1}{5}\left(T_4-T_2-2T_1\right). \tag{10}$$

The switching times T_1 to T_4 can be replaced by the minimum and maximum switching times, $T_{\rm min}$ and $T_{\rm max}$ respectively. From Fig. 7(a)

$$T_{\rm max}+T_{\rm mid1}+T_{\rm mid2}+T_{\rm mid3}+T_{\rm min}=\ 0;$$
$$T_{\rm s}=T_0+T_{\rm eff};\ T_{\rm eff}=T_{\rm max}-T_{\rm min}. \tag{11}$$

Also

$$T_1=T_{\rm max}-T_{\rm mid3};\quad T_2=T_{\rm mid3}-T_{\rm mid2}$$
$$T_3=T_{\rm mid2}-T_{\rm mid1};\quad T_4=T_{\rm mid1}-T_{\rm min}. \tag{12}$$

Substituting (12) in (10) gives

$$xT_0=\frac{2}{5}T_0-\frac{1}{5}(2T_{\rm min}+3T_{\rm max}). \tag{13}$$

So, to move the region of effective time by $(1-x)T_0$, the offset time, $T_{\rm offset}$ should be varied as given in the following [17]:

$$T_{\rm offset}=(1-x)T_0-T_{\rm min}. \tag{14}$$

Substituting (13) in (14) results in

$$T_{\rm offset}=T_0-\frac{2}{5}T_0+\frac{1}{5}(2T_{\rm min}+3T_{\rm max})-T_{\rm min}. \tag{15}$$

Solving (15) using (11) results in

$$T_{\rm offset\_L}=\frac{3}{5}T_s. \tag{16}$$

Hence, the offset time required by the gate timing signal while clamping the large voltage vector is "$3T_s/5$."

B. Clamping the Medium Voltage Vector

If the medium voltage vector is to be clamped in sector-1, it can be realized using the switching state "16" for inverter-I. The inverter-II is switched using the switching state combinations as provided in Table II. Fig. 6(c) shows the switching trajectory pertaining to this case.

Substituting the CMV contributions and the realization times for particular switching state combinations from Table II in (8) and rewriting the equation results in

$$xT_0=\frac{4}{5}T_0+\frac{1}{5}(3T_4+2T_3+T_2). \tag{17}$$

From (12) and (17)

$$xT_0=\frac{4}{5}T_0-\frac{1}{5}(4T_{\rm min}+T_{\rm max}). \tag{18}$$

TABLE II

SWITCHING STATE COMBINATIONS USED WHEN THE MEDIUM VOLTAGE VECTOR IS CLAMPED IN SECTOR-1

Switching state combination (location)	CMV contribution	Time for realization
16-31' (F)	$2V_{dc}/5$	$(1\text{-}x)T_0$
16-15' (G)	$3V_{dc}/10$	T_4
16-7' (H)	$V_{dc}/5$	T_3
16-6' (B)	$V_{dc}/10$	T_2
16-2' (J)	0	T_1
16-0' (F)	$-V_{dc}/10$	xT_0

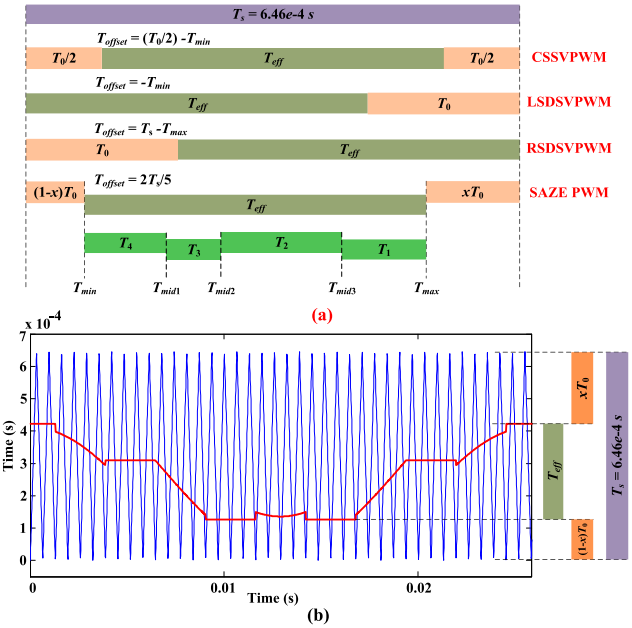

Fig. 7. (a) Time diagram of the modulating (gate timing) waveform showing different times for realizing reference voltage vector. (b) Modulating (gate timing) and the carrier waveforms showing the movement of effective time region.

Similarly, calculating the offset time for clamping medium voltage vector results in

$$T_{\rm offset\_M}\ =\ T_0-\frac{4}{5}T_0+\frac{1}{5}\left(4T_{\rm min}+T_{\rm max}\right)-T_{\rm min}$$
$$\Rightarrow T_{\rm offset\_M}=\frac{T_s}{5}\ (\text{ from }\ (11)). \tag{19}$$

So, the offset time required by the gate timing signal while clamping the medium voltage vector is "$T_s/5$."

Now, the offset time period for clamping both the large and medium voltage vectors together can be obtained by averaging both the offset times. This gives the local switching in all the sectors by covering entire area inside the sector and could eliminate the CMC in average sense. So, the resultant offset time period is given by

$$T_{\rm offset}=\frac{T_{\rm offset\_L}+T_{\rm offset}{}_M}{2}=\frac{2}{5}T_s. \tag{20}$$

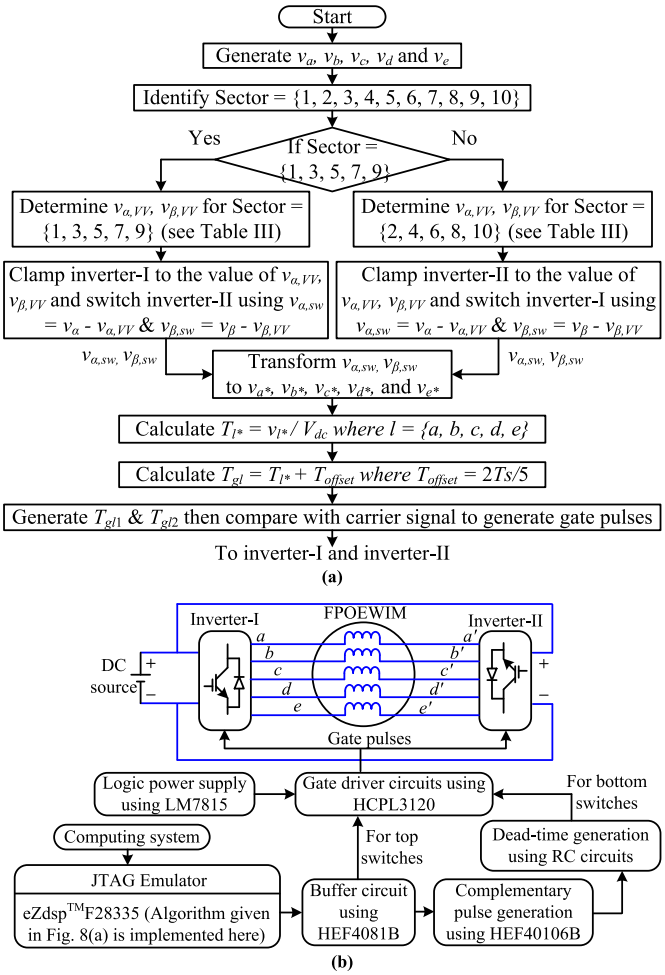

Fig. 8. (a) Flowchart for the proposed PWM technique and (b) block diagram of the FPOEWIM drive system.

Therefore, an offset time period of $2T_s/5$ is used to move the region of effective time period. This can be observed from Fig. 7(b), where the modulating (gate timing) and the carrier waveforms are shown together and the modulating (gate timing) waveform is not center-spaced (CS) with respect to the carrier waveform. This proves the use of the concept of effective time period placement to eliminate the CMC. Furthermore, the effective time period can be conventionally placed in three different ways *viz.* the CS, left shifted (LS), and right shifted (RS) as shown in Fig. 7(a) [26]. The SV-PWM techniques using these three ways *viz.* CSSVPWM, LS discontinuous SVPWM (LSDSVPWM) and RS discontinuous SVPWM (RSDSVPWM) are implemented by varying the offset time periods as given in the following:

$$\begin{aligned} T_{\text{offset}} &= \frac{T_0}{2} - T_{\min};\ \text{for CSSVPWM} \\ &= -T_{\min};\ \text{for LSDSVPWM} \\ &= T_s - T_{\max};\ \text{for RSDSVPWM.} \end{aligned} \tag{21}$$

In addition, the implementation of the proposed PWM technique is described using the flowchart and the block diagram as shown in Fig. 8(a) and (b), respectively. The five-phase reference voltage signals are initiated using the information of modulation index m_a. The boundary of linear modulation can

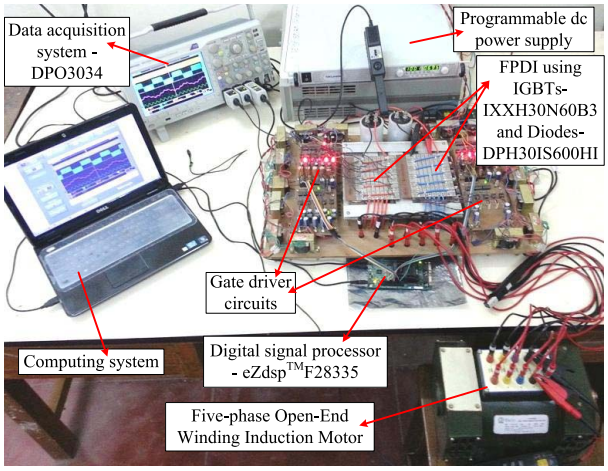

Fig. 9. Photograph of the experimental setup.

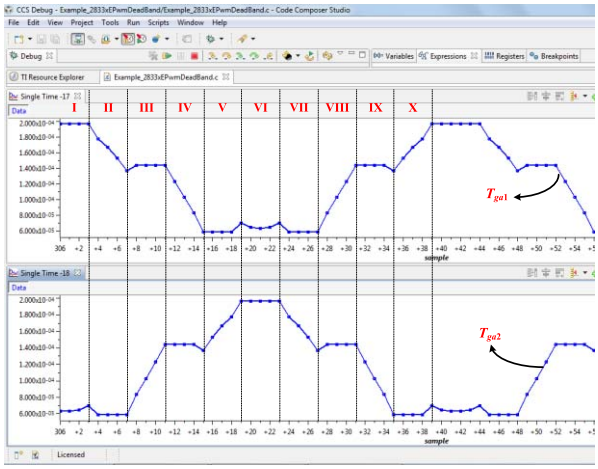

Fig. 10. Modulating (gate timing) waveforms generated inside the eZdsp™F28335 digital signal controller, which are used to implement the proposed PWM technique for inverter-I (top) and inverter-II (bottom).

be defined as follows:

$$m_{a,\max} = \frac{V_{\max}}{V_{\text{dc}}} \tag{22}$$

where $V_{\max}$ is the maximum fundamental phase voltage. Using the proposed PWM technique, the value of $V_{\max}$ is equal to $0.618 \times \cos(\pi/5)$. Here, the value 0.618 is the ratio of medium and large voltage vectors and angle is $\pi/5$ because of the shifting of decagon vertically [18]. The dc bus voltage used is $V_{\text{dc}}/2$. Hence, the maximum modulation index, $m_{a,\max}$ is limited to 1.

The generated reference voltage signals are used to determine the sectors numbered from one through ten. The odd sectors are chosen to clamp the inverter-I to its virtual vector and inverter-II is switched, whereas, the even sectors are chosen vice versa. The clamping of the respective inverter is achieved using the coordinates given in Table III, where either medium or large vector coordinates can be used. The clamping of an inverter does not mean for holding a single switching state throughout the switching time, but it meant for holding the virtual vector, i.e., the medium voltage vector

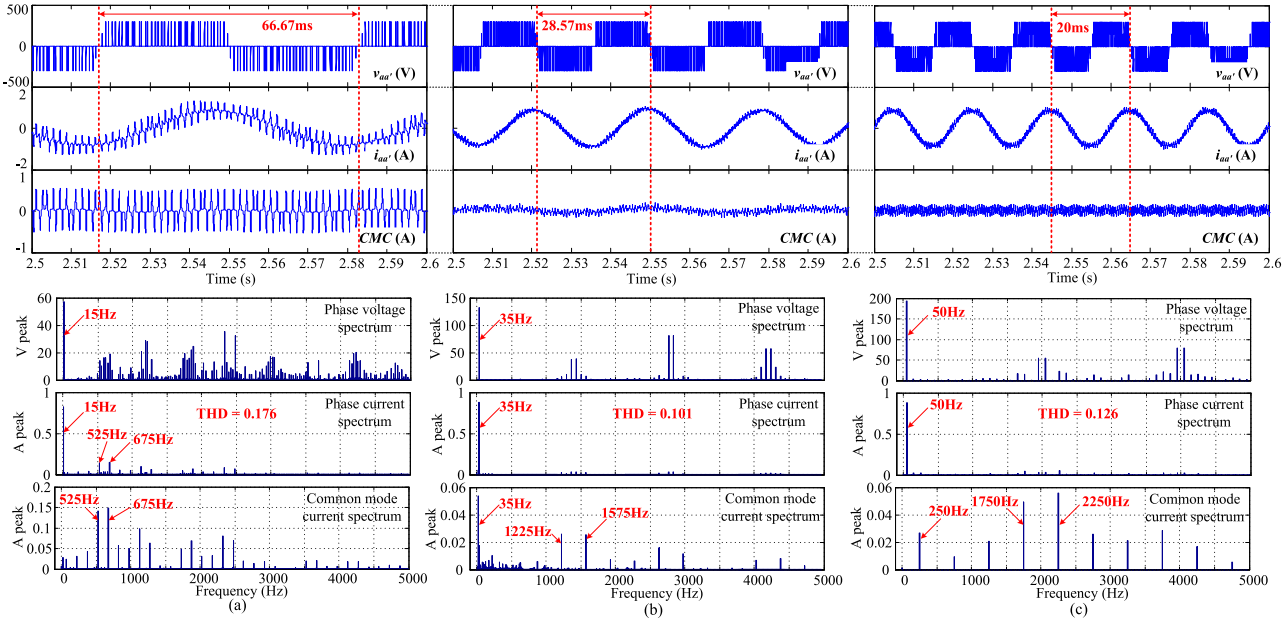

Fig. 11. Simulation results (from top to bottom) phase-aa' voltage, phase-aa' current, CMC, harmonic spectrum of phase voltage, phase current, and CMC, respectively, for (a) $m_a = 0.3$, (b) $m_a = 0.7$, and (c) $m_a = 1$.

TABLE III
LIST OF VIRTUAL VECTORS

Sector	*Medium vectors*			*Large vectors*		
	$v_{\alpha,VV}$	$v_{\beta,VV}$		$v_{\alpha,VV}$	$v_{\beta,VV}$	
1	0.4	0		0.647	0	Clamping Inverter-I
3	0.1236	0.3804		0.2	0.6152	
5	-0.3236	0.2348		-0.5236	0.3804	
7	-0.3236	-0.2348	**OR**	-0.5236	-0.3804	
9	0.1236	-0.3804		0.2	-0.6152	
2	0.3236	0.2348		0.5236	0.3804	Clamping Inverter-II
4	-0.1236	0.3804		-0.2	0.6152	
6	-0.4	0		-0.647	0	
8	-0.1236	-0.3804		-0.2	-0.6152	
10	0.3236	-0.2348		0.5236	-0.3804	

is realized for the duration of 0.382 times switching time (excluding zero time), whereas, the large vector is held for 0.618 times switching time (excluding zero time). This is achieved inherently using the proposed carrier based-SAZE PWM technique and helps in eliminating third harmonics content.

IV. SIMULATION STUDY AND EXPERIMENTAL VERIFICATION

The proposed SAZE PWM technique along with the open-loop V/f control for the FPOEWIM drive shown in Fig. 1 is simulated using MATLAB/Simulink and experimentally verified using a low scale laboratory prototype. The 100 rad/s, six pole FPOEWIM parameters used in the simulation are: stator and rotor resistances -22.63 and 13.1 Ω, respectively; stator and rotor leakage inductances -102 and 35.2 mH,

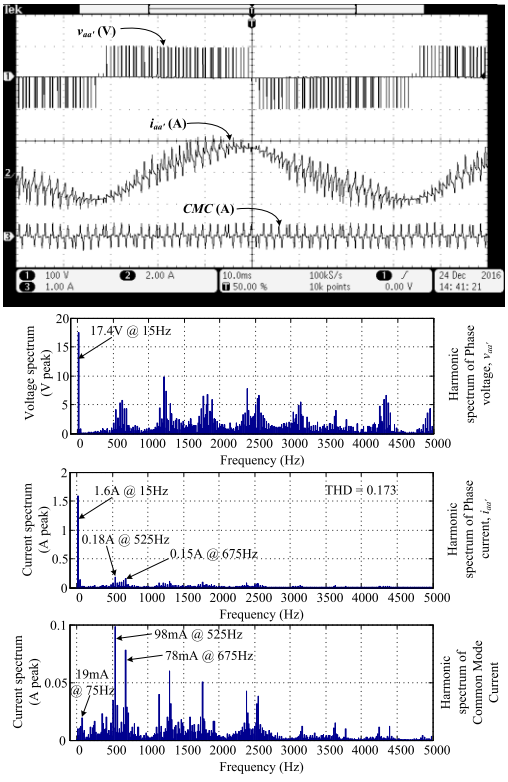

Fig. 12. Experimental results (x-axis: 10 ms/div) phase-aa' voltage (top) (y-axis: 100 V/div), phase-aa' current (middle) (y-axis: 2 A/div), CMC (bottom) (y-axis: 1 A/div) and their corresponding harmonic spectra for $m_a = 0.3$.

respectively, mutual inductance -588 mH in fundamental plane. Whereas, in third-harmonic plane the rotor resistance, stator and rotor leakage inductances are considered to be the same as in the fundamental plane, while, the mutual inductance is assumed to be zero for simulation studies (since distributed wound machine is considered) [25]. The

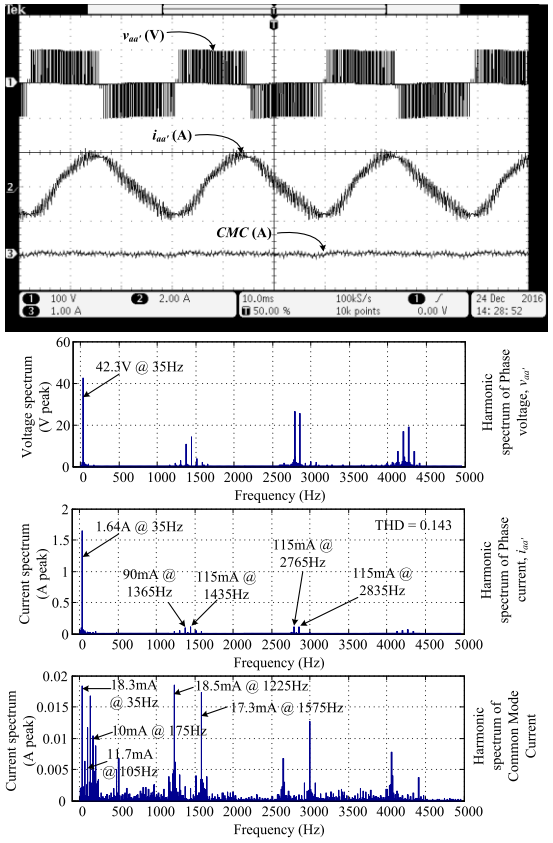

Fig. 13. Experimental results (x-axis: 10 ms/div) phase-aa' voltage (top) (y-axis: 100 V/div), phase-aa' current (middle) (y-axis: 2 A/div), CMC (bottom) (y-axis: 1 A/div), and their corresponding harmonic spectra for $m_a = 0.7$.

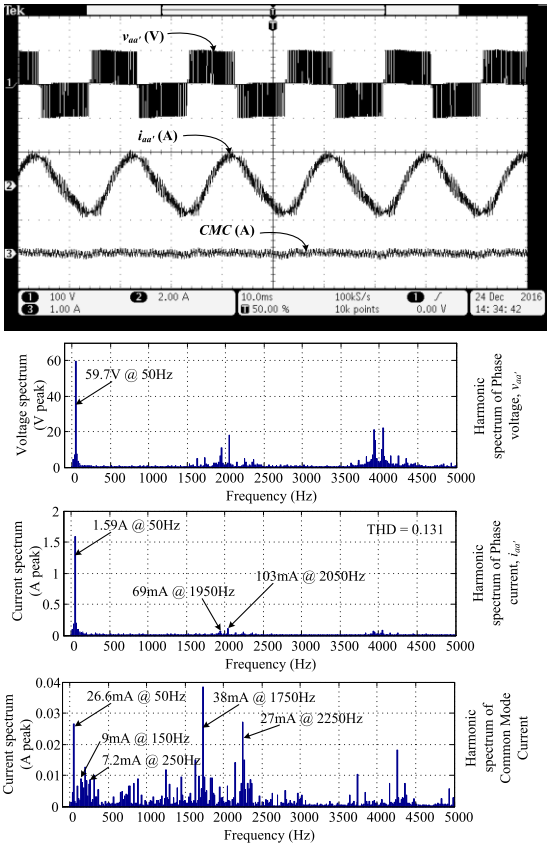

Fig. 14. Experimental results (x-axis: 10 ms/div) phase-aa' voltage (top) (y-axis: 100 V/div), phase-aa' current (middle) (y-axis: 2 A/div), CMC (bottom) (y-axis: 1 A/div) and their corresponding harmonic spectra for $m_a = 1$.

simulation is performed by considering the dc bus voltage of 300 V, 40 samples per fundamental cycle and the dead-band between top and bottom switch of the inverter leg is considered to be 6 μs. The experimental prototype includes a 1 HP, 200 V, 3.4 A, 50 Hz, and 1400 rpm FPOEWIM with the parameters: stator and rotor resistances -1.05 and 1.42 Ω, respectively; stator and rotor leakage inductances -6 mH each; and mutual inductance -84.73 mH in fundamental plane. Whereas, the motor parameters in x-y (third-harmonic) plane are: stator and rotor resistances -1.05 and 2.85 Ω, respectively; stator and rotor leakage inductances -5.34 mH each; and mutual inductance -7.59 mH. All the rotor quantities provided above are referred to stator winding. The FPOEWIM is powered from a single programmable dc power supply *via* a custom made FPDI with a common dc bus connection as shown in Fig. 9. The FPDI is made by using IXYS make discrete insulated-gate bipolar transistors (IGBTs) (IXXH30N60B3) and IXYS make high performance dynamic fast recovery discrete power diodes (DPH30IS600HI) which are connected in antiparallel to the discrete IGBTs.

The gate pulses to the discrete IGBTs are generated using an eZdspF28335 digital signal controller. The digital signal controller is programmed using code composer studio (CCS) where the proposed SAZE PWM technique shown in Fig. 8 is implemented. The modulating (gate timing) waveforms generated inside the controller are captured using the CCS graph window and shown in Fig. 10, which are similar to the waveforms shown in Fig. 5. The complementary nature of clamping and switching behavior of both the inverters can be observed from Fig. 10. The modulating (gate timing) waveforms are compared with the internally generated carrier waveforms and ten independent gate drive signals are obtained from the controller for all the top ten devices of the dual inverter [27]. The complementary pulses for the bottom ten devices are generated using HEF40106B IC (NOT gate IC) and the dead-band circuit with 1-μs delay is introduced to ensure the safe operation [see Fig. 8(b)]. All these 20 gating pulses are given to the discrete IGBTs through the custom made independent twenty gate driver circuits. Each gate driver circuit is constructed using the logic gate (HEF4081B—AND gate IC), gate driver IC (HCPL3120) and the required passive elements like resistors and capacitors. The gate driver IC is used to drive the corresponding IGBT device, in addition it serves for opto-isolation between the control circuit and the power circuit. The logic power supply (isolated) required for all gate driver ICs is obtained using an independent voltage regulator circuit (that uses LM7815-IC). The dc bus voltage of 100 V is applied, and the waveforms are acquired using a Tektronix made 300 MHz DPO3034. The phase voltage is acquired using the differential probe, the phase current and the CMC are measured using current probe. The CMC is measured by passing both the positive and negative dc bus cables through the single current probe.

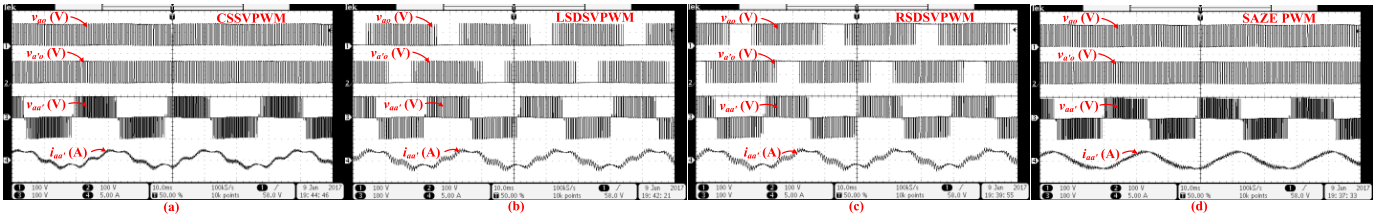

Fig. 15. Experimental results inverter-I pole voltage (y-axis: 100V/div), inverter-II pole voltage (y-axis: 100 V/div), motor phase voltage (y-axis: 100 V/div) and motor phase current (y-axis: 5 A/div) (from top to bottom, all x-axis: 10 ms/div) obtained using (a) CSSVPWM, (b) LSDSVPWM, (c) RSDSVPWM, and (d) SAZE PWM technqiues for $m_a = 0.7$.

Fig. 11 shows the simulation results of the FPOEWIM phase voltage, phase current, and the CMC along with their corresponding harmonic spectra. These waveforms are captured for three different modulation indices *viz.* 0.3, 0.7, and 1. At lower modulation index, the ripple content in the phase current is higher compared to those with the higher value of m_a [see the total harmonic distortion (THD) values in phase current spectrum]. However, the current ripple can be minimized by increasing the number of samples per fundamental cycle. Furthermore, the working of the proposed PWM technique can be verified from the CMC plots where the CMC is forced to zero in average sense for every sampling time interval. In addition, the absence of lower order harmonic components (particularly third and fourth harmonics) in both the spectra of phase voltage and phase current ensures the elimination of CMV and hence the CMC.

Figs. 12–14 show the experimental results of the FPOEWIM phase voltage, phase current, and the CMC along with their corresponding harmonic spectra for modulation indices 0.3, 0.7, and 1, respectively, under no-load condition. The nature of phase voltage, phase current, and CMC along with their harmonic spectra are akin with that of the results shown in Fig. 11. The components of the harmonic spectra are quantified and shown in the bottom plots of Figs. 12–14. The value of no-load phase current at fundamental frequency is nearly 1.6 A for all the three modulation indices. Furthermore, the third and fifth-harmonic components in the spectrum of CMC are very low ($<$ 20 mA for $m_a = 0.3$, 0.7, and 1) when compared to the no-load phase current. Whereas, the maximum harmonic content near the switching frequency is about 98, 18.5, and 38 mA for modulation indices 0.3, 0.7, and 1, respectively. The higher harmonic content (98 mA) for the value of $m_a = 0.3$ is because of its lower switching frequency. However, it could be minimized by increasing the number of samples per fundamental cycle.

Furthermore, to show the working of the proposed technique more effectively, another experiment is conducted ensuring identical operational conditions (dc-bus voltage of 100 V and modulation index of 0.7) for the same system. The only change is the offset time which is used as given in (21) for different PWM techniques. The obtained inverter pole voltages, motor phase voltage, and phase current are shown in Fig. 15(a)–(d) for CSSVPWM, LSDSVPWM, RSDSVPWM, and SAZE PWM techniques, respectively. From Fig. 15, it can be clearly observed that all the three conventional PWM techniques (except the SAZE PWM) would result in the flow

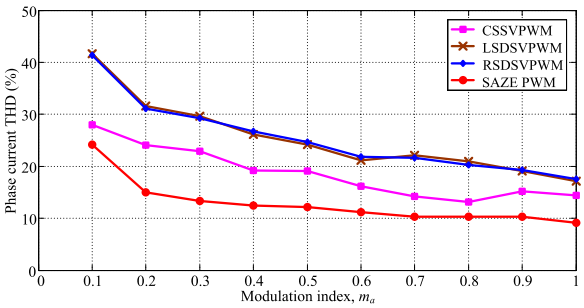

Fig. 16. Comparison of THDs in the experimentally obtained motor phase current using CSSVPWM, LSDSVPWM, RSDSVPWM, and the proposed SAZE PWM technqiues.

of CMC (in this case fourth-harmonic component) in the machine windings. The clamping nature in the inverter pole voltages can be observed from Fig. 15(b) and (c) for LS-D-SV-PWM and RS-D-SV-PWM techniques, which could reduce the switching losses, but induce the lower order harmonics in the motor phase current when single power source is used. However, these three PWM techniques could be used for the system with isolated power supplies, which could further increase the size, weight, and the cost. In addition, the experiment is repeated for the range of m_a from 0.1 to 1 using all the four PWM techniques and the THD in the motor phase current is calculated and the comparative results are plotted in Fig. 16. From Fig. 16, it is evident that the SAZE PWM technique results in lesser THD in the motor phase current when compared to all of the aforementioned conventional PWM techniques.

In addition to the phase current THDs, another parameter that could be compared is the computational burden on the controller/processor. The program execution time for each PWM technique is calculated using the profile clock available in the CCS. The starting and the ending points of the program are selected using the breaking points and the value for CPU cycles from the profile clock is noted. The obtained value of CPU cycles is divided by the processor clock frequency to get the time elapsed in executing the selected code. The calculated execution time for all the four PWM techniques is plotted and shown in Fig. 17. The execution time for CSSVPWM (29.1 μs), LSDSVPWM (28.9 μs), and RSDSVPWM (29 μs) techniques is nearly equal. But, the execution time for the proposed SAZE PWM is about 39.2 μs, which is slightly higher compared to the above three PWM techniques. However, in the present scenario of ever increasing clock frequencies of the processors this need not be portrayed as a shortcoming.

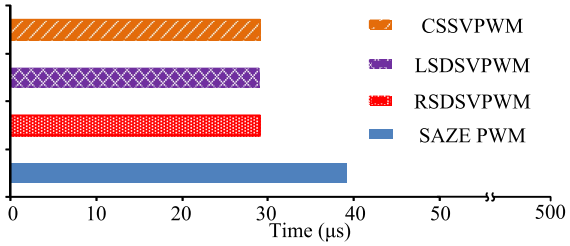

Fig. 17. Comparison of computational burden of the code used for CSSVPWM, LSDSVPWM, RSDSVPWM, and the proposed SAZE PWM techniques for the eZdspF28335 digital signal controller.

V. Conclusion

The SAZE PWM technique is proposed for the FPDI connected FPOEWIM drive with a single dc source. The challenging task for the FPOEWIM drive system is to eliminate both the CMC and the third-harmonic components. However, this is made possible by clamping both the large and medium voltage vectors together alternatively for inverter-I and inverter-II. The realization of large and medium voltage vectors together with the dwell time ratio of 0.618 helps in eliminating the third-harmonic components. In addition, the movement of effective time region helps in eliminating the CMC. This is supported by the simulation results and is verified using the experimental prototype. Hence, the proposed SAZE PWM technique eliminates the CMC as well as the third-harmonic content and could avoid heating of the machine [17] in the EV system.

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