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Discontinuous decoupled SVPWM schemes for a four-level open-end winding induction motor drive with waveform symmetries

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Suresh Lakhimsetty[1] ✉, *V.T. Somasekhar*[1]

[1]*Department of Electrical Engineering, National Institute of Technology Warangal, Warangal, India*

✉ *E-mail: suresh.201@gmail.com*

Abstract: A four-level open-end winding induction motor drive (OEWIMD) is realised by feeding the open stator windings of a three-phase induction motor from either end with two-level voltage source inverters (VSIs). These VSIs are operated with unequal DC-link voltages, which are in the ratio of 2:1. This circuit configuration has the disadvantage of overcharging the DC-link capacitor of the inverter operated with the lower input voltage. Decoupled space vector pulse-width modulation (DSVPWM) schemes, which were suggested in the previous literature to circumvent this problem, result in higher switching power loss in the dual-inverter topology. It is known that the discontinuous pulse-width modulation (PWM) schemes reduce the switching power loss. However, lack of structural symmetry of the power circuit renders it unwieldy to devise these PWM schemes. This study explores the applicability of discontinuous decoupled SVPWM (DDPWM) techniques for the four-level OEWIMD, without compromising on the waveform symmetries. With the aid of an improvised loss model, it is shown that these PWM schemes achieve the reduction of the overall loss of the four-level OEWIMD compared to the DSVPWM schemes. It has also been observed that one of the proposed DDPWM schemes result in reduced dv/dt in the motor phase voltages.

1 Introduction

Multilevel inverters (MLIs) are gaining popularity in the area of medium and high power industrial drive applications such as mining, petrochemical, cement, and marine industries [1]. The main advantages of MLIs compared to two-level inverters are (i) enhanced spectral performance, (ii) operability with higher DC-link voltages with low voltage devices, (iii) reduced stress on the switching devices, (iv) lower EMI and (v) lower bearing currents [2]. The most popular MLI topologies are divided into three generic categories, namely neutral point clamped (NPC), flying capacitor (FC) and cascaded H-bridge (CHB) types. In addition to these basic topologies, new and hybrid combinations of these topologies are reported in the literature [3]. Moreover, many pulse-width modulation (PWM) schemes are proposed for the control of these MLIs [4].

Of these power circuit configurations, the NPC topology requires special modulation techniques to control the unbalance in voltage of the neutral point. It also needs an increased number of clamping diodes at a higher number of voltage levels, leading to an increased complexity and decreased reliability in the power circuit. In the FC MLI topology, the requirement of capacitors increases exponentially with the number of voltage levels, making it difficult to balance the capacitor voltages. The major drawback of the CHB MLI is the requirement of several DC sources, as each H-bridge cell requires a separate DC source.

The concept of dual inverter fed open-end winding induction motor drive (OEWIMD) is relatively new, wherein the stator windings of a 3-∅ induction motor are opened and are fed with a two-level inverter from either side. While a motor is considered as a load for the rest of the MLI configurations, it is an inseparable entity in the case of an OEWIMD. It was shown that it is possible to derive multilevel phase voltage waveforms from this power circuit configuration [5–7]. The advantages and limitations of this configuration compared to the other MLI topologies are well documented [8]. The potential applications for the OEWIMD are electric vehicles [9, 10], aircraft motion control [11] and electric propulsion of ships [12], wherein employment of two individual DC power supplies may not be considered to be disadvantageous. It has also been reported that open-end winding topologies extend the operating speed range of PMSM [13] and three-phase induction motor drives [14].

The work reported in [15] describes a four-level OEWIMD. This topology is realised by feeding either end of the open stator windings of an induction motor with two-level VSIs with unequal DC-link voltages. These DC-link voltages are in the ratio of 2 : 1. This drive has a disadvantage; the lower voltage DC-link capacitor is overcharged by the DC-link capacitor of higher voltage [16].

The work reported in [15] identifies the space vector locations, which cause the overcharging of the lower DC-link capacitor and avoids them. This space vector PWM (SVPWM) technique calls for the sector identification and look-up tables making it complex to implement. The work reported in [17] proposes an alternative approach to the implementation of SVPWM, which is based on the concept of fractals. This PWM strategy results in a faster computation, despite the necessity of sector identification and switching vector determination. However, the problem of overcharging of the lower DC-link capacitor is not addressed in this work.

The problem of overcharging of the lower DC-link capacitor is tackled with the decoupled SVPWM techniques reported in [16]. Two variants of the decoupled SVPWM schemes were described in [16], namely the equal duty PWM (EDPWM) technique and the proportional duty PWM (PDPWM) technique. In both of these schemes, the reference voltage space vector of the dual-inverter scheme is resolved into two anti-phased references for the individual inverters, which are in the proportion of 2 : 1. These individual reference voltage vectors are then synthesised with the respective inverters. It was shown that compared to the EDPWM scheme, the PDPWM scheme results in 10% lesser switching power loss in the dual-inverter scheme [16]. These decoupled SVPWM schemes make use of the concepts developed in [18] to obtain the quarter-wave, half-wave and the three-phase symmetries.

The circuit topology reported in [19] avoids overcharging of the lower DC-link capacitor as well as the flow of zero-sequence current. However, it has a serious limitation in that its applicability is restricted to motors with '6n' (where 'n' is a positive integer) number of poles. The circuit topology described in [20] avoids the flow of zero-sequence current, only in the average sense. It achieves this objective by resorting to the so-called sample

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averaged zero-sequence elimination PWM scheme. However, this power circuit configuration suffers from the disadvantage of requiring three separate power supplies. Also, the instantaneous value of the zero-sequence current is not equal to zero, which manifests as higher ripple content in the motor phase current.

Thus, there is an adequate motivation to investigate if the power circuit configuration shown in Fig. 1*a* [15], which needs only two power supplies, does not restrict the number of poles and suppresses the zero-sequence current at every instant, is amenable to further improvisation.

This paper presents discontinuous decoupled SVPWM (DDPWM for the rest of the paper) techniques for a four-level OEWIMD shown in Fig. 1*a*. Admittedly, these PWM schemes are well known for a simple two-level voltage source inverter (VSI). However, the extension of these PWM techniques for the four-level OEWIMD is not straightforward on account of the unsymmetrical nature of the power circuit. It is an interesting as well as a challenging proposition to derive the switching patterns to implement the DDPWM scheme (to lower switching power losses) and derive all the aforementioned waveform symmetries from an unsymmetrical network with DDPWM schemes.

In this paper, a critical comparison of the DDPWM schemes with the EDPWM and the PDPWM schemes is also undertaken. To this end, an improvised loss model is devised to evaluate the conduction and the switching power losses in the dual-inverter scheme. This model also calculates the ripple in the motor phase current, leading to the estimation of the I^2R (i.e. ohmic) losses in the motor. It is, therefore, possible to estimate the overall power loss incurred in the four-level OEWIMD, which is the sum of the power loss in the dual-inverter topology and the ohmic loss in the motor. Also, this model facilitates the evaluation of various indices of performance such as total harmonic distortion (THD), weighted THD (WTHD) and the switching loss factor (SLF).

Simulation and experimental results indicate that the DDPWM techniques perform better compared to the decoupled centre spaced SVPWM techniques while avoiding the overcharging of the capacitor of the lower voltage DC link.

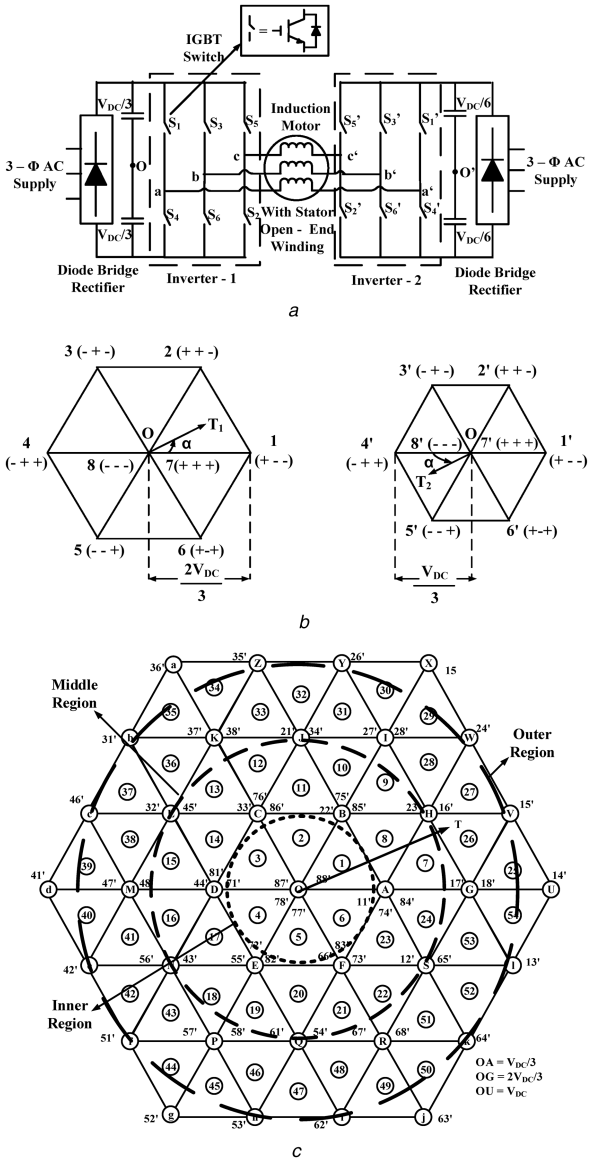

Fig. 1 *Circuit configuration, individual space vector diagrams and resultant space vector diagram of four-level OEWIMD*

(a) Circuit configuration for four-level OEWIMD, ***(b)*** Individual space vector diagrams for inverter-1 (left) and 2 (right), ***(c)*** Resultant Space vector diagram of the four-level OEWIMD

2 Four-level OEWIMD

The four-level OEWIMD is obtained by the dual-inverter configuration, which is constituted by two two-level VSIs, which have their respective DC-link voltages in the ratio of 2:1. Each VSI feeds one end of the open stator windings of the motor as shown in Fig. 1*a*. It may be noted from Fig. 1*a* that, inverter-1 is operated with a higher DC-link voltage ($2V_{DC}/3$), while inverter-2 is operated with a lower DC-link voltage ($V_{DC}/3$). Each inverter can individually assume eight states. The states of inverter-1 are denoted as 1–8, while those of inverter-2 are represented as $1' - 8'$ (Fig. 1*b*). The resultant space vector diagram, having 64 space vectors is shown in Fig. 1*c*.

The pole voltages of inverter-1 have denoted as v_{ao}, v_{bo} and v_{co}. The inverter-1 pole voltage is made to toggle between the levels $+V_{DC}/3$ and $-V_{DC}/3$. Similarly, the inverter-2 pole voltages are represented as $v_{a'o'}, v_{b'o'}$ and $v_{c'o'}$, and are switched between the levels $+V_{DC}/6$ and $-V_{DC}/6$. To begin with, it is assumed that the points 'o' and 'o'' (Fig. 1*a*) are connected together (i.e. they are equipotential). Thus, the differences between them, which are essentially the motor phase voltages in an OEWIM, are given by

$$\Delta v_{aa'} = v_{ao} - v_{a'o'} \tag{1}$$

$$\Delta v_{bb'} = v_{bo} - v_{b'o'} \tag{2}$$

$$\Delta v_{cc'} = v_{co} - v_{co'} \tag{3}$$

Table 1 enumerates the levels in the pole voltages of individual inverters and the difference between them.

It is well known that denial of a closed path hinders the flow of zero-sequence current in OEWIMDs. It is achieved by feeding individual VSIs of OEWIMD with isolated DC power supplies. Under these conditions, the zero-sequence voltage is dropped across the points 'o' and 'o''. The zero-sequence voltage is defined as

$$v_{oo'} = \frac{1}{3}(\Delta v_{aa'} + \Delta v_{bb'} + \Delta v_{cc'}) \tag{4}$$

Consequently, the phase voltage across the OEWIM is defined as the difference between the difference of pole voltages and the zero-sequence voltage across the points 'o' and 'o'', and is given as

$$v_{aa'} = \Delta v_{aa'} - v_{oo'} \tag{5}$$

$$v_{bb'} = \Delta v_{bb'} - v_{oo'} \tag{6}$$

$$v_{cc'} = \Delta v_{cc'} - v_{oo'} \tag{7}$$

3 DDPWM strategy for four-level OEWIMD with equal duty

The vector ***OT*** (i.e. $|v_{ref}|$) shown in Fig. 1*c* represents the reference voltage space vector for the overall dual-inverter fed four-level OEWIMD system. The vector ***OU*** (Fig. 1*c*), which measures V_{DC},

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represents the effective DC-link voltage of the dual-inverter topology (the sum of the respective DC-link voltages of individual inverters). The vector $\boldsymbol{OT}$ is to be produced in the average sense using a suitable SVPWM technique. The reference voltage space vector $\boldsymbol{OT}$ is sampled 42 times per cycle, irrespective of the fundamental frequency. For a conventional two-level inverter, such a sampling would result in seven samples per sector. The angular interval between successive samples would then be equal to 8.57° (i.e. 360°/42) and the first sample of any cycle is placed at 4.28°, to avoid samples on the sector boundaries. It was shown in [18] that such measures achieve the attainment of the waveform symmetries mentioned in Section 1.

In this work, the proposed SVPWM scheme is applied to the four-level OEWIMD, which is operated in open-loop with v/f control. The rated voltage and the rated frequency of the motor are 400 V (line–line) and 50 Hz, respectively. The modulation index of dual inverter drive is defined as

$$m_a = \frac{|\boldsymbol{v}_{\text{ref}}|}{V_{\text{DC}}} \tag{8}$$

Further, the overall DC-link voltage ($|\boldsymbol{OU}|$, Fig. 1*c*) is scaled in such a way that the rated voltage and the rated frequency are applied at the edge of liner modulation (i.e. $m_a = \sqrt{3}/2$). For the aforementioned motor, the overall DC-link voltage becomes equal to 564 V. Thus, the frequency of the fundamental component of the dual inverter drive, operated with a modulation index of m_a is given by

$$f_1 = \frac{m_a}{\sqrt{3}/2} \times 50 \tag{9}$$

The sampling time period (T_{s}) of each inverter of dual inverter topology can be defined as

$$T_{s1} = T_{s2} = T_{\text{s}} = T_{\text{o}}/42 \tag{10}$$

where $T_{\text{o}} = 1/f_1$ is the time period of the fundamental component of the dual-inverter drive.

The operating principle of DDPWM techniques is explained with the help of Fig. 1*b*. The reference voltage vector $\boldsymbol{OT}$ (Fig. 1*c*) of the dual inverter topology is realised with the help of two two-level VSIs having reference voltage vectors of $\boldsymbol{OT}_1$ (for inverter-1) and $\boldsymbol{OT}_2$ (for inverter-2) as shown in Fig. 1*b*. Since the DC-link voltages of respective inverters are in the ratio of 2 : 1, it is logical to resolve the reference vectors for the individual inverters in the same ratio. It is also obvious that the reference vectors for the individual inverters should be opposite to each other as the motor phase voltage is the *difference* of the individual pole voltages (1)–(7).

Thus, when the reference voltage space vector for the dual-inverter system is equal to $|\boldsymbol{v}_{\text{ref}}|\angle\alpha$ (Fig. 1*c*), the reference vectors of the individual inverters are $|2\boldsymbol{v}_{\text{ref}}/3|\angle\alpha$ and $|\boldsymbol{v}_{\text{ref}}/3|\angle(180^\circ + \alpha)$, respectively. For the situation depicted in Figs. 1*c* and *b* (wherein $\boldsymbol{OT} = \boldsymbol{OT}_1 + \boldsymbol{OT}_2$), the vector $\boldsymbol{OT}_1$ is synthesised with inverter-1, by switching among the states $8 - 1 - 2 - 7$ (states corresponding to sector-1, Fig. 1*b*), while the opposite vector $\boldsymbol{OT}_2$ is synthesised by the inverter-2, while switching among the states $8' - 5' - 4' - 7'$ (states corresponding to sector-4, Fig. 1*b*).

The switching algorithm presented in [21] for the conventional two-level VSI is extended to the dual-inverter system pertaining to the four-level OEWIMD, by applying it to the individual inverters. This switching algorithm needs only the instantaneous phase reference voltages unlike the conventional implementation of the SVPWM scheme (which needs look-up tables and sector identification).

The above discussion leads to the fact that, if the reference voltage space vector $\boldsymbol{OT}$ (which corresponds to the dual-inverter system) is constructed by the instantaneous phase voltage references – (v_a^*, v_b^* and v_c^*), then the reference voltage vectors for the individual inverters ($\boldsymbol{OT}_1$ and $\boldsymbol{OT}_2$) are constituted by the sets: $\{2v_a^*/3,\ 2v_b^*/3,\ 2v_c^*/3\}$ (for inverter-1) and $\{-v_a^*/3,\ -v_b^*/3,\ -v_c^*/3\}$ (for inverter-2).

The algorithm presented in [21] is based on the concept of imaginary switching times. The imaginary switching times for the inverter-1 and inverter-2 are given as

$$T_{xs1} = (T_{\text{s}}/V_{\text{DC}}) \times (2v_x^*/3), \quad x \in a, b, c \tag{11}$$

$$T_{xs2} = (T_{\text{s}}/V_{\text{DC}}) \times (-v_x^*/3), \quad x \in a, b, c \tag{12}$$

The time period during which active power is transferred from the input DC bus to the output AC lines of the inverter is called the effective time period and is denoted with the symbol $\boldsymbol{T}_{\text{eff}}$. This duration is equal to the sum of the switching periods of the two active states of the pertinent sector. Thus, for the individual inverters of the dual-inverter scheme [21]

$$T_{\text{eff1}} = T_{\text{max1}} - T_{\text{min1}} \tag{13}$$

$$T_{\text{eff2}} = T_{\text{max2}} - T_{\text{min2}} \tag{14}$$

where $T_{\text{max1}} = \max(T_{as1}, T_{bs1}, T_{cs1})$, $T_{\text{min1}} = \min(T_{as1}, T_{bs1}, T_{cs1})$, $T_{\text{max2}} = \max(T_{as2}, T_{bs2}, T_{cs2})$ and $T_{\text{min2}} = \min(T_{as2}, T_{bs2}, T_{cs2})$.

During the remaining time period of the sampling time interval $\boldsymbol{T}_{\text{s}}$, there is no power flow from the input DC rails to the output AC side of the inverter. This time interval is called as the zero-vector (or the null-vector) time period and is denoted as $\boldsymbol{T}_z$. The null-vector time periods for the individual inverters are given by

$$T_{z1} = T_{\text{s}} - T_{\text{eff1}} \tag{15}$$

$$T_{z2} = T_{\text{s}} - T_{\text{eff2}} \tag{16}$$

The offset time needed for the centre spacing of the effective time period within the sampling time interval of $\boldsymbol{T}_{\text{s}}$ for both inverters given as

$$T_{\text{offset1}} = T_{z1}/2 - T_{\text{min1}} \tag{17}$$

$$T_{\text{offset2}} = T_{z2}/2 - T_{\text{min2}} \tag{18}$$

The phase switching time period of any given phase of the constituent inverters is defined as the time period for which that phase terminal is connected to the positive rail of the respective input DC bus. It is shown in [21] that the phase switching time periods $\{T_{ga1}, T_{gb1}, T_{gc1}\}$ for inverter-1 and $\{T_{ga2}, T_{gb2}, T_{gc2}\}$for inverter-2 are related to imaginary switching time periods T_{xs1} and T_{xs2}, respectively, by a simple expression

Table 1 Voltage levels in dual inverter system

Pole voltage of inverter-1 (v_{ao})	Pole voltage of inverter-2 ($v_{a'o'}$)	Difference of pole voltages ($v_{ao} - v_{a'o'}$)
$V_{\text{DC}}/3$	$-V_{\text{DC}}/6$	$V_{\text{DC}}/2$
$V_{\text{DC}}/3$	$V_{\text{DC}}/6$	$V_{\text{DC}}/6$
$-V_{\text{DC}}/3$	$-V_{\text{DC}}/6$	$-V_{\text{DC}}/6$
$-V_{\text{DC}}/3$	$V_{\text{DC}}/6$	$-V_{\text{DC}}/2$

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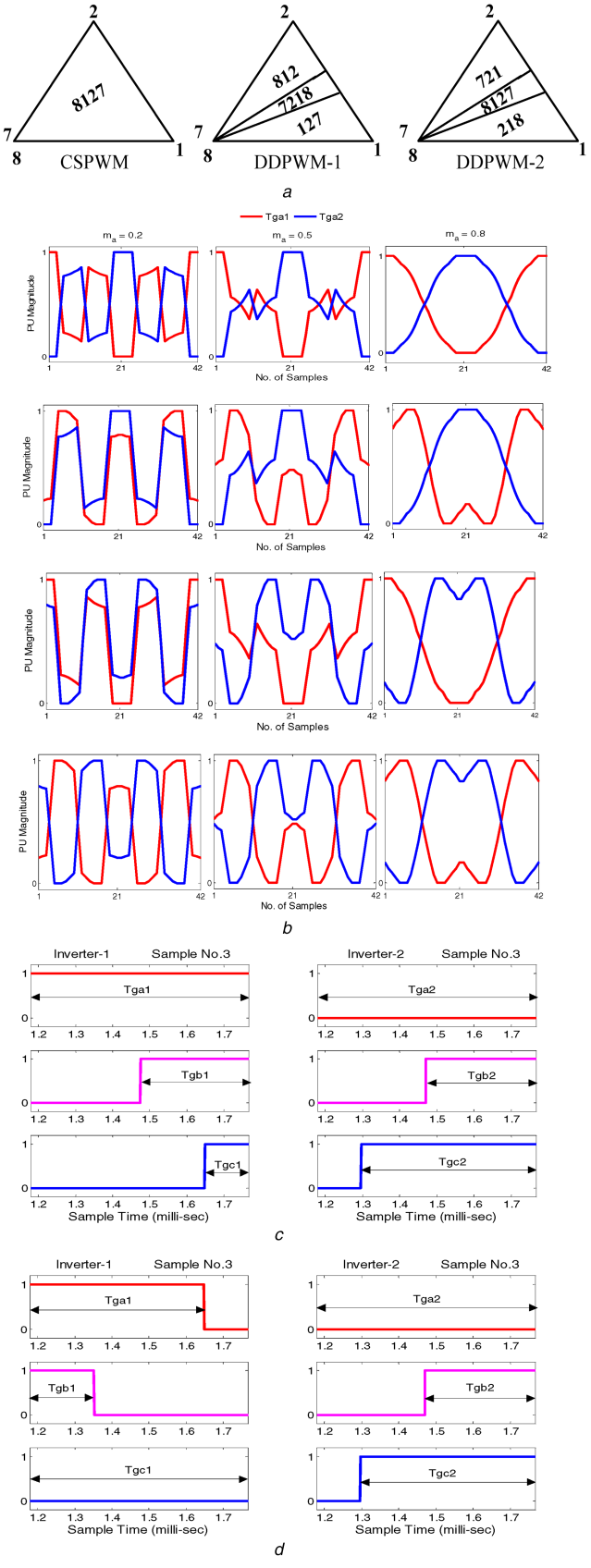

Fig. 2 *Sequence of voltage vectors applied, modulating signals and switching time periods of the DDPWMs*

(a) Sequence of voltage vectors applied in sector-I for the conventional two-level VSI for CSPWM (left), DDPWM-1 (middle), DDPWM-2 (right), ***(b)*** Modulating signals for DDPWM-1 (top), DDPWM-2 (second), DDPWM-3 (third) and DDPWM-4 (bottom), ***(c)*** Switching time periods for inverter-1 (left column) and inverter-2 (right column) with DDPWM-1, ***(d)*** Switching time periods for inverter-1 (left column) and inverter-2 (right column) with DDPWM-2

$$T_{gx1} = T_{xs1} + T_{\text{offset}_1}, \quad x \in a, b, c \tag{19}$$

$$T_{gx2} = T_{xs2} + T_{\text{offset}_2}, \quad x \in a, b, c \tag{20}$$

It could be helpful to recapitulate briefly about the implementation of SVPWM schemes for the conventional two-level inverter, which provides an impetus for the four-level dual-inverter fed OEWIMD. For the conventional two-level VSI, the PWM strategy implemented with the offset time period given by (17) (or 18) results in the centre spacing of the effective time period ($\boldsymbol{T}_{\text{eff}}$) in any given sampling time period. For this reason, this decoupled PWM scheme is called as the *Centre-Spaced PWM* (CSPWM). Two more well-known variants of the PWM scheme, called *Discontinuous Decoupled PWM* (DDPWM) schemes, which are also known as the *Phase-Clamped SVPWM* schemes, are implemented by the placement of the effective time periods at either end of a sampling time period. In the first variant of these two, the *DDPWM-1*, the effective time period is kept at the extreme left corner, while in the other, the *DDPWM-2*, it is placed at the extreme right corner. These two PWM schemes are implemented with simple alterations in the offset time period. The offset time periods of $(-T_{\min})$ and $(T_s - T_{\max})$, respectively, implement *DDPWM-1* and *DDPWM-2* [21]. The switching sequences used for the implementation of these three PWM schemes for the conventional two-level VSI in *sector-1* are depicted in Fig. 2*a*. It is assumed that 42 samples are employed per cycle (i.e. 7 samples/sector).

It may be noted that the CSPWM employs the conventional sequences 8-1-2-7 and 7-2-1-8 alternatively as shown on the left of Fig. 2*a*. It may also be noted that the beginning and ending sequences for *DDPWM-1*, respectively, are 1-2-7 and 8-1-2 (i.e. for samples 1 and 7). The centre sample (i.e. sample no. 4) should be so implemented as to facilitate a natural transition between these two sequences. Also, in the interest of symmetry, the effective time period should be centre spaced as shown in Fig. 2*a* (middle). Both of these requirements are automatically achieved by implementing the centre sample with CSPWM, using the sequence 7-2-1-8 [18]. The switching sequences for the other sectors may similarly be worked out. It then follows that the centre samples of all the six sectors, which are situated at 30°, 90°, 150°, 210°, 270° and 330°, should be implemented with centre spacing [18]. One can devise the switching sequences for DDPWM-2 in a similar manner by choosing the initial, centre and end sequences as 2-1-8, 8-1-2-7 and 7-2-1, respectively, (Fig. 2*a* (right)).

As mentioned in the earlier section, the reference phase voltages corresponding to the four-level dual-inverter scheme ***OT*** (Fig. 1*c*) are resolved in the ratio of 2 : 1 for the individual inverters and are anti-phased w.r.t. each other to implement the *Decoupled SVPWM* scheme [16]. The references of the individual inverters are then synthesised in the average sense using SVPWM technique. The *effective time period*, which is the sum of the time periods during the active vectors are switched ($\boldsymbol{T}_1 + \boldsymbol{T}_2$), is kept exactly at the centre of each sampling time interval [16]. The principal drawback of this scheme is that it calls for the switching of all the three phases of both inverters (i.e. a total of six switching's in any given sampling time interval), causing excessive switching loss.

This is the motivating factor to explore the possibilities of implementing the DDPWM schemes for the dual-inverter system. However, deriving waveform symmetries with DDPWM schemes is a difficult proposition due to the lack of symmetry in the structure of the power circuit configuration (Fig. 1*a*) as well as the DDPWM schemes.

Table 2 demonstrates the switching sequences used for both of the inverters to implement the DDPWM schemes in sector-1 (i.e. for a span of 60°). As explained earlier, in the decoupled SVPWM scheme, the references of inverter-2 are anti-phased w.r.t. the references of inverter-1. Consequently, the vectors output by inverter-2 are opposite to those output by inverter-1 (Table 2). The modulating signals corresponding to the inner, the middle and the outer regions of the hexagon corresponding to the modulation indices of 0.2, 0.5 and 0.8 are presented in Fig. 2*b*. It is easily observed that the inner region corresponds to $m_a \leq 1/2\sqrt{3}$. The

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Table 2 Switching sequences of DDPWMs-1, 2, 3 and 4 in sector-1

Sample no.	Switching sequences of individual inverters with DDPWM-1		Switching sequences of individual inverters with DDPWM-2		Switching sequences of individual inverters with DDPWM-3		Switching sequences of individual inverters with DDPWM-4	
	Inverter-1	Inverter-2	Inverter-1	Inverter-2	Inverter-1	Inverter-2	Inverter-1	Inverter-2
1	1-2-7	8-5-4	2-1-8	8-5-4	1-2-7	7-4-5	2-1-8	7-4-5
2	7-2-1	4-5-8	8-1-2	4-5-8	7-2-1	5-4-7	8-1-2	5-4-7
3	1-2-7	8-5-4	2-1-8	8-5-4	1-2-7	7-4-5	2-1-8	7-4-5
4	7-2-1-8	7-4-5-8	8-1-2-7	7-4-5-8	7-2-1-8	8-5-4-7	8-1-2-7	8-5-4-7
5	8-1-2	5-4-7	7-2-1	5-4-7	8-1-2	4-5-8	7-2-1	4-5-8
6	2-1-8	7-4-5	1-2-7	7-4-5	2-1-8	8-5-4	1-2-7	8-5-4
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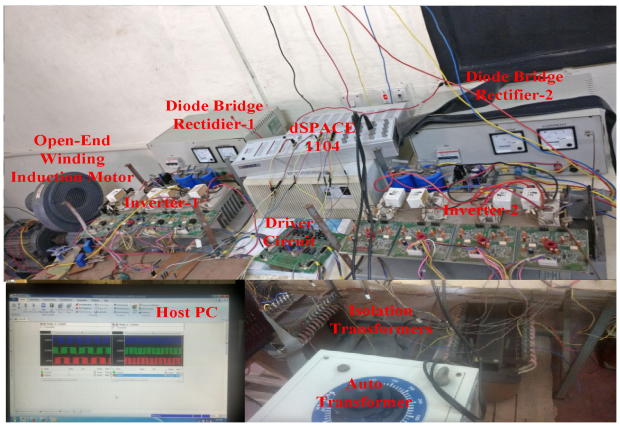

Fig. 3 *Experimental setup of four-level OEWIMD*

middle and the outer regions, respectively, correspond to $(1/2\sqrt{3} \leq m_a \leq 1/\sqrt{3})$ and $m_a \geq 1/\sqrt{3}$ (Fig. 1*c*).

It is evident from the traces presented in Fig. 2*b*, that each phase is clamped for 120°. It may, therefore, be anticipated that the switching losses would be less with DDPWM schemes as compared to the decoupled SVPWM strategies proposed in [16]. From the modulating signals, it can be observed that the modulating waves of the individual inverters are in two different shapes and are alternatively assigned to the individual inverters of the dual inverter system to form the four proposed DDPWMs. Figs. 2*c* and *d* present the typical gating signals for the proposed DDPWM-1 and 2 schemes at sample no. 3 (i.e. $\alpha = 21.42°$, Fig. 1*c*). The PWM signals for the other two DDPWM schemes are not presented in the interest of brevity.

From these traces, it is evident that the A-phase is clamped for both of the inverters with DDPWM-1. In contrast, two different phases are clamped in the respective inverters with DDPWM-2 (Phase-A for inverter-1 and Phase-C for inverter-2). Also, the sequence of switching is the same for both of the inverters with DDPWM-1 ('low' to 'high'). However, with DDPWM-2, the sequences are different for the two inverters. It may be observed that while inverter-2 has the same switching sequence as in the case of DDPWM-1, inverter-1 has the reverse switching sequence ('high' to 'low'). This behaviour is the direct consequence of the fact that while the modulating functions are identical for inverter-2, they are different for inverter-1 (Fig. 2*b*). It may, therefore, be intuitively reasoned out that DDPWM-1 should result in a better harmonic performance compared to DDPWM-2 on account its structural symmetry. Similar observations and conclusions can be drawn for the DDPWM-3 and DDPWM-4 as well.

4 Simulation and experimental results

The simulation and experimental results for the four-level OEWIMD, with the proposed DDPWM techniques are presented in this section. For verification, an experimental setup of Fig. 1 has been built in the laboratory. Its physical layout is given in Fig. 3. The experimental set up consists of an auto-transformer, two isolation transformers, two diode bridge rectifiers, two three-phase voltage source inverters, a *dSPACE-1104* control platform with a host PC to produce the gating signals and a three-phase OEWIMD.

Inverter-1 and inverter-2 (Fig. 1*a*) are operated with the respective DC-link voltages of 200 and 100 V, to obtain an effective DC-link voltage of 300 V for the dual-inverter system ($|\boldsymbol{OU}|$, Fig. 1*c*).

The voltage to frequency ratio is maintained in such a way that the rated frequency of 50 Hz is applied at the edge of linear modulation. Above this limit, the dual inverter system operates in the region of overmodulation, wherein the relationship between the modulation index and the output voltage of the dual-inverter system is non-linear.

The simulated waveforms are presented for the cases of linear modulation, at modulation index (m_a, (8)) of 0.2 and 0.7. The frequency of the fundamental component corresponding to $m_a = 0.2$ and 0.7 is 11.55 and 40.4 Hz (9), respectively. Fig. 4 shows the simulated phase-A voltage, current and FFT analysis for the DDPWM-1, 2, 3 and 4 techniques at $m_a = 0.2$. The simulated waveforms of the dual inverter control signals, phase-A voltage, current and phase-A voltage harmonic spectrum for the DDPWM-1, 2, 3 and 4 techniques at the modulation index of 0.7 are shown in Fig. 5.

Comparing the voltage spectra (bottom trace) presented in Figs. 5*a–d*, it is clear that DDPWM-1 results in a better spectral performance compared to DDPWM-2, 3 and 4 for the four-level dual-inverter system (as predicted in the previous section). This fact is also evident from the traces of motor phase-A voltage and current (Figs. 5*a–d*).

The experimental waveforms are presented for the cases of (i) linear modulation, at a modulation index of 0.2, 0.7 and (ii) for the case of over modulation. The experimental common mode voltage, which is dropped across the points o and o' (Fig. 1*a*), phase-A voltage and current waveforms are shown in Fig. 6, at $m_a = 0.2$, for all of the four DDPWM techniques. The control signals generated from the dSPACE 1104 for the DDPWM-1 and 2 techniques in one cycle are shown in Fig. 7. The experimental waveforms at $m_a = 0.7$ are shown in Fig. 8. Fig. 8*a* shows the experimental waveforms of

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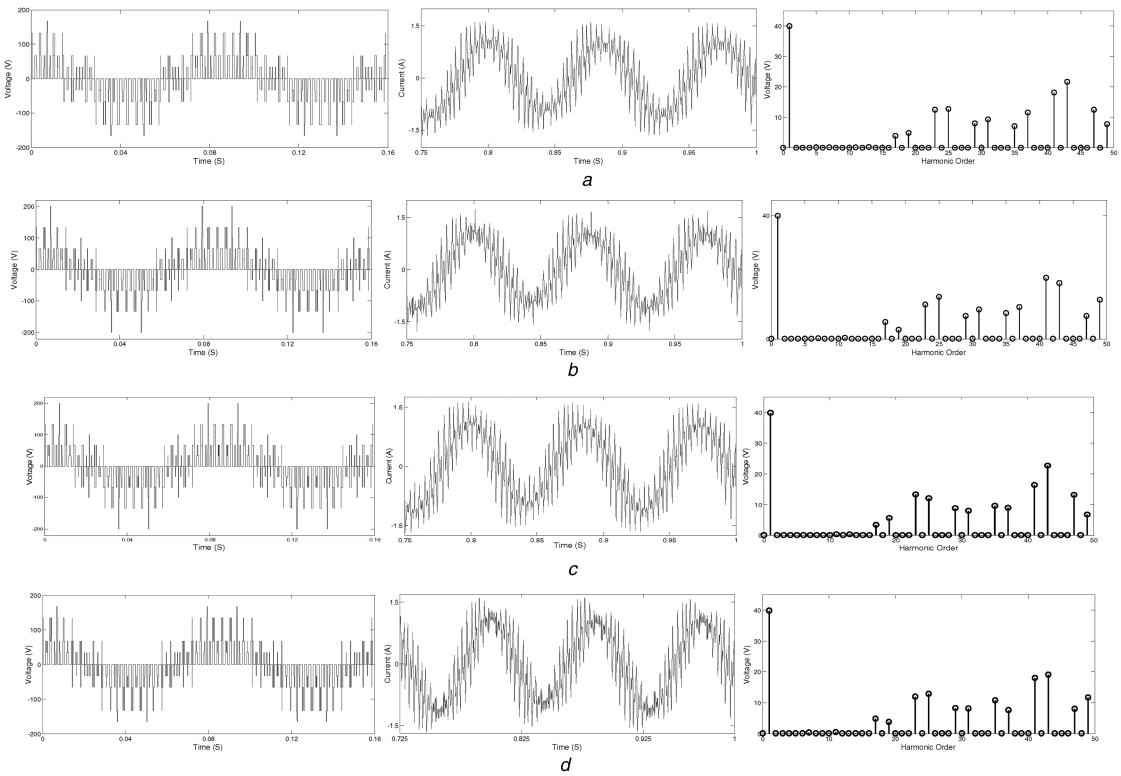

Fig. 4 *Simulated Phase-A voltage, current and harmonic spectrum of DDPWMs-1, 2, 3 and 4 at $m_a = 0.2$*
(a)–(d) Simulated Phase-A voltage (left), current (middle) waveforms and harmonic spectrum of phase-A voltage (right) of DDPWMs-1, 2, 3 and 4, respectively

inverter-1 (left) and inverter-2 (right) pole voltages. Fig. 8*b* shows the experimentally obtained zero-sequence voltage. The experimentally obtained phase-A voltage and current waveforms are shown in Fig. 8*c*. The experimental voltage and current waveforms of phase-A in the case of over modulation (i.e. $m_a \geq 1$) are shown in Fig. 8*d*.

The experimental results for the case of the DDPWM-2 technique are shown in Fig. 9 for $m_a = 0.7$ and for over modulation. The experimental pole voltage waveforms for both of the inverters are shown in Fig. 9*a*. Comparison of the pole voltages obtained for DDPWM-1 (Fig. 8*a*) and DDPWM-2 (Fig. 9*a*) reveals that the pole voltages of inverter-2 appear identical, while the pole voltages are different for inverter-1. This result is anticipated as the modulating functions of inverter-2 are identical for both of the DDPWM schemes, while they are different for inverter-1 (Fig. 2*b*). Fig. 9*b* shows the experimental waveform of common mode voltage for DDPWM-2. The practically obtained phase-A current and voltage waveforms are shown in Fig. 9*c*. In the case of over modulation, the experimentally obtained phase-A voltage and current waveform are shown in Fig. 9*d*.

Similar experimental waveforms are presented in the case of DDPWMs-3 and 4 in Figs. 10 and 11, respectively. In the case of the DDPWMs-3 and 4, the experimental pole voltages are not presented. In DDPWM-3, the switching sequences of the respective inverters are the reversed versions of those for DDPWM-2 in any given sector. For example, the switching sequence corresponding to the first sample in DDPWM-3 (1-2-7) is obtained by reversing the switching sequence corresponding to the seventh sample (7-2-1) of DDPWM-2. In DDPWM-4, the switching sequences applied to inverter-1 and inverter-2 are identical to the switching sequence of the inverter-1 of the DDPWM-2 and inverter-2 of the DDPWM-3, respectively (see Table 2).

5 Comparative analysis of DDPWM and CSPWM strategies

This section critically compares the proposed decoupled DDPWM techniques with the decoupled *Centre-Spaced* PWM schemes proposed in [16]. The decoupled SVPWM techniques proposed in [16] are named as *Equal-Duty PWM* (EDPWM) and *Proportional-Duty* PWM (PDPWM). To ensure fairness in comparison, both inverters are switched with 42 samples /cycle, for all the four of the PWM schemes. However, the comparable situation in the case of PDPWM technique is to switch inverter-1 and inverter-2 (Fig. 1*a*) with 30 and 54 samples/cycle, respectively [16]. In order to be consistent with the experimental results, inverter-1 and inverter-2 are operated with individual DC-link voltages of 200 and 100 V, respectively (i.e. the total effective DC-link voltage of the dual-inverter system is 300 V).

The loss analysis for the dual-inverter system is carried out on the basis of the losses incurred per one phase-leg (say phase-A of inverter-1), as shown in Fig. 12*a*. The IGBTs of the phase-A leg are represented as T_A^+, T_A^- and their anti-parallel diodes are denoted by D_A^+, D_A^-.

The top trace of Fig. 12*b* shows the typical gating waveform for the IGBT T_A^+. The second trace shows the current flowing through the switching device T_A^+ and the anti- parallel diode D_A^- while considering the diode reverse recovery current into account. The third trace shows the voltage across the switch T_A^+ and the anti-parallel diode D_A^- [22]. The last trace shows the total power loss incurred in the device, which includes the switching, and conduction power losses in T_A^+ and the conduction loss in the diode D_A^-.

The switching power loss (P_{SW}) and conduction power loss (P_{CON}) are given by [22]

$$P_{\mathrm{SW}} = \left[\frac{1}{2} v_{\mathrm{SW}} i_{\mathrm{SW}} (t_{ri} + t_{\mathrm{fv}}) + \frac{1}{2} v_{\mathrm{SW}} i_{\mathrm{SW}} (t_{\mathrm{rv}} + t_{\mathrm{fi}})\right] \times f_{\mathrm{s}} \quad (21)$$

$$P_{\mathrm{CON}} = \frac{V_{\mathrm{ON}} I_{\mathrm{ON}} t_{\mathrm{ON}}}{T_{\mathrm{s}}} \quad (22)$$

where v_{SW} is the voltage blocked by the switch in its OFF-state (i.e. V_{DC}), $i_{\mathrm{SW}} = I_{\mathrm{ON}}$ is the current flowing through the switch in its ON-state, f_{s} is the switching frequency, $T_{\mathrm{s}} = 1/f_{\mathrm{s}}$ is the switching time period, v_{ON} is the on-state voltage drop, t_{ri}, t_{rv} are the rise

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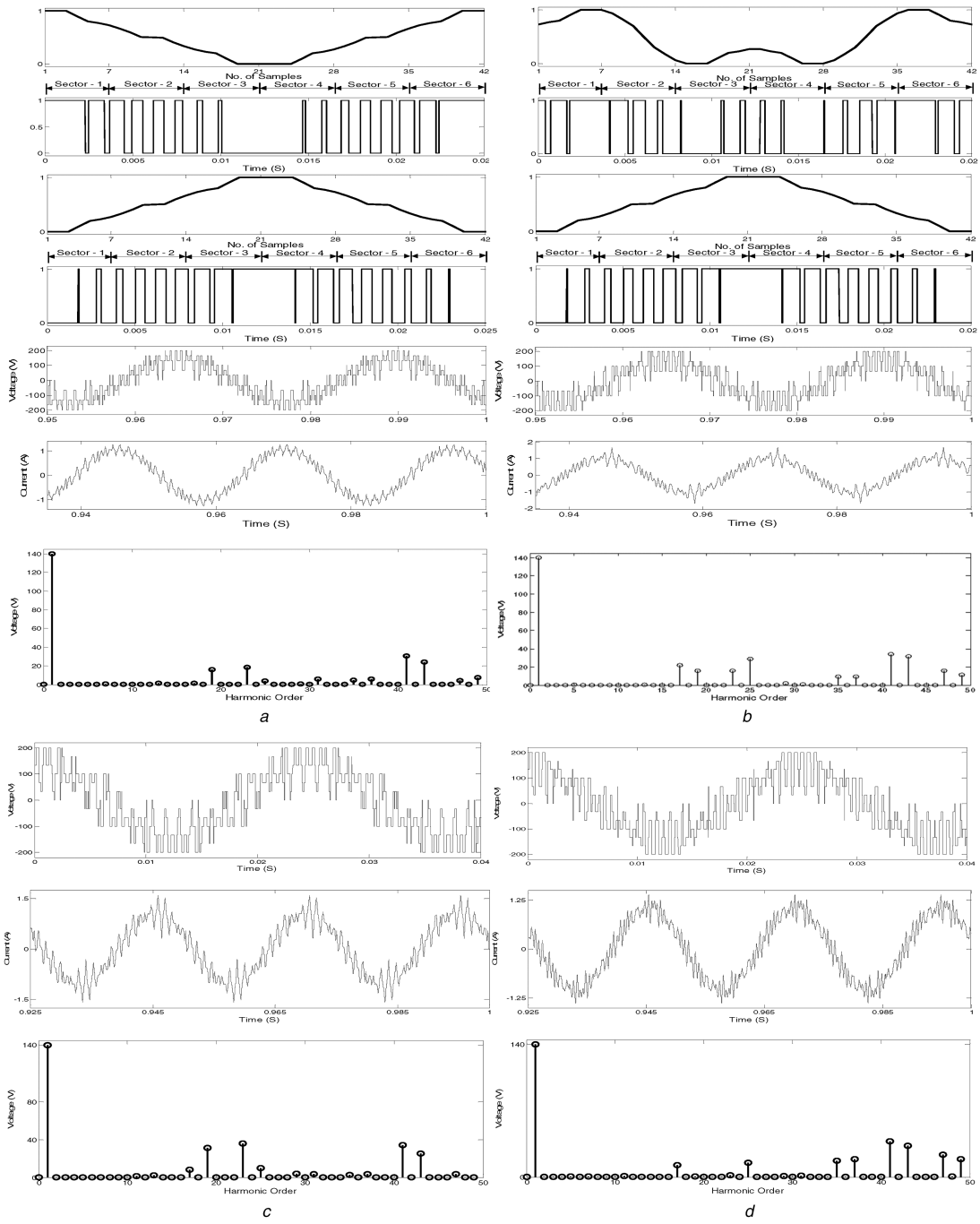

Fig. 5 *Simulated control signals, Phase-A voltage, current and harmonic spectrum of DDPWMs-1, 2, 3 and 4 at $m_a = 0.7$*

(a), ***(b)***Simulated control signals of inverter-1 (top), inverter-2 (second), Phase-A voltage (third), current (fourth) waveforms and harmonic spectrum of phase-A voltage (bottom) of DDPWMs-1 and 2, respectively, ***(c)***, ***(d)*** Simulated Phase-A voltage (top), current (second) waveforms and harmonic spectrum of phase-A voltage (bottom) of DDPWMs-3 and 4, respectively

times of current and voltage, t_{fv}, t_{fi} are the fall times of voltage and current, and t_{ON} is the switch turn-on time.

Computation of the switching and conduction losses of the switching devices is facilitated by the loss-computation model, suggested in [23]. However, the loss model suggested in [23], neglects the diode conduction loss and the additional power loss incurred due to the reverse recovery current of the diode. Fig. 12*c* shows an improvised loss-model, developed in [24], which accounts for these losses (Fig. 12*c*). This model is further improvised in this paper by adding the feature of extracting the RMS value of the motor phase current (which contains the ripple component due to the switching action of the inverters). The RMS value of the motor phase current is pivotal to the computation of the ohmic loss in the motor. Thus, it is possible to estimate the overall loss in the drive system with the improvised model, which is the sum of the losses occurring in the dual-inverter system and the motor.

The switching and conduction losses in each switching device are computed by assuming the following data: $t_{fv} = 1\ \mu s$, $t_{rv} = 2\ \mu s$, $t_{fi} = 4\ \mu s$, $t_{ri} = 2\ \mu s$ and $v_{ON} = 1\ V$. To ensure a fair comparison, this data is kept identical for all the six PWM schemes (i.e. the four proposed DDPWM techniques and the two centre spaced decoupled SVPWM schemes described in [16]). Keeping in view of the fact that the losses in the power semi-conductor switching devices as well as the motor ohmic loss are both load dependent, a load torque of 5 N m is applied to the OEWIM chosen for analysis (5 HP, i.e. 3.7 kW, 1430 RPM, 50 Hz). The parameters of the OEWIMD, which are needed to extract the RMS phase current are given in Table 3.

Fig. 12*d* shows the simulation results in per-unit representation, which are obtained by using the improvised loss, model (Fig. 12*c*).

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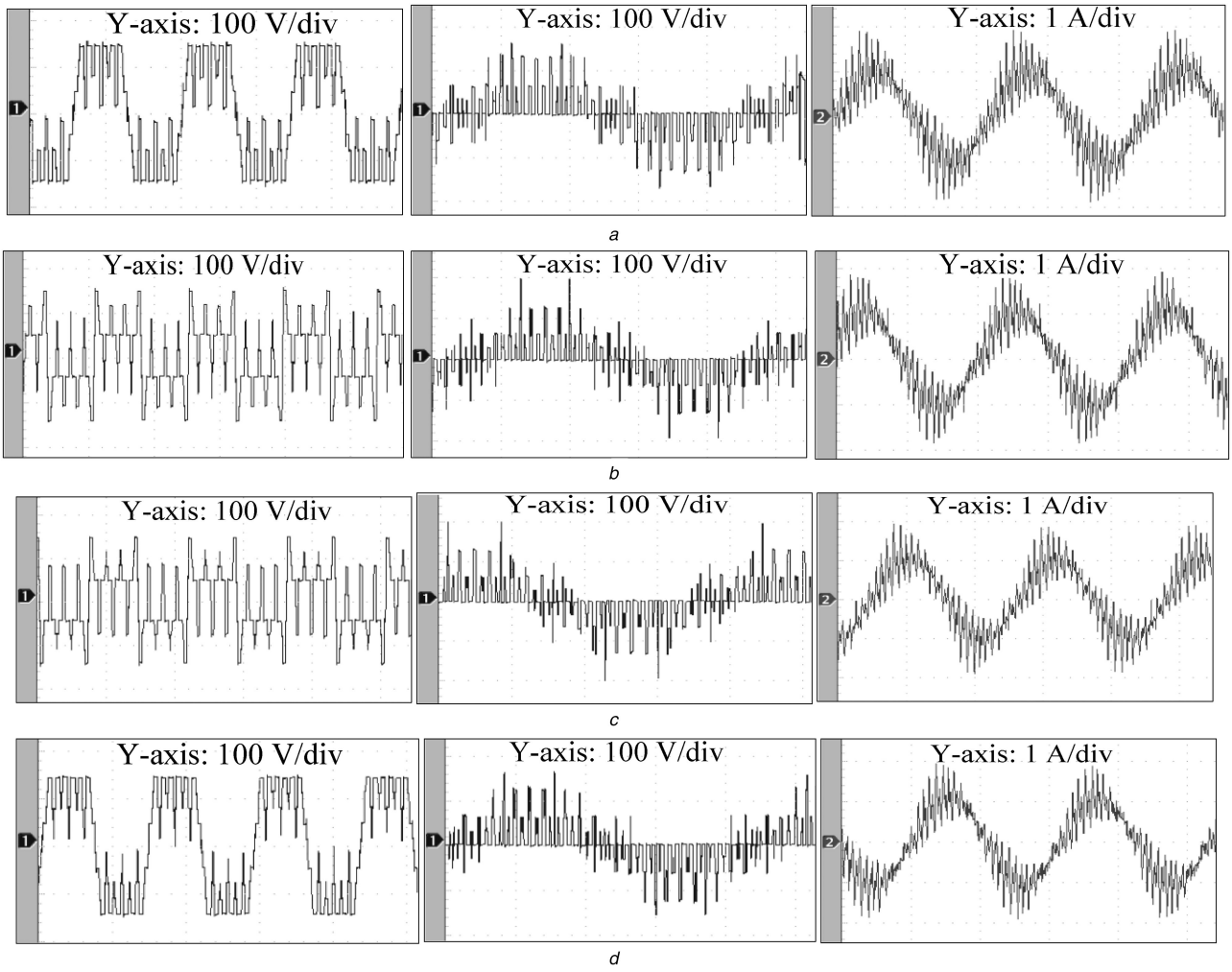

Fig. 6 *Experimental waveforms of common mode voltage (left), Phase-A voltage (middle) and current (right) for DDPWMs-1, 2, 3 and 4 at m_a = 0.2 (X-axis: 10 ms/div)*
(a) DDPWM-1,
(b) DDPWM-2,
(c) DDPWM-3,
(d) DDPWM-4

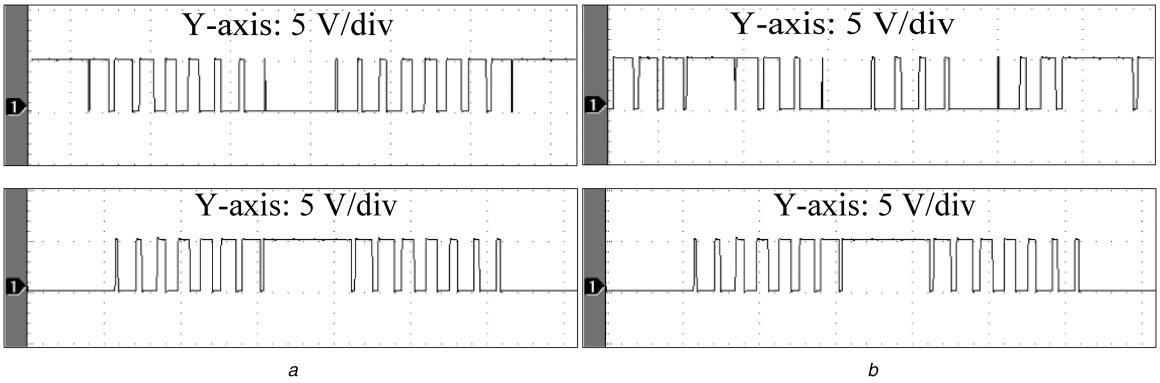

Fig. 7 *Experimental control signals for Phase-A of dual inverters at m_a = 0.7 (X-axis: 4 ms/div)*
(a) DDPWM-1,
(b) DDPWM-2

The top trace shows the typical turn-on current through a top-device (such as T_A^+ of inverter-1, Fig. 12*a*), which includes the diode reverse recovery current. The middle trace shows the voltage across it and the bottom trace shows the voltage across the bottom-diode (such as D_A^-, Fig. 12*a*).

The overall loss (i.e. the sum of the switching and the conduction loss) of the dual-inverter system is shown in Fig. 13*b*. The simulation results reveal that the proposed DDPWM techniques result in lesser overall loss compared to the decoupled SVPWM schemes. As reasoned out in the foregoing section, DDPWM-1 performs better amongst the four DDPWM techniques. The overall power loss increases linearly with the modulation index up to the limit of linear modulation (0.866), as the fundamental frequency depends on the modulation index (m_a) (9). Thus, the sampling time period decreases (or in other words, the switching frequency is increased) with the increase of the modulation index as the number of samples per cycle are fixed at

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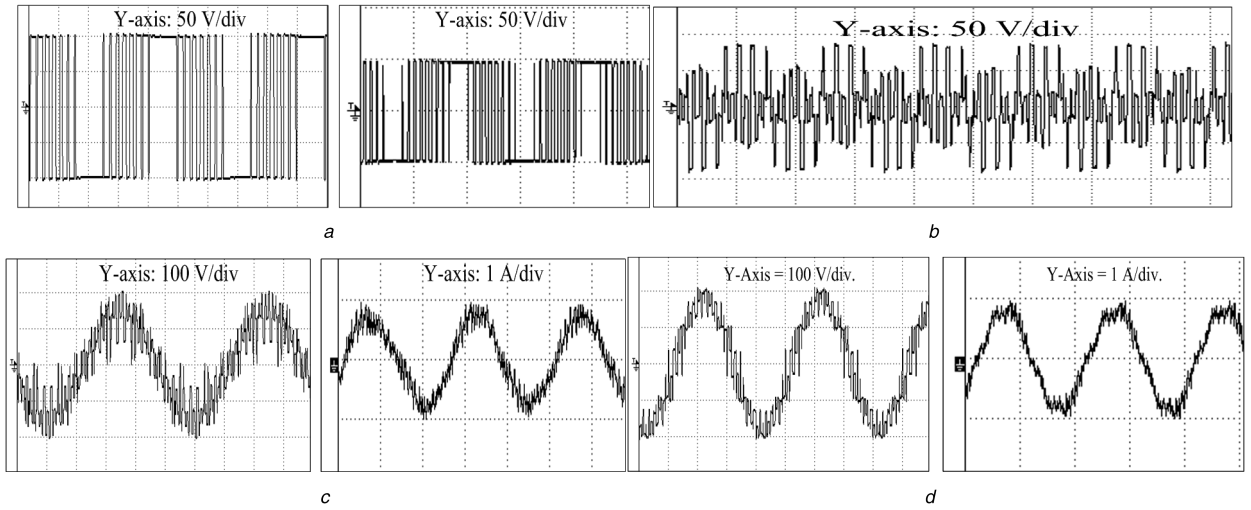

Fig. 8 *Experimental waveforms of pole voltages, common mode voltage, Phase-A voltage and current for DDPWM-1 (X-axis: 10 ms/div)*

(a) Pole voltages of inverter-1(left) and inverter-2 (right) at $m_a = 0.7$,

(b) Common mode voltage at $m_a = 0.7$,

(c) Phase-A voltage (left) and current (right) at $m_a = 0.7$,

(d) Phase-A voltage (left) and current (right) at $m_a = 1$

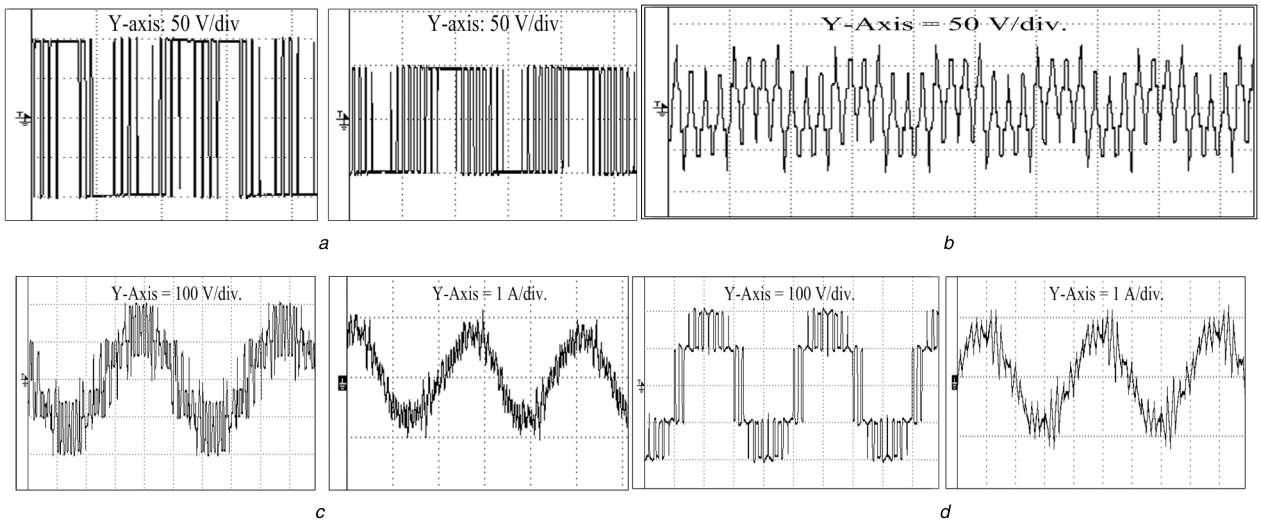

Fig. 9 *Experimental waveforms of pole voltages, common mode voltage, Phase-A voltage and current for DDPWM-2 (X-axis: 10 ms/div)*

(a) Pole voltage of inverter-1 (left) and inverter-2 (right) at $m_a = 0.7$,

(b) Common mode voltage at $m_a = 0.7$,

(c) Phase-A voltage (left) and current (right) at $m_a = 0.7$,

(d) Phase-A voltage (left) and current (right) at $m_a = 1$

42 per cycle. In the case of overmodulation (i.e. $m_a \geq 0.866$), the fundamental frequency is clamped to 50 Hz, which results in the decrease of switching loss. Consequently, the total power loss also decreases.

Fig. 13*c* shows the ohmic loss incurred in the motor with all the six PWM techniques. It is evident at the DC-link voltage of 300 V, all of the PWM schemes perform alike almost in the entire range of modulation.

The total loss of the OEWIMD, which is the sum of the overall dual-inverter loss (Fig. 13*b*) and the ohmic loss (Fig. 13*c*) in the motor, is presented in Fig. 13*d*. As one may expect, the total power loss in the drive is lower for the DDPWM-1 technique compared with the other PWM techniques. These simulations suggest that DDPWM-1 technique is suitable to realise an energy efficient four-level OEWIMD.

The THD is one of the most extensively used indices of performance, which quantifies the harmonic contamination in the output of inverter circuits. It is defined as

$$V_{\text{THD}} = \frac{\sqrt{\sum_{n=2}^{\infty} V_n^2}}{V_1} \tag{23}$$

In (23), V_1 and V_n, respectively, represent the fundamental component and n^{th} harmonic components of the RMS phase voltage. THD is a measure of the harmonic pollution in voltage, which is expressed in per unit or percentage, taking the fundamental quantity as the base value. The THD is evaluated for the motor phase voltage with all of the six SVPWM techniques, as a function of modulation. It is again seen that the PWM schemes proposed in this paper perform considerably better than the decoupled SVPWM techniques, as shown in Fig. 14*a*. Again, as one might expect, the DDPWM-1 scheme gives a better harmonic performance amongst the four DDPWM schemes.

However, in motor drive applications, it is more apt to quantify the harmonic distortion in the motor phase current rather than the motor phase voltage, as the primary interest is to draw currents which are as close to a sinusoid as possible. The THD in current (iTHD) is such a measure, which is expressed as

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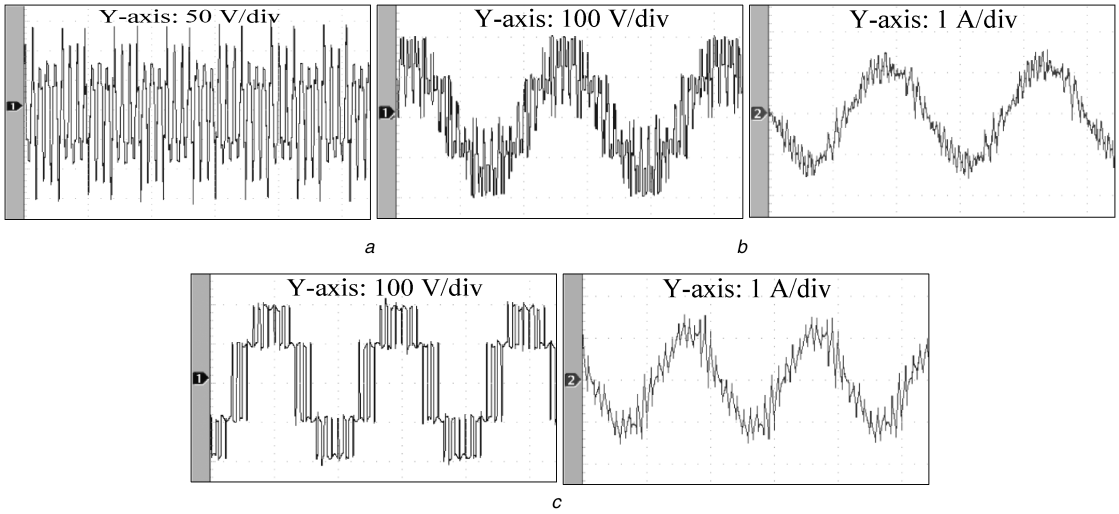

Fig. 10 *Experimental waveforms of common mode voltage, Phase-A voltage and current for DDPWM-3 (X-axis: 10 ms/div)*
(a) Common mode voltage at $m_a = 0.7$,
(b) Phase-A voltage (left) and current (right) at $m_a = 0.7$,
(c) Phase-A voltage (left) and current (right) at $m_a = 1$

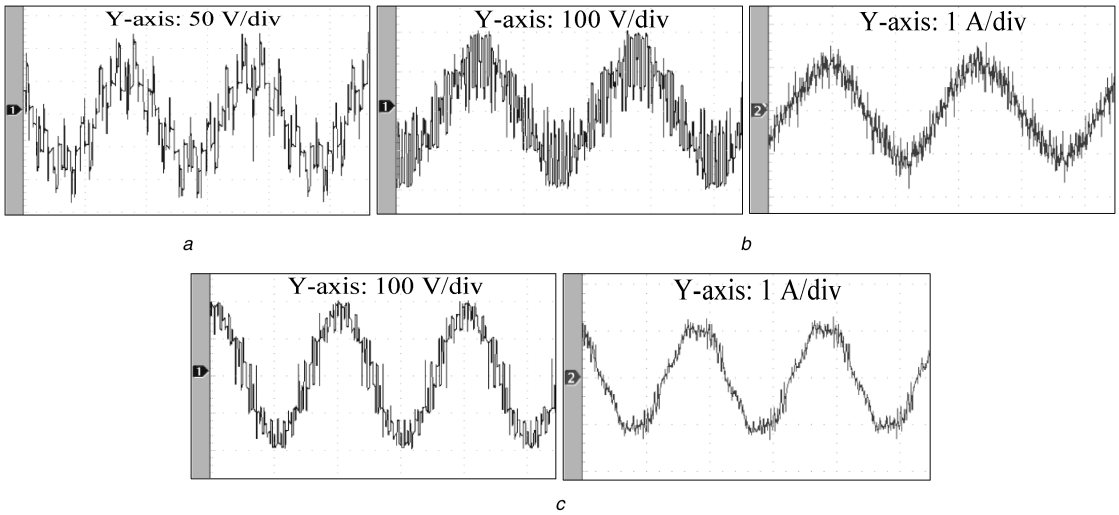

Fig. 11 *Experimental waveforms of common mode voltage, Phase-A voltage and current for DDPWM-4 (X-axis: 10 ms/div)*
(a) Common mode voltage at $m_a = 0.7$,
(b) Phase-A voltage (left) and current (right) at $m_a = 0.7$,
(c) Phase-A voltage (left) and current (right) at $m_a = 1$

$$i_{\mathrm{THD}} = \frac{\sqrt{\sum_{n=2}^{\infty} I_n^2}}{I_1} \tag{24}$$

When a sinusoidal voltage source feeds an induction motor, the motor draws only magnetising current at no-load. Neglecting the leakage inductance, which is often small compared to the magnetising inductance L_m, the no-load current is approximately equal to $(V_1/\omega L_m)$. However, when a non-sinusoidal source (such as a VSI) supplies the motor, any harmonic current component of n^{th} order is given by $(V_n/n\omega L_m)$. Thus, the RMS value of all harmonic components put together is given by $\sum_{n \neq 1}(V_n/n\omega L_m)^2$. Thus, the WTHD is given by

$$V_{\mathrm{WTHD}} \triangleq \frac{\sqrt{\sum_{n=2}^{\infty}\left(\frac{V_n}{n}\right)^2}}{V_1} \tag{25}$$

Fig. 14*b* shows that the WTHD with all of the six PWM schemes. From Fig. 14*b*, as per the expectation, the DDPWM-1 scheme performs better than the other SVPWM schemes.

The SLF is another performance indicator, which quantifies the normalised switching power loss incurred in an inverter [25]. It is defined as follows

$$\mathrm{SLF} \triangleq \frac{\Delta P_{\mathrm{SW}}}{m_{\mathrm{f}}} \tag{26}$$

In (26), P_{SW} and m_f, respectively, represent the switching energy lost in the dual-inverter topology per fundamental period and the frequency modulation ratio (the ratio of the carrier frequency and fundamental frequency) [22]. The frequency modulation ratio is determined by halving the sampling frequency for each value of the amplitude modulation ratio m_a. Equation (26) suggests that SLF can be used as a figure-of-merit for PWM schemes. For a given m_f, a lower SLF is obtained with a lower value of switching power loss (ΔP_{SW}). Thus, a lower SLF is indicative of a better harmonic performance for a given m_f.

From Fig. 14*c*, it is evident that the DDPWM techniques proposed in this paper exhibit lower *SLF*s in the entire range of modulation compared to the decoupled SVPWM technique. Amongst the decoupled SVPWM schemes, the PDPWM performs

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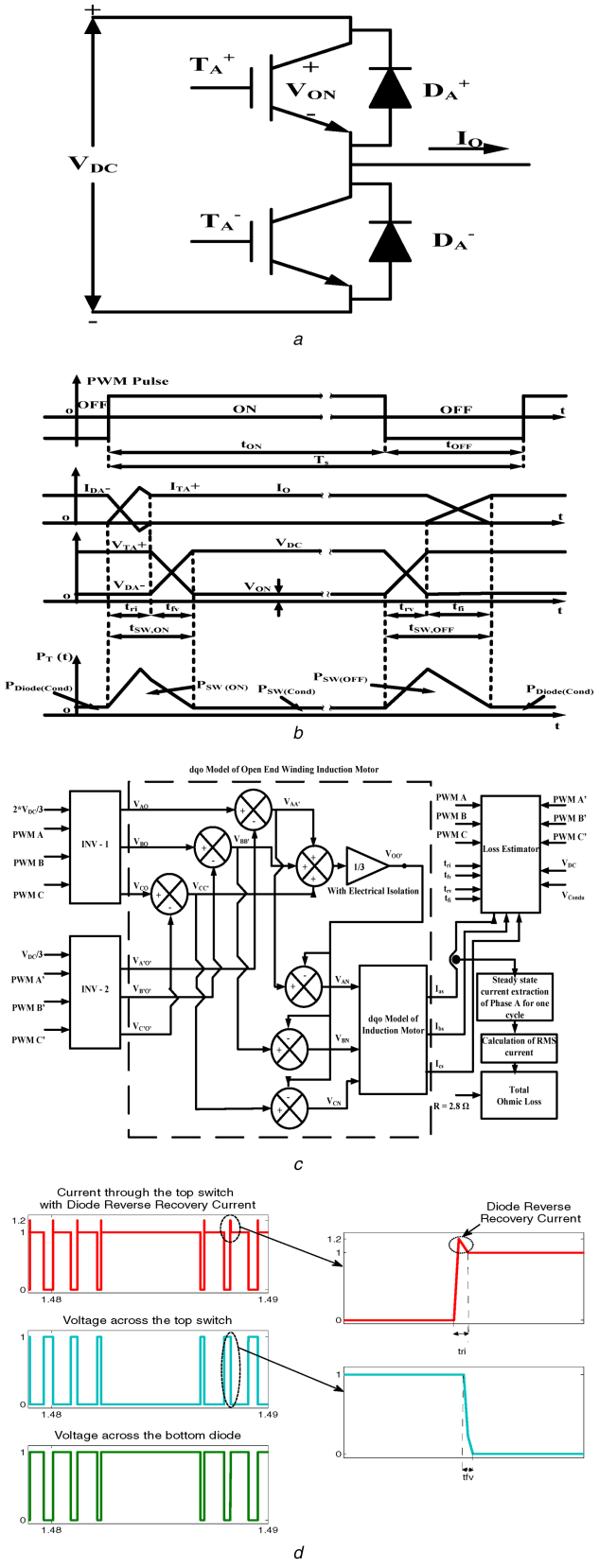

Fig. 12 *A-Phase leg, current through and voltage across the switching device and anti-parallel diode, loss model and simulated waveforms*

(a) One of the A-Phase leg of dual inverter topology,

(b) Current through and voltage across T_A^+, D_A^- with diode reverse recovery current,

(c) Improvised loss model for four-level OEWIMD,

(d) Simulated current and voltage waveforms of the top switching device with diode reverse recovery current and the bottom diode

better than the EDPWM as the switching power loss with the former is lesser than the latter by about 10% [16].

Reviewing all aspects and the graphical data presented in Figs. 13*b–d* and 14*a–c*, it is apparent that the DDPWM techniques perform better than the decoupled SVPWM techniques. The quantified values of the all the performance indices at a modulation index of 0.4 (inner region), 0.7 (middle region) and at 1 (outer region) (see Fig. 1*c*) are shown in Table 4.

It is fairly well known that application of PWM voltages with a large value of dv/dt is deleterious to the motor [26]. In this aspect, the DDPWM-1 scheme performs better compared to the decoupled SVPWM schemes. The magnified versions of the simulated motor phase voltage waveforms with the proposed DDPWMs and the decoupled SVPWM schemes are shown in Fig. 14*d*. It may be noted that the voltage pulses appearing across the motor phase windings with the DDPWM-1 scheme show lower levels of transition compared to the centre-spaced decoupled SVPWM schemes [15, 16]. This indicates that the motor phase windings are subject lower dv/dt with the proposed DDPWM schemes (Fig. 14*d*).

6 Conclusion

In this paper, the application of DDPWM schemes for a four-level OEWIMD is investigated. Though the application of DDPWM (also called phase clamped PWM) is very well known for the conventional two-level inverters, its application for a four-level OEWIMD is not reported in the literature in the case of decoupled SVPWM with equal duty. Application of DDPWM schemes poses problems owing to the fact that the power circuit configuration is not symmetrical. It is difficult to derive waveform symmetries from an unsymmetrical power circuit using an unsymmetrical (i.e. non-centre spaced) decoupled PWM scheme.

Simulation studies reveal that, of the several possibilities of placing the effective time period at the edge of sampling time interval, only four succeed in resulting all the three symmetries namely, the quarter-wave, the half-wave and the three-phase symmetries. These four possibilities are named as DDPWM-1, DDPWM-2, DDPEM-3 and DDPWM-4. Simulations, as well as experimental studies, reveal that DDPWM-1 performs better than DDPWMs-2, 3, and 4. Apart from obtaining waveform symmetries, the proposed DDPWM schemes also ensure that the DC-link capacitor of the inverter operating with lower DC-link voltage is not overcharged by its high voltage counterpart, which is a nagging problem in the unsymmetrical four-level OEWIMD.

Further, the relative performances of these PWM schemes are investigated by comparing them with the decoupled centre-spaced SVPWM schemes reported in the earlier literature, namely, the EDPWM and the PDPWM schemes. To this end, an improvised loss model is developed, which computes the RMS value of the motor phase current, taking the ripple content into consideration. This model also accounts for the conduction losses incurred in the anti-parallel diodes and the additional power loss due to the reverse recovery current of the diodes.

A comparative study is undertaken covering various aspects such as total losses in the dual-inverter system, ohmic loss in the motor, overall losses in the OEWIMD, THD, WTHD and SLF are considered for the sake of comparison. Simulation results reveal that DDPWM schemes perform better than the EDPWM and the PDPWM schemes in all of the above aspects.

Additionally, the DDPWM schemes result in considerably lower dv/dt across the power semiconductor devices when compared to the decoupled centre-spaced SVPWM schemes, resulting in longevity of bearings and winding insulation.

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Table 3 OEWIMD Parameters

Name of the parameter	Value
R_s	4.215 Ω
$R_{r'}$	4.185 Ω
$x_{ls} = x_{lr'}$	5.502 Ω
X_m	162.3 Ω
J	0.0131 kg m^2
B	0.002985 N m s
P	4

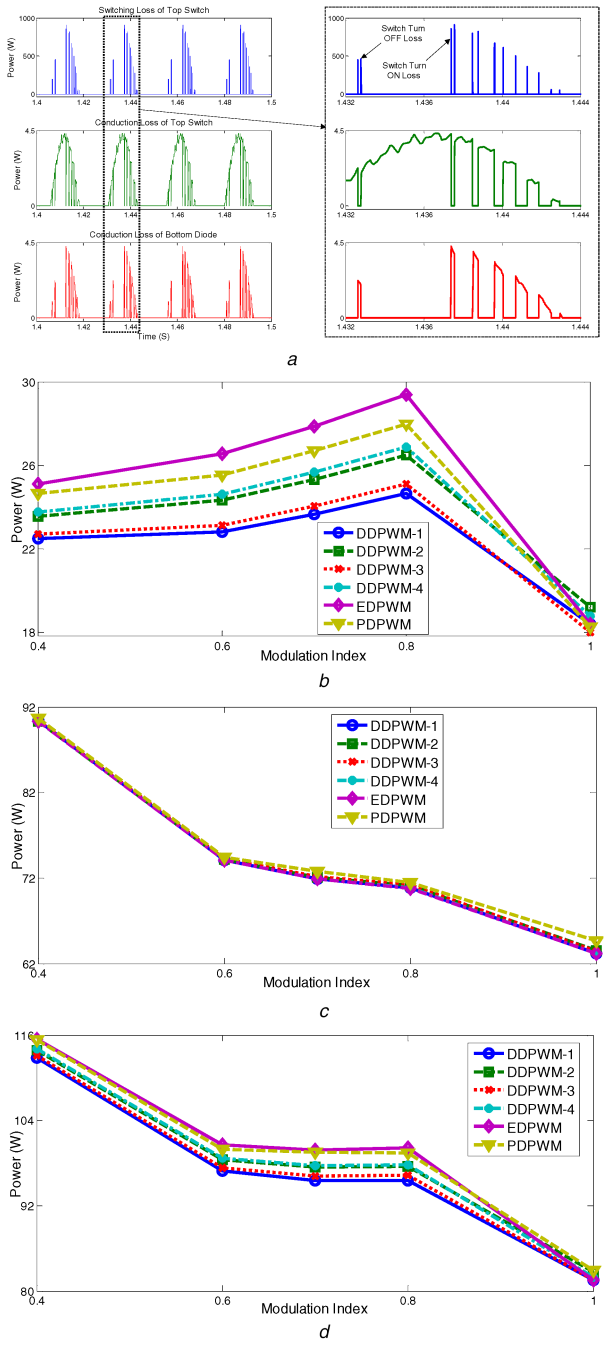

Fig. 13 *Simulated waveforms of top switch and bottom diode, dual inverter loss, ohmic loss and total loss of four-level OEWIMD*

(a) Simulated loss waveforms of top switching device and bottom anti-parallel diode with zoomed portion, ***(b)*** Overall Dual inverter loss, ***(c)*** Ohmic loss, ***(d)*** Total drive loss

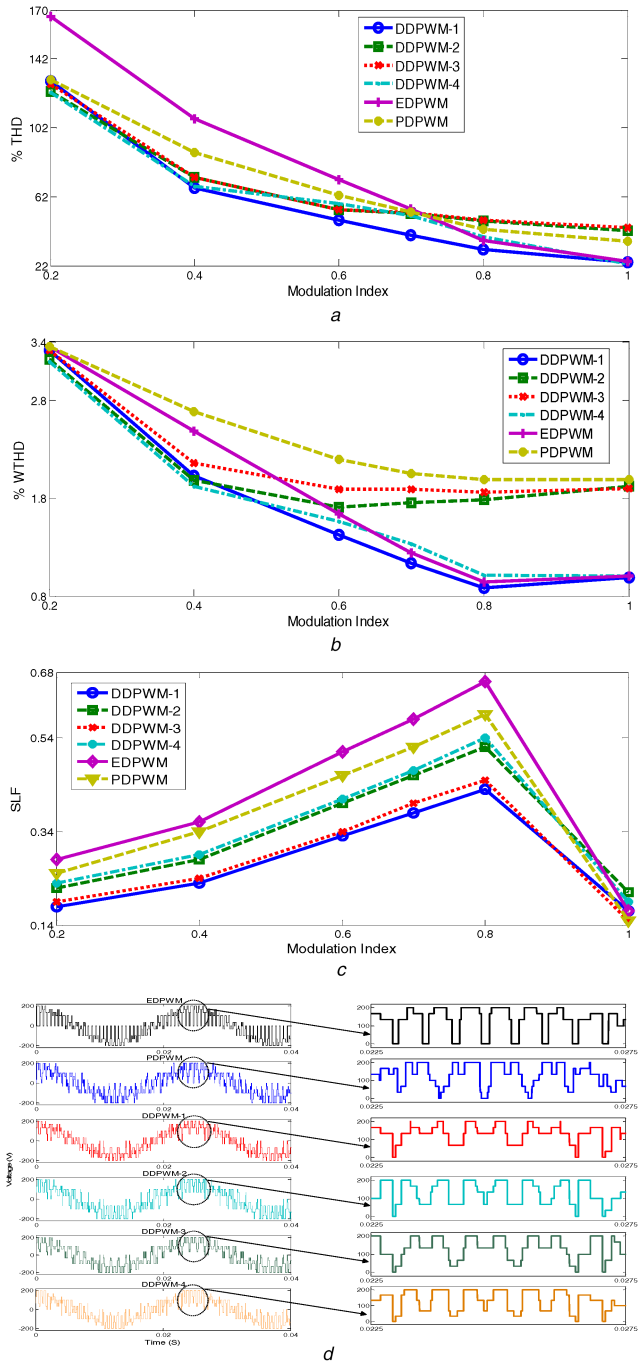

Fig. 14 *THD, WTHD, SLF and dv/dt comparison of six SVPWM techniques for four-level OEWIMD*

(a) THD, ***(b)*** WTHD, ***(c)*** SLF, ***(d)*** Voltage pulses appearing across the motor winding with the EDPWM (top), PDPWM scheme (second), DDPWM-1 (third) DDPMW-2 (fourth), DDPWM-3 (fifth) and the DDPWM-4 (bottom) techniques

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Table 4 Quantified values of the performance indices

Modulation index (m_a)	Name of the performance indices						Name of the PWM
	Total dual inverter losses, (W)	Ohmic losses, (W)	Total drive losses, (W)	%THD	%WTHD	SLF	
0.4	22.50	90.37	112.86	67.17	2.03	0.23	DDPWM-1
	23.57	90.32	113.89	73.34	1.98	0.28	DDPWM-2
	22.70	90.41	113.11	73.34	2.16	0.24	DDPWM-3
	23.78	90.28	114.06	67.74	1.92	0.29	DDPWM-4
	25.12	90.27	115.39	106.99	2.49	0.36	EDPWM
	24.68	90.64	115.32	87.19	2.67	0.34	PDPWM
0.7	23.66	71.90	95.56	39.52	1.13	0.38	DDPWM-1
	25.34	72.08	97.42	52.17	1.75	0.46	DDPWM-2
	24.06	72.14	96.20	52.83	1.89	0.40	DDPWM-3
	25.69	71.93	97.62	51.03	1.33	0.47	DDPWM-4
	27.90	71.92	99.82	54.77	1.24	0.58	EDPWM
	26.72	72.80	99.52	53.30	1.96	0.52	PDPWM
1	18.39	63.17	81.55	24.17	0.99	0.17	DDPWM-1
	19.21	63.50	82.71	42.16	1.92	0.21	DDPWM-2
	18.01	63.46	81.47	43.79	1.90	0.15	DDPWM-3
	18.78	63.17	81.96	23.17	1.00	0.19	DDPWM-4
	18.39	63.17	81.55	24.17	0.99	0.17	EDPWM
	18.26	64.62	82.89	36.19	1.91	0.15	PDPWM

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