A Single-Phase Quasi-Z-Source based Seven-Level Inverter with Capacitor Voltage Balancing

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***Abstract*—In this paper a Quasi-Z-source based seven level inverter is proposed. The output capacitor of the quasi-Z-source network is split into four parts to generate the levels with minimum number of switches. A switch sharing based auxiliary circuit with proportional-integral (PI) controller is used to balance the capacitor voltages. Simulation of the proposed inverter is performed in MATLAB SIMULINK environment for R load and the simulation results show that the auxiliary circuit can balance the proposed Quasi-Z-source based seven level inverter and the simulation results are presented.**

***Index Terms*—Quasi-Z-source, Proportional-integral (PI) controller, Switch sharing, capacitor voltage balancing.**

I. Introduction

Z-source inverters are the emerging topologies in the area of power electronics ever since proposed by F.Z. Peng[1] in 2002. They became popular due to their added advantages over traditional voltage source and current source inverters. The limitations such as limited output voltage, dead band requirement problems and reliability concerns can be overcome by the help of these Z-source inverters. They have the added advantage in the form of shoot through duty pulse which can boost the output voltage to the required level. Moreover they help in single stage power conversion and hence the efficiency can be improved compared to traditional two stage power conversion processes. The Quasi-Z-source network is derived from the existing Z-source network which is published in [1]-[2].

Now a day's multilevel inverters are having a wide range of applications due there immense advantages. They improve the power quality by performing the power conversion in small voltage steps and hence the harmonics are also greatly reduced [3]-[4]. The peak output voltage of traditional multilevel inverters is same as the input voltage. This can be overcome by the use of Quasi-Z-source network. The qZSI provides single stage power conversion along with the boosting option. Moreover the input current of qZSI is continuous. The Quasi-Z-source inverters are integrated with the traditional multilevel inverters[5]-[7] to get voltage boosting capability. The output voltage boost can be controlled with the help of shoot through duty ratio Do. A single phase three level neutral point clamped quasi-Z-source inverter is proposed in [8] which provides advantages such as short-circuit withstand capability and boosted output voltage. Generally the qZSI network is interfaced to other multilevel inverter networks; but in the proposed paper the capacitors of qZSI network itself is used for level generation. This paper proposes the integration of quasi with seven-level inverter with reduced switch count[10] and capacitor voltage balancing[11].

Switch-sharing based multilevel inverter has there own advantages such as smaller filter size compared to there counter parts especially for renewable energy applications. The main problem in switch sharing based inverters is proper division of voltage across each capacitor. If the proper division is not happened then there will be a problem in the output waveform as the levels may get disturbed. Hence in-order to avoid this problem there are two methods proposed to balance the capacitor voltages in flying capacitor based inverters. By adjusting the switching logic[9] such that based on the voltage level of the capacitor the proper switching states must be applied in-order to charge or discharge the capacitor whichever is needed. But this involves higher control complexity and this can be done at only lower modulation indexes. The other method is by using an auxiliary circuit [11]. This is used whenever there is no possibility of any redundant states which is the case in this paper. In this method the main advantage is the voltage balance is proper and there is no effect on the output voltage. Hence a satisfactory operation is obtained.

An auxiliary circuit based balancing technique is used for the proposed inverter for capacitor voltage balance with the help of PI controller. In this paper a Quasi-Z-source based inverter is implemented which offers higher boosting ability with minimum number of components required for the general seven level operation[10]. The boosting is controlled with the shoot through duty ratio D_o. The paper flow will be as follows: In section II the operation of the proposed topology along with the PWM technique is explained, followed by auxiliary circuit in section III and then the simulation results are shown in section IV, conclusions in section V followed by references.

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II. Description and Operation of the Proposed Topology

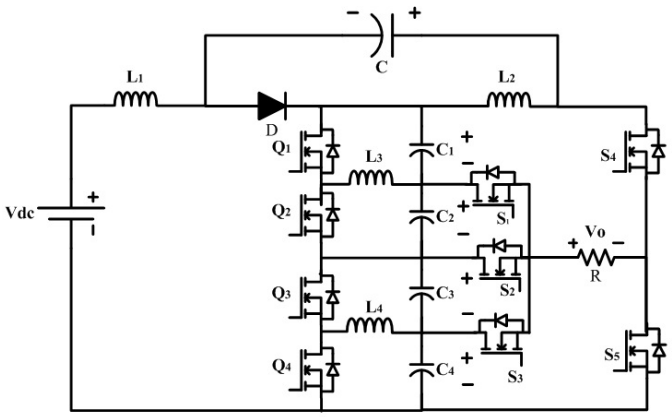


Fig. 1. Proposed Seven-Level Inverter

A. Quasi-Z-source Network

Fig. (1) shows the proposed topology of the seven-level inverter. The switches S_1-S_5 are used for the level generation and the switches Q_1-Q_4 are part of the auxiliary circuit which is explained in detail in the further sections. The proposed circuit shows a Quasi-Z-source network. qZSI has two inductors (L_1 and L_2) and two capacitors (C and combination of C_1-C_4). The other capacitance in the qZSI network is split in to four capacitances of equal value and thereby they are used for the level generation. The parameters of Quasi-Z-Source network are chosen according to [2] and output voltage and boost factors are calculated form equations (1)- (4). Quasi-Z-Source Inverter has high reliability due to the shoot through withstanding capability and low inrush current during starting. The shoot through duty ratio T_{sh} is controlled to increase the boost factor. From [2] we get,

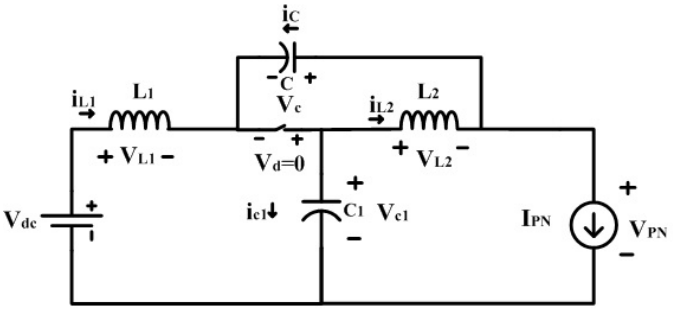


Fig. 2. Non-Shoot through state

$$V_o = \frac{V_{dc}}{1-2D_o} = B \times V_{dc} \tag{1}$$

$$B = \frac{1}{1-2D_o} \tag{2}$$

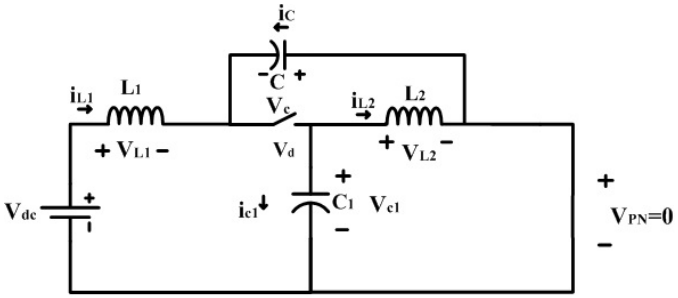


Fig. 3. Shoot through sate

$$Do = \frac{T_{sh}}{T} \tag{3}$$

$$M = 1 - D_o \tag{4}$$

By controlling the shoot through duty ratio D_o the output voltage can be controlled. The Shoot through duty ratio can be controlled by the modulation index M which is the ratio of magnitude of sinusoidal reference to carrier reference. The operation of the circuit during shoot through mode and non-shoot through mode are shown in Fig. (2) and Fig. (3).

B. Modulation Technique

The switches S_1-S_5 are used for the level generation. A level shifted sine PWM modulation technique is used for the proposed inverter as shown in the Fig.(4). Since the inverter is for seven levels hence six carrier waveforms are compared with a sinusoidal reference signal. The switching table is shown in Table I hence the switching sequence is followed to get the desired output. The shoot through is done by the help

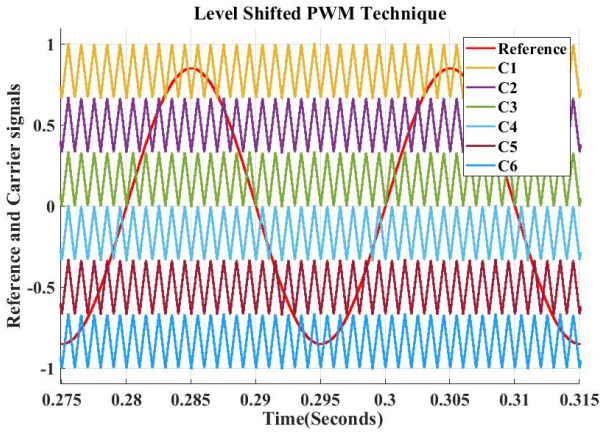


Fig. 4. Level Shifted PWM Technique for Seven-Level Inverter

of switches S_1 and S_5. To implement shoot through a simple boost control technique is used as shown in the Fig. (5) where two constant signals of magnitude less than or equal to the magnitude of the reference voltage is taken and compared with the carrier signal to generate the shoot through pulses which

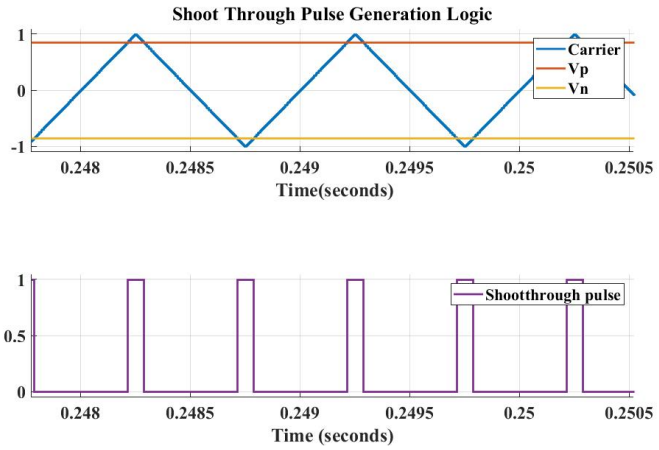


Fig. 5. Shoot through Pulse Generation Logic using Simple Boost Method

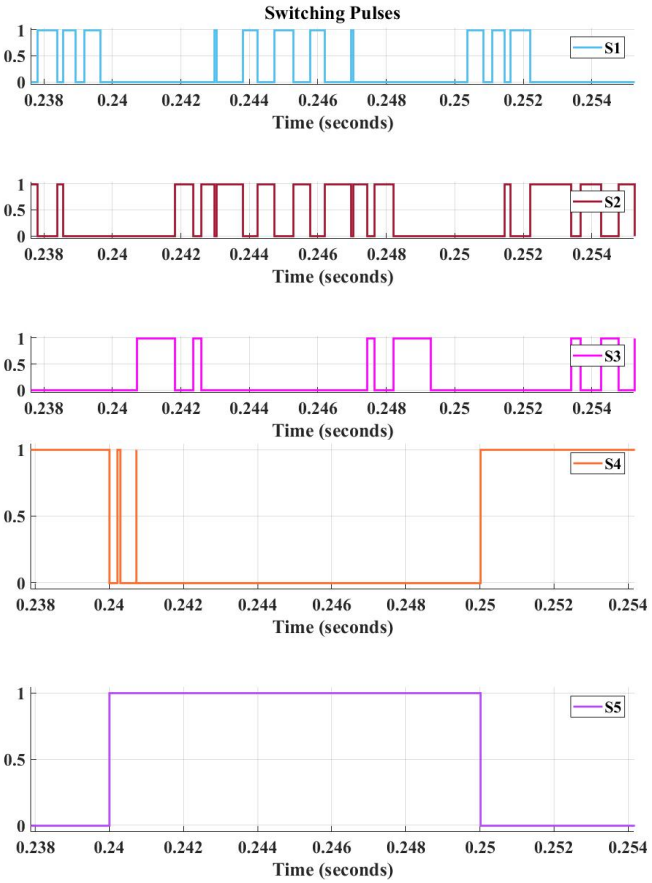


Fig. 6. Gate Pulses for switches S1-S5

are given to the switched S_4 and S_5. They are shorted for a small duration during which the output voltage is Zero and the switches S_1-S_3 are in OFF state. Hence the shoot through duty interval is calculated and the value is obtained as T_{sh}=1.7ms. The shoot through is inserted only when the output voltage is zero and the shoot through duty ratio value is obtained as D_o=0.15. During the process of level generation the capacitor voltages must be balanced, this is taken care by the auxiliary circuit which is explained in the next section. Without the boosting network i.e., qZSI network if input voltage is V_{dc} then each capacitor is maintained at a voltage of $\frac{V_{dc}}{4}$. But due to the presence of the boosting network for the same input voltage of V_{dc} each capacitor is maintained at a voltage of V_{dc} only. This is achieved with the help of proper shoot through for qZSI network. The simulation is done for V_{dc}=100 Volts and each capacitor voltage is maintained at 100 Volts and the DC link voltage V_{dc_link} is maintained at 400 Volts. The output peak voltage is boosted to 300 Volts with the help of Quasi-Z-source network. The switching pulses for the level generation switches S_1-S_5 are shown in the Fig. (6) and that of the auxiliary circuit switches Q_1-Q_4 are shown in Fig. (7).

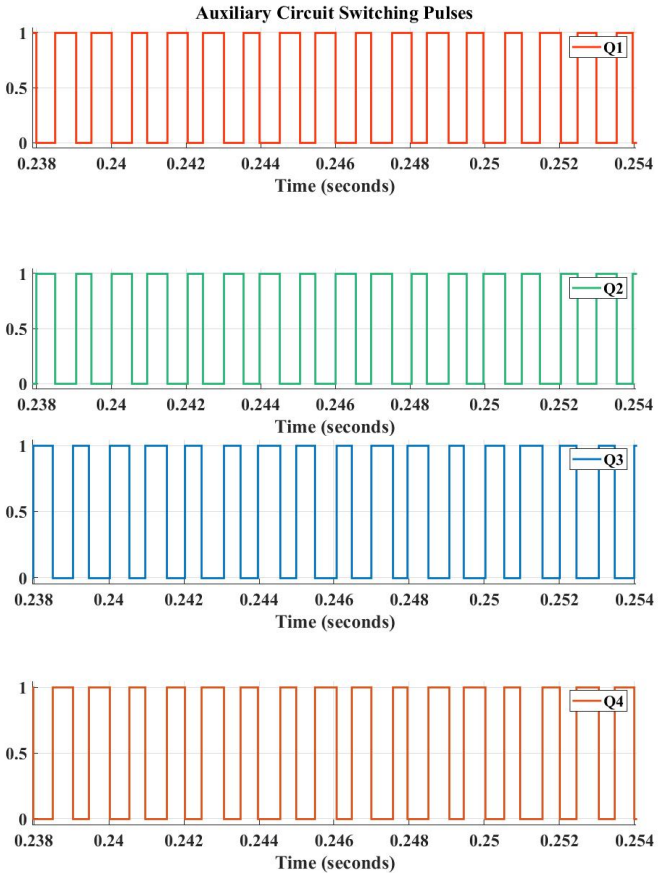


Fig. 7. Gate Pulses for Switches Q1-Q4

TABLE I
SWITCHING TABLE

S1	S2	S3	S4	S5	Vo
0	0	1	0	1	Vdc
0	1	0	0	1	2Vdc
1	0	0	0	1	3Vdc
0	0	0	0	0	0
1	0	0	1	0	-Vdc
0	1	0	1	0	-2Vdc
0	0	1	1	0	-3Vdc

III. Auxiliary Circuit

A. Auxiliary Circuit Operation

Fig. (8) shows the auxiliary circuit for the proposed configuration. It is a buck-boost chopper [11]-[12] consists of two inductors (L_3 and L_4) and four power switches (Q_1-Q_4) which will be used to balance the four capacitors (C_1-C_4). There are two separate PI controllers used for the balancing purpose as shown in Fig. (9). One is for the top two capacitors (C_1,C_2) and the other is for the bottom two capacitors (C_3,C_4). The switches Q_1 and Q_2 are complementary to each other and same is the case with Q_3 and Q_4. When ever the output of PI controller is less than the carrier signal switch Q_1 is turned off and hence Q_2 will be ON. C_1 and C_2 starts charging and discharging depending on the switching signals of Q_1 and Q_2. One of the case is shown in the Fig. (8) which shows the operation of the auxiliary circuit when Q_2 and Q_3 are ON.

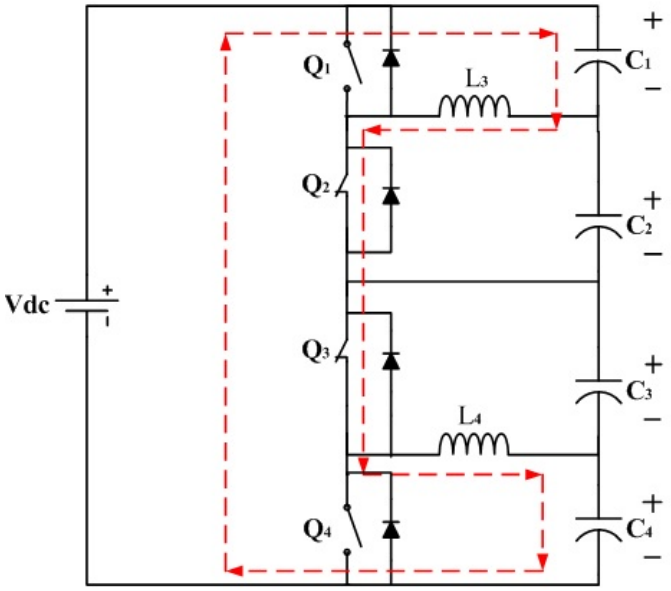


Fig. 8. Capacitor Voltage Balancing Circuit

B. Closed Loop Control Operation for Capacitor Voltage Balancing

Two PI controllers are used for balancing four capacitor voltages at its reference value [11]-[12].The block diagram of the PI control technique is shown in the Fig. (9).There are two error signals generated due to two PI controllers and by properly tuning the values of the proportional gain(K_p) and Integral gain(K_i) and comparing the output of PI controllers with the reference carrier wave suitable pulses are generated to switches Q_1-Q_4 and the error is minimized hence the capacitor voltages are always balanced to its reference value of 100 Volts as shown in Fig. (10).

$$e_1(t) = V_1 - V_2 \tag{5}$$

$$e_2(t) = V_4 - V_3 \tag{6}$$

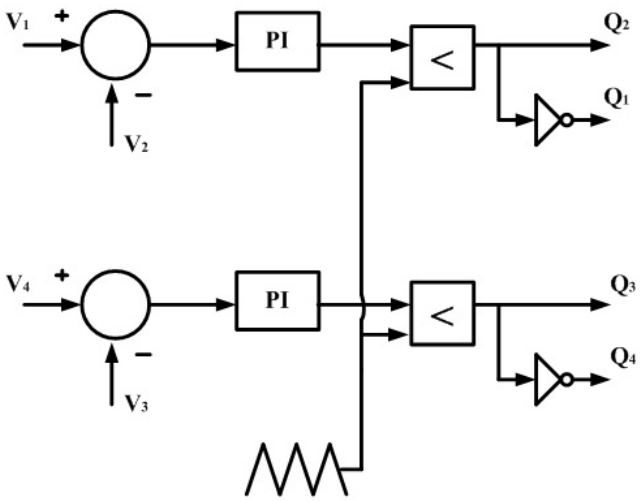


Fig. 9. PI Controller Implementation

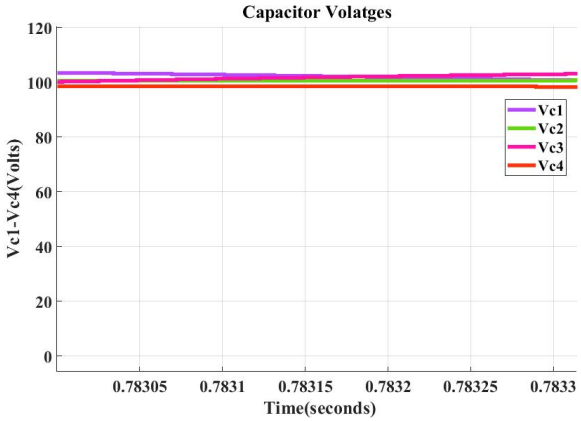


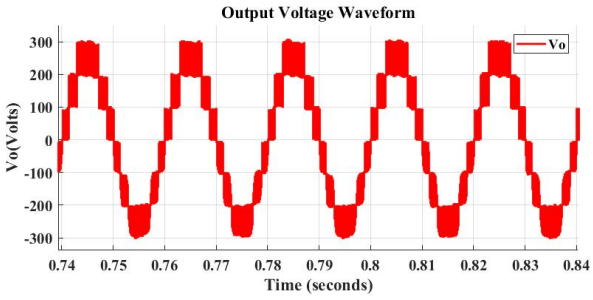
Fig. 10. Capacitor Voltages V_{c1}-V_{c4}

$$y(t) = K_p \times e(t) + \frac{K_i}{s} \times e(t) \tag{7}$$

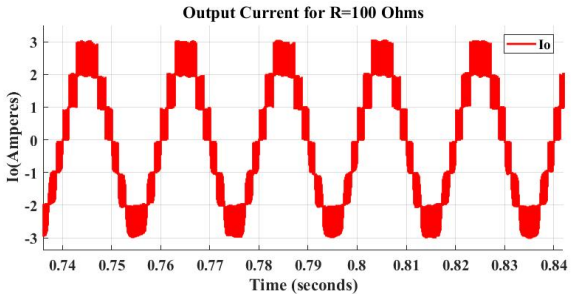
The signals y(t) obtained in equation (7) is compared with the reference carrier signals to generate the gate pulses for the switches Q_1-Q_4 which are shown in the Figure.

IV. Simulation

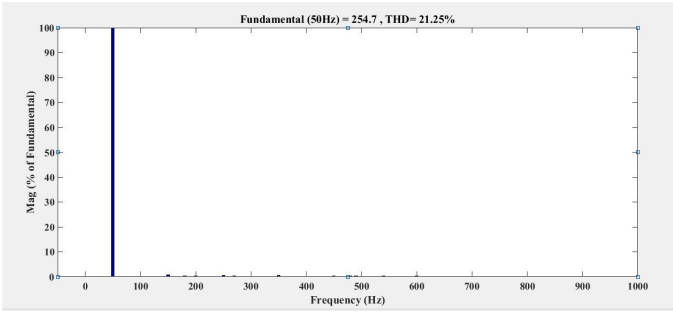
In-order to verify the working of the proposed configuration a simulation is carried out in the MATLAB SIMULINK environment. The inverter is supplying an R-Load of 100 Ohms and the parameters of the Quasi-Z-source network are chosen as L_1=L_2=1.5mH and C=500uF and the capacitances C_1=C_2=C_3=C_4=2200uF. The parameters of the auxiliary circuit inductors are L_3=L_4=3mH. The PI controller is designed for the values K_p=1 and K_i=0.01 for both the controllers. The switching frequency is taken as f_{sw}=10KHz and the modulation index of the reference sinusoidal waveform is chosen as M=0.85. For the input of V_{dc}=100 Volts the simulation results are shown in the Fig. (11) which shows that the Quasi-Z-source network is used to generate the required seven levels



(a)



(b)



(c)

Fig. 11. Simulation results for M=0.85(a)Seven-level output voltage waveform, (b)Output current waveform for R=100 Ohms, (c)FFT analysis of output voltage waveform

TABLE II
VOLTAGE STRESS ACROSS SWITCHES

S1,S2,S3	S4,S5	Q1,Q2,Q3 and Q4
V_{dc} Volts	$1.5\times V_{dc} Volts$	$0.5\times V_{dc} Volts$

with boosting up the output peak voltage to 300 Volts, the capacitor voltages are balanced at 100 Volts as shown in the Fig. 11(b), the output current waveform and THD analysis of the output voltage is shown in the Fig. 11(c) and Fig. 11(a) respectively. The voltage stresses across the switches is shown in Table II. The current stress across the switches is same as the peak output load current I_{o_peak} which is 3 Amps in the present case. The results shows that the proposed topology is having a THD in the output voltage waveform as 21.25%. And it is true that as modulation index increases THD of the voltage waveform decreases. Hence the inverter is operated at high modulation index in this case it is 0.85. Hence the proposed configuration is working properly and the desired results are obtained which are verified through the MATLAB Simulation.

V. CONCLUSIONS

This paper presents a single-phase Quasi-Z-source based seven-level inverter with capacitor voltage balancing with the help of buck-boost based chopper circuit. The PI controllers used for generating the gate pulses for auxiliary circuit and a level shifted Sine PWM technique is used with only five switches for seven-level generation and four switches for the auxiliary circuit. The SIMULINK model is developed in the MATLAB environment and the results shows the satisfactory operation of the proposed inverter. It is planned for the experimental setup in the near future to validate the simulation results. The proposed configuration can be used for the renewable energy applications where the input voltage is very low which can be boosted with the help of Quasi-Z-Source network.

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