A Novel Hybrid Quasi Z-Source Based T-Type Seven-Level Inverter

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***Abstract*—This paper presents a new structure of Hybrid Quasi Z-source based T-type seven-level inverter for renewable applications. The proposed topology comprises of three quasi Z-source based impedance networks cascaded with a T-type seven-level inverter structure consisting of H-bridge and bidirectional switches. The bidirectional switches operate at high frequency and are utilized for level generation. Only two switches in the H-bridge are utilized for shoot-through insertion, while the other two switches operate at the fundamental frequency. The proposed switching scheme along with the different operating modes are addressed for each level generation and the simulation is carried out in Matlab software to verify the performance. An experimental setup is also developed to validate the simulation results. Further, the merits of the proposed topology are highlighted with the comparison of recently proposed topologies.**

***Keywords*—Quasi Z-source, shoot-through, switching scheme, power quality.**

I. INTRODUCTION

Recent advancements in Z-Source based converters have led to tremendous growth in its usage among various power electronic applications[1]. The Z-source Inverter alleviates the issues of limited output voltage, reliability associated with conventional Voltage Source and Current Source Inverters[2]. The dead band between the switches is eliminated which reduces the waveform distortion and enhances reliability. It enables dc-ac power conversion in a single-stage with buck-boost capability which improves the efficiency when compared to a two-stage conversion system. The output voltage is boosted to a value based on the shoot-through duty cycle D_0. The shoot-through is obtained by turning on the switches of a phase or all the phases for a duration equal to D_0T. Several shoot-through control techniques are reported in literature[3].

Quasi Z-source inverter (qZs) [4] inherits the features of Z-source inverter and in addition provides continuous input current, reduced capacitor C_2 size and common dc-rail between source and load making them suitable for the distributed generation[5]. On the other hand, multilevel inverter (MLI) offers improved quality of output voltage and current with reduced THD. It enables the use of fast semiconductor switches with low voltage stress, which leads to reduced switching losses and increased reliability[6]. Integration of Z-source based network with MLI is becoming popular due to its combined features of an increased output voltage with better quality, short circuit immunity, reduced voltage stress and enhanced reliability. However, shoot-through must be inserted properly such that the average output voltage remains unchanged. In this context, several topologies are reported based on the combinations of Quasi–Z source network with popular Neutral Point Clamped (NPC), Cascaded H-bridge (CHB) based MLI. A 3L-NPC based on double qZs networks is presented in [7]. A qZs-based CHB for seven-level operation is reported in [8] for PV based distributed generation. A qZs based cascaded seven-level inverter with reduced switch count is presented in [9]. However, the above topologies demand more component count for increased voltage levels, thus increasing the size and cost of the system.

Therefore, in this paper, a two-input qZs based five-level inverter reported in[10] is considered for the study. The lack of shoot-through control and modularity feature motivates the authors to develop the proposed T-type seven-level inverter structure cascaded with quasi Z-source networks for multi-string PV applications. The Table I also demonstrates the merit of the proposed topology in terms of reduced device count and modularity. Therefore, the detailed working operation along with the proposed switching scheme based on Level-shifted Pulse width modulation technique is presented. Simulation work is carried out in Matlab software to show the seven-level output voltage waveform and the experimental results are also presented to validate the results.

TABLE I
COMPARISON WITH OTHER EXISTING TOPOLOGIES

	CHB-qZSI [8]	Cascaded qZSI [9]	Proposed Topology
Inductors	6	6	6
Capacitors	6	6	6
Diodes	3	3	3
Switches	12	10	8
Total Blocking Voltage	12 V_{DC}	18 V_{DC}	18 V_{DC}
Switches for shoot-through	6	3	2

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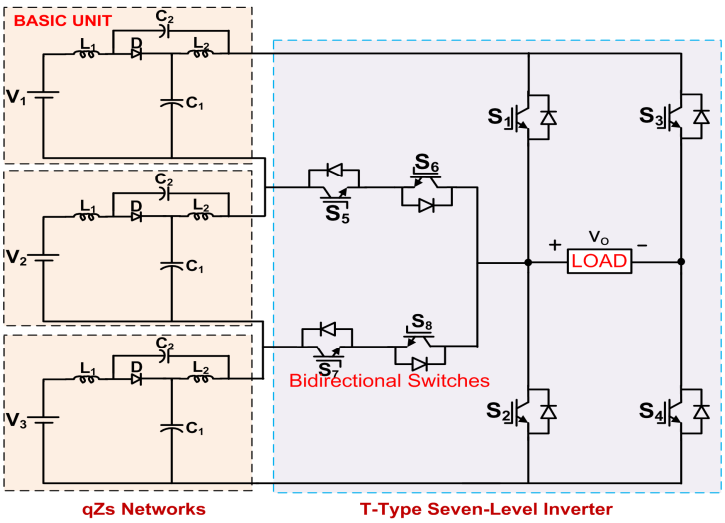

Fig. 1. Proposed hybrid quasi Z-source based T-type seven-level inverter.

II. Configuration of the Proposed Topology

Fig. 1 shows the configuration of the proposed topology which comprises of three qZs based impedance networks cascaded with a T-type seven-level inverter [11] consisting of H-bridge inverter through two units of bidirectional switches. Each qZs based impedance network acts as a basic unit which typically consists of two inductors L_1, L_2 and two capacitors C_1, C_2. The switches S_1 and S_2 operate at high frequency and are utilized for shoot-through insertion for each impedance network. The switches S_3 and S_4 operate at line frequency. The two units of bidirectional switches (S_5, S_6) and (S_7, S_8) acts as an intermediate link and used for voltage level generation. It requires three isolated dc-sources which can be identical or different. The peak dc-link voltage needs to be maintained constant for all the qZs networks in case of different input voltages for obtaining symmetrical seven-level output. The number of basic units determines the number of output voltage levels.

If n is the number of basic units, then the number of output voltage levels can be represented as

$$N=2n+1 \quad (1)$$

Similarly, the number of switches required for realizing the required number of levels can be represented as

$$S=2(n+1) \quad (2)$$

This shows the modularity of the proposed structure.

III. Switching Scheme

The switching states corresponding to each voltage level is shown in Table II. A simple Level Shifted pulse width modulation (LSPWM) technique is employed for the generation of control pulses. A reference sine wave of amplitude M is compared with six carrier triangular waveforms as shown in Fig.2. The switching algorithm for generating the control pulses is shown in Fig. 3. A simple boost control method is used for proper insertion of shoot-through. The shoot-through pulse D_{ST} is generated by comparing the upper carrier wave C_1 and lower carrier wave $C_6$with a control variable ST, where $ST \geq M$. The equivalent shoot-through pulse D_{ST} is inserted to the switches $S_1$and S_2. The different modes of operation and their corresponding output level generation are illustrated in Fig. 4. It can be observed that switch S_4 conducts for entire positive half cycle. Similarly, switch S_3 conducts for the entire negative half cycle; also only two switches are in conduction for any voltage level. But the limitation of the proposed switching algorithm is that, independent control of each qZs network is not possible as a common shoot-through pulse is applied to all the qZs networks.

TABLE II
SWITCHING STATES AND CORRESPONDING OUTPUT VOLTAGE LEVELS

S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	V_o
0	0	0	1	0	0	1	0	V_{dc}
0	0	0	1	1	0	1	0	$2V_{dc}$
1	0	0	1	0	0	1	0	$3V_{dc}$
0	1	0	1	0	0	0	0	0
1	0	1	0	0	0	0	0	
0	0	1	0	0	1	0	0	$-V_{dc}$
0	0	1	0	0	1	0	1	$-2V_{dc}$
1	0	1	0	0	1	0	0	$-3V_{dc}$

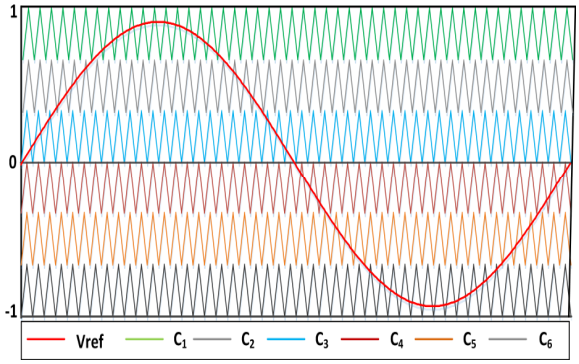

Fig. 2. Level Shifted Sinusoidal PWM for 7-level output voltage.

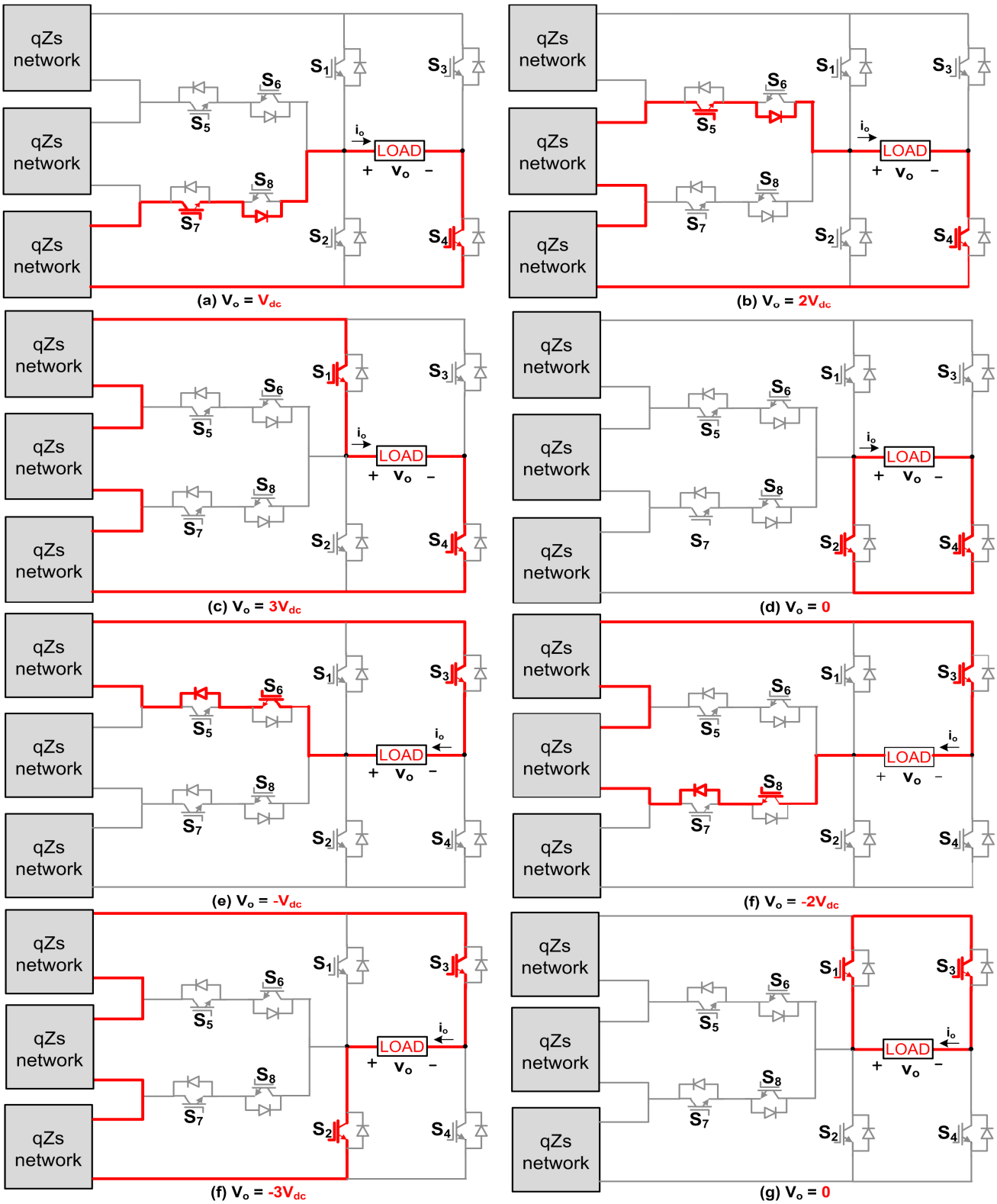

Fig. 4. Different Modes of operation of the proposed topology.

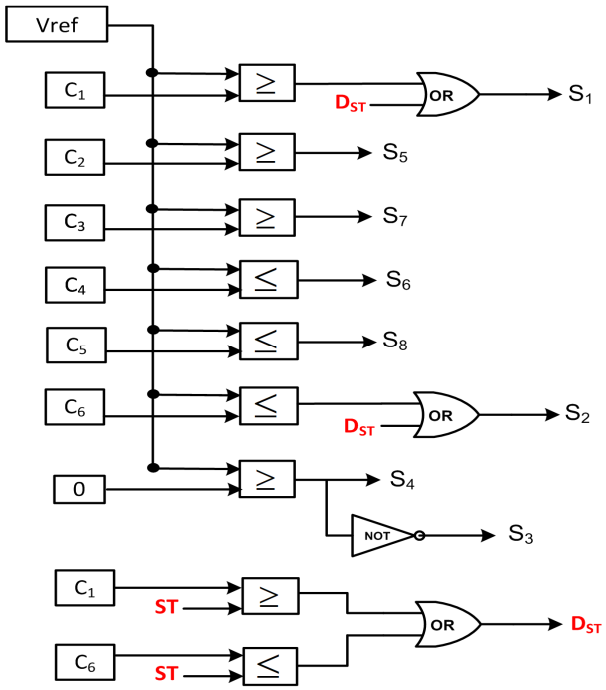

Fig. 3. Proposed Switching algorithm for control pulse generation.

IV. Simulation Results

In order to verify the operation of the proposed inverter, the simulation is performed in Matlab with the following specifications shown in Table III. Each impedance network is operated at an input voltage of 40V and shoot-through duty cycle of 0.2 for a resistive loading of 80Ω in order to obtain 110Vrms ac output. The dc-link voltage is boosted to around 76V for each qZs network. Fig. 5 shows the simulated waveforms of input voltage, input current and capacitor voltages of one qZs network. It can be observed that the input current increases linearly during the shoot-through mode and decreases during the active state. The capacitor voltages V_{c1}, & V_{c2} are boosted to around 58V and 18V respectively and are almost constant under steady state.

Fig. 6 shows the dc-link voltage waveform which is pulsating in nature. Fig. 7 shows the simulated waveforms of the inverter output voltage, filtered output voltage and output current. It can be observed that the output voltage is associated with high THD due to the nature of the waveform. Hence, a LCL filter is employed to filter out the switching harmonics present at $2f_s$ which is evident from the harmonic profile as shown in Fig. 8.

Table III
Specifications of the Parameters

Parameters	Values
Input dc voltage V	40 V
Inductor L	0.5 mH
Capacitor C	1000 μF
LCL Filter	1mH, 1μF
Switching Frequency	10kHz

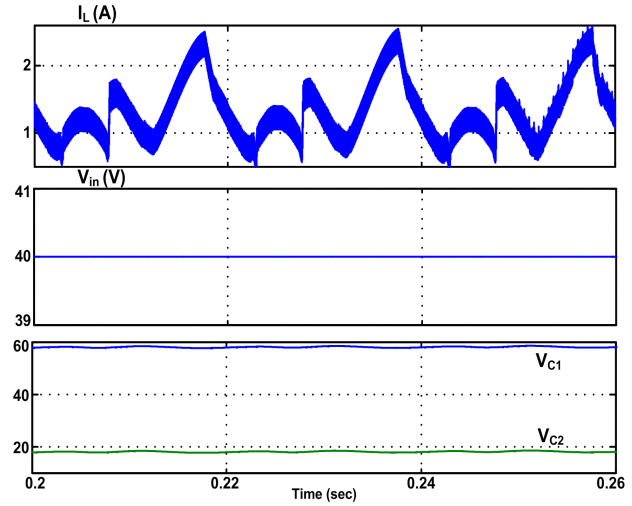

Fig. 5. Input voltage (V_{in}), Input current (I_L), & Capacitor voltages(V_{c1},V_{c2}).

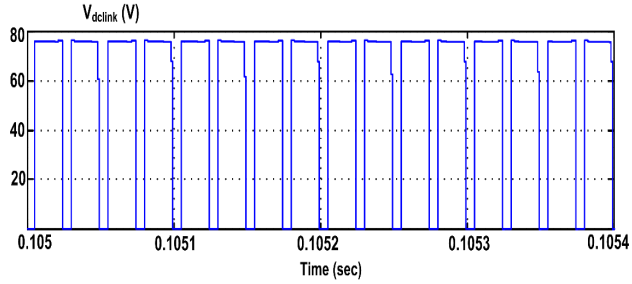

Fig. 6. DC Link Voltage V_{dclink}.

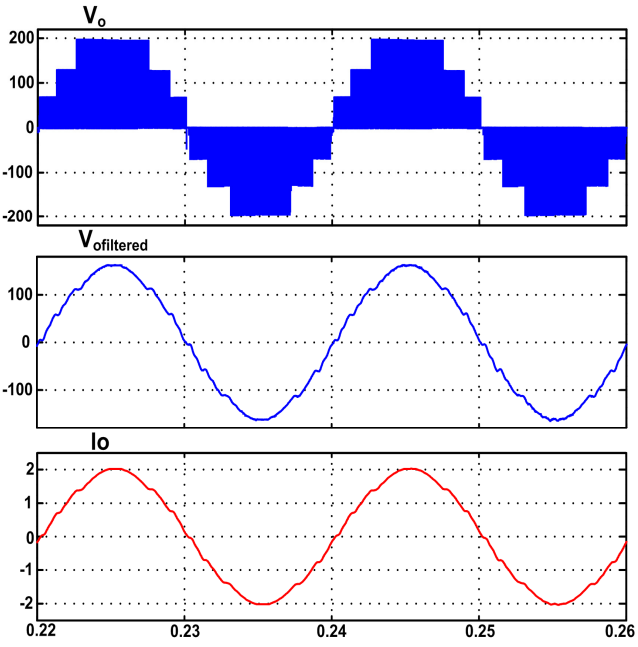

Fig. 7. Inverter Output Voltage(V_o), Filtered Output Voltage $V_{o(filtered)}$, &Output current.

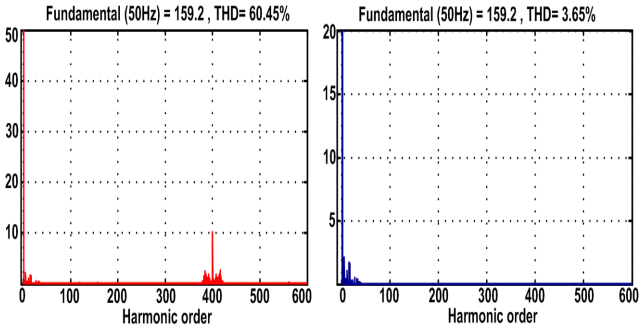

Fig.8. FFT spectrum of Inverter output voltage V_o and Filtered output voltage.

The LCL filter is designed as per the guidelines given in [12]. The inductor and capacitor of the qZs network are designed based on the switching frequency, output power, input current ripple and dc-link voltage ripple [13]. However, a large value of capacitor is required to mitigate the oscillations present in the dc-link voltage for high power applications.

V. Experimental Results

In order to validate the simulation results a scaled down prototype model is constructed in the laboratory with the available infrastructure. Three isolation 1:1 transformers fed by variac followed by rectifier units and large value capacitor is employed for realizing three isolated dc-sources. The switches are realized in a readily available IGBT module based on CT60-AZ which is equipped with inbuilt driver circuits. A low-cost Xilinx FPGA Spartan-6 processor is used for generation of control pulses using Xilinx system generator blocks. Here the experimentation is carried out for an input voltage of 10V for all the qZs networks and duty cycle of 0.2 with other specifications similar to simulation. Fig. 9 depicts the experimental waveforms of inverter output voltage, filtered output voltage and output current. It can be noticed that the pattern of output waveforms are in good agreement with the simulation results.

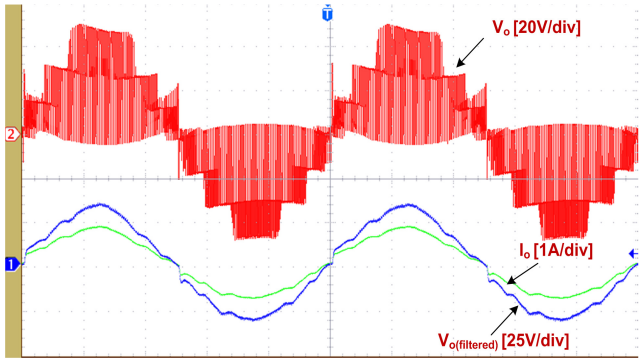

Fig .9. Inverter output voltage, Filtered output voltage and Output current.

V. Conclusion

A new hybrid quasi Z-source based T-Type seven-level inverter is presented for renewable applications. The proposed structure has reduced device count and modularity. A simple control technique is developed in which only two switches are in operation to synthesize any voltage level and the different modes of operation for each level generation is also presented. The performance of the proposed qZs based seven-level inverter operation and switching scheme has been verified through simulation and experimental results.

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