A Hybrid-Bridge Asymmetrical Transformerless Five-Level Photovoltaic Inverter

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***Abstract*— This paper presents a new Hybrid-bridge asymmetrical transformerless five-level photovoltaic(PV) inverter and also addresses the behavior of common mode voltage(CMV) and their modulation scheme. The proposed inverter topology is derived from the combination of half-bridge and diode-clamped module, which shall be able to produce less variations in the total CMV and suppress the leakage current as per the DIN VDE 0126 1-1 standards. This can be done through an asymmetrical filter inductor introduced between the inverter and loads. Moreover, the losses due to switching and conduction are less because of the lower voltage stress and reduced switching count which results in higher efficiency of operation. The voltage/current THD of the proposed five-level PV inverter is also within the standard limits. To realize the operation of the five-level inverter output voltage, CMV and leakage current measurement the simulation work is performed in Matlab software and their results are presented.**

Keywords*— *Transformerless multi level Inverter, Common mode voltage, Sinusoidal pulse width modulation, Total harmonic distortion.

I. INTRODUCTION

Transformerless PV inverters are gaining more popularity in the recent years because of their reduced size, cost and reliability. The features of the transformer in the grid connected inverter systems are that they boost inverter output voltage and provides isolation while feeding power from panels into the grid. The cost and size of such configuration is more as well as the efficiency is falls to nearly 2-3% with the usage of line frequency transformer [1]-[2]. To serve the above mentioned features a high frequency transformer with DC-DC conversion stage is depicted between PV source and inverter which reduces the cost and size of the system. But efficiency of the system is still challengeable due to increase in conversion stages [3]. Hence transformerless inverters are the best option for the grid integration from the PV panel [4]. The variation in CMV causes more leakage current flow across the grid and PV panel is the major drawback of the system and also not advisable as per the safety standards [4]-[5]. Many topologies are reported in the literature to overcome these drawbacks by employing the proper filter circuit, choosing effective modulation technique, design of an efficient inverter topology, and proper placement of an inductor [6]. The typical transformerless inverter shown in Fig.1.

The transformerless PV inverters are addressed using the following common structures of diode clamped also called

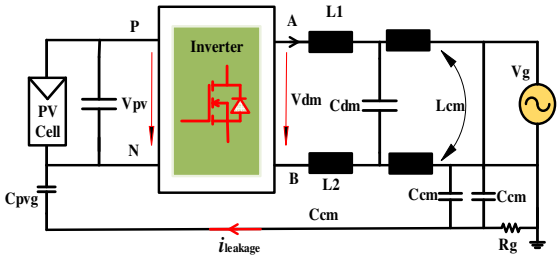

Fig.1 Typical transformerless PV inverter [4]

NPC, Flying capacitor and H-bridge inverter [7]. In NPC topology [8] and Flying capacitor clamped inverters [9] the neutral point of the grid is always taken to the centre of the DC capacitors to balance the CMV even in the freewheeling period. But these topologies requires double the PV voltage, complex control structure, less efficiency, and more component count than the H-bridge inverters for the same output power [10]-[11].

In the recent literatures some efforts are carried towards multi-level transformerless inverters with reduced switch count and control complexity. In [12] a 5L-ANPC transformerless inverter with flying capacitor is presented. The 5L-ANPC is already commercially available in the market for medium power applications because of its reduced costs and volume compared to the conventional flying capacitor and diode clamped inverters. But it requires a complex modulation strategy to maintain a stable DC voltage across the flying capacitors. Further development of a reduced switch count 6S-5L ANPC is proposed in [13]. Here the balancing of flying capacitor voltage is carried out with the available redundant states in the PWM generation. Some other five-level transformerless inverters are reviewed in [14], instead of using flying capacitor for the level generation coupled inductor are used across the load to support the reactive power sharing to the load and to achieve constant CMV. But the coupled inductor based inverter structure will increase overall system size and cost. Venu Sonti and Sachin Jain proposed [15-16], five-level module type transformerless PV inverters and the levels in output voltage waveform is achieved by using less number of active switches. But the circuit needs dead-time between each semi-conductor switch which are on the same leg to avoid short-circuit and conduction losses also be more.

G.Vazquez and P.R Martinez-Rodriguez proposed in [18]-[19], five-level transformerless inverter for grid tied PV

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systems using H5&Heric concept. In this topology eight power semiconductor switches are used to produce five-level output voltage and which can capable to limit the leakage ground current. M.J. Lopez-Sanchez proposed in [17], a single phase asymmetrical NPC inverter topology. But the conduction losses are more in the freewheeling period due to the use of three active switches. The switching losses also more in the NPC leg because it's operating at high switching frequency. The limitation of the above said topology has large value of leakage current due to the absence of dead time during switching. Some other Hybrid-bridge transformerless inverter topology also proposed in [21], to reduce the complexity and to improve the efficiency. But the output filter size, THD and switching stress of the power semiconductor switches are high. Moreover it can only produce three-level operations.

Therefore, in this paper a new Hybrid-bridge asymmetrical transformerless five-level photovoltaic inverter derived from the topology taken for the study [22]. The topology utilizes two isolated DC voltage sources in order to realize the five-level output voltage. Moreover, the analysis majorly focuses on the grid independent five-level inverter under fault conditions. Hence, in this work addressing of common mode voltage behavior and its corresponding leakage current are majorly taken for the proposed transformerless five-level inverter topology. This topology is derived with the use of a half-bridge module and diode clamped module for the generation of level voltage and to maintain constant common mode voltage (CMV). The proposed inverter is found to have higher efficiency due to the effective conduction and reduction in the switching voltage stresses. Moreover, the size, cost and control complexity of the inverter are minimized due to the absence of flying capacitors and coupled inductors. The simple sine PWM is employed to generate the triggering pulses to the inverter switches and it can also minimize the leakage current flowing into the PV panel from grid through parasitic capacitances.

II. Hybrid-Bridge Five Level Inverter

The schematic arrangement of the proposed hybrid-bridge five-level PV inverter consisting of eight active switches and two diodes are shown in Fig. 2. It is derived from the combination of a half bridge module with the NPC module hence it's referred as Hybrid-bridge. The five level output voltage is achieved with the use of bidirectional switches by dividing the dc voltage. Hybrid-bridge asymmetrical topology uses an inductor filter between VSI and the load. This also limits the CMV variations. The detailed operation of the five-level production and all the possible switching states are depicted in Table I.

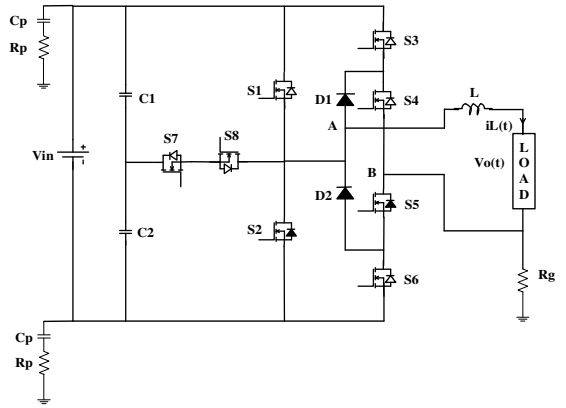


Fig.2 Proposed Transformerless PV inverter.

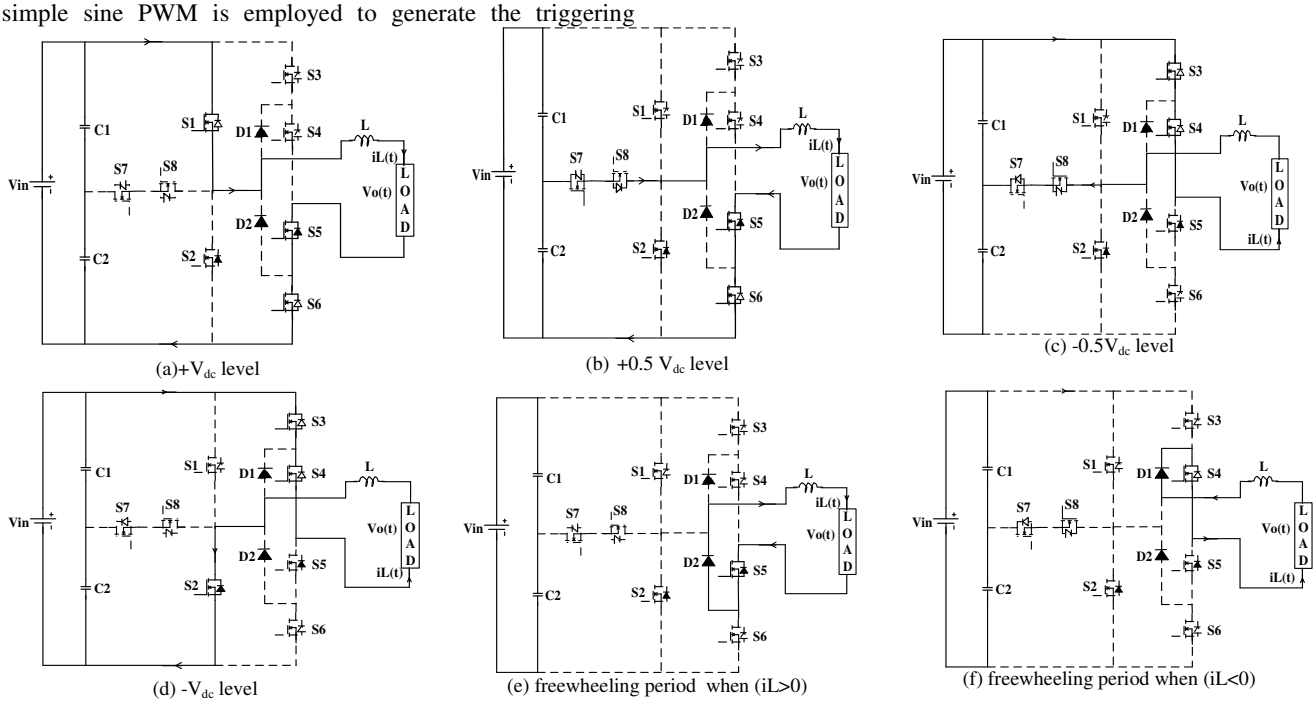


Fig.3 Different modes of operation.

TABLE.1 SWITCHING STATES OF THE PROPOSED INVERTER

Modes of operation		Switching States								Current path	Source combination	V_{AN}	V_{BN}
		S1	S2	S3	S4	S5	S6	S7	S8				
Positive	V_{dc}	1	0	0	0	1	1	0	0	S1-Load-S5-S6	$V_{C1} + V_{C2}$	V_{dc}	0
	0.5 V_{dc}	0	0	0	0	1	1	1	0	S7-Load-S5-S6	V_{C1}	0.5 V_{dc}	0
Zero	$i_L > 0$	0	0	0	0	1	0	0	0	D2-Load-S5	0	0	0
	$i_L < 0$	0	0	0	1	0	0	0	1	S4-Load-D1	0	0	0
Negative	-0.5 V_{dc}	0	0	1	1	0	0	0	1	S8-Load-S3-S4	V_{C2}	0.5 V_{dc}	V_{dc}
	$-V_{dc}$	0	1	1	1	0	0	0	0	S2-Load-S3-S4	$V_{C1} + V_{C2}$	0	V_{dc}

This explains the level generation, current path and corresponding switches which are under operation. The very popular level shifted sine PWM technique is employed to produce the level with simple control operation. Figs. 3(a) & (b) illustrates the V_{dc}, $0.5V_{dc}$ voltage level production and the conducting switches when power delivered to load at positive-half cycle operation. Similarly, $-0.5V_{dc}$ and $-V_{dc}$ voltage level generation and conducting switches when power delivered to load at negative half-cycle operation is given in Figs. 3(c) & (d) respectively. Table I clearly highlights the various switching conditions under level generation are used. Moreover, during the freewheeling period, when load current is more than zero the switch S5 and D2 will conduct. If it's less than zero the switch S4 and D1 will conduct as shown in Figs. 3(e) and (f) respectively. The special feature of the proposed topology is not using any dead time circuit during its operation. Hence the developed of the proposed configuration is simple.

III. COMMON MODE VOLTAGE & MODULATION STRATEGY

A. *Common Mode Voltage Calculation*

The common model used to estimate the CMV voltage for single phase PV applications is given in Fig. 4[5]. The common-mode behavior for the proposed topology can be expressed with the help of generalized common mode model. The expression used for the calculation of common-mode voltage (V_{tcm}) and differential-mode voltage (V_{dm}) is as follows;

$$V_{tcm} = V_{cm} + V_{s1} \quad (1)$$

$$V_{dm} = V_{AN} - V_{BN} \quad (2)$$

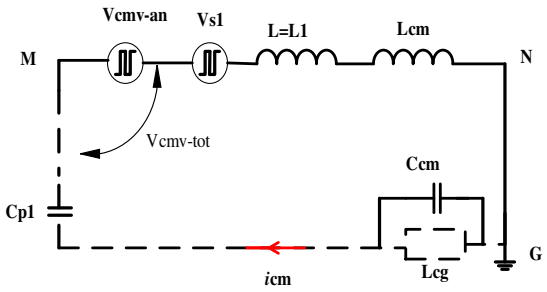


Fig.4 Equivalent common mode model [5].

$$V_{cm} = \frac{V_{AN}+V_{BN}}{2} \quad (3)$$

$$V_{S1} = V_{dm}\frac{L2-L1}{2(L1+L2)} \quad (4)$$

From the Eq. 4. The location of the filter can directly affect the current mode behavior. If the filter inductor split into two equal half's between line and the neutral wires, some leakage current will flow in the ground path from the above mentioned equations. Besides, if the filter inductor is implemented in the phase between inverter and grid, the leakage current in the ground path is to be reduced to desired limits. Therefore, filter inductor is used as just like NPC inverter [5].

The calculated results from the Equations (1) to (4) as tabulated in Table II. It can be observed that the CMV remains constant in the positive half-cycle. This shows that the leakage current flows in the ground wire is close to zero from Eq.5. From Table II there will be a change in the magnitude of Vtcm after the freewheeling period, which can allows flowing small leakage current in the ground path. Finally, in the negative half-cycle, the common-mode voltage of V_{dc} is maintained constant, which results in the leakage current is reduced to zero current.

$$i_{Leak} = C_{PV}\frac{dV_{tcm}}{dt} \quad (5)$$

TABLE II COMMON MODE VOLTAGE CALCULATION

Level		V_{dm}	V_{cm}	V_{s1}	V_{tcm}
Positive	V_{dc}	V_{dc}	0.5 V_{dc}	-0.5 V_{dc}	0
	0.5 V_{dc}	0.5 V_{dc}	0.25 V_{dc}	- 0.25 V_{dc}	0
Zero	0	0	0	0	0
	0	0	0	0	0
Negative	-0.5 V_{dc}	-0.5 V_{dc}	0.75 V_{dc}	0.25 V_{dc}	V_{dc}
	$-V_{dc}$	$-V_{dc}$	0.5 V_{dc}	0.5 V_{dc}	V_{dc}

B. Modulation Strategy

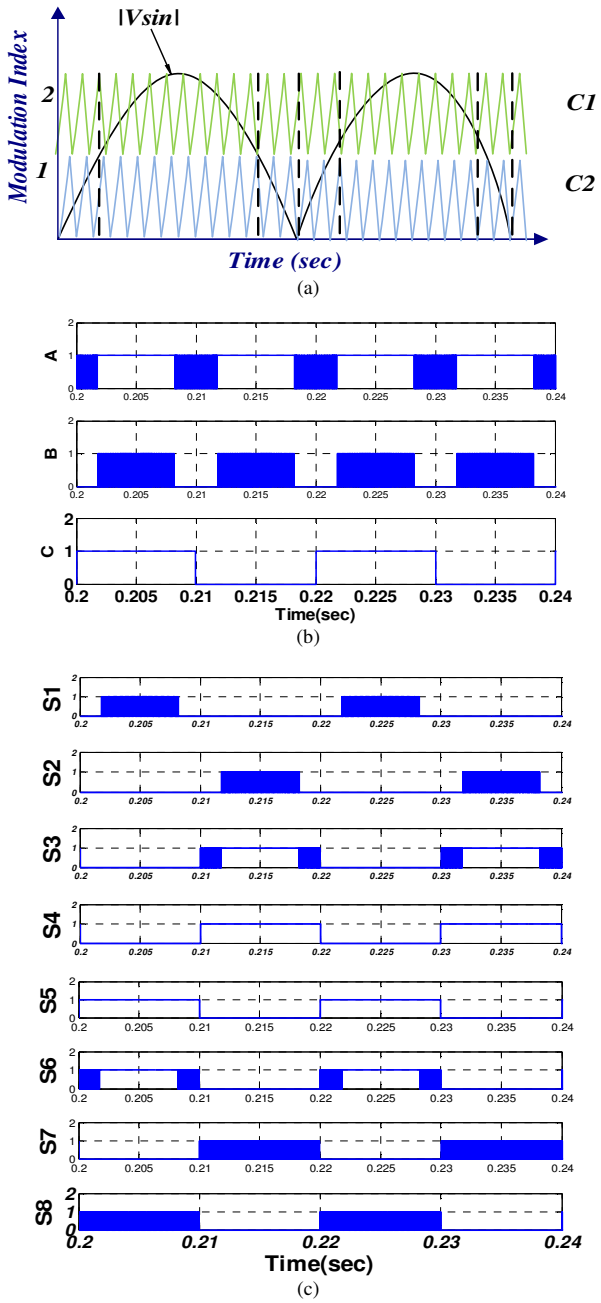


Fig.5(a) Waveform of the proposed SLS-PWM. (b) Modulation PWM scheme (c) Switching pattern.

The modulation strategy is implemented based on the level-shifted sine PWM described in [20]. Fig. 5(a) shows the level shifted sinusoidal PWM modulation is used for generating the control signals [20]. Where *Vsin* represents the absolute reference signal and carrier signals C1, C2 are used for the comparison of the reference signal. The implementation of sinusoidal level-shifted PWM technique is based on the two outputs of PWM schemes and a sign function, which are explained with the following expressions.

A = 1, if $V_{sin} > C2$ otherwise 0

B = *1, if* $V_{sin} >$ C1 otherwise 0

C = 1, if $V_{sin} > 0$

The switching pattern for the inverter switches are depicted in Fig. 5(b). The sum of A and B with C represents the reconstruction of V_{sin} during positive half cycle, while the sum of A and B with inverted C represents the reconstruction of V_{sin} during negative half cycle. Finally, reconstruction of the reference wave (V_{sin}) achieved out of this PWM signals. The PWM pulses used to generate the switching sequences by applying logical operations are as follows;

$$S1 = BC; \quad S2 = B\overline{C}; \quad S3 = A\overline{C}; \quad S4 = \overline{C}$$

$$S5 = C; \quad S6 = AC; \quad S7 = (A\overline{B} + \overline{A}B)\overline{C}$$

$$S8 = (A\overline{B} + \overline{A}B)C$$

By applying these PWM pulses, the reference wave V_{sin} is reconstructed trough the switching sequences for each one of the eight switches as shown in Table I. The periods of conduction of switches are very less as compared to the existing topologies. This improves the overall efficiency of the proposed five-level inverter due to reduced losses. The general expression used for the calculation of modulation index is

$$M = \frac{V_{sin}}{2V_c} \tag{6}$$

Where *Vsin* is the magnitude of reference sine waveform and *Vc* is the height of the all carrier waves.

IV. Comparison between Proposed Inverter and the Existing Topologies

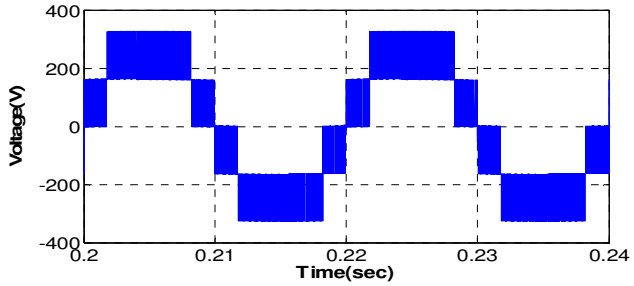
For better illustrations of the proposed topology the comparison made among the existing topologies in terms of device count, number of conducting devices in different modes, dead-time requirement and losses. From Table III the total active switches used in the proposed topology are more except topology [19], even though the total number of switches conducting in one cycle is less as compared to other topologies. Hence the proposed inverter having less conduction losses and more efficiency. The practical implementation of the proposed inverter is quite simpler because of no need of dead-time circuit between the active switches.

V. Simuation Results

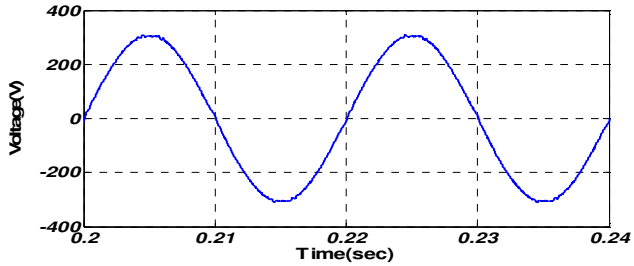
Inorder to study the feasibility of the proposed hybrid-bridge five-level inverter, the simulation work is taken in Matlab environment. The simulations are focused on the output level generation, power injected to the load, CMV, leakage current and THD. The parameters considered for the simulation study are as follows; P=750W, Vpv=325V, fs=2.5kHz, L=1.5mH, R=65Ω, Cp=100nF, Rp=0.1Ω, and Rg=1Ω. Where Rp and Cp are the parasitic values of resistance and capacitance of the PV panel and Rg is the ground resistance. The measured inverter output voltage, filtered output voltage and load current waveforms are given in Fig.6. It can be seen that all the output waveforms shows better response under loading.

TABLE.III COMPARISON OF VARIOUS TRANSFORMERLESS INVERTER TOPOLOGIES

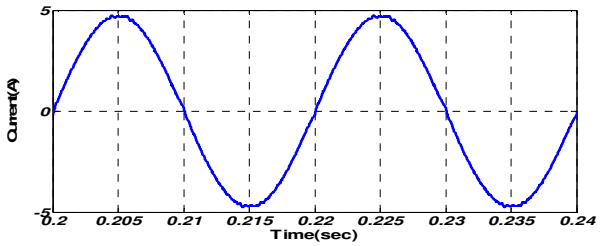
Parameter			Topology[15]	Topology [16]	Topology[13]	Topology [19]	Proposed
No. of Active switches			8	7	6	8	8
No. of Diodes			0	0	2	4	2
Conduction of switches	Positive	V_{dc}	4	3	3	2	3
		0.5 V_{dc}	4	4	3	2	3
	Zero	0	2	2	3	1	1
	Negative	-0.5 V_{dc}	4	4	3	3	3
		$-V_{dc}$	4	3	3	3	3
Dead-time			Needed	Needed	Needed	Needed	Not needed
Losses			More	Medium	Medium	Less	Less



(a)

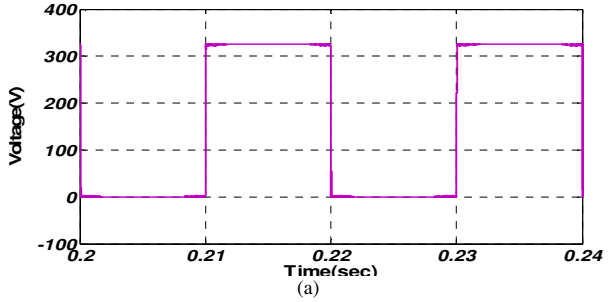


(b)

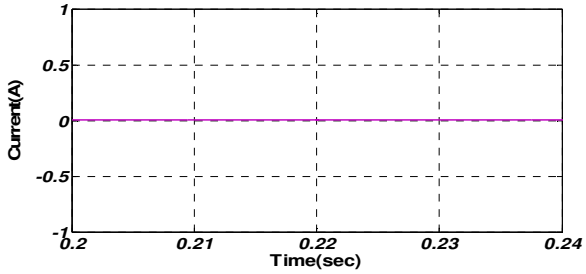


(c)

Fig.6 Simulation results of (a) Inverter output voltage (b) Filtered output voltage and (c) load current waveforms



(a)



(b)

Fig.7 Simulation results of (a) Common mode voltage and (b) Leakage current waveforms.

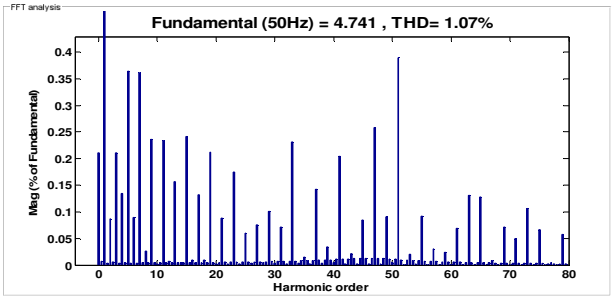


Fig.8 FFT window for the output current

The total common mode voltage is calculated in section III is depicted in Fig. 7(a). It's to be noticed that the common mode voltage having variations during changes in output levels from 0 to $-V_{dc}$ and reaches as same as Vpv of 325V. This shows the calculated value matches with the simulation results as derived in Table II. For every cycle of operation the change in the common mode voltage develops a small peak current spikes in the ground path and almost invisible in the enlarged diagram as shown in Fig. 7(b). The leakage current is also within the standards of DIN VDE 0126 1-1. This ensures the employability of the proposed hybrid-bridge five-level inverter for transformerless PV applications. Moreover, the output current THD waveform is within 5% and same as shown in Fig. 8.

VI. CONCLUSION

The hybrid-bridge asymmetrical transformerless five-level inverter is presented. The proposed topology can provide the five-level output voltage which can be the special feature as compared with the commercial single-phase transformerless inverters. The proposed inverter significantly maintains the

common mode voltage and also limits the leakage current within the standards. The harmonic contents in the output of multilevel inverter are less which reduces the cost of filter components. The simulated results show better response during loading conditions. The number of conducting devices is also less which results in higher efficiency that motivates the utilization of proposed topology for transformerless PV applications.

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