Xilinx FPGA Based Single Phase Five-Level Cascaded Z-Source Inverter

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***Abstract*—This paper presents a single phase five-level cascaded Z-source inverter with reduced number of switches for PV/FC/Wind power applications. The inherent benefits of z-source inverter are higher boost gain and fault ride through capability compared with the traditional VSI and CSI inverters. Therefore five-level Z-source converter is simulated in MATLAB/Simulink environment and the generation of control pulses with the help of Xilinx System Generator is presented. A prototype model is developed to validate the theoretical concepts through experimental and simulation results.**

Keywords—Z-Source inverter; Shoot Through; PSPWM; FPGA; Xilinx System Generator

I. INTRODUCTION

In present scenario, modernization of any industries focusing on drives system with digital controller because of fast, lower cost and compact in size. The development of multi level inverter is getting popularity not only for merits of reduced voltage stress, low EMI and %THD and also for reduced component counts as reported in the literatures[1-3]. Power electronic interfaces plays an important for PV/FC based power supply system to interface their lower output voltage of 50-100V DC and boosted to higher voltage of 600V and further converted into AC using Inverters. This can be done either using traditional voltage source inverters(VSI) or current source inverters(CSI). But the VSI is generally operated in buck mode which required always higher DC link voltage greater than the inverter output voltage. whereas CSI inverter requires additional series diode and prevents the use of low cost switches[4].

Therefore, a two stage converter is proposed using half full bridge, push pull, fly back and conventional boost converters in [5] with an intermediate state of DC-DC conversion. However, two stage conversion increases the size and cost of the system, and thus efficiency of the converter is less due to increased components. To overcome the above problems a high gain z-source converter is introduced between the source and inverter [6]. But the traditional two-level inverters have the inherent problems of producing electromagnetic interference(EMI). Development of suitable power electronic interface and their controller requires enormous effort to meet end users demands at lower cost and compact size.

Therefore, in this paper a five-level cascaded z-source inverter with reduced component count, high efficiency and better quality of supply is considered. A simple carrier based PWM scheme and shoot through states are implemented to generate the switching signals and the simulink model is developed in MATLAB/Simulink environment. To validate the concepts an experimental setup is developed. The control scheme is implemented in high speed low cost SPARTAN 6 FPGA board using Xilinx Blocks in MATLAB software and the results are presented.

II. FIVE-LEVEL Z-SOURCE INVERTER

Fig.1 shows the five-level cascaded z-source inverter topology and consists of a set series connected smaller multilevel inverter blocks. In general the single stage block with z-source consists of two parallel connected inductor and capacitors and switches S1 and S2. Here the boost operation can be done by introducing a shoot through by turning on both switches at same time. This is decided by the duty cycle for which DC link voltage to be amplified. During active state S1 is turned on and S2 is turned off. The desired output level can be implemented by connecting this single stage block with z source in cascaded structure and the output of the cascade stage is connected with H-Bridge.

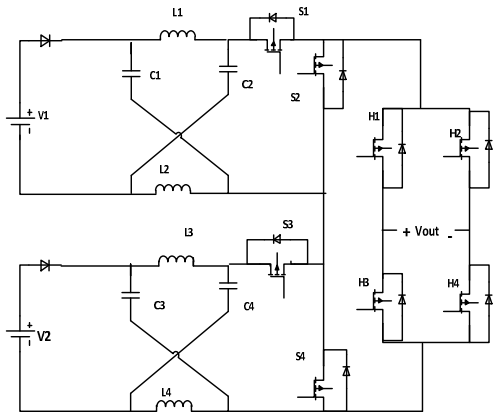

Fig. 1. Cascaded Five-Level Z-Source Inverter.

In this work phase shifted carrier pulse width modulation is implemented to generate the five-level. Each cell is modulated independently using sinusoidal unipolar pulse width modulation and bipolar pulse width modulation respectively, providing an even power distribution among the cells. A carrier phase shift of 180°/m for cascaded inverter is introduced across the cells to generate the stepped multilevel output waveform with lower distortion. Simple boost control method is implemented with phase shifted carrier pulse width modulation to introduce shoot through state [7], [8].

Gate pulses for switch S1 and S2 are obtained by comparing the first triangular carrier wave with modulating

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wave and latter shoot through pulse is added. Gate pulses for S3 and S4 are obtained by the same procedure as above said but the triangular carrier wave is shifted to 180 degree. Switches in H Bridge operate at 50 Hz square wave pulses. Switches H1 and H4 are turned on at the same time and switches H2 and H3 are turned on at same time. The pulsating DC link voltage and inverter output voltage can be calculated using the following equations;

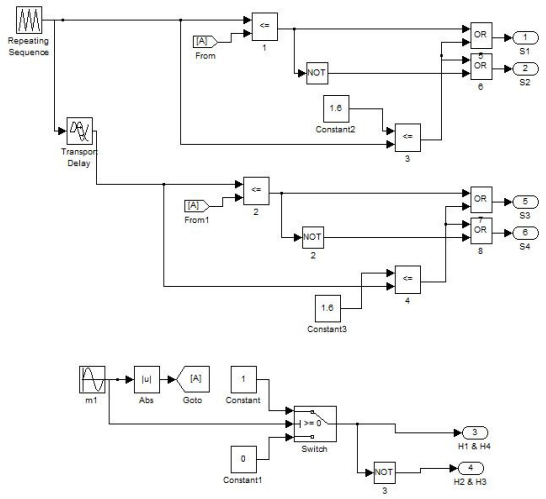
$$V_{dcn} = 2V_c - V_G = \frac{T}{T_1 - T_0} V_G = \frac{1}{1-2D} V_G = BV_G \qquad (1)$$

$$V_{ac} = M \frac{V_{dcn}}{2} \qquad (2)$$

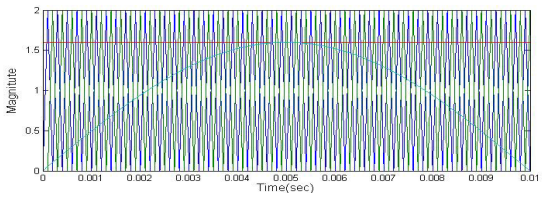
where B is known as the boosting factor based on D; V_{dcn} is the steady state value of the peak dc-link voltage; V_c is the steady state DC value of the capacitor voltage; V_G is the steady state value of the input voltage; M is the modulation index of the inverter.

III. Simulation Results

Configuration shown in Fig. 1 has been modeled by MATLAB/SIMULINK to verify the capabilities of mentioned inverter. Simulated multilevel inverter parameters are given in Table 1. The developed control scheme and the implementation of shoot-through concept comparing the magnitude of modulation wave and constant are shown in Figs. 2(a) & (b). The proposed inverter is studied for Vp=1.6. It is expected that boost gain, B=1.66. Fig. 2(a) presents the five-level load voltage and desired five-levels are approximately 0, ±20V, ±40V. The corresponding load current, z-source output voltages for R and RL loads are given in Figs. 3(a) & (b) respectively. The frequency spectrum for the line voltage and currents for RL load are shown in Figs. 3(c) & (d). It is observed that the current THD of RL load is within the limits of IEEE standards.

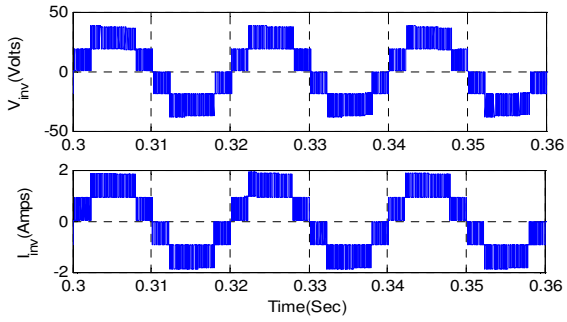


(a)

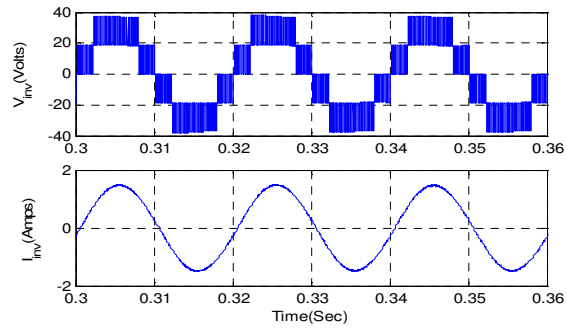


(b)

Fig. 2(a) control scheme developed in MATLAB simulation (b) Simple boost phase shifted carrier technique.



(a)



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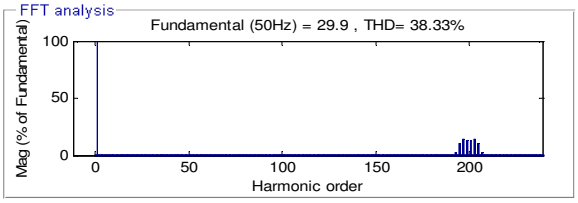
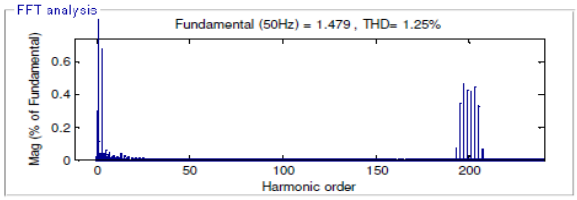


(c)



(d)

Fig. 3. (a) Inveter output voltage and current waveforms for R Load; (a) Inveter output voltage and current waveforms for RL Load; (c) %THD of inverter output voltage for RL Load; and (d) %THD of inverter output current for RL Load.

TABLE I SIMULATION PARAMETERS VALUES

PARAMETERS	VALUES
Vin	12
C1=C2=C	6.6 mF
L1=L2=L	3 mH
Do (Shoot-through Duty cycle)	0.2
Ma	0.8
switching frequency	5 kHz
Line frequency	50 Hz
Load	R=20 Ω L=10 mH

IV. XILINX SYSTEM GENERATOR

In earlier days, the PWM pulses were generated using micro controllers. However, the easiest way of implementation of control algorithm using DSP or FPGA interfaced with MATLAB software overcomes the lower speed, hierarchical rules and commands over its input and output signal which are followed while programming and execution with microcontroller. Fig. 4 shows the control scheme developed in Matlab using Xilinx tools. The counter block generates the saw-tooth and triangular waveforms either by selecting up/up-down mode operations. Here, the maximum counting period is limited by the number of bits selection. For example, the counter is enabled for free running value of 256 counts for 8 bit operation. However, the designer can limit/select suitable count periods based on their demands. The ROM block is used to generate the sine signal up to given count period and frequency can also be adjusted. The generated sine wave is compared with the triangular waveform and the logical blocks are build as per the control signal patterns given to the switches using Xilinx block tools. The Gateway Out is used to assign proper I/O as per the pin assignment given in the Atlys Spartan 6 users manual[10]. Further system generator can simulate and generate VHDL codes for the developed circuit in MATLAB.

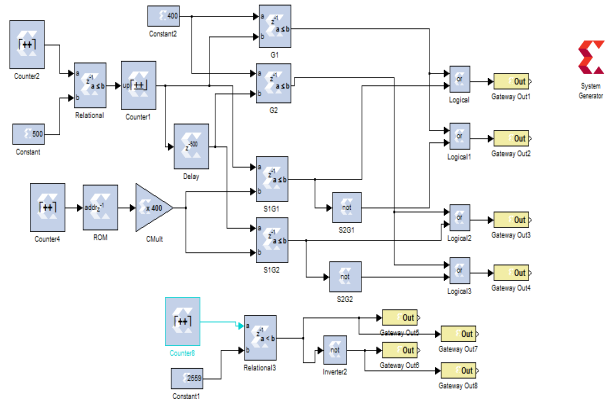


Fig. 4. Control scheme developed in MATLAB using Xilinx blocks & system generator.

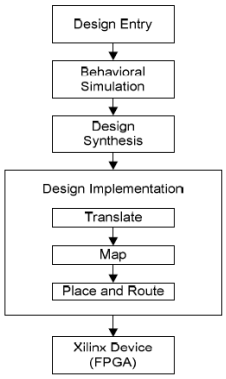


Fig. 5. FPGA design flow[9].

The FPGA can be redesigned for any converter and inverter control. Fig. 5 shows the design flow of FPGA using Xilinx tools. The procedure for implementation is as follows:

1. Develop the control scheme in MATLAB/Simulink model using Xilinx blocks
2. Built the model using system generator for the desired frequency to convert the blocks into VHDL code.
3. Generate .Bit stream program file using ISE Design suite.
4. Load the program into FPGA board via SPI FLASH programming.
5. Test the pulses using digital storage oscilloscope at the output of VHDL connector.

V. EXPERIMENTAL RESULTS

Fig. 6 shows the photograph of experimental set-up tested in the laboratory. The experimental components and their corresponding values are given in Table I. The generated gate pulses for the level production and for the H-bridge inverter using Spartan 6 FPGA is given in Figs. 7(a) to (c). The output of the FPGA signal is boosted and isolated from the power circuit using a buffer circuit and TLP250 opto-coupler IC. The measured experimental inverter output voltage and current waveforms for R and RL are given in Figs. 7(d)&(e). It is observed that the experimental waveforms exactly match with the simulation results that validate the performance of the developed model.

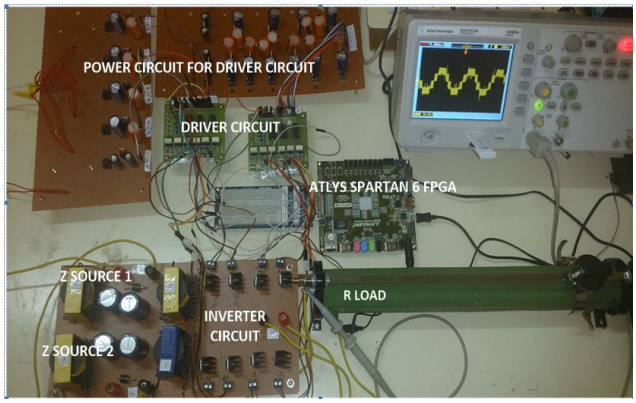
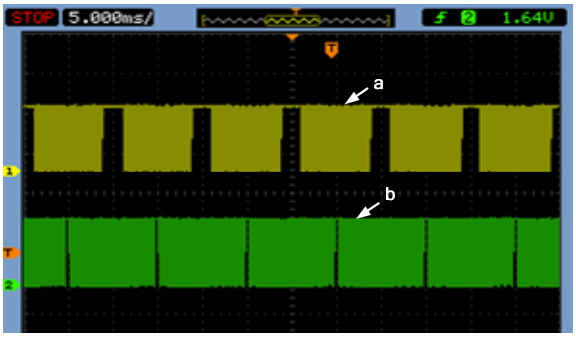
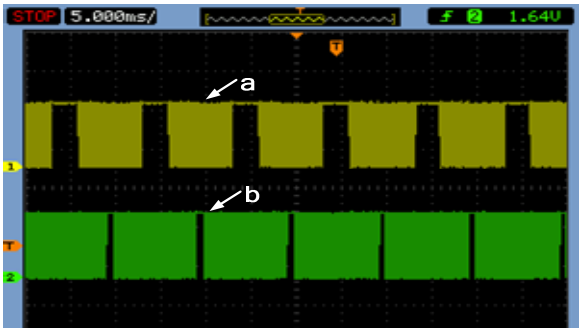


Fig. 6. Experimental setup.



(a)



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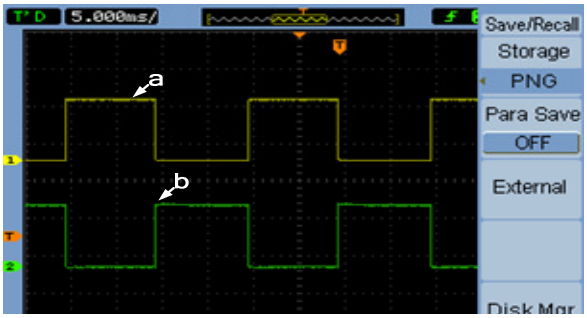

(c)

(d)

(e)

Fig. 7. (a)-(c) control pulses for switches generated at the output of FPGA, (d) & (e) Inverter output voltage and current waveform for R and RL load.

VI. Conclusion

In this paper, a single phase cascaded z-source five-level inverter is developed using lower switching devices and the results are presented for R and RL loads. An experimental setup is developed to validate the simulation results and the control scheme is implemented in high speed SPARTAN 6 FPGA development kit using Xilinx block sets and system generator with MATLAB software. The experimental results prove the performance of the developed five-level cascaded z-source inverter.

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