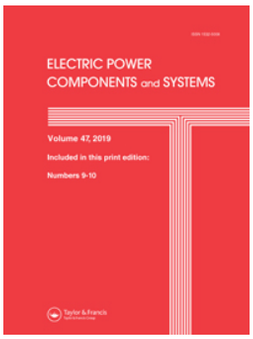

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Cost Effective Single-Phase DSTATCOM for Low Power Applications

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CONTENTS

Abstract—In this article, a single-phase Distribution Static Compensator (DSTATCOM) with reduced dc-link voltage is proposed for power quality improvement in a distribution system. Generally, the dc-link voltage of DSTATCOM is maintained twice the peak of Point of Common Coupling (PCC) voltage by voltage regulation loop. But, the dc-link voltage is maintained itself without voltage regulation loop in the proposed method. For this case, the required dc-link voltage magnitude is less when compared to conventional method. Under predefined load conditions such as agriculture pump set loads, this less voltage is sufficient to give satisfactory performance. Therefore, the rating of DSTATCOM is reduced and thereby the cost of system is reduced. The proposed method enables compensation of reactive power and mitigation of source current harmonics in a distribution system for low power applications. The advantages of the proposed method are elimination of dc voltage sensing elements, minimization of switching loss of Voltage Source Inverter (VSI) and cost effective. The proposed single-phase DSTATCOM performance is demonstrated through MATLAB/simulink and validated by experimental results with agriculture pump set load.

1. INTRODUCTION

Harmonic current distortions and reactive power demand are the major power quality issues in the distribution system, which leads to poor power factor, high Total Harmonic Distortion (THD), low efficiency and temporary/permanent failure of the system components [1, 2]. These issues mainly arise due to the proliferation of different non-linear and reactive loads in the distribution system. In initial stages, passive filters are used to mitigate current harmonics of tunned frequency and fixed reactive power compensation. However, passive filters are bulky in nature, fixed compensation only possible and suffer from resonance problem [3]. In distribution system, to mitigate current harmonics and reactive power compensation, DSTATCOM is most preferable solution [4–6]. The DSTATCOM is established with Voltage Source Inverter (VSI) having dc-link capacitor on dc-side and interfacing inductor on ac-side. The dc capacitor acts as a constant dc source for the VSI to produce the compensating

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NOMENCLATURE

L_s	Source side feeder Inductance	i_{D1}	Anti-parallel diode current of upper switch
R_s	Source side feeder resistance	i_{D2}	Anti-parallel diode current of lower switch
C_{dc1}, C_{dc2}	Upper and lower dc-link capacitances	i_{S1}	Instantaneous current of upper switch
L_f	Interfacing inductance	i_{S2}	Instantaneous current of lower switch
i_f	Instantaneous filter current	Q	Rated reactive power demand by load
i_s	Instantaneous source current	$f_{sw,max}$	Maximum switching frequency
i_l	Instantaneous load current	h	Hysteresis band
$i_{f,ref}$	Instantaneous reference filter current	f_{sw}	Switching frequency
i_{dc1}	Charging current of upper dc-link capacitor	E_{sw}	Energy dissipation in switch
i_{dc2}	Charging current of lower dc-link capacitor	I_f	RMS filter current
V_{dc1}, V_{dc2}	Upper and lower dc-link capacitor voltages	THD	Total Harmonic Distortion
I_{fn}	RMS filter current at nominal test conditions	PCC	Point of Common Coupling
TC_{sw}	Temperature coefficient	UCC	Unit Capacitor Constant
T_j	Junction temperature of IGBT switch	VSI	Voltage Source Inverter
V_{dc}	Total dc-link voltage	IGBT	Integrated Gate Bipolar Transistor
$V_{dc,n}$	Total dc-link voltage at nominal test condition		

current such that to make the source current sinusoidal and harmonic free [7]. The dc voltage maintained across dc capacitor plays a very important role in the compensation performance.

Different approaches are discussed in literature to maintain the dc capacitor voltage. In [8], through rectifier circuit, the dc capacitor is charged and maintained constant, because of rectifier circuit the system cost increases. Later on, the dc capacitor voltage is maintained by voltage control loop, in which the error between instantaneous dc voltage and reference dc voltage is given as input to controller. In this method, the dc voltage is not accurately controlled, as a result unclean voltage is produced, which increases the Total Harmonic Distortion (THD) [9, 10]. In [11], PI controller is implemented to maintain the dc-link voltage constant, forcefully. The dynamic model of the DC voltage regulator is discussed in [12], which adopts PI controller to maintain constant dc-link voltage. The PI controller suffers from tunning of gains for proportional and integral, and the response also sluggish for load variations. In [13, 14], Fuzzy Logic Controller (FLC) is implemented because of its faster and accurate performance, and also it do not required mathematical designing, tunning like PI controller. FLC handles non-linearity system effectively and robust in nature. The dc voltage control for single-phase shunt active power filter with step size error cancelation in self-charging algorithm is discussed for better dynamic response compare to PI and FLC in [15].

The dc voltage controller maintains the dc capacitor voltage to the reference dc voltage. In general, the dc reference voltage is selected as twice the peak of PCC voltage, which leads to high voltage stress across switching devices and increases switching loss during reduced load conditions [16]. In [17], the required dc voltage is reduced by connecting an ac capacitor in series with the filter inductor. But, this method requires more voltage sensors and fails to compensate when load current having dc off-set. Because, the ac capacitor connected in series with DSTATCOM does not allow dc off-set filter currents. In [18], compensation performance is investigated by varying the dc voltage and interfacing inductance. In which, the required dc voltage is selected as 1.6 times peak of PCC voltage from the empirical relation and the analytical expression. In the above discussed controlling methods, in addition to PCC voltage sensor, another two voltage sensors are required for dc-link voltage control. This will increase the total cost of the controller. In low power applications, the cost is one of the important factors for real time implementation. Also, the improvement of the system efficiency, depends on the converter losses. This motivates to implement a cost minimization and loss reduction approach. In general, the computational burden on controller depends on the control logic and usage of ADCs and DACs. As the measuring sensors are reduced, the usage of ADCs come down, which reduces the computation burden on controller. In low power applications of distribution system, for a predefined load condition the require dc voltage is less when compared conventional methods. Therefore, DSTATCOM with less dc-link voltage and giving satisfactory performance for compensation is proposed in this article.

In the proposed method, the required dc voltage for power quality improvement is maintained itself without the dc voltage regulation loop. For that, a proper design of DSTATCOM parameters is required and it is explained in this article. Advantages of the proposed method are elimination of voltage sensing elements, reduced dc voltage is

sufficient for compensation in low power applications, which indirectly reduces the switching loss of voltage source inverter and cost effective. In order to show the effectiveness of the proposed method, different cases are considered and are validated through simulation and experimental studies. Also, the proposed method is validated experimentally with agriculture pump-set load. As the dc-link voltage is reduced in the proposed method, it supports direct connection of renewable source (PV) on dc side of VSI for real power injection [19, 20].

2. DSTATCOM CONFIGURATION, OPERATION AND DESIGN PARAMETERS

A single-phase DSTATCOM in distribution system is shown in Figure 1. To analyze the performance of DSTATCOM, two loads (linear and non-linear) are considered. The feeder inductance and resistance are denoted as L_s and R_s, respectively. The DSTATCOM is realized by IGBT with anti-parallel diode as switch based VSI, two dc-link capacitors $(C_{dc1}$ & $C_{dc2})$ and interfacing inductor (L_f). The IGBT switches and anti-parallel diodes are denoted as S_1, S_2, and D_1, D_2, respectively. The two dc-link capacitors are charged to peak of PCC voltage, v_{pcc} through an anti-parallel diodes when DSTATCOM is connected at PCC and maintained constant during the operation. The DSTATCOM will inject filter current, i_f such that source current, i_s becomes harmonics free and in-phase with source voltage even though load current, i_l having harmonics. The single-phase DSTATCOM operation with proposed method is analyzed by simulation in next section.

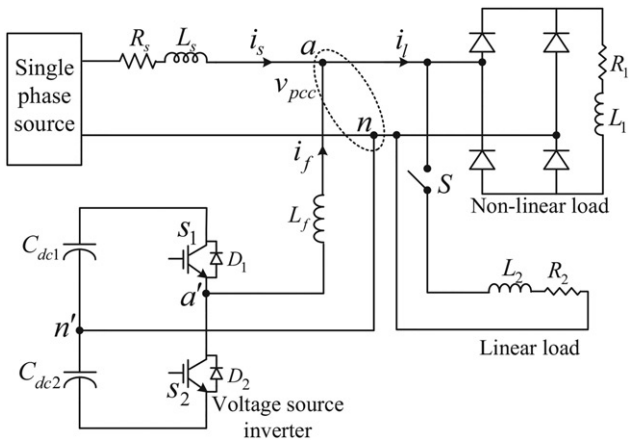

FIGURE 1. Single-phase split capacitor DSTATCOM topology.

2.1. Charging of DC Capacitors during DSTATCOM Operation

The charging of dc capacitor during the operation of DSTATCOM without and with gate pulses applied to IGBT switches of VSI are discussed in this section.

2.1.1. Without gate pulses applied to DSTATCOM. The charging paths of dc-link capacitors without applying gate pulses to switches are shown in Figure 2. The capacitors (C_{dc1}, C_{dc2}) are charged through an anti-parallel diodes (D_1, D_2) of switches (S_1, S_2) during positive half cycle and negative half cycle of source voltage respectively. The simulated wave forms without gate pulses applied are

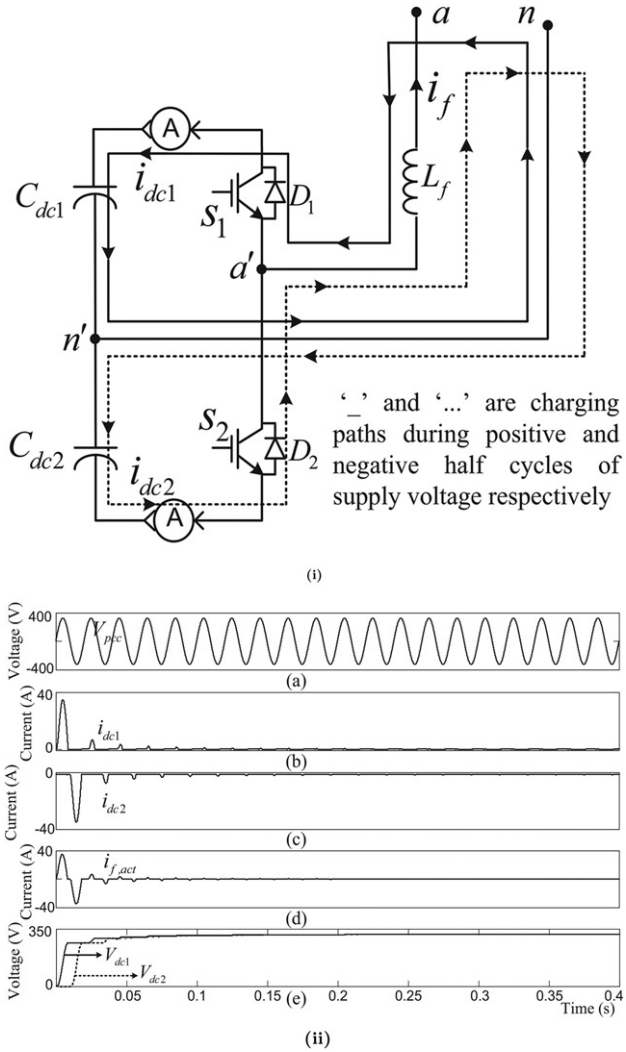

FIGURE 2. (i) Charging paths of dc capacitors without gate pulses applied to DSTATCOM, (ii) (a) PCC voltage, (b) charging current of capacitor (C_{dc1}), (c) charging current of capacitor (C_{dc2}), (d) filter current $(i_{f,act})$, and (e) dc side voltages $(V_{dc1,2})$.

shown in Figure 2(ii). The applied source voltage is 230 V (325 V peak), which is shown in Figure 2(ii)a. The charging currents of the dc-link capacitors C_{dc1} and C_{dc2} are shown in Figure 2(ii)b and (ii)c, respectively. After 1 to 2 cycles, the charging currents becomes zero and it is observed from Figure 2(ii)d and (ii)e. The reason is, the dc-link capacitors are almost charged to peak of PCC voltage and there is no discharging path.

2.1.2. Gate pulses applied to DSTATCOM. The DSTATCOM starts functioning, when the gate pulses are applied to switches based on the control algorithm. In conventional DSTATCOM, the dc-link capacitor voltages maintained constant to twice the peak of PCC voltage by a voltage regulation loop [21]. In the proposed method, the dc-link capacitors are charged to peak of PCC voltage through anti-parallel diodes. The conduction of switches and diodes are given in Table 1. The advantages in proposed method are (1) less dc-link voltage (*i.e.*, peak of PCC voltage) is sufficient for compensation, therefore voltage stress of switches reduced, (2) switching losses are reduced.

For better understanding the operation of DSTATCOM, simulation waveforms with *R–L* load are shown in Figure 3. The reference filter current ($i_{f,ref}$), currents through the switching devices (S_1, D_1, S_2, D_2) and dc-link capacitor voltages are shown in Figure 3(i)–(vi), respectively. It is observed from one full cycle of operation in Figure 3, that the dc capacitors are discharging through S_1 and S_2 for positive and negative half cycle of reference filter current, respectively. And, the capacitors (C_{dc1} and C_{dc2}) are charged through diodes, D_1 and D_2 for negative and positive half of the reference filter current, respectively. However, the dc voltages are having oscillations because of charging and discharging, which are shown in Figure 3(vi), the average dc voltages across the capacitors are maintained constant. This voltage magnitude is equal to the peak of PCC voltage and which is less when compared to dc voltage in conventional method, so the rating of DSTATCOM and cost of system are reduced.

Reference current	Conducting device	dc-link capacitor voltages
$i_f>0$ & $\frac{di_f}{dt}>0$	S_1	Discharging of C_{dc1}
$i_f>0$ & $\frac{di_f}{dt}<0$	D_2	Charging of C_{dc2}
$i_f<0$ & $\frac{di_f}{dt}>0$	D_1	Charging of C_{dc1}
$i_f<0$ & $\frac{di_f}{dt}<0$	S_2	Discharging of C_{dc2}

Table 1. Conditions for conduction of switches and diodes.

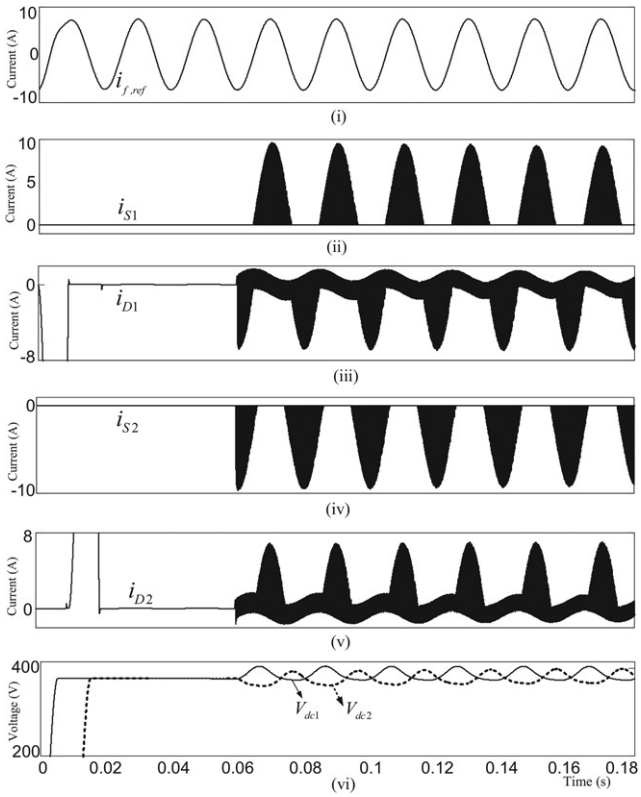

FIGURE 3. Simulation waveforms for *R–L* load (i) Reference filter current, (ii) Current through device S_1, (iii) Current through device D_1, (iv) Current through device S_2, (v) Current through device D_2, and (vi) dc-link voltages.

The satisfactory performance of the proposed method without the voltage regulation loop, depends on the design of dc capacitor value. In general, super capacitor is used in dc side of DSTATCOM to improve the performance [22]. In conventional methods, the calculated dc capacitor value is high, this results capacitor to charge continuously if the dc voltage regulation loop is not present. In addition, large capacitor value will also slow down the system dynamic performance. This problem will be rectified by using PI controller. But, it increases cost due to involvement of large capacitor and dc voltage sensors. In practical cases, under predefined load conditions (*e.g.*, Agriculture pump-set load), there is no need of dc voltage regulation loop if the dc capacitor value chosen properly. In the proposed method, capacitor value is designed based on Unit Capacitor Constant (UCC), which is similar to that of unit inertia constant in synchronous rotary condenser is given as, [23].

$$UCC = \frac{\frac{1}{2} C_{dc} V_{dc}^2}{Q} \tag{1}$$

where Q is the rated reactive power demand by load, C_{dc} is dc-link capacitance, V_{dc} is dc-link voltage. The dc-link voltage is maintained constant (*i.e.*, peak of PCC voltage) through an anti-parallel diodes of IGBT switches. During design of dc capacitor, the allowable dc voltage ripple (5%) is also considered. For example, at supply voltage of 230 V and load maximum reactive power of 3.8 kVAR, the value of UCC is chosen as 0.02 J/VA for faster response. Then, the calculated dc-link capacitor value from (1) is equal to 1600 μF. This capacitance value is less when compared to value in conventional methods [24, 25, 26].

2.2. DSTATCOM Parameters Selection

The selection of DSTATCOM parameters like dc-link voltage, interfacing inductor and dc-link capacitor are required for proper tracking of reference filter current. The selection of these parameters in the proposed method are discussed below.

2.2.1. Selection of dc-link voltage (V_{dc}). The dc-link voltage plays a very important role in design of the DSTATCOM parameters. In general, the reference dc-link voltage of DSTATCOM is selected as twice the peak of PCC voltage [18].

In the proposed method, the two dc-link capacitors are charged to peak of PCC voltage through an anti-parallel diodes of IGBTs. This voltage is sufficient to improve power quality without voltage regulation loop, but a proper design of the DSTATCOM parameters is required. During DSTATCOM operation PCC voltage will varies, therefore PCC voltage variation of 10% is also considered in the design of DSTATCOM parameters. For a given supply voltage of 230 V, the dc-link voltage is considered as 357 V $(325 + 10\%)$ and this voltage is utilized for design of dc-link capacitors and interfacing inductor.

2.2.2. Interfacing inductor (L_f). The interfacing inductor is connected in between PCC and VSI to eliminate switching frequency harmonics in the filter current. The value of interfacing inductance is calculated from below equation [27],

$$L_f = \frac{V_{dc}}{4hf_{swmax}}. \tag{2}$$

where h is hysteresis band width and f_{swmax} is maximum switching frequency. The hysteresis band value is chosen in between 5% and 15% of the rated filter current. For the above considered system (*i.e.*, $Q = 3.8$ kVAR), h value is taken as 0.8 A (5% of rated filter current). Then, the calculated interfacing inductor value from (2) is 11 mH.

In addition to the proper design of DSTATCOM parameters, the reference filter current generation and control algorithm are also important to improve the power quality. In this article, the reference filter current is obtained from single-phase equivalent synchronous reference frame theory with Enhanced Phase Locked Loop (EPLL) scheme [28] and the reference filter current is tracked by hysteresis controller. The proposed design of DSTATCOM parameters and control algorithm maintains the low dc-link voltage when compared to conventional method. Therefore, the proposed method reduces the switching losses and calculation of losses is explained here under.

The switching losses are calculated from switching frequency (f_{sw}) and energy dissipation (E_{sw}). The energy dissipation of switch is dependent on the current through switch (I_f), voltage across switch (V_{dc}) during OFF-state and junction temperature (T_j). The energy dissipation under working condition with respect to nominal test condition is obtained from below equation [29].

$$E_{sw} = E_{sw,n}\left(\frac{I_f}{I_{fn}}\right)^{k_i}\left(\frac{V_{dc}}{V_{dc,n}}\right)^{k_v}(1 + TC_{sw}(T_j - T_{jn})) \tag{3}$$

where I_{fn}, $V_{dc,n}$, T_{jn} and energy dissipation $E_{sw,n}$ are reference values at nominal test condition, by the data sheet of IGBT switch (SKM 75GB123D), k_i is the current dependency (for IGBT $\simeq$ 1, diode $\simeq$ 0.5), k_v is the voltage dependency (for IGBT $\simeq$ 1.2 or 1.4, diode $\simeq$ 0.6), TC_{sw} is the temperature coefficient of switching losses (for IGBT $\simeq$ 0.003, diode $\simeq$ 0.005). The reduction in the switching losses with the proposed method is validated with the simulation and experimental studies, discussed in next sections.

3. SIMULATION STUDIES

The simulation results for the proposed method are presented in this section. The system parameters utilized are given in Table. 2. To demonstrate the steady state and dynamic performance four load conditions are considered. The obtained simulation waveforms of source current (i_s), load current (i_l), DSTATCOM current (i_f) and dc-link voltage (V_{dc}) during load variations are shown in Figure 4. The source current becomes sinusoidal as shown in Figure 4(i), even though loads are distorted as shown in Figure 4(ii). The filter current injected by DSTATCOM are shown in Figure 4(iii). It is observed from Figure 4(iv) that, the dc-link voltage is maintained constant with voltage ripple less than 5% even under load variation.

The harmonic spectrum of the source current for maximum load condition (Load-4) before and after compensation are

System parameters	Values
Supply voltage, frequency	230 V rms, 50 Hz
Source impedance (R_s, L_s)	1 Ω, 0.1 mH
Interfacing inductance (L_f)	11 mH
capacitance (C_{dc1}, C_{dc2})	1600 μF
Load-1 ($0.2 < t < 0.3$)	42 Ω, 36 mH (DB*), 22 Ω, 12 mH (NL#)
Load-2 ($0.3 < t < 0.4$)	42 Ω, 36 mH (DB*)
Load-3 ($0.4 < t < 0.5$)	42 Ω, 36 mH (DB*), 28 Ω, 200 mH (NL#)
Load-4 ($0.5 < t < 0.6$)	10 Ω, 84 mH (DB*), 22 Ω, 12 mH (NL#)

Table 2. Simulation parameters.
*DB: Diode bridge, #NL: Nonlinear load.

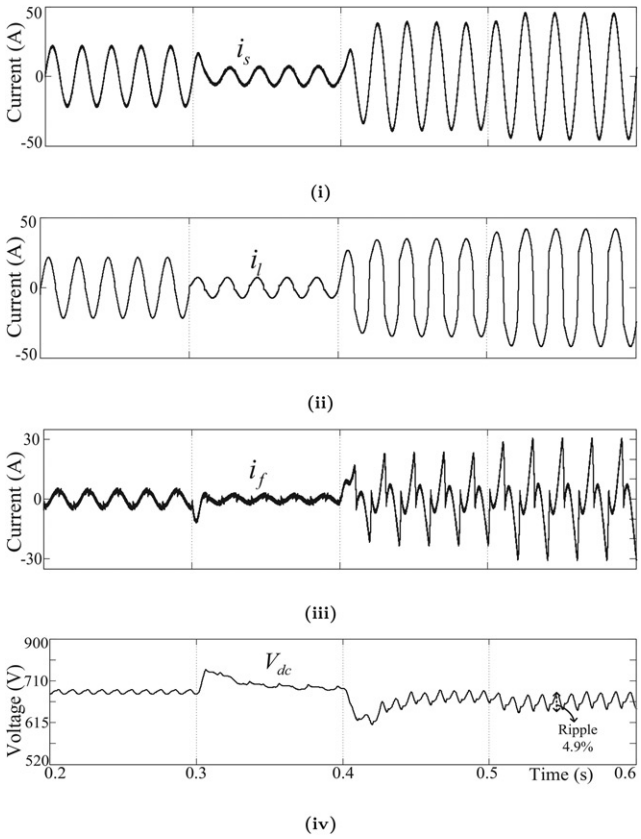

FIGURE 4. DSTATCOM performance for load variations, (i) source current (i_s), (ii) load current (i_l), (iii) DSTATCOM current (i_f) and (iv) dc-link voltage (V_{dc}).

shown in Figure 5(i) and (ii), respectively. It is observed that, the source current THD before compensation is 24.06% and after compensation is reduced to 3.62%. The %THDs of source current, before and after compensation for all load conditions are given in Table 3. It is observed that, the %THDs are reduced and within the limits of IEEE-519 standards (*i.e.*, less than 5%) after compensation.

The comparison of the proposed method with conventional methods (single capacitor VSI and split capacitor VSI) are mentioned in Table 4. The rating of VSI is reduced in the proposed method, because of lower dc-link voltage requirement. As, the dc voltage is reduced, the voltage stress across switches will be reduced and it leads to reduction of switching losses to 43.8 W in proposed method. The dc-link voltage ripple in proposed method is limited to 5% for satisfactory compensation. The reason is, for high nonlinearity loads (more than 24% THD), the ripple in the dc-link voltage is more than the allowable limit of 5%. This makes limitation on step load variations. However, in low power applications the proposed method have more advantages, like lower dc-link, less switching losses, more efficient and low cost.

4. EXPERIMENTAL STUDIES

A laboratory prototype model of a single-phase split-capacitor DSTATCOM is developed to carry out experimental studies. The specifications of the prototype are given in Table 5.

The schematic diagram of single-phase DSTATCOM is shown in Figure 6. The current drawn by load (i_l) and DSTATCOM current (i_f) are sensed by hall effect current transducers (LEM-LA55-P). The PCC voltage (v_{pcc}) is sensed by hall effect voltage transducer (LEM-LV25-P). The output of transducers is given to the DSP controller (28335) through signal conditioning circuit.

The reference current generation algorithm and hysteresis controller for gate pulses generation are implemented in DSP controller. The actual DSTATCOM current is compared with the reference filter current and the error is given to hysteresis controller. It will generate the switching pulses to gate G_1 and G_2 of switches S_1 and S_2 depending on error, respectively. The gate pulses are taken out from DSP controller and are given to driver circuit of IGBT switches through opto-isolation circuit. Based on gate pulses applied, DSTATCOM tracks the reference filter current. The experimental performance of conventional and proposed DSTATCOMs are analyzed below.

4.1. Performance Analysis with Conventional DSTATCOM

The conventional DSTATCOM waveforms are shown in Figure 7. The PCC voltage (v_{pcc}), source current (i_s), load current (i_l) and filter current (i_f) are shown in Figure 7(i). It is observed that, the source current (i_s) is sinusoidal and

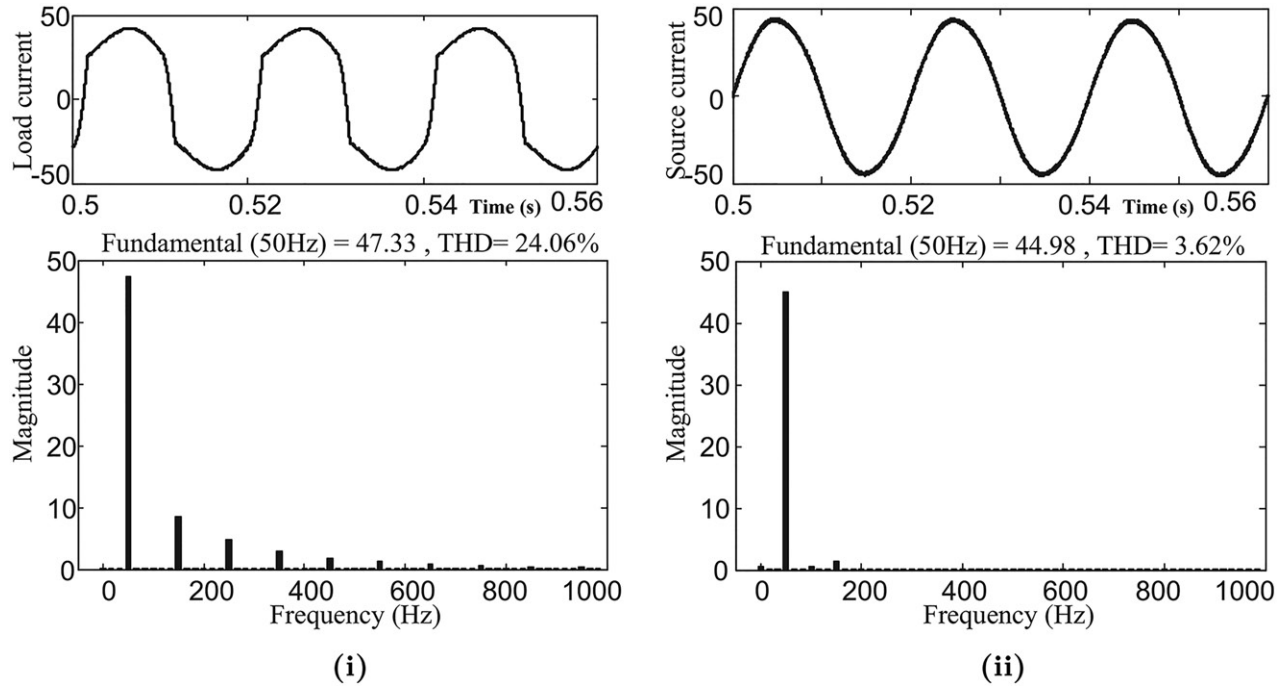

FIGURE 5. Harmonic spectrum of source current for load-4, (i) before compensation and (ii) after compensation.

Type of load	(%THD) Before compensation	(%THD) After compensation
Load-1 ($0.2 < t < 0.3$ in Figure 4)	9.2	1.79
Load-2 ($0.3 < t < 0.4$ in Figure 4)	10.9	3.6
Load-3 ($0.4 < t < 0.5$ in Figure 4)	20.7	2.09
Load-4 ($0.5 < t < 0.6$ in Figure 4)	24.06	3.62

Table 3. %THD of source current with proposed method (Simulation).

Parameters	Single capacitor VSI [25]	Split-capacitor VSI [26]	Proposed
Number of switches	4	2	2
Current sensors	2	2	2
Voltage sensors	2	3	1
DC capacitor value	4400 μF	3300 μF	1600 μF
Rated dc voltage V_{dc}	$2V_{pcc}$	$1.6V_{pcc}$	V_{pcc}
VSI rating	$2V_{pcc}{}^{*}I_f$	$1.6V_{pcc}{}^{*}I_f$	$V_{pcc}{}^{*}I_f$
Switching losses	97 W	85.2 W	43.8 W

Table 4. Comparison of the proposed method with conventional methods.

System parameters	Proposed method	Conventional method
System voltage	50 V rms	50 V rms
Supply frequency	50 Hz	50 Hz
Inductance (L_f)	2 mH	8 mH
Capacitors (C_{dc1}, C_{dc2})	1250 μF	3100 μF
Diode bridge load	10 Ω, 23 mH	10 Ω, 23 mH
RL-load	8 Ω, 16 mH	8 Ω, 16 mH

Table 5. Experimental parameters.

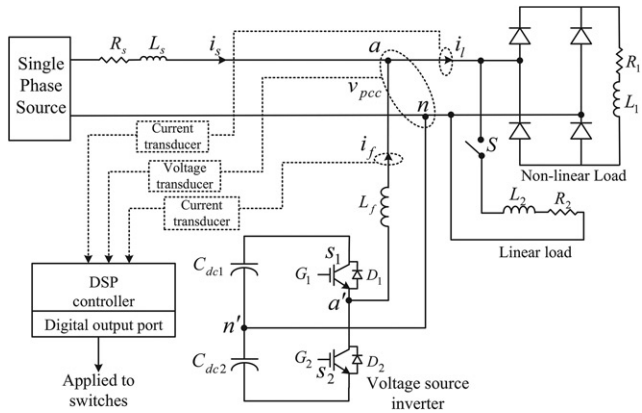

FIGURE 6. Schematic diagram of proposed single-phase DSTATCOM topology.

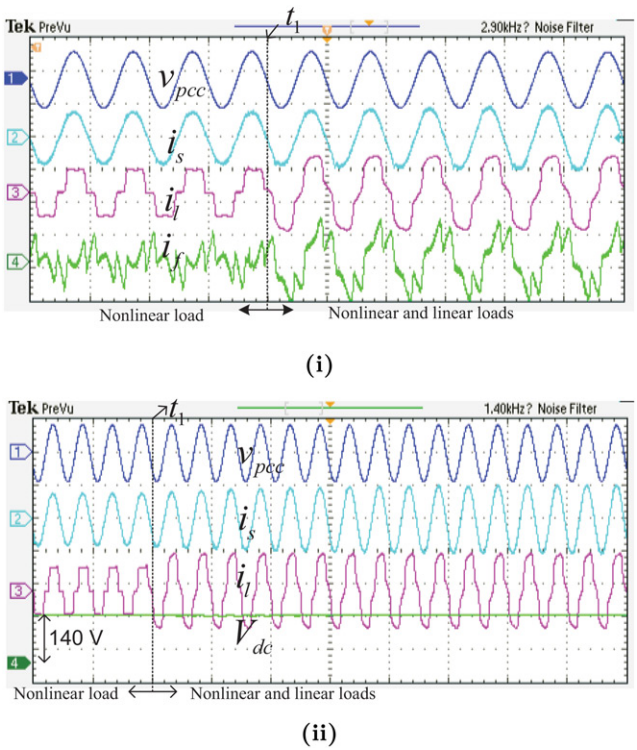

FIGURE 7. DSTATCOM performance in conventional method (i) For load variation at $t = t_1$, (ii) Dynamics of dc-link capacitor voltage (scale: voltage 100 V/div, current 4 A/div).

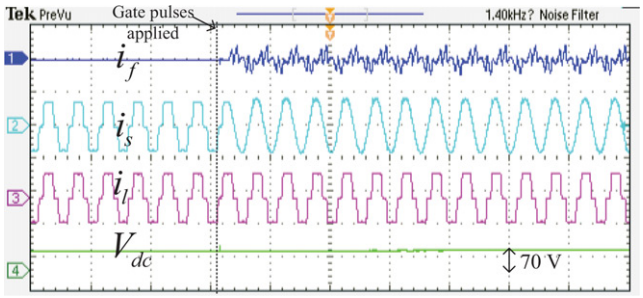

FIGURE 8. DSTATCOM performance before and after gate pulses are applied to IGBT switches with proposed DSTATCOM (scale: voltage 100 V/div, current 4 A/div). (Case-A).

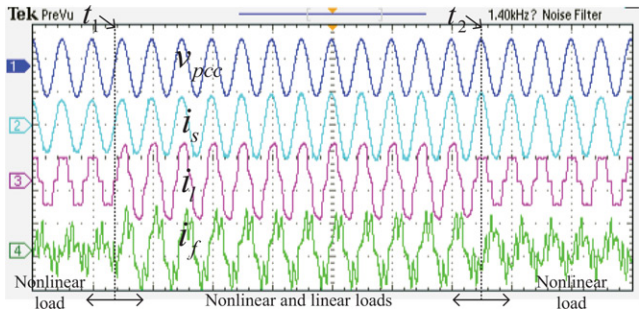

FIGURE 9. DSTATCOM performance for load variations at time t_1 and t_2 with proposed DSTATCOM (scale: voltage 100 V/div, current 4 A/div). (Case-B).

in-phase with PCC voltage (v_{pcc}). Even though load is varied at $t = t_1$, the source current is sinusoidal and in-phase with PCC voltage.

The PCC voltage (v_{pcc}), source current (i_s), load current (i_l) and dc-link voltage (V_{dc}) are shown in Figure 7(ii). The reference dc voltage in conventional method is twice the peak of PCC voltage (*i.e.*, 140 V for supply voltage of 50 V). Therefore, the dc-link capacitor is charged to reference voltage as shown in Figure 7(ii). The load is increased at $t = t_1$, then also the dc-link capacitor voltage maintained constant, because the voltage regulation loop always forced the dc-link voltage to reference value.

4.2. Performance Analysis with Proposed DSTATCOM

The DSTATCOM performance, when the source is connected to a diode bridge harmonic generating load (non-linear) and linear load is analyzed experimentally for three different cases here.

4.2.1. Case A: DSTATCOM performance before and after gate pulses are applied. The filter current (i_f), load current (i_l), source current (i_s) and dc-link voltage (V_{dc}) without and with gate pulses are shown in Figure 8. It is observed that before gate pulses are applied, the DSTATCOM will not injects any compensating current therefore the source current is not compensated charged to peak of PCC voltage (*i.e.*, 70 V) through an anti-parallel diodes of IGBT switches. Once gate pulses are enabled, the DSTATCOM injects filter current such that the source current (i_s) becomes sinusoidal. During the compensation, the dc-link capacitor voltage is maintained same as that of before gate pulses applied (*i.e.*, peak of PCC voltage).

4.2.2. Case B: DSTATCOM performance for load variations. The PCC voltage (v_{pcc}), source current (i_s), load current (i_l) and filter current (i_f) for load variations at t_1 and t_2 are shown in Figure 9. The load is increased at t_1 and decreased at t_2. It is observed that the source current is harmonics free and sinusoidal. It shows that, the proposed DSTATCOM can able to compensate the harmonic and reactive component currents even under load variations also.

4.2.3. Case C: Dynamic responses of dc-link capacitor voltages for load variations. The PCC voltage (v_{pcc}), source current (i_s), load current (i_l) and dc-link voltage (V_{dc}) are shown in Figure 10. The dc-link voltage (V_{dc}) decreases at the instant of load is increased at t_1. However, the dc-link capacitor charged to peak of PCC voltage through an anti-parallel diodes and maintained that voltage in steady state.

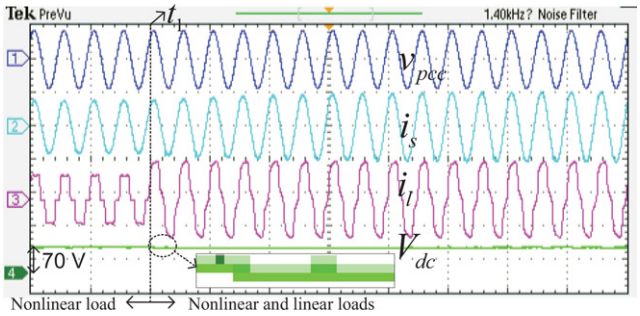

FIGURE 10. Dynamic responses of dc capacitor voltage for load variations (scale: voltage 100 V/div, current 4 A/div). (Case-C).

The harmonic spectrum of source current before and after compensation for load-1 and load-2 are show in Figure 11. It is observed from Figure 11(i), that for load-1 the THDs of source current is reduced from 23.4% (before compensation) to 3.7% (after compensation). It is observed from Figure 11(ii), that for load-2 the THDs of source current is reduced from 14.4% (before compensation) to 2.8% (after compensation). The THDs of source current for load-1 and load-2 are given in Table 6. In both load conditions the source current THDs are within specified limit (below 5% according to IEEE-519 standards).

4.2.4. Case D: Performance analysis of proposed method with agriculture pump-set load.. A single-phase motor is considered as agriculture pump-set load of rating 230 V, 10 A, 2 HP and 0.707 pf. The pump-set load consumes

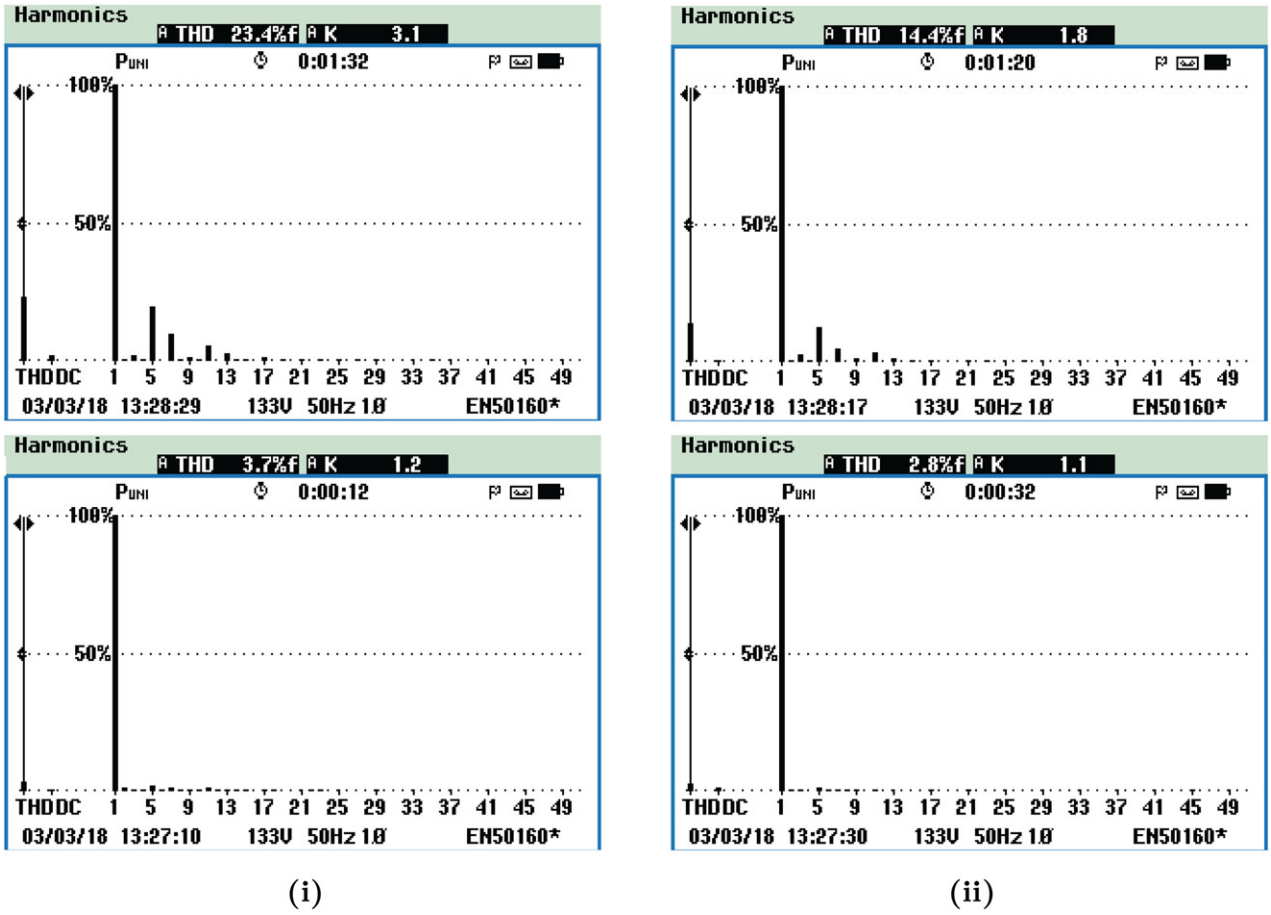

FIGURE 11. Harmonic spectrum of source current before compensation and after compensation during (i) load-1 and (ii) load-2.

Type of load	(%THD) Before compensation	(%THD) After compensation
Load-1 (up to t_1 in Figure 9)	23.4	3.7
Load-2 (from t_1 to t_2 in Figure 9)	14.4	2.8

Table 6. %THD of source current with proposed method (Experimental).

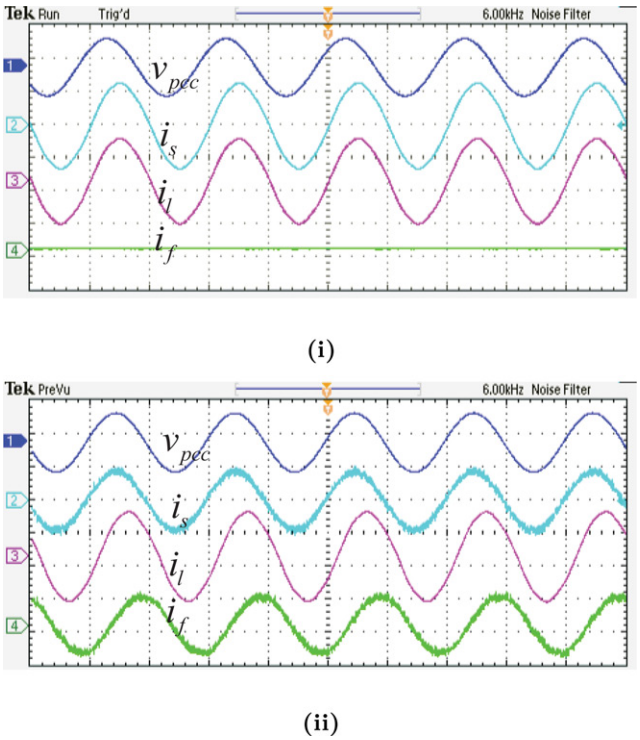

FIGURE 12. Experimental waveforms for agriculture pump-set type load (i) without operating DSTATCOM and (ii) with operating DSTATCOM (scale: voltage 400 V/div, current 8 A/div).

reactive power, if it is supplied by DSTATCOM, then the grid side power factor becomes unity.

The source voltage (v_{pcc}), source current (i_s), current draw by pump-set load (i_l) and filter current when DSTATCOM is not operated are shown in Figure 12(i). It is observed that, DSTATCOM is not injecting any current, then the source current lags PCC voltage. During DSTATCOM operation, the results are shown in Figure 12(ii). The source current becomes in-phase with PCC voltage because the reactive power required for pump-set load is supplied by DSTATCOM. The phasor diagram of source

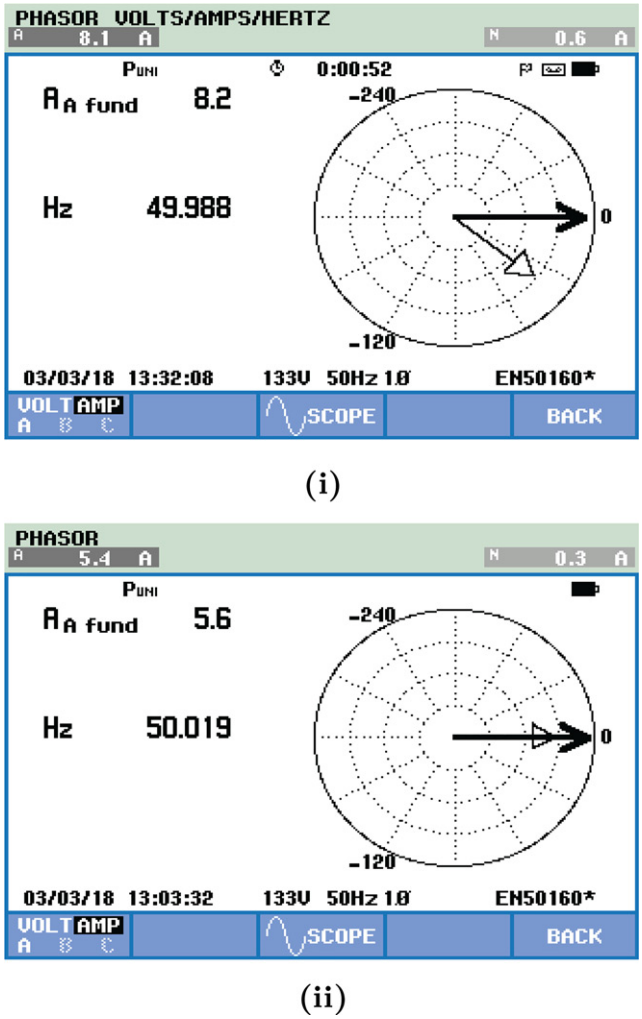

FIGURE 13. Phasor diagram of source current (i) before compensation (ii) after compensation.

current before and after compensation are shown in Figure 13(i) and (ii), respectively. It is observed that, the current lags voltage by 36° and the fundamental current magnitude is 8.2 A before compensation. After compensation, the source current is in-phase with voltage and fundamental current is 5.6 A. The reason for reduction in fundamental source current magnitude is that the required reactive component current is injected by DSTATCOM.

The cost comparison between conventional and proposed DSTATCOM system are given in Table. 7. It is observed that, the total cost required for proposed DSTATCOM system is Rs. 25,390, which is less when compared to conventional DSTATCOM system cost of Rs. 40,560. In low power applications, the proposed DSTATCOM system is more preferable in terms of cost reduction without effecting compensation performance.

Parameters	Conventional		Proposed	
	Quantity	Cost	Quantity	Cost
Current sensors (LA-55P)	2	1650	2	1650
Voltage sensors (LV-25P)	3	19530	1	6510
Inductor (0–10 mH)	1	2130	1	2130
DC capacitor	2	2600 (2800 μF)	2	1000 (1200 μF)
IGBT switches (Semikron)	2	5650 (SKM50GB12T4)	2	4900 (SKM50GB063D)
Dedicated DSP controller (28335)	1	9000	1	9000
Total cost		Rs. 40,560		Rs. 25,390

Table 7. Cost comparison between conventional and proposed DSTATCOMs.

5. CONCLUSION

The simulation and experimental results demonstrate the effectiveness of the proposed single-phase DSTATCOM. The advantages of proposed method are,

1. The voltage measuring sensors are reduced without effecting the reactive power compensation and the source current harmonic mitigation.
2. It has been observed from experimental results, that the dc-link voltage required is less when compared to conventional method.
3. The switching losses are reduced and required rating of the DSTATCOM is low, therefore cost is reduced.
4. The proposed method is more suitable for constant load application, like agriculture pump-set load connected to grid.

The proposed method in this article has more scope to use in solar application. In which, the solar PV is connected across dc-link of the voltage source inverter such that real power injection is also possible.

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