IET Generation, Transmission & Distribution

Research Article

IET Journals
The Institution of Engineering and Technology

Three-phase four switch DSTATCOM topologies with special transformers for neutral current compensation and power quality improvement

ISSN 1751-8687
Received on 8th January 2018
Revised 9th June 2018
Accepted on 18th October 2018
E-First on 9th January 2019
doi: 10.1049/iet-gtd.2018.5841
www.ietdl.org

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Abstract: Three-phase four switch (TPFS) inverters are an effective solution to reduce the size and cost of the distribution STATic COMpensator (DSTATCOM). The performance of TPFS inverter is identical to three-phase four leg, three-phase split capacitor inverter topologies during balanced load conditions. During unbalanced load conditions, the absence of the neutral wire in TPFS topologies does not allow the DSTATCOM to compensate the unbalance in load currents. To overcome this limitation, a special purpose transformer is connected across the load along with the DSTATCOM. This special transformer provides a path for neutral current, reduces the cost and rating of the inverter, improve the performance under stringent unbalanced currents generated by computer loads and also improves short duration overloading capability. In the proposed work, two different TPFS topologies namely four switch one capacitor and four switch split capacitor are proposed along with two special purpose transformers which include zigzag and T-connected for three-phase four-wire distribution systems. The combination of TPFS inverter and special transformer can achieve power factor improvement, harmonic elimination, neutral current compensation and load balancing. The evaluation of the proposed method has done using simulation and experimental investigations.

1 Introduction

In recent years, the continuous proliferation of non-linear loads for domestic and industrial purposes, is leading to various power quality problems. Sometimes, these non-linear loads are also single-phase with distinct ratings. These unbalanced and non-linear loads in the distribution system, cause current related power quality problems such as harmonic currents, reactive power burden, excessive neutral currents and load unbalance. Distribution STATic COMpensator (DSTATCOM) is the requisite solution to compensate the current related power quality problems [1]. There are many DSTATCOM topologies presented in the literature [2–4]. Among them, three-phase four leg (TPFL) and three-phase split capacitor (TPSC) topologies occupied the dominant position because of their simple structure [5–9]. These DSTATCOM topologies are used to control reactive power, harmonic currents, load balancing. However, the usage of an excess number of power electronic switches in these topologies makes the system expensive [10]. In the literature, to reduce the cost and size, TPFL and TPSC inverters are replaced with three-phase four switch (TPFS) inverters [11, 12]. The available TPFS topologies are four-switch split capacitor (FSSC) topology [10] and four-switch one capacitor (FSOC) topology [13]. In these two topologies four switches are formed as two legs of the DSTATCOM and they are connected to two phases at the point of common coupling (PCC), whereas the third phase is connected to the mid-point of the dc link in FSSC topology and in the case of FSOC topology it is connected to the negative terminal of the dc link. In the FSOC topology, the direct connection between supply and negative terminal of the capacitor will shift the voltage at PCC. Therefore, the third phase is connected through a passive filter tuned to dominant harmonics (usually fifth and seventh) in load current. This helps to enable coupling between supply and negative terminal of the dc bus. The design for fifth and seventh order harmonic passive filters is given in [14–16]. In these two topologies, the third phase will be automatically controlled by controlling the two phases [10, 13].

In a distribution system, most of the loads are single-phase, non-linear with unequal ratings. These unbalanced load currents are leading to unnecessary neutral currents and harmonic losses in the system. The non-linear currents drawn by computer loads will generate a high amount of neutral current even though the phases are balanced [17]. Sometimes, the value of neutral current is more than the load current and it makes severe damage to the distribution system. A survey was conducted to evaluate the effects of excessive neutral current which is presented in [17, 18]. To compensate the neutral current, several techniques are proposed in the literature such as synchronous machines, passive filters, special transformers and three-phase four-wire (3P4W) DSTATCOM or active power filters (APFs) [19]. The high maintenance and initial cost of the synchronous machine are limiting it, not to use in all applications. Even though the passive filters are simple to use they are expensive and occupies more space. In four-leg DSTATCOM topologies, the neutral wire is connected to an extra leg and the switches in this leg are controlled to compensate the neutral current. The connection of an extra leg will increase the number of power electronic devices, which increases the size, cost and control circuitry [20]. In split capacitor DSTATCOM topology, neutral wire is connected to the midpoint of two capacitors. A large amount of load unbalance increases the difference between the voltages across the two capacitors which further affects the overall performance of the compensator [21]. In [20, 22] special transformer based DSTATCOM topologies are presented to reduce the overall rating of the DSTATCOM. However, these topologies are complex and require more number of switching devices. On the other hand, the absence of neutral wire in TPFS topologies does not allow the DSTATCOM to compensate the neutral current created by the harmonic and unbalanced loads.

Therefore, in this paper, four different DSTATCOM topologies are proposed by combining FSSC or FSOC inverter configuration with a zigzag or T-connected transformer. FSSC or FSOC inverter configuration is responsible for the compensation of phase-current harmonics, reactive power produced by the load, also reduces the number of power devices and cost. The zigzag or T-connected transformer is designed and connected in such a way that, it circulates the neutral current between load and transformer so that neutral currents flowing through the source will be nullified [23–26]. The combination of these four switch topologies with special

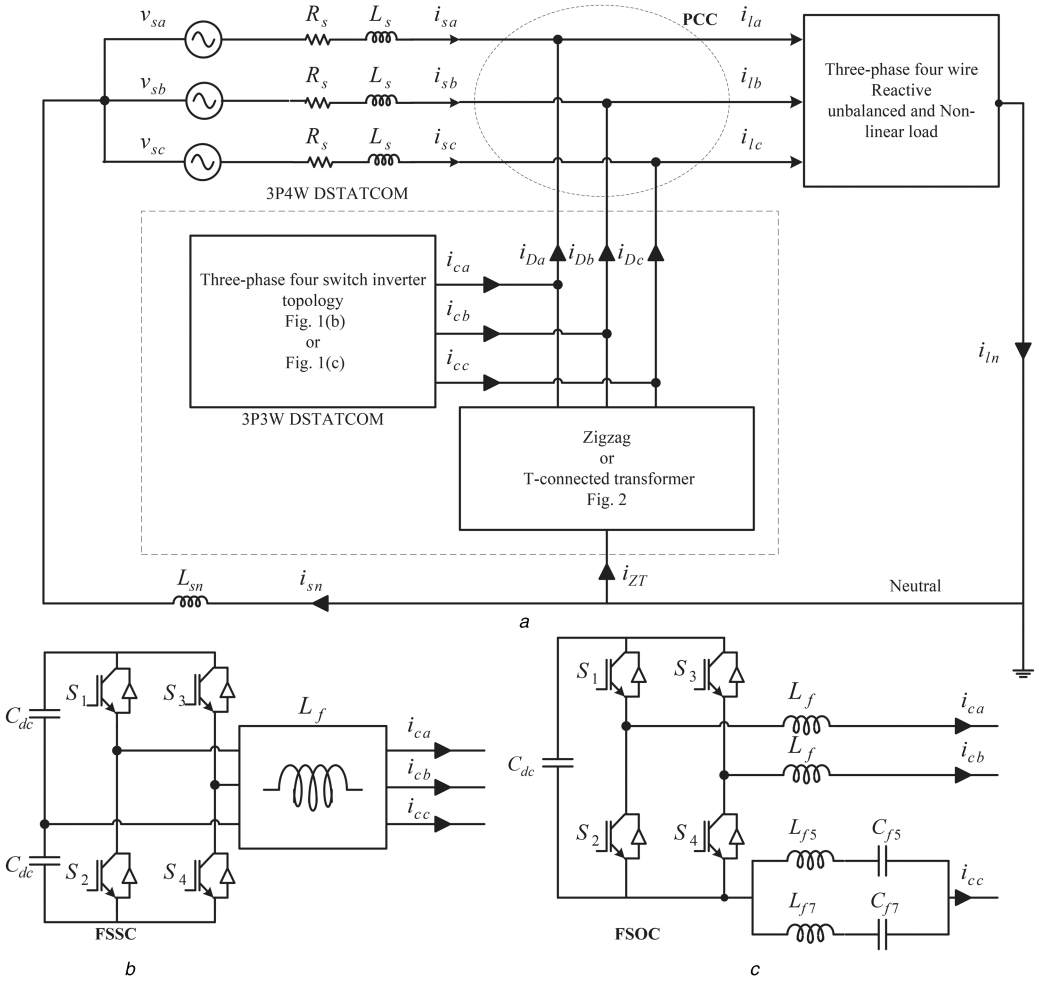

Fig. 1 *Schematic diagram of TPFS DSATCOM connected distribution system*

transformer can achieve three-phase balanced sinusoidal source currents with unity power factor during balanced and unbalanced load conditions. The other advantages of this combination are a reduction in complexity, reduction in rating of four switch inverter, the overall cost of the inverter, improved performance under stringent unbalanced currents generated by computer loads and capable to meet short duration overload conditions.

In order to verify the efficacy of the proposed DSTATCOM topologies simulation and experimental studies are carried out. To control the FSSC or FSOC inverter configuration, Instantaneous Symmetrical Component Theory (ISCT) is used [27–29]. In experimental studies, the control algorithm is implemented in the dSPACE Micro LabBox 1202 controller. Further, a complete comprehensive comparison is incorporated with 3P4W DSTATCOM topologies presented in the literature.

This paper is organised as follows. The configuration of TPFS topologies and special transformers with required design considerations are explained in Section 2. ISCT control algorithm is explained in Section 3. Neutral current compensation using a special transformer is explained in Section 4. Simulation studies and experimental investigations are analysed in Sections 5 and 6. Finally, Section 7 summarises the proposed work.

2 Configuration of TPFS topologies with special transformers

The schematic diagram of TPFS DSTATCOM connected to a three-phase distribution system is shown in Fig. 1. Design of various parameters of DSTATCOM is mentioned in the literature [2, 3, 8]. The minimum dc-bus voltage of DSTATCOM is 1.6–2 times of peak value of phase voltage [8]. In this paper for optimal performance, dc-link voltage is considered as two times of the peak of phase voltage [2, 3]

$$V_{\mathrm{dc}} = \frac{2\sqrt{2}V_l}{\sqrt{3}m} \tag{1}$$

where V_l is the line voltage and m is the modulation index usually the value of m is considered as a unity. In this work, for simulation studies, the supply voltage is considered as 415 V. Using the above formula V_{dc} is equal to 677.6 V and is selected as 700 V. In a similar way for split capacitor topology $V_{\mathrm{dc1}} = V_{\mathrm{dc2}} = 700$ V. In experimentation supply voltage is considered as 50 V. Using (1) V_{dc} is equal to 81.54 V and it is chosen as 100 V for FSOC and $V_{\mathrm{dc1}} = V_{\mathrm{dc2}} = 100$ V for FSSC. The output of the DSTATCOM is connected at PCC through an interfacing inductor, which eliminates ripples in the compensating current. Here, a non-linear and unbalanced load is connected to the distribution system through the feeder impedance. A zigzag or T-connected transformer is connected across the load terminals to compensate neutral current created by the unbalanced loads.

2.1 FSSC topology

FSSC inverter topology shown in Fig. 1*b* is formed by eliminating one leg from existing split capacitor topology, so that, cost and size of the DSTATCOM are reduced. The midpoint of two capacitors is connected to the third phase at PCC for proper compensation. By controlling the two legs of this inverter the third phase will be automatically controlled for required compensation. However, the dc-link voltage is almost two times than the conventional three-leg voltage source inverter. Cost and complexity of the inverter are reduced compared to TPSC topology because of the lesser number of switches.

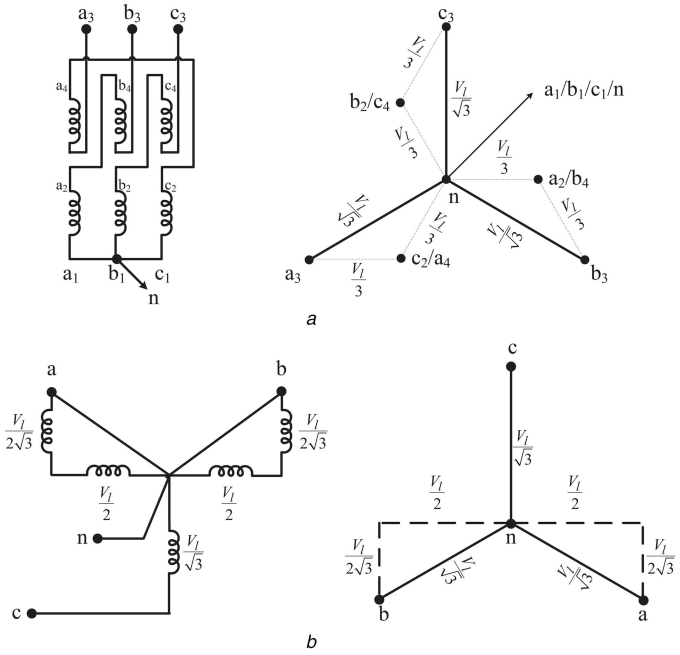

Fig. 2 *Connection diagram and phasor diagram of a zigzag and T-connected transformer*
(a) Zigzag transformer, ***(b)*** T-Connected transformer

2.2 FSOC topology

In FSOC topology shown in Fig. 1*c*, the third phase is connected to the negative terminal of the dc bus. Because of the direct connection, there is an offset added to the third phase voltage. To rectify this, a passive filter is connected between PCC and inverter terminals. This passive filter is used to maintain the rated terminal voltage and to provide harmonic and reactive power to the distribution system. The values of inductor and capacitor of the passive filter depend upon the load harmonic content. Therefore, these are designed to eliminate most dominant fifth and seventh order harmonics in addition with reactive power support and to improve voltage profile. In general, a large value of the capacitor will make the filter bulky and small value of the inductor will not compensate the ripples in the filter current [11].

2.3 Zigzag transformer

The zigzag transformer is a special type of transformer used to provide a neutral point, which allows the flow of neutral and zero-sequence currents developed by the non-linear and unbalanced loads in the three-phase distribution system. Three single-phase transformers with turns ratio 1:1 are connected in a zigzag manner to engender a three-phase zigzag transformer. The connection diagram and the phasor diagram of a three-phase zigzag transformer are shown in Fig. 2*a*. The voltages of the primary and secondary winding's of the three identical single-phase transformers are considered as 1/3 times of the rated PCC line-to-line voltage to make the equal rated voltage at the terminal of the zigzag transformer and PCC. The amount of current flowing through the windings of the three transformers is always equal because of equal voltage and power ratings and the value of neutral current is (I_n/3). From the above voltages and currents, the rating of the zigzag transformer is given as

$$\mathrm{kVA}_{\mathrm{Zigzag}} = 3 \times \left(\frac{V_l}{3}\right) \times \left(\frac{I_n}{3}\right) = \frac{V_l \times I_n}{3} \tag{2}$$

2.4 T-connected transformer

The T-connected transformer is a special type of transformer formed by using a single-phase two winding transformer and a single-phase three winding transformer, which is used to compensate the neutral current in the three-phase distribution system. A zigzag transformer can be replaced with a T-connected transformer having almost similar kVA rating, to further reduce the cost and space occupied. The connection diagram and the phasor diagram are shown in Fig. 2*b*. The ratio between the voltages of primary and secondary windings of the three winding and two winding transformers are given as $(V_l/\sqrt{3}):(V_l/2\sqrt{3}):(V_l/2\sqrt{3})$ and $(V_l/2):(V_l/2)$, respectively [23], where V_l is the line-to-line voltage. The given voltage ratings of the single-phase transformers will make the rated voltage of the T-connected transformer and PCC equal which is shown by the phasor diagram in Fig. 2*b*. The kVA rating of the T-connected transformer is given as

$$\mathrm{kVA}_{\mathrm{T-Connected}} = \left(\frac{V_l}{\sqrt{3}} \times \frac{I_n}{3} + \frac{V_l}{2} \times \frac{I_n}{3}\right) = \left(\frac{1}{3\sqrt{3}} + \frac{1}{6}\right) V_l I_n \tag{3}$$

In the proposed work, four DSTATCOM configurations are formed by connecting FSSC or FSSC inverter topology with zigzag or T-connected transformer.

3 Instantaneous symmetrical component theory (ISCT)

ISCT with hysteresis controller is used here to generate the gate pulses for both FSOC, FSSC topologies [25]. Here, by controlling two phases, the third phase will be automatically controlled [9, 11]. The block diagram for the control algorithm is shown in Fig. 3. Initially, PCC voltages and load currents are sensed to calculate the instantaneous load power demand. The equation to calculate load power is given as

$$p_l = v_{sa} i_{la} + v_{sb} i_{lb} + v_{sc} i_{lc} \tag{4}$$

Instantaneous load power in (4) is the sum of a DC component power ($p_{l\mathrm{dc}}$) and oscillating AC component power ($p_{l\mathrm{ac}}$). The sum of $p_{l\mathrm{dc}}$ and power (p_{loss}) required to maintain a constant voltage across the dc link should be the total active power supplied by the source for harmonic less source current with unity power factor operation. Usually, instantaneous load power is passed through a low-pass filter to extract the average load power demand ($p_{l\mathrm{dc}}$). The difference between the measured and actual dc-link voltage is given to a PI controller to estimate the power required by the DSTATCOM to maintain the constant dc-link voltage

$$p_{\mathrm{loss}} = K_{\mathrm{p}}(V_{\mathrm{dc}}^{*} - V_{\mathrm{dc}}) + K_{\mathrm{i}} \times \int (V_{\mathrm{dc}}^{*} - V_{\mathrm{dc}}) \tag{5}$$

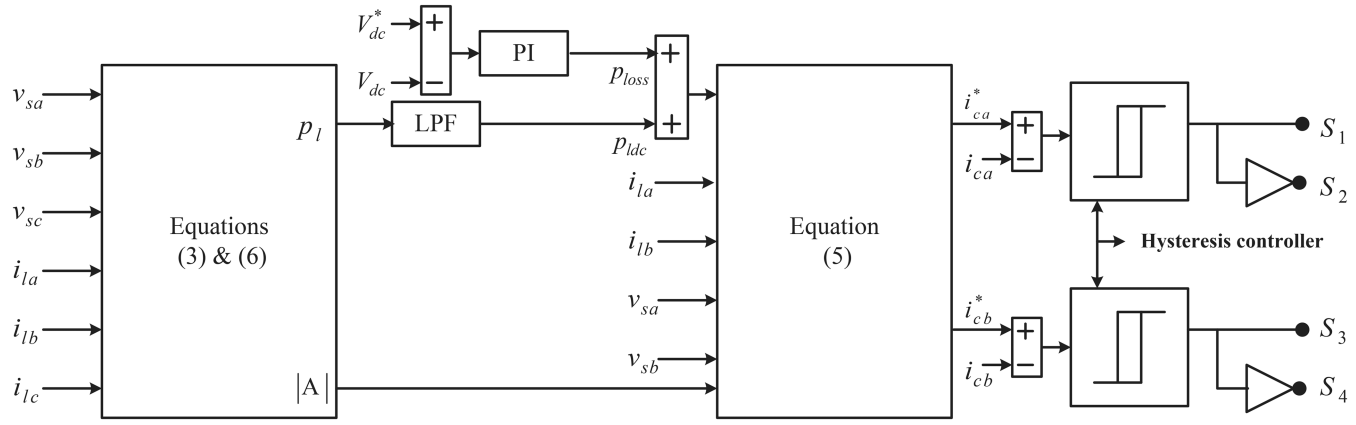

Fig. 3 *Generation of gate pulses using ISCT*

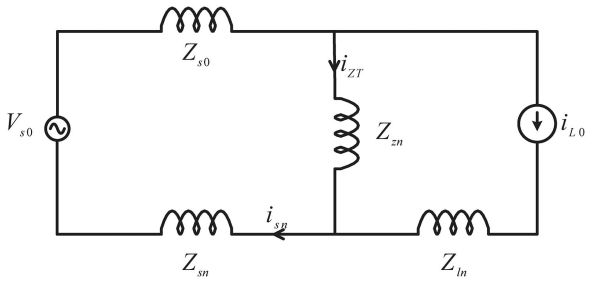

Fig. 4 *Zero sequence equivalent circuit of the special transformer connected distribution system*

After estimating the active power supplied by the source the reference filter currents will be given as

$$\begin{aligned} i_{ca}^* &= i_{la} - \frac{v_{sa} + \beta(v_{sb} - v_{sc})}{|A|} \times (p_{ldc} + p_{loss}) \\ i_{cb}^* &= i_{lb} - \frac{v_{sb} + \beta(v_{sc} - v_{sa})}{|A|} \times (p_{ldc} + p_{loss}) \end{aligned} \tag{6}$$

where $|A|$ is expressed as

$$|A| = v_{sa}^2 + v_{sb}^2 + v_{sc}^2$$

The angle β is defined as

$$\beta = \frac{\tan\theta}{\sqrt{3}}$$

where θ is the angular difference between PCC voltage and supply fundamental current. The amplitude of PCC voltage is given as

$$V_t = \sqrt{\frac{2}{3}\left(v_{sa}^2 + v_{sb}^2 + v_{sc}^2\right)} \tag{7}$$

The difference between measured and desired amplitude of PCC voltage is passed through a PI controller to estimate β. To maintain the unity power factor operation at PCC the value of β should be zero. The difference between reference compensator current and actual compensator current is given to a hysteresis controller to generate the gate pulses for the DSTATCOM operation.

4 Neutral current compensation using zigzag or T-connected transformer

The zero sequence equivalent circuit of the special transformer connected distribution system is shown in Fig. 4. There are two sources for zero sequence current, one is zero sequence voltage source (V_{s0}) which is because of unbalance in the supply voltage and the other is zero sequence current source (i_{L0}) which is because of unbalance and harmonics in load current. In the proposed work, the supply voltage is considered as balanced and sinusoidal. Therefore (V_{s0}) is taken as zero. In Fig. 4, Z_{s0} represents the feeder impedance, Z_{sn} represents the impedance between the supply and neutral, Z_{ln} is the impedance between load and neutral and Z_{tn} is the impedance offered by the special transformer. The neutral current flowing through the source is calculated using current division rule and it is given below:

$$i_{sn} = \frac{Z_{tn}}{Z_{sn} + Z_{s0} + Z_{tn}} i_{L0} \tag{8}$$

From the above equation, to minimise the current flowing through the source the impedance offered by the transformer (Z_{tn}) should be as less as possible.

5 Simulation studies

In this section, the simulation results of proposed four DSTATCOM configurations with two different load conditions are discussed and also they are compared with existing three-phase four leg topology and three-phase split capacitor topology in terms of various components, cost and kVA rating. The parameters used in simulation studies are given in Table 1. DSTATCOM is connected to the distribution system at 0.1 s, during this period, the initial capacitor voltage is considered as 90% rated voltage. During 0–0.35 s the three-phase diode bridge rectifier is connected to the PCC as a balanced load and a single-phase diode bridge rectifier is connected to phase 'a' only, which make load as unbalanced and it is considered as load-1. At 0.35 s a single phase diode bridge rectifier load is added to the existing load on phase 'b' and it is considered as load-2. These non-linear and unbalanced loads are collectively compensated by inverter topology and transformer. Here, the inverter will inject required harmonic and reactive currents so that the source currents will be sinusoidal and they are in phase with the voltages at PCC. To compensate neutral current because of load unbalance, a special transformer connected at PCC provide a low impedance path so that source neutral current is nullified which indicates the source currents are balanced. In simulation studies, inverter and special transformer are turned on at 0.1 s for all the four configurations.

Table 1 System configuration

Parameters	Values
supply voltage (V_l)	415 V (line-line)
feeder impedance (Z_s)	(0.7 + 0.942j) Ω
ac load inductor (L_{ac})	3 mH
ripple filter (R_f, C_f)	10 Ω, 10 μF
neutral impedance (L_{sn})	1 mH
filter inductor (L_5, L_7)	8 mH, 4 mH
filter capacitor (C_5, C_7)	50 μF, 50 μF
FSSC topology (V_{dc}, C_{dc})	1400 V, 4700 μF
FSOC topology (V_{dc}, C_{dc})	700 V, 4700 μF
zigzag transformer	three-single phase transformers of voltage rating 150/150 V with 3 kVA power rating
t-connected transformer	one single-phase three-winding transformer of voltage rating 240/120/120 V, and one single-phase two-winding transformer of voltage rating 208/208 V with power rating of 5 kVA each
load	three-phase diode bridge rectifier with 20 Ω, 150 μF
	two single-phase full bridge rectifiers one is connected to 'a' phase with 4 Ω, 100 μF, and the other is connected to 'b' phase at 0.6 s with 8 Ω, 200 μF
	—

5.1 Performance of FSOC with zigzag transformer

Fig. 5*a* shows the performance of FSOC inverter topology with a zigzag transformer as DSTATCOM. In this figure unbalanced and non-linear load currents, voltages at PCC, balanced sinusoidal source currents, filter currents, neutral currents of load and source and variation of dc-link voltage during load change are shown. The rms values of source currents during load-1 without compensation are 72.19, 17.84 and 19.73 A and the THDs are 8.43, 47.05, 53.47% for three phases, respectively. After connecting the DSTATCOM, rms values of the source currents are changed to 35.92, 36.14 and 36.22 A, respectively, which indicates that the source currents are balanced, similarly, THD's are reduced to 1.36,1.51, 1.51% which are well within the limits of IEEE standards. Similarly, rms values and THD's for load-2 are mentioned in Tables 2 and 3. The unbalanced load currents are leading to a load neutral current of 52.91 A during load-1 and 51.83 A during load-2 but the source neutral current is almost zero because the entire load neutral current is flowing through the transformer.

5.2 Performance of FSOC with T-connected transformer

The performance of FSOC with T-connected transformer is similar to FSOC with a zigzag transformer. However, the only change is the number of single-phase transformers required to implement a zigzag transformer is three whereas only two transformers are enough to implement a T-connected transformer. Fig. 5*b* presents the performance of FSOC with a T-connected transformer. During load-1, rms values of the source currents after compensation are 35.86, 36.07, 35.84 A which indicates the source currents are balanced and the THD's are lowered to 1.40, 1.55 and 1.63% which indicates they are well within the IEEE standards. During load-2 rms values of the source currents before compensation are 70.82, 44.90, 18.64 with THD's 9.47, 18.62, 49.36%. After compensation, source currents are modified to 44.36, 44.43, 44.39 A with THD's 1.14, 1.20, 1.17%. Load neutral currents during load-1 and load-2 are 52.91 and 51.85 A but the source neutral current is almost zero which is shown in Fig. 5*b*.

5.3 Performance of FSSC with zigzag transformer

In this DSTATCOM configuration, TPSC inverter topology is replaced with FSSC topology by eliminating two switches and the neutral current is compensated by connecting a zigzag transformer across the load terminals. The performance FSSC inverter along with a zigzag transformer is shown in Fig. 6*a*, in this figure, unbalanced load currents, PCC voltages, balanced source currents, filter currents, neutral currents and variation of dc-link voltage during both the load conditions are presented. The RMS values of balanced source currents during load-1 are 35.42, 35.99, 35.66 A with THD's 2.84, 2.86, 2.38%. During load-2, they are modified to 43.99, 44.29 and 44.08 A and THD's are scale down to 2.28, 2.24 and 1.82%. During 0–0.1 s, DSTATCOM and transformer are not connected to the distribution system so that the source neutral current is the same as load neutral current which is shown in Fig. 6*a*. During load-1, the load neutral current is 52.84 A similarly during load-2 it is 51.67 A but in these two load conditions source, neutral currents is almost zero.

5.4 Performance of FSSC with T-connected transformer

The performance of FSSC inverter topology with T-connected transformer is presented in Fig. 6*b*. RMS values of load currents during load-1 are 71.90, 17.87 and 19.76 A which shows they are unbalanced, but the rms values of source currents are 35.32, 35.85 A and 35.68 which indicates they are balanced. The THD's of source currents during load-1 are 2.84, 2.90 and 2.89%. The rms values of balanced source currents during load-2 are 43.88, 44.26 and 45.19 A and the THD's are 2.32, 2.30 and 2.20% for *a*, *b* and *c* phases, respectively.

5.5 Comparison of proposed topologies

In general, KVA rating of the TPFL or TPSC inverter is calculated using the below mentioned formula:

$$S = V_s(|i_{ca}| + |i_{cb}| + |i_{cc}| + |i_{cn}|), \tag{9}$$

rating of the four switch inverter with zigzag transformer is calculated as

$$S = V_s(|i_{ca}| + |i_{cb}| + |i_{cc}|) + \left(\frac{V_l \times I_n}{3}\right) \tag{10}$$

similarly, the rating of the four switch inverter with T-connected transformer is calculated as

$$S = V_s(|i_{ca}| + |i_{cb}| + |i_{cc}|) + \left(\frac{1}{3\sqrt{3}} + \frac{1}{6}\right)V_l I_n\,. \tag{11}$$

The rms values of filter currents for all the topologies are clearly mentioned in Table 2. Using this filter current, the kVA rating of the TPFL and TPSC topologies is calculated and it is given as 30 kVA during load-1 and 25 kVA during load-2. However, the kVA rating of the proposed configurations is 21 kVA for load-1 and 17 kVA for load-2. From the above values, it is observed that the kVA rating of the proposed DSTATCOM configurations is significantly less compared to the TPFL and TPSC topologies. Table 2 also shows the rms values of source currents before and after compensation, filter currents and rating of the inverter. From this

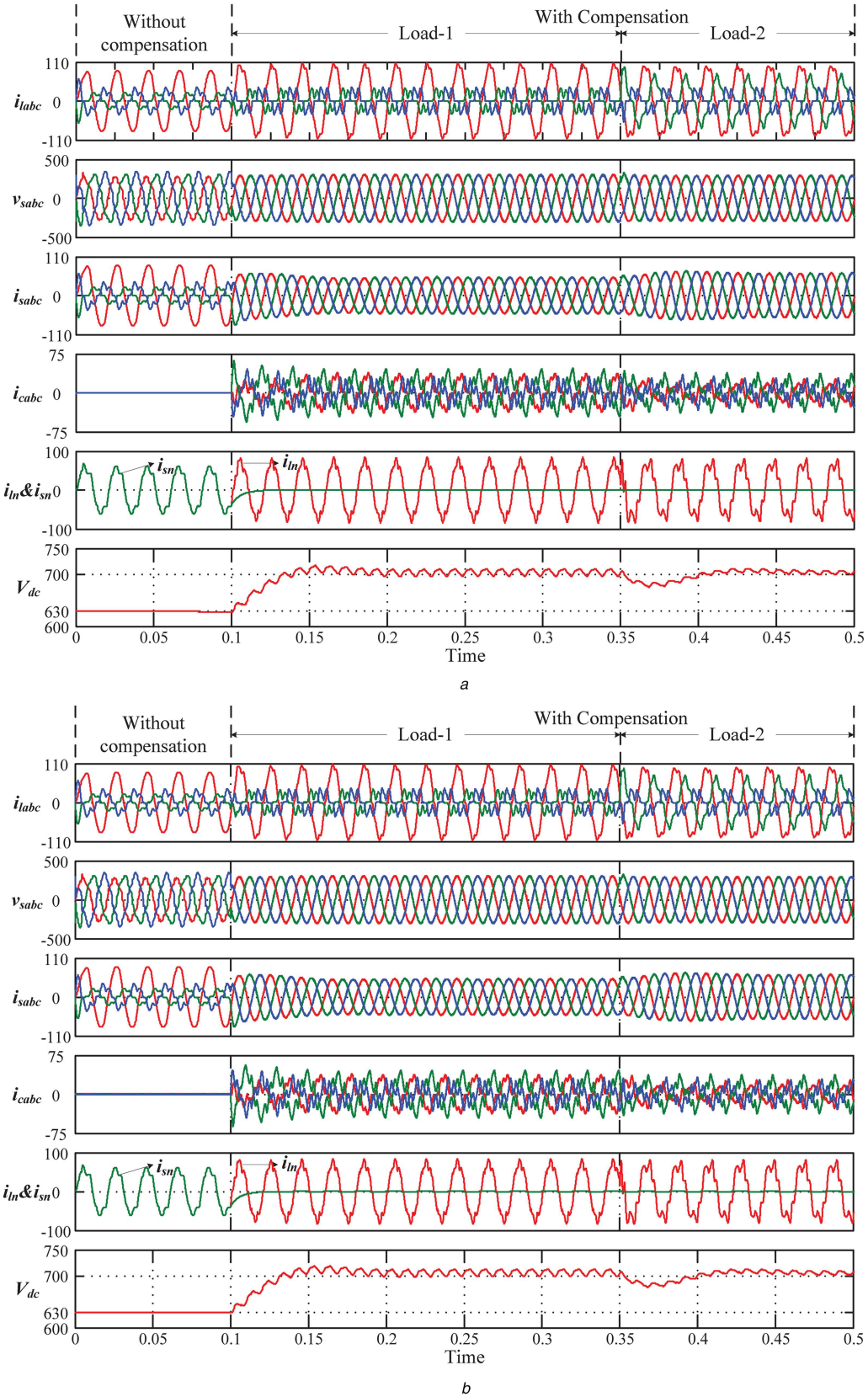

Fig. 5 *Four switch one capacitor topology with*
(a) Zigzag transformer, ***(b)*** T-connected transformer

table, it is observed that the performance of the all the proposed DSTATCOM configurations is almost similar in terms harmonic compensation, load balancing, neutral current compensation and kVA rating of the inverter. The THD values of source currents are mentioned in Table 3 and they are well within the limits according to IEEE 519 standards. The comparison between the proposed work and conventional topologies in terms devices are given in Table 4. The number of switches required in these topologies is less compared to existing four leg topology and split capacitor topology. In general, the rating of the switch means its voltage and current ratings. For a particular load rating of the switches in proposed FSOC and FSSC-based DSTATCOM topologies is less compared to the TPFL and TPSC topologies. This reduction in the number of switches, make the control circuitry further simple

Table 2 Comparison of proposed topologies with an existing split capacitor and four leg topologies

Duration	Topology	Source currents before compensation, A				Source currents after compensation, A			Filter currents, A				Rating of inverter, kVA
		i_{sa}	i_{sb}	i_{sc}	i_{sn}	i_{sa}	i_{sb}	i_{sc}	i_{ca}	i_{cb}	i_{cc}	i_{cn}/i_{zt}	
0.10–0.35 s	TPFL	72.24	17.84	19.72	52.93	35.88	36.15	35.96	37.45	19.48	17.18	52.93	30.436
	TPSC	72.28	17.82	19.70	53.08	35.92	36.14	36.22	37.59	19.49	17.43	52.93	30.534
	FSOC (Z)	72.19	17.84	19.73	52.91	35.90	36.12	35.96	20.70	24.17	11.69	52.75	20.844
	FSOC (T)	72.15	17.81	19.72	52.91	35.86	36.07	35.84	20.72	24.18	11.62	52.7	21.396
	FSSC (Z)	71.97	17.91	19.71	52.84	35.42	35.99	35.66	20.67	24.61	12.10	52.75	21.040
	FSSC (T)	71.90	17.87	19.76	52.82	35.32	35.85	35.68	20.63	24.61	12.17	52.61	21.595
0.35–1 s	TPFL	70.85	44.89	18.62	51.86	44.3	44.42	44.45	27.85	0.5037	26.17	51.76	25.489
	TPSC	71.06	44.94	18.44	53.08	44.65	44.40	44.70	27.73	0.5453	26.50	52.05	25.590
	FSOC (Z)	70.81	44.91	18.62	51.83	44.37	44.35	44.43	12.18	17.42	10.61	51.67	16.777
	FSOC (T)	70.82	44.90	18.64	51.85	44.36	44.43	44.39	12.19	17.43	10.58	51.65	17.329
	FSSC (Z)	70.66	44.99	18.6	51.67	43.99	44.29	44.08	12.49	18.02	11.24	51.58	17.134
	FSSC (T)	70.61	45.07	18.6	51.68	43.88	44.26	45.19	12.56	18.03	11.48	51.48	17.752

(Z) implies zigzag transformer and (T) implies T-connected transformer.

Table 3 THD Comparison of four configurations

Duration	Topology	i_{sa}, % THD	i_{sb}, % THD	i_{sc}, % THD
0.1–0.35 s	without compensation	8.43	47.05	53.47
	FSOC (Z)	1.36	1.51	1.51
	FSOC (T)	1.40	1.55	1.63
	FSSC (Z)	2.84	2.86	2.38
	FSSC (T)	2.84	2.90	2.89
0.35–1 s	without compensation	9.47	18.62	49.36
	FSOC (Z)	1.19	1.18	1.26
	FSOC (T)	1.14	1.20	1.17
	FSSC (Z)	2.28	2.24	1.82
	FSSC (T)	2.32	2.30	2.20

because it is necessary to control only four switches. The voltage rating of the switches in TPSC and FSSC topologies are same and it is given as 1400 V. Similarly, in TPFL and FSOC topologies voltage rating of the switches is given as 700 V. However, from Table 2, it is observed that the current flowing through the switches in proposed topologies is less compared to existing TPFL and TPSC topologies. In four switch topologies, the FSSC topologies are preferred over FSOC, if capacitor balancing problem and higher value of dc-link voltage is not a constraint. Neglecting the size and minute problems created by the addition of a passive filter, FSOC topologies are preferred over FSSC topologies because only one capacitor is required for dc link and the dc-link voltage also reduced to half. The rating of the zigzag transformer and T-connected transformer is nearly equal, but it is better to choose T-connected transformer if it is impelled to reduce the size of the transformer. Quantity and cost of major components namely capacitors, IGBT module (one leg), driver circuits and special transformers are clearly mentioned in Table 5. From this table, it is observed that cost offered by TPFS topologies is less compared to existing TPFL and TPSC topologies. Because the cost added by including a special transformer is less compared to cost reduced by eliminating IGBT modules. In four switch topologies also, cost of FSOC topology is less compared to FSSC topology because of reduction in a number of capacitors used for dc link. Therefore, after observing the above comparative analysis in terms control circuitry, cost and complexity TPFS topologies are the effective solutions for DSTATCOM.

6 Experimental studies

A prototype is developed in the laboratory to verify the performance of the TPFS topologies using special transformers. The experiment is carried out for both FSOC and FSSC topologies with zigzag and T-connected transformer for supporting the simulation results presented in the previous section. Requisite parameters to implement experimental setup are given in Table 6. Supply voltages, load currents and DC link voltages are sensed using LEM made voltage and current transducers. The outputs of the voltage and current transducers are given to dSPACE Micro LabBox 1202 which acts as an interface between real-time environment and Personnel Computer (PC). ISCT is implemented using sensed signals to generate the switching pulses and they are given to the inverter using Micro LabBox 1202. The photograph of the complete experimental setup is shown in Fig. 7. In the experimental setup, the required number of transducers are reduced because the number of phases to be controlled is always two only.

6.1 Performance of FSOC inverter topology with a special transformer

Fig. 8 shows the experimental results of the FSOC topology with special transformers. In this figure, PCC voltages, load currents, source currents and filter currents are shown while load changing from balanced load to unbalanced load. A three-phase diode bridge rectifier is connected as a balanced load and the unbalanced load is realised by connecting three unequal values of impedance along with balanced load. During balanced load, the neutral current flowing through the load is zero, therefore source neutral current is also zero. However, during unbalanced load, a considerable amount of neutral current will flow the source before compensation, but after compensation entire neutral current is flowing through the special transformer. Fig. 9*a* shows source neutral currents, load neutral currents, source current and dc-link voltages before and after connecting DSTATCOM during unbalanced load. Initially, before connecting DSTATCOM source neutral and load currents are same, but after connecting the DSTATCOM, source neutral current is nullified which is clearly shown in Fig. 9*a*. In this FSOC topology, the required dc-link voltage is 100 V for 50 V of line voltage which is already mentioned in the previous sections, and it is also shown in experimental results. Fig. 9*b* also shows that the source neutral

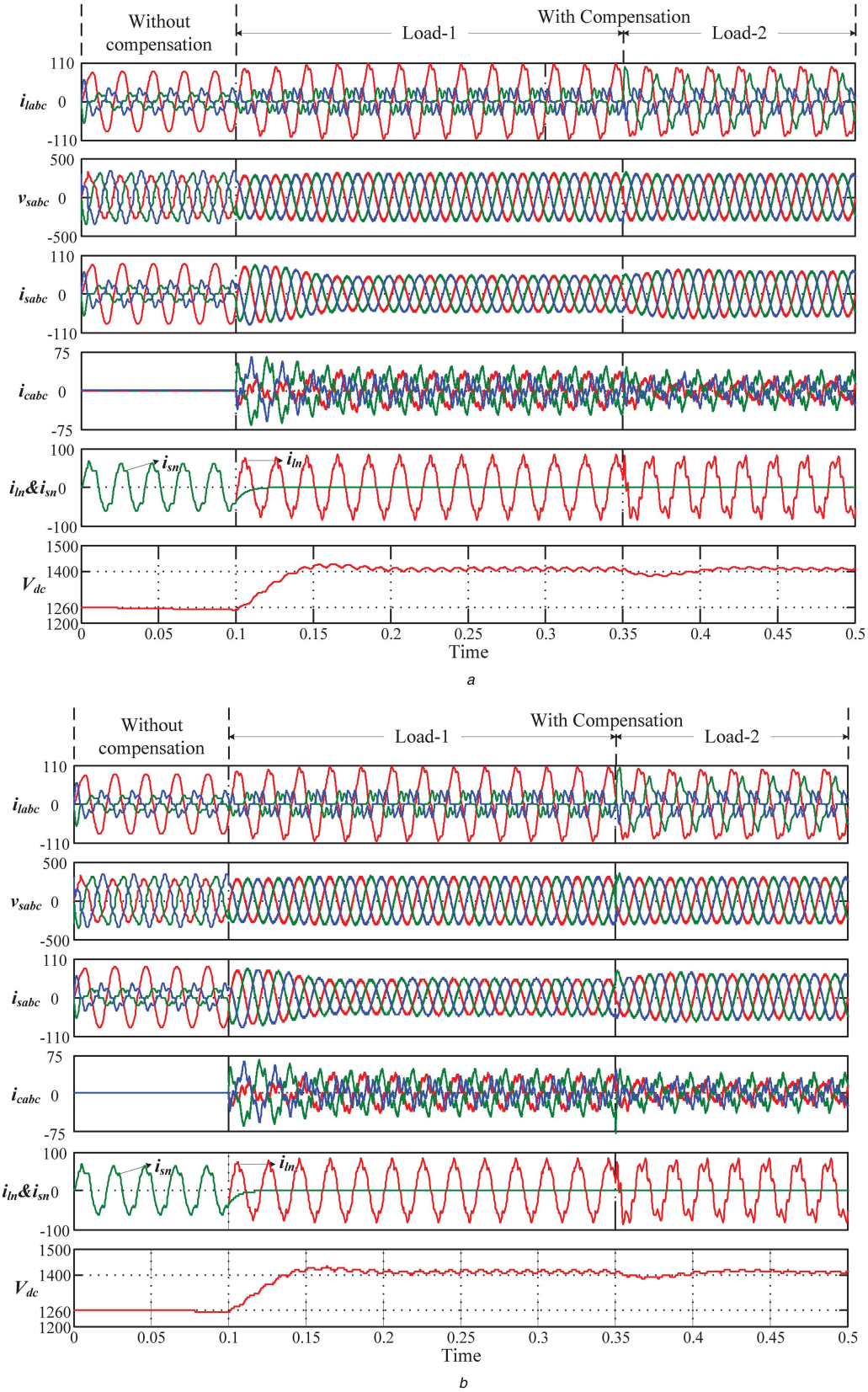

Fig. 6 *Four switch split capacitor topology with*
(a) Zigzag transformer, ***(b)*** T-connected transformer

current, dc-link voltage is not varying when the load is varying from balanced to unbalanced.

6.2 Performance of FSSC inverter topology with a special transformer

Experimental results during FSSC inverter with zigzag of the T-connected transformer connected as a DSTATCOM is shown in Fig. 10. In this figure, PCC voltages, non-linear and balanced, unbalanced load currents, balanced source currents and filter currents are shown separately for both zigzag and T-connected FSSC DSTATCOM topologies. During non-linear balanced load condition, DSTATCOM makes source currents sinusoidal which are also in-phase with the respective voltages. During unbalanced load, FSSC inverter topology makes harmonic free source currents which are also in-phase with the voltages and the special

Table 4 Comparison in terms of various components

Parameters	TPFL	TPSC	FSOC (Z)	FSOC (T)	FSSC (Z)	FSSC (T)
switches	8	6	4	4	4	4
capacitors	1	2	1	1	2	2
LC filters $1-\phi$	0	0	2	2	0	0
transformers	0	0	3	2	3	2
v_{dc}	$2V_{mp}$	$4V_{mp}$	$2V_{mp}$	$2V_{mp}$	$4V_{mp}$	$4V_{mp}$

Table 5 Cost comparison of various topologies

Topology	Capacitor (4700 μF/450 V) B43743A5478M000 (12,143 Rs)	IGBT module (ONE LEG) (SKM75GB12T4 = 7051 Rs) (SKM75GB17E4 = 8640 Rs)	Drivers (SKYPER 32R) (12,593 Rs)	Special transformer (15,000 Rs)	Total cost
TPFL	1	4 (SKM75GB12T4)	4	0	90,719 Rs
TPSC	2	3 (SKM75GB17E4)	3	0	87,985 Rs
FSOC	1	2 (SKM75GB12T4)	2	1	66,431 Rs
FSSC	2	2 (SKM75GB17E4)	2	1	81,752 Rs

Table 6 Parameters for experimental setup

Parameters	Value
supply voltage	V_l (line–line) = 50 V
interfacing inductance	$L_f = 8\,\text{mH}$
dc-link capacitance	$C_{dc} = 3600\,\mu\text{F}$
rated dc voltage (FSOC)	$V_{dc} = 100\,\text{V}$
rated dc voltage (FSSC)	$V_{dc} = 200\,\text{V}$
filter inductor (FSOC)	$L_5 = 8\,\text{mH}$, $L_7 = 4\,\text{mH}$
filter capacitor (FSOC)	$C_5 = 50\,\mu\text{F}$, $C_7 = 50\,\mu\text{F}$
hysteresis band	$h = \pm 0.1$ A
load-1	3−ϕ diode bridge rectifier load with 30 Ω, 150 mH
load-2	unbalanced linear load
	a-ph: 14 Ω, 18 mH
	b-ph: 14 Ω, 32 mH
	c-ph: 14 Ω, 25 mH

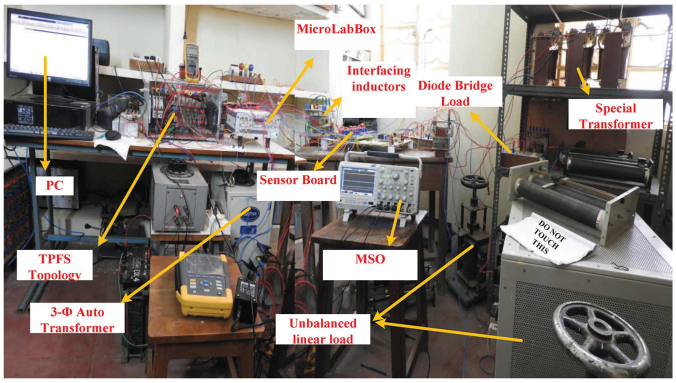

Fig. 7 *Photograph of complete Experimental setup*

transformer is providing a path for the entire neutral current sot that the source currents become balanced.

7 Conclusion

In this paper, four DSTATCOM configurations are proposed by using FSSC or FSOC inverter topology with a zigzag transformer or T-connected transformer to compensate neutral current generated by the non-linear and unbalanced loads. In addition, it will also make source currents sinusoidal with unity power factor. The other advantages of the proposed configurations are effective compensation during stringent load conditions, short-term overloading capability and the rating and cost of is less compared to TPFL and TPSC topologies which are explained clearly in Section 5. The experimental results of four proposed configurations are also proven that the performance is satisfactory during balanced and unbalanced load conditions.

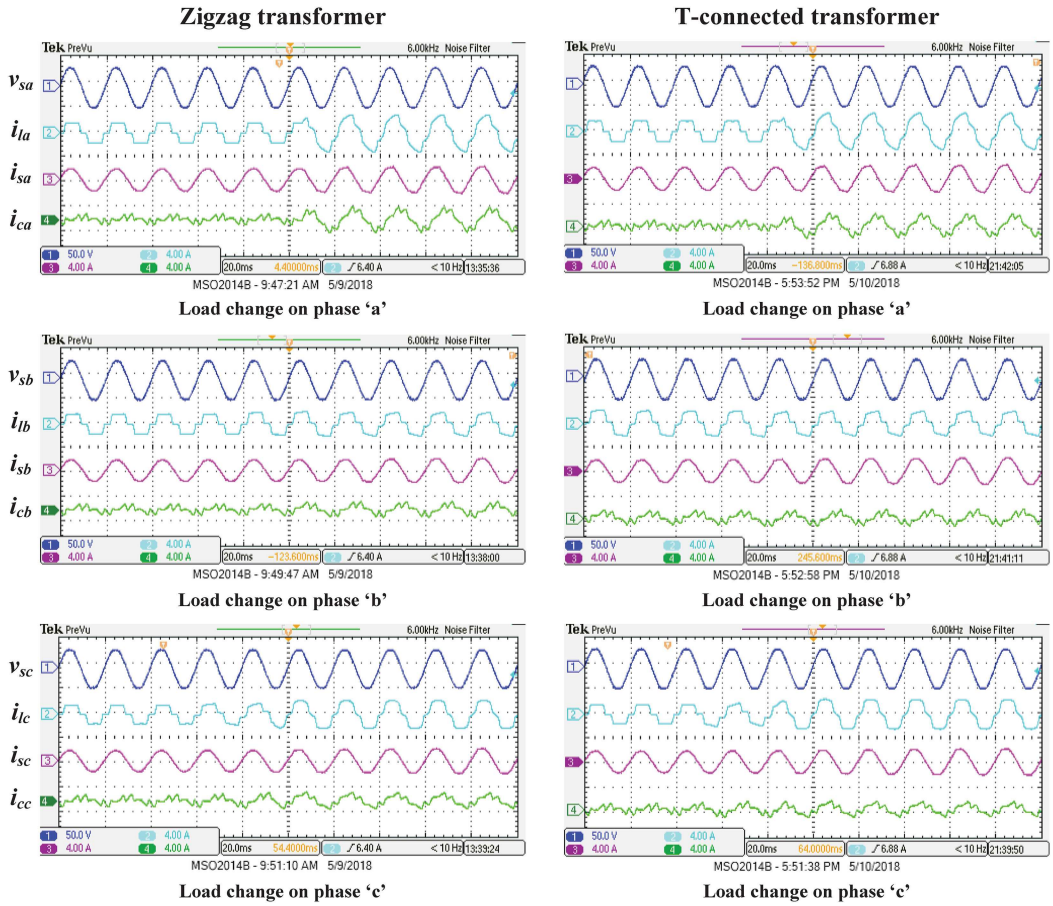

Fig. 8 *Experimental results during FSOC with special as DSTATCOM*

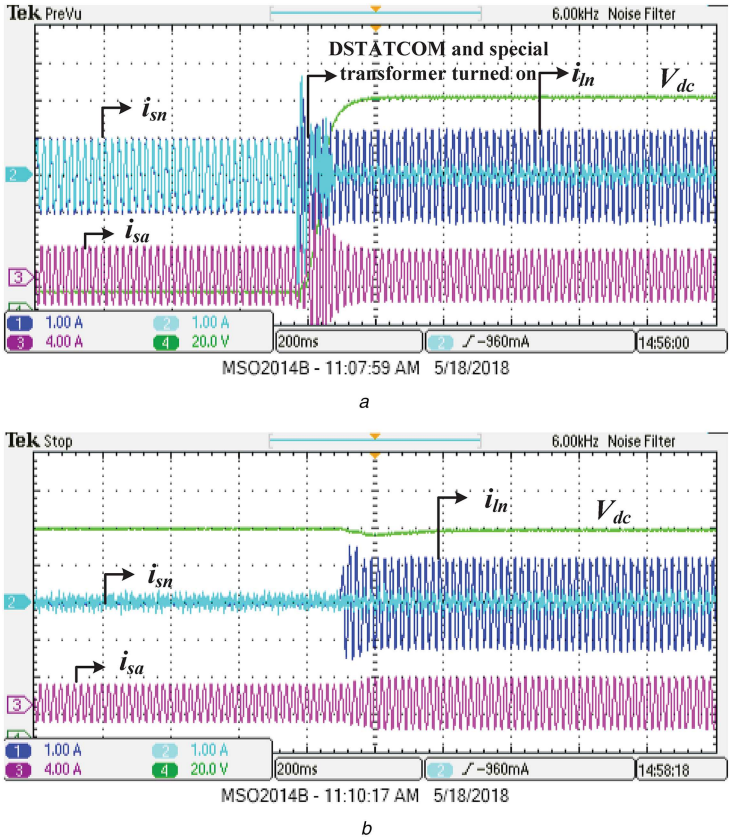

Fig. 9 *Variation of neutral currents and dc-link voltage*
(a) Before and after connecting DSTATCOM, ***(b)*** During balanced and unbalanced loads

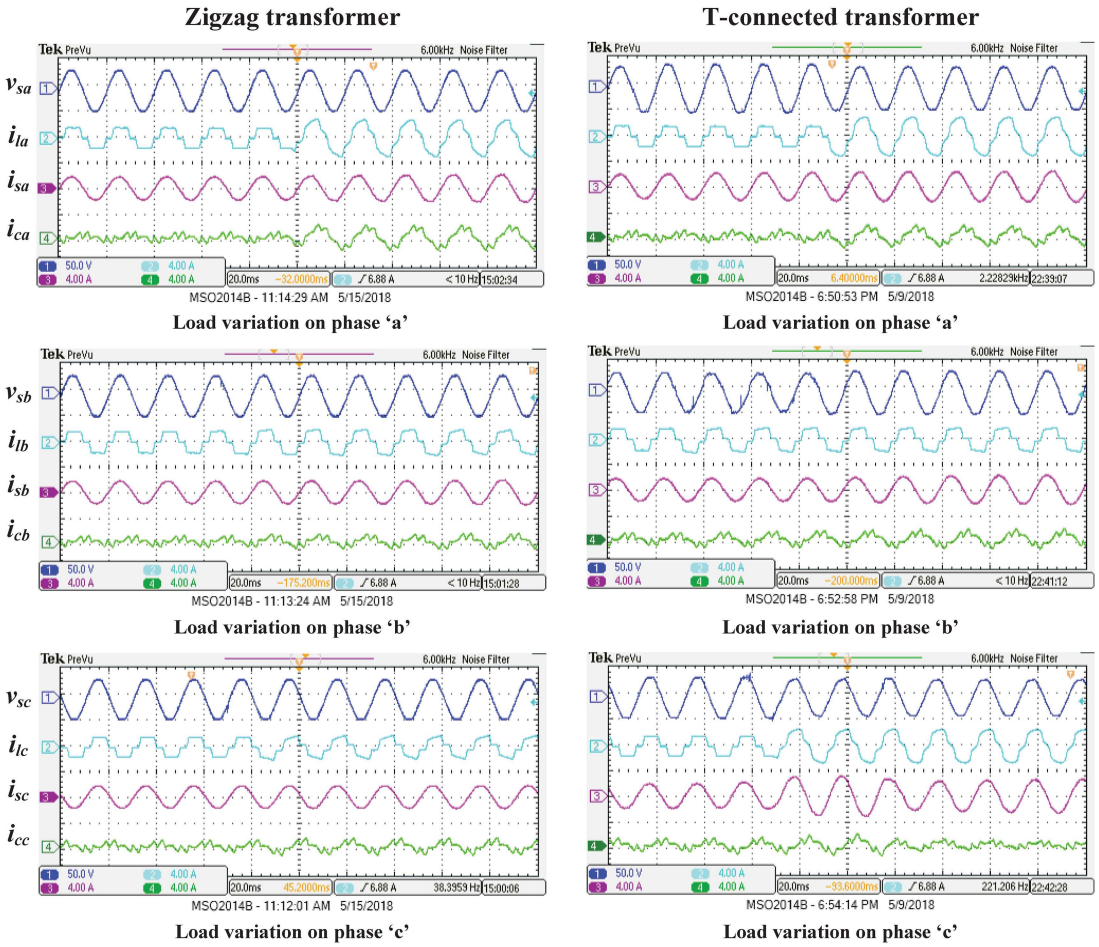

Fig. 10 *Experimental results during FSSC with a special transformer as DSTATCOM*

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