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Model predictive current control of DSTATCOM with simplified weighting factor selection using VIKOR method for power quality improvement

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Alladi Pranay Kumar[1], *Ganjikunta Siva Kumar*[1] ✉, *Dharmavarapu Sreenivasarao*[1], *Hareesh Myneni*[1]

[1]*Department of Electrical Engineering, National Institute of Technology, Warangal, India*

✉ *E-mail: ganjikuntask@gmail.com*

Abstract: In this study, model predictive control (MPC) of the three-phase split capacitor (TPSC) distribution static compensator (DSTATCOM) using VIseKriterijumska Optimizacija I Kompromisno Resenje (VIKOR) method is proposed. Power quality improvement using MPC involves the selection of switching state which minimises the difference between reference and actual DSTATCOM currents. However, the limitation of MPC is higher switching frequency and limitation of TPSC DSTATCOM is voltage divergence of dc-link capacitors. To alleviate these problems, one constraint is to suppress the voltage divergence and the other is to reduce the switching frequency is included in the cost function using weighting factors. Optimal selection of switching state for minimisation of a multi-constraint cost function is depending on the weighting factor; however, its tuning is a challenging task. In this study, the simplification of weighting factor tuning is achieved using the VIKOR method and it further selects the optimal switching state based on a specific measure of closeness to the ideal solution and multi-criteria ranking index. The advantages of the proposed work are compensation of power quality issues, balance the dc-link voltages, switching frequency reduction of inverter and simplification of weighting factor tuning. Finally, the proposed work is evaluated using simulation and experimental studies.

1 Introduction

The continuous research in the area of power electronic devices attracts various industries in the global market to use them as feedstock for their products. Most of the products are utilised by domestic appliances such as fans, air conditioners, refrigerators, washing machines and lighting loads. These appliances draw non-linear load currents due to the presence of power electronic devices and these are also leading to the flow of neutral currents if the ratings of them are distinct. In the distribution system, these non-linear and unbalanced load currents cause current-related power quality issues and they are compensated using custom power devices (CPD) [1–3]. Distribution static compensator (DSTATCOM) is a shunt-connected CPD, which is used to mitigate the current-related power quality issues especially power factor correction, harmonic mitigation, load balancing and neutral current compensation [4–7]. There are various DSTATCOM topologies discussed in the literature along with their parameter design [8–10]. Among them, three-phase four-leg (TPFL) and three-phase split capacitor (TPSC) voltage-source inverter-based (VSI) DSTATCOM topologies are ahead in the utilisation because of its simple structure and easy implementation. In these two topologies, three legs are compensating the non-linear load currents and improving the power factor. The fourth leg of TPFL topology is used for load balancing and neutral current compensation. However, it will increase the number of switches and control circuitry [10]. TPSC topology has conquered this limitation by connecting the neutral wire to the common point of two capacitors [10].

In recent years, model predictive control (MPC) methods are used in many research areas, because of its easy implementation, providing good dynamic and steady-state response, and constraints can be easily added to the cost function [11, 12]. Process control industry is the first field, where MPC is applied. However, the extended development in the area of microprocessors and digital controllers improves the usage of MPC techniques in several other areas such as grid-connected inverters, active filters, motor control etc. [13, 14]. Utilisation of MPC methods to the DSTATCOM for power quality improvement mainly depends on minimisation of a single constraint cost function, which consists of the difference between the reference and actual filter currents as a control parameter [15–17].

The distinct leakage currents, asymmetrical charging of dc-link capacitors during compensation of loads with higher unbalance factor initiate voltage unbalance across the capacitors of TPSC topology, which deteriorate the DSTATCOM performance [18, 19]. In the literature, the switching of the inverter is adjusted to overcome this limitation; however, it further increases the control complexity [19–21]. As mentioned that, the advantage of MPC is, easy inclusion of control parameters; therefore, the voltage unbalance problem can be eliminated by taking the difference between capacitor voltages as an additional control parameter and it is added to the cost function using a weighting factor. However, the switching frequency, which is related to control effort is high using MPC, and it is leading to higher switching losses. This higher switching frequency limitation of MPC is controlled by considering the difference between the present and previous switching states as a control parameter and it is added to the cost function using another weighting factor. The selection of suitable switching state during multi-constraint case depends on the weighting factor. However, weighting factor tuning is a challenging task [22]. Therefore, the simplification of weighting factor tuning is necessary and in this paper it is achieved using a multi-criteria decision-making (MCDM) [23] method, namely VIseKriterijumska Optimizacija I Kompromisno Resenje (VIKOR). In this method, initially ranking and selection from the available set of alternatives are done in the presence of multi-criteria. Then, based on the specific measure of closeness to the ideal solution and multi-criteria ranking index, it selects the optimal solution from the available alternatives.

Therefore, in this paper, MPC of TPSC DSTATCOM with VIKOR method is proposed to compensate the current-related power quality issues, capacitor voltage balancing, reduce the switching frequency along with the simplification of the weighting factor tuning. Initially, cost function of MPC consists of only current control term. However, to compensate the capacitor voltage unbalancing problem in the DSTATCOM topology, higher

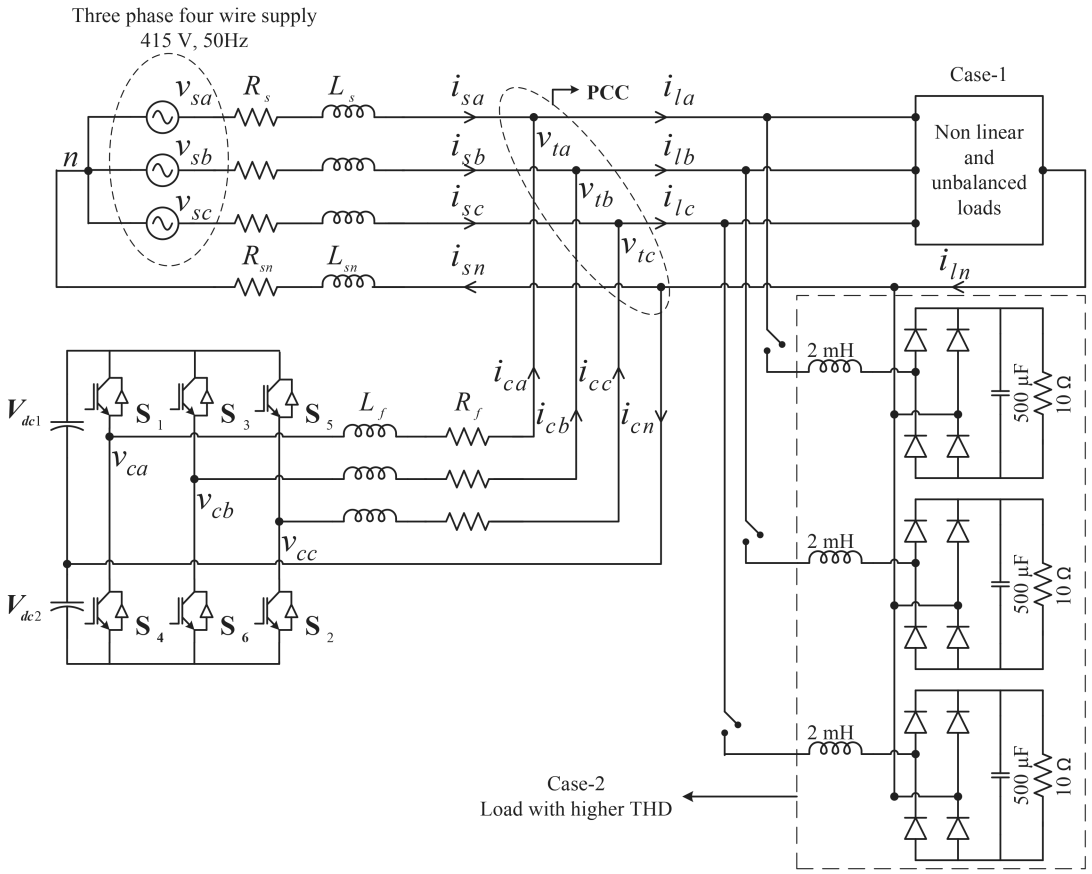

Fig. 1 *Schematic diagram of DSTATCOM-connected distribution system*

switching frequency of MPC, two additional constraints are included in the cost function using weighting factors. Finally, VIKOR method is used to simplify the weighting factor tuning under multi-constraint case for the selection of suitable switching state.

The proposed work is organised as follows. Section 2 explains about the schematic diagram of the DSTATCOM-connected distribution system, design of various parameters of DSTATCOM and the proposed MPC with VIKOR method. Simulation and experimental results are analysed in Sections 3 and 4, followed by conclusion in Section 5.

2 Proposed MPC with VIKOR method

The schematic diagram of TPSC DSTATCOM-connected distribution system is shown in Fig. 1. Here, DSTATCOM is connected through an interfacing inductor (L_f) at the point of common coupling (PCC) which eliminates ripples from filter currents and internal resistance of L_f is represented as R_f. The source and load neutrals are connected to the mid-point of dc link, which eliminates the requirement of additional switches such as TPFL topology to compensate the unbalanced load currents. In Fig. 1, i_{sa}, i_{sb} and i_{sc} represents the source currents. i_{la}, i_{lb} and i_{lc} represents the load currents. i_{ca}, i_{cb} and i_{cc} represents the filter currents. PCC voltages are represented with v_{ta}, v_{tb} and v_{tc}. Voltages at the inverter terminals are represented with v_{ca}, v_{cb} and v_{cc}. Source, load and DSTATCOM neutral currents are represented with i_{sn}, i_{ln} and i_{cn}, respectively.

The design of various parameters of DSTATCOM such as dc-link voltage, dc-link capacitance and interfacing inductor are explained as follows.

2.1 DC-link voltage (V_{dc1}, V_{dc2})

The voltage across each individual dc-link capacitor is considered as 1.6 times of peak value of phase voltage [10]. The dc-bus voltage is calculated as

$$V_{dc1} = V_{dc2} = \frac{1.6\sqrt{2}V_{LL}}{\sqrt{3}m} \tag{1}$$

where V_{LL} is the line-to-line voltage and m is the amplitude modulation index, usually it is considered as unity.

2.2 DC-link capacitance (C_{dc1}, C_{dc2})

The capacitance value of each dc-link capacitor depends on kVA (X) of the system, allowed voltage change (1.4–1.8 times of peak voltage), fundamental time period (T) and the number of cycles with transient operation (n) [10]. Therefore, the dc-link capacitance is given as

$$C_{dc1} = C_{dc2} = \frac{2(2X - (X/2))nT}{(1.8V_m)^2 - (1.4V_m)^2} \tag{2}$$

Interfacing Inductor (L_f): The value of interfacing inductance mainly depends on acceptable ripple current (ΔI), maximum switching frequency ($f_{s\,max}$) and peak value of phase voltage (V_m) [10]

$$L_f = \frac{1.6V_m}{4\Delta I f_{s\,max}} \tag{3}$$

During simulation studies, supply voltage (V_{LL}) is considered as 415 V, $X = 25$ kVA, $n = 0.5$, $T = 0.02$ s, $\Delta I = 1.6$ A and $f_{s\,max} = 20$ kHz. Therefore, using (1)–(3), the obtained value of dc-link voltage $V_{dc1} = V_{dc2} = 540$ V of the dc-link capacitance $C_{dc1} = C_{dc2} = 5100\,\mu$F. The calculated value of L_f is 4.33 mH and in this paper it is considered as 5 mH.

Similarly, for experimental studies, V_{LL} is considered as 50 V, $X = 300$ VA, $n = 0.5$, $T = 0.02$ s, $\Delta I = 0.4$ A and $f_{s\,max} = 5$ kHz. Owing to the rating constraints, the experimental setup is developed at lower voltage and power ratings. Using (1), the obtained value of dc-link voltage $V_{dc1} = V_{dc2} = 70$ V. Using (2), the

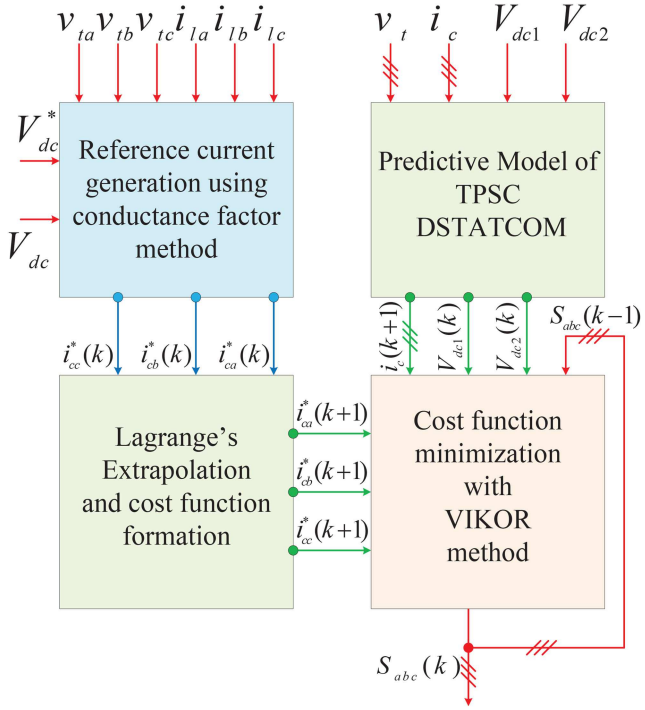

Fig. 2 *Proposed MPC control algorithm with VIKOR method*

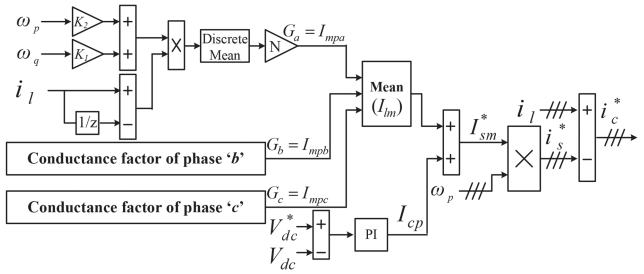

Fig. 3 *Reference current extraction using conductance factor method*

calculated value of dc-link capacitance is 4220 μF. Therefore, the nearest available rating 4700 μF is selected for both capacitors ($C_{dc1} = C_{dc2} = 4700$ μF). Using (3), the calculated value of L_f is 8.164 mH and in this paper it is considered as 9 mH.

The block diagram of the complete control algorithm is shown in Fig. 2. There are mainly four steps involved in the implementation of MPC with VIKOR method for DSTATCOM control:

(i) *Reference current extraction using conductance factors*: In this, sensed PCC voltages, load currents and dc-link voltage are used to extract the reference compensator currents (i_c^*) using conductance factor method.

(ii) Predictive model of TPSC DSTATCOM is used to estimate the compensator currents at the $(k + 1)$th instant [i.e. $i_c(k + 1)$].

(iii) Implementing Lagrange's extrapolation, to calculate reference filter currents at the $(k + 1)$th instant (i.e. $i_c^*(k + 1)$) and cost function formation.

(iv) Selection of optimal switching state from available switching states using VIKOR method.

2.3 Reference current extraction using conductance factor method

The main objective of implementing this control algorithm is to make source currents balanced, sinusoidal and in-phase with the voltages at PCC. Fig. 3 shows the conductance factor-based control method which is used in the proposed work to extract the fundamental in-phase component of load currents [24]. Initially, load currents, voltages at PCC and dc-link voltages are sensed. The in-phase and quadrature unit vectors are calculated from sensed PCC voltages, which are very much essential to implement this control algorithm. In-phase unit vectors are expressed as

$$w_{pa} = \frac{v_{ta}}{V_{mt}}; \quad w_{pb} = \frac{v_{tb}}{V_{mt}}; \quad w_{pc} = \frac{v_{tc}}{V_{mt}}, \tag{4}$$

where V_{mt} represents the amplitude of phase voltage at PCC and it is given as

$$V_{mt} = \sqrt{\frac{2}{3}(v_{ta}^2 + v_{tb}^2 + v_{tc}^2)} \tag{5}$$

Similarly, quadrature unit vectors are calculated as

$$w_{qa} = \frac{-w_{pb} + w_{pc}}{\sqrt{3}}; \quad w_{qb} = \frac{3w_{pa} + w_{pb} - w_{pc}}{2\sqrt{3}}; \quad w_{qc} = \frac{-3w_{pa} + w_{pb} - w_{pc}}{2\sqrt{3}}. \tag{6}$$

Load current is a combination of active, reactive, harmonic and dc components and it is given as

$$i_l(t) = i_{lp}(t) + i_{lq}(t) + i_h(t) + I_{dc} \tag{7}$$

Equation (7) can also be written as

$$i_l(t) = Gv_t(t) + B\int v_t(t)\mathrm{d}t + i_h(t) + I_{dc}. \tag{8}$$

where G is the conductance and B is the susceptance. The value of G is obtained by taking derivative of (8) using trapezoidal rule

$$i_{l(j)} - i_{l(j-1)} = G(v_{t(j)} - v_{t(j-1)}) + \frac{T_s}{2}(v_{t(j)} - v_{t(j-1)})B + (i_{h(j)} - i_{h(j-1)}). \tag{9}$$

The matrix form representation of (9) is

$$\begin{bmatrix} v_{t1} - v_{t0} & \frac{T_s}{2}(v_{t1} + v_{t0}) & i_{h1} - i_{h0} \\ \vdots & \vdots & \vdots \\ v_{tN} - v_{t(N-1)} & \frac{T_s}{2}(v_{tN} + v_{t(N-1)}) & i_{hN} - i_{h(N-1)} \end{bmatrix}_{N\times 3} \begin{bmatrix} G \\ B \\ 1 \end{bmatrix}_{3\times 1} = \begin{bmatrix} i_{l1} - i_{l0} \\ \vdots \\ i_{lN} - i_{l(N-1)} \end{bmatrix}_{N\times 1}. \tag{10}$$

where T_s is the sampling time and N is the ratio of fundamental time period to the sampling time. Equation (10) is of the form $PX = Q$. Then, the value of G is obtained by computing $X = (P^TP)^{-1}P^TQ$ and it is given as

$$G(t) = \frac{\sum_{j=1}^{N}(i_{l(j)} - i_{l(j-1)})(v_{t(j)} - v_{t(j-1)})}{\sum_{j=1}^{N}(v_{t(j)} - v_{t(j-1)})^2}. \tag{11}$$

After finding $G(t)$, fundamental active component of load current can be written as

$$i_{lp}(t) = G(t)v_t(t). \tag{12}$$

However, fundamental active component of load current is the product of its amplitude and unit vector, which is in-phase with the voltage at PCC

$$i_{lp}(t) = i_{lmp}w_p. \tag{13}$$

After Comparing (13) with (12), the amplitude of fundamental active component of load current is same as the conductance factor, if we replace the voltage (v_t) in (11) and (12) with in-phase unit vector (w_p). Therefore

$$i_{lmp}(t) = G(t) = \frac{\sum_{j=1}^{N}(i_{l(j)} - i_{l(j-1)})(w_{p(j)} - w_{p(j-1)})}{\sum_{j=1}^{N}(w_{p(j)} - w_{p(j-1)})^2}. \quad (14)$$

Riemann integral is used to simplify (14) and the simplified equation is given as

$$i_{lmp}(t) = \sum_{j=1}^{N}(i_{l(j)} - i_{l(j-1)})(w_{q(j)} \times K_1 + w_{p(j)} \times K_2), \quad (15)$$

where $K_1 = (\cos(\omega T_s/2)/N \sin(\omega T_s/2))$, $K_2 = (1/N)$.

After computing conductance factors for each phase, the average (I_{lm}) of these three values will give fundamental active component of load current which is used to make balanced source currents even though the load currents are unbalanced. VSI draws active power to maintain the constant voltage across its dc link. The dc-link voltage of the self-supported dc bus is regulated using a proportional–integral (PI) controller. The input for the PI controller is the difference between the reference dc-link voltage and the measured dc-link voltage and the output (I_{cp}) of it is added to the fundamental active component of load current to get the amplitude of reference source current ($I^*_{sm} = I_{lm} + I_{cp}$). The reference source current is obtained by multiplying amplitude of source current with in-phase unit vector ($i^*_s = I^*_{sm} w_p$). Then, reference filter current is the difference between measured load current and the reference source current

$$i^*_c = i_l - i^*_s \quad (16)$$

2.4 Predictive model of TPSC DSTATCOM

In this paper, TPSC-based VSI is used to implement the DSTATCOM and there are only eight switching states available for this topology. The dynamic model of the DSTATCOM is used to predict the future value of the DSTATCOM current for every available switching state, which mainly depends on present voltages and currents. Then, compare the predicted future current of every switching state with reference current and select a state, which will give the minimum error. The gradual procedure of switching state selection is explained as follows.

From Fig. 1, the voltage at the inverter terminal is equal to the sum of voltage drop across the inductor along with its internal resistance and voltage at PCC, i.e.

$$v_c = i_c R_f + L_f \frac{di_c}{dt} + v_t \quad (17)$$

$$\frac{di_c}{dt} = \left(\frac{v_c - v_t}{L_f}\right) - i_c \frac{R_f}{L_f} \quad (18)$$

The forward Euler approximation method is used to replace (di_c/dt) in (18), and it is represented as

$$\frac{di_c}{dt} = \frac{i_c(k+1) - i_c(k)}{T_s} \quad (19)$$

The discrete time representation of (18) is given as follows:

$$\frac{i_c(k+1) - i_c(k)}{T_s} = \left(\frac{v_c(k) - v_t(k)}{L_f}\right) - i_c(k)\frac{R_f}{L_f}. \quad (20)$$

From (20), the DSTATCOM current at the $(k+1)$th instant is

$$i_c(k+1) = (v_c(k) - v_t(k))\frac{T_s}{L_f} + i_c(k)\left(1 - \frac{R_f T_s}{L_f}\right) \quad (21)$$

In (21), $v_c(k)$ represents the voltage at the inverter terminals, which mainly depends on the switching states of the VSI, $v_t(k)$ represents the voltage at PCC and $i_c(k)$ represents the measured filter current. The various switching combinations and the voltages available at the terminals of the VSI are given in Table 1. The filter currents at the $(k+1)$th instant are calculated by substituting the voltages and currents in (21) with respective values. As discussed in Section 1, the limitation of TPSC DSTATCOM is voltage divergence across the two capacitors of dc link. To overcome this limitation, it is required to find the voltage across the capacitors and include the difference between them as a control parameter in the cost function. Current flowing through each capacitor is a function of dc-link voltage and it is given as

$$i_{dc} = C_{dc}\frac{dV_{dc}}{dt} \quad (22)$$

The dc-link voltages in discrete form is obtained by applying forward Euler approximation to (22) and it is given as follows:

$$\frac{V_{dc}(k+1) - V_{dc}(k)}{T_s} = \frac{i_{dc}(k)}{C_{dc}} \quad (23)$$

Voltage across each capacitor is given as

$$V_{dc1}(k+1) = V_{dc1}(k) + i_{dc1}(k)\frac{T_s}{C_{dc}}$$
$$V_{dc2}(k+1) = V_{dc2}(k) + i_{dc2}(k)\frac{T_s}{C_{dc}} \quad (24)$$

Therefore, it is necessary to calculate current flowing through the capacitor to find the voltage across each capacitor. The value of i_{dc} depends on the state of the switch and current flowing through each phase and it is given as

$$i_{dc1}(k) = -(S_a i_{ca} + S_b i_{cb} + S_c i_{cc})$$
$$i_{dc2}(k) = (\overline{S_a} i_{ca} + \overline{S_b} i_{cb} + \overline{S_c} i_{cc}) \quad (25)$$

2.5 Lagrange's extrapolation and cost function formation

The cost function of the proposed control algorithm mainly consists of three terms. The first term in the cost function is the difference between the reference filter currents and actual filter

Table 1 Switching states with respective voltages

State	S_1	S_3	S_5	v_{ca}	v_{cb}	v_{cc}
1	0	0	0	$-V_{dc2}$	$-V_{dc2}$	$-V_{dc2}$
2	1	0	1	V_{dc1}	$-V_{dc2}$	V_{dc1}
3	1	1	0	V_{dc1}	V_{dc1}	$-V_{dc2}$
4	0	1	0	$-V_{dc2}$	V_{dc1}	$-V_{dc2}$
5	0	1	1	$-V_{dc2}$	V_{dc1}	V_{dc1}
6	0	0	1	$-V_{dc2}$	$-V_{dc2}$	V_{dc1}
7	1	0	0	V_{dc1}	$-V_{dc2}$	$-V_{dc2}$
8	1	1	1	V_{dc1}	V_{dc1}	V_{dc1}

currents at the $(k+1)$th sampling. The value of $i_c(k+1)$ is given in (21) and $i_c^*(k+1)$ is calculated from $i_c^*(k)$ using second-order Lagrange's extrapolation

$$i_c^*(k+1) = 3i_c^*(k) - 3i_c^*(k-1) + i_c^*(k-2) \tag{26}$$

Therefore, the first term in the cost function is given as

$$C_1 = \sum_{j=a,\,b,\,c} \left| i_{cj}^*(k+1) - i_{cj}(k+1) \right| \tag{27}$$

The second term in the cost function is the difference between the voltages across two capacitors of the dc link, which is used to suppress the voltage divergence

$$C_2 = |V_{dc1}(k+1) - V_{dc2}(k+1)| \tag{28}$$

The main limitation of using MPC is higher switching frequency and it is reduced by adding the difference between the present switching state and the previous switching state as an additional control parameter to the cost function

$$C_3 = \sum_{j=a,\,b,\,c} \left| (S_j(k) - S_j(k-1)) \right| \tag{29}$$

In (29), the value of $S_j(k-1)$ is obtained by considering it is a feedback variable. Therefore, using conventional predictive control method, the complete cost function is formed by adding three individual cost functions using weighting factors

$$C = C_1 + \lambda_1 C_2 + \lambda_2 C_3 \tag{30}$$

where λ_1 and λ_2 are the weighting factors.

However, the tuning of weighting factors is a challenging task and also the number of weighting factors will increase by increasing the number of constraints in the cost function. Therefore, in the proposed work the complexity in the tuning is reduced by choosing an MCDM method, namely VIKOR. This method initially gives rankings and selects the optimal switching state from the available switching states and the selected state will be applied to the DSTATCOM.

2.6 Application of VIKOR method for selecting optimal switching state

Step 1: In (30), C_1 represents the cost function belongs to current control, C_2 represents the cost function belongs to voltage balancing and C_3 is for switching frequency reduction. In this method, initially cost functions C_1, C_2 and C_3 are individually evaluated for each available switching state and those values are represented as follows:

$$\boldsymbol{C}_{IJ} = \begin{bmatrix} C_{11} & C_{12} & C_{13} \\ C_{21} & C_{22} & C_{23} \\ C_{31} & C_{32} & C_{33} \\ C_{41} & C_{42} & C_{43} \\ C_{51} & C_{52} & C_{53} \\ C_{61} & C_{62} & C_{63} \\ C_{71} & C_{72} & C_{73} \\ C_{81} & C_{82} & C_{83} \end{bmatrix}_{8\times 3} \tag{31}$$

The order of the matrix $\boldsymbol{C}_{IJ}$ depends on the number of available switching states and the number of control parameters.

Step 2: After evaluating the cost functions for each switching state, select the positive and negative best values for each cost function. Positive best value represents the maximum and negative best value represents the minimum value in each column of $\boldsymbol{C}_{IJ}$. The objective of this method is to minimise the error; therefore, the negative best value is considered as the ideal solution

$$\begin{aligned} C_1^- &= \min(C_{i1}); \quad C_2^- = \min(C_{i2}); \quad C_3^- = \min(C_{i3}). \\ C_1^+ &= \max(C_{i1}); \quad C_2^+ = \max(C_{i2}); \quad C_3^+ = \max(C_{i3}). \end{aligned} \tag{32}$$

Step 3: Utility measure S_i represents the average scores and regret measure R_i represents the worst group scores and they are represented as follows:

$$S_i = \sum_{j=1}^{3} w_j \frac{C_j^- - C_{ij}}{C_j^- - C_j^+} \tag{33}$$

$$R_i = \max_j \left[w_j \frac{(C_j^- - C_{ij})}{(C_j^- - C_j^+)} \right] \tag{34}$$

In (33) and (34), w_j represents the weight assigned to the jth cost function. According to VIKOR method, the sum of all weights should be always equal to one, i.e.

$$\sum_{j=1}^{3} w_j = 1 \tag{35}$$

Step 4: The last step in this method is selection of optimal switching state from available switching states using VIKOR index (Q). The value of Q is calculated using

$$Q_i = m\left[\frac{(S_i - S^-)}{(S^+ - S^-)}\right] + (1-m)\left[\frac{(R_i - R^-)}{(R^+ - R^-)}\right] \tag{36}$$

where the superscripts '–' represents the minimum value and '+' represents the maximum value and usually the group utility factor 'm' is set to be 0.5. Q is estimated for each switching state and the state which is giving the minimum Q will be the optimal switching state that has to be applied at next instant for DSTATCOM control.

For example, Table 2 shows the values of VIKOR index (Q) for all the switching states during one sample time. Among all the states, the switching state '7' is giving the minimum Q, so that it will be applied in the next instant.

3 Simulation results

Various parameters of the distribution system and DTSTACOM, which are required to implement the proposed control algorithm, are mentioned in Table 3. Three different loads considered for simulation studies. Load-1 is a combination of three single-phase diode bridge rectifiers with different *RL* values at its dc side, load-2 is a three-phase balanced *RL* load and load-3 is a combination of three single-phase diode bridge rectifiers with equal *RC* values at its dc side. Using these three loads, two different case studies are formed to analyse the performance of the proposed control algorithm. In case-1, during 1–1.75 s, load-1 and load-2 are connected to the distribution system, which draws non-linear and unbalanced load currents. During 1.75–3 s, load-2 is removed and it is again connected at 3 s to analyse the dynamic performance. In case-2, load-3 is connected to analyse the performance during compensation of loads with higher THD values. As mentioned, the cost function of the proposed control algorithm consists of three individual control parameters. However, to understand the efficacy of the proposed control algorithm, dc-link voltages and switching frequencies are shown without considering and with considering of their control parameters in cost function.

3.1 Performance during compensation of non-linear and unbalanced loads

As mentioned, distinct leakage currents, asymmetrical charging of dc-link capacitors during compensation of loads with higher unbalance factor are leading to an unequal flow of currents through the two capacitors of the dc link, which results the voltage across

one capacitor continuously rising and falling voltage across the other capacitor. Fig. 4 shows the complete dc-link voltage (V_{dc}) and the voltage across the two capacitors (V_{dc1} and V_{dc2}). It is observed that the complete dc-link voltage is maintained constant with respect to the reference value; however, individual voltages are getting diverged during load changes. The average switching frequency is estimated from instantaneous switching frequencies, which are calculated by measuring the time period of every switching cycle in one fundamental time period. The calculated switching frequencies of MPC method without adding any switching frequency constraint in the cost function are 22,280, 22,836 and 22,100 Hz for each leg and they are illustrated in Fig. 5. These capacitor voltage divergence and higher switching frequency limitations are conquered by adding them as control parameters to the cost function along with DSTATCOM currents.

Fig. 6 shows PCC voltage, source current, load current, filter current, load and source neutral currents, after adding all the control parameters to the cost function. As mentioned, at 1.75 s, three-phase balanced linear load is removed and it is observed from Fig. 6 that the transient performance using the proposed method is good. It is also observed that the source currents are balanced and sinusoidal even though the load currents are non-linear and unbalanced. Unbalanced loads cause the flow of neutral current, but the compensator is not allowing it through the source neutral wire, which is shown in Fig. 6. Root-mean-square (RMS) values of unbalanced and non-linear of load currents are 41.94, 47.23 and 54.92 A with THDs 21.4, 24.87 and 25.5% for '*a*', '*b*' and '*c*' phases, respectively. However, the RMS values of source currents 42.5, 42.67 and 42.45 A indicate they are balanced and THD values 2.42, 2.41 and 2.46% indicate they are sinusoidal.

Fig. 7 shows the complete dc-link voltage and individual capacitor voltages and it is observed that after adding voltage difference between two capacitors as a cost function, the complete dc-link voltage is maintained with respect to its reference value and individual capacitor voltages are also balanced.

Table 2 Selection of optimal switching state using *Q*

State	C_1	C_2	C_3	*S*	*R*	*Q*
1	6.2399	0.3178	2	0.6019	0.2667	0.5546
2	3.4657	0.3133	1	0.246	0.1333	0.2211
3	7.3465	0.3089	2	0.6107	0.3107	0.6066
4	10.1207	0.3133	3	0.9667	0.5	1
5	9.4463	0.3089	2	0.754	0.454	0.8368
6	5.5656	0.3133	1	0.3893	0.1893	0.3577
7	**2.7913**	**0.3089**	**0**	**0.0333**	**0.0333**	**0**
8	6.6721	0.3044	1	0.3981	0.2647	0.4433

Bold values indicate that among all the states, the switching state '7' is giving the minimum Q, so that it will be applied in the next instant.

Table 3 System parameters for simulation

Parameter	Value
system voltage	415 V
feeder impedance (Z_s)	0.07 Ω, 0.2 mH
interfacing inductor (L_f)	5 mH ($R_f = 0\,\Omega$)
dc-link voltage (V_{dc})	1080 V
dc capacitor (C_{dc1}, C_{dc2})	5100 μF
w_1, w_2 and w_3	0.5, 0.1 and 0.4
PI controller	$k_p = 0.45$, $k_i = 4.5$
unbalanced non-linear load (three single-phase diode bridge rectifiers) (load-1)	6 Ω, 150 mH (phase-a) 5 Ω, 150 mH (phase-b) 4 Ω, 150 mH (phase-c)
three-phase balanced linear load (load-2)	15 Ω, 30 mH (on each phase)
loads with higher THD (load-3)	three single-phase diode bridge rectifiers feeding parallel connection of 10 Ω, 500 μF (on each phase)
sampling time (T_s)	10 μs

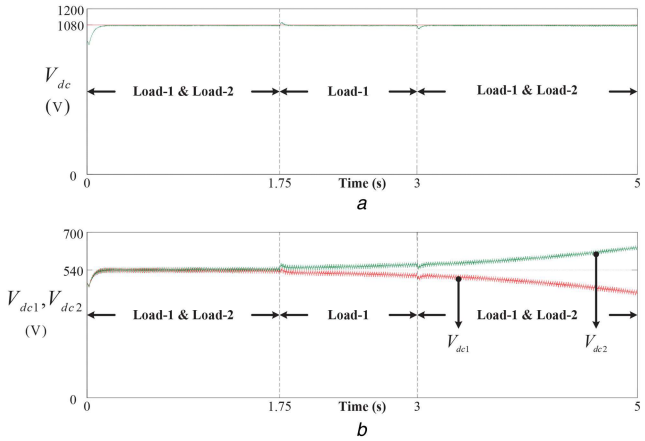

Fig. 4 *Without adding additional constraints*
(a) Voltage across complete dc link, ***(b)*** Voltage across individual capacitors

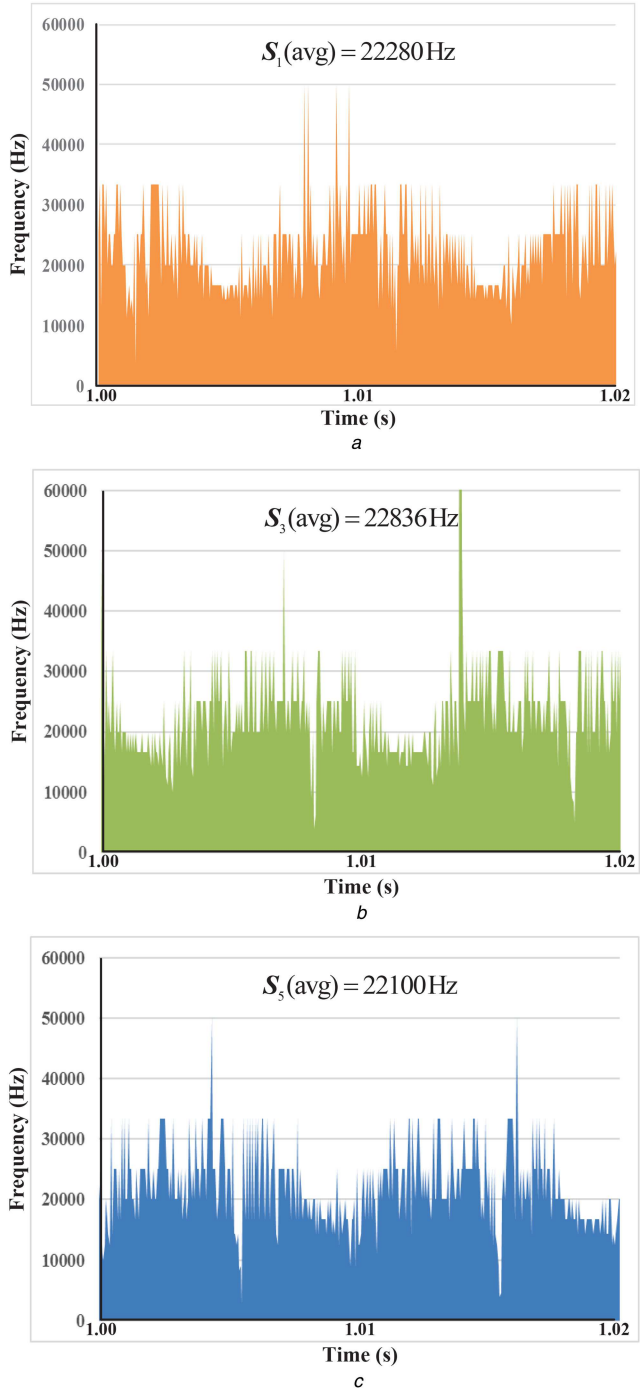

Fig. 5 *Average switching frequency without adding additional constraints*
(a) S_1, ***(b)*** S_3, ***(c)*** S_5

Fig. 8 shows the switching frequency for one fundamental time period (0.02 s), it shows that the average switching frequency is reduced using the proposed method and the reduced switching frequencies are 12,875, 12,652 and 12,929 Hz for S_1, S_3 and S_5, respectively. Fig. 9 shows the tracking of compensator current and switching pulses for one fundamental time period. It is observed that after adding switching state as a control parameter in the cost function, the switching frequency is reduced. The reduction in switching frequency causes increase in tracking error, which is also shown in Fig. 9. However, from Table 4, it is observed that the THDs are well within the limits of IEEE Std 519-1992 standards (<5%), which emphasises that the proposed control algorithm is efficient.

3.2 Performance during loads with higher THD

In this case, three single-phase diode bridge rectifiers feeding parallel connections of R and C is connected as load which is

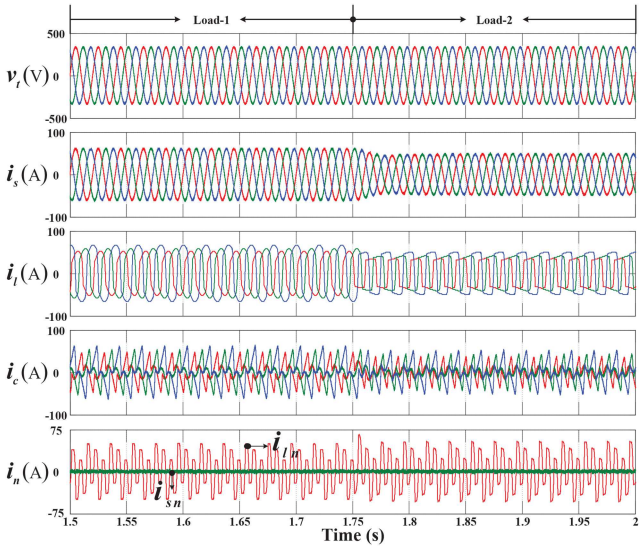

Fig. 6 *Simulation results using the proposed method*

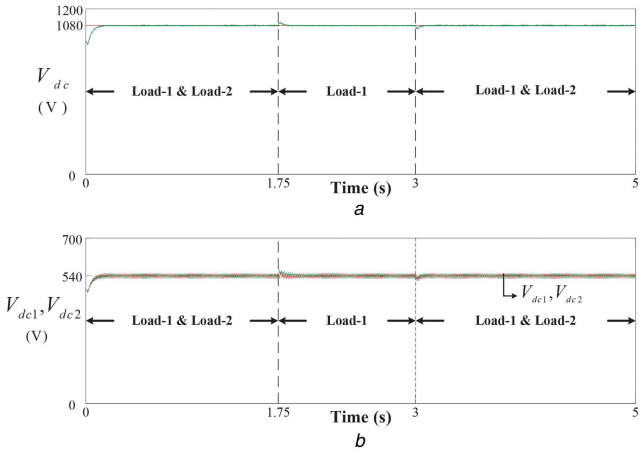

Fig. 7 *After including additional constraints*
(a) Voltage across complete dc link, ***(b)*** Voltage across individual capacitors

shown in Fig. 1, and they are connected to the distribution system to achieve load currents with higher THD. During 0–0.5 s, the DSTATCOM is operated with only current control and at 0.5 s additional constraints are added to the cost function. Fig. 10 shows the source currents, load currents, DSTATCOM currents and PCC voltages. The THD of load currents is 70% for all the three phases. Table 5 shows the THD values of source currents, switching frequencies with and after including the additional constraints. From Table 5, it is observed that the THDs of source currents without adding switching frequency constraint are 1.75, 1.72 and 1.72%, respectively, for phases a, b and c. During this, the switching frequencies are 28,506, 28,426 and 28,891 Hz for a, b and c phases, respectively. After adding the switching frequency constraint, the frequency values are reduced to 17,723, 18,192 and 17,799 Hz. However, the THD values 2.62, 2.65 and 2.62% show that they are well under the limits of IEEE 519-1992 standards. Therefore, the proposed method will be applicable to higher THD loads also.

4 Experimental results

In this paper, performance of the proposed control algorithm is also evaluated using experimental studies. Various parameters considered for experimental studies are given in Table 6. Owing to the rating constraints, the experimental setup is built for less voltage and power ratings. The design procedure of the parameters such as dc-link voltage, dc-link capacitance and interfacing inductor are explained in Section 2. The photograph of the experimental setup is shown in Fig. 11. Two different loads are considered for experimentation. Load-1 is a three-phase diode

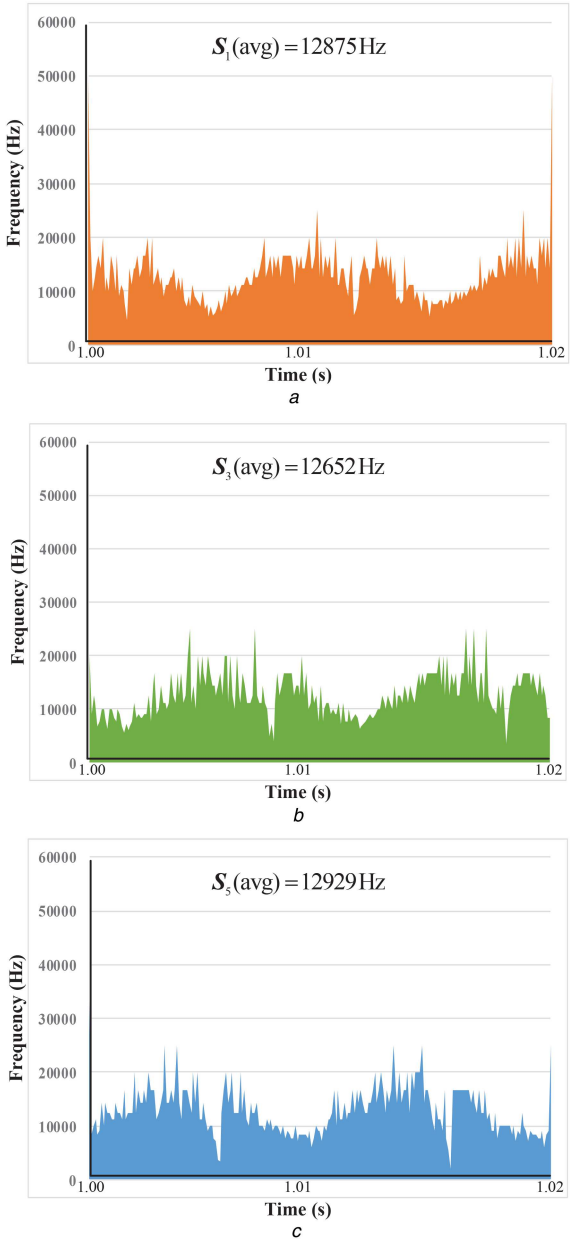

Fig. 8 *Average switching frequency after adding additional constraints*
(a) S_1, ***(b)*** S_3, ***(c)*** S_5

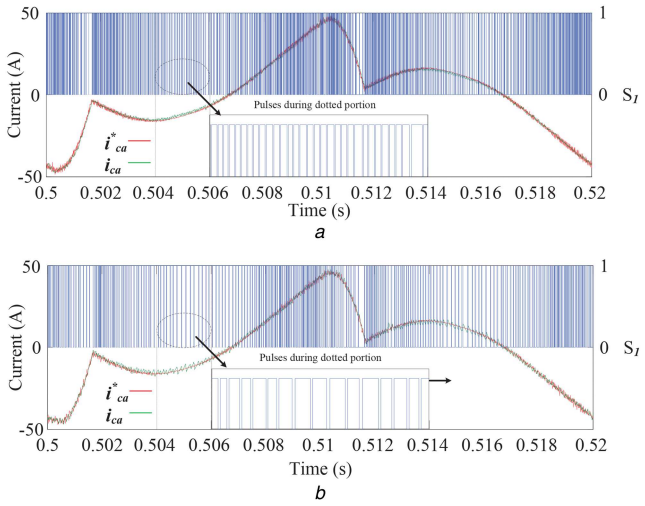

Fig. 9 *Current tracking and switching pulses comparison*
(a) Without adding switching frequency constraint, ***(b)*** After including switching frequency constraint in the cost function

Table 4 Comparison of THD and switching frequency

Parameter	THD			Switching frequency, Hz		
	i_{sa}	i_{sb}	i_{sc}	S_1	S_3	S_5
without adding additional constraints	1.57%	1.46%	1.69%	22,280	22,836	22,100
after adding additional constraints	2.42	2.41%	2.46%	12,875	12,652	12,929

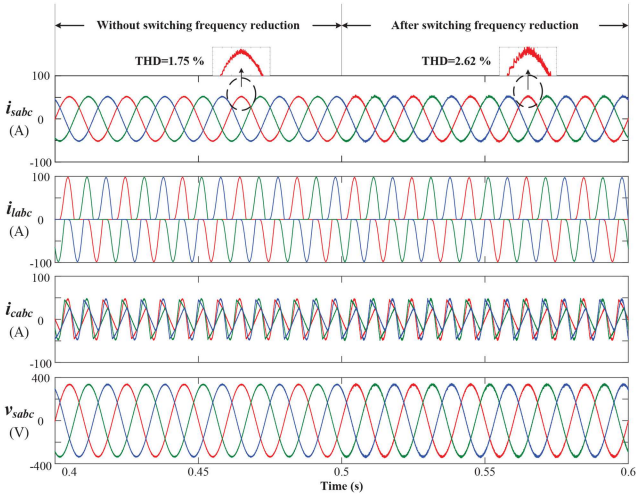

Fig. 10 *Voltages and currents without and with additional constraints during higher THD loads*

Table 5 Source currents THD and switching frequency comparison for loads with higher THD

Parameter	THD			Switching frequency, Hz		
	i_{sa}	i_{sb}	i_{sc}	S_1	S_3	S_5
without adding additional constraints	1.75%	1.72%	1.72%	28,506	28,426	28,891
after adding additional constraints	2.62%	2.65%	2.62%	17,723	18,192	17,799

Table 6 Experimental parameters

Parameter	Value
system voltage	50 V
interfacing inductor (L_f)	9 mH (with $R_f = 0.02\,\Omega$)
dc-link voltage (V_{dc})	140 V
dc capacitor (C_{dc1}, C_{dc2})	4700 μF
w_1, w_2 and w_3	0.5, 0.1 and 0.4
non-linear load	three-phase diode bridge rectifier with load 20 Ω, 150 mH
unbalanced linear load	5 Ω, 10 mH (phase-a)
—	34 Ω (phase-b)
—	17 Ω (phase-c)
sampling time (T_s)	50 μs

bridge rectifier and load-2 is a combination of load-1 and three-phase unbalanced linear load. A dSPACE MicroLabBox 1202 used as interface between the Simulink model and real-time environment. Fig. 12 shows various parameters such as PCC voltage, load currents, filter currents and source currents during load variation. In this figure, voltage scaling is 50 V/div and current scaling is 4 A/div. From Fig. 12, it is observed that during load-1, DSTATCOM injects filter currents such that the source currents are sinusoidal even though the load currents are non-linear. Similarly, during load-2 source currents are balanced and sinusoidal regardless of the unbalanced and non-linear load currents. Fig. 13 shows voltage across two capacitors of the dc link. From this figure, it is observed that complete dc-link voltage of 140 V is equally shared between the capacitors and further this voltage is constant during load variations.

Table 7 shows the THDs of source currents, switching frequencies with only current control and after including additional constraint. Initially, the THDs of source currents are 3.4, 2.7 and 1.8%, and after adding additional constraints the THD's are 3.9, 3.6 and 2.8% for a, b and c phases, respectively. Fig. 14 is also showing the THD results using power analyser (Fluke make), which supports the THD values mentioned in Table 7. The average switching frequencies of the switch in each individual leg before including the additional constraint in the cost functions are 4748, 4720 and 4803 Hz for and it is shown in Fig. 15. As mentioned that with the proposed method, the average switching frequencies are reduced after adding the switching state as a control parameter which is shown in Fig. 16 and they are given as 2807, 2823 and 2810 Hz. Therefore, from Figs. 12, 13 and 16, it is observed that the proposed VIKOR-based MPC technique is selecting an optimal switching state from the available switching states, which makes source current balanced and sinusoidal, eliminates the voltage divergence, reduces the switching frequency and also simplifying the weighting factor selection.

5 Conclusion

In this paper, MPC of TPSC DTSTACOM with VIKOR method is proposed. Capacitor voltage divergence which is the imitation of TPSC DSTATCOM topology and higher switching frequency,

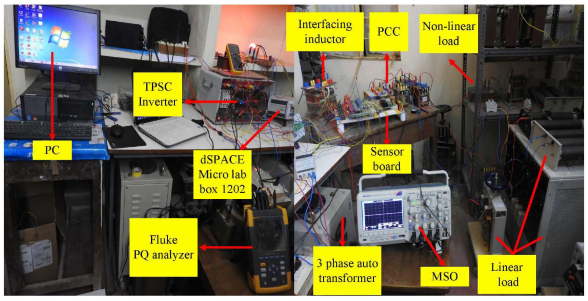

Fig. 11 *Photograph of the experimental setup*

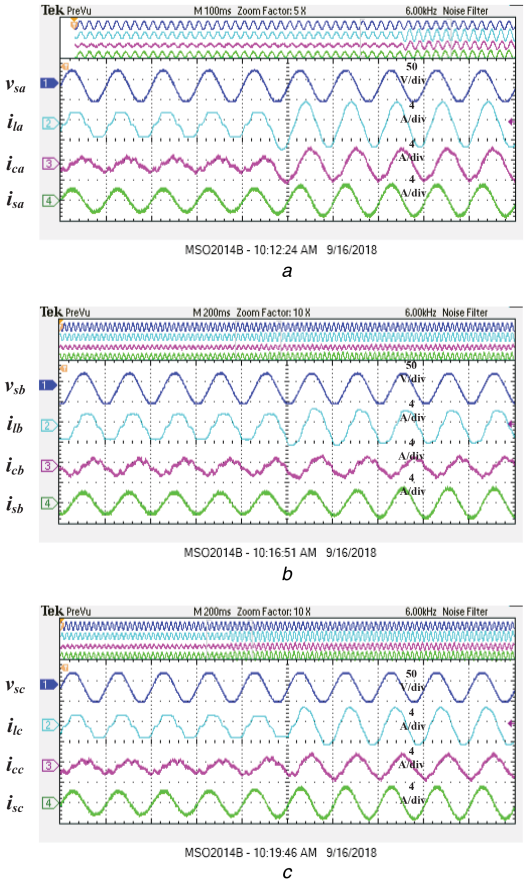

Fig. 12 *Parameters during load variation*
(a) Phase-a, ***(b)*** Phase-b, ***(c)*** Phase-c

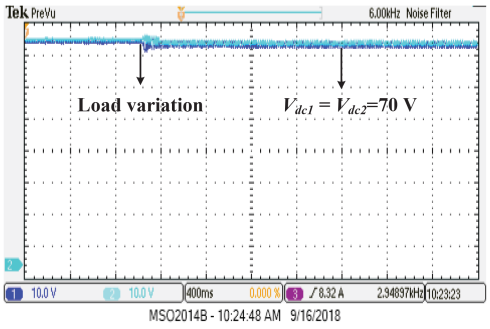

Fig. 13 *dc-Link voltage during load variation*

Table 7 THD and switching frequency during experimental studies

Parameter	THD			Switching frequency, Hz		
	i_{sa}	i_{sb}	i_{sc}	S_1	S_3	S_5
without adding additional constraints	3.4%	2.7%	1.8%	4748	4720	4803
after adding additional constraints	3.9%	3.6%	2.8%	2807	2823	2810

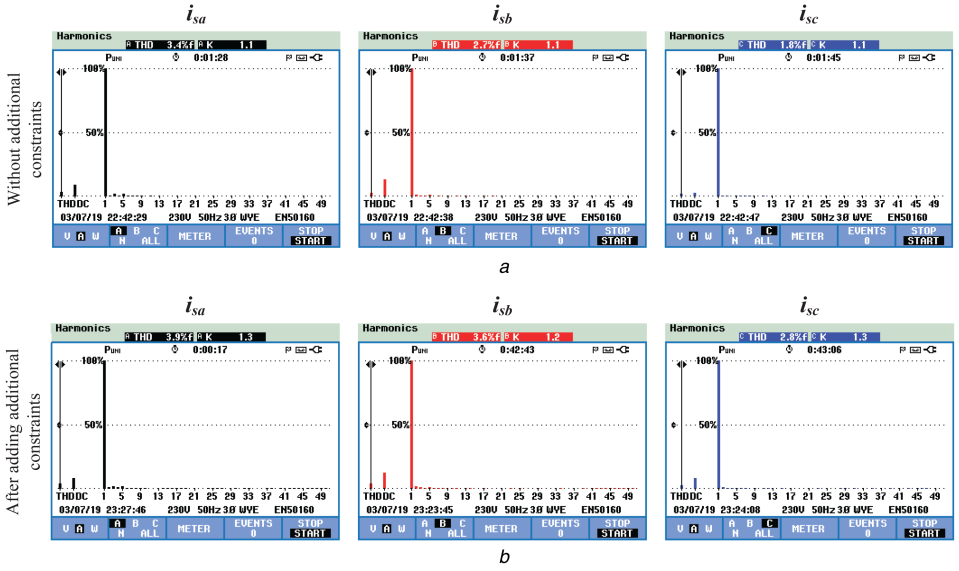

Fig. 14 *THD's of source currents*
(a) Without adding additional constraints, ***(b)*** After including additional constraints

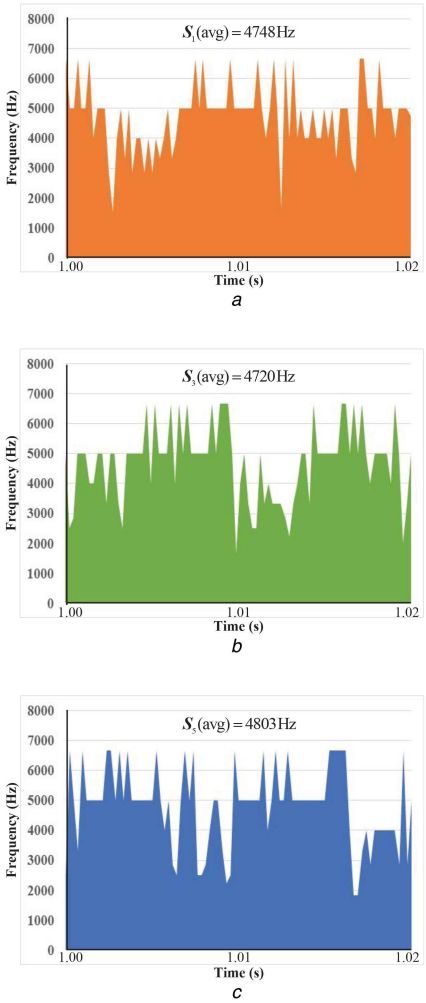

Fig. 15 *Average switching frequency without adding additional constraints during experimental test*
(a) S_1, ***(b)*** S_3, ***(c)*** S_5

which is the limitation of MPC is conquered by adding them in the cost function as two additional control parameters along with the DSTATCOM current. The weighting factor selection is simplified by using VIKOR method so that proper balance is maintained among all the control parameters of the cost function. The simulation and experimental results prove that the proposed method is efficiently compensating the current-related power quality issues, maintain equal voltage across two capacitors of dc link, reduce the switching frequency and also simplify the weighting factor selection.

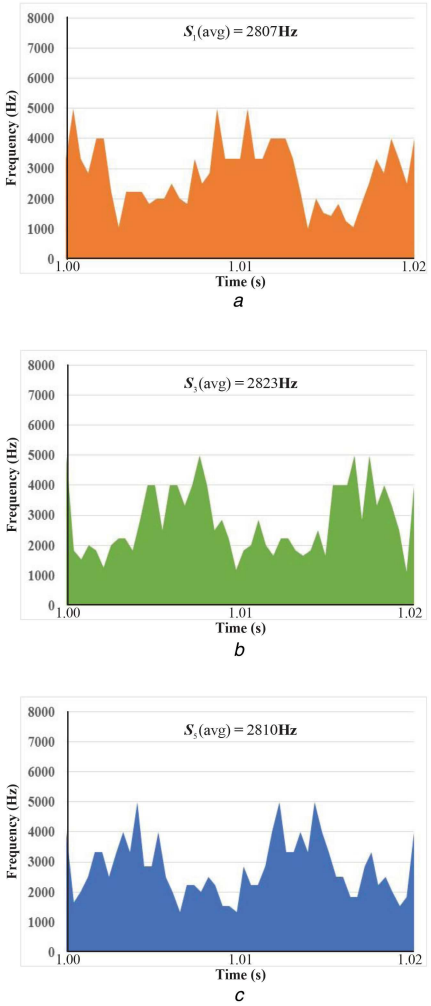

Fig. 16 *Average switching frequency after adding additional constraints during experimental test*
(a) S_1, ***(b)*** S_3, ***(c)*** S_5

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