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Modified H-bridge inverter based fault-tolerant multilevel topology for open-end winding induction motor drive

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Kedika Narender Reddy[1] ✉, *Srinivasan Pradabane*[1]

[1]*Department of Electrical Engineering, National Institute of Technology, Warangal, India*

✉ *E-mail: nit.knreddy@gmail.com*

Abstract: This study presents a three-phase modified H-bridge based multilevel inverter (MLI) topology for an open-end winding induction motor drive (OEWIMD). The operation of the proposed topology under open-circuit and short-circuit fault conditions of a switch is investigated. Proposed MLI topology is designed with three three-phase modified H-Bridge inverters connected in a star configuration to feed an OEWIMD. This topology has advantage of delivering a maximum voltage of twice the supply voltage and is replicated as nine levels in the phase windings of OEWIMD, thereby reducing the total harmonic distortion. Therefore, lower voltage rating sources such as solar cells or fuel cells can be used for this topology. This topology becomes cost effective since the operating voltage range required for the devices is less. Controlling methods such as conventional level-shifted and multi-reference sinusoidal pulse width modulation techniques can be applied for this topology. A fault-tolerance strategy is proposed for inverter switch open-circuit and short-circuit faults that adds fault-tolerance capability to the proposed topology. Simulations were performed using MATLAB/Simulink and experimental results are presented for both normal operating and fault-tolerance mode that confirms the inherent fault-tolerance property of the proposed MLI topology.

1 Introduction

In three-phase systems, for low voltage drive applications, (especially for <1 kV), voltage source inverters (VSIs) with two or three levels in the output voltage are usually employed. Whereas, for medium and high voltage applications multilevel VSIs are the best solution. Multilevel VSIs exhibit many advantages compared to conventional two-level or three-level VSIs such as increased voltage levels, improved harmonic performance, the reduced voltage stress on switching devices, the flexibility of operation with an optimum switching frequency which lowers the interference with the communication signals, lower slew rates in output voltages [1, 2]. Owing to the above advantages, multilevel converters find huge applications in HVDC transmission, flexible AC transmission interfaces for non-conventional energy sources and in low and medium power AC drives.

Topologies for multilevel outputs were realised by using open-end stator windings of induction motor. This modification (of open-end winding) provides six terminals of the three-phase stator windings. For these categories of drives, several multilevel inverter (MLI) topologies were proposed. Of all, the most adopted is the dual inverter fed open-end winding induction motor drive (OEWIMD) configuration. In this configuration, stator windings are fed from both ends with two three-phase two-level VSIs one on either end of the winding [3]. This configuration may be extended for multi-phase OEWIMD. Several switching schemes were presented in [4–6] for dual inverter configuration. Deployment of two independent DC sources eliminates the problems associated with voltage balancing across the capacitors. Due to this advantage, this configuration finds extensive industrial applications.

In [7–9], the authors presented the same topology with a single DC source. The increase in the output levels ends in complex power circuit and control circuit. In [10, 11], the authors have proposed MLI topologies with less DC sources and capacitors compared to conventional topologies. However, the drawback of these topologies is that the output voltage takes five or nine levels, but the maximum output voltage obtained across the load terminals is the same DC link voltage, which triggers to have high rating voltage sources. In the topologies presented in [12], the authors modified the hardware circuit, which delivers fault-tolerance property resulting in an increase in the cost of the circuit by 50% with a reduced output power capacity of 58% only. Moreover, in [12] the authors have put forth a cascaded inverters scheme with fault-tolerance capability with less cost compared to other topologies.

In [13], the authors proposed four-leg inverters provide fault tolerance only to switch open faults with relatively high cost [13]. Few topologies were proposed with fault-tolerance capability, but are highly complex to control. Although they might provide constant output power with the switch open and switch short faults conditions; control and operation during normal conditions is highly complex and can be used only when the reliability and constant power output are of utmost importance [13–15]. Few topologies which employ a bi-directional switch that adds the advantage of continuous operation even under some switch fault conditions were presented in [16–18]. Along with novel topologies, the authors in [19] have proposed novel control techniques, for continuous operation of the topology even under fault conditions, but with a reduction in the output voltage levels (post-fault conditions).

In [20] the authors have proposed fault-tolerant topologies with the inclusion of extra hardware with conventional flying capacitor (FC) and neutral point clamped (NPC) topologies by using additional substitutes for a faulty leg. In [21] the authors have proposed modular topologies that can be controlled by conventional sinusoidal pulse width modulation (SPWM) techniques, which exhibit fault-tolerance capability without any additional hardware. Authors have proposed various topologies for obtaining increased levels in output voltage for OEWIMD [22–24]. Complex power circuits were presented in [25] for increased levels in the output power. Modulation schemes for complex topologies for any level of outputs were also proposed [26]. In [27], the authors have proposed MLI topologies with fault-tolerant capability that is achieved through the reconfiguration of the circuit after an open-switch fault.

In [28], authors have presented modified modulation techniques for reduced switch count topology. In [29, 30], types of faults that possibly occur and the reasons for their occurrence in MLIs was analysed and presented.

Under these circumstances, a new MLI topology for OEWIMD is proposed. The proposed MLI topology is a flexible topology in view of the fact that it combines three modified three-phase H-

bridge inverters in star connection. Conventional three-phase H-bridge inverter is modified such that one of the three legs is connected at the centre of the capacitors using a bi-directional switch. Here the bi-directional switch is realised with two insulated-gate bipolar transistors (IGBTs) connected in anti-series with the common-emitter configuration where both switches are operated by same switching pulses. Three such modified inverters are used for this topology, which can deliver a maximum output voltage of twice the source voltage, V_{dc}. This output voltage is a stair of nine levels with a voltage magnitude of $0.5V_{dc}$ each across any phase winding of OEWIMD.

Modulation strategies such as SPWM technique can be applied directly for the proposed MLI topology. The modulation techniques such as level-shifted carriers (LSCs) SPWM and multi-reference SPWM with carriers in-phase disposition (IPD) are adopted for this topology. This topology ensures fault-tolerance operation of the drive under fault conditions such as a switch open-circuit or short-circuits condition with the same known modulation techniques as discussed in the following sections.

The paper is arranged as follows: Section 2 depicts the proposed topology and switching sequence of the inverter for one of the phase winding is explained. Comparison of inverter cost and component count of the proposed MLI topology with existing Nine-level inverter topologies feeding OEWIMDs is investigated. Detailed explanation about modulation strategies is presented in Section 3. Section 4 explains about fault tolerant strategies used for different fault conditions that could possibly occur in the proposed MLI topology. Experimental results for normal and various abnormal conditions are presented in Section 5 and conclusion in Section 6.

2 Proposed topology

Several topologies for OEWIMD were presented in the recent past. Out of them, commonly used topology is a dual inverter fed OEWIMD, which involves two three-phase inverters connected on either end of the windings as shown in Fig. 1. This configuration extracts the advantage of employing known three-phase VSIs to obtain a modular topology. The maximum output voltage attainable with this topology is $1.33V_{dc}$ with three levels in the output voltage [31]. Nevertheless, this configuration shortfall the advantage of direct usage of the existing PWM schemes such as SPWM. A new MLI topology is proposed for OEWIMD, which can overcome these drawbacks. The proposed MLI topology can produce a maximum output voltage of twice the input voltage (V_{dc}) with conventional SPWM techniques.

The proposed MLI topology employs three modified three-phase two-level VSIs each with an isolated DC source connected in a star configuration as depicted in Fig. 2. The switches S_{a1} through S_{a8} represent inverter-a. Similarly, the switches S_{b1} through S_{b8} and S_{c1} through S_{c8} represent inverter-b and inverter-c, respectively. Out of three output terminals of each three-phase inverters, the midpoint of first legs (between S_{a1} and S_{a4}), (between S_{b1} and S_{b4}), and (between S_{c1} and S_{c4}) is connected to the midpoint between the capacitors of the corresponding inverters using a bi-directional

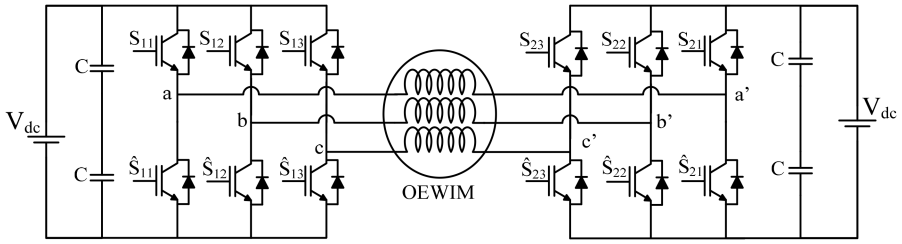

Fig. 1 *Dual-inverter fed OEWIM drive*

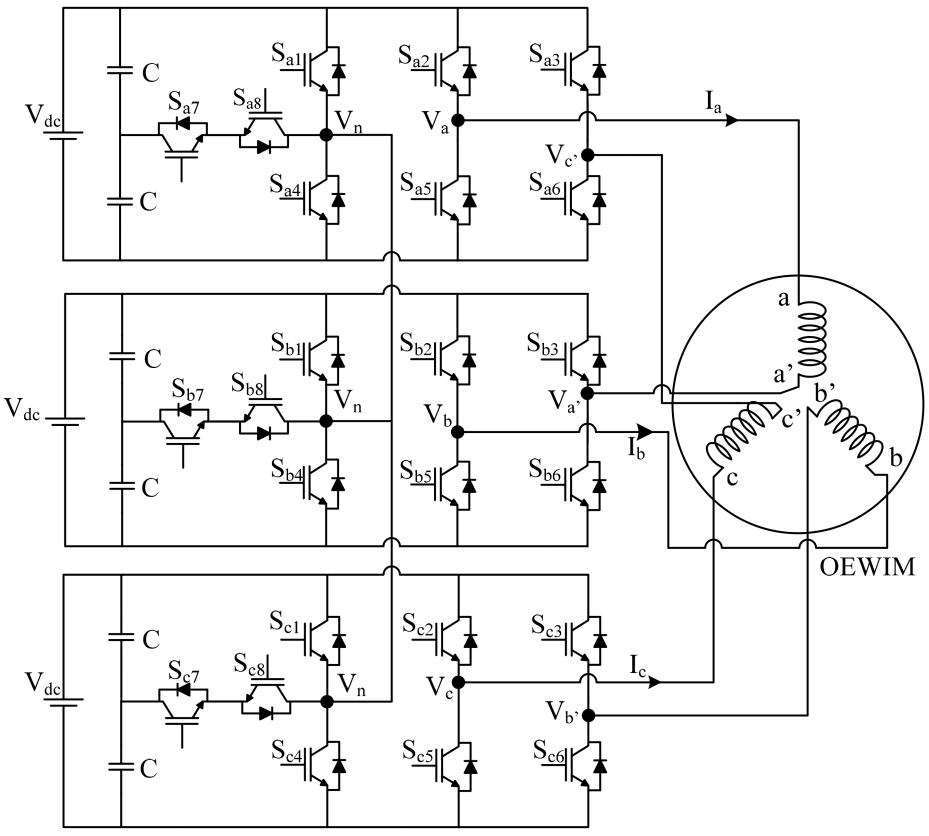

Fig. 2 *Proposed modified H-bridge MLI topology*

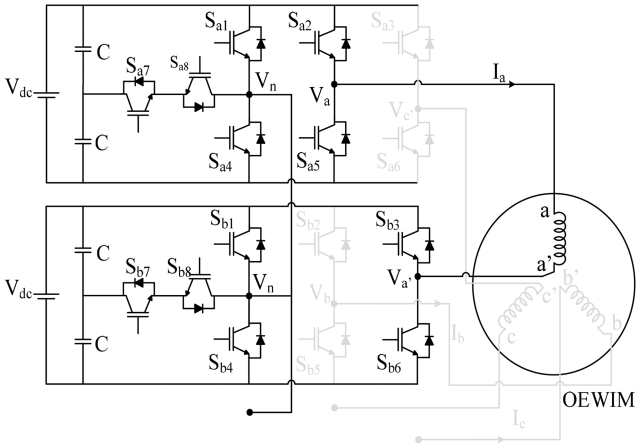

Fig. 3 *Inverter connection for phase-a winding of OEWIM*

switch, this leg is termed as modified leg of the inverter. The bi-directional switch is realised with two switches (here IGBTs) connected in anti-series. From Fig. 2, S_{a7} and S_{a8} denote the anti-series switches connected in inverter-a. Similarly, S_{b7} and S_{b8} and S_{c7} and S_{c8} represent the anti-series switches for inverter-b and inverter-c, respectively. Although, two switches S_{x7} and S_{x8} are used in all three inverters, from now on they will be treated as a bidirectional switch S_{x7} (where x ε a, b, c) since they are operated by the same switching signal with common-emitter configuration.

The output terminals of the modified legs of all the inverters are shorted which will create a neutral point by forming a star configuration of the three inverters. The other two output terminals of each VSI are connected to two different windings of the stator of the OEWIMD as illustrated in Fig. 2. Comparing this topology with the dual inverter, an extra VSI along with a DC source is required additionally but provides increased maximum output voltage, i.e. $2V_{dc}$ whereas $1.33V_{dc}$ in case of the dual inverter. This result in increased output power or for the same power rating, the voltage ratings of the DC sources used can be reduced which would lower the blocking voltages of the switches. This gives more scope for using lower power rating high frequency switching semiconductor switches such as MOSFETs, which is an added advantage. Another advantage with the proposed topology is the possibility of direct application of conventional PWM schemes such as level-shifted PWM, multi-carrier PWM schemes, even for fault-tolerance operating conditions. The topology connection considering only phase a of the OEWIMD is shown in Fig. 3.

From the analysis of Fig. 3, the different output voltage levels that can be obtained across the terminals of the motor phase a winding for various combinations of switching states are presented in Table 1. The combination of the second leg of inverter-a and third leg of inverter-b along with modified legs of both the inverters are presented since these legs affect the voltage that is applied across the motor phase a winding. From Table 1 and Fig. 3, it can be observed that the maximum voltage across the terminals of phase a obtained is twice the supply voltage V_{dc} resulted by connecting the two DC sources in series.

Note that V_{DC} is the DC-link voltage required by a conventional three-phase inverter, whereas V_{dc} mentioned in the proposed circuit configuration is half the DC-link voltage i.e., $V_{dc} = V_{DC}/2$.

The output voltages across the terminals are dependent on the states of the power switches. Consider the switches are ideal, their conduction and blocking states are represented by binary variables as 1 and 0, respectively.

i.e. if $S_{xy} = 1$ then $S_{xz} = 0$,
-switch S_{xy} is ON and switch S_{xz} is OFF
if $S_{xz} = 1$ then $S_{xy} = 0$,
-switch S_{xz} is ON and switch S_{xy} is OFF.
Where x ε a, b, c & y ε 2, 3, & z ε 5, 6.

Likewise for switches 1, 4, & 7 of all the inverters, the switching condition would be
if $S_{x1} = 1$, then $S_{x4} = S_{x7} = 0$,
-switch S_{x1} is ON, S_{x4}, and S_{x7} are OFF,
if $S_{x4} = 1$, then $S_{x1} = S_{x7} = 0$,
-switch S_{x4} is ON, S_{x1}, and S_{x7} are OFF,
Similarly, if $S_{x7} = 1$, then $S_{x1} = S_{x4} = 0$,
-switch S_{x7} is ON, S_{x1}, and S_{x4} are OFF, and $S_{x7} = \hat{S}_{x1} + \hat{S}_{x4}$.
With this representation, output voltages undergoing various voltage levels can be written in accordance with

$$V_{aa'} = (1/2)V_{dc} * (V_{an} - V_{na'}); \quad (1)$$

where

$$V_{an} = [\hat{S}_1 (S_2 \hat{S}_4 \hat{S}_5 S_7 + 2 S_2 S_4 \hat{S}_5 \hat{S}_7) +$$

$$(S_4 - 1)*(\hat{S}_1 \hat{S}_2 S_5 S_7 + 2 S_1 \hat{S}_2 S_5 \hat{S}_7)]_a \text{ and}$$

$$V_{na'} = [\hat{S}_1 (S_3 \hat{S}_4 \hat{S}_6 S_7 + 2 S_3 S_4 \hat{S}_6 \hat{S}_7) +$$

$$(S_4 - 1)*(\hat{S}_1 \hat{S}_2 S_6 S_7 + 2 S_1 \hat{S}_3 S_6 \hat{S}_7)]_b$$

$$\text{Similarly, } V_{bb'} = (1/2)V_{dc} * (V_{bn} - V_{nb'}); \quad (2)$$

$$V_{cc'} = (1/2)V_{dc} * (V_{cn} - V_{nc'}); \quad (3)$$

Here, $\hat{S}_x$ - represents complementary of switch S_x switching signal.

A comparison of component count of the proposed MLI topology with existing nine-level topologies in terms of various parameters such as number of levels in the output voltage (N_L), number of switches (N_{sw}), number of DC sources (N_{source}), number of gate drivers (N_{driver}), number of diodes (N_{diode}), number of capacitors ($N_{capacitor}$), total blocking voltage (TBV) in p.u. and total component count and is illustrated in Table 2. As can be seen from Table 2, both NPC and FC topologies require only one DC source with a voltage rating of V_{DC}; whereas conventional cascaded H bridge (CCHB) requires 12 isolated DC sources of the voltage rating of $V_{DC}/8$. Similarly, asymmetrical CHB (ACHB) requires three isolated DC sources of voltage rating $3V_{DC}/8$ and three controlled DC sources of voltage rating $V_{DC}/8$. The topology proposed in [11, 21] requires two and three isolated DC sources, respectively of voltage rating V_{DC}. The topology in [22] requires only one dc source of voltage rating $V_{DC}/2$. The topology in [23] requires isolated DC sources of voltage rating $3V_{DC}/4$ and $V_{DC}/4$ for each phase and the topology in [24] requires six isolated DC sources of voltage rating $V_{DC}/12$. The proposed topology requires three isolated DC sources of voltage rating $V_{DC}/2$. From Table 2, the component count for topology in [21] is least of all but the number of levels in the output is five and the number of components required for the proposed topology is less when compared with other existing nine-level topologies. The TBV

Table 1 Voltage of phase-a winding ($V_{aa'}$) according to switching states

$V_{aa'}$	Inverter-a					Inverter-b				
	S_{a1}	S_{a2}	S_{a4}	S_{a5}	S_{a7}	S_{b1}	S_{b3}	S_{b4}	S_{b6}	S_{b7}
$2V_{dc}$	0	1	1	0	0	1	0	0	1	0
$1.5V_{dc}$	0	1	1	0	0	0	0	0	1	1
	0	1	0	0	1	1	0	0	1	0
V_{dc}	0	1	1	0	0	1	1	0	0	0
	0	1	1	0	0	0	0	1	1	0
	1	1	0	0	0	1	0	0	1	0
	0	0	1	1	0	1	0	0	1	0
$0.5V_{dc}$	0	1	0	0	1	1	1	0	0	0
	0	1	0	0	1	0	0	1	1	0
	1	1	0	0	0	0	0	0	1	1
	0	0	1	1	0	0	0	0	1	1
0	1	1	0	0	0	0	0	1	1	0
	0	0	0	0	0	0	0	0	0	0
	1	1	0	0	0	1	1	0	0	0
	0	0	1	1	0	1	1	0	0	0
	0	0	1	1	0	0	0	1	1	0
$-0.5V_{dc}$	0	0	0	1	1	1	1	0	0	0
	0	0	0	1	1	0	0	1	1	0
	1	1	0	0	0	0	1	0	0	1
	0	0	1	1	0	0	1	0	0	1
$-V_{dc}$	1	0	0	1	0	1	1	0	0	0
	1	0	0	1	0	0	0	1	1	0
	1	1	0	0	0	0	1	1	0	0
	0	0	1	1	0	0	1	1	0	0
$-1.5V_{dc}$	1	0	0	1	0	0	1	0	0	1
	0	0	0	1	1	0	1	1	0	0
$-2V_{dc}$	1	0	0	1	0	0	1	1	0	0

Table 2 Component count comparison of the proposed MLI with other MLI topologies feeding OEWIMDs

MLI type	N_L	N_{sw}	N_{driver}	N_{diode}	N_{source}	$N_{capacitor}$	TBV(p.u.)	Component count
NPC	9	48	48	168	1	9	48	274
FC	9	48	48	48	1	85	48	230
CCHB	9	48	48	48	12	12	48	168
ACHB	9	24	24	24	6	6	24	84
topology in [11]	9	36	36	36	2	12	36	122
topology in [21]	5	18	18	18	3	0	18	57
topology in [22]	5	24	24	24	1	3	24	76
topology in [23]	17	36	36	36	6	9	36	123
topology in [24]	7	48	48	60	6	6	48	168
proposed Topology (Pr.Top.)	9	24	24	24	3	6	24	81

Table 3 Price comparison of the proposed MLI topology with other MLI topologies feeding OEWIMDs

Part	Part Number	Ratings	Unit Price*($)	NPC	FC	CCHB	ACHB	[11]	[21]	[22]	[23]	[24]	Pr Top.
MOSFETs	IRFP240PBF	200 V, 20 A	2.1					12	18		12		
	IRFP140PBF	100 V, 20 A	1.93				12	12		24	12		24
	IRFIZ34GPBF	60 V, 20 A	1.28	48	48	48	12	12			12	48	
diodes	STPS20SM60D	60 V, 20 A	1.24	168								12	
capacitor	LLG2D222-MELC40	200 V, 2.2 mF	6										6
	LLS2A222-MELA	100 V, 2.2 mF	3.93	9	85	12	6	12		3	9	6	
gate driver	IR2110STRPBF		1.34	48	48	48	24	36	18	24	36	48	24
total cost ($)				369.45	459.81	172.92	94.26	159.12	61.92	90.27	147.33	164.22	114.48

Courtesy: www.galco.com, www.digikey.in. * Price may vary subjected to market growth.

remain same as the switch count for NPC, FC, and CCHB topologies because the maximum blocking voltage and peak inverse voltage (PIV) of switches are same as the source voltage of the topology.

To further asses the lucrative merits of the proposed topology, a cost comparison based on the cost-influencing factors that dictate the overall cost of the inverter is done and illustrated in Table 3. In order to evaluate the merits of a case study with a load of 2 kW with an input voltage V_{DC} of 200 V is considered [32]. The ratings of the components are chosen in accordance with the configuration of the topologies under comparison. The total cost for each

topology is enlisted in Table 3. The cost evaluation assigns equal importance to the number of components, TBV, and PIV while considering voltage rating and current rating of the components without margin. However, components of lower voltage rating are selected considering rated current parameters. It can be seen from Table 3 that the cost of the inverter circuit in [21] is less comparatively and the cost of the proposed topology is lower than all other nine-level topologies except ACHB. However, the ACHB is to be operated with controlled and uncontrolled DC sources, which makes it operation typical. Therefore, the proposed topology has the least component count and has comparatively low cost for the inverter that makes its usage viable.

3 Modulation strategies

The proposed modified H-bridge MLI topology can be controlled by conventional SPWM techniques, which are usually used for controlling multilevel topologies as explained in [33, 34]. Therefore, SPWM techniques such as LSCs (IPD) and multi-reference LSC SPWM techniques are implemented for this topology.

3.1 LSC SPWM

LSC-IPD SPWM scheme is used to generate switching pulses for the proposed MLI. This switching scheme's operating principle applied to inverter-a of the proposed MLI topology is illustrated in Fig. 4. For the other two inverters *b* and *c*, the sinusoidal reference and carrier waves are phases shifted by 120° and 240°, respectively. This operation scheme is identical to conventional SPWM schemes used for multilevel topologies. A sinusoidal reference will be compared with four LSC. The carriers V_{cr1} and V_{cr2} are level shifted above zero and carriers V_{cr3} and V_{cr4} are levels shifted below zero as shown in Fig. 4. The switching pulses are generated by comparison and with the logic circuits. The switches S_{x2}–S_{x3} and switches S_{x5}–S_{x6} are switched simultaneously. The switching pulses for switches S_{x2}–S_{x3} and switches S_{x5}–S_{x6} are complementary and will be active high (switch ON) for half cycle and active low (switch OFF) for another half cycle of sinusoidal reference. These switches (legs) are directly connected to phase windings of the stator of OEWIM.

The switches connected in the neutral leg are driven with pulses generated by comparing sinusoidal reference with LSC.

Comparison of reference wave with carriers V_{cr2} and V_{cr4} will generate pulses for switch S_{x1} and comparison of reference wave with carriers V_{cr1} and V_{cr3} will generate pulses for switch S_{x4}. The complementary pulses of switches S_{x1} and S_{x4} are given to bidirectional switch S_{x7}. With this configuration of modified three-phase H-bridge, each inverter generates voltages in five levels between each phase leg and neutral leg. The connections of the stator windings in this proposed MLI topology are transposed such that nine voltages levels are obtained across each phase winding (see (1)–(3)).

3.2 Multi-reference SPWM

Level-shifted multi-reference IPD (LSMR-IPD) SPWM scheme is applied for the proposed MLI topology. Fig. 5 shows the modulation scheme adopted for inverter-a of the proposed MLI topology. Like in LSC-IPD technique mentioned in the above section, the switching of devices S_{x2}–S_{x3} and S_{x5}–S_{x6} are simultaneously done and switching pulses will be complementary and will be active high for half cycle and active low for another half cycle of the sinusoidal reference V_{ref1}. These switches (legs) are directly connected to phase windings of the stator of OEWIM. In this scheme, two sinusoidal reference waves (V_{ref1} and V_{ref2}) and three LSC waves (V_{cr1}, V_{cr2}, and V_{cr3}) are employed. Carriers V_{cr1} is level shifted above zero and carriers V_{cr2} and V_{cr3} are levels shifted below zero. Two references used are level shifted, where the shift is equal to the magnitude of one carrier used. These references are compared with LSCs to generate switching pulses as shown in Fig. 5. Comparison of reference V_{ref1} with carrier V_{cr1} and V_{cr3} will yield the switching pulses for switch S_{x1} and comparison of reference V_{ref1} with carrier V_{cr2} and reference V_{ref2} with carrier V_{cr1} will generate pulses for switch S_{x4}. The complementary pulses of switches S_{x1} and S_{x4} are summed up and given to bidirectional switch S_{x7}. Figs. 6*a* and *b* illustrate the block diagram for switching signals generation for one of the inverters using LSC-IPD technique and LSMR-IPD, respectively.

The connections of the stator windings here are transposed such that nine voltages levels are obtained across each phase winding. Since the resultant voltage across any phase is the phasor sum of two voltages, which are phase shifted by 120°, its fundamental component value will be equal to $\sqrt{3}V_{dc}$, which is faintly $<2V_{dc}$. Fig. 7 shows the switching signals for two cycles for switches in one inverter generated from dSPACE 1104.

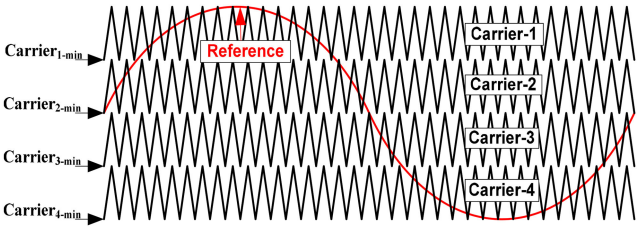

Fig. 4 *LSC-IPD SPWM used in the proposed MLI topology*

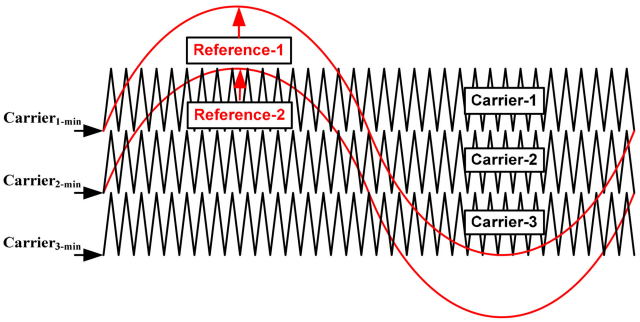

Fig. 5 *LSMR-IPD SPWM used in the proposed MLI topology*

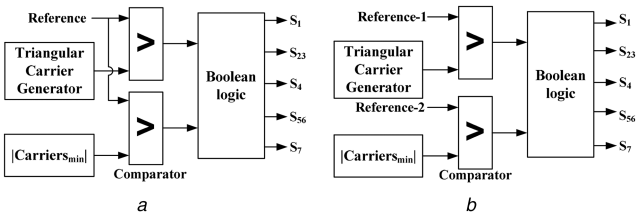

Fig. 6 *Block diagram of switching circuit for the proposed inverter*
(a) Using LSC-IPD SPWM technique, ***(b)*** Using LSMR-IPD SPWM technique

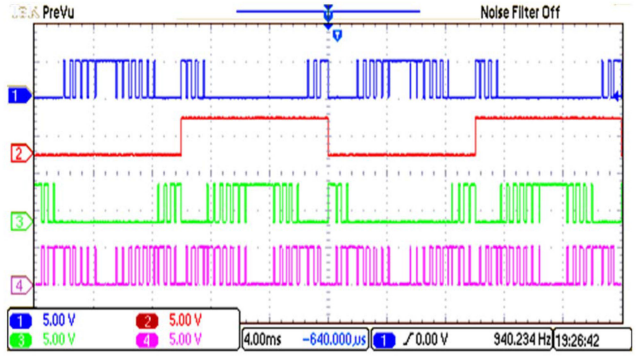

Fig. 7 *Switching pulses for switches S_1 (blue trace), S_{23} (or) $\hat{S}_{56}$ (red trace), S_4 (green trace), S_7 (pink trace) for inverter-a obtained from dSPACE*

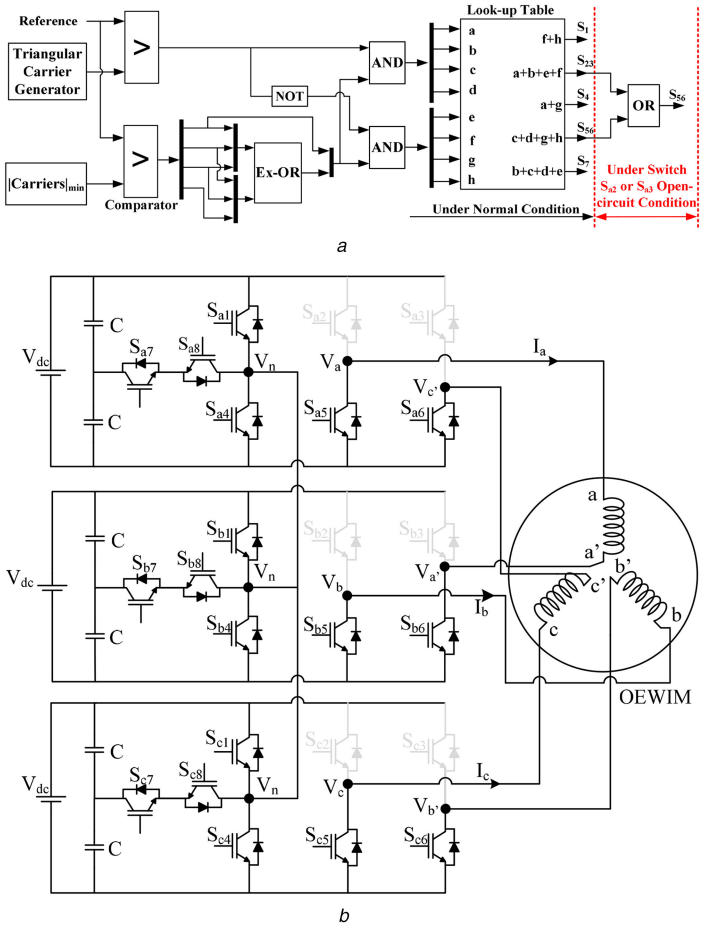

Fig. 8 *Circuits for implementation of Fault Tolerance Strategy*
(a) Schematic diagram of switching circuit for inverter-a with LSC-IPD for normal and fault-tolerance condition, ***(b)*** Working state circuit of proposed topology after applying FTS

4 Proposed fault tolerance strategy (FTS)

The proposed MLI topology is characterised by fault-tolerance capability under switch open-circuit and short-circuit conditions without requirement of any additional hardware but by post-processing of the switching PWM signals. During switch open-circuit or short-circuit condition in any of the inverter leg, the converter topology continues to operate without any changes in the modulation technique that is being used before the fault has occurred.

4.1 For switch open-circuit faults

For switch open-circuit faults in legs, which are connected to motor phase windings in any of the inverters, the number of levels in the output voltage will reduce from nine to seven and the maximum output voltage applied across the phase windings are reduced from $2V_{dc}$ to V_{dc} or $-2V_{dc}$ to $-V_{dc}$. This will affect only the winding connected to the faulty leg of the inverter, which will result in unbalanced supply voltage for the OEWIMD. For switch open-circuit faults in switches S_{x1} and S_{x4} in the modified leg, which are connected to neutral, the number of levels in the output voltage, are reduced from nine to eight and the maximum output voltage gets reduced from $2V_{dc}$ to $1.5V_{dc}$ or from $-2V_{dc}$ to $-1.5V_{dc}$. This will affect two windings connected to that faulty inverter. If the switch open-circuit fault occurs in the bidirectional switch, then the output voltage gets distorted and the currents in the two windings connected to such faulty inverter get affected.

Therefore, with FTS for open-circuit fault in any switch except bidirectional switch S_7, in any of the inverter, the switches in the position of the faulty switch in other inverters are to be turned-OFF completely. Along with this, the switching signals of both faulty switch and healthy switch are to be given to the healthy switch in all the inverters.

For example, if the switch S_{a2} or switch S_{a3} gets open circuited then switches S_{b2} and S_{b3} and S_{c2} and S_{c3} has to be turned-OFF. The switching pulses of S_{a2} and S_{a3} have to be given to S_{a5} and S_{a6}, respectively along with switching pulses of S_{a5} and S_{a6} as shown in Fig. 8*a*. Likewise, switching pulses of S_{b23} and S_{b56} has to be given to S_{b5} and S_{b6} and switching pulses of S_{c23} and S_{c56} has to be given to S_{c56}. Fig. 8*b* illustrate working of the proposed topology after applying FTS for switch S_{a2} open-circuit fault condition. Similarly, if switch S_7 gets open-circuited, then all the switches in a similar position in other inverters have to be open circuited, i.e. if S_{a7} gets open circuited then switches S_{b7} and S_{c7} are also open circuited. This will provide identical switching of inverters and balanced voltage for the OEWIMD.

4.2 For switch short-circuit faults

If a short-circuit fault occurs in any one switch of the leg, then the inverter leg will create a short circuit across the source and draws heavy currents. It will result in reduced levels in output voltage. Hence, if any switch gets short-circuited, then immediately another switch in the corresponding leg has to be turned-OFF.

FTS for switch short-circuit faults will be opposite to the one mentioned in FTS for open-circuit fault, i.e. instead of turning-OFF of the switches in similar positions of the other inverters, here switches are turned-ON completely and healthy switches are turned-OFF completely. For example, if switch S_{a2} gets short-circuited, then switch S_{a5} has to be turned-OFF. The switches S_{b5} and S_{c5} are to be turned-OFF completely and switches S_{b2} and S_{c2} are to be turned-ON completely. For short-circuit faults in any switch of the modified leg, the other two healthy switches have to be turned-OFF completely. In addition, the switches in similar position of the other inverters have to be turned-ON completely and other two healthy switches in other inverters have to be turned-

OFF completely. For example, if switch S_{a1} gets short-circuited, then switches S_{a4} and S_{a7} are to be turned-OFF completely and switches S_{b1} and S_{c1} are to be turned-ON completely and switches S_{b4}, S_{b7}, S_{c4}, and S_{c7} are to be turned-OFF.

5 Experimental results

The proposed MLI topology based on three modified three-phase H-Bridge inverters, each with isolated 100 V DC source is experimentally implemented to feed 1-hp OEWIM. The proposed topology is simulated with conventional SPWM techniques. The open-circuit and short-circuit fault conditions of the switches are then introduced at a suitable interval of time and its response is captured in oscilloscopes. The application of the proposed FTS algorithm is simulated in the MATLAB/Simulink environment. The switching pulses for the prototype are dispensed using dSPACE 1104. A sinusoidal reference wave of 50 Hz is compared with the triangular carrier signal of 1.5 kHz to generate switching pulses. The experimentally obtained waveforms for the voltages and currents from the star connected VSI MLI topology using

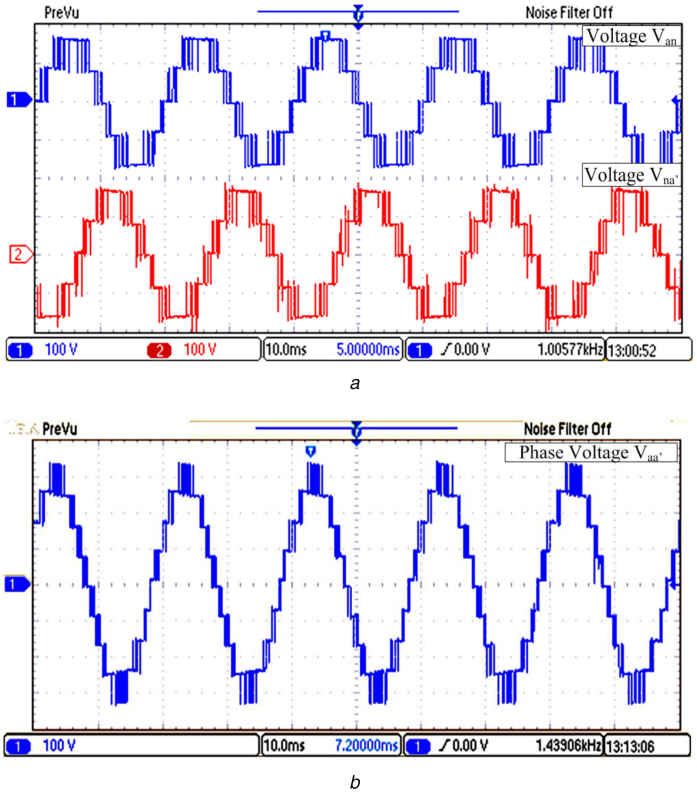

Fig. 9. *Experimental results of*
(a) Voltages V_{an} and voltage V_{na}', ***(b)*** Phase voltage V_{aa}'

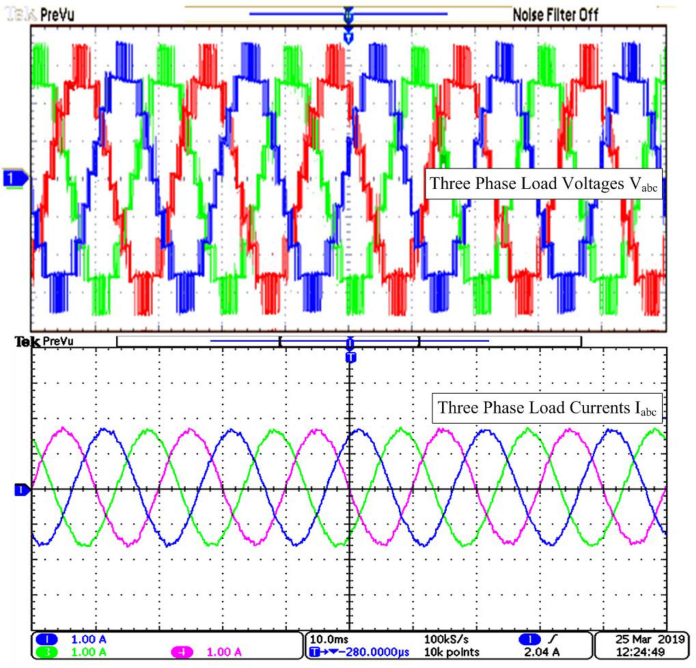

Fig. 10 *Motor phase voltages with 50 V/div in top trace: V_{aa}' (red), V_{bb}' (blue), V_{cc}' (green); and no-load motor phase currents in bottom trace: i_a (blue), i_b (green), i_c (pink)*

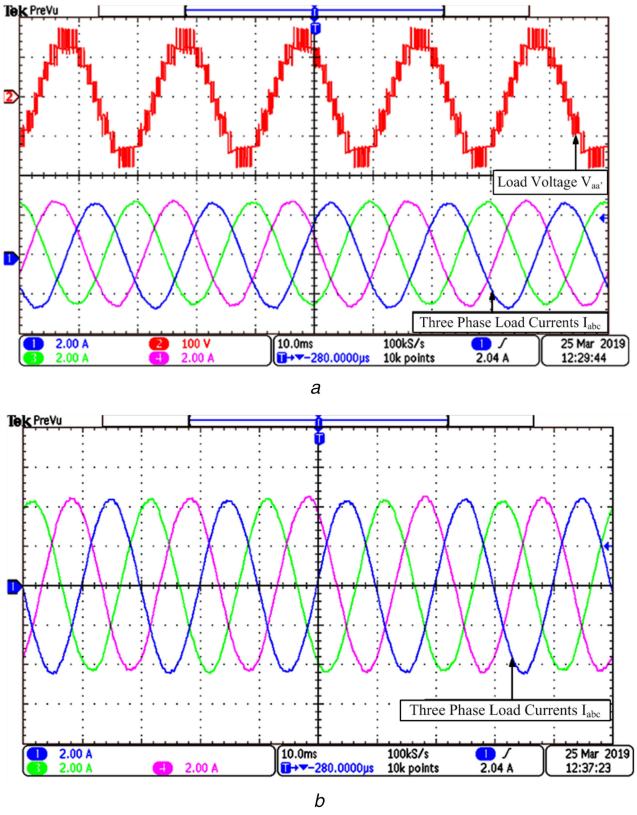

Fig. 11 *Experimental results of*
(a) Load voltage $V_{aa'}$ and three phase load currents I_{abc} for 2 A of load current, ***(b)*** Three phase load currents I_{abc} for 3.2 A of load current

LSPWM strategy is illustrated in Fig. 9 and 10. Fig. 9*a* represents voltage V_{an}, the voltage across points 'a' and neutral, whereas voltage $V_{na'}$, is the potential across the point 'a'' and neutral (from inverter-b) and Fig. 9*b* represents the voltage $V_{aa'}$ across the phase-*a* winding.

The output voltage waveforms of the inverter-a and inverter-b have five possible voltage levels ($+2V_{dc}, +V_{dc}, 0, -V_{dc}$ and $-2V_{dc}$). Hence the load voltage across any phase winding will have nine output voltages ($-4V_{dc}, -3V_{dc}, -2V_{dc}, -V_{dc}, 0+V_{dc}, +2V_{dc}, +3V_{dc}$, and $+4V_{dc}$) because the load voltage is the difference between the output voltages of inverter-a and inverter-b. This is evident for the multilevel operation of the proposed topology with the output voltage magnitude twice that of the DC source. Fig. 10 depicts the experimentally obtained waveforms of three-phase motor phase voltages and no-load currents of the OEWIM. The top trace in Fig. 11*a* indicates the motor phase voltage $V_{aa'}$ whereas the bottom trace in Figs. 11*a* and *b* depicts the motor phase currents for a load current of 2 A and full load rated current of 3.2 A, respectively, with a current scale of 2 A/div.

Fig. 12*a* shows the harmonic spectrum of the phase-*a* load voltage ($V_{aa'}$) and Fig. 12*b* shows the harmonic spectrum of current in phase-*a* for LSPWM-IPD strategy. It is clear from the spectrum that the dominant harmonics are crowded around the range of carrier frequency and its integral multiples. The measured total harmonic distortion (THD) of the unfiltered output voltage was $THD_v = 11\%$ similarly the THD of load current was $THD_i = 3\%$, confirming very low distortion of the currents in the load. Since both the switching strategies (mentioned in Section 3), when applied this proposed topology will yield identical output for all operating conditions. Hence, LSPWM-IPD is explicitly considered in the experimental analysis of the proposed topology.

The output load voltage of phase-*a* or voltage across phase-*a* winding ($V_{aa'}$) for various values of modulation indices is illustrated in Fig. 13. From this, it is observed that the proposed topology can operate at any modulation index (for $M_i = 1$, 0.8, 0.6, 0.4, 0.2). Reduction in the value of M_i will reduce the levels in the output voltage.

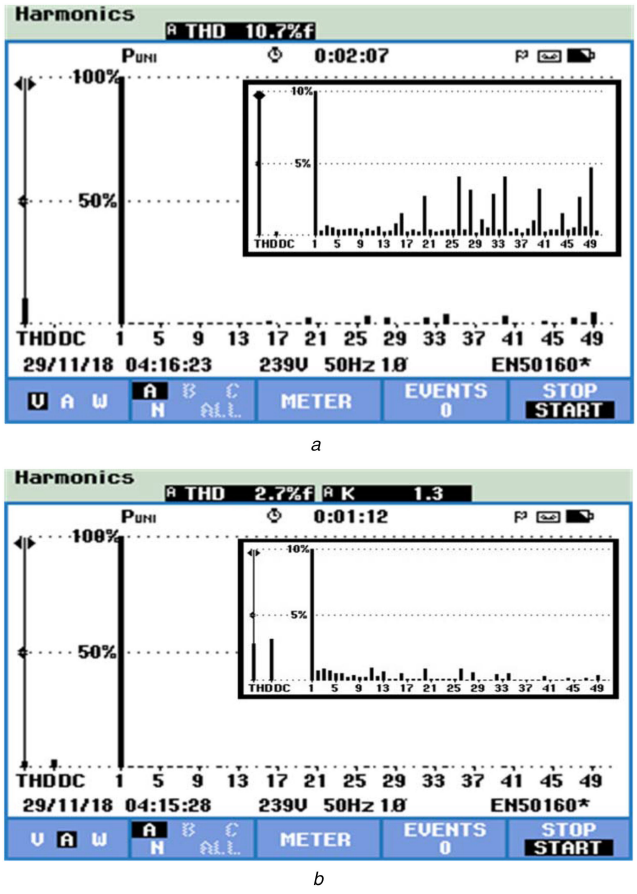

Fig. 12 *Experimental results of*
(a) FFT analysis of motor phase voltage, $V_{aa'}$ and its zoomed view (inside), ***(b)*** FFT Analysis of motor phase current i_a and its zoomed view (inside)

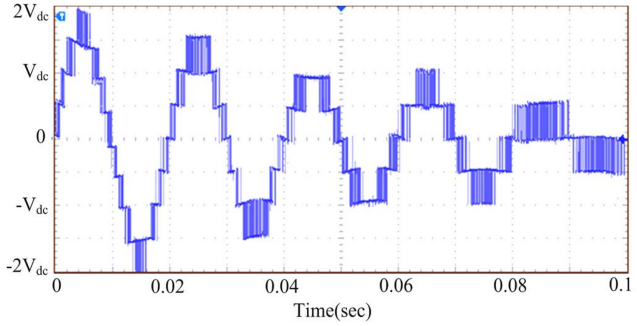

Fig. 13 *$V_{aa'}$ with modulation indices, $M_i = 1$ from 0 to 0.02 s, $M_i = 0.8$ from 0.02 to 0.04 s, $M_i = 0.6$ from 0.04 to 0.06 s, $M_i = 0.4$ from 0.06 to 0.08 s, $M_i = 0.2$ from 0.08 to 0.1 s*

5.1 For switch open-circuit faults

The proposed MLI topology under switch open-circuit and short-circuit conditions are tested with LSPWM-IPD strategy. For the sake of clarity, two cases of open-circuit faults are considered. First, if the fault occurs in any one switch (S_{x1} or S_{x4}) of the first leg of the inverter, which formed the neutral point (V_n). To affect the supposedly considered open-circuited fault condition of S_{a1}, the switching pulses are disengaged from S_{a1} and the corresponding results were presented in Fig. 14. Fig. 14 shows the phase-a voltage across the motor winding ($V_{aa'}$) and three-phase no-load motor phase currents i_a (blue trace), i_b (green trace), and i_c (pink trace) under with switch S_{a1} open circuited at time $t = 50$ ms. The waveform of $V_{aa'}$ appears to have reduced voltage levels in the

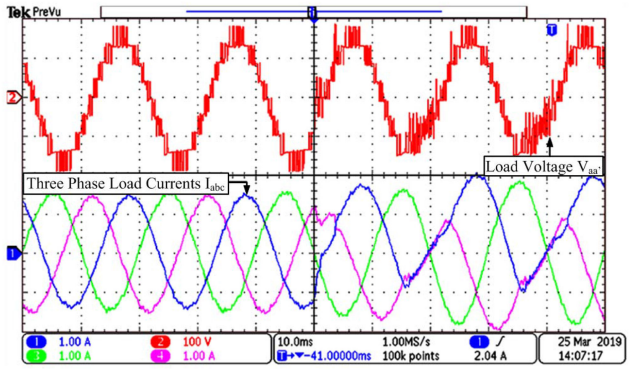

Fig. 14 *Waveforms of $V_{aa'}$ (top trace in red) and no-load phase currents i_a (blue), i_b (green), i_c (pink) with S_{a1} open-circuit fault at t = 50ms*

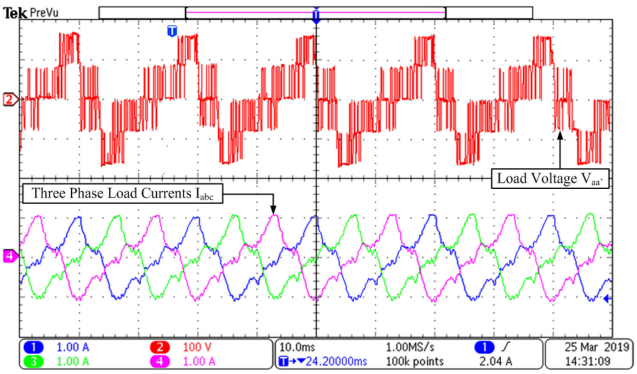

Fig. 15 *Waveforms of $V_{aa'}$ (top trace) and no-load phase currents i_a (blue), i_b (green), i_c (pink) with FTS for S_{a1} open-circuit fault*

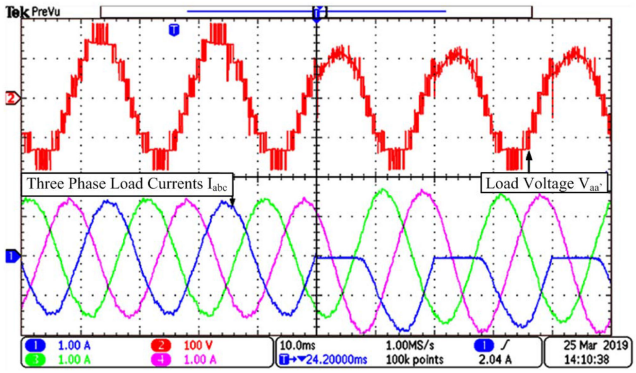

Fig. 16 *Waveforms of $V_{aa'}$ (top trace) and no-load phase currents i_a (blue), i_b (green), i_c (pink) for S_{a2} open-circuit fault at t = 50ms*

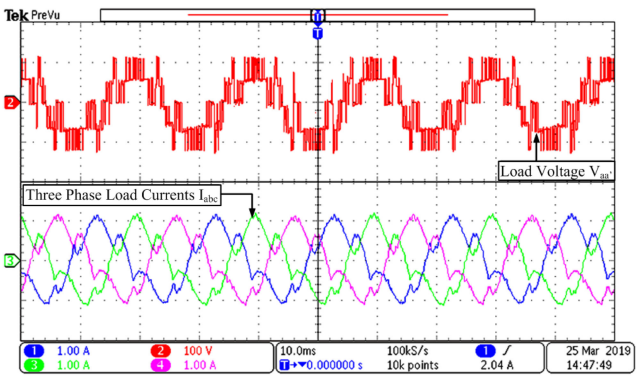

Fig. 17 *Waveforms of $V_{aa'}$ (upper trace) and no-load phase currents i_a (blue), i_b (green), i_c (pink) with FTS for S_{a2} open-circuit fault*

negative cycle with distortions. From the current traces of i_a and i_c, it is observed that they are unbalanced and possess DC component, while the i_b is undisturbed (as elucidated in Section 3). For S_{a1} open-circuited condition, the proposed FTS (as discussed in Section 4.1) is applied to the switching pulses of the inverters and the experimental results were presented in Fig. 15. Both $V_{aa'}$ and no-load currents across the three-phase windings of the motor appears to be balanced. The current waveforms may not be sinusoidal but are balanced and symmetrical without DC component. Applying FTS will ensure continuous operation of the OEWIM drive without any circuit hardware alterations.

On the other hand, consideration is the occurrence of an open-circuit fault in any switch (S_{x2} through S_{x6}) of the legs from where the motor phase windings are connected. For simplicity, assuming the open-circuit fault on switch S_{a2} of the second leg of inverter-a, from where one of the phase-a terminals of the OEWIM is connected.

Fig. 16 depicts the phase-a voltage across the motor winding ($V_{aa'}$) and the three-phase currents under no-load condition with switch S_{a2} open circuited at time $t = 50$ ms. The waveform of $V_{aa'}$ appears to have reduced voltage levels in the positive half cycle with distortions. Again from the same figure, the three-phase no-load motor phase currents i_a (blue trace), i_b (green trace), and i_c (pink trace) are depicted. At the occurrence of a fault, both i_b and i_c are undisturbed, while the phase-a current (i_a) appears to have high DC content. It is observed from i_a trace, the nature of current waveform in the motor phase-a winding of OEWIM is similar to a half-wave rectifier output, which is not desirable. This undesirable current waveform may cause further complications affecting the power circuit configuration and the performance of the OEWIM drive system. To address this situation, the proposed FTS algorithm is applied, i.e. the switching pulses supplied to the healthy switches of the inverters are amended (as discussed in Section 4.1). Fig. 17 depicts the results of the proposed FTS algorithm to the proposed MLI topology. It is observed from Fig. 17, that the motor phase voltage across phase-a winding and the traces of no-load currents i_a (blue), i_b (green), and i_c (pink) are symmetrical in nature.

5.2 For switch short-circuit faults

In the event of a short-circuit fault in any of the switches, then the healthy switch of that particular leg has to be turned-OFF and FTS algorithm has to be applied. Turning-OFF the healthy switch in the leg of the faulty switch prevents short-circuit across the source. Applying FTS for switch short-circuit fault in legs connected to windings will yield the same results as FTS applied to switch open-circuit fault. However, for short-circuit faults in switches of the modified leg the strategy is explained (as in Section 4.2).

To infer the characteristics of the proposed MLI topology with FTS for the short-circuited switch S_{a1}, the switch S_{a1} is completely turned-ON and switches S_{a4} and S_{a7} are completely turned-OFF. As mentioned in FTS (in Section 4.2) the switches S_{b1} and S_{c1} are turned-ON completely and switches S_{b4}, S_{b7}, S_{c4}, and S_{c7} are turned-OFF completely. The experimental results for $V_{aa'}$ and the no-load three phase currents i_a (blue trace), i_b (green trace), and i_c (pink trace) are depicted in Fig. 18 after adopting FTS for switch S_{a1} short-circuit fault. The output voltages and load currents resemble the same even for other two switches (S_{a4} and S_{a7}) under short-circuit conditions.

The voltage of the dc-link capacitors is at balance during normal operating condition with the switching strategy used (as mentioned in Section 3). The proposed MLI topology may be subjected to different fault conditions such as switch open-circuit and short-circuit conditions. These types of fault affect the voltage balance in the capacitors. The nature of capacitor voltages under normal operating conditions, during switch open-circuit fault condition and during FTS condition are depicted in Fig. 19. From Fig. 19, the upper trace indicates the voltage across the upper capacitor and lower trace indicates the voltage across the lower capacitor of the inverter-a. The voltage across the upper capacitor during switch open-circuit condition sees a voltage rise from $V_{dc}/2$

to V_{dc} (top trace of Fig. 19). The capacitor unbalance occurs because of open-circuit fault. Under normal operating conditions due to symmetry in switching pattern of switches, load current flowing through both the upper and lower capacitor is equal and hence the voltage across the capacitors will be equal. Due to open-circuit in switch S_{a2}, the switching symmetry gets affected and hence the current flowing through the capacitors and therefore the voltage across capacitors gets affected. The voltage across the upper capacitor increases near the source voltage V_{dc}, whereas the voltage across the lower capacitor decreases near to zero.

Once the FTS is applied, the symmetry in switching pattern is regained and the voltage across capacitors is equalised. Since the voltage across upper capacitor during switch open-circuit condition has increased from a value of $V_{dc}/2$ to V_{dc}, the capacitors used should be of sufficiently high capacity to withstand the increase in voltage during fault conditions until the FTS is applied. Therefore, the voltage rating of the capacitors should be equal to source voltage such that the topology can sustain during switch open-circuit faults. Fig. 20 depicts the pre-fault and post-fault voltages across the capacitors for switch S_{a2} short-circuit condition. Fig. 21 shows the experimental setup for the proposed H-Bridge MLI topology for a 1-hp OEWIM drive.

The proposed MLI topology ensures its operation under normal conditions with nine levels in the output voltage across each of the phase winding with a voltage level of $V_{dc}/2$. Under switch fault conditions such as switch open-circuit or short-circuit conditions, the proposed topology will ensure continuous operation with the reduction in output power level as the voltage levels gets decreased due to the fault in the switches. This continuous operation of the proposed topology accomplished by modifying the switching pulses fed to the switches. With the analysis of proposed topology under normal and abnormal conditions with pre and post-fault analysis, it can be justified that the proposed topology exhibits fault-tolerance property for all possible faults in switches.

Every MLI topology has its own merits and demerits depending on the field of application. The proposed MLI topology is not an exception. Compared to the conventional topologies like NPC topology, FC topology, and CHB topologies, the proposed topology has some demerits like its non-modular structure and this requires three DC sources. Nevertheless, in applications such as the battery-driven electric vehicles fed by solar PV panels or fuel cells the proposed topology suits well because of its low supply voltage requirement and its fault-tolerance property. Since the proposed topology can also be used with Volt/Hertz control of induction motor (discussion of *V*/*F* control of proposed topology was beyond the scope of this paper) and hence finds application in industries such as steel rolling mills, paper rolling mills, etc.

6 Conclusion

This paper presents a new star connected MLI topology for OEWIMD. The proposed model employs three modified H-Bridge inverters connected in the star configuration. This arrangement attains the output voltage of twice the DC link voltage in nine levels for the OEWIMD. The proposed topology ensures the fault-tolerance capability for switch open-circuit faults and switch short-circuit faults without using any external hardware but by simple post-processing of the PWM signals. Proposed topology can employ conventional PWM techniques that add additional advantage when implemented in digital platforms such as dSPACE or DSP. In this work, to generate switching pulses LSC SPWM (with IPD) is used. Component count of the topology is comparatively less whereas, the effective cost of the inverter is less when compared with other nine-level inverter topologies except for ACHB topology. The drawback of this topology is that it employs capacitors of voltage rating equal to the source which will increase the cost and size of inverter. The behaviour of the proposed topology is analysed under various possible switch open-circuit and switch short-circuits fault conditions. A FTS is proposed for switch open-circuit and short-circuit faults, which adds fault-tolerance capability to the proposed topology. Implementation of FTS does not require any additional hardware, hence no increase in the cost of the topology. This topology is capable of providing

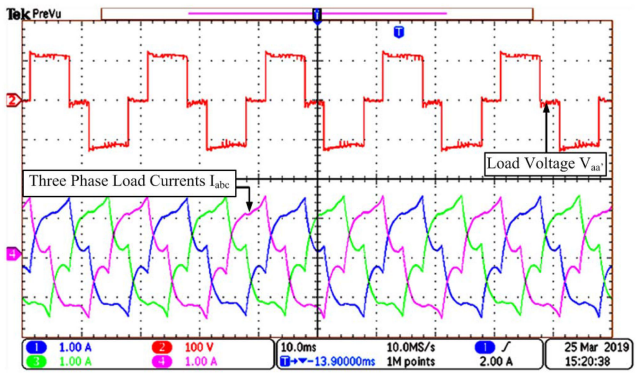

Fig. 18 *Waveforms of $V_{aa'}$ (top trace) and no-load phase currents i_a (blue), i_b (green), i_c (pink) with FTS for S_{a1} short-circuit fault*

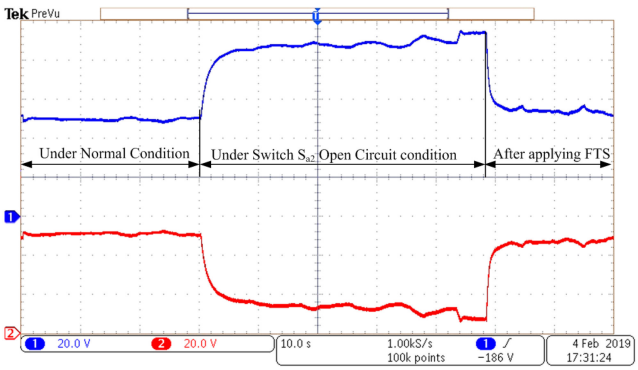

Fig. 19 *Voltage across capacitors during normal operation, during switch S_{a2} open circuit condition and after application of FTS*

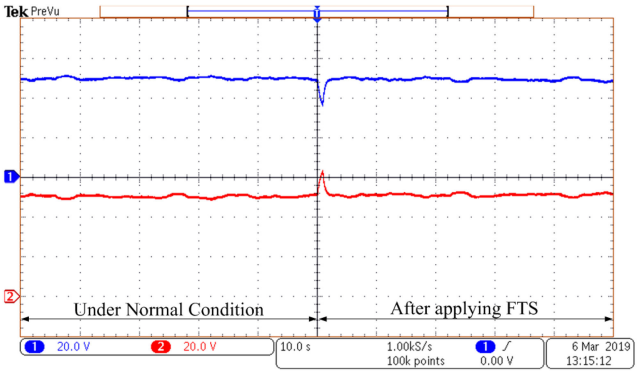

Fig. 20 *Voltage across capacitors during normal operation and after application of FTS for switch S_{a2} short circuit*

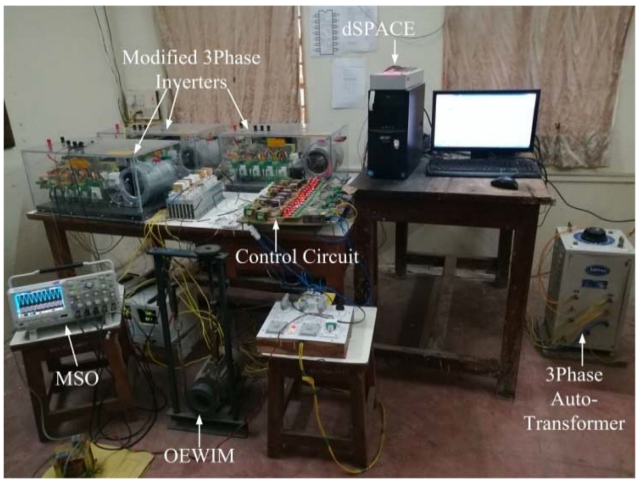

Fig. 21 *Experimental setup of the proposed MLI Topology*

balanced three-phase output voltage for OEWIMD even under switch fault conditions. Although the inverter operates at reduced power rating, it ensures continuity in operation of the drive with a balanced three-phase supply and reduced DC component in output voltage.

7 References

[1] Franquelo, L.G., Rodriguez, J., Leon, J.I., *et al.*: 'The age of multilevel converters arrives', *IEEE Ind. Electron. Mag.*, 2008, **2**, (2), pp. 28–39

[2] Kouro, S., Malinowski, M, Gopakumar, K, *et al.*: 'Recent advances and industrial applications of multilevel converters', *IEEE Trans. Ind. Electron.*, 2010, **57**, (8), pp. 2553–2580

[3] Stemmler, H., Guggenbach, P.: 'Configurations of high-power voltage source inverter drives'. 1993 Fifth European Conf. on Power Electronics and Applications, Brighton, UK, 1993, vol. 5, pp. 7–14

[4] Srinivasan, P., Narasimharaju, B.L., Srikanth, N.V.: 'Space-vector pulse width modulation scheme for open-end winding induction motor drive configuration', *IET Power Electron.*, 2015, **8**, (7), pp. 1083–1094

[5] Lakhimsetty, S., Surulivel, N., Somasekhar, V.T.: 'Improvised SVPWM strategies for an enhanced performance for a four-level open-end winding induction motor drive', *IEEE Trans. Ind. Electron.*, 2017, **64**, (4), pp. 2750–2759

[6] Srinivasan, P., Venugopal Reddy, B., Somasekhar, V.T.: 'PWM switching strategy for the elimination of common mode voltage of a two-level inverter drive with an open-end winding induction motor configuration'. 2010 Joint Int. Conf. on Power Electronics, Drives and Energy Systems & 2010 Power India, New Delhi, 2010, pp. 1–6

[7] Wu, D., Wu, X., Su, L., *et al.*: 'A dual three-level inverter-based open-end winding induction motor drive with averaged zero-sequence voltage elimination and neutral-point voltage balance', *IEEE Trans. Ind. Electron.*, 2016, **63**, (8), pp. 4783–4795

[8] Somasekhar, V.T., Srinivas, S., Kumar, K.K.: 'Effect of zero-vector placement in a dual-inverter fed open-end winding induction-motor drive with a decoupled space-vector PWM strategy', *IEEE Trans. Ind. Electron.*, 2008, **55**, (6), pp. 2497–2505

[9] Sekhar, K.R., Srinivas, S.: 'Torque ripple reduction PWMs for a single DC source powered dual-inverter fed open-end winding induction motor drive', *IET Power Electron.*, 2018, **11**, (1), pp. 43–51

[10] Gautam, S.P., Kumar, L., Gupta, S., *et al.*: 'A single-phase five-level inverter topology with switch fault-tolerance capabilities', *IEEE Trans. Ind. Electron.*, 2017, **64**, (3), pp. 2004–2014

[11] Rajeevan, P.P., Sivakumar, K., Gopakumar, K., *et al.*: 'A nine-level inverter topology for medium-voltage induction motor drive with open-end stator winding', *IEEE Trans. Ind. Electron.*, 2013, **60**, (9), pp. 3627–3636

[12] Welchko, B.A., Lipo, T.A., Jahns, T.M., *et al.*: 'Fault tolerant three-phase AC motor drive topologies: a comparison of features, cost, and limitations', *IEEE Trans. Power Electron.*, 2004, **19**, (4), pp. 1108–1116

[13] Chen, A., Hu, L., Chen, L., *et al.*: 'A multilevel converter topology with fault-tolerant ability', *IEEE Trans. Power Electron.*, 2005, **20**, (2), pp. 405–415

[14] Ambusaidi, K., Pickert, V., Zahawi, B.: 'New circuit topology for fault tolerant h-bridge DC–DC converter', *IEEE Trans. Power Electron.*, 2010, **25**, (6), pp. 1509–1516

[15] Lezana, P., Aceiton, R.: 'Hybrid multicell converter: topology and modulation', *IEEE Trans. Ind. Electron.*, 2011, **58**, (9), pp. 3938–3945

[16] Madhukar Rao, A., Sivakumar, K.: 'A fault-tolerant single-phase five-level inverter for grid-independent PV systems', *IEEE Trans. Ind. Electron.*, 2015, **62**, (12), pp. 7569–7577

[17] Jalhotra, M., Kumar, L., Gautam, S.P., *et al.*: 'Development of fault-tolerant MLI topology', *IET Power Electron.*, 2018, **11**, (8), pp. 1416–1424

[18] Choi, U., Blaabjerg, F., Lee, K.: 'Reliability improvement of a t-type three-level inverter with fault-tolerant control strategy', *IEEE Trans. Power Electron.*, 2015, **30**, (5), pp. 2660–2673

[19] Maddugari, S.K., Borghate, V.B., Sabyasachi, S., *et al.*: 'A fault tolerant cascaded multilevel inverter topology for open circuit faults in switches'. 2017 IEEE Transportation Electrification Conf. (ITEC-India), Pune, 2017, pp. 1–5

[20] Ceballos, S., Pou, J., Zaragoza, J., *et al.*: 'Fault-tolerant neutral-point-clamped converter solutions based on including a fourth resonant leg', *IEEE Trans. Ind. Electron.*, 2011, **58**, (6), pp. 2293–2303

[21] Pires, V.F., Foito, D., Silva, J.F.: 'Fault-tolerant multilevel topology based on three-phase h-bridge inverters for open-end winding induction motor drives', *IEEE Trans. Energy Convers.*, 2017, **32**, (3), pp. 895–902

[22] Sivakumar, K., Das, A., Ramchand, R., *et al.*: 'A hybrid multilevel inverter topology for an open-end winding induction-motor drive using two-level inverters in series with a capacitor fed h-bridge cell', *IEEE Trans. Ind. Electron.*, 2010, **57**, (11), pp. 3707–3714

[23] Kshirsagar, A., Kaarthik, R. S., Rahul, A., *et al.*: '17-level inverter with low component count for open-end induction motor drives', *IET Power Electron.*, 2018, **11**, (5), pp. 922–929

[24] Mondal, G., Sivakumar, K., Ramchand, R., *et al.*: 'A dual seven-level inverter supply for an open-end winding induction motor drive', *IEEE Trans. Ind. Electron.*, 2009, **56**, (5), pp. 1665–1673

[25] Vinod, B.R., Baiju, M.R., Shiny, G.: 'Five level inverter fed space vector based direct torque control of open-end winding induction motor drive', *IEEE Trans. Energy Convers.*, 2018, **33**, (3), pp. 1392–1401

[26] Rahim, N.A., Chaniago, K., Selvaraj, J.: 'Single-phase seven-level grid-connected inverter for photovoltaic system', *IEEE Trans. Ind. Electron.*, 2011, **58**, (6), pp. 2435–2443

[27] Pires, V.F., Foito, D., Cordeiro, A.: 'Three-phase qZ-source inverter with fault tolerant capability', *IET Power Electron.*, 2017, **10**, (14), pp. 1852–1858

[28] Vemuganti, H.P., Sreenivasarao, D., Siva Kumar, G.: 'Improved pulse-width modulation scheme for t-type multilevel inverter', *IET Power Electron.*, 2017, **10**, (8), pp. 968–976

[29] Zhang, W., Xu, D., Enjeti, P.N., *et al.*: 'Survey on fault-tolerant techniques for power electronic converters', *IEEE Trans. Power Electron.*, 2014, **29**, (12), pp. 6319–6331

[30] Lezana, P., Pou, J., Meynard, T.A., *et al.*: 'Survey on fault operation on multilevel inverters', *IEEE Trans. Ind. Electron.*, 2010, **57**, (7), pp. 2207–2218

[31] Grandi, G., Ostojic, D.: 'Carrier-based discontinuous modulation for dual three-phase two-level inverters'. SPEEDAM 2010, Pisa, 2010, pp. 839–844

[32] Sandeep, N., Sathik, J., Yaragatti, U., *et al.*: 'A self-balancing five-level boosting inverter with reduced components', *IEEE Trans. Power Electron.*, 2019, **34**, (7), pp. 6020–6024, doi: 10.1109/TPEL.2018.2889785

[33] McGrath, B.P., Holmes, D.G.: 'Multicarrier PWM strategies for multilevel inverters', *IEEE Trans. Ind. Electron.*, 2002, **49**, (4), pp. 858–867

[34] Rodriguez, J., Lai, J.-S, Peng, F.Z.: 'Multilevel inverters: a survey of topologies, controls, and applications', *IEEE Trans. Ind. Electron.*, 2002, **49**, (4), pp. 724–738

8 Appendix:

8.1 Inverter parameters

Make-SEMIKRON, Model:SKM-4M7-45A-3, Semiconductor switches: IGBT, Model: SKM75GB063D, Capacitors: 2 (each of 2200 uF) Table 4.

Table 4 Motor parameters

Parameter	Quantity
stator resistance (R_s)	8.45 Ω
rotor resistance (R_r)	7.2 Ω
stator inductance (L_s)	0.025 H
rotor inductance (L_r)	0.025 H
mutual inductance (L_m)	0.615 H
poles (P)	4
inertia (J)	0.06816 kg/m^2
motor nominal voltage	400 V (Line–Line)