Parametric Analysis of Surge Test Circuit for Auto Recloser to Resolve Experimental Difficulties

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Abstract— **Automatic circuit reclosers or fault interrupters are self-controlled device for making, carrying, and automatically interrupting and reclosing an alternating-current circuit. The automatic circuit recloser consist an assembly of control elements required to detect over currents and control the recloser operation. These equipment capability to survive fast lightning induced surges have to be verified by simulated surge arrester operation test. This paper discusses about the International standard stipulated test requirements and practical difficulties encountered while performing the test. This paper also presents the PSPICE based parametric analysis and the effectiveness of the variation in each component of test circuit on the parameters of test voltage and current waveforms.**

Keywords— Automatic circuit recloser, Fault interrupter, Simulated Surge, Parametric analysis, PSPICE.

I. INTRODUCTION

Insulation is the weak point in a power system and is subject to break down when exposed to extremely high voltages caused by lightning, faults or re energization of a line. Since the beginning of the electric grid direct lightning strikes and indirect effects of it have been a challenge. We use different devices to handle with different problems caused by lightning**.** Simulated surge arrester operation tests have traditionally been used to verify recloser/Fault Interrupter (FI) system operation and its capability to survive fast lightning induced surges. This test falls into a broader category of electromagnetic compatibility tests normally applied to protective relay devices and defined in:

a) IEEE Std C37.90 [1]

b) IEEE Std C37.90.1 (SWC)

c) IEEE Std C37.90.2 (RF susceptibility) [2]

d) IEEE Std C37.90.3 (electrostatic discharge tests for protective relays) [3]

e) IEC 60255-22-1 (1 MHz burst immunity tests)

f) IEC 60255-22-2 (electrostatic discharge tests) [4]

g) IEC 60255-22-3 (radiated electromagnetic field disturbance tests) [5]

h) IEC 60255-22-4 (fast transient burst immunity test

i) IEC 60255-22-6 [6]

Experience has shown that an electronic control built and tested to meet the above standards may often misoperate or be permanently damaged after exposure to lightning surges normally encountered on a distribution power system. The problem is easily understood by observing that the standards noted above were developed for a power system substation environment. In this environment, individual control devices can rely on well-established EMC protection practices, including: high quality earth grid, bonding, lightning shields, substation class arresters, greater distance between switching devices and the control house, and extensive shielding as found in metal clad and GIS switchgear. Few, if any, of these measures are available to protect or shield a mid-line distribution recloser. The control conductors, local distribution class arresters, and the local earthing (grounding) system are called upon to absorb the full impact of the lightning strike [1-7]. Hence, The International standard IEC introduced different test procedure for distribution class reclosers.

In this paper the standard stipulated surge simulation test on recloser and difficulties in achieving the test voltage and current parameters simultaneously were discussed. This paper also discusses about changes in the parameters of test voltage and current waveforms due to change in the test circuit parameters by using the parametric analysis in PSPICE simulation software.

II. TEST CONNECTIONS

For surge simulated test, the test connection plays a significant role as it defines the Electro Magnetic (EM) and fast transient stresses in the recloser/FI. This section discusses about test connections of the simulated surge arrester operation test on electronic element control unit (which should be well protected from the EM disturbances) of recloser/FI.

A rod gap connected from one source bushing terminal to the recloser/FI earth lead shall be used to simulate a surge arrester for conditions 1), 2) and 3) of III Section (Test procedure) as shown in Fig. 1. For condition 4) and 5) of III Section (Test procedure), the rod gap shall be connected from one bushing of the transformer to the transformer earth lead as shown in Fig. 2. The gap shall be set to flashover at 80 % (±10 %) of the rated lightning impulse withstand voltage of the recloser/FI on which the control element is to be applied. The surge voltage shall rise to flashover in 1.2 μs (± 0.5 μs). The earth lead shall be connected to the normal earth terminal of the recloser/FI under test and may be adjacent to the control cable connection. The control cable shall be spaced 15 cm from and run parallel to the recloser/FI earth lead. The earth lead shall be #12 AWG or 2.5 mm^2 copper wire. The control earth lead shall be a maximum of 1.5 m to the point where it connects to the recloser/FI earth lead and the laboratory earth point.

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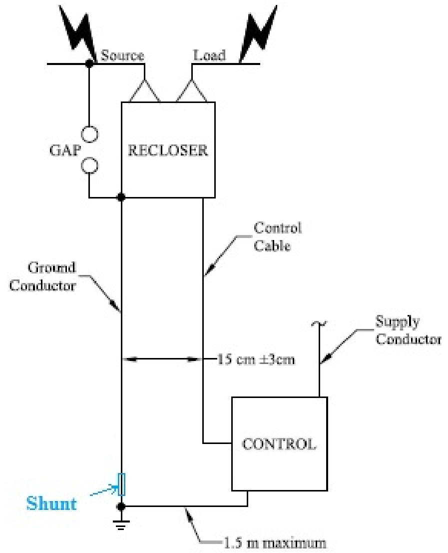


Fig. 1. Schematic diagram of test circuit for test conditions 1, 2 & 3.

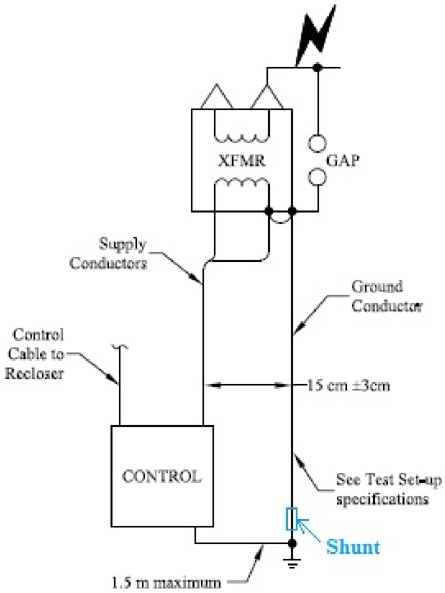


Fig. 2. Schematic diagram of test circuit for test conditions 4 & 5.

III. Test Procedure

Fifteen positive and fifteen negative surges shall be applied under each of the five conditions listed below with the gap on the source bushing. The gap shall remain connected to the source bushing for conditions 1, 2 and 3. If the device under test has a self-contained power source, conditions 4 and 5 may be omitted.

1) to the source terminal with the recloser/FI open;

2) to the source terminal with the recloser/FI closed;

3) to the load terminal with the recloser/FI closed;

4) to a properly rated transformer, connected as shown in Fig.2 with the recloser/FI open;

5) to a properly rated transformer, connected as shown in Fig.2 with the recloser/FI closed.

When testing under conditions 4 and 5, the supply transformer shall be energized to supply the normal control power to the control under test. This may be accomplished by energizing the primary or by back feeding through the secondary. In either case, care should be taken to isolate the transformer from the laboratory (house) power supply.

IV. Experimental Test

The surge withstand test on electronic elements of control unit of auto recloser rated for 33kV nominal operating voltage has been carried out at High Voltage Division, CPRI, Bangalore. The experimental setup is shown in photographs for test conditions 4 & 5 are shown in Fig.3-6.


Fig. 3. Test setup photograph

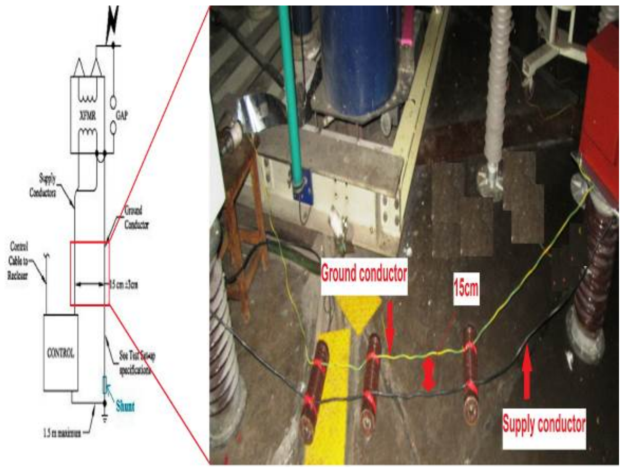


Fig. 4. Test setup photograph with conductor spacing details

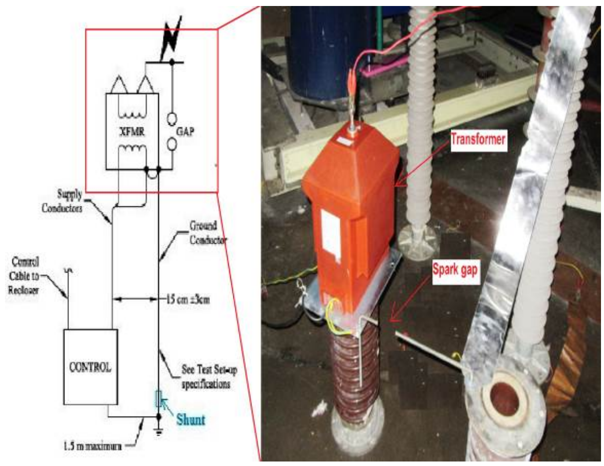


Fig. 5. Test setup photograph with transformer & spark gap

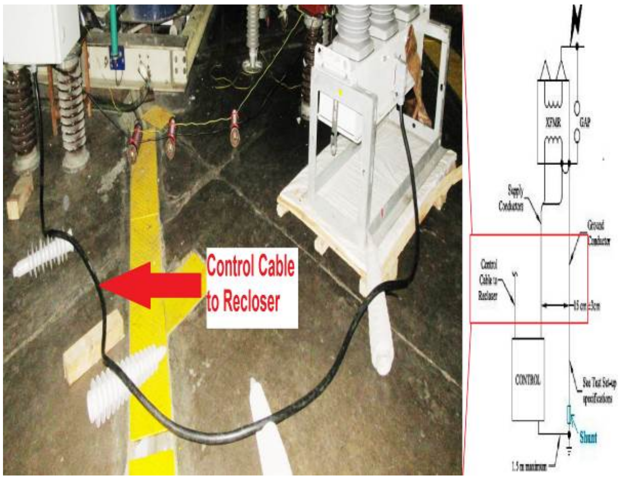


Fig. 6. Test setup photograph with control cable view

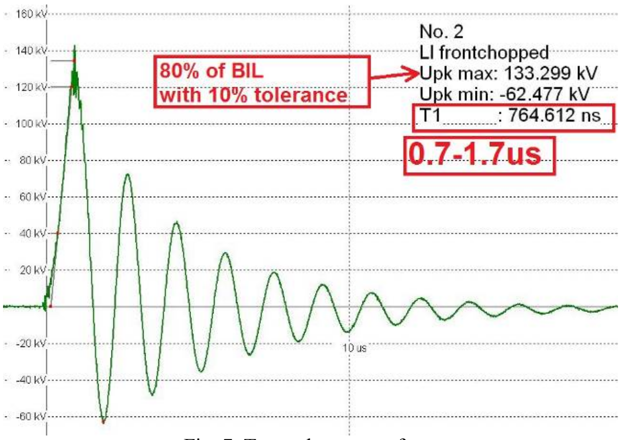


Fig. 7. Test voltage waveform

As per IEC standard, for the 33 kV system equipment BIL is 170 kV and the required test voltage should be 80 % (±10 %) of BIL i.e. 122.4 kV to 149.6 kV with rise time of 0.7**µ**s to 1.7**µ**s. The external surge generator current limiting resistance shall be chosen to provide a surge current following the spark gap flashover having a peak value of 6 000 A (±10 %) i.e. 5400A to 6600 A. The rate-of-rise of current waveform shall be 5 kA/µs to 10 kA/ µs over the initial 2 000 A rise. The experimental test voltage and current waveforms are shown in Fig.7 & 8 respectively.

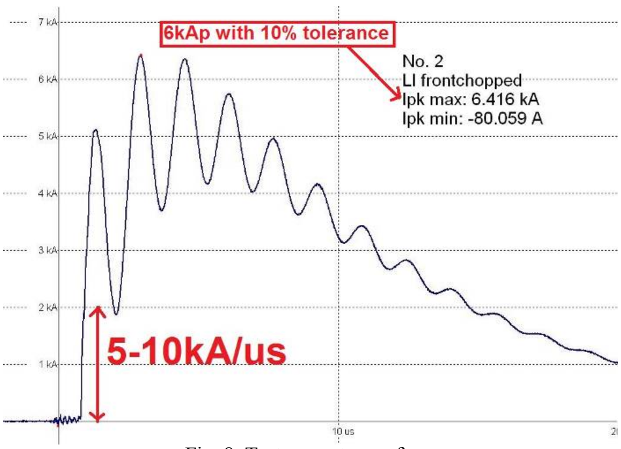


Fig. 8. Test current waveform

V. Parametric Analysis

The IEC standard mandate of test voltage waveform is its peak value (80% of BIL with 10% tolerance) and front time T1 (1.2**µ**S with 0.5**µ**S tolerance). The mandate of test current waveform is its peak value (6000 A with 10% tolerance) and initial rate of rise (5-10 kA/**µ**S) for first 2000 A. To obtain the standard mandate of four parameters experimental test the time taken is almost four days with trail and error method. It is very difficult to attain the standard requirement in two waveforms without experience and skill in practical impulse testing.

The parametric analysis of a simplified test circuit provides knowledge about effectiveness of the test circuit parameters on four mandate parameters of the test waveforms. The circuit shown in Fig. 9. consists of

Cg-Impulse generator capacitor with initial charge IC

R1- Front resistance of the generator

R2- Tail resistance of the generator

L – External inductance in series with test object

C2- External capacitance in parallel to test object

S – Spark gap represented by a simple switch in parallel to test object.

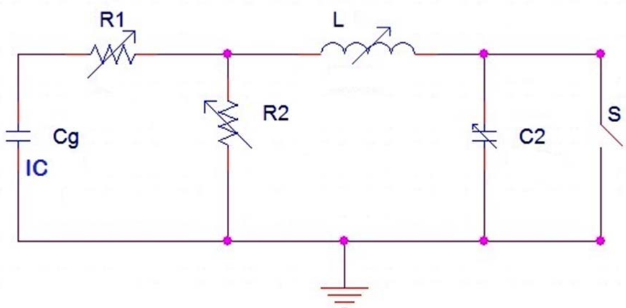


Fig. 9. Simplified test simulation circuit for parametric analysis

The PSPICE software transient mode was used to carry out the parametric analysis of the test circuit [8]. The parametric analysis was carried out by varying a single parameter while keeping all other parameters at fixed values. The fixed values of parameters considered are Cg: 0.75 uF; IC: 150 kV; R1: 10 **Ω**; R2: 1040 **Ω**; L: 120 uH & C2:1800 pF. The fixed and variation of the values considered in the analysis are based on laboratory availability of the circuit components.

A. Case1-The effect of the front resistance value

To find the effect of change in front resistance value on the test waveforms, R1 is varied in steps 5 **Ω**, 10 **Ω**, 20 **Ω** & 40 **Ω** while keeping other circuit parameters constant. The respective voltage waveforms, current waveforms and initial portion of the current waveforms (for di/dt information) are tabulated in the second row of the Table I. It is observed from the simulation results that the increase of the front resistance is leading to drastic reduction in peak value test current waveform with a minimum effect on the test voltage waveform and initial di/dt of the current waveform.

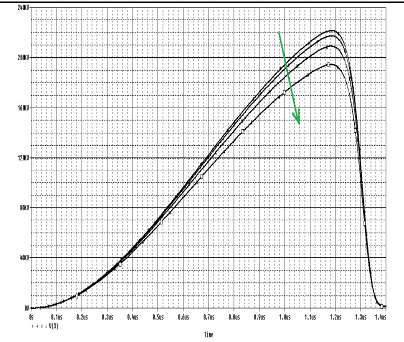
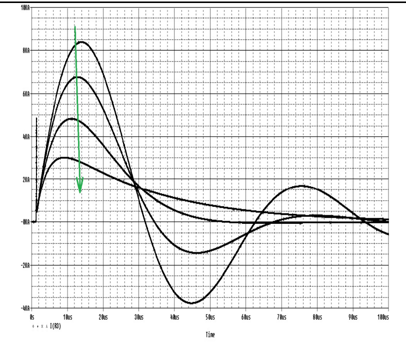
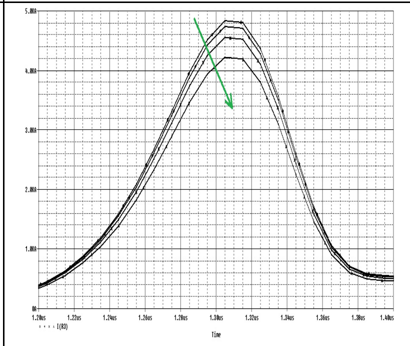
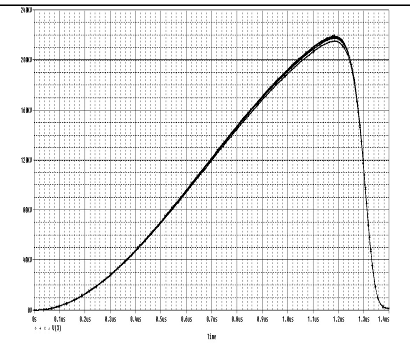
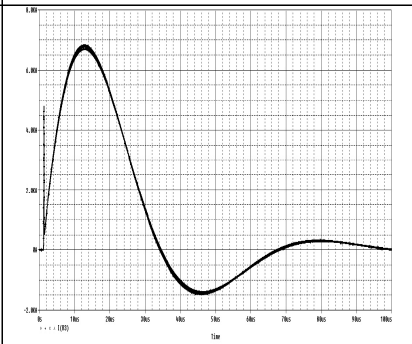
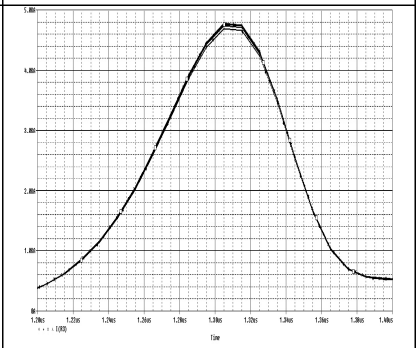
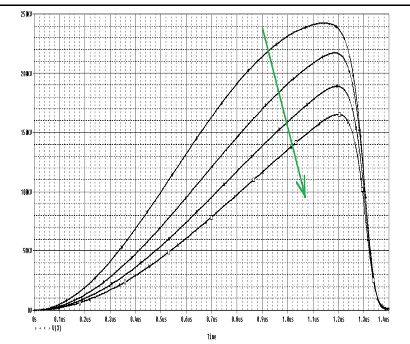
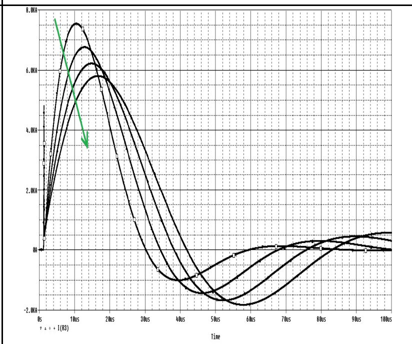
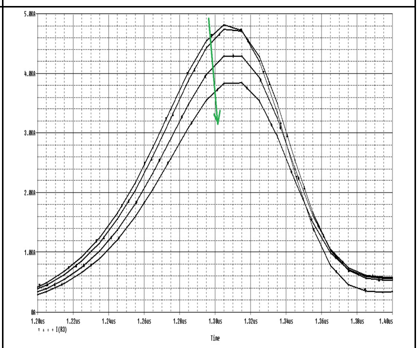
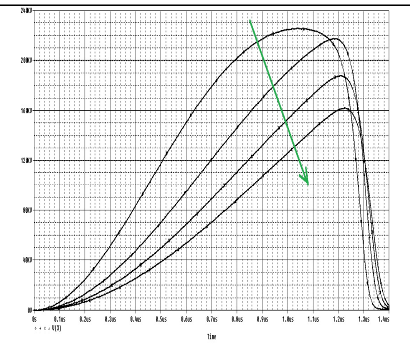
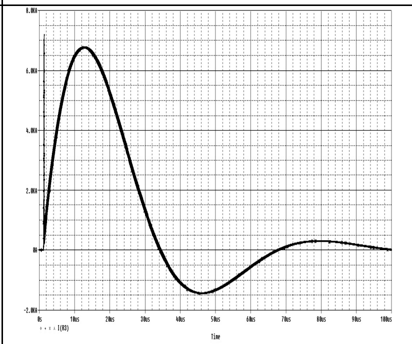
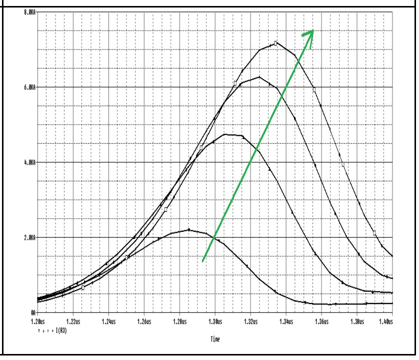
B. Case 2-The effect of the tail resistance value

To find the effect of change in tail resistance value on the test waveforms, R2 is varied in steps 520 **Ω**, 1040 **Ω**, 2080 Ω & 6000 Ω while keeping other circuit parameters constant. The respective voltage waveforms, current waveforms and initial portion of the current waveforms (for di/dt information) are tabulated in the third row of the Table I. It is observed from the simulation results that the change in value of the tail resistance is not having effect on the any test voltage waveforms.

C. *Case 3-The effect of the external inductance value*

To find the effect of change in external series inductance value on the test waveforms, Inductance is varied in steps 80 µH, 120 µH, 160 µH & 200 µH while keeping other circuit parameters constant. The respective voltage waveforms, current waveforms and initial portion of the current waveforms (for di/dt information) are tabulated in the fourth row of the Table I. It is observed from the simulation results that the increase of the external inductance is leading to reduction in peak values of test current and voltage waveforms and also leading to reduction in initial di/dt of the current waveform.

TABLE I. TEST VOLTAGE & CURRENT WAVEFORMS OF PARAMETRIC ANALYSIS

	Voltage	***Current***	***Initial di/dt of current***
R1: 5, 10, 20 & 40Ω			
R2: 520, 1040, 2080 & 6000Ω			
L: 80, 120, 160 & 200µH			
C2: 900, 1800, 2700 & 3600pF			

D. *Case4-The effect of the external capacitance value*

To find the effect of change in external parallel capacitance value on the test waveforms, the C2 is varied in steps 900pF, 1800pF, 2700pF & 3600pF while keeping other circuit parameters constant. The respective voltage waveforms, current waveforms and initial portion of the current waveforms (for di/dt information) are tabulated in the fifth row of the Table I. It is observed from the simulation results that the increase of the external capacitance is leading to drastic increase in initial di/dt of current and considerable reduction in peak of test voltage without affecting the test current waveform.

VI. CONCLUSIONS

The EM disturbances experienced by electronic control unit of station class recolser and mid-line reclosers are entirely different due to the different levels of EMC shielding. The EMC tests applicable to station class recloser are not sufficient to simulate the field conditions for mid-line reclosers because of inferior EMC shielding practices. Hence, the simulated surge operation test was stipulated in the International standard to ensure sufficient EMC isolation of the recloser control unit.

The standard stipulated test mandates four parameters of test waveforms to simulate harsh field condition. The peak and front time of test voltage wave shall be 80% of BIL with 10% tolerance and 1.2**μ**S with 0.5**μ**S tolerance respectively. The peak and initial di/dt of test current waveform shall be 6000A with 10% tolerance and 5 to 10kA/**μ**S respectively. To obtain the four mandate test parameters of voltage and current waveforms one may require experience and skill in impulse testing. The test was performed as per all the standard requirements first time in India at CPRI, Bangalore.

This paper also discuss about the parametric analysis of test circuit by using PSPICE software. It is observed that the increase of front resistance R1 will result into drastic reduction in current peak with meager effect on other waveform parameters. The change in tail resistance R2 has no effect on the test waveforms. The increase in series inductance results into considerable reduction in all required parameters of waveforms. The increase in external parallel capacitance leads to drastic increase in initial di/dt of current without altering its peak and decrease in voltage peak and front time. The conclusions drawn from the parametric analysis can be used in practical testing while rigging the test circuit.

ACKNOWLEDGMENT

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