A Seven-Level Hybrid Inverter with DC-Link and Flying Capacitor Voltage Balancing

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***Abstract*—Hybrid Multi-Level Inverter(MLI) topologies are gaining attention over conventional ones due to their extended applications in the power, industrial and renewable energy sectors. MLIs are optimized which can provide compact size, reduced cost and higher efficiency compared to the conventional types. In this paper, a hybrid structure of novel three-phase seven-level inverter is proposed. This topology is a combination of cascade-connected two-level cells and H-bridge cells with flying capacitors (FCs). The operating principle and the balancing technique for the DC-link capacitors and FCs are also presented. The generation of various output voltage levels using Sinusoidal Pulse Width Modulation (SPWM) is presented. The comparative analysis is carried out to show the number of components in the proposed circuit configuration and their voltage ratings are considerably lower compared to the conventional and recently proposed topologies. The performance of the proposed topology is verified with simulation studies and also in the experimentation. The simulation and experimental results validate the effectiveness of the proposed topology and the control technique.**

Keywords—Multilevel inverters, Hybrid inverters, H-bridge, Flying capacitors.

I. Introduction

MLI technology was started with the three basic topologies, namely, (i) Neutral point clamped converter (NPCC), (ii) Flying capacitor converter (FCC) and (iii) Cascaded H-bridge converter (CHBC). The three-level (3-L) NPC [1] was introduced by *Nabae et.al* in the year 1981 to meet the high-power demands of the industrial needs. Unequal power loss distribution and the requirement for a greater number of clamping diodes for higher voltage levels are its limitations. The FCC [2] is another MLI technology with energy storage facility. The requirement for bulky capacitors and the complex control algorithms for FC balancing puts a limitation on this converter. The CHBC [3] which is appropriate for renewable applications requires only power semiconductor devices in its structure. It does not require clamping diodes and flying capacitors in its structure. However, the necessity for independent sources in each H-bridge cell increases the cost and complexity of the overall system.

The problem of unequal loss distribution is nullified in the 3-L ANPC converter [4]. Several variants of FCCs [5-6] are reported in the literature which limits the requirement of bulky capacitors and simplifies the balancing techniques. The requirement of independent dc sources in CHBC can be reduced by choosing the dc sources of unequal magnitudes [7], this strategy results in a reduction of switching devices as well.

In order to reduce the cost of the converter and to improve the efficiency of the system, the combinations of the classical converters and their several variants were reported in the literature. These converters are regarded as the hybrid MLIs. The combination of NPC and H-bridge converters is proposed in [8], in this topology, the NPC section acts as a level generation part and the H-bridge section acts as a polarity generation part. This topology generates five-level at the output with reduced current and voltage harmonics. However, it retains the disadvantages of NPC and it requires high voltage blocking switches in the H-bridge. The NPC section in recent times has been replaced with a T-type structure [9]. The requirement of higher blocking voltage switches in H-bridge is reduced by connecting an FC in it [10]. The combination of FC and H-bridge results in the reduction in blocking voltage of the switches and increase in the number of output voltage levels. The higher blocking voltage of the switches in H-bridge is reduced by another 3-L structure proposed in [11].

The proposed topology is a combination of Cascaded two-level structure and an H-bridge with FC. The proposed topology has the merits of reduced blocking voltage of the switches compared to [10] and reduced number of components compared to the classical converters. The proposed topology is fed from a single dc voltage source, the dc-link capacitors (C_1 and C_2) along with the dc source acts as a common dc-link for a three-phase system. The dc-link capacitor voltage and FC voltage balancing techniques are presented.

II. Working of the Proposed Topology

A. Seven-Level Operation

Fig. 1 shows the proposed hybrid MLI which is able to generate a seven-level output voltage. The DC-link capacitors C_1 and C_2 are connected in series with a mid-point (O) acts as dc neutral. The dc source of magnitude V_{dc} charges C_1 and C_2 to a voltage of $V_{dc}/2$ each. According to the developed control logic, the FCs C_r, C_y and C_b in H-bridges are charged to $V_{dc}/4$.

The following modes of operation gives the method of generating seven-level output across the pole voltages V_{RO}, V_{YO} and V_{BO}. The operating modes of the proposed MLI in its single-phase structure as shown in Fig. 2 is presented in detail as follows.

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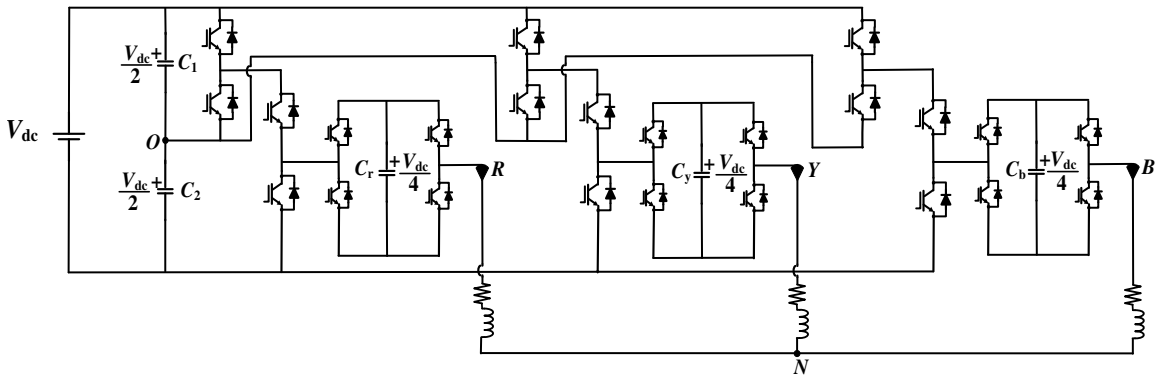


Fig. 1. Proposed seven-level hybrid inverter.

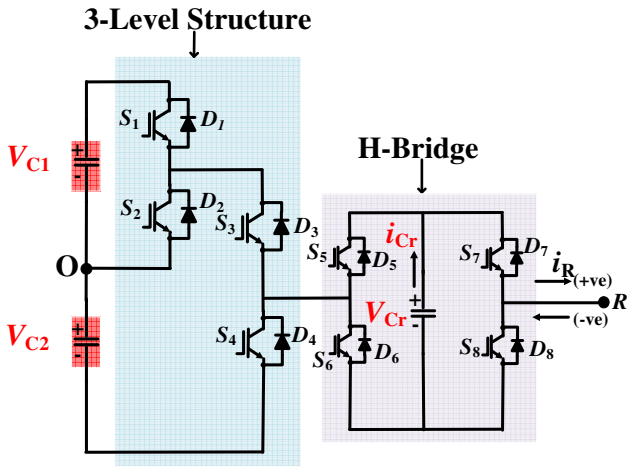


Fig. 2. Single-phase diagram of the proposed seven-level inverter.

B. Modes of Operation

Mode-A [V_{RO} = 0]: Switches S_2 and S_3 are gated with continuous pulses, the combination of S_5, S_7 and S_6, S_8 are gated during positive and negative zero crossings respectively.

Mode-B [V_{RO} =V_{dc}/4]: Switch S_3 is gated with a continuous pulse, the combination of switches S_2, S_6, S_7 and S_1, S_5, S_8 are triggered during discharging and charging states of FC.

Mode-C [V_{RO} = V_{dc}/2]: Switches S_1, S_3, S_5 and S_7 are gated with a constant pulse to clamp the top capacitor voltage of the dc-link.

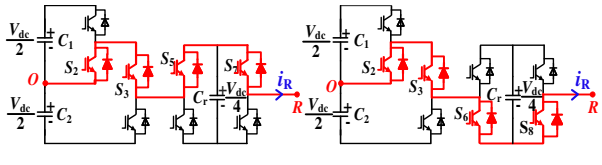


Fig. 3. Zero-level operating modes(a)$V_{RO} = 0^+$, (b)$V_{RO} = 0^-$.

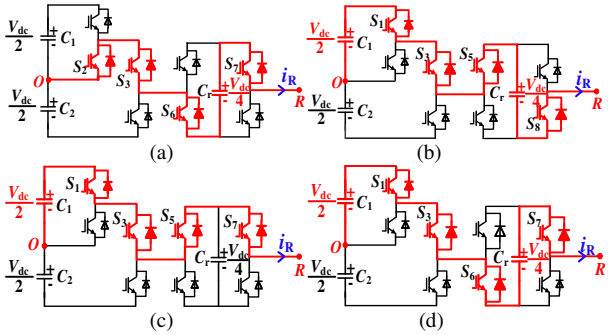


Fig. 4. Positive-level operating modes (a) V_{RO} = V_{Cr}, (b)V_{RO} = $-V_{Cr}$+V_{C1}, (c)V_{RO} =V_{C1}, and (d)V_{RO} =V_{Cr}+V_{C1}.

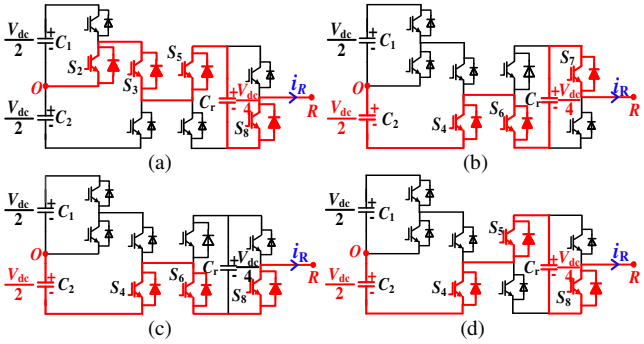


Fig. 5. Negative-level operating modes(a)V_{RO} = $-V_{Cr}$, (b)V_{RO} = V_{Cr}–V_{C2}, (c)V_{RO} = $-V_{C2}$, and (d)V_{RO} = $-V_{Cr}$–V_{C2}.

Mode-D [V_{RO} = 3V_{dc}/4]: Switches S_1, S_3, S_6 and S_7 are triggered continuously to connect C_1 and C_r voltages in series aiding.

Mode-B' [V_{RO} = –V_{dc}/4]: The combination of switches S_2, S_3, S_5, S_8 and S_4, S_6, S_7 are triggered during discharging and charging states of FC.

Mode-C' [V_{RO} = –V_{dc}/2]: Switches S_4, S_6, and S_8 are gated with a constant pulse to clamp the bottom capacitor voltage of the dc-link.

Mode-D' [V_{RO} = –3V_{dc}/4]: Switches S_4, S_5, and S_8 are triggered continuously to connect C_1 and C_r voltages in series aiding.

Figs. 3, 4 & 5 shows the current direction for the above said zero-level, positive-level and negative-level operating modes. The list of all operating modes along with the conducting devices and the effect of each switching state on the FC is represented in Table I.

TABLE I. SWITCHING TABLE

V_{RO} (V)	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	i_A	(a)	(b)	(c)
3V_{dc}/4	1	0	1	0	0	1	1	0	>0	D	4	V_4
									<0	C		
V_{dc}/2	1	0	1	0	1	0	1	0	--	N.E	4	V_3
V_{dc}/4	0	1	1	0	0	1	1	0	>0	D	4	V_2
									<0	C		
	1	0	1	0	1	0	0	1	>0	C	4	V_1
									<0	D		
0$^+$	0	1	1	0	1	0	1	0	--	N.E	4	V_0
0$^-$	0	1	1	0	0	1	0	1				
–V_{dc}/4	0	1	1	0	1	0	0	1	>0	C	4	V_5
									<0	D		
	0	0	0	1	0	1	1	0	>0	D	3	V_6
									<0	C		
–V_{dc}/2	0	0	0	1	0	1	0	1	--	N.E	3	V_7
–3V_{dc}/4	0	0	0	1	1	0	0	1	>0	C	3	V_8
									<0	D		

C- Charging, D- Discharging and N.E- No Effect, ×- don't care, (a)- Status of FC, (b) Number of conducting devices/ph and (c) switching state

III. Modulation Method And DC-Link Voltage Control

A. Sine-Triangle Comparison

A Level-Shifted SPWM [12], [13] technique is adapted to generate the gate pulses in the inverter switches. The modulation method is shown in Fig. 6. The required pulse pattern to each switching device is generated using the logic blocks to produce the seven-level inverter output across the pole-voltages.

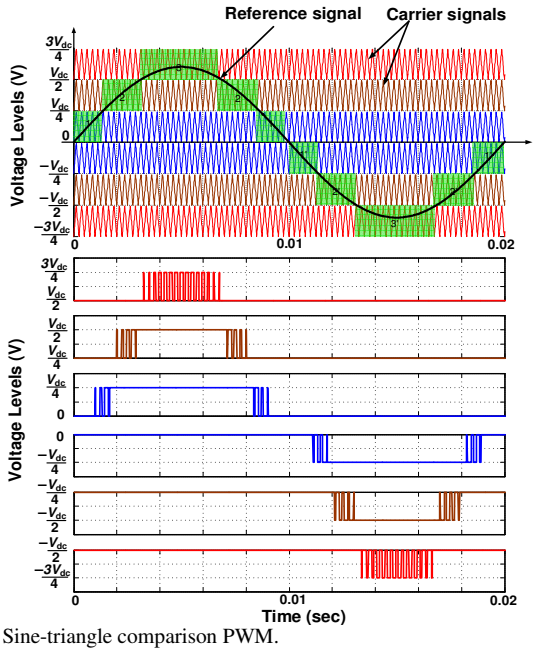


Fig. 6. Sine-triangle comparison PWM.

B. DC-link Capacitor Voltage Control

A voltage controlling method [14] is adapted to control the DC-link capacitor voltages (V_{C1} and V_{C2}) as shown in Fig. 7. It works by sensing one of the dc-link capacitor voltages, the error signal obtained by comparing with its desired value. This error signal is passed through a proportional-integral (P-I) controller, which generates a control signal to modulate the reference waveform accordingly to control the dc-link capacitor voltages.

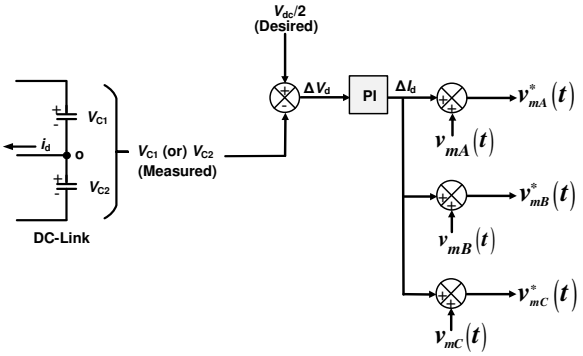


Fig. 7. DC-link capacitor voltage control.

IV. Flying Capacitor Voltage Control

The problem of FC voltage control arises during the switching states in which the FC is involved in the conduction path. As per Table I, the action of FC takes place during the voltage levels of $\pm V_{dc}/4$ and $\pm 3V_{dc}/4$. The availability of both charging and discharging states controls the FC voltages during $\pm V_{dc}/4$ levels. Since there is no presence of redundant switching states during $\pm 3V_{dc}/4$ levels, therefore, the FC voltage control is possible by limiting the value of modulation index (m_a). The variation of voltage ripple in the FC voltage with respect to (w.r.t) m_a at different power factors (PFs) is shown in Fig. 8.

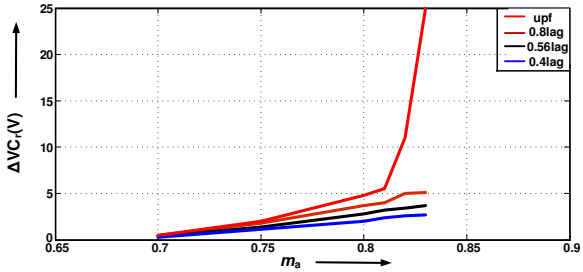


Fig. 8. Variations of FC voltage ripple in phase-A w.r.t m_a at different PFs.

V. Comparison of the Proposed Topology with Various MLI Configurations

The requirement of various components in the proposed topology w.r.t the classical and other recently proposed topologies is shown in Table II. It can be seen that the proposed configuration suppresses the requirement of clamping diodes, a huge number of FCs and independent sources in NPCC, FCC and CHBC respectively. It also has the advantages of reduced switch count and the reduced blocking voltage of the switches compared to recently proposed topologies in the literature. The need for V_{dc} switches is only three as compared to six in [10].

TABLE II. Comparison of the Proposed Topology with Various Topologies

Components	Voltage rating	NPC [1]	FC [2]	CHB [3]	[10]	[15]	[16]	Proposed
Switches	V_{dc}	--	--	--	6	--	--	3
	$3V_{dc}/4$	--	--	--	--	12	--	--
	$V_{dc}/2$	--	--	--	6	--	--	9
	$V_{dc}/4$	36	36	36	12	21	36	12
Clamping diodes	$5V_{dc}/4$	6	--	--	--	--	--	--
	V_{dc}	6	--	--	--	--	--	--
	$3V_{dc}/4$	6	--	--	--	--	--	--
	$V_{dc}/2$	6	--	--	--	--	--	--
	$V_{dc}/4$	6	--	--	--	--	--	--
Flying Capacitors	$5V_{dc}/4$	--	3	--	--	--	--	--
	V_{dc}	--	3	--	--	--	--	--
	$3V_{dc}/4$	--	3	--	--	--	--	--
	$V_{dc}/2$	--	3	--	--	--	--	--
	$V_{dc}/4$	--	3	--	3	--	18	3
Inductors	--	--	--	--	--	--	6	--
DC-link Capacitors	$V_{dc}/4$	6	6	--	--	--	--	--
	$V_{dc}/2$	--	--	--	2	--	--	2
Independent DC sources	$V_{dc}/4$	--	--	9	--	9	--	--
	V_{dc}	1	1	--	1	--	1	1
Total component count		73	58	45	30	42	61	30

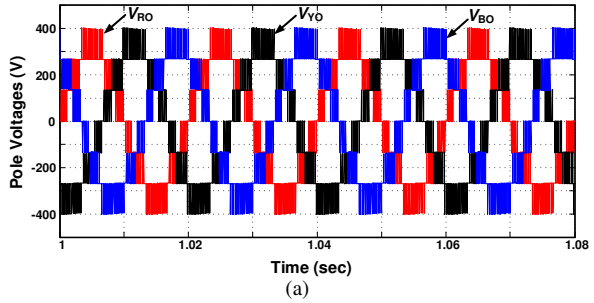
VI. Simulation Results

The operation, working and the performance of the proposed 3-phase MLI is evaluated in MATLAB simulation and the simulation studies are carried out at 540 V DC-link voltage and 135 V FC voltage to obtain 400 V(L-L) three-phase AC voltages. The gating pulses are generated using sine-triangle level shifted PWM technique. The output pole voltages of the proposed model are shown at a modulation index of 0.8. The working of the voltage controllers for balancing the dc-link capacitor voltages and FC voltages are also verified. Figs. 9(a)-(c) shows the inverter output results consisting of the pole-voltages, line-voltages, phase-R voltage and current. Fig. 9(d) shows the steady-state FC

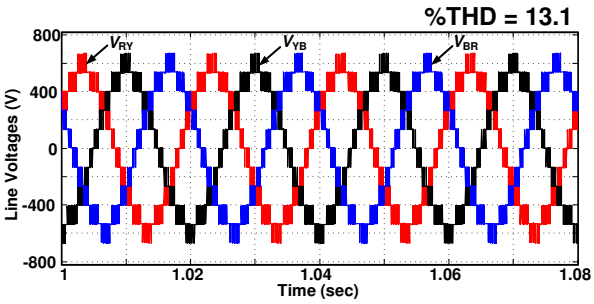
voltages of all the three phases. It can be seen that the voltage ripple in FC voltages is small. Fig. 9(e) indicates the harmonic profile of the pole voltage of the proposed MLI at an $m_a$of 0.8. It can be observed that the Total Harmonic Distortion (THD) value is 24.12%, which is within the specified limits as per the standards of seven-level operation.

TABLE III. SYSTEM PARAMETERS

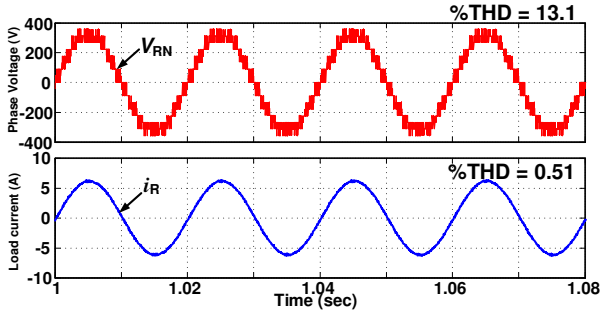
Parameter	Simulation	Experiment
DC-link Voltage	540 V	160 V
FC Voltage	135 V	40 V
DC-link Capacitance	1000 µF	1000 µF
Flying Capacitance	1000 µF	1000 µF
Output Power (P_O)	3 kW	600 W
Switching frequency (f_{sw})	4 kHz	4 kHz
Fundamental Frequency (f_m)	50 Hz	50 Hz



(a)



(b)



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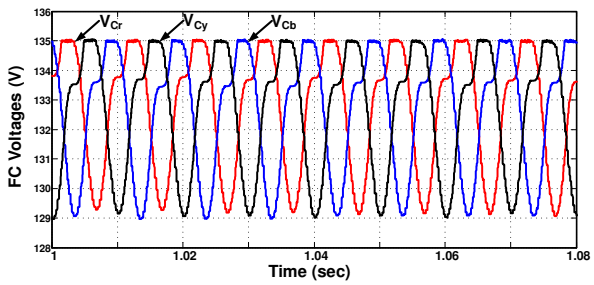
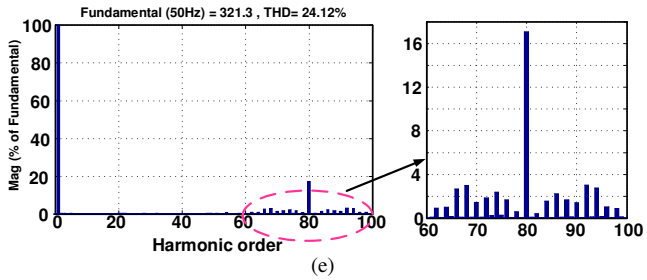


(d)



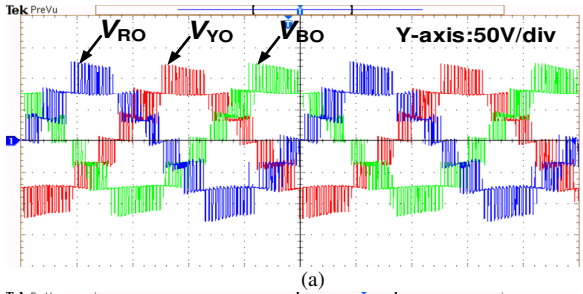
(e)

Fig. 9. Simulation results at $m_a = 0.8$ (a) Pole-voltages, (b) Line-voltages, (c) Phase-R Voltage and Current, (d) Steady-state FC voltages, and (e) FFT analysis of V_{RO}.

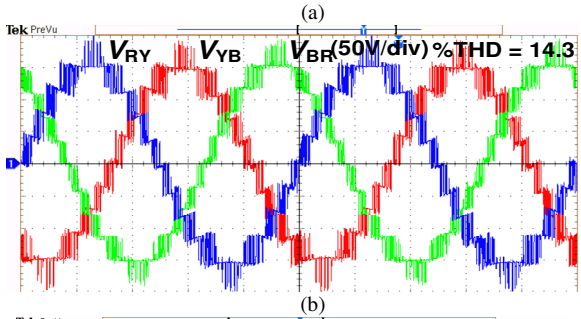
VII. EXPERIMENTAL RESULTS

The experimental scale down prototype is developed for a lower dc-link voltage of 160 V. Figs. 10(a)-(c) are the three-phase pole-voltages, line-voltages, phase-*R* voltage and current at an m_a of 0.8. Fig. 11(a) shows the transient response of Phase-R FC voltage w.r.t load variation. The FC voltage ripple is decreasing w.r.t load. This shows that the proposed topology is able to handle the load variations with a small difference in voltage ripples.

Fig. 11(b) shows the performance of the DC-link voltage controller, it is observed that the dc-link capacitor voltages become unbalanced when the controller is off and restores to the equal values (balanced) when the controller is switched on. Finally, Figs. 11(c) indicates the harmonic graph of the pole-voltage of the proposed topology at m_a= 0.8.



(a)



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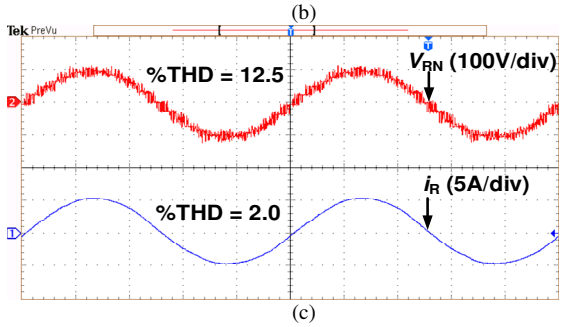

(c)

Fig. 10. Experimental results at $m_a = 0.8$ (a) Pole-voltages, (b) Line-voltages, and (c) Phase-R voltage and current; Time scale (4 ms/div).

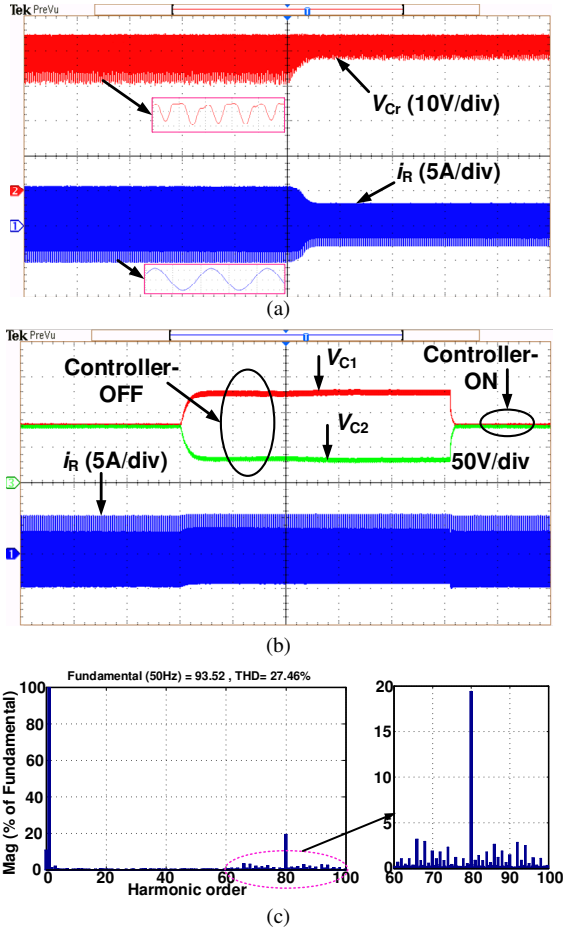

Fig. 11. (a) Voltage across FC (C_r) w.r.t load change; Time scale (1s/div), (b) Voltages across the DC-link capacitors and current (i_R) during the controller ON and OFF; Time scale (1s/div), and (c) FFT analysis of V_{RO} at $m_a = 0.8$.

VIII. Conclusion

An innovative MLI configuration is proposed in this paper with a single dc source, reduced component count and reduced voltage rated devices as compared to conventional and recently proposed topologies in the literature. A sine-triangle comparison PWM method is employed in which the dc-link capacitor and flying capacitor voltage balancing techniques are embedded. The balancing procedures are comprehensively presented. The steady-state simulation results are presented and the same is verified experimentally along with the dynamic variations in load and the operation of the controller.

References

[1] Nabae, I. Takahashi, and H. Akagi, "A New Neutral-Point-Clamped PWM Inverter," *IEEE Trans. Ind. Appl.*, vol. IA-17, no. 5, pp. 518-523, Sep./Oct. 1981.

[2] T. A. Meynard and H. Foch, "Multi-level choppers for high voltage applications," *EPE Journal*, vol. 2, no. 1, pp. 45-50, 1992.

[3] M. Marchesoni, M. Mazzucchelli, and S. Tenconi, "A nonconventional power converter for plasma stabilization," *IEEE Tran. Power Electron.*, vol. 5, no. 2, pp. 212-219, Apr. 1990.

[4] T. Bruckner, S. Bernet, and H. Guldner, "The active NPC converter and its loss-balancing control," *IEEE Trans. Ind. Electron.*, vol. 52, no. 3, pp. 855-868, Jun. 2005.

[5] M. Narimani, B. Wu, Z. Cheng, and N. R. Zargari, "A New Nested Neutral-Point-Clamped (NNPC) Converter for Medium-Voltage (MV) Power Conversion," *IEEE Trans. Power. Electron.*, vol. 29, no. 12, pp. 6375-6382, 2014.

[6] M. Narimani, B. Wu, and Z. Navid Reza, "A Novel five-level voltage source inverter with sinusoidal pulse-width modulator for medium-voltage applications," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 1959–1967, Mar. 2016.

[7] S. Mariethoz and A. Rufer, "Design and control of asymmetrical multi-level inverters," *In IEEE 2002 28th Annual Conference of the Industrial Electronics Society,* vol. 1, pp. 840-845, 2002.

[8] C. A. Silva, L. A. Cordova, P. Lezana, and L. Empringham, "Implementation and control of a hybrid multilevel converter with floating dc links for current waveform improvement," *IEEE Trans. Ind. Electron.*, vol. 58, no. 6, pp. 2304-2312, Jun. 2011.

[9] G. Ceglia, V. Guzman, C. Sanchez, F. Ibanez, J. Walter, and M. I. Gimenez, "A new simplified multilevel inverter topology for DC–AC conversion," *IEEE Trans. power electron.*, vol. 21, no. 5, pp. 1311-1319, Sep. 2006.

[10] H. Yu, B. Chen, W. Yao, and Z. Lu, "Hybrid Seven-Level Converter Based on T-Type Converter and H-bridge Cascaded Under SPWM and SVM," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 689-702, Jan. 2018.

[11] V. T. Somasekar and K. Gopa kumar, "Three-level inverter configuration cascading two two-level inverters," *IEE Proc.-Electr. Power Appl.*, vol.150, no. 3, pp. 245-254, 2003.

[12] G. Carrara, S. Gardella, M. Marchesoni, R. Salutari, and G. Sciutto, "A new multilevel PWM method: a theoretical analysis," *IEEE Trans. Power Electron.*, vol. 7, no. 3, pp. 497-505, Jul. 1992.

[13] V. G. Agelidis and M. Calais, "Application specific harmonic performance evaluation of multicarrier PWM techniques," *Proc. 29th IEEE Power Electronics Specialists Conf.*, pp. 172-178, 1998.

[14] H. Akagi, S. Inoue, and T. Yoshii, "Control and Performance of a Transformerless Cascade PWM STATCOM With Star Configuration," *IEEE Trans. Ind. Appl.*, vol. 43, no. 4, pp. 1041-1049, Jul./Aug. 2007.

[15] S. Sabyasachi, V. B. Borghate, R. R. Karasani, S. K. Maddugari, and A. H. M. Suryawanshi, "Hybrid Control Technique-Based Three-Phase Cascaded Multilevel Inverter Topology," *IEEE Access*, vol. 5, pp. 26912-26921, 2017.

[16] M. Hagiwara and H. Akagi, "Control and Experiment of Pulse width-Modulated Modular Multilevel Converters," *IEEE Trans. Power Electron.*, vol. 24, no. 7, pp.1737-1746, Jul. 2009.