Received: 23 January 2019 | Revised: 2 April 2019 | Accepted: 28 April 2019

DOI: 10.1002/cta.2648

RESEARCH ARTICLE

WILEY

A new structure of three-phase five-level inverter with nested two-level cells

Abhilash Tirupathi | Kirubakaran Annamalai | Somasekhar Veeramraju Tirumala

Department of Electrical Engineering, National Institute of Technology Warangal, Warangal, India

Correspondence
Kirubakaran Annamalai, Department of Electrical Engineering, National Institute of Technology Warangal, Warangal 506 004, India.
Email: kiruba81@nitw.ac.in

Summary

This paper presents a new structure of three-phase five-level inverter with a single direct current (DC) source for low- and medium-voltage applications. The proposed configuration is built with a cascade connection of two-level cells in a nested form and owns the advantages of a reduced number of passive components, total blocking voltage of the switches, and isolated DC sources. In order to make this topology attractive, a comparison is made with five-level inverter topologies proposed for low- and medium-voltage applications in recent years. The proposed circuit is powered using a single DC source and an auxiliary voltage-balancing circuit (AVBC) to maintain the desired DC-link capacitor voltages. A sinusoidal pulse width modulation (SPWM) scheme is implemented in field-programmable gate array (FPGA), using Xilinx blocks developed in MATLAB/SIMULINK environment, to control the inverter switches. The performance of the proposed topology is verified through MATLAB simulation and prototype model for a step change in load. Finally, the experimental results are presented to validate the effectiveness of the proposed topology.

KEYWORDS

auxiliary voltage-balancing circuit, multilevel inverter, pulse width modulation, total harmonic distortion, two-level cells

1 | INTRODUCTION

Multilevel inverters (MLIs) are an attractive solution for various medium-voltage applications such as industrial drives,[1,2] FACTs,[3] HVDC,[4,5] and renewable energy sources.[6,7] They are also extended for low-power applications due to the benefits of reduced device stress, electromagnetic interference, and filter size with a capability to synthesize the sinusoidal output voltage waveform with improved harmonic spectrum as compared with the two-level inverters.[8,9] The emergence of MLIs started with the discovery of three topologies, namely, (a) diode-clamped converter[10] (DCC), (b) flying capacitor converter[11] (FCC), and (c) cascaded H-bride converter (CHBC).[12] The inherent advantages of DCC and FCC include higher efficiency, equal voltage stress across the switches, and require a single direct current (DC) source, whereas CHBC requires a smaller component count to achieve the same output quality. However, these topologies suffer from numerous drawbacks of additional clamping diodes, flying capacitors, and complex control algorithms for balancing of DC-link capacitor voltages for the increase in output voltage levels. Moreover, the requirement of the number of isolated DC sources and an increase in the size of phase-shifting transformer challenges the use of CHBC.

Therefore, to overcome the issues of conventional MLIs, active neutral point-clamped (ANPC) MLIs and hybrid MLIs have been introduced in recent years. Among these, the ANPC is constructed from the combination of NPC and FC without the use of clamping diodes.[13] However, the use of additional sensors for FC voltage balancing restricts its applicability. Therefore, hybrid MLIs make attractive for medium-voltage applications. A detailed review of various hybrid MLIs is reported in the latest literature.[14] Most of them are CHB-based hybrid topologies and demand multiwinding transformers to develop independent sources, a large number of semiconductor devices, and increased control complexity. On the other hand, M. Narimani et al[15] introduced a novel four-level-nested neutral point-clamped (NNPC) inverter with reduced component count compared with 4L DCC and 4L FCC. This configuration is built by connecting all the central points of external and internal legs to the output terminals of the phase legs. A five-level-nested VSI is also proposed with the advantage of higher DC-link voltages with the increment of a capacitor and two switches per leg.[16] Further, a nested T-type four-level inverter has been introduced with the aim of reduced switch count to suit for medium-voltage and high-power applications.[17] However, the aforementioned topologies demand additional voltage and current sensors and a complex control algorithm to maintain the desired flying capacitor voltages. A generalized nested MLI[18] is proposed with a single DC source and reduced component count for higher level generation. But the inner leg T-type structure demands a higher total blocking voltage (TBV) of the semiconductor devices. Therefore, simplified structures of novel-nested MLI configurations for 4L, 5L, and 6L operations were introduced without any flying capacitors,[19] whereas the nested five-level inverter proposed uses a T-type structure. However, it suffers from higher blocking voltage requirement of the switches, which results in a slower response, higher loss, and increases the cost of the system.

Therefore, in this paper, a modified structure of three-phase five-level (5L) inverter topology using nested two-level cells (TLCs) with a single DC source is presented. The proposed topology is also referred as nested TLC five-level (NTLC-5L) inverter. The proposed NTLC-5L inverter owns the advantages of reduced TBV of the switches and losses with higher efficiency. An auxiliary voltage-balancing circuit (AVBC) is employed to balance the DC-link capacitor voltages. The detailed operation and balancing algorithm are presented. A comparison is also made to demonstrate the attractive features of the proposed configuration with conventional and some of the recently proposed 5L inverter topologies. Finally, the performance and feasibility of the proposed topology are verified through MATLAB simulation and experimental results.

2 | NESTED THREE-PHASE 5L INVERTER

2.1 | Proposed topology

Figure 1 depicts the proposed nested three-phase five-level inverter for one phase (A phase). This configuration is assembled by connecting three TLCs in each phase across a common DC link, wherein the series-connected capacitors

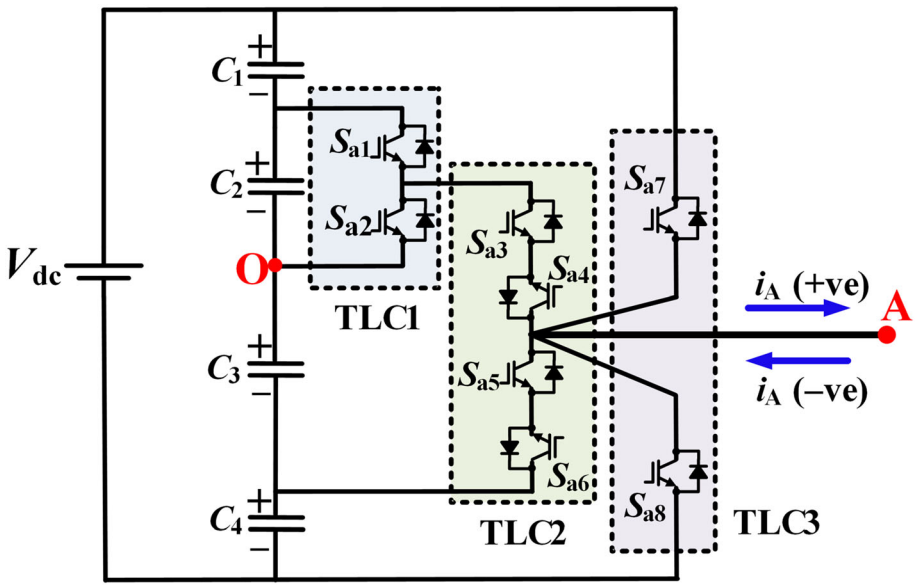

FIGURE 1 Phase A of the proposed nested five-level inverter [Colour figure can be viewed at wileyonlinelibrary.com]

C_1, C_2, C_3, and C_4 fed on a single DC source (V_{dc}) for all the three phases. The TLC1 consists of switches (IGBT/MOSFET) S_{a1} and S_{a2}, which are connected across the capacitor C_2. TLC2 consists of two bidirectional switches (B.Ss), which are realized by connecting two switching devices in antiseries connection. TLC3 consists of switches S_{a7} and S_{a8}, which are connected at the +ve and −ve rails of the DC link. Here, the TLCs 1 and 2 form the internal leg, and TLC3 is referred as the external leg. Figure 2 shows the complete three-phase circuit, wherein the output of the TLC3 in each phase is fed to the star-connected load. It may be noted that all four DC-link capacitors are charged to a voltage of $V_{dc}/4$ from a single DC supply, with the aid of an AVBC.[20]

With an appropriate operation of the switching devices, five voltage levels are produced at the pole voltages (V_{xO}), where x= A, B, and C in the range of $-V_{dc}/2$ to $+V_{dc}/2$ with a step size of $V_{dc}/4$. The switching devices S_{a1}, S_{a2}, S_{a4}, and S_{a6} are required to block a voltage of $V_{dc}/4$, whereas the switches S_{a3} and S_{a5} block the voltages of $2V_{dc}/4$ and $3V_{dc}/4$, respectively. The switches in TLC3, ie, S_{a7} and S_{a8}, should block a voltage of V_{dc}. Hence, the TBV of the switches in each phase is equal to $4.25V_{dc}$, whereas the estimated TBV of the switches in each phase of the nested T-type 5L inverter[19] (NNT-5L) is $5V_{dc}$. This proves that the proposed nested 5L inverter offers a considerable reduction in the overall rating of the switches. By considering a safety factor of 2, it can be observed from the three-phase configuration of Figure 2 that 12 switches are rated for $V_{dc}/2$, three switches are rated for V_{dc}, three switches are rated for $3V_{dc}/2$, and six switches are to be rated for $2V_{dc}$. Because the voltage ratings of the switches should be chosen as 1.8 to two times of their blocking voltage, to withstand the higher voltages appearing because of switching transients.[21,22] The detailed description of the conduction of switching devices to generate various output voltage levels is given in the following section.

2.2 | Operating modes

The operation of the proposed topology is explained through the following five modes of operation for various output voltage levels in phase A. In this configuration, the DC-link capacitor voltage balancing is carried out with the use of the AVBC. A positive direction is assigned to the instantaneous phase current if it leaves the output terminal (eg, the current "i_A" in Figure 1) and vice versa. The pole voltage pertaining to phase A is captured between the terminals "A" and "O." It is shown that the proposed five-level MLI is capable of generating five levels at V_{AO}, namely, $-V_{dc}/2$, $-V_{dc}/4$, 0, $V_{dc}/4$, and $V_{dc}/2$. Figure 3 presents the operating modes along with the details of conducting devices and their corresponding load current (i_A) directions.

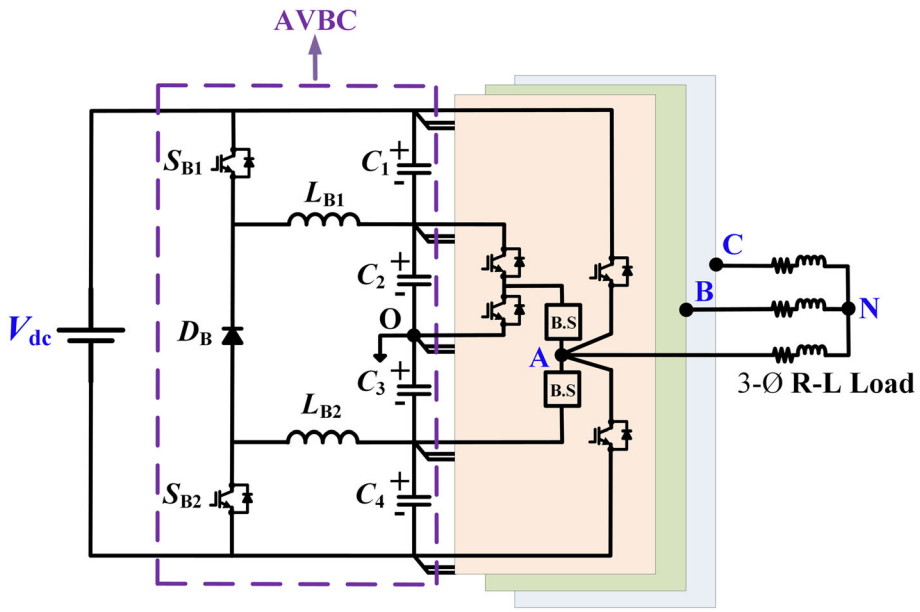

FIGURE 2 Proposed nested three-phase five-level inverter [Colour figure can be viewed at wileyonlinelibrary.com]

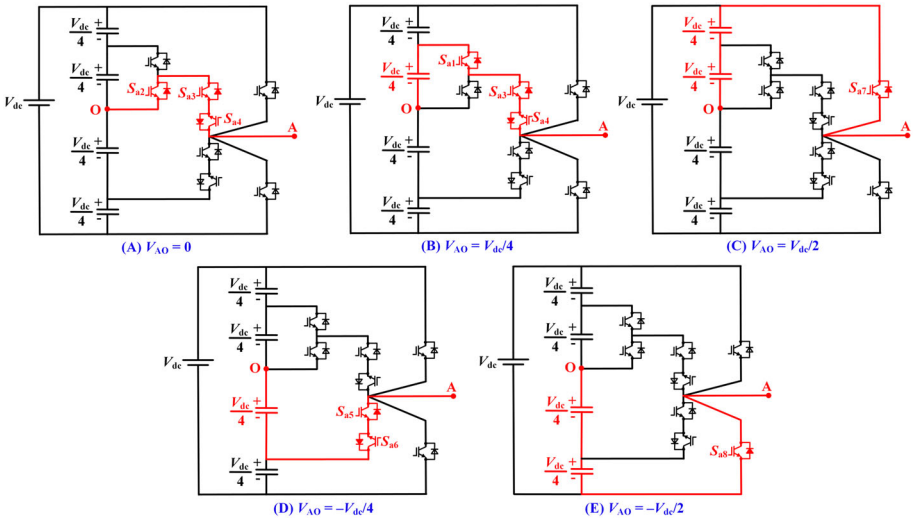

FIGURE 3 Operating modes in a fundamental cycle [Colour figure can be viewed at wileyonlinelibrary.com]

Mode-0 ($V_{AO} = 0$): In this mode, for zero output voltage, S_{a2}, S_{a3}, and S_{a4} are continuously gated. The conduction of a switch or its antiparallel diode is decided by the direction of i_A. If i_A is +ve, D_{a2}, S_{a3}, and D_{a4} conduct; otherwise, S_{a4}, D_{a3}, and S_{a2} conduct.

Mode-1 (V_{AO}=$V_{dc}/4$): When switching from Mode-0 to Mode-1, switch S_{a1} is triggered after the complete turnoff of S_{a2}. A sufficient dead time (t_d) is allowed between the switches S_{a1} and S_{a2}, to avoid the short circuiting of C_2. The switches S_{a3} and S_{a4} remain gated. This connects the pole point (A) to the positive terminal of the capacitor C_2. Therefore, $V_{AO} = V_{C2} = V_{dc}/4$. If i_A is +ve, S_{a1}, S_{a3}, and D_{a4} conduct; otherwise, S_{a4}, D_{a3}, and D_{a1} conduct.

Mode-2 ($V_{AO} = V_{dc}/2$): When switching from Mode-1 to Mode-2, switch S_{a7} is triggered after the complete turnoff of the switches conducting during Mode-1. This connects the terminal A to positive DC rail. Therefore, $V_{AO} = V_{C1} + V_{C2} = V_{dc}/2$. If i_A is +ve, S_{a7} conducts; otherwise, D_{a7} conducts.

Mode-3 ($V_{AO} = -V_{dc}/4$): In this mode, switches S_{a5} and S_{a6} are gated; this connects the terminal A to the negative terminal of C_3. Thus, $V_{AO} = -V_{C3} = -V_{dc}/4$. If i_A is −ve, S_{a5} and D_{a6} conduct; otherwise, S_{a6} and D_{a5} conduct.

Mode-4 ($V_{AO} = -V_{dc}/2$): When switching from Mode-3 to Mode-4, switch S_{a8} is triggered after the complete turnoff of the switches conducting during Mode-3. This connects the terminal A to negative DC rail. Therefore, $V_{AO} = -(V_{C3} + V_{C4}) = -V_{dc}/2$. If i_A is −ve, S_{a8} conducts; otherwise, D_{a8} conducts.

Table 1 summarizes the switching sequence for the generation of all the five levels present in the pole voltage (V_{AO}). The digits "1" and "0" represent the switching states of ON and OFF, respectively. It is noticed that a maximum of 9 (ie, 3 × 3) devices out of 24 conducts in any given mode and the number of switching transitions between any two voltage levels is not more than two. This results in reduced semiconductor losses and higher efficiency of the proposed topology.

3 | MODULATION TECHNIQUE AND CAPACITOR VOLTAGE BALANCING

3.1 | Pulse width modulation generation

In this paper, the level-shifted in-phase disposition sine pulse width modulation (LSIPD-SPWM) scheme is implemented for developing the control signals. This is due to the advantages of the lowest harmonic content in the output voltage as compared with the other PWM schemes such as selective harmonic elimination technique and space-vector PWM.[23,24] Figure 4 illustrates the schematic diagram of LSIPD-SPWM. It can be seen that the fundamental sine wave waveform is compared with a level-shifted in-phase carrier waves and the corresponding output pulses for each voltage level for one complete cycle. The required pulse pattern to each switch is generated using logic gates to produce the five-level output. Here, the change in magnitude of the modulation index (m_a) of the sine wave results in the change in the output pole voltages from three levels to five levels or vice versa.

TABLE 1 Switching states of the proposed nested five-level inverter (phase-a)

V_{AO}	S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}	No. of Conductor Devices/Phase
$V_{dc}/2$	0	0	0	0	0	0	1	0	1
$V_{dc}/4$	1	0	1	1	0	0	0	0	3
0	0	1	1	1	0	0	0	0	3
$-V_{dc}/4$	0	0	0	0	1	1	0	0	2
$-V_{dc}/2$	0	0	0	0	0	0	0	1	1

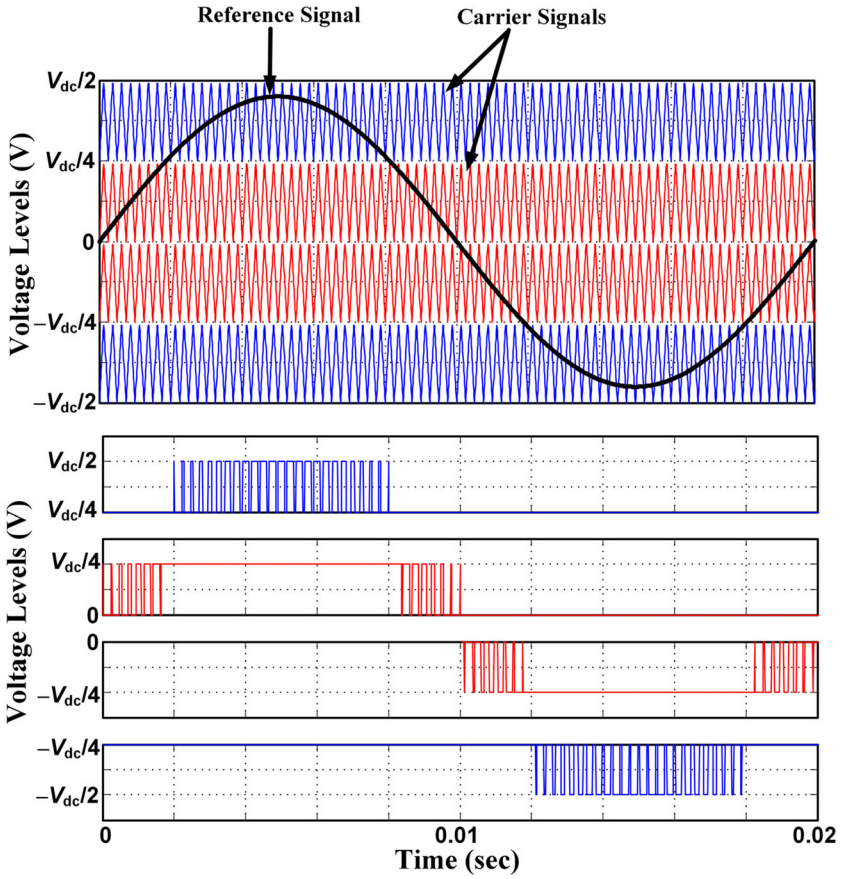

FIGURE 4 Generation of control pulses using level-shifted in-phase disposition sine pulse width modulation (LSIPD-SPWM) [Colour figure can be viewed at wileyonlinelibrary.com]

3.2 | Capacitor voltage balancing

In the proposed topology, four DC capacitors are connected across a single-input DC source. Normally, the balancing of these capacitor voltages is tedious due to unequal charging and discharging periods. Also, in most of the practical cases, unbalancing occurs in the middle capacitors. Therefore, to balance voltage across the DC-link capacitors, an auxiliary balancing circuit is constructed as shown in Figure 2. It consists of two inductors, two power switches, and a diode.[20] The two power switches S_{B1} and S_{B2} (balancing switches) are operated effectively in PWM mode to maintain the desired voltage across the DC-link capacitors. Figure 5 shows the flowchart for the implementation of the capacitor charging process. Here, the two balancing switches are operated at the same time by sensing the middle capacitor voltages V_{C2} and V_{C3} and charges to $V_{dc}/4$ each through the balancing inductors L_{B1} and L_{B2}. The AVBC ensures the voltage regulation of C_2 and C_3 and also the voltage balancing of capacitors C_1 and C_4, because the charging and discharging path for the C_1 and C_4 is associated with C_2 and C_3. Thus, the regulation of C_2 and C_3 voltages also ensures the balancing of C_1 and C_4 voltages.[25]

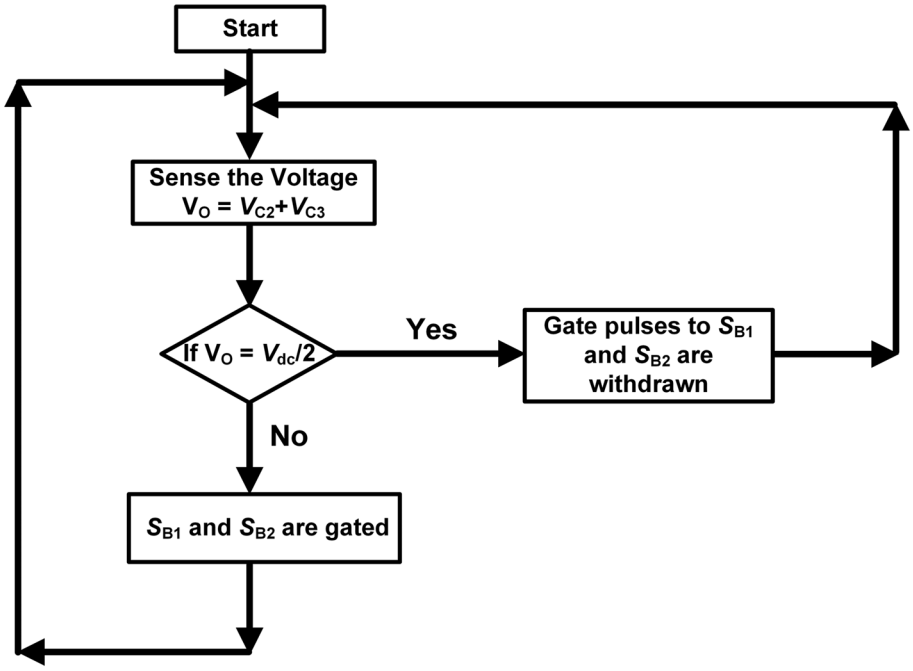

FIGURE 5 Flowchart for capacitor voltage balancing

4 | ADVANTAGES AND COMPARISON OF THE PROPOSED TOPOLOGY

The lower number of conducting switches and reduced TBV of the switches in each phase are the main advantages of the proposed nested 5L inverter. At any voltage level, two switches and a diode or one switch and a diode or a single switch conducts per phase, which imparts higher efficiency to the MLI. The calculated TBV of the switches in a three-phase configuration is 17% less compared with the NTT-5L inverter,[19] because the proposed topology does not require clamping diodes or FCs, which results in compactness and saving of floor space. The number of capacitors required is 33% less compared with the 5L inverter proposed by N. D. Dao et al.[21] The need for only one DC supply renders the topology suitable for all power grid applications (similar to NPC and FC). The proposed MLI reduces the requirement of DC sources by 83% compared with a conventional CHB inverter. Further, Table 2 provides a detailed comparison of proposed topology with conventional and recent topologies based on switches, device ratings, clamping diodes, flying capacitors, and the number of DC sources. Moreover, the absence of clamping diodes, flying capacitors, and simple control makes the proposed configuration very attractive for renewable as well as industrial applications.

TABLE 2 Comparison of various three-phase five-level inverter topologies

Topology	Switches (SWs)	Clamping Diodes	DC-link Capacitors	Flying Capacitors	Balancing Inductors	DC Sources	TBV of the SWs/Phase	Total Components
NPC-5L	24	18	4	-	-	1	$2V_{dc}$	47
FC-5L	24	-	4	18	-	1	$2V_{dc}$	47
CHB-5L	24	-	-	-	-	6	$2V_{dc}$	30
ANPC-5L[13]	24	-	2	3	-	1	$3V_{dc}$	30
NNPC-5L[16]	24	6	-	9	-	2	$2V_{dc}$	41
HFC-5L[24]	26	1	3	3	2	1	$3.5V_{dc}$	36
NTT-5L[19]	26	1	4	-	2	1	$6V_{dc}$	34
NTLC-5L (proposed)	26	1	4	-	2	1	$5.25V_{dc}$	34

Abbreviations: DC, direct current; TBV, total blocking voltage.

5 | RESULTS AND DISCUSSION

5.1 | Simulation results

In order to verify the feasibility of the proposed nested three-phase five-level inverter and the control scheme, first, the model was developed in the MATLAB/SIMULINK software using the Xilinx blocks. The parameters selected for both the simulation and experimental works are given in Table 3. The performance of the model is first tested in a simulation environment for a power rating of 3.5 kW and 0.9 power factor (PF) lagging. The magnitude of 720-V DC link is considered to produce 400 V (L-L) at the output. The LSIPD-SPWM control pulses are developed at 4-kHz switching frequency for both simulation and experimental work. In addition, a modulation index of 0.9 is chosen to produce the five-level output voltage waveforms.

Figure 6A-C shows the measured waveforms of pole voltages, line voltage, and their corresponding load currents of the proposed 5L inverter. The DC-link voltages of V_{C1} to V_{C4} across capacitors under steady state are given in Figure 6D. It can be noticed that the capacitor voltages are maintained constant at the average of 180 V and the voltage ripples are around 5% in V_{C1} and V_{C4} and 3% in V_{C2} and V_{C3}. This shows the effectiveness of the auxiliary balancing circuit in balancing the capacitor voltages during loading conditions. Also, Figure 6E illustrates the % total harmonic distortion (THD) of the synthesized inverter output pole-A voltage waveform, and most of the harmonics are dominated around the switching frequency of 4 kHz.

5.2 | Experimental results

Figure 7 depicts the prototype model of the proposed nested three-phase five-level inverter. The inverter circuit is built with IGBT-based VSI with in-built driver circuits. The auxiliary balancing circuit is constructed to balance the DC-link capacitors voltages. The control algorithm is implemented using a high-speed low-cost SPARTAN-6 (XC6SLX45) field-programmable gate array (FPGA). The output of the FPGA pulses is as low as a magnitude of 3.3 V and boosted to 15 V through an in-built driver circuit to trigger the IGBT switches. A 100-V DC power supply is used to feed the power circuit, and the response of the proposed topology is measured using a four-channel DPO3034 Tektronix Oscilloscope.

Figure 8A,B illustrates the response of pole voltages and a line voltage with the corresponding load current at an m_a of 0.9. Figure 8C,D illustrates the DC-link capacitor voltages for a step change in load current approximately from 2 to 5 A. It is observed that the developed control scheme and the AVBC well balance the DC-link capacitor voltages. Moreover, Figure 8E illustrates that the measured THD of pole-A voltage is 34.1%, which is very close to the simulated result of 33.85%. The close agreement between the simulation and experimental results shows the effectiveness of the proposed structure, and it is well suitable for medium-voltage applications

5.3 | Efficiency calculation

Figure 9 depicts the measured efficiency comparison of the proposed nested 5L inverter with NTT-5L inverter. The efficiency curves are evaluated in PSIM[26] using discrete IGBT thermal modules of distinct voltage ratings as per the device

TABLE 3 System parameters

Parameter	Simulation	Experimental
DC-link voltage	720 V	100 V
Output power	3.5 kW	500 W
Each capacitor voltage	180 V	25 V
Capacitors (C_1, C_2, C_3, and C_4)	1, 2, 2, 1 mF, respectively	1, 1, 1, and 1 mF, respectively
Inductors (L_{B1} and L_{B2})	1 and 1 mH, respectively	1 and 1 mH, respectively
Rated load	8 A	5 A
Switching frequency	4 kHz	4 kHz
Fundamental frequency	50 Hz	50 Hz

Abbreviation: DC, direct current.

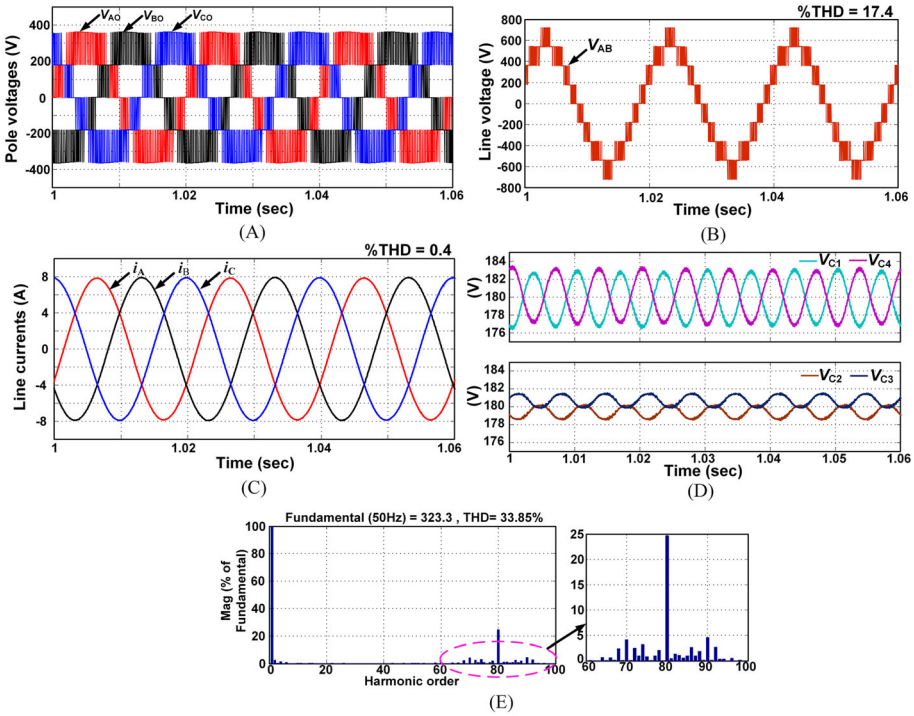

FIGURE 6 Simulation results. A, Pole voltages. B, Line voltage. C, Three-phase line currents. D, Direct current (DC)–link capacitor voltages. E, Harmonic spectrum of pole voltage (V_{AO}) [Colour figure can be viewed at wileyonlinelibrary.com]

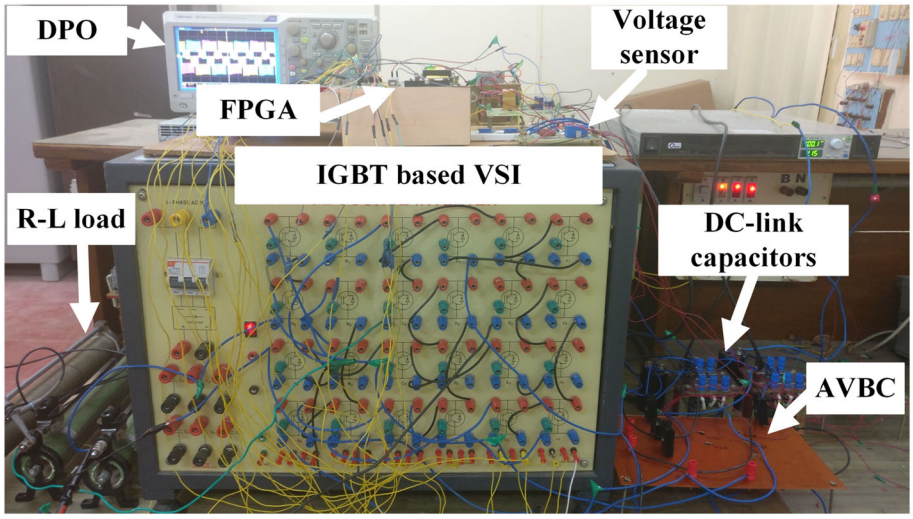

FIGURE 7 Experimental setup [Colour figure can be viewed at wileyonlinelibrary.com]

stress, at different loading conditions, wherein the maximum power output, m_a, and PF are fixed to 3.5 kW, 0.9 and 0.9 lag, respectively. Table 4 lists out the selected IGBT semiconductor devices for efficiency computation. It is noticed that the efficiency of the proposed configuration is high compared with the NTT-5L inverter and maximum efficiency of 95.7% is achieved. This shows the effectiveness of the proposed nested 5L inverter, and it is well suitable for medium-voltage applications.

5.4 | Applications

The proposed topology can be adopted for various applications:

1. It has the ability to operate in all four quadrants of V-I plane; hence, it is suitable for speed control of motor drives.[20]

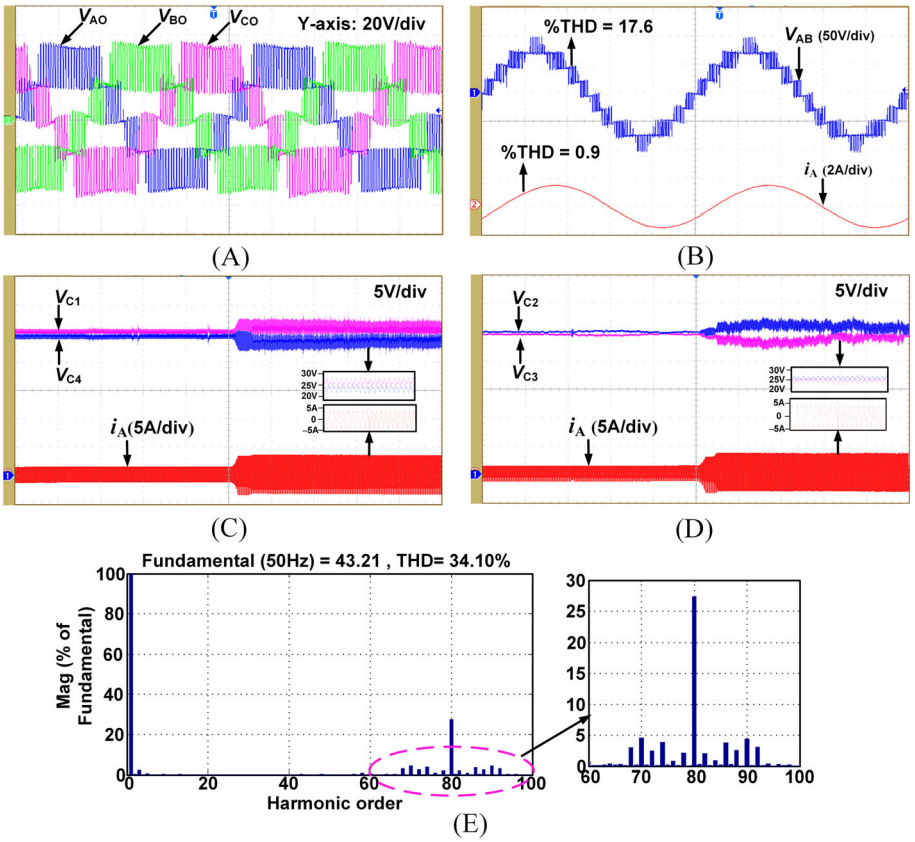

FIGURE 8 Experimental results at $m_a = 0.9$. A, Pole voltages. B, Line voltage (V_{AB}) and line current (i_A); time scale (4 ms/div). C, Variation of voltage across direct current (DC)–link capacitors C_1 and C_4 with regard to change in load. D, Variation of voltage across DC-link capacitors C_2 and C_3 with regard to change in load; time scale (4 s/div). E, Harmonic spectrum of pole-A voltage (from comma-separated values [CSV] file) [Colour figure can be viewed at wileyonlinelibrary.com]

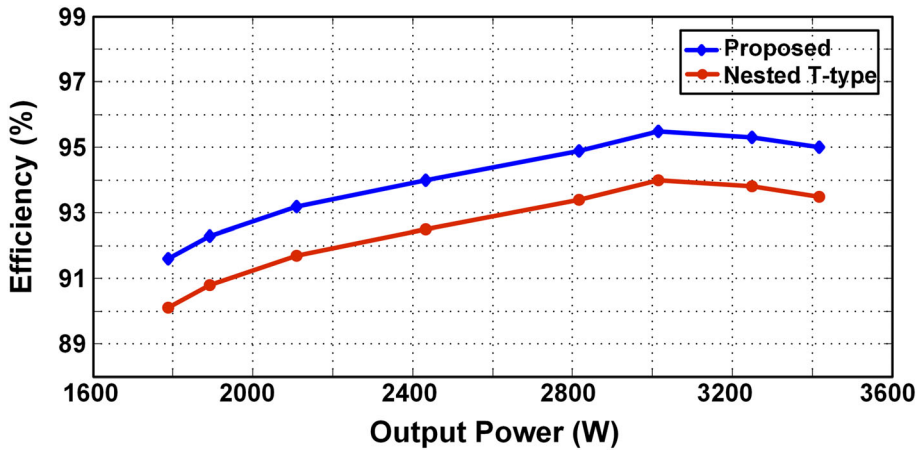

FIGURE 9 Efficiency curves [Colour figure can be viewed at wileyonlinelibrary.com]

2. It has the capability of absorb or delivering the reactive power; hence, it is suitable as a static volt-ampere reactive (VAR) compensator.[27]
3. The proposed topology also facilitates to use solar power at the DC input, to produce AC output from the inverter for grid integration. Hence, the proposed topology is suitable for grid integration of renewable energy sources.[6]
4. The input DC voltage can scaled to higher values to produce an output voltage of 3.3/6.6 kV, which makes the proposed topology suitable for medium-voltage industrial drives.[1,21]

TABLE 4 Selection of IGBTs for efficiency calculation

Switches	Device Voltage Stress (V) for V_{dc} = 720 V	Part Number	Device Parameters	
			BV_{CES} (V)	$V_{CES(sat)}$ (V)
S_{x1}, S_{x2}, S_{x4}, and S_{x6}	180	HGTG20N60A4D	600	1.8
S_{x3}	360	FGH40T70SHD	700	1.7
S_{x5}	540	IHW30N110R3	1100	1.55
S_{x7} and S_{x8}	720	FGA20S140P	1400	1.9

Note. x = phase number = A, B, and C; BV_{CES} = collector to emitter breakdown voltage; $V_{CES(sat)}$ = collector to emitter saturation voltage.

6 | CONCLUSION

This paper introduces an improved nested MLI configuration for single DC source-fed three-phase five-level hybrid inverter for medium-voltage applications. This configuration is developed by the nested connection of TLCs to build a common DC link with a reduced blocking voltage of the switches and to get rid of FCs. LSIPD-SPWM control scheme using logic functions is employed in Xilinx FPGA processor. The merits of the proposed topology are investigated with a single DC source, reduced component count, and TBV of the switches. Finally, the working and feasibility of the proposed 5L inverter are examined through simulation and experimental studies under steady state as well as during load changes. The DC-link voltages are well balanced with the AVBC using the simplest control scheme. Maximum efficiency of 96% can be achieved with the proposed configuration, which makes it suitable for various industrial and renewable applications.

ORCID

Kirubakaran Annamalai https://orcid.org/0000-0002-3800-1776

REFERENCES

1. Tolbert LM, Peng FZ, Habetler TG. Multilevel converters for large electric drives. *IEEE Trans Ind Appl*. 1999;35(1):36-44.
2. Veenstra M, Rufer A. Control of a hybrid asymmetric multilevel inverter for competitive medium-voltage industrial drives. *IEEE Trans Ind Appl*. 2005;41(2):655-664.
3. Sotoodeh P, Miller RD. Design and implementation of an 11-level inverter with FACTS capability for distributed energy systems. *IEEE J Emerg Sel Top Power Electron*. 2014;2(1):87-96.
4. Flourentzou N, Agelidis VG, Demetriades GD. VSC-based HVDC power transmission systems: an overview. *IEEE Trans Power Electron*. 2009;24(3):592-602.
5. Deng N, Wang P, Zhang XP, Tang G, Cao J. A DC current flow controller for meshed modular multilevel converter multiterminal HVDC grids. *CSEE J Power Energy Syst*. 2015;1(1):43-51.
6. Agrawal R, Jain S. Multilevel inverter for interfacing renewable energy sources with low/medium and high-voltage grids. *IET Renew Power Gener*. 2017;11(14):1822-1831.
7. Jena S, Panda G, Peesapati R. FPGA-based implementation for improved control scheme of grid-connected PV system with 3-phase 3-level NPC-VSI. *Int J Circ Theor Appl*. 2018;46(4):942-964.
8. Choupan R, Nazarpour D, Golshannavaz S. A simple unit cell structure for an efficient sketch of series-connected multilevel inverters. *Int J Circ Theor Appl*. 2017;45(10):1397-1417.
9. Santhosh Kumar M, Borghate VB, Karasani RR, Sabyasachi S, Suryawanshi HM. A fault tolerant modular multilevel inverter topology. *Int J Circ Theor Appl*. 2018;46(5):1028-1043.
10. Nabae A, Takahashi I, Akagi H. A new neutral point clamped PWM inverter. *IEEE Trans Ind Appl*. 1981;17(5):518-523.
11. Lai J, Peng F. Multilevel converters—a new breed of power converters. *IEEE Trans Ind Appl*. 1996;32(3):509-517.
12. Rodriguez J, Bernet S, Wu B, Pontt JO, Kouro S. Multilevel voltage-source-converter topologies for industrial medium-voltage drives. *IEEE Trans Ind Electron*. 2007;54(6):2930-2945.
13. Barbosa P, Steimer P, Steinke J, Winkelnkemper M, Celanovic N. Active-neutral-point-clamped (ANPC) multilevel converter technology. European Conference on Power Electronics and Applications, 2005:1–10.
14. Islam R, Mahfur-Ur-Rahman AM, Muttaqi KM, Sutanto D. State of the art of the medium-voltage power conversion technologies for grid integration of solar photovoltaic power plants. *IEEE Trans Energy Conv*. 2019;34(1):372-384.

15. Narimani M, Wu B, Cheng Z, Zargari NR. A new nested neutral-point-clamped (NNPC) converter for medium-voltage (MV) power conversion. *IEEE Trans Power Electron*. 2014;29(12):6375-6382.
16. Narimani M, Wu B, Navid Reza Z. A novel five-level voltage source inverter with sinusoidal pulse-width modulator for medium-voltage applications. *IEEE Trans Power Electron*. 2016;31(3):1959-1967.
17. Bahrami A, Narimani M. A sinusoidal pulse width modulation (SPWM) technique for capacitor voltage balancing of a nested T-type four-level inverter. *IEEE Trans Power Electron*. 2019;34(2):1008-1012.
18. Bhagwat PM, Stefanovic VR. Generalized structure of a multilevel PWM inverter. *IEEE Trans Ind Appl*. 1983;IA-19(6):1057-1069.
19. Santos ECD, Muniz JHG, Da Silva ERC, Jacobina CB. Nested multilevel topologies. *IEEE Trans Power Electron*. 2015;30(8):4058-4068.
20. Rojas R, Ohnishi T, Suzuki T. PWM control method for a four-level inverter. *IEE Proc—Electric Power Appl*. 1995;142(6):390-396.
21. Dao ND, Lee D. Operation and control scheme of a five-level hybrid inverter for medium voltage motor drives. *IEEE Trans Power Electron*. 2018;33(12):10178-10187.
22. Backlund B, Carroll E. Voltage ratings of high power semiconductors. Semiconductors, 2006.
23. Carrara G, Gardella S, Marchesoni M, Salutari R, Sciutto G. A new multilevel PWM method: a theoretical analysis. *IEEE Trans Power Electron*. 1992;7(3):497-505.
24. Agelidis VG, Calais M. Application specific harmonic performance evaluation of multicarrier PWM techniques. Proc IEEE-PESC, 1998:172–178.
25. Choi J, Kang F. Seven-level PWM inverter employing series-connected capacitors paralleled to a single DC voltage source. *IEEE Trans Ind Electron*. 2015;62(6):3448-3459.
26. Kuncham SK, Annamalai K, Nallamothu S. A new structure of single-phase two-stage hybrid transformerless multilevel PV inverter. *Int J Circ Theor Appl*. 2018;47:1-23.
27. Peng FZ, Lai JS, McKeever JW, Van Coevering J. A multilevel voltage-source inverter with separate DC sources for static VAR generation. *IEEE Trans Ind Appl*. 1996;32(5):1130-1138.

How to cite this article: Tirupathi A, Annamalai K, Veeramraju Tirumala S. A new structure of three-phase five-level inverter with nested two-level cells. *Int J Circ Theor Appl*. 2019;47:1435–1445. https://doi.org/10.1002/cta.2648