A Four-Level Open-End Winding Induction Motor Drive With a Nested Rectifier–Inverter Combination With Two DC Power Supplies

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***Abstract*—This paper proposes a new nested rectifier–inverter circuit topology for a four-level (4-L) open-end winding induction motor drive (OEWIMD). To realize the 4-L inversion, the nested rectifier–inverter topology operates with unequal dc-link voltages, which are in the ratio of 2:1. The proposed topology has the inherent ability of avoiding the overcharging of the lower dc-link voltage capacitor by its higher voltage counter-part unlike in the case of the power circuit configuration proposed in the earlier literature. This paper also proposes a new sample-averaged zero-sequence elimination pulsewidth modulation (PWM) scheme for the proposed circuit configuration to avoid the flow of zero-sequence current through the motor windings. It is shown that the proposed power circuit is also capable of displaying immunity to a particular type of fault, as it can produce the same output voltage despite the unbalancing of one of the dc-link capacitor voltages without changing the modulation strategy. The proposed 4-L OEWIMD along with the associated PWM schemes is simulated and is validated with experimental results.**

***Index Terms*—Capacitor overcharging, fault tolerant, nested rectifier–inverter, open-end winding induction motor drive (OEWIMD), sample-averaged zero-sequence elimination (SAZE), zero-sequence voltage (ZSV).**

I. Introduction

MULTILEVEL inverters (MLIs) are gaining popularity in applications such as ac drives, active power filters, HVdc transmission systems, renewable energy sources, hybrid electric vehicles, ship-propulsion, etc. Compared to the conventional 2-level (2-L) voltage source inverters (VSIs), the advantages obtained with MLIs are well documented. Some of these are as follows:

1) high output voltages with low voltage power semiconductor devices;
2) reduced harmonic distortion;
3) lower electromagnetic interference;
4) lower dv/dt on semiconductor devices;
5) operation at lower switching frequencies [1].

The classical MLIs reported in the literature are as follows:

1) neutral point clamped (NPC) MLI;
2) flying capacitor (FC) MLI;
3) cascaded H-bridge (CHB) MLI [2].

A recent addition to the family of MLIs, which is applicable exclusively to the ac motor drive systems, is the open-end winding configuration. In this power circuit configuration, two VSIs of two or higher number of levels feed either ends of the load. When such a configuration is applied to an induction motor, it results in the so-called open-end winding induction motor (OEWIM) drive [3]. The OEWIM is obtained either by opening the star-point for the star-connected motor or by opening the end-connections for the delta-connected stator windings, respectively.

The OEWIM drive (OEWIMD) offers several advantages over their conventional counterparts. Some of them are as follows:

1) redundancy in the space vector locations (SVLs), which offers the possibility to implement several interesting pulsewidth modulation (PWM) schemes [4]–[8];
2) adequacy of lower voltage ratings of the semiconductor devices;
3) capability of operating under faulted conditions;
4) absence of clamping diodes (when compared to the NPC MLI);
5) avoidance of the problems associated with voltage imbalance of floating capacitors (when compared to the FC MLI);
6) employment of a lower number of dc sources (as compared to the CHB MLI).

The principal drawbacks of the OEWIMD are as follows:

1) the presence of zero-sequence voltages (ZSVs) in the motor phase windings;
2) the non-uniformity of voltage ratings of the devices;
3) the requirement of additional cabling.

The ZSVs cause zero-sequence current (ZSC), which causes an additional power-loss in the motor and call for a conservative peak-current rating of the power semiconductor devices.

In the past literature, different circuit topologies were reported for OEWIMD to generate three-level [4], four-level (4-L) [5], five-level [6], seven-level [7], and nine-level [8] by using either the conventional 2-L VSIs or the three-level NPC MLI or the cascaded connection of two 2-L VSIs. These power circuit configurations generally use more than one dc power supply to realize more than three levels. Recently, an *n*-level modular MLI using single dc-link power supply is also proposed [9] with fault-tolerant capability.

However, at a higher number of voltage levels, the cost and complexity of MLI circuits increase. The reliability of the system could decrease with the increase in the number of compo-

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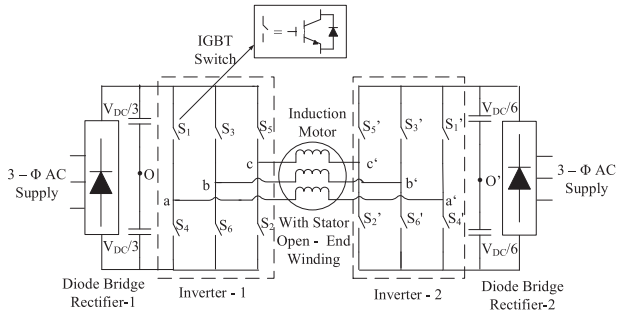


Fig. 1. 4-L OEWIM with isolated dc-power supplies.

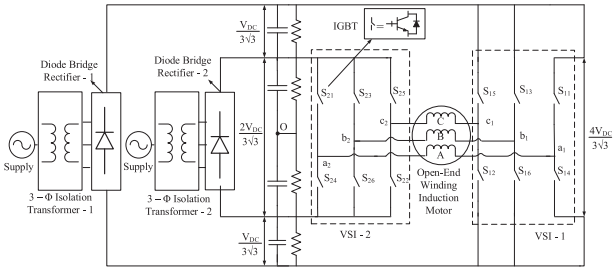


Fig. 2. Proposed topology for 4-L OEWIMD.

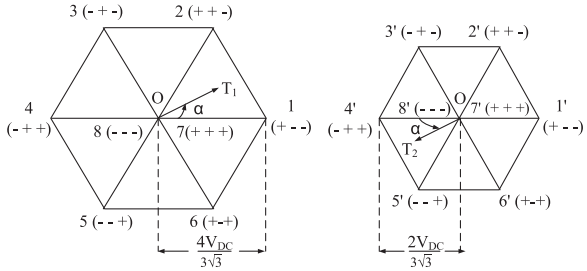


Fig. 3. Individual SVLs of VSI-1 (left) and -2 (right).

nents and the associated control and the driver circuitry. Hence, one of the concerns in the design of MLIs is the exploration of new topologies with reduced device count.

Though it is possible to implement the different number of levels with the open-end winding configuration, 4-L inversion seems to be an optimal proposition [10]. The spectral quality of the output would not improve appreciably despite a large number of switching devices, diodes, and capacitors beyond 4-L inversion. The motivation is to improvise that the existing 4-L OEWIMD owes to this fact, coupled with the consideration of reducing the number of components, to enhance reliability.

The first 4-L OEWIMD, proposed in [5], is realized by feeding an OEWIM with two 2-L conventional VSIs with unequal dc-link voltages, which are in the ratio of 2:1 (see Fig. 1). The main difficulty associated with this power circuit is that for some of the space vector switching combinations, the lower dc-link voltage capacitor is overcharged by its counterpart (i.e., higher dc-link voltage capacitor). The undesirable effects of such an overcharging phenomenon are well documented in [5].

To avoid the overcharging of the lower voltage dc-link capacitor, a circuit topology was proposed in [11], which embeds a rectifier–inverter combination operating with a lower dc-link voltage in an outer combination of similar construction operating with a higher dc-link voltage. This topology uses the decoupled sample-averaged zero-sequence elimination (DSAZE) space vector pulsewidth modulation (SVPWM) [11] and the sample-averaged zero-sequence elimination (SAZE) SVPWM techniques [12], to avoid the ZSVs. However, this power circuit configuration uses three isolation transformers and three diode bridge rectifiers, causing an increase in the device count.

The work reported in [13] uses a floating capacitor bank connected to the second bridge converter (lower dc-link voltage, Fig. 1) and eliminates the bulky isolation transformer. However, as stated in [3], the efficiency in this configuration may have to be compromised due to the charging of the bulky capacitor through the motor windings.

Recently, a new discontinuous PWM was proposed to the circuit configuration shown in Fig. 1 [14], to avoid the overcharging of lower dc-link voltage capacitor. However, the capability of the proposed technique to avoid such an overcharging, arising out of higher dwell times at those SVLs, where *all* the space vector combinations result in overcharging, is not reported under loaded conditions.

In this paper, a modified nested rectifier–inverter topology is proposed for the 4-L OEWIMD, in which one side of the OEWIM is fed with a 2-L VSI and the other end is fed with a nested rectifier–inverter combination. The proposed topology uses only two isolation transformers, to avoid the overcharging phenomenon of the lower dc-link voltage capacitor. The dc link is better utilized in this power circuit as the sum of the individual dc-link voltages of the constituent inverters is equal to $0.77\ V_{\rm DC}$ (i.e., a decrease of around 23%). The ZSVs are eliminated by employing 1) the DSAZE SVPWM technique [11] and 2) a modified version of the SAZE SVPWM technique. The performance indices considered for the comparative evaluation are conduction loss, switching loss, and the total losses in the dual-inverter system.

The rest of the paper is organized as follows. The detailed description of the proposed topology, avoidance of the overcharging phenomenon and its comparison with other 4-L topologies are presented in Section II. Section III explains the SVPWM techniques used for the proposed topology to avoid the ZSVs. The detailed simulation, experimental results, fault-tolerant capability, and performance evaluation of the SVPWM techniques for the proposed topology are presented in Section IV. Finally, Section V summarizes the conclusion.

II. New Nested Rectifier–Inverter Configuration for 4-L OEWIMD

A. Description of Topology

The proposed circuit topology for the 4-L open-end winding induction motor drive (OEWIMD) is shown in Fig. 2. The proposed configuration consists of two isolation transformers, which maintain the rectified dc-link voltages that are in the ratio of 2:1. Two conventional 2-L VSIs (VSI-1 and VSI-2) are used in the proposed topology, wherein VSI-1 feeds one side of the OEWIMD, whereas VSI-2 feeds the other side and is nested within VSI-1. The individual space vectors corresponding to the VSI-1 and -2 (see Fig. 2) are shown in Fig. 3. The resultant space vector diagram of the dual-inverter configuration consists of 64 (8×8) space vector combinations, spread over 37 locations with 54 sectors, as shown in Fig. 4.

The pole voltage of VSI-1 (v_{a_1o}) is switched between $2V_{\rm DC}/3\sqrt{3}$ and $-2V_{\rm DC}/3\sqrt{3}$. Similarly, the pole voltage of VSI-2 (v_{a_2o}) is switched between $V_{\rm DC}/3\sqrt{3}$ and $-V_{\rm DC}/3\sqrt{3}$.

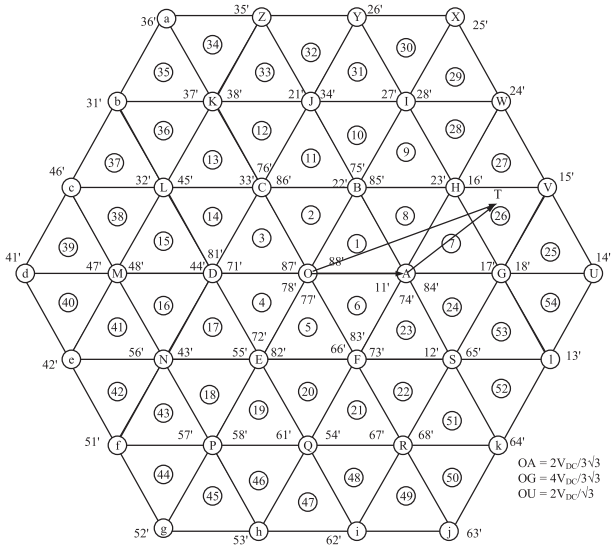


Fig. 4. Resultant space vector diagram of the proposed 4-L OEWIMD.

TABLE I
4-L IN THE PHASE VOLTAGE OF PROPOSED TOPOLOGY

v_{a_1o}	v_{a_2o}	$v_{a_1a_2} = v_{a_1o} - v_{a_2o}$
$-2V_{DC}/3\sqrt{3}$	$V_{DC}/3\sqrt{3}$	$-V_{DC}/\sqrt{3}$
$-2V_{DC}/3\sqrt{3}$	$-V_{DC}/3\sqrt{3}$	$-V_{DC}/3\sqrt{3}$
$2V_{DC}/3\sqrt{3}$	$V_{DC}/3\sqrt{3}$	$V_{DC}/3\sqrt{3}$
$2V_{DC}/3\sqrt{3}$	$-V_{DC}/3\sqrt{3}$	$V_{DC}/\sqrt{3}$

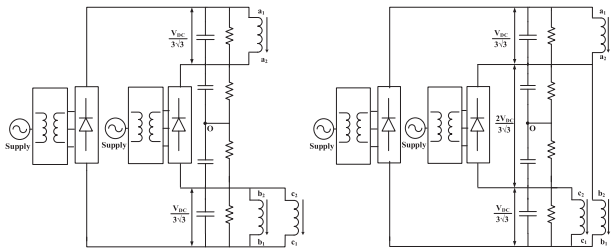


Fig. 5. OEWIM winding connections for the switching combinations $11'$ (left) and $12'$ (right).

Thus, the resultant voltage applied across the system (see Fig. 2) displays 4-Ls in the dual inverter (motor phases). The different voltage levels of phase-A $(v_{a_1a_2})$ are listed in Table I.

Table I clearly demonstrates that the *open-end winding* topology is capable of rendering 4-L inversion if the dc-link voltages of the individual inverters are maintained in the ratio of 2:1.

In general, the ZSV expression for the OEWIMD is given by [15]

$$v_{zs} = \frac{1}{3}\left(v_{a_1a_2} + v_{b_1b_2} + v_{c_1c_2}\right) \tag{1}$$

where

$$v_{a_1a_2} = v_{a_1o} - v_{a_2o}$$
$$v_{b_1b_2} = v_{b_1o} - v_{b_2o}$$
$$v_{c_1c_2} = v_{c_1o} - v_{c_2o}.$$

Now, (1) can be rewritten as

$$v_{zs} = \frac{1}{3}\left(v_{a_1o} - v_{a_2o} + v_{b_1o} - v_{b_2o} + v_{c_1o} - v_{c_2o}\right)$$
$$v_{zs} = \frac{1}{3}\left(v_{a_1o} + v_{b_1o} + v_{c_1o}\right) - \frac{1}{3}\left(v_{a_2o} + v_{b_2o} + v_{c_2o}\right)$$
$$v_{zs} = v_{zs_1} - v_{zs_2}. \tag{2}$$

Thus, from (2), it can be concluded that the ZSV of the OEWIMD is the difference between the ZSVs of the individual inverters of the dual-inverter system.

This ZSV causes the circulation of the ZSC in the proposed topology. The ZSC is principally determined by the zero-sequence impedance, which in turn is determined by the stator-leakage reactance of the motor [16].

B. Avoidance of Lower DC-Link Voltage Capacitor Overcharging

As explained in [5], for the circuit configuration shown in Fig. 1, the switching combinations $11'$, $22'$, $33'$, $44'$, $55'$, $66'$, $12'$, $16'$, $23'$, $34'$, $45'$, and $56'$ (see Fig. 4) overcharge the lower dc-link voltage capacitor by its counterpart.

The present topology avoids such an undesirable overcharging while preventing the flow of the ZSC. For the switching combinations $11'$ and $12'$, the avoidance of such an overcharging is explained in the following paragraphs:

For the switching combination $11'$, VSI-1 assumes state 1 ($+--$), whereas VSI-2 assumes state $1'$ ($+--$). Consequently, the insulated-gate bipolar transistor (IGBTs) S_{11}, S_{16}, and S_{12} are turned ON for VSI-1, whereas the IGBTs S_{21}, S_{26}, and S_{22} are turned ON for VSI-2. Fig. 5 (left) refers to the equivalent circuit of the proposed topology (see Fig. 2) for the switching combination $11'$. Phase-A winding of the OEWIM is directly connected across the positive rails of the isolated power supplies, whereas phase-B and -C windings of the OEWIM are connected across the negative rails of the isolated power supplies. A similar situation prevails for the combinations $33'$ and $55'$, wherein one of the motor winding either B or C is directly connected across the positive rails of the isolated power supplies. For the combinations $22'$, $44'$, and $66'$, two motor windings are connected between the positive rails of the isolated power supplies. In all of these circuit situations, the capacitor dc-link voltage of VSI-1 is not connected to the counterpart capacitors of VSI-2. From this, it can be concluded that the capacitor voltages are balanced and are maintained in the ratio of 2:1.

For the switching combination $12'$, the equivalent circuit of the present topology is depicted in Fig. 5 (right). It may be readily observed that the dc-link capacitors of VSI-2 are not connected to its high-voltage counterpart in this circuit situation also. The vector combination $16'$ also results in a similar circuit situation, wherein the motor windings B and C reverse their roles.

It can therefore be concluded that the overcharging of the lower dc-link voltage capacitors by their higher dc-link voltage counterparts is avoided in the proposed topology, as is evident from Fig. 5, and similar explanation can be applicable to the other switching combinations.

The concept of balancing the capacitor voltages in the proposed topology for 2-L and 4-L operation is explained in the equivalent circuits presented in Fig. 6. The capacitor balancing for 2-L operation is depicted in Fig. 6(a). The 2-L operation is obtained by employing the voltage vector combinations:

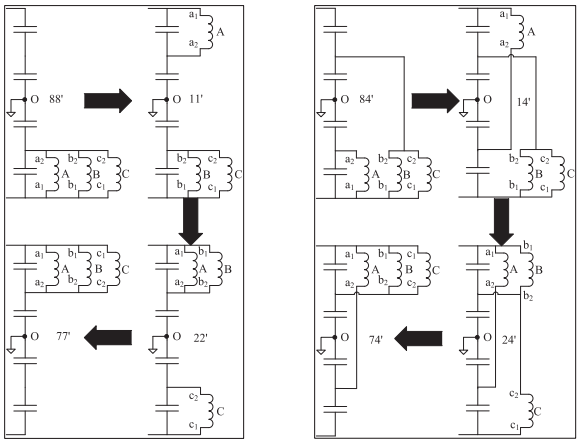


Fig. 6. OEWIM phase connections during mode-by-mode transition. (a) 2-L operation. (b) 4-L operation.

TABLE II
COMPARISON BETWEEN 4-L MLI TOPOLOGIES

Component	Voltage Rating	4-Level			
		NPC	FC	*Ref [11]	*Proposed Topology
IGBT	$2V_{DC}/3$	0	0	6	6
	$V_{DC}/3$	18	18	6	6
Clamping diodes	$V_{DC}/3$	12	0	0	0
Diodes in Bridge Rectifier	V_{DC}	6	6	0	0
	$2V_{DC}/3$	0	0	6	6
	$V_{DC}/3$	0	0	0	6
	$V_{DC}/6$	0	0	12	0
Floating capacitors	$2V_{DC}/3$	0	12	0	0
Uncontrolled DC Sources	$2V_{DC}/3$	0	0	1	1
	$V_{DC}/3$	1	1	0	1
	$V_{DC}/6$	0	0	2	0
Total		37	37	33	26

*The required total dc-link voltage is $0.77^{*}V_{DC}$.

$88' - 11' - 22' - 77'$, i.e., sector OAB belonging to the core-hexagon ABCDEF (see Fig. 4). Similarly, Fig. 6(b) depicts the capacitor balancing for the 4-L operation, wherein the voltage vector combinations $84' - 14' - 24' - 74'$ (i.e., sector AUW in Fig. 4) are selected.

C. Comparison With Other 4-L MLI Topologies

The comparison between the proposed topology and previously reported 4-L MLI topologies for induction motor drives is summarized in Table II. It is generally known that any MLI, irrespective of its topology needs an isolation transformer for high-power high-voltage applications [17]–[20]. Also, the power rating of the transformer corresponds to that of the MLI. Thus, the sum of individual ratings of the constituent transformers would practically remain the same across the circuit topologies. From this discussion, it is evident that even though the operation of this circuit is identical to the one proposed in [11], the number of dc-power supplies are reduced from 3 to 2 in the proposed circuit. The number of IGBTs used in the proposed topology and recently proposed topology [11] is 12, whereas in the NPC and FC MLI topologies, the count is 18. The number of isolation transformers used in the present topology is two, whereas the required isolation transformers are three in the power circuit proposed in [11]. The total device count in the proposed topology is 26, whereas in [11], NPC and FC MLIs, the count is 33, 37, and 37, respectively. As the overall device count of the proposed topology is less as compared to others, the reliability of the proposed topology is increased and it does not require fast recovery clamping diodes and floating capacitors of large ratings as compared to NPC and FC MLIs.

III. SVPWM TECHNIQUES FOR THE ELIMINATION OF ZSVS

The OEWIMD configuration shown in Fig. 1 mainly suffers from two problems: 1) overcharging of the lower dc-link voltage capacitor by its counterpart and 2) the presence of the ZSVs across the motor phase windings.

The present topology avoids the problem of overcharging as explained in Section II. To eliminate the ZSVs, the SVPWM techniques called SAZE and DSAZE proposed for the 3-L OEWIMD in [21] are extended to the topology presented in [11]. The proposed SVPWM techniques do not require any lookup table and sector identification and are implemented by using the instantaneous phase reference voltages. The proposed topology uses these two SVPWM techniques to eliminate the ZSV of the 4-L OEWIMD [11], [12].

The SVPWM techniques are explained by assuming that the reference voltage vector (v_{sr}) OT is located in sector 26 (see Fig. 4). The vector **OU** represents the total dc-link voltage required by the dual-inverter system. These two vectors are related by the modulation index $(\boldsymbol{m}_a)$, which is defined as

$$m_a = \frac{|v_{sr}|}{2V_{\mathrm{DC}}/\sqrt{3}}. \tag{3}$$

The motor is operated with the open-loop v/f control. At the edge of the linear modulation (i.e., $m_a = \sqrt{3}/2$), the rated fundamental voltage and the frequency component (f_{base}) of the OEWIMD are 400 V (line–line, RMS) and 50 Hz, respectively. The frequency of the fundamental component corresponding to m_a is given in the following equation:

$$f_1 = \frac{f_{\mathrm{base}} \times m_a}{\sqrt{3}/2}. \tag{4}$$

The vector **OT** of the dual-inverter system is synthesized with $N_{\mathrm{S}} = 66$ samples/cycle irrespective of the fundamental frequency, and the sampling time of the dual-inverter system is given as

$$T_S = 1/\left(f_1 \times N_S\right). \tag{5}$$

In the DSAZE PWM scheme, the reference vector **OT** is decomposed into two anti-phased components, which are in the ratio of the respective dc-link voltages of the individual inverters (i.e., 2:1). Both of these components are then synthesized independently using the principles of space vector modulation. While the DSAZE PWM scheme modulates each VSI individually, the SAZE PWM scheme views the entire dual-inverter scheme as a single entity. In the SAZE scheme, the reference vector **OT** is resolved into two components **OA** and **AT** (see Fig. 4). The vectors **OA** and **AT** are named as clamping and switching vectors, respectively. The switching vector is switched around the nearest sub-hexagonal center of the clamped vector [15] and [21]. The PWM scheme presented in [15] avoids of the overcharging of the lower dc-link capacitor, whereas the PWM suggested in [21] manages to suppress the ZSC through the motor phase windings by the dynamic balancing of the ZSC. In this paper, these two PWM strategies are combined. Since the dc-link capacitor of the nested inverter has the tendency to get overcharged, it is clamped emulating the PWM scheme

proposed in [15]. Thus, this PWM technique is named as the nested inverter clamped sample-averaged zero-sequence elimination (NICSAZE). The detailed principle operation of both PWM techniques is explained as follows.

A. DSAZE PWM Technique

As mentioned above, the reference voltage vector **OT** is resolved into two components $\mathbf{OT}_1$ and $\mathbf{OT}_2$ in the ratio of 2:1, as shown in Fig. 3, which are anti-phased (see Fig. 3). The switching algorithm presented in [22] for the 2-L VSI is extended to the dual-inverter system of the present topology. The imaginary switching time periods [22] for VSI-1 are given as

$$T_{xs_1} = \frac{T_s}{4V_{\mathrm{DC}}/3\sqrt{3}}\frac{2v_{xs}}{3} \quad x \in a,\ b,\ c. \tag{6}$$

The effective time period for VSI-1, where the power transfers from input dc side to the output ac side of the inverter is given as

$$T_{\mathrm{eff}_1} = T_{\max_1} - T_{\min_1} \tag{7}$$

where $T_{\max_1} = \max(T_{xs_1}), T_{\min_1} = \min(T_{xs_1})\ \ x \in a, b, c.$

The time period where no power flows from the input dc side to the output ac side of the inverter is called as the zero-vector (or the null-vector) time period and is denoted as T_N. The null-vector time periods for VSI-1 is given by

$$T_{N_1} = T_s - T_{\mathrm{eff}_1}. \tag{8}$$

The offset time needed for the center spacing of the effective time period within the sampling time interval of $\boldsymbol{T}_s$ for VSI-1 is given as

$$T_{\mathrm{offset}_1} = T_{N_1}/2 - T_{\min_1}. \tag{9}$$

It is shown in [22] that the phase switching time periods T_{gx_1} for VSI-1 are related to imaginary switching time periods T_{xs_1} by a simple expression

$$T_{gx_1} = T_{xs_1} + T_{\mathrm{offset}_1} \quad x \in a,\ b,\ c. \tag{10}$$

It is shown in [5] that the phase switching time periods of VSI-2 are simply obtained as

$$T_{gx_2} = T_s - T_{gx_1}. \tag{11}$$

It is also proven in [5] that the offset time needed to eliminate the ZSVs in DSAZE PWM technique, is given as

$$T_{\mathrm{offset}} = T_s/2. \tag{12}$$

By using (4) and (5), the sampling time period T_s can be rewritten in terms of modulation index and number of samples as

$$T_s = \frac{\sqrt{3}}{2\left(f_{\mathrm{base}} \times m_a \times N_S\right)}. \tag{13}$$

Now, by using (13), (12) can be rewritten as

$$T_{\mathrm{offset}} = \frac{\sqrt{3}}{4(f_{\mathrm{base}} \times m_a \times N_S)}. \tag{14}$$

B. NICSAZE SVPWM Strategy

The NICSAZE SVPWM technique, proposed for the present topology, is explained with help of Fig. 7. The resultant space vector diagram of the dual-inverter system, shown in Fig. 7, is divided into six regions, which are centered around the SVLs *A*, *B*, *C*, *D*, *E*, and *F*. A typical hexagon centered on the sub-hexagonal center "*A*" (the hexagon UWJDQk) is also shown in Fig. 7, with a hatched boundary.

Assume that the reference vector for the dual-inverter system is located in sector 27 (vector **OT** in Fig. 7). It is intended to realize this vector with the help of the component sets: either $\{\mathrm{OA},\ \mathrm{AT}\}$ or $\{\mathrm{OB},\ \mathrm{BT}\}$. The space vectors available at A, U, and W are utilized to realize the vector $\overline{\mathrm{AT}}$ in the average sense. Similarly, the vectors available at the locations B, V, and X can be used to synthesize the vector $\overline{\mathrm{BT}}$. Thus, by using the vectors $\overline{\mathrm{OA}}$ and $\overline{\mathrm{OB}}$ as biasing vectors and the vectors $\overline{\mathrm{AT}}$ and $\overline{\mathrm{BT}}$ as switching vectors, one may construct the overall reference vector $\overline{\mathrm{OT}}$ using the method of space vector modulation.

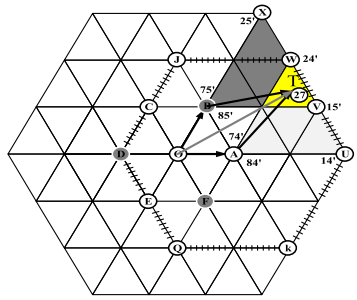


Fig. 7. Principle operation of NICSAZE SVPWM.

Vectors such as $\overline{\mathrm{OA}},\ \overline{\mathrm{OB}},\ \overline{\mathrm{OC}}$, etc., are applied to the dual-inverter system with VSI-2 and remain clamped throughout a given sample time period. On the other hand, VSI-1 acts as the switching inverter and produces the switching vectors such as $\overline{\mathrm{AT}},\ \overline{\mathrm{BT}},\ \overline{\mathrm{CT}}$, etc. (see Fig. 4).

For the switching inverter (i.e., VSI-1), the space vector switching locations are switched, respectively, for the time periods T_N, T_1, and T_2, which sum up to the sampling time period T_s.

To avoid the common mode voltages on average sense, the null vector switching time period (T_N) is divided in the ratio of $(1-x)T_N$ and xT_N [21] to strategically place the effective time period (T_1+T_2) in T_s. Let it be assumed that $\overline{\mathrm{OA}}$ and $\overline{\mathrm{AT}}$ are the clamping and switching vectors, respectively. The vector $\overline{\mathrm{OA}}$ is applied to the dual-inverter system by clamping VSI-2 to the state of $4'(-++)$ (see Fig. 4). The switching vector $\overline{\mathrm{AT}}$ is applied to the dual-inverter system with VSI-1 (i.e., the switching inverter), by switching through the state 8-1-2-7. Thus the space vector combination deployed by the dual-inverter system to the OEWIM is $84' - 14' - 24' - 74'$ (see Fig. 7).

In the proposed SVPWM technique (NICSAZE), the time durations for these switching combinations are given by$(1-x)T_N,\ T_1,\ T_2,$ and xT_N, respectively. From [5], the ZSVs for these combinations are calculated as$-14V_{\mathrm{DC}}/18\sqrt{3}$, $-6V_{\mathrm{DC}}/18\sqrt{3}$, $2V_{\mathrm{DC}}/18\sqrt{3}$, and $10V_{\mathrm{DC}}/18\sqrt{3}$. It stands to reason that if one intends to suppress the ZSC, the ZSV must be suppressed (as the ZSV causes ZSC). Generally speaking, it is the best proposition to suppress the ZSV on an instantaneous basis. However, in the proposed topology, this will not be possible because all of the available 64 switching vector combinations possess a non-zero value of ZSV. Thus, the only alternative is to suppress the ZSV in the average sense over a period of the time (the smaller the time period the better). With the proposed NICSAZE PWM scheme, it is intended to suppress the ZSV to an average value of zero in every sampling time period.

The sampled average ZSV is forced to zero over the time period T_s, in the region centered on the SVL "*A*" and the corresponding offset time period T_{offset} can be calculated as follows.

Let the sampled average ZSV $(V_{\mathrm{zs,\ Samp\ avg.}})$ is zero, i.e.,

$$V_{\mathrm{zs,\ Samp\ avg.}} = 0. \tag{15}$$

The value of $V_{\text{zs, Samp avg.}}$ over a time T_s in terms of ZSVs and their respective dwell times is given in the following equation:

$$V_{\text{zs, Samp avg.}} = \frac{1}{T_S}\left[\left(-\frac{14V_{\text{DC}}}{18\sqrt{3}}\right)(1-x)\,T_N + \left(-\frac{6V_{\text{DC}}}{18\sqrt{3}}\right)T_2 + \left(\frac{2V_{\text{DC}}}{18\sqrt{3}}\right)T_1 + \left(\frac{10V_{\text{DC}}}{18\sqrt{3}}\right)(xT_N)\right] = 0. \tag{16}$$

After simplifying (16), one obtains: $2T_1 - 6T_2 - 14T_N + 24xT_N = 0$

$$\text{i.e., } xT_N = \frac{T_1}{12} - \frac{T_2}{4} - \frac{7T_N}{12}. \tag{17}$$

From (9), the offset time period corresponding to the SVLs "*A*," "*C*," and "*E*" is denoted as $T_{\text{offset}-A,C,E}$. Thus

$$T_{\text{offset}-A,C,E} = (1-x)\,T_N - T_{\min} = T_N - xT_N - T_{\min}. \tag{18}$$

By using (17) and (18), the simplified form of $T_{\text{offset}-A,C,E}$ is given as

$$T_{\text{offset}-A,C,E} = T_N - \left[\frac{T_1}{12} - \frac{T_2}{4} - \frac{7T_N}{12}\right] - T_{\min}$$

$$T_{\text{offset}-A,C,E} = \frac{T_1 - 3T_2 + 10T_N - 12T_{\min}}{12}. \tag{19}$$

From [22], the dwell time periods can be rewritten as

$$\left.\begin{aligned} T_1 &= T_{\max} - T_{\text{mid}} \\ T_2 &= T_{\text{mid}} - T_{\min} \\ T_{\text{eff}} &= T_{\max} - T_{\min} \\ T_N &= T_s - T_{\text{eff}} \text{ and} \\ T_{\max} + T_{\text{mid}} + T_{\min} &= 0 \end{aligned}\right\}. \tag{20}$$

By substituting (20) in (19), the modified equation for the $T_{\text{offset}-A,C,E}$ is given as

$$T_{\text{offset}-A,C,E} = \frac{(T_{\max} - T_{\text{mid}}) - 3\,(T_{\text{mid}} - T_{\min}) + 10T_N - 12T_{\min}}{12}$$

$$T_{\text{offset}-A,C,E} = \frac{5(T_{\max} - T_{\min} + T_N)}{12}. \tag{21}$$

Using (20) in (21) can be rewritten as

$$T_{\text{offset}-A,C,E} = \frac{5T_S}{12}. \tag{22}$$

Now, by using (13), (22) can be modified as

$$T_{\text{offset}} = \frac{5\sqrt{3}}{24\,(f_{\text{base}} \times m_a \times N_S)}. \tag{23}$$

Thus, by simply affecting the offset time period given by (23) in terms of modulation index and number of samples, one would succeed in forcing the average value of the ZSV over a sampling time period to zero in the region centered on SVL "*A*." It can be proved that for the alternating SVLs "*C*," "*F*" would also have the same T_{offset}.

Let it be considered that the sample to be synthesized is located in sector-27 with space vector switching locations *B*, *V*, and *X*, which is centered on SVL "*B*." The associated switching vector combinations (see Fig. 7) 85′, 15′, 25′, and 75′ are to be switched for the time periods $(1-x)T_N$, T_1, T_2, and xT_N, respectively, to implement the NICSAZE PWM technique, to suppress the ZSVs. Adopting the above procedure, the T_{offset} needed for the SVLs "*B*," "*D*," and "*F*" is given by

$$T_{\text{offset}-B,D,F} = \frac{7T_S}{12}. \tag{24}$$

Now, by using (13), (24) can be rewritten in terms of modulation index and number of samples as

$$T_{\text{offset}-B,D,F} = \frac{7\sqrt{3}}{24\,(f_{\text{base}} \times m_a \times N_S)}. \tag{25}$$

TABLE III
COMPUTER SIMULATION CONDITIONS

Dual-inverter DC-link voltage	300 V
Induction motor	Squirrel cage type, 3-Φ, 50 Hz, 400 V
Stator resistance	4.215 Ω
Rotor resistance (referred to stator)	4.185 Ω
Stator leakage inductance	17.52 mH
Rotor leakage inductance (referred to stator)	17.52 mH
Magnetizing inductance	516.6 mH
Moment of inertia	0.0131Kg m^2
Damping coefficient	0.002985 N/rad/s

TABLE IV
PARAMETERS OF THE OEWIMD

Motor parameters	Voltage (Line-Line)	415 V
	Rotor speed	1443 RPM
	Power	3.7 KW
	No. of poles	4

IV. SIMULATION AND EXPERIMENTAL RESULTS

To test and validate the proposed topology, initially the simulation results are carried out using MATLAB/*Simulink* software and the parameters used for modeling of the OEWIM are given in Table III. The experimental results are carried out on a 3-∅, 50-Hz OEWIM using open-loop v/f control. The name plate details of the motor are summarized in Table IV. The VSI-1 and VSI-2 (see Fig. 2) are operated with dc-link voltages of 200 and 100 V, respectively (in the ratio of 2:1). Therefore, the resultant dual-inverter configuration will have an equivalent dc-link voltage of 300 V (i.e., the magnitude of **OU** in Fig. 4).

A. Simulation Results

Simulation results are presented for the modulation indices of 0.7 (from (4), the fundamental frequency (f_1) is 40.41 Hz) and overmodulation ($f_1 = 50$ Hz) to cover the entire speed range of the drive. Overmodulation corresponds to the case, wherein the magnitude of the reference vector $|\boldsymbol{OT}| \geq |\boldsymbol{OU}|$ (see Fig. 4), where $|\boldsymbol{OU}|$ represents the effective dc-link voltage of the dual-inverter system.

Fig. 8 shows the simulated waveforms of the phase voltage, current, and their fast Fourier transform (FFT) analysis, for a modulation index of 0.7, with a center-spaced SVPWM. From the phase current and FFT analysis of both voltage and the current, it can be observed that the motor phase current shows the presence of ZSCs (as the motor phase voltage itself contains the zero-sequence component).

Figs. 9 and 10 show the motor phase voltage $(v_{a_1a_2})$, phase current (i_a), and the spectra corresponding to them, while oper-

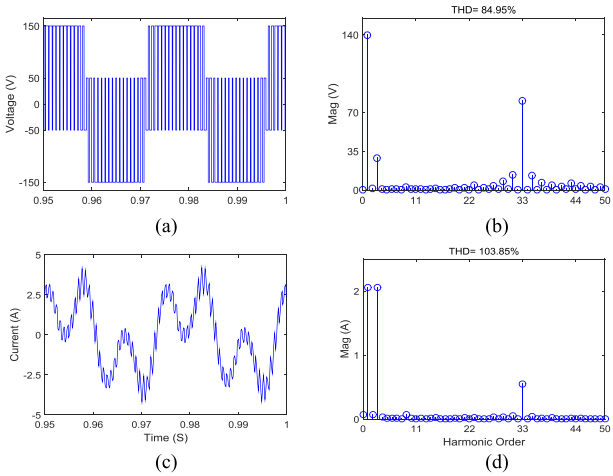


Fig. 8. Simulation results for center-spaced SVPWM technique at $m_a = 0.7$. (a) $v_{a_1a_2}$. (b) $v_{a_1a_2}$ FFT analysis. (c) i_a. (d) i_a FFT analysis.

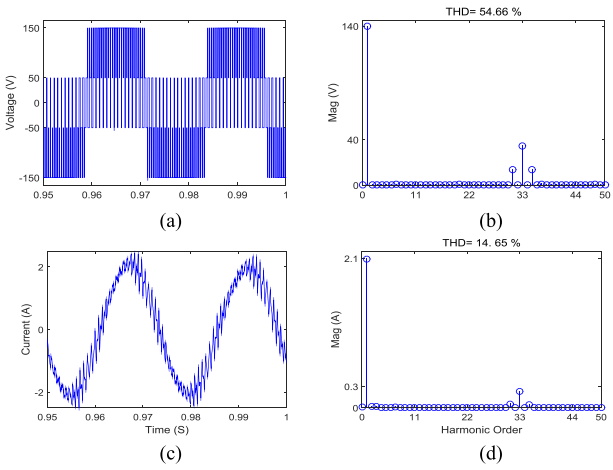


Fig. 9. Simulation results for DSAZE PWM technique at $m_a = 0.7$. (a) $v_{a_1a_2}$. (b) $v_{a_1a_2}$ FFT analysis. (c) i_a. (d) i_a FFT analysis.

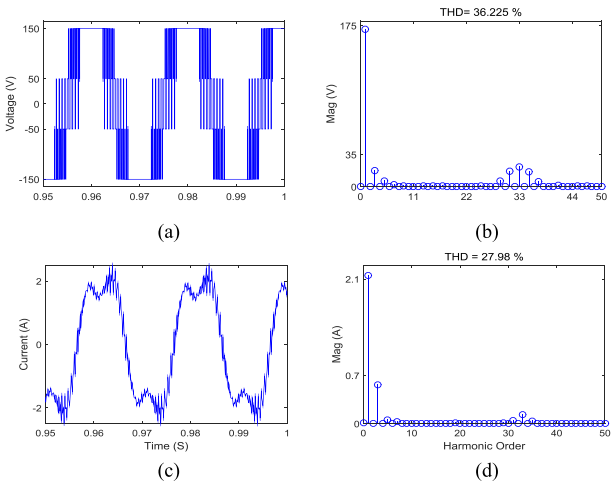


Fig. 10. Simulation results for DSAZE PWM technique at $m_a = 1$. (a) $v_{a_1a_2}$. (b) $v_{a_1a_2}$ FFT analysis. (c) i_a. (d) i_a FFT analysis.

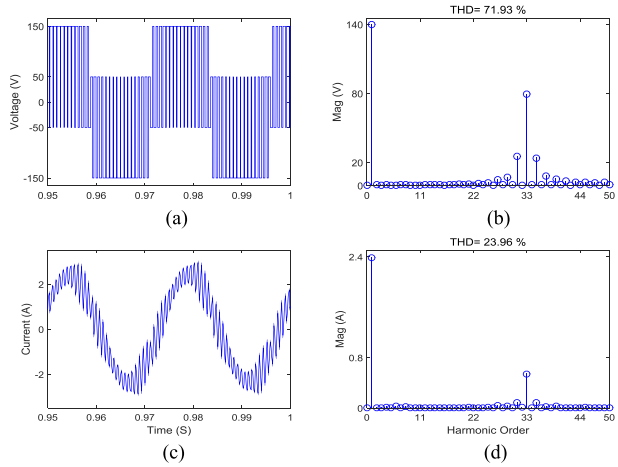


Fig. 11. Simulation results for NICSAZE PWM technique at $m_a = 0.7$. (a) $v_{a_1a_2}$. (b) $v_{a_1a_2}$ FFT analysis. (c) i_a. (d) i_a FFT analysis.

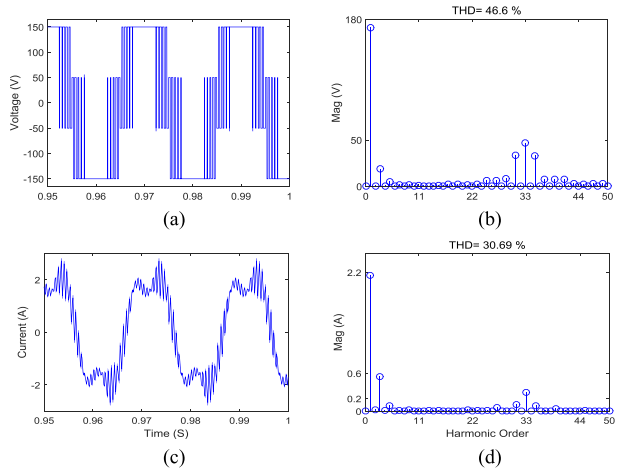


Fig. 12. Simulation results for NICSAZE PWM technique at $m_a = 1$. (a) $v_{a_1a_2}$. (b) $v_{a_1a_2}$ FFT analysis. (c) i_a. (d) i_a FFT analysis.

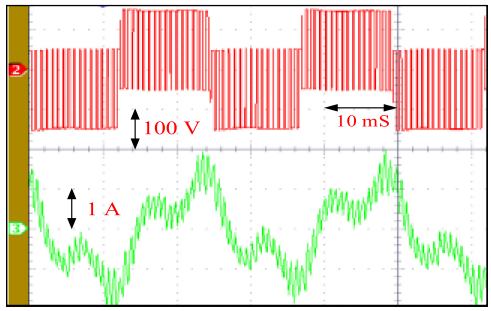


Fig. 13. Experimental results for center-spaced SVPWM technique at $m_a = 0.7$: $v_{a_1a_2}$ (top) and i_a (bottom).

ating drive system using the DSAZE PWM technique. Figs. 11 and 12 show similar results with the proposed NICSAZE PWM technique. The simulation results reveal that the currents are sinusoidal despite the presence of some of the harmonic components of the triplen family (i.e., the zero-sequence component).

From the FFT analysis, it can be concluded that there is the presence of odd harmonics with their multiples in the motor phase voltage, but they are not reflected on the motor current

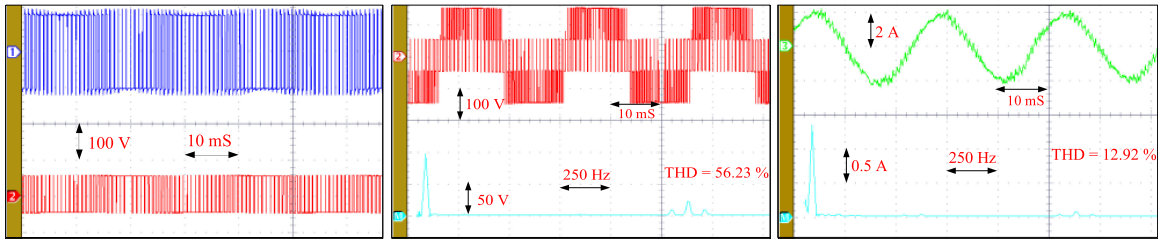


Fig. 14. Experimental results for DSAZE PWM technique at $m_{\mathrm{a}} = 0.7$. (a) Pole voltage of VSI-1 (top) and -2 (bottom). (b) $v_{a_1 a_2}$ and its harmonic spectrum. (c) i_a and its harmonic spectrum.

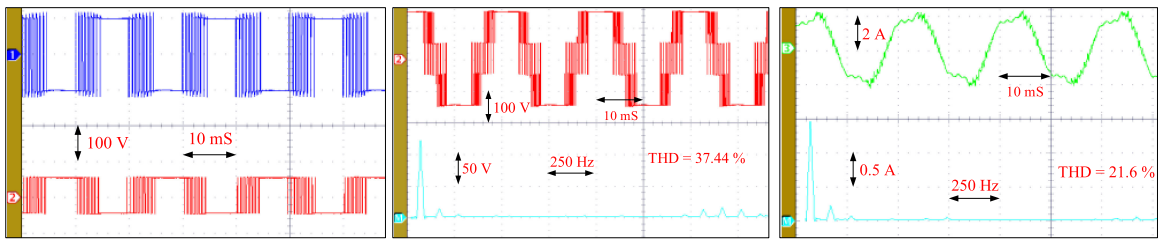


Fig. 15. Experimental results for DSAZE PWM technique at $m_{\mathrm{a}} = 1$. (a) Pole voltage of VSI-1 (top) and -2 (bottom). (b) $v_{a_1 a_2}$ and its harmonic spectrum. (c) i_a and its harmonic spectrum.

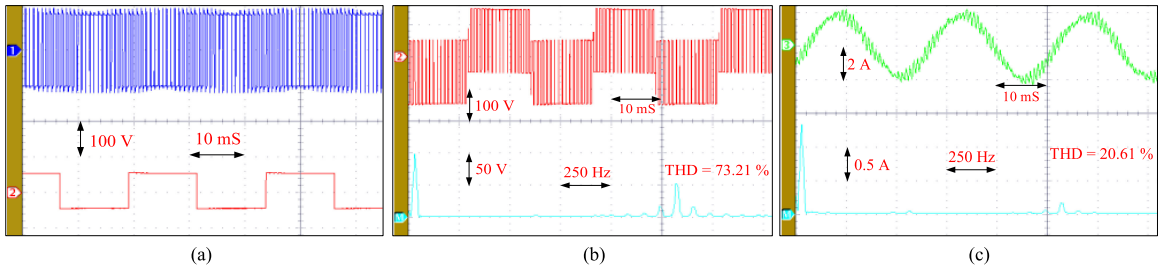


Fig. 16. Experimental results for NICSAZE PWM technique at $m_{\mathrm{a}} = 0.7$. (a) Pole voltage of VSI-1 (top) and -2 (bottom). (b) $v_{a_1 a_2}$ and its harmonic spectrum. (c) i_a and its harmonic spectrum.

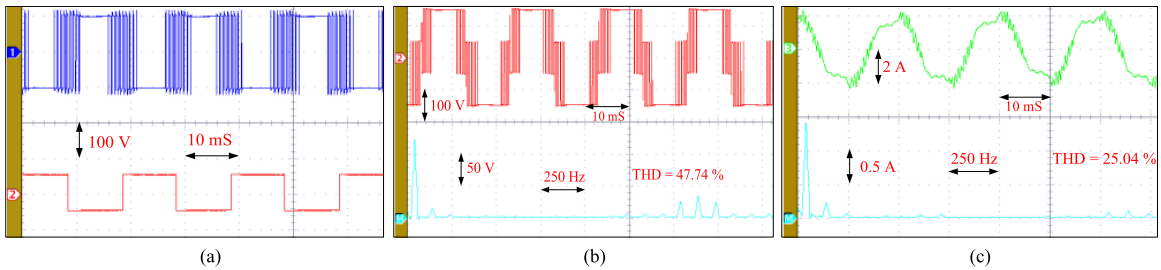


Fig. 17. Experimental results for NICSAZE PWM technique at $m_{\mathrm{a}} = 1$. (a) Pole voltage of VSI-1 (top) and -2 (bottom). (b) $v_{a_1 a_2}$ and its harmonic spectrum. (c) i_a and its harmonic spectrum.

because of forcing the common mode voltages to zero on the sampled average.

It may be noted that the motor phase voltages do not contain lower order harmonics of triplen order (3rd, 9th, etc.), which proves the effectiveness of the proposed NICSAZE PWM scheme.

B. Experimental Results

To validate the proposed power circuit configuration and the NICSAZE PWM scheme, a dual-inverter system is fabricated with dc-link voltages of 200 and 100 V, respectively, for VSI-1 and VSI-2. To achieve waveform symmetries, 66 samples are used in any given cycle [5], irrespective of the modulation index. This means that at a modulation index of unity, the sampling frequency would be equal to 3.3 KHz and the switching frequency is half of the sampling frequency [23]. The hardware control platform *dSPACE-1104* is used to generate the gating pulses for the dual-inverter configuration.

Fig. 13 shows the experimentally obtained waveforms for the motor phase voltage and current with the conventional (i.e., the center-spaced) SVPWM technique. It may be noted that

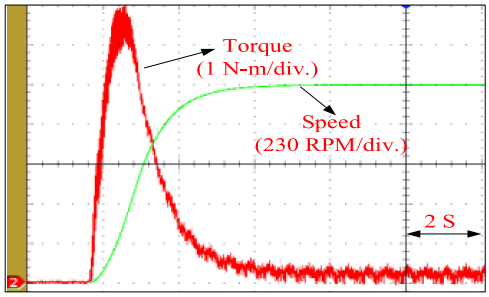


Fig. 18. Experimental torque and speed waveforms of OEWIMD with NICSAZE PWM technique at $m_a = 0.7$.

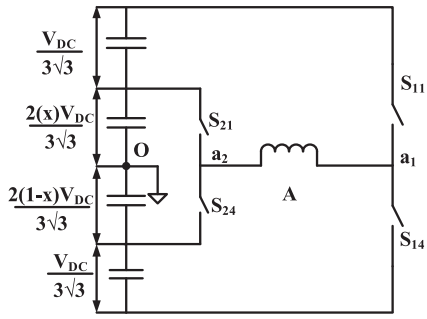


Fig. 19. Distribution of dc-link voltages for the proposed topology with unbalance.

the experimental results are in agreement with the simulation results. It is evident that the motor phase current has a significant zero-sequence component in it.

Experimentation is carried out for both of the PWM techniques to validate the simulations results presented in Figs. 14–17. Figs. 14 and 15 show the pole voltages of VSI−1 and −2, motor phase voltage, and current waveforms with the FFT analysis when the DSAZE PWM technique is applied to the system. Figs. 16 and 17 show similar results, when the proposed 4-L OEWIMD is operated using the proposed NICSAZE PWM scheme.

The agreement of simulation and experimental results validate the applicability of the proposed NICSAZE PWM scheme for the proposed circuit configuration for the 4-L OEWIMD.

From the pole voltages presented in Figs. 14(a) and 16(a), it can be easily observed that both inverters are switched in the case of the DSAZE PWM technique. It may also be observed that VSI-2 is clamped, whereas VSI-I is switched in the case of the proposed NICSAZE PWM scheme.

It may also be readily observed that the motor phase voltage waveforms show the 4-Ls with both of the PWM schemes. However, based on the harmonic spectrum of the current waveforms, it can be observed that the current ripple is less with the DSAZE PWM compared to the NICSAZE PWM scheme.

This is not surprising considering the fact that higher switching would decrease the ripple in the current. However, the switching loss in the inverter is increased with the DSAZE PWM scheme. In contrast, the NICSAZE PWM results in a lower switching loss. Thus, it is evident that the proposed NICSAZE PWM scheme is an engineering compromise between the elimination of the ZSC and the minimization of switching power loss in the dual-inverter system. It would be interesting to compare the switching and conduction losses occurring in the dual-inverter system with these two PWM schemes.

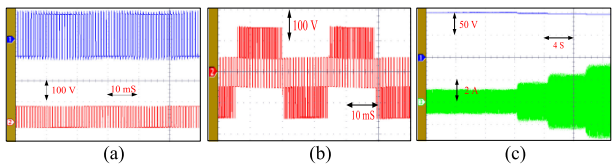
The experimental torque and speed waveforms of the OEWIMD with the proposed topology are shown in Fig. 18 for the NICSAZE PWM technique.

C. Fault-Tolerant Capability of the Proposed Power Circuit Configuration

A certain type of fault tolerance is observed with this circuit configuration. The proposed circuit shows fault tolerance toward the imbalance of the dc-link capacitor of the nested rectifier. Fig. 19 shows the distribution of the dc-link capacitors of the nested rectifier. The sum of these two dc-link capacitors must remain the same, even though the voltages of individual dc-link capacitors are different. Let it be assumed that the variable

TABLE V
UNBALANCED VOLTAGE LEVELS ACROSS PHASE-A WINDING OF OEWIMD

Pole Voltage	Voltage Level	Switch turned on	Switch turned off
V_{a_2o}	$\frac{2x}{3\sqrt{3}}V_{DC}$	S_{21}	S_{24}
	$\frac{-2(1-x)}{3\sqrt{3}}V_{DC}$	S_{24}	S_{21}
V_{a_1o}	$\frac{2}{\sqrt{3}}\left\{\frac{xV_{DC}}{3}+\frac{V_{DC}}{6}\right\}$	S_{11}	S_{14}
	$\frac{-2}{\sqrt{3}}\left\{\frac{(1-x)V_{DC}}{3}+\frac{V_{DC}}{6}\right\}$	S_{14}	S_{11}



(a) (b) (c)

Fig. 20. (a) Unbalanced pole voltages of VSI-1 (top), VSI-2 (bottom). (b) Balanced phase voltage. (c) OEWIMD phase current in loaded conditions at $m_a = 0.6$ with lower dc-link voltage.

"x" denotes the degree of such an imbalance. The voltage levels impressed on the terminals a_1 and a_2 are summarized in Table V.

It can easily be verified that the difference between these two pole voltages (which is equal to the motor phase voltage) would be the same for any value of "x". It may be noted that $x = 1/2$ corresponds to the case of balanced operation of the dc-link capacitors of the nested rectifier.

To practically demonstrate this assertion, an imbalance is deliberately introduced on the dc-link capacitors of the nested rectifier by removing an equalizing resistor connected across the capacitor. Fig. 20(a) shows the pole voltages of individual inverters, which clearly shows the imbalance. However, the motor phase voltage [see Fig. 20(b)] (i.e., the difference between the pole voltages) remains balanced, despite the imbalance of the individual pole voltages. The dual-inverter system is loaded to explain its ruggedness under this condition. Fig. 20(c) shows the motor phase current and the total dc-link voltage under loaded conditions, corresponding to the case of $x = 0.35$. It may be noted that the sum of the voltages of the individual dc links remains unaltered even when the dual-inverter system is loaded with such an unbalanced condition. Thus, the fault-tolerant capability of the dual-inverter system is demonstrated.

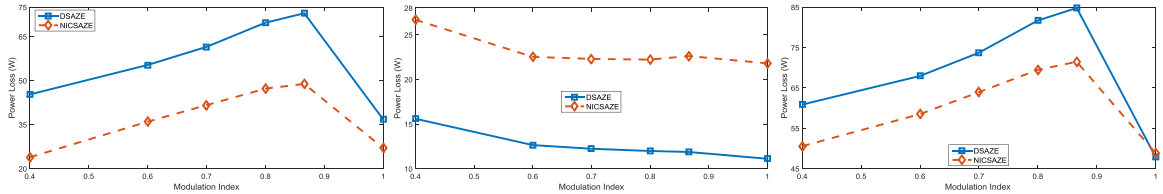


Fig. 21. Simulation results. (a) P_{SW} versus m_{a}, (b) P_{Con} versus m_{a}, and (c) P_{DI} versus m_{a}.

D. Performance Characteristics of the Proposed Topology

The performance characteristics of the proposed topology mainly depend on the PWM strategy. In this section, the performance of the PWM techniques (namely, DSAZE and NICSAZE) are critically compared in terms of the switching power loss, conduction power loss, total power loss in the dual-inverter system.

In order to make a fair comparison, an equal number of samples are used for both PWM schemes, and the same effective dc-link voltage is chosen: the number of samples employed is 66, as an odd number of samples/sector would ensure all types of symmetries [5]. A dc-link voltage of 564 V ensures that the rated voltage (230 V) is applied to the motor phases at the limit of linear modulation $(\sqrt{3}/2)$. A load of 20 N·m (approx. 80% of the full load, see Tables III and IV for the motor parameters) is applied to the motor to compute the power loss incurred in the dual-inverter system.

All of the aforementioned performance indices are computed by employing an *improvised loss model*, which was proposed in [15] for the loss calculation of the 4-L OEWIMD. The same model was extended to this paper to compute the losses occurred in the 4-L OEWIMD.

The total power loss in the dual-inverter system comprises switching loss (P_{SW}) in power semiconductor devices and the conduction loss (P_{Con}) in them.

The switching power loss (P_{SW}) is the sum of the $P_{\mathrm{SW,ON}}$ and $P_{\mathrm{SW,OFF}}$, where $P_{\mathrm{SW,ON}}$ is the switching loss during the turn-ON transition of the switch, and $P_{\mathrm{SW,OFF}}$ is the switching loss during the turn-OFF transition of the switching device. P_{SW} and P_{Con} are measured by extracting the simulation data of the voltage across the switch (v_{SW}) and the current through the switch (i_{SW}). To get a reasonable accuracy in the loss calculation, the simulation step is selected as 1 μS. The expressions for the P_{SW} and P_{Con} are given as [24]

$$P_{\mathrm{SW}} = \left[\frac{1}{2} v_{\mathrm{SW}} i_{\mathrm{SW}} \left(t_{\mathrm{SWON}} + t_{\mathrm{SWOFF}}\right)\right] \times f_S$$

$$P_{\mathrm{SW}} = \left[\frac{1}{2} v_{\mathrm{SW}} i_{\mathrm{SW}} \left(t_{ri} + t_{fv}\right) + \frac{1}{2} v_{\mathrm{SW}} i_{\mathrm{SW}} \left(t_{rv} + t_{fi}\right)\right] \times f_s \tag{26}$$

$$P_{\mathrm{Con}} = \frac{v_{\mathrm{ON}}\ i_{\mathrm{ON}} t_{\mathrm{ON}}}{T_S} \tag{27}$$

where $v_{\mathrm{ON}} = V_t + i_{\mathrm{ON}} R_{\mathrm{CE}}$ for IGBT

$v_{\mathrm{ON}} = V_f + i_{\mathrm{ON}} R_{\mathrm{AK}}$ for the anti – parallel diode

where V_t is the IGBT fixed voltage drop under the zero-current condition, R_{CE} is the IGBT on-drop resistance, V_f is the diode fixed voltage drop under the zero-current condition, and R_{AK} is the diode on-drop resistance. The parameters of the IGBT module-*SKM150GB12T4* are considered for the evaluation of the conduction loss. The following data is assumed to compute the switching and conduction loss in each device: $t_{fv} = 1\ \mu\mathrm{s},\ t_{rv} = 2\ \mu\mathrm{s},\ t_{fi} = 4\ \mu\mathrm{s},$ and $t_{ri} = 2\ \mu\mathrm{s}$.

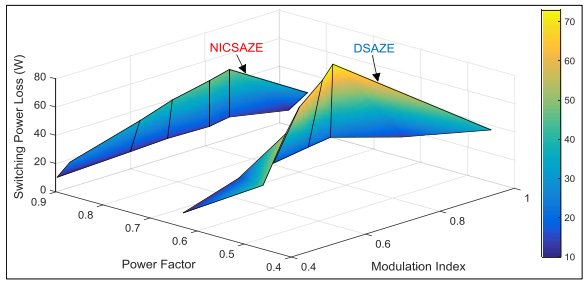


Fig. 22. Dependence of power factor of the open-end winding induction motor on the switching power loss (P_{sw}) and the modulation index (m_{a}).

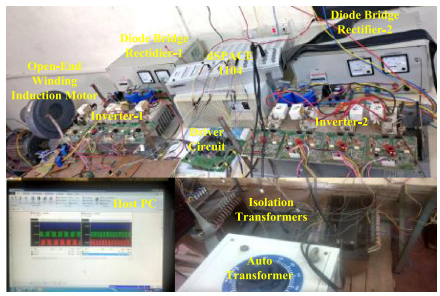


Fig. 23. Experimental setup for the proposed OEWIMD.

The plots of P_{SW}, P_{Con}, and overall loss for the dual-inverter system (P_{DI}) for the entire modulation range are shown in Fig. 21(a)–(c), respectively. As explained earlier, the switching loss is more with DSAZE because of the switching of both of the inverters.

As one might expect, the conduction loss is more for the NICSAZE PWM technique because of the clamping of VSI-2 compared to the DSAZE PWM scheme. The overall loss for the dual-inverter system (P_{DI}) is less with the NICSAZE PWM as compared to the DSAZE, as the loss in the dual-inverter system is dominated by P_{SW}.

The operating power factor of the open-end winding induction motor is presented in Fig. 22. As the quantities involved in (26) are instantaneous in nature, it could be a difficult proposition to derive a closed-form expression for the switching losses involving the load power factor. Therefore, the impact of the load power factor on the switching loss is graphically presented in Fig. 22. The switching power loss is computed for two values of load torque (20 and 5 N·m) on the motor at various modulation indices as the no-load speed depends on the modulation index. The power factor is assessed by taking the product of the displacement factor and the harmonic factor. These quantities are

obtained by subjecting the motor phase voltage and motor phase current to the FFT analysis. Fig. 23 shows the experimental setup used in this paper.

V. Conclusion

This paper suggests a new circuit topology for the 4-L OEWIMD, which is operated with unequal dc-link voltages, which are in the ratio of 2:1. The proposed circuit configuration avoids the overcharging of the lower dc-link voltage capacitor by its counterpart, when compared to the conventional topology and requires only two isolated dc-power supplies compared to the nested rectifier–inverter configuration proposed earlier. The proposed circuit configuration exhibits immunity to the internal imbalance of the dc-link voltages of the nested rectifier.

A new PWM strategy called the NICSAZE is also proposed to arrest the flow of ZSC in the circuit. Simulation studies indicate that the overall power loss incurred in the dual-inverter system is lower compared to the DSAZE PWM scheme proposed earlier. However, the THD with the NICSAZE PWM scheme is marginally higher compared to the DSAZE PWM scheme and results in a slightly higher ohmic power loss in the motor.

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