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RESEARCH ARTICLE

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A new hybrid flying capacitor–based single-phase nine-level inverter

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Abstract

Multilevel inverters (MLIs) with reduced part count are becoming popular in the arena of medium voltage and medium power applications. This proposed topology owns the advantages of reduced number and voltage stress across the switching devices and higher efficiency. It also combines the method of utilizing full DC-link voltage to improve the RMS output voltage. The proposed hybrid topology is constructed using three different sections consisting of a cascaded two two-level inverter, H-bridge with a flying capacitor, and single-leg low-frequency circuit. The complete modes of operation to generate 9-level A. C voltage at the inverter output including the FC voltage balancing has been comprehensively presented. A comparison is constructed with the proposed and recent topologies in the literature to show the merits of the proposed configuration. The proposed topology is tested in MATLAB/SIMULINK environment and a scale-down prototype has been developed in the laboratory. The feasibility of the proposed topology is verified through simulation and experimental results.

KEYWORDS

efficiency, multilevel inverter, pulse width modulation, total harmonic distortion

1 | INTRODUCTION

Energy generation through alternate sources is gaining attention because of the depletion of natural resources and environmental concerns. In this regard, MLI is the one which can circumvent these problems and offers additional benefits of high-power quality, reduced voltage stress, and lower losses.[1-3] The traditional multilevel topologies are categorized into (a) diode clamped, (b) flying capacitor, and (c) cascaded H-bridge (CHB) inverters.[4-6] These basic topologies are practicable in many industrial applications. However, the application of these standard topologies to withstand high DC-link voltages and to generate more levels in the output requires a higher device count. Therefore, to overcome this issue, several hybrid structures have been developed.

A generalized MLI is proposed in Satputaley and Borghate, Dewangan et al, and Noroozi et al,[7-9] with a smaller number of switches and of lower voltage ratings to generate a higher number of voltage levels. Some of the MLIs based on T-type and submodule structures reported for single-phase and three-phase applications in Hota et al and Lee et al,[10,11] with reduced semiconductor devices compared with CHB-MLI. However, all these structures need more independent

LIST OF ABBREVIATIONS AND SYMBOLS: FC Flying capacitor; ANPC Active neutral point clamped; ma Modulation index; VAN Load voltage; Vdc DC source voltage; iA Load current; Rq On state resistance of the mosfet; Rd On state resistance of the body diode; Kq,Krr, aq, bq, arr and brr constants calculated from the device data-sheets; Vf On state forward voltage drop of the body diode

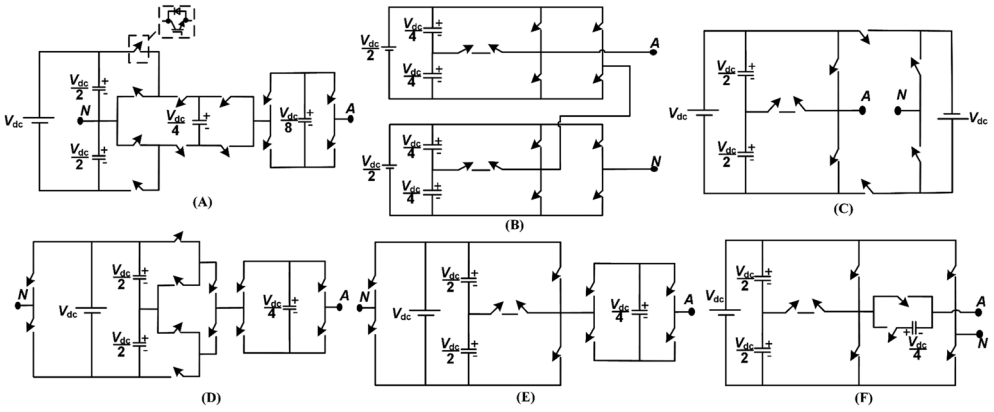

FIGURE 1 Existing nine-level hybrid inverters: A, Li et al[12]; B, Odeh and Nnadi[13]; C, Gautam et al[14]; D, Sandeep and Udaykumar[15]; E, Sandeep and Udaykumar[16]; and F, Sandeep and Udaykumar[17]

DC sources, which limits their application where it is required to deploy a single DC voltage source. Figure 1 depicts some of the recently proposed nine-level (9-L) inverters. A hybrid 9-L inverter is proposed in Odeh and Nnadi,[13] which uses modified T-type H-bridge structure with full utilization of DC-link voltages. However, it requires two independent DC links along with the requirement of high voltage rated switches in H-bridge. With the aim of the reduced number of switching devices to generate higher levels in the output, a topology is introduced in Gautam et al,[14] which uses a smaller number of switches to generate 9-L output. This configuration is also having the same limitation of the requirement of two DC sources. This topology has been modified in Gautam et al,[18] with the addition of self-voltage balancing of the capacitors. However, the requirement of two independent DC sources is inevitable.

Recently, the FC-based hybrid MLIs have become more prevalent[19-21] because of their reduced device count. The topology proposed in Yu et al[19] uses the cascade connection of a T-type, three-level inverter and an H-bridge cell with an FC to produce the seven-level output. However, the T-type circuit needs two switches of $4V_{dc}$ rating. The requirement of high blocking voltage switches is reduced to half in Abhilash et al,[20] which can generate seven-level output with the same number of device count as like in Yu et al.[19] Because of the requirement of only one $4V_{dc}$-rated switch in each phase, topology[20] possess higher efficiency than Yu et al.[19] The common problem in both the topologies in Yu et al and Abhilash et al[19,20] is the incomplete utilization of the DC-link voltage. The topology proposed in Dao and Lee[21] can make use of full DC-link voltage with the use of an FC section. However, the output voltage levels in each phase are limited to only five, which results in a poor output voltage quality. The harmonic spectrum of the output voltage can be improved by increasing the output levels. The higher number of output voltage levels is possible by cascading a greater number of FC sections.

The topology proposed in Li et al[12] uses two cascade sections of FC H-bridges, which increases the number of levels in the output and improves the harmonic spectrum. However, it requires more component count and more conducting devices at any voltage level and fails to utilize the full DC-link voltage. An improvised 9-L inverter structure is proposed in Wang et al[22] to make use of the full DC-link voltage and to increase the redundant switching states for the FC voltage balancing. An innovative 9-L dual boost inverter is proposed in Saeedian et al[23] using switched capacitors and a single DC voltage source, which avoids the need of H-bridge for polarity generation. A modified packed U-cell (PUC) is proposed in Vahedi et al[24] with a single FC to produce the 9-L output. However, these topologies suffer from the requirements of high voltage–rated semiconductor devices, bulky capacitors, and lack of redundant switching states to balance the FC voltages, respectively.

The topologies proposed in previous studies[15-17,25] address the above-said issue by using two low-frequency switches (LFS) across the DC-link, because of which full DC-link voltage is being utilized and the number of levels also increased to nine. The double flying capacitor configuration (DFCM)[25] generates nine-level output using two LFS by eliminating the mid-point of the DC-link. The requirement of a greater number of FCs, voltage balancing issues, and a greater number of conducting devices at any voltage level; increases the complexity with a reduction in efficiency. Sandeep and Udaykumar[15] uses an ANPC converter to equalize the losses in the switching devices, which results in more device count. Whereas in another study, Sandeep and Udaykumar[16] uses a T-type converter, which results in switching devices of higher voltage rating. Therefore, both these topologies result in higher losses. In order to improve the efficiency of the overall system, a slight modification has been made in the proposed topology, which is the usage of the cascaded two two-level inverter (CT^2-LI) structure instead of ANPC or T-type. The CT^2-LI has the advantages of a reduced number of switching devices of comparatively lower voltage rating, which results in improved efficiency of the overall system. The complete operating modes and corresponding level generation are presented. The comparison is made to show

the merits of the proposed topology. Finally, the performance of the proposed 9-L hybrid inverter is evaluated through simulation and experimental results.

2 | PROPOSED NINE-LEVEL HYBRID INVERTER

2.1 | Proposed topology

Figure 2 depicts the proposed single-phase 9-L hybrid multilevel inverter which consists of 10 switching devices S_1, S_2, ... S_{10}, and D_1, D_2, ... D_{10} are the body diodes of the switching devices, respectively. The topology is capable of generating nine-level output voltage waveform with reduced switching devices. This configuration is built by the cascade connection of three different sections. Section-1 consists of two LF switches. Section-2 is a very popular topology in recent times called CT^2-LI. Section-3 consists of a regular H-bridge with an FC (C_a). A single DC source along with two DC-link capacitors (C_{d1} and C_{d2}) are connected between section-1 and section-2. A single-phase, *R-L load* is connected at the output terminals *A* and *N*. The FC in section-3 is source free, the voltage across the FC is maintained constant by exploiting the available redundant switching states. The proposed topology, with the appropriate operation of the switching devices, generates a nine-level voltage at the output in the range of $-V_{dc}$ to $+V_{dc}$, with a step size of $V_{dc}/4$.

For a better understanding of the principle and working, the operation of the proposed topology has been described in different operating modes as depicted in Figure 3. The voltage stress across the switches S_4, S_9, and

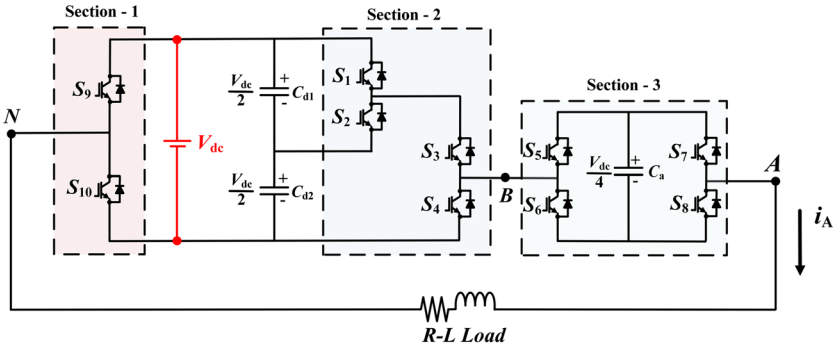

FIGURE 2 Proposed nine-level hybrid-inverter

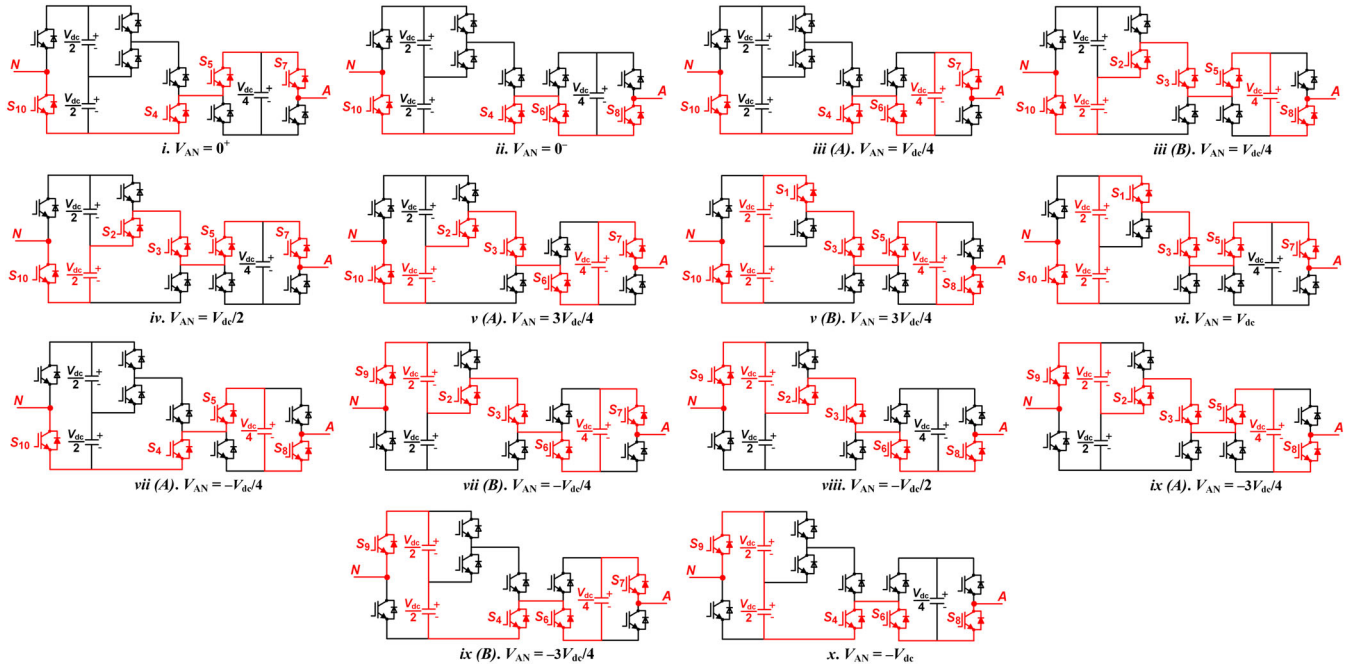

FIGURE 3 Different modes of nine-level operation

S_{10} is V_{dc} and it is $V_{dc}/2$ across the switches S_1, S_2, and S_3. The H-bridge switches (S_5, S_6, S_7, and S_8) in section-3 are having voltage stress that is equal to the magnitude of the FC voltage, ie, $V_{dc}/4$. The decrease in modulation index (m_a) will vary the output voltage from nine-level to seven-level and further to three-level. The detailed description of the conduction of switching devices to generate various voltage levels at the output (V_{AN}) is as follows.

2.2 | Operating modes

In this section, the detailed operation of the proposed topology is explained through the following modes for various output voltage level generations in steady state. Here, the DC-link capacitors share the DC source voltage (V_{dc}), of equal magnitudes, ie, $V_{Cd1} = V_{Cd2} = V_{dc}/2$. In the same way, the FC is charged to a voltage of $V_{Ca} = V_{dc}/4$ through the redundant charging states. Figure 3 presents these modes along with the details concerning the conducting devices and the direction of the load current (i_A).

Mode-0 [$V_{AN} = 0$]. In this mode, during positive zero crossing, the switches S_7, S_5, S_4, and S_{10} are triggered. Switches S_8, S_6, S_4, and S_{10} are triggered during the negative zero crossing, which makes the system thermally stable. The S_4 and S_{10} are commonly triggered either during positive zero crossing or during the negative zero crossing. The conduction of the switch or anti-parallel diode is decided by the direction of i_A.

Mode-1 [$V_{AN} = V_{dc}/4$]:

Case i: if S_7, S_6, S_4, and S_{10} are gated, $V_{AN} = V_{Ca} = V_{dc}/4$ as shown in Figure 3 (*iii*A & *iii*B). When i_A is +ve, FC discharges; the conducting devices are S_{10}, D_4, S_6, and S_7. When i_A is −ve, FC charges through the conducting devices D_{10}, S_4, D_6, and D_7.

Case ii: if S_8, S_5, S_3, S_2, and S_{10} are gated, $V_{AN} = -V_{Ca} + V_{Cd2}$, then $V_{AN} = -V_{dc}/4 + V_{dc}/2 = V_{dc}/4$. When i_A is +ve, FC charges; the conducting devices are S_{10}, D_2, S_3, D_5, and D_8. When i_A is −ve, FC discharges through the conducting devices D_{10}, S_2, D_3, S_5, and S_8. Hence, both the switching states in *case i* and *case ii* are utilized effectively, to maintain the FC voltage constant.

Mode-2 [$V_{AN} = V_{dc}/2$]. The switches S_{10}, S_2, S_3, S_5, and S_7 are triggered, because of which, the load is directly clamped across the DC-link capacitor C_{d2}. This makes $V_{AN} = V_{Cd2} = V_{dc}/2$. It may be noted that the devices S_{10}, D_2, S_3, D_5, and S_7 conduct when i_A is +ve. Similarly, the devices D_{10}, S_2, D_3, S_5, and D_7 conduct when i_A is −ve.

Mode-3 [$V_{AN} = 3V_{dc}/4$].

Case i: if S_7, S_6, S_3, S_2, and S_{10} are gated, $V_{AN} = V_{Cd2} + V_{Ca}$. Assuming that the FC is initially charged to $V_{dc}/4$, then $V_{AN} = 3V_{dc}/4$ as shown in Figure 3 (*v*A & *v*B). When i_A is +ve, FC discharges; the conducting devices are S_{10}, D_2, S_3, S_6, and S_7. When i_A is −ve, C_a charges through the conducting devices D_{10}, S_2, D_3, D_6, and D_7.

Case ii: if S_8, S_5, S_3, S_1, and S_{10} are gated, $V_{AN} = -V_{Ca} + V_{Cd1} + V_{Cd2}$, which gives $V_{AN} = -V_{dc}/4 + V_{dc} = 3V_{dc}/4$. When i_A is +ve, FC charges; the conducting devices are S_{10}, S_1, S_3, D_5, and D_8. When i_A is −ve, FC discharges through the conducting devices D_{10}, D_1, D_3, S_5, and S_8. Hence, both the switching states in *case i* and *case ii* are utilized effectively, to maintain the FC voltage constant.

Mode-4 [$V_{AN} = V_{dc}$]. The switches S_{10}, S_1, S_3, S_5, and S_7 are triggered, because of which, the load is directly clamped to the DC-link capacitors C_{d1} and C_{d2}. This makes $V_{AN} = V_{Cd1} + V_{Cd2} = V_{dc}$. It may be noted that the devices S_{10}, S_1, S_3, D_5, and S_7 conduct when i_A is +ve. Similarly, the devices D_{10}, D_1, D_3, S_5, and D_7 conduct when i_A is −ve.

The voltage levels during the negative half cycle of the fundamental wave will be obtained in a similar fashion as that of mode-0 to mode-4 with different switching combinations listed in Table 1, the redundancies exist in $-V_{dc}/4$ and $-3V_{dc}/4$ levels, which can maintain the FC voltage constant.

For further understanding, the switching sequences for the generation of all the nine-levels are given in Table 1. The digits "1" and "0" represent the switching states of ON and OFF, respectively. The voltage measured between the terminals *A* and *N* is the load voltage (V_{AN}). From Table 1, it may be observed that a maximum of five devices out of 10 conduct in any given mode. One may, therefore, expect a higher efficiency with the proposed topology on account of lower conduction and switching losses in the switching devices.

TABLE 1 Effect of switching states of the proposed 9-L inverter on FC

V_{AN}	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	i_A	FC	No. of Cond Devices/Ph	Switching State
V_{dc}	1	0	1	0	1	0	1	0	0	1	X	N.E.	5	V_1
$\frac{3V_{dc}}{4}$	0	1	1	0	0	1	1	0	0	1	>0 <0	D C	5	V_2
	1	0	1	0	1	0	0	1	0	1	>0 <0	C D	5	V_3
$\frac{V_{dc}}{2}$	0	1	1	0	1	0	1	0	0	1	X	N.E.	5	V_4
$\frac{V_{dc}}{4}$	0	0	0	1	0	1	1	0	0	1	>0 <0	D C	4	V_5
	0	1	1	0	1	0	0	1	0	1	>0 <0	C D	5	V_6
0^+	0	0	0	1	1	0	1	0	0	1	X	N.E.	4	V_7
0^-	0	0	0	1	0	1	0	1	0	1	X	N.E.	4	V_8
$\frac{-V_{dc}}{4}$	0	0	0	1	1	0	0	1	0	1	>0 <0	C D	4	V_9
	0	1	1	0	0	1	1	0	1	0	>0 <0	D C	5	V_{10}
$\frac{-V_{dc}}{2}$	0	1	1	0	0	1	0	1	1	0	X	N.E.	5	V_{11}
$\frac{-3V_{dc}}{4}$	0	1	1	0	1	0	0	1	1	0	>0 <0	C D	5	V_{12}
	0	0	0	1	0	1	1	0	1	0	>0 <0	D C	4	V_{13}
$-V_{dc}$	0	0	0	1	0	1	0	1	1	0	X	N.E.	4	V_{14}

Abbreviations: C, charging; D, discharging, N.E., no effect; X, do not care condition.

3 | MODULATION SCHEME AND CAPACITOR VOLTAGE BALANCING

3.1 | Modulation technique

The proposed topology is modulated using sine-triangle comparison technique. The modulation index (m_a) can be defined as:

$$m_a = \frac{A_r}{(n-1) \times A_c}, \tag{1}$$

where A_r is the amplitude of the reference signal, A_c is the amplitude of the carrier signal, and n is the number of levels in the output.

The total number of carrier waves of equal amplitude required in implementing the sine-triangle pulse-width modulation (PWM) is $n - 1$. Since the proposed topology is a 9-L system, it needs eight carrier signals to be compared with a reference wave as shown in Figure 4. All the carrier waves are placed in-phase across the sine-wave, hence this method is an in-phase disposition sinusoidal PWM (IPD-SPWM). Figure 4 illustrates the schematic diagram of the IPD-SPWM. The gate pulses are generated by comparing a fundamental sine-wave and eight IPD carrier waves, and the corresponding output pulses for each voltage level for one complete cycle is given in Figure 4. With the help of an FPGA, the required pulse pattern to each switch is generated using logical blocks to produce the 9-L output.

3.2 | Flying capacitor voltage balancing

The proposed topology allows the balancing of FC voltage at its desired magnitude because of the presence of redundant switching states. Both charging and discharging paths exists during each level of voltage in which FC involved is given

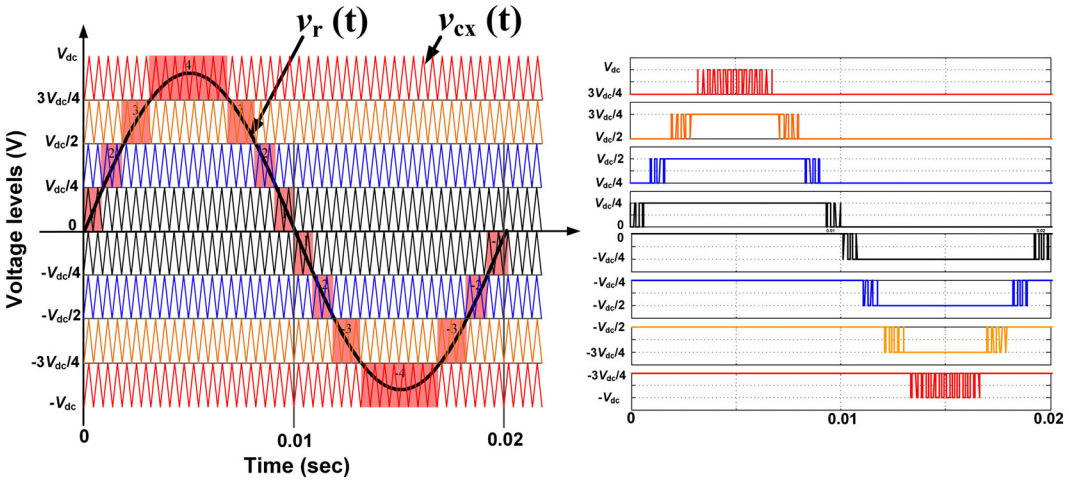

FIGURE 4 In-phase disposition sinusoidal pulse-width modulation (IPD-SPWM) scheme for nine-level (9-L) output

in Zhang et al and Narimani et al.[26,27] The effect on the FC during each switching state is listed in Table 1. Desired switching state, which controls the FC voltage, is selected during the voltage levels of $\pm\frac{V_{dc}}{4}$ and$\pm\frac{3V_{dc}}{4}$, by sensing the magnitude of the FC voltage and the direction of i_A.

Figure 5 depicts the flowchart and the selection of switching states for the FC voltage balancing. During the output-voltage levels of 0, $\pm V_{dc}/2$ and $\pm V_{dc}$, FC is not involved in the conduction path, therefore, V_{Ca} is unaltered. Switching states during these levels are selected without sensing the V_{Ca} and i_A. Two switching states (V_5 and V_6) exists during the output-voltage level of $V_{dc}/4$. The selection of V_5 discharges and charges the FC for $i_A > 0$ and $i_A < 0$, respectively. Similarly, the selection of V_6 charges and discharges the FC for $i_A > 0$ and $i_A < 0$, respectively. In the same way, the corresponding switching states during $-V_{dc}/4$, and $\pm 3V_{dc}/4$ levels are selected depending on the discharging or charging requirements of the FC and the direction of i_A listed in Table 1.

3.3 | Charging process of the FC

Assuming that FC (C_a) is initially uncharged, $V_{Ca} = 0$ V. When the gate pulses and the DC supply are switched on, charging states of the FC listed in Table 1 are selected in the control platform as per the FC voltage balancing method. The automatic selection of charging states charges the FC, which gives $V_{Ca} = V_{dc}/4$. For example, V_6 and V_8 are selected during $\pm V_{dc}/4$ levels, respectively, for $i_A > 0$. Similarly, V_3 and V_{11} are selected during $\pm 3V_{dc}/4$ levels respectively, for

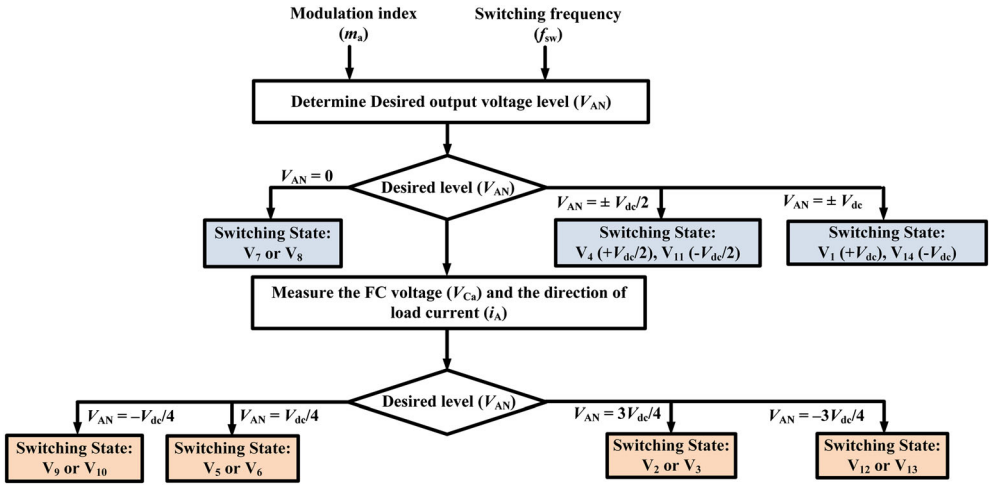

FIGURE 5 Flying capacitor voltage balancing method

$i_A > 0$. Figure 6 shows the charging process of the FC (C_a) during 9-L operation of the inverter observed in the experimentation. It shows that when the DC supply is switched on, the FC starts charging from the available charging states and reaches to a voltage of $V_{dc}/4 = 25$ V in a period of 40 ms (two fundamental cycles). The time taken for the charging process of the FC depends on the amount of load on the inverter and the modulation index (m_a). In practice, FCs are charged to the desired voltage with the presence of redundant switching states in two to three fundamental cycles.

3.4 | Selection of capacitors

The design of a capacitor depends on three important factors, namely, the % voltage ripple allowed, magnitude of the current flowing through it, and the operating period. Hence, the synthesized expression for designing of a capacitor is

$$C = \frac{I_m}{\Delta V_C \times f_{sw}}, \tag{2}$$

where I_m is the maximum value of current flowing through the capacitor, ΔV_C is the peak-to-peak voltage ripple, and f_{sw} is the switching frequency. In the proposed topology, both the DC-link and the flying capacitors are designed in accordance with the (2). The DC-link capacitor voltages V_{Cd1} and V_{Cd2} are naturally balanced due to equal conduction intervals of C_{d1} and C_{d2}. Whereas, the FC voltage V_{Ca} is maintained constant, due to the rich number of redundant switching states both during positive and negative half cycles.

4 | ADVANTAGES AND COMPARISON OF THE PROPOSED TOPOLOGY

The main advantages of the proposed topology include the lower voltage–rated semiconductor devices and a smaller number of conducting switches. At any voltage level, a maximum of five switches conducts, which gives higher efficient operation. Since the proposed topology does not demand clamping diodes, this results in saving of cost and floor space. Two switches, S_9 and S_{10}, operating at the fundamental switching-frequency results in minimized switching losses. Table 2 gives a detailed comparison of the number of switches, clamping diodes, flying capacitors, and DC sources required with respect to (w.r.t) the recently proposed and the conventional topologies. It can be noted that the complexity in the implementation of the proposed circuit is less because of a lower component count compared with conventional and other recent topologies in previous studies.[12,15,22,23] Moreover, for the same number of output voltage levels, the number of V_{dc}-rated switches required in the proposed topology are less by 62.5% and 25% compared with Gautam et al[14] and Sandeep and Udaykumar,[16] respectively. The FC voltage ripple is more in Sandeep and Udaykumar and Vahedi et al[17,24] because of the reduced number of redundant switching states. Finally, the proposed topology is compared with the coupled-inductor–based 9-L inverters in Salehahari and Babaei and Salehahari et al.[28,29] The topology presented in Salehahari and Babaei[28] requires three coupled–inductors and a DC source to produce the 9-L output with reduced charging currents and output voltage ripple. Further, an improvised hybrid structure is proposed in Salehahari et al[29] with reduced switch count and coupled-inductor count. In addition to that, coupled inductors share the load currents equally, which results in the reduction of switch currents. However, these topologies are associated with the problems of magnetic saturation, balancing of coupled inductor currents, and magnetic losses.

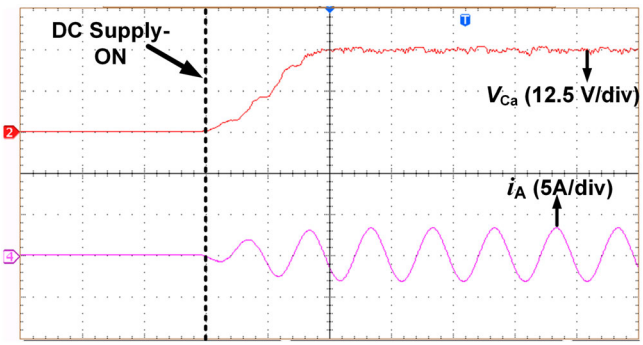

FIGURE 6 Charging process of the flying capacitor (C_a); time scale (20 ms/div)

TABLE 2 Comparison of the various 9-L inverter topologies

Components	[NPC]	[fc]	[CHB]	Gautam et al[14]	Li et al[12]	Wang et al[22]	Saeedian et al[23]	Vahedi et al[24]	Sandeep and Udaykumar[15]	Sandeep and Udaykumar[16]	Sandeep and Udaykumar[17]	Salehahari and Babaei[28]	Salehahari et al[29]	Proposed
Switches	16	16	16	8	12	12	12	10	12	10	8	10	8	10
Clamping diodes	56	--	--	--	--	--	--	--	--	--	--	--	--	--
Flying capacitors	--	36	--	--	2	2	2	1	1	1	1	--	--	1
DC-link capacitors	8	8	--	2	2	2	--	--	2	2	2	--	--	2
Coupled inductors	--	--	--	--	--	--	--	--	--	--	--	3	2	--
DC sources	1	1	4	2	1	1	1	1	1	1	2	1	1	1
Total no. of components	81	61	20	12	17	17	15	12	16	14	13	14	11	14

5 | SIMULATION AND EXPERIMENTAL RESULTS

5.1 | Simulation results

To verify the feasibility of the proposed single-phase 9-L inverter and the control scheme, the model is developed in MATLAB/Simulink environment. Table 3 lists the various system parameters taken for the study. In simulation studies, the DC bus voltage is considered as 100 V. The IPD-SPWM control pulses are generated at a switching frequency of 4 kHz. The performance of the model is tested for a load of 150 W.

Figure 7 shows the inverter response of output voltages (V_{BN}), (V_{AN}), load current (i_A), DC-link capacitor voltages, and the FC voltage in steady-state. It is noted that the 9-L output comprises with a step-size of 25 V. Figure 8B shows the inverter output voltage (V_{AN}) and current waveforms (i_A) for a step change in m_a and load during the periods at 1.62 and 1.66 seconds, respectively. Figure 8C illustrates the variation of the FC and the DC-link capacitor voltages for the above-said conditions. For a better understanding, the variation of capacitor voltages during the step change in m_a and load are zoomed and shown in Figure 8D. It can be noted that the FC voltage is well-balanced with almost negligible voltage ripple of 0.2% to 0.4% w.r.t load change. The DC-link capacitors' voltage ripple is varying from 6.4% to 16% before and after the load change. In order to show the reliability of PWM controller in balancing the FC voltage, a step-disturbance is created by switching off the FC voltage controller (FCVC) at a time (t) = 1 second as shown in Figure 8E. When the controller is off, the output voltage (V_{AN}) and current (i_A) are distorted, and the FC voltage is increasing. When the controller is turned on at t = 1.1 seconds, V_{AN} and i_A restore

TABLE 3 System parameters

Parameter	Simulation	Experimental
DC-link voltage	100 V	100 V
FC voltage	25 V	25 V
Capacitance (C_{d1}, C_{d2} and C_a)	1000 μF	1000 μF
Output power	150 W	150 W
Switching frequency(f_{sw})	4 kHz	4 kHz
Fundamental frequency (f_m)	50 Hz	50 Hz

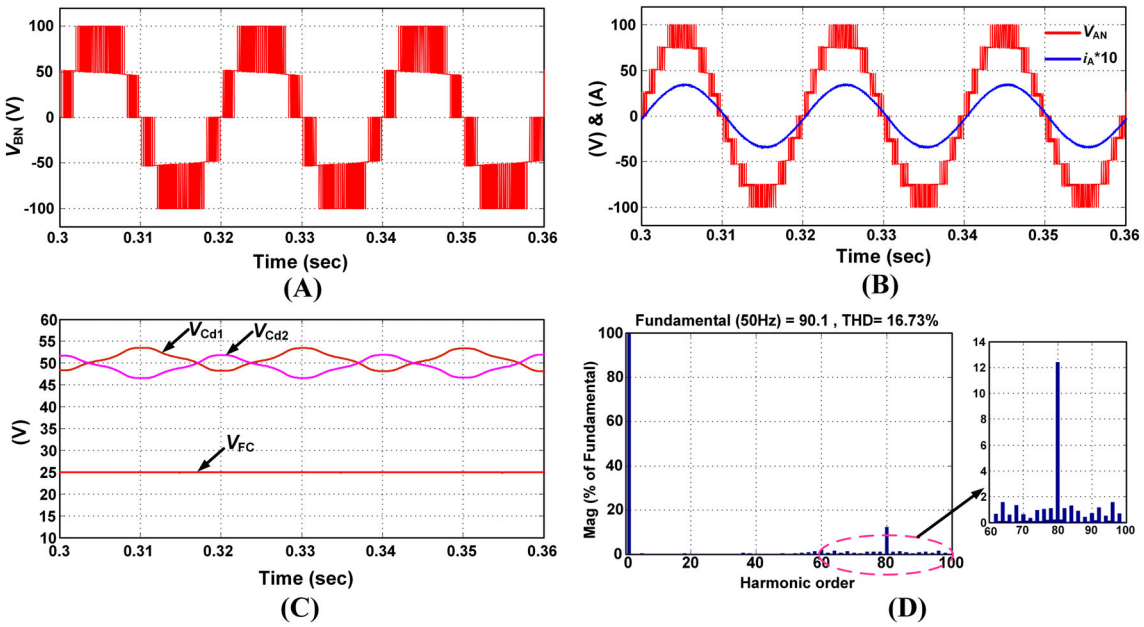

FIGURE 7 Simulation results of the proposed nine-level (9-L) inverter with R-L load in steady-state: A, voltage between section-1 and section-2; B, 9-L output voltage and the load-current; C, DC-link capacitors and FC voltages; D, harmonic spectrum of 9-L output voltage

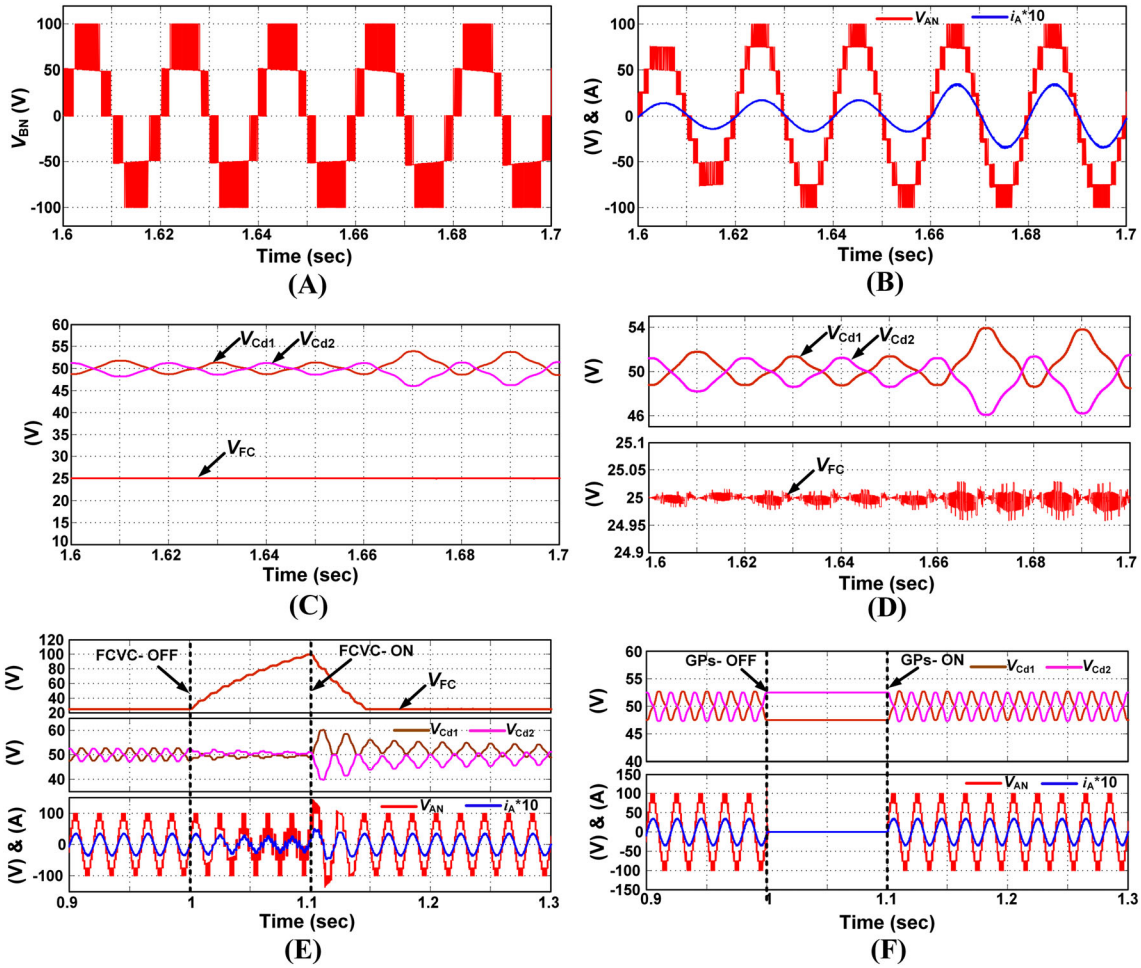

FIGURE 8 Dynamic results during the step change in m_a and load: A, voltage between section-1 and section-2; B, output voltage and the load-current; C, DC-link capacitors and FC voltages; D, zoomed waveforms of (C); E, FC voltage, output voltage, and load-current when pulse-width modulation (PWM) controller is switching; F, response of DC-link capacitor voltages by switching the GPs on and off

to normal shape and the FC voltage also decreasing and settle down to 25 V within four fundamental cycles. Figure 8F shows the response of the DC-link capacitor voltages (V_{Cd1} and V_{Cd2}) w.r.t disturbance in gate pulses (GPs) when the inverter is operating in steady-state. It shows that the voltages V_{Cd1} and V_{Cd2} are constant and ripple-free when the GPs are turned-off. A slight ripple appears in V_{Cd1} and V_{Cd2} due to the flow of load current through C_{d1} and C_{d2}, when the GPs are turned on. The equal charging and discharging intervals of C_{d1} and C_{d2} takes place inherently in the proposed topology, which results in the natural balancing of V_{Cd1} and V_{Cd2}. This shows the capability of the proposed topology, the FC voltage balancing technique, and natural balancing of DC-link capacitor voltages during transients.

5.2 | Experimental results

The experimental prototype shown in Figure 9 is fabricated for the parameters listed in Table 3. A single DC source has been used to generate the 9-L output. The control pulses of magnitude 3.3 V are generated in Xilinx FPGA processor using IPD-SPWM scheme and using logic gates. These low voltage pulses are magnified using a TLP250 driver circuit and given to the MOSFETs in the inverter. The DC-link capacitor voltages are naturally balanced with a single DC source, whereas the FC voltage is balanced by sensing the FC voltage and feedback to the processor. Logical programming has been implemented inside the processor to select the required switching state depending on the magnitude of the FC voltage. Figure 10A shows the FC voltage, 9-L inverter output voltage (V_{AN}) and current (i_a) for an m_a of 0.9. Figure 10B shows the FC voltage, 7-L inverter output voltage (V_{AN}) and current (i_A) for an m_a of 0.74. In order to show

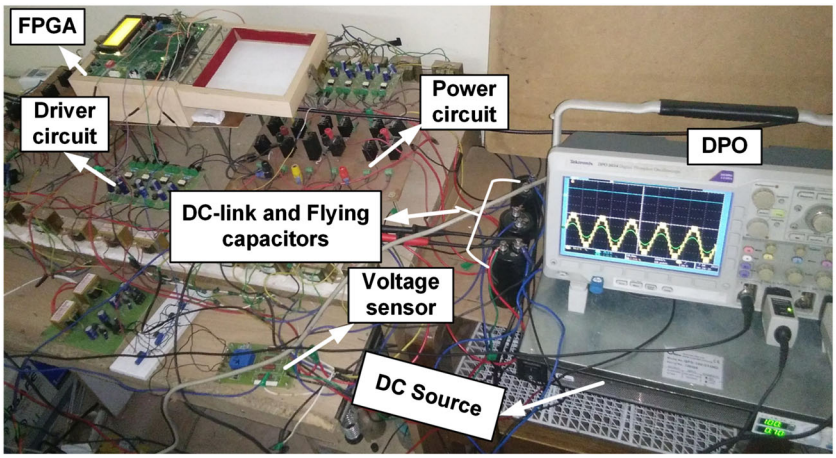

FIGURE 9 Experimental setup

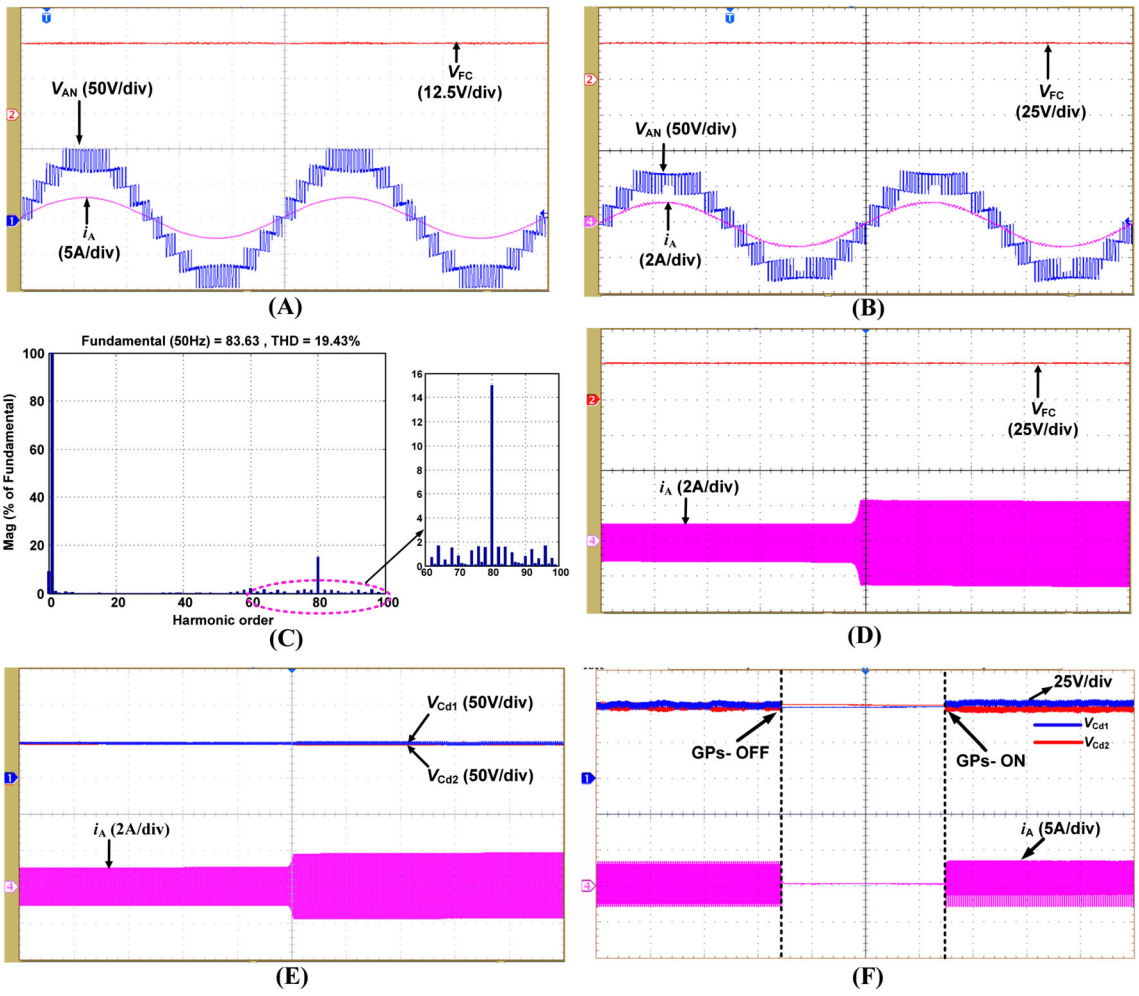

FIGURE 10 Experimental results: A, FC voltage (V_{FC}), output voltage (V_{AN}), and output current (i_A) at $m_a = 0.9$; time scale (4 ms/div); B, V_{FC}, V_{AN}, and i_A at $m_a = 0.74$; time scale (4 ms/div); C, harmonic spectrum of nine-level (9-L) voltage of V_{AN} (from CSV-file); D, FC voltage and output current for a step change in load; time scale (4 s/div); E, DC-link capacitor voltages (V_{Cd1} and V_{Cd2}) for a step change in load; time scale (4 s/div); F, response of V_{Cd1} and V_{Cd2} when switching the GPs on and off; time scale (1 s/div)

the reliability of the circuit, a step change in load is applied, and the corresponding FC voltage and the DC-link capacitor voltages are shown in Figure 10D,E. It is observed that the FC voltage remains constant with no change in voltage ripple. Whereas the DC-link capacitor voltage ripples are observed to be slightly increasing w.r.t the load. Further,

Figures 8F and 10F verifies the natural balancing of the DC-link capacitor voltages for a step change in gate pulses through simulation and experimentation, respectively.

Figure 11 shows the magnitude of the voltage stress and its pattern across all switches in the inverter. Figure 11A indicates the voltage stress waveforms across the switches in section-2. It shows that S_1, S_2, and S_3 are blocking a voltage of $V_{dc}/2$. However, S_4 is blocking a voltage of V_{dc}. Figure 11B shows the voltage stress waveforms across the switches in section-3. Since section-3 is an H-bridge, because of its symmetry in the structure, all switches are required to block an equal voltage of $V_{dc}/4$. Figure 11C shows the voltage stress across the switches in section-1. Since these switches are directly connected across the DC-link, therefore, the blocking voltage is of V_{dc}.

Further, Table 4 shows the performance and output quality of V_{AN} and i_A in terms of percentage total harmonic distortion (%THD) for different levels and for changes in m_a from 0.5 to 0.9. The theoretical values of voltage THD are obtained from the mathematical formulae introduced in Ruderman et al and Kirubakaran.[30,31] The derived value of %THD depends on two parameters, modulation index (m_a) and the number of output voltage levels (L), which is expressed as

$$\%THD = \frac{1}{\sqrt{3}(L-1)m_a} * 100 = \frac{57.7}{(L-1)m_a}\%. \quad (3)$$

For example, at $m_a = 0.5$, the possible number of output voltage-levels are only five, hence, the theoretical %THD according to the above equation is 28.8%. It can be noted that the theoretical, simulation, and experimental results are approximately equal, and the increase in output voltage levels by increasing the m_a reduces the %THD with improved quality in the output voltage. Also, the %THD of the current is less than 5%. Finally, Figure 12 shows the

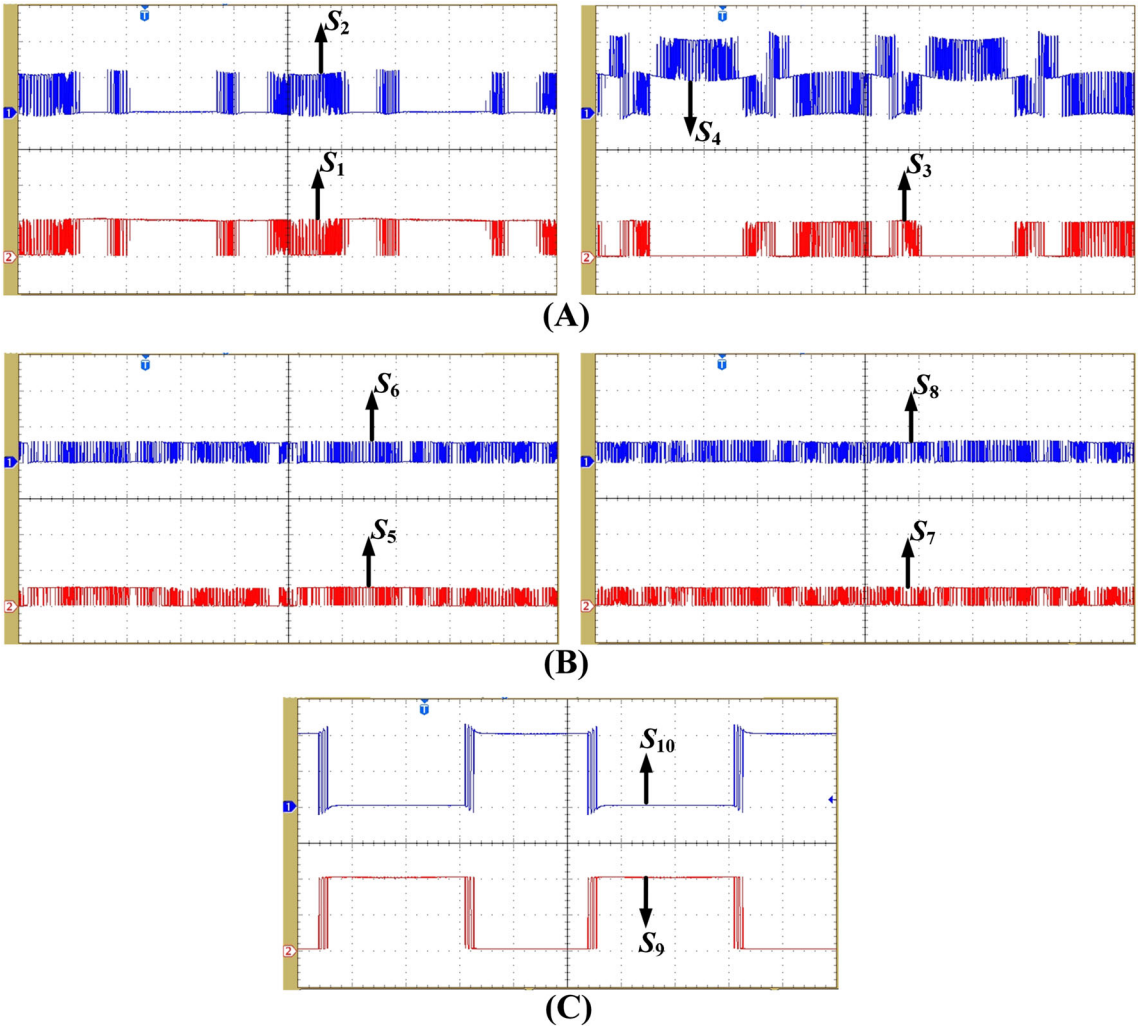

FIGURE 11 Voltage stress across the switches (scale on: Y-axis: 50 V/div, X-axis:4 ms/div)

TABLE 4 %THD of 5-, 7-, and 9-level output voltage (VAN) and load current (iA)

m_a	Output voltage-levels (L)	Voltage THD			Current THD	
		Theoretical	Simulation	Experimental	Simulation	Experimental
0.5	5	28.8	26.9	31	2.43	2.5
0.74	7	19.5	18.9	20.4	1.75	2.0
0.9	9	16.0	16.7	19.4	1.63	1.8

Abbreviation: THD, total harmonic distortion.

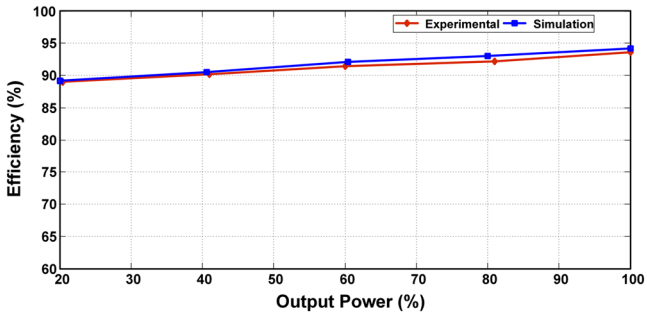

FIGURE 12 Efficiency curve

efficiency curves of the proposed hybrid inverter, the simulated efficiency is computed in MATLAB environment using the mathematical equations for loss calculations.[32]

The efficiency of the proposed 9-L inverter is evaluated for different loading conditions. The following expressions are used to calculate the various losses of the Mosfets and body diodes in the inverter switches.

$$P_Q = I_{on}^2 R_q \tag{4}$$

$$P_{sw} = K_q I_{on}^{a_q} V_{off}^{b_q} f_{sw} \tag{5}$$

$$P_D = I_{on} V_f + I_{on}^2 R_d \tag{6}$$

$$P_{rr} = K_{rr} I_{on}^{a_{rr}} V_{off}^{b_{rr}} f_{sw}, \tag{7}$$

where P_Q and P_{sw} are conduction and switching losses of the Mosfets, respectively; P_D and P_{rr} are conduction and reverse recovery losses of the body diode, respectively; I_{on} is the on state device current; f_{sw} is the switching frequency; and V_{off} is the off state device blocking voltage. The efficiency analysis is carried by calculating various losses of all switches in Matlab environment at a DC-link voltage of 100 V at different power outputs. Figure 12 shows the simulation and experimental efficiency curves of the proposed topology. It can be noticed that the efficiency of the experimental prototype is very close to the theoretical value, and a maximum of 94% can be achieved by the proposed topology.

6 | CONCLUSION

A novel 9-L hybrid inverter with reduced number of switches, FCs, and DC sources is proposed in this paper. The operating modes, charging process, and voltage balancing of FC are presented comprehensively. The PWM control to generate the output voltage levels and to regulate the FC voltage using redundant switching states is studied. The

natural balancing of DC-link capacitor voltages using single DC source has been verified. The stiffness of the FC voltage and DC-link capacitor voltages are confirmed with low voltage ripples through simulation and experimental results. Further, the working and feasibility of the proposed topology to produce 9-L output voltage with sinusoidal nature of load current are confirmed through simulation and experimental studies in steady-state and transient conditions. Finally, the simulated and experimental efficiency curves shows that a maximum of 94% efficiency can be achieved for medium voltage applications.

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