A Space Vector Modulated Quasi-Z-Source Based Four-Level VSI for PV Application

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***Abstract*—A Four-level Inverter system is presented in this paper, which employs a Space Vector Modulated Quasi-Z-Source to obtain high-boost inversion for PV applications. Unlike the conventional Multilevel Inverters, such as Neutral-Point Clamped (NPC) and the Cascaded H-Bridge (CHB) configurations, the proposed inverter uses only 19 power semiconductor switching devices and three Quasi-Impedance networks. It is also shown that by employing level-shifted carrier modulation, one can achieve higher shoot through duty ratio, enhancing the boosting capability of the proposed inverter. The performance of the proposed power circuit is assessed with simulation studies, which reveal its applicability for PV applications.**

Keywords—Cascaded Configuration, Four-Level Inversion, Space Vector Modulation (SVM), Quasi-Z-Source.

I. Introduction

Owing to the growing emphasis on PV generation, several power circuit configurations are being suggested by various researchers [1]. Of these, the circuit topologies involving the Z-Source and the quasi-Z-Source (qZS) attracted the attention of researchers owing to the achievement of the twin objectives of voltage boosting and the DC-AC conversion in a single stage. Of the two aforementioned topologies, the qZS converter is more advantageous, as it results in a continuous input current, which is essential for PV based applications. Also, the qZS converter results in a considerably smaller size and reduced stress on the capacitors [2].

On the other hand, multilevel inversion is the most viable technology for PV applications, as it is capable of producing output with lower Total Harmonic Distortion (THD), lower stress on the semiconductors and low Electro Magnetic Interference (EMI) [3]. Thus, the fusion of impedance-source with multilevel inverters can achieve the benefits associated with both of these topologies.

In this direction, some authors have proposed to connect either a three-level or a five-level Neutral Point Clamped (NPC) Multi-Level Inverter (MLI) to the output terminals of either a dual- or a single- impedance-source [4] - [6]. Other topologies include magnetically coupled inductors for the Z-source to enhance the boost factor [7], [8]. These converters, being based on the NPC topology, require several fast-recovery clamping diodes. Therefore the cost and complexity of these circuits is more. Also, owing to the discontinuous current caused by simple Z-source front-ends, these converters are not preferred for PV based applications. To improvise this situation, some authors have proposed the employment of qZS front-ends of either conventional type or coupled-inductor type [9] and [10]. However, these topologies still use the NPC MLIs at the back-end.

To avoid the problems associated with the NPC back-ends, some authors have proposed the employment of Cascaded H-Bridge Multi-Level Inverters (CHB-MLIs) [11-13]. While these circuits facilitate independent MPPT with shoot through, the circuit cost and complexity increases for increased number of levels.

Thus, there exists a necessity to improvise the PV-based three-phase MLI topologies, which facilitate not only independent MPPT, but also reduce the circuit complexity associated with the NPC and CHB MLIs. To this end, this paper proposes a qZS based four-level VSI. The proposed topology uses only 19 power semiconductor devices and no clamping diodes. It also facilitates independent MPPT for the constituent PV strings. The four-level VSI employs level-shifted carrier modulation, which can achieve a higher shoot through duty ratio and consequently a higher boosting capability.

II. Proposed Topology

The proposed power circuit configuration is illustrated in Fig.1. It may be observed that the proposed topology consists of three quasi-Z-sources, the outputs of which are connected to the four-level VSI proposed in [14]. Unlike the NPC configuration, the proposed power circuit employs the time-tested, industry-proven two-level inverter as the basic building block. Thus, 12 fast-recovery clamping diodes are avoided in the proposed power circuit configuration.

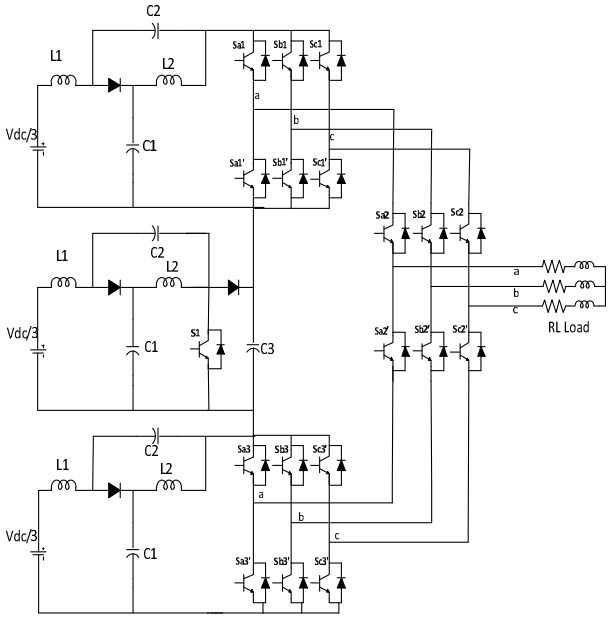

Fig. 1. Proposed power circuit configuration for 4-level VSI with quasi-Z-source inputs.

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It may be observed that the proposed power circuit employs a total of 19 power semiconductor switching devices. For the top and bottom quasi-Z-sources, the shoot through states are provided by the phase-legs of the two-level VSIs. However, for the middle stage, the shoot through is provided by an exclusive device (S_1, in Fig. 1) to boost and regulate the desired level of DC-link voltage.

III. Control Scheme

It is well known that the Space Vector Pulse Width Modulation (SVPWM) results in 15% more utilization of dc link when compared to the sine-triangle PWM technique. The two main variants of the SVPWM schemes widely used in MLIs are: (i) Phase-Shifted PWM (PSPWM) (ii) Level-Shifted PWM (LSPWM). Of these two schemes, the LSPWM is widely used as it results in a lesser harmonic content in the output voltage waveform [15]. Hence, in this paper, the LSPWM is implemented.

In SVPWM the reference voltage vector in a sector is synthesized by using active vectors and zero vectors.

T_1, T_2 are active switching times and T_0 = Zero time which are stated below by following expression

$$T_1 = [Msin(60-\theta)]T_s$$

$$T_2 = [Msin(\theta)]T_s$$

$$T_0 = [1-Mcos(30-\theta)]T_s$$

Where $0 < M < 1$

$$0 < \theta < \pi/3$$

Where M is modulation index and is defined as $\frac{\sqrt{3}V_{ref}}{V_{dc}}$ and θ is the angle of voltage reference vector.

So from the above equation, it is evident that, T_0 is minimum when theta equal to $\pi/6$ and maximum at zero and $\pi/3$, so the inserted shoot through state must be less than or equal to the minimum T_0 time period available for a particular modulation index.

In this work, the SVPWM is implemented by adopting the procedure described in [16], wherein the concept of imaginary switching time periods is employed. This technique avoids the cumbersome task of sector identification, reducing the computation burden on the processor. The imaginary switching times T_{as}, T_{bs}, T_{cs}, which are directly proportional to the phase voltages of the inverter are calculated from the following expression.

$$T_{as} = \left(\frac{T_s}{V_{dc}}\right)va^*;\ T_{bs} = \left(\frac{T_s}{V_{dc}}\right)vb^*;\ T_{cs} = \left(\frac{T_s}{V_{dc}}\right)vc^* \quad (1)$$

Maximum and minimum imaginary switching times are calculated at each instant by the following equations

$$T_{Max} = max\ (T_{as}, T_{bs}, T_{cs})\ and\ T_{Min} = min\ (T_{as}, T_{bs}, T_{cs}) \quad (2)$$

The effective time period is calculated as:

$$T_{eff} = T_{Min} - T_{Min} \quad (3)$$

The offset time period is added to each imaginary switching time period (T_{as}, T_{bs}, T_{cs}) to make it as center spaced PWM technique.

$$T_{Offset} = T_0/2 - T_{Min} \quad (4)$$

where

$$T_o = (T_s - T_{eff}) \quad (5)$$

which gives actual switching times for each inverter leg as:

$$\left.\begin{aligned} T_{ga} &= (T_{as} + T_{Offset}) \\ T_{gb} &= (T_{bs} + T_{Offset}) \\ T_{gc} &= (T_{cs} + T_{Offset}) \end{aligned}\right\} \quad (6)$$

The modulating waves T_{ga}, T_{gb}, T_{gc} that are produced using the above set of equations, are compared with three level shifted carriers of equal magnitude placed one over the other.

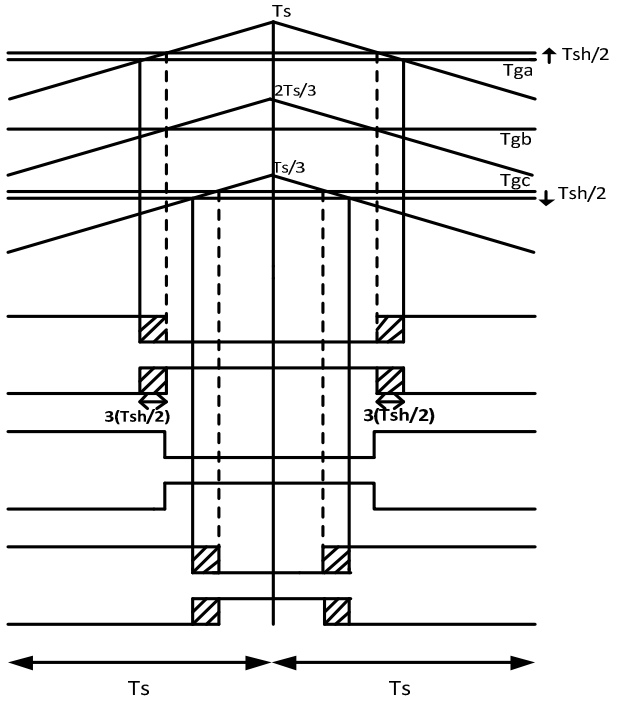

Fig. 2. Shoot through state insertion technique.

As shown in Fig. 2 T_{ga}, T_{gb}, T_{gc} are the modulating waveforms obtained by the application of the aforementioned switching algorithm. These modulating waves are compared with three level-shifted carrier waves to produce the required switching for the proposed four-level VSI. To introduce the shoot through state, two additional reference signals are generated, which are obtained by shifting the maximum and minimum of the modulating signals by half of the shoot through time.

$$T_{gmax} = max\ (T_{ga}, T_{gb}, T_{gc}) \quad (7)$$

$$T_{gmin} = min\ (T_{ga}, T_{gb}, T_{gc}) \quad (8)$$

Switching logic for the upper and lower switches of the three constituent inverters is described by the following set of equations:

$$\left.\begin{aligned} T_{gmaxu} &= T_{gmax} + \frac{T_{sh}}{2} \\ T_{gmaxl} &= T_s - T_{gmax} \\ T_{gmidu} &= T_{gmid} \\ T_{gmidl} &= T_s - T_{gmid} \\ T_{gminu} &= T_{gmin} \\ T_{gminl} &= T_s - T_{gmin} - \frac{T_{sh}}{2} \end{aligned}\right\} \quad (9)$$

In the above set of equations, the subscripted letters '*u*' and '*l*' respectively denote the upper and the lower switches of the inverter

From Fig. 2 and eq. (9), it may be noted that, an increment of '$T_{sh/2}$'in the reference signal (T_{ga}) manifests as an increment in the shoot through time period (introduced in phase-A) of $3T_{sh/2}$. Thus, it is evident that the LSPWM results in scaling-up of the shoot through time by a factor of 3. Consequently, the increase in the shoot through time increases the boosting capability of the inverter.

The symbols D and B_{conv} respectively denote the shoot through duty ratio and the boost factor obtained by employing the conventional SVPWM scheme. The relationship between them is given by [2]

$$B_{conv} = \frac{1}{1-2D} \tag{10}$$

The proposed LSPWM scheme offers the possibility of increasing the shoot through duty ratio (D) to (3D/2). Consequently the boost factor with the proposed SVPWM scheme becomes:

$$B = \frac{1}{1-2(\frac{3D}{2})} = \frac{1}{1-3D} \tag{11}$$

Fig. 3 depicts the switching states of the middle inverter. When the middle carrier wave is compared with T_{ga}, T_{gb}, T_{gc}, it is evident that only the active states 110 and 100 are generated, with no zero-state present in the sampling time period. This removes the capability of inserting the shoot through time in the middle inverter.

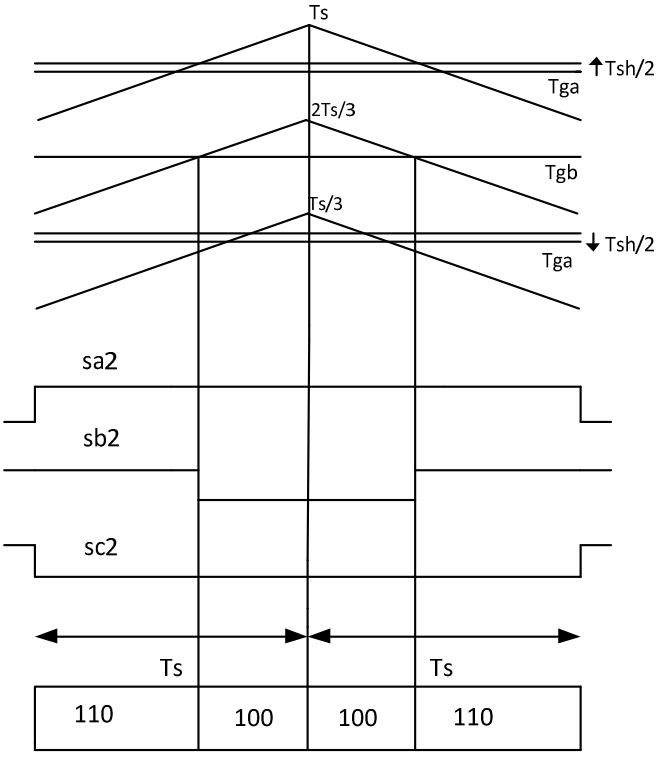

Fig. 3. Switching states of middle inverter in proposed cascaded MLI.

Thus, in order to insert the shoot through in the middle inverter, an additional switching device (S_1) is employed at the output terminals of the qZS network as shown in the Fig. 1. The shoot through action of the second Quasi Z source is synchronized with either top or bottom Quasi Z source networks. Thereby entire shoot through is inserted only by a single switch (S_1) which enables the middle inverter to be shoot through free.

Table I presents the switching states to obtain the pole voltages and the shoot through state for a phase-A in the proposed inverter topology.

As shown in Table I, the shoot through state is inserted either by turning on sa1 and sa1' (for the top inverter) or sa3, sa3' (for the bottom inverter). There is no shoot through state inserted in the middle inverter switches Sa2 and Sa2' as there is no availability of zero time.

TABLE I. SWITCHING STATES OF FOUR LEVEL CASCADED Z-SOURCE INVERTER

Pole Voltage (V_{A0})	**State of switch**					
	Sa1	**Sa1'**	**Sa2**	**Sa2'**	**Sa3**	**Sa3'**
Vdc	ON	OFF	ON	OFF	OFF	OFF
2Vdc/3	OFF	ON	ON	OFF	OFF	OFF
Vdc/3	OFF	OFF	OFF	ON	ON	OFF
0	OFF	OFF	OFF	ON	OFF	ON
Shoot through	ON	ON	OFF	OFF	OFF	OFF
Shoot through	OFF	OFF	OFF	OFF	ON	ON

IV. SIMULATION RESULTS

The performance of the proposed power circuit is simulated for 1 kW design configuration for R-L type of load and is assessed using MATLAB Simulink. A modulation index (M) of 0.77 and a shoot through duty cycle (D) of 0.196 is considered for simulation studies. Table-II presents the circuit parameters.

TABLE II. SPECIFICATIONS OF THE INDUCTOR AND CAPACITOR VALUES USED DURING SIMULATION

Parameters	**Values**
Output Power	1 kW
DC voltage V_{dc}	300 V
Inductor (L)	3.5 mH
Capacitor (C)	1000 µF
RL-Load	157 Ω, 22 mH
Frequency	20 kHz

Fig. 4 shows the respective DC-link voltages of the quasi-Z sources. It may be observed that, the DC-links of the top- and bottom Z-sources switch between the levels of zero and 243 volts (as the shoot through is provided by the phase-legs of the output inverter), while the middle DC-link is steady at 243 V. This figure, thus demonstrates the basic working principle of the proposed inverter topology.

The line, phase and pole voltages of the proposed four-level VSI are shown in the top three traces Fig. 5. The waveform of the load current is presented in the bottom trace of Fig. 5. The effectiveness of the power circuit is evident as it results in sinusoidal current. Fig. 6 shows the switching pulses for the upper, middle and lower leg of inverter phase A.

Fig. 7 shows the FFT of the phase voltage waveform. It can be observed that the calculated modulation and boost factors result in the desired phase voltage of 230 V (RMS).

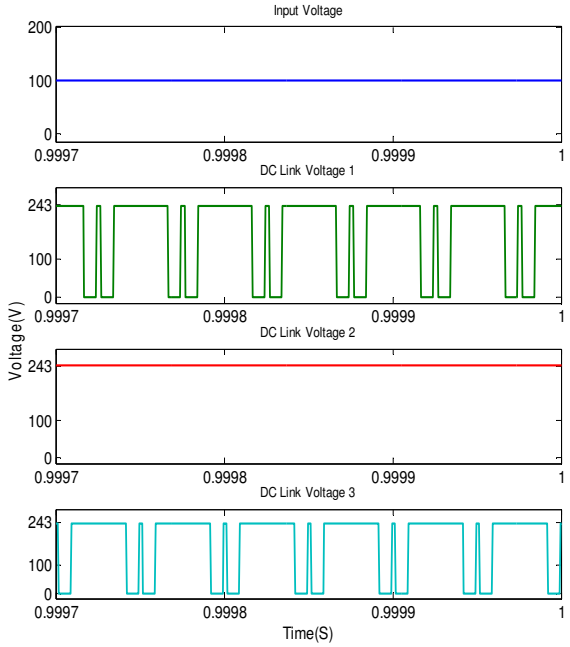

Fig. 4. Outputs of the front-end quasi-Z sources.

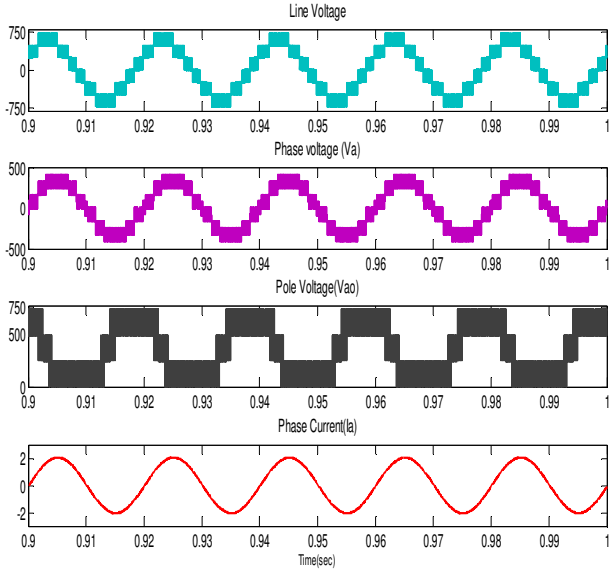

Fig. 5. Line voltage, phase voltage, pole voltage and line current for RL load for M = 0.77 and D_0 = 0.19.

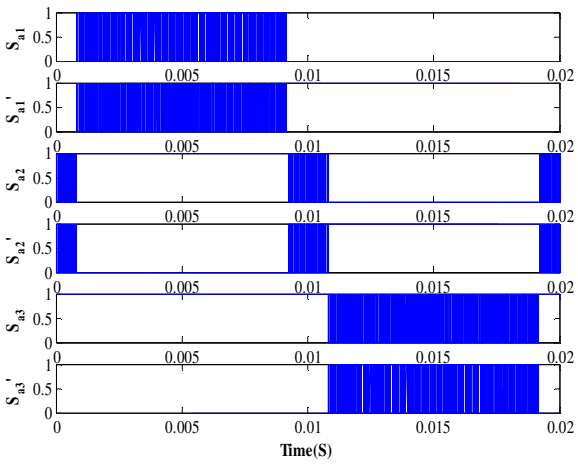

Fig. 6. Switching pulses of phase A.

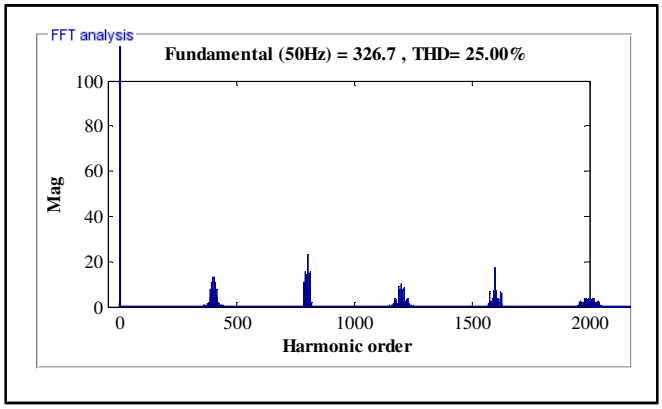

Fig. 7. FFT of the phase voltage waveform.

V. Conclusion

This paper presents a new qZS-based four-level VSI for PV applications. The proposed topology employs only 19 power semiconductor devices of which 12 devices provide a natural shoot through condition for boosting the input voltage. It is shown that, the implementation of SVPWM with level -shifted carrier waveforms results in an increased boost factor. Finally, the effectiveness of the proposed topology is verified through *Matlab/Simulink* software.

References

[1] O. Ellabban and H. Abu-ub, "Z-Source Inverter-Topology Improvements Review," *IEEE Ind.Magazine*, vol. 10, no. 1, pp.6–24, Mar. 2016.

[2] Y. Li, J. Anderson, F. Z. Peng, and D. Liu, "Z-Source Inverter-Topology Improvements Review," *24th Annual IEEE Applied Power Electronics Conference and Exposition,* pp.918–924, Mar. 2009.

[3] A. El-Hosainy, H. A. hamed, H. Z. Azazi, and E. E. El-Kholy, "A review of multilevel inverter topologies, control techniques, and applications," *IEEE 19th International Middle East Power Systems Conference*, pp.504–510, Dec. 2017

[4] P. C. Loh, F. Blaabjerg, and C. P. Wong, "Comparative evaluation of pulse width modulation strategies for Z-source neutral-point-clamped inverter," *IEEE Trans. Power Electron.*, vol. 22, no. 3, pp. 1005–1013, May 2007.

[5] P. C. Loh, S. W. Lim, F. Gao, and F. Blaabjerg, "Three-level Z-source inverters using a single LC impedance network," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 706–711, Mar. 2007.

[6] O. Husev, C. Roncero-Clemente, E. Romero-Cadaval, D. Vinnikov, and S. Stepenko, "Single phase three-level neutral-point-clamped quasi-Z-source inverter," *IET Power Electron.*, vol. 8, no. 1, pp. 1–10, 2015.

[7] F. Gao, P. C. Loh, F. Blaabjerg, R. Teodorescu, and D. M. Vilathgamuwa, "Five-level Z-source diode-clamped inverter," *IET Power Electron.*, vol. 3, no. 4, pp. 500–510, 2010.

[8] R. Strzelecki, M. Adamowicz, and D. Wojciedchowski, "Buck-Boost Inverters with Symmetrical Passive Four-terminal Networks," *Proc. CPE*, pp. 1-9, 2007.

[9] H. F. Ahmed, H. Cha, S. H. Kim, H. G. Kim, "Switched-Copuled-Indctor Quasi-Z-Source Inverter," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1241–1254, Mar. 2015.

[10] W. Mo, P. C. Loh, D. Li, F. Blaabjerg, "Trans-z-source neutral point clamped inverter," *in Proc. of Power Electronics, Machines and Drives*, pp.1-5, Mar. 2012.

[11] Y. Liu, B. Ge, H. Abu-Rub, and F. Z. Peng, "An effective control method for quasi-Z-source cascade multilevel inverter-based grid-tie single phase photovoltaic power system," *IEEE Trans. Ind. Inform.*, vol. 10, no. 1, pp. 399–407, Feb. 2014.

[12] Y. Liu, B. Ge, H. Abu-Rub, and F. Z. Peng, "An effective control method for quasi-Z-source cascade multilevel inverter based three-phase grid-tie photovoltaic power system," *IEEE Trans. Ind. Electron.*, vol. 61, no. 12, pp. 6794–6802, Dec. 2014.

[13] D. Sun, B. Ge, X. Yan, D. Bi, H. Zhang, Y. Liu, H. Abu-Rub, L. Ben-Brahim, F. Z. Peng, "Modeling, Impedance Design and Efficiency Analysis of Quasi-Z Source Moduel in Cascaded Phtotovoltaic Power System," *IEEE Trans. on Ind. Electron.,* vol. 61, no.11, pp. 6108-6117, 2014.

[14] B. Krishna Chaithanya, and A. Kirubakaran, "A Novel Four Level Cascaded Z-Source Inverter," *IEEE PEDES Conference*, pp.1-5, 2014.

[15] Bin Wu, Mehadi Narimani "High Power Converters and AC Drives," *Wiley-IEEE Press*, 2nd edition, 2017.

[16] Joohn-Sheok Kim and Seung-Ki Sul, A Novel Voltage Modulation Technique of the space vector PWM," *The Transactions of the Institute of Electrical Engineers of Japan*, vol.116-D, pp. 820-825, Jul. 1996.