Two-Stage SEPIC Based Single-Phase Five-Level Inverter for Photovoltaic Applications

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***Abstract*—This paper presents a modified two-stage sepic based five-level inverter for photovoltaic applications. The proposed configuration is built with a frond-end sepic converter cascaded with full bridge inverter through a high-frequency transformer and auxiliary circuit. The merits of the proposed configuration are high boost output voltage level, modularity, reduced device parts, and better quality of supply. In this paper, detailed construction and operation of the proposed two-stage configuration is presented. In order to validate the concept, simulation work is carried out through Matlab software and their results are presented.**

Keywords—photovoltaic, sepic converter, full bridge inverter, power quality.

I. INTRODUCTION

Energy generation from photovoltaic (PV) system has been growing in the past ten years due to the availability of large resource of sun energy and eco-friendly nature. The cost of the PV panels has significantly reduced in the last few years due to the technology development which results in reduction in the cost of power generation from the photovoltaic system. However, the challenge is on the integration of PV systems to cope with power fluctuations during climate changes, common mode voltage and leakage current due to parasitic components; the development of suitable power electronic interfaces and controllers has therefore assumed significance.

There is an adequate number of single-stage DC/AC inverters and two-stage consisting of DC/DC converters cascaded with DC/AC inverters have been developed to convert PV output voltage into a suitable form of energy for standalone/grid connection. Each configuration has its own merits and demerits. However, the direct DC/AC in always buck in nature and demands large DC-link voltage. The use of conventional boost converter has also limited high output voltage gain due to an increase in energy losses and poor efficiency at higher duty cycle. Therefore, the sepic converter is considered for the study which has advantages of step-up and step-down operation; cascading to the high-frequency transformer leads to further increase in voltage gain. In this way, high gain can be achieved by the proposed configuration.

Recently, multilevel inverters(MLIs) with reduced parts count topologies have become popular. MLIs offer the advantages of high power quality, reduced device ratings and lower electromagnetic interference; MLIs also considerably reduce the size of the filter compared to conventional Two-level inverter. Some of the recent literature reveals that the output voltage quality is improved by the reduction in total harmonic distortion for the increase in output levels[1-3]. However, the complexity of the circuit and the number of switching devices and driver units will increase for increased output levels. Therefore, a five-level z source based MLI is proposed in [4]. Among the various MLIs, Cascaded H-Bridge(CHB) is the most popular one. However, it demands independent DC sources and a large number of semiconductor devices for the increase in level. Later, asymmetric MLIs became popular with CHB configurations for increased output voltage levels with the same switches using different ranges of DC sources. Without compromise in the increase in output level and devices counts, a transistor clamped five-level inverter with reduced devices is proposed for multi-string PV applications in [5-6]. The same inverter is cascaded for more output levels in [7]. This is achieved using a frond end multi-winding transformer with three-phase rectifier units for three-phase induction motor applications. However, the boosting is achieved only with a transformer design and is bulky. Some of the recently proposed flying capacitor based MLIs [8] and other MLIs with modified configuration with H-bridge circuit [9] are found to perform better for five-level operation with better quality of output waveforms. But, these configurations demand more switching devices than usual.

Therefore, in this paper, a five-level inverter consisting of a full bridge inverter connected to an auxiliary circuit cascaded with the sepic converter through a high-frequency transformer is presented. The main advantage of the proposed topology is that high voltage boosting can be achieved with simple control. The complete operation of the proposed configuration is presented. Moreover, simulation work has been carried out to validate the concept in using Matlab software and their results are presented.

II. PROPOSED TWO-STAGE SEPIC BASED FIVE-LEVEL INVERTER

Fig. 1 shows the proposed two-stage configuration of the sepic based five-level inverter for photovoltaic applications. It consists of various parts of sepic dc/dc converter, HF transformer, Full bridge inverter and auxiliary circuits. The proposed configuration is more useful for single phase applications. The five-level inverter is basically a modular structure and the levels can be extended by clamping the DC-link voltage with additional auxiliary circuits. The detailed operation of each part is as follows;

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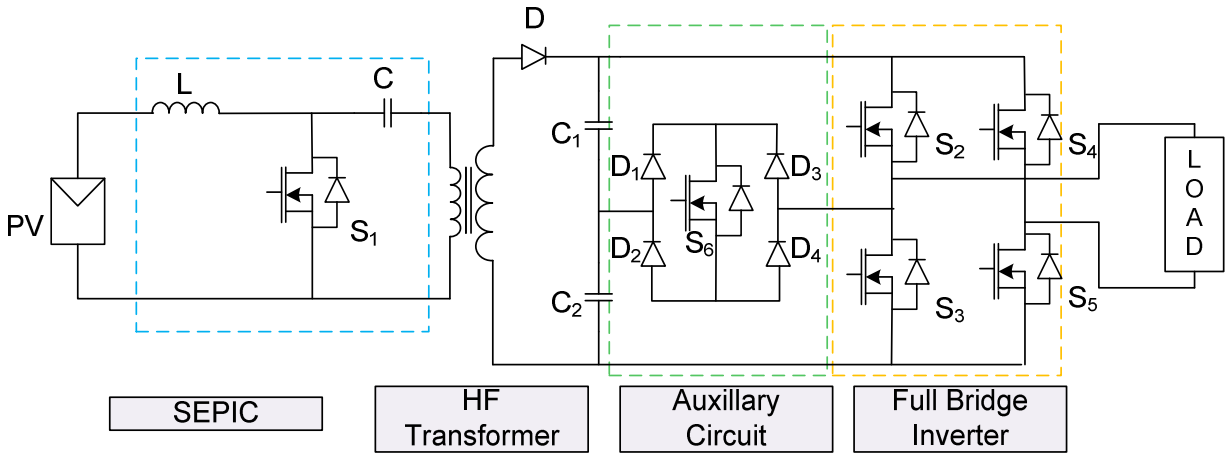

Fig. 1. Proposed two-stage sepic based five-level inverter.

A. SEPIC Converter

The single-ended primary inductor converter(SEPIC) is constructed using two inductors, one capacitor and a single switch. The main function this converter is it can be operated at less than, greater than or equal to the input voltage by adjusting the duty cycle. The main advantage of this converter is one of the inductors is utilized as the primary winding of the HF transformer. This results in a reduction in the volume and size of the system.

Fig. 2 depicts the simple circuit configuration of the SEPIC converter. The voltage transfer gain(M) of the converter can be derived using the following formulae by applying volt-sec balance equations.

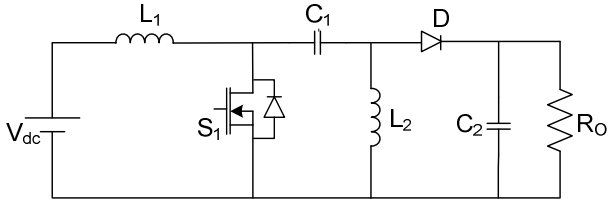

Fig.2. SEPIC Converter.

$$M = \frac{V_o}{V_{dc}} = \frac{D}{1-D} \tag{1}$$

where V_{dc} is the input dc voltage, V_o is the output voltage and D is the duty cycle.

B. Multilevel Inverter

Fig. 3 depicts the single-phase five-level inverter with reduced number of switches on a single DC source. The source voltage is split into two half over the DC-links using two capacitors. The positive half cycle and the negative half cycle is obtained with the use of a full bridge circuit; wherein the auxiliary circuit is used to generate levels such as V_{dc} and $2V_{dc}$. Table I shows the switching states and corresponding output voltage levels. It can be noticed that only two switches are conducting for each level generation, which results in higher efficiency of the inverter topology.

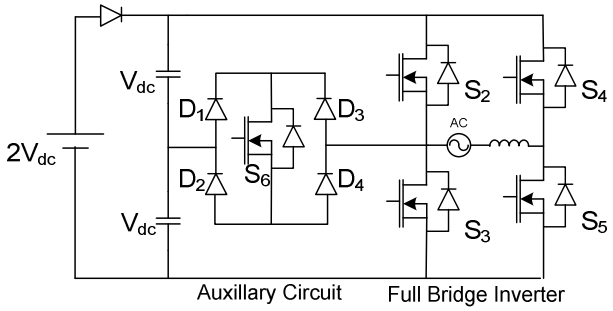

Fig. 3. Single-phase five-level inverter.

TABLE I
SWITCHING STATES AND CORRESPONDING OUTPUT VOLTAGE LEVELS

S_2	S_3	S_4	S_5	S_6	V_o	Number of conducting switches
1	0	0	1	0	$2V_{dc}$	2
0	0	0	1	1	V_{dc}	2
0	1	0	1	0	0	2
0	0	1	0	1	$-V_{dc}$	2
0	1	1	0	0	$-2V_{dc}$	2

III. CONTROL ALGORITHM

The control signals for the five-level inverter is generated using sine pulse width modulation as shown in Fig. 4. A high-frequency carrier is compared with the level shifted modulated sine waveform to produce the switching signals for switches S_1 to S_5. It can be noticed that the switching pulses S3 and S4 are complementary and operate at a fundamental switching frequency; wherein other switches are operating at higher switching frequency. The output level is decided by the modulation index M_a. It should be maintained between 0-1 for linear control in output voltage. M_a >1 leads to over modulation which results in higher harmonics in the output phase voltages.

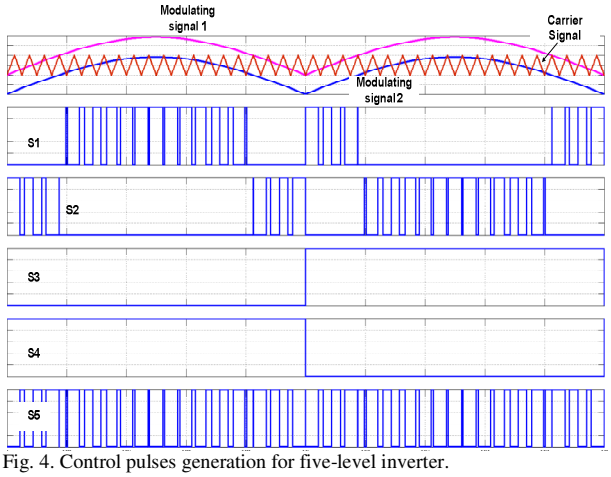

Fig. 4. Control pulses generation for five-level inverter.

IV. Comparison of Various Five-Level Inverters

In order to demonstrate the advantage of the proposed auxiliary circuit; a detailed comparison is made with the recently proposed five-level inverters in the literature along with conventional CHB topology. From Table II it can be observed that the proposed MLI configuration demands less number of switches and better regulation of DC-link voltage and the voltage level can be enhanced by adjusting the duty cycle of the sepic converter. In the case of CHB and flying capacitor based MLIs, it is difficult to enhance the voltage unless changes in the source voltages occur.

TABLE II
COMPARISON OF RECENTLY PROPOSED FIVE-LEVEL INVERTERS

Topology	Number of DC Sources	Number of Switches	DC link Voltage regulation
CHB	2	8	No
Ref. [8]	1	8	No
Ref. [9]	1	8	No
Ref. [10]	1	6	Yes
Proposed	1	5	Yes

V. Simulation Results

In this section, the proposed topology is verified through Matlab simulation software. The parameters considered for the simulation study are given in Table II. Fig. 5 shows the simulated waveforms of the input voltage, dc-link capacitor voltages, five-level inverter output voltage and their corresponding load currents respectively.

It can be observed that the input voltage is maintained constant and boosted to an output voltage of 150V by SEPIC converter and further stepped up to 300V with HF transformer. Also, the voltage across the capacitors is maintained at 150V to generate five-level output voltage waveform. It can be noticed that the output voltage is always maintained constant during load transitions from 3A to 8A peak to peak at 1 sec. By employing a suitable controller the output voltage can be regulated for both step changes in load as well as input voltage changes. Fig. 6 illustrates the measured frequency spectrum of both inverter five-level output voltage and load current waveforms. The %THD of the output current is within IEEE standard limits. This shows that the proposed configuration is well suited for PV applications.

TABLE III
SPECIFICATIONS OF THE PARAMETERS

Parameters	Values
Input dc voltage V	100 V
Inductor L	500 μH
Capacitors C, C_1 & C_2	100 μF, 2000 μF, 2000 μF
LCL Filter	1mH, 1μF
Switching Frequency of the SEPIC converter	50 kHz
Switching Frequency of the five-level inverter	40 kHz
RL Loads	100Ω, 10mH; 50Ω, 10mH

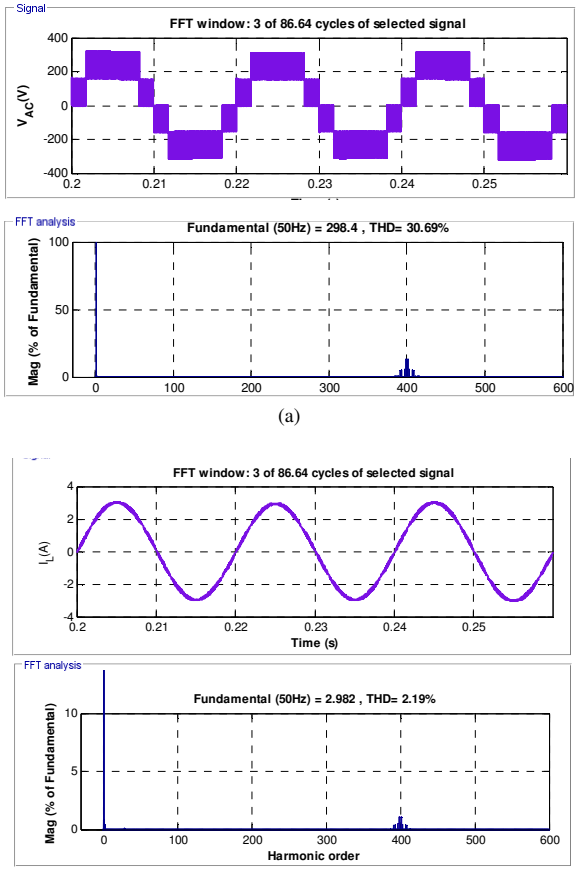

Fig. 6. FFT spectrum of (a) Inverter output voltage (V_{ac}) and Load current (I_L).

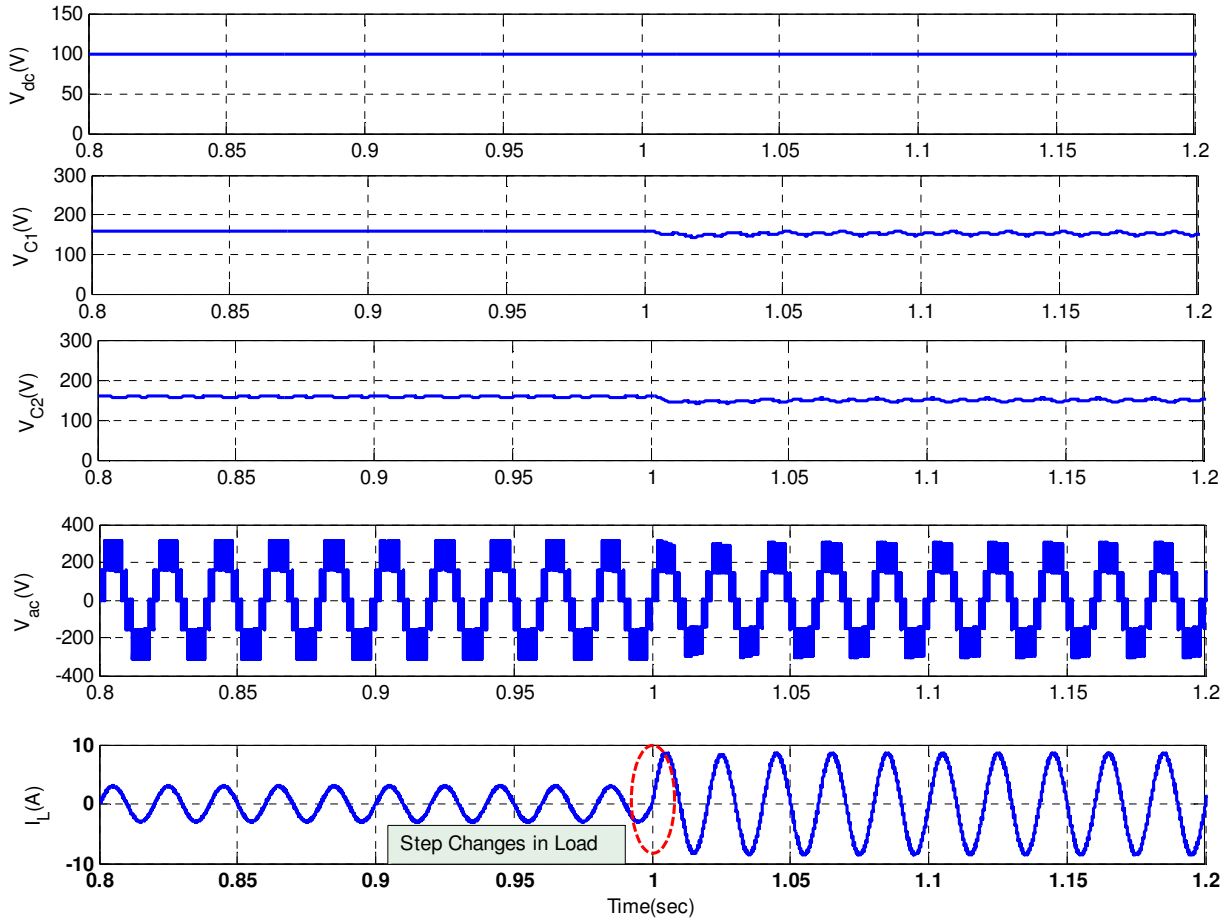

Fig. 5. Input voltage (V_{dc}), Capacitor voltages(V_{c1}, V_{c2}), Inverter Output Voltage(V_{ac}), & Load current(I_L).

VI. Conclusion

In this a paper, a new two-state sepic based five-level inverter is presented for photovoltaic applications. The paper also addresses the complete operating and switching control schemes developed for the proposed configuration. Simulation work is carried out in Matlab software and tested for load changes to observe their performance. The %THD of the voltage and current waveforms are also measured and results show better response. Development of experimental setup is in progress and their results will be presented in future publications. Finally, it is concluded that the proposed topology is eminently suited for PV applications.

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