

A Complete Fault-Tolerant Solution For A Single-Phase Five-Level Hybrid Flying Capacitor Inverter

Bolishetti Sunil Kumar

Department of Electrical Engineering
National Institute of Technology, Warangal
Warangal, India
sunilbolishetti@gmail.com

A.Kirubakaran, Senior Member IEEE

Department of Electrical Engineering
National Institute of Technology, Warangal
Warangal, India
kiruba81@nitw.ac.in

Abstract—Inverters generally experience the problem of switch failures, whether it is open circuit or short circuit. Hence topologies which can withstand these type of fault scenarios are gaining importance. Therefore, in this paper, a fault-tolerant solution is proposed for a five-level hybrid flying capacitor inverter. This inverter can withstand both open circuit and short circuit faults and additionally, the flying capacitor is always balanced. The inverter is studied for fault in both the legs and a complete fault solution is proposed by addition of a few switches. The DC source and other components such as switches and capacitors requirement for the same number of level generation are also reduced with the proposed topology when compared to existing ones. An advantage of the topology is that it can maintain the same number of levels for flying capacitor leg in case of a fault. The proposed topology is implemented in MATLAB/SIMULINK environment and the results for R-L load is shown for faults in both the legs of the inverter. A fault is created at a particular point of time and pre-fault, fault and post-fault scenarios are studied with the help of simulation results. The results strongly validate the satisfactory operation of the proposed inverter in all three cases.

Index Terms—Fault-tolerant, Flying Capacitor, Multilevel inverter.

I. INTRODUCTION

Modern multilevel inverters (MLIs) have a wide range of applications because of the immense advantages on offer. In applications such as UPS (Uninterrupted Power Supply) and Electric vehicles, reliability is the most important parameter. Hence fault-tolerant inverters have been gaining importance in recent times. IGBTs are the major component that are prone to fault [1]-[2]. As the number of switches in the multilevel inverters is many, the operation of MLI is likely to get affected in case of a fault. Hence research on fault-tolerant inverters is increasing in recent days [3]. The causes for IGBT failures are many which have been reported in [4]. A simple bidirectional switch can be a solution for the fault in most cases [5]-[6], but it is not the only possible solution always. There can be a requirement of a redundant leg in some cases such as [7]-[8]. Hence according to the configuration chosen, the circuit can be modified to operate under fault scenario. In [8] the fault

scenario is addressed with the help of SCR and a bidirectional switch which increases the complexity of the circuit. Hence the proposed fault solution should be addressed in a simpler manner.

According to the equivalent circuit that is chosen under fault cases, a suitable control technique must be adopted. Hence the switching strategy must be modified with respect to equivalent circuit [8]. This is taken as one reason in this paper to address the fault situation. This paper proposes a five-level topology of which one leg is of a normal two-level H-bridge leg and the other leg is of a three-level flying capacitor leg. Hence they are combined for five-level generation. The fault scenario of the proposed topology is studied for both the legs of the inverter. For H-bridge leg, the post-fault operation will be three-level and for the flying capacitor leg, it is five-level itself. Hence a complete fault solution for both the legs is proposed. The proposed topology can withstand both short-circuit and open-circuit faults. Fault in H-bridge leg is cleared by the use of a bidirectional switch whereas for flying capacitor leg, a redundant leg is added to overcome the fault. The detailed operation of the proposed circuit is explained in further sections.

The proposed work is organized as the operation is explained in section II, fault scenario is explained in section III for both the legs of the inverter separately, the simulation results are shown in section IV followed by conclusion and then references.

II. DESCRIPTION AND OPERATION OF PROPOSED TOPOLOGY

Fig. 1 shows the proposed topology where S_1 and S_2 are used for top and bottom levels while the remaining switches S_3 - S_6 are used for different states generation. The switching table is shown in Table I. A level shifted sine PWM technique is implemented for the generation of the five-level output voltage. Capacitor C is maintained at a voltage of $+\frac{V_{dc}}{2}$ with the help of redundant states. $+V_{dc}$ and $-V_{dc}$ levels are generated by giving complementary 50 Hz pulses to switches S_1 and S_2 ,

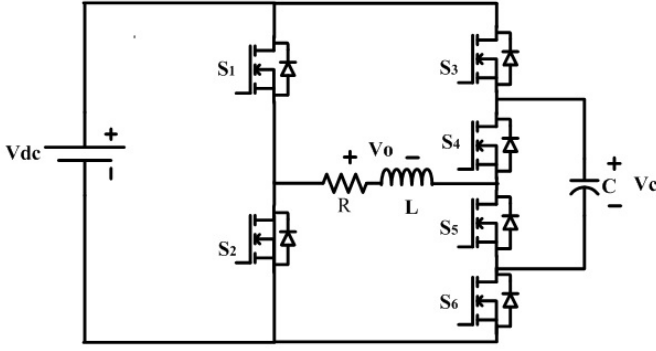


Fig. 1. Proposed Five-Level Inverter

 TABLE I
SWITCHING TABLE FOR FIVE-LEVEL GENERATION

S ₁	S ₂	S ₃	S ₄	S ₅	S ₆	C	V _o
1	0	0	0	1	1	No effect	+V _{dc}
1	0	0	1	0	1	Charging	+ $\frac{V_{dc}}{2}$
1	0	1	0	1	0	Discharging	+ $\frac{V_{dc}}{2}$
0	1	1	0	1	0	Discharging	- $\frac{V_{dc}}{2}$
0	1	0	1	0	1	Charging	- $\frac{V_{dc}}{2}$
0	1	1	1	0	0	No effect	-V _{dc}
0	1	0	0	1	1	No effect	0

whereas $+\frac{V_{dc}}{2}$ and $-\frac{V_{dc}}{2}$ levels are generated with the help of capacitor voltage. There are two redundant states for $+\frac{V_{dc}}{2}$ level as well as for $-\frac{V_{dc}}{2}$ in order to maintain the capacitor at the required level by applying a suitable switching state Table I. The various level generation states of the proposed five-level inverter are shown in Fig. 2. The results in Fig. 4(a) show the operation of the proposed inverter wherein the capacitor voltage is maintained at 50 Volts.

III. FAULT SCENARIO ON FIVE-LEVEL HYBRID FLYING CAPACITOR INVERTER

Fault scenario is studied based on different types of faults. The analysis is done for two legs of the proposed inverter as shown in Figs. 4 and 5. In order to achieve the reliability of the proposed inverter, a suitable switching strategy must be employed with proper combination of the switches. Hence based on the switching combination and equivalent circuit after fault, the number of levels can be maintained at the same level or decreased. Different steps that are to be performed during fault operation are:

1. The switch that is affected by the fault must be isolated with the help of fast acting fuses.
2. If there is a reduced level of operation, the modulation index must be modified to half of its value.
3. According to the new equivalent circuit after fault, the switching strategy also must be changed.

The above fault tolerant procedure is for both open circuit

 TABLE II
SWITCHING TABLE FOR FAULT IN S₁

S ₃	S ₄	S ₅	S ₆	S ₇	C	V _o
1	0	1	0	1	No effect	0
0	0	1	1	1	No effect	+ $\frac{V_{dc}}{2}$
1	1	0	0	1	No effect	- $\frac{V_{dc}}{2}$

 TABLE III
SWITCHING TABLE FOR FAULT IN S₃

S ₁	S ₂	S ₇	S ₈	S ₉	S ₁₀	C	V _o
1	0	0	0	1	1	No effect	+V _{dc}
0	0	1	0	1	1	No effect	+ $\frac{V_{dc}}{2}$
0	1	0	0	1	1	No effect	0
0	0	1	1	0	1	No effect	- $\frac{V_{dc}}{2}$
0	1	0	1	0	1	No effect	-V _{dc}

and short circuit faults. For open circuit fault, only the last two points are to be followed whereas for short circuit faults all the three steps are to be performed. The fault operation is explained for both the legs of inverter separately and the modified circuits are proposed accordingly. The above three steps are to be performed irrespective of the type of fault. For OC fault, only step-2 and step-3 are implemented and for SC faults, all steps are implemented. The fault scenario for the proposed topology is explained below along with the equivalent circuits during post-fault conditions.

A. Fault Scenario on Leg-1 Of the Proposed Inverter

First, the fault study is carried out by creating fault at first leg of switch S₁. The modified circuit for fault operations is shown in Fig. 3(a). For any kind of fault in leg-1 with respect to switches S₁ and S₂, a bidirectional switch S₇ is added for post-fault operations as shown in Fig. 3(a). Considering a fault in S₁, the switching strategy is changed according to Table II to obtain a three-level operation. Here the observation is that the capacitor is not involved in any of the level generation part on account of which the capacitor voltage C₃ is not a major concern. The capacitors C₁ and C₂ are used as a DC link whose voltages will always be balanced. The results in Fig. 4(b) show that capacitor C₃ voltage is always maintained at 50 Volts for an input voltage of 100 Volts. The output voltage of the inverter and load current for R-L load are also shown in Fig. 4(b); they show that a three-level operation is obtained satisfactorily. Only one extra bidirectional switch is added if a fault occurred in leg-1. Hence the cost, as well as the complexity involved, is also low in this case. The other switch of leg-1 S₂ voltage is also shown in Fig. 5(a) which has a voltage stress from V_{dc} to $\frac{V_{dc}}{2}$. This voltage helps in detection of fault in leg-1. Hence the operating switches post-fault in leg-1 are S₃-S₆ and S₇.

B. Fault Scineario on Leg-2 of Proposed Inverter

In order to study fault scenario in second leg of the proposed inverter, switch S₃ is made faulty. In this case, an extra

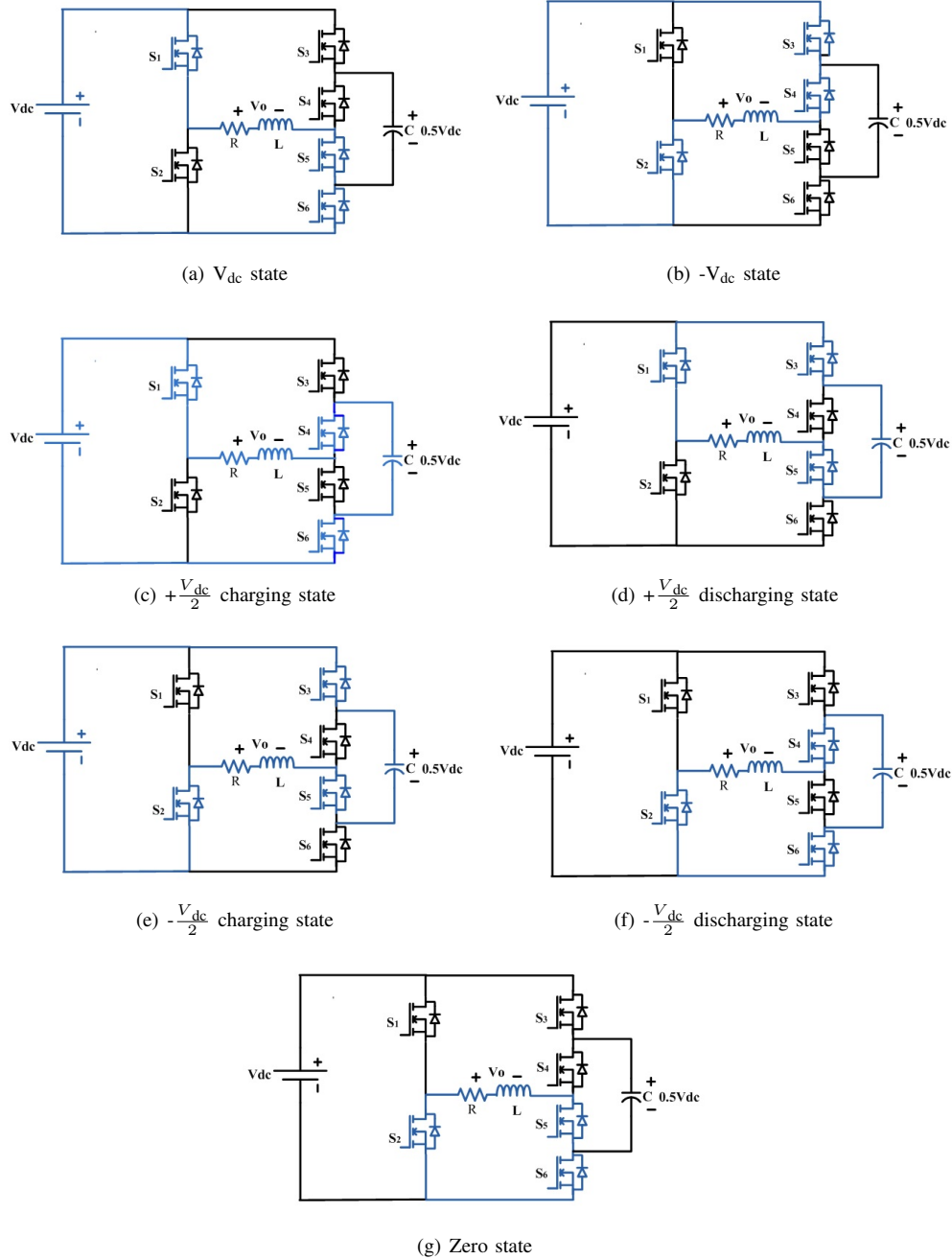


Fig. 2. Different voltage levels of proposed five-level inverter

redundant leg is required for maintaining five-level operation which is made by the switches S_8 - S_{10} . Here continuous operation is maintained by isolating leg-2 during the post-fault scenario. The Capacitor voltage is always maintained at the required level since the leg-2 is isolated during the fault conditions. Different operating switches for level generation are shown in Table III, hence the switching strategy is modified from Table I to Table III for a fault in leg-2 of the proposed inverter. Modulation index value need not be changed in this case because the number of levels is not decreased here. The

result in Fig. 5(b) shows that the operation of the five-level inverter is quite satisfactory and there is no effect in the voltage level of the capacitor, which is maintained at 50 Volts before and after the fault. The output voltage, load current for R-L load are also shown in Fig. 5(b). In order to detect the fault in the flying capacitor leg, the capacitor voltage must be sensed which is beyond the purview of this paper.

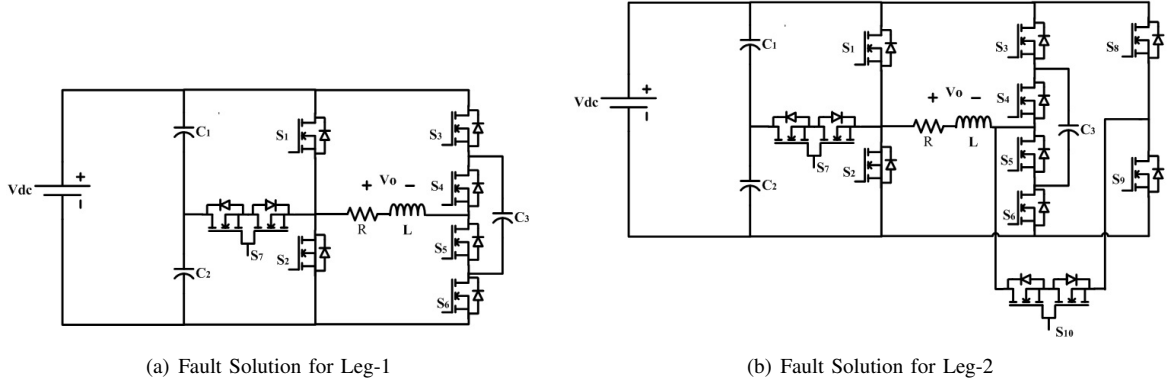
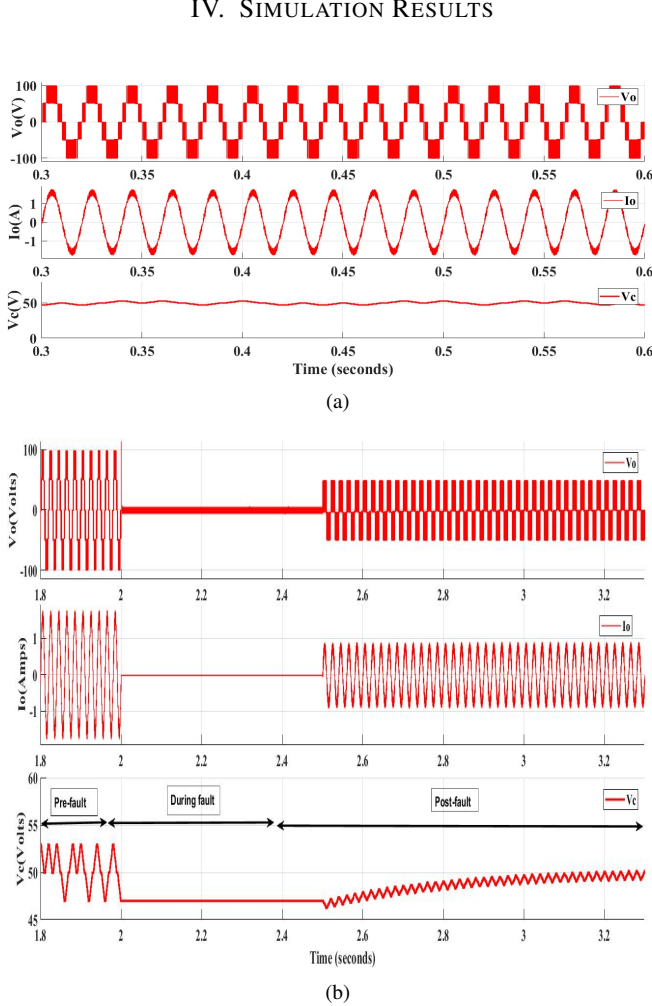
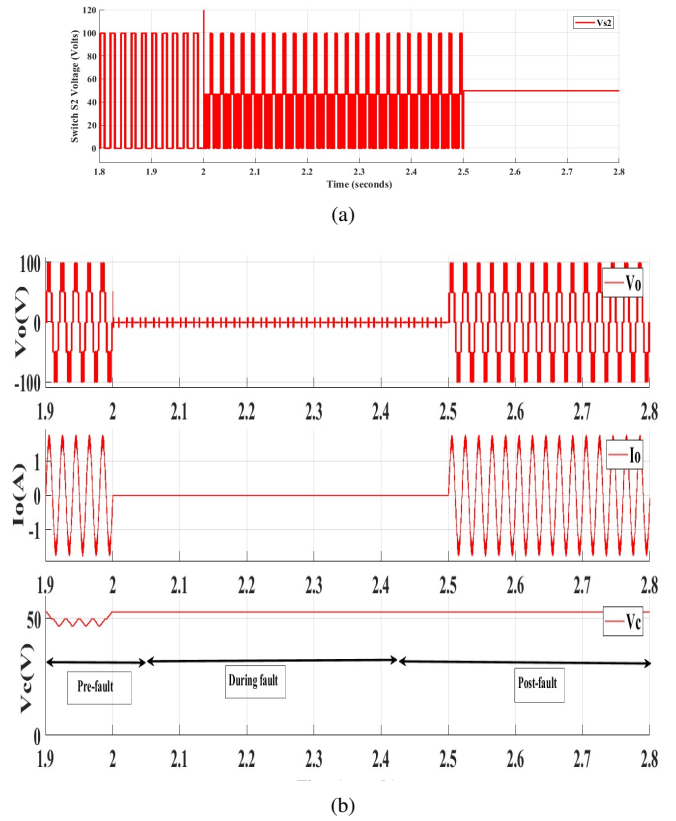


Fig. 3. Proposed post-fault equivalent circuit for both the legs of inverter

IV. SIMULATION RESULTS


 Fig. 4. Output Voltage, Output Current, Capacitor Voltage for (a) Proposed Five-Level Inverter, (b) For fault in Switch S_1

The simulation of the proposed fault-tolerant inverter is carried out in MATLAB/SIMULINK environment for R-L load. The simulation parameters are input voltage V_{dc} of 100 Volts and R-L load with $R=50$ ohms and $L=10$ mH; the


 Fig. 5. (a) Switch S_2 blocking voltage during fault in S_1 (b) Output Voltage, Output Current, Capacitor Voltage for fault in Switch S_3

capacitance C_3 is chosen as 2000 μF and C_1 and C_2 are 1000 μF each. A switching frequency f_s of 3 KHz and modulation index as $M=0.8$ is chosen. From Fig. 4 and 5, it is observed that a fault is created at 2 seconds and cleared at 2.5 seconds in both the cases. Fig. 4(b) is the case for fault in leg-1, post-fault at $t=2.5$ s it is shown that a three-level operation is maintained satisfactorily. Fig. 5(b) gives information about the fault in leg-2 and it is seen that after $t=2.5$ s, five-level operation is maintained and the capacitor voltage is maintained constant

in both the cases. Hence the proposed fault-tolerant topology for the five-level inverter is working fine, which is also verified using MATLAB.

V. CONCLUSIONS

This paper proposes a complete fault-tolerant solution for a single-phase five-level hybrid flying capacitor inverter. The various situations for fault are studied in both the legs of the inverter and the equivalent circuit for both the legs is presented. The simulation model is developed in MATLAB and the results show satisfactory operation of the proposed inverter. An experimental setup is planned for future to validate the simulation results. The proposed configuration can be used for Renewable energy, Electric vehicle and Defence applications where there is requirement of continuous operation.

REFERENCES

- [1] Arun Singh, Anup Anurag, and Sandeep Anand, "Evaluation of Vce at inflection point for monitoring bond wire degradation in discrete packaged IGBTs," *IEEE Trans. Power Electron.*, vol. 32, no. 4, pp. 2481–2484, Apr. 2017.
- [2] Mokhtar Aly, Emad M. Ahmed, and Masahito Shoyama, "Thermal and reliability assessment for wind energy systems with DSTATCOM functionality in resilient microgrids," *IEEE Trans. Sustain. Energy*, vol. 8, no. 3, pp. 953–965, Jul. 2017.
- [3] Mokhtar Aly, Emad M. Ahmed, and Masahito Shoyama, "A New Single-Phase Five-Level Inverter Topology for Single and Multiple Switches Fault Tolerance," in *IEEE Transactions on Power Electronics*, vol. 33, no. 11, pp. 9198–9208, Nov. 2018.
- [4] Ui-Min Choi, Frede Blaabjerg, and Kyo-Beum Lee, "Study and handling methods of power IGBT module failures in power electronic converter systems," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2517–2533, May 2015.
- [5] S. Karimi, P. Poure and S. Saadate, "Fast power switch failure detection for fault tolerant voltage source inverters using FPGA," in *IET Power Electronics*, vol. 2, no. 4, pp. 346–354, July 2009.
- [6] Wenping Zhang, Dehong Xu, Prasad N. Enjeti, Haijin Li, Joshua T. Hawke and Harish S. Krishnamoorthy, "Survey on Fault-Tolerant Techniques for Power Electronic Converters," in *IEEE Transactions on Power Electronics*, vol. 29, no. 12, pp. 6319–6331, Dec. 2014.
- [7] Shiva Prakash Gautam, Lalit Kumar, Shubhrata Gupta and Nitesh Agrawal, "A Single-Phase Five-Level Inverter Topology With Switch Fault-Tolerance Capabilities," in *IEEE Transactions on Industrial Electronics*, vol. 64, no. 3, pp. 2004–2014, March 2017.
- [8] X.Kou, K. A. Corzine, and Y. Familant, "A unique fault-tolerant design for flying capacitor multilevel inverter," *IEEE Trans. Power Electron.*, vol. 19, no. 4, pp. 979–987, Jul. 2004.